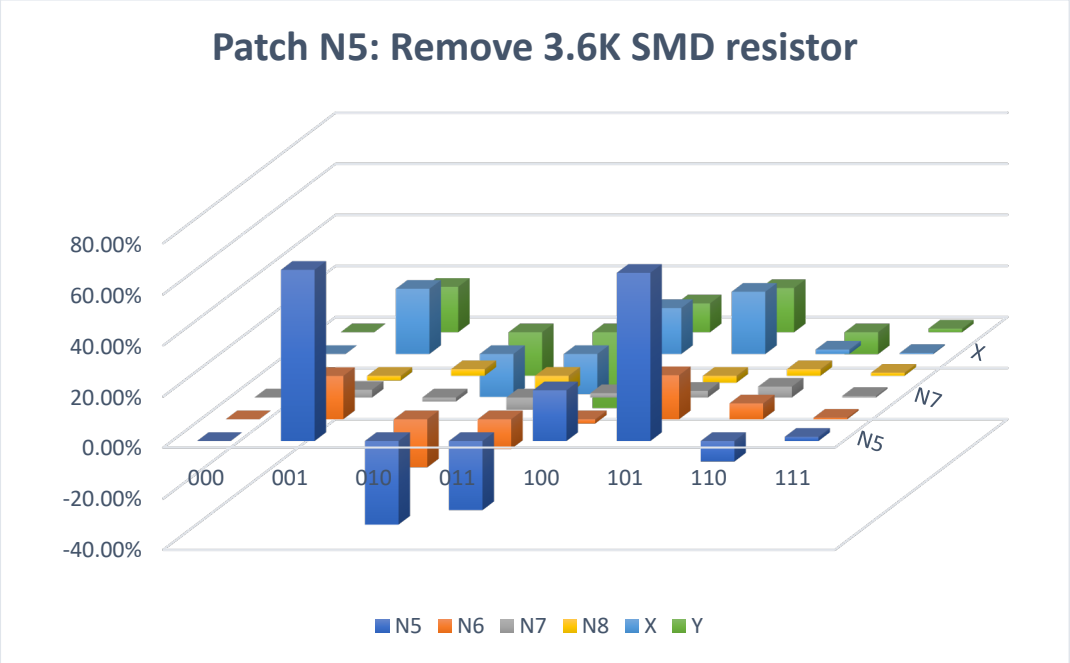
Fault Tolerance Simulation Tests.

Test: Patch N5 remove 3.6K resistor connection

% Voltage change following Simulation Test

	N5	N6	N7	N8	X	Y
000	0.00%	0.00%	0.00%	0.00%	0.00%	0.00%
001	67.02%	16.97%	3.03%	-1.90%	25.54%	17.78%
010	-32.73%	-18.83%	-1.55%	2.59%	-16.78%	-17.02%
011	-27.06%	-11.64%	-4.69%	-7.11%	-15.72%	-29.69%
100	19.86%	-1.69%	1.70%	-8.66%	17.99%	11.30%
101	65.85%	17.25%	2.61%	-2.73%	24.38%	17.32%
110	-8.05%	6.20%	4.26%	2.59%	1.74%	-8.58%
111	1.64%	0.61%	0.60%	1.21%	0.40%	1.43%

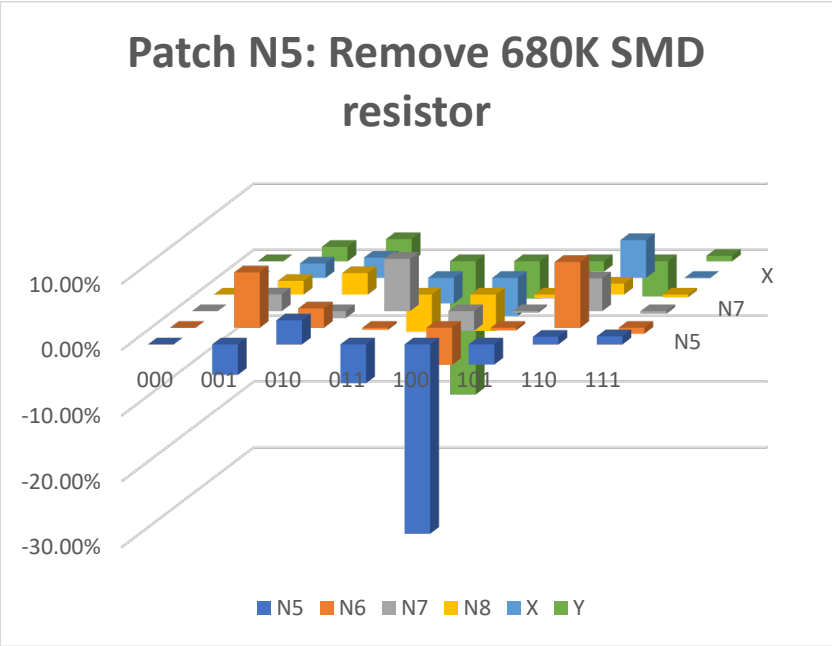


Truth table outputs	Truth table outputs
original	Output removed 3.6K SMD
00	00
00	00
10	10
11	11
00	00
10	11
11	11
11	11

Test: Patch N5 remove 680K resistor connection

% Voltage change following Simulation Test

	N5	N6	N7	N8	X	Y
000	0.00%	0.00%	0.00%	0.00%	0.00%	0.00%
001	-4.61%	8.39%	2.53%	2.06%	2.18%	2.19%
010	3.64%	2.93%	-1.04%	3.24%	3.08%	3.35%
011	-5.88%	-0.30%	7.94%	-5.64%	-3.87%	-20.19%
100	-28.77%	-5.62%	-2.98%	-5.51%	-5.76%	-5.65%
101	-3.05%	-0.39%	-0.24%	-0.55%	-1.99%	-1.57%
110	1.15%	9.97%	4.96%	1.65%	5.72%	-5.34%
111	1.23%	-0.90%	-0.40%	-0.40%	-0.02%	0.82%

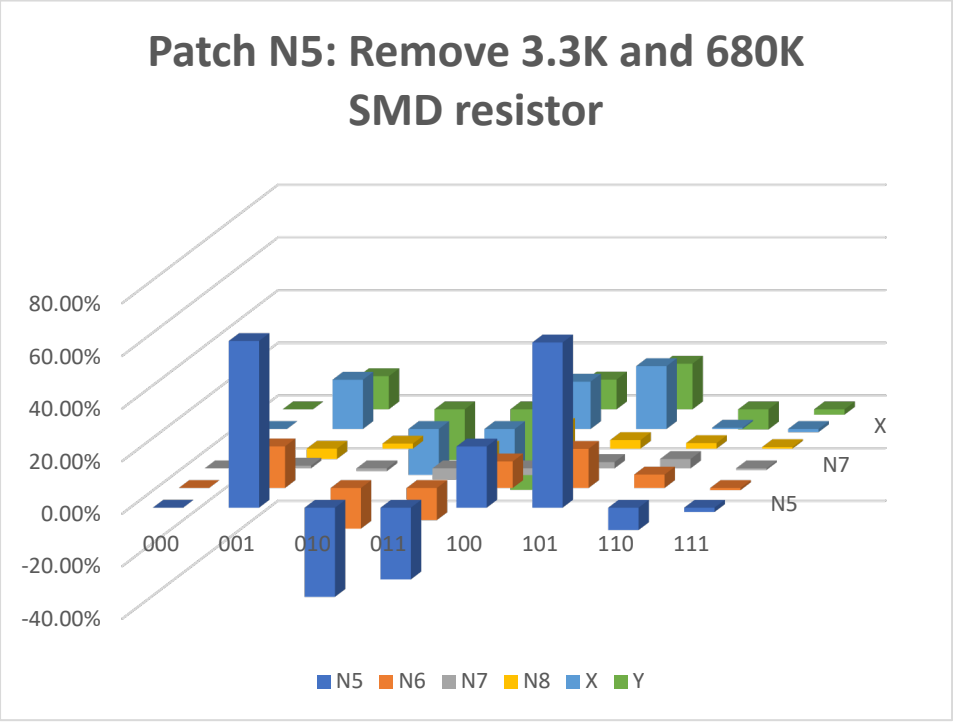


Truth table outputs	
original	Removed 680K SMD
00	00
00	00
10	11
11	11
00	00
10	01
11	11
11	11

Test: Patch N5 remove 3.3K and 680K resistor connection

% Voltage change following Simulation Test

	N5	N6	N7	N8	X	Y
000	0.00%	0.00%	0.00%	0.00%	0.00%	0.00%
001	63.36%	15.83%	1.01%	-3.96%	18.72%	12.59%
010	-33.94%	-15.48%	-1.04%	1.94%	-17.47%	-19.25%
011	-27.29%	-12.24%	-4.33%	-7.60%	-15.72%	-30.66%
100	23.29%	10.11%	-2.55%	8.66%	17.99%	11.30%
101	62.80%	14.90%	2.38%	3.28%	23.88%	17.32%
110	-8.51%	5.12%	3.55%	2.12%	0.50%	-7.66%
111	-1.64%	-0.81%	-0.60%	0.61%	-1.21%	-2.04%

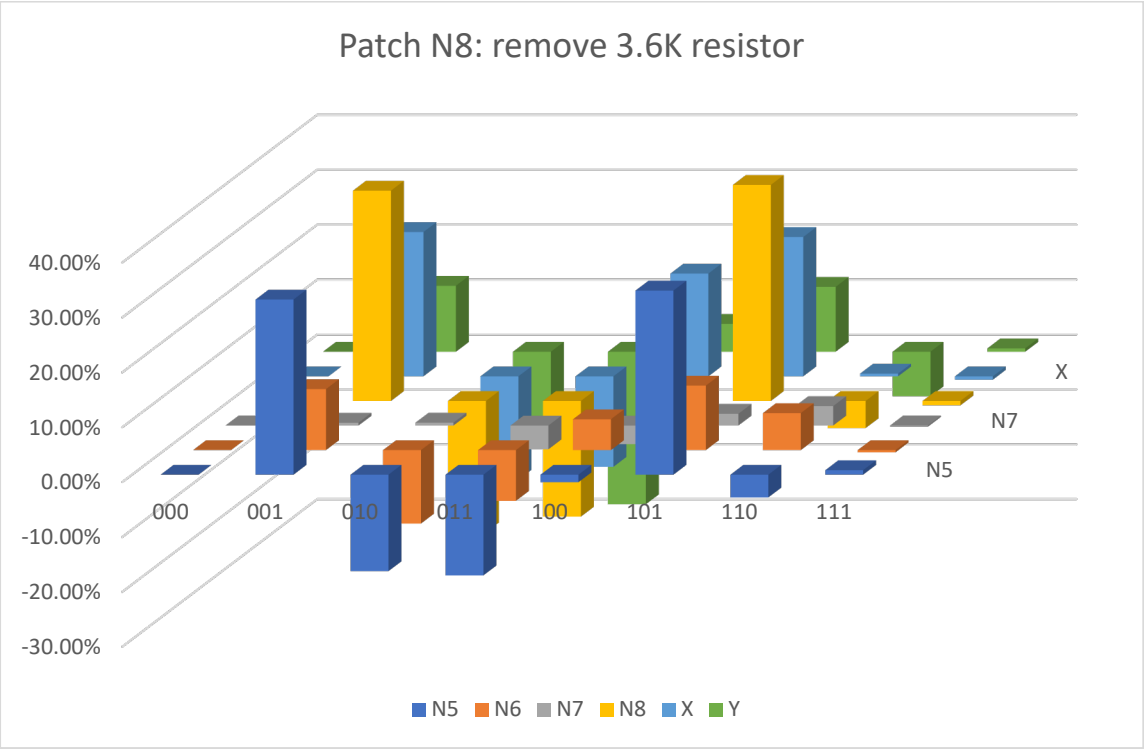


Truth table outputs	
original	removed 3.3K +680K SMD
00	00
00	00
10	10
11	11
00	00
10	11
11	11
11	11

Test: Patch N8 remove 3.6K resistor connection

% Voltage change following Simulation Test

	N5	N6	N7	N8	X	Y
000	0.00%	0.00%	0.00%	0.00%	0.00%	0.00%
001	31.91%	11.12%	0.51%	38.29%	26.27%	12.01%
010	-17.58%	-13.39%	0.52%	-23.95%	-18.84%	-12.97%
011	-18.35%	-9.25%	-4.33%	-21.08%	-16.49%	-27.79%
100	-1.37%	5.62%	-3.40%	0.40%	18.71%	5.08%
101	33.54%	11.76%	2.14%	39.34%	25.37%	11.81%
110	-4.14%	6.74%	3.55%	-4.95%	0.50%	-8.12%
111	0.82%	-0.40%	-0.20%	-0.81%	-0.61%	0.61%

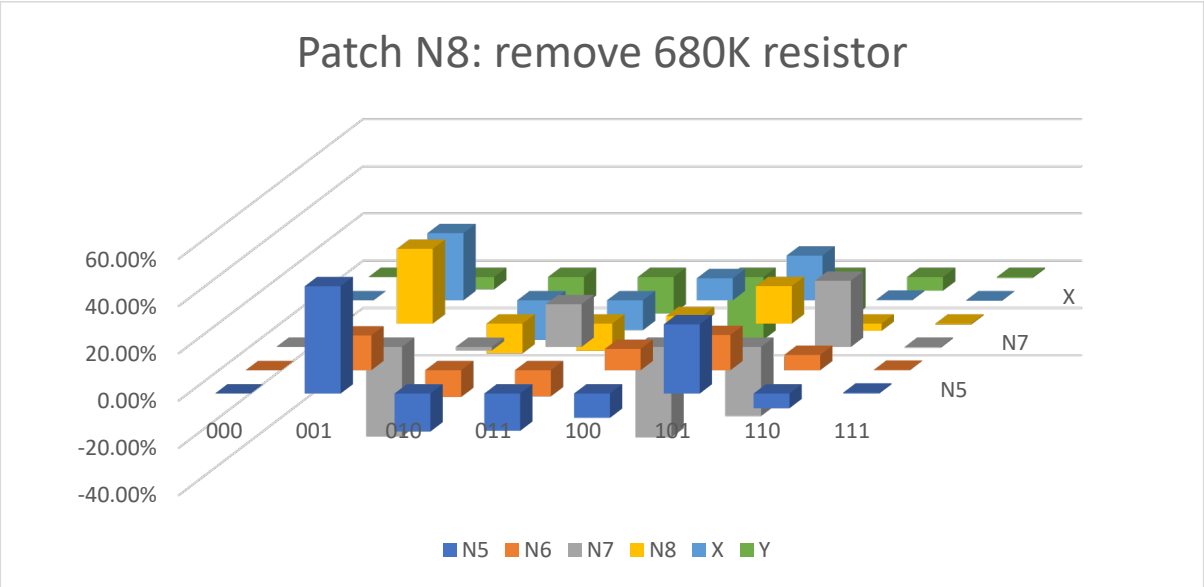


Truth table outputs	
original	removed 3.3K
00	00
00	00
10	00
11	11
00	00
10	11
11	11
11	11

Test: Patch N8 remove 680K resistor connection

% Voltage change following Simulation Test

	N5	N6	N7	N8	X	Y
000	0.00%	0.00%	0.00%	0.00%	0.00%	0.00%
001	45.39%	14.68%	-37.88%	31.65%	28.45%	-5.20%
010	-16.06%	-11.33%	-1.55%	-12.62%	-16.78%	-11.72%
011	-15.76%	-11.04%	18.05%	-11.52%	-12.63%	-15.44%
100	-10.27%	8.99%	-38.30%	3.15%	9.35%	-26.55%
101	29.27%	14.90%	-29.22%	15.85%	18.91%	-16.93%
110	-6.21%	6.47%	28.01%	-3.07%	0.25%	-5.80%
111	0.41%	0.20%	-0.40%	-0.40%	-0.20%	-0.41%

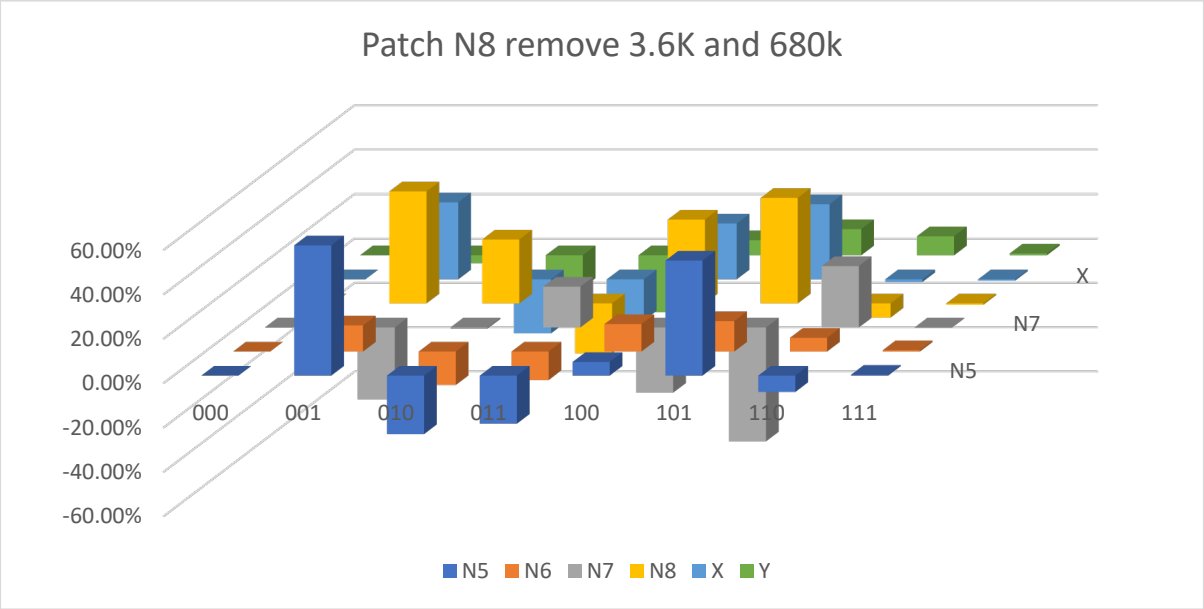


Truth table outputs	
original	removed 680K last row
00	00
00	00
10	10
11	11
00	00
10	00
11	11
11	11

Test: Patch N8 remove 680K resistor connection

% Voltage change following Simulation Test

	N5	N6	N7	N8	X	Y
000	0.00%	0.00%	0.00%	0.00%	0.00%	0.00%
001	58.69%	11.81%	-32.32%	50.47%	34.69%	-3.58%
010	-26.36%	-15.06%	-0.52%	28.80%	-24.32%	-14.64%
011	-21.65%	-12.84%	18.41%	-22.55%	-18.56%	-25.65%
100	6.16%	12.36%	-29.36%	37.80%	25.18%	6.78%
101	51.83%	13.73%	-51.31%	47.54%	33.83%	11.81%
110	-7.36%	6.20%	27.66%	-6.37%	-1.24%	8.58%
111	0.41%	0.61%	-0.20%	-0.61%	-0.61%	0.82%



Truth table outputs	
original	removed 3.6K first row and 680K last row
00	00
00	00
10	00
11	11
00	00
10	11
11	11
11	11