Weekly Plan for the term project: **Single Cycle 16 Bit Pipelined CPU Design Term 141**

Week 1: 23/11/2014 - 29/11/2014:

During the lab:

1. **Introduction to Logisim**
2. Adder/Subtractor Design
3. Logic Unit
4. Shifter
5. Complete ALU
6. **Register File (RF)**

Assignment:

1. Complete ALU
2. Write report about ALU

Week 2: 30/11/2014 - 01/12/2014:

During the lab:

1. Program Counter, Instruction Memory and Data Memory
2. Splitter to separate different fields in the instruction code
3. Connect R Type Instruction Data Path (PC, Memory, RF, ALU)
4. Tests
5. Complete I type instruction data path (from previous lab)
6. **Extender Circuit (zero/sign)**
7. **Next PC Circuit**
8. Test basic R, J and I type instructions without the control signals. This could be done by manually activating the control signals.
9. Complete both control units (AU and MCU) from previous lab.
10. Connect all components and perform tests.
11. Test basic R, J and I type instructions with the control units (ALU and main)

Assignment:

1. Separate the different stages and propose an implementation of the Pipelined Version.
2. Write report about register file, extender, next PC and relative connections and testing R and I type instructions.

Week 3: 02/12/2014 - 09/12/2014:

During the lab:

- Discuss the proposed design and start its implementation.
- Implement the different pipeline registers between the stages, and connect all components:
    - Connect data signals and perform tests,
    - Connect control signals and perform tests.
    - Do not consider Hazards at this level.
- Perform tests of the basic R, J and I type instructions with the pipeline registers inserted between stages.

Assignment:

- **Hazards**
- Report about the Single Cycle CPU should be ready by next week

Week 4: 10/12/2014 - 17/12/2014:

During the lab:

- Design control logic to detect data dependencies among instructions
- Implement the forwarding logic
- Implement the necessary logic for jump instructions:
    - Jump delay is set to one cycle.
    - After an unconditional jump instruction the pipeline is stalled for one clock cycle
    - Assume a branch is never taken and the pipeline is not stalled in this case.
    - In case the branch is taken, the wrongly fetched instructions are converted into bubbles.
- The pipeline is stalled after a load LW instruction that is followed by a dependent instruction.
- Test sequences of dependent instructions to ensure the correctness of the forwarding logic.
- Test the LW instruction followed by a dependent instruction to ensure stalling the pipeline correctly by one clock cycle.
- Test the behavior of taken and untaken branch instructions and their effect on stalling the pipeline.

Assignment:

- Propose and write a program that takes into considerations all hazard situations. Prepare final tests and final report.

Week 5: 18/12/2014 - 24/12/2014:

- Final Tests and submission: Each group has to submit their work and make a demo to the instructor. Each student in a group is asked independently and may get a different grade.
- Submit the final report.

Guidelines on writing the final report:

Consider the following points when writing your report:

1. Writing Style, Spelling and Grammar: The report should contain an introduction, body and conclusion. Optionally some appendixes may be added. Improve your writing style using simple statements, and avoid spelling mistakes.

2. Design Description and Drawings: Figures should be explicit on a single page if needed and labelled.

3. Test cases, verifying correct execution: provide details of your test cases and mention their outcomes, results and in case of errors try to point those errors and explain their cause, source and origin, and how to avoid them if possible

4. Describing group work, meetings, and contributions of each group member: use a Gantt chart or a table with details of the work of each group member.