RTL8761B Series
(RTL8761BUV-CG/RTL8761BTV-CG)

BLUETOOTH 5 CONTROLLER

PRELIMINARY DATASHEET
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USING THIS DOCUMENT

This document is intended for the software engineer's reference and provides detailed programming information.

Though every effort has been made to ensure that this document is current and accurate, more information may have become available subsequent to the production of this guide.

ELECTROSTATIC DISCHARGE (ESD) WARNING

This product can be damaged by Electrostatic Discharge (ESD). When handling, care must be taken. Damage due to inappropriate handling is not covered by warranty.

Do not open the protective conductive packaging until you have read the following, and are at an approved anti-static workstation.

- Use an approved anti-static mat to cover your work surface

- Use a conductive wrist strap attached to a good earth ground

- Always discharge yourself by touching a grounded bare metal surface or approved anti-static mat before picking up an ESD-sensitive electronic component

- If working on a prototyping board, use a soldering iron or station that is marked as ESD-safe

- Always disconnect the microcontroller from the prototyping board when it is being worked on

REVISION HISTORY

Revision	Release Date	Summary
0.7	2019/05/06	First release.
0.8	2019/06/12	Modify USB description.
0.9	2019/06/25	Modify internal LDO output voltage.
1.0	2019/0719	Modify internal LDO output voltage tolerance.
1.1	2019/10/30	Add information about PCM.
1.2	2019/11/04	Modify Storage Temperature.
1.3	2019/11/13	Modify and add some feature descriptions.

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1. General Description

The Realtek RTL8761B is a highly integrated single-chip Bluetooth 5 controller with a UART (RTL8761BTV)/ USB (RTL8761BUV) interface. It combines a BT Protocol Stack (LM, LL, L2CAP, GATT, RFCOMM, SPP, and LE), BT Baseband, modem, and BT RF in a single chip.

The RTL8761B Bluetooth controller complies with Bluetooth core specification v5 and supports dual mode (BR/EDR + Low Energy Controllers). It is compatible with previous versions, including v2.1 + LE. For BR/EDR, it allows multiple active links in either slave mode or master mode. For Low Energy, it supports multiple states and allows multiple active links in slave mode. A BR/EDR link and an LE link can be active at the same time.

2.   Features

General Features

- Bluetooth 5 specification compliant

- Single-end RF radio output with high performance 10dBm of BR transmitter power and -94.5dBm 2M EDR receiver sensitivity.

- Supports Bluetooth classic (BDR/EDR)

- Supports Bluetooth Low Energy (BLE)

Host Interface

- RTL8761BTV Complies with HS-UART with configurable baud rate for Bluetooth

- RTL8761BUV Complies with USB1.1 full speed mode.

Bluetooth Controller

- Compatible with Bluetooth v2.1Systems

- HS-UART interface for Bluetooth data transmission compliant H5 specification

- Integrated MCU to execute Bluetooth protocol stack

- Supports all packet types in basic rate and enhanced data rate

- Supports Secure Simple Pairing

- Enhanced BT/Wi-Fi Coexistence Control to improve transmission quality in different profiles

- Supports multiple Low Energy states

Bluetooth Transceiver

- Fast AGC control to improve receiving dynamic range

- Supports Power Control

- Bluetooth Low Energy Support

- Integrated 32K oscillator for power management

Peripheral Interfaces

- Configurable LED pin

- PCM

- GPIO

Clock system

- Build-in 32K oscillator

- 40MHz main clock

RF

- Chipset typical default TX output power is +4.5dBm for all data rate

- Supports TX +10dBm maximum output power for Bluetooth BR/BLE

- Supports TX +7.5dBm maximum output power for Bluetooth EDR

- Receive sensitivity: -94 dBm (2Mbps EDR Minimum)

- Receive sensitivity: -98 dBm (BLE Minimum)

- Receiver sensitivity: -106 dBm (125K BLE long range Minimum)

Operating Condition

- Operating voltage: 2.97V to 3.63V

- Temperature range: 0 ℃ to +70 ℃
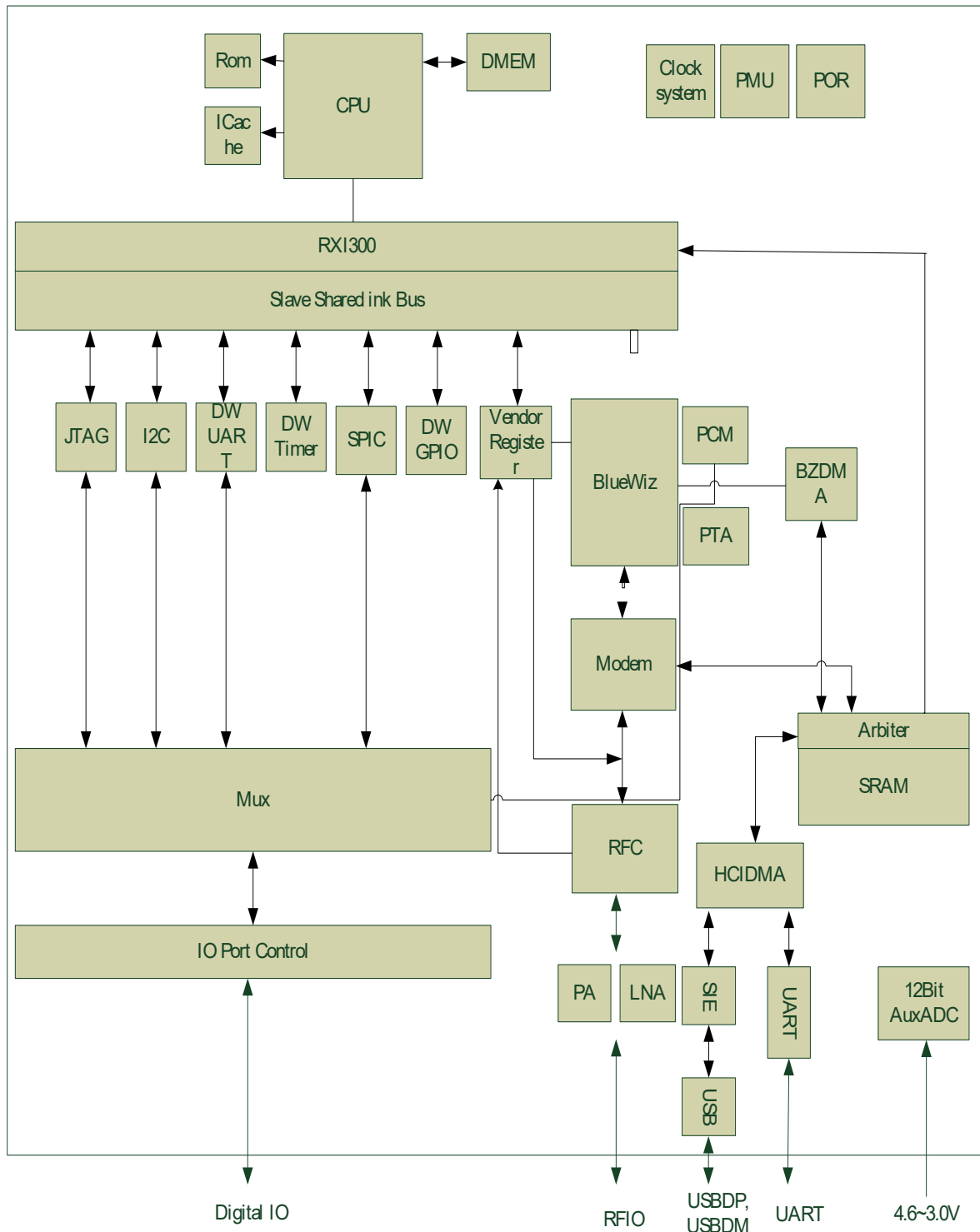
3. Block Diagram

Figure 1. Block Diagram

4. Pin Assignments

4.1. *Package Identification*

Green package is indicated by the 'G' in GXXXXV. The version is shown in the location marked 'V'.

Figure 2.   Package Identification

4.2. *Pin Out (TOP VIEW) --RTL8761BTV*

Figure 3.   RTL8761BTV Pin Assignments

Table 1. Signal Description of RTL8761BTV

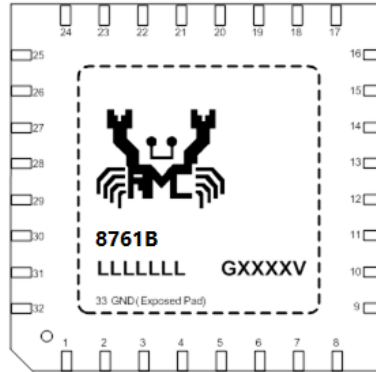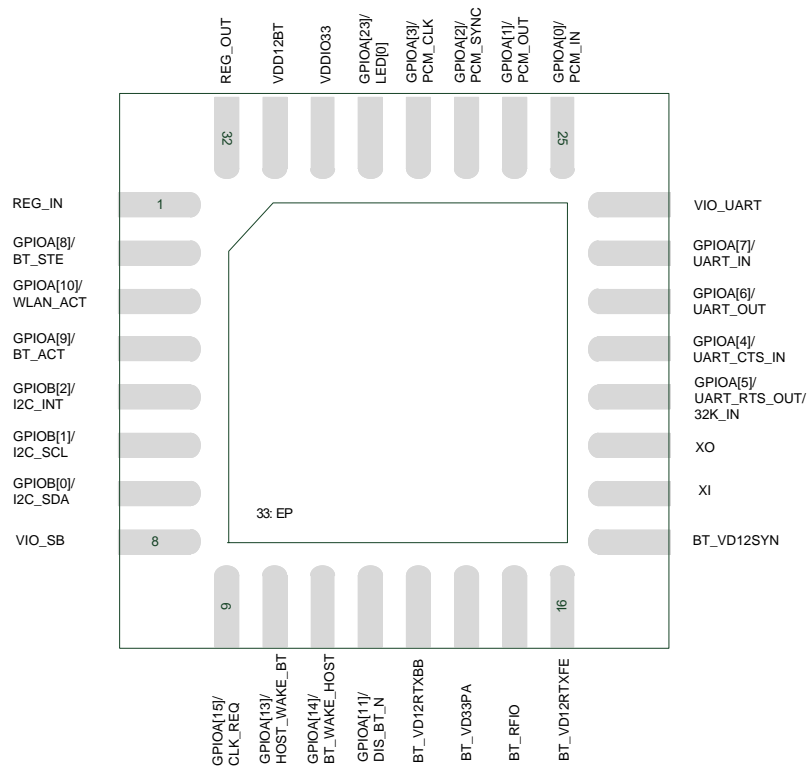| Pin Name	No.	Type	Power Domain	Description
REG_IN	1	Power	-	Internal LDO input
GPIOA[8]	2	Digital I/O	VDDIO33	BT_STE
GPIOA[10]	3	Digital I/O	VDDIO33	WLAN_ACT
GPIOA[9]	4	Digital I/O	VDDIO33	BT_ACT
GPIOB[2]	5	Digital I/O	VDDIO33	GPIO signal/RT_INT
GPIOB[1]	6	Digital I/O	VDDIO33	GPIO signal/RT SCL
GPIOB[0]	7	Digital I/O	VDDIO33	GPIO signal/RT_SDA
VIO_SB	8	Power	-	3.3/1.8V IO power input
GPIOA[15]	9	Digital I/O	VIO_SB	CLK_REQ
GPIOA[13]	10	Digital I/O	VIO_SB	HOST_WAKE_BT
GPIOA[14]	11	Digital I/O	VIO_SB	BT_WAKE_HOST
GPIOA[11]	12	Digital I/O	VIO_SB	DIS_BT_N, bt function disable
BT_VD12RTXBB	13	Power	-	1.26V input, typically connect to output of internal DC-DC
BT_VD33PA	14	Power	-	3.3V power input
BT_RFIO	15	Analog I/O	-	RFIO
BT_VD12RTXFE	16	Power	-	1.26V input, typically connect to output of internal DC-DC
BT_VD12SYN	17	Power	-	1.26V input, typically connect to output of internal DC-DC
XI	18	Analog I/O	-	Crystal Pin
XO	19	Analog I/O	-	Crystal Pin
GPIOA[5]	20	Digital I/O	VIO_UART	UART_RTS/32K_IN
GPIOA[4]	21	Digital I/O	VIO_UART	UART_CTS
GPIOA[6]	22	Digital I/O	VIO_UART	UART_OUT
GPIOA[7]	23	Digital I/O	VIO_UART	UART_IN
VIO_UART	24	Power	-	3.3V/1.8V IO power
GPIOA[0]	25	Digital I/O	VIO_UART	PCM_IN
GPIOA[1]	26	Digital I/O	VIO_UART	PCM_OUT
GPIOA[2]	27	Digital I/O	VIO_UART	PCM_SYNC
GPIOA[3]	28	Digital I/O	VIO_UART	PCM_CLOCK
GPIOA[23]	29	Digital I/O	VDDIO33	LED/system log
VDDIO33	30	Power	-	3.3V power input
VDD12BT	31	Power	-	1.26V input, typically connect to output of internal DC-DC
REG_OUT	32	Power	-	Internal LDO output

4.2.1. Power-On Trap Pins

Table 2. Power-On Trap Pins of RTL8761BTV

Symbol	Pin No	Power Domain	Description
ICFG(0)	25	VIO_UART	Test mode number io0
ICFG(1)	26	VIO_UART	Test mode number io1

Symbol	Pin No	Power Domain	Description
ICFG(2)	27	VIO_UART	Test mode number io2
ICFG(3)	28	VIO_UART	Test mode number io3
SPS_LDO_SEL	4	VDDIO33	LDO mode selection
TEST_MODE_SEL	2	VDDIO33	Test mode selection. Keep low when 3.3V power attach
EEPROM_SEL	11	VIO_SB	Keep low when 3.3V power attached

4.3. *Pin Out (TOP VIEW) --RTL8761BUV*
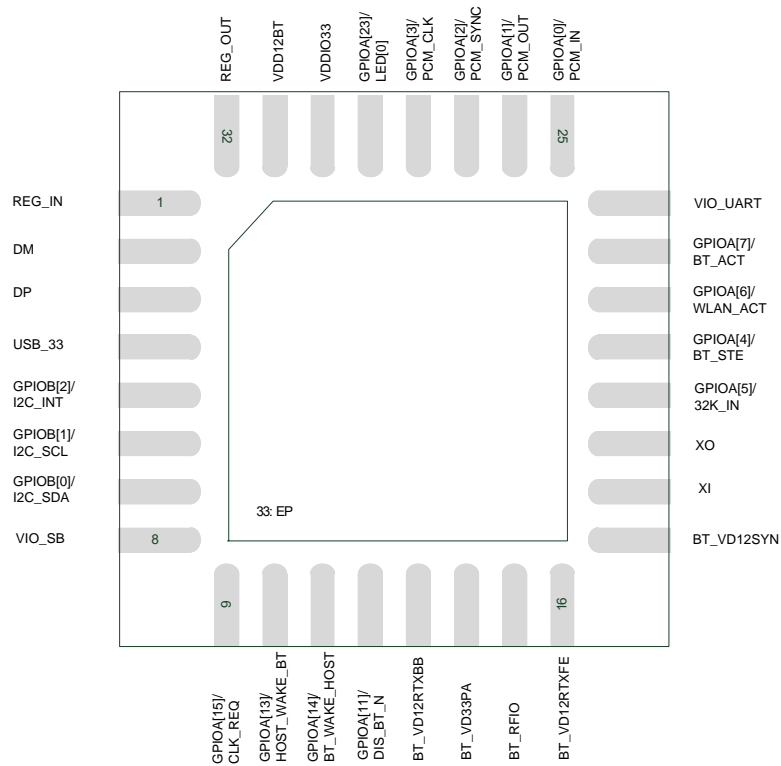
Figure 4.   RTL8761BUV Pin Assignments

Table 3.   Signal Description of RTL8761BUV

Pin Name	No	Type	Power Domain	Description
REG_IN	1	Power	-	Internal LDO input
DM	2	Analog I/O	-	USB DM, connect to host USB DP
DP	3	Analog I/O	-	USB DP, connect to host USB DP
USB_33	4	Power	-	USB 3.3V input
GPIOB[2]	5	Digital I/O	VDDIO33	GPIO signal/RT_INT
GPIOB[1]	6	Digital I/O	VDDIO33	GPIO signal/RT_SCL
GPIOB[0]	7	Digital I/O	VDDIO33	GPIO signal/RT_SDA
VIO_SB	8	Power	-	3.3/1.8V IO power input

Pin Name	No	Type	Power Domain	Description
GPIOA[15]	9	Digital I/O	VIO_SB	CLK_REQ
GPIOA[13]	10	Digital I/O	VIO_SB	HOST_WAKE_BT
GPIOA[14]	11	Digital I/O	VIO_SB	BT_WAKE_HOST
GPIOA[11]	12	Digital I/O	VIO_SB	DIS_BT_N, bt function disable
BT_VD12RTXBB	13	Power	-	1.26V input, typically connect to output of internal DC-DC
BT_VD33PA	14	Power	-	3.3V power input
BT_RFIO	15	Analog I/O	-	RF IO
BT_VD12RTXFE	16	Power	-	1.26V input, typically connect to output of internal DC-DC
BT_VD12SYN	17	Power	-	1.26V input, typically connect to output of internal DC-DC
XI	18	Analog I/O	-	crystal pin
XO	19	Analog I/O	-	crystal pin
GPIOA[5]	20	Digital I/O	VIO_UART	32K_IN
GPIOA[4]	21	Digital I/O	VIO_UART	BT_STE
GPIOA[6]	22	Digital I/O	VIO_UART	WLAN_ACT
GPIOA[7]	23	Digital I/O	VIO_UART	BT_ACT
VIO_UART	24	Power	-	3.3V/1.8V IO power input
GPIOA[0]	25	Digital I/O	VIO_UART	PCM_IN
GPIOA[1]	26	Digital I/O	VIO_UART	PCM_OUT
GPIOA[2]	27	Digital I/O	VIO_UART	PCM_SYNC
GPIOA[3]	28	Digital I/O	VIO_UART	PCM_CLOCK
GPIOA[23]	29	Digital I/O	VDDIO33	LED/system log
VDDIO33	30	Power	-	3.3V power input
VDD12BT	31	Power	-	1.26V input, typically connect to output of internal DC-DC
REG_OUT	32	Power	-	Internal LDO output

4.3.1. Power-On Trap Pins

Table 4.   Power-On Trap Pins of RTL8761BUV

| Symbol	Pin No	Power Domain	Description
ICFG(0)	25	VIO_UART	Test mode number io0
ICFG(1)	26	VIO_UART	Test mode number io1
ICFG(2)	27	VIO_UART	Test mode number io2
ICFG(3)	28	VIO_UART	Test mode number io3
SPS_LDO_SEL	23	VIO_UART	LDO mode selection
TEST_MODE_SEL	21	VIO_UART	Test mode selection. Keep low when 3.3V power attach
EEPROM_SEL	11	VIO_SB	Keep low when 3.3V power attach

5. Power Architectonics

8761B circuit is separate into always-on, partial on, partial off power domain. Except always-on domain, each power domain can be turn off when system go into different power state.

5.1. Regulation architecture
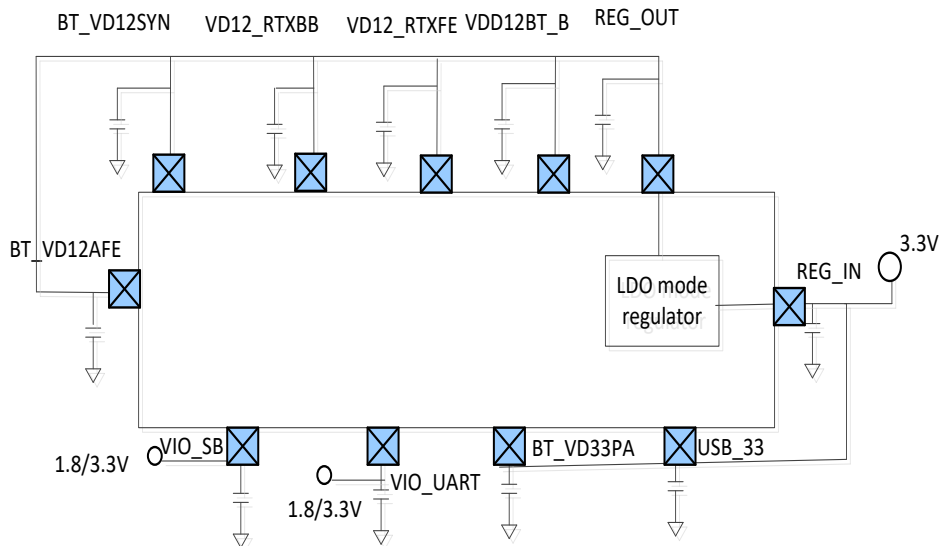
Figure 5. Regulators Architectonics of RTL8761B series

5.2. *USB Power On Sequence*
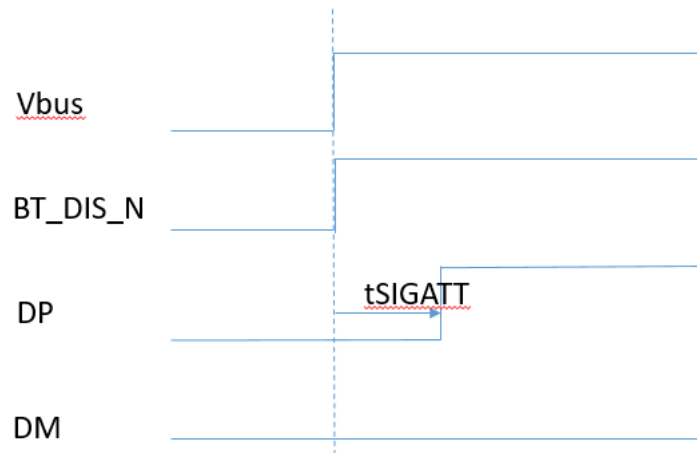
Figure 6.   Chip USB Power Sequence

Table 5.   USB Interface USB Attach Timing

Parameter	Symbol	Min	Typical	Max
Timing between VBUS valid to USB device attach (ms)	t_{SIGATT}	3	6.68	20

6. Pin Function Description
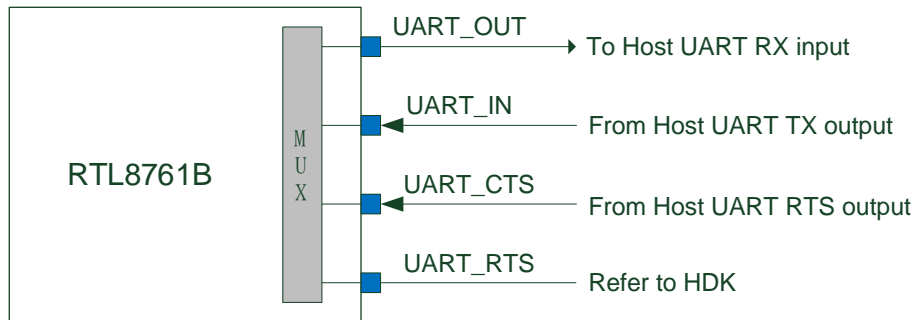
6.1. UART Interface

Figure 7.   UART Interface

6.2. BT Wi-Fi Co-Existence (PTA)

The RTL8761B series support a BT/Wi-Fi co-existence scheme, PTA (Packet Traffic Arbiter)

PTA is a handshake algorithm between Wi-Fi and Bluetooth in a Wi-Fi and Bluetooth co-existence system.
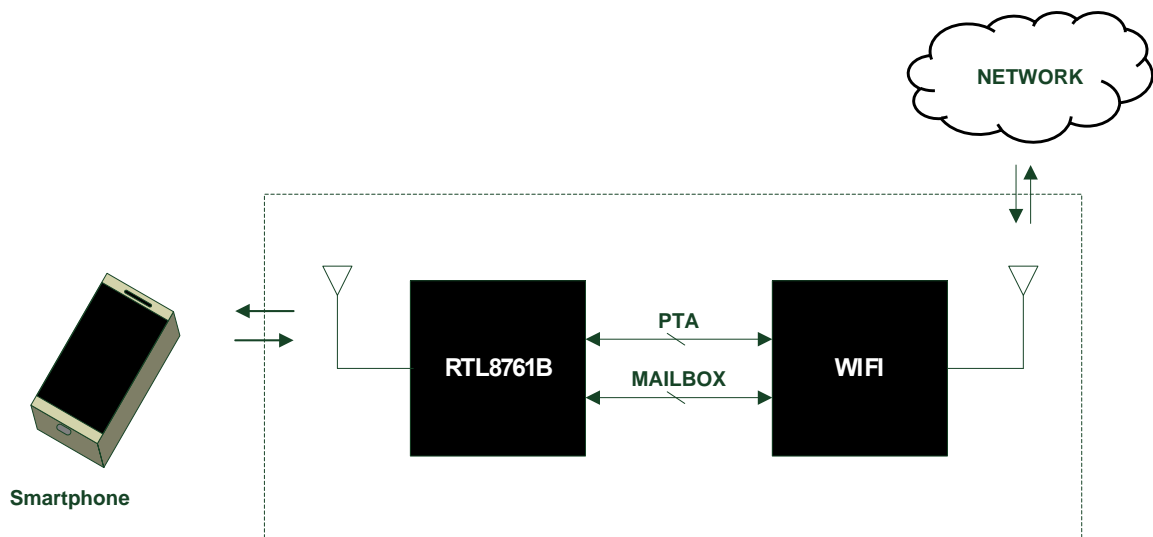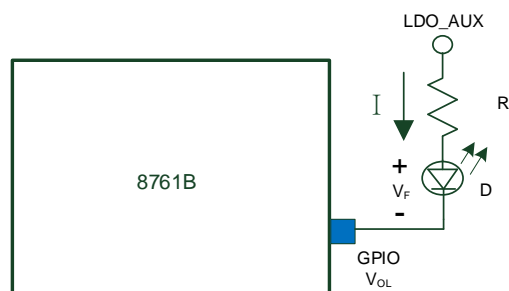

Figure 8.   BT Wi-Fi Co-Existence (PTA)

6.3. *LED*

The RTL8761B series support GPIO assignment to drive the LED for status indication.

Table 6.   LED Specification Suggestions

Parameter	Min.	Typ.	Max.	Unit
Driving capacity	-	-	12	mA
GPIO V_{OH}	1.8	-	3.6	V
GPIO V_{OL}	-	0.2	-	-

Figure 9.   LED Sample Circuit

6.4. *PCM Interface Characteristics*

The RTL8761B supports a PCM digital audio interface that is used for transmitting digital audio/voice data to/from the Audio Codec. Features are supported as below:

- Supports Master and Slave mode
- Programmable long/short Frame Sync
- Supports 8-bit/16-bit linear PCM formats
- PCM Master Clock Output: 64, 128, 256, or 512kHz
- Supports SCO/ESCO link

7. Electrical and Thermal Characteristics

7.1. Temperature Limit Ratings

Table 7.   Temperature Limit Ratings

Parameter	Minimum	Maximum	Units
Ambient Operating Temperature	0	70	°C

7.2. Power Supply DC Characteristics

Table 8.   Power Supply DC Characteristics

| Symbol	Parameter	Minimum	Typical	Maximum	Units
REG_IN, USB33, VDDIO33	3.3V Supply Voltage	3.0	3.3	3.63	V
BT_VDD33PA	RF PA Supply Voltage	3.0	3.3	3.63	V
VDD12BT,	1.26V Supply Voltage	1.23	1.26	1.29	V
BT_VD12SYN	Synthesizer control	1.23	1.26	1.29	V
BT_VD12RTXBB, BT_VD12RTXFE	RF transceiver control	1.23	1.26	1.29	V
VDDIO_SB	IO Supply Voltage	1.8	3.3	3.63	V

7.3. Power Management Unit: Switch Mode Regulator for Digital Core, RF

Table 9.   Switch Mode Regulator

Item	Min.	Typ.	Max.	Unit
Input voltage	2.97	3.3	3.63	V
Output voltage	-	1.26	-	V
Inductor inductance	-	2.2	-	µH
Inductor specification, saturation current	-	500	-	mA
Inductor specification, DCR	-	0.1	0.6	Ω
Input capacitor	-	10	-	µF
Output capacitor	-	4.7	-	µF

8. RF Characteristics

8.1. RF Radio
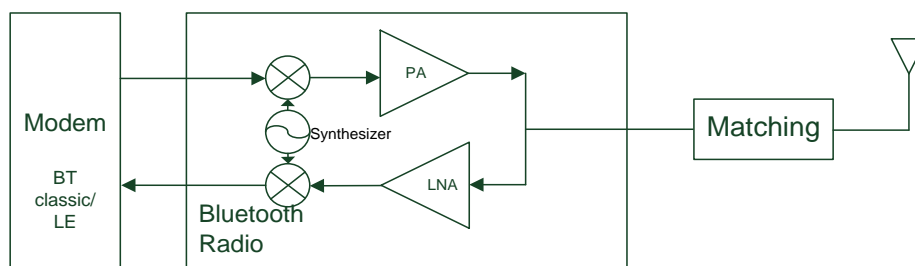
Figure 10. RF Radio Block Diagram

Transceiver

This is a fully integrated all parts of radio transceiver and compliant with Bluetooth SIG test specification. It is designed for low power consumption and excellent transmit and receive performance in the ISM band.

Transmit Part

Transmit mixer: The transmit mixer translates the baseband input signal to form the RF signal. It is designed to provide good stability and modulation characteristics.

Power Amplifier: The power amplifier integrated in the chip can provide up to +3 dBm in the ISM band.

Receive Part

Low Noise Amplifier: Amplifies the low energy RF signal to the desired level without significantly increasing the noise power. It is designed to maintain with good linearity in high input power environments.

Receive mixer: The Receiver mixer receives an input RF signal and outputs an IF signal. The IF signal is then passed along the IF path to the demodulator.

Synthesizer: This is a control loop that compares the crystal and VCO between their phases. If the VCO frequency shifts, then the phase difference produces an error signal for the control loop.

8.2. *Reference RFIO Circuit*

Reference RFIO circuit: please refer to Realtek 8761B series HDK

The RFIO recommended circuits are composed of the pi-matching (1.2pF – 2.7nH – 1.2pF) and an AC-coupled capacitor (22pF).
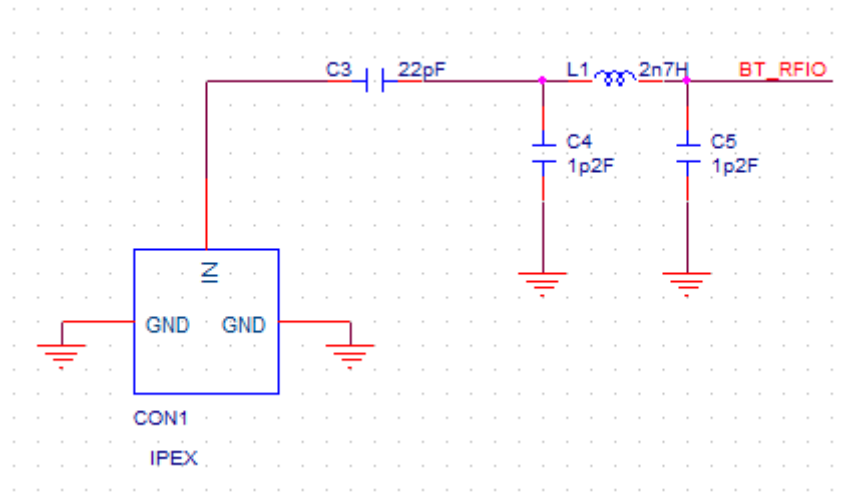
Figure 11. Reference RFIO Circuit

9. ESD Protection and Latch up

The table below shows the ESD and Latch-up capability of RTL8761B.

The ESD protection scheme should be applied during manufacture procedure to avoid unconditional ESD damage.

Table 10. ESD & Latch-up Protection

Parameter	Condition	Min.	Typ.	Max.
Human Body Mode	All pins, test method: JESD22	-	±3.5kV (all pins)	-
Machine Mode	All pins, test method: JESD22	-	±100V	-
Charged Device Model	All pins, test method: JESD22	-	±500V (all pins)	-
Latch up	All pins, test method: JESD78E		±100mA (all pins)	-
Latch up	All pins, test method: JESD78E		1.5 x VDD (all pins)	

10. Storage Condition

Table 11. Storage Condition

	MIN.	TYP.	MAX.
Storage Temperature	-55°C	22°C	125°C
Storage Humidity	40%	50%	60%

11. Mechanical Dimensions

11.1. MQFN32_4x4
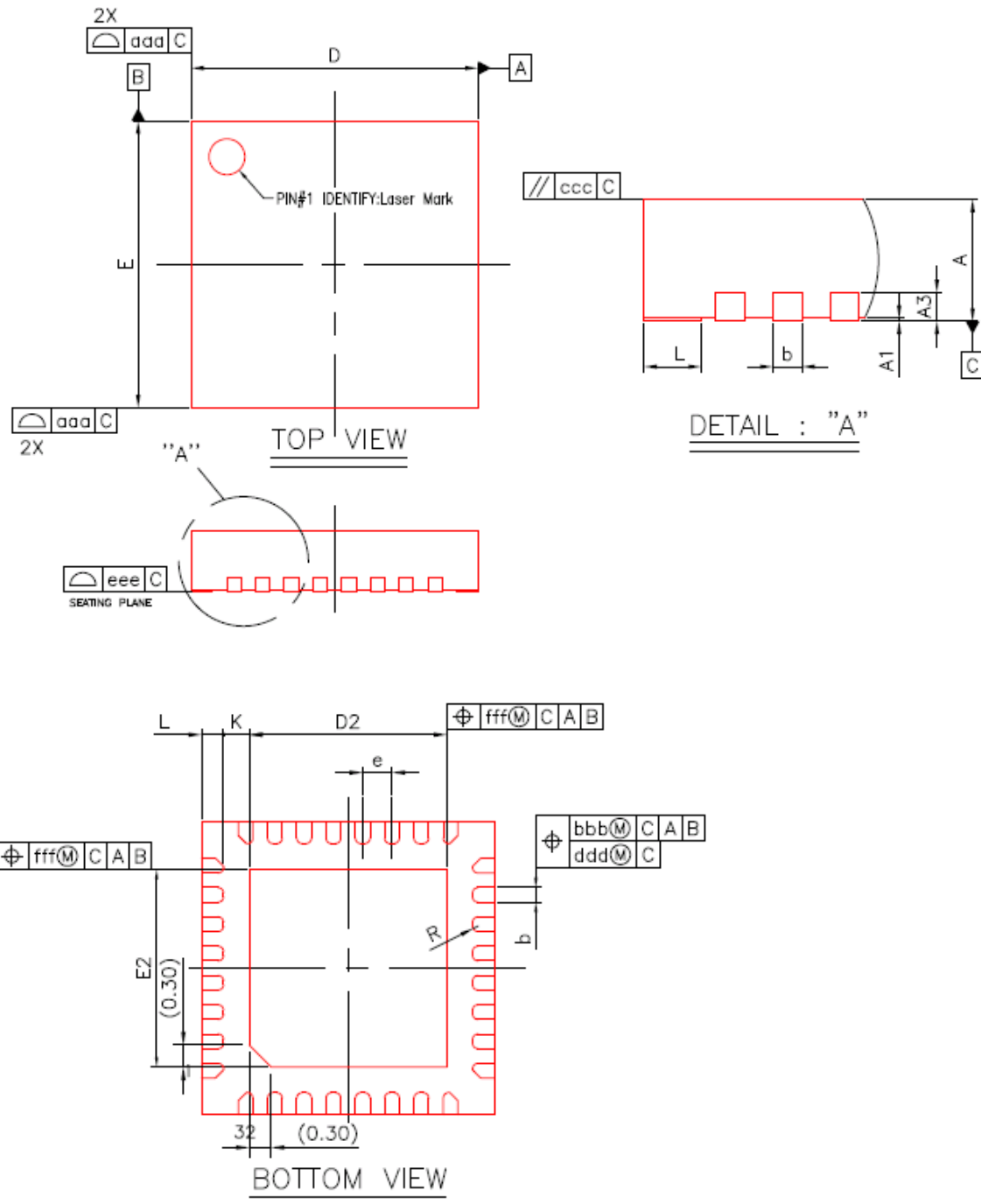
Table 12. QFN32_4x4 Dimension Note.

Symbol	Dimension in nm			Dimension in inch		
	MIN	**MON**	**MAX**	**MIN**	**MON**	**MAX**
A	0.80	0.85	0.90	0.031	0.033	0.035
A1	0.00	0.02	0.05	0.000	0.001	0.002
A3	0.20 REF			0.008 REF		
b	0.15	0.20	0.25	0.006	0.008	0.010
D/E	3.90	4.00	4.10	0.154	0.157	0.161
D2/E2	2.60	2.70	2.80	0.102	0.106	0.110
e	0.40 BSC			0.16 BSC		
L	0.20	0.30	0.40	0.008	0.012	0.016
K	0.20	---	---	0.008	---	---
R	0.075	---		0.003	---	0.005
aaa	0.10			0.004		
bbb	0.07			0.003		
ccc	0.10			0.004		
ddd	0.05			0.002		
eee	0.08			0.003		
fff	0.10			0.004		

12. Ordering Information

Table 13. Order Information

Part Number	Package/Features	Status
RTL8761BTV-CG	QFN32, 4x4mm Outline, "Green Package". UART, PTA, mailbox, PCM	ES
RTL8761BUV-CG	QFN32, 4x4mm Outline, "Green Package". USB, PTA, mailbox, PCM	ES