

$I_{max}$

- (i) Emitter: Highly  
 (ii) collector: moderately } doped  
 (iii) base: lightly

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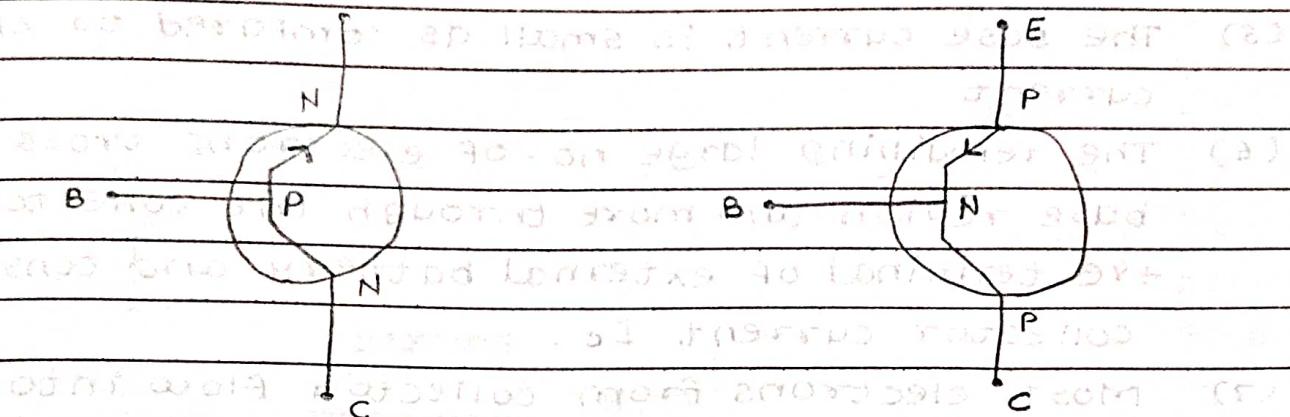
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Arrow from P  $\rightarrow$  N

## UNIT - 2

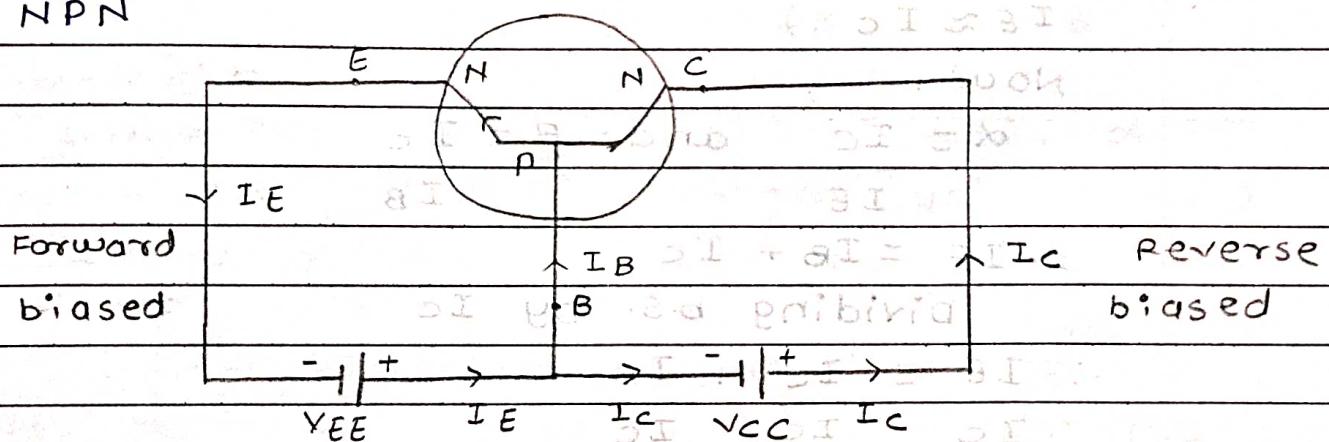
Emitter = Forward biased

\* NPN: Doped  $E$  &  $B$  \* PNP: Doped  $C$  &  $B$



\* Working of Transistor: at  $AI = BI + CPT$

(i) NPN



- (1) The D.C. sources  $V_{EE}$  and  $V_{CC}$  are applied in such a way that B-E junction is forward biased and C-B junction is reverse bias.
- (2) The depletion region of B-E is less than that of C-B as shown in figure.
- (3) since the B-E junction is forward biased, the electrons in N-type emitter flow towards the base, they combine with holes in P-region of the base and constitute the current  $I_E$ .
- (4) As base region is thin and lightly doped, it has

$$\alpha = \frac{I_C}{I_E} \quad \beta = \frac{I_C}{I_B}$$

$$I_E = I_B + I_C \quad I_C = \alpha_{dc} \times I_E$$

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less no. of holes. Therefore very few electrons get injected into base from emitter. They recombine with holes and constitute the base current  $I_B$ .

- (5) The base current is small as compared to emitter current.
  - (6) The remaining large no. of electrons cross the base region and move through the collector to +ve terminal of external battery and constitute collector current  $I_C$ . emitter
  - (7) Most electrons from collector flow into collector region.  $I_C > I_B$

$$I_E \approx I_c$$

NOW,

$$\alpha = I_C \quad \text{and} \quad \beta = I_C$$

$\alpha$  is always smaller

$$I_E = I_B + I_C$$

$I_B$        $\beta$  is always greater  
than 1

Dividing b.s. by Ic

$$\therefore \frac{I_E}{I_C} = \frac{I_C}{I_C} + \frac{I_B}{I_C}$$

$\alpha = \beta_{dc} + 1$  and  $\beta = \frac{1}{\alpha - 1}$  (Power)

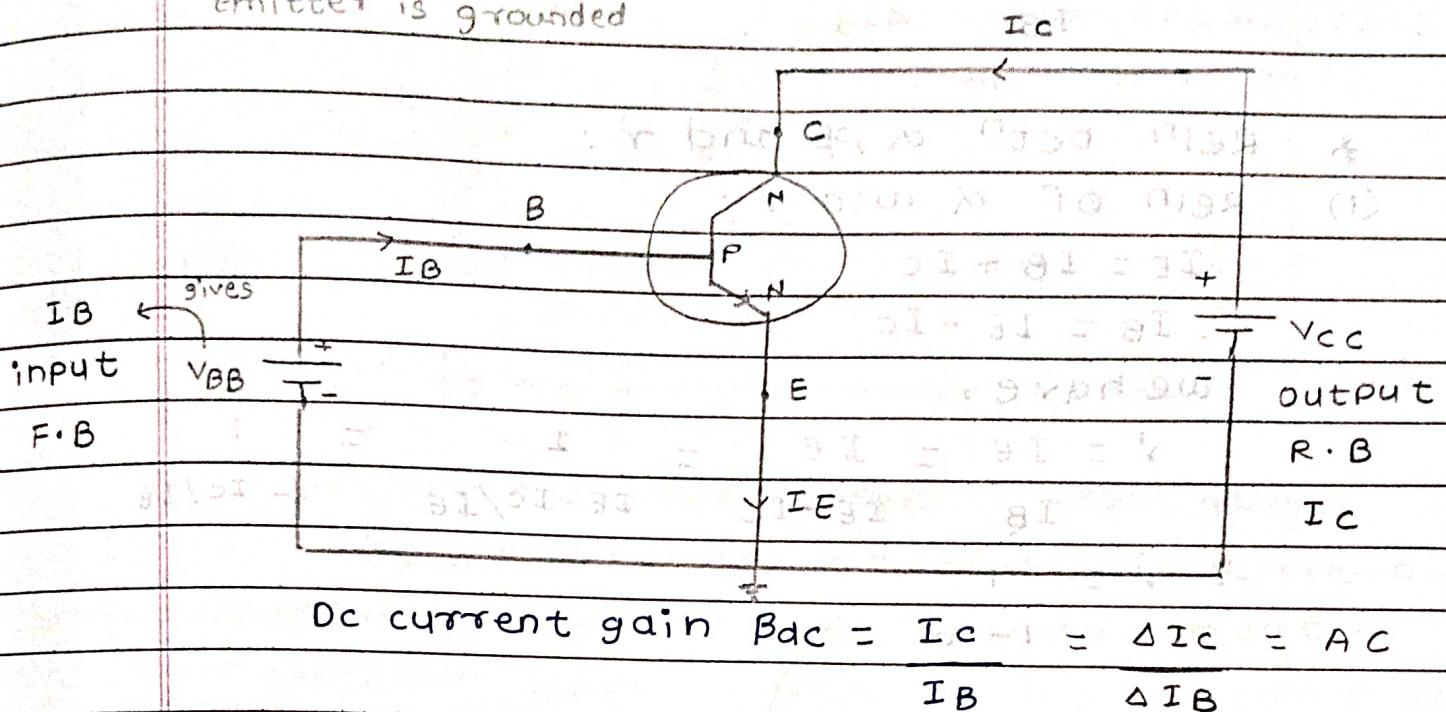
- (iii) In P-N-P transistor, the majority carriers are holes and polarities of  $V_{EE}$  and  $V_{CC}$  are reversed as compared to the N-P-N junction.

So  $V_{EE}$  is to +ve end and  $V_{CC}$  to -ve end. The biasing circuit is same as shown in figure.

DC current gain =  $\frac{\text{output}}{\text{input}}$

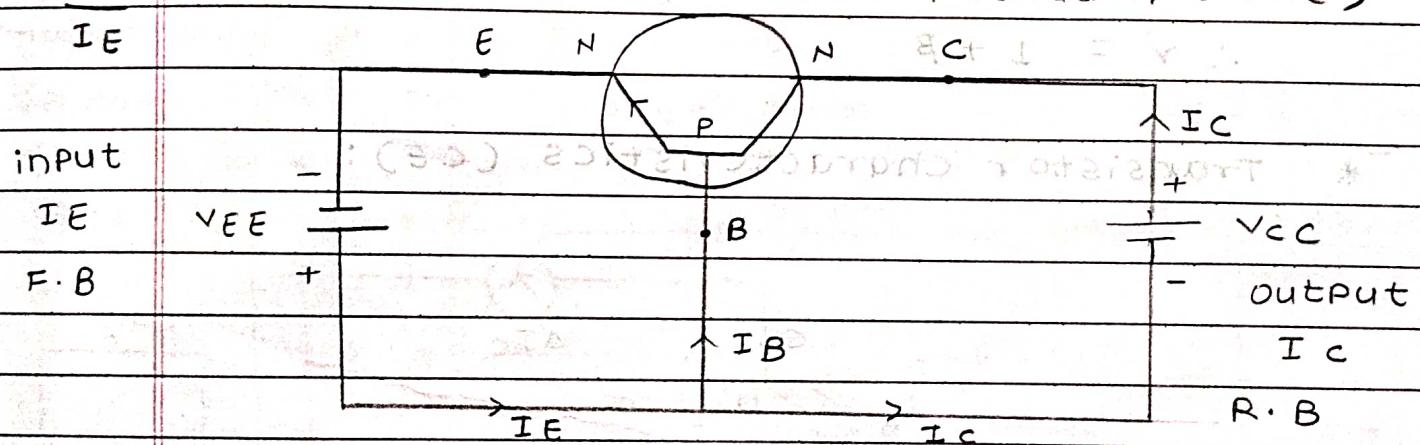
### \* Common Emitter connection (CE): $\beta$

Emitter is grounded

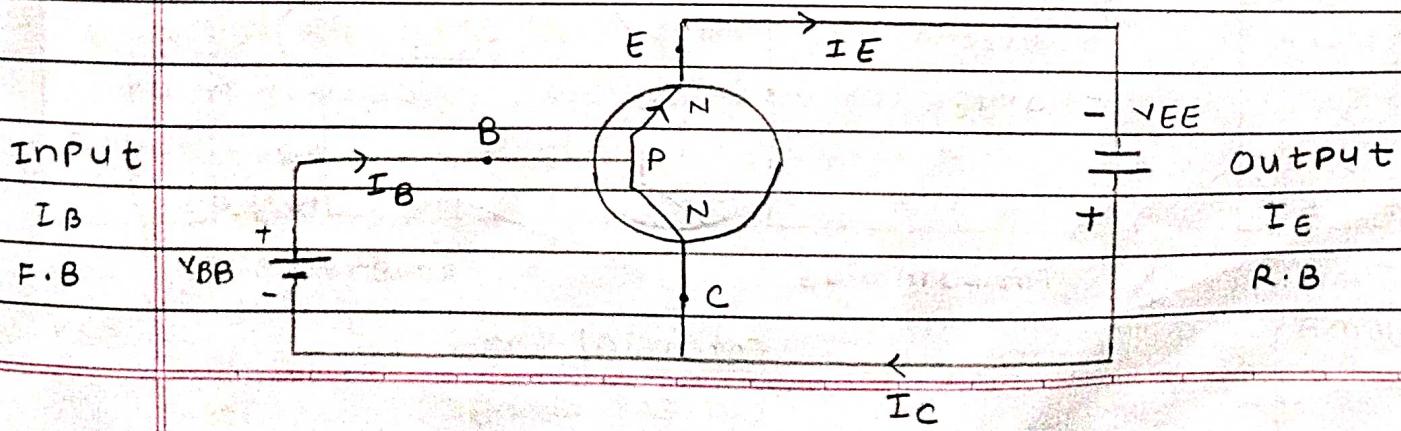


### \* Common Base configuration (CB): $\alpha$

$\alpha = I_c$  (current gain same)



### \* Common collector configuration (cc): $\gamma$



$$E = \beta = I_C/I_B$$

$$B = \alpha = I_C/I_E$$

$$C = \gamma = I_E/I_B$$

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$$\gamma = I_E/I_B - \alpha I_E$$

$$I_B = I_E - I_C$$

\* Reln betn  $\alpha$ ,  $\beta$  and  $\gamma$ :

(1) Reln of  $\alpha$  and  $\gamma$ :

$$I_E = I_B + I_C$$

$$\therefore I_B = I_E - I_C$$

we have,

$$\gamma = \frac{I_E}{I_B} = \frac{I_E}{I_E - I_C} = \frac{1}{1 - I_C/I_E} = 1 + \frac{I_C}{I_E}$$

$$\therefore \gamma = 1 + \alpha$$

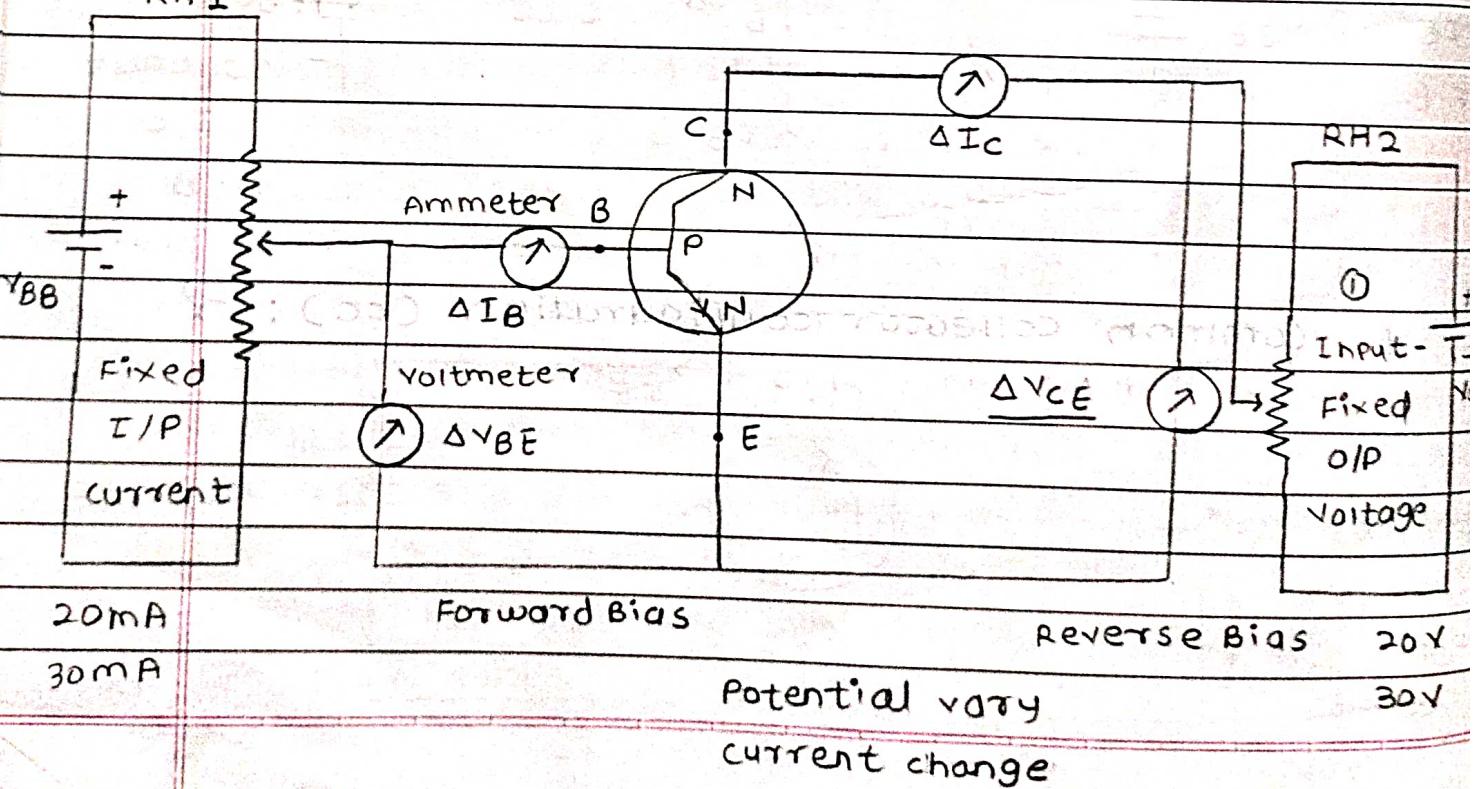
(2) Reln  $\beta$  and  $\gamma$ :

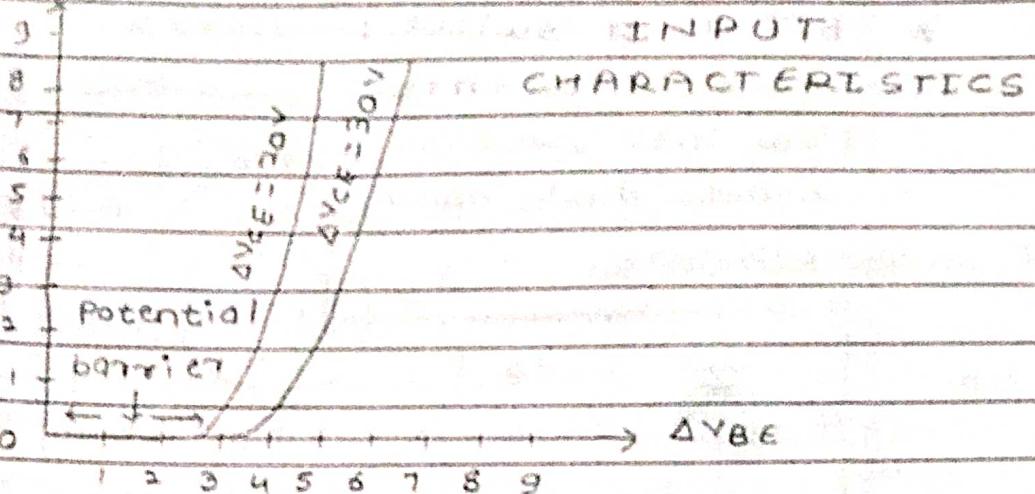
$$\gamma = 1 + \alpha = 1 + \beta/\alpha = 1 + \beta^2/\beta + \beta = 1 + \beta/(1 + \beta)$$

$$\therefore \gamma = 1 + \beta$$

\* Transistor characteristics (CE):  $V$  vs  $I$

RH<sub>1</sub>



$\Delta I_B$ 

↑ cut in voltage/knee voltage - current start

Potential barrier < Potential = current

Output voltage ↑ Reverse biased → current ↑

depletion layer + barrier till depletion ↑ as  
ΔVBE →  $\Delta I_B$  (current increase w.r.t. voltage ↑)

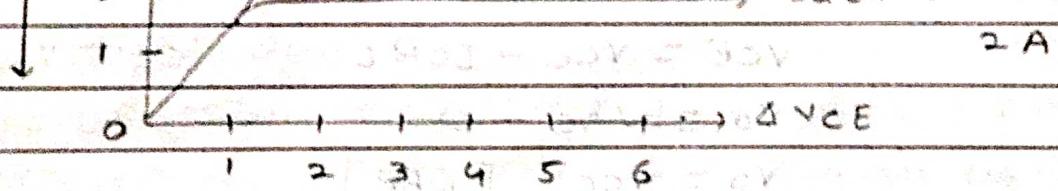
when input is 0 → saturation w.r.t. output

20mA, it can go up to 6V →  $\Delta I_B$  vs.  $\Delta V_{CE}$  CHARACTISTICS

assure only 2A max current

similarly for  $\Delta V_{CE}$  →  $\Delta I_B = 30 \text{ mA} \rightarrow 6 \text{ V}$  → 2A

30mA - 3A →  $\Delta I_B = 20 \text{ mA} \rightarrow$  saturated current



The input is limited/assured. Max = 2A as per cond'n. Input-limit → output limit which does not depend upon potential  $\Delta V$ .

- \* In Input side, with help of RHJ, we vary potential and measure current starting - no current (T) but initially we have to fix the O/P voltage at certain voltage.

### \* BJT as a switch:

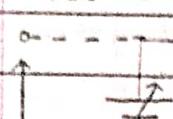
Resistance-Avoid direct current

Flow into junction

Avoids diode damage

↑-variable Potential  $V_{RB}$

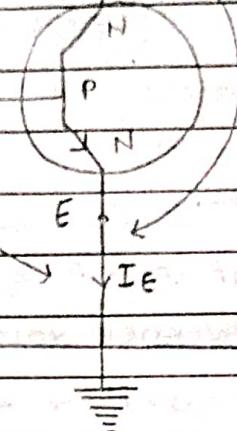
F-B



$I_B$

$V_{BE}$

$V_{BB}$



$V_{CE}$

$I_C$

$V_{CC}$

$V_O$

$R \cdot B$

$I_E$

For switching operation, BJT is biased in cut-off or saturation regions. Most popularly it is used as a switch in digital Electronics.

Figure shows an NPN transistor in common emitter configuration with  $V_i$  and  $V_o \rightarrow R_L$ .

No Potential drop, no current IF  $V_i < 0.7$  Volt [ $V_i < V_{BE}$ ]

current  $I_B = 0$  thus  $I_C = 0$ , bulb does not glows

• Output:  $V_{CC} = I_C R_L + V_{CE}$

$$V_{CE} = V_{CC} - I_C R_L$$

$$V_{CE} = V_{Output}$$

$$V_O = V_{CC} - 0$$

$$I_C R_L = 0 \text{ as } I_B = 0$$

$$V_O = 5V,$$

$$V_O = V_{CC} \quad [\text{OFF}]$$

$V_{in}$  is less

$$V_{CC} = 5V$$

current does not flow through

the resistor. As a result, bulb does not glows up.

And the switch is OFF / No Potential drop

• Case-II: Input voltage  $>$  Potential barrier

IF  $V_i > 0.7$  Volt [ $V_i > V_{BE}$ ]

$$I_B \neq 0$$

$$V_O = V_{CC} - I_C R_L$$

generation of  $I_B$  current

$$\text{current flows}$$

$$V_O \neq V_{CC} \quad [\text{ON}]$$

$$I_C \neq 0$$

$V_o$ 

Advantage of Transistor

cut off region  $V_o = 0$  or  $I_C = 0$  $V_o \propto V_i$ 

saturation region

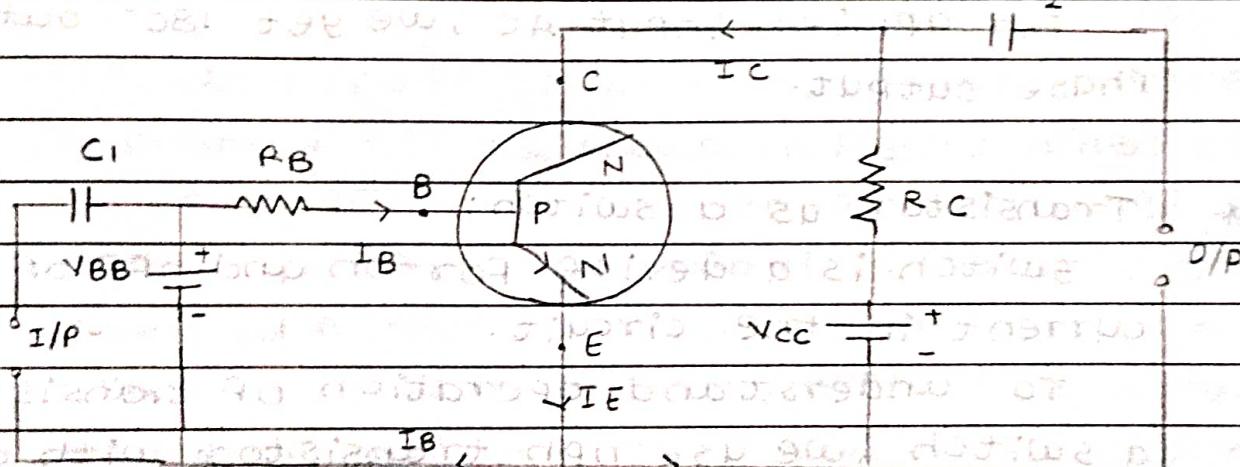
and no saturation region

2.  $V_o > V_i$   $\Rightarrow$  ~~saturation~~ region3.  $V_o < V_i$   $\Rightarrow$  ~~saturation~~ region $V_o = f(V_i)$   $\rightarrow$  ~~transfer characteristic curve~~

Fig: Output Voltage vs Input Voltage

Transfer characteristics curve

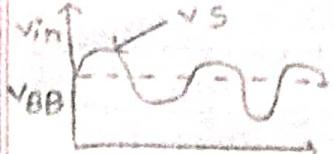
\* Transistor as an Amplifier



gain of  $\times 10^3$ . The circuit diagram of common Emitter NPN amplifier transistor is shown in Fig. Here emitter base junction is made forward biased with battery  $V_{BB}$  and collector emitter junction is made reverse bias. When no AC input is applied, then electrons of the emitter are repelled by -ve terminal of battery  $V_{BB}$ . Due to which  $I_E$  increases and hence collector current also increases.

$$I_E = I_B + I_C$$

circuit which amplifies small input signal to give magnified output signal having same frequency as of the input signal is called an amplifier.



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output is given by

$$V_O = V_{CC} - I_C R_C \quad \text{--- (2)}$$

#### \* Phase Relationship:

Let input AC is applied, initially +ve half cycle is applied it favours forward biasing of BE junction. so IE increases i.e. by eq. (1)  $I_C$  also increases followed by increase in  $I_C R_C$ . we get -ve output of this input.

Let -ve half cycle is applied it opposes the F.B of BE junction, by which IE decreases.

Also  $I_C$  decreases by (1).  $I_C R_C$  decreases and we get +ve output for -ve input.

For applied input AC, we get  $180^\circ$  out of phase output.

#### \* Transistor as a switch:

Switch is a device for on and off of the current in the circuit.

To understand operation of transistor as a switch, we use NPN transistor with common emitter transistor.

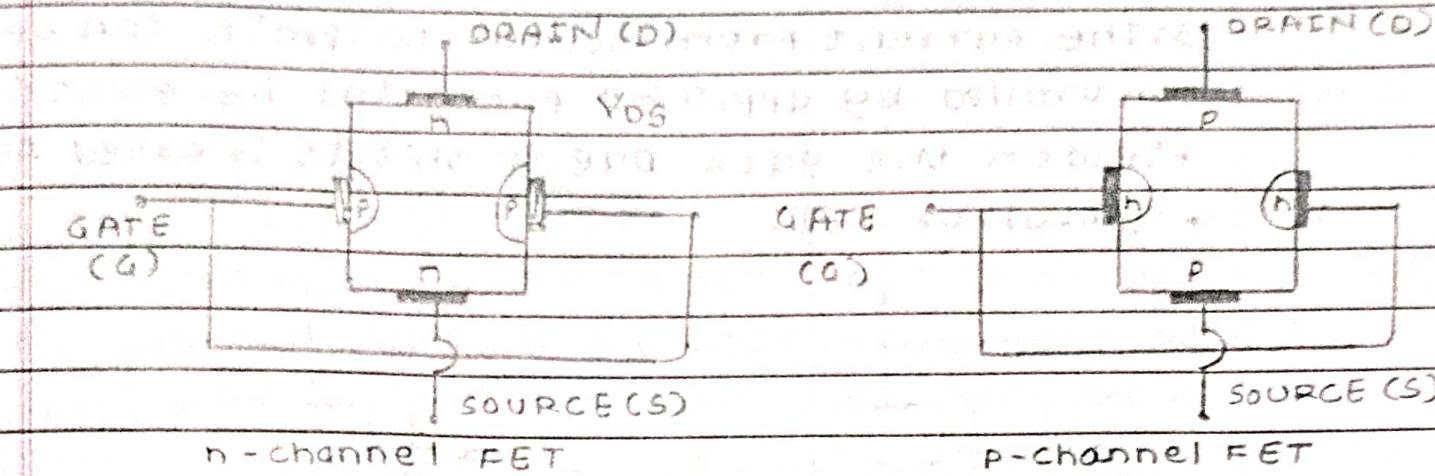
In case of Si transistor  $V_{BE}$  is 0.7 V  
Low input - OFF state, switches transistor off

High input - ON state, switches transistor on.

This indicates that a transistor acts as a switch.

#### \* Field Effect Transistor (FET):

It is a three-terminal semiconductor device in which current conduction is completed by one type of charge carriers i.e. either by hole or electron. The FET has high input impedance and low noise level.



- construction of FET:

(1) A FET consists of p-type and n-type silicon bar containing two p-n junctions at 2 p-n sides.

(2) When bar FET is of n-type, it is called as diode n-channel FET as shown in figure. When bar FET connected is of p-type, it is called as p-channel FET.

(3) Their common terminal is called a gate. other terminals of FET are source and drain.

(4) Thus, a FET has essentially three terminals viz, gate (G), source (S) and drain (D). V<sub>GS</sub>

- working of FET: Two circuit diagrams V<sub>DS</sub>

(1) When voltage V<sub>DS</sub> is applied between drain and source terminals, voltage on gate is zero.

The two p-n junction on sides of bar establish depletion layers. Electron will flow from source to drain. The size of layers determines width of channel).

(2) When reverse voltage V<sub>GS</sub> is applied between gate and source, the width of depletion layer is increased. Current from source to drain is decreased. Reverse voltage on gate is decreased, then width of depletion layer also decreases.

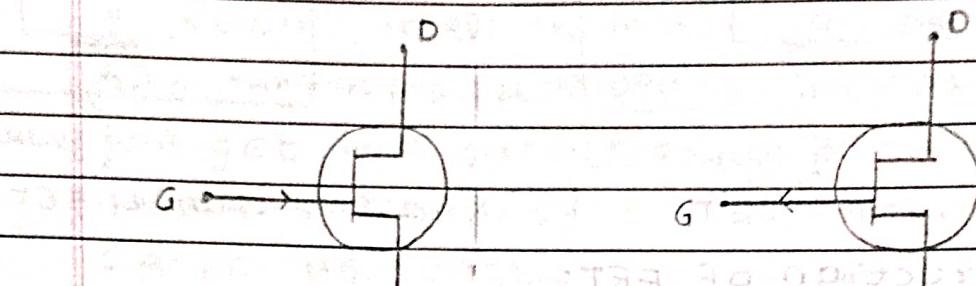
N and P channel FET operates in same manner, current carriers - holes polarities of  $V_{GS}$  and  $V_{DS}$  - reversed

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(3) The current from source to drain can be controlled by appn of potential i.e. electric field on the gate. Due to this it is called FET.

#### • Symbol of FET:

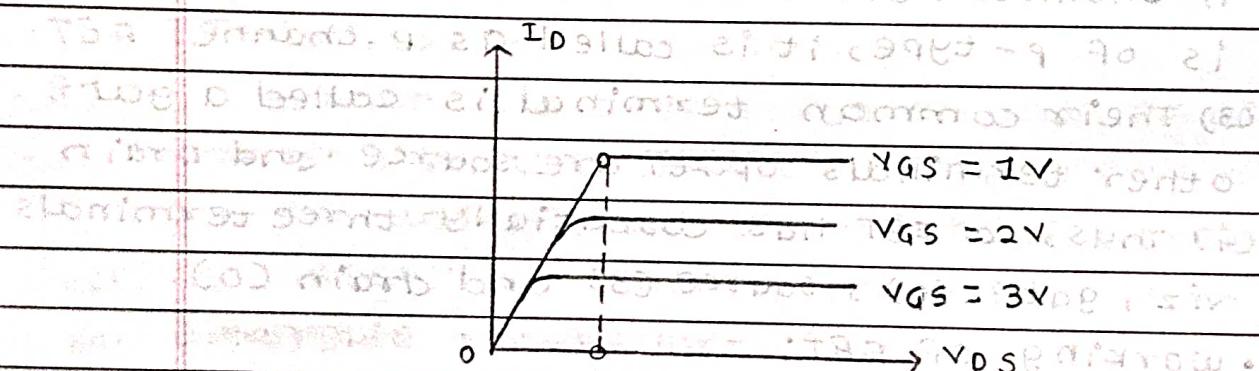


The n-channel FET and p-channel FET

Vertical line = channel

D and S are symmetrical and interchangeable

#### • Output characteristics:



current: for two direction at 80V 900A on one direction

Ques	Sr.	BJT is current controlled device (IC = $\beta I_B$ )	FET is voltage controlled device i.e. field effect transistor.
1.	1.	BJT is current controlled device (IC = $\beta I_B$ )	FET is voltage controlled device i.e. field effect transistor.
2.	2.	BJT is bipolar device i.e. both holes (+) and electrons (-) take part in conduction.	FET is unipolar device holes (P) take part in conduction.
3.	3.	Input impedance is high $R = 1K$ to $5K$	Input impedance is extremely high $M\Omega$ .

current depends

### Holes and electrons

### Holes or electrons

Sr.	BJT	FET
4.	Output impedance is medium.	Output impedance is very high.
5.	Voltage gain is high	Voltage gain is low.
6.	Noise generated by BJT is high bcoz it is bipolar device (two carriers).	FET is unipolar, hence noise generated is low (one carrier).
7.	For voltage amplification BJT is operated in 'active region'.	For voltage amplification, FET is operated in saturation.
8.	Large size.	small size

ANSWER: PROBLEMS BASED ON BIPOLAR JUNCTION TRANSISTOR (BJT)

\* Ques: What is MOSFET? Metadioxide semiconductor field effect transistor (MOSFET) is another

Enhancement MOSFET

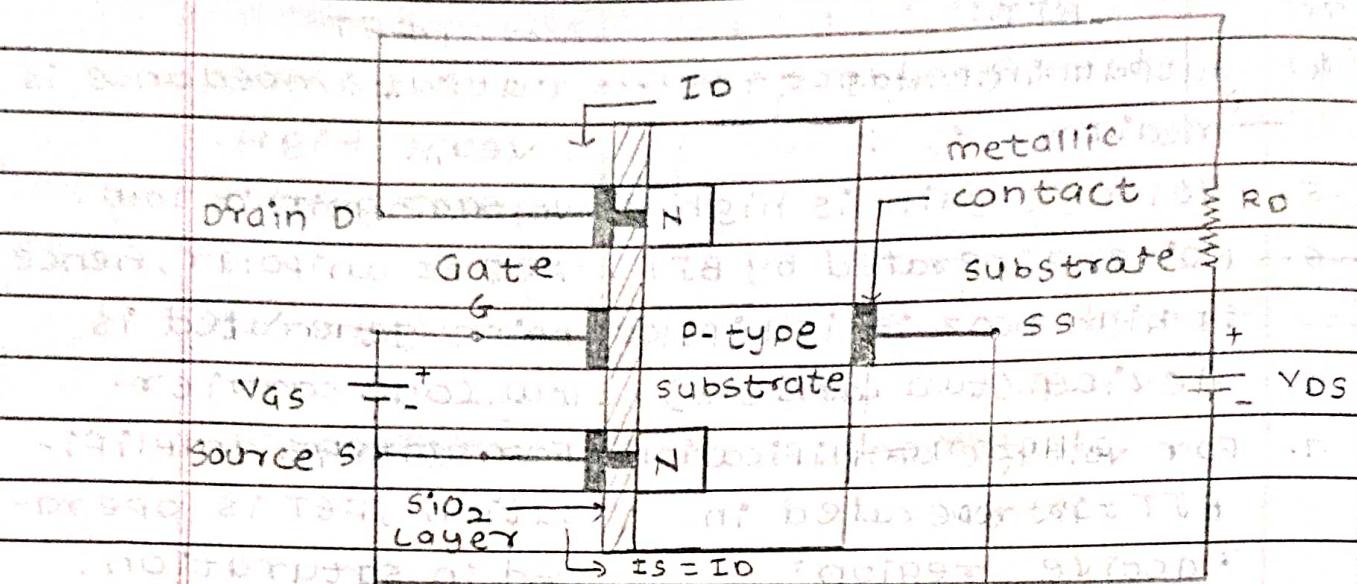
- (1) MOSFET is voltage controlled device, by controlling V<sub>GS</sub>, we can control current I<sub>D</sub>.
- (2) It has four terminals: Gate, drain, source, and substrate.
- (3) It has high switching speed (ON/OFF).
- (4) It has high input impedance.

\* Ques: A FET which operates in enhancement mode is known as

MOSFET, i.e. (TVD)

N-channel EMOSFET

- (1) The figure shows construction of N-channel EMOSFET.
- (2) Here, two highly doped N-regions are diffused into a lightly doped P-type substrate.



(3) Two terminals drain (D) and source (S) are taken out through metallic contacts. A thin layer of silicon dioxide ( $\text{SiO}_2$ ) isolates the gate from the substrate. Tungsten doped n-mosfet.

operation: All started a gap of  $V_{GS} = 0$ .

(1) When  $V_{GS} = 0$ , even if  $V_{DS}$  is applied, between drain and source, no current flows through the device. Any voltage does not constitute any current flow.

(2) If  $V_{GS}$  is increased in the direction, conc. of electrons from p-substrate increases near  $\text{SiO}_2$  layer.

(3) At particular value of  $V_{GS}$ , threshold voltage ( $V_T$ ) is developed and hence current starts flowing from source to drain.

(4) If  $V_{GS}$  is increased further, density of electrons, getting pulled into conducting channel increases, which enhances value of drain current.

(5) For voltage less than  $V_T$ , conduction does not take place because, the channel cannot be formed.

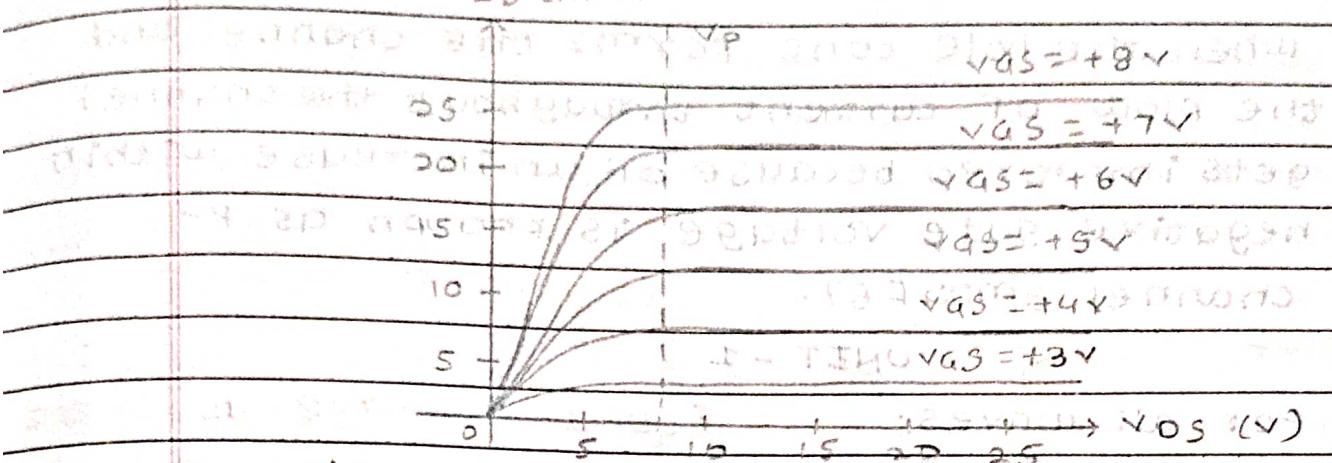
Transfer - +ve region

$I_D$  does not flow until  $V_{GS} = V_T$

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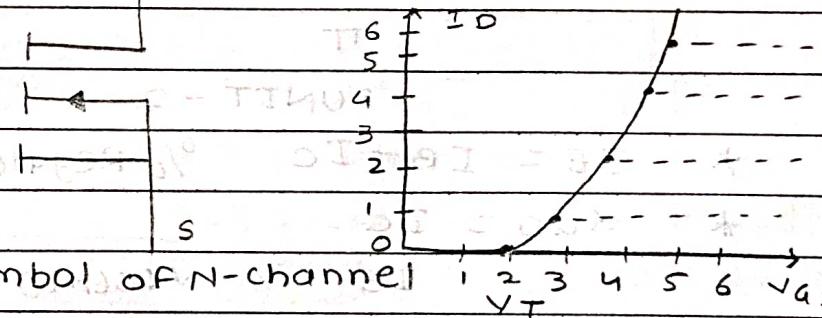
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$I_D$  (mA)

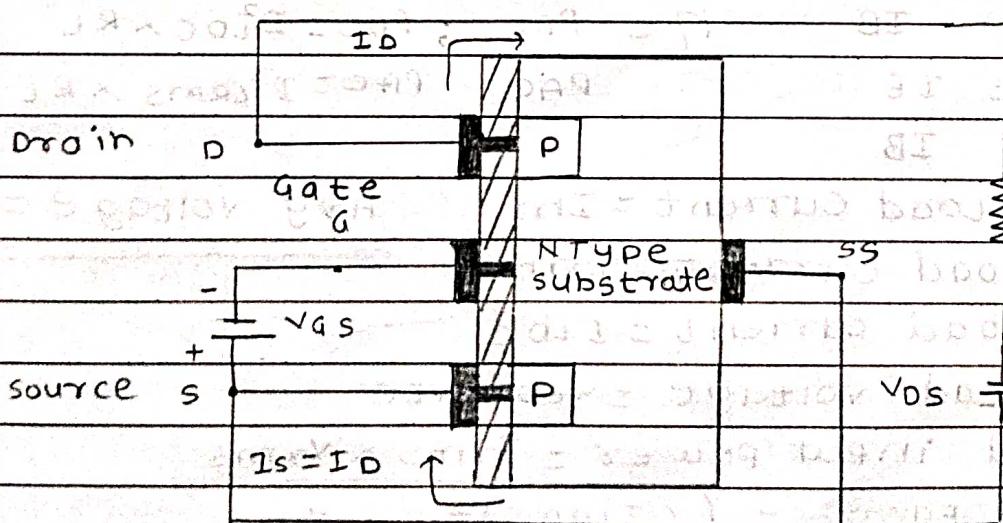


- (1) From Fig, we can see that the drain current increases as voltage  $V_{DS}$  is increased beyond threshold voltage.
- (2) The drain current reaches saturation level at certain value of input voltage  $V_{DS}$ .

• Transfer characteristics:



\* P-channel MOSFET: \*



Half	Full	Bridge
1.21	0.48	0.48
121%	48%	48%

When the hole conc. forms the channel and the flow of current throughout the channel gets improved because of an increase within negative gate voltage is known as P-channel MOSFET.

### UNIT - 1

\* For all waves:  $I_{LDC}$  = Average dc current  
 $V_m = \sqrt{2} \times V_{rms}$  PIV - Peak Inverse Voltage

\* Peak load current  $I_m = \frac{V_m}{R_f + R_L}$

\*  $V_{LDC} = \frac{V_m}{\pi} \left( 1 - \frac{1}{\pi} \right)$  Average dc voltage }  
 } Half Wave Rectifier

\*  $I_{LDC} = \frac{I_m}{\pi}$

### UNIT - 2

\*  $I_E = I_B + I_C$  % Regulation =  $\frac{V_{DC(NL)} - V_{DC(FL)}}{V_{DC(FL)}} \times 100$

\*  $\alpha_{dc} = \frac{I_C}{I_E}$   $V_{DC(NL)} = V_{LDC}$

\*  $\beta_{dc} = \frac{I_C}{I_B}$   $V_{DC(FL)} = V_{DC(NL)} - I_{LDC} (R_{input})$

$\eta = \frac{P_{DC}}{P_{AC}}$ ;  $P_{DC} = I_{LDC}^2 \times R_L$

\*  $\gamma_{dc} = \frac{I_E}{I_B}$   $P_{AC} = I_{rms}^2 \times R_L$

- Peak load current =  $I_m$  Avg voltage =  $V_{LDC}$

- AC load current =  $I_{rms}$

- Dc load current =  $I_{LDC}$

- DC load voltage =  $V_{DC}$

- Total input power =  $I_{rms} \times V_{rms}$

- Ripple factor =  $\sqrt{\frac{(I_{LRMS})^2 - 1}{(I_{LDC})^2}}$

$$\% \text{ Regulation} = \frac{R_F}{R_L} \times 100$$

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\* EMOSFET :

\* MOSFET as a switch:

EMOSFET are generally used for switching applications because of their threshold characteristics  $V_{GS}$

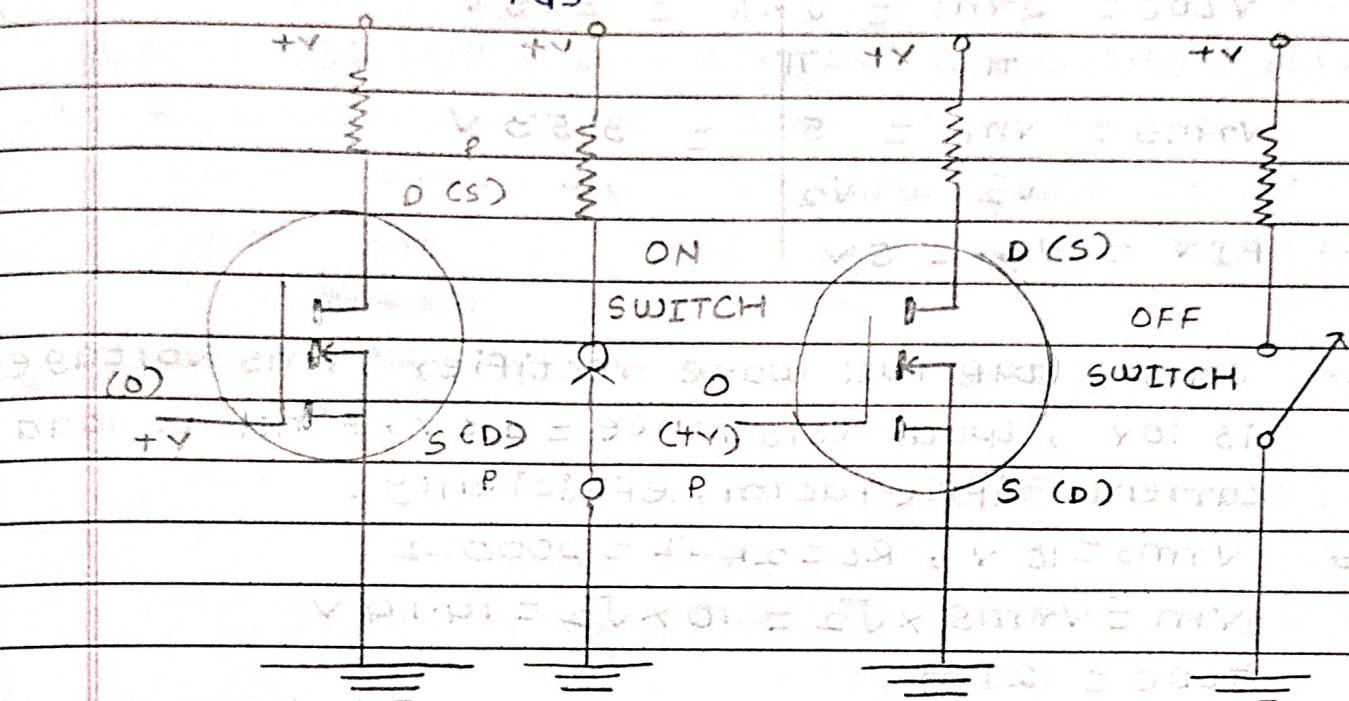


Fig : n-channel MOSFET ; switch Equivalence

Fig : P-channel MOSFET ; switch Equivalence  
when gate to source volt is less than the threshold volt, the MOSFET is OFF.

when gate to source volt is greater than the threshold value, the MOSFET is ON.

- Advantages:

- (i) MOSFET switches has 'high speed' compared to mechanical switches.
- (ii) MOSFET switches are more reliable as compared to mechanical switches.
- (iii) When  $V_{GS}$  is varied between  $V_{GS(T)}$  and  $V_{GS(ON)}$ , the MOSFET is being operated as a switch.

## UNIT - 1

## \* Numericals:

1. For Bridge full wave rectifier, applied voltage is  $5 \sin \omega t$ . Find avg output, rms and PIV voltage

$$\rightarrow V_m = 5 \text{ V}$$

$$V_{DC} = \frac{2V_m}{\pi} = \frac{2 \times 5}{\pi} = 3.18 \text{ V}$$

$$V_{rms} = \frac{V_m}{\sqrt{2}} = \frac{5}{\sqrt{2}} = 3.53 \text{ V}$$

$$PIV = V_m = 5 \text{ V}$$

2. Centre tap full wave rectifier, rms voltage is 10V, load resistance = 2kΩ, Find DC load current, ripple factor, efficiency.

$$\rightarrow V_{rms} = 10 \text{ V}, R_L = 2k\Omega = 2000 \Omega$$

$$V_m = V_{rms} \times \sqrt{2} = 10 \times \sqrt{2} = 14.14 \text{ V}$$

$$I_{DC} = 2Im$$

$$\therefore I_m = \frac{V_m}{R_L} = \frac{14.14}{2000} = 7.07 \times 10^{-3} = 7.07 \text{ mA}$$

$$\therefore I_{DC} = 2 \times 7.07 = 4.52 \text{ mA}$$

$$I_{rms} = \frac{I_m}{\sqrt{2}} = \frac{7.07}{\sqrt{2}} = 4.99 \text{ mA}$$

$$\text{Ripple Factor} = \sqrt{(I_{rms})^2 - I_m^2}$$

$$= \sqrt{(4.99)^2 - (7.07)^2} = 0.483 \text{ or } 48.3 \%$$

$$\text{Efficiency} = \frac{P_{DC}}{P_{AC}} = \frac{40.53}{50} \times 100 = 81.07 \%$$

$$P_{DC} = I^2 L_{DC} \times R_L = 40.53 \text{ mW}$$

$$P_{AC} = I^2 L_{rms} \times R_L = 50 \text{ mW}$$

- .3. A diode internal resistance is  $20\text{V}$  which supply power to  $1000\text{ ohms}$  load of  $110\text{V}_{\text{rms}}$  source. calculate: (Half Wave)
- (1) Peak load current
  - (2) DC load current
  - (3) AC load current
  - (4) DC diode voltage
  - (5) Total input power
  - (6) Percentage regulation

$$\rightarrow R_L = 1000 \Omega, R_F = 20\text{V}, V_{\text{rms}} = 110\text{V}$$

$$V_m = V_{\text{rms}} \times \sqrt{2} = 110 \times \sqrt{2} = 155.56\text{V}$$

$$I_m = \frac{V_m}{R_L + R_F} = \frac{155.56}{1000 + 20} = 0.1525\text{A}$$

$$I_{\text{DC}} = \frac{I_m}{\pi} = \frac{0.1525}{\pi} = 0.0485\text{A}$$

$$I_{\text{LRMS}} = \frac{I_m}{2} = \frac{0.1525}{2} = 0.07625\text{A}$$

$$V_{\text{DC}} = I_{\text{DC}} \times R_L = 0.0485 \times 1000 = 48.5\text{V}$$

$$\text{Total input} = I_{\text{LRMS}}^2 \times (R_L + R_F)$$

Power (PAC)

$$= (0.07625)^2 \times (1000 + 20)$$

$$= (0.07625)^2 \times 1020$$

$$\therefore \text{PAC} = 5.93\text{W}$$

$$V_{\text{DC(FL)}} = V_{\text{DC}} = 48.5\text{V}$$

$$V_{\text{DC(NL)}} = \frac{V_m}{\pi} = \frac{155.56}{\pi} = 49.49$$

$$\% \text{ Regulation} = \frac{V_{\text{DC(NL)}} - V_{\text{DC(FL)}}}{V_{\text{DC(FL)}}} \times 100$$

$$= 49.49 - 48.5 \times 100$$

$$\% \text{ Regulation} = 2\%$$

## OP-AMP Practical characteristics:

### Ideal characteristics:

- (1) Infinite voltage gain ( $A_V$ )
- (2) Infinite input impedance ( $R_{IN}$ )
- (3) zero output impedance ( $R_{OUT}$ )
- (4) zero output voltage when input voltage is zero.
- (5) infinite bandwidth ( $BW$ )
- (6) infinite slew rate (SR)

### \* Photo Diode:

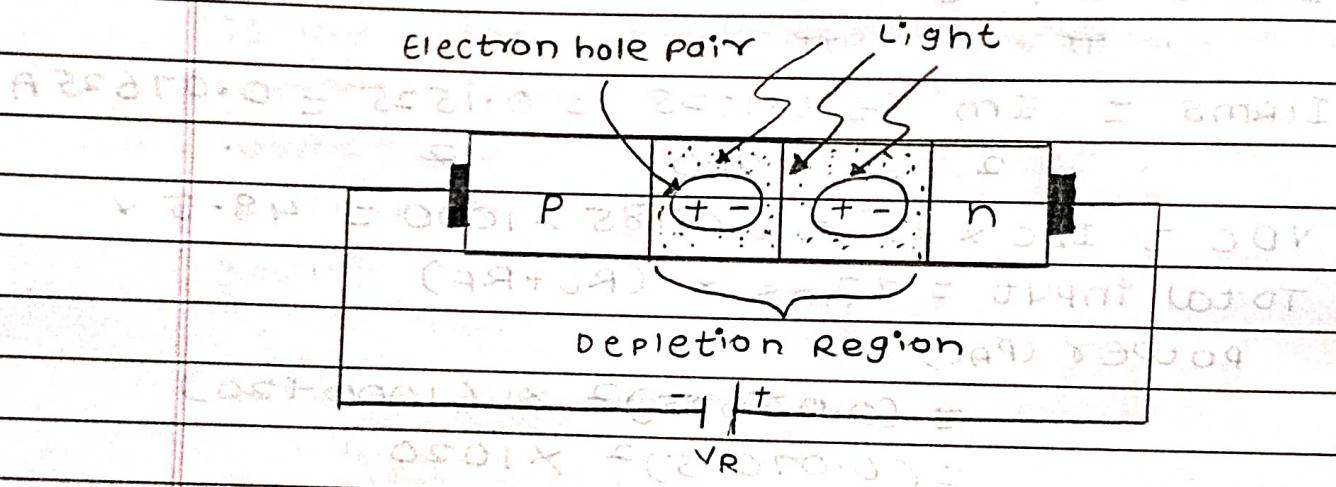


Fig: Photo Diode

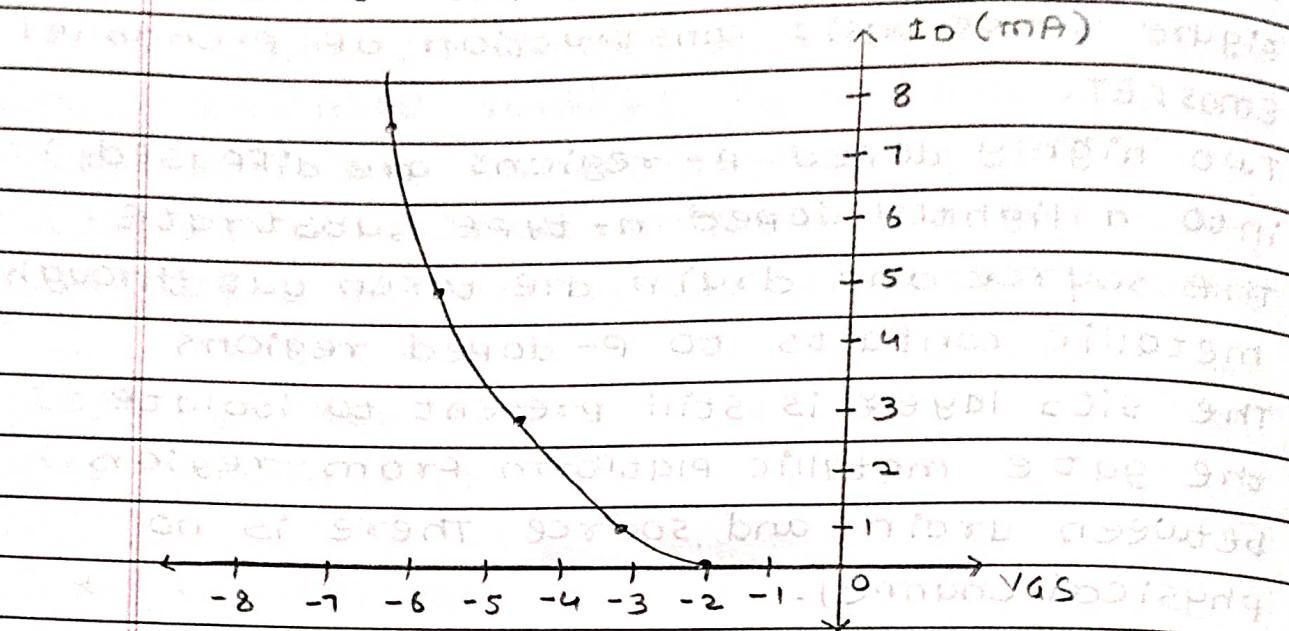
No.	LED	Photodiode
1.	It is a photoemitter device.	It is a photodetector device.
2.	It converts electrical energy to light energy.	It converts light energy into electrical energy.
3.	It is operated in F.B.	It is operated in R.B.
4.	More the forward current, more is light output	more light intensity, more is photocurrent.
5.	Materials used for manufacturing are GaAs, GaAsP, GaP, etc.	Materials used for manufacturing are Si, Ge, InGaAs, etc.

- \* P-channel EMOSFET:
- (1) Figure shows basic construction of P-channel EMOSFET.
- (2) Two highly doped p-regions are diffused into a lightly doped n-type substrate.
- (3) The source and drain are taken out through metallic contacts to p-doped regions.
- (4) The  $\text{SiO}_2$  layer is still present to isolate the gate metallic platform from region between drain and source. There is no physical channel.

• Operation: P-channel MOSFET avoids depletion mode

- (1) This type of MOSFET operates only in the enhancement mode and has no depletion mode.
- (2)  $V_{GS} = 0$ : Even if  $V_{DS}$  is applied between drain and source, no current flows through device. Any voltage does not constitute any current flow.
- (3)  $V_{GS} < 0$ : If we increase magnitude of  $V_{GS}$  in -ve direction, conc. of holes near  $\text{SiO}_2$  surface increases.
- (4) At particular value of  $V_{GS}$ , threshold voltage ( $V_T$ ) is developed and hence current starts flowing from drain and source.
- (5) In P-channel EMOSFET, a -ve gate voltage above a threshold value induces a channel.
- (6) For voltage less than  $V_T$ , conduction does not take place because the channel cannot be formed.

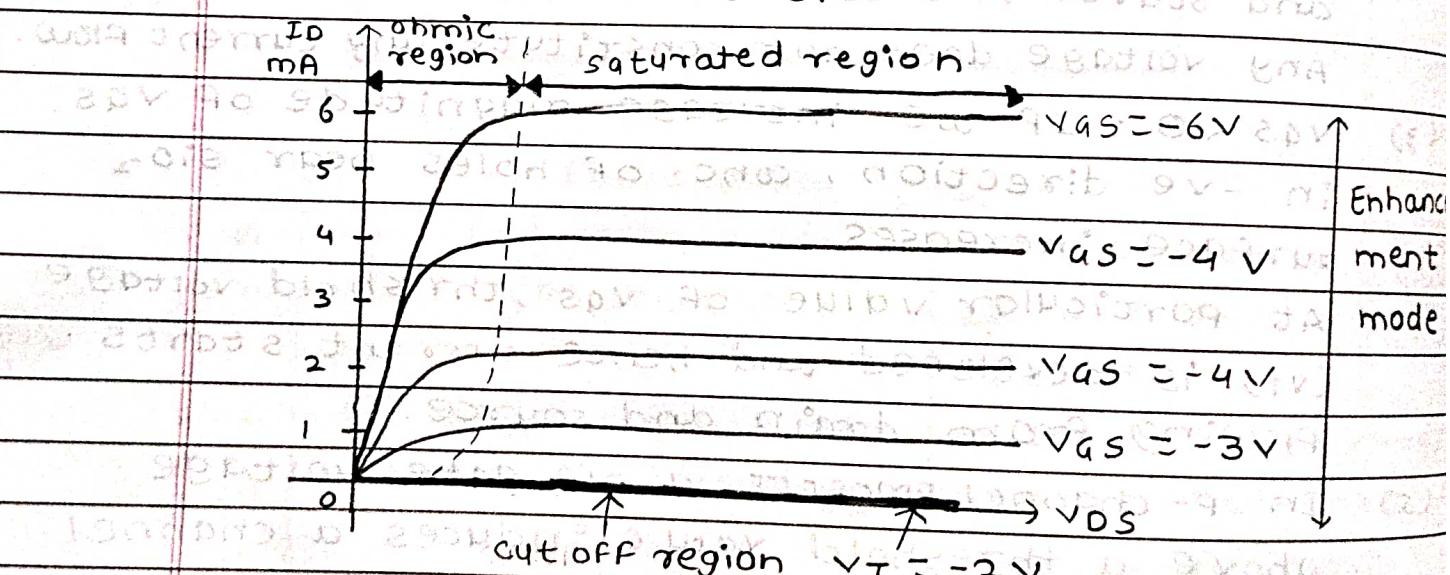
## \* Transfer characteristics:



(1) Figure shows transfer characteristics.

(2) Here, the transfer characteristics is a mirror image about  $I_D$  axis (Y-axis) of transfer characteristics of n-channel MOSFET, since  $V_{GS}$  is negative.

## \* Drain characteristics:



(1) The figure shows drain characteristics.

(2) Here, we can figure out that drain current increases with increase in negative gate to source voltage ( $V_{GS}$ ).

• Numericals:

- \* An OP-amp is used in non-inverting mode with  $R_i = 1\text{ k}\Omega$ ,  $R_f = 12\text{ k}\Omega$ ,  $V_{CC} = \pm 15\text{ V}$ . calc output voltage for

$$(i) v_{in} = 250\text{ mV} \quad (ii) v_{in} = 3\text{ V}$$

→ For non-inverting mode

$$A = \left( 1 + \frac{R_f}{R_i} \right) = 1 + 12 = 13$$

$$\therefore V_o = 13$$

$v_{in}$

$$\therefore V_o = 13 \times v_{in}$$

$$(i) v_{in} = 250\text{ mV}$$

$$\therefore V_o = A \cdot v_{in}$$

$$= 13 \times 250 \times 10^{-3}$$

$$\therefore V_o = 3.25\text{ V}$$

$$(ii) v_{in} = 3\text{ V}$$

$$\therefore V_o = A \cdot v_{in}$$

$$= 3 \times 13$$

$$\therefore V_o = 39\text{ V}$$

• FORMULA

For inverting amplifier

$$A = \frac{V_o}{V_i} = - \frac{R_f}{R_1}$$

For non-inverting

amplifier

$$A = \frac{V_o}{V_i} = \left( 1 + \frac{R_f}{R_1} \right)$$

But OP-amp output saturates at  $+V_{CC}$  i.e.  $\pm 15\text{ V}$ . Thus practically output saturates at  $+15\text{ V}$  and  $39\text{ V}$  output is not practically possible.

- \* calc. output voltage ' $V_o$ ' of OP-amp. Draw E/P and O/P waveforms:

→ For non-inverting mode,

$$R_f = 20\text{ k}\Omega, R_i = 10\text{ k}\Omega$$

$$\therefore V_o = \left( 1 + \frac{R_f}{R_i} \right) V_p = \left( 1 + \frac{20}{10} \right) \times 3 \sin \omega t$$

$$\therefore V_o = 9 \sin \omega t$$

• Input waveform:  $y_i$  • Output waveform:  $y_o$

