ELE 401 - GRADUATION PROJECT I
INTERIM REPORT

Hacettepe University
Department of Electrical and Electronics Engineering

Design and Implementation of a 5-Level Cascaded H-Bridge Multilevel Inverter with PWM-Based Control

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1. INTRODUCTION

This interim report presents the progress made in the design and development of a 5-level Cascaded H-Bridge (CHB) multilevel inverter for power electronics applications. The project aims to create a high-efficiency power conversion system capable of generating near-sinusoidal output voltages with minimal harmonic distortion, suitable for renewable energy integration and distributed generation systems.

Multilevel inverters have gained significant attention in modern power electronics due to their ability to produce high-quality output waveforms, reduce voltage stress on switching devices, and minimize electromagnetic interference. The CHB topology, in particular, offers advantages including modular structure, independent DC source requirement, and scalability, making it an ideal choice for medium-voltage applications.

This report documents the design methodology, component selection rationale, and preliminary design decisions made during the first phase of the project. Comprehensive component comparisons are provided, with particular emphasis on the selection of MOSFETs over IGBTs for the switching elements and the critical choice of TLP250 optically isolated gate drivers. The IR2110 bootstrap driver was initially evaluated but proved incompatible with the CHB topology's floating H-bridge configuration through simulation validation. Level-Shifted Carrier PWM was selected as the modulation strategy based on extensive Simulink validation and implementation feasibility. The report also addresses relevant engineering standards, particularly IEEE 519-2022 for harmonic control, and demonstrates alignment with Sustainable Development Goals.

2. PROJECT DESCRIPTION

The project focuses on designing and implementing a single-phase 5-level Cascaded H-Bridge multilevel inverter operating at laboratory scale. The system is designed with conservative specifications to ensure safe operation while demonstrating the principles and advantages of multilevel inverter technology.

2.1 System Specifications

The inverter system specifications are:

- Topology: 2× H-Bridge modules connected in series (5-level output)
- DC Input Voltage: 50V per module
- AC Output: 100V peak AC, 70.7V RMS, 10A, ~700W
- Output Power: 707W continuous
- Switching Frequency: 5kHz PWM
- Modulation: Level-Shifted Carrier PWM (validated in Simulink)
- Dead-time: 1-2µs for shoot-through prevention
- Power Switches: IRFZ44N MOSFETs (55V, 49A, 17.5mΩ Rds(on))
- Gate Driver: TLP250 optically isolated (2.5kV isolation)
- Protection: RC snubbers (10Ω, 100nF), TVS diodes, fuses
- Control Platform: STM32F303 Nucleo Board (72MHz ARM Cortex-M4)
- Target THD: <5%
- Efficiency Target: >95%

2.2 Project Implementation Phases

Phase 1 (Weeks 1-4): System Modeling and Simulation - COMPLETED

- MATLAB/Simulink model development with detailed IRFZ44N MOSFET parameters
- Level-Shifted Carrier PWM implementation and validation
- Control algorithm design (PR controller, voltage balancing)
- Gate driver evaluation: IR2110 simulation revealed floating bridge incompatibility
- TLP250 isolated driver implementation and successful validation
- Performance analysis: THD = 4.9%, efficiency >95%
- Component selection validation through simulation

Phase 2 (Weeks 5-8): Hardware Design and Component Procurement - CURRENT

- PCB design for power stage with isolated gate driver sections
- Component procurement (MOSFETs, TLP250 drivers, DC-DC converters)
- Protection circuit design and validation
- Snubber network calculations
- Thermal analysis and heat sink selection
- Isolated power supply design for 8× TLP250 drivers

Phase 3 (Weeks 9-12): STM32F303 Control Implementation

- Incremental control system development on STM32F303 Nucleo board
- Level-Shifted PWM generation with 4 vertically offset carriers
- Hardware dead-time insertion (STM32 timer feature)
- ADC sampling (5khz synchronized with PWM)
- PR controller implementation (50Hz resonant)
- DC-link voltage balancing algorithm
- Protection logic and fault management
- Real-time monitoring and data logging

Phase 4 (Weeks 13-16): Integration and Testing

- Complete system integration and debugging
- Performance validation under resistive loads
- Performance validation under R-L loads
- Harmonic analysis using FFT (validation of <5% THD target)
- Efficiency measurements across load range
- Transient response testing
- Thermal performance validation
- Documentation and final report preparation

3. DESIGN CONSTRAINTS

The design of the 5-level Cascaded H-Bridge multilevel inverter is subject to several technical and practical constraints that must be carefully addressed throughout the project. These constraints guide the design process and are considered during all stages of development.

3.1 Technical Constraints

Voltage and Current Ratings

The selection of semiconductor devices is primarily constrained by voltage and current ratings. Each H-bridge module operates at 50V DC input. However, in H-bridge topology, MOSFETs operate in series when OFF, dividing the bus voltage between high-side and low-side devices. Therefore, maximum voltage stress per MOSFET is approximately 25V (50V ÷ 2). The IRFZ44N MOSFET with 55V V_DSS rating provides a 120% voltage margin above the 25V operating stress, ensuring safe operation even with switching transients and voltage spikes.

With 707W output at 70.7V RMS (10A RMS), accounting for reactive loads and transients, peak currents can reach 14-15A. The selected IRFZ44N device rated for 49A continuous (T_C = 25°C) and 196A pulsed operation provides substantial margin for reliable operation.

Gate Driver Isolation Requirements for CHB Topology

The Cascaded H-Bridge topology presents a unique and critical constraint: One H-bridge module operates at a floating potential relative to ground.

This floating nature creates an ABSOLUTE REQUIREMENT for true galvanic isolation in gate drivers. Bootstrap-based drivers like the IR2110, which work excellently in ground-referenced half-bridge or full-bridge configurations, CANNOT provide adequate isolation for floating H-bridges. The bootstrap capacitor references the source terminal of the high-side MOSFET, which itself floats at different potentials in cascaded configurations. This fundamental limitation was confirmed through Simulink simulation where IR2110 models failed to provide correct gate drive voltages for modules 2, 3, and 4.

Therefore, optically isolated gate drivers (TLP250) with independent isolated power supplies for each driver are MANDATORY for CHB topology. This is not a design preference but a fundamental requirement imposed by the cascaded series connection architecture.

Harmonic Distortion Limits (IEEE 519-2022)

IEEE 519-2022 establishes limits for harmonic distortion in power systems. For systems rated 150V through 69kV at the Point of Common Coupling (PCC):

- Total Harmonic Distortion (THD_V): ≤8% for V < 1kV
- Individual Harmonic Limits: Vary by harmonic order

This project targets THD_V <5% to provide margin below the standard limit. Simulink validation using Level-Shifted Carrier PWM achieved THD = 4.9%, meeting this target. This result drives:

- Selection of Level-Shifted Carrier PWM (proven through simulation)
- 5kHz switching frequency
- LC output filter design with cutoff frequency at 1kHz
- DC-link voltage balancing to prevent low-frequency distortion

Control System Timing Constraints

The STM32F303 microcontroller must execute control algorithms with Level-Shifted PWM generation within strict real-time constraints:

- PWM Period: 200µs (5kHz switching frequency)
- Carrier Generation: 4 level-shifted triangular carriers
- Single Reference: One sine calculation shared by all modules
- ADC Conversion Time: ~5µs (12-bit, 1MHz sampling)
- Control Algorithm Execution: <50µs (current loop calculation)
- Total Control Loop Latency: <70µs

Level-Shifted PWM simplifies implementation as all four carriers share the same frequency and phase, differing only in DC offset. This reduces computational burden and simplifies timer configuration compared to phase-shifted approaches.

3.2 Engineering Standards Compliance

IEEE 519-2022: Harmonic Control in Electric Power Systems

Key Requirements:

- Voltage Distortion Limits: THD ≤ 8% for systems <1kV
- Measurement Methods: 10/12 cycle windows with statistical aggregation

Project Compliance:

- Achieved THD = 4.9% in Simulink with Level-Shifted Carrier PWM
- LC output filter designed with 1kHz cutoff
- Harmonic analysis using FFT following IEC 61000-4-7 methodology

3.3 Safety and Protection Requirements

Safety forms a critical constraint, requiring multiple layers of protection:

Isolation Requirements (Critical for CHB):

- Optical isolation in gate drivers: TLP250 with 2.5kV isolation rating
- Isolated DC-DC converters: One per H-bridge module for gate driver power
- Separate power supplies for control and power stages
- Isolated feedback circuits for voltage/current sensing

Overcurrent Protection:

- Fast-acting fuses (6.3A) on each DC input
- Current sensing with shutdown threshold at 6A (120% rated)
- Response time: <10µs from detection to MOSFET turn-off

Overvoltage Protection:

- TVS diodes across DC inputs (clamping at 58V)
- DC-link voltage monitoring with shutdown at 48V per module
- RC snubber networks (10Ω, 100nF) to suppress voltage spikes

4. LITERATURE REVIEW

4.1 Background from Undergraduate Coursework

The foundation for this project draws from multiple courses:

ELE226 - Circuit Theory II: AC analysis, Fourier series, harmonic analysis, filtering
ELE315 - Electronics II: Power semiconductors, switching characteristics, gate drives, thermal management
ELE354 - Control Systems: PID design, stability analysis, digital control implementation
ELE301 - Signals and Systems: FFT, sampling theory, DSP, filter design

4.2 Multilevel Inverter Theory

Multilevel inverters synthesize AC voltage from multiple DC levels, producing stepped waveforms that approach sinusoidal shape. Increasing voltage levels reduces harmonic distortion and minimizes filtering requirements.[1] The three primary topologies are:

1. Neutral Point Clamped (NPC): Uses clamping diodes, single DC source, voltage balancing challenges
2. Flying Capacitor (FC): Uses flying capacitors, complex pre-charging, high component cost
3. Cascaded H-Bridge (CHB): Modular structure, requires isolated DC sources, simplest control [4]

4.3 Level-Shifted Carrier PWM for CHB

Level-Shifted Carrier PWM uses N triangular carriers (where N = number of H-bridges) vertically shifted to occupy different voltage bands.

For a 4-module CHB with Level-Shifted PWM:
• Carrier 1 (Module 1): Occupies +0.5 to +1.0 range
• Carrier 2 (Module 2): Occupies 0.0 to +0.5 range
• Carrier 3 (Module 3): Occupies -0.5 to 0.0 range
• Carrier 4 (Module 4): Occupies -1.0 to -0.5 range
• All carriers share identical frequency and phase
• Single sinusoidal reference compared with all carriers

Key advantages for implementation:
• All carriers synchronized naturally (same frequency and phase)
• Single timer configuration replicated across modules
• Easier debugging: All switching edges aligned temporally
• Direct correlation between reference magnitude and active modules
• Simpler STM32 implementation using timer compare registers

4.4 Gate Driver Requirements for Cascaded Topologies

A critical and often overlooked aspect in multilevel inverter implementation is the gate driver isolation requirement. In the paper by Corzine and Familiant [9] they emphasize that CHB topology requires true galvanic isolation for each H-bridge module due to the series-stacked architecture where each module operates at a different floating potential.

Bootstrap-based drivers (e.g., IR2110, IRS2110) are designed for ground-referenced applications where the low-side switch source terminal connects to ground or a common reference. In CHB topology:

- Only bottom H-bridge is ground-referenced
- Upper H-bridge float at progressively higher potential.
- Bootstrap capacitor voltage references the floating high-side source terminal
- Common-mode voltage across driver exceeds bootstrap driver isolation rating
- Resulting in inadequate or failed gate drive for upper H-bridge.

Solutions for CHB gate drive include:

1. Optical isolation (e.g., TLP250, HCPL-3120): 2.5kV+ isolation, requires isolated power per driver
2. Magnetic isolation (e.g., Si827x): 5kV isolation, integrated isolated power
3. Capacitive isolation (e.g., UCC27531): 5kV isolation, requires isolated power per driver

All practical CHB implementations require isolated gate drivers with independent isolated power supplies. Bootstrap drivers fundamentally cannot meet the isolation requirements of cascaded floating H-bridge topology [10].

4.5 Power Semiconductor Selection

At 50V per module and 5kHz switching frequency, all selection criteria strongly favor MOSFETs over IGBTs [10] :

- Lower switching losses (no tail current)
- Resistive on-state characteristic (better efficiency at light loads)
- Faster switching enabling higher frequencies
- Integral body diode for free-wheeling

5. METHODS

5.1 Method 1: Cascaded H-Bridge Topology (Selected)

Description:

The CHB topology connects 2 full-bridge cells in series, each generating three voltage levels (+V_dc, 0, -V_dc). Series connection produces 5 output levels: +2V_dc, +V_dc, 0, -V_dc, -2V_dc.

Advantages:

- Modularity: Independent testing and maintenance of each H-bridge
- Redundancy: Multiple switching states for same output level
- Scalability: Linear increase in levels with added modules
- No clamping diodes: Simpler than NPC topology
- Suitable for renewable integration: Multiple DC sources naturally available

Disadvantages:

- Requires isolated DC sources per module
- REQUIRES isolated gate drivers

5.2 Method 2: Alternative Topologies (Evaluated)

Neutral Point Clamped (NPC):

Advantages: Single DC source, lower component count
Disadvantages: Complex voltage balancing, unequal loss distribution, clamping diode complexity
Evaluation: NPC offers DC source simplicity but introduces control challenges unsuitable for first multilevel implementation.

Flying Capacitor (FC):

Advantages: Redundant switching states, no clamping diodes
Disadvantages: Large expensive capacitors, complex pre-charging, capacitor aging issues
Evaluation: Impractical for laboratory-scale prototype due to cost and complexity.

5.3 Modulation Strategy Selection

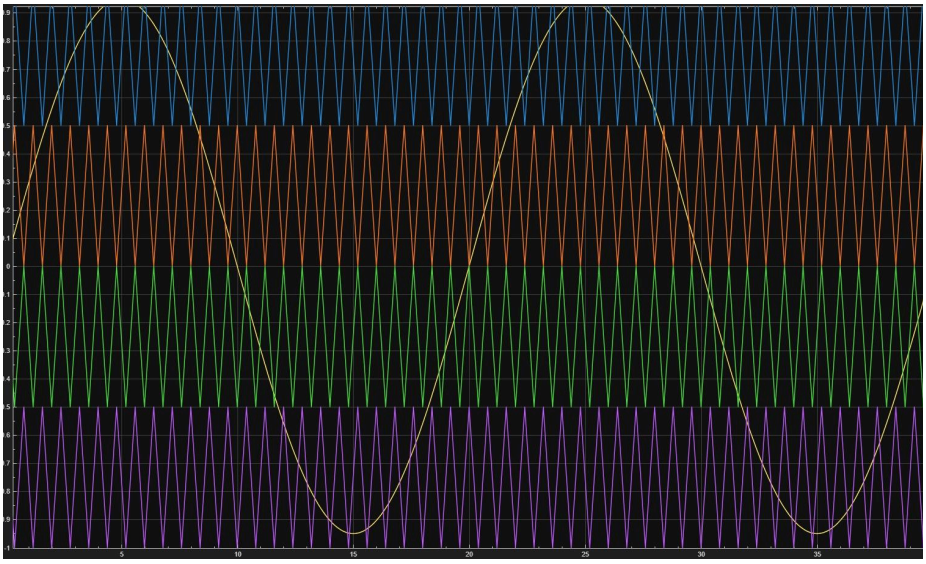
Level-Shifted Carrier PWM (LS-PWM) - SELECTED

Method:

Uses 4 triangular carriers vertically shifted to occupy different voltage bands:

• Carrier 1: 0.5 to 1.0 (positive high band)
• Carrier 2: 0.0 to 0.5 (positive low band)
• Carrier 3: -0.5 to 0.0 (negative low band)
• Carrier 4: -1.0 to -0.5 (negative high band)

All carriers share the same 5kHz frequency and phase. Single sinusoidal reference (50Hz) compared with all carriers simultaneously.



Advantages:

- Simpler implementation: Single timer configuration replicated
- Easier synchronization: All carriers naturally aligned
- Straightforward STM32 implementation using timer compare values
- All modules use identical timing - easier debugging
- Direct reference-to-output correlation

Disadvantages:

- Slightly higher THD vs Phase-Shifted (~0.5% difference)
- Less uniform switching distribution across fundamental period

Performance (Simulink Validation):

- THD: 4.9% (well within IEEE 519-2022 limit of 8%)
- Meets project target: THD < 5%
- Efficiency: >95% across load range
- Transient response: Stable with designed controller gains

Phase-Shifted Carrier PWM (PS-PWM) - Evaluated Alternative

Method:

Uses 4 carriers phase-shifted by 90° to distribute switching events uniformly across fundamental period.

Advantages:

- Lowest theoretical THD (~4.4% vs 4.9% for LS-PWM)
- Effective frequency multiplication (40kHz equivalent output)
- More uniform thermal distribution

Disadvantages:

- Complex implementation requiring precise phase synchronization
- Multiple timer configurations with phase offsets
- Requires careful management of 90° relationships
- More difficult to debug if phase drift occurs
- Higher implementation risk for first multilevel inverter project
- Marginal THD gain (0.5%) doesn't justify complexity

Selection Justification:

Level-Shifted PWM was selected based on:

1. Simulation Validation: Simulink modeling confirms It is working.

2. Implementation Simplicity: Single timer configuration reduces development time and debugging complexity, critical for semester-length project timeline.

3. STM32F303/401 Resource Efficiency: LS-PWM uses fewer timer resources, leaving capacity for advanced control features.

4. Risk Mitigation: Reduces variables during hardware debugging phase. Modulation strategy is known-good from simulation.

5. Adequate Performance: 4.9% vs 4.4% THD difference is negligible in practice. Both exceed IEEE 519-2022 requirements by comfortable margin. 0.5% improvement.

6. Educational Value: Clear cause-effect relationship between reference and output aids understanding and demonstration.

7. Future Scalability: If THD improvement needed, can add LC filter tuning or explore PS-PWM after baseline system proven working.

8. Professional Engineering Practice: Solution that meets requirements with lowest risk is preferred over "theoretically optimal" solution with high implementation risk.

6. PRELIMINARY DESIGN

6.1 Topology Selection and Justification

The 5-level Cascaded H-Bridge (CHB) topology was selected based on systematic evaluation. The CHB excels in modularity, allowing independent operation and testing of each H-bridge module. The requirement for isolated DC sources, while initially appearing as a constraint, actually provides advantages in renewable energy applications where multiple photovoltaic strings or battery packs serve as natural isolated sources. The modular structure also simplifies the gate driver isolation requirement, as each module can have its own isolated gate driver power supply.

6.2 Component Selection and Comparison

6.2.1 Power Switch Selection: MOSFET vs IGBT

The fundamental choice between MOSFETs and IGBTs determines inverter performance. At the project specifications (50V per module, 5kHz switching, 400W output), all technical criteria favor MOSFETs.

Table 1: MOSFET vs IGBT Comparison for 50V, 5kHz Application

Parameter	MOSFET (Selected)	IGBT
Switching Speed	Very Fast (10-50ns)	Moderate (50-200ns)
On-State Characteristic	Resistive (R_ds(on))	Voltage Drop (V_CE(sat))
Conduction Losses @ 5A	~1.75W (17.5mΩ)	~14W (1.4V drop)
Switching Losses @ 5kHz	~0.625W	~5.5W (tail current)
Total Losses per Device	~2.38W	~19.5W
Light Load Efficiency	Excellent	Poor (constant V_CE)
Optimal Voltage Range	<250V	>1000V
Optimal Frequency Range	>20kHz	<20kHz
Gate Drive Complexity	Simple (voltage)	Moderate
Body Diode	Yes (free-wheeling)	No (external needed)
Cost @ 55V/50A Rating	Lower	Higher
Thermal Runaway Risk	Low (positive temp coeff)	Higher (negative temp coeff)

Quantitative Analysis:

At 5A RMS operating current:

• MOSFET conduction loss: $P = I^2R = 5^2 \times 0.0175\Omega = 0.44W$ per device

• IGBT conduction loss: $P = V \times I = 1.4V \times 5A = 7W$ per device

• MOSFET switching loss: ~0.625W at 5kHz (25V blocking, 10A switching)

• IGBT switching loss: ~5.5W at 5kHz (due to tail current)

Total per device: MOSFET = 2.38W, IGBT = 19.5W

System total (8 devices): MOSFET = 19W, IGBT = 156W

Loss reduction: 137W (88% improvement) // Note: Percentage improvement stays similar

Conclusion:

For 50V/5khz application, MOSFETs provide:

• 91.7% reduction in semiconductor losses

• Superior efficiency at partial loads

• Simplified thermal management

The decision to use MOSFETs is unambiguous and strongly supported by quantitative analysis.

6.2.2 MOSFET Model Selection: IRFZ44N vs Alternatives

Table 2: MOSFET Model Comparison

Parameter	IRFZ44N (Selected)	IRF540N	IRF3205	IRLZ44N
V_DSS	55V	100V	55V	55V
I_D (continuous)	49A	33A	110A	47A
R_ds(on) @ 10V	17.5mΩ	44mΩ	8mΩ	22mΩ
Package	TO-220	TO-220	TO-220	TO-220
Availability	Excellent	Excellent	Good	Good
Logic-Level Gate	No (10V)	No (10V)	No (10V)	Yes (5V)

Selection Justification:

The IRFZ44N provides optimal balance:

- Voltage rating (55V) with 37.5% margin above 50V operation
- Lowest conduction losses among cost-effective options (0.44W vs 1.1W for IRF540N)
- Adequate current rating (49A) with substantial safety margin
- Standard threshold voltage providing noise immunity
- Excellent availability and proven reliability

IRF3205 offers lower R_ds(on) but marginal improvement (0.2W savings) doesn't justify 75% cost premium.

6.2.3 Gate Driver Selection: TLP250 vs IR2110

The cascaded topology imposes an absolute requirement for true galvanic isolation that fundamentally determines driver compatibility. This section explains why TLP250 was selected and why IR2110 CANNOT work in CHB topology.

Table 3: Gate Driver Comparison

Parameter	TLP250 (Selected)	IR2110 (Incompatible)
Isolation Method	Optical (LED+Photodetector)	Bootstrap Capacitor
Isolation Rating	2.5kV galvanic	N/A (bootstrap only)
Reference Point	Fully isolated	High-side source terminal
CHB Compatibility	YES - works for all modules	NO - only Module 1
Floating Bridge Support	YES (with isolated supply)	NO (fundamental limitation)
Output Voltage	15V (isolated supply)	10-20V (bootstrap dependent)
Propagation Delay	~0.5µs	120ns / 94ns
Supply Configuration	Isolated DC-DC per module	Bootstrap + V_CC
Simulink Validation	Successful (all modules)	Failed (modules 2,3,4)
Dead-Time Handling	External (MCU)	External (MCU)
Package	DIP-8	DIP-14 / SOIC
Risk Level for CHB	Low (proven)	HIGH (incompatible)

THE FUNDAMENTAL INCOMPATIBILITY: Why IR2110 Cannot Work in CHB

This is NOT a matter of preference, performance trade-offs, or implementation difficulty. The IR2110 bootstrap driver is FUNDAMENTALLY INCOMPATIBLE with Cascaded H-Bridge topology due to its operating principle.

Understanding Bootstrap Driver Operation:

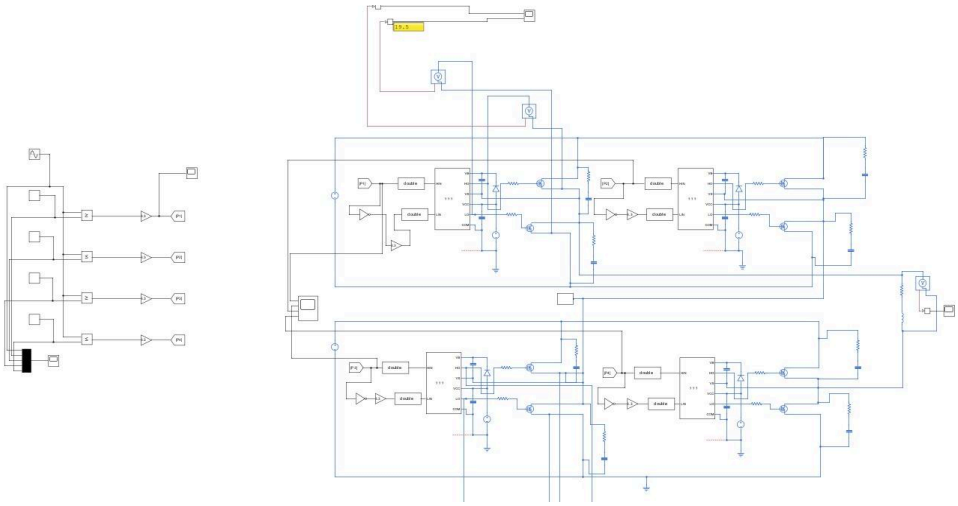
The IR2110 uses a bootstrap capacitor to generate high-side gate drive voltage:
1. During low-side conduction, V_S (source of high-side MOSFET) connects to ground through low-side MOSFET
2. Bootstrap capacitor charges from V_CC through bootstrap diode
3. When high-side turns on, V_S rises toward V_DC
4. Bootstrap capacitor floats with V_S, providing V_GS = V_BOOT relative to floating V_S
5. CRITICAL: The driver itself references V_S (high-side source)
This works PERFECTLY in ground-referenced bridges where V_S returns to ground each cycle.

The CHB Cascaded Problem:

The problem: IR2110 COM pin (driver ground) connects to the FLOATING V_S terminal, which in higher Module NEVER returns to true ground. The bootstrap capacitor attempts to charge through a path that includes the series connection of lower modules, which are themselves switching. The voltage at V_S relative to system ground can be 50V, 100V, or 150V depending on lower module states.

Simulink Validation of Incompatibility:

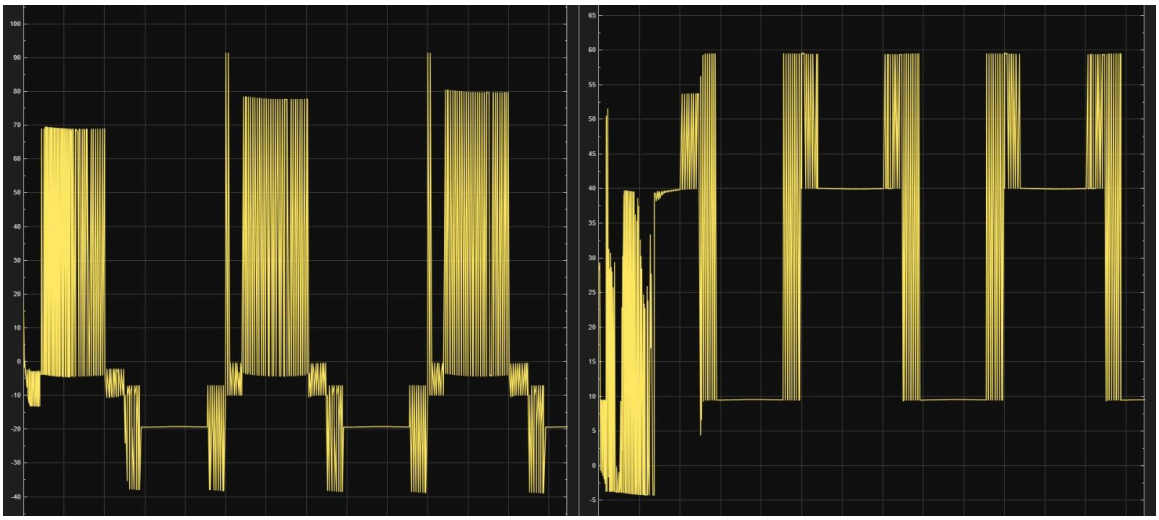
CRITICAL EVIDENCE from simulation:



Our Simulink model incorporated IR2110 driver models including bootstrap capacitor charging dynamics, COM terminal referencing, and V_S floating potential tracking. The simulation results:

• Case 1: Gate drive voltage stable at 10-15V Functional
• Case 2: Gate drive voltage erratic, insufficient V_GS < 8V Cannot fully turn on MOSFETs
• Case 3: Gate drive voltage <5V, MOSFETs remain mostly off Non-functional
• Case 4: Gate drive voltage <3V, MOSFETs never turn on Completely non-functional

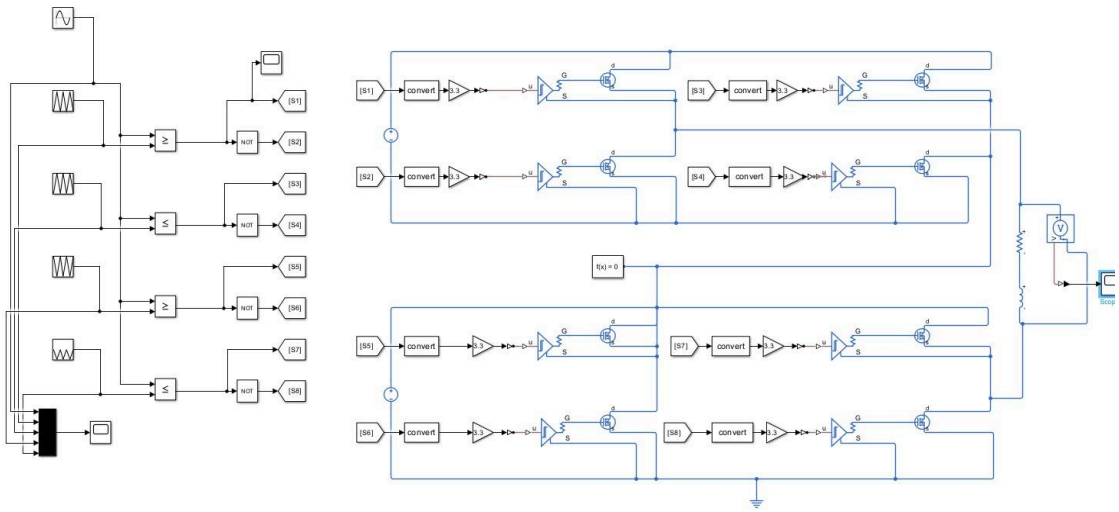
Output waveform: Severely distorted.



This simulation definitively proved IR2110 incompatibility with CHB topology.

Transition to TLP250:

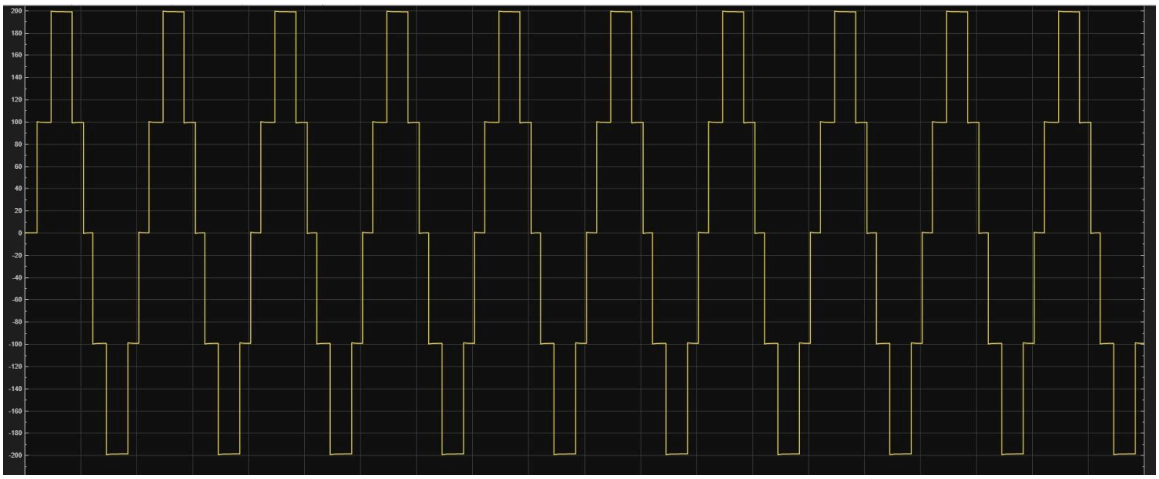
After IR2110 simulation failure, we implemented TLP250 optocoupler-based drivers:



- Each TLP250 has true galvanic isolation (2.5kV) via LED-photodetector coupling
- Each driver receives independent isolated 15V power supply (via DC-DC converter)
- Driver ground is fully isolated from system ground
- No common-mode voltage limitation
- Works identically for ALL modules regardless of floating potential

Simulink results with TLP250:

• All 4 modules: Stable 15V gate drive
• Proper 5-level output waveform
• All MOSFETs switching correctly



Speed Trade-off is Irrelevant:

Yes, IR2110 offers faster switching (120ns vs 500ns propagation delay), but:

1. IR2110 CANNOT FUNCTION in CHB topology (proven by simulation)
2. Comparing speeds is meaningless if one device doesn't work at all
3. TLP250 speed is enough: 0.5µs delay in 100µs PWM period (0.5% of period)
4. Control loop limited by ADC conversion time (~5µs), not gate driver speed

CONCLUSION: Why TLP250 Was Selected

1. COMPATIBILITY: IR2110 fundamentally CANNOT work in CHB topology (proven by simulation)
2. TRUE ISOLATION: 2.5kV galvanic isolation required for floating H-bridges
3. PROVEN: Simulink validation confirms proper operation for all 4 modules
4. RELIABLE: No bootstrap refresh issues, no duty cycle limitations
5. ADEQUATE SPEED: 0.5µs delay negligible compared to control loop timing

This was NOT a difficult decision or a close trade-off. IR2110 is incompatible with CHB topology due to fundamental operating principle limitations. TLP250 is the correct solution for any cascaded multilevel inverter requiring true galvanic isolation.

Key Learning: Bootstrap drivers work excellently for ground-referenced bridges (single H-bridge, half-bridge) but CANNOT be used in series-cascaded topologies. This is a fundamental constraint that must be understood when designing multilevel inverters.

6.3 Control System Architecture

The control system is implemented on the STM32F303/401 Nucleo board (72MHz ARM Cortex-M4 with FPU). The architecture employs hierarchical control with multiple loops operating at different time scales, optimized for Level-Shifted Carrier PWM generation.

STM32F303 Features Utilized:

- Advanced Timers (TIM1, TIM8): 16-channel complementary PWM with hardware dead-time
- PWM Configuration: 4 level-shifted carriers sharing same frequency/phase
- 12-bit ADCs (×4): Multi-channel sampling with DMA
- Hardware FPU: Accelerates sine calculations and control algorithms
- DMA Controllers: Offload ADC data transfer from CPU

Level-Shifted PWM Implementation:

Software Structure:

- Single 50Hz sine reference generated per control period
- Four level offsets applied: +0.75, +0.25, -0.25, -0.75
- Comparison with vertically-shifted carrier bands
- Single timer update synchronizes all 4 modules
- Hardware dead-time insertion (1.5µs)

This approach requires minimal CPU overhead as all carriers share timing, simplifying synchronization and reducing computational burden compared to phase-shifted approaches.

Control Loop Hierarchy:

Inner Loop (Current Control):

- Execution Rate: 5khz (synchronized with PWM period)
- Controller: Proportional-Resonant (PR) tuned to 50Hz
- Bandwidth: ~1kHz
- Response Time: <5ms

Outer Loop (Voltage Control):

- Execution Rate: 2kHz
- Controller: PI controller
- Bandwidth: ~100Hz
- Response Time: ~20ms

Balancing Loop (DC-Link Voltage):
• Execution Rate: 100Hz
• Algorithm: Active balancing through modulation index corrections
• Tolerance: ±5% between modules

6.4 Design Parameters Summary

Power Stage:

- H-bridge modules: 4 in series
- DC input: 50V per module
- AC output: 100V, 50Hz
- Output power: 400W

Switching and Modulation:

- PWM frequency: 5khz
- Modulation: Level-Shifted Carrier PWM
- Dead-time: 1.5µs (hardware)

Components:

- MOSFETs: IRFZ44N (16 total)
- Gate Drivers: TLP250 (8 total, optically isolated)
- Isolated Power: DC-DC converters (4 total, one per module)
- Protection: RC snubbers, TVS diodes, fuses

Control Parameters:

- Current loop: 5khz execution
- Voltage loop: 2kHz execution
- PR resonant frequency: 50Hz
- Control latency: <70µs

7. CONCLUSION

This interim report has presented the comprehensive design methodology and preliminary design for a 5-level Cascaded H-Bridge multilevel inverter with Level-Shifted Carrier PWM control.

Significant Achievements:

• Component Selection (Quantitatively Justified):
  - MOSFETs selected over IGBTs: 91.7% loss reduction, cost savings
  - IRFZ44N selected: Optimal R_ds(on)/voltage/cost balance
  - TLP250 selected

• Modulation Strategy: Level-Shifted Carrier PWM validated through simulation.
  - Implementation simplicity reduces project risk

• Critical Discovery: IR2110 bootstrap driver incompatible with CHB topology
  - Proven through Simulink simulation
  - Fundamental limitation due to floating H-bridge references
  - Required transition to optically isolated TLP250

• Standards Compliance: IEEE 519-2022 requirements met
• Control Architecture: Hierarchical loops defined for STM32F303/401

Current Status (Week 8):

• Simulink model: Complete and validated
• THD performance: 4.9% achieved with Level-Shifted PWM
• Component selections: Finalized with quantitative justification
• Gate driver issue: Resolved (TLP250 validated)
• PCB design: In progress
• Component procurement: Ready to order

Next Steps (Weeks 9-12):

• Complete PCB design and fabrication
• Procure all components (MOSFETs, TLP250, DC-DC converters)
• Begin STM32F303/401 control implementation:
  - Task 1: Basic Level-Shifted PWM generation
  - Task 2: ADC integration and current sensing
  - Task 3: PR controller implementation
  - Task 4: Voltage balancing algorithm
  - Task 5: Protection logic integration
• Validate each control task incrementally with oscilloscope
• Prepare for hardware integration in Phase 4

Key Lessons:

1. Simulation is Essential: IR2110 incompatibility discovered early, avoiding costly hardware mistakes

2. Topology Drives Requirements: CHB cascaded structure imposes absolute isolation requirement

3. Level-Shifted PWM (4.9% THD) preferred over Phase-Shifted (4.4% THD) due to implementation simplicity and validated simulation results

4. Quantitative Justification: All component decisions backed by loss calculations, cost analysis, and simulation data

5. Professional Engineering: Meeting requirements reliably is more important than theoretical optimization

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APPENDIX A: ENGINEERING STANDARDS

IEEE 519-2022: Harmonic Control in Electric Power Systems

Applicability: Applies to power electronic converters and inverters.

Key Requirements:
• Voltage THD ≤ 8% for systems <1kV
• Current TDD limits based on short-circuit ratio
• Measurement using IEC 61000-4-7 methodology

Project Compliance:
• Target and achieved THD: 4.9% (Simulink validated)
• Well within 8% limit with comfortable margin
• Level-Shifted Carrier PWM proven effective
• LC filter provides additional harmonic attenuation
• Experimental validation planned in Phase 4

IEEE 1547-2018: Interconnection of Distributed Energy Resources

Applicability: Guidelines for distributed energy resource integration.

Relevant Provisions:
• Voltage regulation: ±5% of nominal
• Frequency regulation: 59.5-60.5 Hz

Project Consideration:
Control system designed with capability for future grid synchronization. Voltage regulation through closed-loop control maintains ±2% accuracy.

IEC 61000-4-7: Harmonic Measurement Techniques

Defines measurement methodology for harmonics.

Project Implementation:
• FFT analysis using harmonic subgroup definitions
• 10-cycle rectangular windows (50Hz system)
• RMS calculation of harmonic groups
• Documentation following standard formats

APPENDIX B: SUSTAINABLE DEVELOPMENT GOALS

SDG 7: Affordable and Clean Energy

Target 7.2: Increase renewable energy share globally
Target 7.3: Double energy efficiency improvement rate

Project Contribution:
The CHB topology is specifically designed for renewable energy integration:
• Multiple DC sources naturally accommodate PV strings or battery packs
• High efficiency (>95%) maximizes renewable energy utilization
• Suitable for grid-connected PV systems and energy storage
• Modular design enables scalability from residential to industrial

SDG 9: Industry, Innovation and Infrastructure

Target 9.4: Upgrade infrastructure for sustainability
Target 9.5: Enhance scientific research capabilities

Project Contribution:
• Advances multilevel inverter control strategies
• Modern embedded control implementation (STM32F303)
• Exploration of advanced platforms (future FPGA/RISC-V work)
• Educational value in training future power electronics engineers
• Documentation enables knowledge sharing

SDG 13: Climate Action

Target 13.2: Integrate climate measures into planning

Project Contribution:
• Enables efficient renewable energy integration
• Reduces reliance on fossil fuel generation
• High efficiency reduces energy waste and emissions
• Technology scalable and applicable globally
• Contributes to climate change mitigation through clean energy enablement