NVIDIA JETSON TX1 AND JETSON TX2 INTERFACE COMPARISON AND MIGRATION

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Application Note

DOCUMENT CHANGE HISTORY

DA-08408-001_v1.1

Version	Date	Description of Change
1.0	May 1, 2017	Initial Release
1.1	June 1, 2017	Added SDIO section with details related to SDIO support on Jetson TX1 versus Jetson TX2

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INTRODUCTION

This application note compares the features and interfaces supported on the NVIDIA® Jetson™ TX1 and Jetson TX2 modules. This application note also describes the migration path for designers intending to design a carrier board that will support both, with either the same common functionality or be able to take advantage of the features supported on only one or the other module.

Note: Jetson TX2 utilizes NVIDIA® Tegra® X2 which is a Parker series SoC.

JETSON TX1 VS JETSON TX2

The Jetson TX1 and Jetson TX2 modules are pin compatible, but there are some differences to note when designing a new carrier board if both modules are to be supported.

The following figures show the Jetson TX1 and Jetson TX2 block diagrams. The interfaces that are supported only by one of the modules are highlighted in red. These block diagrams depict the connections used on the NVIDIA Jetson TX1 Developer Kit carrier board, and not all module differences are shown. All the significant interface differences will be described later in this application note.

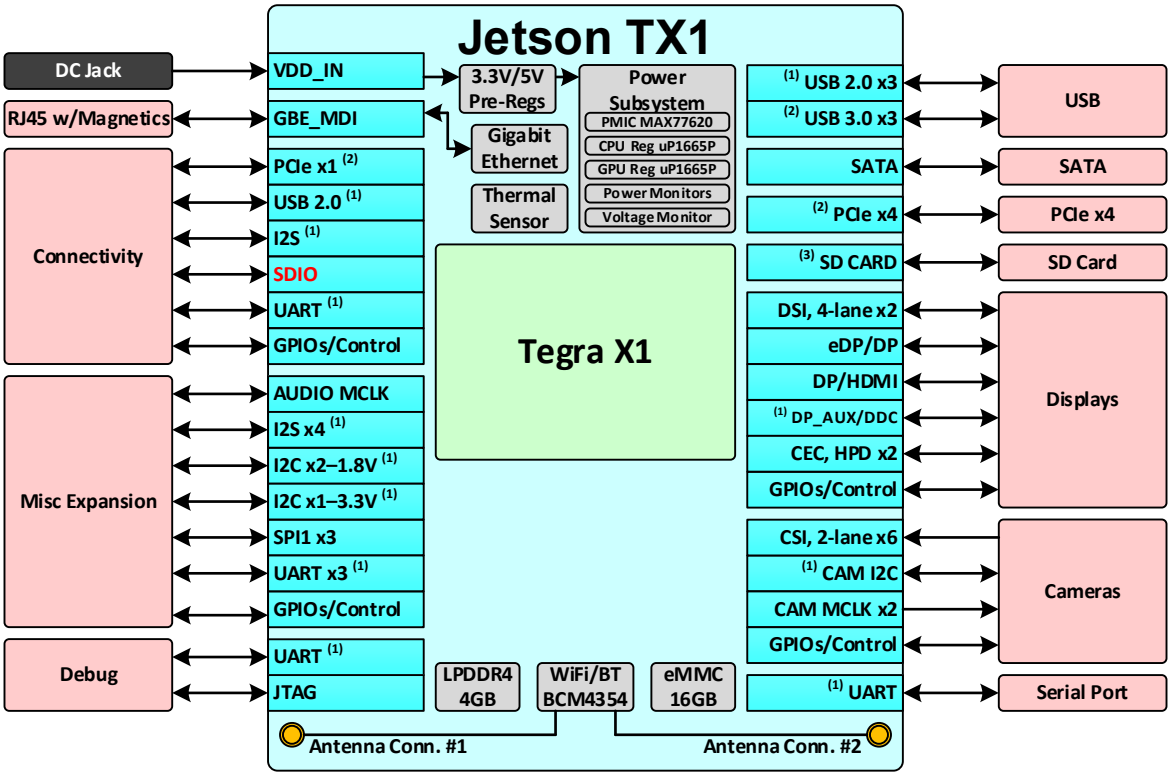

Figure 1. Jetson TX1 Block Diagram

Notes:

1. Some interfaces are shown in multiple locations. There are a total of 4x I2S, 6x I2C (including DP_AUX/DDC and CAM_I2C), 3x UART, and 3x USB 2.0.
2. USB 3.0, PCIe, and SATA share lanes. Not all instances shown in Figure 1 can be brought out together. See the USB 3.0, PCIe, and SATA lane mapping configuration tables in the “USB 3.0, PCIe, and SATA Mapping” section.
3. If SDCARD pins are not used for the SD card, they can be used for an additional SDIO interface.

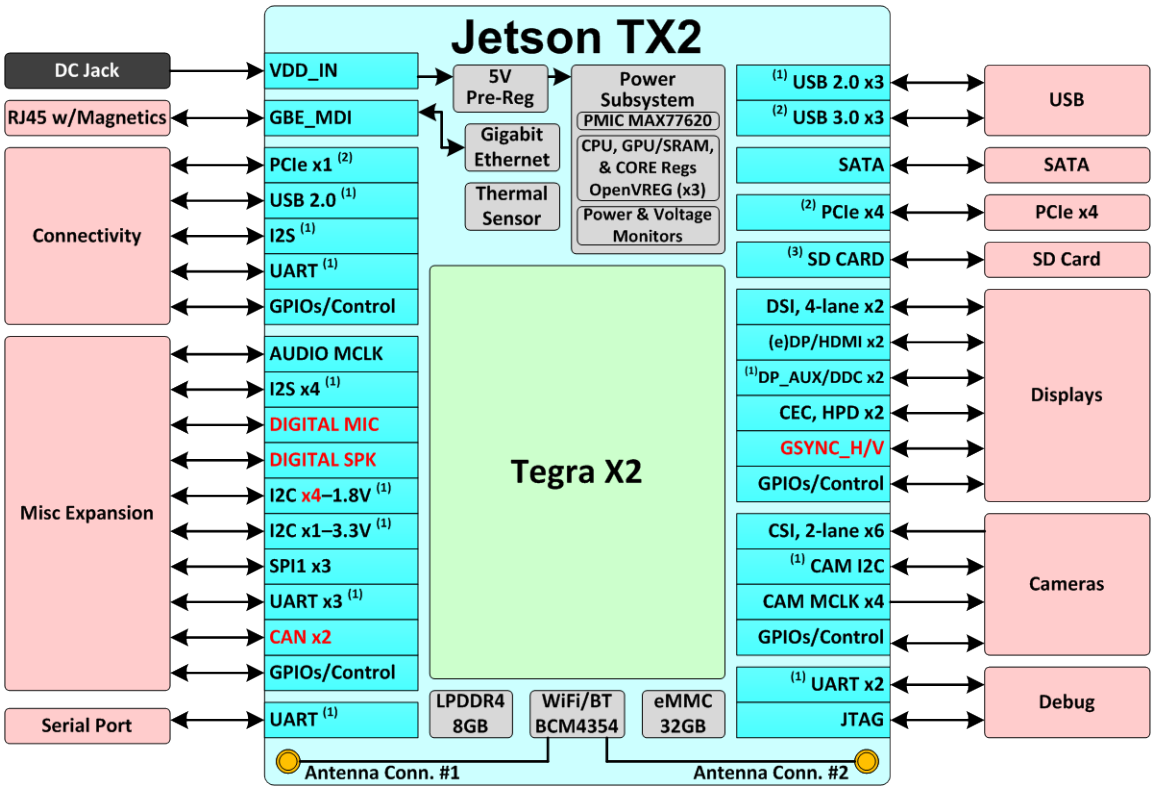

Figure 2. Jetson TX2 Block Diagram

Notes:

1. Some interfaces are shown in multiple locations. There are a total of 4x I2S, 8x I2C (including DP_AUX/DDC and CAM_I2C), 5x UART, and 3x USB 2.0.
2. USB 3.0 and PCIe share lanes. Not all instances shown in Figure 2 can be brought out together. See the USB 3.0, PCIe, and SATA lane mapping configuration tables in the "USB 3.0, PCIe, and SATA Mapping" section.
3. If SDCARD pins are not used for the SD card, they can be used for an additional SDIO interface.

MODULE INTERFACE COMPARISONS

Table 1 lists the various interfaces that are supported on either the Jetson TX1 or the Jetson TX2 module. In some cases, an interface is only supported on one or the other. While in other cases, there is some difference between the levels of support.

Table 1. Interfaces Brought to Module Connector

Interface	Sub-Category	Jetson TX1	Jetson TX2
USB (see Note 1)	2.0 PHY	3x	
	3.0 PHY	Up to 3x	
PCIe (see Note 1)		1x4 + 1x1	Up to 1x4 + 1x1 or 2x1 +1x2
SATA (see Note 1)		Yes	Yes (with DEV_SLP)
Camera	CSI	CSI (6 x2 or 3 x4)	
	MCLK	2x	4x
Display	eDP/DP/HDMI™	2x (HDMI on DP1 only)	2x (Symmetrical – eDP/DP/HDMI on either)
	DP_AUX/DDC	2x	
	DSI	2 x4	2 x4 (with split link)
	Tearing effect	Supported	
	Backlight PWM	1x	2x
	GYNSC_HSYNC/VSYNC	Not available	Supported
Audio	I2S	4x	
	MCLK	Supported	
	Digital Mic	Not available	Supported
	Digital speaker	Not available	Supported
SDMMC		SD card + SDIO	SD card or SDIO
Gigabit Ethernet		Supported	
I2C (see Note 2)		6x	8x

Interface	Sub-Category	Jetson TX1	Jetson TX2
UART		3x (4-pin)	4x (4-pin, 1x (2-pin)
SPI		3x	
CAN		Not available	2x
Fan		PWM and Tach	

Notes:

1. See the USB 3.0, PCIe and SATA interface mapping comparison tables for details on lane sharing.
2. Including DP_AUX/DDC and CAM_I2C.

Table 2 (included in the OEM product design guides for both Jetson TX1 and Jetson TX2), shows the main module connector pinout with pin and interface differences highlighted.

Table 2. Module Connector (8x50) Pinout Matrix

	A	B	C	D	E	F	G	H
1	VDD_IN	VDD_IN	VDD_IN	RSVD	FORCE_RECOV#	AUDIO_MCLK	I2S0_SDIN	I2S0_LRCLK
2	VDD_IN	VDD_IN	VDD_IN	RSVD	SLEEP#	GPIO19_AUD_RST	I2S0_CLK	I2S0_SDOUT
3	GND	GND	GND	RSVD	SPI0_CLK	SPI0_CS0#	GND	GPIO20_AUD_INT
4	GND	GND	GND	RSVD	SPI0_MISO	SPI0_MOSI	DSPK_OUT_CLK	DSPK_OUT_DAT
5	RSVD	RSVD	RSVD	UART7_RX	I2S3_SDIN	I2S3_LRCLK	I2S2_CLK	I2S2_LRCLK
6	I2C_PM_CLK	I2C_PM_DAT	I2C_CAM_CLK	I2C_CAM_DAT	I2S3_CLK	I2S3_SDOUT	I2S2_SDIN	I2S2_SDOUT
7	CHARGING#	CARRIER_STBY#	BATLOW#	GPIO5_CAM_ FLASH_EN	CAM2_MCLK	GPIO1_CAM1_ PWR#	GPIO4_CAM_ STROBE	GPIO3_CAM1_ RST#
8	GPIO14_AP_WAKE _MDM	VIN_PWR_BAD#	BATT_OC	UART7_TX	CAM_VSYNC	CAM1_MCLK	GPIO0_CAM0_ PWR#	GPIO2_CAM0_ RST#
9	GPIO15_AP2MDM_ READY	GPIO17_MDM2AP_ READY	WDT_TIME_OUT	UART1_TX	UART1_RTS#	CAM0_MCLK	UART3_CTS#	UART3_RX
10	GPIO16_MDM_ WAKE_AP	GPIO18_MDM_ COLDBOOT	I2C_GP2_DAT	UART1_RX	UART1_CTS#	GND	UART3_RTS#	UART3_TX
11	JTAG_GP1	JTAG_TCK	I2C_GP2_CLK	RSVD	RSVD	RSVD	UART0_RTS#	UART0_CTS#
12	JTAG_TMS	JTAG_TDI	I2C_GP3_CLK	RSVD	RSVD	RSVD	UART0_RX	UART0_TX
13	JTAG_TDO	JTAG_GP0	I2C_GP3_DAT	I2S1_LRCLK	SPI1_CS1#	SPI1_MOSI	SPI1_CLK	GPIO8_ALS_PROX_ INT
14	JTAG_RTCK	GND	I2S1_SDIN	I2S1_SDOUT	SPI1_CS0#	SPI1_MISO	GPIO9_MOTION_IN T	SPI2_CLK
15	UART2_CTS#	UART2_RX	I2S1_CLK	I2C_GP0_DAT	I2C_GP0_CLK	GND	SPI2_MOSI	SPI2_MISO
16	UART2_RTS#	UART2_TX	FAN_PWM	AO_DMIC_IN_DAT	AO_DMIC_IN_CLK	SPI2_CS1#	SPI2_CS0#	SDCARD_PWR_EN
17	USB0_EN_OC#	FAN_TACH	CAN1_STBY	CAN1_RX	RSVD	SDCARD_CD#	GND	SDCARD_D1
18	USB1_EN_OC#	RSVD	CAN1_TX	CAN0_RX	CAN0_ERR	SDCARD_D3	SDCARD_CLK	SDCARD_D0
19	RSVD	GPIO11_AP_WAKE _BT	CAN1_ERR	CAN0_TX	GND	SDCARD_D2	SDCARD_CMD	GND
20	I2C_GP1_DAT	GPIO10_WIFI_ WAKE_AP	CAN_WAKE	GND	CSI5_D1-	SDCARD_WP	GND	CSI4_D1-
21	I2C_GP1_CLK	GPIO12_BT_EN	GND	CSI5_CLK-	CSI5_D1+	GND	CSI4_CLK-	CSI4_D1+
22	GPIO_EXP1_INT	GPIO13_BT_WAKE _AP	CSI5_D0-	CSI5_CLK+	GND	CSI4_D0-	CSI4_CLK+	GND
23	GPIO_EXP0_INT	GPIO7_TOUCH_ RST	CSI5_D0+	GND	CSI3_D1-	CSI4_D0+	GND	CSI2_D1-
24	LCD1_BKLT1_PWM	TOUCH_CLK	GND	CSI3_CLK-	CSI3_D1+	GND	CSI2_CLK-	CSI2_D1+
25	LCD_TE	GPIO6_TOUCH_ INT	CSI3_D0-	CSI3_CLK+	GND	CSI2_D0-	CSI2_CLK+	GND
26	GSYNC_HSYNC	LCD_VDD_EN	CSI3_D0+	GND	CSI1_D1-	CSI2_D0+	GND	CSI0_D1-
27	GSYNC_VSYNC	LCD0_BKLT_PWM	GND	CSI1_CLK-	CSI1_D1+	GND	CSI0_CLK-	CSI0_D1+
28	GND	LCD_BKLT_EN	CSI1_D0-	CSI1_CLK+	GND	CSI0_D0-	CSI0_CLK+	GND
29	SDIO_RST#	SDIO_CMD	CSI1_D0+	GND	DSI3_D1+	CSI0_D0+	GND	DSI2_D1+
30	SDIO_D3	SDIO_CLK	GND	DSI3_CLK+	DSI3_D1-	GND	DSI2_CLK+	DSI2_D1-

	A	B	C	D	E	F	G	H
31	SDIO_D2	GND	DSI3_D0+	DSI3_CLK-	GND	DSI2_D0+	DSI2_CLK-	GND
32	SDIO_D1	SDIO_D0	DSI3_D0-	GND	DSI1_D1+	DSI2_D0-	GND	DSI0_D1+
33	DP1_HPD	HDMI_CEC	GND	DSI1_CLK+	DSI1_D1-	GND	DSI0_CLK+	DSI0_D1-
34	DP1_AUX_CH-	DP0_AUX_CH-	DSI1_D0+	DSI1_CLK-	GND	DSI0_D0+	DSI0_CLK-	GND
35	DP1_AUX_CH+	DP0_AUX_CH+	DSI1_D0-	GND	DP1_TX3-	DSI0_D0-	GND	DP0_TX3-
36	USB0_OTG_ID	DP0_HPD	GND	DP1_TX2-	DP1_TX3+	GND	DP0_TX2-	DP0_TX3+
37	GND	USB0_VBUS_DET	DP1_TX1-	DP1_TX2+	GND	DP0_TX1-	DP0_TX2+	GND
38	USB1_D+	GND	DP1_TX1+	GND	DP1_TX0-	DP0_TX1+	GND	DP0_TX0-
39	USB1_D-	USB0_D+	GND	PEX_RFU_TX+	DP1_TX0+	GND	PEX_RFU_RX+	DP0_TX0+
40	GND	USB0_D-	PEX2_TX+	PEX_RFU_TX	GND	PEX2_RX+	PEX_RFU_RX-	GND
41	PEX2_REFCLK+	GND	PEX2_TX-	GND	PEX1_TX+	PEX2_RX-	GND	PEX1_RX+
42	PEX2_REFCLK -	USB2_D+	GND	USB_SS1_TX+	PEX1_TX-	GND	USB_SS1_RX+	PEX1_RX-
43	GND	USB2_D-	USB_SS0_TX+	USB_SS1_TX-	GND	USB_SS0_RX+	USB_SS1_RX-	GND
44	PEX0_REFCLK+	GND	USB_SS0_TX-	GND	PEX0_TX+	USB_SS0_RX-	GND	PEX0_RX+
45	PEX0_REFCLK-	PEX1_REFCLK+	GND	SATA_TX+	PEX0_TX-	GND	SATA_RX+	PEX0_RX-
46	RESET_OUT#	PEX1_REFCLK-	PEX2_CLKREQ#	SATA_TX-	GND	GBE_LINK1000#	SATA_RX-	GND
47	RESET_IN#	GND	PEX1_CLKREQ#	SATA_DEV_SLP	GBE_LINK_ACT#	GBE_MDI1+	GND	GBE_MDI3+
48	CARRIER_PWR_ON	RSVD	PEX0_CLKREQ#	PEX_WAKE#	GBE_MDI0+	GBE_MDI1-	GBE_MDI2+	GBE_MDI3-
49	CHARGER_PRSNT#	RSVD	PEX0_RST#	PEX2_RST#	GBE_MDI0-	GND	GBE_MDI2-	GND
50	VDD_RTC	POWER_BTN#	RSVD	RSVD	PEX1_RST#	GBE_LINK100#	GND	RSVD

Legend	Ground	Power	Not available (RSVD) on Jetson TX1	Not available (RSVD) on Jetson TX2	Reserved

Note: RSVD (Reserved) pins on the module must be left unconnected.

INTERFACE DIFFERENCE DETAILS

USB 3.0, PCI EXPRESS, AND SATA MAPPING

The following tables show the different options for mapping USB 3.0, PCIe, and SATA to the common set of interface pins. Jetson TX2 has an additional PCIe controller and an on-module mux that selects either one of the Tegra X2 PCIe lanes or USB 3.0. Table 5 shows the configurations that can be supported on both modules with a single carrier board.

Table 3. Jetson TX1 USB 3.0, PCIe, and SATA Lane Mapping Configurations

	Jetson TX1 Pin Names			PEX1	PEX_RFU	PEX2	USB_SS1	PEX0	USB_SS0	na	SATA
	Tegra X1 Lanes			Lane 0	Lane 1	Lane 2	Lane 3	Lane 4	Lane 5	Lane 6	SATA
	Avail. IFs on Jetson TX1										
Configs	USB 3.0	PCIe	SATA								
1(CB Default)	1	1x1 + 1x4	1	PCIe#1_0	PCIe#0_3	PCIe#0_2	PCIe#0_1	PCIe#0_0	USB_SS#1	USB_SS#0 On-Jetson TX1	SATA
2	2	1x1 + 1x4	0	PCIe#1_0	PCIe#0_3	PCIe#0_2	PCIe#0_1	PCIe#0_0	USB_SS#1		USB_SS#3
3	2	1x4	1	USB_SS#2	PCIe#0_3	PCIe#0_2	PCIe#0_1	PCIe#0_0	USB_SS#1	For Gigabit Ethernet	SATA
4	2	2x1	1	PCIe#1_0			USB_SS#2	PCIe#0_0	USB_SS#1		SATA
5	3	2x1	0	PCIe#1_0			USB_SS#2	PCIe#0_0	USB_SS#1		USB_SS#3
Default Usage on Carrier Board				M.2 Conn.	X4 PCIe Connector				USB 3.0 Type A	Ethernet	SATA

Table 4. Jetson TX2 USB 3.0, PCIe, and SATA Lane Mapping Configurations

	Jetson TX2 Pin Names			PEX1	PEX_RFU	PEX2	USB_SS1	PEX0	USB_SS0	SATA
	Tegra X2 Lanes			Lane 0	Lane 1	Lane 3	Lane 2	Lane 4		Lane 5
	Avail. IFs on Jetson TX2									
Configs	USB 3.0	PCIe	SATA							
1	0	1x1 + 1x4	1	PCIe#2_0	PCIe#0_3	PCIe#0_2	PCIe#0_1	PCIe#0_0		SATA
2 (CB Default)	1	1x4	1		PCIe#0_3	PCIe#0_2	PCIe#0_1	PCIe#0_0	USB_SS#0	SATA
3	2	3x1	1	PCIe#2_0	USB_SS#1	PCIe#1_0	USB_SS#2	PCIe#0_0		SATA
4	3	2x1	1		USB_SS#1	PCIe#1_0	USB_SS#2	PCIe#0_0	USB_SS#0	SATA
5	1	2x1 + 1x2	1	PCIe#2_0	USB_SS#1	PCIe#1_0	PCIe#0_1	PCIe#0_0		SATA
6	2	1x1 + 1x2	1		USB_SS#1	PCIe#1_0	PCIe#0_1	PCIe#0_0	USB_SS#0	SATA
Default Usage on CB (carrier board)				Unused	X4 PCIe Connector				USB 3.0 Type A	SATA

Note: PCIe Controller #2 can be brought to the PEX1 pins, or USB 3.0 Controller #1 can be brought to the USB_SS0 pins on Jetson Tx2 depending on the setting of the multiplexer on the module. The selection is controlled by QSPI_IO2 configured as a GPIO.

Table 5. Jetson TX1 and Jetson TX2 Compatible USB 3.0, PCIe, and SATA Lane Mapping Configurations

	Module Pin Names			PEX1	PEX_RFU	PEX2	USB_SS1	PEX0	USB_SS0		SATA
	Avail. Outputs from Module										
Configs	USB 3.0	PCIe	SATA								
A	0	1x1 + 1x4	1	PCIe x1	PCIe x4 L3	PCIex4 L2	PCIex4 L1	PCIex4 L0			SATA
B	1	1x4	1		PCIe x4 L3	PCIex4 L2	PCIex4 L1	PCIex4 L0	USB_SS (1)		SATA
C	1	2x1	1	PCIe x1			USB_SS (2)	PCIex4 L0			SATA
D	2	1x1	1				USB_SS (2)	PCIex4 L0	USB_SS (1)		SATA
Default Usage on Carrier Board				Unused	X4 PCIe Connector				USB SS		SATA

PCI EXPRESS

There are a number of differences between the two modules for PCIe support. Jetson TX1 has two PCIe controllers and can support 1 x1 lane + up to 1 x4 lane configuration. Jetson TX2 has three controllers and can support the same options as Jetson TX1, but can also support up to 2 x1 + 1 x2 configuration. Jetson TX2 has a multiplexer on the module that selects whether the Tegra X2 lane is directed to PEX1 for PCIe Controller #2 (x1) or to USB_SS0 for USB 3.0. On Jetson TX1, these are independent. If the carrier board must support both Jetson TX1 and Jetson TX2, the configurations should come from the "Jetson TX1 and Jetson TX2 Module Compatible USB 3.0, PCIe, and SATA Lane Mapping Configurations" table.

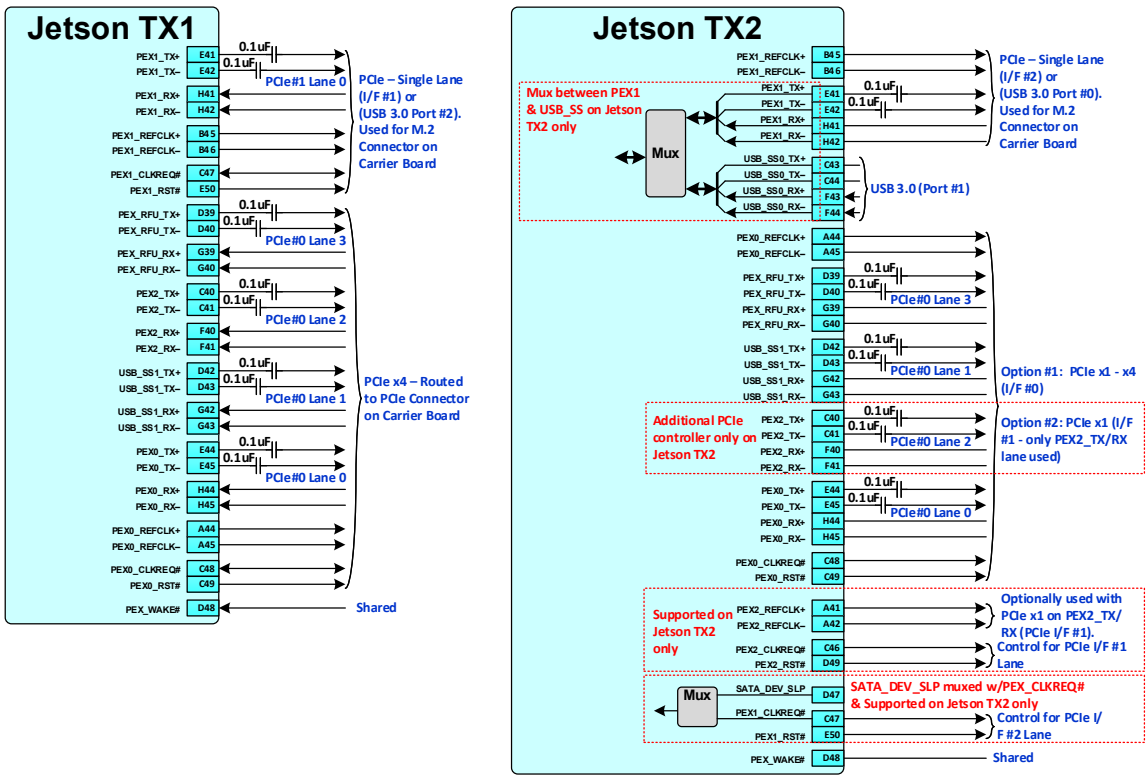

Figure 3. Jetson TX1 and Jetson TX2 PCIe Block Diagram

SATA

Support for SATA is the same for Jetson TX1 and Jetson TX2 except that Jetson TX2 can optionally bring out the SATA Device Sleep function as shown in the following. This function is multiplexed with PEX1_CLKREQ#, so only one or the other can be used in a design.

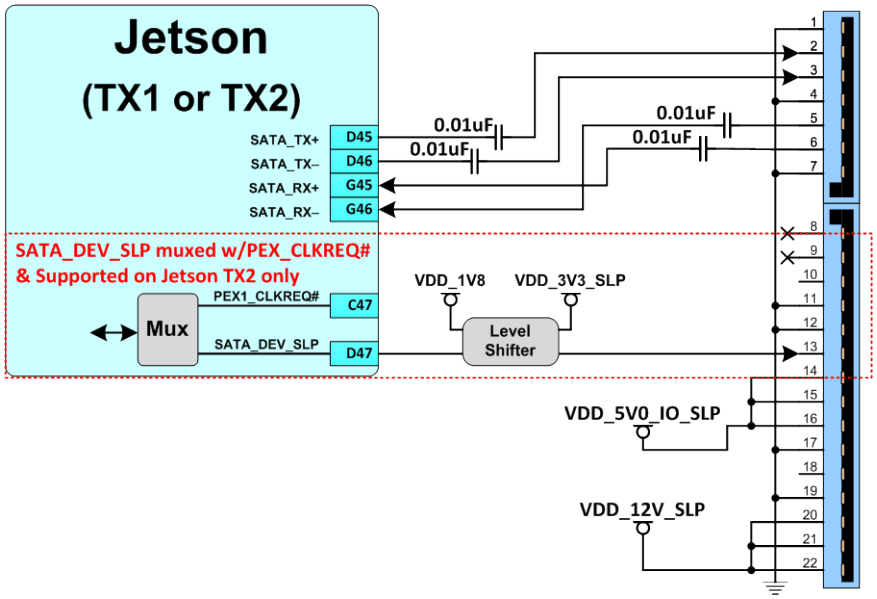

Figure 4. Jetson TX1 and Jetson TX2 SATA Support

DISPLAY

DSI

Jetson TX1 and Jetson TX2 both support up to a dual-link DSI configuration which includes two sets of four data lanes, each with a clock lane. The first set uses DSI0 clock and DSI0 and DSI1 data lanes (2+2). The second set uses DSI2 clock and DSI2 and DSI3 data lanes (2+2). Jetson TX2 also supports a split-link configuration where there are 4 sets of 2 data lanes, each with a clock lane.

Figure 5. DSI Configuration

eDP/DP/HDMI

Both Jetson TX1 and Jetson TX2 can support eDP, DP, and HDMI™ displays. Jetson TX1 limits the support for HDMI to the DP1 pins. The DP1 pins can also support eDP/DP. The DP0 pins can support only support eDP/DP. On Jetson TX2, the DP0 and DP1 pins can be used for any of these interfaces (eDP/DP/HDMI).

General

Jetson TX1 supports a single PWM for display backlight use (LCD0_BKLT_PWM). Jetson TX2 adds support for a second PWM (LCD1_BKLT_PWM). In addition, Jetson TX2 supports GSYNC_HSYNC/VSYNC functionality on the GSYNC_HSYNC (A26) and GSYNC_VSYNC (A27) pins.

CAMERA

The same number of CSI data lanes (12 total) and possible cameras (6 x2 or 3 x4) are supported on both Jetson TX1 and Jetson TX2. Jetson TX2 adds the option to bring out two additional MCLKs (master reference clocks). One is available on CAM2_MCLK and the other on GPIO1_CAM1_PWR#. In addition, a CAM_VSYNC function is supported on Jetson TX2 only.

SDIO

Jetson TX1 brings Tegra X1 SDMMC interfaces to both the SDCARD and SDIO pins of the module and uses USB/PCIe as the interface to the on-module Ethernet Controller. Jetson TX2 uses an SDMMC (as EQOS) interface for Ethernet, so does not bring an SDMMC interface to the SDIO pins of the module. Jetson TX2 can support SDIO, but would have to use the SDCARD pins instead.

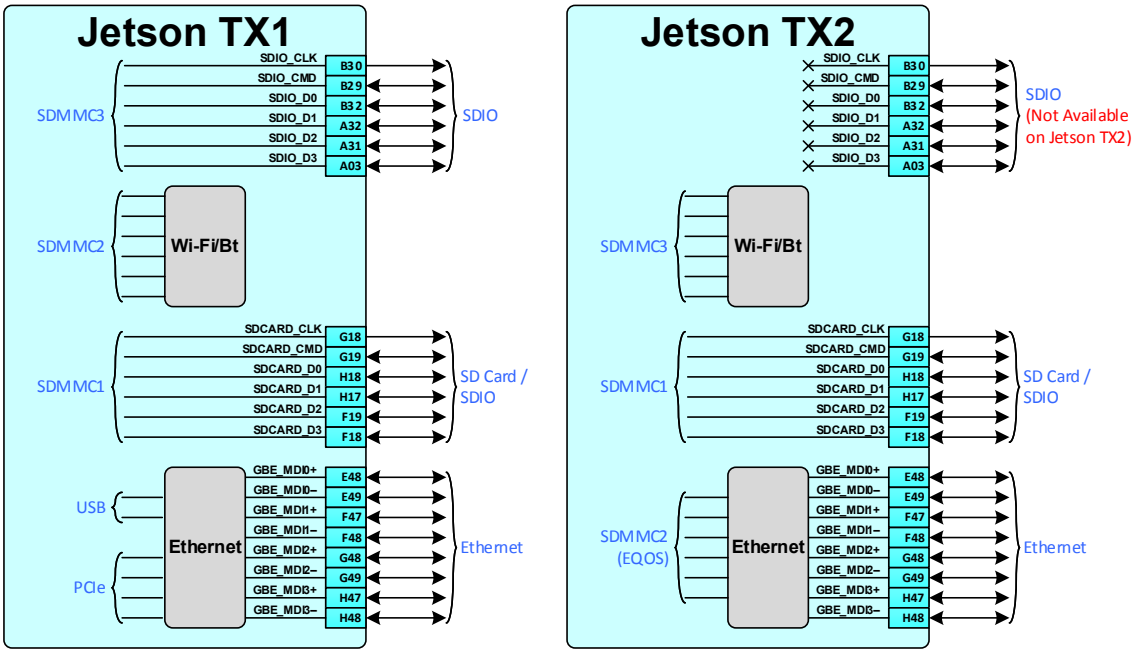

Figure 6. SDIO Support

AUDIO

Both Jetson TX1 and Jetson TX2 support four I2S interfaces (I2S[3:0]) as well as an Audio MCLK and GPIOs for Reset and Interrupt. Jetson TX2 also supports both a digital microphone interface (AO_DMIC_IN_CLK/DAT) and digital speaker interface (DSPK_OUT_CLK/DAT).

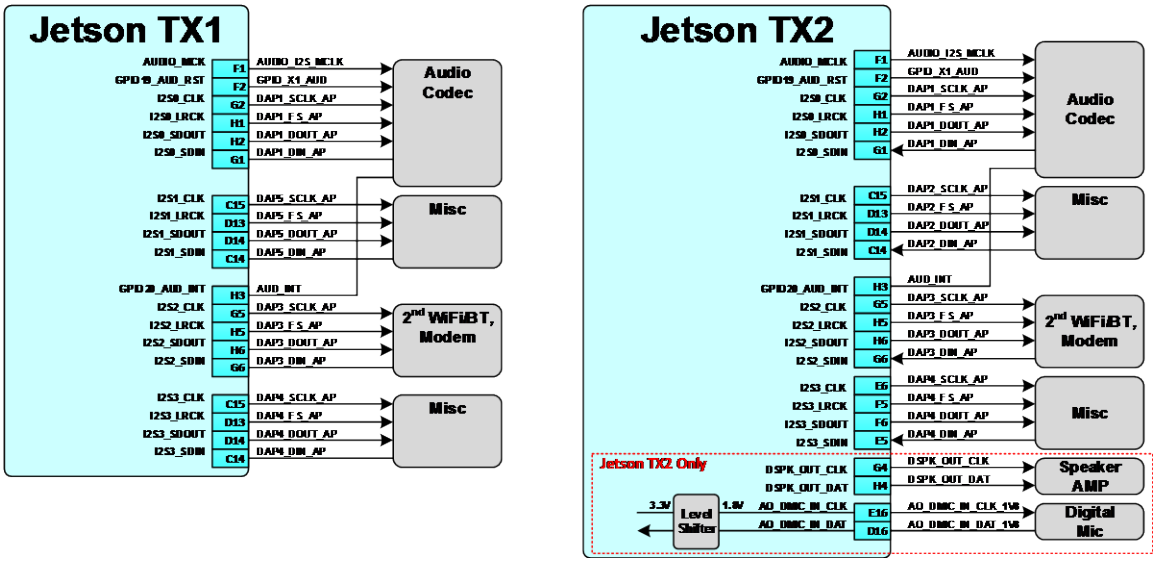

Figure 7. Audio Support

CONTROLLED AREA NETWORK FOR JETSON TX2 ONLY

Jetson TX2 supports two controlled area network (CAN) interfaces. Jetson TX1 does not support this interface.

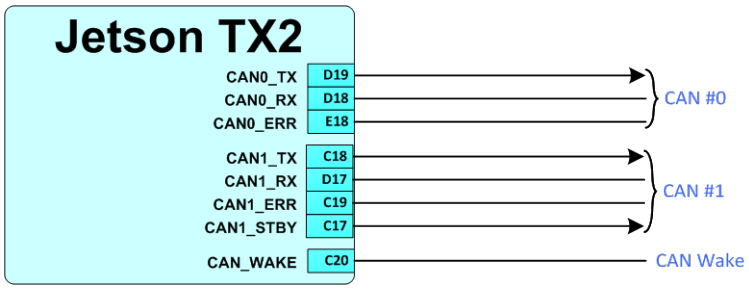

Figure 8. Jetson TX2 CAN Interface Support

I2C

Jetson TX2 has two additional I2C interfaces available at the module pins. These are I2C_GP[3:2].

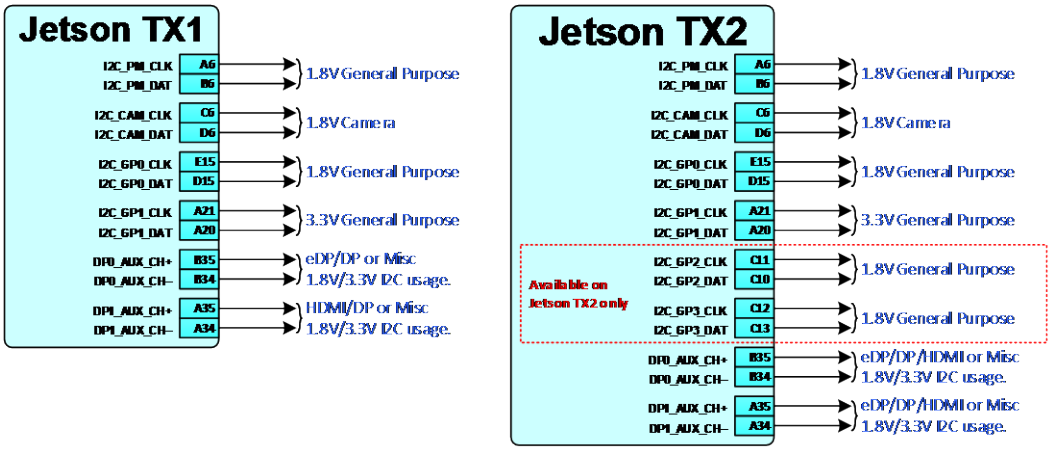

Figure 9. I2C Interface Support

UART

In addition to bringing UART[2:0] out on the module pins, Jetson TX2 also provides an option to bring out UART3. This is multiplexed with the on-module WLAN/BT, so if this is being used, UART3 will not be available. A 2-pin UART (UART7) is also available on RSVD Pin D8 and Pin D5 on Jetson TX2.

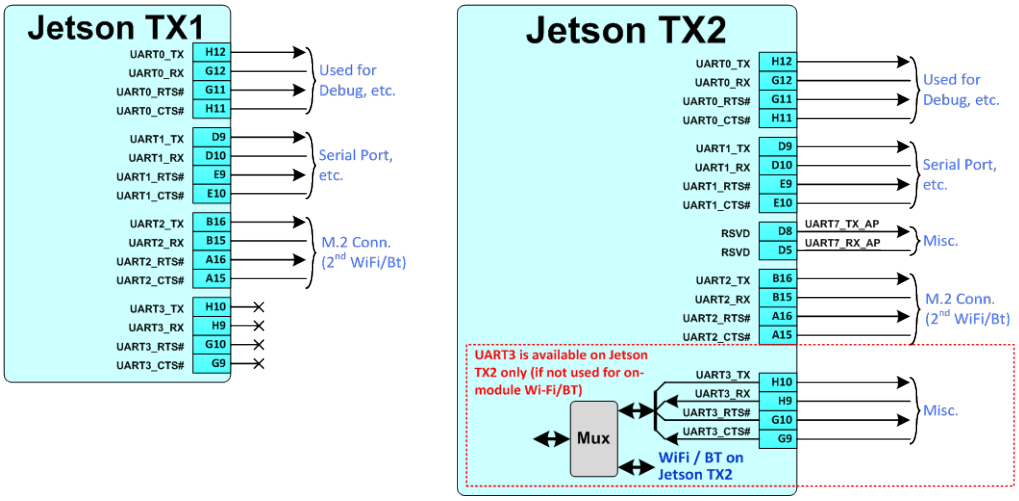

Figure 10. UART Support

DEBUG

Jetson TX1 and Jetson TX2 both support JTAG and assign UART0 for the debug UART. Jetson TX2 adds another UART (UART7_TX/RX) on the reserved pins D8/D5. Jetson TX1 and Jetson TX2 differ in the way the JTAG_GP[1:0] pins are used.

- For Jetson TX1, JTAG_GP0 is left unconnected (pull-down on module) for normal operation or when using JTAG for debug purposes. The pin is pulled high to support Boundary Scan test mode. The TRST_N pin on the JTAG connector is left unconnected. JTAG_GP1 is not used and left unconnected.
- For Jetson TX2, JTAG_GP0 can be connected to the JTAG connector TRST_N pin and a pull-up should be provided as shown in Figure 10. JTAG GP1 is left unconnected (pull-down on module) for normal/debug modes, or pulled to 1.8V to support Boundary Scan test mode.

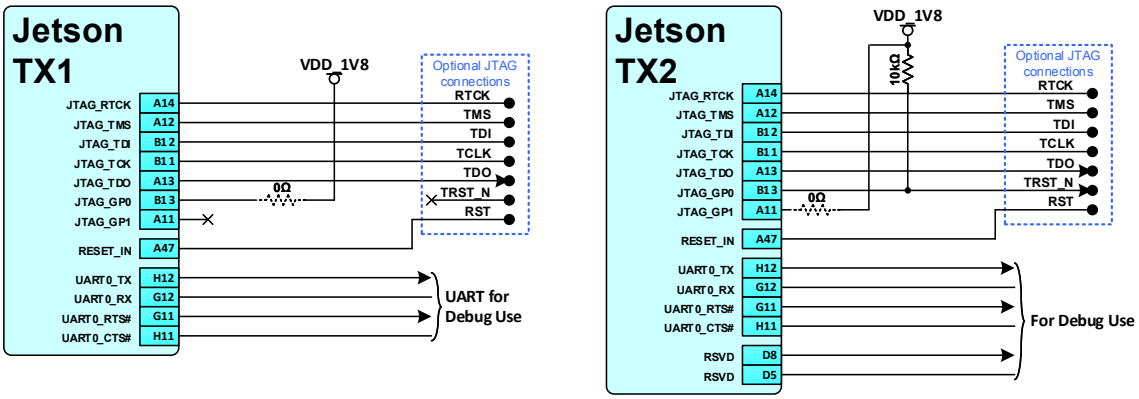

Figure 11. Debug Support Differences

STRAPPING

The actual strapping on the modules cannot be altered, but some of the strapping involves module pins. These pins must be handled carefully so that the strapping selections are not affected. The strapping bits are set at power-on when the Tegra X1 or Tegra X2 reset is released. Check the Jetson TX1 and Jetson TX2 OEM product design guides (“Strapping” section) for details on how the pins involved in strapping should be handled. The following figure shows the affected module pins.

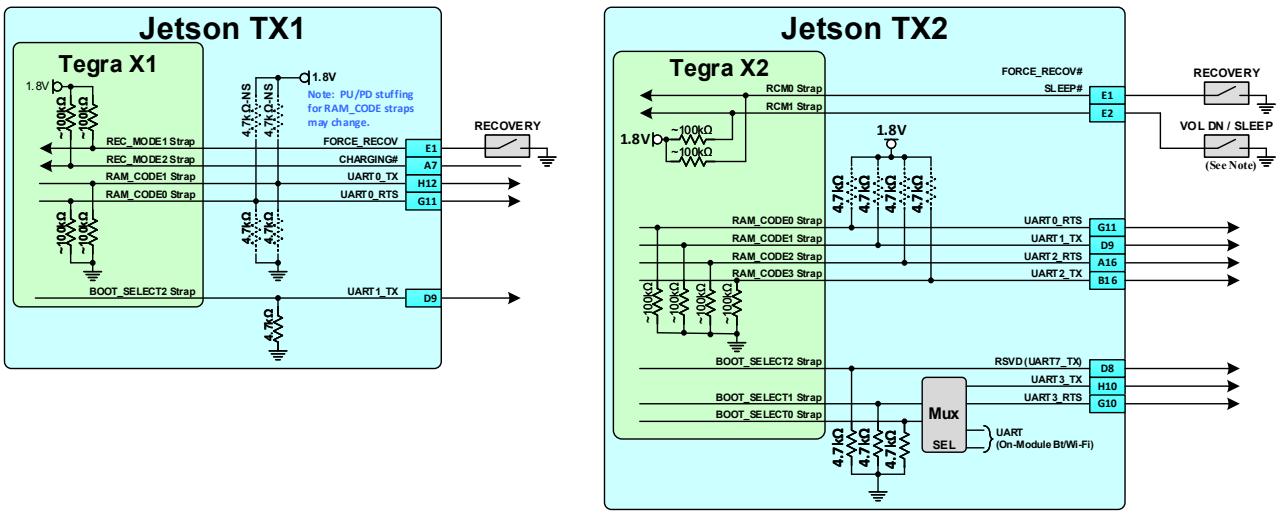

Figure 12. Strapping Pins on the Modules

MISCELLANEOUS

SPI1_CS1#

Pin E13 (SPI1_CS1#) on the main module connector, is supported on Jetson TX1 only. Jetson TX2 does not route a signal to that pin. On Jetson TX2, the pin is reserved. SPI1_CS1# is routed to Pin 26 on the expansion header (J21). When Jetson TX2 is used, Pin 26 will not connect to a signal on Tegra X2.

WDT_TIME_OUT#

Jetson TX2 supports a Watch-dog Timer Time-out function on the WDT_TIME_OUT# pin. This was not supported on Jetson TX1.

BATT_OC Pin Functionality

Jetson TX2 supports BATT_OC functionality on Pin C8 of the module, although the schematic symbol shows Pin C8 as RSVD. This pin is connected to the output of the on-module power monitor for the VDD_IN, CPU and DDR power rails. This pin is reserved on Jetson TX1.

Auto-Power-On

Jetson TX2 includes Auto-Power-On circuitry. This allows the platform to power on when the main power supply is connected to the carrier board without pressing the power button. This circuit is enabled by tying the CHARGER_PRSNT# pin to GND. On the Developer Kit carrier board (P2597) this can be done by installing the 0Ω R313 near the charger control header (J27).

Jetson TX1 does not include this circuitry. To support Auto-Power-On with Jetson TX1, see the "Optional Auto-Power-On Support" section in the *Jetson TX1 OEM Product Design Guide*. One of the options shown can be implemented on a custom carrier board.

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