COURSE REVIEW

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K17-501F

Overview

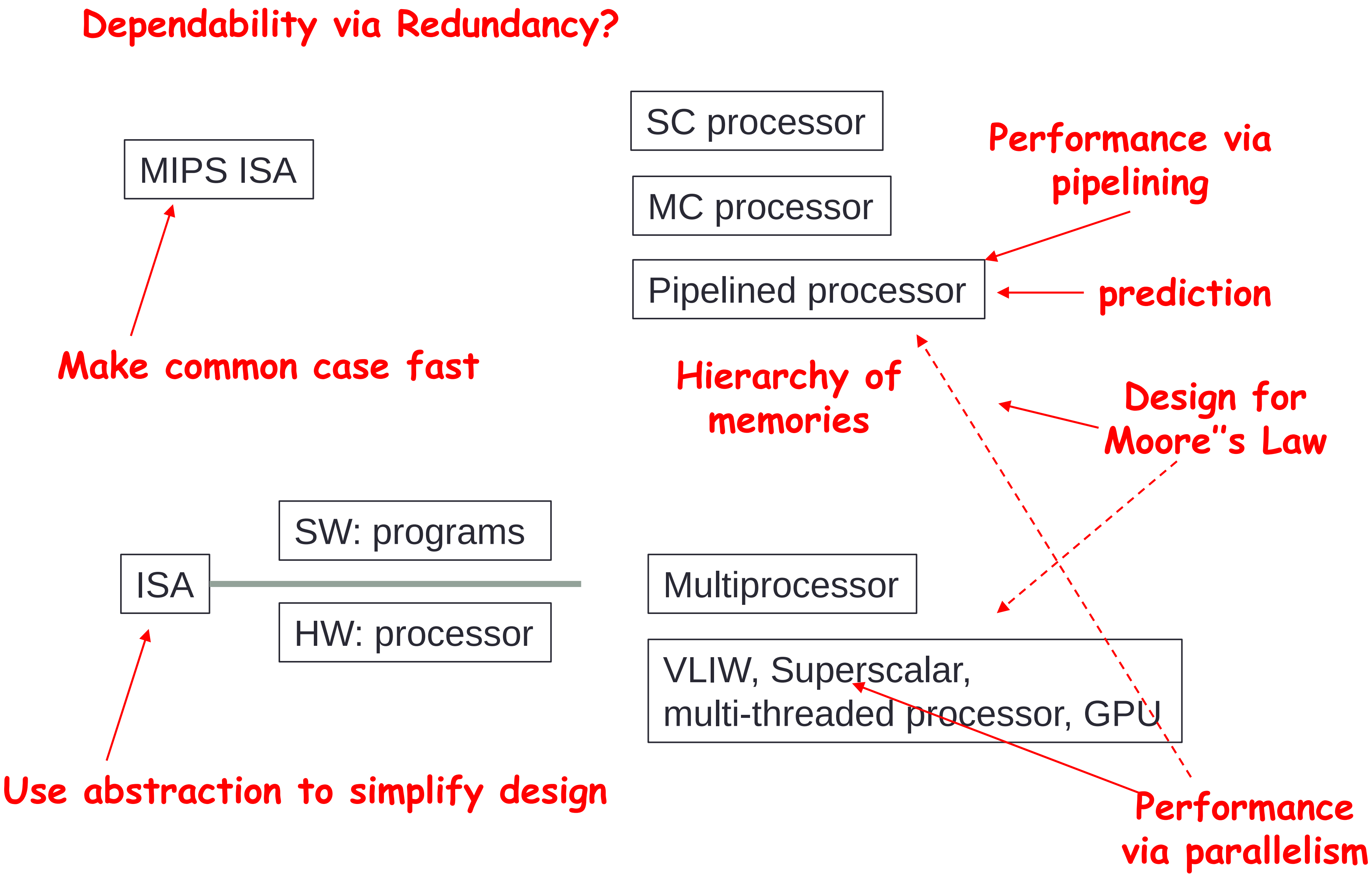
- **What have we learned in this course?**
  - **Design ideas in computer architecture**
  - **Techniques for hardware implementation**
  - **How to communicate our designs to fellow students**
- **What can we do after completing this course?**

Eight great ideas

The integrated circuit resources double every 18-24 months.

- **Design for Moor’s Law**
- **Use abstraction to simplify design**
- **Make the common case fast**
- **Performance via parallelism**
- **Performance via pipelining**
- **Performance via prediction**
- **Hierarchy of memories**
- **Dependency via redundancy**

Design ideas



Dependability via Redundancy?

MIPS ISA

Make common case fast

SC processor

MC processor

Pipelined processor

Performance via pipelining

prediction

Hierarchy of memories

Design for Moore"s Law

SW: programs

ISA

HW: processor

Use abstraction to simplify design

Multiprocessor

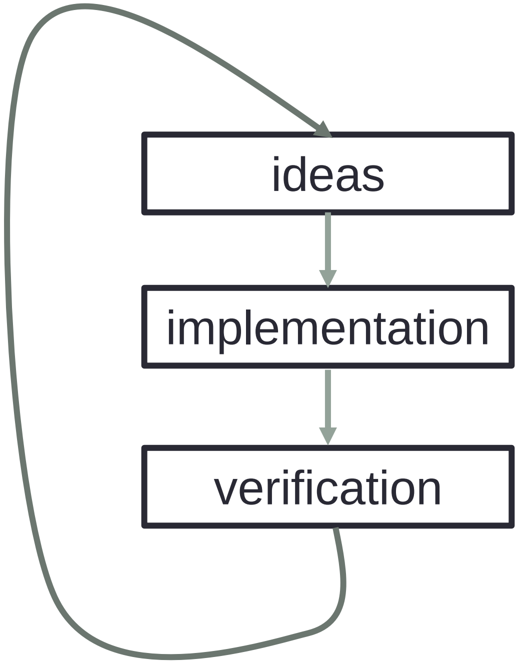
VLIW, Superscalar, multi-threaded processor, GPU

Performance via parallelism

Implementation

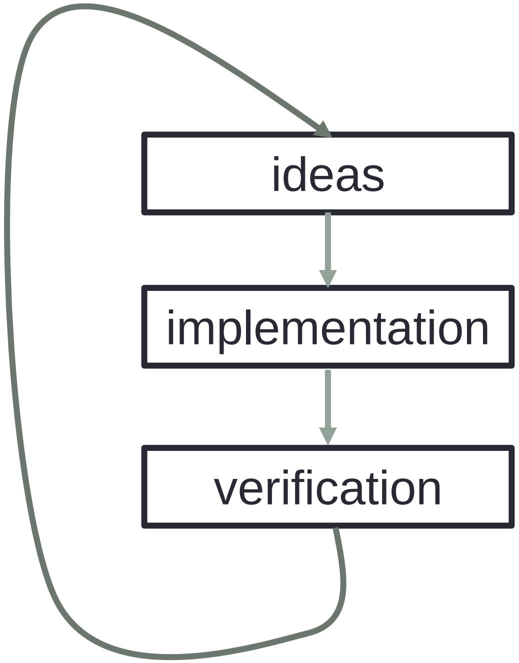
- Following an iterative process
- Each iteration
  - ideas → more concrete
  - implementation → more technical
- Typical solutions
  - design principles?
    - for ISA
    - for processor
    - for memory hierarchy

    - for performance improvement
    - for power consumption
  - techniques?



Verification

- **Analytical**
- **Simulation**
- **Prototype**



Communication

- Communicate your design
  - To your team members
  - To class members
- Via lab presentation
  - Learn from each other
  - Get quick feedback
  - Enhance presentation skills
- Via group project
  - What is your experience now?

What can we do after completing this course?

- Be able to explain
  - How a processor is created
  - When and why we need to use memory hierarchy
  - How a hierarchical memory system is designed and used
  - How a parallel processing hardware design can achieve high performance
- Be able to design a simple processor system
- Be able to investigate and validate a hardware design using simulation

What can we do after completing this course? (cont.)

- Be able to capture the hardware design features and make good use of them at different SW design levels
    - E.g. at the assembly level
- Design custom processors
    - Embedded systems
    - Application Specific Instruction-set processors
- And more
    - Research and innovations
    - Contributions to new design areas

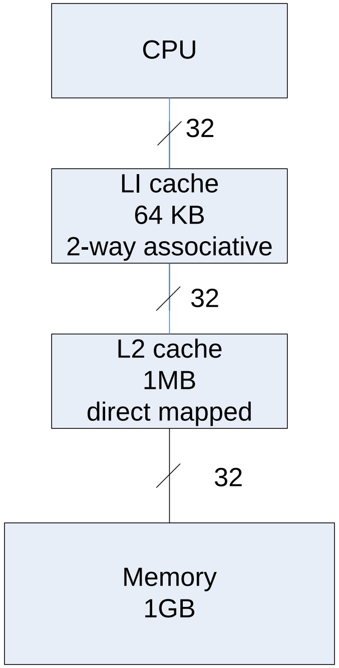
Example 1

To improve the performance, a compiler makes the following change. What are the possible reasons?

```
/* before */
for (j=0; j <20; j++)
     for (i=0; i <200; i++)
           a[i][j] = a[i][j] + 1;

/* after */
for (i=0; i<200; i++)
     for (j=0; j <20; j++)
           a[i][j] = a[i][j] + 1;
```

Example 2

- ***The inclusion property*** **is commonly required by the multi-level cache design. For example, for a two-level cache L1 and L2, the property requires that if a memory block is in the L1 cache, then it must also be in the L2 cache. Figure 2 shows a system with a two-level cache. Does this design hold the inclusion property? Why?**



About final exam

- Exam type
  - Moodle online exam
- Time: Sat, 1st May
- Duration:
  - 2 hours
- Exam open time:
  - 14:00 (Sydney time)
- Exam close time:
  - 17:00 (Sydney time)

About final exam (cont.)

- Covers materials discussed in Weeks 1-9
  - Mainly focus on first 8 weeks
  - For Week 9, understanding at the conceptual level is sufficient
- Number of questions:
  - Four multiple choice questions (20 marks)
  - Seven Short Answer questions (80 marks)
    - May consist of sub questions
- Question style
  - Similar to the quiz questions

About final exam (cont.)

- **All questions use the Moodle essay format**
  - **Including MC questions**
  - **You can either write your answer in the text box (preferred) or upload your answer file**
  - **For each question, you are allowed to explain your solution or show your working**
    - **Text editing and graph drawing tools may be helpful**
    - **Photocopies of hand-writing and drawing are also acceptable**

About final exam (cont.)

- Question types
  - Descriptive questions
  - Concept related questions
  - Quantitative questions
  - Design related questions

Example questions

Descriptive questions

1. What is the forwarding unit used for in a processor? Please briefly describe its operational function. (5 marks)

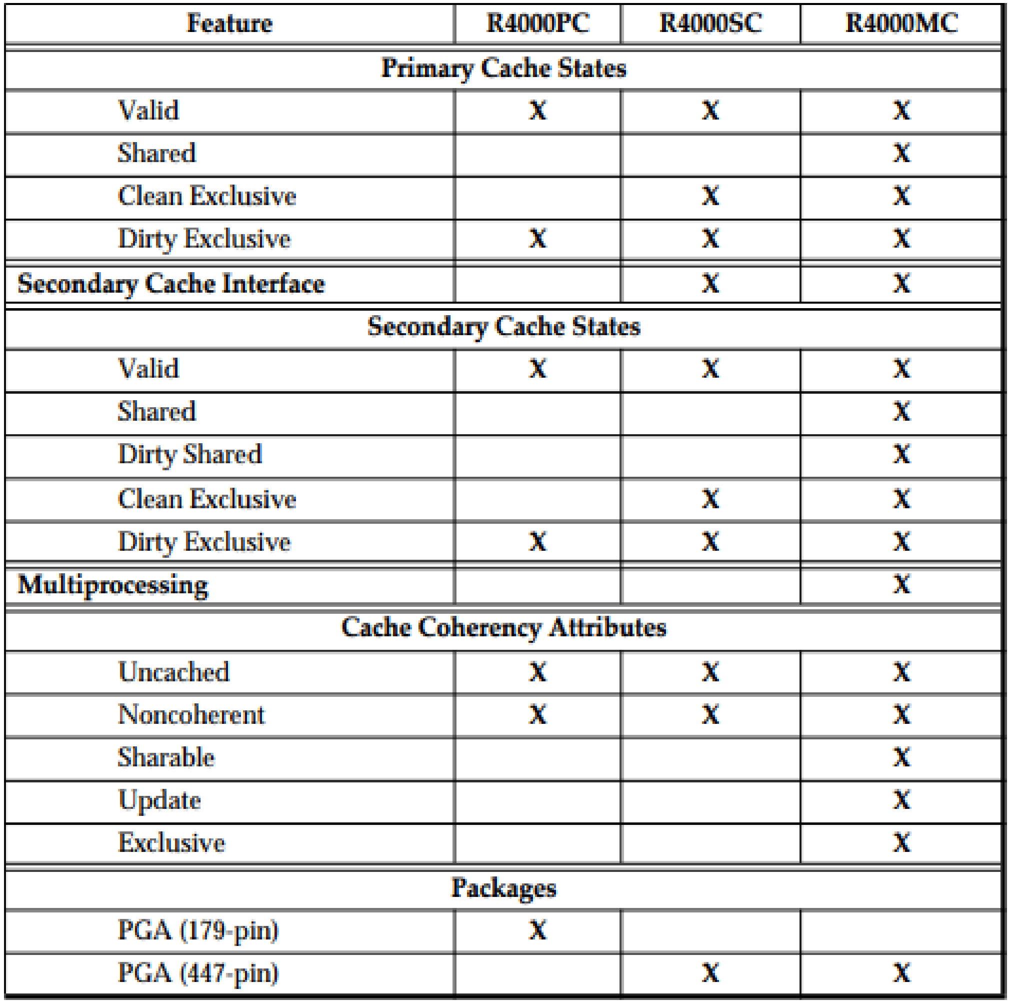
2. What are the two main issues in the shared-memory multiprocessor design? (3 marks)

Example questions

Concept related questions

1. The table below lists the cache design features included by three different MIPS processors, where clean is used to indicates a clean cache copy and dirty is used to indicate a modified cache copy. What write policy does R4000SC likely use for the primary cache? Please explain. (6 marks)

Table 1-1 R4000 Features



Feature	R4000PC	R4000SC	R4000MC
Primary Cache States			
Valid	X	X	X
Shared			X
Clean Exclusive		X	X
Dirty Exclusive	X	X	X
Secondary Cache Interface		X	X
Secondary Cache States			
Valid	X	X	X
Shared			X
Dirty Shared			X
Clean Exclusive		X	X
Dirty Exclusive	X	X	X
Multiprocessing			X
Cache Coherency Attributes			
Uncached	X	X	X
Noncoherent	X	X	X
Sharable			X
Update			X
Exclusive			X
Packages			
PGA (179-pin)	X		
PGA (447-pin)		X	X

Example Questions

Concept related question

2. Why might a compiler perform the following optimizations? Please explain. Here assume the matrix is stored in the memory in the row-major order (i.e row after row) (6 marks)

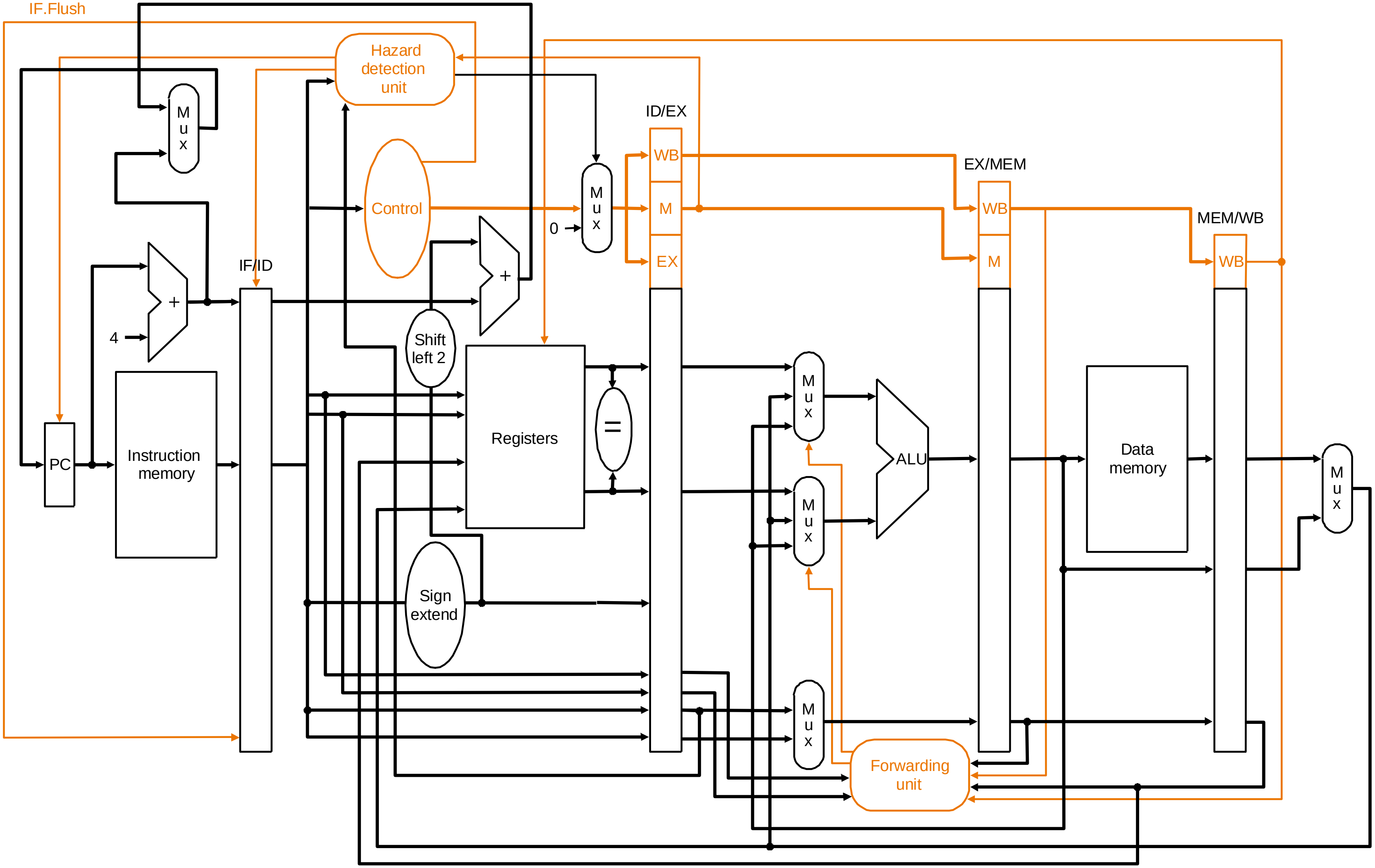
```
/* before */
for (j=0; j <20; j++)
        for (i=0; i <200; i++)
                x[i][j] = x[i][j] +1;

/* after */
for (i=0; i<200; i++)
        for (j=0; j <20; j++)
                x[i][j] = x[i][j] +1;
```

Example questions

Quantitative questions

1. Given the pipelined processor shown in the next slide, how many clock cycles are required to execute one iteration of the following loop? Show your working. (5 marks)

```
D1:     lw      s3, 20(s1)
        add     s1, s2, s3
        sub     s3, s1, s5
        and     s12, s2, s5
        add     s2, s3, s12
        or      s13, s6, s2
        sw      s13, 20(s1)
        breq    s0, s0, D1
```


IF.Flush
Hazard detection unit
M u x
Control
0
M u x
ID/EX
WB
M
EX
EX/MEM
WB
M
MEM/WB
WB
IF/ID
+
4
+
Shift left 2
PC
Instruction memory
Registers
=
M u x
ALU
M u x
Data memory
M u x
M u x
Sign extend
Forwarding unit

Example questions

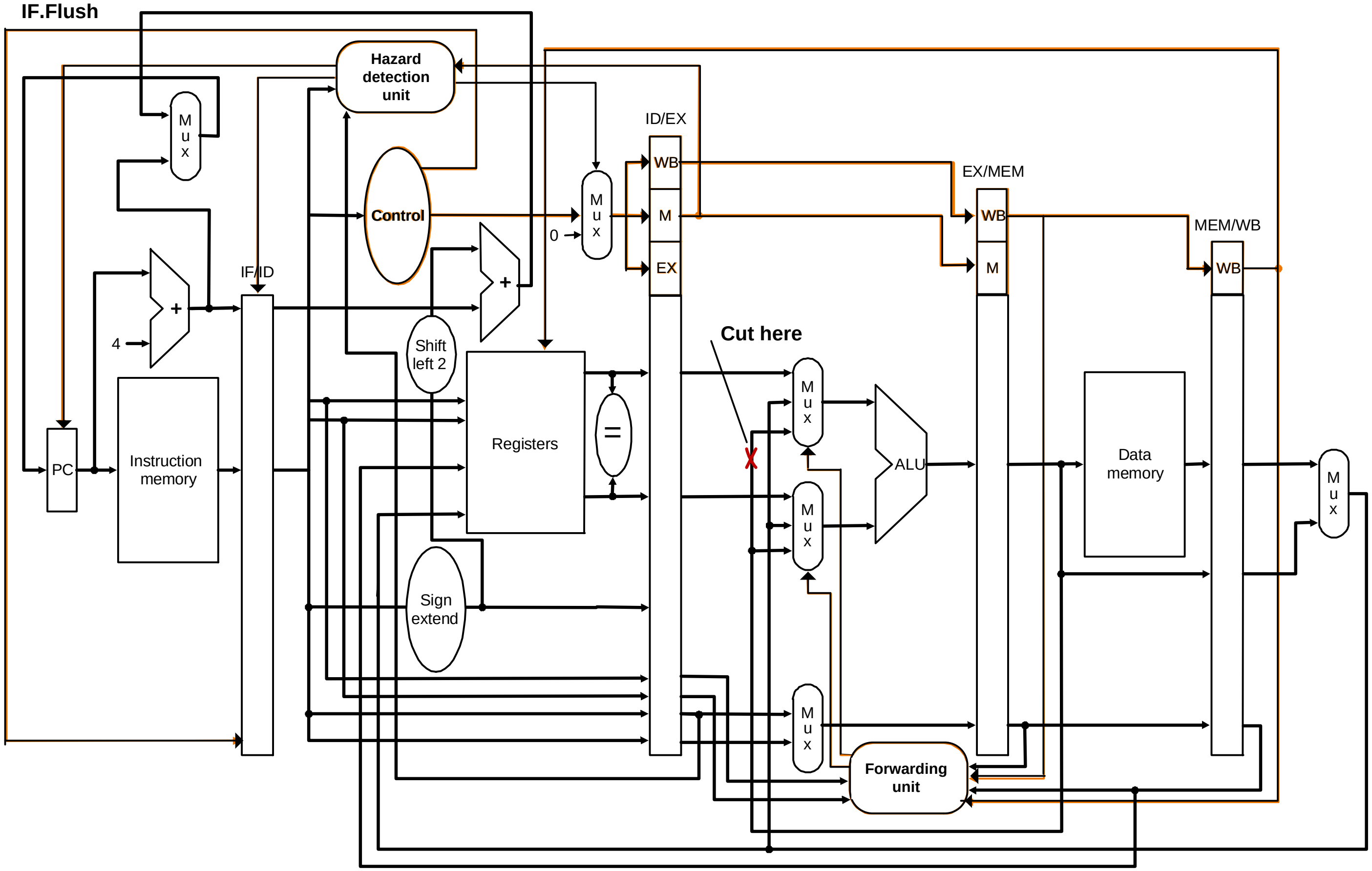
Quantitative questions

2. Assume the processor in Question 1 in the previous slide is connected to a large data memory with a two-level hierarchy (i.e cache + main memory) and the data memory access penalty is 100 clock cycles. What is the CPI for this program? Here the instruction cache is 100% hit, the data cache hit rate is 90%, and the cache hit time is 1 cc. Show your working. (8 marks)

Examples

Design question

Figure below shows a pipelined processor. What is the consequence of cutting the line as indicated in the figure? Provide a snippet of code that will fail and a snippet of code that will still work in this case.



Exam consultation

- **Friday, 3-5pm**
- **Make an appointment for other times.**

Thank You!

myExperience Survey

- Please participate
- If you have some feedback not covered by the survey, please send your comments to me.
- Your feedback is much appreciated and will be considered for future improvement.