COMP3211/COMP9211 Computer Architecture

Lab 3 Pipelined Processor

The lab is the extension of your work of Lab 2.

Goals

1. Build a simple pipelined processor.
2. Learn how to model, debug and evaluate your design.

Tasks:

Task 1: (20 marks)

Based on the single-cycle processor you built in Lab 2, build a pipelined processor model that can handle the data hazard. In your model, the control hazard is assumed to be handled by the software approach.

Task 2: (20 marks)

Verify the function of your model and determine the minimal clock cycle time of the pipeline.

For each task, you need also to design how to effectively present your work during the peer assessment. For example, your presentation for Task 1 may focus on techniques of building the model; while for Task2, your presentation may focus on the strategy of verification and results.

Due Time: your TLB class in Week 7.

Peer Assessment Scheme:

Your work on the lab tasks will be assessed by your peer students and tutor. Similar for Labs 1 & 2, for this lab

- Your TLB class is randomly divided into two assessement groups, each capped at 11 students. This is to allow sufficient time for the assessment to be completed in the 2-hour lab class.
- Each student is given 7 mins for presentation and 2 mins for Q&A.

    - The presentation covers three areas:
        - idea (that is related to design for Task 1 and verification for Task 2, respectively),
        - implementation (that is related to HD model for Task 1 and test for Task 2, respectively)
        - dicussion/conclusion
- The work is assessed based on three categories:
    - Presentation (0-4)
        - clarity
        - logic
        - timing management
    - Completion (0-4)
    - Quality (0-4)
- The link of the assessment form will is available in your MS team.
- Your tutor will organize and steer the lab.
- By the end of the lab class, all students are required to submit their assessment forms. Your participation to the assessment will be taken into account to the overall lab participation marks.