SYSC 5001W: Project deliverable 2

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1 Model Verification and Validation

The goal of the validation is to produce a model that represents true system behavior closely enough for the model to be used as a substitute for the actual system.

1.1 Verification of Simulation Models

Verification is concerned with building the model correctly. It proceeds by the comparison of the conceptual model to the computer representation what implements that conception.

1.1.1 Flow Diagram

I made a flow diagram that includes each logically possible action a system can take when an event occurs.

CLOCK = Simulation Clock

ETYPE = Event Type

NCUST = Number of Customer in the WorkStation

STATUS = Status of WorkStation (1-busy 0-idle)

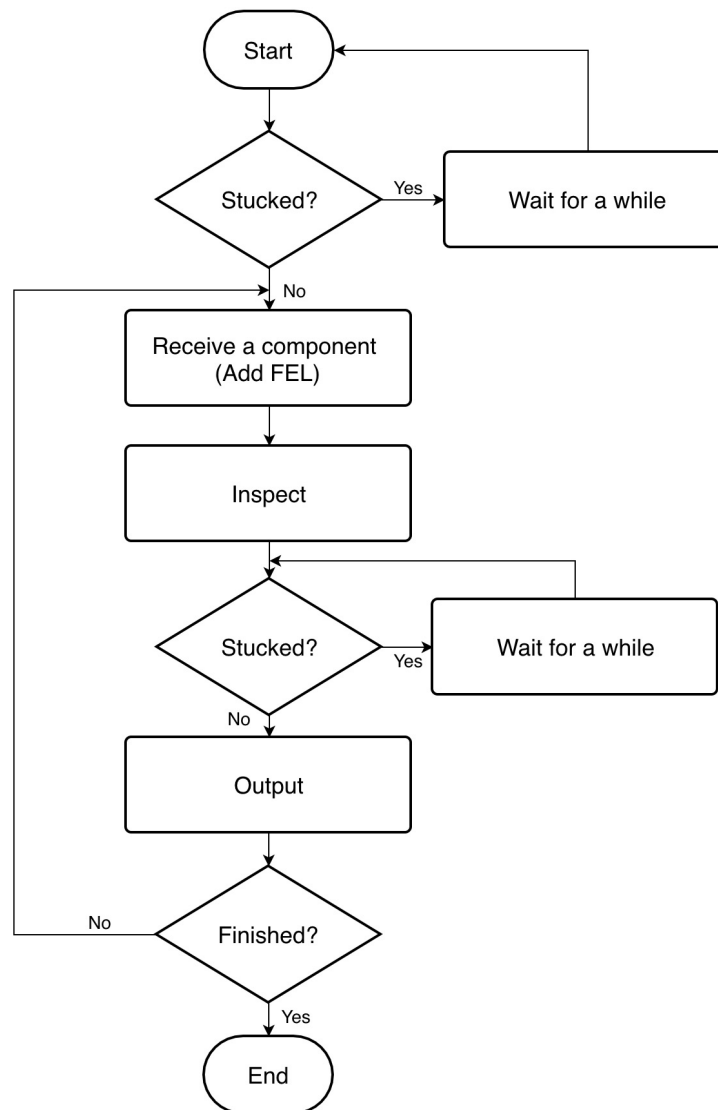| CLOCK	ETYPE	NCUST	STATUS
0	Start	0	0
7.46	Arrival	1	0
8.31	Output	0	0
22.65	Arrival	1	0
34.56	Output	0	0

Figure 1: Simulation Trace
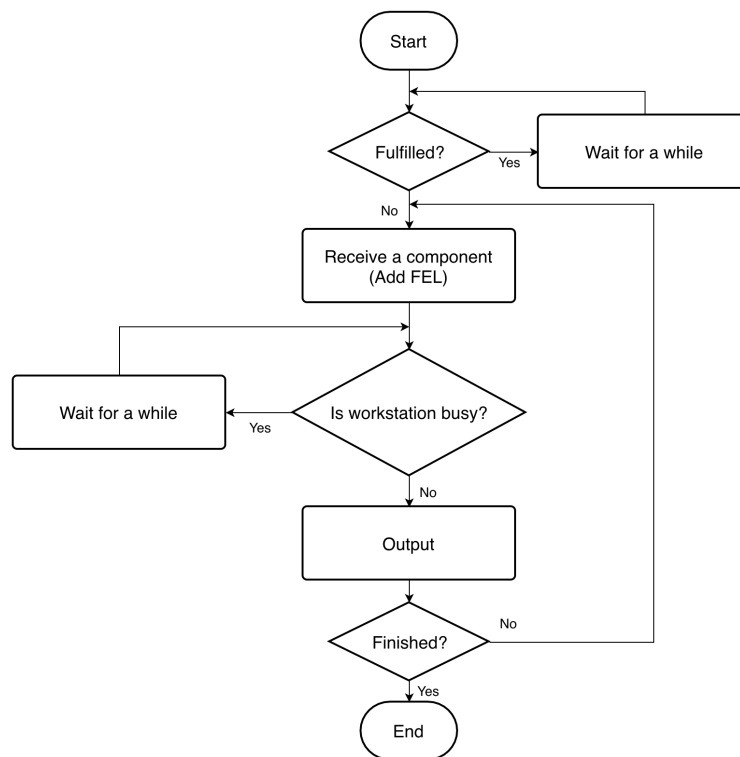
Figure 2: Work flow of Inspectors
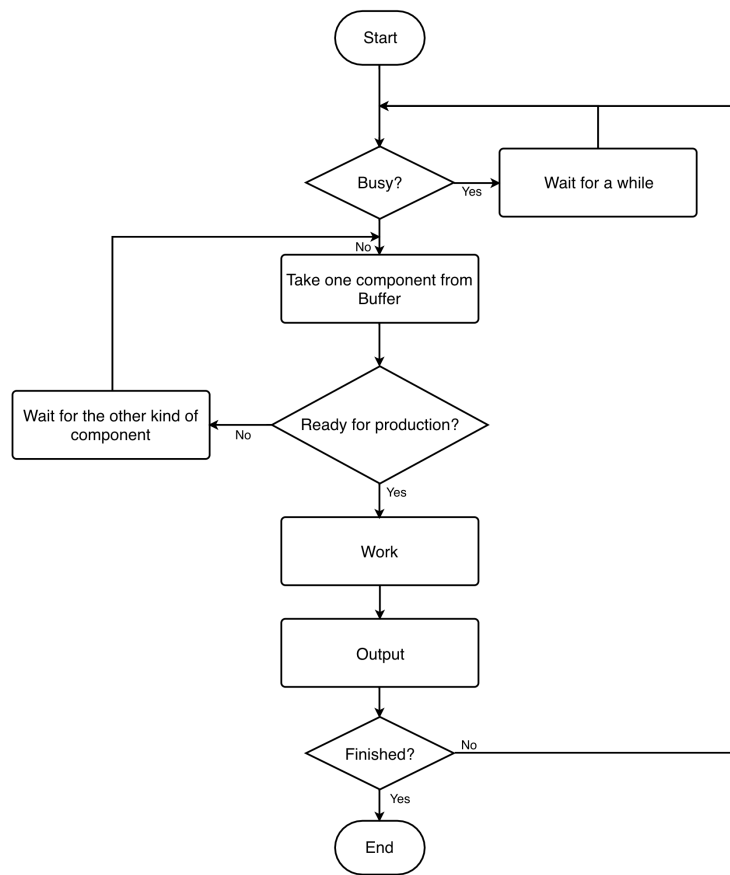
Figure 3: Work flow of Buffer

Figure 4: Work flow of Workstation

This simulation trace table indicates how the Workstation 1 work in this process. It just wait for Component 1, deal with it and then output. If the station is busy and a new one comes, the new arrival will stay at the buffer for now.

1.1.2 Model Output

The output of model is reasonable because it tracks each component of the whole process and the total time it costs is similar to the real time cost. For each object in the process, I can extract what it is doing at a certain point in time.

1.1.3 Sequence of dealing events

My code follows the rule that proceed events as time goes. The primary key of every event happened in this process is the clock. When we know that something is certain to happen, we put it in the FEL. Then we sort it according to the time of the occurrence of these things. The earlier event comes out first and latter event comes out the last.

1.1.4 Little's Law

Little's Law works for any blackbox, where the blackbox can be a complex system, or any subunit such as a single waiting line or a single server, a waiting line plus a sever, etc.

For each queue system in this project, we do a Little's law verification.

$$\hat{L} = \hat{\lambda}\hat{w} \tag{1}$$

$\hat{L}$ means average number of components in the queue. $\hat{\lambda}$ means the arrival rate of components. $\hat{w}$ means average working time for each component.

For Inspector system, consider the supply of the component for each inspector is sufficient, which means theres always a component waiting outside and there's always existing one component in each inspector. It's easy to calculate that the average dealing time for each inspector but things are little different here. If the corresponding workstation has a full buffer already and can't hold more components, the component must stay in the inspector and the inspector stop receiving new components. Here we have $L = \hat{L} = 1$

1.2 Validation

1.3 Face Validity