DATA SHEET

旭曜科技 ORISE TECH

SPFD5408A

720-channel 6-bit Source Driver with System-on-chip for Color Amorphous TFT-LCDs

Preliminary

DEC. 20, 2006

Version 0.1

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720-CHANNEL DRIVER WITH SYSTEM-ON-CHIP (SOC) FOR COLOR AMORPHOUS TFT LCD

1. GENERAL DESCRIPTION

The SPFD5408A, a 262144-color System-on-Chip (SoC) driver LSI designed for small and medium sizes of TFT LCD display, is capable of supporting up to 240xRGBx320 in resolution which can be achieved by the designated RAM for graphic data. The 720-channel source driver has true 6-bit resolution, which generates 64 Gamma-corrected values by an internal D/A converter.

The SPFD5408A is able to operate with low IO interface power supply up to 1.6V and incorporate with several charge pumps to generate various voltage levels that form an on-chip power management system for gate driver and source driver.

The built-in timing controller in SPFD5408A can support several interfaces for the diverse request of medium or small size portable display. SPFD5408A provides system interfaces, which include 8-/9-/16-/18-bit parallel interfaces and serial interface (SPI), to configure system. Not only can the system interfaces be used to configure system, they can also access RAM at high speed for still picture display. In addition, the SPFD5408A incorporates 6, 16, and 18-bit RGB interfaces for picture movement display. The SPFD5408A also supports a function to display eight colors and a standby mode for power control consideration.

2. FEATURE

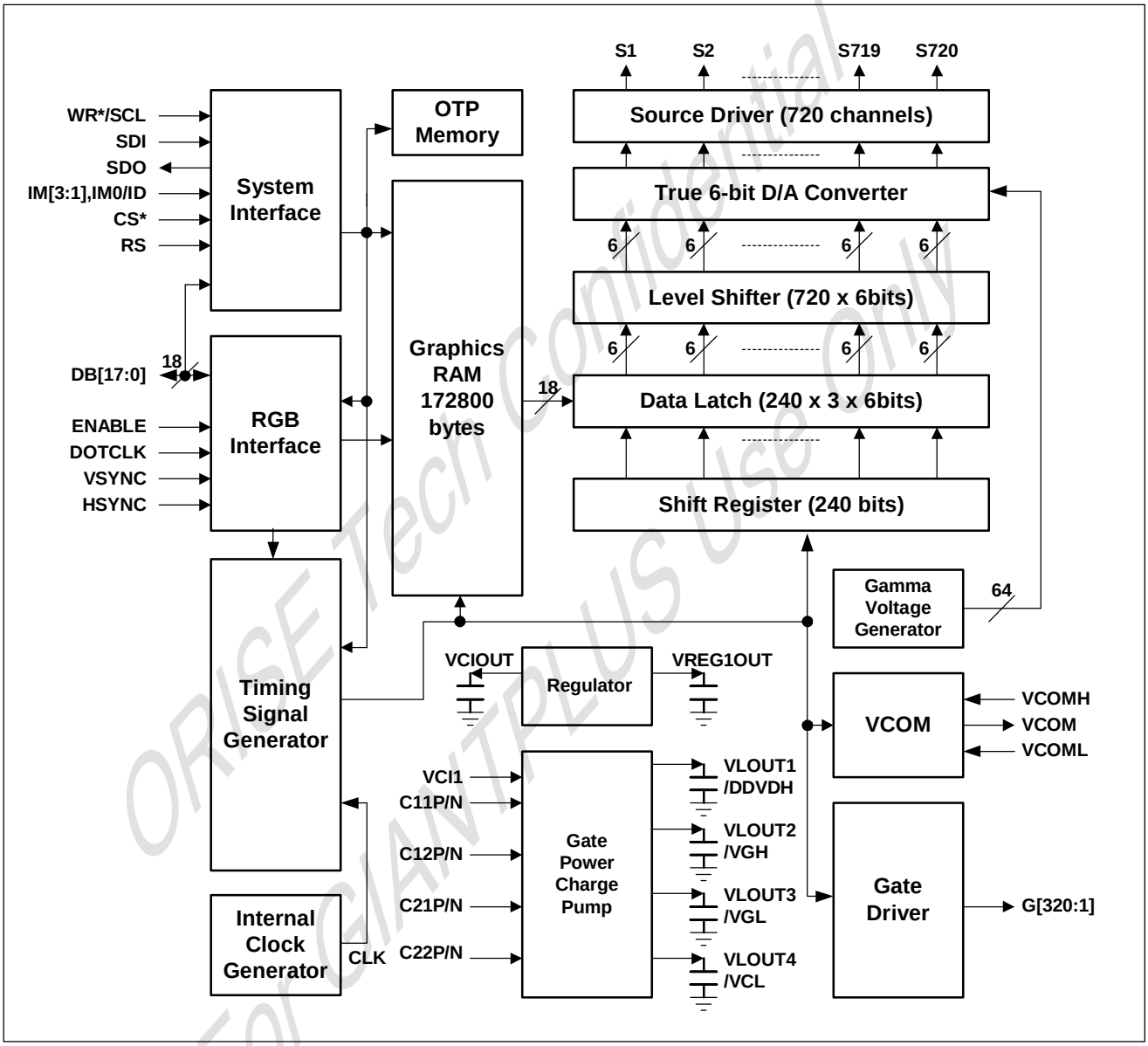
- One-chip solution for amorphous TFT-LCD.
- Supports resolution up to 240xRGBx320, incorporating a 720-channel source driver and a 320-channel gate driver
- Outputs 64 γ -corrected values using an internal true 6-bit resolution D/A converter to achieve 262K colors
- Built-in 172800 bytes internal RAM
- Line Inversion AC drive / frame inversion AC drive
- System interfaces
  - High-speed interfaces to 8-, 9-, 16-, and 18-bit parallel ports
  - Serial Peripheral Interface (SPI)
- Interfaces for moving picture display
  - 6-, 16-, and 18-bit RGB interfaces
- Diverse RAM accessing for functional display
  - Window address function to display at any area on the screen via a moving picture display interface
  - Window address function to limit the data rewriting area and reduce data transfer
  - Moving and still picture can display at the same time
  - Vertical scrolling function
  - Partial screen display
- Power supply
  - Logic power supply voltage (Vcc): 2.5 ~ 3.3 V
  - I/O interface supply voltage (IOVcc): 1.65 ~ 3.3 V
  - Analog power supply voltage (Vci): 2.5 ~ 3.3 V
- Resize function(x 1/2, x 1/4)
- On-chip power management system
  - Power saving mode (standby / 8-color mode, etc)
  - Low power consumption structure for source driver.
- Built-in Charge Pump circuits
  - Source driver voltage level : DDVDH-GND=4.5V ~ 6V.
  - Gate driver voltage level (VGH, VGL)
    VGH = 10.0V ~20.0V
    VGL = -4.5V ~ -13.5V
    VGH – VGL < 28.0V
  - Built-in internal oscillator and hardware reset
- Built–in One-Time-Programming (OTP) function for VCOM amplitude and VcomH voltage adjustment. User identification code,4 bits, VCOM level adjustment, 5 bits x 2 sets

3. ORDERING INFORMATION

Product Number	Package Type
SPFD5408A-C	Chip Form with Gold Bump

4. BLOCK DIAGRAM

4.1. Block Function



4.2. System Interface

4.2.1. The SPFD5408A supports three high-speed system interfaces:

1. 80-system high-speed interfaces with 8-, 9-, 16-, 18-bit parallel ports.
2. Serial Peripheral Interface (SPI).

The SPFD5408A has a 16-bit index register (IR) and two 18-bit data registers, a write-data register (WDR) and a read-data register (RDR). The IR register is used to store index information from control registers. The WDR register is used to temporarily store data to be written for register control and internal GRAM. The RDR register is used to temporarily store data read from the GRAM. When graphic data is written to the internal GRAM from MCU/graphic engine, the data is first written to the WDR and then automatically written to the internal GRAM in internal operation. When graphic data read operation is executed, graphic data is read via the RDR from the internal GRAM. Therefore, invalid data is first read out to the data bus when the SPFD5408A executes the 1st read operation. Thus, valid data can be read out after the SPFD5408A executes the 2nd read operation.

4.2.2. External Display Interface

The SPFD5408A supports external RGB interface for picture movement display.

The SPFD5408A allows switching between one of the external display interfaces and the system interface via pin configuration so that the optimum interface is selected for still / moving picture displayed on the screen.

When the RGB interface is chosen, display operations are synchronized with external supplied signals, VSYNC, HSYNC, and DOTCLK. Moreover, valid display data (DB17-0) is written to GRAM, which synchronized with signal (DE) enabling.

4.2.3. Address Counter (AC)

SPFD5408A features an Address Counter (AC) giving an address to the internal GRAM. The address in the AC is automatically updated plus or minus 1. The window address function enables writing data only in the rectangular area arbitrarily set by users on the GRAM.

4.2.4. Graphics RAM (GRAM)

SPFD5408A features a 172800-byte (240 x 320 x 18 / 8) Graphic RAM (GRAM).

4.2.5. Grayscale Voltage Generating Circuit

SPFD5408A has true 6-bit resolution D/A converter, which generates 64 Gamma-corrected values and cooperates with OP-AMP structure to enhance display quality. The grayscale voltage can be adjusted by grayscale data set in the γ-correction register.

4.2.6. Timing Controller

SPFD5408A has a timing controller, which can generate a timing signal for internal circuit operation such as gate output timing, RAM accessing timing, etc.

4.2.7. Oscillator (OSC)

The SPFD5408A also features an internal oscillator to generate RC oscillation with an internal resistor. In standby mode, RC oscillation is halted to reduce power consumption.

4.2.8. Source Driver Circuit

SPFD5408A consists of a 720-output source driver circuit (S1 ~ S720). Data in the GRAM are latched when the 720th bit data is input. The latched data controls the source driver and generates a drive waveform.

4.2.9. Gate Driver Circuit

SPFD5408A consists of a 320-output gate driver circuit (G1~G320). The gate driver circuit outputs gate driver signals at either VGH or VGL level.

4.2.10. LCD Driving Power Supply Circuit

The LCD driving power supply circuit generates the voltage levels DDVDH, VLOUT1, VLOUT2 and VCOM for driving an LCD. All this voltages can be adjusted by register setting.

5. SIGNAL DESCRIPTIONS

<table>
<tr><th>Signal</th><th>Pin No.</th><th>I/O</th><th>Connected with</th><th>Function</th></tr>
<tr><td colspan="5">System Configuration Input Signal</td></tr>
<tr><td>IM3~1, IM0/ID</td><td>4</td><td>I</td><td>GND/ IOVcc</td><td>Select a mode to interface to an MPU. In serial interface operation, the IM0 pin is used to set the ID bit of device code.
<table>
<tr><th>IM3</th><th>IM2</th><th>IM1</th><th>IM0/ I D</th><th>Interface Mode</th><th>DB Pin</th><th>Colors</th></tr>
<tr><td>0</td><td>0</td><td>0</td><td>0</td><td>Setting disabled</td><td>-</td><td>-</td></tr>
<tr><td>0</td><td>0</td><td>0</td><td>1</td><td>Setting disabled</td><td>-</td><td>-</td></tr>
<tr><td>0</td><td>0</td><td>1</td><td>0</td><td>80-system 16-bit interface</td><td>DB17-10, DB8-1</td><td>262,144 see Note 1</td></tr>
<tr><td>0</td><td>0</td><td>1</td><td>1</td><td>80-system 8-bit interface</td><td>DB17-10</td><td>262,144 see Note 2</td></tr>
<tr><td>0</td><td>1</td><td>0</td><td>*(ID)</td><td>Clock synchronous serial interface</td><td>-</td><td>65,536</td></tr>
<tr><td>0</td><td>1</td><td>1</td><td>0</td><td>Setting disabled</td><td>-</td><td>-</td></tr>
<tr><td>0</td><td>1</td><td>1</td><td>1</td><td>Setting disabled</td><td>-</td><td>-</td></tr>
<tr><td>1</td><td>0</td><td>0</td><td>0</td><td>Setting disabled</td><td>-</td><td>-</td></tr>
<tr><td>1</td><td>0</td><td>0</td><td>1</td><td>Setting disabled</td><td>-</td><td>-</td></tr>
<tr><td>1</td><td>0</td><td>1</td><td>0</td><td>80-system 18-bit interface</td><td>DB17-0</td><td>262,144</td></tr>
<tr><td>1</td><td>0</td><td>1</td><td>1</td><td>80-system 9-bit interface</td><td>DB17-9</td><td>262,144</td></tr>
<tr><td>1</td><td>1</td><td>0</td><td>0</td><td>Setting disabled</td><td>-</td><td>-</td></tr>
<tr><td>1</td><td>1</td><td>0</td><td>1</td><td>Setting disabled</td><td>-</td><td>-</td></tr>
<tr><td>1</td><td>1</td><td>1</td><td>0</td><td>Setting disabled</td><td>-</td><td>-</td></tr>
<tr><td>1</td><td>1</td><td>1</td><td>1</td><td>Setting disabled</td><td>-</td><td>-</td></tr>
</table>
Notes: 1. 65,536 colors in one transfer mode
2. 65,536 colors in two transfers mode</td></tr>
<tr><td>/RESET</td><td>1</td><td>I</td><td>MPU or external RC circuit</td><td>RESET pin. This is an active low signal.</td></tr>
<tr><td colspan="5">Interface input Signals</td></tr>
<tr><td>/CS</td><td>1</td><td>I</td><td>MPU</td><td>Chip select signal.
Low: the SPFD5408A is accessible
High: the SPFD5408A is not accessible
Must connect to the GND or IOVCC level when not used.
This pin has weak pull high/low resistors and can be modified to high / low by metal layer change for customer’s request.</td></tr>
<tr><td>RS</td><td>1</td><td>I</td><td>MPU</td><td>Register select signal.
Low: Index register or internal status is selected.
High: Control register is selected.
Must connect to the GND or IOVCC level when not used.
This pin has weak pull high/low resistors and can be modified to high / low by metal layer change for customer’s request.</td></tr>
<tr><td>(/WR) / (SCL)</td><td>1</td><td>I</td><td>MPU</td><td>(A) In 80-system interface mode, a write strobe signal can be input via this pin and initializes a write operation when the signal is low.
(B) In SPI mode, served as a synchronizing clock signal.
This pin has weak pull high/low resistors and can be modified to high / low by</td></tr>
</table>

Signal	Pin No.	I/O	Connected with	Function
				metal layer change for customer's request.
/RD	1	I	MPU	In 80-system interface mode, a read strobe signal can be input via this pin and initializes a read operation when the signal is low. Must connect to the GND or IOVCC level when not in use. This pin has weak pull high/low resistors and can be modified to high / low by metal layer change for customer's request.
SDI	1	I	MPU	Series Data is the input on the rising edge of the SCL signal in SPI mode. Must connect to the GND or IOVCC level when not in use. This pin has weak pull high/low resistors and can be modified to high / low by metal layer change for customer's request.
SDO	1	O	MPU	Series Data is the output on the rising edge of the SCL signal in SPI mode.
DB0-DB17	1	I/O	MPU	Served as an 18-bit parallel bi-directional data bus. Data bus pin assignment corresponding to different modes are summarized in the table: **Mode** / **Pin Assignment** 8-bit system interface: DB17-DB10 9-bit system interface: DB17-DB9 16-bit system interface: DB17-DB10, DB8-DB1 18-bit system interface: DB17-DB0 18-bit External (RGB) interface: DB17-DB12 16-bit External (RGB) interface: DB17-10, DB8-DB1 18-bit External (RGB) interface: DB17-DB0 Must connect to the GND or IOVCC level when not in use. These pins have weak pull high/low resistors and can be modified to high / low by metal layer change for customer's request.
VSYNC	1	I	MPU	In external interface mode, served as a vertical synchronize signal input Must connect to the IOVCC level when not in use. This pin has weak pull high/low resistors and can be modified to high / low by metal layer change for customer's request.
HSYNC	1	I	MPU	In external interface mode, served as a horizontal synchronized signal input Must connect to the IOVCC level when not used. This pin has weak pull high/low resistors and can be modified to high / low by metal layer change for customer's request.
ENABLE	1	I	MPU	In external interface mode, polarity of ENABLE signal is synchronized with valid graphic data input. Low: Valid data on DB17-DB0 High: Invalid data on DB17-DB0 Moreover, setting EPL bit can change the polarity of the ENABLE signal. Must connect to the GND or IOVCC level when not in use. This pin has weak pull high/low resistors and can be modified to high / low by metal layer change for customer's request.
DOTCLK	1	I	MPU	In external interface mode, served as a dot clock signal. When DPL = "0": Input data on the rising edge of DOTCLK When DPL = "1": Input data on the falling edge of DOTCLK It is fixed to the IOVcc level when not in use. This pin has weak pull high/low resistors and can be modified to high / low by metal layer change for customer's request.

Signal	Pin No.	I/O	Connected with	Function
FMARK	1	O	MPU	Frame head pulse signal, which is used when writing data to the internal RAM.
Charge Pump and Power Supply Signal				
C11P/N, C12P/N C13P/N C21P/N, C22P/N C23P/N	12	-	Step-up capacitor	Connect boost capacitors for the internal DC/DC converter circuit to these pins. Leave the pins open when DC/DC converter circuits are not used.
VCIOUT	1	O	Stabilizing capacitor, VCI1	Output voltage from the step-up circuit 1, generated from the reference voltage. VC bits set the output factor. Make sure to connect to stabilizing capacitor.
VCI1	1	I/O	VCIOUT	Reference voltage of step-up circuit 1. Make sure the output voltage levels from VLOUT1, VLOUT2, and VLOUT3 do not exceed the respective setting ranges.
VLOUT1	1	O	Stabilizing capacitor, DDVDH	Output voltage from the step-up circuit 1, generated from VCI1. The step-up factor is set by BT. Make sure to connect to stabilizing capacitor. VLOUT1 = 4.5V ~ 6.0V
DDVDH	1	I	VLOUT1	Power supply for the source driver liquid crystal drive unit and VCOM drive. Connect to VLOUT1. DDVDH = 4.5V ~ 6.0V
VLOUT2	1	O	Stabilizing capacitor, VGH	Output voltage from the step-up circuit 2, generated from VCI1 and DDVDH. The step-up factor is set by BT. Make sure to connect to stabilizing capacitor. VLOUT2 = max 15.0V
VGH	1	I	VLOUT2	Liquid crystal drive power supply. Connect to VLOUT2.
VLOUT3	1	O	Stabilizing capacitor, VGL	Output voltage from the step-up circuit 2, generated from VCI1 and DDVDH. The step-up factor is set by BT bits. Make sure to connect to stabilizing capacitor. VLOUT3 = min –12.5V
VGL	1	I	VLOUT3	Liquid crystal drive power supply. Connect to VLOUT3.
VCL	1	O	Stabilizing capacitor	VCOML drive power supply. Make sure to connect to stabilizing capacitor. VCL = -1.9V ~ -3.0V
VCILVL		I	Reference power supply	VCILVL must be at the same electrical potential as VCI. VCILVL = 2.5V ~ 3.3V. Connect to external power supply. In case of COG, connect to VCI on the FPC to prevent noise.
VOTP		I	Power supply or open	OTP power supply.
Source/Gate Driver and VCOM Signals				
G1~G320	320	O	LCD	Output gate driver signals, which has the swing from VGH to VGL
S1~S720	720	O	LCD	Output source driver signals. The D/A converted 64-gray-scale analog voltage is output.
VREG1 OUT	1	O	Stabilizing capacitor	Output voltage generated from the reference voltage (VCILVL or VCIR). The factor is determined by instruction (VRH bits). VREG1OUT is used for (1) source driver grayscale reference voltage, (2) VCOMH level reference voltage, and (3) VCOM amplitude reference voltage. Connect to a stabilizing capacitor when in use. VREG1OUT = 4.0V ~ (DDVDH – 0.5)V
VCOM	1	O	TFT panel common electrode	Power supply to TFT panel's common electrode. VCOM alternates between VCOMH and VCOML. The alternating cycle is set by internal register. Also, the VCOM output can be started and halted by register setting.

Signal	Pin No.	I/O	Connected with	Function
VCOMH	1	O	Stabilizing capacitor	The High level of VCOM amplitude. The output level can be adjusted by either external resistor (VCOMR) or electronic volume. Make sure to connect to stabilizing capacitor.
VCOML	1	O	Stabilizing capacitor	The Low level of VCOM amplitude. The output level can be adjusted by instruction (VDV bits). VCOML = (VCL+0.5)V ~ 0V. Make sure to connect to stabilizing capacitor.
VCOMR	1	I	Variable resistor or open	Connect a variable resistor when adjusting the VCOMH level between VREG1OUT and GND.
VGS	1	I	GND	Reference level for the grayscale voltage generating circuit.
VCC	1	-	Power supply	Internal logic power: VCC = 2.5V ~3.3V. VCC > IOVCC.
GND	1	-	Power supply	Internal logic GND: GND = 0V.
RGND	1	-	Power supply	Internal RAM GND. RGND must be at the same electrical potential as GND. In case of COG, connect to GND on the FPC to prevent noise.
VDD	1	O	Stabilizing capacitor	Internal logic regulator output, which is used as the power supply to internal logic. Connect a stabilizing capacitor.
IOVCC	1	-	Power supply	Power supply to the interface pins: RESET*, CS*, WR, RD*, RS, DB17-0, VSYNC, HSYNC, DOTCLK, ENABLE. IOVCC = 1.65V ~ 3.3V. VCC ≥IOVCC. In case of COG, connect to VCC on the FPC if IOVCC=VCC, to prevent noise.
IOGND	1	-	Power supply	GND for the interface pins: RESET*, CS*, WR, RD*, RS, DB17-0, VSYNC, HSYNC, DOTCLK, ENABLE. IOGND = 0V. In case of COG, connect to GND on the FPC to prevent noise.
AGND	1	-	Power supply	Analog GND (for logic regulator and liquid crystal power supply circuit): AGND = 0V. In case of COG, connect to GND on the FPC to prevent noise.
VCI	1	I	Power supply	Power supply to the liquid crystal power supply analog circuit. Connect to an external power supply of 2.5V ~ 3.3V.
VCILVL	1	I	Reference power supply	VCILVL must be at the same electrical potential as VCI. VCILVL = 2.5V ~ 3.3V. Connect to external power supply. In case of COG, connect to VCI on the FPC to prevent noise.
Misc. Signal				
Test/Dummy		O	Open	Test pins. Leave them open. SPFD5408A use these pins to do self-test. No any signal on panel can cross these pins, otherwise function fail.

6. INSTRUCTIONS

6.1. Outline

The SPFD5408A supports 18-bit data bus interface to access command register to configure system. When the command register accessing is desired, sending the command information to specify which index register would be accessed and following the data to that control register. Moreover, register accessing operation should cooperate with RS, /WR, /RD signal for SPFD5408A to recognize the control instruction. And command instruction can be accomplished by using all system interfaces (18-bit, 16-bit, 9-bit, 8-bit 80 system and SPI). The corresponding pin assignment of different system interface are shown in **Figure 6-1** to **Figure 6-6**

The instruction can be categorized into 8 groups. And the 8 groups are:

1. Specify the index of register
2. Read a status
3. Display control
4. Power management Control
5. Graphics data processing
6. Set internal GRAM address
7. Transfer data to and from the internal GRAM
8. Internal grayscale γ-correction

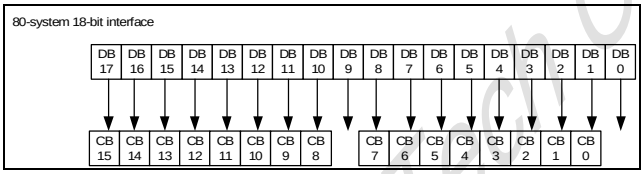


Figure 6-1

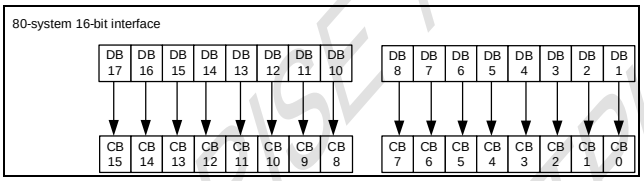


Figure 6-2

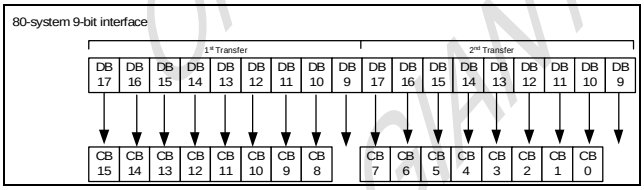


Figure 6-3

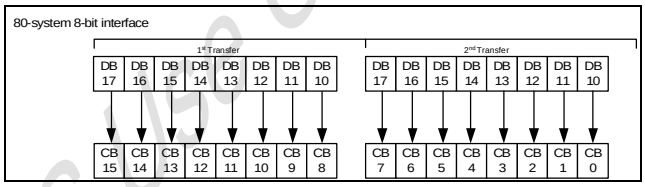


Figure 6-4

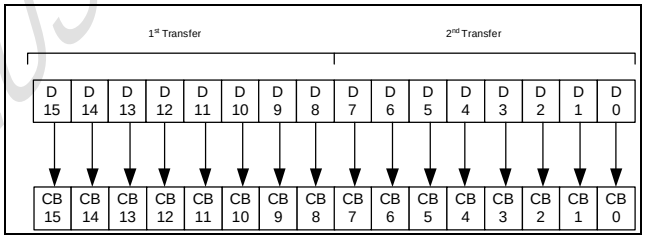


Figure 6-5

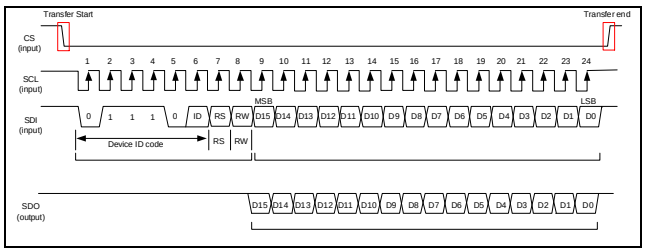


Figure 6-6

6.2. Instruction

Table 6-1 Instruction List Table

Category.	Register No	Register	Upper 8-bit								Lower 8-bit							
			CB15	CB14	CB13	CB12	CB11	CB10	CB9	CB8	CB7	CB6	CB5	CB4	CB3	CB2	CB1	CB0
	00h	ID Read	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	1
	01h	Driver Output Control	0	0	0	0	0	SM (0)	0	SS (0)	0	0	0	0	0	0	0	0
	02h	LCD AC Drive Control	0	0	0	0	0	1	B/C (0)	EOR (0)	0	0	0	0	0	0	0	NW0 (0)
	03h	Entry Mode	TRIREG (0)	DFM (0)	0	BGR (0)	0	0	HWM (0)	0	ORG (0)	0	I/D1 (1)	I/D0 (1)	AM (0)	0	0	0
	04h	Resizing Control	0	0	0	0	0	0	RCV1 (0)	RCV0 (0)	0	0	RCH1 (0)	RCH0 (0)	0	0	RSZ1 (0)	RSZ0 (0)
	07h	Display control (1)	0	0	PTDE1 (0)	PTDE0 (0)	0	0	0	BASEE (0)	0	VON (0)	GON (0)	DTE (0)	COL (0)	0	D1 (0)	D0 (0)
	08h	Display control (2)	0	0	0	0	FP3 (1)	FP2 (0)	FP1 (0)	FP0 (0)	0	0	0	0	BP3 (1)	BP2 (0)	BP1 (0)	BP0 (0)
	09h	Display control (3)	0	0	0	0	0	PTS2 (0)	PTS1 (0)	PTS0 (0)	0	0	PTG1 (0)	PTG0 (0)	ISC3 (0)	ISC2 (0)	ISC1 (0)	ISC0 (0)
	0Ah	Display control (4)	0	0	0	0	0	0	0	0	0	0	0	0	FMARKOE (0)	FMI2 (0)	FMI1 (0)	FMI0 (0)
	0Ch	External interface control (1)	0	ENC2 (0)	ENC1 (0)	ENC0 (0)	0	0	0	RM (0)	0	0	DM1 (0)	DM0 (0)	0	0	RIM1 (0)	RIM0 (0)
	0Dh	Frame Maker Position	0	0	0	0	0	0	0	FMP8 (0)	FMP7 (0)	FMP6 (0)	FMP5 (0)	FMP4 (0)	FMP3 (0)	FMP2 (0)	FMP1 (0)	FMP0 (0)
	0Fh	External interface control (2)	0	0	0	0	0	0	0	0	0	0	0	VSPL (0)	HSPL (0)	0	EPL (0)	DPL (0)
	10h	Power Control (1)	0	0	0	SAP (0)	BT3 (0)	BT2 (0)	BT1 (0)	BT0 (0)	APE (0)	0	AP1 (0)	AP0 (0)	0	DSTB (0)	SLP (0)	0
	11h	Power Control (2)	0	0	0	0	0	DC12 (0)	DC11 (0)	DC10 (0)	0	DC02 (0)	DC01 (0)	DC00 (0)	0	VC2 (0)	VC1 (0)	VC0 (0)
	12h	Power Control (3)	0	0	0	0	0	0	0	0	0	0	0	PON (0)	VRH3 (0)	VRH2 (0)	VRH1 (0)	VRH0 (0)
	13h	Power Control (4)	0	0	0	VDV4 (0)	VDV3 (0)	VDV2 (0)	VDV1 (0)	VDV0 (0)	0	0	0	0	0	0	0	0
	17h	Power Control (5)	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	PSE (0)
	20h	GRAM address Set Horizontal Address	0	0	0	0	0	0	0	0	AD7 (0)	AD6 (0)	AD5 (0)	AD4 (0)	AD3 (0)	AD2 (0)	AD1 (0)	AD0 (0)
	21h	GRAM address Set Vertical Address	0	0	0	0	0	0	0	AD16 (0)	AD15 (0)	AD14 (0)	AD13 (0)	AD12 (0)	AD11 (0)	AD10 (0)	AD9 (0)	AD8 (0)
	22h	GRAM data																
	28h	NVM read data (1)	0	0	0	0	0	0	0	0	0	0	0	0	UID3 (0)	UID2 (0)	UID1 (0)	UID0 (0)
	29h	NVM read data (2)	0	0	0	0	0	0	0	0	0	0	0	VCM14 (0)	VCM13 (0)	VCM12 (0)	VCM11 (0)	VCM10 (0)
	2Ah	NVM read data (3)	0	0	0	0	0	0	0	0	VCMSEL(0)	0	0	VCM24 (0)	VCM23 (0)	VCM22 (0)	VCM21 (0)	VCM20 (0)
	30h	γ Control (1)	0	0	0	0	0	P0KP12 (0)	P0KP11 (0)	P0KP10 (0)	0	0	0	0	0	P0KP02 (0)	P0KP01 (0)	P0KP00 (0)
	31h	γ Control (2)	0	0	0	0	0	P0KP32 (0)	P0KP31 (0)	P0KP30 (0)	0	0	0	0	0	P0KP22 (0)	P0KP21 (0)	P0KP20 (0)
	32h	γ Control (3)	0	0	0	0	0	P0KP52 (0)	P0KP51 (0)	P0KP50 (0)	0	0	0	0	0	P0KP42 (0)	P0KP41 (0)	P0KP40 (0)
	33h	γ Control (4)	0	0	0	0	0	0	P0FP11 (0)	P0FP10 (0)	0	0	0	0	0	0	P0FP01 (0)	P0FP00 (0)
	34h	γ Control (5)	0	0	0	0	0	0	P0FP31 (0)	P0FP30 (0)	0	0	0	0	0	0	P0FP21 (0)	P0FP20 (0)
	35h	γ Control (6)	0	0	0	0	0	P0RP12 (0)	P0RP11 (0)	P0RP10 (0)	0	0	0	0	0	P0RP02 (0)	P0RP01 (0)	P0RP00 (0)
	36h	γ Control (7)	0	0	0	V0RP14 (0)	V0RP13 (0)	V0RP12 (0)	V0RP11 (0)	V0RP10 (0)	0	0	0	V0RP04 (0)	V0RP03 (0)	V0RP02 (0)	V0RP01 (0)	V0RP00 (0)
	37h	γ Control (8)	0	0	0	0	0	P0KN12 (0)	P0KN11 (0)	P0KN10 (0)	0	0	0	0	0	P0KN02 (0)	P0KN01 (0)	P0KN00 (0)
	38h	γ Control (9)	0	0	0	0	0	P0KN32 (0)	P0KN31 (0)	P0KN30 (0)	0	0	0	0	0	P0KN22 (0)	P0KN21 (0)	P0KN20 (0)
	39h	γ Control (10)	0	0	0	0	0	P0KN52 (0)	P0KN51 (0)	P0KN50 (0)	0	0	0	0	0	P0KN42 (0)	P0KN41 (0)	P0KN40 (0)
	3Ah	γ Control (11)	0	0	0	0	0	0	P0FN11 (0)	P0FN10 (0)	0	0	0	0	0	0	P0FN01 (0)	P0FN00 (0)
	3Bh	γ Control (12)	0	0	0	0	0	0	P0FN31 (0)	P0FN30 (0)	0	0	0	0	0	0	P0FN21 (0)	P0FN20 (0)
	3Ch	γ Control (13)	0	0	0	0	0	P0RN12 (0)	P0RN11 (0)	P0RN10 (0)	0	0	0	0	0	P0RN02 (0)	P0RN01 (0)	P0RN00 (0)
	3Dh	γ Control (14)	0	0	0	V0RN14 (0)	V0RN13 (0)	V0RN12 (0)	V0RN11 (0)	V0RN10 (0)	0	0	0	V0RN04 (0)	V0RN03 (0)	V0RN02 (0)	V0RN01 (0)	V0RN00 (0)
	50h	Window Horzontal RAM address start	0	0	0	0	0	0	0	0	HSA7 (0)	HSA6 (0)	HSA5 (0)	HSA4 (0)	HSA3 (0)	HSA2 (0)	HSA1 (0)	HSA0 (0)
	51h	Window Horzontal RAM address start	0	0	0	0	0	0	0	0	HEA7 (1)	HEA6 (1)	HEA5 (1)	HEA4 (0)	HEA3 (1)	HEA2 (1)	HEA1 (1)	HEA0 (1)
	52h	Window Vertical RAM address start	0	0	0	0	0	0	0	VSA8 (0)	VSA7 (0)	VSA6 (0)	VSA5 (0)	VSA4 (0)	VSA3 (0)	VSA2 (0)	VSA1 (0)	VSA0 (0)
	53h	Window Vertical RAM address start	0	0	0	0	0	0	0	VEA8 (1)	VEA7 (0)	VEA6 (0)	VEA5 (1)	VEA4 (1)	VEA3 (1)	VEA2 (1)	VEA1 (1)	VEA0 (1)
	60h	Driver Output Control	GS (0)	0	NL5 (0)	NL4 (0)	NL3 (0)	NL2 (0)	NL1 (0)	NL0 (0)	0	0	SCN5 (0)	SCN4 (0)	SCN3 (0)	SCN2 (0)	SCN1 (0)	SCN0 (0)
	61h	Image Display Control	0	0	0	0	0	0	0	0	0	0	0	0	0	NDL (0)	VLE (0)	REV (0)

	6Ah	Vertical Scoll ing Control	0	0	0	0	0	0	0	VL8 (0)	VL7 (0)	VL6 (0)	VL5 (0)	VL4 (0)	VL3 (0)	VL2 (0)	VL1 (0)	VL0 (0)
	80h	Display Position 1	0	0	0	0	0	0	0	PTDP 08 (0)	PTDP 07 (0)	PTDP 06 (0)	PTDP 05 (0)	PTDP 04 (0)	PTDP 03 (0)	PTDP 02 (0)	PTDP 01 (0)	PTDP 00 (0)
	81h	GRAM start line address 1	0	0	0	0	0	0	0	PTSA 08 (0)	PTSA 07 (0)	PTSA 06 (0)	PTSA 05 (0)	PTSA 04 (0)	PTSA 03 (0)	PTSA 02 (0)	PTSA 01 (0)	PTSA 00 (0)
	82h	GRAM end line address 1	0	0	0	0	0	0	0	PTEA 08 (0)	PTEA 07 (0)	PTEA 06 (0)	PTEA 05 (0)	PTEA 04 (0)	PTEA 03 (0)	PTEA 02 (0)	PTEA 01 (0)	PTEA 00 (0)
	83h	Display Position 2	0	0	0	0	0	0	0	PTDP 18 (0)	PTDP 17 (0)	PTDP 16 (0)	PTDP 15 (0)	PTDP 14 (0)	PTDP 13 (0)	PTDP 12 (0)	PTDP 11 (0)	PTDP 10 (0)
	84h	GRAM start line address 2	0	0	0	0	0	0	0	PTSA 18 (0)	PTSA 17 (0)	PTSA 16 (0)	PTSA 15 (0)	PTSA 14 (0)	PTSA 13 (0)	PTSA 12 (0)	PTSA 11 (0)	PTSA 10 (0)
	85h	GRAM end line address 2	0	0	0	0	0	0	0	PTEA 18 (0)	PTEA 17 (0)	PTEA 16 (0)	PTEA 15 (0)	PTEA 14 (0)	PTEA 13 (0)	PTEA 12 (0)	PTEA 11 (0)	PTEA 10 (0)
	90h	Panel interface Control 1	0	0	0	0	0	0	DIVI1 (0)	DIVI0 (0)	0	0	0	RTNI4 (1)	RTNI3 (0)	RTNI2 (0)	RTNI1 (0)	RTNI0 (0)
	92h	Panel Interface Control 2	0	0	0	0	0	NOWI 2(0)	NOWI 1(0)	NOWI 0(0)	0	0	0	0	0	0	0	0
	93h	Panel Interface Control 3	0	0	0	0	0	0	VEQW 11(0)	VEQW 10(0)	0	0	0	0	0	MCPI2 (0)	MCPI1 (0)	MCPI0 (0)
	95h	Panel Interface Control 4	0	0	0	0	0	0	DIVE1 (0)	DIVE0 (0)	0	0	RTNE5 (0)	RTNE4 (1)	RTNE3 (1)	RTNE2 (1)	RTNE1 (1)	RTNE0 (0)
	97h	Panel Interface Control 5	0	0	0	0	NOW E3(0)	NOW E2(0)	NOW E1(0)	NOW E0(0)	0	0	0	0	0	0	0	0
	98h	Panel Interface Control 6	0	0	0	0	0	0	0	0	0	0	0	0	0	MCPE2 (0)	MCPE1 (0)	MCPE0 (0)
	A0h	NVM Conmtrol1	0	0	0	0	0	0	0	0	TE (0)	0	EOP1 (0)	EOP0 (0)	0	0	EAD1 (0)	EAD0(0)
	A1h	NVM Control 2	0	0	0	0	0	0	0	0	ED7 (0)	0	0	ED4 (0)	ED3 (0)	ED2 (0)	ED1 (0)	ED0 (0)
	A4h	Calibration control	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	CALB (0)

The following are detailed explanations of instructions with illustrations of instruction bits (CB15-0) assigned to each interface.

6.2.1. Index Register (IR)

R/W	RS	CB15	CCB14	CB13	CB12	CB11	CB10	CB9	CB8	CB7	CB6	CB5	CB4	CB3	CB2	CB1	CB0
W	0	□	□	□	□	□	□	□	□	ID7	ID6	ID5	ID4	ID3	ID2	ID1	ID0

The index register specifies the index (R00h ~ RFFh) of a control register. The index range is from “000_0000” to “111_1111” in binary format.

6.2.2. ID Read Register (SR)

R/W	RS	CB15	CB14	CB13	CB12	CB11	CB10	CB9	CB8	CB7	CB6	CB5	CB4	CB3	CB2	CB1	CB0
R	0	0	1	0	1	0	1	0	0	0	0	0	0	1	0	0	0

The IC code of SPFD5408A can be accessed by read operation. ‘5408H can be read out when read ID operation is exectured.

6.2.3. Driver Output Control Register (R01h)

R/W	RS	CB15	CB14	CB13	CB12	CB11	CB10	CB9	CB8	CB7	CB6	CB5	CB4	CB3	CB2	CB1	CB0
W	1	0	0	0	0	0	SM	0	SS	0	0	0	0	0	0	0	0

SS: Shift direction of the source driver output selection.
When SS = “0”, source driver shift from S1 to S528. When SS = “1”, source driver shift from S528 to S1. Moreover, SS can cooperate with BGR for different color filter configuration of LCD panel. The combination of SS and BGR bit are summarized at **Table 6-**2.

Table 6-2

SS=0;BGR=0;	S1	S2	S3	-	-▶	S526	S527	S528
SS=0;BGR=1;	S1	S2	S3	-	-▶	S526	S527	S528
SS=1,BGR=0;	S1	S2	S3	◀-		S526	S527	S528
SS=1,BGR=1;	S1	S2	S3	◀-		S526	S527	S528

SM: Set the scan mode of the gate driver output. Moreover, SM can cooperate with GS for different LCD panel gate line layout. The combination of GS and SM bit are summarized at **Table 6-**3

Table 6-3

SM	GS	Shift Direction (begin,…..,end)
0	0	G1, G2, G3, G4……G317, G318, G319, G320
0	1	G320, G319, G318, G317……G4, G3, G2, G1
1	0	G1, G3, G5, …G317, G319, …G2, G4,.. G318, G320
1	1	G320, G318, G316,..G4, G2, ..G319, G317,...G3, G1

6.2.4. LCD Driving Waveform Control (R02h)

R/W	RS	CB15	CB14	CB13	CB12	CB11	CB10	CB9	CB8	CB7	CB6	CB5	CB4	CB3	CB2	CB1	CB0
W	1	0	0	0	0	0	1	B/C	EOR	0	0	0	0	0	0	0	NW0

NW0: SPFD5408A provides N-line inversion for Vcom. NW5 to NW0 is to set the number of gate line that Vcom polarity will toggle (when B/C=1). The polarity is alternated at an interval of n+1 gate lines.

EOR: In N-line inversion, in order to insure that every pixel can avoid DC bias, SPFD5408A provides EOR (EOR=1) to force Vcom to toggle at the beginning of the frame.

B/C: This bit .is to set the Vcom toggle at frame rate format of N-line inversion format.
B/C=0: Frame inversion.
B/C=1: N-line inversion.

6.2.5. Entry Mode (R03h)

R/W	RS	CB15	CB14	CB13	CB12	CB11	CB10	CB9	CB8	CB7	CB6	CB5	CB4	CB3	CB2	CB1	CB0
W	1	TRIREG	DFM	0	BGR	0	0	HWM	0	ORG	0	I/D1	I/D0	AM	0	0	0

Table 6-4

Operation mode	ID1	ID0	AM	Function
Mode 1	0/1	0	0	Replace horizontal data
Mode2	0/1	1	1	Replace vertical data
Mode3	0/1	0	0	Conditionally replace horizontal data
Mode	0/1	1	1	Conditionally replace vertical data

AM: To set the update direction when writing data to GRAM. If AM=1, data will write in vertical direction. If AM=0, data will write in horizontal direction. Moreover, if a fixed window GRAM accessing is desired, the writing direction can be set by ID1-0 and AM bits.

I/D1-0: To specify address counter increment /decrement automatically function while GRAM is accessing. I/D[0] indicates the increment or decrement in horizontal direction. I/D[1] indicates the increment or decrement in vertical direction.
I/D[0]=0: decrement in horizontal direction automatically
I/D[0]=1: increment in horizontal direction automatically
I/D[1]=0: decrement in vertical direction automatically
I/D[1]=1: increment in vertical direction automatically
ID[1-0] setting can cooperate with Am bit to set the data updating direction.

ORG: SPFD5408A provides the option of start address definition when window function is selected.
ORG=0: RAM address setting (R20h, R21h) should set to the window start address, as normal operation case.
ORG=1: RAM address setting (R20h, R21h) should set to (00000h) no matter where the window start address is. In this case, the window start postion is treated as (00000h), regardless the physical location in GRAM.

HWM: SPFD5408A provides a high speed GRAM accessing mode that updated GRAM data in 1-line unit. Be aware that data can be written to GRAM if accessing GRAM operation is halted before writing complete data for 1-line. Make sure the AMis set to “0”, when HWM function is set to “1”.

BGR: To set the order of RGB dot location in GRAM.
BGR=0: same assignment of RGB allocation of WM17-0
BGR=1: inverse assignment of RGB allocation of WM17-0

DFM: In combination with TRIREG setting to set the different data transfer mode.

TRIREG: to set 1–3 time transfer mode for system interface. TRI bit should cooperate with DFM1-0 to meet the specific transfer mode.
For 8-bit databus interface mode:
TRIREG=0: 2 time transfer mode for 16-bit GRAM data.
TRIREG=1: 3 time transfer mode for 16-bit GRAM data
For 16-bit databus interface mode:
TRIREG=0: 1 time transfer mode for 16-bit GRAM data.
TRIREG=1: 2 time transfer mode for 16-bit GRAM data
Note: Set TRIREG=0, when using neither 8-bit nor 16-bit.

6.2.6. Scalling Control register (R04h)

R/W	RS	CB15	CB14	CB13	CB12	CB11	CB10	CB9	CB8	CB7	CB6	CB5	CB4	CB3	CB2	CB1	CB0
W	1	0	0	0	0	0	0	RCV1	RCV0	0	0	RCH1	RCH0	0	0	RSZ1	RSZ0

RSZ [1:0]: SPFD5408A provides scalling factor to give the display more flexibility to show different picture size. For detail, refer to “Scalling function”.

RSZ1	RSZ0	Scalling Factor
0	0	No Scalling
0	1	1/2 times
1	0	Setting Disable
1	1	1/4 times

RCH [1:0]: To set the surplus pixel number in horizontal direction when scalling mode is selected. When scalling mode is not selected, make sure RCH[1:0]= “00”

RCH1	RCH0	Surplus pixel number in Horzontal direction
0	0	0 Pixel
0	1	1 Pixels
1	0	2 Pixels
1	1	3 Pixels

RCH [1:0]: To set the surplus pixel number in Vertical direction when scalling mode is selected. When scalling mode is not selected, make sure RCV[1:0]= “00”

RCV1	RCV0	Surplus pixel number in Vertical direction
0	0	0 Pixel
0	1	1 Pixel
1	0	2 Pixels
1	1	3 Pixels

6.2.7. Display Control (R07h)

R/W	RS	CB15	CB14	CB13	CB12	CB11	CB10	CB9	CB8	CB7	CB6	CB5	CB4	CB3	CB2	CB1	CB0
W	1	0	0	PTDE1	PTDE0	0	0	0	BASEE	0	VON	GON	DTE	COL	0	D1	D0

D1-0: To set the internal operation, source driver output and VCOM output function. When D1-0=00; SPFD5408A is set to standby mode. The combination of D1-0 and AM bit is summarized at **Table 6-5**.

Table 6-5

D1	D0	BASEE	Source, VCOM output	Internal Operation	FLM
0	0	*	GND	Terminated	OFF
0	1	*	GND	Normal Operation	ON
1	0	*	Non-lit display	Normal Operation	ON
		0	Non-lit display	Normal Operation	ON
		1	Normal display	Normal Operation	ON

COL: 8-color mode selection. When CL=1 SPFD5408A enter to 8-color mode. When CL=0, SPFD5408A is in normal operation mode.

DTE, GON: Specify the high/low level of gate driver output signal. The combination of DTE and GON bit is summarized at **Table 6-6**.

Table 6-6

APE	DTE	GON	Gate Output
0	*	*	VGL(=GND)
1	0	0	VGH
	0	1	VGL
	1	0	VGH
	1	1	VGH/VGL

VON: To Control VCOM output signal. The combination of APE, AP[1:0] and VON bit is summarized at **Table 6-67**

Table 6-7

APE	AP [1:0]	VON	VCOM Output
0	*	*	GND
1	0	0	GND
	0	1	Setting disable
	1~3	0	VCOML
	1~3	1	VCOMH/VCOML

BASEE: To enable Base image display

BASEE	
0	(1) Non-lit display (2) Partial image display
1	Base image is display on the LCD

PTDE1-0: To set the partial-display enables function.
PTDE [0]: "0" Partial image 1 display "Off".
"1" Partial image 1 display "On".
PTDE [1]: "0" Partial image 2 display "Off".
"1" Partial image 2 display "On".

6.2.8. Display Control 2 (R08h)

R/W	RS	CB15	CB14	CB13	CB12	CB11	CB10	CB9	CB8	CB7	CB6	CB5	CB4	CB3	CB2	CB1	CB0
W	1	0	0	0	0	FP3	FP2	FP1	FP0	0	0	0	0	BP3	BP2	BP1	BP0

FP3-0: Set the amount of blank period of front porch
BP3-0: Set the amount of blank period of back porch

Table 6-8 summarized the function of FP3-0/BP3-0 setting.
When setting this register, make sure that:
BP + FP ≤ 16 lines
FP ≥ 2 lines
BP ≥ 2 lines

In external display interface mode, a back porch (BP) period starts on the falling edge of the VSYNC signal, followed by a display operation period. After driving the number of lines set with NL bits, a front porch period starts. After the front porch period, a blank period continues until the next input of VSYNC signal. Be aware that different interface mode, has different BP/ FP setting. **Table 6-9** summarized the setting for each interface mode.

Table 6-8

FP3	FP2	FP1	FP0	Number of lines for the Front Porch
BP3	**BP2**	**BP1**	**BP0**	**Number of lines for the Back Porch**
0	0	0	0	Setting disabled
0	0	0	1	Setting disabled
0	0	1	0	2 lines
0	0	1	1	3 lines
0	1	0	0	4 lines
0	1	0	1	5 lines
0	1	1	0	6 lines

FP3	FP2	FP1	FP0	Number of lines for the Front Porch
BP3	BP2	BP1	BP0	Number of lines for the Back Porch
0	1	1	1	7 lines
1	0	0	0	8 lines
1	0	0	1	9 lines
1	0	1	0	10 lines
1	0	1	1	11 lines
1	1	0	0	12 lines
1	1	0	1	13 lines
1	1	1	0	14 lines
1	1	1	1	Setting disabled

Table 6-9

Operation of Internal clock	BP ≥ 2 lines	FP ≥ 2 lines	FP +BP ≤ 16 lines
RGB interface	BP ≥ 2 lines	FP ≥ 2 lines	FP +BP ≤ 16 lines
VSYNC interface	BP ≥ 2 lines	FP ≥ 2 lines	FP +BP = 16 lines

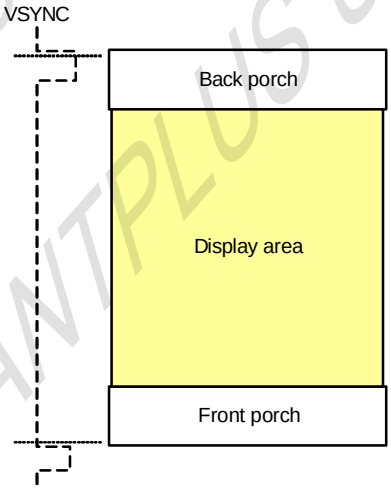


Figure 6-7 Front porch and back porch function diagram

6.2.9. Display Control 3 (R09h)

R/W	RS	CB15	CB14	CB13	CB12	CB11	CB10	CB9	CB8	CB7	CB6	CB5	CB4	CB3	CB2	CB1	CB0
W	1	0	0	0	0	0	PTS2	PTS1	PTS0	0	0	PTG1	PTG0	ISC3	ISC2	ISC1	ISC0

ISC3-0: To set the gate driver scan cycle in non-display area.

Table 6-10 summarized the function of ISC3-0 setting

Table 6-10

ISC3	ISC2	ISC1	ISC0	Scan cycle	fFLM=60Hz
0	0	0	1	Setting disable	
0	0	1	0	3frames	50 mS
0	0	1	1	5 frames	84 mS
0	1	0	0	7 frames	117 mS
0	1	0	1	9 frames	150 mS
0	1	1	0	11 frames	184 mS
0	1	1	1	13 frames	217 mS
1	0	0	0	15 frames	251 mS
1	0	0	1	19 frames	317 mS
1	0	1	0	21 frames	351 mS
1	0	1	1	23 frames	384 mS
1	1	0	0	25 frames	418 mS

ISC3	ISC2	ISC1	ISC0	Scan cycle	fFLM=60Hz
1	1	0	1	27 frames	451 mS
1	1	1	0	29 frames	484 mS
1	1	1	1	31 frames	518 mS

PTG1-0: To set the gate driver scan mode in non-display area.
Table 6-11 summarized the function of PTG1-0 setting

Table 6-11

PTG1	PTG0	Gate outputs in non-display area	Source outputs in non-display area	Vcom output
0	0	Normal scan	Based on the PT2-0 bits setting	VcomH/VcomL
0	1	Setting Disable		
1	0	Interval scan	Based on the PT2-0 bits setting	VcomH/VcomL
1	1	Setting Disable		

PTS2-0: To set the source driver output level in non-display area of partial display mode. **Table 6-2** summarized the function of PTS2-0 setting.

Table 6-2

PTS2	PTS1	PTS0	Source output in non-display area		Operation amplifier in non-display area
			+ polarity	- polarity	
0	0	0	V63	V0	V0-V63
0	0	1	Invalid setting	Invalid setting	-
0	1	0	GND	GND	V0-V63
0	1	1	High impedance	High impedance	V0-V63
1	0	0	V63	V0	V0, V63
1	0	1	Invalid setting	Invalid setting	-
1	1	0	GND	GND	V0, V63
1	1	1	High impedance	High impedance	V0, V63

6.2.10. Frame Cycle Control (R0Ah)

R/W	RS	CB15	CB14	CB13	CB12	CB11	CB10	CB9	CB8	CB7	CB6	CB5	CB4	CB3	CB2	CB1	CB0
W	1	0	0	0	0	0	0	0	0	0	0	0	0	FMARKOE	FMI2	FMI1	FMI0

FMI [2:0]: SPFD5408 provide FMARK signal to prevent tearing effect. FMI [2:0] can set FMARK output interval.

FMI2	FMI1	FMI0	Output interval
0	0	0	1 frame
0	0	1	2 frames
0	1	1	4 frames
1	0	1	6 frames
Other Setting			Setting Disable

FMARKOE: Initialized the output signal FMARK from FMARK pin.
FMARK="0": Output FMARK disable
FMARK="1". Output FMARK enables.

6.2.11. External Display Interface Control 1 (R0Ch)

R/W	RS	CB15	CB14	CB13	CB12	CB11	CB10	CB9	CB8	CB7	CB6	CB5	CB4	CB3	CB2	CB1	CB0
W	1	0	ENC2	ENC1	ENC0	0	0	0	RM	0	0	DIM1	DIM0	0	0	RIM1	RIM0

RIM1-0: To set the different transfer modes of RGB interface.

Table 6-3 summarized the function of RIM1-0 setting.

Table 6-3

RIM1	RIM0	RGB Interface Mode	Colors	Data Bus
0	0	18-bit RGB interface (one transfer/pixel)	262K	DB 17-0
0	1	16-bit RGB interface (one transfer/pixel)	65K	DB 17-13; DB 11-1
1	0	6-bit RGB interface (three transfers/pixel)	262K	DB17-12
1	1	Setting disabled	-	-

DM1-0: To specify the display interface mode. DM1-0 Setting can switch the display interface among system interface, RGB interface and VSYNC interface.

Table 6-4 summarized the function of DM1-0 setting.

Table 6-4

DM1	DM0	Display Interface
0	0	Internal clock operation
0	1	RGB interface
1	0	VSYNC interface
1	1	Setting disabled

RM: Select the interface to access the SPFD5408A's internal GRAM. Set RM to "1" when writing display data via the RGB interface. The SPFD5408A allows for setting the RM bit not constrained by the mode used for the display operation. This means it is possCBle to rewrite display data via a system interface by setting RM = "0" even while display operations are performed via the RGB interface.

Table 6-5 summarized the function of RM bit setting.

Table 6-5

RM	Interface for RAM Access
0	System interface/VSYNC interface
1	RGB interface

ENC2-0: Set the RAM data write cycle in RGB interface mode.

Table 6-6 summarized the function of ENC2-0 setting.

Table 6-6 ENC1-0 bits

ECN2	ECN1	ECN0	RAM data write cycle
0	0	0	1 frame
0	0	1	2 frames
0	1	0	3 frames
0	1	1	4 frames
1	0	0	5 frames
1	0	1	6 frames
1	1	0	7 frames

1	1	1	8 frames

Table 6-7

Display State	Operation Mode	RAM Access (RM)	Display Operation Mode (DM1-0)
Still pictures	Internal clock operation	System interface (RM = 0)	Internal clock operation (DM1-0 = 00)
Moving pictures	RGB interface (1)	RGB interface (RM = 1)	RGB interface (DM1-0 = 01)
Rewrite still picture area while displaying moving pictures.	RGB interface (2)	System interface (RM = 0)	RGB interface (DM1-0 = 01)
Moving pictures	VSYNC interface	System interface (RM = 0)	VSYNC interface (DM1-0 = 10)

Note1: Instructions are set only via the system interface.
Note2: The RGB-I/F and the VSYNC-I/F are not used simultaneously.
Note3: Do not make changes to the RGB-I/F mode setting (RIM-0) while the RGB I/F is in operation.
Note4: See the "External Display Interface" section for the flowcharts to follow when switching from one mode to another.
Note5: Use the high-speed write mode (HWM/LHWM = "1") when writing data in RGB or VSYNC interface mode.

6.2.12. Frame Maker Position (R0Dh)

R/W	RS	CB15	CB14	CB13	CB12	CB11	CB10	CB9	CB8	CB7	CB6	CB5	CB4	CB3	CB2	CB1	CB0
W	1	0	0	0	0	0	0	0	FMP8	FMP7	FMP6	FMP5	FMP4	FMP3	FMP2	FMP1	FMP0

FMP 8-0: indicates the output position of frame cycle signal (frame maker) relation with back porch. When FMP[8:0] =9'h000, FMARK is outputted at the start of back porch. When FMP[8:0] =9'h001, FMARK is outputted one line after the start of back porch.

FMP [8:0]	RAM data write cycle
9'h000	immedated
9'h001	1 line
9'h002	2 line
9'h175	373 lines
9'h176	374 lines
9'h177	375 lines

6.2.13. External Display Interface Control 2 (R0Fh)

R/W	RS	CB15	CB14	CB13	CB12	CB11	CB10	CB9	CB8	CB7	CB6	CB5	CB4	CB3	CB2	CB1	CB0
W	1	0	0	0	0	0	0	0	0	0	0	0	VSPL	HSPL	0	EPL	DPL

EPL: The polarity of ENABLE signal selection in RGB interface mode.
EPL = "0": ENABLE: Low active
EPL = "1": ENABLE: High active

DPL: Select the data latch edge of the DOTCLK signal in RGB interface mode.
DPL = "0": rising edge of the DOTCLK.
DPL ="1": falling edge of the DOTCLK.

VSPL: The polarity of VSYNC signal selection in RGB interface mode.
VSPL = "0": Low active.
VSPL = "1": High active.

HSPL: The polarity of HSYNC signal selection in RGB interface mode.
HSPL = "0": Low active.

HSPL = ”1”: High active.

6.2.14. Power Control 1 (R10h)

R/W	RS	CB15	CB14	CB13	CB12	CB11	CB10	CB9	CB8	CB7	CB6	CB5	CB4	CB3	CB2	CB1	CB0
W	1	0	0	0	SAP	BT3	BT2	BT1	BT0	APE	0	AP1	AP0	0	DSTB	SLP	0

SLP: Sleep mode selection. When SLP =1, SPFD5408A set to sleep mode. In sleep mode, all internal operations are terminated except internal RC oscillation. Be sure that a display off sequence should be executed before set SLP to “1”. In sleep mode, no instruction can be accepted except R11h, R13h, bit 3-0 of R12h and R10h (except SAP2-0). Set STB=0 can exit sleep mode. Moreover, when exit from sleep mode, data in GRAM and in instruction registers are keep the same with these before set to SLP mode.

DSTB: Deep Standby mode selection. When DSTB =1, SPFD5408A set to deep standby mode. In this mode, all internal operations are terminated including internal RC oscillation. Be sure that a display off sequence should be executed before set DSTB to “1”. Set DSTB=0 can exit standby mode. Be sure that start oscillation following by 10ms delay should be executed before set DSTB to “0”. Moreover, when exit from deep standby mode, data in GRAM and register might be lost, reset and re-sending command and data into GRAM is necessary.

AP1-0: Operational amplifier DC bias current adjustment. Set AP1-0 = “00” to stop operational amplifier and DC/DC charge pump circuits to reduce current consumption during no display period. **Table 6-8** summarized the function of AP1-0 setting

Table 6-8

AP1	AP0	Constant current in power supply circuit	Constant current in Gamma circuit
0	0	Halt	Halt
0	1	0.5	0.62
1	0	0.75	0.71
1	1	1	1

APE: Enable bit for both liquid crystal power supply and gamma voltage generation circuit.

APE=”0”, Enable liquid crystal power supply and gamma voltage generation circuit.

APE=”1”, Halt liquid crystal power supply and gamma voltage generation circuit.

BT3-0: Set the voltage level of DDVDH, VGH, VGL and DD4OUT.

Table 6-9 summarized the function of BT3-0 setting

BT3	BT2	BT1	BT0	DDVDH	VGH	VGL	VCL	Capacitor connection pins
0	0	0	0	VCI1 x 2 [x2]	DDVDH x 3 [VCI1 x 6]	-(VCI1+DDVDHx 2) [VCI1x -5]	-VCI1	C23 can be eliminated
0	0	0	1	VCI1 x 2 [x2]	DDVDH x 4 [VCI1 x 8]	-(DDVDHx 2) [VCI1x -4]	-VCI1	
0	0	1	0	VCI1 x 2 [x2]	DDVDH x 4 [VCI1 x 8]	-(VCI1+DDVDH) [VCI1x -3]	-VCI1	
0	0	1	1	VCI1 x 2 [x2]	DDVDH x 3 + VCI1 [VCI1 x 7]	-(VCI1+DDVDHx 2) [VCI1x -5]	-VCI1	
0	1	0	0	VCI1 x 2 [x2]	DDVDH x 3 + VCI1 [VCI1 x 7]	-(DDVDHx 2) [VCI1x -4]	-VCI1	
0	1	0	1	VCI1 x 2 [x2]	DDVDH x 3 + VCI1 [VCI1 x 7]	-(VCI1+DDVDH) [VCI1x -3]	-VCI1	
0	1	1	0	VCI1 x 2 [x2]	DDVDH x 3 [VCI1 x 6]	-(DDVDHx 2) [VCI1x -4]	-VCI1	C23 can be eliminated
0	1	1	1	VCI1 x 2 [x2]	DDVDH x 3 [VCI1 x 6]	-(VCI1+DDVDH) [VCI1x -3]	-VCI1	C23 can be eliminated

1	0	0	0	VCI1 x 3 [x3]	DDVDH x 3 [VCI1 x 9]	-(VCI1+DDVDHx 2) [VCI1x -7]	-VCI1	C23 can be eliminated
1	0	0	1	VCI1 x 3 [x3]	DDVDH x 4 [VCI1 x 12]	-(DDVDHx 2) [VCI1x -6]	-VCI1	
1	0	1	0	VCI1 x 3 [x3]	DDVDH x 4 [VCI1 x 12]	-(VCI1+DDVDH) [VCI1x -4]	-VCI1	
1	0	1	1	VCI1 x 3 [x3]	DDVDH x 3 + VCI1 [VCI1 x 10]	-(VCI1+DDVDHx 2) [VCI1x -7]	-VCI1	
1	1	0	0	VCI1 x 3 [x3]	DDVDH x 3 + VCI1 [VCI1 x 10]	-(DDVDHx 2) [VCI1x -6]	-VCI1	
1	1	0	1	VCI1 x 3 [x3]	DDVDH x 3 + VCI1 [VCI1 x 10]	-(VCI1+DDVDH) [VCI1x -4]	-VCI1	
1	1	1	0	VCI1 x 3 [x3]	DDVDH x 3 [VCI1 x 9]	-(DDVDHx 2) [VCI1x -6]	-VCI1	C23 can be eliminated
1	1	1	1	VCI1 x 3 [x3]	DDVDH x 3 [VCI1 x 9]	-(VCI1+DDVDH) [VCI1x -4]	-VCI1	C23 can be eliminated

SAP: Enable bit for gamma voltage generation circuit.

SAP="0", Enable gamma voltage generation circuit.

SAP="1", Halt gamma voltage generation circuit.

6.2.15. Power Control 2 (R11h)

R/W	RS	CB15	CB14	CB13	CB12	CB11	CB10	CB9	CB8	CB7	CB6	CB5	CB4	CB3	CB2	CB1	CB0
W	1	0	0	0	0	0	DC12	DC11	DC10	0	DC02	DC01	DC00	0	VC2	VC1	VC0

VC2-0: Set the voltage of VCIOUT. VCIOUT is generated by VCILVL. **Table 6-20** summarized the function of VC2-0 setting

Table 6-20

VC2	VC1	VC0	VDCOUT
0	0	0	0.94 x VciLVL
0	0	1	0.89 x VciLVL
0	1	0	Setting Disable
0	1	1	Setting Disable
1	0	0	0.76 x VciLVL
1	0	1	Setting Disable
1	1	0	Setting Disable
1	1	1	1.00 x VCILVL

0	1	1	Oscillation clock / 8
1	0	0	Oscillation clock / 16
1	0	1	Invalid Setting
1	1	0	Halt Step-up Circuit 1
1	1	1	Invalid Setting

DC02-00: Set DC/DC charge pump circuit 1 operating frequency. **Table 6-210** summarized the function of DC02-00 setting

Table 6-210

DC02	DC01	DC00	DC/DC charge pump circuit 1 frequency (fDCDC1)
0	0	0	Oscillation clock
0	0	1	Oscillation clock / 2
0	1	0	Oscillation clock / 4

DC12-10: Set DC/DC charge pump circuit 2 operating frequency. **Table 6-11** summarized the function of DC02-00 setting

Note: Be aware that DC/DC charge pump 1 frequency ≥ DC/DC charge pump 2 frequency

Table 6-11

DC12	DC11	DC10	Step-up circuit 2 step-up frequency (fDCDC2)
0	0	0	Oscillation clock / 16
0	0	1	Oscillation clock / 32
0	1	0	Oscillation clock / 64
0	1	1	Oscillation clock / 128

1	0	0	Oscillation clock / 256
1	0	1	Setting disabled
1	1	0	Halt Step-up Circuit 2
1	1	1	Setting disabled

Note: Be sure fDCDC1≥fDCDC2 when setting DC02-00, DC12-10.

6.2.16. Power Control 3 (R12h)

R/W	RS	CB15	CB14	CB13	CB12	CB11	CB10	CB9	CB8	CB7	CB6	CB5	CB4	CB3	CB2	CB1	CB0
W	1	0	0	0	0	0	0	0	VCMR[0]	VREG1R	0	PSON	PON	VRH3	VRH2	VRH1	VRH0

VRH3-0: Set the voltage level of VS. VS is generated by REGP. **Table 6-12** summarized the function of VRH3-0 setting

Table 6-12

VRH3	VRH2	VRH1	VRH0	VREG1OUT voltage		VRH3	VRH2	VRH1	VRH0	VREG1OUT voltage	
				VCILVL	VCIR					VCILVL	VCIR
0	0	0	0	Halt	Halt	1	0	0	0	VCILVLx1.6	2.5Vx1.6
0	0	0	1	Halt	Halt	1	0	0	1	VCILVLx1.65	2.5Vx1.65
0	0	1	0	Halt	Halt	1	0	1	0	VCILVLx1.7	2.5Vx1.7
0	0	1	1	Halt	Halt	1	0	1	1	VCILVLx1.75	2.5Vx1.75
0	1	0	0	Setting disable	Setting disable	1	1	0	0	VCILVLx1.8	2.5Vx1.8
0	1	0	1	Setting disable	Setting disable	1	1	0	1	VCILVLx1.85	2.5Vx1.85
0	1	1	0	Setting disable	Setting disable	1	1	1	0	VCILVLx1.9	2.5Vx1.9
0	1	1	1	Setting disable	Setting disable	1	1	1	1	Setting disable	Setting disable

PON: VDD3OUT ON/OFF control. Set PON = “0” to stop VDD3OUT. Set PON = “1” to start VDD3OUT.

PSON: Power Supply control bit for ON/OFF. When turning on power supply, Set PSE = “1” and Set PSON = “1” to start internal power supply operation..

VREG1R: Select reference voltage for VREG1OUIT

VREG1R = “0” (default): VCILVL (External) as reference voltage for VREG1OUT.

VREG1R = ”1”: VCIR (internal) as reference voltage for VREG1OUT.

VCMR[0]: Select VCOMH external resistance or internal setting for VCOMH voltage level.

VCMR[0] = “0” use VCOMR (External) setting as VCOMH voltage.

VCMR[0] = ”1”: use register (internal) setting as VCOMH voltage.

6.2.17. Power Control 4 (R13h)

R/W	RS	CB15	CB14	CB13	CB12	CB11	CB10	CB9	CB8	CB7	CB6	CB5	CB4	CB3	CB2	CB1	CB0

R/W	RS	CB15	CB14	CB13	CB12	CB11	CB10	CB9	CB8	CB7	CB6	CB5	CB4	CB3	CB2	CB1	CB0
W	1	0	0	0	VDV4	VDV3	VDV2	VDV1	VDV0	0	0	0	0	0	0	0	0

VDV4-0: Set the Vcom amplitude. Vcom amplitude is generated by VREG1OUT.

Table 6-13

VDV4	VDV3	VDV2	VDV1	VDV0	Vcom amplitude
0	0	0	0	0	VREG1OUT x 0.70
0	0	0	0	1	VREG1OUT x 0.72
0	0	0	1	0	VREG1OUT x 0.74
0	0	0	1	1	VREG1OUT x 0.76
0	0	1	0	0	VREG1OUT x 0.78
0	0	1	0	1	VREG1OUT x 0.80
0	0	1	1	0	VREG1OUT x 0.82
0	0	1	1	1	VREG1OUT x 0.84
0	1	0	0	0	VREG1OUT x 0.86
0	1	0	0	1	VREG1OUT x 0.88
0	1	0	1	0	VREG1OUT x 0.90
0	1	0	1	1	VREG1OUT x 0.92
0	1	1	0	0	VREG1OUT x 0.94
0	1	1	0	1	VREG1OUT x 0.96
0	1	1	1	0	VREG1OUT x 0.98
0	1	1	1	1	VREG1OUT x 1.00
1	0	0	0	0	VREG1OUT x 0.94
1	0	0	0	1	VREG1OUT x 0.96
1	0	0	1	0	VREG1OUT x 0.98
1	0	0	1	1	VREG1OUT x 1.00
1	0	1	0	0	VREG1OUT x 1.02
1	0	1	0	1	VREG1OUT x 1.04
1	0	1	1	0	VREG1OUT x 1.06
1	0	1	1	1	VREG1OUT x 1.08
1	1	0	0	0	VREG1OUT x 1.10
1	1	0	0	1	VREG1OUT x 1.12
1	1	0	1	0	VREG1OUT x 1.14
1	1	0	1	1	VREG1OUT x 1.16
1	1	1	0	0	VREG1OUT x 1.18
1	1	1	0	1	VREG1OUT x 1.20
1	1	1	1	0	VREG1OUT x 1.22
1	1	1	1	1	VREG1OUT x 1.24

6.2.18. Power Control 5 (R17h)

R/W	RS	CB15	CB14	CB13	CB12	CB11	CB10	CB9	CB8	CB7	CB6	CB5	CB4	CB3	CB2	CB1	CB0
W	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	PSE

PSE: Power supply enable bit

PSE = “1”, and set PSON can start SPFD5408 power supply system.

PSE = ”0”, power supply system reset. .

6.2.19. GRAM Address Set (Horizontal Address) (R20h)

R/W	RS	CB15	CB14	CB13	CB12	CB11	CB10	CB9	CB8	CB7	CB6	CB5	CB4	CB3	CB2	CB1	CB0
W	1	0	0	0	0	0	0	0	0	AD7	AD6	AD5	AD4	AD3	AD2	AD1	AD0

6.2.20. GRAM Address Set (Vertical Address) (R21h)

R/W	RS	CB15	CB14	CB13	CB12	CB11	CB10	CB9	CB8	CB7	CB6	CB5	CB4	CB3	CB2	CB1	CB0
W	1	0	0	0	0	0	0	0	AD16	AD15	AD14	AD13	AD12	AD11	AD10	AD9	AD8

AD16–0: To set the initial address counter for GRAM address. Based on AM and I/D[1:0] setting, the address counter is automatically increment or decrement while data are written to the internal GRAM There is no need to updated AD16-0 every data transfer if AD16-0 was set in the beginning of one frame graphic data. Be aware that address counter is not automatically updated if reading data from the internal GRAM instruction is executed. Moreover, the address counter cannot be accessed when the SPFD5408A is in standby mode.

Table 6-14 summarized the function of AD15-0 setting

Note1: The address AD16-0 should be set in the address counter every frame on the falling edge of VSYNC if RGB interface mode is selected.

Note2: The address AD16-0 should be set when executing an instruction if system or VSYNC interface mode is selected.

Table 6-14

AD16–AD0	GRAM Setting
“00000”H – “000EF”H	Bitmap data for G1
“00100”H – “001EF”H	Bitmap data for G2
“00200”H – “002EF”H	Bitmap data for G3
“00300”H – “003EF”H	Bitmap data for G4
:	:
“13600”H – “13CEF”H	Bitmap data for G317
“13700”H – “13DEF”H	Bitmap data for G318
“13800”H – “13EEF”H	Bitmap data for G319
“13900”H – “13FEF”H	Bitmap data for G320

6.2.21. Write Data to GRAM (R22h)

R/W	RS	CB15	CB14	CB13	CB12	CB11	CB10	CB9	CB8	CB7	CB6	CB5	CB4	CB3	CB2	CB1	CB0
W	1	RAM write data (WD17-0) The DB17-0 pin assignment is different in different interface modes.															

WD17-0: SPFD5408A supports 18 bits data format. However, if only 16-bit (565format) is input to GRAM, SPFD5408A will expand the 16 bit data into 18-bit format. Same case when RGB interface is selected. Based on the graphic data in GRAM, the grayscale voltage of source driver is selected. **Table 6-15** summarized the source driver grayscale voltage output versus graphic data in GRAM. **Figure 6-8** ~ **Figure 6-18** illustrates the pin assignment among data bus (DB17-0), R22 (WD17-0) and GRAM.

Table 6-15

Data in GRAM	Source Driver Grayscale Output	
RGB	**Negative**	**Positive**
000000	V0	V63
000001	V1	V62
000010	V2	V61
000011	V3	V60
000100	V4	V59
000101	V5	V58
000110	V6	V57
000111	V7	V56
001000	V8	V55
001001	V9	V54
001010	V10	V53
001011	V11	V52
001100	V12	V51
001101	V13	V50
001110	V14	V49
001111	V15	V48
010000	V16	V47
010001	V17	V46
010010	V18	V45
010011	V19	V44
010100	V20	V43
010101	V21	V42
010110	V22	V41
010111	V23	V40
011000	V24	V39
011001	V25	V38
011010	V26	V37
011011	V27	V36
011100	V28	V35
011101	V29	V34
011110	V30	V33
011111	V31	V32
100000	V32	V31
100001	V33	V30
100010	V34	V29
100011	V35	V28
100100	V36	V27
100101	V37	V26
100110	V38	V25
100111	V39	V24
101000	V40	V23
101001	V41	V22
101010	V42	V21
101011	V43	V20
101100	V44	V19
101101	V45	V18
101110	V46	V17
101111	V47	V16
110000	V48	V15
110001	V49	V14
110010	V50	V13
110011	V51	V12
110100	V52	V11
110101	V53	V10
110110	V54	V9
110111	V55	V8
111000	V56	V7
111001	V57	V6
111010	V58	V5
111011	V59	V4
111100	V60	V3
111101	V61	V2
111110	V62	V1
111111	V63	V0

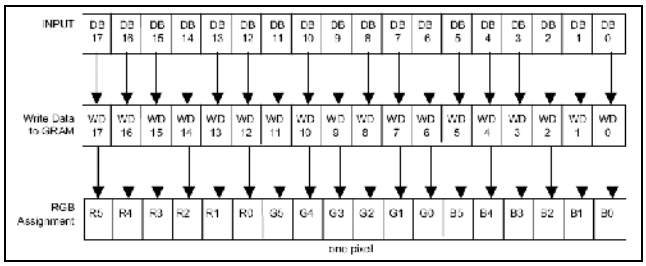


Figure 6-8 18-bit interface (262,144 colors)

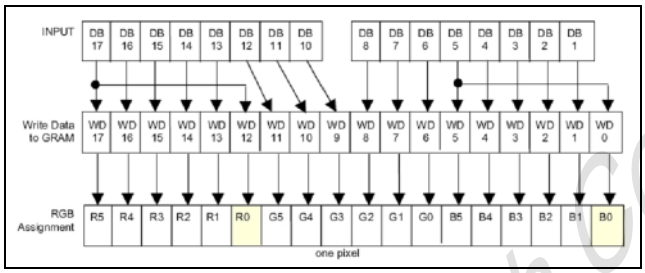


Figure 6-9 16-bit interface(65,536 colors) TRIREG= 0

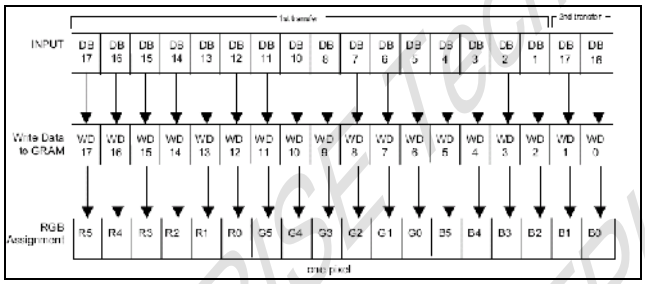


Figure 6-10 16-bit interface(262,144 colors) TRIREG = 1, DFM = 0

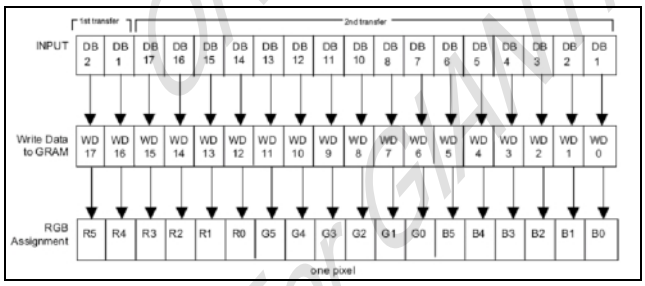


Figure 6-11 16-bit interface(262,144 colors) TRIREG = 1, DFM = 1

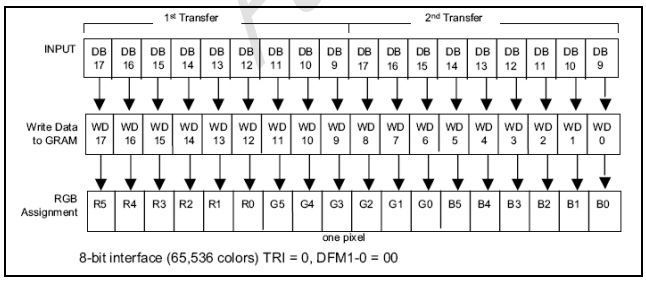


Figure 6-12 9-bit interface (262,144 colors)

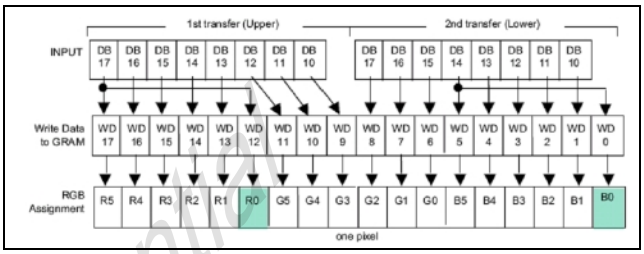


Figure 6-13 8-bit interface (65,536 colors) TRIREG = 0

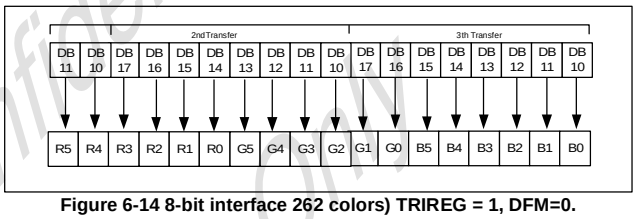


Figure 6-14 8-bit interface 262 colors) TRIREG = 1, DFM=0.

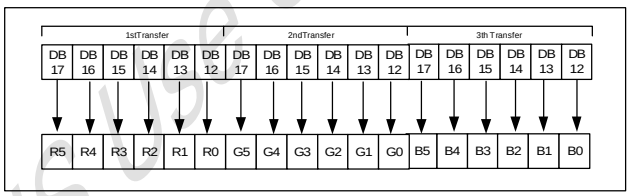


Figure 6-15 8-bit interface (262K colors) TRIREG = 1, DFM=1

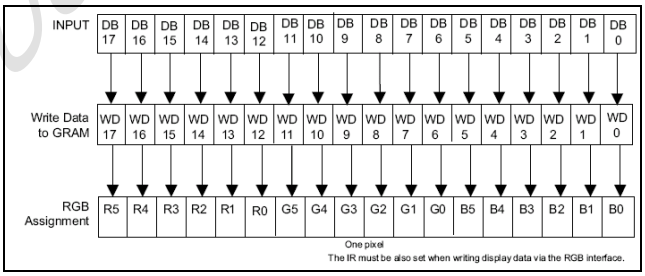


Figure 6-16 18-bit RGB interface (262,144 colors)

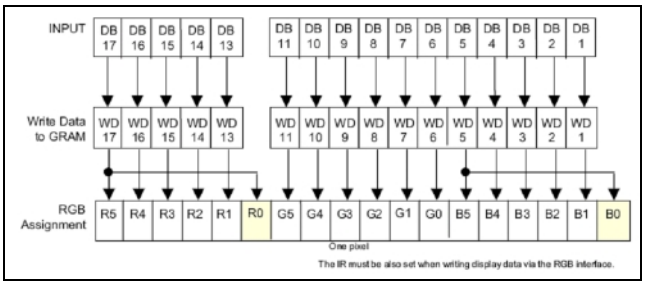


Figure 6-17 16-bit RGB interface (65,563 colors)

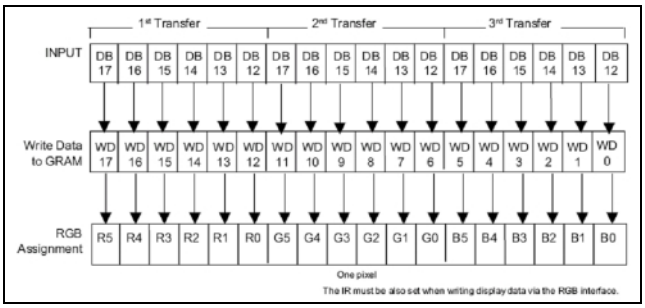


Figure 6-18 6-bit RGB interface (262,144 colors)

SPFD5408A supports external (RGB) interface. In RGB interface mode, all graphic data are stored in GRAM. To meet the diverse requirement of small size LCD panel, SPFD5408A also supports in a fix window using RGB interface and outside the window still use system interface.

In RGB interface mode, data writing to the internal RAM is synchronized with DOTCLK during ENABLE = “Low”. Set ENABLE “High” to terminate writing data to RAM. Wait for a write/read bus cycle time. If accessing internal RAM using the RGB interface is desired after accessing the RAM via the system interface. **Figure 6-19** illustrates the timing diagram while RGB and system interface are both use in the same time.

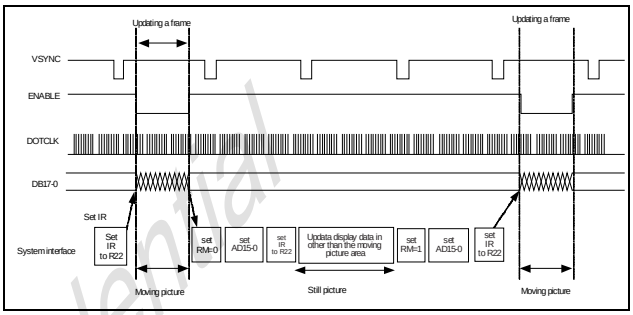


Figure 6-19

6.2.22. Read Data Read from GRAM (R22h)

R/W	RS	CB15	CB14	CB13	CB12	CB11	CB10	CB9	CB8	CB7	CB6	CB5	CB4	CB3	CB2	CB1	CB0
W	1	RAM Read data (RD17-0) The DB17-0 pin assignment is different in different interface modes.															

R22 also served as a register, which store the data read out from GRAM. When data are read out from the GRAM is desired, first sets the RAM address and executes first word read, and issues second word read. When first word read instruction is issued, Invalid data are sent to the data bus DB17-0. Valid data are sent to the data bus as second word data is executed.

The LSBs of R and B dots cannot read out, when the 8 or 16-bit interface is selected,

Note: This register is not available with the RGB interface. **Figure 6-20** and **Figure 6-23** illustrates the pin assignment among data bus (DB17-0), R22 (WD17-0) and GRAM in read data instruction.

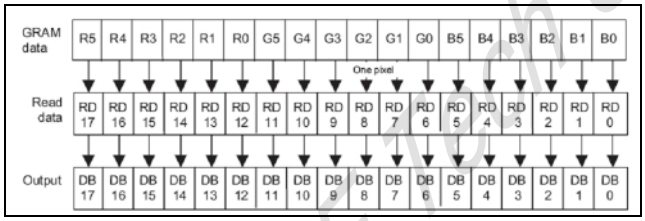


Figure 6-20 18-bit interface

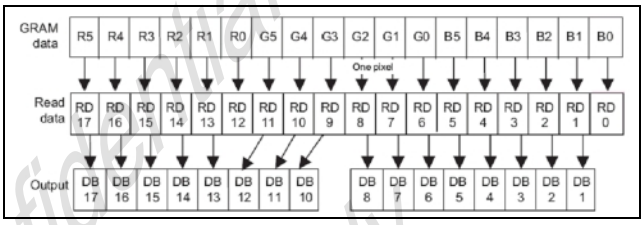


Figure 6-21 16-bit interface

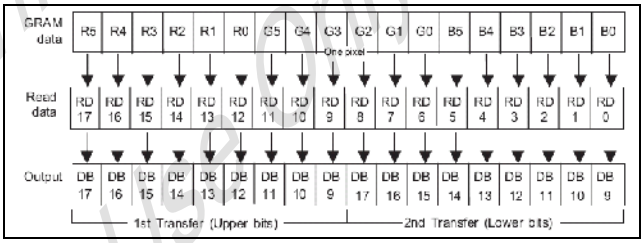


Figure 6-22 9-bit interface

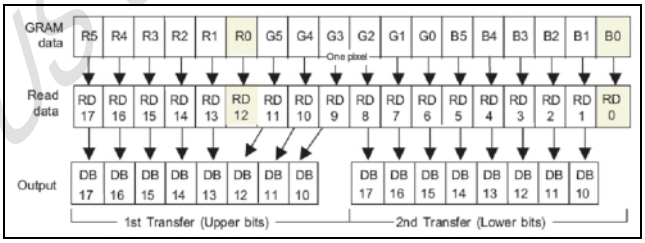


Figure 6-23 8-bit interface / SPI

6.2.23. NVM read data 1 (R28h)

R/W	RS	CB15	CB14	CB13	CB12	CB11	CB10	CB9	CB8	CB7	CB6	CB5	CB4	CB3	CB2	CB1	CB0
W	1	0	0	0	0	0	0	0	0	0	0	0	0	UID3	UID2	UID1	UID0

6.2.24. NVM read data 2 (R29h)

R/W	RS	CB15	CB14	CB13	CB12	CB11	CB10	CB9	CB8	CB7	CB6	CB5	CB4	CB3	CB2	CB1	CB0
W	1	0	0	0	0	0	0	0	0	0	0	0	VCM 14	VCM 13	VCM 12	VCM 11	VCM 10

6.2.25. NVM read data 3 (R2Ah)

R/W	RS	CB15	CB14	CB13	CB12	CB11	CB10	CB9	CB8	CB7	CB6	CB5	CB4	CB3	CB2	CB1	CB0
W	1	0	0	0	0	0	0	0	0	VCM SEL	0	0	VCM 24	VCM 23	VCM 22	VCM 21	VCM 20

UID[3:0]: SPFD5408A provides a 4-bit identification code UID[3:0] for user to use. UID[3:0] can be write / read from NVM. UID can be read out via R28h when CALB(RA4h, CB0) is set to 1.

VCM1[4:0]:

6.2.26. γ Control (R30h to R3Fh)

Table 6-16

	R/W	RS	CB15	CB14	CB13	CB12	CB11	CB10	CB9	CB8	CB7	CB6	CB5	CB4	CB3	CB2	CB1	CB0
R30	W	1	0	0	0	V1RP4	V1RP3	V1RP2	V1RP1	V1RP0	0	0	0	V1RN4	V1RN3	V1RN2	V1RN1	V1RN0
R31	W	1	0	0	V2RP5	V2RP4	V2RP3	V2RP2	V2RP1	V2RP0	0	0	V2RN5	V2RN4	V2RN3	V2RN2	V2RN1	V2RN0
R32	W	1	0	0	V3RP5	V3RP4	V3RP3	V3RP2	V3RP1	V3RP0	0	0	V3RN5	V3RN4	V3RN3	V3RN2	V3RN1	V3RN0
R33	W	1	0	0	V4RP5	V4RP4	V4RP3	V4RP2	V4RP1	V4RP0	0	0	V4RN5	V4RN4	V4RN3	V4RN2	V4RN1	V4RN0
R34	W	1	0	0	V5RP5	V5RP4	V5RP3	V5RP2	V5RP1	V5RP0	0	0	V5RN5	V5RN4	V5RN3	V5RN2	V5RN1	V5RN0
R35	W	1	0	0	0	V6RP4	V6RP3	V6RP2	V6RP1	V6RP0	0	0	0	V6RN4	V6RN3	V6RN2	V6RN1	V6RN0
R36	W	1	0	0	0	V7RP4	V7RP3	V7RP2	V7RP1	V7RP0	0	0	0	V7RN4	V7RN3	V7RN2	V7RN1	V7RN0
R37	W	1	0	0	0	V8RP4	V8RP3	V8RP2	V8RP1	V8RP0	0	0	0	V8RN4	V8RN3	V8RN2	V8RN1	V8RN0
R38	W	1	0	0	0	0	V9RP3	V9RP2	V9RP1	V9RP0	0	0	0	0	V9RN3	V9RN2	V9RN1	V9RN0
R39	W	1	0	0	0	0	V10RP3	V10RP2	V10RP1	V10RP0	0	0	0	0	V10RN3	V10RN2	V10RN1	V10RN0
R3A	W	1	0	0	0	0	V11RP3	V11RP2	V11RP1	V11RP0	0	0	0	0	V11RN3	V11RN2	V11RN1	V11RN0
R3B	W	1	0	0	0	0	V12RP3	V12RP2	V12RP1	V12RP0	0	0	0	0	V12RN3	V12RN2	V12RN1	V12RN0
R3C	W	1	0	0	0	0	V13RP3	V13RP2	V13RP1	V13RP0	0	0	0	0	V13RN3	V13RN2	V13RN1	V13RN0
R3D	W	1	0	0	0	0	V14RP3	V14RP2	V14RP1	V14RP0	0	0	0	0	V14RN3	V14RN2	V14RN1	V14RN0
R3E	W	1	0	0	0	0	V15RP3	V15RP2	V15RP1	V15RP0	0	0	0	0	V15RN3	V15RN2	V15RN1	V15RN0
R3F	W	1	0	0	0	0	V16RP3	V16RP2	V16RP1	V16RP0	0	0	0	0	V16RN3	V16RN2	V16RN1	V16RN0

γ Control (R30h to R3Fh): SPFD5408A provides 16 gamma registers to fine tune gamma output voltage.

V1RP[4:0]: register for positive VSD0 fine tune adjustment.
V2RP[5:0]: register for positive VSD1 fine tune adjustment.
V3RP[5:0]: register for positive VSD2 fine tune adjustment.
V4RP[5:0]: register for positive VSD61 fine tune adjustment.
V5RP[5:0]: register for positive VSD62 fine tune adjustment.
V6RP[4:0]: register for positive VSD63 fine tune adjustment
V7RP[4:0]: register for positive VSD13 fine tune adjustment
V8RP[4:0]: register for positive VSD50 fine tune adjustment
V9RP[3:0]: register for positive VSD4 fine tune adjustment
V10RP[3:0]: register for positive VSD8 fine tune adjustment
V11RP[3:0]: register for positive VSD20 fine tune adjustment
V12RP[3:0]: register for positive VSD27 fine tune adjustment
V13RP[3:0]: register for positive VSD364 fine tune adjustment
V14RP[3:0]: register for positive VSD43 fine tune adjustment
V15RP[3:0]: register for positive VSD55 fine tune adjustment
V16RP[3:0]: register for positive VSD59 fine tune adjustment

V1RN[4:0]: register for negative VSD0 fine tune adjustment.
V2RN[5:0]: register for negative VSD1 fine tune adjustment.
V3RN[5:0]: register for negative VSD2 fine tune adjustment.
V4RN[5:0]: register for negative VSD61 fine tune adjustment.
V5RN[5:0]: register for negative VSD62 fine tune adjustment.
V6RN[4:0]: register for negative VSD63 fine tune adjustment
V7RN[4:0]: register for negative VSD13 fine tune adjustment
V8RN[4:0]: register for negative VSD50 fine tune adjustment
V9RN[3:0]: register for negative VSD4 fine tune adjustment
V10RN[3:0]: register for negative VSD8 fine tune adjustment
V11RN[3:0]: register for negative VSD20 fine tune adjustment
V12RN[3:0]: register for negative VSD27 fine tune adjustment
V13RN[3:0]: register for negative VSD364 fine tune adjustment
V14RN[3:0]: register for negative VSD43 fine tune adjustment
V15RN[3:0]: register for negative VSD55 fine tune adjustment
V16RN[3:0]: register for negative VSD59 fine tune adjustment

6.2.27. Window Horzontal RAM Address Start (R50h)

R/W	RS	CB15	CB14	CB13	CB12	CB11	CB10	CB9	CB8	CB7	CB6	CB5	CB4	CB3	CB2	CB1	CB0
W	1	0	0	0	0	0	0	0	0	HSA7	HSA6	HSA5	HSA4	HSA3	HSA2	HSA1	HSA0

6.2.28. Window Horzontal RAM Address End (R51h)

R/W	RS	CB15	CB14	CB13	CB12	CB11	CB10	CB9	CB8	CB7	CB6	CB5	CB4	CB3	CB2	CB1	CB0
W	1	0	0	0	0	0	0	0	0	HEA7	HEA6	HEA5	HEA4	HEA3	HEA2	HEA1	HEA0

6.2.29. Window Vertical RAM Address Start (R52h)

R/W	RS	CB15	CB14	CB13	CB12	CB11	CB10	CB9	CB8	CB7	CB6	CB5	CB4	CB3	CB2	CB1	CB0
W	1	0	0	0	0	0	0	0	VSA8	VSA7	VSA6	VSA5	VSA4	VSA3	VSA2	VSA1	VSA0

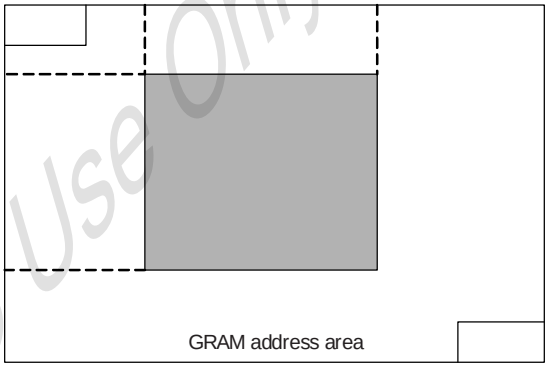
6.2.30. Window Vertical RAM Address End (R53h)

R/W	RS	CB15	CB14	CB13	CB12	CB11	CB10	CB9	CB8	CB7	CB6	CB5	CB4	CB3	CB2	CB1	CB0
W	1	0	0	0	0	0	0	0	VEA8	VEA7	VEA6	VEA5	VEA4	VEA3	VEA2	VEA1	VEA0

HSA7-0/HEA7-0: SPFD5408A provides window access function. Set HSA7-0 and HEA7-0 represent the start address and end address of the window function in horizontal direction. To use window-accessing function, HSA and HEA bits must be set before starting RAM write operation. Be aware that “00”h ≤ HSA7-0< HEA7-0 ≤ “EF”h and HEA-HAS>=”04h”.

VSA8-0/VEA8-0: SPFD5408A provides window access function. Set VSA8-0 and VEA8-0 represent the start address and end address of the window in vertical direction. To use window-accessing function, VSA and VEA bits must be set before starting RAM write operation. Be aware that “00”h ≤ VSA8-0< VEA8-0 ≤ 9’h13F.

Figure 6-24 illustrates the window-accessing function using R44and R45.



6.2.31. Driver Output Control (R60h)

R/W	RS	CB15	CB14	CB13	CB12	CB11	CB10	CB9	CB8	CB7	CB6	CB5	CB4	CB3	CB2	CB1	CB0
W	1	GS	0	NL5	NL4	NL3	NL2	NL1	NL0	0	0	SCN5	SCN4	SCN3	SCN2	SCN1	SCN0

SCN5-0: Set the SCN5-0 bits can specify the starting position of the gate driver. The start position of gate driver is determined by the combination of the setting of GS and SM. **Table 6-17** summarized the starting position for each SCN5-0 setting.

Table 6-17 (whenSM=0)

SCN5	SCN4	SCN3	SCN2	SCN1	SCN0	Scan Start Position (Gate line)	
						GS = “0”	GS = “1”
0	0	0	0	0	0	G1	G320
0	0	0	0	0	1	G9	G312
0	0	0	0	1	0	G17	G304
0	0	0	0	1	1	G25	G296
0	0	0	1	0	0	G33	G288
0	0	0	1	0	1	G41	G280
0	0	0	1	1	0	G49	G272
0	0	0	1	1	1	G57	G264
0	0	1	0	0	0	G65	G256
0	0	1	0	0	1	G73	G248
0	0	1	0	1	0	G81	G240
0	0	1	0	1	1	G89	G232
0	0	1	1	0	0	G97	G224
0	0	1	1	0	1	G105	G216
0	0	1	1	1	0	G113	G208
0	0	1	1	1	1	G121	G200
0	1	0	0	0	0	G129	G192
0	1	0	0	0	1	G137	G184
0	1	0	0	1	0	G145	G176
0	1	0	0	1	1	G153	G168
0	1	0	1	0	0	G161	G160
0	1	0	1	0	1	G169	G152
0	1	0	1	1	0	G177	G144
0	1	0	1	1	1	G185	G136
0	1	1	0	0	0	G193	G128

SC N5	SC N4	SC N3	SC N2	SC N1	SC N0	Scan Start Position (Gate line)	
						GS = "0"	GS = "1"
0	1	1	0	0	1	G201	G120
0	1	1	0	1	0	G209	G112
0	1	1	0	1	1	G217	G104
0	1	1	1	0	0	G225	G96
0	1	1	1	0	1	G233	G88
0	1	1	1	1	0	G241	G80
0	1	1	1	1	1	G249	G72
1	0	0	0	0	0	G257	G64
1	0	0	0	0	1	G265	G56
1	0	0	0	1	0	G273	G48
1	0	0	0	1	1	G281	G40
1	0	0	1	0	0	G289	G32
1	0	0	1	0	1	G297	G24
1	0	0	1	1	0	G305	G16
1	0	0	1	1	1	G313	G8
1	0	1	0	0	0	Setting disable	
Setting disable							
1	1	1	1	1	1	Setting	

NL5-0: NL4-0: Set the number of gate lines for different resolution of display panel. The combination of NL4-NL0 represents the gate line number are summarized at **Table 6-18**

Table 6-18

NL5	NL4	NL3	NL2	NL1	NL0	Display Size	Lines	Driven gate lines
0	0	0	0	0	0	Setting disabled	Setting disabled	Setting disabled
Setting disable								
0	1	0	1	0	1	720 x 176 dots	176	G1 ~ G176
Setting disable								
0	1	1	1	0	1	720 x 240 dots	240	G1 ~ G240
0	1	1	1	1	0	720 x 248 dots	248	G1 ~ G248
0	1	1	1	1	1	720 x 256 dots	256	G1 ~ G256
1	0	0	0	0	0	720 x 264 dots	264	G1 ~ G264
1	0	0	0	0	1	720 x 272 dots	272	G1 ~ G272
1	0	0	0	1	0	720 x 280 dots	280	G1 ~ G280
1	0	0	0	1	1	720 x 288 dots	288	G1 ~ G288
1	0	0	1	0	0	720 x 296 dots	296	G1 ~ G296
1	0	0	1	0	1	720 x 304 dots	304	G1 ~ G304
1	0	0	1	1	0	720 x 312 dots	312	G1 ~ G312
1	0	0	1	1	1	720 x 320 dots	320	G1 ~ G320
Setting disable								

Note: Back porch and a front porch (set with BP/FP bits respectively) are inserted before/ after driving all gate lines,

GS: Shift direction of the gate driver output selection. When

GS="0", gate driver shift from G1 to G320. When GS = "1", gate driver shift from G320 to G1.

6.2.32. Driver Output Control (R61h)

R/W	RS	CB15	CB14	CB13	CB12	CB11	CB10	CB9	CB8	CB7	CB6	CB5	CB4	CB3	CB2	CB1	CB0
W	1	0	0	0	0	0	0	0	0	0	0	0	0	0	NDL	VLE	REV

REV: To set the grayscale corresponding to normally white or normally black LCD panel from same data input.

Table 6-30 summarized REV bit function.

Table 6-30

REV	GRAM data	Source Driver Output	
		Positive Polarity	Negative Polarity
0	18'h00000 ' 18'h3FFFF	V63 ' V0	V0 ' V63
1	18'h00000 ' 18'h3FFFF	V0 ' V63	V63 ' V0

VLE: SPFD5408 provides vertical scrolling function which can be set by VLE bit.

VLE = "1", vertical scrolling function enable. The amout of scrolling line from the first line is determined by VL[8:0].

VLE = "0", normal display.

NDL: set the source duiver output level in non-lit area..

NDL = "1", .

NDL = "0", .

6.2.33. Vertical Scroll Control (R6Ah)

R/W	RS	CB15	CB14	CB13	CB12	CB11	CB10	CB9	CB8	CB7	CB6	CB5	CB4	CB3	CB2	CB1	CB0
W	1	0	0	0	0	0	0	0	VL8	VL7	VL6	VL5	VL4	VL3	VL2	VL1	VL0

VL8-0: SPFD5408A provides scrolling function. The start position for displaying the image is shifted vertically by the number of lines based on the setting of the VL8-0 bits. Be aware that the vertical scrolling function is not available in the external (RGB) display interface mode. **Table 6-31** summarized the function of VL8-0 setting.

Table 6-31

VL8	VL7	VL6	VL5	VL4	VL3	VL2	VL1	VL0	Scrolling lines
0	0	0	0	0	0	0	0	0	0 line
0	0	0	0	0	0	0	0	1	1 line
0	0	0	0	0	0	0	1	0	2 lines
	:	:	:	:	:	:	:	:	:
1	0	0	1	1	1	1	1	1	319 lines
1	0	1	0	0	0	0	0	0	320 lines

Note: VL8-0 bits cannot set more than 320 lines.

6.2.34. Display Position – Partial Display 1 (R80h)

R/W	RS	CB15	CB14	CB13	CB12	CB11	CB10	CB9	CB8	CB7	CB6	CB5	CB4	CB3	CB2	CB1	CB0
W	1	0	0	0	0	0	0	0	PTD P08	PTD P07	PTD P06	PTD P05	PTD P04	PTD P03	PTD P02	PTD P01	PTD P00

6.2.35. RAM Address Start – Partial Display 1 (R81h)

R/W	RS	CB15	CB14	CB13	CB12	CB11	CB10	CB9	CB8	CB7	CB6	CB5	CB4	CB3	CB2	CB1	CB0
W	1	0	0	0	0	0	0	0	PTS A08	PTS A07	PTS A06	PTS A05	PTS A04	PTS A03	PTS A02	PTS A01	PTS A00

6.2.36. RAM address End – Partail Display 1 (R82h)

R/W	RS	CB15	CB14	CB13	CB12	CB11	CB10	CB9	CB8	CB7	CB6	CB5	CB4	CB3	CB2	CB1	CB0
W	1	0	0	0	0	0	0	0	PTE A08	PTE A07	PTE A06	PTE A05	PTE A04	PTE A03	PTE A02	PTE A01	PTE A00

6.2.37. Display Position – Partial Display 2 (R83h)

R/W	RS	CB15	CB14	CB13	CB12	CB11	CB10	CB9	CB8	CB7	CB6	CB5	CB4	CB3	CB2	CB1	CB0
W	1	0	0	0	0	0	0	0	PTDP18	PTDP17	PTDP16	PTDP15	PTDP14	PTDP13	PTDP12	PTDP11	PTDP10

6.2.38. RAM Address Start – Partial Display 2 (R84h)

R/W	RS	CB15	CB14	CB13	CB12	CB11	CB10	CB9	CB8	CB7	CB6	CB5	CB4	CB3	CB2	CB1	CB0
W	1	0	0	0	0	0	0	0	PTSA18	PTSA17	PTSA16	PTSA15	PTSA14	PTSA13	PTSA12	PTSA11	PTSA10

6.2.39. RAM Address End – Partial Display 2 (R85h)

R/W	RS	CB15	CB14	CB13	CB12	CB11	CB10	CB9	CB8	CB7	CB6	CB5	CB4	CB3	CB2	CB1	CB0
W	1	0	0	0	0	0	0	0	PTEA18	PTEA17	PTEA16	PTEA15	PTEA14	PTEA13	PTEA12	PTEA11	PTEA10

PTDP0[8:0]: Set the physical starting position of partial display 1 on the LCD panel

PTDP1[8:0]: Set the physical starting position of partial display 2 on the LCD panel

The partial display 1 and partial display 2 should not overlap with each other. And make sure the PTDP0[8:0] < PTDP1[8:0].

PTSA0[8:0]: Set the start line address of display RAM of partial display 1 which will be display according to PTDP0[8:0].

PTEA0[8:0]: Set the end line address of display RAM of partial display 1 which will be display according to PTDP0[8:0].

Make sure PTSA0<=PTEA0

PTSA1[8:0]: Set the start line address of display RAM of partial display2 which will be display according to PTDP1[8:0].

PTEA1[8:0]: Set the end line address of display RAM of partial display2 which will be display according to PTDP1[8:0]

Make sure PTSA1<=PTEA1

6.2.40. Frame Cycle Control (R90h)

R/W	RS	CB15	CB14	CB13	CB12	CB11	CB10	CB9	CB8	CB7	CB6	CB5	CB4	CB3	CB2	CB1	CB0
W	1	0	0	0	0	0	0	DIV1	DIV0	0	0	0	RTN4	RTN3	RTN2	RTN1	RTN0

RTN3-0: Set the clock cycle per line **Table 6-19** summarized the function of RTN3-0 setting.

Table 6-19

RTN4	RTN3	RTN2	RTN1	RTN0	Clock Cycles per line
0	0	0	0	0	Setting disable
Setting disable					
1	0	0	0	0	16 clocks
1	0	0	0	1	17 clocks
1	0	0	1	0	18 clocks
1	0	0	1	1	19 clocks
1	0	1	0	0	20 clocks
1	0	1	0	1	21 clocks
1	0	1	1	0	22 clocks
1	0	1	1	1	23 clocks
1	1	0	0	0	24 clocks

RTN4	RTN3	RTN2	RTN1	RTN0	Clock Cycles per line
1	1	0	0	1	25 clocks
1	1	0	1	0	26 clocks
1	1	0	1	1	27 clocks
1	1	1	0	0	28 clocks
1	1	1	0	1	29 clocks
1	1	1	1	0	30 clocks
1	1	1	1	1	31 clocks

DIV1-0: To specified the division ratio of internal operation clock frequency. Set the RTN and DIV bits to adjust frame frequency. Be aware of that if the number of lines for driving liquid crystal is changed, the frame frequency must also be adjusted. Moreover, In RGB interface mode, the DIV1-0 bits are disabled. **Table 6-20** summarized the function of DIV1-0 setting.

Table 6-20

DIV1	DIV0	Division Ratio	Internal Operation Clock Frequency
0	0	1	fosc / 1
0	1	2	fosc / 2
1	0	4	fosc / 4
1	1	8	fosc / 8

fosc =Frequency of RC oscillation

Formula to calculate frame frequency

$$\text{Frame frequency} = \frac{fosc}{\text{Clock cycles per line} \times \text{division ratio} \times (\text{Line} + \text{BP} + \text{FP})} \quad [\text{Hz}]$$

fosc: frequency of RC oscillation

Line: number of lines for driving liquid crystal (NL bits)

Division ratio: DIV bits

Clock cycles per line: RTN bits

FP: the number of lines for the front porch period

BP: the number of lines for the back porch period

6.2.41. Panel Interface Control 2 (R92h)

R/W	RS	CB15	CB14	CB13	CB12	CB11	CB10	CB9	CB8	CB7	CB6	CB5	CB4	CB3	CB2	CB1	CB0
W	1	0	0	0	0	0	NOWI2	NOWI1	NOWI0	0	0	0	0	0	0	0	0

NOWI [2:0]: Set the adjacent gate driver output non-overlap period. **Table 6-21** summarized the function of NO1-0 setting.

Table 6-21

NOWI2	NOW!1	NOWI0	Gate output non-overlap period Internal Operation (reference clock: internal oscillator)
0	0	0	0 clock
0	0	1	1 clocks
0	1	0	2 clocks
0	1	1	3 clocks
1	0	0	4 clocks
1	0	1	5 clocks
1	1	0	6 clocks
1	1	1	7 clocks

6.2.42. Panel Interface control 3 (R93h)

R/W	RS	CB15	CB14	CB13	CB12	CB11	CB10	CB9	CB8	CB7	CB6	CB5	CB4	CB3	CB2	CB1	CB0
W	1	0	0	0	0	0	0	VEQW11	VEQW10						MCPI2	MCPI1	MCPI0

MCPI[2:0]: Set source driver start output timing. The source driver output position is measure from internal reference point.

MCPE2	MCPE1	MCPE0	Source driver start output position
0	0	0	0 clock
0	0	1	1 clocks
0	1	0	2 clocks
0	1	1	3 clocks
1	0	0	4 clocks
1	0	1	5 clocks
1	1	0	6 clocks
1	1	1	7 clocks

VEQW1[1:0]: Set VCOM equalize period.

VEQW1	VEQW0	VCOM Equalize Period
0	0	0 clock
0	1	1 clock
1	0	2 clocks
1	1	3 clocks

6.2.43. Frame Cycle Control (R95h)

R/W	RS	CB15	CB14	CB13	CB12	CB11	CB10	CB9	CB8	CB7	CB6	CB5	CB4	CB3	CB2	CB1	CB0
W	1	0	0	0	0	0	0	DIVE1	DIVE0	0	0	RTNE5	RTNE4	RTNE3	RTNE2	RTNE1	RTNE0

RTNE5-0: Set the clock cycle per line **Table 6-19** summarized the function of RTN3-0 setting.

Table 6-22

RTN4	RTN3	RTN2	RTN1	RTN0	Clock Cycles per line
0	0	0	0	0	Setting disable
Setting disable					
1	0	0	0	0	16 clocks
1	0	0	0	1	17 clocks
1	0	0	1	0	18 clocks
1	0	0	1	1	19 clocks
1	0	1	0	0	20 clocks
1	0	1	0	1	21 clocks
1	0	1	1	0	22 clocks
1	0	1	1	1	23 clocks
1	1	0	0	0	24 clocks
1	1	0	0	1	25 clocks
1	1	0	1	0	26 clocks
1	1	0	1	1	27 clocks
1	1	1	0	0	28 clocks
1	1	1	0	1	29 clocks
1	1	1	1	0	30 clocks
1	1	1	1	1	31 clocks

DIV1-0: To specified the division ratio of internal operation clock frequency. Set the RTN and DIV bits to adjust frame frequency. Be aware of that if the number of lines for driving liquid crystal is changed, the frame frequency must also be adjusted. Moreover, In RGB interface mode, the DIV1-0 bits are disabled. **Table 6-20** summarized the function of DIV1-0 setting.

Table 6-23

DIV1	DIV0	Division Ratio	Internal Operation Clock Frequency
0	0	1	fosc / 1
0	1	2	fosc / 2
1	0	4	fosc / 4
1	1	8	fosc / 8

fosc =Frequency of RC oscillation

6.2.44. Panel Interface Control 5 (R97h)

R/W	RS	CB15	CB14	CB13	CB12	CB11	CB10	CB9	CB8	CB7	CB6	CB5	CB4	CB3	CB2	CB1	CB0
W	1	0	0	0	0	NOWE3	NOWE2	NOWE1	NOWE0	0	0	0	0	0	0	0	0

NOWE [3:0]: Set the adjacent gate driver output non-overlap period inRGB interface. **Table 6-21** summarized the function of NO1-0 setting.

Table 6-24

NOWE3	NOWE2	NOWE1	NOWE0	Gate output non-overlap period Internal Operation (reference clock: internal oscillator)
0	0	0	0	0 clock
0	0	0	1	1 clocks
0	0	1	0	2 clocks
0	0	1	1	3 clocks
0	1	0	0	4 clocks
0	1	0	1	5 clocks
0	1	1	0	6 clocks
0	1	1	1	7 clocks
1	0	0	0	8 clocks
1	0	0	1	9 clocks
1	0	1	0	10 clocks
1	0	1	1	11 clocks
1	1	0	0	12 clocks
1	1	0	1	13 clocks
1	1	1	0	14 clocks
1	1	1	1	15 clocks

6.2.45. Panel Interface Control (R98h)

R/W	RS	CB15	CB14	CB13	CB12	CB11	CB10	CB9	CB8	CB7	CB6	CB5	CB4	CB3	CB2	CB1	CB0
W	1	0	0	0	0	0	0	0	0	0	0	0	0	0	MCPE2	MCPE1	MCPE0

MCPE[2:0]: Set source driver start output timing in RGB interface. The source driver output position is measure from internal reference point.

MCPE2	MCPE1	MCPE0	Source driver start output position
0	0	0	0 clock
0	0	1	1 clocks
0	1	0	2 clocks
0	1	1	3 clocks
1	0	0	4 clocks
1	0	1	5 clocks
1	1	0	6 clocks
1	1	1	7 clocks

6.2.46. Calibration Control (RA4h)

R/W	RS	CB15	CB14	CB13	CB12	CB11	CB10	CB9	CB8	CB7	CB6	CB5	CB4	CB3	CB2	CB1	CB0
W	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	CALB

CALB: .the enable bit for the read function of the NVM.

When CALB=”1”: Read function from NVM is enable.

When CALB=”0”: Read function from NVMis disable.

7. GRAM

Table 7-1 GRAM address and display panel position (SS = “0”)

S/G pin		S1	S2	S3	S4	S5	S6	S7	S8	S9	S10	S11	S12	….	S709	S710	S711	S712	S713	S714	S715	S716	S717	S718	S719	S720
GS=0	GS=1	DB17-0			DB17-0			DB17-0			DB17-0			….	DB17-0			DB17-0			DB17-0			DB17-0		
G1	G320	“00000"H			“00001"H			“00002"H			“00003"H			….	“000EC"H			"000ED"H			"000EE"H			"000EF"H		
G2	G319	"00100"H			"00101"H			"00102"H			"00103"H			….	"001EC"H			"001ED"H			"001EE"H			"001EF"H		
G3	G318	"00200"H			"00201"H			"00202"H			"00203"H			….	"002EC"H			"002ED"H			"002EE"H			"002EF"H		
G4	G317	"00300"H			"00301"H			"00302"H			"00303"H			….	"003EC"H			"003ED"H			"003EE"H			"003EF"H		
G5	G316	"00400"H			"00401"H			"00402"H			"00403"H			….	"004EC"H			"004ED"H			"004EE"H			"004EF"H		
G6	G315	"00500"H			"00501"H			"00502"H			"00503"H			….	"005EC"H			"005ED"H			"005EE"H			"005EF"H		
G7	G314	"00600"H			"00601"H			"00602"H			"00603"H			….	"006EC"H			"06ED"H			"06EE"H			"06EF"H		
G8	G313	"00700"H			"00701"H			"00702"H			"00703"H			….	“007EC"H			“007ED"H			“007EE"H			“007EF"H		
G9	G312	“00800"H			“00801"H			“00802"H			“00803"H			….	“008EC"H			“008ED"H			“008EE"H			“008EF"H		
G10	G311	“00900"H			“00901"H			“00902"H			“00903"H			….	“009EC"H			“009ED"H			“009EE"H			“009EF"H		
G11	G310	“00E00"H			“00E01"H			“00E02"H			“00E03"H			….	“00EEC"H			“00EED"H			“00EEE"H			“00EEF"H		
G12	G309	“00B00"H			“00B01"H			“00B02"H			“00B03"H			….	“00BEC"H			“00BED"H			“00BEE"H			“00BEF"H		
G13	G308	“00C00"H			“00C01"H			“00C02"H			“00C03"H			….	“00CEC"H			“00CED"H			“00CEE"H			“00CEF"H		
G14	G307	“00D00"H			“00D01"H			“00D02"H			“00D03"H			….	“00DEC"H			“00DED"H			“00DEE"H			“00DEF"H		
G15	G306	“00E00"H			“00E01"H			“00E02"H			“00E03"H			….	“00EEC"H			“00EED"H			“00EEE"H			“00EEF"H		
G16	G305	“00F00"H			“00F01"H			“00F02"H			“00F03"H			….	“00FEC"H			“00FED"H			“00FEE"H			“00FEF"H		
G17	G304	“01000"H			“01001"H			“01002"H			“01003"H			….	“010EC"H			“010ED"H			“010EE"H			“010EF"H		
G18	G303	“01100"H			“01101"H			“01102"H			“01103"H			….	“011EC"H			“011ED"H			“011EE"H			“011EF"H		
G19	G302	“01200"H			“01201"H			“01202"H			“01203"H			….	“012EC"H			“012ED"H			“012EE"H			“012EF"H		
G20	G301	“01300"H			“01301"H			“01302"H			“01303"H			….	“013EC"H			“013ED"H			“013EE"H			“013EF"H		
:	:	:			:			:			:				:			:			:			:		
:	:	:			:			:			:				:			:			:			:		
G313	G8	“13800"H			“13801"H			“13802"H			“13803"H			….	“138EC"H			“138ED"H			“138EE"H			“138EF"H		
G314	G7	“13900"H			“13901"H			“13902"H			“13903"H			….	“139EC"H			“139ED"H			“139EE"H			“139EF"H		
G315	G6	“13A00"H			“13A01"H			“13A02"H			“13A03"H			….	“13AEC"H			“13AED"H			“13AEE"H			“13AEF"H		
G316	G5	“13B00"H			“13B01"H			“13B02"H			“13B03"H			….	“13BEC"H			“13BED"H			“13BEE"H			“13BEF"H		
G317	G4	“13C00"H			“13C01"H			“13C02"H			“13C03"H			….	“13CEC"H			“13CED"H			“13CEE"H			“13CEF"H		
G318	G3	“13D00"H			“13D01"H			“13D02"H			“13D03"H			….	“13DEC"H			“13DED"H			“13DEE"H			“13DEF"H		
G319	G2	“13E00"H			“13E01"H			“13E02"H			“13E03"H			….	“13EEC"H			“13EED"H			“13EEE"H			“13EEF"H		
G320	G1	“13F00"H			“13F01"H			“13F02"H			“13F03"H			….	“13FEC"H			“13FED"H			“13FEE"H			“13FEF"H		

Table 7-2 GRAM address and display panel position (SS = "1")

S/G pin		S1	S2	S3	S4	S5	…	S7	S8	S9	S10	S11	S12	….	S709	S710	S711	S712	S713	S714	S715	S716	S717	S718	S719	S720
GS=0	GS=1	DB17-0			DB17-0			DB17-0			DB17-0			….	DB17-0			DB17-0			DB17-0			DB17-0		
G1	G320	"000EF"H			"000EE"H			"000ED"H			"000EC"H			….	"00003"H			"00002"H			"00001"H			"00000"H		
G2	G319	"001EF"H			"001EE"H			"001ED"H			"001EC"H			….	"00103"H			"00102"H			"00101"H			"00100"H		
G3	G318	"002EF"H			"002AE"H			"002ED"H			"002EC"H			….	"00203"H			"00202"H			"00201"H			"00200"H		
G4	G317	"003EF"H			"003EE"H			"003ED"H			"003EC"H			….	"00303"H			"00302"H			"00301"H			"00300"H		
G5	G316	"004EF"H			"004EE"H			"004ED"H			"004EC"H			….	"00403"H			"00402"H			"00401"H			"00400"H		
G6	G315	"005EF"H			"005EE"H			"005ED"H			"005EC"H			….	"00503"H			"00502"H			"00501"H			"00500"H		
G7	G314	"006EF"H			"006EE"H			"006ED"H			"006EC"H			….	"00603"H			"00602"H			"00601"H			"00600"H		
G8	G313	"007EF"H			"007EE"H			"007ED"H			"007EC"H			….	"00703"H			"00702"H			"00701"H			"00700"H		
G9	G312	"008EF"H			"008EE"H			"008ED"H			"008EC"H			….	"00803"H			"00802"H			"00801"H			"00800"H		
G10	G311	"009EF"H			"009EE"H			"009ED"H			"009EC"H			….	"00903"H			"00902"H			"00901"H			"00900"H		
G11	G310	"00AEF"H			"00AEE"H			"00AED"H			"00AEC"H			….	"00E03"H			"00A02"H			"00A01"H			"00A00"H		
G12	G309	"00BEF"H			"00BEE"H			"00BED"H			"00BEC"H			….	"00B03"H			"00B02"H			"00B01"H			"00B00"H		
G13	G308	"00CEF"H			"00CEE"H			"00CED"H			"00CEC"H			….	"00C03"H			"00C02"H			"00C01"H			"00C00"H		
G14	G307	"00DEF"H			"00DEE"H			"00DED"H			"00DEC"H			….	"00D03"H			"00D02"H			"00D01"H			"00D00"H		
G15	G306	"00EEF"H			"00EEE"H			"00EED"H			"00EEC"H			….	"00E03"H			"00E02"H			"00E01"H			"00E00"H		
G16	G305	"00FEF"H			"00FEE"H			"00FED"H			"00FEC"H			….	"00F03"H			"00F02"H			"00F01"H			"00F00"H		
G17	G304	"010EF"H			"010EE"H			"010ED"H			"010EC"H			….	"01003"H			"01002"H			"01001"H			"01000"H		
G18	G303	"011EF"H			"011EE"H			"011ED"H			"011EC"H			….	"01103"H			"01102"H			"01101"H			"01100"H		
G19	G302	"012EF"H			"012EE"H			"012ED"H			"012EC"H			….	"01203"H			"01202"H			"01201"H			"01200"H		
G20	G301	"013EF"H			"013EE"H			"013ED"H			"013EC"H			….	"01303"H			"01302"H			"01301"H			"01300"H		
:	:	:			:			:			:				:			:			:			:		
:	:	:			:			:			:				:			:			:			:		
G233	G8	"E8EF"H			"138EE"H			"138ED"H			"138EC"H			….	"13803"H			"13802"H			"13801"H			"13800"H		
G234	G7	"139EF"H			"139EE"H			"139ED"H			"139EC"H			….	"13903"H			"13902"H			"13901"H			"13900"H		
G235	G6	"13AEF"H			"13AEE"H			"13AED"H			"13AEC"H			….	"13A03"H			"13A02"H			"13A01"H			"13A00"H		
G236	G5	"13BEF"H			"13BEE"H			"13BED"H			"13BEC"H			….	"13B03"H			"13B02"H			"13B01"H			"13B00"H		
G237	G4	"13CEF"H			"13CEE"H			"13CED"H			"13CEC"H			….	"13C03"H			"13C02"H			"13C01"H			"13C00"H		
G238	G3	"13DEF"H			"13DEE"H			"13DED"H			"13DEC"H			….	"13D03"H			"13D02"H			"13D01"H			"13D00"H		
G239	G2	"13EEF"H			"13EEE"H			"13EED"H			"13EEC"H			….	"13E03"H			"13E02"H			"13E01"H			"13E00"H		
G240	G1	"13FEF"H			"13FEE"H			"13FED"H			"13FEC"H			….	"13F03"H			"13F02"H			"13F01"H			"13F00"H		

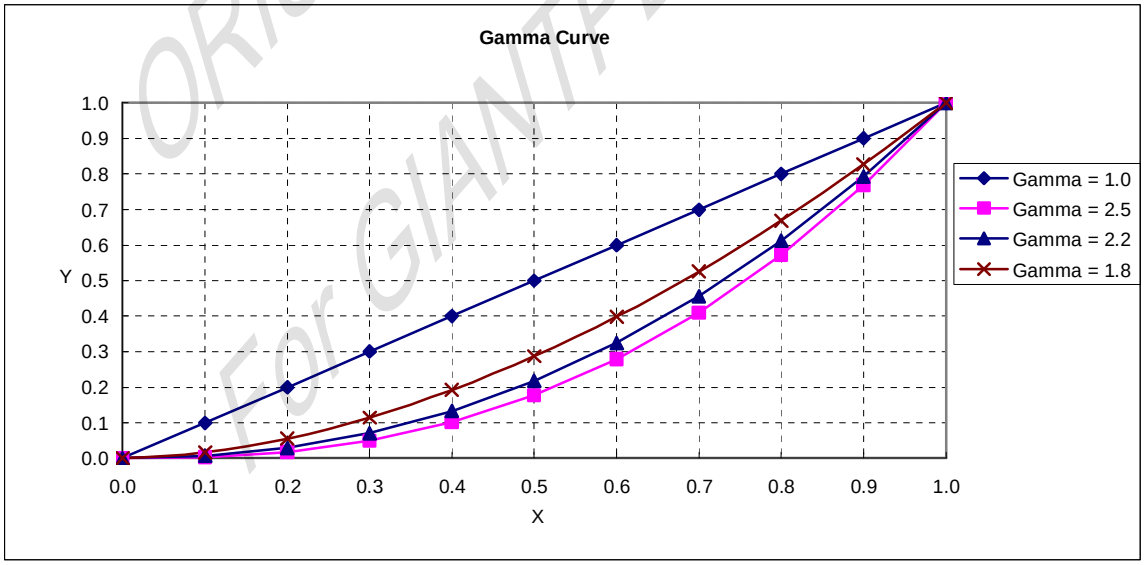
10.5. Gamma Correction function:

SPFD54508A adopt Gamma voltage generation circuit which can provide wider output voltage range to fit the difrerent kind of liquid crystal for Gamma curve from 1.0~2.5. The Gamma output voltage can be set by R30h!~R3Fh.

V1RP[4:0]: register for positive VSD0 fine tune adjustment.
V2RP[5:0]: register for positive VSD1 fine tune adjustment.
V3RP[5:0]: register for positive VSD2 fine tune adjustment.
V4RP[5:0]: register for positive VSD61 fine tune adjustment.
V5RP[5:0]: register for positive VSD62 fine tune adjustment.
V6RP[4:0]: register for positive VSD63 fine tune adjustment
V7RP[4:0]: register for positive VSD13 fine tune adjustment
V8RP[4:0]: register for positive VSD50 fine tune adjustment
V9RP[3:0]: register for positive VSD4 fine tune adjustment
V10RP[3:0]: register for positive VSD8 fine tune adjustment
V11RP[3:0]: register for positive VSD20 fine tune adjustment
V12RP[3:0]: register for positive VSD27 fine tune adjustment
V13RP[3:0]: register for positive VSD364 fine tune adjustment
V14RP[3:0]: register for positive VSD43 fine tune adjustment
V15RP[3:0]: register for positive VSD55 fine tune adjustment
V16RP[3:0]: register for positive VSD59 fine tune adjustment

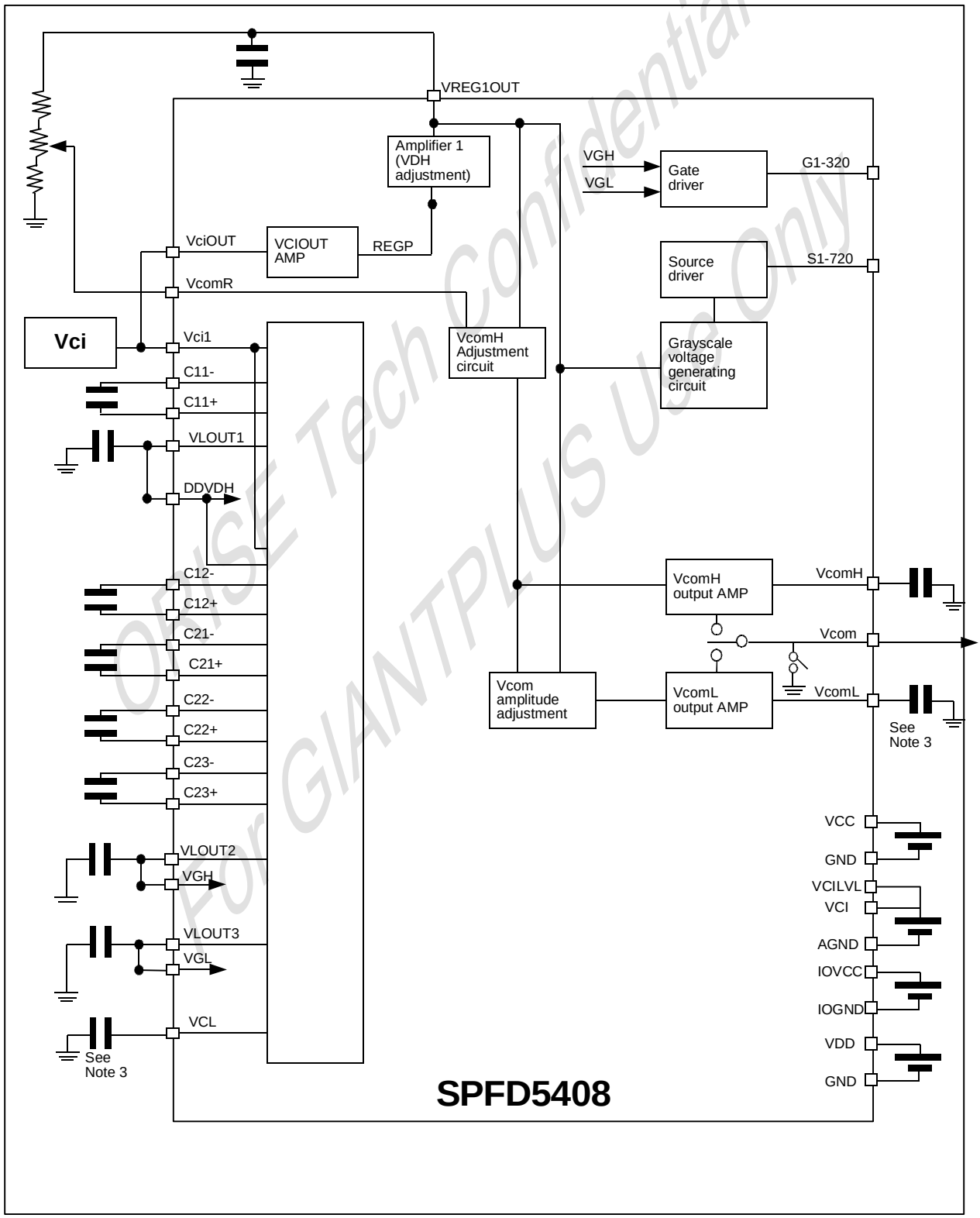
V1RN[4:0]: register for negative VSD0 fine tune adjustment.
V2RN[5:0]: register for negative VSD1 fine tune adjustment.
V3RN[5:0]: register for negative VSD2 fine tune adjustment.
V4RN[5:0]: register for negative VSD61 fine tune adjustment.
V5RN[5:0]: register for negative VSD62 fine tune adjustment.
V6RN[4:0]: register for negative VSD63 fine tune adjustment
V7RN[4:0]: register for negative VSD13 fine tune adjustment
V8RN[4:0]: register for negative VSD50 fine tune adjustment
V9RN[3:0]: register for negative VSD4 fine tune adjustment
V10RN[3:0]: register for negative VSD8 fine tune adjustment
V11RN[3:0]: register for negative VSD20 fine tune adjustment
V12RN[3:0]: register for negative VSD27 fine tune adjustment
V13RN[3:0]: register for negative VSD364 fine tune adjustment
V14RN[3:0]: register for negative VSD43 fine tune adjustment
V15RN[3:0]: register for negative VSD55 fine tune adjustment
V16RN[3:0]: register for negative VSD59 fine tune adjustment

Figure 10.5.1 illustrated 4 diffrerent Gamma Curve.

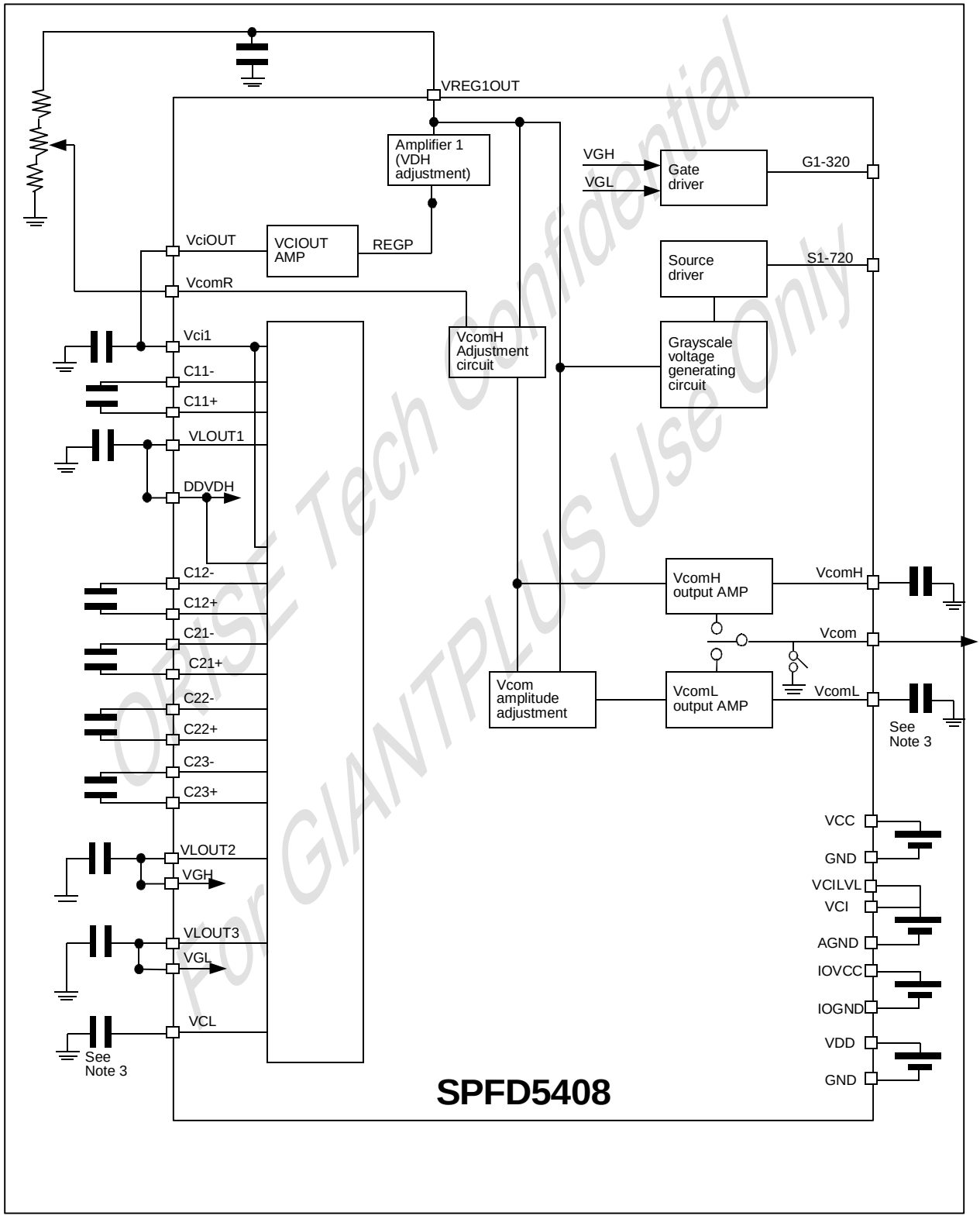


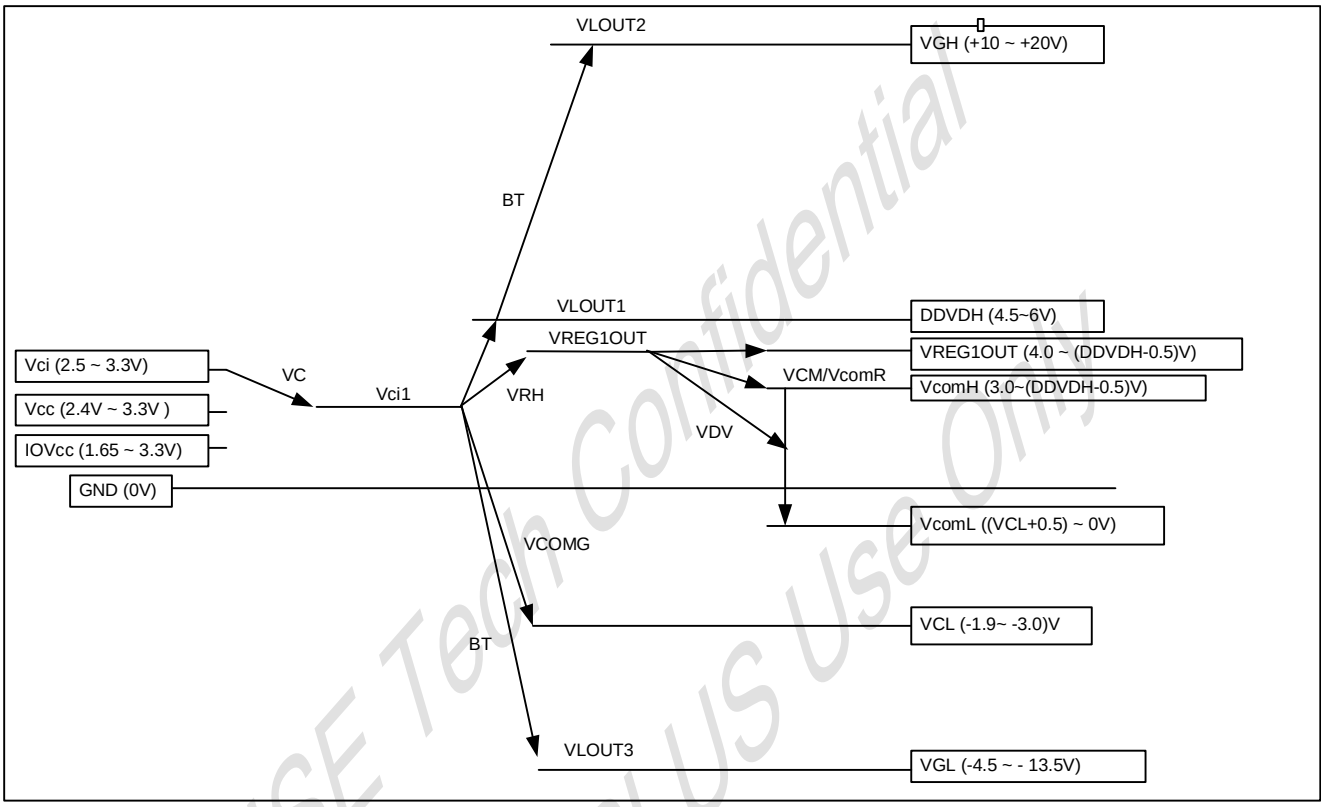
11. Power Management System:

(a) VCI1=VCI direct input:

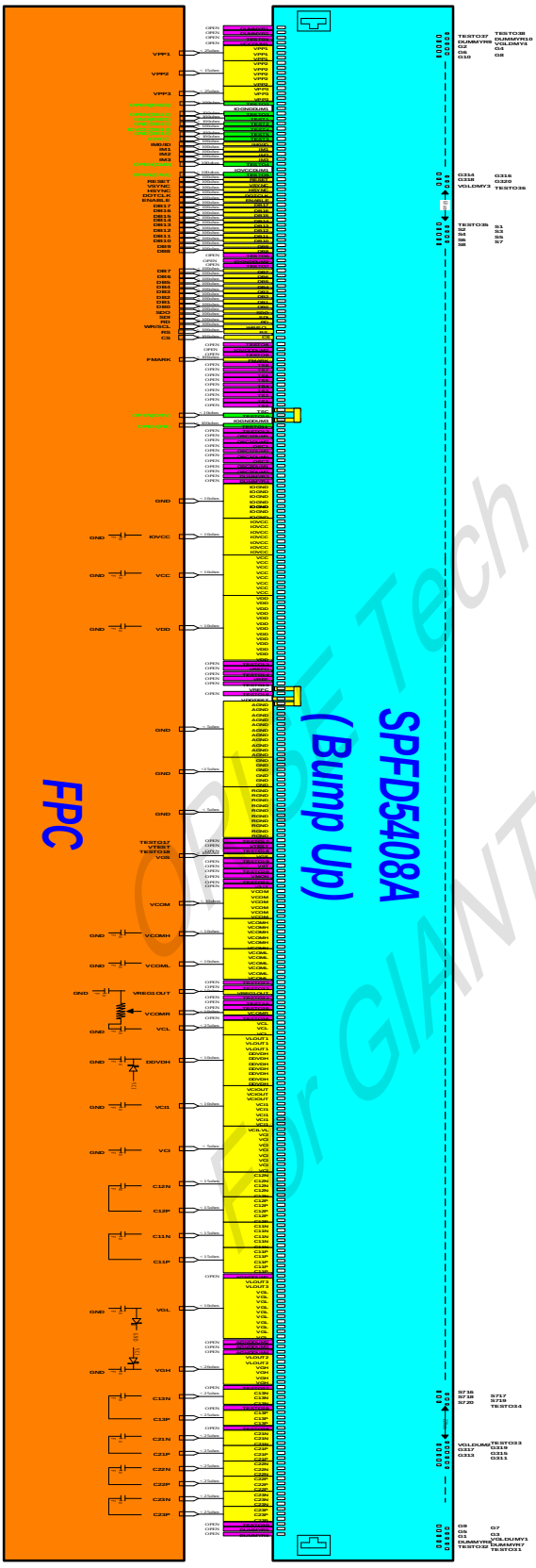


(b) VCI1=VCIOUT:





12. Application circuits:



13. Initial Code:

Step	Register Address	Register Value	Note
1	R00h	0x0001h	
2	R01h	0x0000h	
3	R02h	0x0701h	
4	R03h	0xD010h	
5	R04h	0x0000h	
6	R08h	0x0207h	
7	R09h	0x0000h	
8	R0Ah	0x0000h	
9	R0Ch	0x0000h	
10	R0Dh	0x0000h	
11	R0Fh	0x0000h	
12	R07h	0x0101h	
13	R10h	0x10B0h	
14	R11h	0x0007h	
15	R17h	0x0001h	
16	R12h	0x013Bh	
17	R13h	0x0B00h	
18	R29h	0x0012h	
19	R2Ah	0x0095h	
20	R50h	0x0000h	
21	R51h	0x00EFh	
22	R52h	0x0000h	
23	R53h	0x013Fh	
24	R60h	0x2700h	
25	R61h	0x0001h	
26	R6Ah	0x0000h	
27	R80h	0x0000h	
28	R81h	0x0021h	
29	R82h	0x0061h	
30	R83h	0x0173h	
31	R84h	0x0000h	
32	R85h	0x0000h	
33	R90h	0x0013h	
34	R92h	0x0000h	
35	R93h	0x0003h	
36	R95h	0x0110h	
37	R97h	0x0000h	
38	R98h	0x0000h	
39	R07h	0x0173	

Note: This initial code is not including Gamma setting. Please contact Orise Technology for desired Gamma setting.