Contents

1 Abstract

A high step-up DC-DC converter with active switched LC-network is proposed here, which can be used in the photovoltaic (PV) system as the front-end stage to generate the required dc bus voltage. Based on the transformerless DC-DC converter with an active switched inductor (ASL) network, this proposed converter introduces an active switched capacitor (ASC) network, only one capacitor and one diode are added, while the voltage gain is efficiently increased by a compound of ASL and ASC network. The structure of the proposed converter is simple and voltage stresses on the additional diode and capacitor are low. In addition, unlike other voltage-boosting structures that utilized switched capacitor, the proposed converter avoids the extreme instantaneous currents of capacitor. The detailed analysis of the proposed converter and performance comparison with transformerless DC-DC converter with an active switched inductor (ASL) network is presented here.

2 Introduction

DC-DC converters having high gain are widely used to generate the required DC bus voltage for grid-connected inverters in photovoltaic (PV) systems.Traditional DC-DC boost converter requires high rated power switch, because the voltage stress on the active switch is equal to the output voltage. Consequently, the conduction loss is increased due to the high on state resistance RDS(ON) and the voltage gain is limited accordingly even with a very large duty cycle[2]. Compared to boost converter, the transformerless DC-DC converter with an active switched inductor (ASL) network[3] ,receives more attention owing to its advantages including simple structure and low voltage stresses on the active switches.

A SC based ASL converter proposed in [4] can achieve high voltage gain without extremely high duty cycle and the voltage stresses of active switches and output diodes are low. Though high voltage gain is achieved, these converters all suffer from the extreme instantaneous currents of capacitor, which results in extra power losses and electromagnetic noises.The ASL-PSC converter presented in [5] raised the voltage gain through the cascaded passive switched-capacitor (PSC) network. However, the inductor in output LC filter which used to eliminate the discharging current spike of capacitors will lead to a bulky circuit according to the calculated inductance.

Based on the SL cell and SC cell, a multicell SL/SC combined ASL network converter was proposed in [14], this converter provides a higher voltage conversion ratio

with a lower voltage/current stress on the power devices. In addition, this topology can be adjusted with flexible structure to meet different voltage gain and stress requirements. Despite these merits, the above-mentioned demerits of SC and SL based converters still exist. By adding one diode and one switch to the conventional ASL converter, this presented converter provides an additional energy-stored loop where two inductors are in series to the source. However, the supplementary elements will increase the fault risk and also result in additional switching and conduction losses.

Our proposed topology for a high step-up DC-DC converter with active switched LC-network solves the aforementioned drawbacks of the ASL based converters. The proposed converter only adds one capacitor and one diode to the conventional ASL converter, but the voltage gain is efficiently increased through an active switched LC-network. In addition, voltage stresses on the additional diode and capacitor are low. Though ASC network is adopting, the high-current transients, which is the intrinsic drawback of switched capacitors circuits, are avoided in the proposed converter.

3 Analysis of Proposed Converter

3.1 Circuit Diagram

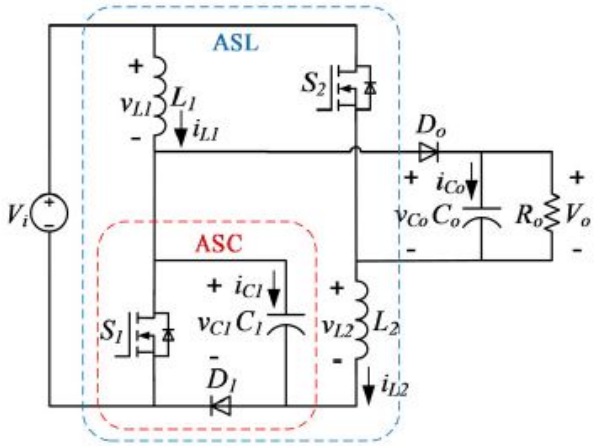


Figure 3.1: Proposed ASLC converter

Fig.3.1 shows the schematic of the proposed topology in which the original ASL network is combined with an ASC network and thus named ASLC converter. The original ASL network, which consists of inductors L1 and L2 and switches S1 and S2, shares a common switch S1 with the ASC network, which consists of switch S1, diode D1 and capacitor C1. Therefore, only one diode and one capacitor are added, and the simple structure is retained.

3.2 Modes of Operation

The proposed converter has six possible operation modes and their equivalent circuits are shown in Fig. 3.2 According to the currents of capacitor C1, inductor L1 and inductor L2, six operational cases, including two CCMs and four DCMs, can be further distinguished. The detailed states of components in different modes are shown in Fig 3.3. Transitions between modes and key waveforms in different cases are shown in Table 3.4 and Fig.3.5, respectively. To simplify the analysis, all the components are assumed ideal, i.e., parasitic parameters are ignored, and the capacitance of capacitors is considered high enough to maintain constant voltage.

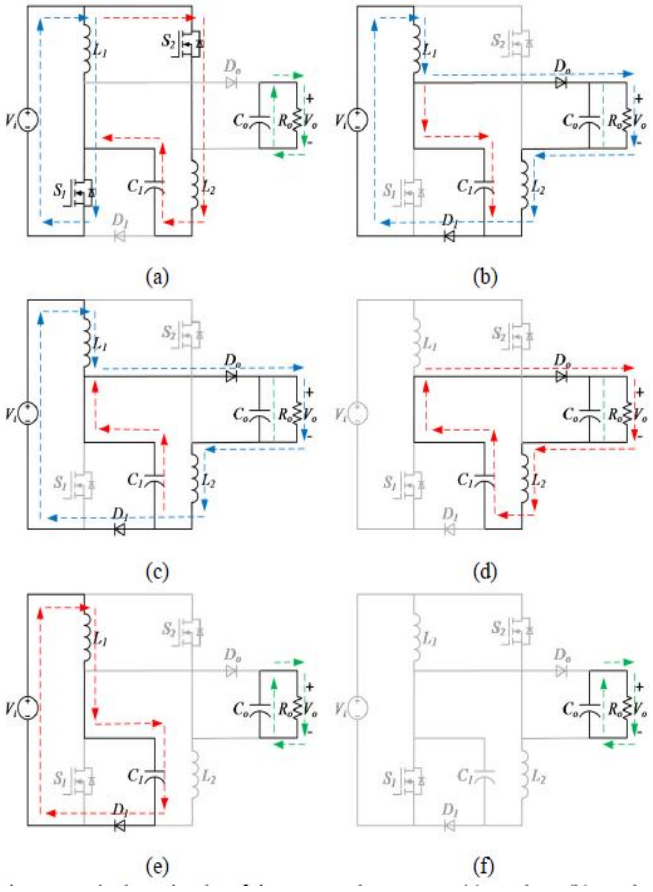


Figure 3.2: (a) Mode 1.(b) Mode 2.(c) Mode 3.(d) Mode 4.(e) Mode 5.(f) Mode 6.

	Mode 1	Mode 2	Mode 3	Mode 4	Mode 5	Mode 6
S_1, S_2	ON	OFF	OFF	OFF	OFF	OFF
D_1	OFF	ON	ON	OFF	ON	OFF
D_o	OFF	ON	ON	ON	OFF	OFF

Figure 3.3: States of Components in Different Modes

Mode	Transition
CCM	Case 1: Mode 1→Mode 2 Case 2: Mode 1→Mode 2→Mode 3
DCM	Case 3: Mode 1→Mode 2→Mode 3→Mode 4 Case 4: Mode 1→Mode 2→Mode 5 Case 5: Mode 1→Mode 2→Mode 3→Mode 4→Mode 6 Case 6: Mode 1→Mode 2→Mode 5→Mode 6

Figure 3.4: Transition between modes in different cases

3.3 CCM Operation

As shown in fig 3.4, there are two cases in the CCM.

3.3.1 Case 1

In this case, two modes are involved, i.e., Mode 1 and Mode 2, whose equivalent circuits are shown in Fig. 3.2(a) and (b). The key waveforms of driven voltage of two switches (VGS1,2), two inductor currents (iL1, iL2) and two capacitor currents (iC1, iCo) in this case are shown in Fig. 3.5(a), from top to bottom.

Mode 1 [t0, t1]: During this time interval, S1 and S2 are turned ON and diodes D1 and Do are in reverse bias condition. As shown in Fig. 3.2(a), the inductors L1 and L2 are charged in parallel from the dc source Vi, and the energy previously stored in the capacitor C1 and Co are released to inductor L2 and the load, respectively. The two inductor voltages (vL1, vL2) and two capacitor currents (iC1, iCo) in this

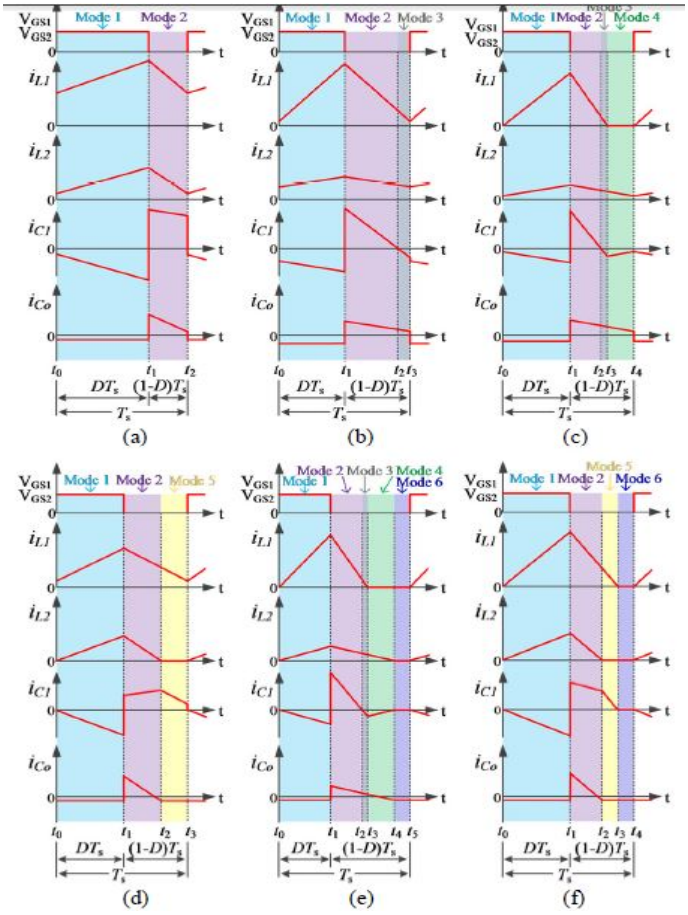


Figure 3.5: (a) Case 1. (b) Case 2. (c) Case 3. (d) Case 4. (e) Case 5. (f) Case 6.

mode are derived as

$$\begin{cases} v_{L1} = L_1 \dfrac{di_{L1}}{dt} = V_i \\ v_{L2} = L_2 \dfrac{di_{L2}}{dt} = V_i + v_{C1} \end{cases}$$

$$\begin{cases} i_{C1} = C_1 \dfrac{dv_{C1}}{dt} = -i_{L2} \\ i_{Co} = C_o \dfrac{dv_{Co}}{dt} = -I_o \end{cases}$$

Mode 2 [t1, t2]: During this time interval, S1 and S2 are turned OFF and diodes D1 and Do are forward biased. As shown in Fig. 3.2(b), the inductors L1 and L2 are series connected with the dc source to transfer the energies to capacitor Co and the

load Ro. Meanwhile, capacitor C1 is charged from the input source through inductor L1. The voltage and current relations in this mode can be written as

$$\begin{cases} v_{L1} = L_1 \dfrac{di_{L1}}{dt} = V_i - v_{C1} \\ v_{L2} = L_2 \dfrac{di_{L2}}{dt} = v_{C1} - V_o \end{cases}$$

$$\begin{cases} i_{C1} = C_1 \dfrac{dv_{C1}}{dt} = i_{L1} - i_{L2} \\ i_{Co} = C_o \dfrac{dv_{Co}}{dt} = i_{L2} - I_o \end{cases}$$

3.3.2 Case 2

Different to Case 1, there are three modes in this case due to the direction of iC1. Mode 3, whose equivalent circuit is shown in Fig. 3.2(c), occurs when iC1 decreases to 0. The key waveforms in this case are shown in Fig. 3.5(b).

Mode 1 [t0, t1]:The operating principle is the same as that for Mode 1 in Case 1.

Mode 2 [t1, t2]: The operating principle is similar to that for Mode 2 in Case 1 except that iC1 decreases to 0 at t2.

Mode 3 [t2, t3]: In this mode, the energy stored in the inductors are not enough to supply the load and thus capacitor C1 starts to discharge its energy, and iC1 decreases from 0 to negative. The equations of voltage and current relations in Mode 3 are the same as those in Mode 2.

3.4 DCM Operation

Four cases in the DCM in terms of the discontinuous currents of inductors L1 and L2 will be introduced in this section.

3.4.1 Case 3

As shown in fig 3.4, there are four modes in this case. Mode 4, whose equivalent circuit is shown in Fig. 3.2(d), occurs when iL1 decreases to 0. The key waveforms in this case are shown in Fig. 3.5(c).

Mode 1,2 [t0, t2]: The operating principles are the same as those for Mode 1 and Mode 2 in Case 2, respectively.

Mode 3 [t2, t3]: The operating principle is similar to that for Mode 3 in Case 2 except that iL1 decreases to 0 at t3.

Mode 4 [t3, t4]: When iL1 decreases to 0, C1 and L2 discharge the energy to Co and Ro. The equations of voltage and current relations in Mode 4 are the same as those in Mode 2 except that iL1 and VL1 are both zero.

3.4.2 Case 4

Similar to Case 3, Mode 5 appears when iL2 decreases to 0. As shown in fig 3.4, there are three modes in this case. The equivalent circuit of Mode 5 and key waveforms in this case are shown in Fig. 3.2(e) and Fig. 3.5(d), respectively. Mode 1,2 [t0, t2]: The operating principles are the same as those for Mode 1 and Mode 2 in Case 1, respectively. Mode 5 [t2, t3]: When iL2 decreases to 0, the energy stored in Co is discharged to Ro. Meantime, C1 is charged from Vi through L1. The equations of voltage and current relations in Mode 5 are the same as those in Mode 2 except that iL2 and VL2 are both zero.

3.4.3 Case 5

When iL2 decreases to 0 in Mode 4 of Case 3, then there is only one loop left shown in Fig. 3.2(f), i.e., Mode 6 occurs. As shown in fig 3.4, there are five modes in this case. The key waveforms in this case are shown in Fig. 3.5(e).

Mode 1,2,3,4 [t0, t4]: The operating principles are the same as those for Mode 1, Mode 2, Mode 3 and Mode 4 in Case 3, respectively.

Mode 6 [t4, t5]: When iL2 decreases to 0, only the energy stored in Co is discharged to Ro, and iCo = -Io.

3.4.4 Case 6

Akin to Case 5, when iL1 decreases to 0 in Mode 5 of Case 4, Mode 6 follows. As shown in Table , there are four modes in this case. The key waveforms in this case are shown in Fig. 3.5(f).

Mode 1,2,5 [t0, t3]: The operating principles are the same as those for Mode 1, Mode 2 and Mode 5 in Case 4, respectively. Mode 6 [t3, t4]: When iL1 decreases to 0, only the energy stored in Co is discharged to Ro, and iCo = -Io.

4 Design

As the CCM is normally employed in industrial applications, the following steady-state analysis of the proposed converter is made only for CCM.

4.1 Voltage Gain Derivation

Applying the volt-second balance principle to the inductor L1 from, we have Similarly,

$$V_{C1} = \frac{1}{1-D} V_i$$

by considering the voltage balance law for the inductor L2, we obtain the ideal voltage

$$V_o = \frac{DV_i + V_{C1}}{1-D}$$

gain of the proposed converter can be derived as

$$M_{Ideal} = \frac{V_o}{V_i} = \frac{1+D-D^2}{(1-D)^2}$$

4.2 Parameters Design

According to the aforementioned operation principle, the inductor currents increase linearly in Mode 1. The inductors current ripple can be obtained as

$$\begin{cases} \Delta i_{L1} = D\dfrac{V_i}{L_1 f_s} \\ \Delta i_{L2} = \dfrac{D(2-D)}{(1-D)}\dfrac{V_i}{L_2 f_s} \end{cases}$$

where fs is the switching frequency

$$\begin{cases} L_1 = D\dfrac{V_i}{\Delta i_{L1} f_s} \\ L_2 = \dfrac{D(2-D)}{(1-D)}\dfrac{V_i}{\Delta i_{L2} f_s} \end{cases}$$

Applying the principle of capacitor charge balance to C1 and Co , the average currents of inductors can be derived as follows

$$\begin{cases} I_{L1} = \dfrac{1}{(1-D)^2} I_o \\ I_{L2} = \dfrac{1}{1-D} I_o \end{cases}$$

The capacitors voltage ripple can be obtained as follows

$$\begin{cases} \Delta v_{C1} = \dfrac{D}{1-D}\dfrac{I_o}{C_1 f_s} \\ \Delta v_{Co} = D\dfrac{I_o}{C_o f_s} \end{cases}$$

Therefore, the capacitors can be designed by

$$\begin{cases} C_1 = \dfrac{D}{1-D}\dfrac{I_o}{\Delta v_{C1} f_s} \\ C_o = D\dfrac{I_o}{\Delta v_{Co} f_s} \end{cases}$$

Parameters	Values
Input voltage (V_i)	20 V
Output voltage (V_o)	200 V
Rated power (P_o)	100 W
Switching frequency (f_S)	50 kHz
Duty ratio (D)	0.65
Inductors current ripple (Δi_L)	1.3 A
MOSFETs (S_1, S_2)	S_1: IRFP4321Pbf S_2: IRFP4868Pbf
Diodes (D_1, D_o)	MUR1560G
Inductors (L_1, L_2)	Core:CS467060 L_1: 200 µH, L_2: 800 µH
Capacitors (C_1, C_o)	C_1: 22 µF/200 V C_o: 100 µF/400 V

Figure 4.1: Parameters used for Simulation

4.3 Transfer Function Design

Using state-space averaging method and Laplace transformation, the small signal state equations of the proposed topology can be obtained as

$$\begin{cases} sL_1\hat{i}_{L1}(s) = -(1-D)\hat{v}_{C1}(s) + \hat{v}_i(s) + \dfrac{V_i}{1-D}\hat{d}(s) \\ sL_2\hat{i}_{L2}(s) = \hat{v}_{C1}(s) - (1-D)\hat{v}_{C2}(s) + D\hat{v}_i(s) + \dfrac{(2-D)V_i}{(1-D)^2}\hat{d}(s) \\ sC_1\hat{v}_{C1}(s) = (1-D)\hat{i}_{L1}(s) - \hat{i}_{L2}(s) - \dfrac{(1+D-D^2)V_i}{(1-D)^4 R_o}\hat{d}(s) \\ sC_2\hat{v}_{C2}(s) = (1-D)\hat{i}_{L2}(s) - \dfrac{1}{R_o}\hat{v}_{C2}(s) - \dfrac{(1+D-D^2)V_i}{(1-D)^3 R_o}\hat{d}(s) \end{cases}$$

Solving the small signal state equations, the control-to-output transfer function can be derived as follows.

$$G_{vd}(s)=\left.\frac{\hat{v}_o(s)}{\hat{d}(s)}\right|_{\hat{v}_i(s)=0}$$

$$=-\frac{1+D-D^2}{(1-D)^3}\frac{V_i}{R_oC_2}\frac{s^3+b_2s^2+b_1s+b_0}{s^4+a_3s^3+a_2s^2+a_1s+a_0}$$

$$\begin{cases} a_3=\dfrac{1}{R_oC_2}, a_2=\dfrac{1}{L_2C_1}+\dfrac{(1-D)^2}{L_1C_1}+\dfrac{(1-D)^2}{L_2C_2}, \\ a_1=\dfrac{1}{R_oL_2C_1C_2}+\dfrac{(1-D)^2}{R_oL_1C_1C_2}, a_0=\dfrac{(1-D)^4}{L_1L_2C_1C_2} \\ b_2=-\dfrac{(1-D)^2R_o}{L_2}, b_1=\dfrac{2}{L_2C_1}+\dfrac{(1-D)^2}{L_1C_1}, \\ b_0=-\dfrac{2(1-D)^4R_o}{L_1L_2C_1} \end{cases}$$

The Bode plot of the proposed converter with the parameters given in Fig.4.1. is given as

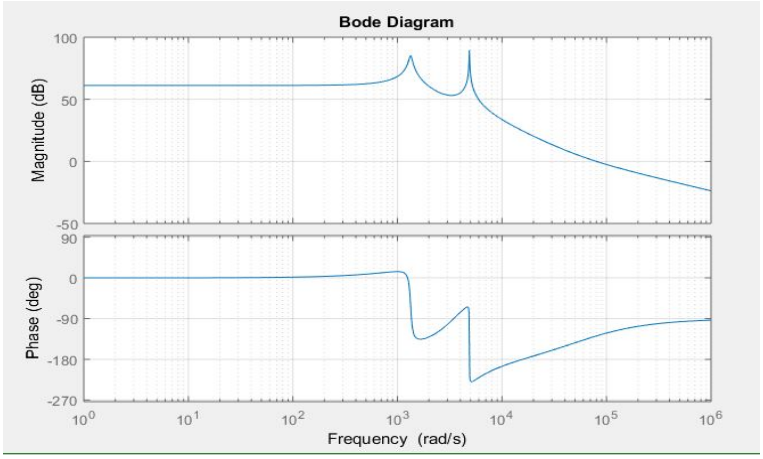


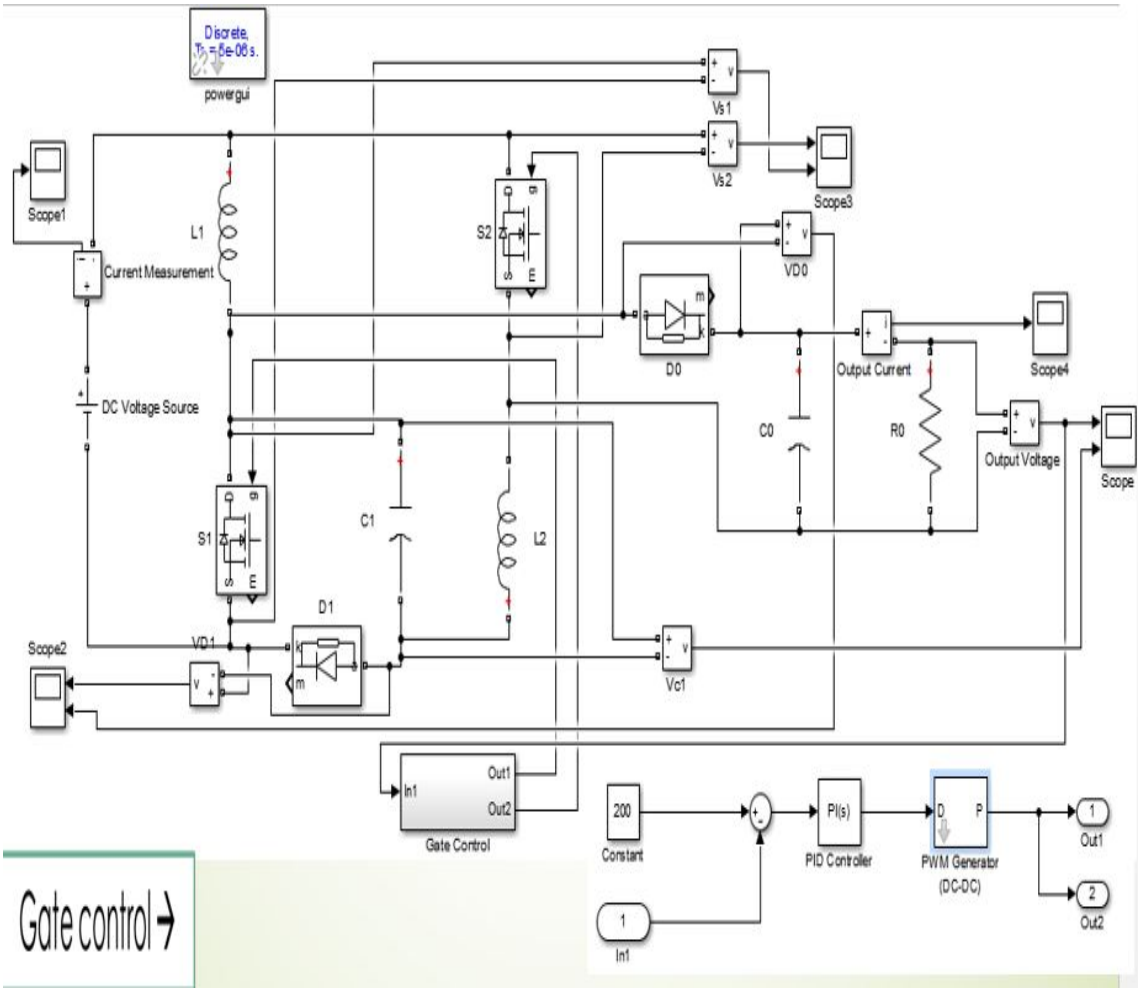
Figure 4.2: Bode plot of the control-to-output transfer function of the proposed converter.

4.4 Gate Control

In order to achieve stable operation, the voltage loop control strategy with a PI controller is used. Its transfer function could be found out by using trial and error method. The transfer function of the PI controller is

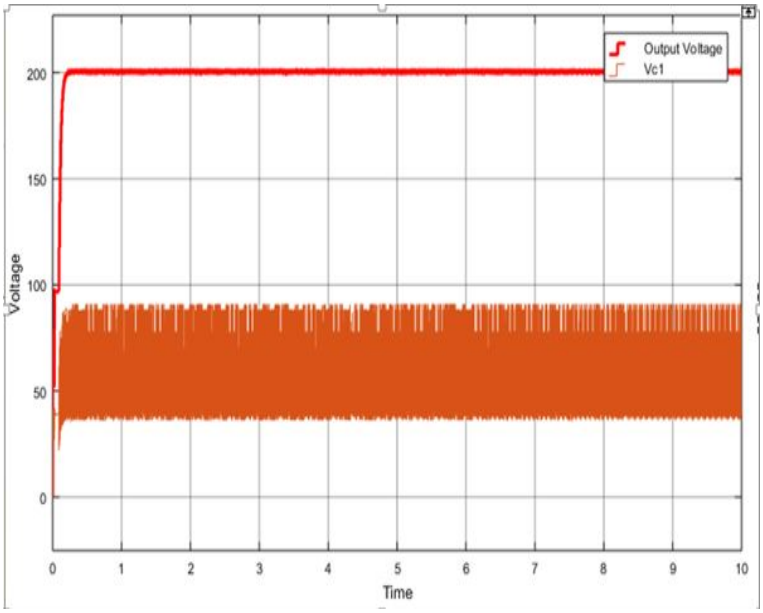
$$G_c(s) = 0.001 + 0.04\frac{1}{s}$$

5 Simulink Modelling



6 Results and Discussions

6.1 Output voltage and Capacitor voltage(Vc1)



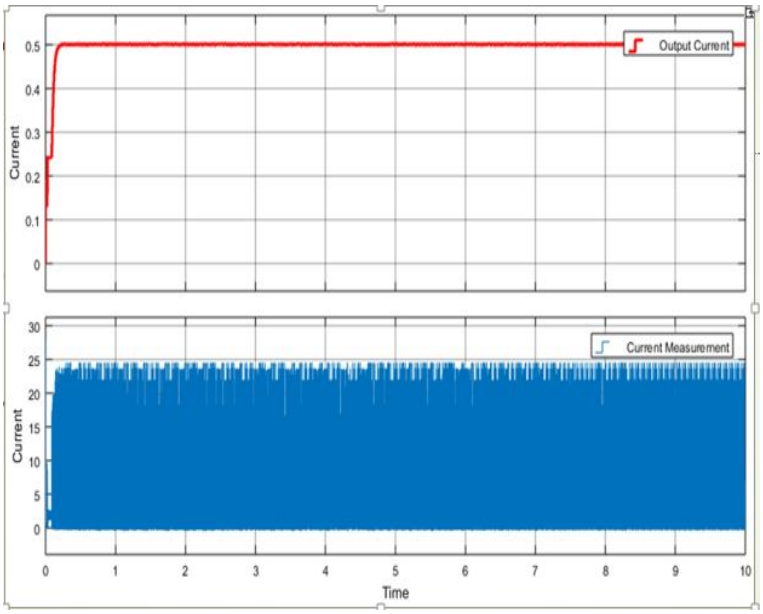
Inferences:

High gain is achieved (M=10)

Voltage stress on capacitor , C1=90.08V

Both objectives are met.

6.2 Output Current and Input Current



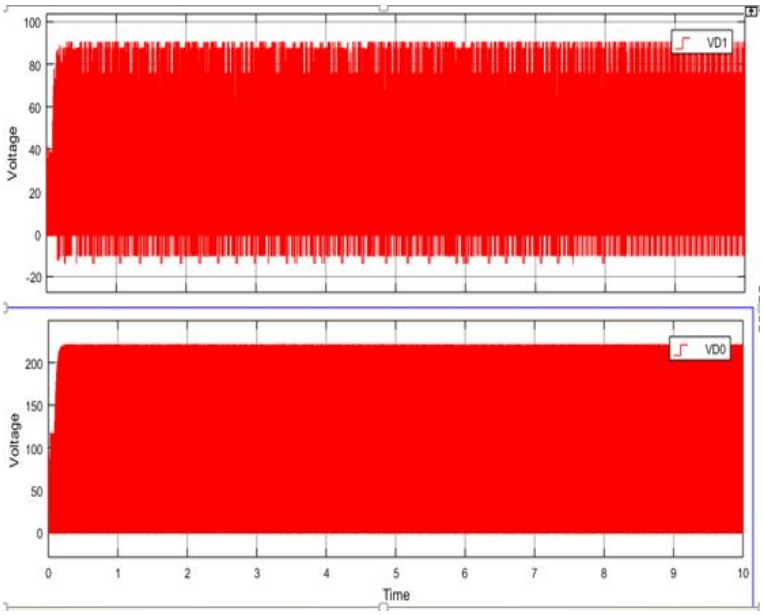
Inferences:

From output and input current value we can calculate efficiency of the converter.

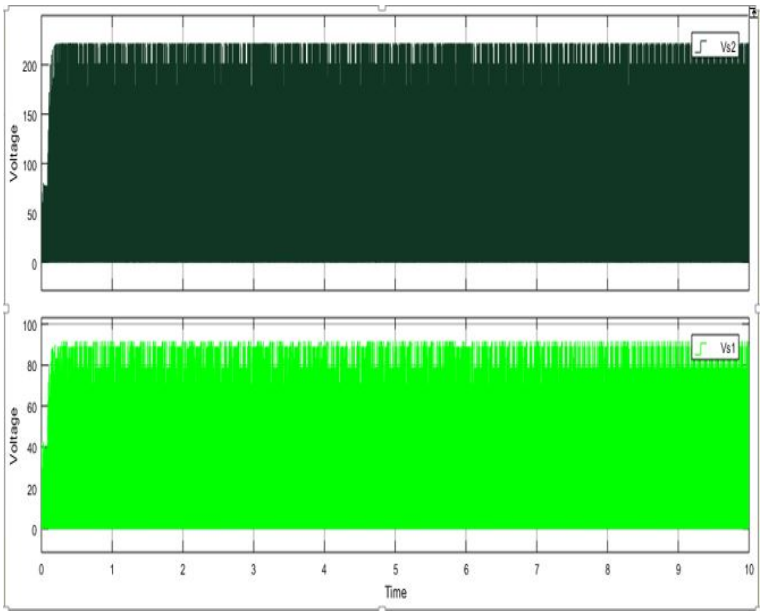
It is around 94.66 percent for a duty cycle of 0.65

6.3 Diode Voltages

The voltage stress of diode D1 (VD1) is less than 90 V, which is much smaller than the output voltage, and for diode Do (VD0), it is the sum of the input and output voltages.

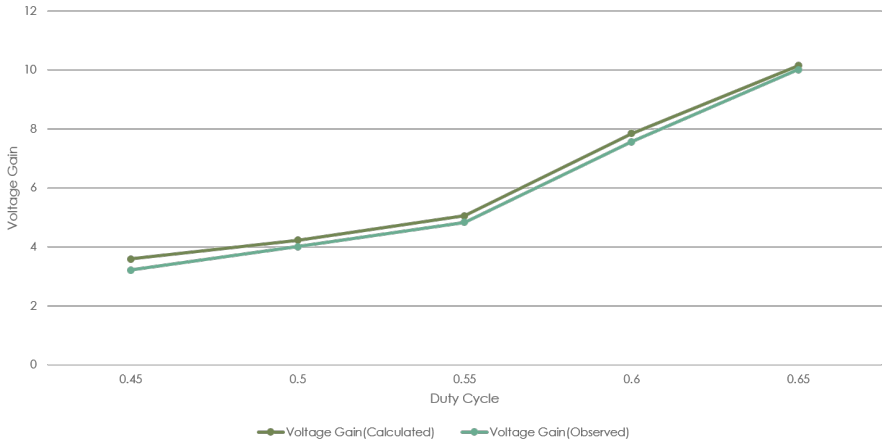


6.4 Voltage across switches

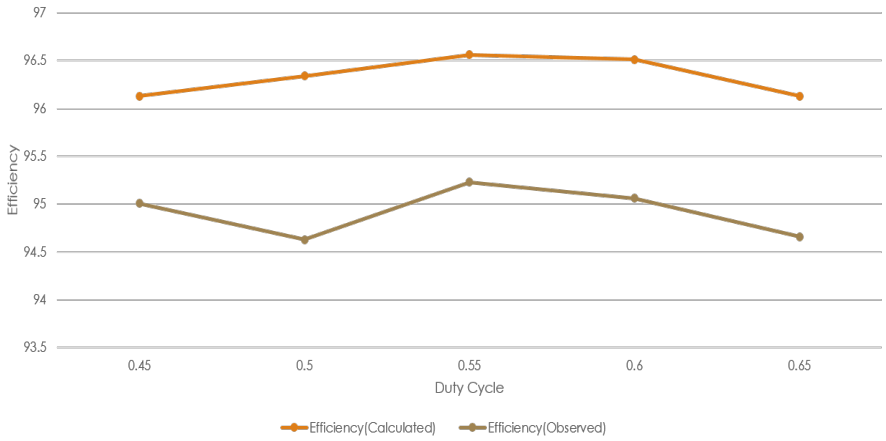


It is observed that the voltage stress of switch S1 (Vs1) is also less than 90 V, and for switch S2 (Vs2), it is a bit large, while it is still lower than the output voltage.

6.5 Voltage gain for different Duty cycles



6.6 Efficiency for different Duty cycles



6.7 Comparison

Parameters	ASLC Converter	Transformer less DC to DC Converter in [4]
1)Output Voltage	200V	105.8V
2)Output Current	0.5A	0.35A
3)Input Current	5.282A	3.839A
4)V_{s1}	86V	102.24V
5)V_{s2}	212V	111.11V
6)V_{D0}	210.1V	163.1V

7 Conclusion

A high step-up DC-DC converter with active switched LC network was introduced here, it has the following advantages:

1)High voltage gain (10) at high efficiency(94.66 percent)

2)The ASC network shared a common switch with the ASL network, only one diode and one capacitor are added to the ASL converter, thus the simple structure is retained.

3)Voltage stresses of the power devices are relatively low.

(Vs1=86V, Vs2=212V,Vd0=210.1V)

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