PY32F002BF1xP-START V2

User Guide

Puya Semiconductor (Shanghai) Co., Ltd

Contents

1. Introduction

The PY32F002BF1xP-START V2 development board integrates a PY-LINK emulator. For detailed usage instructions of PY-LINK, please refer to the document " PY-LINK OB_UserManual_EN.pdf". The START board uses the PY32F002BF1xP as the main controller. This development board, equipped with a 32-bit ARM® Cortex®-M0+ CPU core from Puya, provides a simple hardware development environment. The board is powered via the USB interface of PY-LINK. It offers peripheral resources including extension pins, as well as SWD, Reset, User key, Reset key, LED, and more. This document provides detailed hardware schematics and related application examples.
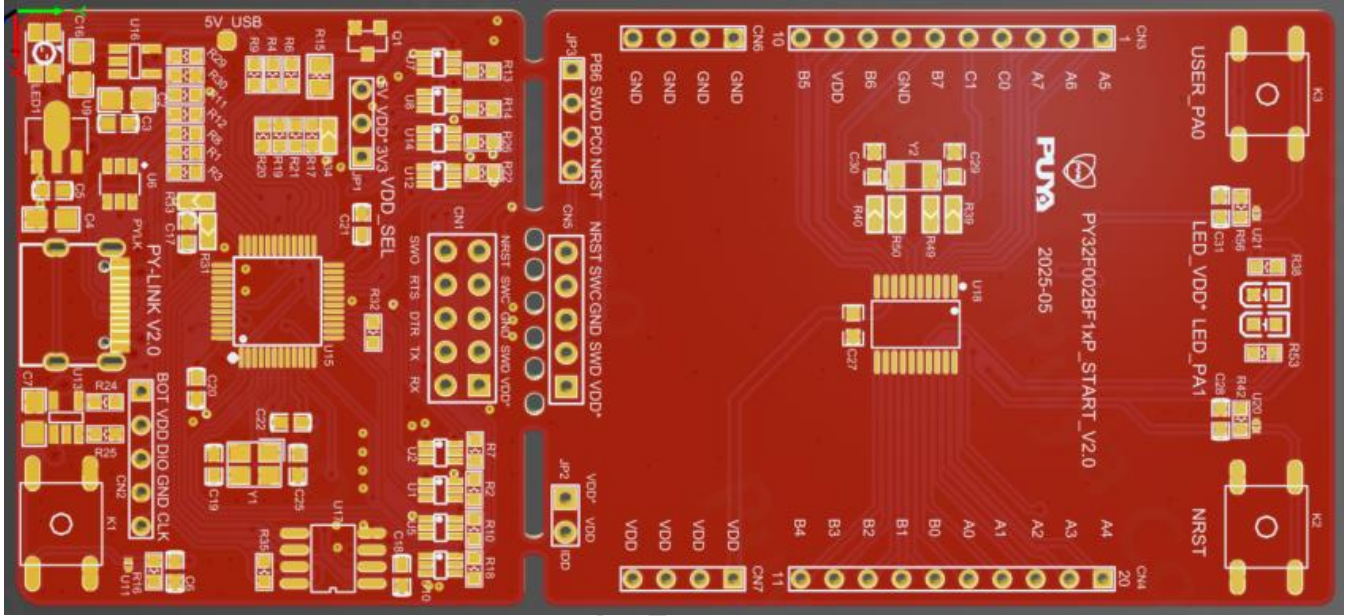

Figure 1-1 PCB 3D renderings

2. Functional pin assignment

Table 2-1 Pin Assignment

Function	Pin	Description	Note
LED	\	LED1	PY-LINK LED
	\	LED2	VDD*
	PA1	LED3	User LED
KEY	\	K1	PY-LINK Key
	PA0	K2	User Key
	PC0	K3	Reset Key
SPI	PA6	SPI_NSS	ExternalFLASH
	PB2	SPI_CLK	ExternalFLASH
	PA1	SPI_MISO	ExternalFLASH
	PA7	SPI_MOSI	ExternalFLASH

3. Overview of Hardware Design

The development board is powered via a Type-C USB connection. To download programs to the board, a Type-C USB cable is required. Select the correct boot mode, connect the USB cable, and if LED1 lights up, it indicates a proper power connection.
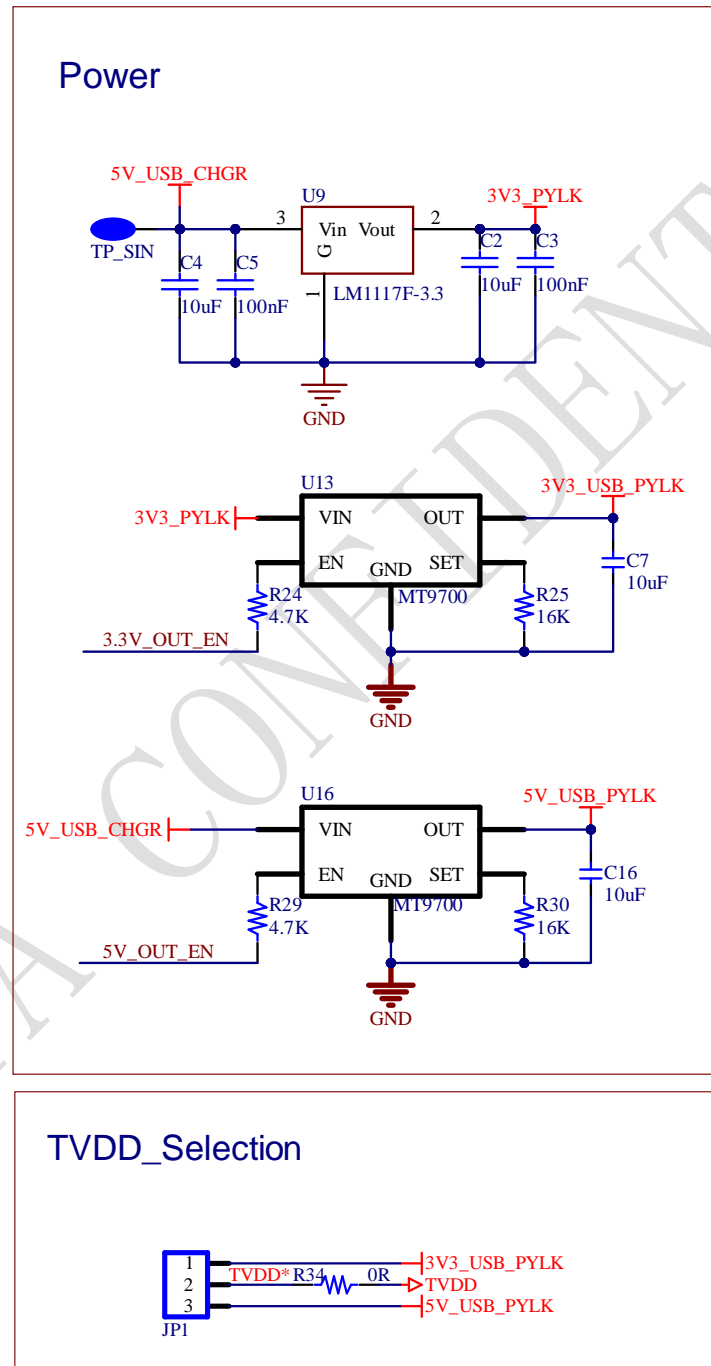
3.1 Power Supply

Figure 3-1 Power Supply Schematic

3.2 I$_{DD}$ TEST

When JP2 OFF (symbol IDD) and R37 OFF, an ammeter can be connected to measure the power consumption of MCU.

JP2 OFF, R37 ON: MCU is powered. (Default setting and JP3 plug is not mounted before shipping)

JP3 ON, R37 OFF: MCU is powered.

JP3 OFF, R37 OFF: An ammeter must be connected. If there is no ammeter available, the MCU cannot be powered.
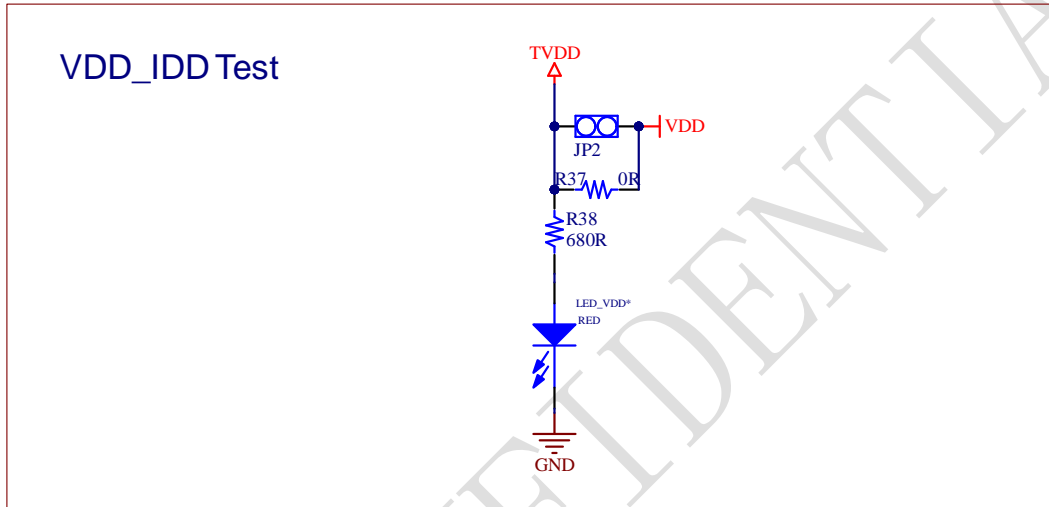

Figure 3-2 I$_{DD}$ Schematic

3.3 LED Indicator Light

The red LED indicates that the board TVDD is powered as shown in the figure above; The green LED is the user LED connected to the PA1 pin of the MCU.
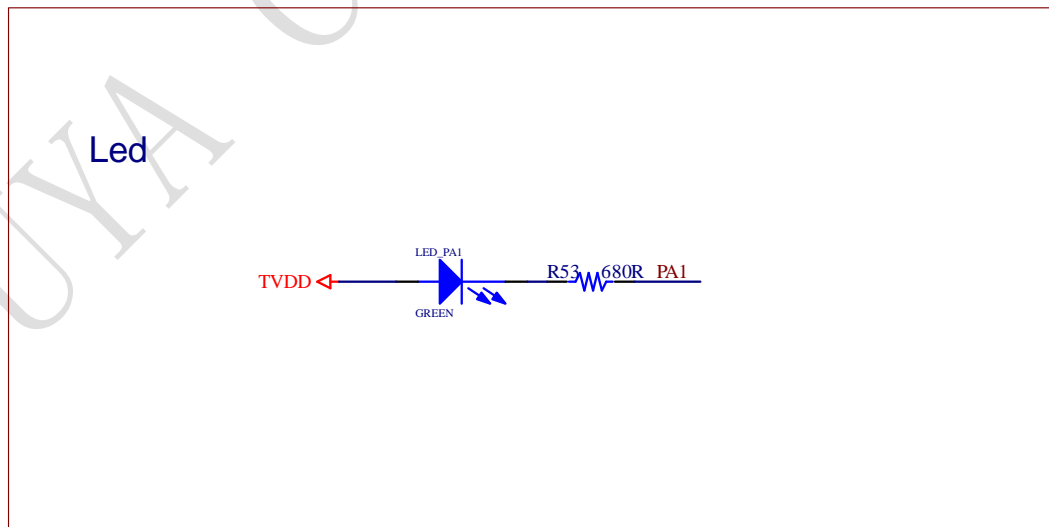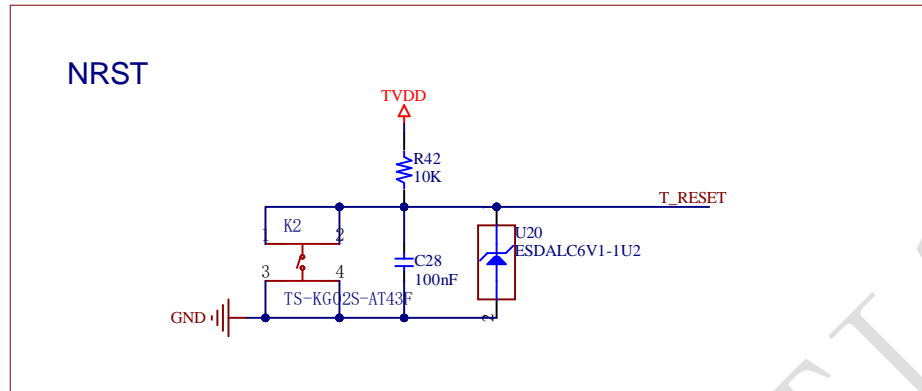

Figure 3-3 LED Schematic

3.4 Reset Key
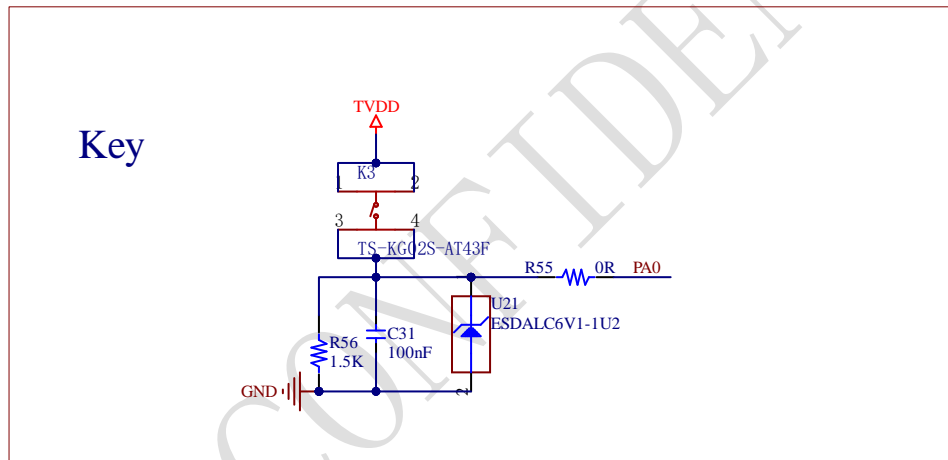

Figure 3-4 Reset Key Schematic

3.5 User Key

Figure 3-5 User Key Schematic

3.6 Boot Mode Selection

Through configuration bit nBOOT0/ nBOOT1(stored in Option bytes), three different boot modes can be selected, as shown in the following table:

Table 3-6 Boot configuration

Boot mode configuration		Mode	
nBOOT1 bit	nBOOT0 bit	Boot memory size ==0	Boot memory size !=0
X	0	Main Flash boots	Main Flash boots
0	1	SRAM boots	SRAM boots
1	1	N/A	Load Flash boots

3.7 NRST_SWD_Mode Selection

Configure the NRST_MODE and SWD_MODE bits in the option area to redirect the functions of PC0 and PB6, PB6 can be redirected to GPIO and SWD, and PC0 can be redirected to NRST, GPIO, and SWD, as shown in the following table. By default, the hardware is connected according to PB6 as SWD and PC0 as NRST, as shown in the following figure, JP3 shorts 1 and 2 pins and 3 and 4 pins respectively. If the option is modified and the redirection is redirected, the hardware also needs to modify the corresponding connection.
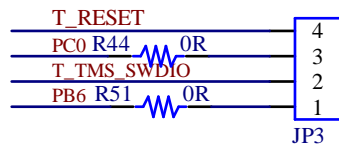

Figure 3-7 NRST_SWD_Mode schematic

Table 3-7 NRST_SWD_Mode Configuration

NRST_SWD_MODE Configuration		GPIO Function
NRST_MODE	**SWD_MODE**	
X	0	**PC0：NRST PB6：SWD**
0	1	PC0：GPIO PB6：SWD
1	1	PC0：SWD PB6：GPIO

3.8 External Clock Source

LSE clock source

There are three methods to configure the external low-speed clock sources by hardware:
On-board crystal (Factory default setting):
On-board 32.768 kHz crystal is used as HSE clock source.
Oscillator from external PC1:
External oscillator is injected from the PC1 of CN3. The hardware must be configured: R49 OFF.
LSE unused
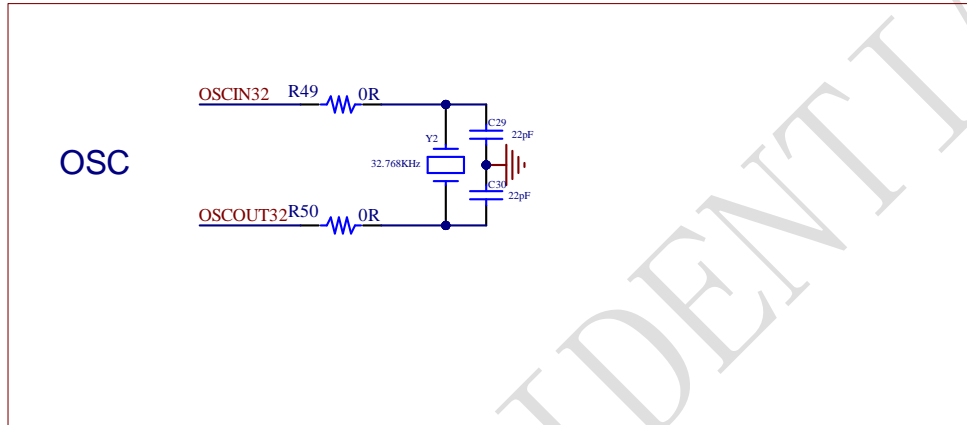MCU PB7 and PC1 are used as GPIOs.

Figure 3-8 LSE Clock Source Schematic

3.9 Programming and debugging:

The evaluation board integrates PY-LINK for users to program/debug the PY32F002BF1xP on the PY32F002BF1xP-START V2 board. PY-LINK supports SWD interface mode, and supports a set of virtual serial ports (VCP) and PY32F002BF1xP's USART1_TX/USART1_RX (PB4/PB5) to connect and communicate through Dupont wire, please refer <USART>to the official PY32xxxx_Firmware Example. For more information about PY-LINK operation, firmware upgrade, and precautions, please refer to the "PY-LINK OB_UserManual_EN.pdf "document.The PY-LINK on board can be disassembled or separated from the PY32F002BF1xP-START V2. In this case, the PY32F002BF1xP-START V2 can still be connected to the CN1 interface of PY-LINK through CN5 interface (not mounted before leaving factory), or to another PY-LINK, in order to continue to program and debug the PY32F002BF1xP.

4. Guide to Using the Example

4.1 LED Example

Purpose of the Example

There is one LED on the development board, the LED is controlled by GPIO. This sample program will tell how to light up the LED.

Execution Results

Download the official PY32xxxx_Firmware Example <GPIO_Toggle>to the board, reset and run, and the green LED flashes.

4.2 KEY Example

Purpose of the Example

There is 1 user button on the board. The user key is detected by the GPIO. This routine will show you how to detect a key with an external interrupt.

Execution Results

Download the official PY32xxxx_Firmware Example < EXTI_IT >to the board, reset and run, press the button once, and the green LED will switch to the on-off state once.
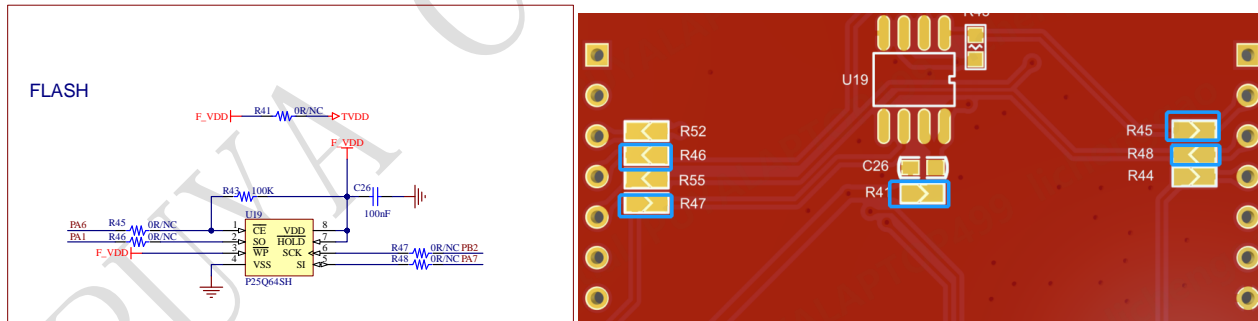
4.3 FLASH Example

Purpose of the Example

There is a flash on the development board, and the FLASH communication interface is connected to the SPI interface. This example will show you how to read and write FLASH via SPI.
Note:
1. To use this routine, the user needs to weld the 0R resistor at the position of R41, R45, R46, R47, and R48 by himself, and the specific position needs to be welded as shown in the figure below.
2. The maximum working voltage of FLASH is 3.6V. It is recommended that the supply voltage of TVDD should not exceed 3.3V.

Execution Results

Download the official PY32xxxx_Firmware Example < SPI_FullDuplex_ExternalFLASH >to the board, reset and run, If the green LED is always on, the FLASH read and write is successful, otherwise the FLASH read and write fails.
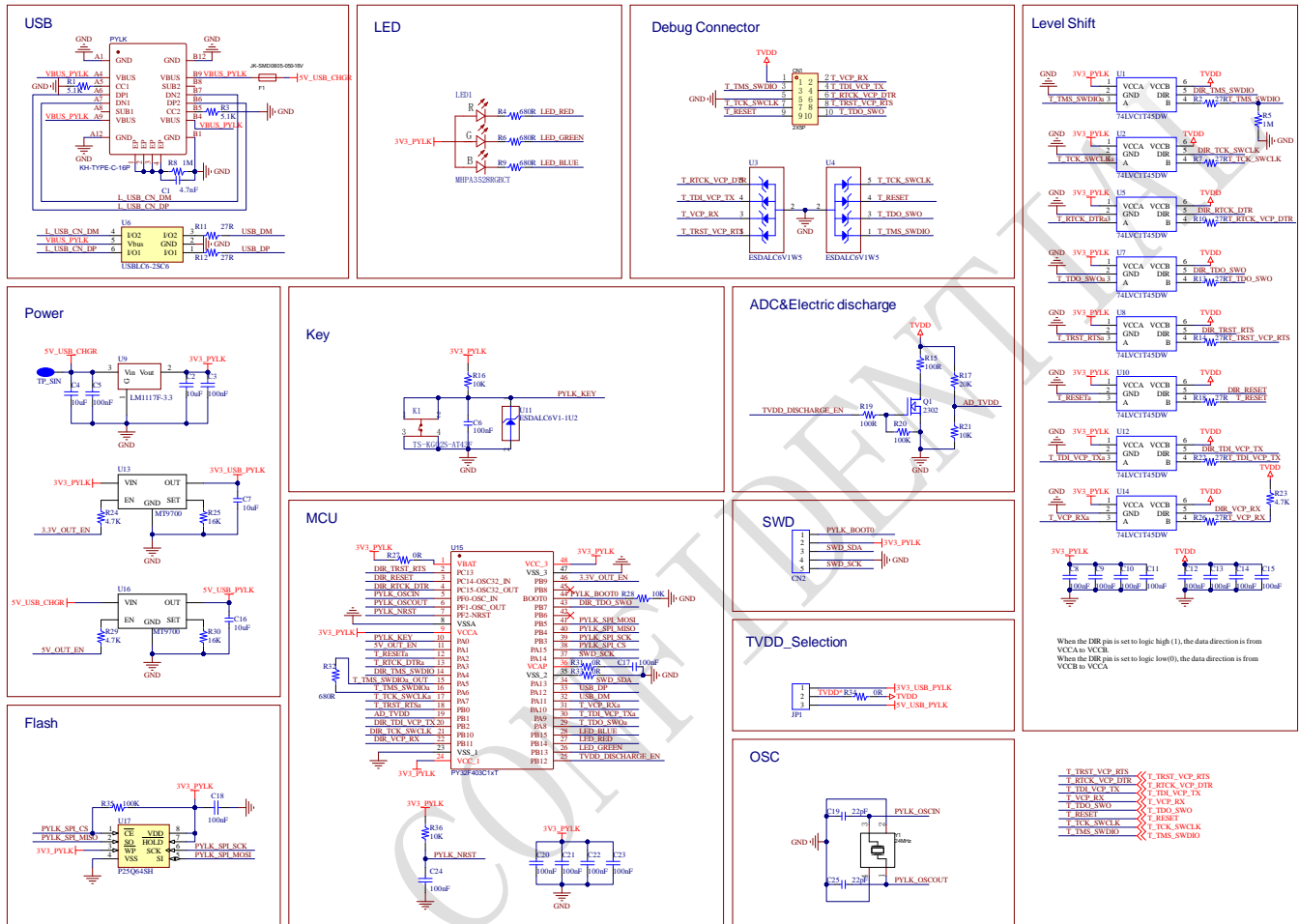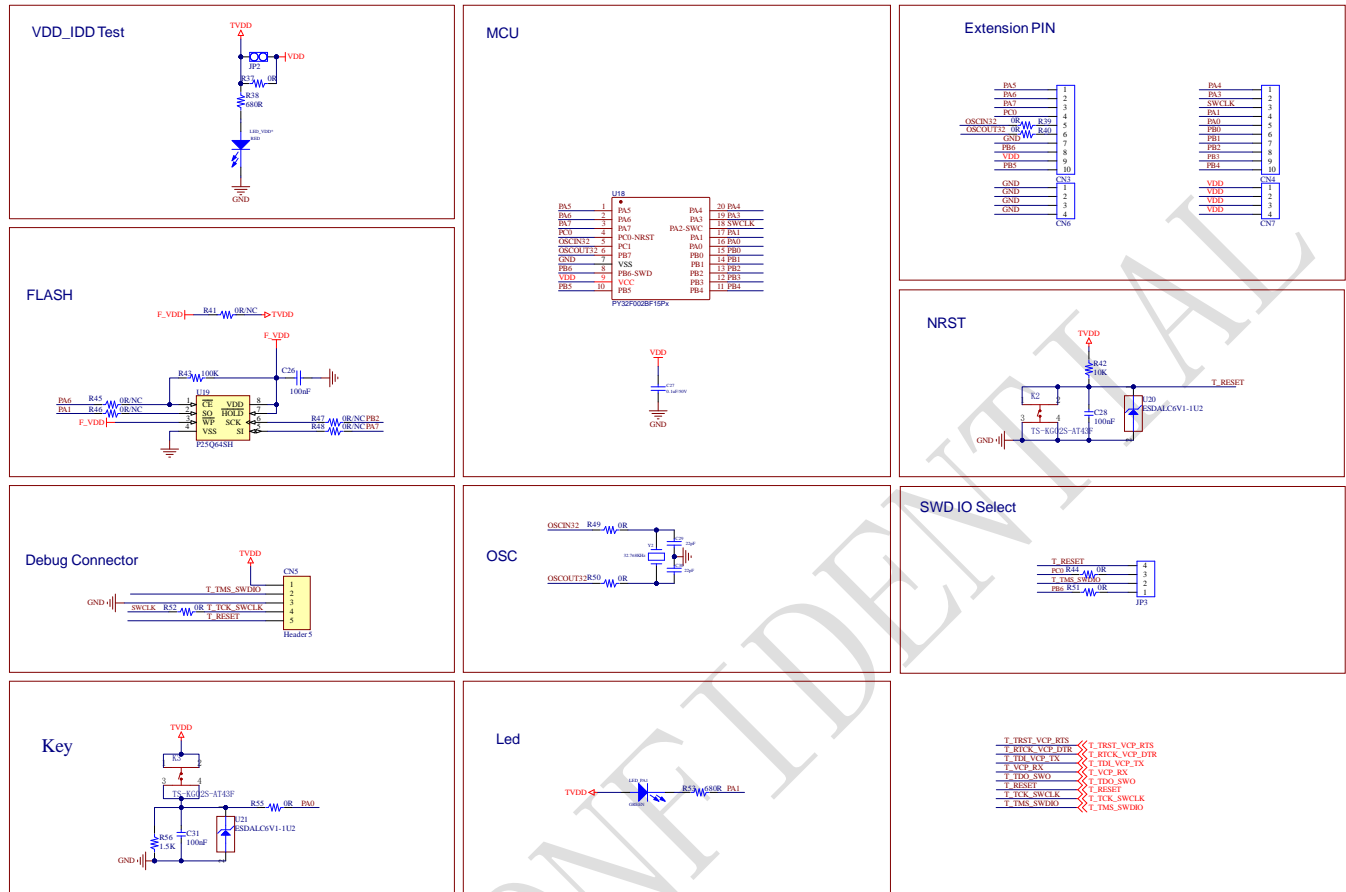
5. Schematic

5.1 PY-LINK Schematic

Figure 5-1 PY-LINK Schematic

5.2 MCU Schematic

VDD_IDD Test

MCU

Extension PIN

FLASH

NRST

Debug Connector

OSC

SWD IO Select

Key

Led

Figure 5-2 MCU Schematic

6. Updated History

Version	Content	Date
V1.0	Initial version	2025/06/30

PUYA

Puya Semiconductor Co., Ltd.