

Dual-Port Synchronous SRAM 512 Words X 8 Bits, Mux 4 Instance TSMC CLN90G 90nm Process

Overview

The dual-port synchronous SRAM is optimized for speed and density. The memory is designed to take full advantage of TSMC's 90nm CLN90G CMOS process.

The storage array is composed of eight-transistor bit cells with fully static circuitry. The SRAM operates at a voltage of 0.9V to 1.1V and a junction temperature range of -40°C to 125°C.

Instance Settings

| Parameter | Setting |
|-------------------------|-------------|
| Instance Name | SRAM_DP_ADV |
| Process | CLN90G |
| Words | 512 |
| Bits | 8 |
| Mux | 4 |
| Write Mask | off |
| Extra Margin Adjustment | on |
| Redundancy | off |
| Soft Error Repair | none |
| BIST Muxes | off |
| Output Drive | 6 |
| Power Routing Type | rings |
| Ring Width | 2μm |
| Horizontal Ring Layer | MET3 |
| Vertical Ring Layer | MET4 |
| Top Metal | MET5-9 |
| Frequency | 1.0 MHz |

Description

The dual-port synchronous RAM is a fully static memory with write enable (WENA, WENB), chip enable (CENA, CENB), address (AA, AB), data in (DA, DB) and data out (QA, QB) pins. The RAM is self-timed and consumes the minimum amount of power for read or write operations.

All synchronous inputs are latched on the rising-edge of the clock signal. When CENA is low and WENA is high the memory will read. When CENA and WENA are both low the word on the DA will be written to the memory and it will appear at the outputs (write-through).

When CENA is high the memory is deselected and forced into a low-power standby mode. Stored data is fully retained but memory access is disabled for data read or data write, the existing data outputs continue to drive their previous values.

The Extra Margin Adjustment allows you to adjust the width of the self timing pulse.

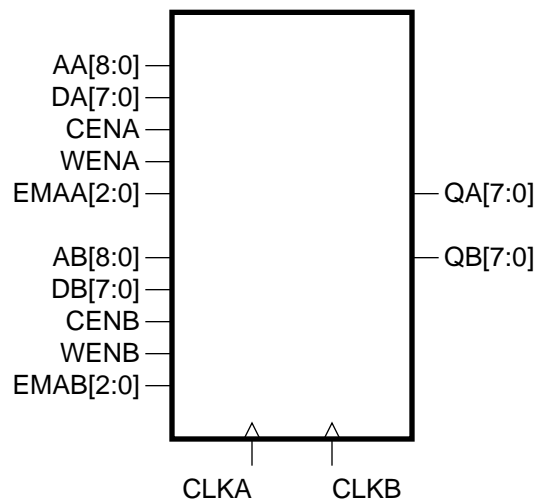
Refer to the users manual for a more detailed description of memory operation.

Physical Dimensions (units = μm)

| Parameter | Size |
|------------------|-------|
| Core Width | 179.8 |
| Core Height | 224.1 |
| Footprint Width | 197.6 |
| Footprint Height | 241.8 |

The footprint area includes the core area and user defined power routing and pin spacing.

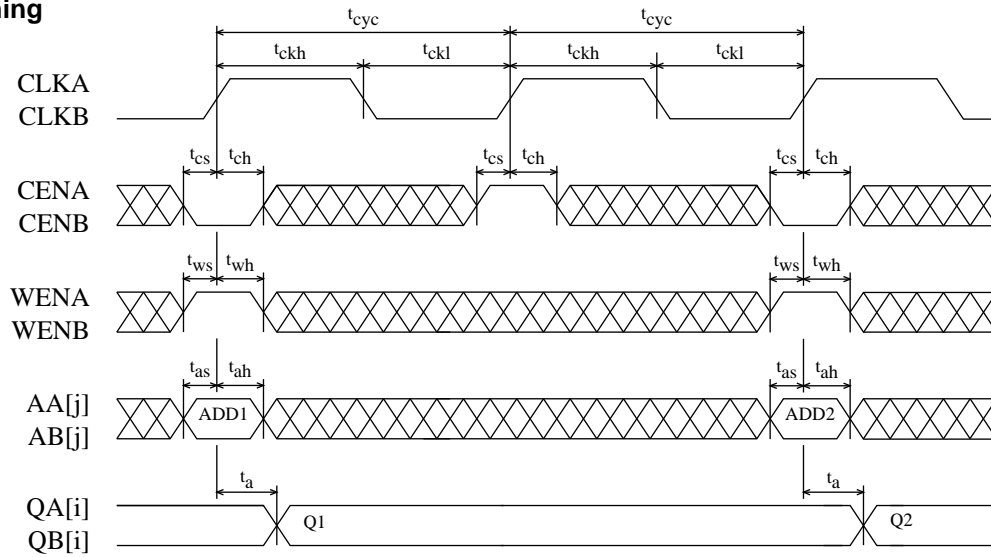
Symbol



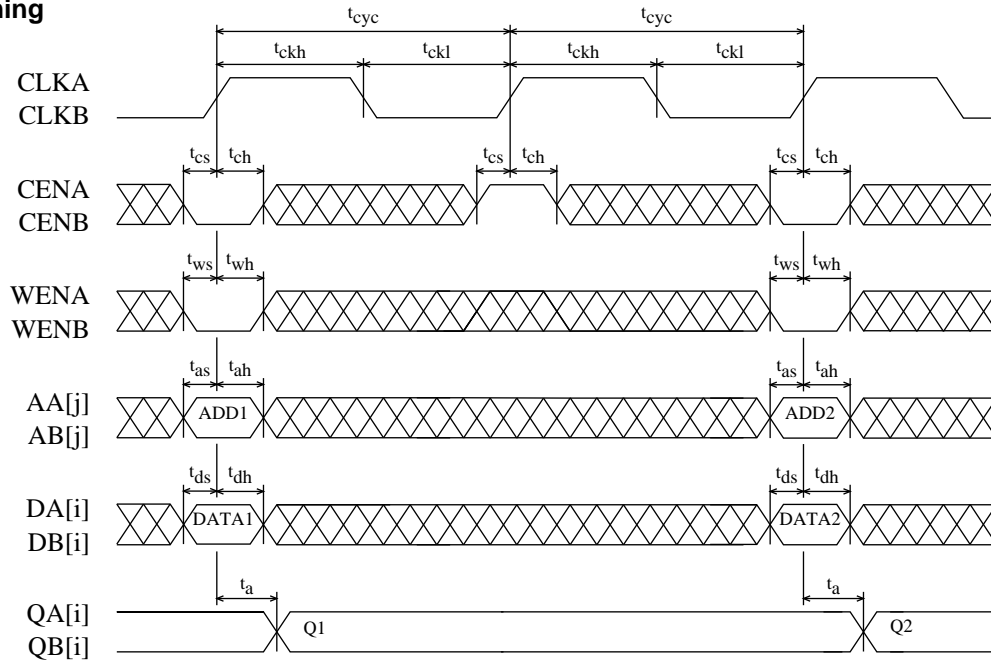
Pin Description

| Pin | Description |
|----------------------|--|
| AA[8:0], AB[8:0] | Port A & B Addresses (AA[0],AB[0] = LSB) |
| DA[7:0], DB[7:0] | Port A & B Data Inputs (DA[0],DB[0] = LSB) |
| CLKA, CLKB | Port A & B Clocks |
| CENA, CENB | Port A & B Chip Enables |
| WENA,WENB | Port A & B Write Enables (Active low) |
| QA[7:0], QB[7:0] | Port A & B Data Outputs (QA[0],QB[0] = LSB) |
| EMAA[2:0], EMAB[2:0] | Port A & B Margin Adjustment (EMAA[0],EMAB[0] = LSB) |

Read Cycle Timing



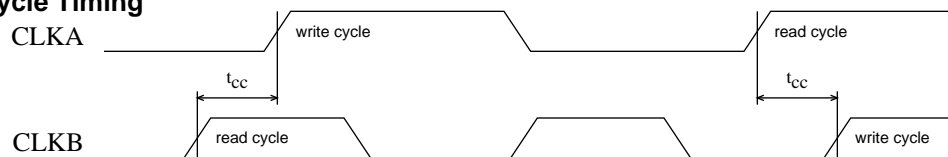
Write Cycle Timing



Write to Read Cycle Timing



Read to Write Cycle Timing



Write to Write Cycle Timing



Timing (units = ns)

The timing tables show values measured from the output threshold to the input threshold. The input pins are driven by standard slews. The slews and thresholds vary depending upon the process corner. The timing tables values are applicable to both A and B ports of the memory even though only the A side is shown.

| Pin | Symbol | Fast Process 1.1V, -40°C | | Fast Process 1.1V, 125°C | | Typical Process 1.0V, 25°C | | Slow Process 0.9V, 125°C | |
|---------------------------------|------------|-----------------------------|-------|-----------------------------|-------|-------------------------------|-------|-----------------------------|-------|
| | | Min | Max | Min | Max | Min | Max | Min | Max |
| Cycle time | t_{cyc0} | 0.695 | | 0.869 | | 1.056 | | 1.731 | |
| Access time ^{1,2} | t_{a0} | 0.513 | | 0.608 | | | 0.925 | | 1.559 |
| Address setup | t_{as} | 0.194 | | 0.236 | | 0.313 | | 0.486 | |
| Address hold | t_{ah} | 0.000 | | 0.000 | | 0.000 | | 0.000 | |
| Data setup | t_{ds} | 0.154 | | 0.188 | | 0.216 | | 0.348 | |
| Data hold | t_{dh} | 0.000 | | 0.000 | | 0.000 | | 0.000 | |
| Chip enable setup | t_{cs} | 0.250 | | 0.316 | | 0.375 | | 0.629 | |
| Chip enable hold | t_{ch} | 0.000 | | 0.000 | | 0.000 | | 0.000 | |
| Write enable setup | t_{ws} | 0.234 | | 0.311 | | 0.336 | | 0.527 | |
| Write enable hold | t_{wh} | 0.000 | | 0.000 | | 0.000 | | 0.000 | |
| Clock high | t_{ckh} | 0.042 | | 0.046 | | 0.068 | | 0.111 | |
| Clock low | t_{ckl} | 0.258 | | 0.323 | | 0.407 | | 0.689 | |
| Clock rise slew | t_{ckr} | | 1.000 | | 1.000 | | 1.000 | | 1.000 |
| Output load factor ³ | K_{load} | | 0.419 | | 0.525 | | 0.743 | | 1.100 |

¹ Output delays and a load dependency (K_{load}) which is used to calculate: $TotalDelay = FixedDelay + (K_{load} \times C_{load})$.

² Access time is defined as the longest possible delay to valid output for the typical and slow corners, and the shortest possible delay for the fast corners.

³ The output load factor units are ns/pF.

Cycle and Access Timing for Different Values of Extra Margin Adjustment (units = ns)

| Pin | Symbol | Fast Process 1.1V, -40°C | | Fast Process 1.1V, 125°C | | Typical Process 1.0V, 25°C | | Slow Process 0.9V, 125°C | |
|--------------------|-------------------|-----------------------------|-----|-----------------------------|-----|-------------------------------|-------|-----------------------------|-------|
| | | Min | Max | Min | Max | Min | Max | Min | Max |
| Cycle time EMAA=0 | t _{cyc0} | 0.695 | | 0.869 | | 1.056 | | 1.731 | |
| Cycle time EMAA=1 | t _{cyc1} | 0.798 | | 0.998 | | 1.223 | | 2.023 | |
| Cycle time EMAA=2 | t _{cyc2} | 0.980 | | 1.243 | | 1.518 | | 2.541 | |
| Cycle time EMAA=3 | t _{cyc3} | 1.072 | | 1.359 | | 1.666 | | 2.808 | |
| Cycle time EMAA=4 | t _{cyc4} | ** | | ** | | ** | | ** | |
| Cycle time EMAA=5 | t _{cyc5} | ** | | ** | | ** | | ** | |
| Cycle time EMAA=6 | t _{cyc6} | ** | | ** | | ** | | ** | |
| Cycle time EMAA=7 | t _{cyc7} | ** | | ** | | ** | | ** | |
| Access time EMAA=0 | t _{a0} | 0.513 | | 0.608 | | | 0.925 | | 1.559 |
| Access time EMAA=1 | t _{a1} | 0.615 | | 0.737 | | | 1.093 | | 1.852 |
| Access time EMAA=2 | t _{a2} | 0.798 | | 0.982 | | | 1.387 | | 2.370 |
| Access time EMAA=3 | t _{a3} | 0.890 | | 1.097 | | | 1.535 | | 2.637 |
| Access time EMAA=4 | t _{a4} | ** | | ** | | | ** | | ** |
| Access time EMAA=5 | t _{a5} | ** | | ** | | | ** | | ** |
| Access time EMAA=6 | t _{a6} | ** | | ** | | | ** | | ** |
| Access time EMAA=7 | t _{a7} | ** | | ** | | | ** | | ** |
| EMAA setup | t _{emas} | 0.695 | | 0.869 | | 1.056 | | 1.731 | |
| EMAA hold | t _{emah} | 0.695 | | 0.869 | | 1.056 | | 1.731 | |

** Illegal setting of EMAA for this corner.

Pin Capacitance (units = fF)

| Pin | Fast Process 1.1V, -40°C | Fast Process 1.1V, 125°C | Typical Process 1.0V, 25°C | Slow Process 0.9V, 125°C |
|-----------|-----------------------------|-----------------------------|-------------------------------|-----------------------------|
| AA,AB | 60.260 | 59.740 | 59.570 | 57.060 |
| DA,DB | 1.889 | 1.873 | 1.856 | 1.746 |
| CLKA,CLKB | 115.600 | 113.400 | 111.300 | 109.100 |
| CENA,CENB | 42.810 | 42.070 | 42.900 | 41.640 |
| WENA,WENB | 48.770 | 48.010 | 48.760 | 47.240 |
| EMAA,EMAB | 39.520 | 38.860 | 39.510 | 38.260 |

Power (current units = mA)

| Pin | Fast Process 1.1V, -40°C | Fast Process 1.1V, 125°C | Typical Process 1.0V, 25°C | Slow Process 0.9V, 125°C |
|--|-----------------------------|-----------------------------|-------------------------------|-----------------------------|
| AC Current (EMAA=0) ^{1,4} | 6.27E-3 | 1.22E-2 | 5.37E-3 | 4.99E-3 |
| AC Current (EMAA=1) ^{1,4} | 6.27E-3 | 1.22E-2 | 5.36E-3 | 4.99E-3 |
| AC Current (EMAA=2) ^{1,4} | 6.27E-3 | 1.22E-2 | 5.36E-3 | 4.99E-3 |
| AC Current (EMAA=3) ^{1,4} | 6.27E-3 | 1.22E-2 | 5.36E-3 | 4.99E-3 |
| AC Current (EMAA=4) ^{1,4} | 6.27E-3 | 1.23E-2 | 5.36E-3 | 4.99E-3 |
| AC Current (EMAA=5) ^{1,4} | 6.27E-3 | 1.23E-2 | 5.37E-3 | 4.99E-3 |
| AC Current (EMAA=6) ^{1,4} | 6.27E-3 | 1.23E-2 | 5.36E-3 | 4.99E-3 |
| AC Current (EMAA=7) ^{1,4} | 6.27E-3 | 1.23E-2 | 5.37E-3 | 4.99E-3 |
| Read AC Current (EMAA=0) ⁴ | 6.18E-3 | 1.21E-2 | 5.28E-3 | 4.91E-3 |
| Read AC Current (EMAA=1) ⁴ | 6.18E-3 | 1.21E-2 | 5.28E-3 | 4.91E-3 |
| Read AC Current (EMAA=2) ⁴ | 6.18E-3 | 1.21E-2 | 5.28E-3 | 4.91E-3 |
| Read AC Current (EMAA=3) ⁴ | 6.18E-3 | 1.21E-2 | 5.28E-3 | 4.91E-3 |
| Read AC Current (EMAA=4) ⁴ | 6.18E-3 | 1.22E-2 | 5.28E-3 | 4.91E-3 |
| Read AC Current (EMAA=5) ⁴ | 6.18E-3 | 1.22E-2 | 5.28E-3 | 4.91E-3 |
| Read AC Current (EMAA=6) ⁴ | 6.18E-3 | 1.22E-2 | 5.28E-3 | 4.91E-3 |
| Read AC Current (EMAA=7) ⁴ | 6.18E-3 | 1.22E-2 | 5.28E-3 | 4.91E-3 |
| Write AC Current (EMAA=0) ⁴ | 6.37E-3 | 1.23E-2 | 5.45E-3 | 5.07E-3 |
| Write AC Current (EMAA=1) ⁴ | 6.37E-3 | 1.23E-2 | 5.45E-3 | 5.07E-3 |
| Write AC Current (EMAA=2) ⁴ | 6.37E-3 | 1.23E-2 | 5.45E-3 | 5.07E-3 |
| Write AC Current (EMAA=3) ⁴ | 6.37E-3 | 1.23E-2 | 5.45E-3 | 5.07E-3 |
| Write AC Current (EMAA=4) ⁴ | 6.37E-3 | 1.24E-2 | 5.45E-3 | 5.07E-3 |
| Write AC Current (EMAA=5) ⁴ | 6.37E-3 | 1.24E-2 | 5.45E-3 | 5.07E-3 |
| Write AC Current (EMAA=6) ⁴ | 6.37E-3 | 1.24E-2 | 5.45E-3 | 5.07E-3 |
| Write AC Current (EMAA=7) ⁴ | 6.37E-3 | 1.24E-2 | 5.45E-3 | 5.07E-3 |
| Peak Current | 37.97 | 33.28 | 24.57 | 15.13 |
| Deselected Current ^{2,4} | 2.60E-3 | 1.20E-3 | 2.18E-3 | 1.93E-3 |
| Standby Current ³ | 1.86E-1 | 5.57 | 9.67E-2 | 2.61E-1 |

** Illegal setting of EMAA for this corner.

¹ The AC current value assumes 50% read and write operations, where all addresses and 50% of input and output pins switch at the user defined frequency of 1.0MHz. It is assumed that EMAA pins do not switch.

² The deselected current assumes the memory is deselected, all addresses switch, and 50% of input pins switch at the user defined frequency of 1.0MHz. The logic switching component of deselected power becomes negligibly small if the input pins are held stable by externally controlling these signals with chip select. It is assumed that EMAA pins do not switch.

³ The standby current value is independent of frequency and assumes all inputs and outputs are stable.

⁴ The standby current component is not included in this value.

Clock Noise Limit

| Symbol | Fast Process 1.1V, -40°C | | Fast Process 1.1V, 125°C | | Typical Process 1.0V, 25°C | | Slow Process 0.9V, 125°C | |
|------------|-----------------------------|---------|-----------------------------|---------|-------------------------------|---------|-----------------------------|---------|
| | Pulse Width | Voltage | Pulse Width | Voltage | Pulse Width | Voltage | Pulse Width | Voltage |
| CLKA, CLKB | 10.0ns | 0.3V | 10.0ns | 0.2V | 10.0ns | 0.3V | 10.0ns | 0.3V |

The clock noise limit is the maximum voltage allowed (for the indicated pulse width) that does not cause an unintentional memory cycle or other memory failure.

Supply Noise Limit (units = V)

| Pin | Fast Process 1.1V, -40°C | Fast Process 1.1V, 125°C | Typical Process 1.0V, 25°C | Slow Process 0.9V, 125°C |
|--------|-----------------------------|-----------------------------|-------------------------------|-----------------------------|
| Power | 0.11 | 0.11 | 0.10 | 0.09 |
| Ground | 0.11 | 0.11 | 0.10 | 0.09 |

The power and ground noise limit is the maximum supply voltage transition that is allowed without causing a memory failure.

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