Dual-Port Synchronous SRAM
1024 Words X 8 Bits, Mux 4 Instance
TSMC CLN90G 90nm Process

Overview

The dual-port synchronous SRAM is optimized for speed and density. The memory is designed to take full advantage of TSMC's 90nm CLN90G CMOS process.

The storage array is composed of eight-transistor bit cells with fully static circuitry. The SRAM operates at a voltage of 0.9V to 1.1V and a junction temperature range of -40°C to 125°C.

Instance Settings

Parameter	Setting
Instance Name	SRAM_DP_ADV
Process	CLN90G
Words	1024
Bits	8
Mux	4
Write Mask	off
Extra Margin Adjustment	on
Redundancy	off
Soft Error Repair	none
BIST Muxes	off
Output Drive	6
Power Routing Type	rings
Ring Width	2µm
Horizontal Ring Layer	MET3
Vertical Ring Layer	MET4
Top Metal	MET5-9
Frequency	1.0 MHz

Description

The dual-port synchronous RAM is a fully static memory with write enable (WENA, WENB), chip enable (CENA, CENB), address (AA, AB), data in (DA, DB) and data out (QA, QB) pins. The RAM is self-timed and consumes the minimum amount of power for read or write operations.

All synchronous inputs are latched on the rising-edge of the clock signal. When CENA is low and WENA is high the memory will read. When CENA and WENA are both low the word on the DA will be written to the memory and it will appear at the outputs (write-through).

When CENA is high the memory is deselected and forced into a low-power standby mode. Stored data is fully retained but memory access is disabled for data read or data write, the existing data outputs continue to drive their previous values.

The Extra Margin Adjustment allows you to adjust the width of the self timing pulse.

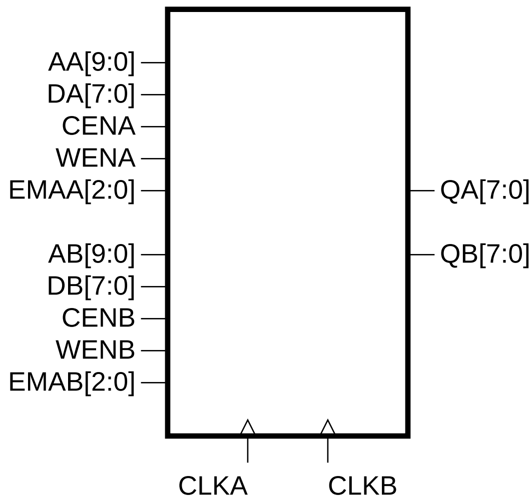
Refer to the users manual for a more detailed description of memory operation.

Physical Dimensions (units = µm)

Parameter	Size
Core Width	184.8
Core Height	342.2
Footprint Width	202.6
Footprint Height	360.0

The footprint area includes the core area and user defined power routing and pin spacing.

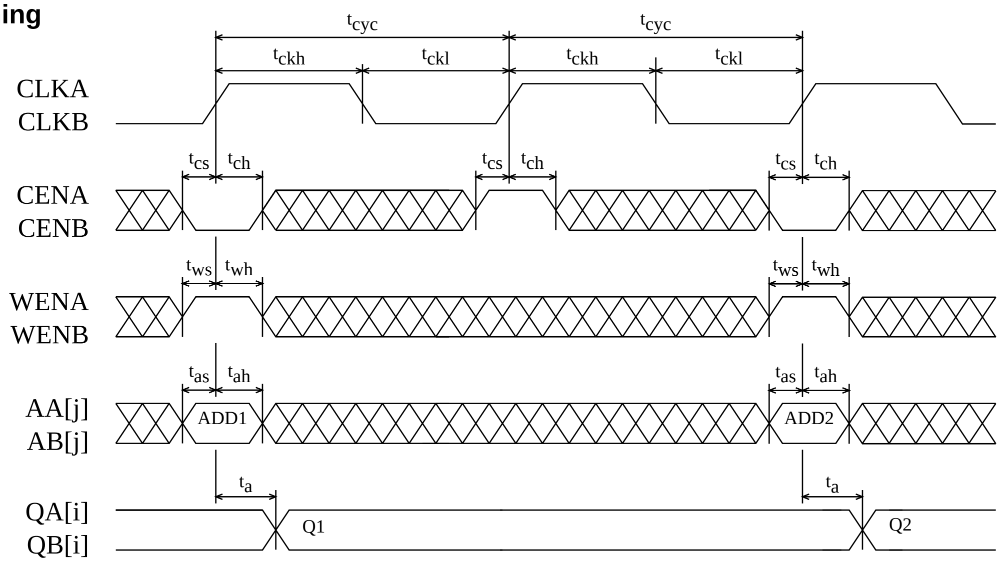
Symbol



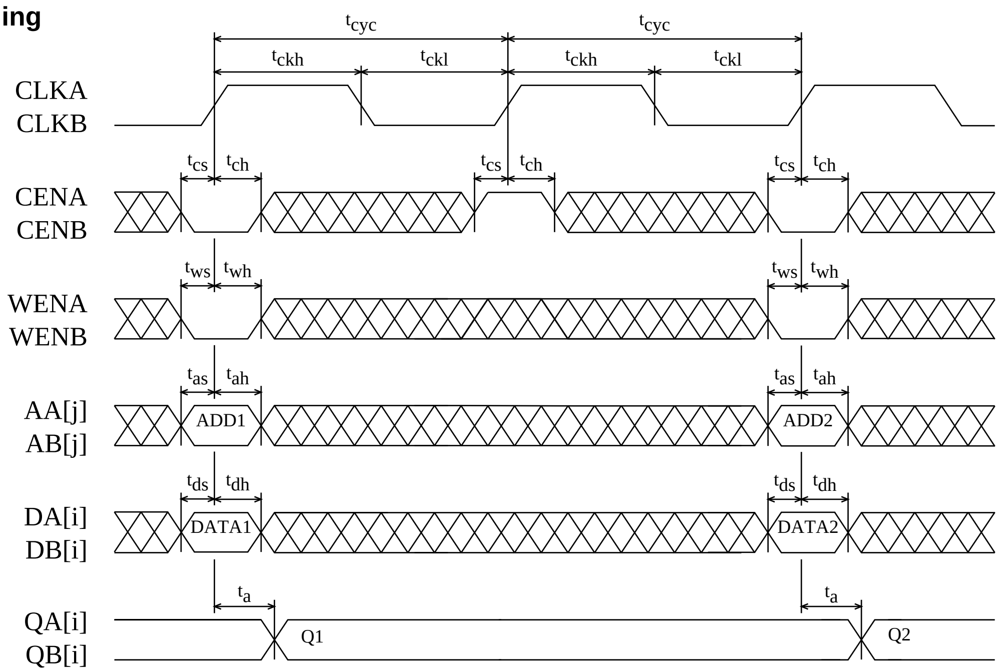
Pin Description

Pin	Description
AA[9:0], AB[9:0]	Port A & B Addresses (AA[0],AB[0] = LSB)
DA[7:0], DB[7:0]	Port A & B Data Inputs (DA[0],DB[0] = LSB)
CLKA, CLKB	Port A & B Clocks
CENA, CENB	Port A & B Chip Enables
WENA,WENB	Port A & B Write Enables (Active low)
QA[7:0], QB[7:0]	Port A & B Data Outputs (QA[0],QB[0] = LSB)
EMAA[2:0], EMAB[2:0]	Port A & B Margin Adjustment (EMAA[0],EMAB[0] = LSB)

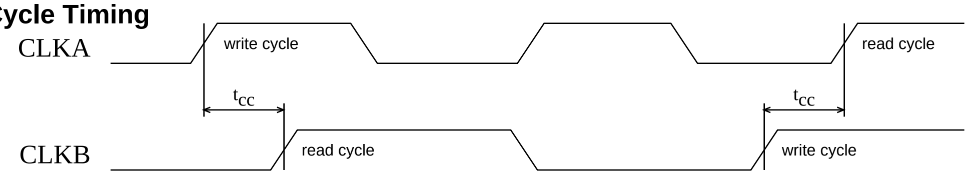
Read Cycle Timing



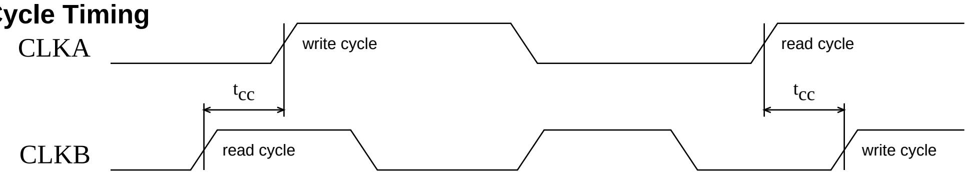
Write Cycle Timing



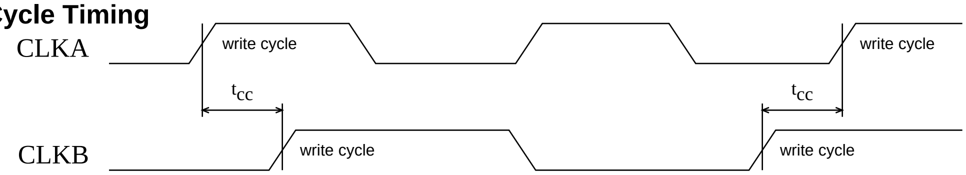
Write to Read Cycle Timing



Read to Write Cycle Timing



Write to Write Cycle Timing



Timing (units = ns)

The timing tables show values measured from the output threshold to the input threshold. The input pins are driven by standard slews. The slews and thresholds vary depending upon the process corner.
The timing tables values are applicable to both A and B ports of the memory even though only the A side is shown.

Pin	Symbol	Fast Process 1.1V, -40°C		Fast Process 1.1V, 125°C		Typical Process 1.0V, 25°C		Slow Process 0.9V, 125°C	
		Min	Max	Min	Max	Min	Max	Min	Max
Cycle time	t_{cyc0}	0.721		0.902		1.099		1.812	
Access time[1,2]	t_{a0}	0.557		0.667			0.995		1.683
Address setup	t_{as}	0.191		0.238		0.306		0.485	
Address hold	t_{ah}	0.000		0.000		0.000		0.000	
Data setup	t_{ds}	0.151		0.182		0.210		0.339	
Data hold	t_{dh}	0.000		0.000		0.000		0.000	
Chip enable setup	t_{cs}	0.250		0.315		0.376		0.629	
Chip enable hold	t_{ch}	0.000		0.000		0.000		0.000	
Write enable setup	t_{ws}	0.230		0.305		0.331		0.519	
Write enable hold	t_{wh}	0.000		0.000		0.000		0.000	
Clock high	t_{ckh}	0.046		0.052		0.074		0.119	
Clock low	t_{ckl}	0.258		0.323		0.406		0.690	
Clock rise slew	t_{ckr}		1.000		1.000		1.000		1.000
Output load factor[3]	K_{load}		0.419		0.525		0.743		1.100

[1] Output delays and a load dependency (Kload) which is used to calculate: *TotalDelay = FixedDelay + (Kload x Cload).*
[2] Access time is defined as the longest possible delay to valid output for the typical and slow corners, and the shortest possible delay for the fast corners.
[3] The output load factor units are ns/pF.

Cycle and Access Timing for Different Values of Extra Margin Adjustment (units = ns)

Pin	Symbol	Fast Process 1.1V, -40°C Min	Max	Fast Process 1.1V, 125°C Min	Max	Typical Process 1.0V, 25°C Min	Max	Slow Process 0.9V, 125°C Min	Max
Cycle time EMAA=0	t_{cyc0}	0.721		0.902		1.099		1.812	
Cycle time EMAA=1	t_{cyc1}	0.824		1.030		1.266		2.106	
Cycle time EMAA=2	t_{cyc2}	1.007		1.275		1.561		2.625	
Cycle time EMAA=3	t_{cyc3}	1.098		1.390		1.709		2.892	
Cycle time EMAA=4	t_{cyc4}	**		**		**		**	
Cycle time EMAA=5	t_{cyc5}	**		**		**		**	
Cycle time EMAA=6	t_{cyc6}	**		**		**		**	
Cycle time EMAA=7	t_{cyc7}	**		**		**		**	
Access time EMAA=0	t_{a0}	0.557		0.667			0.995		1.683
Access time EMAA=1	t_{a1}	0.659		0.796			1.162		1.977
Access time EMAA=2	t_{a2}	0.842		1.040			1.457		2.496
Access time EMAA=3	t_{a3}	0.933		1.155			1.605		2.763
Access time EMAA=4	t_{a4}	**		**			**		**
Access time EMAA=5	t_{a5}	**		**			**		**
Access time EMAA=6	t_{a6}	**		**			**		**
Access time EMAA=7	t_{a7}	**		**			**		**
EMAA setup	t_{emas}	0.721		0.902		1.099		1.812	
EMAA hold	t_{emah}	0.721		0.902		1.099		1.812	

**Illegal setting of EMAA for this corner.

Pin Capacitance (units = fF)

Pin	Fast Process 1.1V, -40°C	Fast Process 1.1V, 125°C	Typical Process 1.0V, 25°C	Slow Process 0.9V, 125°C
AA,AB	60.260	59.740	59.570	57.060
DA,DB	1.889	1.873	1.856	1.746
CLKA,CLKB	115.600	113.400	111.300	109.100
CENA,CENB	42.810	42.070	42.900	41.640
WENA,WENB	48.770	48.010	48.760	47.240
EMAA,EMAB	39.520	38.860	39.510	38.260

Power (current units = mA)

Pin	Fast Process 1.1V, -40°C	Fast Process 1.1V, 125°C	Typical Process 1.0V, 25°C	Slow Process 0.9V, 125°C
AC Current (EMAA=0)[1,4]	6.70E-3	1.26E-2	5.78E-3	5.38E-3
AC Current (EMAA=1)[1,4]	6.70E-3	1.26E-2	5.78E-3	5.38E-3
AC Current (EMAA=2)[1,4]	6.70E-3	1.26E-2	5.78E-3	5.38E-3
AC Current (EMAA=3)[1,4]	6.70E-3	1.26E-2	5.78E-3	5.38E-3
AC Current (EMAA=4)[1,4]	6.70E-3	1.26E-2	5.78E-3	5.38E-3
AC Current (EMAA=5)[1,4]	6.70E-3	1.26E-2	5.78E-3	5.38E-3
AC Current (EMAA=6)[1,4]	6.70E-3	1.26E-2	5.78E-3	5.38E-3
AC Current (EMAA=7)[1,4]	6.70E-3	1.26E-2	5.78E-3	5.38E-3
Read AC Current (EMAA=0)[4]	6.61E-3	1.25E-2	5.70E-3	5.30E-3
Read AC Current (EMAA=1)[4]	6.61E-3	1.25E-2	5.69E-3	5.30E-3
Read AC Current (EMAA=2)[4]	6.61E-3	1.25E-2	5.69E-3	5.30E-3
Read AC Current (EMAA=3)[4]	6.61E-3	1.25E-2	5.69E-3	5.30E-3
Read AC Current (EMAA=4)[4]	6.61E-3	1.25E-2	5.69E-3	5.30E-3
Read AC Current (EMAA=5)[4]	6.61E-3	1.25E-2	5.69E-3	5.30E-3
Read AC Current (EMAA=6)[4]	6.61E-3	1.25E-2	5.69E-3	5.30E-3
Read AC Current (EMAA=7)[4]	6.61E-3	1.25E-2	5.69E-3	5.30E-3
Write AC Current (EMAA=0)[4]	6.80E-3	1.27E-2	5.87E-3	5.46E-3
Write AC Current (EMAA=1)[4]	6.80E-3	1.27E-2	5.87E-3	5.46E-3
Write AC Current (EMAA=2)[4]	6.80E-3	1.27E-2	5.87E-3	5.46E-3
Write AC Current (EMAA=3)[4]	6.80E-3	1.27E-2	5.87E-3	5.46E-3
Write AC Current (EMAA=4)[4]	6.80E-3	1.27E-2	5.87E-3	5.46E-3
Write AC Current (EMAA=5)[4]	6.80E-3	1.27E-2	5.87E-3	5.46E-3
Write AC Current (EMAA=6)[4]	6.80E-3	1.27E-2	5.87E-3	5.46E-3
Write AC Current (EMAA=7)[4]	6.80E-3	1.27E-2	5.87E-3	5.46E-3
Peak Current	37.97	33.28	24.57	15.13
Deselected Current[2,4]	2.57E-3	6.97E-4	2.16E-3	1.91E-3
Standby Current[3]	3.26E-1	8.82	1.64E-1	4.34E-1

** Illegal setting of EMAA for this corner.

[1] The AC current value assumes 50% read and write operations, where all addresses and 50% of input and output pins switch at the user defined frequency of 1.0MHz. It is assumed that EMAA pins do not switch.

[2] The deselected current assumes the memory is deselected, all addresses switch, and 50% of input pins switch at the user defined frequency of 1.0MHz. The logic switching component of deselected power becomes negligbly small if the input pins are held stable by externally controlling these signals with chip select. It is assumed that EMAA pins do not switch.

[3] The standby current value is independent of frequency and assumes all inputs and outputs are stable.

[4] The standby current component is not included in this value.

Clock Noise Limit

Symbol	Fast Process 1.1V, -40°C		Fast Process 1.1V, 125°C		Typical Process 1.0V, 25°C		Slow Process 0.9V, 125°C	
	Pulse Width	Voltage	Pulse Width	Voltage	Pulse Width	Voltage	Pulse Width	Voltage
CLKA, CLKB	10.0ns	0.3V	10.0ns	0.2V	10.0ns	0.3V	10.0ns	0.3V

The clock noise limit is the maximum voltage allowed (for the indicated pulse width) that does not cause an unintentional memory cycle or other memory failure.

Supply Noise Limit (units = V)

Pin	Fast Process 1.1V, -40°C	Fast Process 1.1V, 125°C	Typical Process 1.0V, 25°C	Slow Process 0.9V, 125°C
Power	0.11	0.11	0.10	0.09
Ground	0.11	0.11	0.10	0.09

The power and ground noise limit is the maximum supply voltage transition that is allowed without causing a memory failure.