

1. Introduction

1.1 Features

- Fully integrated battery management solution with battery capacity measurement and programmable protection capability.
- Supports up to 10 Li-ion or Li-Polymer battery cells in series. RAJ240090 supports 3 to 8 series cells, RAJ240100 supports 3 to 10 series cells.
- Integrated with Renesas Ultra Low Power RL78 CPU core for multi-function process
- Memory
 - Code flash memory: 128KB
 - Data flash memory (up to 100,000 erase/write cycles): 4 KB
 - SRAM: 7KB
- Clock generator
 - High speed on-chip oscillator: up to 32 MHz
 - Low speed on-chip oscillator: 32 KHz
 - AFE high speed on-chip oscillator: 4.194 MHz
 - AFE low speed on-chip oscillator: 131.072 KHz
- General Purpose I/O Ports
 - Total: 31 pins
 - CMOS input/output: 20
 - CMOS input: 4
 - N-ch open drain Input/output [6V tolerance]: 4
 - High voltage input/output [VCC tolerance]: 3
- Serial interface
 - CSI (SPI): 2 channels
 - I2C: 1 channel
 - UART: 2 channels
 - Simplified I2C: 2 channels
 - CAN interface (RS-CAN lite): 1 channel
- Timer
 - MCU 16-bit timer: 6 channels
 - MCU 12-bit interval timer: 1 channel
 - MCU Real time clock: 1 channel
 - AFE timer: 2 channels
 - AFE timer A: setting range: 125 ms to 64 s
 - AFE timer B: setting range : 30.52 us to 125 ms
- Embedded A/D converter

1.2 Applications

- E-Bike, E-Scooter, Pedal-Assist Bicycle
- Power Tool, Vacuum Cleaner, Drone
- Battery Backup System, Energy Storage System (ESS)

1.3 Description

RAJ240090 / RAJ240100 are Renesas Li-ion battery fuel gauge IC (FGIC) which consist of a MCU device and an AFE device in a single package. Pack with a variety of battery management features and Renesas RL78 CPU core which has multiple low power modes and capable of achieving high performance in ultra-low power operation. RAJ240090 / RAJ240100 fuel gauge IC have control firmware stored in embedded flash memory to control attached embedded analog and digital circuits to execute battery voltage / current / temperature measurement, remaining capacity estimation, over current / voltage / temperature protection and other battery management operations.

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2. OUTLINE

2.1 Outline of Functions

Caution This outline describes the functions at the time when Peripheral I/O redirection register 0 (PIOR0) is set to “00H”.

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Item		Description
Code flash memory	128 KB	
Data Flash memory	4 KB	
RAM	7 KB	
Address size	1MB	
Main system clock	High speed on-chip Oscillator clock(fIH)	HS (high-speed main) mode: 1 to 32 MHz LS (low-speed main) mode: 1 to 8 MHz ,
Subsystem clock		XT1 (crystal) oscillation, external subsystem clock input (EXCLKS) 32.768 kHz
Low speed on-chip oscillator clock		15 kHz (TYP.)
General purpose register		8 bits × 32 registers (8 bits × 8 registers × 4 banks)
Minimum instruction execution time		0.03125 us(Internal high speed oscillation clock: fIH = 32 MHz) 30.5 us (Subsystem clock : fSUB = 32.768 kHz operation)
Instruction set		<ul style="list-style-type: none"> • Data transmission (8/16 bits) • Addition and subtraction/logical operations (8/16 bits) • Multiplication (8×8 bits,16×16 bits),Division (16÷16 bits,32÷32 bits) • Multiplication and Accumulation (16 bits × 16 bits + 32 bits) • Rotate, barrel shift, bit manipulation (set, reset, test, Boolean operation) etc.
I/O Port	CMOS I/O	20
	CMOS input	4
	N-ch open-drain I/O [6V tolerance)	4
	High voltage I/O	3
Timer	16-bit timer	6 channels (TAU : 4 channels, Timer RD : 2 channels)
	Watchdog timer	1 channel
	Real time clock	1 channel
	12-bit interval timer	1 channel
	Timer output	Timer outputs: 6 channels PWM outputs: 3 channels
	RTC output	1 channel
8/10-bit resolution A/D converter		4 channels
Serial interface	CSI: 1 channel/UART: 1 channel/simplified I2C: 1 channel	
	CSI: 1 channel/UART: 1 channel/simplified I2C: 1 channel	
	I ² C bus	1 channel
Can interface (RS-CAN lite)		1 channel
Vector interrupt source	Internal	22
	External	15 (6 sources is connected to AFE in the chip)
Reset		<ul style="list-style-type: none"> • Reset by RESET pin (reset circuit output of AFE connected to RESETOUT) • Internal reset by watchdog timer • Internal reset by illegal instruction execution <small>Note</small> • internal reset by RAM parity error • internal reset by illegal memory access
On-chip debug function		Support

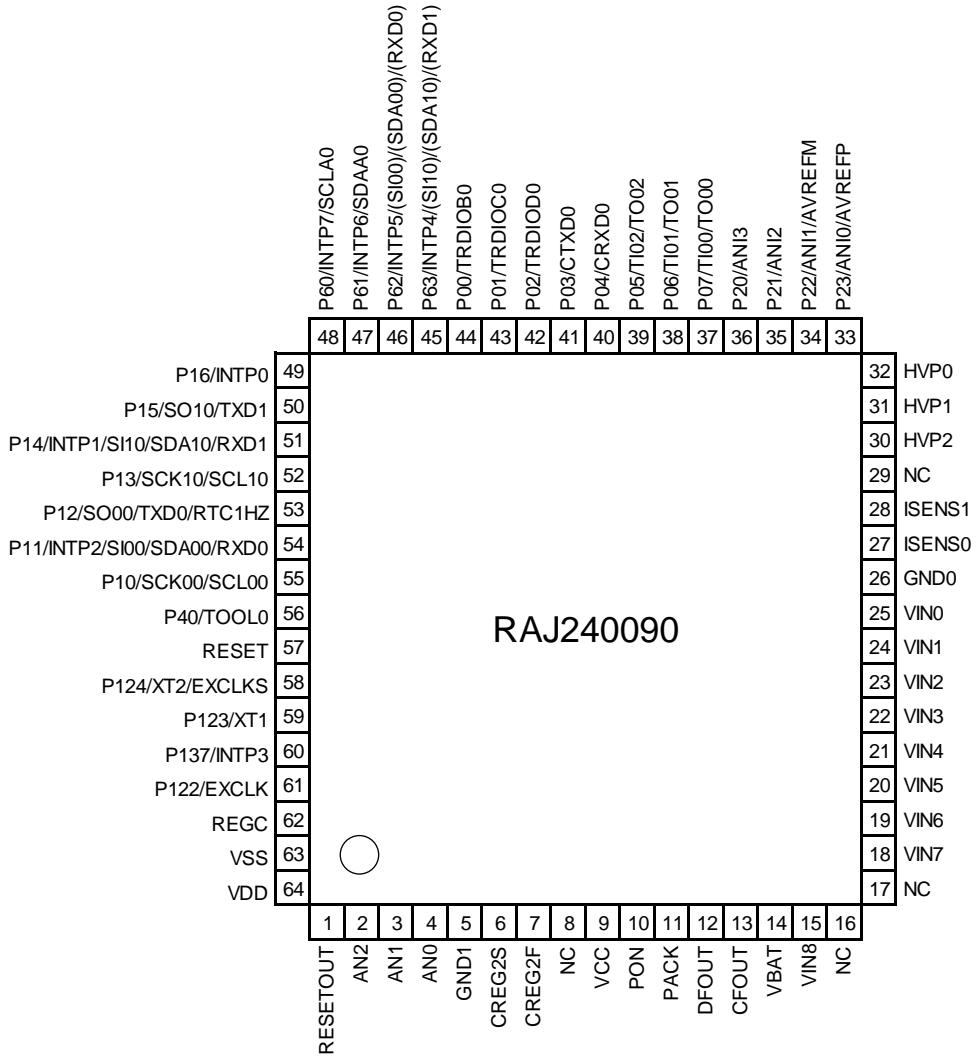
Note The illegal instruction execution is generated when instruction code FFH is executed. Reset by the illegal instruction execution not is issued by emulation with the in-circuit emulator or on-chip debug emulator.

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Item	Description
PWM	8 bits or 10 bits ×1 for FET control
Sigma-delta A/D converter	<p>15-bit resolution (sigma-delta method)</p> <ul style="list-style-type: none"> • Battery Cell voltage (Cell 1 to 8 in RAJ240090, Cell 1 to 10 in RAJ240100) • Battery Cell total voltage (VIN8 pin in RAJ240090, VIN10 pin in RAJ240100) • Charge voltage (PACK pin) • PON pin input voltage • Thermistor sensor port with on-chip pull-up 10kohm resistor: 3 channels • On-chip simple temperature sensor (temperature range: -40 to 85C) • Internal reference and supply voltage (MCU and AFE)
Battery cell voltage and temperature (AN port voltage) detection circuit	<p>Battery Cell voltage detection</p> <ul style="list-style-type: none"> • Over voltage (Overcharge voltage) • Under voltage (Overdischarge voltage) <p>Temperature (AN port voltage) detection</p> <ul style="list-style-type: none"> • Over temperature • Under temperature
Current integrating circuit	1 channel:18-bit resolution
Current integrating circuit for impedance measurement	1 channel:15-bit resolution
Overcurrent detection circuit and wake up current detection circuit	<ul style="list-style-type: none"> • Discharge short-circuit current detection • Discharge overcurrent detection • Charge overcurrent detection, • Wake up current detection (discharge and charge)
Simple temperature sensor	1 channel
Charge/Discharge FET control circuit	NchFET driver for charge control NchFET driver for discharge control
Power on reset circuit	Return from power down mode by detecting voltage and connecting charger
Series regulator	VREG2 : power supply for MCU (3.3 V or 5.0V)
Reset circuit	Series regulator output monitoring (VREG2)
Cell balancing circuit	8 series cells support in RAJ240090 10 series cells support in RAJ240100 (On-resistor: 200ohm TYP)
MCU runaway detection circuit	20 bits×1(2 / 4 / 8 / 16 / 32 / 64 [s] to be selected)
AFE On-chip oscillator	4.194 MHz (TYP)
AFE low speed On-chip oscillator	131.972KHz(TYP)
AFE timer	2 channels <ul style="list-style-type: none"> • AFE timer A (setting range : 125 ms to 64 s) • AFE timer B (setting range : 30.52 us to 125 ms)
MCU-AFE communication interface(C2C)	AFE ~ MCU communication (Chip to Chip Interface)
Power supply voltage	VCC = 4.0 to 50 V
Operation ambient temperature	-20 to 85C (REG2T6 bit (bit6 of REG2T)= 0) -40 to 85C (REG2T6 bit (bit6 of REG2T)= 1)
Package	64 pin plastic mold LQFP([Body] 10.0mm x 10.0mm , 0.5 mm pitch, 1.4 mm thickness)

2.2 RAJ240090 Pin Configuration

- 64 pin plastic mold LQFP ([Body] 10.0mm x 10.0mm , 0.5 mm pitch)



Caution 1. REGC pin connects to VSS pin through a capacitor (0.47 to 1 μ F)

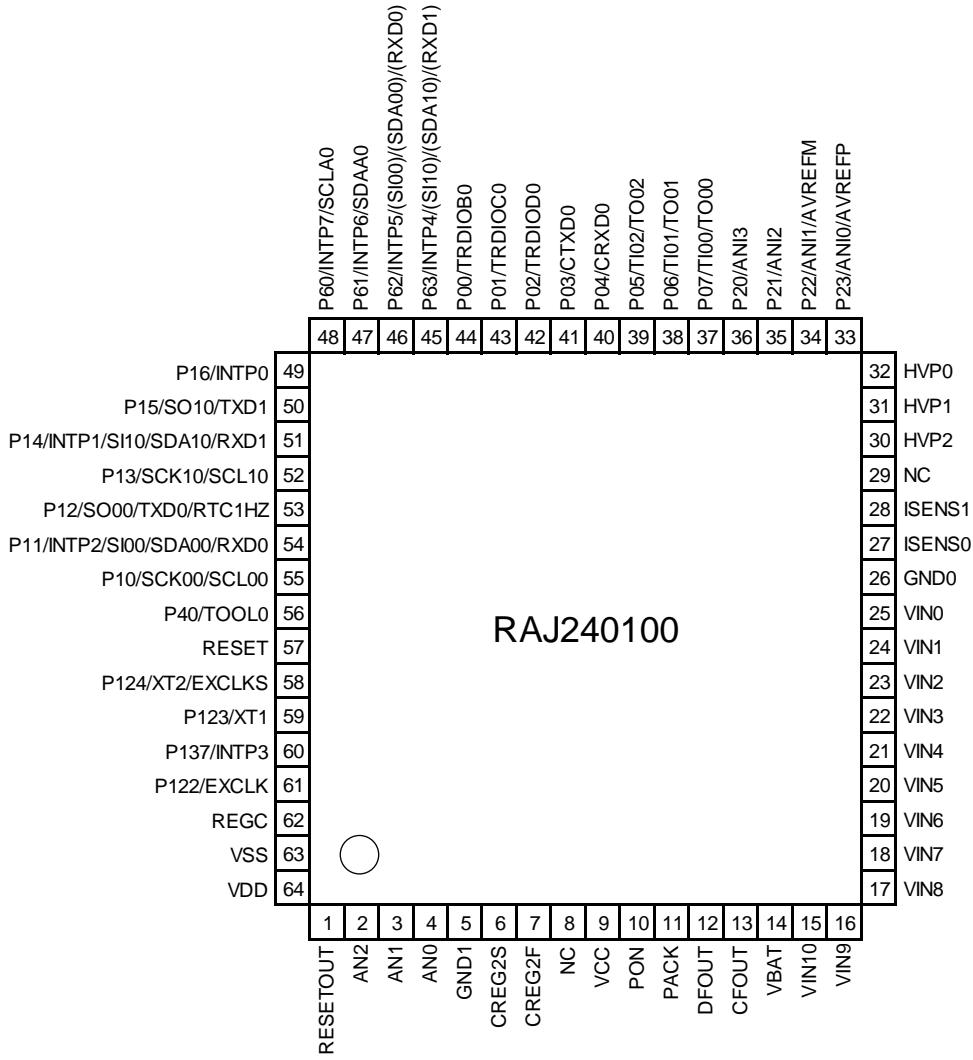
Caution 2. CREG2 pin connects to GND0/GND1 pin through a capacitor (1 to 4.7 μ F).

Remark 1. Pin name refer to [Section 3.1 pin identification].

Remark 2. Functions in parentheses in the above figure can be assigned via settings in the peripheral I/O redirection register 0 (PIOR0).

2.3 RAJ240100 Pin Configuration

- 64 pin plastic mold LQFP([Body] 10.0mm x 10.0mm , 0.5 mm pitch)



Caution 1. REGC pin connects to VSS pin through a capacitor (0.47 to 1 μ F)

Caution 2. CREG2 pin connects to GND0/GND1 pin through a capacitor (1 to 4.7 μ F).

Remark 1. Pin name refer to [Section 3.1 pin identification].

Remark 2. Functions in parentheses in the above figure can be assigned via settings in the peripheral I/O redirection register 0 (PIOR0).

3. PIN FUNCTIONS

3.1 Pin identification

(1/2)

No.	Name	Type	Description
1	RESETOUT	AO	Reset Output
2	AN2	AIN	Analog Input
3	AN1	AIN	Analog Input
4	AN0	AIN	Analog Input
5	GND1	P	Ground
6	CREG2S	P	Regulator Sense
7	CREG2F	P	Regulator Force
8	NC	NC	No connect
9	VCC	P	Power supply
10	PON	HVIN	High voltage Port for power on
11	PACK	HVIN	Charger voltage input
12	DFOUT	HVO	Discharge MOSFET control
13	CFOUT	HVO	Charge MOSFET control
14	VBAT	AIN	Battery voltage input
15	VIN10 for RAJ240100, VIN8 for RAJ240090	AIN	Battery voltage input
16	VIN9 for RAJ240100, NC for RAJ240090	AIN / NC	Battery voltage input (NC for RAJ240090)
17	VIN8 for RAJ240100, NC for RAJ240090	AIN / NC	Battery voltage input (NC for RAJ240090)
18	VIN7	AIN	Battery voltage input
19	VIN6	AIN	Battery voltage input
20	VIN5	AIN	Battery voltage input
21	VIN4	AIN	Battery voltage input
22	VIN3	AIN	Battery voltage input
23	VIN2	AIN	Battery voltage input
24	VIN1	AIN	Battery voltage input
25	VIN0	AIN	Battery voltage input
26	GND0	P	Ground
27	ISENS0	AIN	Analog input for current integration circuit
28	ISENS1	AIN	Analog input for current integration circuit
29	NC	NC	No connect
30	HVP2	HVIO	High Voltage Port
31	HVP1	HVIO	High Voltage Port
32	HVP0	HVIO	High Voltage Port
33	P23 / ANI0 / AVREFP	DIO/AIN	Port2 / Analog Input / Analog Reference Voltage Plus
34	P22 / ANI1 / AVREFM	DIO/AIN	Port2 / Analog Input / Analog Reference Voltage Minus
35	P21 / ANI2	DIO/AIN	Port2 / Analog Input
36	P20 / ANI3	DIO/AIN	Port2 / Analog Input
37	P07 / TI00 / TO00	DIO	Port0 / Timer Input / Timer Output
38	P06 / TI01 / TO01	DIO	Port0 / Timer Input / Timer Output

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No.	Name	Type	Description
39	P05 / TI02 / TO02	DIO	Port0 / Timer Input / Timer Output
40	P04 / CRXD0	DIO	Port0 / CAN Receive Data
41	P03 / CTXD0	DIO	Port0 / CAN Transmit Data
42	P02 / TRDIOD0	DIO	Port0 / Timer Output
43	P01 / TRDIOC0	DIO	Port0 / Timer Output
44	P00 / TRDIOB0	DIO	Port0 / Timer Output
45	P63 / INTP4 / (SI10) / (SDA10) / (RXD1)	DIO	Port6 / External Interrupt Input / Serial Data Input / Serial Data Input/Output / Receive Data
46	P62 / INTP5 / (SI00) / (SDA00) / (RXD0)	DIO	Port6 / External Interrupt Input / Serial Data Input / Serial Data Input/Output / Receive Data
47	P61 / INTP6 / SDAA0	DIO	Port6 / External Interrupt Input / I2C Bus data I/O
48	P60 / INTP7 / SCLA0	DIO	Port6 / External Interrupt Input / I2C Bus clock I/O
49	P16 / INTP0	DIO	Port1 / External Interrupt Input
50	P15 / SO10 / TXD1	DIO	Port1 / Serial Data Output / Transmit Data
51	P14 / INTP1 / SI10 / SDA10 / RXD1	DIO	Port1 / External Interrupt Input / Serial Data Input / Serial Data Input/Output / Receive Data
52	P13 / SCK10 / SCL10	DIO	Port1 / Serial Clock Input/Output
53	P12 / SO00 / TXD0 / RTC1HZ	DIO	Port1 / Serial Data Output / Transmit Data / Real-time Clock Correction Clock (1 Hz) Output
54	P11 / INTP2 / SI00 / SDA00 / RXD0	DIO	Port1 / External Interrupt Input / Serial Data Input / Serial Data Input/Output / Receive Data
55	P10 / SCK00 / SCL00	DIO	Port1 / Serial Clock Input/Output
56	P40 / TOOL0	DIO	Port4 / Data Input/Output for Tool
57	RESET	DIN	Reset Input for MCU
58	P124 / XT2 / EXCLKS	DI	Port12 / Crystal Oscillator Input / External Clock Input
59	P123 / XT1	DI	Port12 / Crystal Oscillator Input
60	P137 / INTP3	DI	Port13 / External Interrupt Input
61	P122/EXCLK	DI	Port12 / External Clock Input
62	REGC	P	Regulator Capacitance
63	VSS	P	Ground
64	VDD	P	Power Supply

Remark Functions in parentheses in the above figure can be assigned via settings in the peripheral I/O redirection register 0 (PIOR0).

HVO: high voltage output**DIO:** digital I/O**HVIN:** high voltage input**DIN:** digital input**HVIO:** high voltage input/output**AIN:** analog input**P:** power**AO:** analog output

3.2 Pin Functions

3.2.1 Pin type and alternate functions

Function name	Pin Type	I/O	After Reset Release	Alternate Function	Function
P00	7-1-7	I/O	Input port	TRDIOB0	Port 0. 8-bit I/O port. Input/output can be specified in 1-bit unit. Use of an on-chip pull-up resistor can be specified by a software setting at input port. Input of P03 and P04 can be set to TTL input buffer. Output of P03 and P04 can be set to N-ch open-drain output (VDD tolerance).
P01	7-1-7			TRDIOC0	
P02	7-1-7			TRDIOD0	
P03	8-1-4			CTXD0	
P04	8-1-4			CRXD0	
P05	7-1-3			TI02/TO02	
P06	7-1-3			TI01/TO01	
P07	7-1-3			TI00/TO00	
P10	8-1-4	I/O	Input port	SCK00/SCL00	Port 1. 7-bit I/O port. Input/output can be specified in 1-bit unit. Use of an on-chip pull-up resistor can be specified by a software setting at input port. Input of P10 to P14 can be set to TTL input buffer. Output of P10 to P16 can be set to N-ch open-drain output (VDD tolerance).
P11	8-1-4			INTP2/SI00/SDA00/RXD0	
P12	7-1-4			SO00/TXD0/RTC1HZ	
P13	8-1-4			SCK10/SCL10	
P14	8-1-4			INTP1/SI10/SDA10/RXD1	
P15	7-1-4			SO10/TXD10	
P16	7-1-4			INTP0	
P20	4-3-3	I/O	Analog function	ANI3	Port 2. 4-bit I/O port. Input/output can be specified in 1-bit unit. Can be set to analog input Note 1.
P21	4-3-3			ANI2	
P22	4-3-3			ANI1/AVREFM	
P23	4-3-3			ANI0/AVREFP	
P30	7-1-3	I/O	Input port	INTP13	Port 3. Note 2. 4-bit I/O port. Input/output can be specified in 1-bit unit. Use of an on-chip pull-up resistor can be specified by a software setting at input port.
P31	7-1-3			INTP12	
P32	7-1-3			INTP11	
P33	7-1-3			INTP10	
P40	7-1-3	I/O	Input port	TOOL0	Port 4. 1-bit I/O port. Input/output can be specified in 1-bit unit. Use of an on-chip pull-up resistor can be specified by a software setting at input port.
P60	12-1-2	I/O	Input port	INTP7/SCLA0	Port 6. 4-bit I/O port. Input/output can be specified in 1-bit unit. Output of P60 to P63 can be set to N-ch open-drain output (6.0V tolerance).
P61	12-1-2			INTP6/SDAA0	
P62	12-1-2			INTP5/(SI00)/(SDA00)/(RXD0)	
P63	12-1-2			INTP4/(SI10)/(SDA10)/(RXD1)	
P70	7-1-3	I/O	Input port	INTP9	Port 7. Note 2. 8-bit I/O port. Input/output can be specified in 1-bit unit. Use of an on-chip pull-up resistor can be specified by a software setting at input port.
P71	7-1-3			INTP8	
P72	7-1-3			EXBSEL	
P73	7-1-3			EXBCK	
P74	7-1-3			EXB00/EXB10	
P75	7-1-3			EXB01/EXB11	
P76	7-1-3			EXB02/EXB12	
P77	7-1-3			EXB03/EXB13	
P122	2-2-2	input	Input port	EXCLK	Port 12. 3-bit input-only port.
P123	2-2-1			XT1	
P124	2-2-1			XT2/EXCLKS	
P137	2-1-2	input	Input port	INTP3	Port 13. 1-bit input-only port.
RESET	2-1-1	input	-	-	Input-only pin for external reset. Connect to VDD directly or via a resistor when external reset is not used.

Note 1. Each pin can be configured as digital or analog pin by setting the port mode in the control register x (PMCx)
(Can be specified in 1-bit units).

Note 2. Connected to internal AFE circuit.

3.2.2 External Pin Functions

(1/2)

Category	Pin name	I/O	Function
Power supply	VCC	—	Power supply input Apply power supply voltage to VCC pin from a charger or battery.
	GND0、GND1	—	Device ground input. Connect the negative input terminal of lithium-ion battery 1 to the GND0 and GND1 pins
	CREG2F	—	Series regulator force port
	CREG2S	—	Series regulator sense port Connect to GND0 and GND1 via a capacitor (1uF to 4.7uF)
	VDD	—	Positive power supply for MCU Connect to CREG2
	VSS	—	Ground input for MCU Connect the negative input terminal of lithium-ion battery 1 to the GND0 and GND1 pins
RESET	RESET	Input	This is the active-low system reset input pin for MCU.
	RESETOUT	output	This is the active-low system reset output pin for AFE.
TOOL0	TOOL0 Note 2	input	Data I/O for flash memory programmer/debugger. Connect to the VDD via an external pull-up resistor in the on chip debug mode
Serial interface (UART0, UART1)	RxD0, RxD1	input	Serial data input pins of serial interface UART0 to UART1
	TxD0, TxD1	output	Serial data output pins of serial interface UART0 to UART1
Serial interface (CSI00, CSI10)	SCK00,SCK10	I/O	Serial clock I/O pins of serial interface CSI00 and CSI10
	SI00, SI10	input	Serial data input pins of serial interface CSI00 and CSI10
	SO00, SO10	output	Serial data output pins of serial interface CSI00 and CSI10
Serial interface (IIC00, IIC10)	SCL00, SCL10	output	Serial clock output pins of serial interface IIC00 and IIC10
	SDA00, SDA10	I/O	Serial data I/O pins of serial interface IIC00 and IIC10
Serial interface (IICA0)	SCLA0	I/O	Serial clock I/O pins of serial interface IICA0
	SDAA0	I/O	Serial data I/O pins of serial interface IICA0,
CAN-BUS interface	CRXD0	input	CAN serial data input
	CTXD0	output	CAN serial data output
A/D converter	AN0, AN1, AN2	input	AFE A/D converter analog input
	AN10, AN11, AN12, AN13	input	MCU A/D converter analog input
	AVREFP	input	A/D converter reference voltage (+ side).
	AVREFM	input	A/D converter reference voltage (- side).
Current integration circuit and overcurrent detection circuit	ISENS0、ISENS1	input	Analog input for current integration circuit and over current detection circuit
Timer	TI00-TI02	input	The pins for inputting an external count clock/capture trigger to 16-bit timers 00 to 02
	TO00-TO02	output	Timer output pins of 16-bit timers 00 to 02
	TRDIOB0 TRDIOC0 TRDIOD0	I/O	Timer RD input/output
	RTC1HZ	output	Real-time clock supports clock (1 Hz) output

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Category	Pin name	I/O	Function
High voltage I/O port	HVP0, HVP1, HVP2	I/O	High voltage I/O in correspondence with VCC tolerance
Subsystem clock	XT1, XT2 ^{Note 3}	—	Resonator connection for subsystem clock
External clock	EXCLK	Input	External clock input for main system clock
	EXCLKS	input	External clock input for subsystem clock
External interrupt input	INTP0 to INTP13	input	Interrupt request input pin. INTP8 to INTP13 connects interrupt request signal of AFE in the package and do not connect to any pin
Power on circuit	PON	input	Power on input for release from power down state
Charger connection detect	PACK	Input	Charger voltage input and source voltage of discharge FET drive port (DFOUT)
Battery connection detect	VBAT	input	Sense voltage input pin for most positive cell and source voltage for charge FET drive port (CFOUT)
Battery voltage detection circuit	VIN10 ^{Note 4}	input	The positive input terminal of lithium-ion battery 10.
	VIN9 ^{Note 4}	Input	The negative input terminal of lithium-ion battery 10 and the positive input terminal of lithium-ion battery 9
	VIN8	Input	The negative input terminal of lithium-ion battery 9 and the positive input terminal of lithium-ion battery 8
	VIN7	Input	The negative input terminal of lithium-ion battery 8 and the positive input terminal of lithium-ion battery 7
	VIN6	Input	The negative input terminal of lithium-ion battery 7 and the positive input terminal of lithium-ion battery 6
	VIN5	Input	The negative input terminal of lithium-ion battery 6 and the positive input terminal of lithium-ion battery 5
	VIN4	Input	The negative input terminal of lithium-ion battery 5 and the positive input terminal of lithium-ion battery 4
	VIN3	Input	The negative input terminal of lithium-ion battery 4 and the positive input terminal of lithium-ion battery 3
	VIN2	Input	The negative input terminal of lithium-ion battery 3 and the positive input terminal of lithium-ion battery 2
	VIN1	Input	The negative input terminal of lithium-ion battery 2 and the positive input terminal of lithium-ion battery 1
	VIN0	Input	The negative input terminal of lithium-ion battery 1
FET control output	DFOUT	Output	ON/OFF signal output pin for discharge FET.
	CFOUT	Output	ON/OFF signal output pin for charge FET.
Communication between AFE and MCU	P72	input	Control signal of communication between AFE and MCU with setting to output port. P72 is connected to AFE in a package and not external pin.
	EXBCK	Output	Clock signal of communication between AFE and MCU
	EXBD0-3	I/O	Data signal of communication between AFE and MCU

Note 1. REGC is not external power supply pin. (Do not draw current from REGC.)

Note 2. After reset release, the connection between P40/TOOL0 and the operating mode are as follows.

Table 3-1 TOOL0 Pin Operation Mode after Reset Release

P40/TOOL0	Operation Mode
VDD	Normal operation mode
0V	Flash memory programming mode

Note 3. Figure 3-1 shows an example of the external circuit for the XT1 oscillator

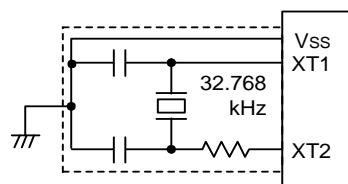


Figure 3-1 Example of External Circuit for XT1 Oscillator

Note 4. VIN10 pin and VIN9 pin are only applicable to RAJ240100.

3.3 Pin Block Diagram

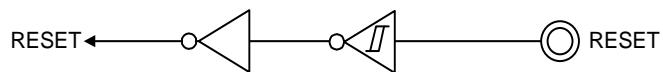
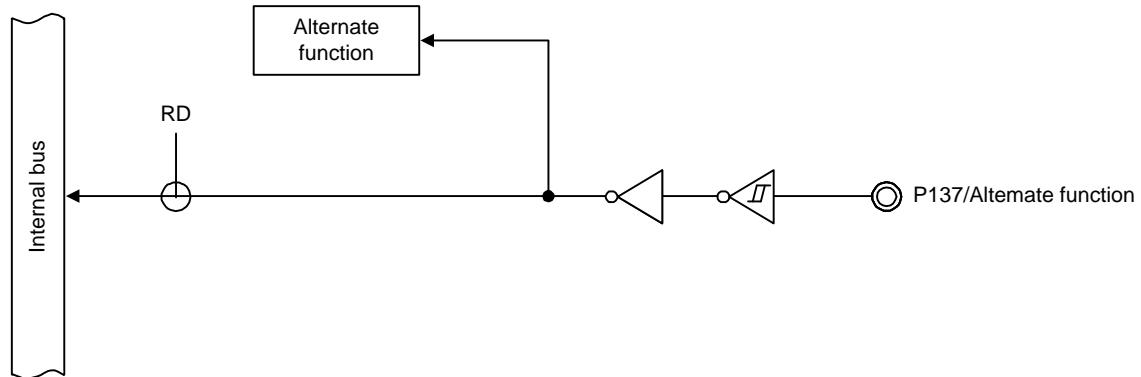
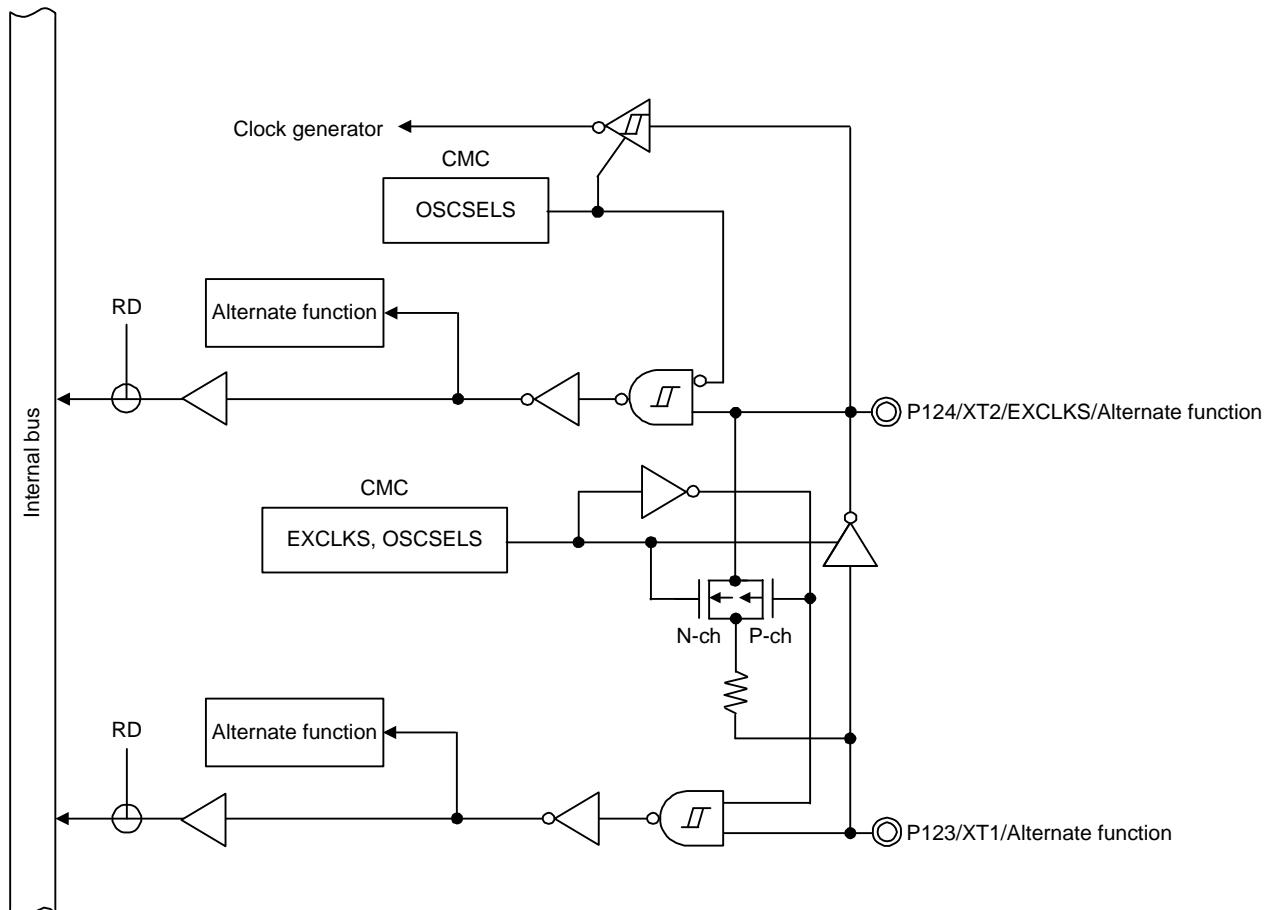


Figure 3-2 Pin Block Diagram for Pin type 2-1-1



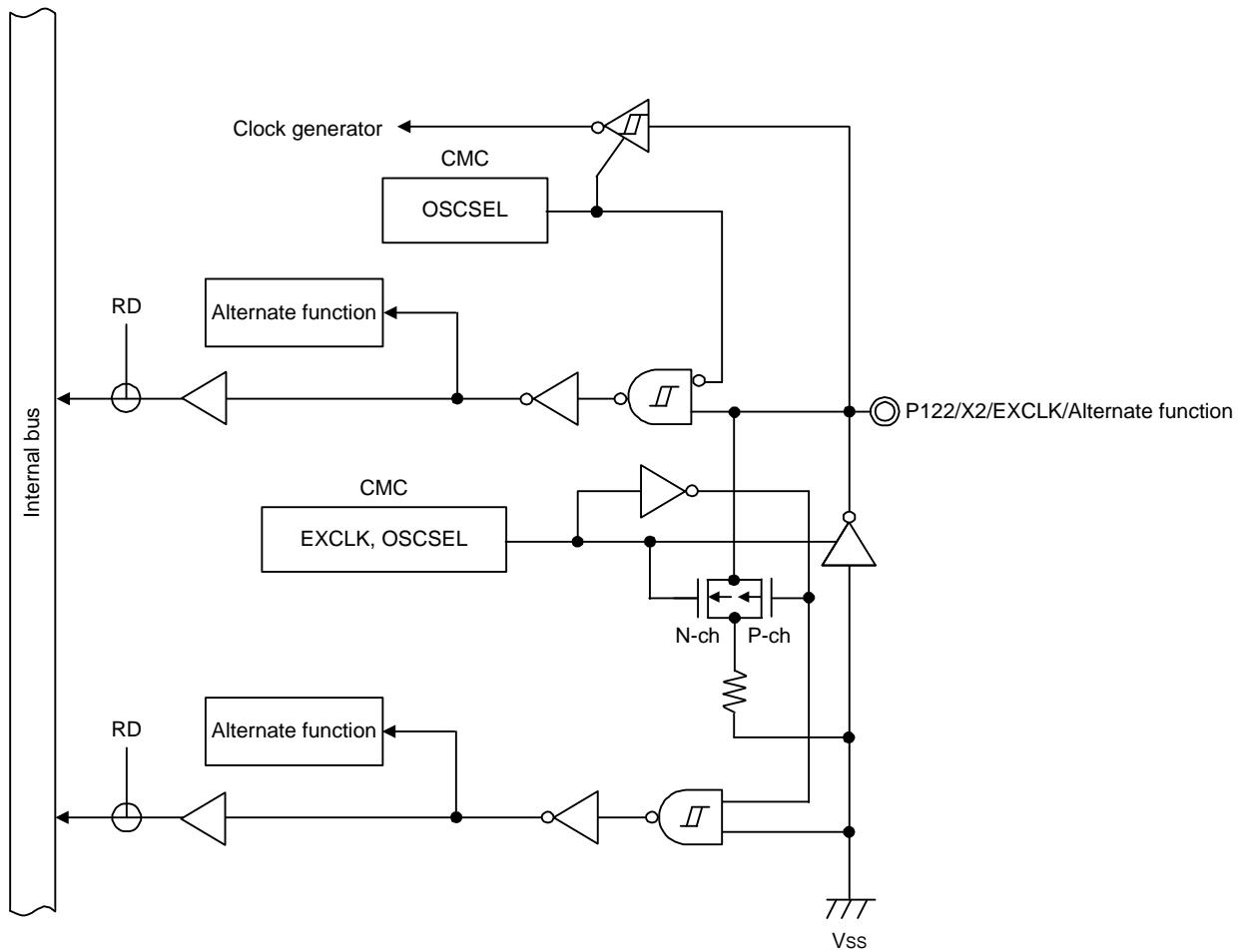
Remark Refer to Section 3.2.1 Pin type and alternate function for alternate functions.

Figure 3-3 Pin Block Diagram for Pin type 2-1-2



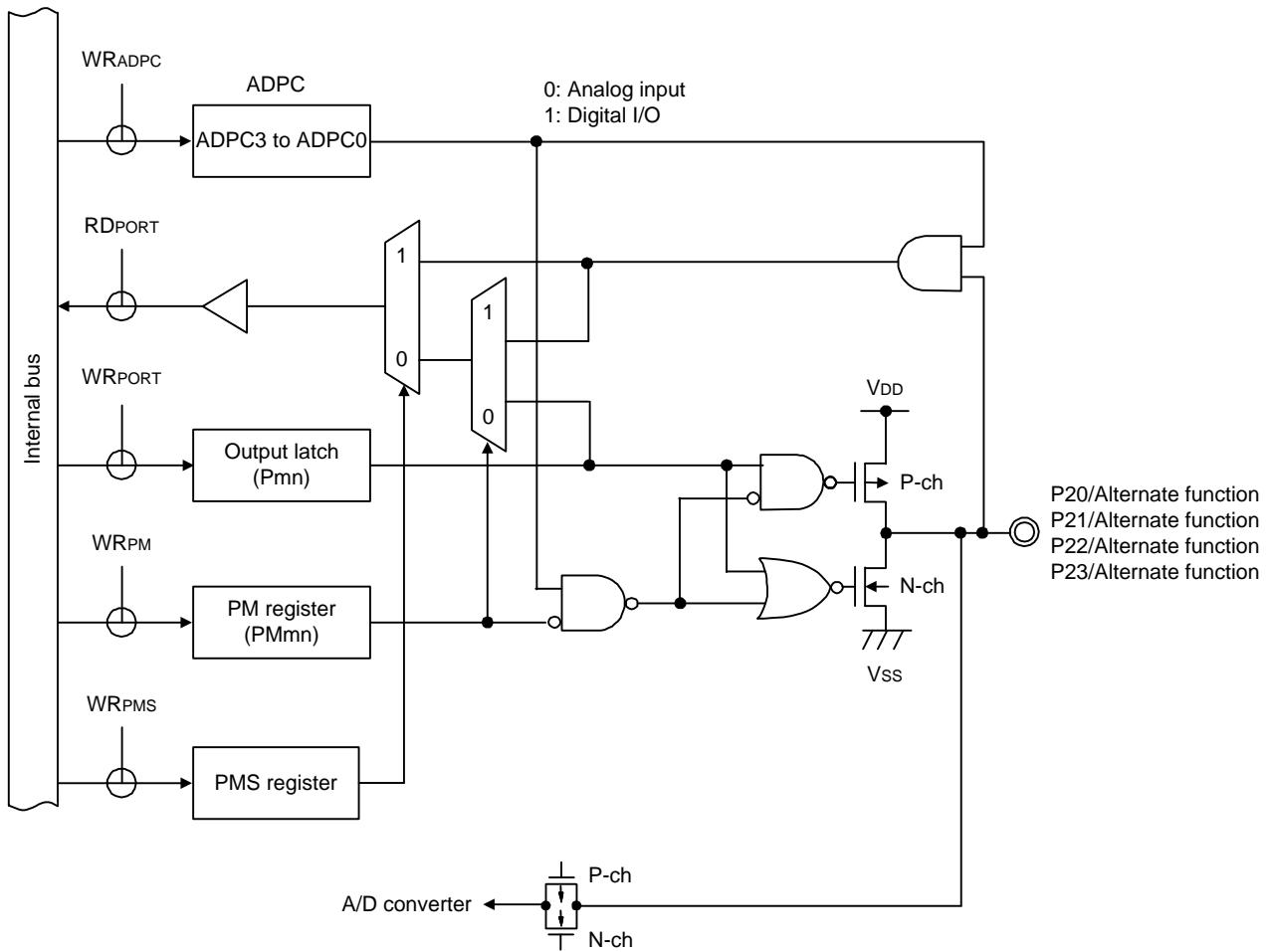
Remark Refer to Section 3.2.1 Pin type and alternate function for alternate functions.

Figure 3-4 Pin Block Diagram for Pin type 2-2-1



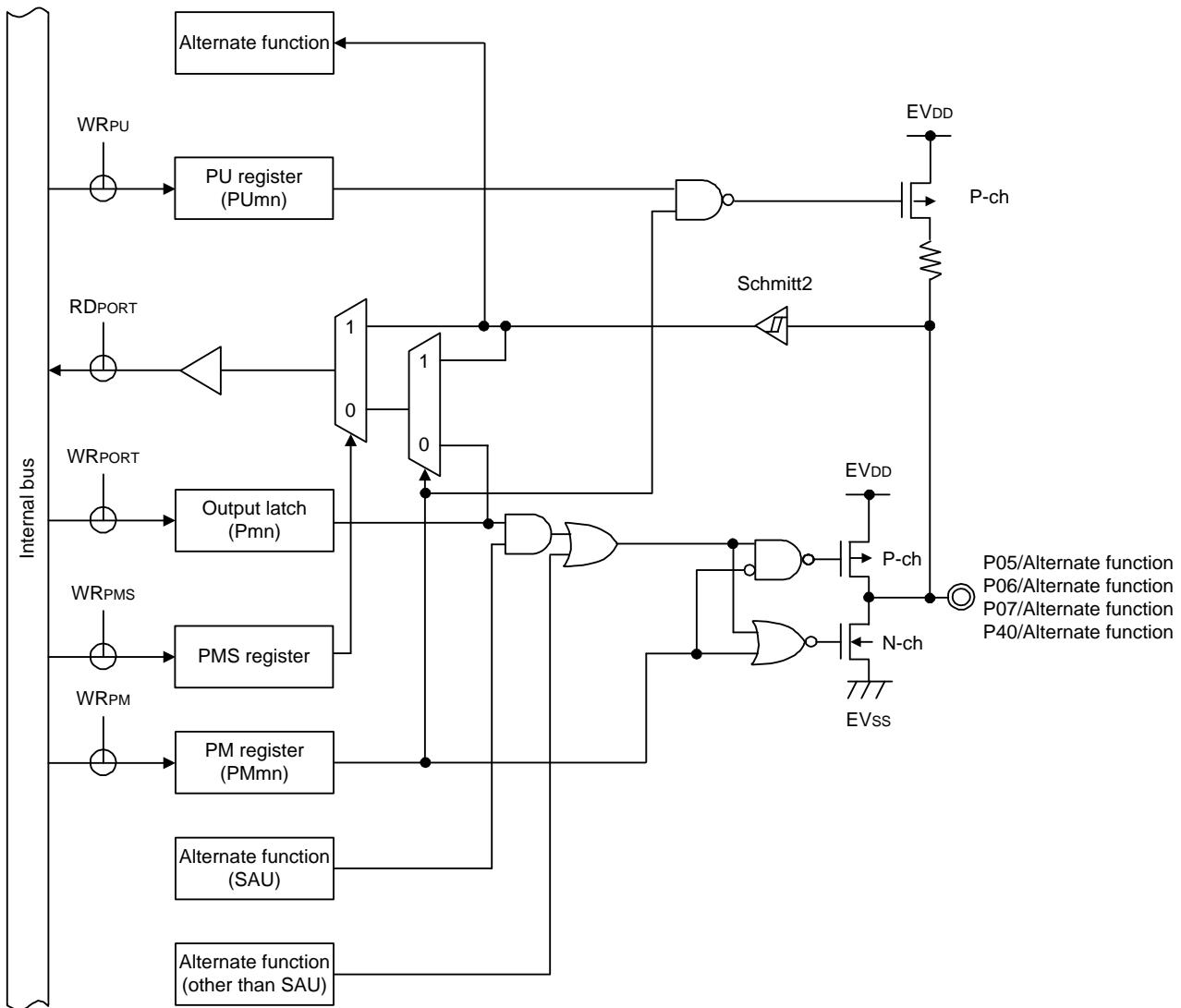
Remark Refer to Section 3.2.1 Pin type and alternate function for alternate functions.

Figure 3-5 Pin Block Diagram for Pin type 2-2-2



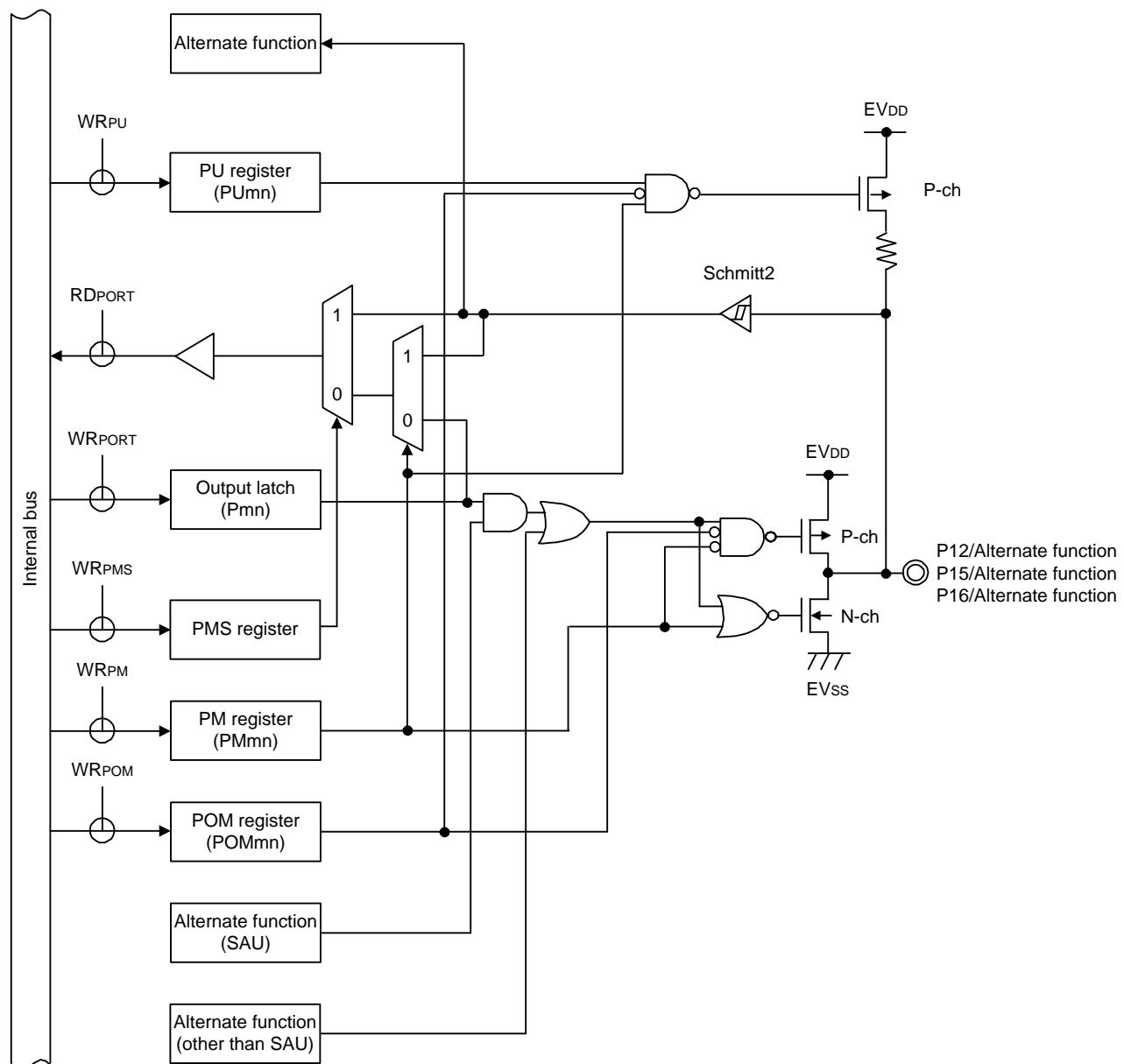
Remark Refer to Section 3.2.1 Pin type and alternate function for alternate functions.

Figure 3-6 Pin Block Diagram for Pin type 4-3-3



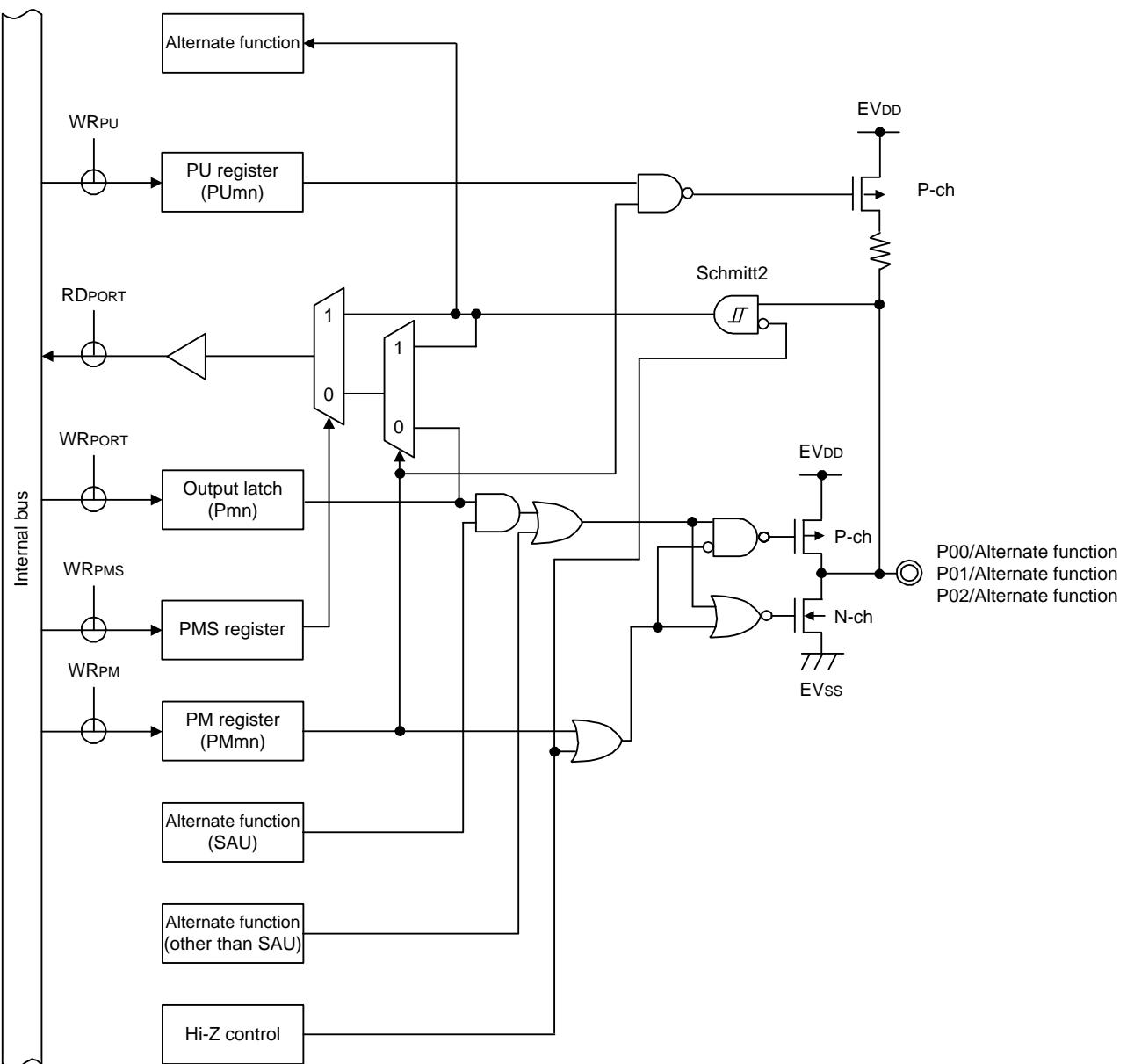
Remark Refer to Section 3.2.1 Pin type and alternate function for alternate functions.

Figure 3-7 Pin Block Diagram for Pin type 7-1-3



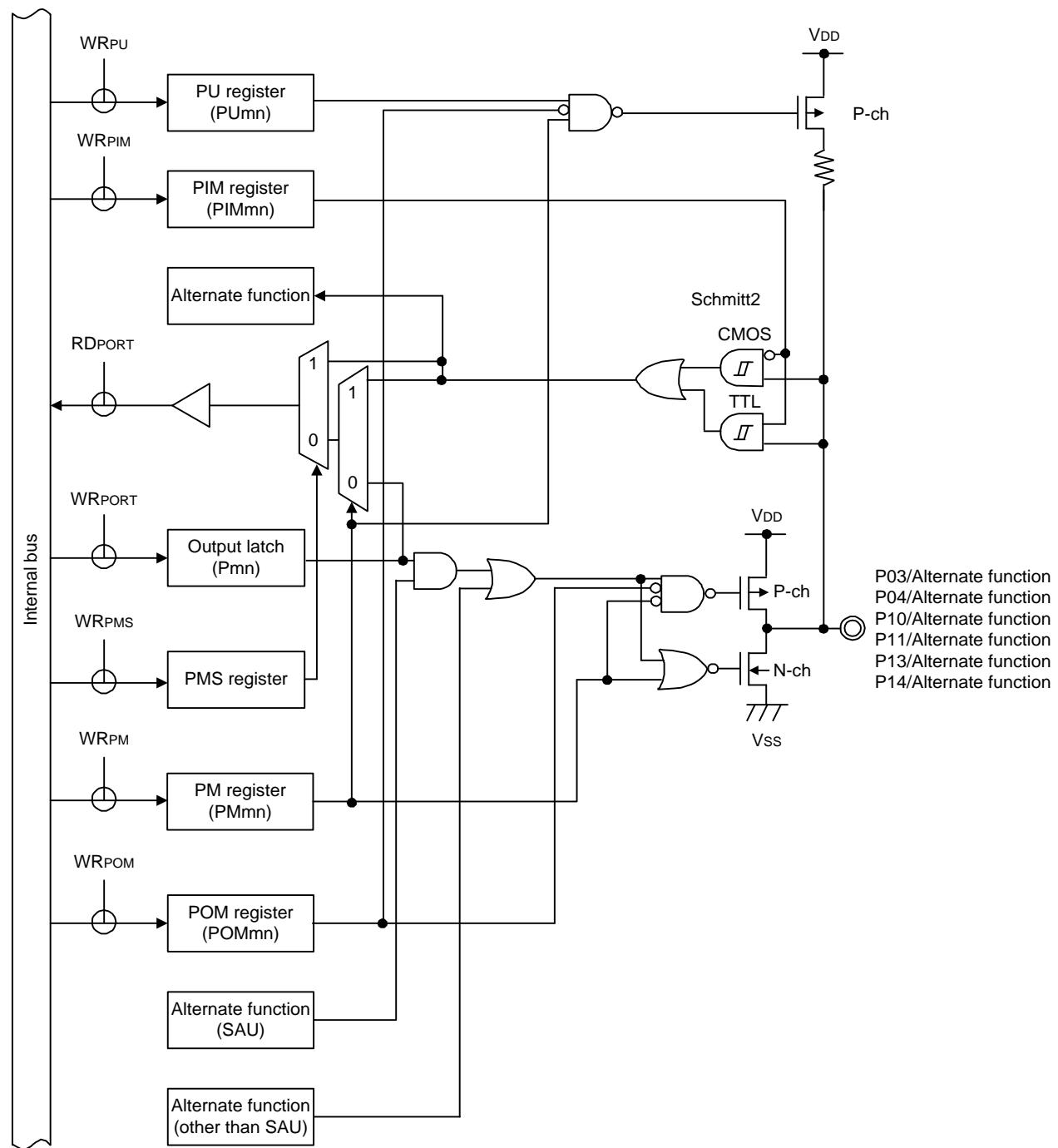
Remark Refer to Section 3.2.1 Pin type and alternate function for alternate functions.

Figure 3-8 Pin Block Diagram for Pin type 7-1-4



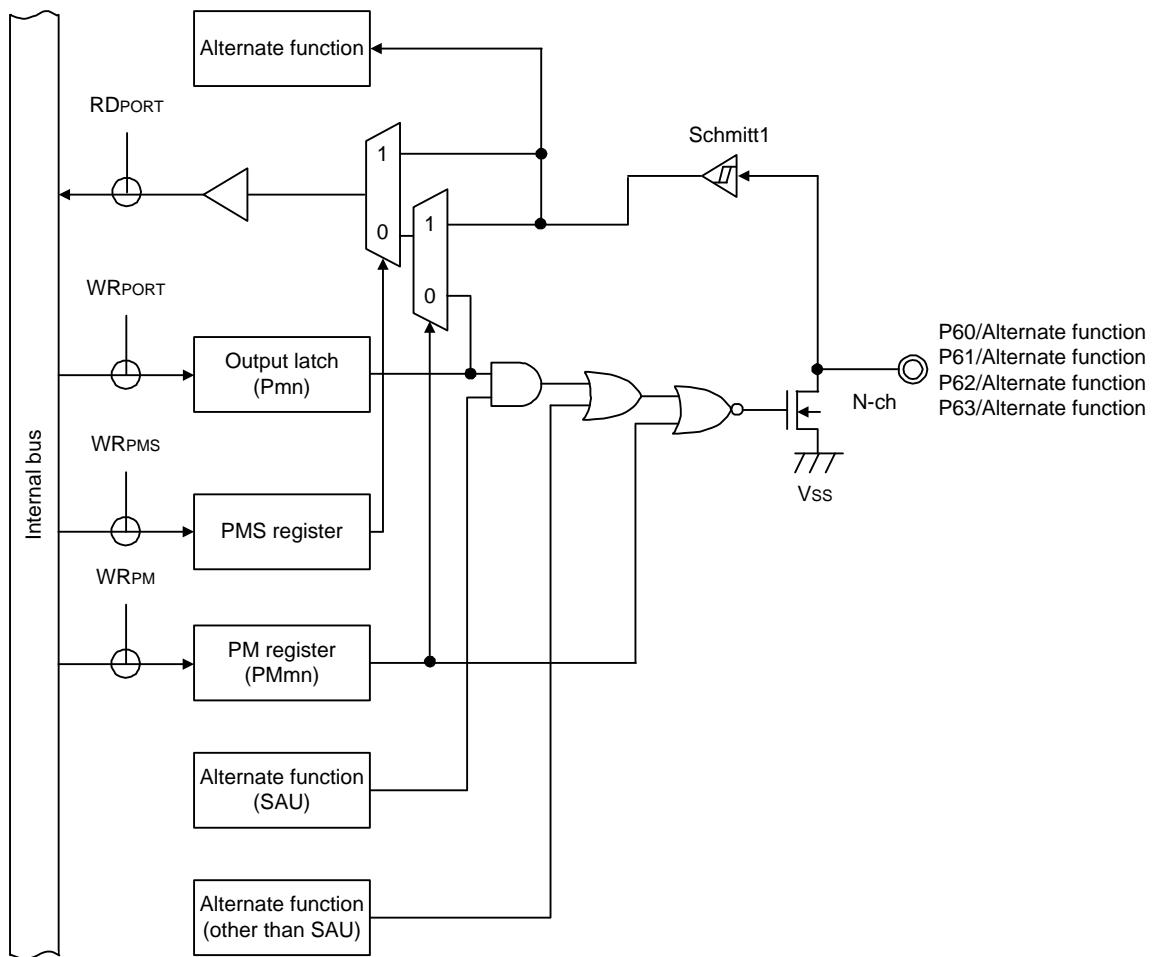
Remark Refer to Section 3.2.1 Pin type and alternate function for alternate functions.

Figure 3-9 Pin Block Diagram for Pin type 7-1-7



Remark Refer to Section 3.2.1 Pin type and alternate function for alternate functions.

Figure 3-10 Pin Block Diagram for Pin type 8-1-4



Remark Refer to Section 3.2.1 Pin type and alternate function for alternate functions.

Figure 3-11 Pin Block Diagram for Pin type 12-1-2

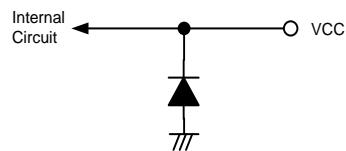


Figure 3-12 Pin Block Diagram for VCC Pin

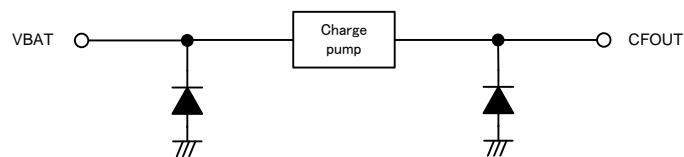


Figure 3-13 Pin Block Diagram for VBAT and CFOUT Pin

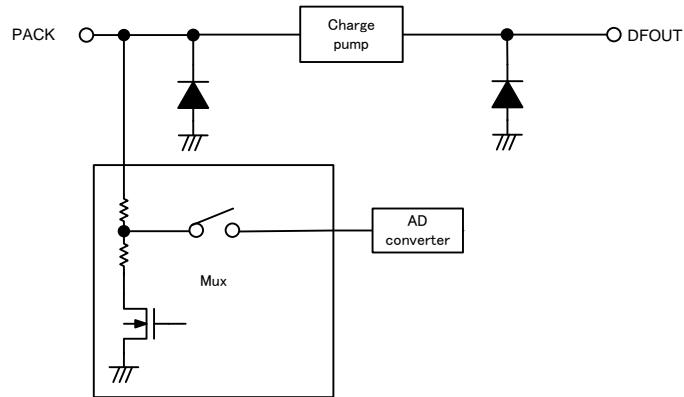


Figure 3-14 Pin Block Diagram for VPACK and DFOUT Pin

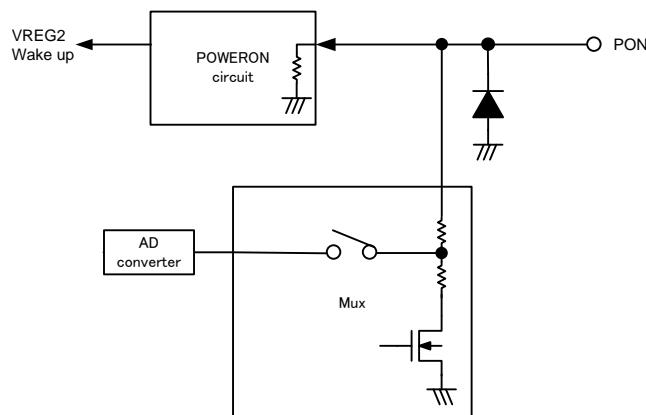
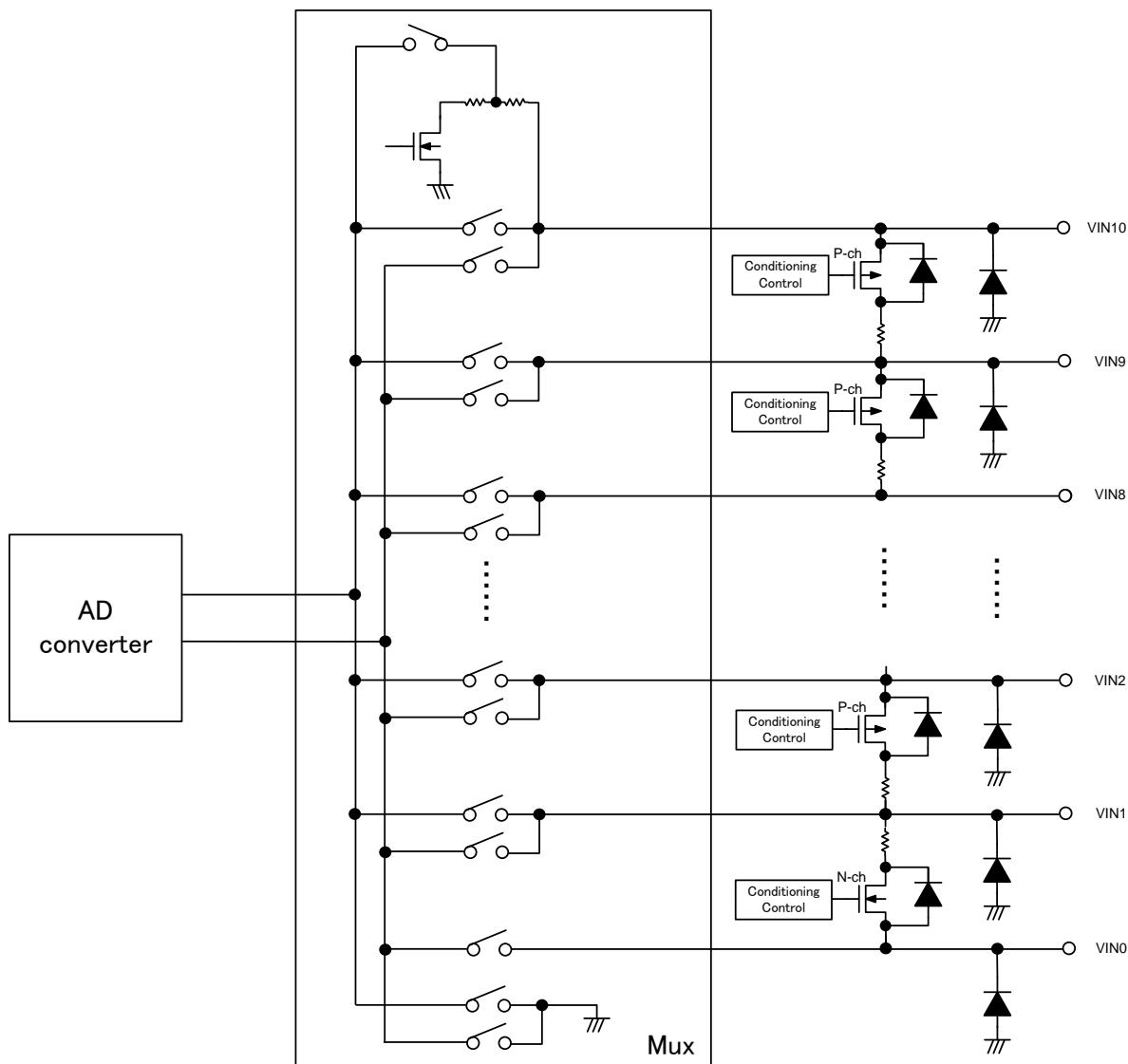


Figure 3-15 Pin Block Diagram for PON Pin



Caution 1. VIN10 pin and VIN9 pin are only applicable to RAJ240100.

Caution 2. For RAJ240090, VIN8 pin is connected to ladder resistors.

Figure 3-16 Pin Block Diagram for VIN10 to VIN0 Pin

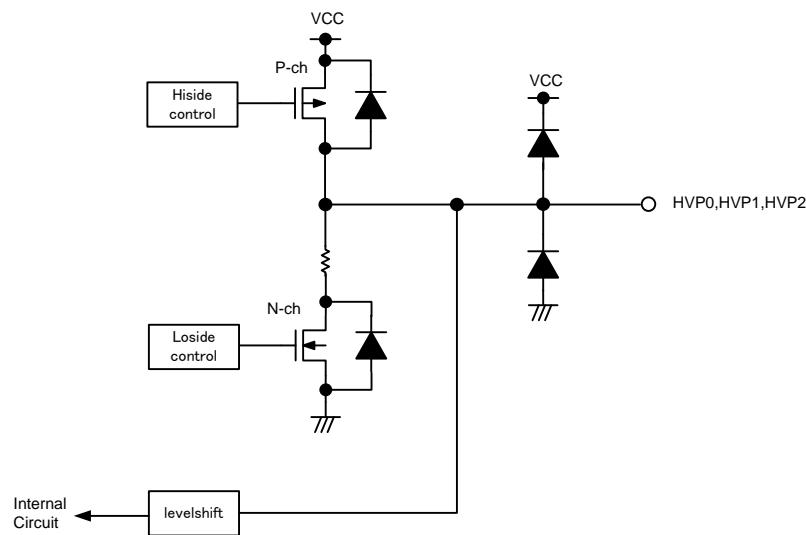


Figure 3-17 Pin Block Diagram for HVP0, HVP1 and HVP2 Pin

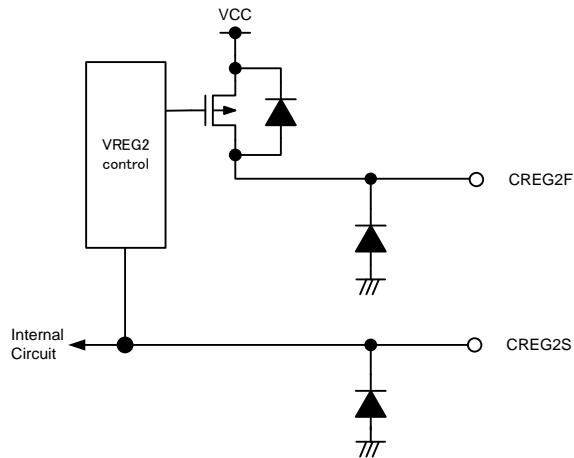


Figure 3-18 Pin Block Diagram for CREG2F and CREG2S Pin

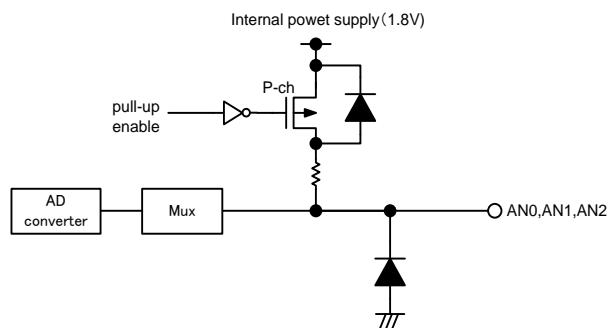


Figure 3-19 Pin Block Diagram for AN0, AN1 and AN2 Pin

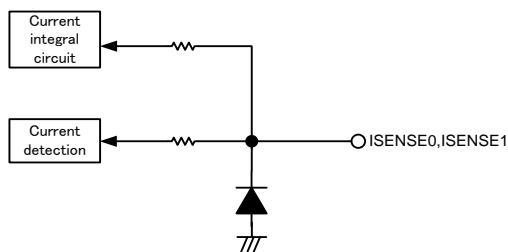


Figure 3-20 Pin Block Diagram for ISENSE0 and ISENSE1 Pin

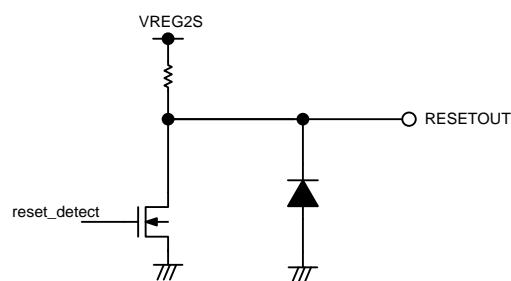


Figure 3-21 Pin Block Diagram for RESETOUT Pin

4. ELECTRICAL SPECIFICATIONS

Caution This product has an on-chip debug function, which is provided for development and evaluation. Do not use the on-chip debug function in products designated for mass production because the guaranteed number of rewritable times of the flash memory may be exceeded when this function is used, and product reliability therefore cannot be guaranteed. Renesas Electronics is not liable for problems occurring when the on-chip debug function is used.

Remark 1. Specifications for VIN10 pin and VIN9 pin are only applicable to RAJ240100.

Remark 2. Operating ambient temperature is configurable by REG2T6 bit of REG2T register setting.

In case of setting REG2T6 bit of REG2T register to "0", this device is available in range of TA= -20 to 85C.

In case of setting REG2T6 bit of REG2T register to "1", this device is available in range of TA= -40 to 85C.

However, even if REG2T6 bit of REG2T register set to "1", the electrical characteristics which is guaranteed in range of TA = -20 to 85C is not changed.

4.1 Absolute Maximum Ratings

Absolute Maximum Ratings

Parameter	Symbols	Conditions		Ratings	Unit
Supply voltage	V _{CC}	V _{CC}		-0.5 to +60.0	V
	V _{DD}	V _{DD}		-0.5 to +6.5	V
	GND	GND ₀ , GND ₁ , V _{SS}		-0.5 to 0.3	V
CREG2 pin input voltage	V _{CREG2}	CREG2F		-0.5 to +60.0	V
		CREG2S		-0.3 to 6.5 Note 2	V
REGC pin input voltage	V _{IREGC}	REGC		-0.3 to 2.8 and -0.3 to (V _{DD} +0.3) Note 1	V
Input voltage	V _{I1}	P00 to P07, P10 to P16, P20 to 23, P40 (TOOL0), P122 to P124, P137, RESET		-0.3 to (V _{DD} +0.3) Note 3	V
	V _{I2}	P60 to P63(N-ch open-drain)		-0.3 to +6.5	V
	V _{IN-H1}	VIN10, VIN9, VIN8, VIN7, VIN6, VIN5, VIN4, VIN3, VIN2, VIN1, VBAT, PACK, PON,		-0.5 to +60.0	V
	V _{IN-H2}	HVP0, HVP1, HVP2		-0.5 to (V _{DD} +0.3) Note 5	V
	V _{IN-B}	VIN10 to VIN9, VIN9 to VIN8, VIN8 to VIN7, VIN7 to VIN6, VIN6 to VIN5, VIN5 to VIN4, VIN4 to VIN3, VIN3 to VIN2, VIN2 to VIN1, VIN1 to VINO		-0.5 to +6.5	V
	V _{IN-M}	VINO		-0.5 to +5.0	V
	V _{IN-L}	AN0, AN1, AN2, ISENS0, ISENS1		-0.5 to +2.0	V
	V _{AI}	ANI00 to ANI03		-0.3 to V _{DD} +0.3 and -0.3 to AVREF(+) +0.3 Notes 3, 4	V
Output voltage	V _{O1}	P00 to P07, P10 to P16, P20 to 23, P40 (TOOL0), P123, P124, RESETOUT		-0.3 to (V _{DD} +0.3) Note 3	V
	V _{O-H}	CFOUT, DFOUT, HVP0, HVP1, HVP2		-0.5 to +60.0	V
High-level output current	I _{OH1}	Per pin	P00 to P07, P10 to P16, P40 (TOOL0)	-40	mA
		Total of all pins	P00 to P07, P10 to P16, P40 (TOOL0)	-70	mA
	I _{OH2}	Per pin	P20 to P23	-0.5	mA
		Total of all pins	P20 to P23	-2.0	mA
Low-level output current	I _{OL1}	Per pin	P00 to P07, P10 to P16, P40 (TOOL0)	+40	mA
		Total of all pins	P00 to P07, P10 to P16, P40 (TOOL0), P60 to P63	+70	mA
Power consumption	P _d	Topr = 25 C		300	mW
Operating ambient Temperature	TA	REG2T6 bit = 0		-20 to +85	C
T _{AL}	REG2T6 bit = 1		-40 to +85		C
Storage temperature	T _{stg}	-		-65 to +150	C

(Note, Caution and Remark are listed on next page.)

- Note 1.** Connect the REGC pin to VSS via a capacitor (0.47 to 1uF). This value regulates the absolute maximum rating of the REGC pin. Do not use this pin with voltage applied to it.
- Note 2.** Connect the CREG2 pin to GND0 or GND1 via a capacitor (2.2uF). This value regulates the absolute maximum rating of the CREG2 pin.
- Note 3.** Must be 6.5V or lower.
- Note 4.** Do not exceed AVREF (+) + 0.3V in case of A/D conversion target pin.
- Note 5.** Must be 60V or lower.
- Caution** **Product quality may degrade if the absolute maximum rating has been exceeded. The absolute maximum ratings are rated values where the product is on the verge of suffering physical damage, therefore the product must be used within conditions that ensure the absolute maximum ratings are not exceeded.**

Remark 1. Unless specified otherwise, the characteristics of alternate-function pins are the same as those of the port pins.

Remark 2. AVREF (+): + side reference voltage of the A/D converter.

Remark 3. GND (GND0, GND1 and VSS): Reference voltage.

4.2 Power supply voltage condition

Parameter	Symbol	Conditions	MIN.	TYP.	MAX.	Unit
Power supply	VCC, VBAT		4.0	-	50.0	V
	VDD		2.7	-	5.5	V
	GND	GND0, GND1, VSS	-	0.0	-	V

<R> 4.3 Supply current characteristics

($T_A = -40/-20$ to $+85^\circ\text{C}$, $4.0\text{V} \leq \text{VCC} \leq 50\text{V}$, $\text{VDD} = \text{CREG2}$, $\text{GND0} = \text{GND1} = 0\text{V}$)

Parameter	Symbol	Conditions	MIN.	TYP.	MAX.	Unit
Power down mode current 1	IPD	VCC=35V			2.0	uA
Power down mode current 2 (Low voltage)	IPDL	VCC=4.0V			1.0	uA
Sleep mode current 1	ISLP1	-20C $\leq T_A \leq 85^\circ\text{C}$, REG2T6 bit = 0, MCU operation mode: STOP mode ALOCO = ON, AOCO = OFF CD = ALL ON, AFE Timer = ON, AFE WDT = ON, CFOUT = L, DFOUT = L, AD(AFE) = OFF, CC = OFF		25.0	50.0	uA
	ISLP1L	-40C $\leq T_A \leq 85^\circ\text{C}$, REG2T6 bit = 1, MCU operation mode: STOP mode ALOCO = ON, AOCO = OFF CD = ALL ON, AFE Timer = ON, AFE WDT = ON, CFOUT = L, DFOUT = L, AD(AFE) = OFF, CC = OFF		35	70.0	uA
Sleep mode current 2	ISLP2	-20C $\leq T_A \leq 85^\circ\text{C}$, REG2T6 bit = 0, MCU operation mode: STOP mode ALOCO = ON, AOCO = OFF CD = ALL ON, AFE timer = ON, AFE WDT = ON, CFOUT = H, DFOUT = H, AD(AFE) = OFF, CC = OFF		50.0	100.0	uA
	ISLP2L	-40C $\leq T_A \leq 85^\circ\text{C}$, REG2T6 bit = 1, MCU operation mode: STOP mode ALOCO = ON, AOCO = OFF CD = ALL ON, AFE timer = ON, AFE WDT = ON, CFOUT = H, DFOUT = H, AD(AFE) = OFF, CC = OFF		60	120.0	uA
Normal mode current	INOM	MCU operation mode: LS (Low-Speed main) mode, fHOCO=8MHz ALOCO = ON, AOCO = ON CD = ALL ON, AFE Timer = ON, AFE WDT = ON, CFOUT = H, DFOUT = H, AD(AFE) = ON, CC = ON		2.0	3.0	mA

Note. "Sleep mode current 1" is the current consumption when PCON register value is set to "63H".

"Sleep mode current 2" is the current consumption when PCON register value is set to "43H".

For details, see 17.18 Power Control function in RAJ240090 / RAJ240100 User's Manual.

Caution After trimming.

4.4 Oscillator Characteristics

4.4.1 XT1 Characteristics

($T_A = -40/-20$ to $+85C$, $2.7V \leq VDD \leq 5.5V$, $GND0 = GND1 = VSS = 0V$)

Parameter	Resonator	Conditions	MIN.	TYP.	MAX.	Unit
XT1 clock oscillation frequency (f_{XT}) ^{Note}	Crystal resonator		32	32.768	35	kHz

Note Indicates only permissible oscillator frequency ranges. Refer to AC Characteristics for instruction execution time. Request evaluation by the manufacturer of the oscillator circuit mounted on a board to check the oscillator characteristics.

4.4.2 MCU On-chip oscillator characteristics

($T_A = -40/-20$ to $+85C$, $2.7V \leq VDD \leq 5.5V$, $GND0 = GND1 = VSS = 0V$)

Parameter	Symbol	Conditions	MIN.	TYP.	MAX.	Unit
High-speed on-chip oscillator clock frequency ^{Note 1, 2}	f_{IH}		1		32	MHz
High-speed on-chip oscillator clock frequency accuracy		-20C $\leq T_A \leq 85C$	-1.0		+1.0	%
		-40C $\leq T_A \leq 85C$	-1.5		+1.5	%
Low-speed on-chip oscillator clock frequency	f_{IL}			15		kHz
Low-speed on-chip oscillator clock frequency accuracy			-15		+15	%

Note 1. High-speed on-chip oscillator frequency is selected with bits 0 to 4 of the option byte (000C2H) and bits 0 to 2 of the HOCODIV register.

Note 2. This only indicates the oscillator characteristics. Refer to AC Characteristics for instruction execution time.

4.4.3 AFE On-chip oscillator characteristics

($T_A = -40/-20$ to $+85C$, $4.0V \leq VCC \leq 50V$, $GND0 = GND1 = VSS = 0V$)

Parameter	Symbol	Conditions	MIN.	TYP.	MAX.	Unit
AFE on-chip oscillator clock frequency	f_{AOCO}		-	4.194	-	MHz
AFE on-chip oscillator clock frequency accuracy			-2	-	+2	%
AFE on-chip oscillator clock frequency stabilization wait time			-	-	(50)	us
AFE Low-speed on-chip oscillator clock frequency	f_{ALOCO}		-	131.072	-	KHz
AFE Low-speed on-chip oscillator clock frequency accuracy			-5	-	+5	%
AFE Low-speed on-chip oscillator clock frequency stabilization wait time			-	-	(50)	us

Caution After trimming.

Remark Values in brackets are design value.

4.5 Pin characteristics

(1/5)

($T_A = -40/-20$ to $+85^\circ\text{C}$, $4.0\text{V} \leq \text{VCC} \leq 50\text{V}$, $2.7\text{V} \leq \text{VDD} \leq 5.5\text{V}$, $\text{GND0} = \text{GND1} = \text{VSS} = 0\text{V}$)

Parameter	Symbol	Conditions		MIN.	TYP.	MAX.	Unit
Output current, high Note 1	I _{OH1}	Per pin for P00 to P07, P10 to P16, P40	$2.7\text{V} \leq \text{VDD} \leq 5.5\text{V}$			-10.0 Note 2	mA
		Total of P00 to P07, P10 to P16, P40 (When duty $\leq 70\%$ Note 3)	$4.0\text{V} \leq \text{VDD} \leq 5.5\text{V}$ $2.7\text{V} \leq \text{VDD} < 4.0\text{V}$			-55.0	mA
		Total of all pins (When duty $\leq 70\%$ Note 3)	$2.7\text{V} \leq \text{VDD} \leq 5.5\text{V}$			-10.0	mA
	I _{OH2}	Per pin for P20 to P23	$2.7\text{V} \leq \text{VDD} \leq 5.5\text{V}$			-0.1 Note 2	mA
		Total of all pins (When duty $\leq 70\%$ Note 3)	$2.7\text{V} \leq \text{VDD} \leq 5.5\text{V}$			-1.5	mA

Note 1. Value of current at which the device operation is guaranteed even if the current flows from the VDD pins to an output pin.

Note 2. Do not exceed the total current value.

Note 3. Specification under conditions where duty factor $\leq 70\%$.

The output current value that has changed to the duty factor $> 70\%$ the duty ratio can be calculated with the following expression (when changing the duty factor from 70% to n%).

- Total output current from pins = $(I_{OH} \times 0.7)/(n \times 0.01)$

<Example> Where n = 80% and I_{OH} = -10.0 mA

$$\text{Total output current from pins} = (-10.0 \times 0.7)/(80 \times 0.01) \approx -8.7 \text{ mA}$$

However, the allowable current flow into one pin does not change with the duty factor.

A current higher than the absolute maximum rating must not flow into any one pin.

Caution P03, P04, and P10 to P16 do not output high level in N-ch open-drain mode.

Remark Unless specified otherwise, the characteristics of alternate-function pins are the same as those of the port pins.

$(T_A = -40/-20 \text{ to } +85C, 4.0V \leq VCC \leq 50V, 2.7V \leq VDD \leq 5.5V, GND0 = GND1 = VSS = 0V)$

Parameter	Symbol	Conditions		MIN.	TYP.	MAX.	Unit
Output current, low ^{Note 1}	I _{OL1}	Per pin for P00 to P07, P10 to P16, P40				20.0 ^{Note 2}	mA
		Per pin for P60-P63				15.0 ^{Note 2}	mA
		Total of P00 to P07, P10 to P16, P40 (When duty \leq 70% ^{Note 3})	4.0V \leq VDD \leq 5.5V			70.0	mA
	I _{OL2}	Total of all pins (When duty \leq 70% ^{Note 3})	2.7V \leq VDD $<$ 4.0V			15.0	mA
						150.0	mA
		Per pin for P20 to P23				0.4 ^{Note 2}	mA
		Total of all pins (When duty \leq 70% ^{Note 3})	2.7V \leq VDD \leq 5.5V			5.0	mA

Note 1. Value of current at which the device operation is guaranteed even if the current flows from an output pin to the VSS pins.

Note 2. Do not exceed the total current value.

Note 3. Specification under conditions where the duty factor \leq 70%.

The output current value that has changed to the duty factor $>$ 70% the duty ratio can be calculated with the following expression (when changing the duty factor from 70% to n%).

- Total output current of pins = $(I_{OL} \times 0.7)/(n \times 0.01)$

<Example> Where n = 80% and I_{OL} = 10.0 mA

$$\text{Total output current of pins} = (10.0 \times 0.7)/(80 \times 0.01) \approx 8.7 \text{ mA}$$

However, the allowable current flow into one pin does not change with the duty factor.

A current higher than the absolute maximum rating must not flow into any one pin.

Remark Unless specified otherwise, the characteristics of alternate-function pins are the same as those of the port pins.

(3/5)

 $(T_A = -40/-20 \text{ to } +85C, 4.0V \leq VCC \leq 50V, 2.7V \leq VDD \leq 5.5V, GND0 = GND1 = VSS = 0V)$

Parameter	Symbol	Conditions		MIN.	TYP.	MAX.	Unit
Input voltage, high	VIH1	P00 to P02, P05 to P07, P10 to P16, P40	Normal input buffer	0.8 VDD		VDD	V
	VIH2	P03, P04, P10, P11, P13, P14	TTL input buffer 4.0V \leq VDD \leq 5.5V	2.2		VDD	V
			TTL input buffer 3.3V \leq VDD $<$ 4.0V	2.0		VDD	V
			TTL input buffer 2.7V \leq VDD $<$ 3.3V	1.5		VDD	V
	VIH3	P20 to P23		0.7 VDD		VDD	V
	VIH4	P60 to P63		0.7 VDD		6.0	V
	VIH5	P122 to P124, P137, RESET		0.8 VDD		VDD	V
Input voltage, low	UIL1	P00 to P02, P05 to P07, P10 to P16, P40	Normal input buffer	0		0.2 VDD	V
	UIL2	P03, P04, P10, P11, P13, P14	TTL input buffer 4.0V \leq VDD \leq 5.5V	0		0.8	V
			TTL input buffer 3.3V \leq VDD $<$ 4.0V	0		0.5	V
			TTL input buffer 2.7V \leq VDD $<$ 3.3V	0		0.32	V
	UIL3	P20 to P23		0		0.3 VDD	V
	UIL4	P60 to P63		0		0.3 VDD	V
	UIL5	P122 to P124, P137, RESET		0		0.2 VDD	V
	UIL6	P03, P04	3.0V \leq VDD \leq 5.5V	0		0.5 VDD	V
			2.7V \leq VDD $<$ 3.0V	0		0.4 VDD	V

Caution The maximum value of VIH of pins P03, P04, P10 to P16 is VDD, even in the N-ch open-drain mode.**Remark** Unless specified otherwise, the characteristics of alternate-function pins are the same as those of the port pins.

(4/5)

 $(T_A = -40/-20 \text{ to } +85C, 4.0V \leq VCC \leq 50V, 2.7V \leq VDD \leq 5.5V, GND0 = GND1 = VSS = 0V)$

Parameter	Symbol	Conditions		MIN.	TYP.	MAX.	Unit
Output voltage, high	V _{OH1}	P00 to P07, P10 to P16, P40	4.0V \leq VDD \leq 5.5V, IOH1 = -10.0mA	VDD - 1.5			V
			4.0V \leq VDD \leq 5.5V, IOH1 = -3.0mA	VDD - 0.7			V
			2.7V \leq VDD \leq 5.5V, IOH1 = -1.5mA	VDD - 0.5			V
	V _{OH2}	P20 to P23	2.7V \leq VDD \leq 5.5V, IOH2 = -100uA	VDD - 0.5			V
	V _{OL1}	P00 to P07, P10 to P16, P40	4.0V \leq VDD \leq 5.5V, IOL1 = 20.0mA		1.3		V
			4.0V \leq VDD \leq 5.5V, IOL1 = 8.5mA		0.7		V
			2.7V \leq VDD \leq 5.5V, IOL1 = 3.0mA		0.6		V
			2.7V \leq VDD \leq 5.5V, IOL1 = 1.5mA		0.4		V
			2.7V \leq VDD \leq 5.5V, IOL1 = 0.6mA		0.4		V
			2.7V \leq VDD \leq 5.5V, IOL1 = 0.3mA		0.4		V
	V _{OL2}	P20 to P23	1.6V \leq VDD \leq 5.5V, IOL2 = 400uA		0.4		V
	V _{OL3}	P60 to P63	4.0V \leq VDD \leq 5.5V, IOL3 = 15.0mA		2.0		V
			4.0V \leq VDD \leq 5.5V, IOL3 = 5.0mA		0.4		V
			2.7V \leq VDD \leq 5.5V, IOL3 = 3.0mA		0.4		V
			1.8V \leq VDD \leq 5.5V, IOL3 = 2.0mA		0.4		V
			1.6V \leq VDD \leq 5.5V, IOL3 = 1.0mA		0.4		V

Caution P03, P04, P10 to P16 do not output high level in N-ch open-drain mode.**Remark** Unless specified otherwise, the characteristics of alternate-function pins are the same as those of the port pins.

($T_A = -40/-20$ to $+85^\circ\text{C}$, $4.0\text{V} \leq V_{CC} \leq 50\text{V}$, $2.7\text{V} \leq V_{DD} \leq 5.5\text{V}$, $GND0 = GND1 = VSS = 0\text{V}$)

Parameter	Symbol	Conditions		MIN.	TYP.	MAX.	Unit	
Input leakage current, high	I _{LH1}	P00 to P07, P10 to P16, P40		VI = VDD		1	uA	
	I _{LH2}	P20 to P23, P137, RESET		VI = VDD		1	uA	
	I _{LH3}	P122 to P124	VI = VDD	In input port or external clock input		1	uA	
Input leakage current, low	I _{LIL1}	P00 to P07, P10 to P16, P40		VI = VSS		-1	uA	
	I _{LIL2}	P20 to P23, P137, RESET		VI = VSS		-1	uA	
	I _{LIL3}	P122 to P124		VI = VSS	In input port or external clock input	-1	uA	
On-chip pull-up resistance	R _U	P00 to P07, P10 to P16, P40		VI = VSS, In input port		10	kΩ	
	R _{UA}	AN0, AN1, AN2				7.5	kΩ	
	R _{UAR}	RESETOUT				20	kΩ	

Remark 1. Unless specified, the characteristics of alternate-function pins are the same as those of the port pins.

Remark 2. Regarding pin characteristics of CFOUT, DFOUT, refer to Section 4.8.6 Charge/discharge FET control circuit characteristics.

Remark 3. Regarding pin characteristics of VIN1 to VIN10 refer to Section 4.8.2 Multiplexer.

Remark 4. Regarding pin characteristics of HVP0 to HVP2 refer to Section 4.8.1 High-voltage port characteristics.

4.6 AC Characteristics

(1/2)

($T_A = -40/-20$ to $+85^\circ\text{C}$, $2.7V \leq VDD \leq 5.5V$, $\text{GND}0 = \text{GND}1 = \text{VSS} = 0V$)

Parameter	Symbol	Conditions		MIN.	TYP.	MAX.	Unit
Instruction cycle (minimum instruction execution time)	TCY	Main system clock (fMAIN) operation	HS (high-speed main) mode	0.03125		1	us
			LS (low-speed main) mode	0.125		1	us
			LV (low-voltage main) mode	0.25		1	us
		Subsystem clock (fsUB) operation		28.5	30.5	31.3	us
		In the self-programming mode	HS (high-speed main) mode	0.03125		1	us
			LS (low-speed main) mode	0.125		1	us
			LV (low-voltage main) mode	0.25		1	us
External system clock frequency	fEXS			32		35	kHz
External system clock input high-level width, low-level width	tEXHS, tEXLS			13.7			us
TI00 to TI02 input high-level width, low-level width	tTIH, tTIL			1/fMCK +10			ns

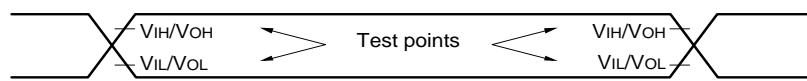
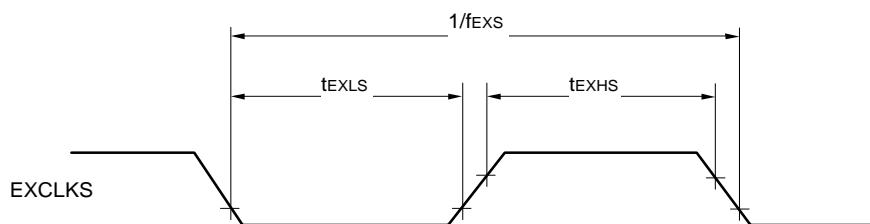
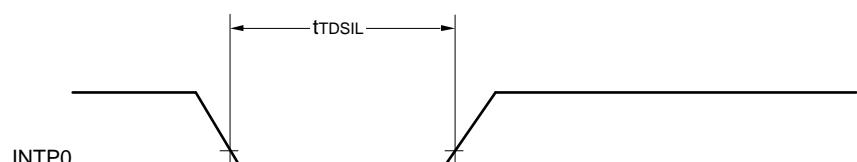
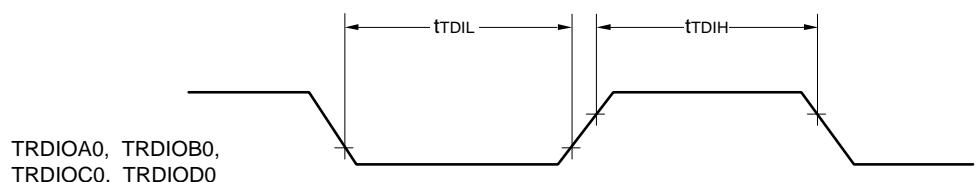
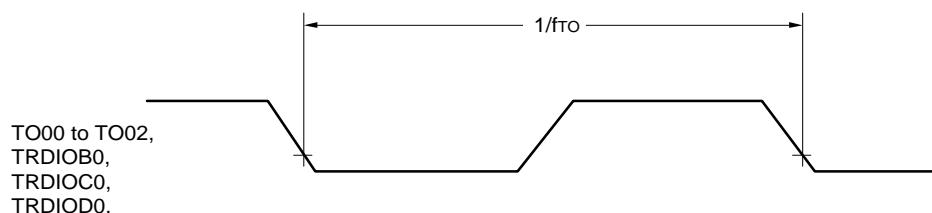
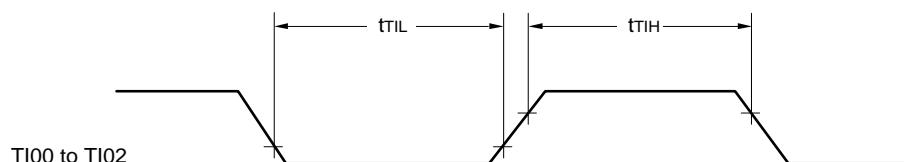
Remark fmck : Timer array unit operation clock frequency

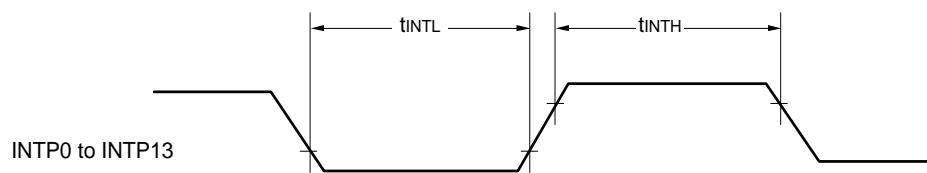
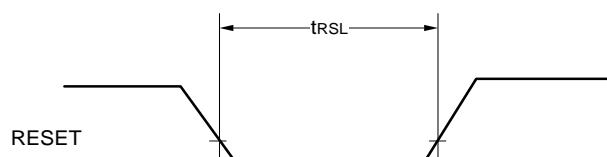
(Operation clock to be set by the CKSmn bit of timer mode register mn (TMRmn). m: Unit number (m = 0, 1), n: Channel number (n = 0 to 3))

(2/2)

 $(T_A = -40/-20 \text{ to } +85C, 2.7V \leq VDD \leq 5.5V, GND0 = GND1 = VSS = 0V)$

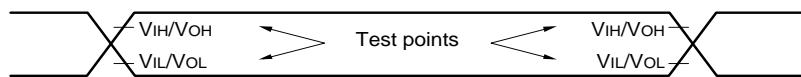
Parameter	Symbol	Conditions		MIN.	TYP.	MAX.	Unit
Timer RD input high-level width, low-level width	tTDIH, tTDIL	TRDIOB0, TRDIOC0, TRDIOD0		3/fCLK			ns
Timer RD forced cutoff signal input low-level width	tTDSIL	P16/INTP0	2MHz < fCLK ≤ 32MHz	1			us
			fCLK ≤ 2 MHz	1/fCLK + 1			
TO00 to TO02, TRDIOB0, TRDIOC0, TRDIOD0 output frequency	fTO	HS (high-speed main) mode	4.0V ≤ VDD ≤ 5.5V			16	MHz
			2.7V ≤ VDD < 4.0V			8	MHz
		LS (low-speed main) mode	2.7V ≤ VDD ≤ 5.5V			4	MHz
		LV(low-voltage main) mode	2.7V ≤ VDD ≤ 5.5V			2	MHz
Interrupt input high-level width, low-level width	tINTH, tINTL	INTP0 to INTP13	1.6V ≤ VDD ≤ 5.5V	1			us
RESET low-level width	tRSL			10			us

AC Timing Test Points**External System Clock Timing****TI/TO Timing**

Interrupt Request Input Timing**RESET Input Timing**

4.7 MCU peripheral circuit characteristics

AC Timing Test Points



4.7.1 Serial array unit

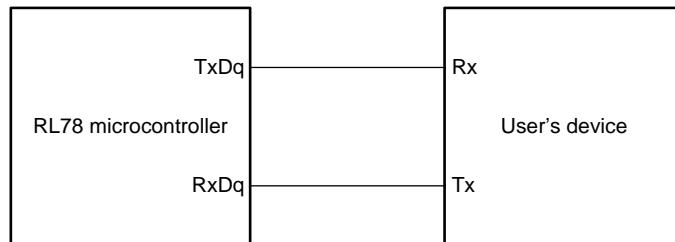
(1) During communication at same potential (UART mode)

($T_A = -40/-20$ to $+85^\circ\text{C}$, $2.7\text{V} \leq V_{DD} \leq 5.5\text{V}$, $GND0 = GND1 = VSS = 0\text{V}$)

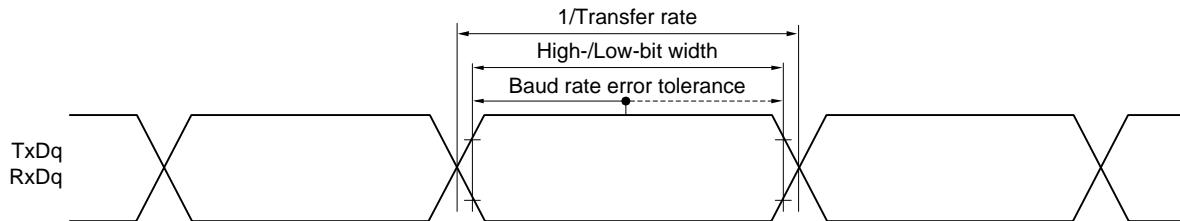
Parameter	Symbol	Conditions	HS (high-speed main) mode		LS (low-speed main) mode		LV (low-voltage main) mode		Unit
			MIN.	MAX.	MIN.	MAX.	MIN.	MAX.	
Transfer rate Note		Theoretical value of the maximum transfer rate $f_{MCK} = f_{CLK}$		$f_{MCK}/6$		$f_{MCK}/6$		$f_{MCK}/6$	bps
				5.3		1.3		0.6	Mbps

Note Transfer rate in the SNOOZE mode is only 4800 bps.

Caution Select the normal input buffer for the RxDq pin and the normal output mode for the TxDq pin by using port input mode register g (PIMg) and port output mode register g (POMg).



UART mode connection diagram (during communication at same potential)



UART mode bit width (during communication at same potential) (reference)

Remark 1. q: UART number ($q = 0$ to 3), g: PIM and POM number ($g = 0, 1, 5, 14$)

Remark 2. f_{MCK} : Serial array unit operation clock frequency

(Operation clock to be set by the CKSmn bit of serial mode register mn (SMRmn). m: Unit number, n: Channel number (mn = 00 to 03, 10 to 13))

(2) During communication at same potential (CSI mode) (master mode, SCKp... internal clock output)

($T_A = -40/-20$ to $+85^\circ\text{C}$, $2.7\text{V} \leq \text{VDD} \leq 5.5\text{V}$, $\text{GND}0 = \text{GND}1 = \text{VSS} = 0\text{V}$)

Parameter	Symbol	Conditions	HS (high-speed main) mode		LS (low-speed main) mode		LV (low-voltage main) mode		Unit
			MIN.	MAX.	MIN.	MAX.	MIN.	MAX.	
SCKp cycle time	tkCY1	tkCY1 $\geq 4/\text{fCLK}$	125		500		1000		ns
SCKp high-/low-level width	tkH1, tkL1	4.0V $\leq \text{VDD} \leq 5.5\text{V}$	tkCY1/2 - 12		tkCY1/2 - 50		tkCY1/2 - 50		ns
		2.7V $\leq \text{VDD} \leq 5.5\text{V}$	tkCY1/2 - 18		tkCY1/2 - 50		tkCY1/2 - 50		ns
Slp setup time (to SCKp \uparrow) ^{Note 1}	tsIK1	4.0V $\leq \text{VDD} \leq 5.5\text{V}$	44		110		110		ns
		2.7V $\leq \text{VDD} \leq 5.5\text{V}$	44		110		110		ns
Slp hold time (from SCKp \downarrow) ^{Note 2}	tksI1		19		19		19		ns
Delay time from SCKp \downarrow to SOp output ^{Note 3}	tkso1	C = 30 pF ^{Note 4}		25		25		25	ns

Note 1. When DAPmn = 0 and CKPmn = 0, or DAPmn = 1 and CKPmn = 1.

The Slp setup time becomes "to SCKp \downarrow " when DAPmn = 0 and CKPmn = 1, or DAPmn = 1 and CKPmn = 0.

Note 2. When DAPmn = 0 and CKPmn = 0, or DAPmn = 1 and CKPmn = 1.

The Slp hold time becomes "from SCKp \downarrow " when DAPmn = 0 and CKPmn = 1, or DAPmn = 1 and CKPmn = 0.

Note 3. When DAPmn = 0 and CKPmn = 0, or DAPmn = 1 and CKPmn = 1.

The delay time to SOp output becomes "from SCKp \uparrow " when DAPmn = 0 and CKPmn = 1, or DAPmn = 1 and CKPmn = 0.

Note 4. C is the load capacitance of the SCKp and SOp output lines.

Caution Select the normal input buffer for the Slp pin and the normal output mode for the SOp pin and SCKp pin by using port input mode register g (PIMg) and port output mode register g (POMg).

Remark 1. p: CSI number (p = 00, 10), m: Unit number (m = 0, 1), n: Channel number (n = 0 to 3),

g: PIM number (g = 0, 1, 3 to 5, 14)

Remark 2. fmck: Serial array unit operation clock frequency (Operation clock to be set by the CKSmn bit of serial mode register mn (SMRmn)).

m: Unit number, n: Channel number (mn = 00, 02))

(3) During communication at same potential (CSI mode) (slave mode, SCKp... external clock input)

($T_A = -40/-20$ to $+85^\circ\text{C}$, $2.7V \leq VDD \leq 5.5V$, $\text{GND}0 = \text{GND}1 = \text{VSS} = 0V$)

Parameter	Symbol	Conditions		HS (high-speed main) mode		LS (low-speed main) mode		LV (low-voltage main) mode		Unit
				MIN.	MAX.	MIN.	MAX.	MIN.	MAX.	
SCKp cycle time Note 5	tkCY2	4.0V \leq VDD \leq 5.5V	20MHz < fmck	8/fmck	—	—	—	—	—	ns
			fmck \leq 20MHz	6/fmck	—	6/fmck	—	6/fmck	—	ns
		2.7V \leq VDD \leq 5.5V	1 MHz < fmck	8/fmck	—	—	—	—	—	ns
			fmck \leq 16MHz	6/fmck	—	6/fmck	—	6/fmck	—	ns
SCKp high-/low-level width	tKH2, tKL2	4.0V \leq VDD \leq 5.5V		tkCY2/2 - 7	—	tkCY2/2 - 7	—	tkCY2/2 - 7	—	ns
		2.7V \leq VDD \leq 5.5V		tkCY2/2 - 8	—	tkCY2/2 - 8	—	tkCY2/2 - 8	—	ns
Slp setup time (to SCKp↑) Note 1	tsIK2			1/fmck + 20	—	1/fmck + 30	—	1/fmck + 30	—	ns
Slp hold time (from SCKp↑) Note 2	tksi2			1/fmck + 31	—	1/fmck + 31	—	1/fmck + 31	—	ns
Delay time from SCKp↓ to SOp output Note 3	tkso2	C = 30pF Note 4		—	2/fmck + 44	—	2/fmck + 110	—	2/fmck + 110	ns

Note 1. When DAPmn = 0 and CKPmn = 0, or DAPmn = 1 and CKPmn = 1.

The Slp setup time becomes "to SCKp↓" when DAPmn = 0 and CKPmn = 1, or DAPmn = 1 and CKPmn = 0.

Note 2. When DAPmn = 0 and CKPmn = 0, or DAPmn = 1 and CKPmn = 1.

The Slp hold time becomes "from SCKp↓" when DAPmn = 0 and CKPmn = 1, or DAPmn = 1 and CKPmn = 0.

Note 3. When DAPmn = 0 and CKPmn = 0, or DAPmn = 1 and CKPmn = 1.

The delay time to SOp output becomes "from SCKp↑" when DAPmn = 0 and CKPmn = 1, or DAPmn = 1 and CKPmn = 0.

Note 4. C is the load capacitance of the SCKp and SOp output lines.

Note 5. The maximum transfer rate when using the SNOOZE mode is 1 Mbps.

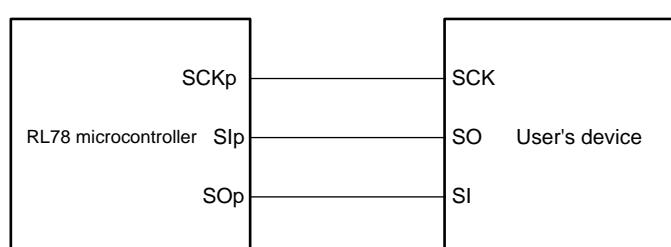
Caution Select the normal input buffer for the Slp pin and the normal output mode for the SOp pin and SCKp pin by using port input mode register g (PIMg) and port output mode register g (POMg).

Remark 1. p: CSI number (p = 00, 10), m: Unit number (m = 0, 1), n: Channel number (n = 0 to 3),

g: PIM number (g = 0, 1, 3 to 5, 14)

Remark 2. fmck: Serial array unit operation clock frequency (Operation clock to be set by the CKSmn bit of serial mode register mn (SMRmn)).

m: Unit number, n: Channel number (mn = 00, 02)

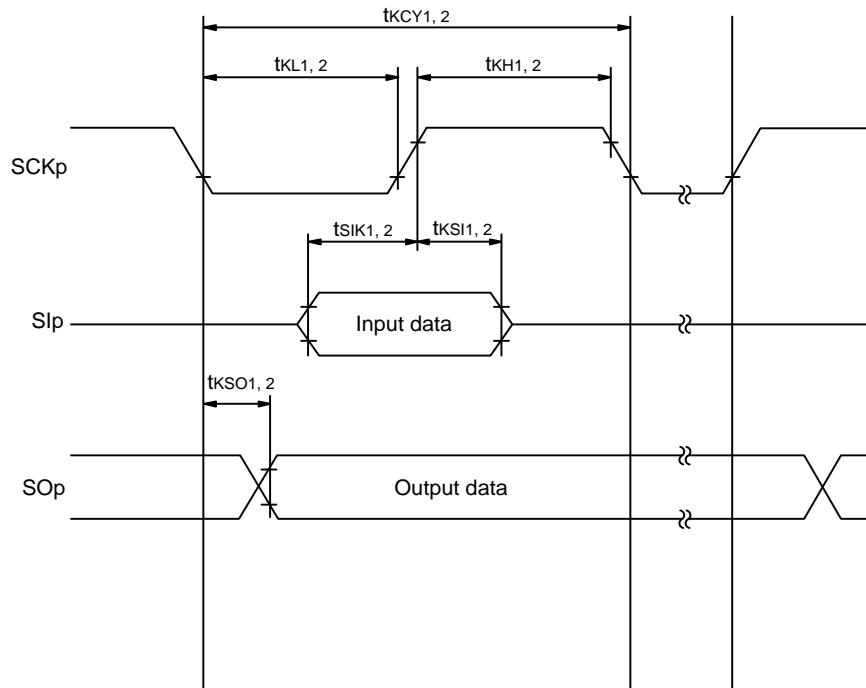


CSI mode connection diagram (during communication at same potential)

Remark 1. p: CSI number (p = 00, 10)

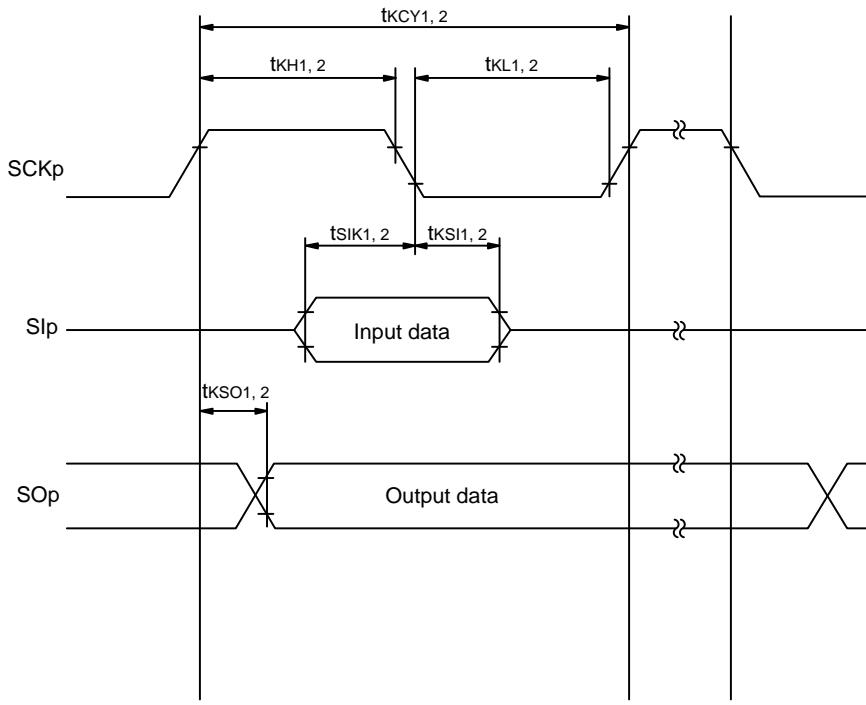
Remark 2. m: Unit number, n: Channel number (mn = 00, 02)

(When DAPmn = 0 and CKPmn = 0, or DAPmn = 1 and CKPmn = 1.)



CSI mode serial transfer timing (during communication at same potential)

(When DAPmn = 0 and CKPmn = 1, or DAPmn = 1 and CKPmn = 0.)



CSI mode serial transfer timing (during communication at same potential)

Remark 1. p: CSI number ($p = 00, 10$)

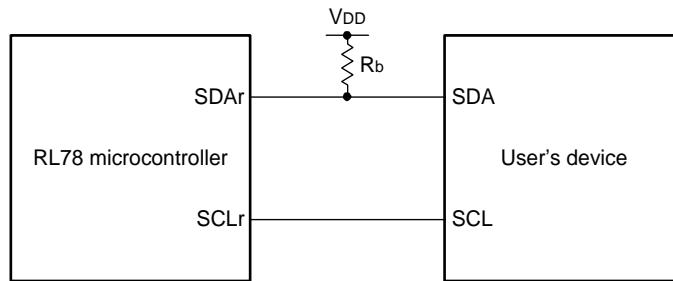
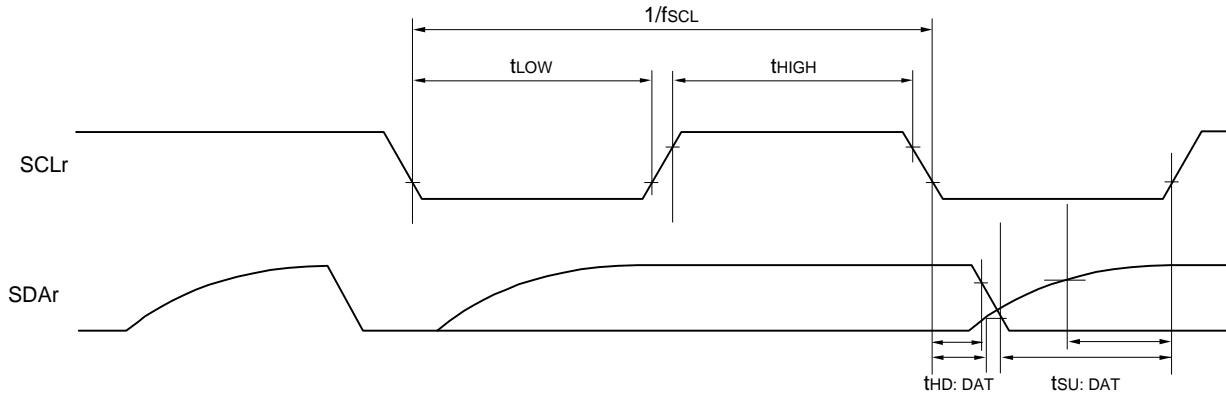
Remark 2. m: Unit number, n: Channel number ($mn = 00, 02$)

(4) During communication at same potential (simplified I²C mode)(T_A = -40/-20 to +85C, 2.7V ≤ VDD ≤ 5.5V, GND0 = GND1 = VSS = 0V)

Parameter	Symbol	Conditions	HS (high-speed main) mode		LS (low-speed main) mode		LV (low-voltage main) mode		Unit
			MIN.	MAX.	MIN.	MAX.	MIN.	MAX.	
SCL _r clock frequency	f _{SCL}	2.7V ≤ VDD ≤ 5.5V, C _b = 50pF, R _b = 2.7kΩ		1000 ^{Note 1}		400 ^{Note 1}		400 ^{Note 1}	kHz
Hold time when SCL _r = "L"	t _{LOW}	2.7V ≤ VDD ≤ 5.5V, C _b = 50pF, R _b = 2.7kΩ	475		1150		1150		ns
Hold time when SCL _r = "H"	t _{HIGH}	2.7V ≤ VDD ≤ 5.5V, C _b = 50pF, R _b = 2.7kΩ	475		1150		1150		ns
Data setup time (reception)	t _{SU: DAT}	2.7V ≤ VDD ≤ 5.5V, C _b = 50pF, R _b = 2.7kΩ	1/f _{MCK} + 85 ^{Note 2}		1/f _{MCK} + 145 ^{Note 2}		1/f _{MCK} + 145 ^{Note 2}		ns
Data hold time (transmission)	t _{HD: DAT}	2.7V ≤ VDD ≤ 5.5V, C _b = 50pF, R _b = 2.7kΩ	0	305	0	305	0	305	ns

Note 1. The value must also be equal to or less than f_{MCK}/4.**Note 2.** Set the f_{MCK} value not to over the hold time of SCL_r = "L" and SCL_r = "H".

Caution Select the normal input buffer and the N-ch open drain output (VDD tolerance) mode for the SDAr pin and the normal output mode for the SCL_r pin by using port input mode register g (PIMg) and port output mode register h (POMh).

**Simplified I²C mode connection diagram (during communication at same potential)****Simplified I²C mode serial transfer timing (during communication at same potential)****Remark 1.** R_b[Ω]: Communication line (SDAr) pull-up resistance, C_b[F]: Communication line (SDAr, SCL_r) load capacitance**Remark 2.** r: IIC number (r = 00, 10), g: PIM number (g = 10, 13), h: POM number (h = 11, 14)**Remark 3.** f_{MCK}: Serial array unit operation clock frequency (Operation clock to be set by the CKSmn bit of serial mode register mn (SMRmn)).

m: Unit number (m = 0, 1), n: Channel number (n = 0 to 3), mn = 00 to 03, 10 to 13

4.7.2 Serial interface IICA

(1) I²C standard mode

(T_A = -40/-20 to +85C, 2.7V ≤ VDD ≤ 5.5V, GND0 = GND1 = VSS = 0V)

Parameter	Symbol	Conditions	HS (high-speed main) mode		LS (low-speed main) mode		LV (low-voltage main) mode		Unit
			MIN.	MAX.	MIN.	MAX.	MIN.	MAX.	
SCLA0 clock frequency	fsCL	Standard mode: fCLK ≥ 1MHz	0	100	0	100	0	100	kHz
Setup time of restart condition	tsU: STA		4.7		4.7		4.7		us
Hold time ^{Note 1}	tHD: STA		4.0		4.0		4.0		us
Hold time when SCLA0 = "L"	tLOW		4.7		4.7		4.7		us
Hold time when SCLA0 = "H"	tHIGH		4.0		4.0		4.0		us
Data setup time (reception)	tsU: DAT		250		250		250		ns
Data hold time (transmission)	tHD: DAT		0	3.45	0	3.45	0	3.45	us
Setup time of stop condition	tsU: STO		4.0		4.0		4.0		us
Bus-free time	tBUF		4.7		4.7		4.7		us

Note 1. The first clock pulse is generated after this period when the start/restart condition is detected.

Note 2. The maximum value (MAX.) of tHD: DAT is during normal transfer and a wait state is inserted in the ACK (acknowledge) timing.

Remark The maximum value of C_b (communication line capacitance) and the value of R_b (communication line pull-up resistor) at that time in each mode are as follows.

Standard mode: C_b = 400pF, R_b = 2.7kΩ

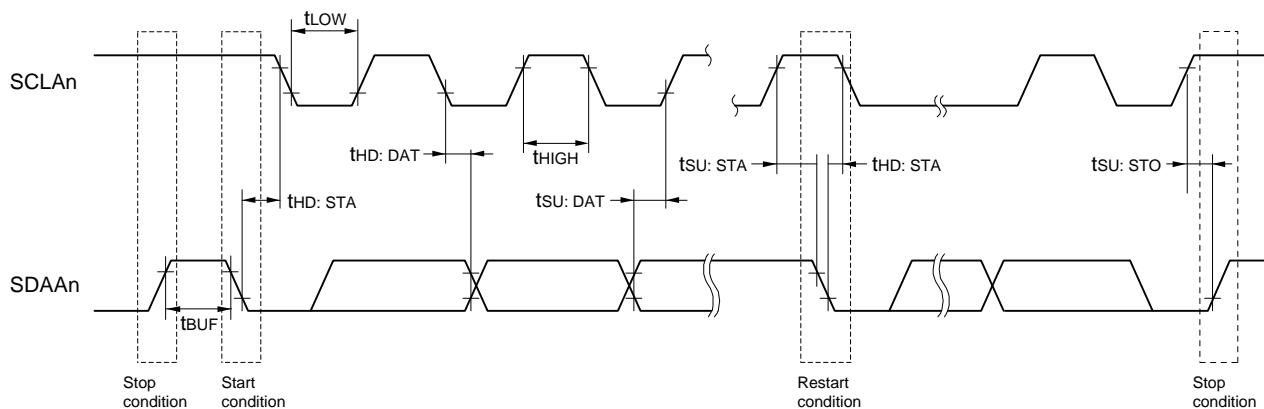
(2) I²C fast mode(T_A = -40/-20 to +85C, 2.7V ≤ VDD ≤ 5.5V, GND0 = GND1 = VSS = 0V)

Parameter	Symbol	Conditions	HS (high-speed main) mode		LS (low-speed main) mode		LV (low-voltage main) mode		Unit
			MIN.	MAX.	MIN.	MAX.	MIN.	MAX.	
SCLA0 clock frequency	fsCL	Fast mode: fCLK ≥ 3.5 MHz	0	400	0	400	0	400	kHz
Setup time of restart condition	tsU: STA		0.6		0.6		0.6		us
Hold time ^{Note1}	tHD: STA		0.6		0.6		0.6		us
Hold time when SCLA0 = "L"	tLOW		1.3		1.3		1.3		us
Hold time when SCLA0 = "H"	tHIGH		0.6		0.6		0.6		us
Data setup time (reception)	tsU: DAT		100		100		100		ns
Data hold time (transmission)	tHD: DAT		0	0.9	0	0.9	0	0.9	us
Setup time of stop condition	tsU: STO		0.6		0.6		0.6		us
Bus-free time	tBUF		1.3		1.3		1.3		us

Note 1. The first clock pulse is generated after this period when the start/restart condition is detected.**Note 2.** The maximum value (MAX.) of tHD: DAT is during normal transfer and a wait state is inserted in the ACK (acknowledge) timing.**Remark** The maximum value of C_b (communication line capacitance) and the value of R_b (communication line pull-up resistor) at that time in each mode are as follows.Fast mode: C_b = 320pF, R_b = 1.1kΩ

(3) I²C fast mode plus(T_A = -40/-20 to +85C, 2.7V ≤ VDD ≤ 5.5V, GND0 = GND1 = VSS = 0V)

Parameter	Symbol	Conditions	HS (high-speed main) mode		LS (low-speed main) mode		LV (low-voltage main) mode		Unit
			MIN.	MAX.	MIN.	MAX.	MIN.	MAX.	
SCLA0 clock frequency	fsCL	Fast mode plus: fCLK ≥ 10 MHz	0	1000					kHz
Setup time of restart condition	tsU: STA		0.26						us
Hold time ^{Note 1}	tHD: STA		0.26						us
Hold time when SCLA0 = "L"	tLOW		0.5						us
Hold time when SCLA0 = "H"	tHIGH		0.26						us
Data setup time (reception)	tsU: DAT		50						ns
Data hold time (transmission)	tHD: DAT	^{Note 2}	0	0.45					us
Setup time of stop condition	tsU: STO		0.26						us
Bus-free time	tBUF		0.5						us

Note 1. The first clock pulse is generated after this period when the start/restart condition is detected**Note 2.** The maximum value (MAX.) of tHD: DAT is during normal transfer and a wait state is inserted in the ACK (acknowledge) timing.**Remark** The maximum value of C_b (communication line capacitance) and the value of R_b (communication line pull-up resistor) at that time in each mode are as follows.Fast mode plus: C_b = 120pF, R_b = 1.1kΩ**IIC serial transfer timing****Remark** n = 0

4.7.3 CAN interface

($T_A = -40/-20$ to $+85^\circ\text{C}$, $2.7\text{V} \leq \text{VDD} \leq 5.5\text{V}$, $\text{GND0} = \text{GND1} = \text{VSS} = 0\text{V}$)

Parameter	Symbol	Conditions	HS (high-speed main) mode		Unit
			MIN.	MAX.	
Transfer rate		Theoretical value of the maximum transfer rate $f_{\text{CAN}} = f_{\text{CLK}}/2$		1	Mbps

4.7.4 A/D converter characteristics

(1) When reference voltage (+) = AVREFP/ANI0 (ADREFP1 = 0, ADREFP0 = 1), reference voltage (-) = AVREFM/ANI1 (ADREFM = 1), target pin: ANI02, ANI03, internal reference voltage, and temperature sensor output voltage

($T_A = -40\text{--}20$ to $+85^\circ\text{C}$, $2.7\text{V} \leq \text{AVREFP} = \text{VDD} \leq 5.5\text{V}$, $\text{GND0} = \text{GND1} = \text{VSS} = 0\text{V}$, Reference voltage (+) = AVREFP, Reference voltage (-) = AVREFM = 0 V)

Parameter	Symbol	Conditions		MIN.	TYP.	MAX.	Unit
Resolution	RES			8		10	bits
Overall error Note 1	AINL	10-bit resolution AVREFP = VDD Note 3	$2.7\text{V} \leq \text{AVREFP} \leq 5.5\text{V}$		1.2	± 3.5	LSB
Conversion time	tCONV	10-bit resolution Target pin : ANI02-ANI03	$3.6\text{V} \leq \text{VDD} \leq 5.5\text{V}$	2.125		39	us
			$2.7\text{V} \leq \text{VDD} \leq 5.5\text{V}$	3.1875		39	us
		10-bit resolution Target pin : Internal reference voltage, and temperature sensor output voltage (HS (high-speed main) mode)	$3.6\text{V} \leq \text{VDD} \leq 5.5\text{V}$	2.375		39	us
			$2.7\text{V} \leq \text{VDD} \leq 5.5\text{V}$	3.5625		39	us
Zero-scale error Note 1, 2	Ezs	10-bit resolution AVREFP = VDD Note 3	$2.7\text{V} \leq \text{AVREFP} \leq 5.5\text{V}$			± 0.25	%FSR
Full-scale error Note 1, 2	Efs	10-bit resolution AVREFP = VDD Note 3	$2.7\text{V} \leq \text{AVREFP} \leq 5.5\text{V}$			± 0.25	%FSR
Integral linearity error Note 1	ILE	10-bit resolution AVREFP = VDD Note 3	$2.7\text{V} \leq \text{AVREFP} \leq 5.5\text{V}$			± 2.5	LSB
Differential linearity error Note 1	DLE	10-bit resolution AVREFP = VDD Note 3	$2.7\text{V} \leq \text{AVREFP} \leq 5.5\text{V}$			± 1.5	LSB
Analog input voltage	VAIN	ANI02 to ANI03		0		AVREFP	V
		Internal reference voltage ($2.7\text{V} \leq \text{VDD} \leq 5.5\text{V}$, HS (high-speed main) mode)			VBGR Note 4		V
		Temperature sensor output voltage ($2.7\text{V} \leq \text{VDD} \leq 5.5\text{V}$, HS (high-speed main) mode)			VTMPS25 Note 4		V

Note 1. Excludes quantization error ($\pm 1/2$ LSB).

Note 2. This value is indicated as a ratio (%FSR) to the full-scale value.

Note 3. When $\text{AVREFP} < \text{VDD}$, the MAX. values are as follows.

Overall error: Add ± 1.0 LSB to the MAX. value when $\text{AVREFP} = \text{VDD}$.

Zero-scale error/Full-scale error: Add $\pm 0.05\%$ FSR to the MAX. value when $\text{AVREFP} = \text{VDD}$.

Integral linearity error/ Differential linearity error: Add ± 0.5 LSB to the MAX. value when $\text{AVREFP} = \text{VDD}$.

Note 4. Refer to Section 4.7.5 Temperature sensor characteristics/internal reference voltage characteristic.

(2) When reference voltage (+) = VDD (ADREFP1 = 0, ADREFP0 = 0), reference voltage (-) = VSS (ADREFM = 0),
target pin: ANI00 to ANI03, internal reference voltage, and temperature sensor output voltage

($T_A = -40/-20$ to $+85^\circ\text{C}$, $2.7V \leq \text{VDD} \leq 5.5V$, $\text{GND0} = \text{GND1} = \text{VSS} = 0V$, Reference voltage (+) = VDD, Reference voltage (-) = VSS)

Parameter	Symbol	Conditions		MIN.	TYP.	MAX.	Unit
Resolution	RES			8		10	bits
Overall error Note 1	AINL	10-bit resolution			1.2	± 7.0	LSB
Conversion time	tCONV	10-bit resolution	3.6V $\leq \text{VDD} \leq 5.5V$	2.125		39	us
		Target pin : ANI00 to ANI03	2.7V $\leq \text{VDD} \leq 5.5V$	3.1875		39	us
		10-bit resolution	3.6V $\leq \text{VDD} \leq 5.5V$	2.375		39	us
		Target pin : Internal reference voltage, and temperature sensor output voltage (HS (high-speed main) mode)	2.7V $\leq \text{VDD} \leq 5.5V$	3.5625		39	us
Zero-scale error Note 1, 2	Ezs	10-bit resolution				± 0.60	%FSR
Full-scale error Note 1, 2	EFS	10-bit resolution				± 0.60	%FSR
Integral linearity error Note 1	ILE	10-bit resolution				± 4.0	LSB
Differential linearity Note 1	DLE	10-bit resolution				± 2.0	LSB
Analog input voltage	VAIN	ANI0 to ANI3		0		VDD	V
		Internal reference voltage (2.7V $\leq \text{VDD} \leq 5.5V$, HS (high-speed main) mode)		VBGR Note 3			V
		Temperature sensor output voltage (2.7V $\leq \text{VDD} \leq 5.5V$, HS (high-speed main) mode)		VTMPS25 Note 3			V

Note 1. Excludes quantization error ($\pm 1/2$ LSB).

Note 2. This value is indicated as a ratio (% FSR) to the full-scale value.

Note 3. Refer to Section 4.7.5 Temperature sensor characteristics/internal reference voltage characteristic.

(3) When reference voltage (+) = Internal reference voltage (ADREFP1 = 1, ADREFP0 = 0), reference voltage (-) = AVREFM/ANI1 (ADREFM = 1), target pin: ANI00, ANI02, ANI03

($T_A = -40/-20$ to $+85C$, $2.7V \leq VDD \leq 5.5V$, $GND0 = GND1 = VSS = 0V$, Reference voltage (+) = VBGR^{Note 3}, Reference voltage (-) = AVREFM = 0V

Note 4, HS (high-speed main) mode)

Parameter	Symbol	Conditions		MIN.	TYP.	MAX.	Unit
Resolution	RES			8		bits	
Conversion time	tCONV	8-bit resolution		17		39	us
Zero-scale error ^{Note 1, 2}	Ezs	8-bit resolution				±0.60	%FSR
Integral linearity error ^{Note 1}	ILE	8-bit resolution				±2.0	LSB
Differential linearity error ^{Note 1}	DLE	8-bit resolution				±1.0	LSB
Analog input voltage	VAIN			0		VBGR Note 3	V

Note 1. Excludes quantization error ($\pm 1/2$ LSB).

Note 2. This value is indicated as a ratio (% FSR) to the full-scale value.

Note 3. Refer to 4.7.5 Temperature sensor characteristics/internal reference voltage characteristic.

Note 4. When reference voltage (-) = VSS, the MAX. values are as follows.

Zero-scale error: Add ±0.35%FSR to the MAX. value when reference voltage (-) = AVREFM.

Integral linearity error: Add ±0.5 LSB to the MAX. value when reference voltage (-) = AVREFM.

Differential linearity error: Add ±0.2 LSB to the MAX. value when reference voltage (-) = AVREFM.

4.7.5 Temperature sensor characteristics/internal reference voltage characteristic

($T_A = -40/-20$ to $+85^\circ\text{C}$, $2.7\text{V} \leq \text{VDD} \leq 5.5\text{V}$, $\text{GND0} = \text{GND1} = \text{VSS} = 0\text{V}$)

Parameter	Symbol	Conditions	MIN.	TYP.	MAX.	Unit
Temperature sensor output	VTMPS25	Setting ADS register = 80H, $T_A = +25^\circ\text{C}$		1.05		V
Internal reference voltage	VBGR	Setting ADS register = 81H	1.38	1.45	1.5	V
Temperature coefficient	FVTMPS	Temperature sensor that depends on the temperature		-3.6		mV/C
Operation stabilization wait time	tAMP		5			us

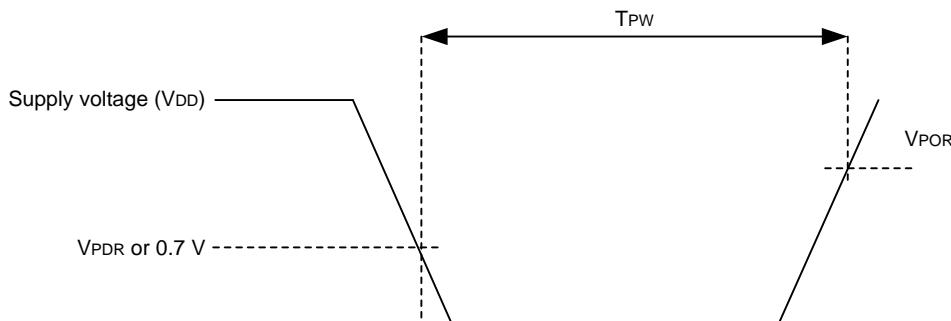
4.7.6 POR circuit characteristics (MCU)

($T_A = -40/-20$ to $+85$ C, GND0 = GND1 = VSS = 0 V)

Parameter	Symbol	Conditions	MIN.	TYP.	MAX.	Unit
Power on/down reset threshold	VPOR	Voltage threshold on VDD rising	1.47	1.51	1.55	V
	VPDR	Voltage threshold on VDD falling Note 1	1.46	1.50	1.54	V
Minimum pulse width Note 2	TPW		300			us

Note 1. However, when operating voltage drops when LVD is off, it enters STOP mode, or enable the reset status using external reset pin before the voltage drops below the operating voltage range shown in Section 4.6 AC Characteristics.

Note 2. Minimum time required for POR to reset when VDD is below VPDR. This is also the minimum time required for a POR reset when VDD exceeds VPOR after VDD is below 0.7 V during STOP mode or while the main system clock is stopped by setting bit 0 (HIOSTOP) and bit 7 (MSTOP) in the clock operation status control register (CSC).



4.7.7 LVD circuit characteristics

(1) Reset Mode and Interrupt Mode

($T_A = -40/-20$ to $+85^\circ\text{C}$, $\text{VPDR} \leq \text{VDD} \leq 5.5 \text{ V}$, $\text{GND0} = \text{GND1} = \text{VSS} = 0 \text{ V}$)

Parameter	Symbol	Conditions	MIN.	TYP.	MAX.	Unit
Voltage detection threshold	$V_{\text{LVI}0}$	Power supply rise time	3.98	4.06	4.14	V
		Power supply fall time	3.90	3.98	4.06	V
	$V_{\text{LVI}1}$	Power supply rise time	3.68	3.75	3.82	V
		Power supply fall time	3.60	3.67	3.74	V
	$V_{\text{LVI}2}$	Power supply rise time	3.07	3.13	3.19	V
		Power supply fall time	3.00	3.06	3.12	V
	$V_{\text{LVI}3}$	Power supply rise time	2.96	3.02	3.08	V
		Power supply fall time	2.90	2.96	3.02	V
	$V_{\text{LVI}4}$	Power supply rise time	2.86	2.92	2.97	V
		Power supply fall time	2.80	2.86	2.91	V
	$V_{\text{LVI}5}$	Power supply rise time	2.76	2.81	2.87	V
		Power supply fall time	2.70	2.75	2.81	V
	$V_{\text{LVI}6}$	Power supply rise time	2.66	2.71	2.76	V
		Power supply fall time	2.60	2.65	2.70	V
	$V_{\text{LVI}7}$	Power supply rise time	2.56	2.61	2.66	V
		Power supply fall time	2.50	2.55	2.60	V
	$V_{\text{LVI}8}$	Power supply rise time	2.45	2.50	2.55	V
		Power supply fall time	2.40	2.45	2.50	V
	$V_{\text{LVI}9}$	Power supply rise time	2.05	2.09	2.13	V
		Power supply fall time	2.00	2.04	2.08	V
	$V_{\text{LVI}10}$	Power supply rise time	1.94	1.98	2.02	V
		Power supply fall time	1.90	1.94	1.98	V
	$V_{\text{LVI}11}$	Power supply rise time	1.84	1.88	1.91	V
		Power supply fall time	1.80	1.84	1.87	V
	$V_{\text{LVI}12}$	Power supply rise time	1.74	1.77	1.81	V
		Power supply fall time	1.70	1.73	1.77	V
	$V_{\text{LVI}13}$	Power supply rise time	1.64	1.67	1.70	V
		Power supply fall time	1.60	1.63	1.66	V
Minimum pulse width	t_{LW}		300			μs
Detection delay time	t_{LD}				300	μs

(1) Interrupt & Reset Mode

(T_A= -40/-20 to +85°C, VPDR ≤ VDD ≤ 5.5 V, GND0 = GND1 = VSS= 0 V)

Parameter	Symbol	Conditions		MIN.	TYP.	MAX.	Unit		
Voltage detection threshold	V _{LVDA0}	VPOC2, VPOC1, VPOC2 = 0, 0, 0, falling reset voltage LVIS0, LVIS1 = 1, 0 LVIS0, LVIS1 = 0, 1 LVIS0, LVIS1 = 0, 0	Rising release reset voltage	1.60	1.63	1.66	V		
	V _{LVDA1}		Falling interrupt voltage	1.74	1.77	1.81	V		
			Rising release reset voltage	1.70	1.73	1.77	V		
	V _{LVDA2}		Falling interrupt voltage	1.84	1.88	1.91	V		
			Rising release reset voltage	1.80	1.84	1.87	V		
	V _{LVDA3}		Falling interrupt voltage	2.86	2.92	2.97	V		
			Rising release reset voltage	2.80	2.86	2.91	V		
	V _{LVDB0}		VPOC2, VPOC1, VPOC0 = 0, 0, 1, falling reset voltage	1.80	1.84	1.87	V		
	V _{LVDB1}		LVIS0, LVIS1 = 1, 0	Rising release reset voltage	1.94	1.98	2.02	V	
			Falling interrupt voltage	1.90	1.94	1.98	V		
	V _{LVDB2}		LVIS0, LVIS1 = 0, 1	Rising release reset voltage	2.05	2.09	2.13	V	
			Falling interrupt voltage	2.00	2.04	2.08	V		
	V _{LVDB3}		LVIS0, LVIS1 = 0, 0	Rising release reset voltage	3.07	3.13	3.19	V	
			Falling interrupt voltage	3.00	3.06	3.12	V		
	V _{LVDC0}	VPOC2, VPOC1, VPOC0 = 0, 1, 0, falling reset voltage LVIS0, LVIS1 = 1, 0 LVIS0, LVIS1 = 0, 1 LVIS0, LVIS1 = 0, 0	Rising release reset voltage	2.40	2.45	2.50	V		
	V _{LVDC1}		Falling interrupt voltage	2.56	2.61	2.66	V		
			Rising release reset voltage	2.50	2.55	2.60	V		
	V _{LVDC2}		Falling interrupt voltage	2.66	2.71	2.76	V		
			Rising release reset voltage	2.60	2.65	2.70	V		
	V _{LVDC3}		Falling interrupt voltage	3.68	3.75	3.82	V		
			Rising release reset voltage	3.60	3.67	3.74	V		
	V _{LVDD0}		VPOC2, VPOC1, VPOC0 = 0, 1, 1, falling reset voltage	2.70	2.75	2.81	V		
	V _{LVDD1}		LVIS0, LVIS1 = 1, 0	Rising release reset voltage	2.86	2.92	2.97	V	
			Falling interrupt voltage	2.80	2.86	2.91	V		
	V _{LVDD2}		LVIS0, LVIS1 = 0, 1	Rising release reset voltage	2.96	3.02	3.08	V	
			Falling interrupt voltage	2.90	2.96	3.02	V		
	V _{LVDD3}		LVIS0, LVIS1 = 0, 0	Rising release reset voltage	3.98	4.06	4.14	V	
			Falling interrupt voltage	3.90	3.98	4.06	V		

4.8 AFE peripheral circuit characteristics

4.8.1 High-voltage port characteristics

($T_A = -40/-20$ to $+85^\circ\text{C}$, $4.0\text{V} \leq \text{VCC} \leq 50\text{V}$, $\text{GND0} = \text{GND1} = \text{VSS} = 0\text{V}$)

Parameter	Symbol	Conditions	MIN.	TYP.	MAX.	Unit
Input voltage, high	V_{IH}		2.6			V
Input voltage, low	V_{IL}				0.7	V
Output voltage, high	V_{OH}	$\text{IOH} = -1\text{mA}$	$\text{VCC}-0.7$		VCC	V
Output voltage, low	V_{OL}	$\text{IOL} = 1\text{mA}$			0.7	V
On resistance, high level output (Pch MOS output)	R_{ONP}	$\text{IOH} = -1\text{mA}$			700	Ω
On resistance, high level output (Nch MOS output)	R_{ONN}	$\text{IOL} = 1\text{mA}$			700	Ω
Pin leakage current	I_{LK}	$\text{VI} = \text{VCC}, \text{GND}$			± 1	μA

4.8.2 Multiplexer characteristics

($T_A = -40/-20$ to $+85C$, $4.0V \leq VCC \leq 50V$, $GND0 = GND1 = VSS = 0V$)

Parameter	Symbol	Conditions	MIN.	TYP.	MAX.	Unit
Gain VIN(n)-VIN(n-1)	GAIN1	VIN10,VIN9,VIN8,VIN7,VIN6,VIN5>2.0V VIN4,VIN3,VIN2,VIN1,VIN0>0V <small>Note</small>		1.0		V/V
Gain PACK, VIN10, PON	GAIN2			0.1		V/V
Gain AN0,1,2	GAIN3			1.0		V/V
Input voltage range VIN(n)-VIN(n-1)	VRA1	VIN10,VIN9,VIN8,VIN7,VIN6,VIN5>2.0V VIN4,VIN3,VIN2,VIN1,VIN0>0V <small>Note</small>	-0.1		5.1	V
Input voltage range PACK, VIN10, PON	VRA2		0.0		50.0	V
Input voltage range AN0, 1, 2	VRA3		0.0		1.8	V
Pin leakage current	ILKV1	VIN1=5V			2	uA
		VIN2=10V			2	uA
		VIN3=15V			2	uA
		VIN4=20V			2	uA
		VIN5=25V			2	uA
		VIN6=30V			2	uA
		VIN7=35V			2	uA
		VIN8=40V			2	uA
		VIN9=45V			2	uA
		VIN10=50V			2	uA

Note Reference voltage is GND0 and GND1

4.8.3 Sigma-delta A/D converter characteristics

($T_A = -40/-20$ to $+85^\circ\text{C}$, $4.0\text{V} \leq \text{VCC} \leq 50\text{V}$, $\text{GND0} = \text{GND1} = \text{VSS} = 0\text{V}$)

Parameter	Symbol	Conditions	MIN.	TYP.	MAX.	Unit
Resolution ^{Note1}	RESAD	Conversion time = 8ms			15	bits
		Conversion time = 4ms			14	bits
		Conversion time = 2ms			13	bits
		Conversion time = 1ms			12	bits
		Conversion time = 0.5ms			11	bits
		Conversion time = 0.25ms			10	bits
Input voltage range	VINAD		-0.1		5.1	V
Integral nonlinearity	INLAD	End fit	-27		27	LSB
Conversion result in zero input	ADZERO	VIN=0V		3317 <small>Note 2</small>		LSB
Temperature dependency In zero input	dTADZERO	VIN=0V	-0.24		+0.24	LSB/C
Conversion result in full-scale input	ADFS	VIN=5.1V		24100 <small>Note 2</small>		LSB
Temperature dependency in full-scale input	dTADFS	VIN=5.1V	-0.24		+0.24	LSB/C
Input resistance	RINAD			(1.0)		MΩ
Battery cell voltage measurement error	ERRCELL1	$T_A = +25^\circ\text{C}$ After calibration			±5	mV
	ERRCELL2	$-20^\circ\text{C} \leq T_A \leq 85^\circ\text{C}$ After calibration			±10	mV
	ERRCELL2L	$-40^\circ\text{C} \leq T_A \leq 85^\circ\text{C}$ After calibration			±12	mV

Note 1. AD conversion result is output in 15-bit.

Note 2. This value is before subtracting the offset voltage.

Caution 1. Except for Battery cell voltage measurement error (ERRCELL), these parameters are sigma-delta converter circuit characteristics.

Caution 2. Calibration is needed to keep high accuracy in system.

Remark Values in brackets are design value.

4.8.4 Current integrating circuit characteristics

($T_A = -40/-20$ to $+85C$, $4.0V \leq VCC \leq 50V$, $GND0 = GND1 = VSS = 0V$)

Parameter	Symbol	Conditions	MIN.	TYP.	MAX.	Unit
Resolution	RESCC				18	bits
Conversion time	TCC			250		ms
Input voltage range	VINCC	$\pm 50mV$ mode ISENS1 to ISENS0	-50		+50	mV
		$\pm 100mV$ mode ISENS1 to ISENS0	-100		+100	mV
		$\pm 200mV$ mode ISENS1 to ISENS0	-200		+200	mV
Integral nonlinearity	INLCC	End fit			0.02	%FSR
Input resistance	RINCC	ISENS0, ISENS1		(1.0)		MΩ
Current measurement error	ERRCURR	$\pm 50mV$ mode, $-20C \leq T_A \leq 85C$ After calibration			(± 25)	uV
		$\pm 50mV$ mode, $-40C \leq T_A \leq 85C$ After calibration			(± 30)	uV
		$\pm 100mV$ mode $-20C \leq T_A \leq 85C$ After calibration			(± 50)	uV
		$\pm 100mV$ mode $-40C \leq T_A \leq 85C$ After calibration			(± 60)	uV
		$\pm 200mV$ mode $-20C \leq T_A \leq 85C$ After calibration Input voltage range : $-100mV$ to $200mV$			(± 100)	uV
		$\pm 200mV$ mode $-40C \leq T_A \leq 85C$ After calibration Input voltage range : $-100mV$ to $200mV$			(± 120)	uV

Caution 1. Except for Current measurement error (ERRCURR), these parameters are current integration circuit characteristics

Caution 2. Calibration is needed to keep high accuracy in system.

Remark Values in brackets are design value.

4.8.5 Overcurrent detection / wakeup current detection circuit characteristics

($T_A = -40/-20$ to $+85C$, $4.0V \leq VCC \leq 50V$, $GND0 = GND1 = VSS = 0V$)

Parameter	Symbol	Conditions	MIN.	TYP.	MAX.	Unit
Discharge short-circuit current detection setting voltage step	dSVSC	25mv to 200mV		12.5		mV
		200mV to 300mV		25		mV
Discharge short-circuit current detection voltage error	dVSC	25mv to 200mV setting			± 12.5	mV
		225mV to 300mV setting			± 25.0	mV
Discharge overcurrent detection setting voltage step	dSVDOC	15mV to 100mV		2.5		mV
		100mV to 200mV		5		mV
Discharge overcurrent detection voltage error ^{Note 1}	dVDOC	15mV to 100mV setting			± 5.0	mV
		105mV to 200mV setting			± 7.5	mV
Charge overcurrent detection setting voltage step	dSVCOC	-60mV to -2.5mV		2.5		mV
		-100mV to -60mV		5		mV
Charge overcurrent detection voltage error ^{Note 1}	dVCOC	-60mV to -2.5mV setting			± 5.0	mV
		-100mV to -65mV setting			± 7.5	mV
Discharge wakeup current detection setting voltage step	dSVDWU	0mV to 140mV		1.25		mV
Charge wakeup current detection setting voltage step	dSVCWU	-140mV to 0mV		1.25		mV
DBPT current detection setting voltage step	dSVDBPT	0mV to 140mV		1.25		mV
Discharge wakeup current detection voltage error ^{Note 1}	dVDWU	20 times mode ISENS1 to ISENS0: 0.25mV to 2.5mV	-0.10	0.0	+0.25	mV
Charge wakeup current detection voltage error ^{Note 1}	dVCWU	20 times mode ISENS1 to ISENS0: -0.25mV to -2.5mV	-0.25	0.0	+0.10	mV
DBPT current detection voltage error ^{Note 1}	dVDBPT	20 times mode ISENS1 to ISENS0: 0.25mV to 2.5mV	-0.10	0.0	+0.25	mV
Discharge short-circuit current detection time error ^{Note 2}	dTSC	0us to 916us (61us step)	0.0		30.5	us
Discharge overcurrent detection time error ^{Note 2}	dTDOC	0.488ms to 32s (0.488ms step)	0.0		122	us
Charge overcurrent detection time error	dTCOC	0us to 15564us (61us step)	0.0		30.5	us
Discharge wakeup current detection time error ^{Note 2}	dTDWU	3.91ms to 62.56ms (61us step)	0		3.9	ms
Charge wakeup current detection time error ^{Note 2}	dTCWU	3.91ms to 62.56ms (61us step)	0		3.9	ms
DBPT current detection time error ^{Note 2}	dTDBPT	0us to 916us (61us step)	0.0		30.5	us

Note 1. This is the specification after zero-calibration is executed.

Note 2. The frequency error of On-chip oscillator (AOCO and ALOCO) is excluded from these detection time error.

4.8.6 Charge/discharge FET control circuit characteristics

($T_A = -40/-20$ to $+85^\circ\text{C}$, $4.0\text{V} \leq \text{VCC} \leq 50\text{V}$, $\text{GND0} = \text{GND1} = \text{VSS} = 0\text{V}$)

Parameter	Symbol	Conditions	MIN.	TYP.	MAX.	Unit
High-side Charge FET control Output voltage, CFOUT=H	CFON1	$4.0\text{V} \leq \text{VCC} < 6.0\text{V}$ Load between CFOUT to VBAT = $50\text{nF}/10\text{M}\Omega$ Based on VBAT pin	5.0	9.5	10.0	V
	CFON2	$6.0\text{V} \leq \text{VCC}, -20^\circ\text{C} \leq T_A \leq 85^\circ\text{C}$ Load between CFOUT to VBAT = $50\text{nF}/10\text{M}\Omega$ Based on VBAT pin	8.0	9.5	10.0	V
	CFON2L	$6.0\text{V} \leq \text{VCC}, -40^\circ\text{C} \leq T_A \leq 85^\circ\text{C}$ Load between CFOUT to VBAT = $50\text{nF}/10\text{M}\Omega$ Based on VBAT pin	6.5	9.5	10.0	V
High-side Charge FET control Output voltage, CFOUT=L	CFOFF	Load between CFOUT to VBAT = $50\text{nF}/10\text{M}\Omega$ Based on VBAT pin	-0.2	0.0	0.2	V
High-side Charge FET control CFOUT rise Time	CFTR1	$4.0\text{V} \leq \text{VCC} < 6.0\text{V}$ Load between CFOUT to VBAT = $50\text{nF}/10\text{M}\Omega$ $\text{Lo}(\text{VBAT}) \rightarrow \text{Hi}(\text{VBAT}+5\text{V})$		1.5	2.5	ms
	CFTR2	$6.0\text{V} \leq \text{VCC}$ Load between CFOUT to VBAT = $50\text{nF}/10\text{M}\Omega$ $\text{Lo}(\text{VBAT}) \rightarrow \text{Hi}(\text{VBAT}+5\text{V})$		1.0	1.5	ms
High-side Charge FET control CFOUT fall Time	CFTF1	Load between CFOUT to VBAT = $50\text{nF}/10\text{M}\Omega$ $\text{Hi}(\text{VBAT}+\text{CFON1}) \rightarrow \text{Lo}(\text{VBAT}+1\text{V})$ OFF speed acceleration = Disable		0.5	1.0	ms
	CFTF2	Load between CFOUT to VBAT = $50\text{nF}/10\text{M}\Omega$ $\text{Hi}(\text{VBAT}+\text{CFON1}) \rightarrow \text{Lo}(\text{VBAT}+1\text{V})$ OFF speed acceleration = Enable		(0.2)	(0.5)	ms
High-side Discharge FET control Output voltage, DFOUT=H	DFON1	$4.0 \leq \text{VCC} < 6.0\text{V}$ Load between DFOUT to PACK = $50\text{nF}/10\text{M}\Omega$ Based on PACK pin	5.0	9.5	10.0	V
	DFON2	$6.0 \leq \text{VCC}, -20^\circ\text{C} \leq T_A \leq 85^\circ\text{C}$ Load between DFOUT to PACK = $50\text{nF}/10\text{M}\Omega$ Based on PACK pin	8.0	9.5	10.0	V
	CFON2L	$6.0\text{V} \leq \text{VCC}, -40^\circ\text{C} \leq T_A \leq 85^\circ\text{C}$ Load between CFOUT to VBAT = $50\text{nF}/10\text{M}\Omega$ Based on VBAT pin	6.5	9.5	10.0	V
High-side Discharge FET control Output voltage, DFOUT=L	DFOFF	Load between DFOUT to PACK = $50\text{nF}/10\text{M}\Omega$ Based on PACK pin	-0.2	0.0	0.2	V
High-side Discharge FET control DFOUT rise Time	DFTR1	$4.0\text{V} \leq \text{VCC} < 6.0\text{V}$ Load between DFOUT to PACK = $50\text{nF}/10\text{M}\Omega$ $\text{Lo}(\text{PACK}) \rightarrow \text{Hi}(\text{PACK}+5\text{V})$		1.5	2.5	ms
	DFTR2	$6.0\text{V} \leq \text{VCC}$ Load between DFOUT to PACK = $50\text{nF}/10\text{M}\Omega$ $\text{Lo}(\text{PACK}) \rightarrow \text{Hi}(\text{PACK}+5\text{V})$		1.0	1.5	ms
High-side Discharge FET control DFOUT fall Time	DFTF1	Load between DFOUT to PACK = $50\text{nF}/10\text{M}\Omega$ $\text{Hi}(\text{PACK}+\text{DFON1}) \rightarrow \text{Lo}(\text{PACK}+1\text{V})$ OFF speed acceleration = Disable		0.5	1.0	ms
	DFTF2	Load between DFOUT to PACK = $50\text{nF}/10\text{M}\Omega$ $\text{Hi}(\text{PACK}+\text{DFON1}) \rightarrow \text{Lo}(\text{PACK}+1\text{V})$ OFF speed acceleration = Enable		(0.2)	(0.5)	ms
Low-side Charge FET control Clamp voltage	CCLPON1	Based on VBAT pin $4.0\text{V} \leq \text{VBAT} < 7.0\text{V}$	-6.0		-3.0	V
	CCLPON2	Based on VBAT pin $7.0\text{V} \leq \text{VBAT}$	-14.0	-10.0	-6.0	V
Low-side Discharge FET control Clamp voltage	DCLPON1	Based on PACK pin $4.0\text{V} \leq \text{PACK} < 7.0\text{V}$	-6.0		-3.0	V
	DCLPON2	Based on PACK pin $7.0\text{V} \leq \text{PACK}$	-14.0	-10.0	-6.0	V

Caution After trimming.

Remark Values in brackets are design value.

4.8.7 Power on circuit characteristics

($T_A = -40/-20$ to $+85C$, $4.0V \leq VCC \leq 50V$, $GND0 = GND1 = VSS = 0V$)

Parameter	Symbol	Conditions	MIN.	TYP.	MAX.	Unit
Input voltage, High	VIH		2.6		VCC	V
Input voltage, Low	VIL		0.0		0.7	V
Pull-down resistance	Rdpdn		12.4			MΩ

Caution To entry power down mode, it is necessary to input power down command while PON port is L.

4.8.8 Series regulator circuit characteristics

($T_A = -40/-20$ to $+85C$, $4.0V \leq VCC \leq 50V$, $GND0 = GND1 = VSS = 0V$)

Parameter	Symbol	Conditions	MIN.	TYP.	MAX.	Unit
Output voltage	VR2O	3.3V setting	Io=50uA to 20mA,	3.20	3.30	3.40
	VR2O5	5.0V setting	6.0V \leq VCC \leq 50.0V, Io=50uA to 20mA	4.85	5.00	5.15
Load drive capability Note	IOMAX	3.3V setting	4.0V \leq VCC $<$ 5.0V	10.0		mA
			5.0V \leq VCC \leq 50.0V	20.0		mA
	IOMAX5	5.0V setting	6.0V \leq VCC $<$ 7.0V	10.0		mA
			7.0V \leq VCC \leq 50.0V	20.0		mA

Note In case of using load drive, total power consumption must be under the maximum ratings power consumption (Pd).

Caution After trimming.

4.8.9 AFE reset circuit characteristics

($T_A = -40/-20$ to $+85C$, $4.0V \leq VCC \leq 50V$, $GND0 = GND1 = VSS = 0V$)

Parameter	Symbol	Conditions	MIN.	TYP.	MAX.	Unit
VREG2 release voltage	VREL		2.8	2.9	3.0	V
VREG2 detection voltage	VDET	After trimming	2.7	2.8	2.9	V

4.8.10 Cell balancing circuit characteristics

($T_A = -40/-20$ to $+85C$, $4.0V \leq VCC \leq 50V$, $GND0 = GND1 = VSS = 0V$)

Parameter	Symbol	Conditions	MIN.	TYP.	MAX.	Unit
1st cell on resistance	RCOND1	VIN1 – VIN0 = 3.5V	100	200	400	Ω
2nd cell on resistance	RCOND2	VIN2 – VIN1 = 3.5V	100	200	400	Ω
3rd cell on resistance	RCOND3	VIN3 – VIN2 = 3.5V	100	200	400	Ω
4th cell on resistance	RCOND4	VIN4 – VIN3 = 3.5V	100	200	400	Ω
5th cell on resistance	RCOND5	VIN5 – VIN4 = 3.5V	100	200	400	Ω
6th cell on resistance	RCOND6	VIN6 – VIN5 = 3.5V	100	200	400	Ω
7th cell on resistance	RCOND7	VIN7 – VIN6 = 3.5V	100	200	400	Ω
8th cell on resistance	RCOND8	VIN8 – VIN7 = 3.5V	100	200	400	Ω
9th cell on resistance	RCOND9	VIN9 – VIN8 = 3.5V	100	200	400	Ω
10th cell on resistance	RCOND10	VIN10 – VIN9 = 3.5V	100	200	400	Ω

4.8.11 VREG2 Voltage Drop Detection Circuit characteristics

($T_A = -40/-20$ to $+85C$, $4.0V \leq VCC \leq 50V$, $GND0 = GND1 = VSS = 0V$)

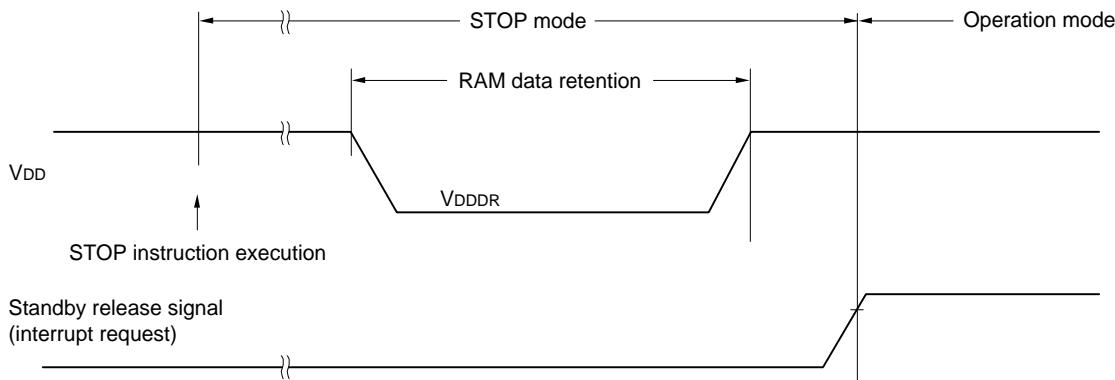
Parameter	Symbol	Conditions	MIN.	TYP.	MAX.	Unit
VREG2 Voltage detection threshold	VR2LVD	3.3V setting	2.85	2.90	2.95	V
	VR2LVD5	5.0V setting	4.55	4.60	4.65	V

4.9 RAM Data Retention Characteristics

($T_A = -40/-20$ to $+85^\circ\text{C}$, $2.7V \leq VDD \leq 5.5V$, $\text{GND}0 = \text{GND}1 = \text{VSS} = 0V$)

Parameter	Symbol	Conditions	MIN.	TYP.	MAX.	Unit
Data retention supply voltage	V _{DDDR}		1.46 ^{Note}		5.5	V

Note The value depends on the POR detection voltage. When the voltage drops, the RAM data is retained before a POR reset is effected, but RAM data is not retained when a POR reset is effected.



4.10 Flash Memory Programming Characteristics

($T_A = -40/-20$ to $+85^\circ\text{C}$, $2.7V \leq VDD \leq 5.5V$, $\text{GND}0 = \text{GND}1 = \text{VSS} = 0V$)

Parameter	Symbol	Conditions	MIN.	TYP.	MAX.	Unit
System clock frequency	f _{CLK}		1		32	MHz
Number of code flash rewrites ^{Note 1, 2, 3}	C _{erwr}	Retained for 20 years $T_A = 85^\circ\text{C}$	1,000			Times
Number of data flash rewrites ^{Note 1, 2, 3}		Retained for 1 year $T_A = 25^\circ\text{C}$		1,000,000		
		Retained for 5 years $T_A = 85^\circ\text{C}$	100,000			
		Retained for 20 years $T_A = 85^\circ\text{C}$	10,000			

Note 1. 1 erase + 1 write after the erase is regarded as 1 rewrite. The retained years are until next rewrite completion.

Note 2. When using flash memory programmer and Renesas Electronics self-programming library

Note 3. These are the characteristics of the flash memory and the results obtained from reliability testing by Renesas Electronics Corporation.

4.11 Dedicated Flash Memory Programmer Communication (UART)

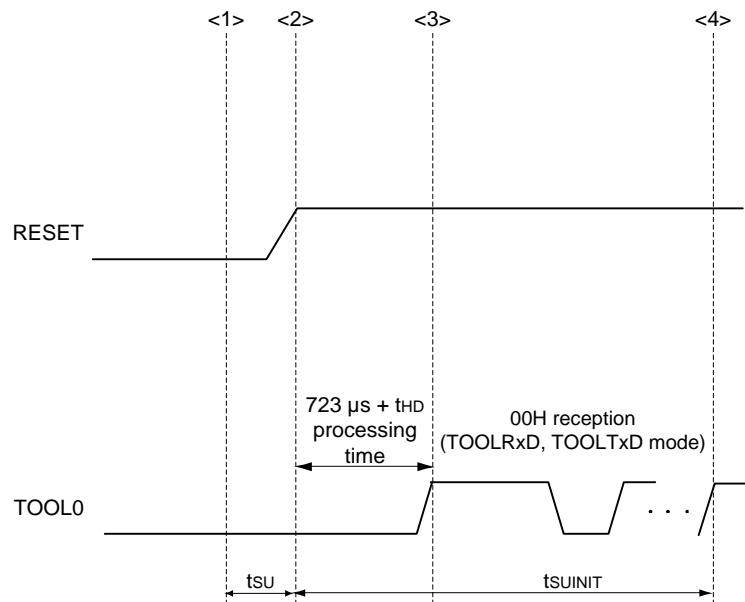
($T_A = -40/-20$ to $+85^\circ\text{C}$, $2.7V \leq VDD \leq 5.5V$, $\text{GND}0 = \text{GND}1 = \text{VSS} = 0V$)

Parameter	Symbol	Conditions	MIN.	TYP.	MAX.	Unit
Transfer rate		During serial programming	115,200		1,000,000	bps

4.12 Timing of Entry to Flash Memory Programming Modes

($T_A = -40\text{--}20$ to $+85^\circ\text{C}$, $2.7V \leq VDD \leq 5.5V$, $GND0 = GND1 = VSS = 0V$)

Parameter	Symbol	Conditions	MIN.	TYP.	MAX.	Unit
The time needed when an external reset ends until the initial communication settings are specified	tsINIT	POR and LVD reset must end before the external reset ends.			100	ms
The time needed from when the TOOL0 pin is placed at low level until an external reset ends	tsU	POR and LVD reset must end before the external reset ends.	10			us
The time needed for the TOOL0 pin must be kept at low level after an external reset ends (excluding the processing time of the firmware to control the flash memory)	tHD	POR and LVD reset must end before the external reset ends.	1			ms



<1> The low level is input to the TOOL0 pin.

<2> The external reset ends (POR and LVD reset must end before the external reset ends).

<3> The TOOL0 pin is set to the high level.

<4> Setting of the flash memory programming mode by UART reception and complete the baud rate setting.

Remark tsINIT: The segment shows that it is necessary to finish specifying the initial communication settings within 100 ms from when the external resets end.

tsU: Time needed for the TOOL0 pin is placed at low level until the pin reset ends

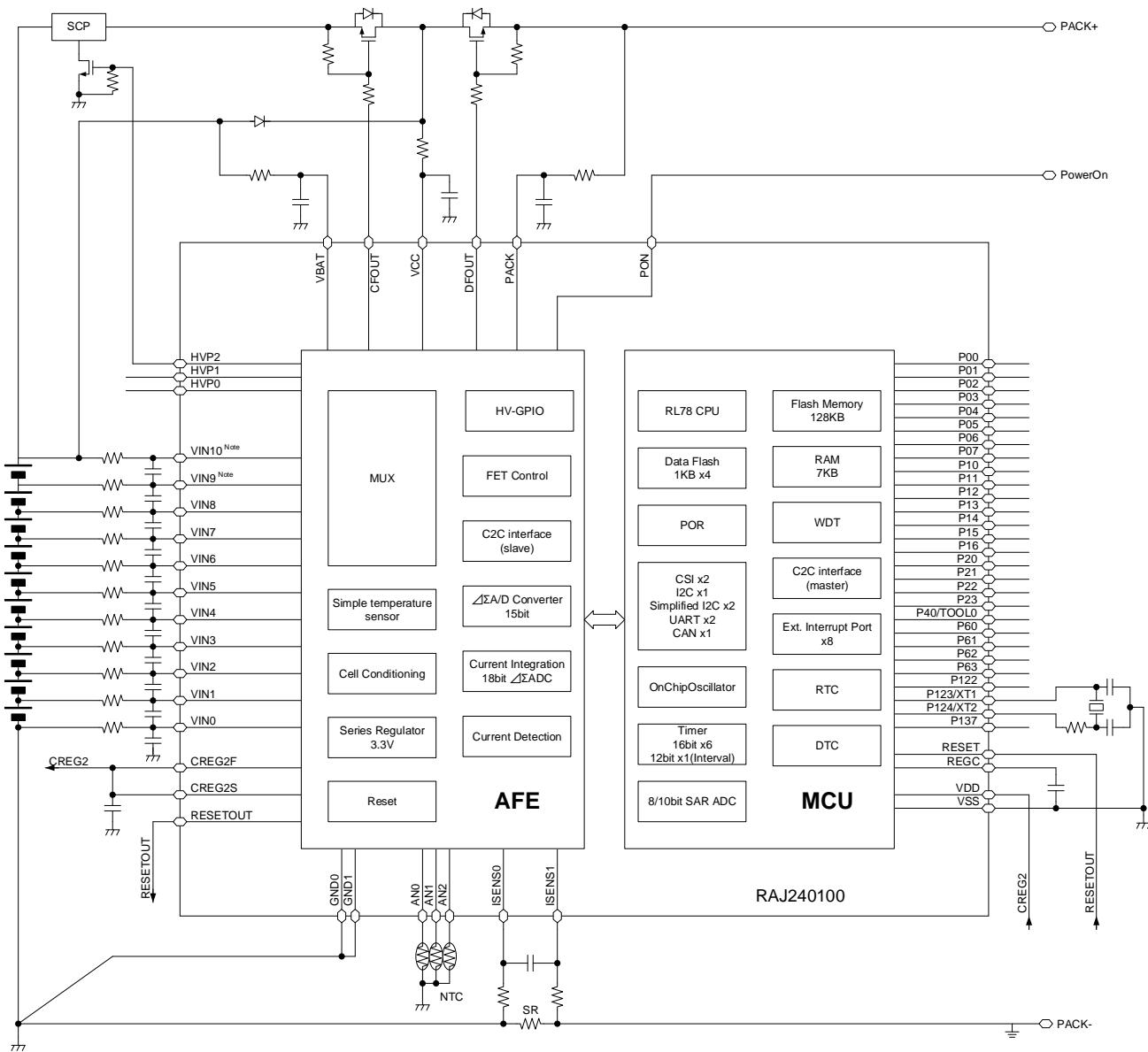
tHD: Time needed for the TOOL0 pin at low level from when the external resets end
(excluding the processing time of the firmware to control the flash memory)

5. Detailed description

5.1 Overview

RAJ240090 / RAJ240100 are Renesas fuel gauge ICs which consist of a MCU block and an AFE block in a single package and accomplish various protection mechanisms. These IC's incorporates advanced battery management features such as primary and secondary protection, voltage and current measurement, current integration, host communication interface. By using the battery management controlled firmware and data are stored in the embedded flash memory to control the embedded analog and digital hardware circuits, optimum battery management operation including high accuracy remaining capacity estimation and battery safety can be achieved.

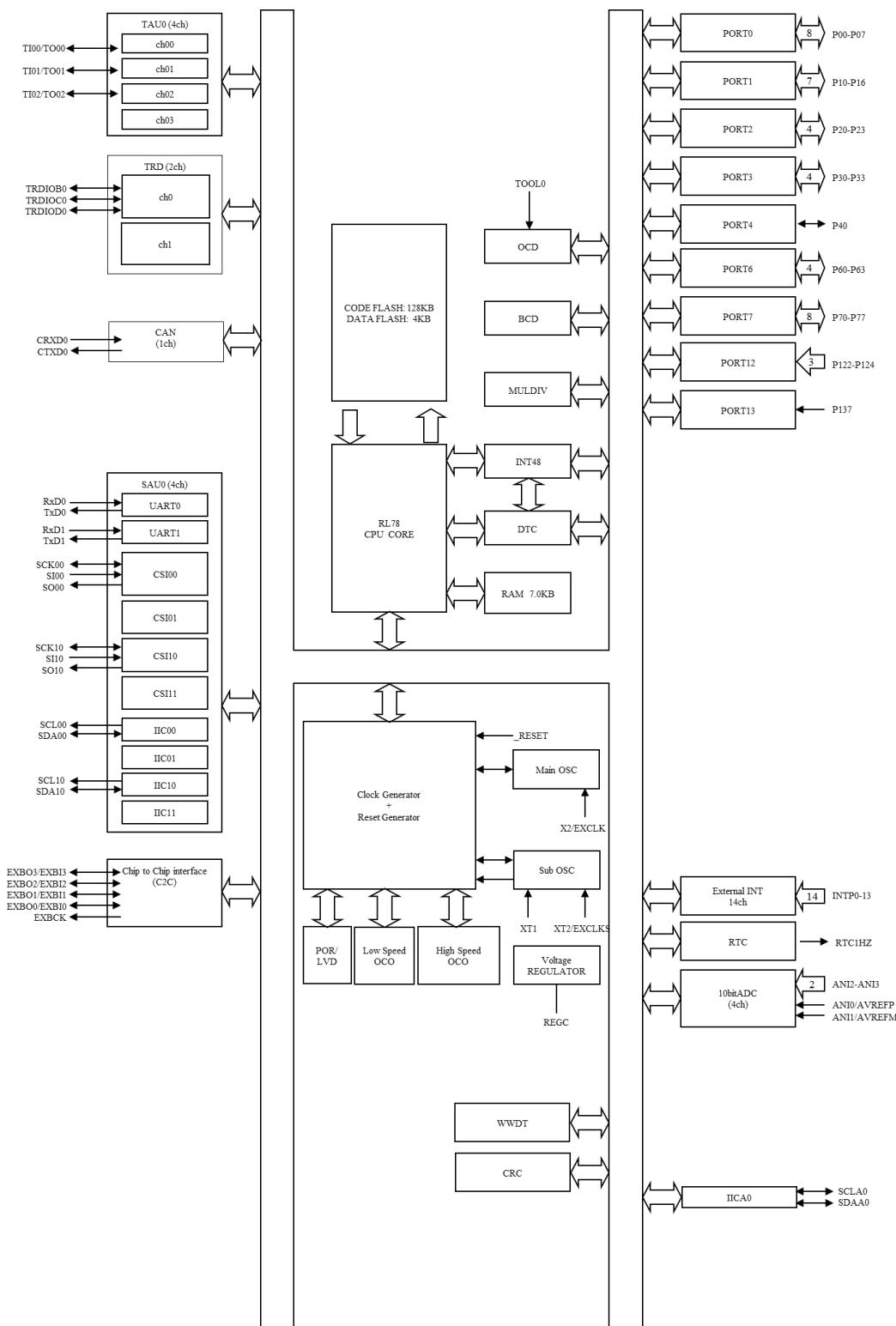
5.2 System block diagram



Note VIN10 pin and VIN9 pin are only applicable to RAJ240100.

Caution The example peripheral circuit does not guarantee proper operation. Please perform sufficient evaluation using the actual application to determine the circuits and peripherals.

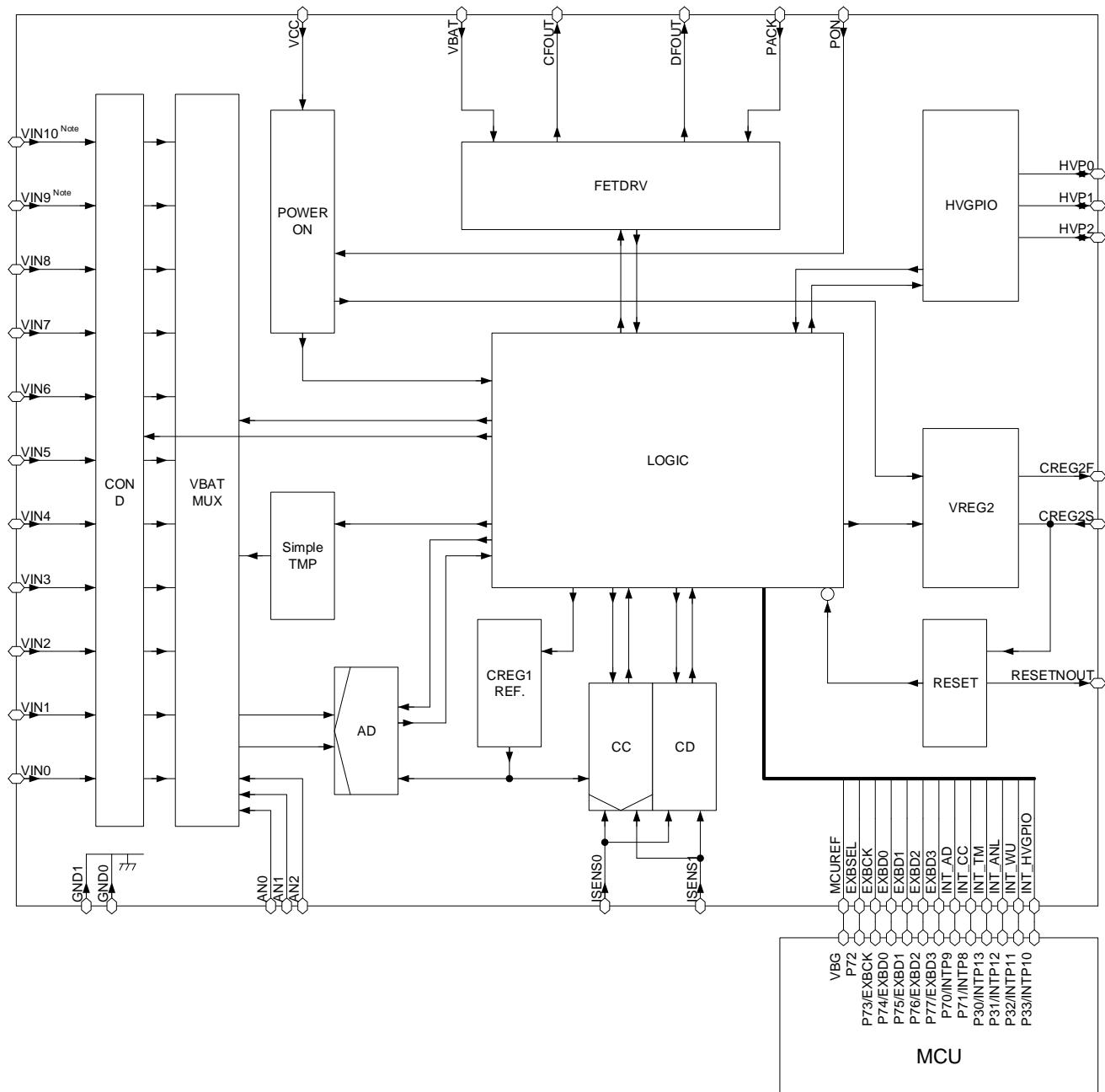
5.3 MCU block diagram



Caution 1. P30, P31, P32, P33, P70, P72, P73, P74, P75, P76 and P77 are connected to the internal AFE chip and not connected to the package external pins.

Caution 2. Each interrupt request of AFE are assigned to P30/INTP13, P31/INTP12, P32/INTP11, P33/INTP10, P70/INTP9 and P71/INTP8.

5.4 AFE block diagram



Note VIN10 pin and VIN9 pin are only applicable to RAJ240100.

6. Application Guideline

6.1 Typical Application Specification

A typical specification example of Li-ion battery management unit as shown below.

From the next page, the typical application guideline is explained for RAJ240100 (10 series cells application).

Battery cell assembly : 8S1P (8 cells in series and 1 cell in parallel) for RAJ240090
: 10S1P (10 cells in series and 1 cell in parallel) for RAJ240100

Host interface : System Management Bus (SMBus) Specification, version 1.1.
: UART
: CAN

Primary protection : charge FET and discharge FET

Secondary protection : Fuse blow by FGIC (RAJ240090 and RAJ240100) or a secondary protection device.

Connector pins:

Pack+ Positive battery pack terminal

SCL SMBus clock

SDA SMBus data

CANH CAN high

CANL CAN low

UART UART communication port

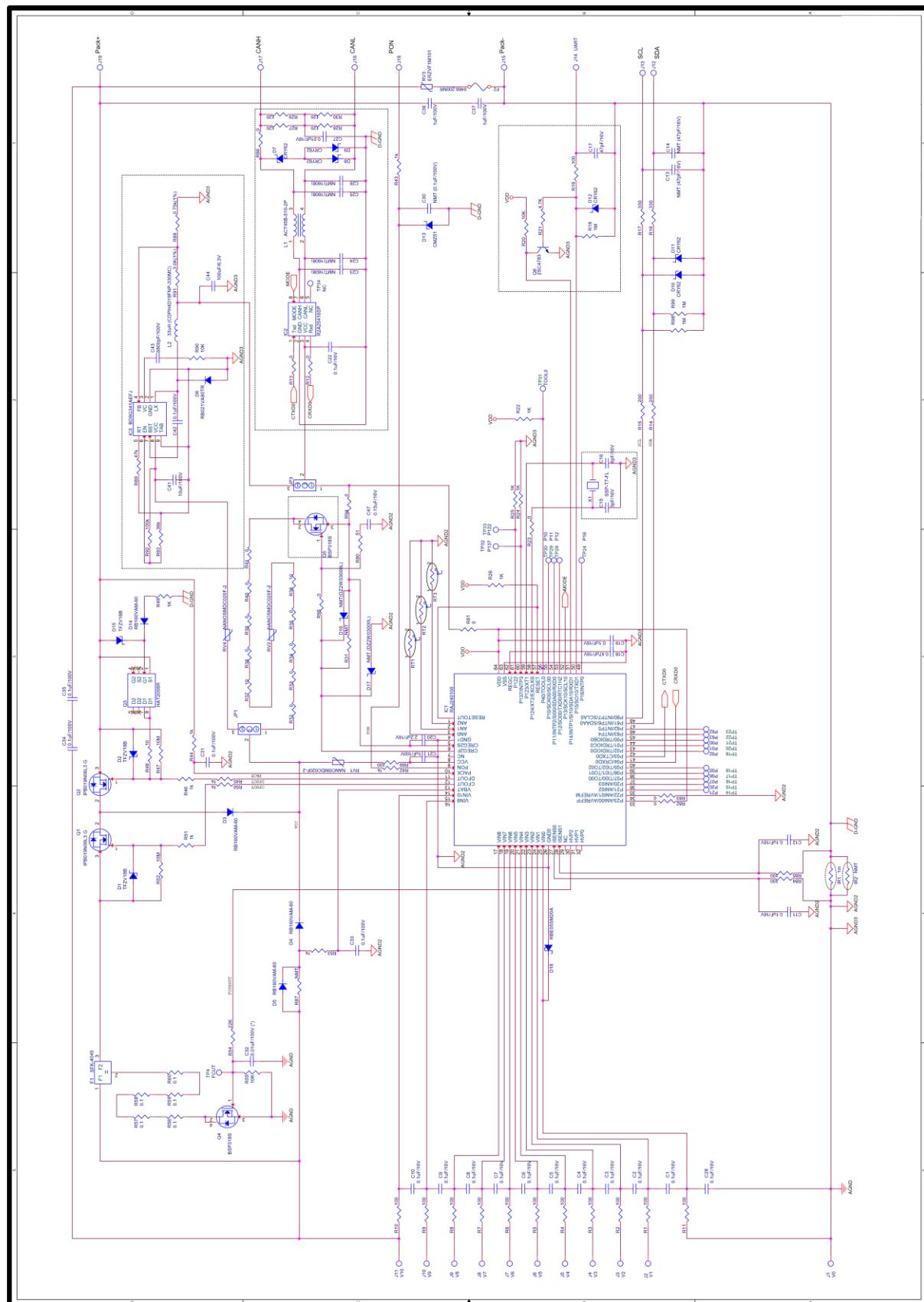
PON High voltage port for battery power on

Pack- Negative battery pack terminal

External reverse charge protection circuit

Battery and charge/discharge MOSFET temperature measurement with three thermistors

6.2 Typical Application Circuit

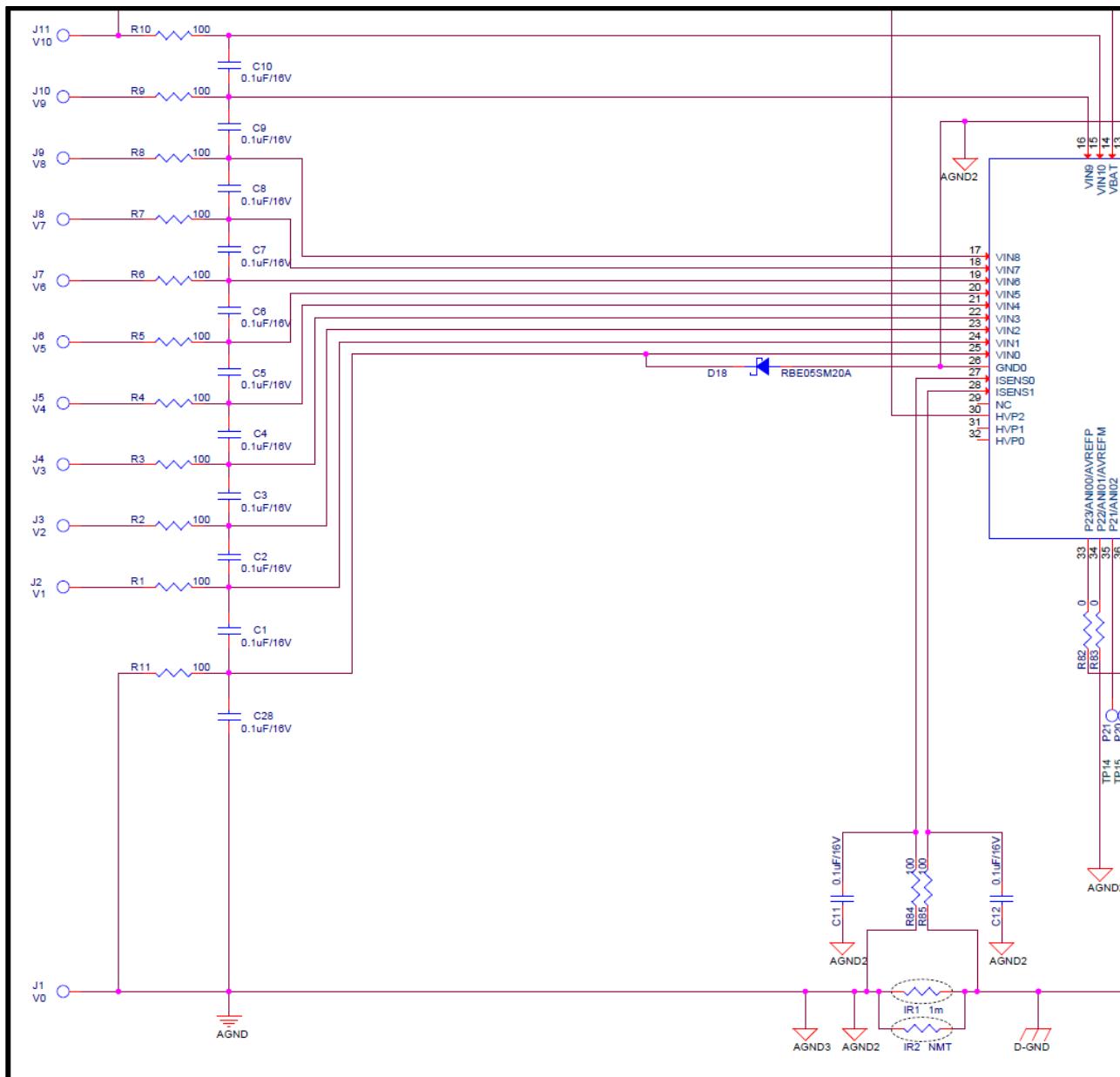


Typical Application Circuit Schematic

6.3 Circuit Design Guideline

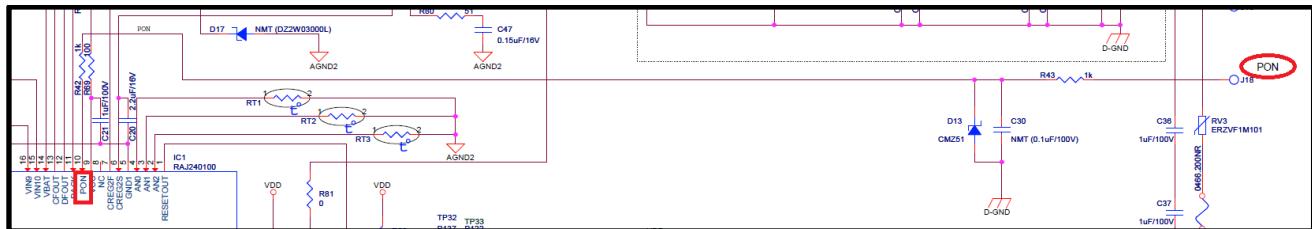
6.3.1 Cell voltage monitor circuit

- Place an input filter between FGIC's VIN port and each of the cells.
- Place resistors valued around 100Ω and capacitors valued around $0.1\mu F$ to $VIN_1 - VIN_{10}$ for surge protection. It is necessary to calculate the cut-off frequency and use correct resistance and capacitance value based on application.



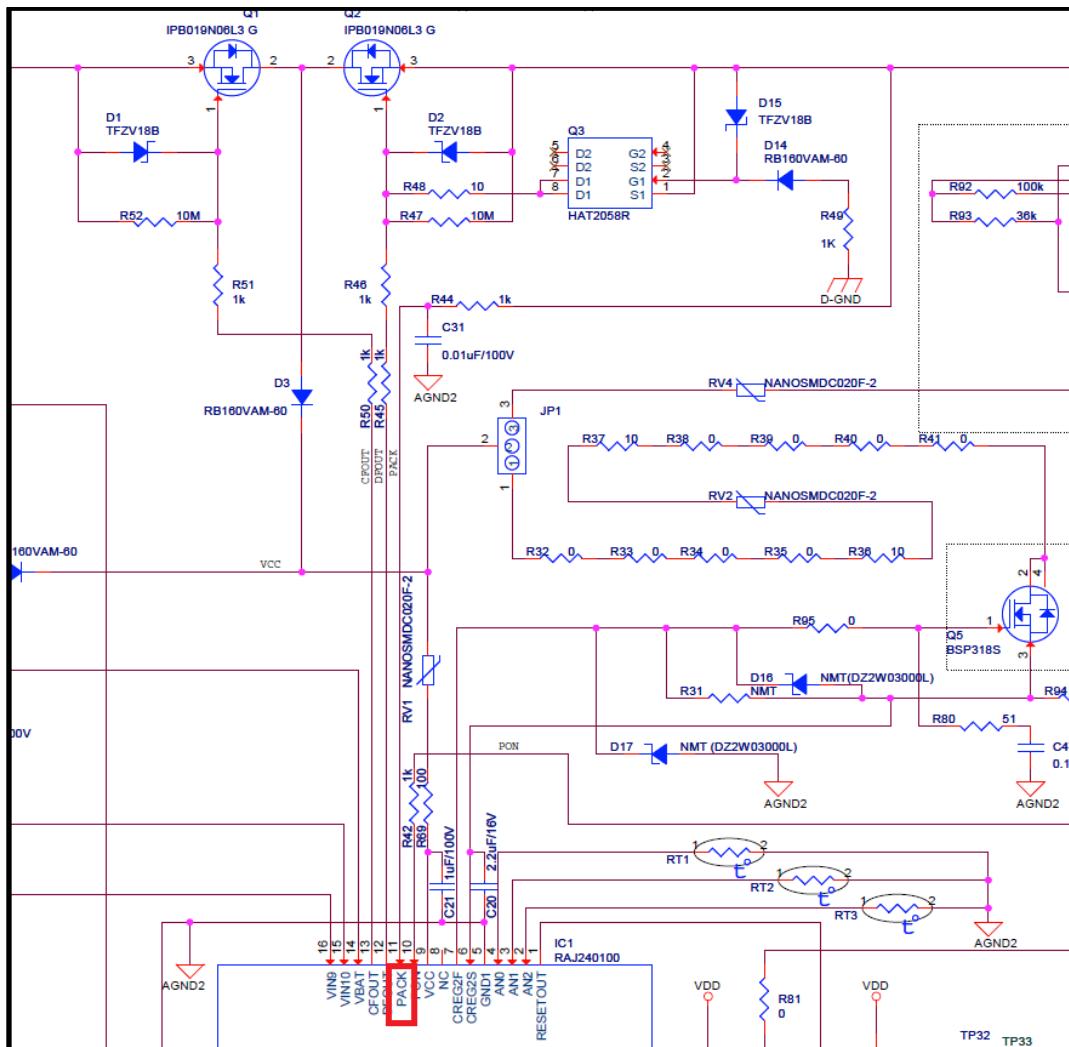
6.3.2 Battery power on circuit

- Place resistors value around $2\text{k}\Omega$ ($1\text{k}\Omega+1\text{k}\Omega$), capacitor $0.1\mu\text{F}$ and zener diode to PON for surge protection. It is necessary to calculate cut-off frequency and use correct resistance and capacitance value based on application.



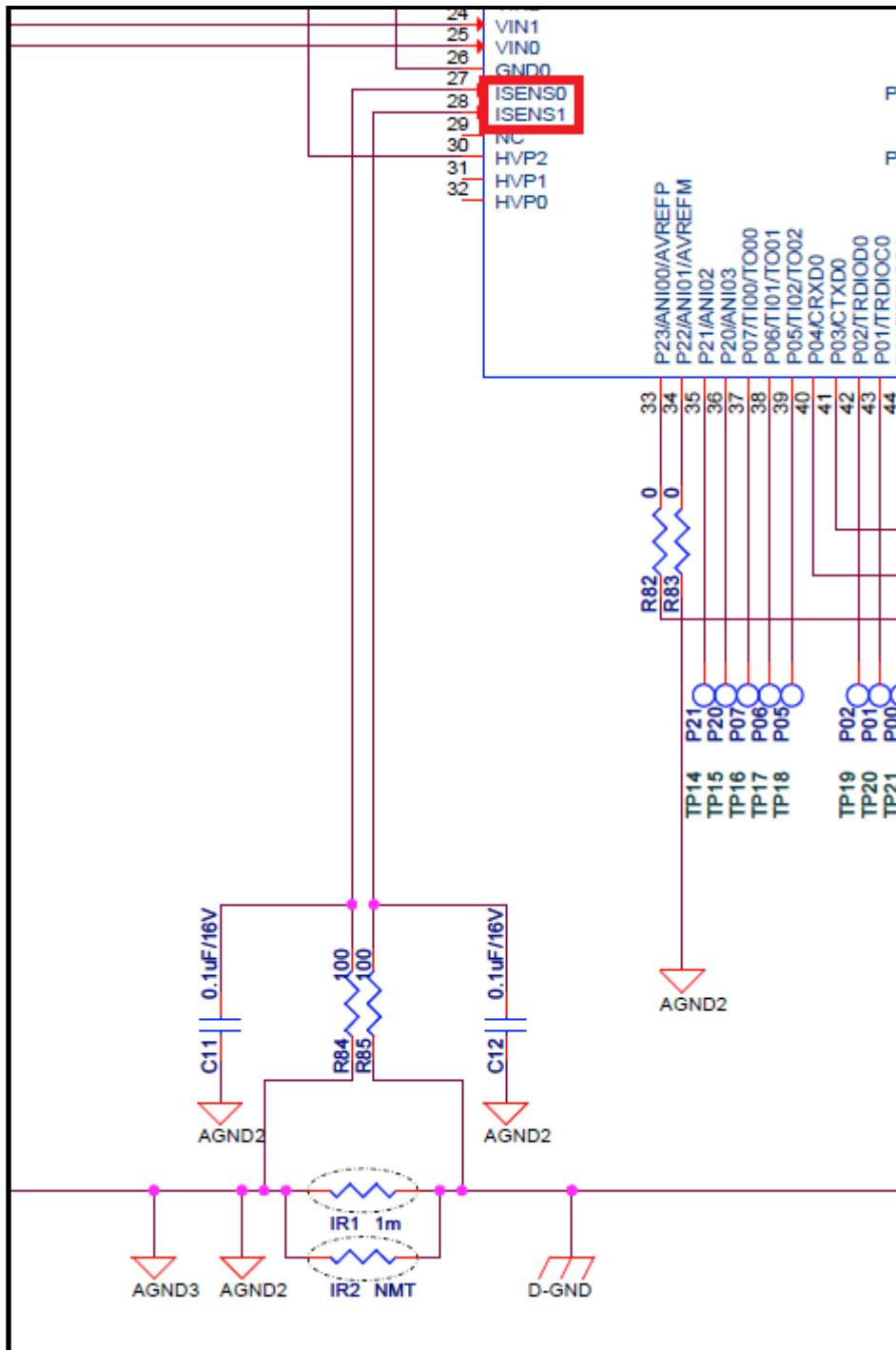
6.3.3 PACK port

- PACK port is source voltage of DFOUT (D-FET gate control signal). R44 plays a role in limiting the current limit when charger is reverse-charged. $1\text{k}\Omega$ is recommended, if it is too large, the D-FET turn off speed will becomes too slow.
- C31 helps provide stable D-FET boost operation. $0.01\mu\text{F}$ is recommended. If it is too large, the D-FET turn off speed will becomes too slow.



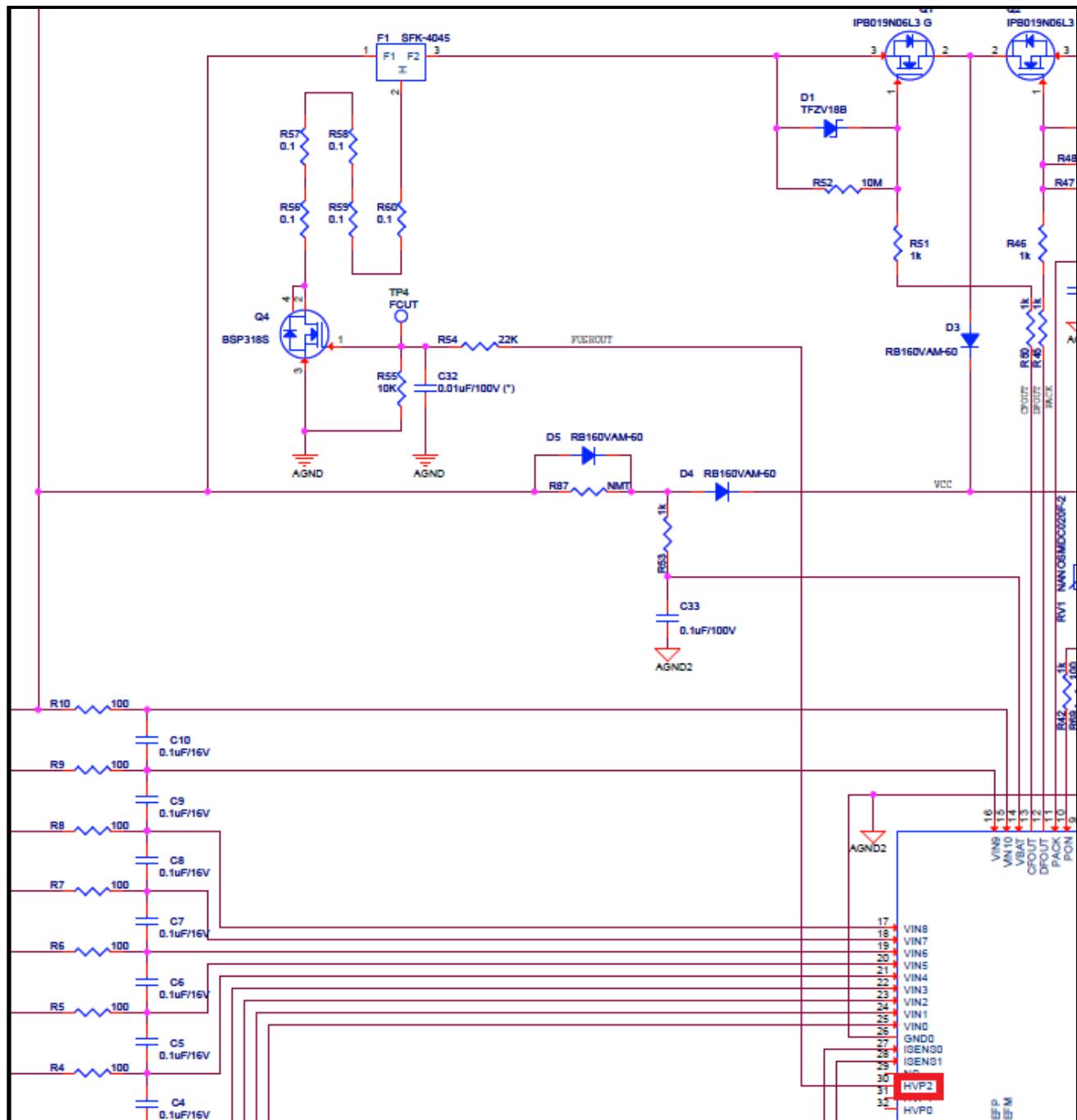
6.3.4 Current monitor

- Potential difference on the sense resistor is monitored by current integration circuit.
- Place a Low Pass Filter (100 Ω, 0.1μF) at input stage.
- Sense lines should be shielded if small voltage difference is detected to ensure high accurate current sensing.



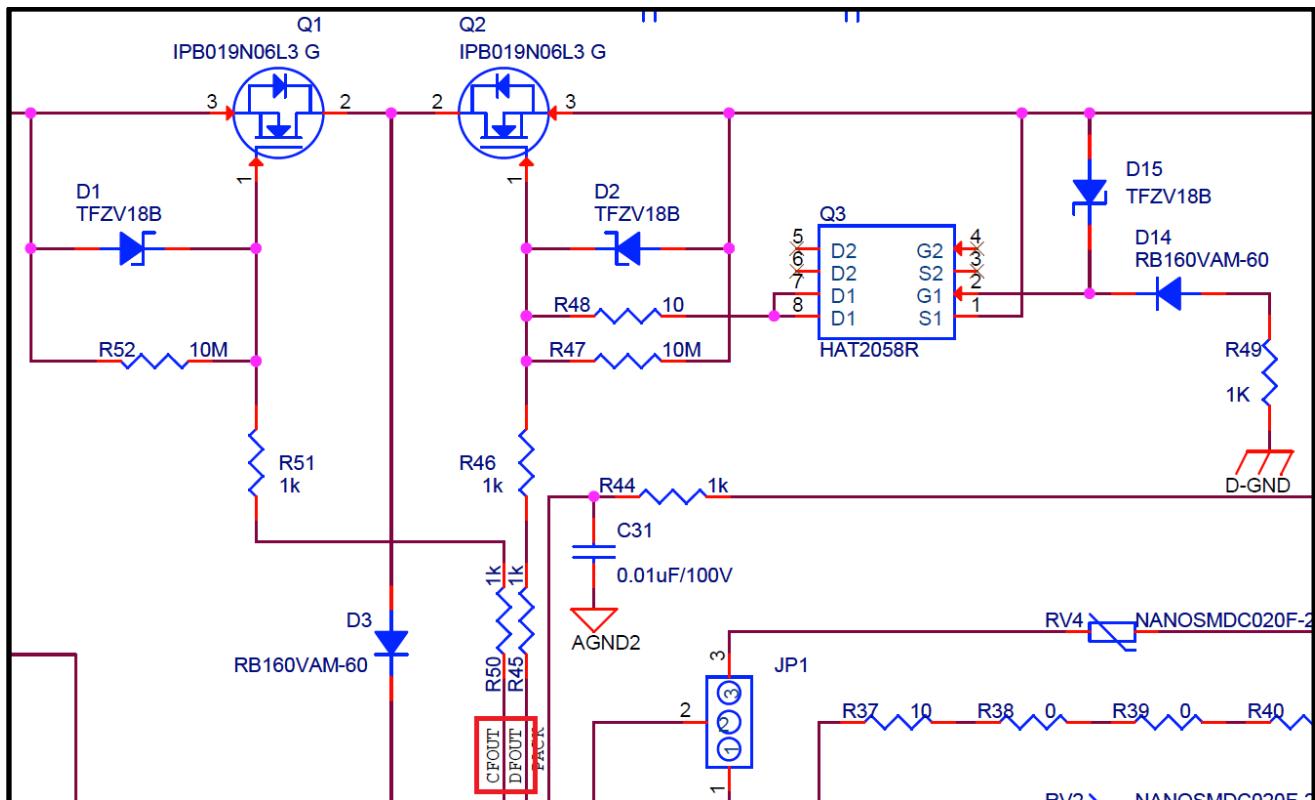
6.3.5 Fuse control

- Self-control protector (SCP) is used for fuse in reference circuit.
 - The fuse will blow when RAJ240100 drives HVP2 (High voltage GPIO) pin high to make Q4 ON.
 - The fuse will blow when overcurrent exceeds the limit of SCP.
 - R56-R60 are used for battery electrochemical migration short circuit countermeasures.



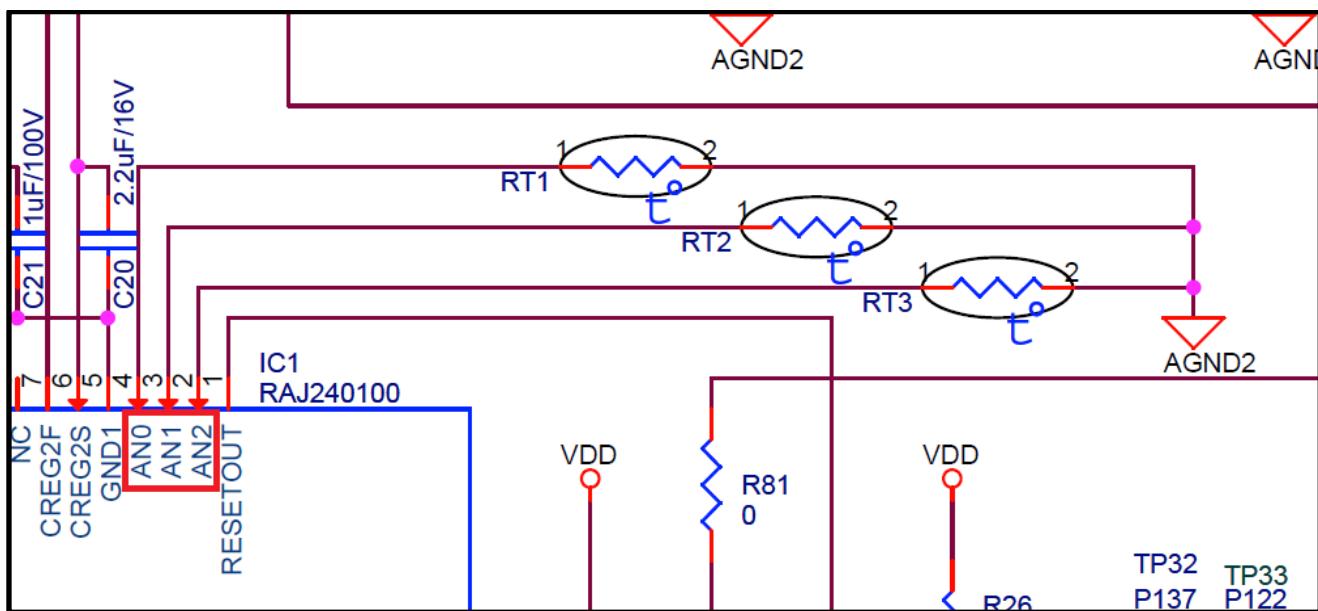
6.3.6 C-FET and D-FET control

- Q3 is located between gate and source of Q2 to make D-FET turn off when charger is reverse connected.
- R49 is for Q3 gate protection. (1kΩ is recommended.)
- R45, R46 and R50, R51 are use as gate protection and C-FET/D-FET noise reduction. (2kΩ is recommended.)
- R47 and R52 are used to fix C-FET/D-FET gate voltage in order to keep stable off state when FET is turn off. 10MΩ is recommended to prevent voltage drop.



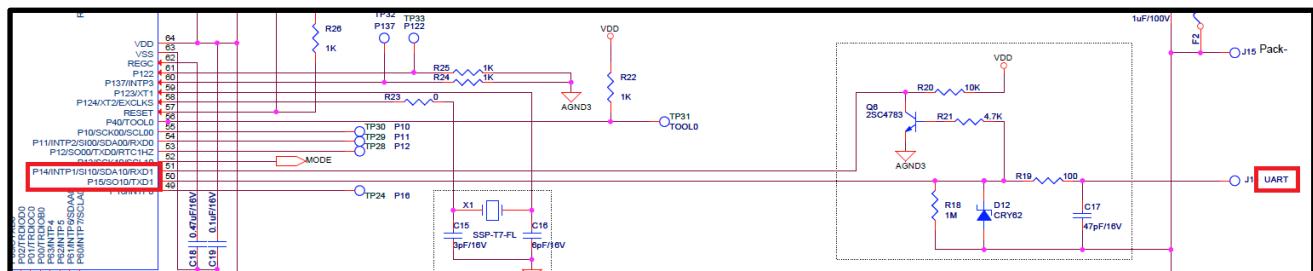
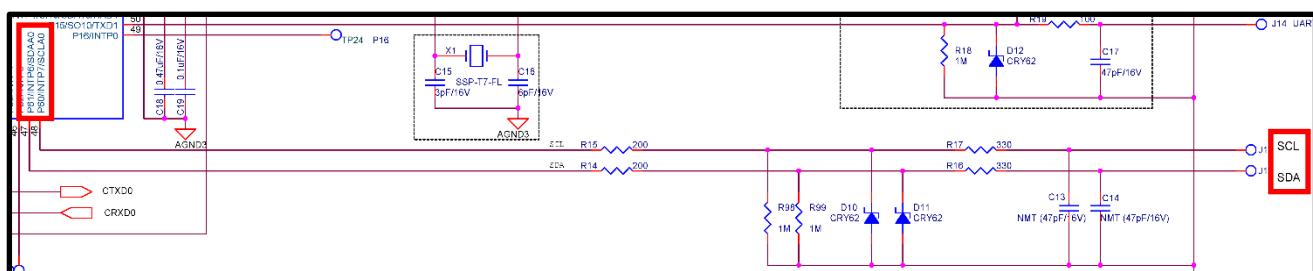
6.3.7 Thermistor

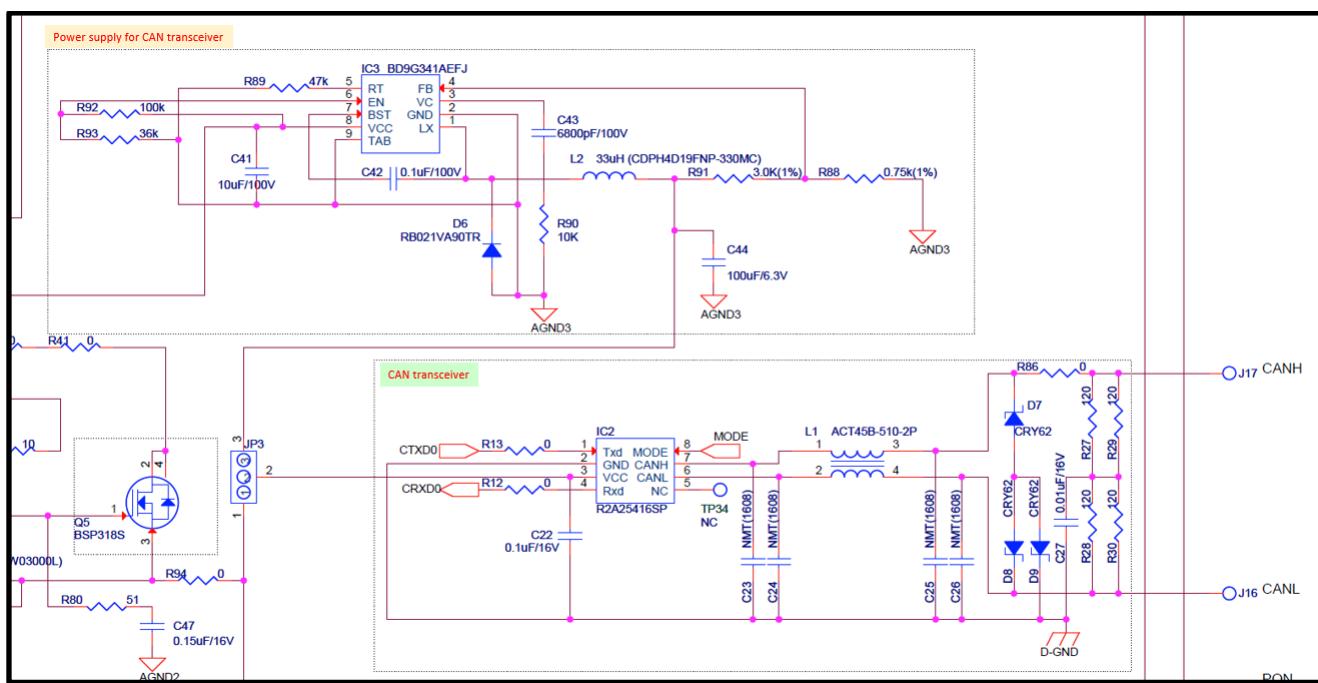
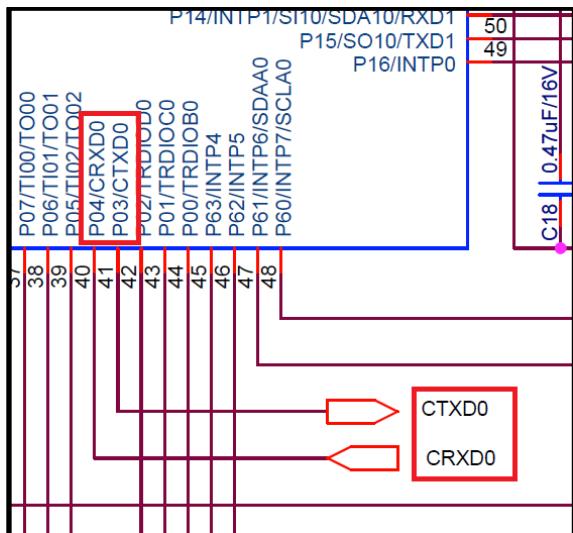
- ADC voltage measurement pins (AN0, AN1, AN2) are assigned for thermistor.



6.3.8 Communication line

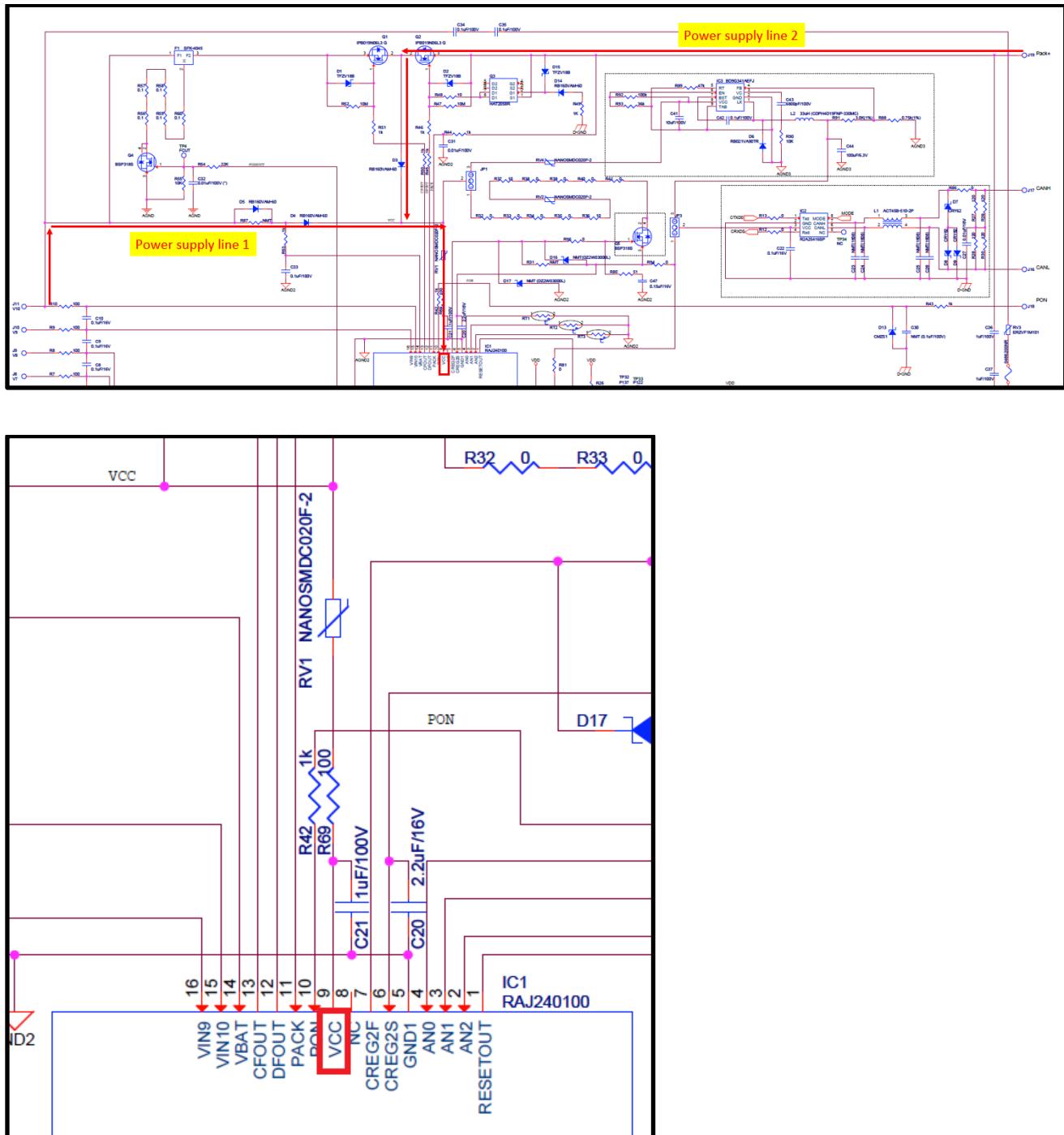
- RAJ240090 / RAJ240100 support 3 kinds of communication, SMBus, UART and CAN.
- For electrical over stress countermeasure, input 200 Ω , 330 Ω resistance, zener diode and capacitance are recommended in SMBus communication line.
- For UART communication, P14 and P15 pins have VDD output circuit, therefore RXD/TXD line pull up voltage should be the same as VDD.
- CAN communication is made possible by adding CAN transceiver externally. It is necessary to adapt external power supply for CAN transceiver.





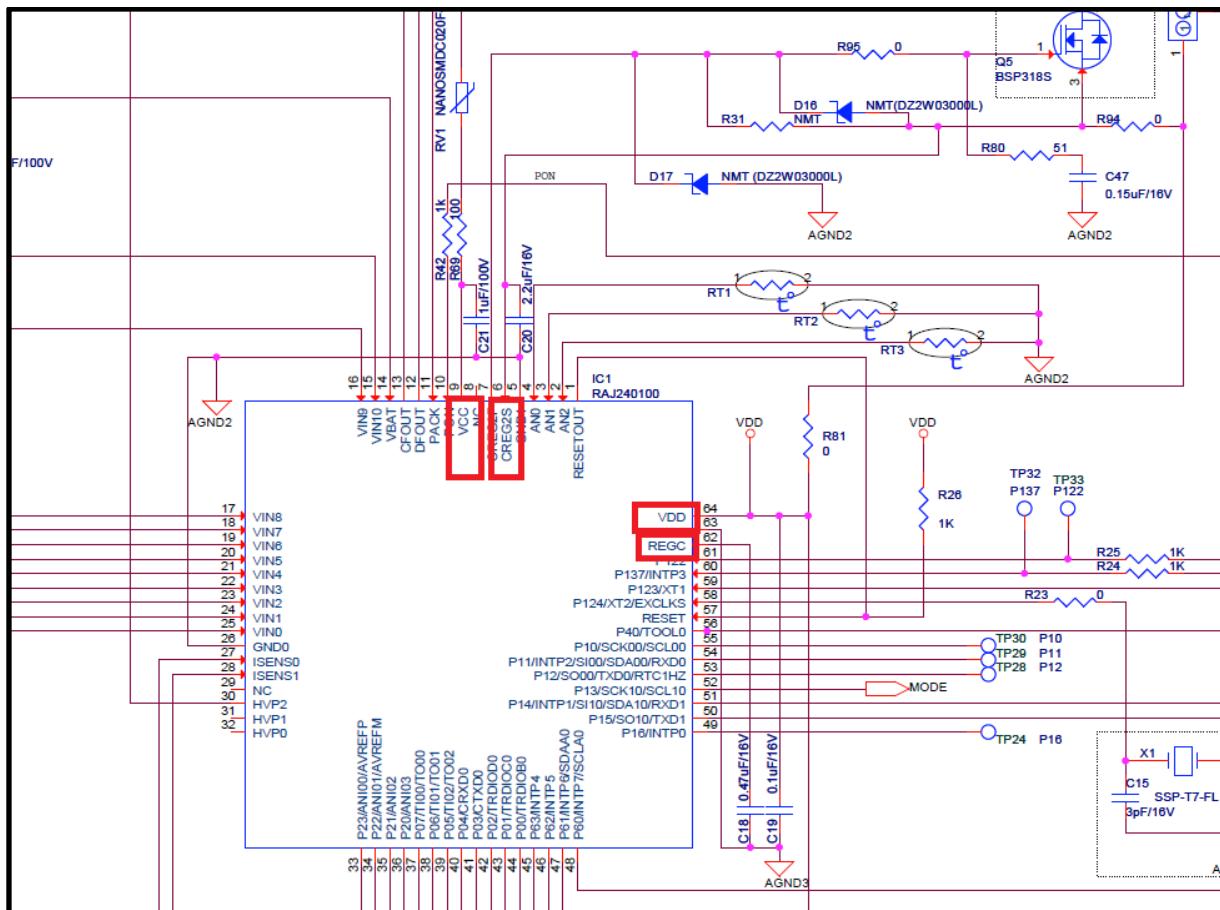
6.3.9 Power supply path

- Power is supplied to VCC through the following two paths depending on circumstance.
- Power supplied from battery side when fuse is blown. See power supply line 1.
- Higher output voltage from battery and charger is used as power supply. See power supply line 2.
- For protection of the VCC pin, it is recommended to add resistor and PTC for current limit.



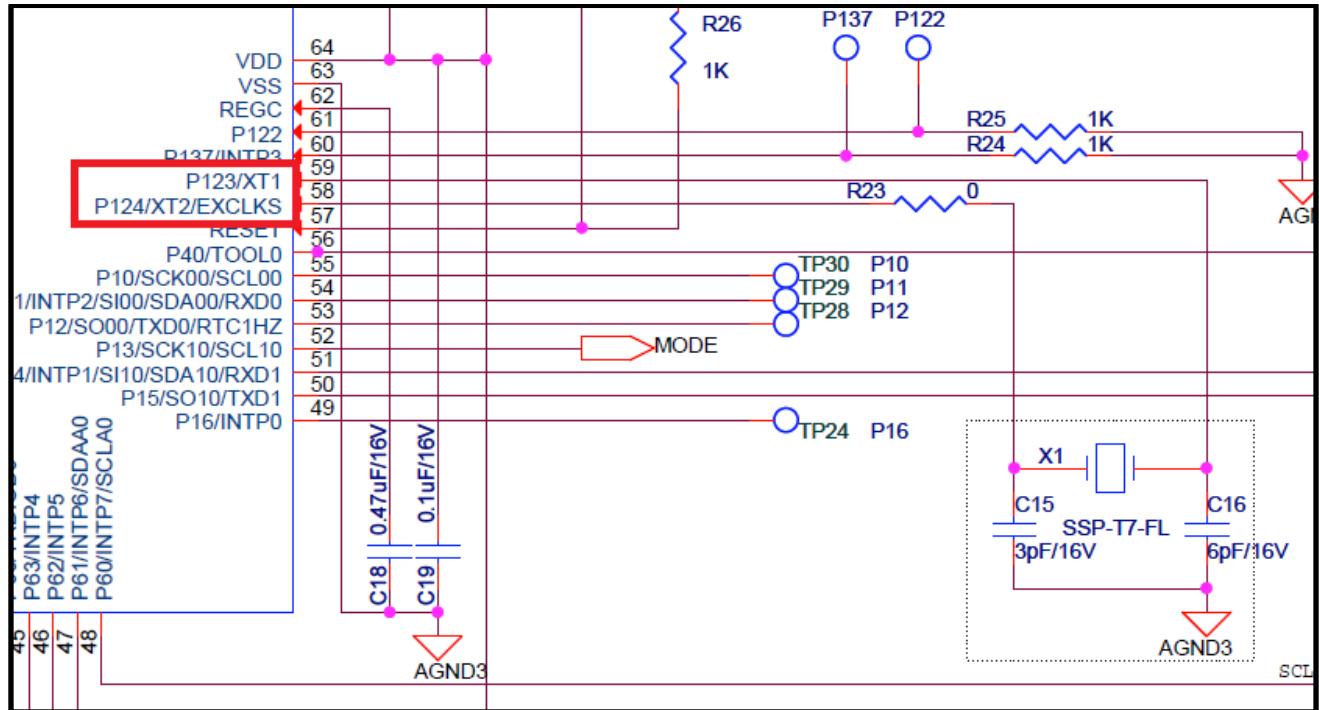
6.3.10 VCC, CREG2S, VDD and REGC capacitance

- The following decoupling capacitors must be located adjacent to each terminal.
- C21: VCC (1μF is recommended.)
- C20: CREG2 (2.2μF is recommended.)
- C19: VDD (0.1μF is recommended.)
- C18: REGC (0.47μF is recommended.)



6.3.11 Crystal oscillators port XT1 and XT2 for RTC

- RAJ240090 / RAJ240100 support RTC (Real time clock).
 - XT1 and XT2 are used for an external crystal oscillator's port. It is recommended to set the XT1 and XT2 line length as short as possible.
 - Shield pattern is necessary to XT1 line.



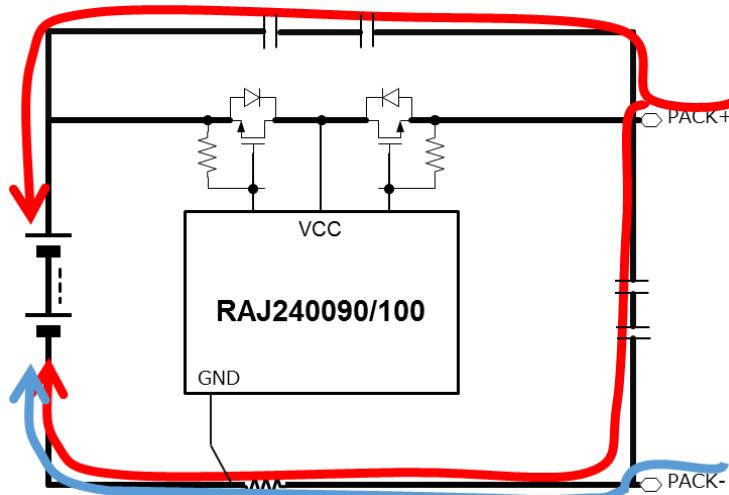
6.4 Layout Guidelines

6.4.1 Summary

- Large current patterns must be wide and short to minimize voltage drop and heat generation.
- Bypass capacitors must be mounted as close as possible to the device VCC / VBAT and GND pins to prevent erroneous operation due to noise from power supply.
- Capacitors for voltage regulators must be located close to regulator pins to ensure loop stability and ESD tolerance.
- All IC ground must be connected to the negative terminal of battery cells except ground for communication lines.
- Communication lines must be away from small signal current sense line to prevent the input signal from being disturbed by the incoming radiation noise.
- FGIC (RAJ240090 and RAJ240100) must be located away from any heat source (FET, current sense resistor and large current patterns) to minimize the influence of heat.

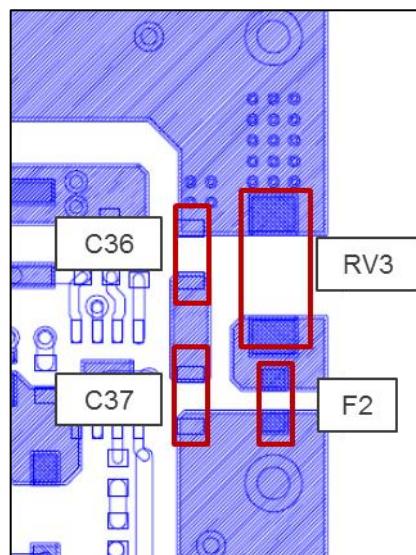
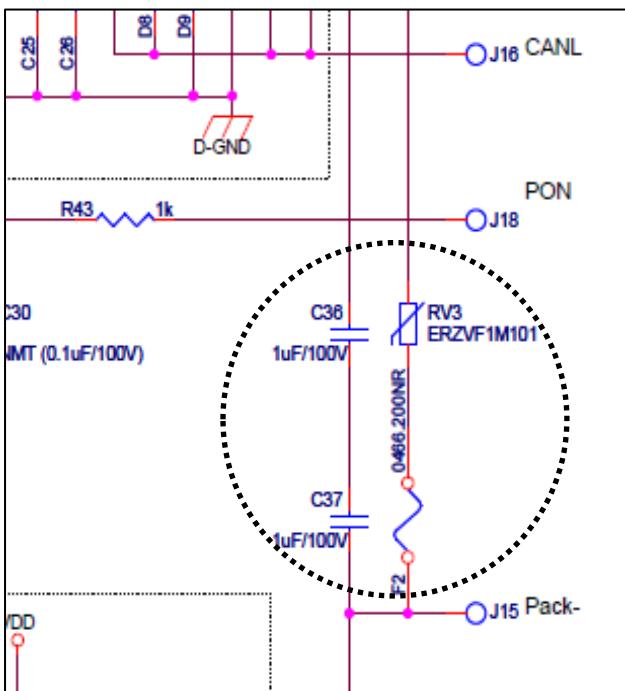
6.4.2 ESD protections on each terminal (basic policy)

- ESD on Pack+ terminal must be discharged to the top side of the cell or to Pack- terminal through a capacitor.
- ESD on Pack- terminal must be discharged to the GND side of the cell.
- ESD on communication terminals and other GPIOs must be discharged to the GND side of the cell via Pack- terminal.
- The noise from PACK+ or PACK- must be discharged to the battery cells so that it will not interfere with FGIC functions and measurements.



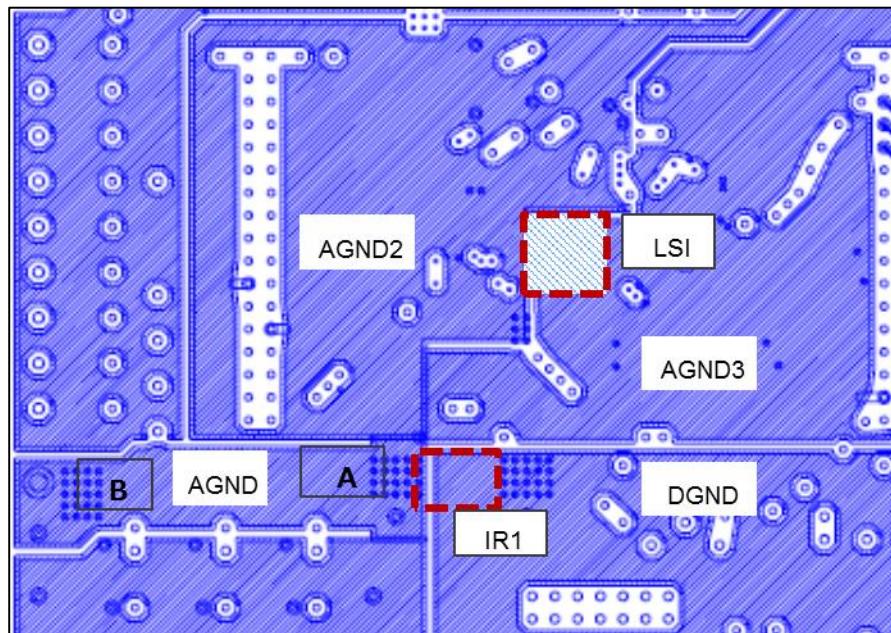
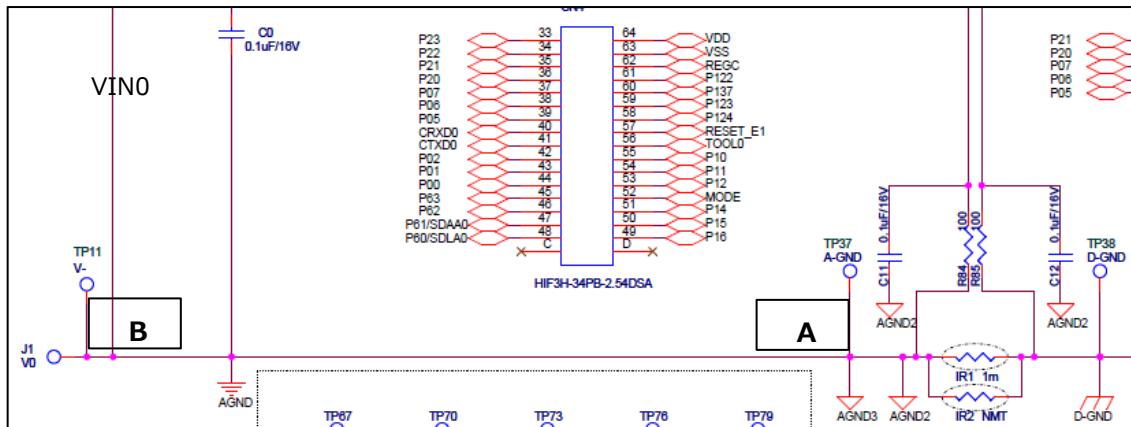
6.4.3 Pack+, Pack- (Noise protection element)

- A bypass capacitor must be placed between Pack+ and Pack-. (Countermeasure against ESD)
- A bypass capacitor must be located adjacent to Pack+, Pack-. (Minimize the ESD influence)
- Capacitors must be placed in series. (Countermeasure against short-circuit of capacitors)
- Don't use tantalum capacitor. (Tantalum capacitor can end up with short-circuited failure when damaged.)
- For the terminal protection against noise and overvoltage, It is recommended that it carries varistor or TVS diode .(RV3)
- It is recommended to add Fuse to prevent short circuit.(F2)
- C36, C37, RV3, F2 must be placed as short as possible between PACK + and PACK-. However, be careful not to narrow the distance between Pack + and Pack-.



6.4.4 GND connection

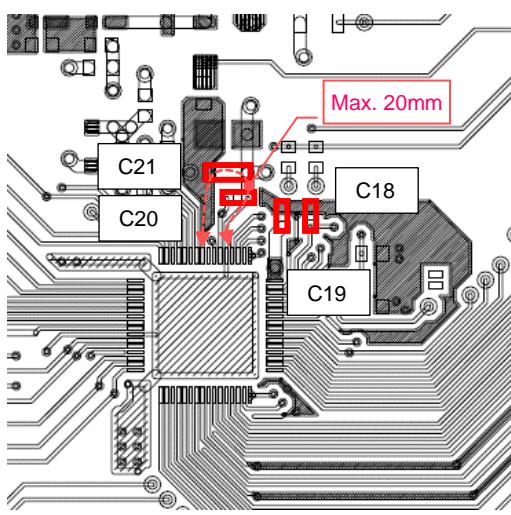
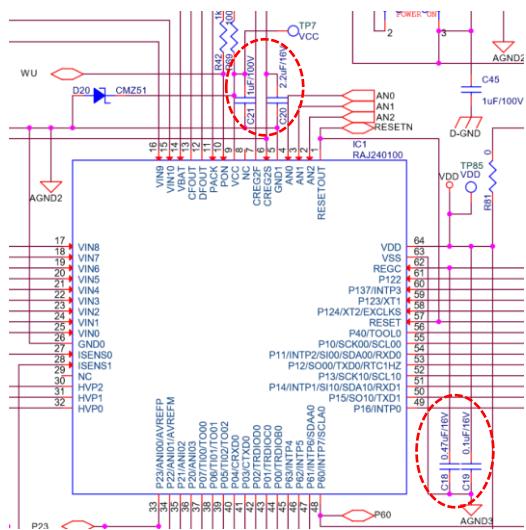
- Each analog GND of FGIC should be connected to the point (A) of current detection resistor of the cell side by the pattern with an adequate width. (Prevent potential variation by large current.)
- VIN0 should be connected near point V0 (B).
- The patterns between AGND, AGND2 and AGND3 must not be divided. (Keeping the GND potential of MCU and AFE equal)



<R> 6.4.5 Bypass capacitor between VCC/VDD/CREG2S/REGC and GND1/VSS

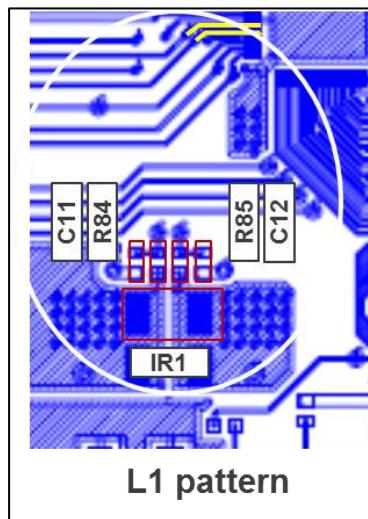
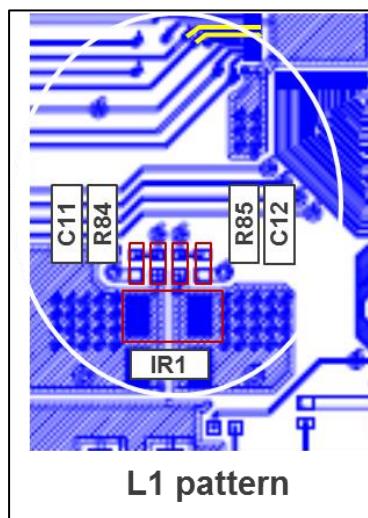
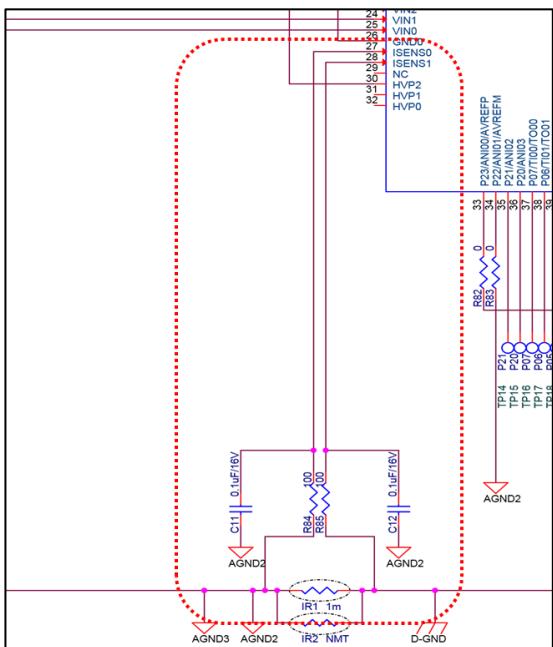
- The patterns between VCC/CREG2S pin and GND1 pin, and VDD/REGC pin and VSS pin, a bypass capacitor is connected and the path must be as short as possible. (Countermeasure for ESD)

The FGIC and bypass capacitor must be placed on the same side of the PCB without through-holes and the maximum loop length must be about 20mm.
- The lines to bypass capacitor must be wide and short. (To keep bypass capacitor effective in suppressing the potential variation.)



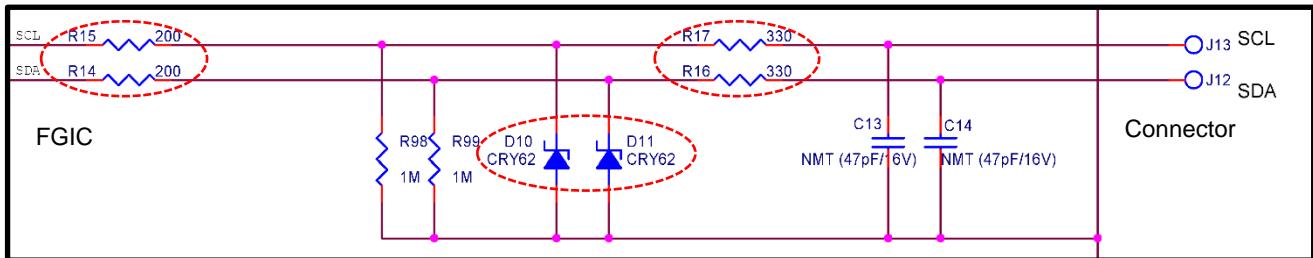
6.4.6 Current Monitor (ISENS0, ISENS1)

- Two lines from current sense resistor to ISENS0, ISENS1 must be the same in width and length, and in parallel with the same space between the two lines. (Prevent erroneous detections due to noise)
- LPF (100 ohm and 0.1 uF) and a shield pattern should be placed to ISENS0/1 lines. (Countermeasure against noise)



6.4.7 Communication line (SMBus)

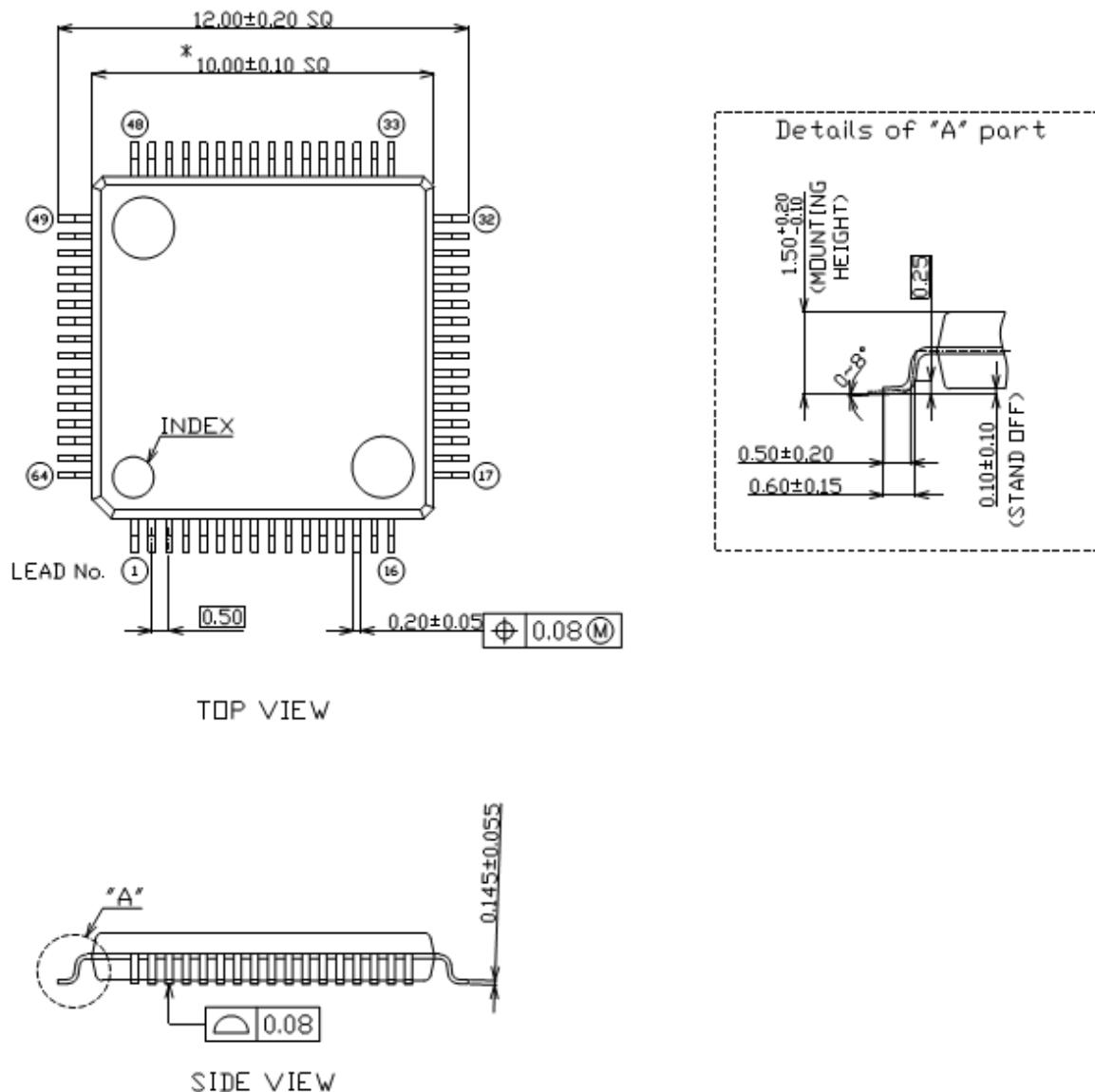
- SMBus lines must be equipped with zener diodes. And it is necessary to mount resistors on the side of FGIC and pack connector. (Zener diode and the resistor on the side of connector are for surge countermeasures, the resistor on the side of FGIC for noise countermeasure.)
- The resistor on the side of the FGIC must be located as close to the FGIC as possible



6.4.8 Unused Pins

- Unused pins are recommended to be connected to GND via resistors as ESD countermeasure. (Setting low output by software prevents the terminal from becoming indefinite).

7. PACKAGE DRAWINGS



Caution Package outline is tentative version. All parameters are expressed in millimeter.

REVISION HISTORY

Rev.	Date	Page	Description
1.00	Nov 27, 2017		First Version()
2.00	May 10, 2018	p.1	1. Introduction Added description of Battery cell voltage and temperature (AN port voltage) detection circuit. Updated description for Operating ambient temperature (extend operating ambient temperature range). Added Note.
		p.4	2. OUTLINE Added description of Battery cell voltage and temperature (AN port voltage) detection circuit Updated description for Operating ambient temperature (extend operating ambient temperature range)
		p.22	4. ELECTRICAL SPECIFICATIONS Updated to extend operating ambient temperature range from (-20degC ~ +85degC) to (-40degC ~ +85degC) in RAJ240100.
2.01	Jun 7, 2018	p.62	5. Detailed description Updated figure of AFE block diagram
2.02	Sep 7, 2018	p.1	1. Introduction Updated description for Operating ambient temperature (extend operating ambient temperature range).
		p.4	2. OUTLINE Deleted Notes.
		p.22	4. ELECTRICAL SPECIFICATIONS Add Remark. Updated to extend operating ambient temperature range from (-20degC ~ +85degC) to (-40degC ~ +85degC) in RAJ240090.
2.03	Jan 17, 2020	P26	Added Note for 4.3 Supply current characteristics
		P80	6.4.5 Bypass capacitor between VCC/VDD/CREG2S/REGC and GND1/VSS Added description about bypass capacitor pattern

General cautions for Handling Microprocessing Unit and Microcontroller Unit Products

The following usage notes are applicable to all Microprocessing unit and Microcontroller unit products from Renesas. For detailed usage notes on the products covered by this document, refer to the relevant sections of the document as well as any technical updates that have been issued for the products.

1. Handling of Unused Pins

Handle unused pins in accordance with the directions given under Handling of Unused Pins in the manual.

- The input pins of CMOS products are generally in the high-impedance state. In operation with an unused pin in the open-circuit state, extra electromagnetic noise is induced in the vicinity of LSI, an associated shoot-through current flows internally, and malfunctions occur due to the false recognition of the pin state as an input signal become possible. Unused pins should be handled as described under Handling of Unused Pins in the manual.

2. Processing at Power-on Processing during Power-on

The state of the product is undefined at the moment when power is supplied.

- The states of internal circuits in the LSI are indeterminate undetermined and the states of register settings and pins are undefined at the moment when power is supplied.
In a finished product where the reset signal is applied to the external reset pin, the states state of pins are not guaranteed from the moment when power is supplied until the reset process is completed.

In a similar way, the states of pins in a product that is reset by an on-chip power-on reset function are not guaranteed from the moment when power is supplied until the power reaches the level at which resetting has been specified.

3. Prohibition of Access to Reserved Addresses

Access to reserved addresses is prohibited.

- The reserved addresses are provided for possible future expansion of functions only. Do not access these addresses; the correct operation of LSI will not guaranteed if they are accessed.

4. Clock Signals

After applying a reset, the reset line will only be released after the operating clock signal has become stable. When switching the clock signal during program execution, wait until the target clock signal has stabilized.

- When the clock signal is generated with an external resonator (or from an external oscillator) during a reset, ensure that the reset line is only released after full stabilization of the clock signal. Moreover, when switching to a clock signal produced with an external resonator (or by an external oscillator) while program execution is in progress, wait until the target clock signal is stable.

5. Differences between Products

Before changing from one product to another, i.e. to a product with a different part number, confirm that the change will not lead to problems.

- The characteristics of Microprocessing unit or Microcontroller unit products in the same group but having a different part number may differ in terms of internal memory capacity, layout pattern, and other factors, which can affect the ranges of electrical characteristics, such as characteristic values, operating margins, immunity to noise, and amount of radiated noise. When changing to a product with a different part number, system-evaluation test needs to be implemented for the given product.

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