66.70 Estructura del Computador

Trabajo Práctico

2do Cuatrimestre 2012

Diseño de la lógica de un sistema de semáforos

Primer entrega: "Solución cableada"

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Índice

1. Introducción

Se ha solicitado desarrollar el sistema para el funcionamiento nocturno del par de semáforos que se encuentran en la esquina de una estación de Bomberos. A continuación se describe cómo debe ser el funcionamiento de los mismos:

- Ambos semáforos se encontrarán por defecto en un estado en el cual la luz amarilla se enciende de forma intermitente (1 seg. prendida – 1 seg. apagada);
- Cuando un peatón desea cruzar, debe pulsar el botón que se encuentra debajo del semáforo. En tal caso, los semáforos seguirán la siguiente secuencia:

    - Por 5 segundos se mantendrá encendida la luz amarilla en el semáforo 1, y se encenderá la luz roja en el semáforo 2.
    - Luego, se encenderá la luz verde del semáforo 1 dejando la luz roja en el semáforo 2. Se permanecerá en este estado por una duración de 30 segundos.
    - Transcurrido ese período, se encenderá la luz amarilla del semáforo 1 mientras que el semáforo 2 continua con la luz roja encendida.
    - Una vez transcurridos 5 segundos, se enciende la luz roja del semáforo 1 mientras que se pone en amarillo el semáforo 2. Se quedará en este estado por 5 segundos.
    - Ahora deberá permanecer el semáforo 1 en rojo mientras que el semáforo 2 prende únicamente la luz verde, quedando en este estado por otros 30 segundos.
    - Cumplido dicho tiempo, se procede a encender la luz amarilla exclusivamente en el semáforo 2, mientras que en el semáforo 1 se mantiene encendida la roja.
    - Luego de 5 segundos, se procede a volver al estado por defecto, en el cual ambos semáforos encienden de forma intermitente sus luces amarillas.

- En caso de volverse a presionar el botón para el cruce de los peatones mientras se ejecuta la secuencia anterior, éste no tiene ningún efecto.
- Existe también un botón que es utilizado al momento que deben salir los camiones de Bomberos. Cuando este es presionado, ambos semáforos deben pasar a encender su luz roja y su luz amarilla simultáneamente. Debido a que el tiempo requerido para la salida de los camiones no es conocido, se debe esperar a que este botón sea pulsado nuevamente para volver al estado por defecto de los semáforos (sin importar en qué estados se encontraban previamente).
- Para tener referencia temporal, existe una señal de reloj de 32kHz que puede ser utilizada en cada uno de los semáforos.

Este primer informe se limita solamente a la búsqueda y desarrollo de una solución cableada, es decir, mediante el uso de compuertas lógicas, flip-flops y demás componentes electrónicos cuyas hojas de datos se encuentran adjuntas en el *Apéndice A*.

2. Diagrama de estados

Para iniciar el camino hacia una solución cableada que cumpla con los requerimientos de forma eficiente, comenzaremos realizando el diagrama de estados pertinente. Paso previo se deben establecer las variables de entrada y de salida principales del sistema, las cuales se muestran en la *Tabla 2.1*.

Tipo de variable	Especificación	ID
Entrada	Botón de cruce del peatón	BP
	Botón de salida de camión de Bomberos	BB
	Timer de 1 segundo	T1
	Timer de 5 segundos	T5
	Timer de 30 segundos	T30
Salida	Luz Roja del Semáforo 1	R1
	Luz Amarilla del Semáforo 1	A1
	Luz Verde del Semáforo 1	V1
	Luz Roja del Semáforo 2	R2
	Luz Amarilla del Semáforo 2	A2
	Luz Verde del Semáforo 2	V2

Tabla 2.1 – *Definición de variables de entrada y salida del sistema.*

Hecho esto pasamos a armar el diagrama de estados (*Figura 2.1*), el cual, como puede apreciarse, se encuentra dividido en tres módulos, siendo estos simplemente una reagrupación de estados correspondientes a cierto evento provocado por las entradas. Para evitar una complejidad innecesaria de dicho diagrama se ha evitado colocar el caso en el que ambos botones son presionados en el mismo instante, situación en la que predominará siempre la secuencia de los bomberos. Es decir, cualquiera sea la secuencia en la que se esté, siempre que se presione el botón de salida del camión de los Bomberos se interrumpirá el estado actual para pasar a ejecutar la secuencia del *Módulo C*.

Nótese que en el extremo inferior derecho de la *Figura 2.1* se especifica la codificación prestablecida para el código de estados, donde cada luz es representada por un bit.

A lo largo del desarrollo se mantendrá esta modularización propuesta en el diagrama ya que esto nos permite reducir de forma considerable la cantidad de componentes electrónicos a utilizar, evitándonos el hecho de realizar una única tabla de transiciones con numerosas variables de entrada y salida. En los siguientes apartados se profundizará acerca de esta decisión de diseño, como así también se hará una detallada explicación de la lógica planteada.

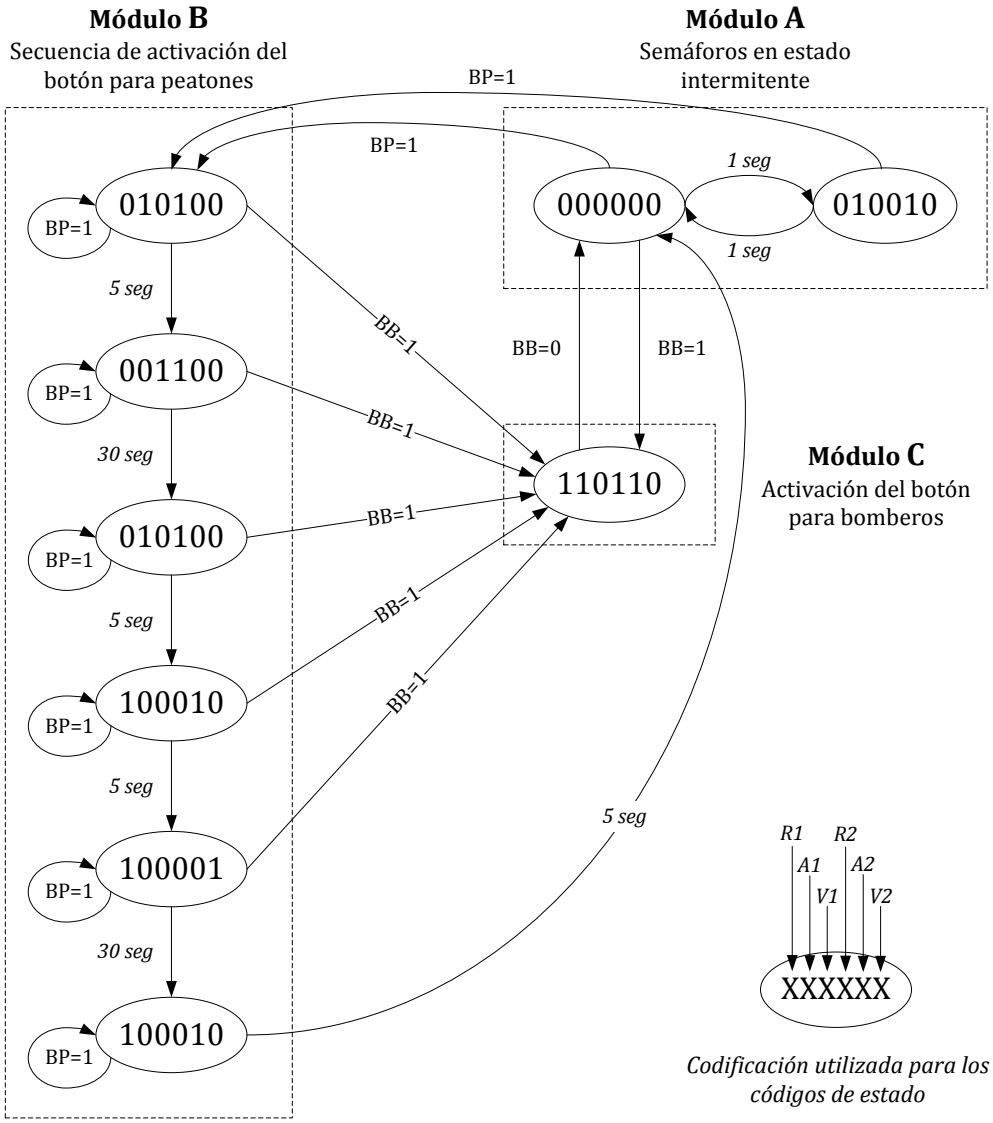


Figura 2.1 – *Diagrama de estados correspondiente al sistema de semáforo.*

3. Diagramas en bloque

Como se ha adelantado en la sección anterior, se ha decidido llevar a cabo una simplificación de manera tal de aprovechar el funcionamiento de componentes electrónicos como lo son los multiplexores y demultiplexores, de manera tal de conseguir mayor simplicidad en el desarrollo de la solución.

En la *Figura 3.1* se muestra el diagrama en bloques general propuesto para el sistema.

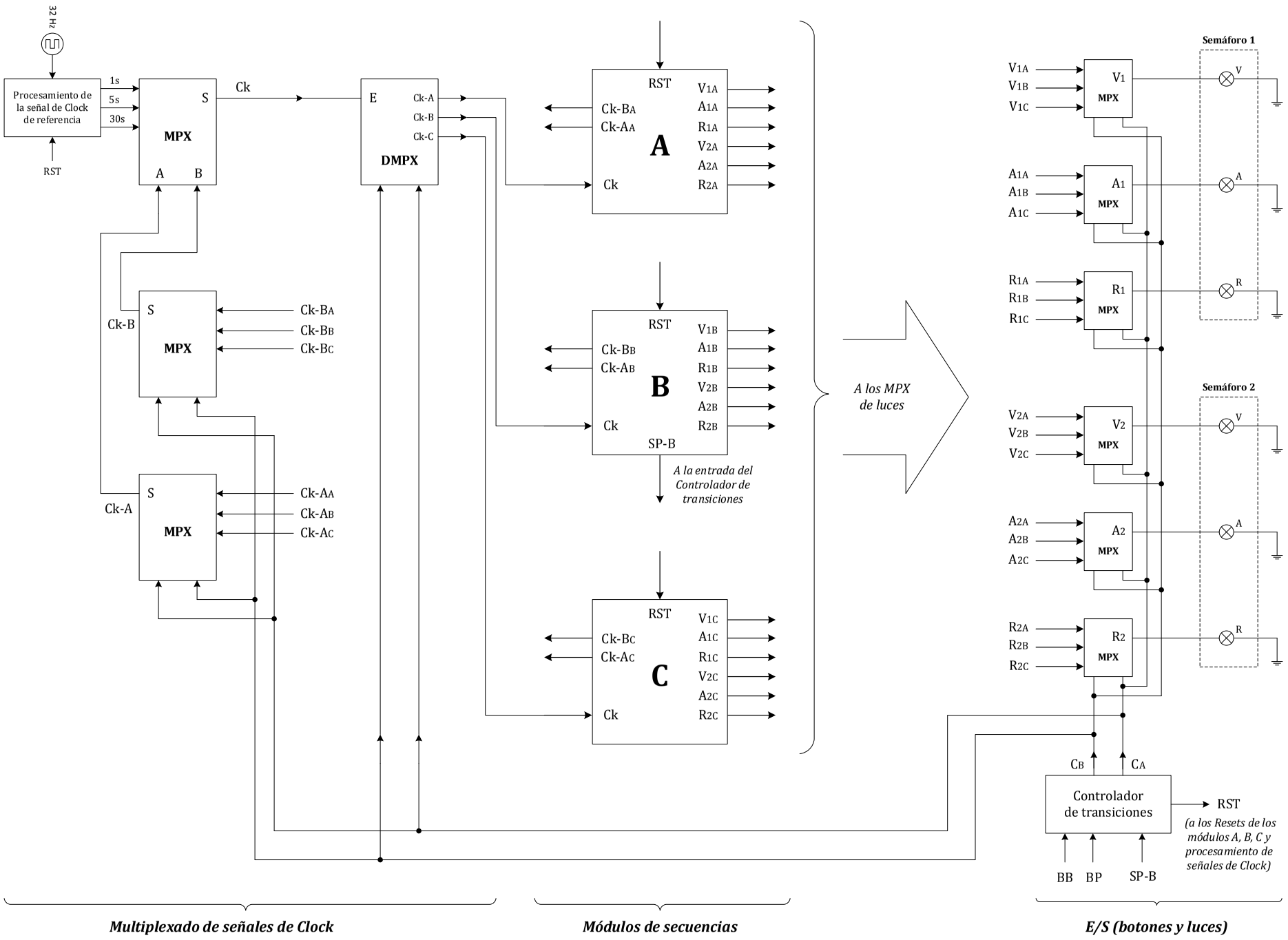


Figura 3.1 – *Diagrama en bloques general del sistema.*

Nótense primeramente los tres módulos que se encuentran en el centro de este diagrama (módulos *A, B* y *C*). Cada uno de ellos representa una de las secuencias existentes en el sistema según lo definido en el diagrama de estados. En este esquema no es de interés qué es lo que ocurre dentro de los mencionados módulos, sino que simplemente se estableció que estos deben constar de un conjunto de entradas y salidas, tal como si fueran cajas negras.

Por un lado, se encuentran seis salidas correspondientes a las seis luces de los semáforos que deben controlarse. Cada módulo pondrá un 1 ó un 0 en cada una de estas salidas según cuales sean las luces que se desean activar en cada estado interno de las secuencias.

Por otro lado, una de las entradas se corresponde con el clock (*Ck*). A través de ella ingresará la señal de clock utilizada en las unidades. Además, cada módulo posee dos salidas relacionadas con esta: *Ck-A* y *Ck-B.* Como bien se pudo observar en el diagrama de estados de la *Figura 2.1*, hay tres tipos de señales de clock: *T1*, *T5* y *T30*. Cada módulo puede utilizar cualesquiera de estas, como es el caso del *Módulo B*. Este último hace uso de todas ellas en distintos momentos de la secuencia. Mediante las dos salidas antes nombradas, la unidad es capaz de seleccionar cual de los timer debe ingresar por la entrada *Ck*. En la *Tabla 3.1* se encuentran los estados que deben tener estas salidas para lograr dicha selección de tiempos.

Ck-B	Ck-A	Timer en entrada Ck
0	0	T1
0	1	T5
1	0	T30
1	1	-

Tabla 3.1 – *Definición de las salidas Ck-B y Ck-A para obtener distintos clocks a la entrada.*

Asimismo, cada módulo cuenta con una entrada de reset (RST), la cual, al ser activada con un 1, resetea la secuencia volviéndola a sus estados iniciales respectivos.

Por último, el lector habrá notado que el *Módulo B* cuenta con una salida adicional denominada *SP-B*, en alusión a *Scape B*. Como se vio en el diagrama de estados, al finalizar la secuencia *B,* se debe regresar automáticamente al estado por defecto definido por la secuencia del *Módulo A*. Esta salida es entonces el medio por el cual la unidad hará aviso al circuito externo de que ha finalizado su secuencia y que es hora de volver al estado por defecto.

Veamos ahora como es que se encuentra conformado lo que resta del sistema.

Como cada módulo debe ser capaz de activar o desactivar las mismas luces, se ha decidido hacer uso de multiplexores que, de acuerdo al módulo *Controlador de transiciones* se conmute cual de las señales de salidas de los módulos de secuencias irá a parar hacia los semáforos. Este último es el encargado de censar los estados de los botones, y conforme a ello decidir a que secuencia se debe desplazar el circuito. Es decir, acorde a los botones de entrada *BP* y *BB*, sumado a la ya mencionada *SP-B*, reaccionará estableciendo un estado sobre sus salidas C_A y C_B. El conjunto de estos dos conforman el código que representa a qué módulo se le debe dar la orden de ser ejecutado. En la *Tabla 3.2* se muestra la correspondencia de estos estados con el módulo a ejecutar.

C_B	C_A	**Módulo ejecutado**
0	0	A
0	1	B
1	0	C
1	1	-

Tabla 3.2 – *Correspondencia de los estados de las salidas C_A y C_B con las secuencias a ejecutar.*

Estas dos mismas señales, C_A y C_B, se distribuyen a lo largo de dos multiplexores más, encontrándose estos a la izquierda de la *Figura 3.1*. De acuerdo a estas entradas, los multiplexores dejarán pasar la señal de los *Ck-A* y *Ck-B* del módulo de secuencia activo en ese momento hacia un tercer multiplexor el cual recibe a sus entradas las tres señales de clock (T1, T5 y T30). Con esto se logra que el módulo de la secuencia activa elija que señal de clock utilizará en cualquier tramo de la secuencia.

Por último, un demultiplexor recibe esa señal seleccionada por la secuencia, y, de acuerdo a las entradas C_A y C_B se encarga de desviar dicha señal solamente hacia el módulo activo. La acción de este dispositivo podría obviarse pero al ser sumado al sistema permite ahorrar energía ya que limita la señal de clock al módulo que se encuentra en funcionamiento, haciendo que los demás módulos permanezcan en un estado de detención total.

En los siguientes apartados se profundizará cada uno de los módulos ya nombrados, haciendo énfasis en sus esquemas circuitales.

3.1. Controlador de transiciones

Ciertamente, este es el módulo responsable de la coordinación de las secuencias de acuerdo a como sean presionados los botones de entrada *BB* y *BP*. En este módulo se considera a *SP-B* (el bit de escape del *Módulo B*) como una entrada. Por una cuestión de prolijidad acortaremos únicamente para el desarrollo de este apartado la denominación de *SP-B* a *SP*. Acorde a estas entradas se determinarán los estados de las salidas a saber: C_B, C_A y *RST*. En la *Tabla 3.1.1* se encuentra la tabla de estados correspondiente. Nótese que en lugar de *BB* y *BP* se han utilizado las notaciónes Q_{BB} *y* Q_{BP} respectivamente. Permítasenos por un momento omitir ese detalle, el cual será expuesto líneas más abajo.

En la tabla de estados mencionada, de acuerdo al diagrama de estados presentado inicialmente y teniendo en cuenta la *Tabla 3.2,* se han dispuesto los distintos valores que deben poseer las salidas del módulo.

SP	Q_{BB}	Q_{BP}	C_B	C_A	RST
0	0	0	0	0	0
0	0	1	0	1	0
0	1	0	1	0	1
0	1	1	1	0	1
1	0	0	0	0	1
1	0	1	0	0	1
1	1	0	1	0	1
1	1	1	1	0	1

Tabla 3.1.1 – *Correspondencia de los estados de las salidas C_A y C_B con las secuencias a ejecutar.*

Hecho esto se procedió con la simplificación de la lógica requerida. Para esto se han utilizado los mapas de Karnaugh. En la *Figura 3.1.1* se muestran los mapas de Karnaugh correspondientes a las salidas C_B, C_A y *RST* de la *Tabla 3.1.1.* Tanto por 1s como por 0s se obtienen exactamente los mismos resultados. De esta manera, se consigue que el controlador de transiciones logre dirigir las transiciones entre estados.

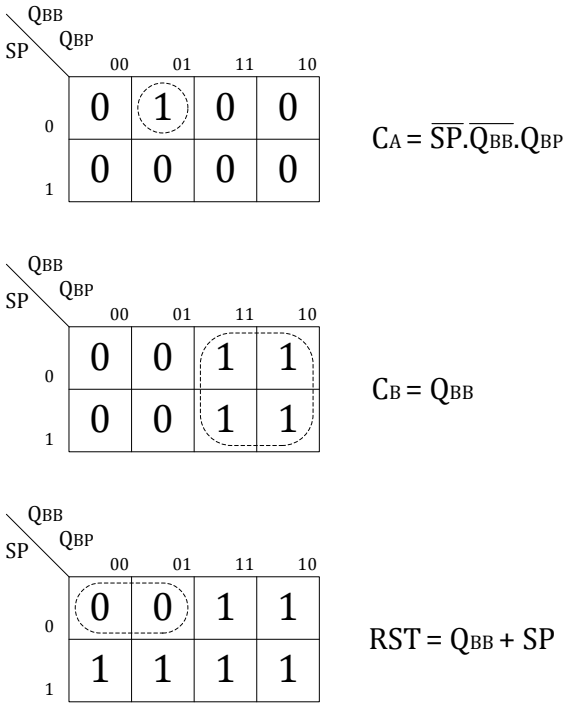


Figura 3.1.1 – *Mapas de Karnaugh correspondientes a las salidas C_A C_B y RST de la Tabla 3.1.1.*

En las especificaciones del sistema se precisaba que el botón *BB* debía presionarse para que los semáforos enciendan las luces de aviso de la salida de los camiones de los bomberos, pero requería que para finalizar dicha secuencia se volviera a presionar el mismo botón. Para lograr este comportamiento no fue necesario realizar ninguna tabla ya que sabemos que los flip-flops tipo T poseen un comportamiento que nos permiten solventar esta problemática. Tal como se muestra en la *Figura 3.1.1* el botón *BB* se encuentra directamente conectado a la entrada de clock de un FF-JK que, de la manera en que enchufado, se comporta como un FF-T. De esta manera, en la salida Q_{BB} del FF tendremos un 1 al pulsar el botón y un 0 al volver a pulsarlo. Aquí hace acto de presencia la antes mencionada Q_{BB}, que tal como puede comprenderse ahora, es la que realmente da cuenta del estado del pulsador de entrada *BB*.

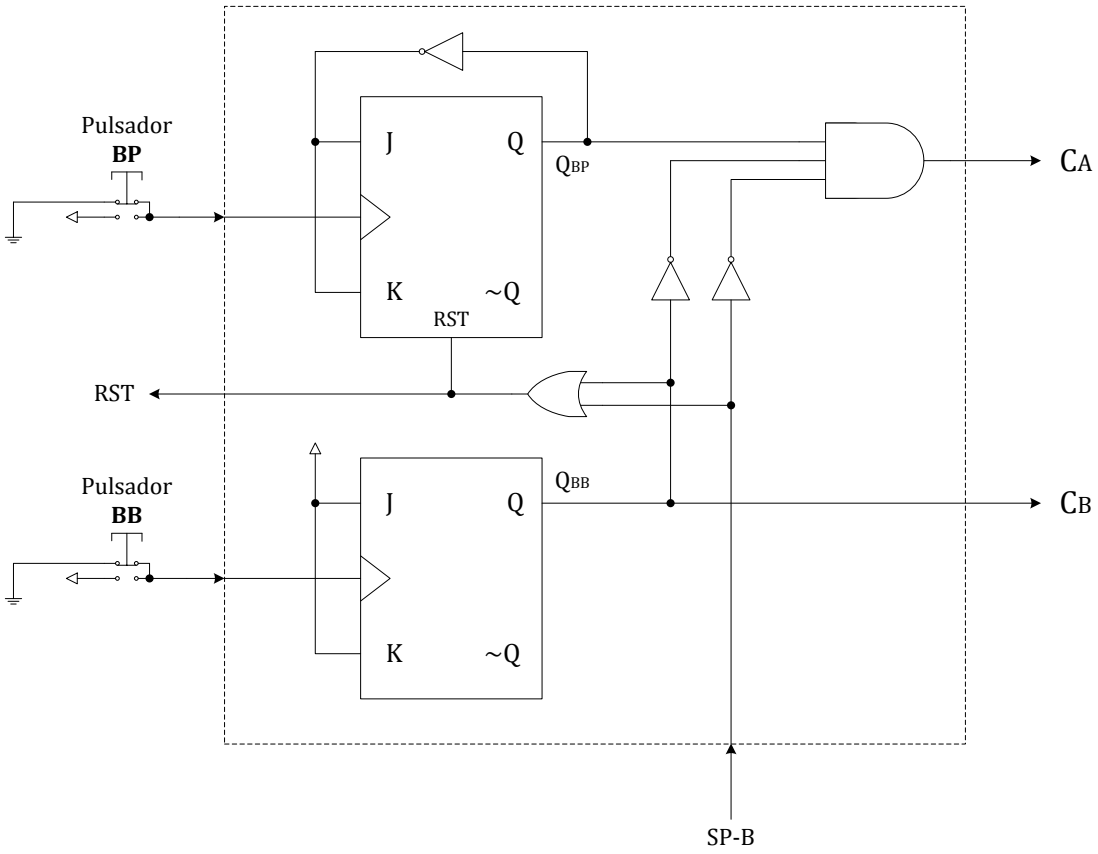


Figura 3.1.1 – *Esquema circuital del módulo Controlador de transiciones.*

En el caso del botón BP, se ha especificado que si al presionarse ya nos encontrábamos en la secuencia *B*, este no debería provocar efecto alguno sobre el sistema. Para lograr ello nuevamente se ha utilizado un FF-JK en configuración FF-T pero con una pequeña diferencia: entre la salida y la entrada del FF se ha colocado una compuerta negadora. Inicialmente la salida se encuentra inactiva, es decir, en 0. Por lo tanto, a causa de la compuerta negadora que se encuentra

entre Q_{BP} y las entradas *J* y *K*, en estas últimas tendremos un 1. Si se presiona el botón *BP*, el cual se encuentra conectado a la entrada de clock del FF, la salida pasará a entregar un 1 (y se iniciará la secuencia de cruce del peatón). De esta manera, las entradas *J* y *K* pasarán a tener un 0. Así, si se vuelve a presionar *BP*, no habrá cambios a la salida. Además, mediante el mismo reset (RST) que se utiliza para resetear las secuencias de los módulos, se resetea a este FF, de manera que únicamente cuando no nos encontramos en la secuencia del *Módulo B* surte efecto el presionar el pulsador *BP*. Nuevamente, aquí aparece la antes nombrada entrada Q_{BP}, la cual, a nuestros fines es la que realmente da cuenta del estado del pulsador de entrada *BP*.

3.2. Procesamiento de la señal de referencia

A partir de una señal de 32Hz que se posee como referencia en ambos semáforos, se usaron 5 FF-JK para dividir su frecuencia hasta 1Hz. En la *Figura 3.2.1* se muestra el diagrama circuital de este.

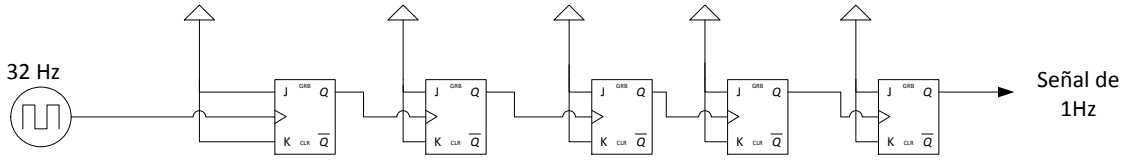


Figura 3.2.1 – *Esquema circuital del timer de 1 segundo (T1).*

Para el timer de 5 segundos se uso un contador (de 0 a 4) que envía una señal cada vez que se pasa por el 0, teniendo como entrada el anterior. El circuito correspondiente se muestra en la *Figura 3.2.2.*

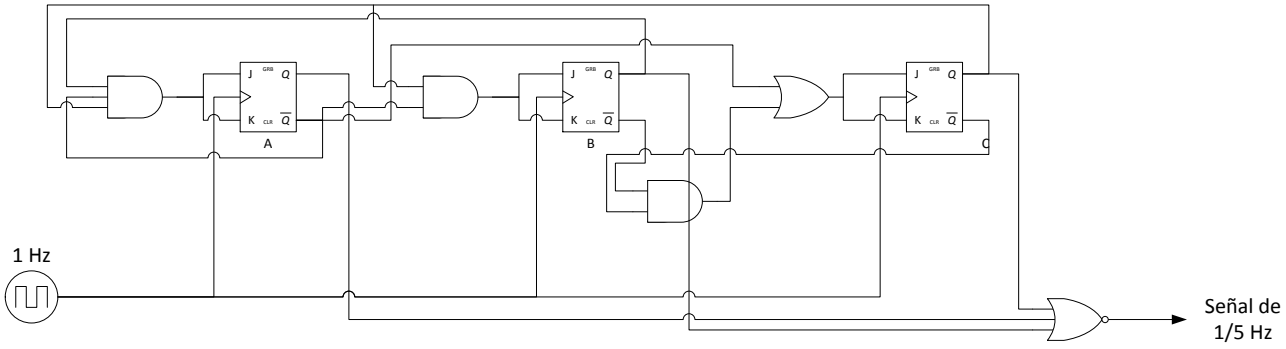


Figura 3.2.2 – *Esquema circuital del timer de 5 segundos (T5).*

Por último, para lograr un pulso cada 30 segundos se uso un FF-JK para dividir la frecuencia de la señal del timer de 5 segundos y un contador (de 0 a 2) que envía una señal cada vez que se pasa por el 0. El circuito correspondiente se muestra en la *Figura 3.2.3.*

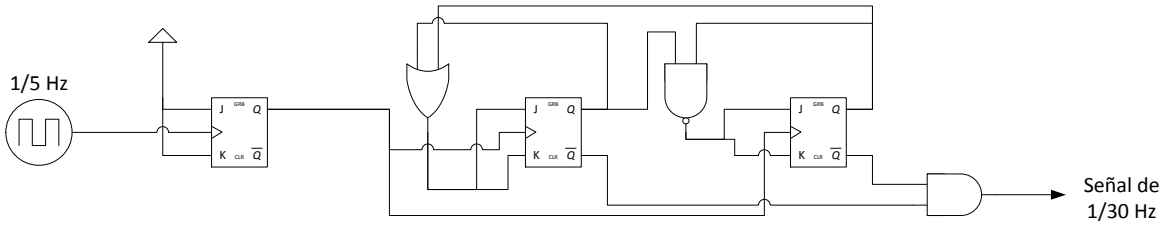


Figura 3.2.3 – *Esquema circuital del timer de 30 segundos (T30).*

No se ha especificado en los circuitos anteriormente mostrados, pero a cada uno de los flip-flops involucrados se les ha conectado a sus entradas de reset el RST de salida del *Módulo del Controlador de transiciones.* El motivo de esto reside en evitar desincronizaciones que pueden aparecer oportunamente en el desenlace de las distintas secuencias.

3.3. Módulo de la *Secuencia A*

Según el diagrama de estados de la *Figura 2.1*, necesitamos hacer que la luz amarilla sea intermitente con un intervalo entre apagado y encendido de 1 segundo. Esto se consigue utilizando un FF-JK funcionando como un FF-T debido a que, a cada pulso de clock deseamos que la salida cambie de estado de 0 a 1 y viceversa. Por lo tanto, solamente las salidas que se dirigen a las luces amarillas se encuentran conectadas a la salida del FF-JK, mientras que las demás salidas correspondientes a las luces restantes se encuentran conectadas a masa, con el fin de establecer un 0 sobre ellas. Este conexionado se muestra en la *Figura 3.3.1*.

Para obtener sobre la entrada *Ck* el pulso de *T1*, se han conectado a masa las salidas Ck-A_C y Ck-B_C. Finalmente, la entrada RST se conecta directamente al FF-JK para resetear la secuencia.

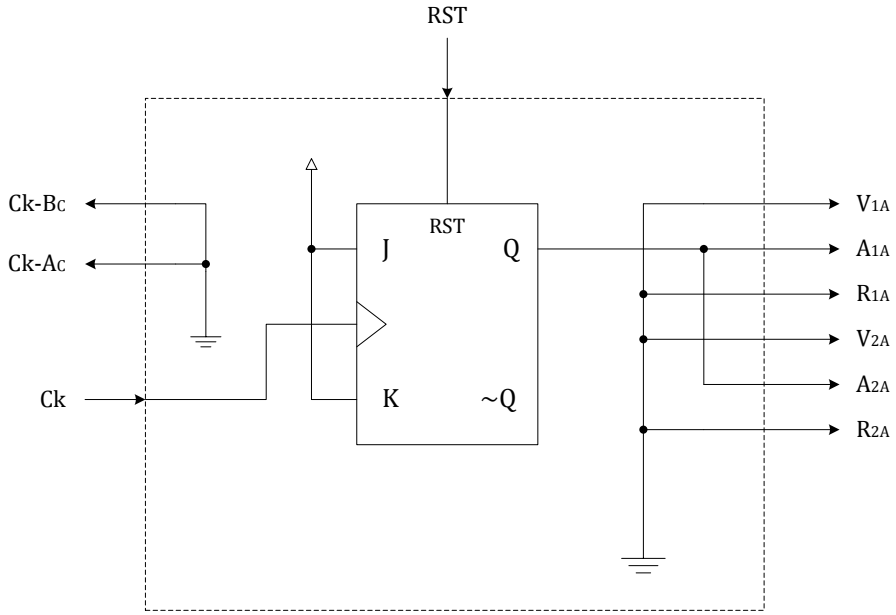


Figura 3.3.1 – *Esquema circuital del módulo de la Secuencia A.*

3.4. Módulo de la *Secuencia B*

Pasaremos ahora a desarrollar la secuencia del *Módulo B*, que sin duda alguna es la mas extensa y compleja de todas. Como decisión de diseño se ha optado por realizar un contador de 0 a 6, de manera de que cada cuenta represente cierto estado de las salidas de las luces. Es decir, las luces que se enciendan dependerán de la cuenta. Una vez que se llega a la última cuenta, se setea en 1 la salida *SP-B*, de forma tal de volver a la secuencia por defecto del sistema al finalizar la secuencia particular del *Módulo B*. Para el contador se han utilizado tres FF-JK. La tabla de transiciones junto con la tabla de estados de las luces se encuentra conjuntamente en la *Tabla 3.4.1.*

Q_2^n	Q_1^n	Q_0^n	Q_2^{n+1}	Q_1^{n+1}	Q_0^{n+1}	R_{1A}	A_{1A}	V_{1A}	R_{2A}	A_{2A}	V_{2A}	SP	J_2	K_2	J_1	K_1	J_0	K_0
0	0	0	0	0	1	0	1	0	1	0	0	0	0	X	0	X	1	X
0	0	1	0	1	0	0	0	1	1	0	0	0	0	X	1	X	X	1
0	1	0	0	1	1	0	1	0	1	0	0	0	0	X	X	0	1	X
0	1	1	1	0	0	1	0	0	0	1	0	0	1	X	X	1	X	1
1	0	0	1	0	1	1	0	0	0	0	1	0	X	0	0	X	1	X
1	0	1	1	1	0	1	0	0	0	1	0	0	X	0	1	X	X	1
1	1	0	0	0	0	X	X	X	X	X	X	1	X	1	X	1	0	X
1	1	1	0	0	0	X	X	X	X	X	X	0	X	1	X	1	X	1

Tabla 3.4.1 – *Tabla de transiciones del contador en conjunto con la tabla de estados de las luces de salida.*

Hecha la tabla de transiciones, pasaremos a armar los mapas de Karnaugh de las entradas de los FF-JK. Dichos mapas se muestran en la *Figura 3.4.1.*

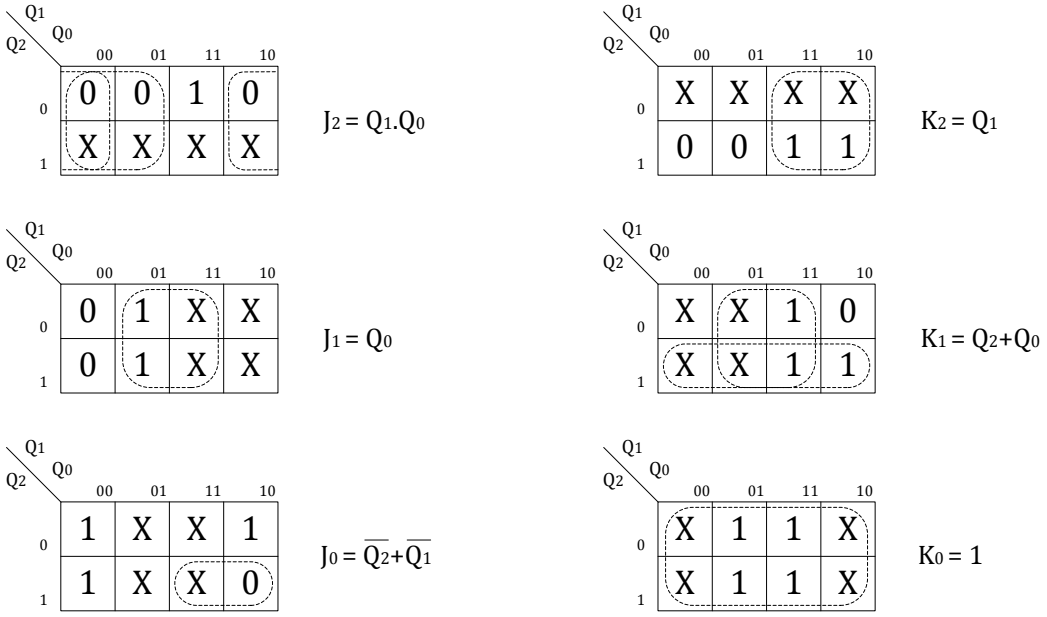


Figura 3.4.1 – *Mapas de Karnaugh correspondientes a las entradas J y K de la Tabla 3.4.1.*

Luego se deben realizar los mapas de Karnaugh de las salidas correspondientes a las luces y a la salida de escape *SP-B*. Estos se muestran en la *Figura 3.4.2*.

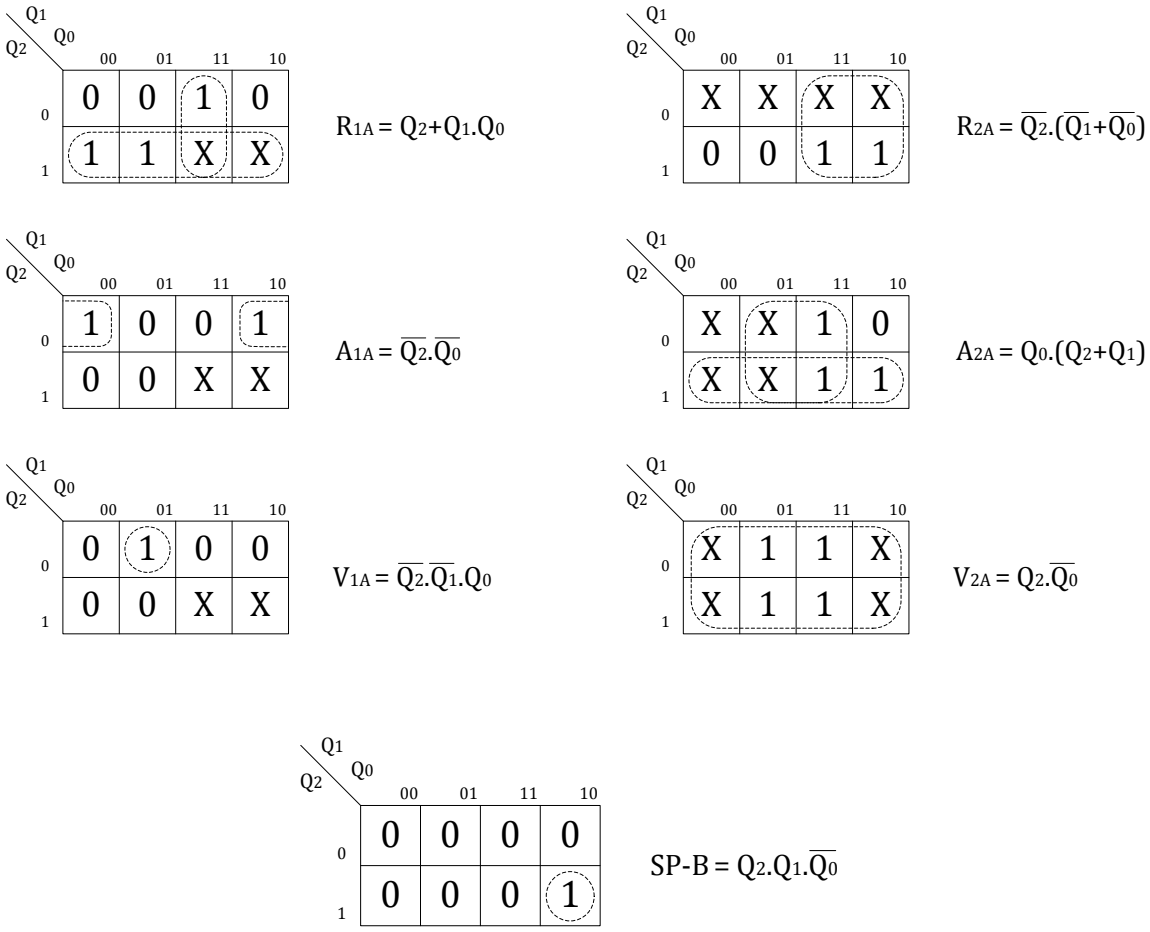


Figura 3.4.2 – *Mapas de Karnaugh correspondientes a las salidas de las luces y SP-B de la Tabla 3.4.1.*

Como se ha mencionado antes, en la secuencia de este módulo se debe hacer uso de los tres timers disponibles. Estos son requeridos en distintos puntos de la secuencia por lo que, de acuerdo al número de cuenta en el que se encuentre el contador, se deberá activar cierta señal de clock en la entrada del módulo. En la *Tabla 3.4.2* se muestra la tabla de estados pertinente, en la cual se usó como referencia la *Tabla 3.1*.

Q_2^n	Q_1^n	Q_0^n	Ck-A_B	Ck-B_B
0	0	0	0	1
0	0	1	1	0
0	1	0	0	1
0	1	1	0	1
1	0	0	1	0
1	0	1	0	1
1	1	0	X	X
1	1	1	X	X

Tabla 3.4.2 – *Tabla de estados de las salidas Ck-A_B y Ck-B_B.*

En la *Figura 3.4.3* se exhiben los mapas de Karnaugh correspondientes a las salidas de la *Tabla 3.4.2*.

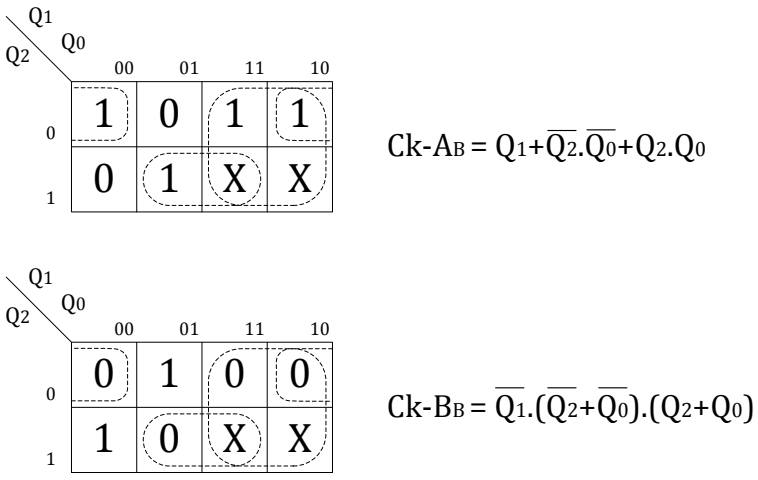


Figura 3.4.3 – *Mapas de Karnaugh correspondientes a las salidas salidas Ck-A_B y Ck-B_B de la Tabla 3.4.2.*

De esta manera se obtiene el circuito mostrado en la *Figura 3.4.4*. Nótese que la entrada RST se encuentra conectada a los reset de los FF-JK, de manera de asegurar que el contador comience desde el principio de la cuenta al iniciar la secuencia.

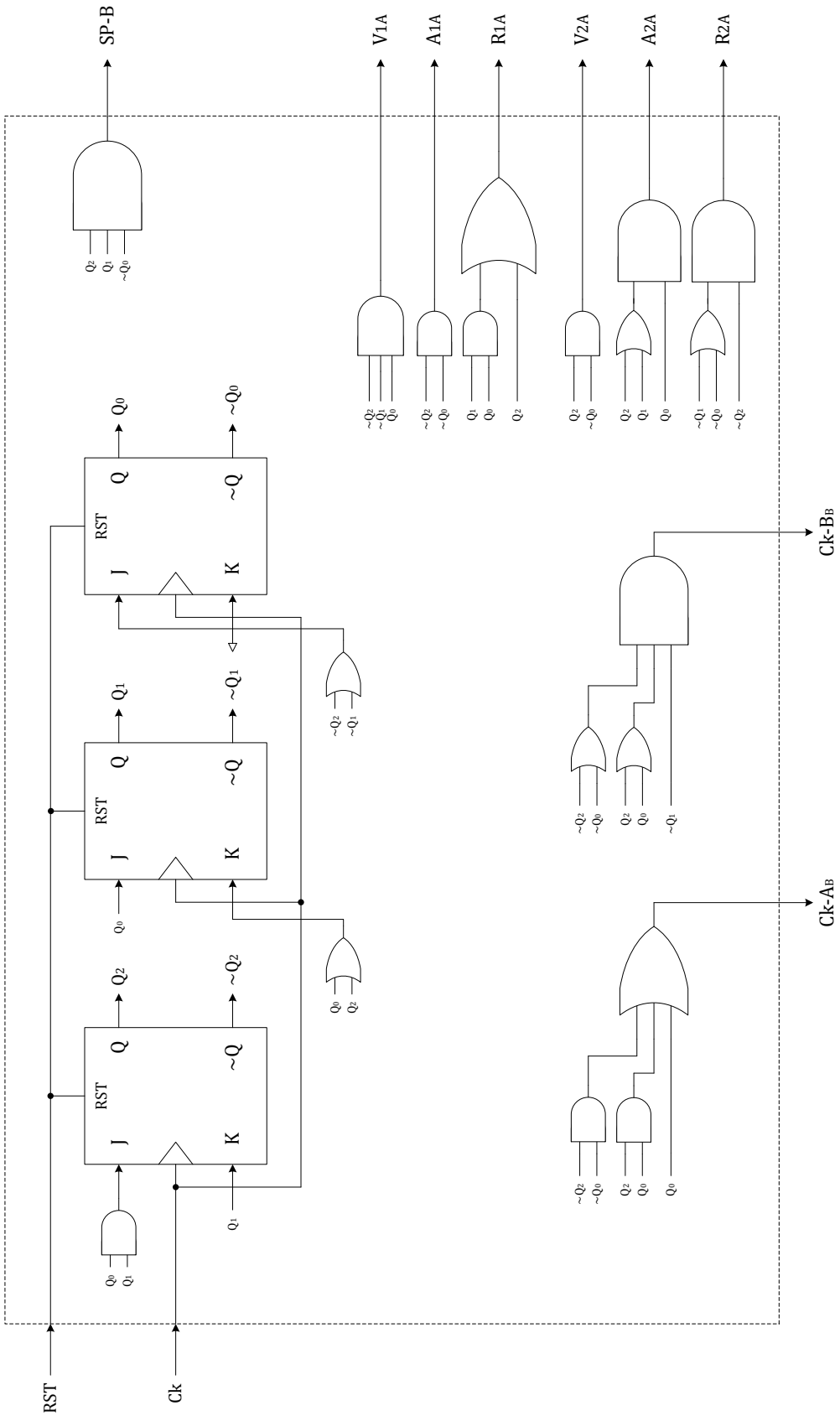


Figura 3.4.4 – *Esquema circuital del módulo de la Secuencia B.*

3.5. Módulo de la *Secuencia C*

La secuencia de este módulo es un estado estacionario en el cual simplemente mantenemos prendidas las luces amarillas y rojas de ambos semáforos. Por esto, las salidas correspondientes a estas se han conectado a 5V, mientras que las salidas de las luces verdes se han conectado a masa.

Las salidas Ck-A_C y Ck-B_C también se han conectado a masa pero en este caso no es de gran importancia, ya que la entrada de clock no se utiliza en la presente unidad. De la misma forma, la entrada RST queda abierta por carecer de significancia.

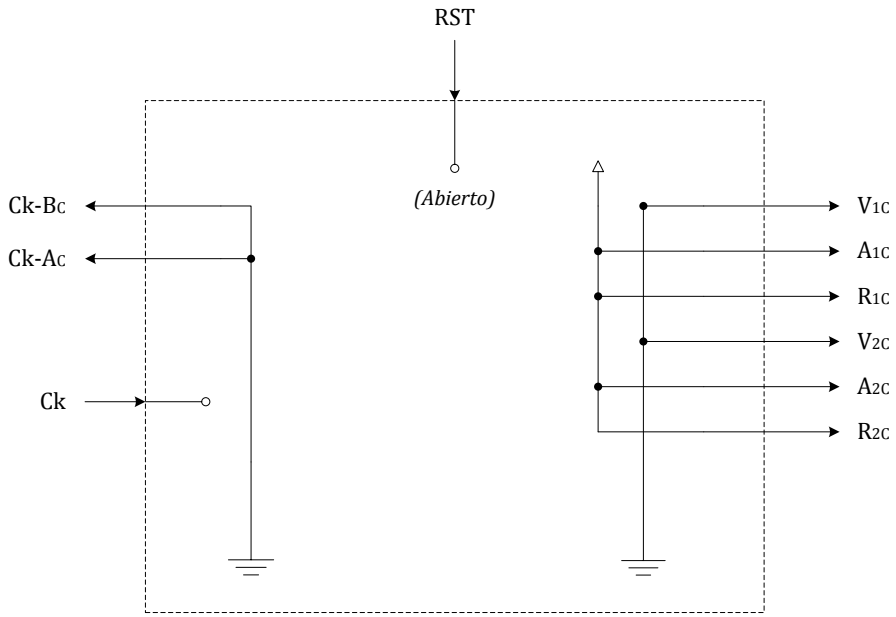


Figura 3.5 – *Esquema circuital del módulo de la Secuencia C.*

4. Simulación

Junto al presente informe se encuentra adjunto un archivo denominado "*TP.Informe.Grupo.8.simulacion.DSN"*, el cual contiene una simulación del sistema completo. Este archivo corresponde al software *Proteus*. Cabe aclarar que se ha realizado la implementación del sistema simplemente con dispositivos genéricos del programa a causa de que ciertos integrados, a pesar de existir en la lista de componentes, no se encuentran modelados para su uso. De todas formas esto no modificará el resultado de la simulación a grandes rasgos, ya que el propósito de esta es mostrar al lector que lo desarrollado funciona de forma óptima y correcta.

5. Componentes electrónicos

Hasta el momento hemos utilizado simplemente los dispositivos teóricos para realizar el desarrollo del sistema. Ahora remplazaremos a estos por sus integrados reales equivalentes de acuerdo a la disponibilidad de componentes electrónicos que nos fue dada. En la *Tabla 6.1* se listan los integrados y componentes electrónicos junto a la cantidad requerida y al precio por unidad. Se adjuntan en el *Apéndice A* las hojas de datos correspondientes a todos los componentes.

Componente	Observaciones	Cantidad	Precio/u ($)
74HC/HCT253	Multiplexor Dual de 4 entradas	5	$3,50
74AHCT139	Demultiplexor Dual de 4 salidas	1	$4,00
74HC/HCT107	FF-JK Dual con Reset	9	$2,30
74HCT1G04	Inversor	3	$1,60
74HC/HCT08	Quad 2-input AND gate	3	$1,90
74HC/HCT11	Triple 3-input AND gate	2	$1,45
74HC/HCT32	Quad 2-input OR gate	3	$1,65
74HC/HCT4075	Triple 3-input OR gate	1	$1,20

Tabla 6.1 – *Componentes electrónicos utilizados. Los precios corresponden a valores aproximados.*

6. Presupuesto

De acuerdo a los precios por unidad y a las cantidades requeridas, sumado a la mano de obra por el diseño, desarrollo y armado del sistema, se presupuesta la siguiente cifra total:

Components electrónicos:	*$61,75*
Mano de obra:	*$200*
Total:	***$261,75***

El tiempo estimado para el desarrollo completo del sistema y puesta en funcionamiento es de 7 días hábiles desde el momento en que es aprobado el presente presupuesto.

7. Conclusión

A lo largo del desarrollo del sistema hemos sido capaces de aplicar lo hasta aquí aprendido, de manera de no solo adoptar los distintos métodos de simplificación conocidos, sino también de utilizar el criterio propio para hallar soluciones mas factibles que nos permitan arribar a una solución mas eficiente y con costos reducidos de componentes electrónicos y mano de obra.

Fácilmente podríamos haber considerado entradas y salidas, todas en una misma tabla de transiciones, y mediante métodos numéricos lograr la simplificación pertinente. Sin embargo, conseguimos en los multiplexores una estrategia de reducción que nos permitió dividir el problema y atacarlo en zonas más pequeñas. De aquí la importancia de acrecentar la destreza en el proceso de minimización de un problema a varios subproblemas de menor complejidad, lo cual nos ha permitido plasmar una solución que cumple con absolutamente todos los requerimientos sin mostrar grandes complejidades circuitales.

Apéndice A

Hojas de datos de componentes electrónicos

DATA SHEET

For a complete data sheet, please also download:

- The IC06 74HC/HCT/HCU/HCMOS Logic Family Specifications
- The IC06 74HC/HCT/HCU/HCMOS Logic Package Information
- The IC06 74HC/HCT/HCU/HCMOS Logic Package Outlines

74HC/HCT107

Dual JK flip-flop with reset; negative-edge trigger

Product specification
File under Integrated Circuits, IC06

December 1990

Philips Semiconductors

PHILIPS

Dual JK flip-flop with reset; negative-edge trigger 74HC/HCT107

FEATURES

- Output capability: standard
- I_{CC} category: flip-flops

GENERAL DESCRIPTION

The 74HC/HCT107 are high-speed Si-gate CMOS devices and are pin compatible with low power Schottky TTL (LSTTL). They are specified in compliance with JEDEC standard no. 7A.

The 74HC/HCT107 are dual negative-edge triggered JK-type flip-flops featuring individual J, K, clock ($n\overline{CP}$) and reset ($n\overline{R}$) inputs; also complementary Q and $\overline{Q}$ outputs.

The J and K inputs must be stable one set-up time prior to the HIGH-to-LOW clock transition for predictable operation.

The reset ($n\overline{R}$) is an asynchronous active LOW input. When LOW, it overrides the clock and data inputs, forcing the Q output LOW and the $\overline{Q}$ output HIGH.

Schmitt-trigger action in the clock input makes the circuit highly tolerant to slower clock rise and fall times.

QUICK REFERENCE DATA

GND = 0 V; T_{amb} = 25 °C; $t_r = t_f$ = 6 ns

SYMBOL	PARAMETER	CONDITIONS	TYPICAL		UNIT
			HC	HCT	
t_{PHL}/ t_{PLH}	propagation delay $n\overline{CP}$ to nQ $n\overline{CP}$ to $n\overline{Q}$ $n\overline{R}$ to nQ, $n\overline{Q}$	C_L = 15 pF; V_{CC} = 5 V	 16 16 16	 16 18 17	 ns ns ns
f_{max}	maximum clock frequency		78	73	MHz
C_I	input capacitance		3.5	3.5	pF
C_{PD}	power dissipation capacitance per flip-flop	notes 1 and 2	30	30	pF

Notes

1. C_{PD} is used to determine the dynamic power dissipation (P_D in μW):

   $P_D = C_{PD} \times V_{CC}^2 \times f_i + \sum (C_L \times V_{CC}^2 \times f_o)$ where:

   f_i = input frequency in MHz

   f_o = output frequency in MHz

   $\sum (C_L \times V_{CC}^2 \times f_o)$ = sum of outputs

   C_L = output load capacitance in pF

   V_{CC} = supply voltage in V

2. For HC the condition is V_I = GND to V_{CC}
   For HCT the condition is V_I = GND to V_{CC} – 1.5 V.

ORDERING INFORMATION

See *"74HC/HCT/HCU/HCMOS Logic Package Information"*.

Dual JK flip-flop with reset; negative-edge trigger 74HC/HCT107

PIN DESCRIPTION

PIN NO.	SYMBOL	NAME AND FUNCTION
1, 8, 4, 11	1J, 2J, 1K, 2K	synchronous inputs; flip-flops 1 and 2
2, 6	$1\overline{Q}$, $2\overline{Q}$	complement flip-flop outputs
3, 5	1Q, 2Q	true flip-flop outputs
7	GND	ground (0 V)
12, 9	$1\overline{CP}$, $2\overline{CP}$	clock input (HIGH-to-LOW, edge-triggered)
13, 10	$1\overline{R}$, $2\overline{R}$	asynchronous reset inputs (active LOW)
14	V_{CC}	positive supply voltage

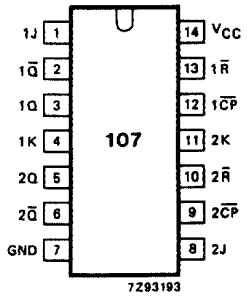


Fig.1 Pin configuration.

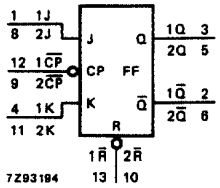


Fig.2 Logic symbol.

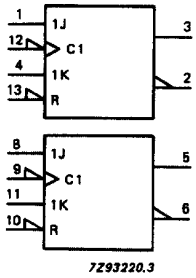


Fig.3 IEC logic symbol.

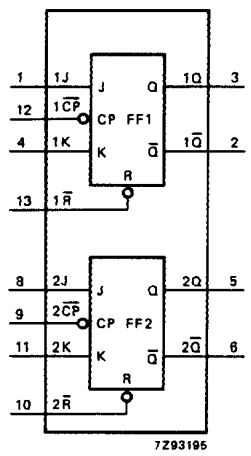


Fig.4 Functional diagram.

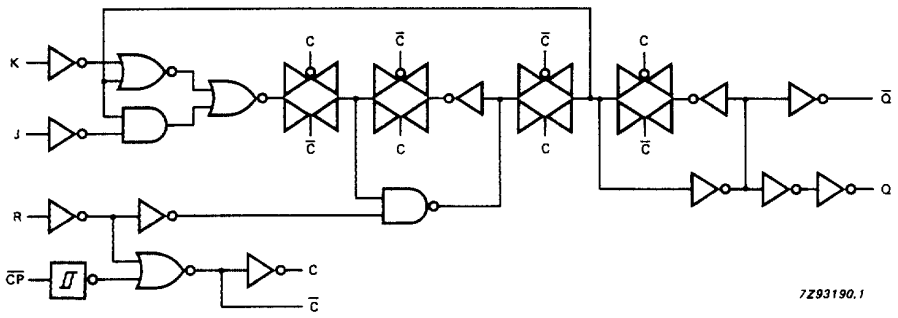


Fig.5 Logic diagram (one flip-flop).

FUNCTION TABLE

OPERATING MODE	INPUTS				OUTPUTS	
	$n\overline{R}$	$n\overline{CP}$	J	K	Q	$\overline{Q}$
asynchronous reset	L	X	X	X	L	H
toggle	H	↓	h	h	$\overline{q}$	q
load “0” (reset)	H	↓	l	h	L	H
load “1” (set)	H	↓	h	l	H	L
hold “no change”	H	↓	l	l	q	$\overline{q}$

Note

1. H = HIGH voltage level
   h = HIGH voltage level one set-up time prior to the HIGH-to-LOW CP transition
   L = LOW voltage level
   l = LOW voltage level one set-up time prior to the HIGH-to-LOW CP transition
   q = lower case letters indicate the state of the referenced output one set-up time prior to the HIGH-to-LOW CP transition
   X = don’t care
   ↓ = HIGH-to-LOW CP transition

DC CHARACTERISTICS FOR 74HC

For the DC characteristics see *"74HC/HCT/HCU/HCMOS Logic Family Specifications"*.

Output capability: standard
I_{CC} category: flip-flops

AC CHARACTERISTICS FOR 74HC

GND = 0 V; $t_r = t_f$ = 6 ns; C_L = 50 pF

SYMBOL	PARAMETER	T_{amb} (°C)							UNIT	TEST CONDITIONS	
		74HC								V_{CC} (V)	WAVEFORMS
		+25			−40 to +85		−40 to +125				
		min.	typ.	max.	min.	max.	min.	max.			
t_{PHL}/ t_{PLH}	propagation delay $n\overline{CP}$ to nQ		52 19 15	160 32 27		200 40 34		240 48 41	ns	2.0 4.5 6.0	Fig.6
t_{PHL}/ t_{PLH}	propagation delay $n\overline{CP}$ to $n\overline{Q}$		52 19 15	160 32 27		200 40 34		240 48 41	ns	2.0 4.5 6.0	Fig.6
t_{PHL}/ t_{PLH}	propagation delay $n\overline{R}$ to nQ, $n\overline{Q}$		52 19 15	155 31 26		195 39 33		235 47 40	ns	2.0 4.5 6.0	Fig.7
t_{THL}/ t_{TLH}	output transition time		19 7 6	75 15 13		95 19 16		110 22 19	ns	2.0 4.5 6.0	Fig.6
t_W	clock pulse width HIGH or LOW	80 16 14	22 8 6		100 20 17		120 24 20		ns	2.0 4.5 6.0	Fig.6
t_W	reset pulse width LOW	80 16 14	22 8 6		100 20 17		120 24 20		ns	2.0 4.5 6.0	Fig.7
t_{rem}	removal time $n\overline{R}$ to $n\overline{CP}$	60 12 10	19 7 6		75 15 13		90 18 15		ns	2.0 4.5 6.0	Fig.7
t_{su}	set-up time nJ, nK to $n\overline{CP}$	100 20 17	22 8 6		125 25 21		150 30 26		ns	2.0 4.5 6.0	Fig.6
t_h	hold time nJ, nK to $n\overline{CP}$	3 3 3	−6 −2 −2		3 3 3		3 3 3		ns	2.0 4.5 6.0	Fig.6
f_{max}	maximum clock pulse frequency	6.0 30 35	23 70 85		4.8 24 28		4.0 20 24		MHz	2.0 4.5 6.0	Fig.6

DC CHARACTERISTICS FOR 74HCT

For the DC characteristics see *"74HC/HCT/HCU/HCMOS Logic Family Specifications"*.

Output capability: standard
I_{CC} category: flip-flops

Note to HCT types

The value of additional quiescent supply current (ΔI_{CC}) for a unit load of 1 is given in the family specifications. To determine ΔI_{CC} per input, multiply this value by the unit load coefficient shown in the table below.

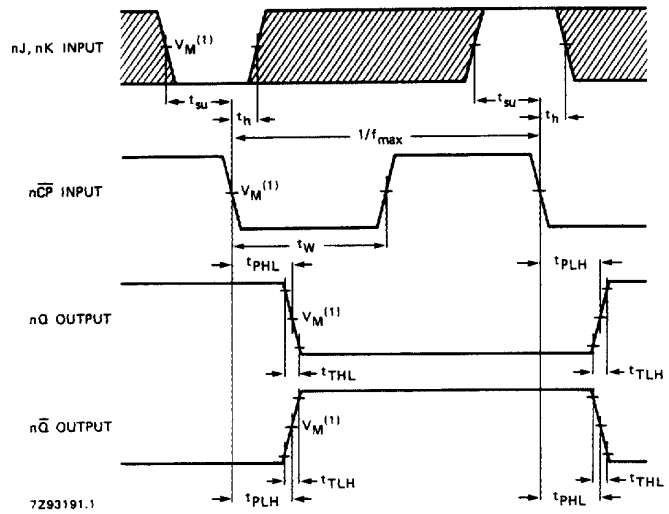
INPUT	UNIT LOAD COEFFICIENT
nK	0.60
$n\overline{R}$	0.65
$n\overline{CP}$, nJ	1.00

AC CHARACTERISTICS FOR 74HCT

GND = 0 V; $t_f = t_f$ = 6 ns; C_L = 50 pF

SYMBOL	PARAMETER	T_{amb} (°C)							UNIT	TEST CONDITIONS	
		74HCT								V_{CC} (V)	WAVEFORMS
		+25			−40 to +85		−40 to +125				
		min.	typ.	max.	min.	max.	min.	max.			
t_{PHL}/ t_{PLH}	propagation delay $n\overline{CP}$ to nQ		19	36		45		54	ns	4.5	Fig.6
t_{PHL}/ t_{PLH}	propagation delay $n\overline{CP}$ to $n\overline{Q}$		21	36		45		54	ns	4.5	Fig.6
t_{PHL}/ t_{PLH}	propagation delay $n\overline{R}$ to nQ, $n\overline{Q}$		20	38		48		57	ns	4.5	Fig.7
t_{THL}/ t_{TLH}	output transition time		7	15		19		22	ns	4.5	Fig.6
t_W	clock pulse width HIGH or LOW	16	9		20		24		ns	4.5	Fig.6
t_W	reset pulse width LOW	20	11		25		30		ns	4.5	Fig.7
t_{rem}	removal time $n\overline{R}$ to $n\overline{CP}$	14	8		18		21		ns	4.5	Fig.7
t_{su}	set-up time nJ, nK to $n\overline{CP}$	20	7		25		30		ns	4.5	Fig.6
t_h	hold time nJ, nK to $n\overline{CP}$	5	−2		5		5		ns	4.5	Fig.6
f_{max}	maximum clock pulse frequency	30	66		24		20		MHz	4.5	Fig.6

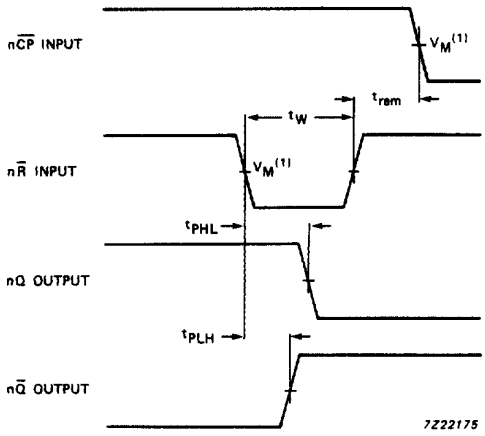
AC WAVEFORMS



The shaded areas indicate when the input is permitted to change for predictable output performance.

(1) HC : V_M = 50%; V_I = GND to V_{CC}.
HCT: V_M = 1.3 V; V_I = GND to 3 V.

Fig.6 Waveforms showing the clock (nCP) to output (nQ, nQ) propagation delays, the clock pulse width, the J and K to nCP set-up and hold times, the output transition times and the maximum clock pulse frequency.



(1) HC : V_M = 50%; V_I = GND to V_{CC}.
HCT: V_M = 1.3 V; V_I = GND to 3 V.

Fig.7 Waveforms showing the reset (nR) input to output (nQ, nQ) propagation delays, the reset pulse width and the nR to nCP removal time.

PACKAGE OUTLINES

See *"74HC/HCT/HCU/HCMOS Logic Package Outlines"*.

DATA SHEET

For a complete data sheet, please also download:

- The IC06 74HC/HCT/HCU/HCMOS Logic Family Specifications
- The IC06 74HC/HCT/HCU/HCMOS Logic Package Information
- The IC06 74HC/HCT/HCU/HCMOS Logic Package Outlines

74HC/HCT253

Dual 4-input multiplexer; 3-state

Product specification
File under Integrated Circuits, IC06

December 1990

Philips Semiconductors

PHILIPS

Dual 4-input multiplexer; 3-state 74HC/HCT253

FEATURES

- Non-inverting data path
- 3-state outputs for bus interface
- and multiplex expansion
- Common select inputs
- Separate output enable inputs
- Output capability: bus driver
- I_{CC} category: MSI

GENERAL DESCRIPTION

The 74HC/HCT253 are high-speed Si-gate CMOS devices and are pin compatible with low power Schottky TTL (LSTTL). They are specified in compliance with JEDEC standard no. 7A.

The 74HC/HCT253 have two identical 4-input multiplexers with 3-state outputs which select two bits from four sources selected by common data select inputs (S_0, S_1). When the individual output enable ($1\overline{OE}$, $2\overline{OE}$) inputs of the 4-input multiplexers are HIGH, the outputs are forced to the high impedance OFF-state. The “253” is the logic implementation of a 2-pole, 4-position switch, where the position of the switch is determined by the logic levels applied to S_0 and S_1.

The logic equations for the outputs are:
$1Y = 1\overline{OE}(1I_0.\overline{S}_1.\overline{S}_0+1I_1.\overline{S}_1.S_0+1I_2.S_1.\overline{S}_0+1I_3.S_1.S_0)$
$2Y = 2\overline{OE}(2I_0.\overline{S}_1.\overline{S}_0+2I_1.\overline{S}_1.S_0+2I_2.S_1.\overline{S}_0+2I_3.S_1.S_0)$

APPLICATIONS

- Data selectors
- Data multiplexers

QUICK REFERENCE DATA

GND = 0 V; T_{amb} = 25 °C; $t_r = t_f$ = 6 ns

SYMBOL	PARAMETER	CONDITIONS	TYPICAL		UNIT
			HC	HCT	
t_{PHL}/ t_{PLH}	propagation delay	C_L = 15 pF; V_{CC} = 5 V			
	$1I_n$, $2I_n$ to nY;		17	17	ns
	S_n to nY		18	19	ns
C_I	input capacitance		3.5	3.5	pF
C_{PD}	power dissipation capacitance per multiplexer	notes 1 and 2	55	55	pF

Notes

1. C_{PD} is used to determine the dynamic power dissipation (P_D in µW):

   $P_D = C_{PD} \times V_{CC}^2 \times f_i + \sum (C_L \times V_{CC}^2 \times f_o)$ where:

   f_i = input frequency in MHz

   f_o = output frequency in MHz

   $\sum (C_L \times V_{CC}^2 \times f_o)$ = sum of outputs

   C_L = output load capacitance in pF

   V_{CC} = supply voltage in V

2. For HC the condition is V_I = GND to V_{CC}
   For HCT the condition is V_I = GND to V_{CC} – 1.5 V

ORDERING INFORMATION

See *“74HC/HCT/HCU/HCMOS Logic Package Information”*.

PIN DESCRIPTION

PIN NO.	SYMBOL	NAME AND FUNCTION
1, 15	$1\overline{OE}$, $2\overline{OE}$	output enable inputs (active LOW)
14, 2	S_0, S_1	common data select inputs
7, 9	1Y, 2Y	3-state multiplexer outputs
8	GND	ground (0 V)
6, 5, 4, 3	$1I_0$ to $1I_3$	data inputs from source 1
10, 11, 12, 13	$2I_0$ to $2I_3$	data inputs from source 2
16	V_{CC}	positive supply voltage

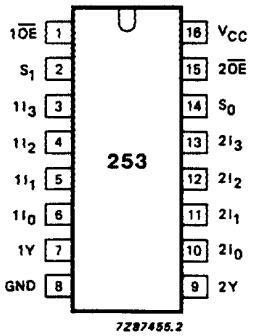


Fig.1 Pin configuration.

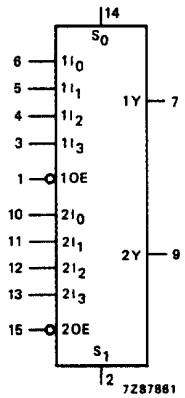


Fig.2 Logic symbol.

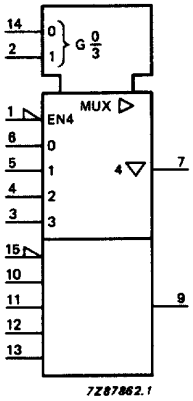


Fig.3 IEC logic symbol.

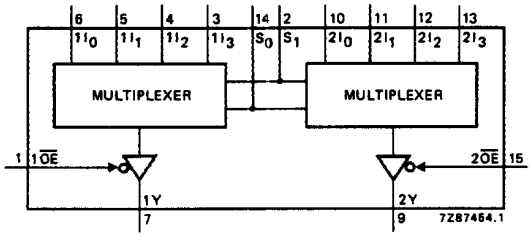


Fig.4 Functional diagram.

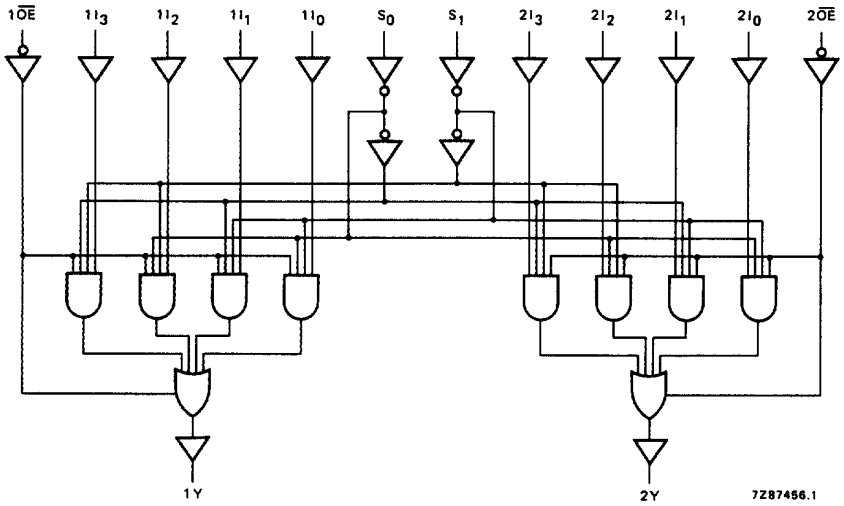


Fig.5 Logic diagram.

FUNCTION TABLE

SELECT INPUTS		DATA INPUTS				OUTPUT ENABLE	OUTPUT
S_0	S_1	nI_0	nI_1	nI_2	nI_3	$n\overline{OE}$	nY
X	X	X	X	X	X	H	Z
L	L	L	X	X	X	L	L
L	L	H	X	X	X	L	H
H	L	X	L	X	X	L	L
H	L	X	H	X	X	L	H
L	H	X	X	L	X	L	L
L	H	X	X	H	X	L	H
H	H	X	X	X	L	L	L
H	H	X	X	X	H	L	H

NOTES

1. H = HIGH voltage level
   L = LOW voltage level
   X = don't care
   Z = high impedance OFF-state

DC CHARACTERISTICS FOR 74HC

For the DC characteristics see *"74HC/HCT/HCU/HCMOS Logic Family Specifications"*.

Output capability: bus driver
I_{CC} category: MSI

AC CHARACTERISTICS FOR 74HC

GND = 0 V; $t_r = t_f$ = 6 ns; C_L = 50 pF

SYMBOL	PARAMETER	T_{amb} (°C)							UNIT	TEST CONDITIONS	
		74HC								V_{CC} (V)	WAVEFORMS
		+25			−40 to +85		−40 to +125				
		min.	typ.	max.	min.	max.	min.	max.			
t_{PHL}/ t_{PLH}	propagation delay $1I_n$ to nY; $2I_n$ to nY		55 20 16	175 35 30		220 44 37		265 53 45	ns	2.0 4.5 6.0	Fig.6
t_{PHL}/ t_{PLH}	propagation delay S_n to nY		58 21 17	175 35 30		220 44 37		265 53 45	ns	2.0 4.5 6.0	Fig.6
t_{PZH}/ t_{PZL}	3-state output enable time $n\overline{OE}$ to nY		30 11 9	100 20 17		125 25 21		150 30 26	ns	2.0 4.5 6.0	Fig.7
t_{PHZ}/ t_{PLZ}	3-state output disable time $n\overline{OE}$ to nY		41 15 12	150 30 26		190 38 33		225 45 38	ns	2.0 4.5 6.0	Fig.7
t_{THL}/ t_{TLH}	output transition time		14 5 4	60 12 10		75 15 13		90 18 15	ns	2.0 4.5 6.0	Fig.6

DC CHARACTERISTICS FOR 74HCT

For the DC characteristics see *"74HC/HCT/HCU/HCMOS Logic Family Specifications"*.

Output capability: bus driver
I_{CC} category: MSI

Note to HCT types

The value of additional quiescent supply current (ΔI_{CC}) for a unit load of 1 is given in the family specifications. To determine ΔI_{CC} per input, multiply this value by the unit load coefficient shown in the table below.

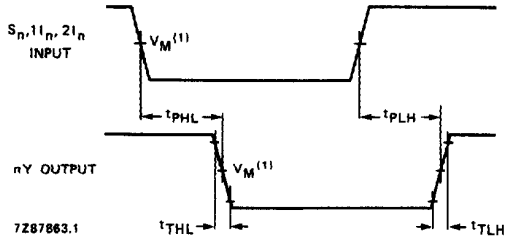
INPUT	UNIT LOAD COEFFICIENT
$1I_n$	0.40
$2I_n$	0.40
$n\overline{OE}$	1.10
S_0	1.10
S_1	1.10

AC CHARACTERISTICS FOR 74HCT

GND = 0 V; $t_r = t_f$ = 6 ns; C_L = 50 pF

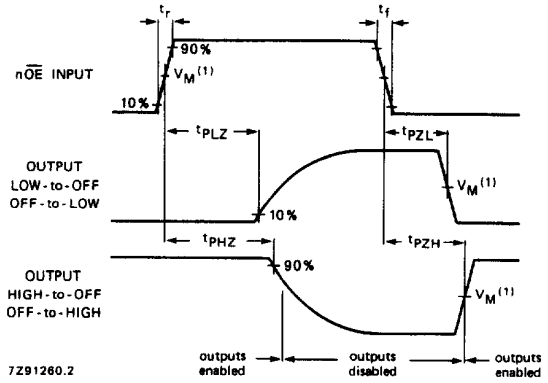
SYMBOL	PARAMETER	T_{amb} (°C)							UNIT	TEST CONDITIONS	
		74HCT								V_{CC} (V)	WAVEFORMS
		+25			–40 to +85		–40 to +125				
		min.	typ.	max.	min.	max.	min.	max.			
t_{PHL}/ t_{PLH}	propagation delay $1I_n$ to nY; $2I_n$ to nY		20	38		48		57	ns	4.5	Fig.6
t_{PHL}/ t_{PLH}	propagation delay S_n to nY		22	40		50		60	ns	4.5	Fig.6
t_{PZH}/ t_{PZL}	3-state output enable time $n\overline{OE}$ to nY		14	30		38		45	ns	4.5	Fig.7
t_{PHZ}/ t_{PLZ}	3-state output disable time $n\overline{OE}$ to nY		13	30		38		45	ns	4.5	Fig.7
t_{THL}/ t_{TLH}	output transition time		5	12		15		18	ns	4.5	Fig.6

AC WAVEFORMS



(1) HC : V_M = 50%; V_I = GND to V_{CC}.
HCT: V_M = 1.3 V; V_I = GND to 3 V.

Fig.6 Waveforms showing the input ($1I_n$, $2I_n$) to output (1Y, 2Y) propagation delays and the output transition times.



(1) HC : V_M = 50%; V_I = GND to V_{CC}.
HCT: V_M = 1.3 V; V_I = GND to 3 V.

Fig.7 Waveforms showing the 3-state enable and disable times.

PACKAGE OUTLINES

See *"74HC/HCT/HCU/HCMOS Logic Package Outlines"*.

DATA SHEET

74AHC139; 74AHCT139
Dual 2-to-4 line decoder/demultiplexer

Product specification
File under Integrated Circuits, IC06

1999 Sep 01

Philips Semiconductors

PHILIPS

Dual 2-to-4 line decoder/demultiplexer

74AHC139; 74AHCT139

FEATURES

- ESD protection:
  HBM EIA/JESD22-A114-A exceeds 2000 V
  MM EIA/JESD22-A115-A exceeds 200 V
  CDM EIA/JESD22-C101 exceeds 1000 V
- Balanced propagation delays
- All inputs have Schmitt trigger actions
- Inputs accept voltages higher than V_{CC}
- For AHC only: operates with CMOS input levels
- For AHCT only: operates with TTL input levels
- Specified from –40 to +85 °C and –40 to +125 °C.

DESCRIPTION

The 74AHC/AHCT139 are high-speed Si-gate CMOS devices and are pin compatible with low power Schottky TTL (LSTTL). They are specified in compliance with JEDEC standard no. 7A.

The 74AHC/AHCT139 are high-speed, dual 2-to-4 line decoder/demultiplexers.

This device has two independent decoders, each accepting two binary weighted inputs (nA_0 and nA_1) and providing four mutually exclusive active LOW outputs ($n\overline{Y}_0$ to $n\overline{Y}_3$). Each decoder has an active LOW enable input ($n\overline{E}$). When $n\overline{E}$ is HIGH, every output is forced HIGH. The enable input can be used as the data input for a 1-to-4 demultiplexer application.

The ‘139’ is identical to the HEF4556 of the HE4000B family.

QUICK REFERENCE DATA

Ground = 0 V; T_{amb} = 25 °C; $t_r = t_f \leq 3.0$ ns.

SYMBOL	PARAMETER	CONDITIONS	TYPICAL		UNIT
			AHC	AHCT	
t_{PHL}/t_{PLH}	propagation delay	C_L = 15 pF; V_{CC} = 5 V			
	nA_n to $n\overline{Y}_n$		3.9	4.7	ns
	$n\overline{E}$ to $n\overline{Y}_n$		3.4	3.6	ns
C_I	input capacitance	$V_I = V_{CC}$ or GND	3.0	3.0	pF
C_O	output capacitance		4.0	4.0	pF
C_{PD}	power dissipation capacitance	C_L = 50 pF; f = 1 MHz; notes 1 and 2	25.76	22.36	pF

Notes

1. C_{PD} is used to determine the dynamic power dissipation (P_D in μW).
   $P_D = C_{PD} \times V_{CC}^2 \times f_i + \sum (C_L \times V_{CC}^2 \times f_o)$ where:
   f_i = input frequency in MHz;
   f_o = output frequency in MHz;
   $\sum (C_L \times V_{CC}^2 \times f_o)$ = sum of outputs;
   C_L = output load capacitance in pF;
   V_{CC} = supply voltage in Volts.
2. The condition is V_I = GND to V_{CC}.

FUNCTION TABLE

See note 1.

INPUTS			OUTPUTS			
$n\overline{E}$	nA_0	nA_1	$n\overline{Y}_0$	$n\overline{Y}_1$	$n\overline{Y}_2$	$n\overline{Y}_3$
H	X	X	H	H	H	H
L	L	L	L	H	H	H
L	H	L	H	L	H	H
L	L	H	H	H	L	H
L	H	H	H	H	H	L

Note

1. H = HIGH voltage level;
   L = LOW voltage level;
   X = don't care.

ORDERING INFORMATION

OUTSIDE NORTH AMERICA	NORTH AMERICA	PACKAGES			
		PINS	PACKAGE	MATERIAL	CODE
74AHC139D	74AHC139D	16	SO	plastic	SOT109-1
74AHC139PW	74AHC139PW DH	16	TSSOP	plastic	SOT403-1
74AHCT139D	74AHCT139D	16	SO	plastic	SOT109-1
74AHCT139PW	74AHCT139PW DH	16	TSSOP	plastic	SOT403-1

PINNING

PIN	SYMBOL	DESCRIPTION
1 and 15	$1\overline{E}$ and $2\overline{E}$	enable inputs (active LOW)
2 and 3	$1A_0$ and $1A_1$	address inputs
4, 5, 6 and 7	$1\overline{Y}_0$, $1\overline{Y}_1$, $\overline{Y}_2$ and $1\overline{Y}_3$	outputs (active LOW)
8	GND	ground (0 V)
9, 10, 11 and 12	$2\overline{Y}_3$, $2\overline{Y}_2$, $2\overline{Y}_1$ and $2\overline{Y}_0$	outputs (active LOW)
13 and 14	$2A_1$ and $2A_0$	address inputs
16	V_{CC}	DC supply voltage

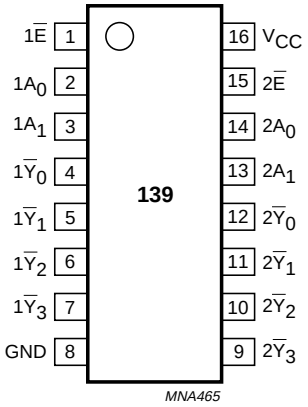


Fig.1 Pin configuration.

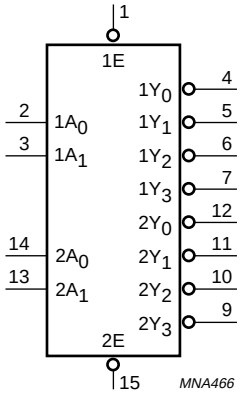


Fig.2 Logic symbol.

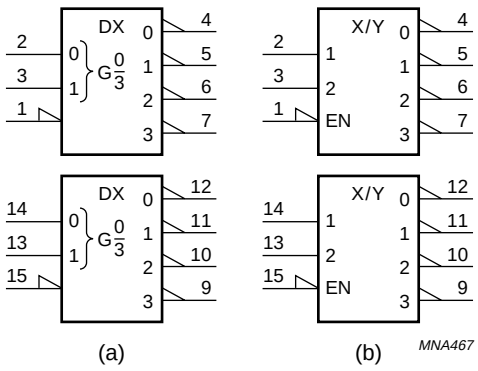


Fig.3 IEC logic symbol.

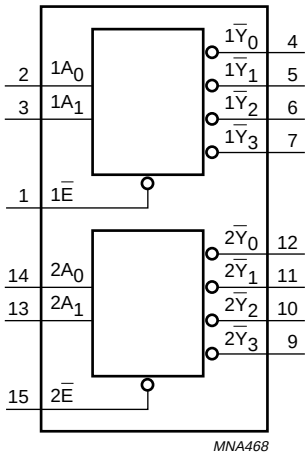


Fig.4 Functional diagram.

RECOMMENDED OPERATING CONDITIONS

SYMBOL	PARAMETER	CONDITIONS	74AHC			74AHCT			UNIT
			MIN.	TYP.	MAX.	MIN.	TYP.	MAX.	
V_{CC}	DC supply voltage		2.0	5.0	5.5	4.5	5.0	5.5	V
V_I	input voltage		0	–	5.5	0	–	5.5	V
V_O	output voltage		0	–	V_{CC}	0	–	V_{CC}	V
T_{amb}	operating ambient temperature	see DC and AC characteristics per device	–40	+25	+85	–40	+25	+85	°C
			–40	+25	+125	–40	+25	+125	°C
t_r, t_f ($\Delta t/\Delta f$)	input rise and fall ratio	V_{CC} = 3.3 ±0.3 V	–	–	100	–	–	–	ns/V
		V_{CC} = 5 ±0.5 V	–	–	20	–	–	20	

LIMITING VALUES

In accordance with the Absolute Maximum Rating System (IEC 134); voltages are referenced to GND (ground = 0 V).

SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.	UNIT
V_{CC}	DC supply voltage		–0.5	+7.0	V
V_I	input voltage		–0.5	+7.0	V
I_{IK}	DC input diode current	V_I < –0.5 V; note 1	–	–20	mA
I_{OK}	DC output diode current	V_O < –0.5 V or V_O > V_{CC} + 0.5 V; note 1	–	±20	mA
I_O	DC output source or sink current	–0.5 V < V_O < V_{CC} + 0.5 V	–	±25	mA
I_{CC}	DC V_{CC} or GND current		–	±75	mA
T_{stg}	storage temperature		–65	+150	°C
P_D	power dissipation per package	for temperature range: –40 to +125 °C; note 2	–	500	mW

Notes

1. The input and output voltage ratings may be exceeded if the input and output current ratings are observed.
2. For SO package: above 70 °C the value of P_D derates linearly with 8 mW/K.
   For TSSOP package: above 60 °C the value of P_D derates linearly with 5.5 mW/K.

DC CHARACTERISTICS

Family 74AHC

Over recommended operating conditions; voltage are referenced to GND (ground = 0 V).

SYMBOL	PARAMETER	TEST CONDITIONS		T_{amb} (°C)							UNIT
		OTHER	V_{CC} (V)	25			–40 to +85		–40 to +125		
				MIN.	TYP.	MAX.	MIN.	MAX.	MIN.	MAX.	
V_{IH}	HIGH-level input voltage		2.0	1.5	–	–	1.5	–	1.5	–	V
			3.0	2.1	–	–	2.1	–	2.1	–	
			5.5	3.85	–	–	3.85	–	3.85	–	
V_{IL}	LOW-level input voltage		2.0	–	–	0.5	–	0.5	–	0.5	V
			3.0	–	–	0.9	–	0.9	–	0.9	
			5.5	–	–	1.65	–	1.65	–	1.65	
V_{OH}	HIGH-level output voltage; all outputs	$V_I = V_{IH}$ or V_{IL}; $I_O = –50$ µA	2.0	1.9	2.0	–	1.9	–	1.9	–	V
			3.0	2.9	3.0	–	2.9	–	2.9	–	
			4.5	4.4	4.5	–	4.4	–	4.4	–	
	HIGH-level output voltage	$V_I = V_{IH}$ or V_{IL}; $I_O = –4.0$ mA	3.0	2.58	–	–	2.48	–	2.40	–	V
		$V_I = V_{IH}$ or V_{IL}; $I_O = –8.0$ mA	4.5	3.94	–	–	3.8	–	3.70	–	
V_{OL}	LOW-level output voltage; all outputs	$V_I = V_{IH}$ or V_{IL}; $I_O = 50$ µA	2.0	–	0	0.1	–	0.1	–	0.1	V
			3.0	–	0	0.1	–	0.1	–	0.1	
			4.5	–	0	0.1	–	0.1	–	0.1	
	LOW-level output voltage	$V_I = V_{IH}$ or V_{IL}; $I_O = 4.0$ mA	3.0	–	–	0.36	–	0.44	–	0.55	V
		$V_I = V_{IH}$ or V_{IL}; $I_O = 8.0$ mA	4.5	–	–	0.36	–	0.44	–	0.55	
I_I	input leakage current	$V_I = V_{CC}$ or GND	5.5	–	–	0.1	–	1.0	–	2.0	µA
I_{OZ}	3-state output OFF current	$V_I = V_{IH}$ or V_{IL}; $V_O = V_{CC}$ or GND	5.5	–	–	±0.25	–	±2.5	–	±10.0	µA
I_{CC}	quiescent supply current	$V_I = V_{CC}$ or GND; $I_O = 0$	5.5	–	–	4.0	–	40	–	80	µA
C_I	input capacitance		–	–	3	10	–	10	–	10	pF

Family 74AHCT

Over recommended operating conditions; voltage are referenced to GND (ground = 0 V).

SYMBOL	PARAMETER	TEST CONDITIONS		T_{amb} (°C)							UNIT
		OTHER	V_{CC} (V)	25			−40 to +85		−40 to +125		
				MIN.	TYP.	MAX.	MIN.	MAX.	MIN.	MAX.	
V_{IH}	HIGH-level input voltage		4.5 to 5.5	2.0	–	–	2.0	–	2.0	–	V
V_{IL}	LOW-level input voltage		4.5 to 5.5	–	–	0.8	–	0.8	–	0.8	V
V_{OH}	HIGH-level output voltage; all outputs	$V_I = V_{IH}$ or V_{IL}; $I_O = –50$ μA	4.5	4.4	4.5	–	4.4	–	4.4	–	V
	HIGH-level output voltage	$V_I = V_{IH}$ or V_{IL}; $I_O = –8.0$ mA	4.5	3.94	–	–	3.8	–	3.70	–	V
V_{OL}	LOW-level output voltage; all outputs	$V_I = V_{IH}$ or V_{IL}; $I_O = 50$ μA	4.5	–	0	0.1	–	0.1	–	0.1	V
	LOW-level output voltage	$V_I = V_{IH}$ or V_{IL}; $I_O = 8.0$ mA	4.5	–	–	0.36	–	0.44	–	0.55	V
I_I	input leakage current	$V_I = V_{IH}$ or V_{IL}	5.5	–	–	0.1	–	1.0	–	2.0	μA
I_{OZ}	3-state output OFF current	$V_I = V_{IH}$ or V_{IL}; $V_O = V_{CC}$ or GND per input pin; other inputs at V_{CC} or GND; $I_O = 0$	5.5	–	–	±0.25	–	±2.5	–	±10.0	μA
I_{CC}	quiescent supply current	$V_I = V_{CC}$ or GND; $I_O = 0$	5.5	–	–	4.0	–	40	–	80	μA
ΔI_{CC}	additional quiescent supply current per input pin	$V_I = V_{CC} – 2.1$ V; other inputs at V_{CC} or GND; $I_O = 0$	4.5 to 5.5	–	–	1.35	–	1.5	–	1.5	mA
C_I	input capacitance		–	–	3	10	–	10	–	10	pF

AC CHARACTERISTICS

Type 74AHC139

Ground = 0 V; $t_r = t_f \leq 3.0$ ns.

SYMBOL	PARAMETER	TEST CONDITIONS		T_{amb} (°C)							UNIT
		WAVEFORMS	C_L	25			−40 to +85		−40 to +125		
				MIN.	TYP.	MAX.	MIN.	MAX.	MIN.	MAX.	
V_{CC} = 3.0 to 3.6 V; note 1											
t_{PHL}/t_{PLH}	propagation delay nA_n to $n\overline{Y}_n$	see Figs 5 and 7	15 pF	–	5.5	11.0	1.0	13.0	1.0	14.0	ns
	propagation delay $n\overline{E}$ to $n\overline{Y}_n$	see Figs 6 and 7		–	4.8	9.2	1.0	11.0	1.0	11.5	ns
	propagation delay nA_n to $n\overline{Y}_n$	see Figs 5 and 7	50 pF	–	7.9	14.5	1.0	16.5	1.0	18.5	ns
	propagation delay $n\overline{E}$ to $n\overline{Y}_n$	see Figs 6 and 7		–	6.9	12.7	1.0	14.5	1.0	16.0	ns
V_{CC} = 4.5 to 5.5 V; note 2											
t_{PHL}/t_{PLH}	propagation delay nA_n to $n\overline{Y}_n$	see Figs 5 and 7	15 pF	–	3.9	7.2	1.0	8.5	1.0	9.0	ns
	propagation delay $n\overline{E}$ to $n\overline{Y}_n$	see Figs 6 and 7		–	3.4	6.3	1.0	7.5	1.0	8.0	ns
	propagation delay nA_n to $n\overline{Y}_n$	see Figs 5 and 7	50 pF	–	5.6	9.2	1.0	10.5	1.0	11.5	ns
	propagation delay $n\overline{E}$ to $n\overline{Y}_n$	see Figs 6 and 7		–	4.9	8.3	1.0	9.5	1.0	10.5	ns

Notes

1. Typical values at V_{CC} = 3.3 V.
2. Typical values at V_{CC} = 5.0 V.

Type 74AHCT139

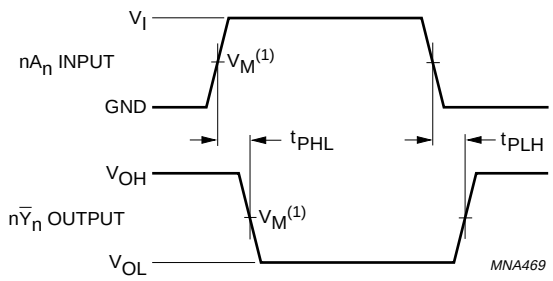
Ground = 0 V; $t_r = t_f \leq 3.0$ ns.

SYMBOL	PARAMETER	TEST CONDITIONS		T_{amb} (°C)							UNIT
		WAVEFORMS	C_L	25			–40 to +85		–40 to +125		
				MIN.	TYP.	MAX.	MIN.	MAX.	MIN.	MAX.	
V_{CC} = 4.5 to 5.5 V; note 1											
t_{PHL}/t_{PLH}	propagation delay nA_n to $n\overline{Y}_n$	see Figs 5 and 7	15 pF	–	4.7	7.2	1.0	8.5	1.0	9.0	ns
	propagation delay $n\overline{E}$ to $n\overline{Y}_n$	see Figs 6 and 7		–	3.6	6.3	1.0	7.5	1.0	8.0	ns
	propagation delay nA_n to $n\overline{Y}_n$	see Figs 5 and 7	50 pF	–	6.5	9.2	1.0	10.5	1.0	11.5	ns
	propagation delay $n\overline{E}$ to $n\overline{Y}_n$	see Figs 6 and 7		–	5.2	8.3	1.0	9.5	1.0	10.5	ns

Note

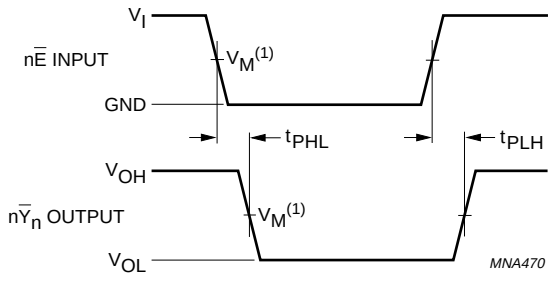
1. Typical values at V_{CC} = 5.0 V.

AC WAVEFORMS



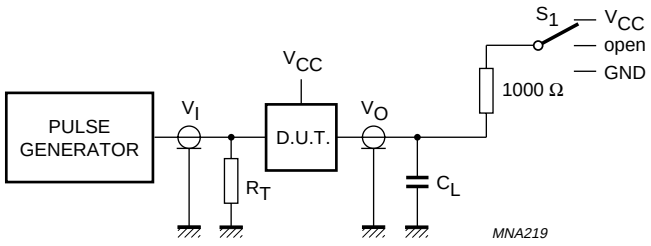
FAMILY	V_I INPUT REQUIREMENTS	V_M INPUT	V_M OUTPUT
AHC	GND to V_{CC}	50% V_{CC}	50% V_{CC}
AHCT	GND to 3.0 V	1.5 V	50% V_{CC}

Fig.5 The address input (nA_n) to output ($n\overline{Y}_n$) propagation delays.



FAMILY	V_I INPUT REQUIREMENTS	V_M INPUT	V_M OUTPUT
AHC	GND to V_{CC}	50% V_{CC}	50% V_{CC}
AHCT	GND to 3.0 V	1.5 V	50% V_{CC}

Fig.6 The enable input ($n\overline{E}$) to output ($n\overline{Y}_n$) propagation delays.



TEST	S_1
t_{PLH}/t_{PHL}	open
t_{PLZ}/t_{PZL}	V_{CC}
t_{PHZ}/t_{PZH}	GND

Definitions for test circuit:

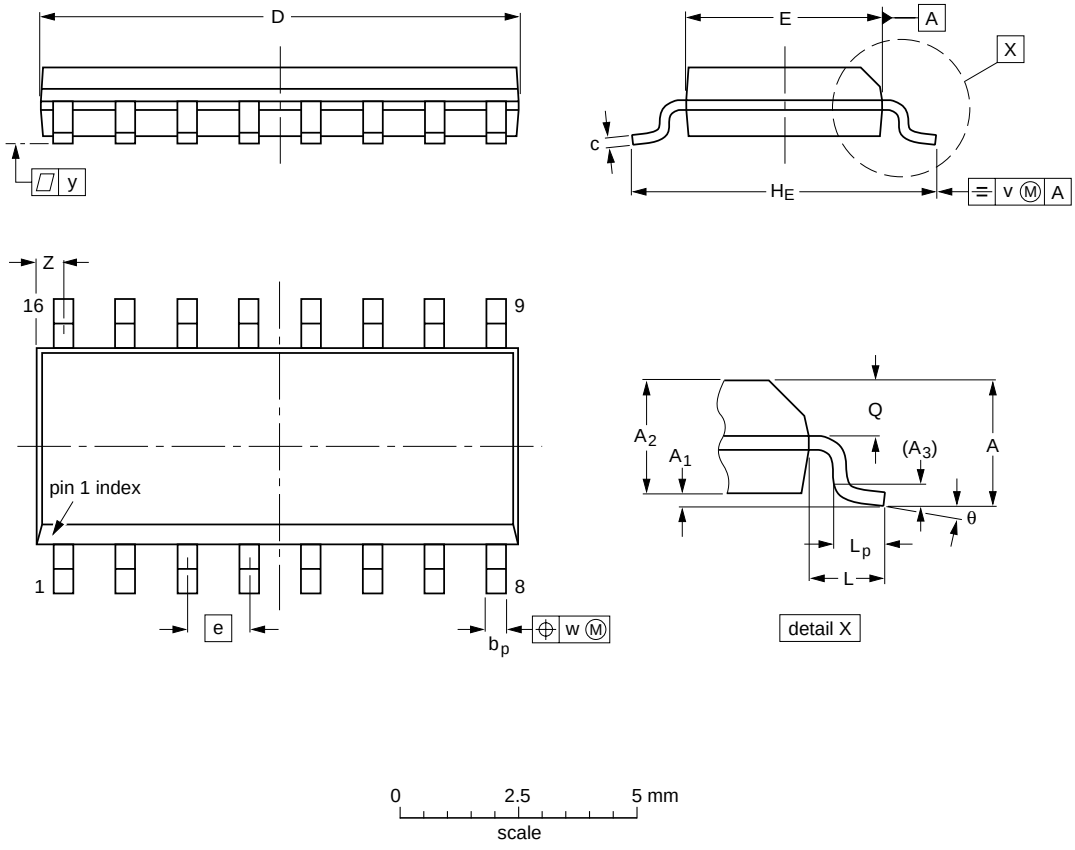
C_L = Load capacitance including jig and probe capacitance. (See Chapter “AC characteristics” for values).

R_T = Termination resistance should be equal to the output impedance Z_o of the pulse generator.

Fig.7 Load circuitry for switching times.

PACKAGE OUTLINES

SO16: plastic small outline package; 16 leads; body width 3.9 mm **SOT109-1**



DIMENSIONS (inch dimensions are derived from the original mm dimensions)

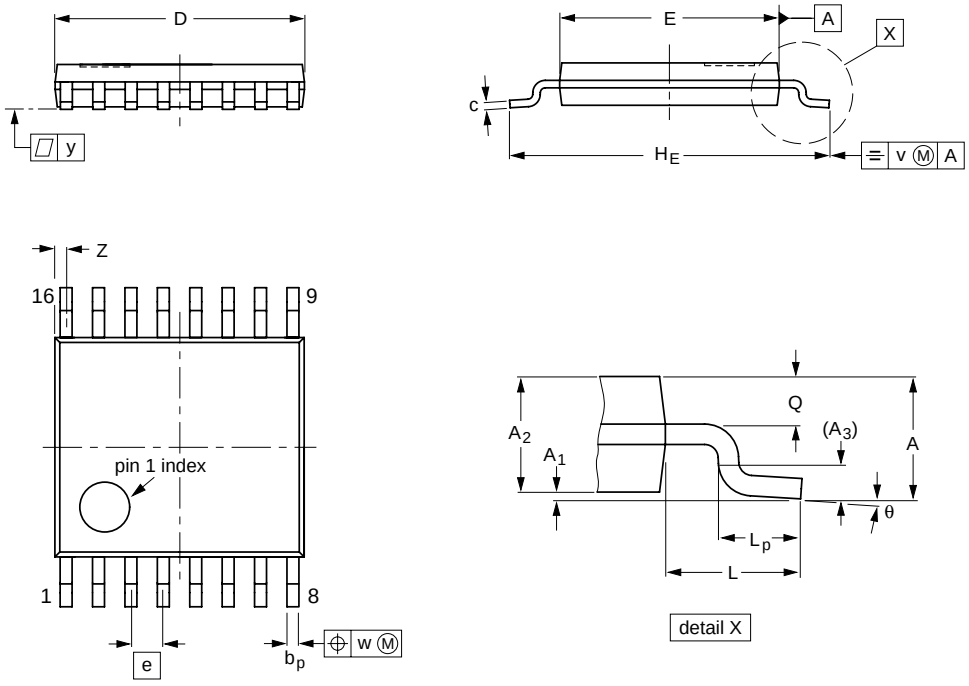
UNIT	A max.	A_1	A_2	A_3	b_p	c	$D^{(1)}$	$E^{(1)}$	e	H_E	L	L_p	Q	v	w	y	$Z^{(1)}$	θ
mm	1.75	0.25 0.10	1.45 1.25	0.25	0.49 0.36	0.25 0.19	10.0 9.8	4.0 3.8	1.27	6.2 5.8	1.05	1.0 0.4	0.7 0.6	0.25	0.25	0.1	0.7 0.3	8^o 0^o
inches	0.069	0.010 0.004	0.057 0.049	0.01	0.019 0.014	0.0100 0.0075	0.39 0.38	0.16 0.15	0.050	0.244 0.228	0.041	0.039 0.016	0.028 0.020	0.01	0.01	0.004	0.028 0.012	

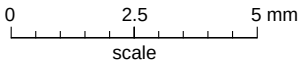
Note

1. Plastic or metal protrusions of 0.15 mm maximum per side are not included.

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	EIAJ			
SOT109-1	076E07S	MS-012AC				~~95-01-23~~ 97-05-22

TSSOP16: plastic thin shrink small outline package; 16 leads; body width 4.4 mm **SOT403-1**





DIMENSIONS (mm are the original dimensions)

UNIT	A max.	A_1	A_2	A_3	b_p	c	D (1)	E (2)	e	H_E	L	L_p	Q	v	w	y	Z (1)	θ
mm	1.10	0.15 0.05	0.95 0.80	0.25	0.30 0.19	0.2 0.1	5.1 4.9	4.5 4.3	0.65	6.6 6.2	1.0	0.75 0.50	0.4 0.3	0.2	0.13	0.1	0.40 0.06	8^o 0^o

Notes

1. Plastic or metal protrusions of 0.15 mm maximum per side are not included.
2. Plastic interlead protrusions of 0.25 mm maximum per side are not included.

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	EIAJ			
SOT403-1		MO-153				~~94-07-12~~ 95-04-04

SOLDERING

Introduction to soldering surface mount packages

This text gives a very brief insight to a complex technology. A more in-depth account of soldering ICs can be found in our *"Data Handbook IC26; Integrated Circuit Packages"* (document order number 9398 652 90011).

There is no soldering method that is ideal for all surface mount IC packages. Wave soldering is not always suitable for surface mount ICs, or for printed-circuit boards with high population densities. In these situations reflow soldering is often used.

Reflow soldering

Reflow soldering requires solder paste (a suspension of fine solder particles, flux and binding agent) to be applied to the printed-circuit board by screen printing, stencilling or pressure-syringe dispensing before package placement.

Several methods exist for reflowing; for example, infrared/convection heating in a conveyor type oven. Throughput times (preheating, soldering and cooling) vary between 100 and 200 seconds depending on heating method.

Typical reflow peak temperatures range from 215 to 250 °C. The top-surface temperature of the packages should preferable be kept below 230 °C.

Wave soldering

Conventional single wave soldering is not recommended for surface mount devices (SMDs) or printed-circuit boards with a high component density, as solder bridging and non-wetting can present major problems.

To overcome these problems the double-wave soldering method was specifically developed.

If wave soldering is used the following conditions must be observed for optimal results:

- Use a double-wave soldering method comprising a turbulent wave with high upward pressure followed by a smooth laminar wave.
- For packages with leads on two sides and a pitch (e):
  - larger than or equal to 1.27 mm, the footprint longitudinal axis is **preferred** to be parallel to the transport direction of the printed-circuit board;
  - smaller than 1.27 mm, the footprint longitudinal axis **must** be parallel to the transport direction of the printed-circuit board.

  The footprint must incorporate solder thieves at the downstream end.
- For packages with leads on four sides, the footprint must be placed at a 45° angle to the transport direction of the printed-circuit board. The footprint must incorporate solder thieves downstream and at the side corners.

During placement and before soldering, the package must be fixed with a droplet of adhesive. The adhesive can be applied by screen printing, pin transfer or syringe dispensing. The package can be soldered after the adhesive is cured.

Typical dwell time is 4 seconds at 250 °C.
A mildly-activated flux will eliminate the need for removal of corrosive residues in most applications.

Manual soldering

Fix the component by first soldering two diagonally-opposite end leads. Use a low voltage (24 V or less) soldering iron applied to the flat part of the lead. Contact time must be limited to 10 seconds at up to 300 °C.

When using a dedicated tool, all other leads can be soldered in one operation within 2 to 5 seconds between 270 and 320 °C.

Suitability of surface mount IC packages for wave and reflow soldering methods

PACKAGE	SOLDERING METHOD	
	WAVE	REFLOW(1)
BGA, SQFP	not suitable	suitable
HLQFP, HSQFP, HSOP, HTQFP, HTSSOP, SMS	not suitable(2)	suitable
PLCC(3), SO, SOJ	suitable	suitable
LQFP, QFP, TQFP	not recommended(3)(4)	suitable
SSOP, TSSOP, VSO	not recommended(5)	suitable

Notes

1. All surface mount (SMD) packages are moisture sensitive. Depending upon the moisture content, the maximum temperature (with respect to time) and body size of the package, there is a risk that internal or external package cracks may occur due to vaporization of the moisture in them (the so called popcorn effect). For details, refer to the Drypack information in the *"Data Handbook IC26; Integrated Circuit Packages; Section: Packing Methods"*.
2. These packages are not suitable for wave soldering as a solder joint between the printed-circuit board and heatsink (at bottom version) can not be achieved, and as solder may stick to the heatsink (on top version).
3. If wave soldering is considered, then the package must be placed at a 45° angle to the solder wave direction. The package footprint must incorporate solder thieves downstream and at the side corners.
4. Wave soldering is only suitable for LQFP, TQFP and QFP packages with a pitch (e) equal to or larger than 0.8 mm; it is definitely not suitable for packages with a pitch (e) equal to or smaller than 0.65 mm.
5. Wave soldering is only suitable for SSOP and TSSOP packages with a pitch (e) equal to or larger than 0.65 mm; it is definitely not suitable for packages with a pitch (e) equal to or smaller than 0.5 mm.

DEFINITIONS

Data sheet status	
Objective specification	This data sheet contains target or goal specifications for product development.
Preliminary specification	This data sheet contains preliminary data; supplementary data may be published later.
Product specification	This data sheet contains final product specifications.
Limiting values	
Limiting values given are in accordance with the Absolute Maximum Rating System (IEC 134). Stress above one or more of the limiting values may cause permanent damage to the device. These are stress ratings only and operation of the device at these or at any other conditions above those given in the Characteristics sections of the specification is not implied. Exposure to limiting values for extended periods may affect device reliability.	
Application information	
Where application information is given, it is advisory and does not form part of the specification.	

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DATA SHEET

For a complete data sheet, please also download:

- The IC06 74HC/HCT/HCU/HCMOS Logic Family Specifications
- The IC06 74HC/HCT/HCU/HCMOS Logic Package Information
- The IC06 74HC/HCT/HCU/HCMOS Logic Package Outlines

74HC/HCT08
Quad 2-input AND gate

Product specification
File under Integrated Circuits, IC06

December 1990

Philips
Semiconductors

PHILIPS

Quad 2-input AND gate 74HC/HCT08

FEATURES

- Output capability: standard
- I_{CC} category: SSI

GENERAL DESCRIPTION

The 74HC/HCT08 are high-speed Si-gate CMOS devices and are pin compatible with low power Schottky TTL (LSTTL). They are specified in compliance with JEDEC standard no. 7A. The 74HC/HCT08 provide the 2-input AND function.

QUICK REFERENCE DATA

GND = 0 V; T_{amb} = 25 °C; $t_r = t_f$ = 6 ns

SYMBOL	PARAMETER	CONDITIONS	TYPICAL		UNIT
			HC	HCT	
t_{PHL}/ t_{PLH}	propagation delay nA, nB to nY	C_L = 15 pF; V_{CC} = 5 V	7	11	ns
C_I	input capacitance		3.5	3.5	pF
C_{PD}	power dissipation capacitance per gate	notes 1 and 2	10	20	pF

Notes

1. C_{PD} is used to determine the dynamic power dissipation (P_D in μW):

   $P_D = C_{PD} \times V_{CC}^2 \times f_i + \sum (C_L \times V_{CC}^2 \times f_o)$ where:

   f_i = input frequency in MHz

   f_o = output frequency in MHz

   C_L = output load capacitance in pF

   V_{CC} = supply voltage in V

   $\sum (C_L \times V_{CC}^2 \times f_o)$ = sum of outputs

2. For HC the condition is V_I = GND to V_{CC}
   For HCT the condition is V_I = GND to V_{CC} –1.5 V

ORDERING INFORMATION

See *"74HC/HCT/HCU/HCMOS Logic Package Information"*.

PIN DESCRIPTION

PIN NO.	SYMBOL	NAME AND FUNCTION
1, 4, 9, 12	1A to 4A	data inputs
2, 5, 10, 13	1B to 4B	data inputs
3, 6, 8, 11	1Y to 4Y	data outputs
7	GND	ground (0 V)
14	V_{CC}	positive supply voltage

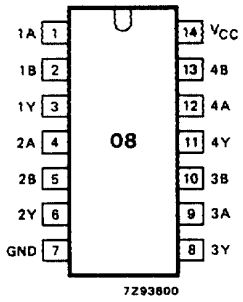


Fig.1 Pin configuration.

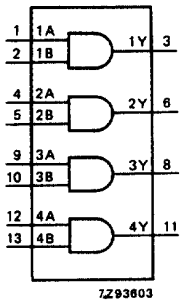


Fig.2 Logic symbol.

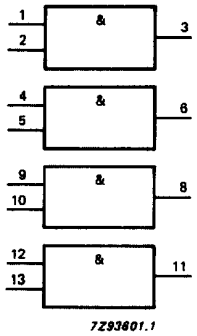


Fig.3 IEC logic symbol.

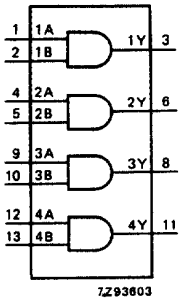


Fig.4 Functional diagram.

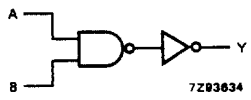


Fig.5 HC logic diagram (one gate).

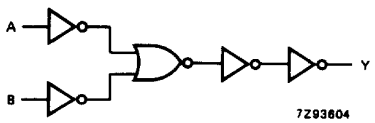


Fig.6 HCT logic diagram (one gate).

FUNCTION TABLE

INPUTS		OUTPUT
nA	nB	nY
L	L	L
L	H	L
H	L	L
H	H	H

Note

1. H = HIGH voltage level
   L = LOW voltage level

DC CHARACTERISTICS FOR 74HC

For the DC characteristics see *"74HC/HCT/HCU/HCMOS Logic Family Specifications"*.

Output capability: standard
I_{CC} category: SSI

AC CHARACTERISTICS FOR 74HC

GND = 0 V; $t_r = t_f$ = 6 ns; C_L = 50 pF

SYMBOL	PARAMETER	T_{amb} (°C)							UNIT	TEST CONDITIONS	
		74HC								V_{CC} (V)	WAVEFORMS
		+25			–40 to +85		–40 to +125				
		min.	typ.	max.	min.	max.	min.	max.			
t_{PHL}/ t_{PLH}	propagation delay nA, nB to nY		25 9 7	90 18 15		115 23 20		135 27 23	ns	2.0 4.5 6.0	Fig.7
t_{THL}/ t_{TLH}	output transition time		19 7 6	75 15 13		95 19 16		110 22 19	ns	2.0 4.5 6.0	Fig.7

DC CHARACTERISTICS FOR 74HCT

For the DC characteristics see *"74HC/HCT/HCU/HCMOS Logic Family Specifications"*.

Output capability: standard
I_{CC} category: SSI

Note to HCT types

The value of additional quiescent supply current (ΔI_{CC}) for a unit load of 1 is given in the family specifications.
To determine ΔI_{CC} per input, multiply this value by the unit load coefficient shown in the table below.

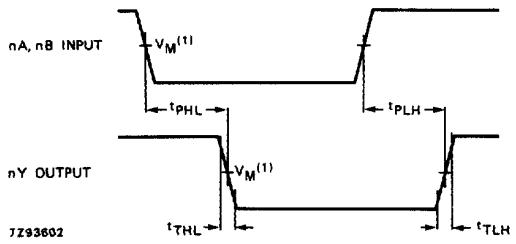
INPUT	UNIT LOAD COEFFICIENT
nA, nB	0.6

AC CHARACTERISTICS FOR 74HCT

GND = 0 V; $t_r = t_f$ = 6 ns; C_L = 50 pF

SYMBOL	PARAMETER	T_{amb} (°C)							UNIT	TEST CONDITIONS	
		74HCT								V_{CC} (V)	WAVEFORMS
		+25			–40 to +85		–40 to +125				
		min.	typ.	max.	min.	max.	min.	max.			
t_{PHL}/ t_{PLH}	propagation delay nA, nB to nY		14	24		30		36	ns	4.5	Fig.7
t_{THL}/ t_{TLH}	output transition time		7	15		19		22	ns	4.5	Fig.7

AC WAVEFORMS



(1) HC : V_M = 50%; V_I = GND to V_{CC}.
HCT: V_M = 1.3 V; V_I = GND to 3 V.

Fig.7 Waveforms showing the input (nA, nB) to output (nY) propagation delays and the output transition times.

PACKAGE OUTLINES

See *"74HC/HCT/HCU/HCMOS Logic Package Outlines"*.

DATA SHEET

For a complete data sheet, please also download:

- The IC06 74HC/HCT/HCU/HCMOS Logic Family Specifications
- The IC06 74HC/HCT/HCU/HCMOS Logic Package Information
- The IC06 74HC/HCT/HCU/HCMOS Logic Package Outlines

74HC/HCT32
Quad 2-input OR gate

Product specification
File under Integrated Circuits, IC06

December 1990

Philips
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Quad 2-input OR gate 74HC/HCT32

FEATURES

- Output capability: standard
- I_{CC} category: SSI

GENERAL DESCRIPTION

The 74HC/HCT32 are high-speed Si-gate CMOS devices and are pin compatible with low power Schottky TTL (LSTTL). They are specified in compliance with JEDEC standard no. 7A.

The 74HC/HCT32 provide the 2-input OR function.

QUICK REFERENCE DATA

GND = 0 V; T_{amb} = 25 °C; $t_r = t_f$ = 6 ns

SYMBOL	PARAMETER	CONDITIONS	TYPICAL		UNIT
			HC	HCT	
t_{PHL}/ t_{PLH}	propagation delay nA, nB to nY	C_L = 15 pF; V_{CC} = 5 V	6	9	ns
C_I	input capacitance		3.5	3.5	pF
C_{PD}	power dissipation capacitance per gate	notes 1 and 2	16	28	pF

Notes

1. C_{PD} is used to determine the dynamic power dissipation (P_D in µW):

   $P_D = C_{PD} \times V_{CC}^2 \times f_i + \sum (C_L \times V_{CC}^2 \times f_o)$ where:

   f_i = input frequency in MHz
   f_o = output frequency in MHz
   $\sum (C_L \times V_{CC}^2 \times f_o)$ = sum of outputs
   C_L = output load capacitance in pF
   V_{CC} = supply voltage in V

2. For HC the condition is V_I = GND to V_{CC}
   For HCT the condition is V_I = GND to V_{CC} – 1.5 V

ORDERING INFORMATION

See *"74HC/HCT/HCU/HCMOS Logic Package Information"*.

PIN DESCRIPTION

PIN NO.	SYMBOL	NAME AND FUNCTION
1, 4, 9, 12	1A to 4A	data inputs
2, 5, 10, 13	1B to 4B	data inputs
3, 6, 8, 11	1Y to 4Y	data outputs
7	GND	ground (0 V)
14	V_{CC}	positive supply voltage

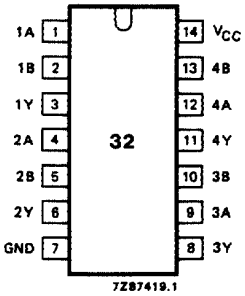


Fig.1 Pin configuration.

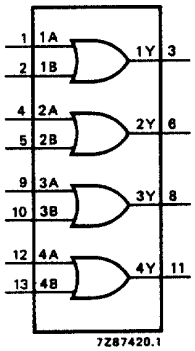


Fig.2 Logic symbol.

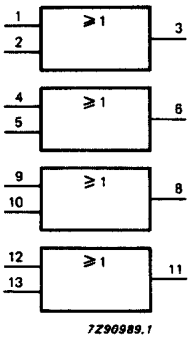


Fig.3 IEC logic symbol.

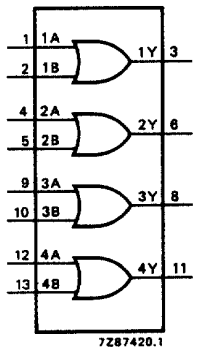


Fig.4 Functional diagram.

FUNCTION TABLE

INPUTS		OUTPUT
nA	**nB**	**nY**
L	L	L
L	H	H
H	L	H
H	H	H

Notes

1. H = HIGH voltage level
   L = LOW voltage level

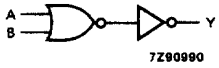


Fig.5 Logic diagram 74HC (one gate).

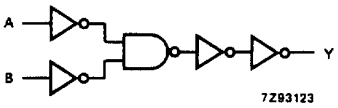


Fig.6 Logic diagram 74HCT (one gate).

DC CHARACTERISTICS FOR 74HC

For the DC characteristics see *"74HC/HCT/HCU/HCMOS Logic Family Specifications"*.

Output capability: standard
I_{CC} category: SSI

AC CHARACTERISTICS FOR 74HC

GND = 0 V; $t_r = t_f$ = 6 ns; C_L = 50 pF

SYMBOL	PARAMETER	T_{amb} (°C)							UNIT	TEST CONDITIONS	
		74HC								V_{CC} (V)	WAVEFORMS
		+25			−40 to +85		−40 to +125				
		min.	typ.	max.	min.	max.	min.	max.			
t_{PHL}/ t_{PLH}	propagation delay nA, nB to nY		22 8 6	90 18 15		115 23 20		135 27 23	ns	2.0 4.5 6.0	Fig.7
t_{THL}/ t_{TLH}	output transition time		19 7 6	75 15 13		95 19 16		110 22 19	ns	2.0 4.5 6.0	Fig.7

DC CHARACTERISTICS FOR 74HCT

For the DC characteristics see *"74HC/HCT/HCU/HCMOS Logic Family Specifications"*.

Output capability: standard
I_{CC} category: SSI

Note to HCT types

The value of additional quiescent supply current (ΔI_{CC}) for a unit load of 1 is given in the family specifications. To determine ΔI_{CC} per input, multiply this value by the unit load coefficient shown in the table below.

INPUT	UNIT LOAD COEFFICIENT
nA, nB	1.20

AC CHARACTERISTICS FOR 74HCT

GND = 0 V; $t_r = t_f$ = 6 ns; C_L = 50 pF

SYMBOL	PARAMETER	T_{amb} (°C)							UNIT	TEST CONDITIONS	
		74HCT								V_{CC} (V)	WAVEFORMS
		+25			−40 to +85		−40 to +125				
		min.	typ.	max.	min.	max.	min.	max.			
t_{PHL}/ t_{PLH}	propagation delay nA, nB to nY		11	24		30		36	ns	4.5	Fig.7
t_{THL}/ t_{TLH}	output transition time		7	15		19		22	ns	4.5	Fig.7

AC WAVEFORMS

(1) HC : V_M = 50%; V_I = GND to V_{CC}.
HCT: V_M = 1.3 V; V_I = GND to 3 V.

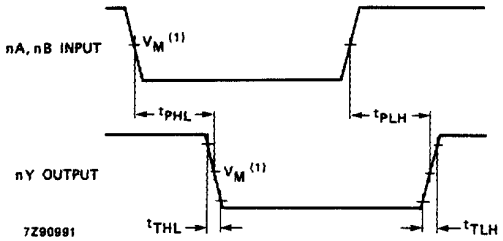


Fig.7 Waveforms showing the input (nA, nB) to output (nY) propagation delays and the output transition times.

PACKAGE OUTLINES

See *"74HC/HCT/HCU/HCMOS Logic Package Outlines"*.

DATA SHEET

74HC1G04; 74HCT1G04
Inverter

Product specification
Supersedes data of 2001 Mar 02

2002 May 17

Philips
Semiconductors

PHILIPS

FEATURES

- Wide supply voltage range from 2.0 to 6.0 V
- Symmetrical output impedance
- High noise immunity
- Low power dissipation
- Balanced propagation delays
- Very small 5 pins package
- Output capability: standard.

DESCRIPTION

The 74HC1G/HCT1G04 is a high-speed Si-gate CMOS device.

The 74HC1G/HCT1G04 provides the inverting buffer. The standard output currents are half the values compared to the 74HC/HCT04.

QUICK REFERENCE DATA

GND = 0 V; T_{amb} = 25 °C; $t_r = t_f \leq 6.0$ ns.

SYMBOL	PARAMETER	CONDITIONS	TYPICAL		UNIT
			HC1G	HCT1G	
t_{PHL}/t_{PLH}	propagation delay A to Y	C_L = 15 pF; V_{CC} = 5 V	7	8	ns
C_I	input capacitance		1.5	1.5	pF
C_{PD}	power dissipation capacitance	notes 1 and 2	16	18	pF

Notes

1. C_{PD} is used to determine the dynamic power dissipation (P_D in μW).
   $P_D = C_{PD} \times V_{CC}^2 \times f_i + \sum (C_L \times V_{CC}^2 \times f_o)$ where:
   f_i = input frequency in MHz;
   f_o = output frequency in MHz;
   C_L = output load capacitance in pF;
   V_{CC} = supply voltage in Volts;
   $\sum (C_L \times V_{CC}^2 \times f_o)$ = sum of outputs.
2. For HC1G the condition is V_I = GND to V_{CC}.
   For HCT1G the condition is V_I = GND to V_{CC} − 1.5 V.

FUNCTION TABLE

See note 1.

INPUT	OUTPUT
A	Y
L	H
H	L

Note

1. H = HIGH voltage level;
   L = LOW voltage level.

ORDERING INFORMATION

TYPE NUMBER	PACKAGES					
	TEMPERATURE RANGE	PINS	PACKAGE	MATERIAL	CODE	MARKING
74HC1G04GW	–40 to +125 °C	5	SC-88A	plastic	SOT353	HC
74HCT1G04GW	–40 to +125 °C	5	SC-88A	plastic	SOT353	TC
74HC1G04GV	–40 to +125 °C	5	SC-74A	plastic	SOT753	H04
74HCT1G04GV	–40 to +125 °C	5	SC-74A	plastic	SOT753	T04

PINNING

PIN	SYMBOL	DESCRIPTION
1	n.c.	not connected
2	A	data input A
3	GND	ground (0 V)
4	Y	data output Y
5	V_{CC}	supply voltage

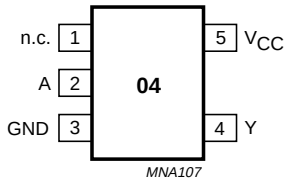


Fig.1 Pin configuration.

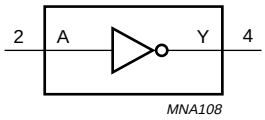


Fig.2 Logic symbol.

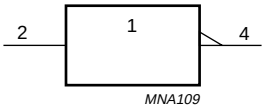


Fig.3 IEC logic symbol.

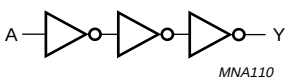


Fig.4 Logic diagram.

RECOMMENDED OPERATING CONDITIONS

SYMBOL	PARAMETER	CONDITIONS	74HC1G04			74HCT1G04			UNIT
			MIN.	TYP.	MAX.	MIN.	TYP.	MAX.	
V_{CC}	supply voltage		2.0	5.0	6.0	4.5	5.0	5.5	V
V_I	input voltage		0	–	V_{CC}	0	–	V_{CC}	V
V_O	output voltage		0	–	V_{CC}	0	–	V_{CC}	V
T_{amb}	operating ambient temperature	see DC and AC characteristics per device	–40	+25	+125	–40	+25	+125	°C
t_r, t_f	input rise and fall times	V_{CC} = 2.0 V	–	–	1000	–	–	–	ns
		V_{CC} = 4.5 V	–	–	500	–	–	500	ns
		V_{CC} = 6.0 V	–	–	400	–	–	–	ns

LIMITING VALUES

In accordance with the Absolute Maximum Rating System (IEC 60134); voltages are referenced to GND (ground = 0 V).

SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.	UNIT
V_{CC}	supply voltage		–0.5	+7.0	V
I_{IK}	input diode current	$V_I < –0.5$ V or $V_I > V_{CC}$ + 0.5 V; note 1	–	±20	mA
I_{OK}	output diode current	$V_O < –0.5$ V or $V_O > V_{CC}$ + 0.5 V; note 1	–	±20	mA
I_O	output source or sink current	$–0.5 \text{ V} < V_O < V_{CC} + 0.5$ V; note 1	–	±12.5	mA
I_{CC}	V_{CC} or GND current	note 1	–	±25	mA
T_{stg}	storage temperature		–65	+150	°C
P_D	power dissipation per package	for temperature range from –40 to +125 °C; note 2	–	200	mW

Notes

1. The input and output voltage ratings may be exceeded if the input and output current ratings are observed.
2. Above 55 °C the value of P_D derates linearly with 2.5 mW/K.

DC CHARACTERISTICS

Family 74HC1G04

At recommended operating conditions; voltages are referenced to GND (ground = 0 V).

SYMBOL	PARAMETER	TEST CONDITIONS		T_{amb} (°C)					UNIT
		OTHER	V_{CC} (V)	–40 to +85			–40 to +125		
				MIN.	TYP.(1)	MAX.	MIN.	MAX.	
V_{IH}	HIGH-level input voltage		2.0	1.5	1.2	–	1.5	–	V
			4.5	3.15	2.4	–	3.15	–	V
			6.0	4.2	3.2	–	4.2	–	V
V_{IL}	LOW-level input voltage		2.0	–	0.8	0.5	–	0.5	V
			4.5	–	2.1	1.35	–	1.35	V
			6.0	–	2.8	1.8	–	1.8	V
V_{OH}	HIGH-level output voltage	$V_I = V_{IH}$ or V_{IL}; $I_O = -20$ μA	2.0	1.9	2.0	–	1.9	–	V
		$V_I = V_{IH}$ or V_{IL}; $I_O = -20$ μA	4.5	4.4	4.5	–	4.4	–	V
		$V_I = V_{IH}$ or V_{IL}; $I_O = -20$ μA	6.0	5.9	6.0	–	5.9	–	V
		$V_I = V_{IH}$ or V_{IL}; $I_O = -2.0$ mA	4.5	4.13	4.32	–	3.7	–	V
		$V_I = V_{IH}$ or V_{IL}; $I_O = -2.6$ mA	6.0	5.63	5.81	–	5.2	–	V
V_{OL}	LOW-level output voltage	$V_I = V_{IH}$ or V_{IL}; $I_O = 20$ μA	2.0	–	0	0.1	–	0.1	V
		$V_I = V_{IH}$ or V_{IL}: $I_O = -20$ μA	4.5	–	0	0.1	–	0.1	V
		$V_I = V_{IH}$ or V_{IL}: $I_O = -20$ μA	6.0	–	0	0.1	–	0.1	V
		$V_I = V_{IH}$ or V_{IL}; $I_O = 2.0$ mA	4.5	–	0.15	0.33	–	0.4	V
		$V_I = V_{IH}$ or V_{IL}; $I_O = 2.6$ mA	6.0	–	0.16	0.33	–	0.4	V
I_{LI}	input leakage current	$V_I = V_{CC}$ or GND	6.0	–	–	1.0	–	1.0	μA
I_{CC}	quiescent supply current	$V_I = V_{CC}$ or GND; $I_O = 0$	6.0	–	–	10	–	20	μA

Note

1. All typical values are measured at T_{amb} = 25 °C.

Family 74HCT1G04

At recommended operating conditions; voltages are referenced to GND (ground = 0 V).

SYMBOL	PARAMETER	TEST CONDITIONS		T_{amb} (°C)					UNIT
		OTHER	V_{CC} (V)	–40 to +85			–40 to +125		
				MIN.	TYP.(1)	MAX.	MIN.	MAX.	
V_{IH}	HIGH-level input voltage		4.5 to 5.5	2.0	1.6	–	2.0	–	V
V_{IL}	LOW-level input voltage		4.5 to 5.5	–	1.2	0.8	–	0.8	V
V_{OH}	HIGH-level output voltage	$V_I = V_{IH}$ or V_{IL}; $I_O = -20$ μA	4.5	4.4	4.5	–	4.4	–	V
		$V_I = V_{IH}$ or V_{IL}; $I_O = -2.0$ mA	4.5	4.13	4.32	–	3.7	–	V
V_{OL}	LOW-level output voltage	$V_I = V_{IH}$ or V_{IL}; $I_O = 20$ μA	4.5	–	0	0.1	–	0.1	V
		$V_I = V_{IH}$ or V_{IL}; $I_O = 2.0$ mA	4.5	–	0.15	0.33	–	0.4	V
I_{LI}	input leakage current	$V_I = V_{CC}$ or GND	5.5	–	–	1.0	–	1.0	μA
I_{CC}	quiescent supply current	$V_I = V_{CC}$ or GND; $I_O = 0$	5.5	–	–	10	–	20	μA
ΔI_{CC}	additional supply current per input	$V_I = V_{CC} - 2.1$ V; $I_O = 0$	4.5 to 5.5	–	–	500	–	850	μA

Note

1. All typical values are measured at $T_{amb} = 25$ °C.

AC CHARACTERISTICS

Type 74HC1G04

GND = 0 V; $t_r = t_f \leq 6.0$ ns; $C_L = 50$ pF.

SYMBOL	PARAMETER	TEST CONDITIONS		T_{amb} (°C)					UNIT
		WAVEFORMS	V_{CC} (V)	−40 to +85			−40 to +125		
				MIN.	TYP.(1)	MAX.	MIN.	MAX.	
t_{PHL}/t_{PLH}	propagation delay A to Y	see Figs 5 and 6	2.0	–	25	105	–	135	ns
			4.5	–	9	21	–	27	ns
			6.0	–	8	18	–	23	ns

Note

1. All typical values are measured at $T_{amb} = 25$ °C.

Type 74HCT1G04

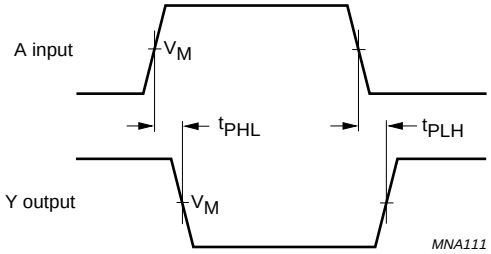
GND = 0 V; $t_r = t_f \leq 6.0$ ns; $C_L = 50$ pF.

SYMBOL	PARAMETER	TEST CONDITIONS		T_{amb} (°C)					UNIT
		WAVEFORMS	V_{CC} (V)	−40 to +85			−40 to +125		
				MIN.	TYP.(1)	MAX.	MIN.	MAX.	
t_{PHL}/t_{PLH}	propagation delay A to Y	see Figs 5 and 6	4.5	–	10	24	–	27	ns

Note

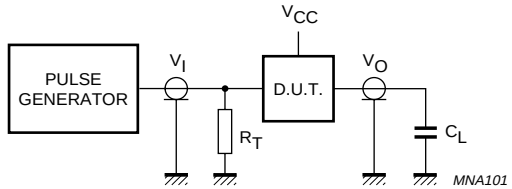
1. All typical values are measured at $T_{amb} = 25$ °C.

AC WAVEFORMS



For HC1G04: V_M = 50% and V_I = GND to V_{CC}.
For HCT1G04: V_M = 1.3 V and V_I = GND to 3.0 V.

Fig.5 The input (A) to output (Y) propagation delays.



Definitions for test circuit:

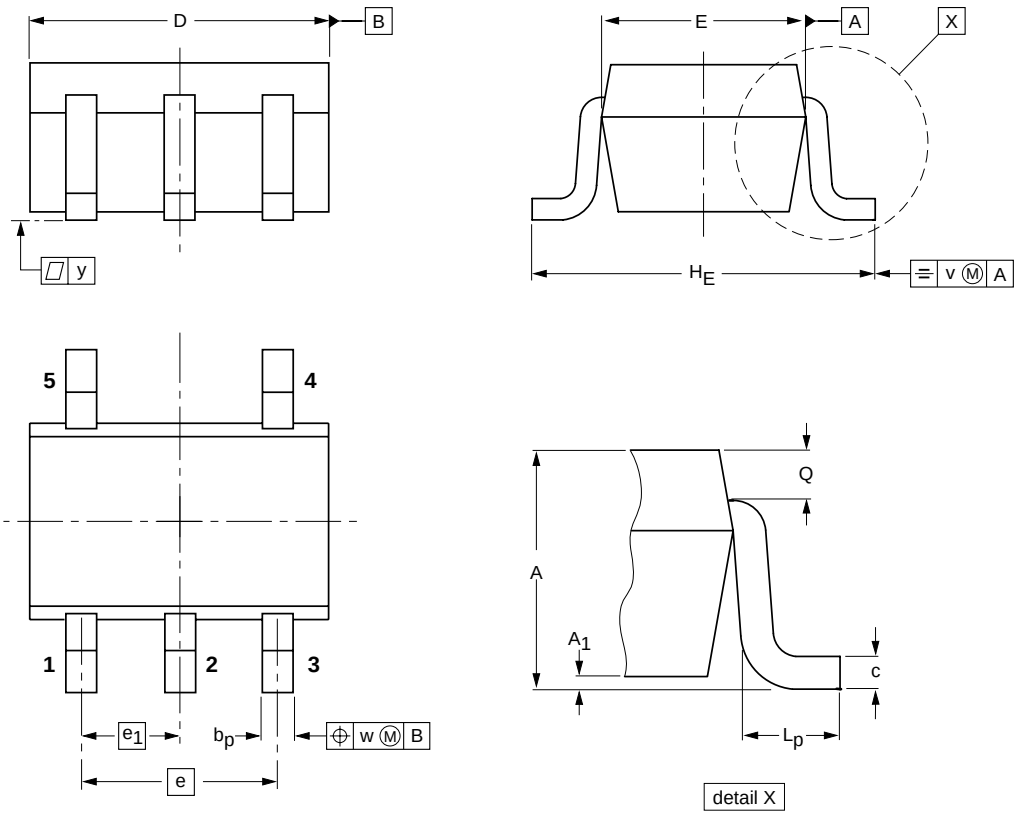
C_L = Load capacitance including jig and probe capacitance (see “AC characteristics”).

R_T = Termination resistance should be equal to the output impedance Z_o of the pulse generator.

Fig.6 Load circuitry for switching times.

PACKAGE OUTLINES

Plastic surface mounted package; 5 leads **SOT353**

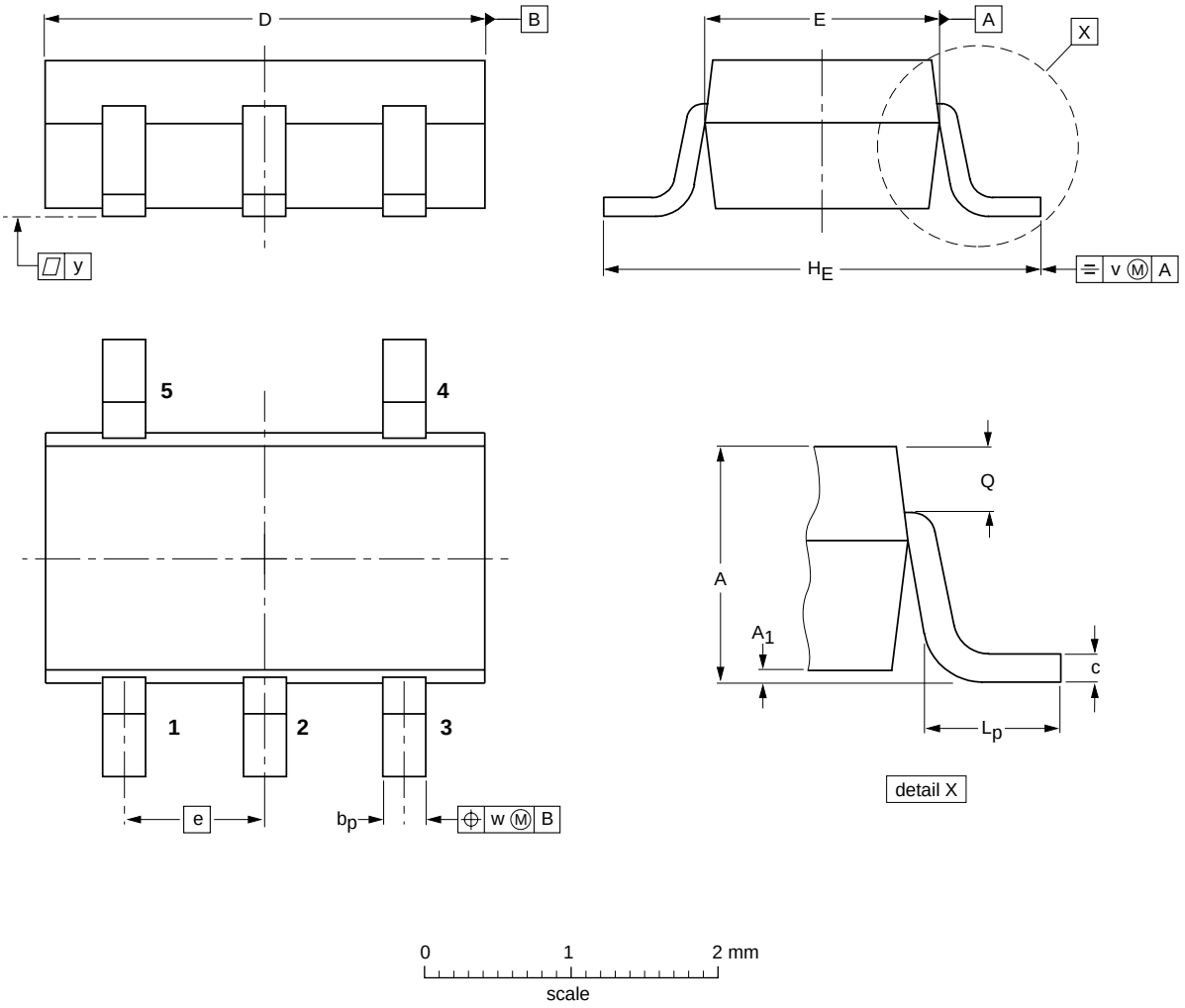


DIMENSIONS (mm are the original dimensions)

UNIT	A	A_1 max	b_p	c	D	E (2)	e	e_1	H_E	L_p	Q	v	w	y
mm	1.1 0.8	0.1	0.30 0.20	0.25 0.10	2.2 1.8	1.35 1.15	1.3	0.65	2.2 2.0	0.45 0.15	0.25 0.15	0.2	0.2	0.1

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	EIAJ			
SOT353			SC-88A			97-02-28

Plastic surface mounted package; 5 leads **SOT753**



DIMENSIONS (mm are the original dimensions)

UNIT	A	A_1	b_p	c	D	E	e	H_E	L_p	Q	v	w	y
mm	1.1 0.9	0.100 0.013	0.40 0.25	0.26 0.10	3.1 2.7	1.7 1.3	0.95	3.0 2.5	0.6 0.2	0.33 0.23	0.2	0.2	0.1

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	JEITA			
SOT753			SC-74A			02-04-16

SOLDERING

Introduction to soldering surface mount packages

This text gives a very brief insight to a complex technology. A more in-depth account of soldering ICs can be found in our *"Data Handbook IC26; Integrated Circuit Packages"* (document order number 9398 652 90011).

There is no soldering method that is ideal for all surface mount IC packages. Wave soldering can still be used for certain surface mount ICs, but it is not suitable for fine pitch SMDs. In these situations reflow soldering is recommended.

Reflow soldering

Reflow soldering requires solder paste (a suspension of fine solder particles, flux and binding agent) to be applied to the printed-circuit board by screen printing, stencilling or pressure-syringe dispensing before package placement.

Several methods exist for reflowing; for example, convection or convection/infrared heating in a conveyor type oven. Throughput times (preheating, soldering and cooling) vary between 100 and 200 seconds depending on heating method.

Typical reflow peak temperatures range from 215 to 250 °C. The top-surface temperature of the packages should preferable be kept below 220 °C for thick/large packages, and below 235 °C for small/thin packages.

Wave soldering

Conventional single wave soldering is not recommended for surface mount devices (SMDs) or printed-circuit boards with a high component density, as solder bridging and non-wetting can present major problems.

To overcome these problems the double-wave soldering method was specifically developed.

If wave soldering is used the following conditions must be observed for optimal results:

- Use a double-wave soldering method comprising a turbulent wave with high upward pressure followed by a smooth laminar wave.
- For packages with leads on two sides and a pitch (e):
  - larger than or equal to 1.27 mm, the footprint longitudinal axis is **preferred** to be parallel to the transport direction of the printed-circuit board;
  - smaller than 1.27 mm, the footprint longitudinal axis **must** be parallel to the transport direction of the printed-circuit board.

  The footprint must incorporate solder thieves at the downstream end.
- For packages with leads on four sides, the footprint must be placed at a 45° angle to the transport direction of the printed-circuit board. The footprint must incorporate solder thieves downstream and at the side corners.

During placement and before soldering, the package must be fixed with a droplet of adhesive. The adhesive can be applied by screen printing, pin transfer or syringe dispensing. The package can be soldered after the adhesive is cured.

Typical dwell time is 4 seconds at 250 °C.
A mildly-activated flux will eliminate the need for removal of corrosive residues in most applications.

Manual soldering

Fix the component by first soldering two diagonally-opposite end leads. Use a low voltage (24 V or less) soldering iron applied to the flat part of the lead. Contact time must be limited to 10 seconds at up to 300 °C.

When using a dedicated tool, all other leads can be soldered in one operation within 2 to 5 seconds between 270 and 320 °C.

Suitability of surface mount IC packages for wave and reflow soldering methods

PACKAGE[1]	SOLDERING METHOD	
	WAVE	REFLOW[2]
BGA, LBGA, LFBGA, SQFP, TFBGA, VFBGA	not suitable	suitable
HBCC, HBGA, HLQFP, HSQFP, HSOP, HTQFP, HTSSOP, HVQFN, HVSON, SMS	not suitable[3]	suitable
PLCC[4], SO, SOJ	suitable	suitable
LQFP, QFP, TQFP	not recommended[4][5]	suitable
SSOP, TSSOP, VSO	not recommended[6]	suitable

Notes

1. For more detailed information on the BGA packages refer to the *"(LF)BGA Application Note*" (AN01026); order a copy from your Philips Semiconductors sales office.
2. All surface mount (SMD) packages are moisture sensitive. Depending upon the moisture content, the maximum temperature (with respect to time) and body size of the package, there is a risk that internal or external package cracks may occur due to vaporization of the moisture in them (the so called popcorn effect). For details, refer to the Drypack information in the *"Data Handbook IC26; Integrated Circuit Packages; Section: Packing Methods"*.
3. These packages are not suitable for wave soldering. On versions with the heatsink on the bottom side, the solder cannot penetrate between the printed-circuit board and the heatsink. On versions with the heatsink on the top side, the solder might be deposited on the heatsink surface.
4. If wave soldering is considered, then the package must be placed at a 45° angle to the solder wave direction. The package footprint must incorporate solder thieves downstream and at the side corners.
5. Wave soldering is suitable for LQFP, TQFP and QFP packages with a pitch (e) larger than 0.8 mm; it is definitely not suitable for packages with a pitch (e) equal to or smaller than 0.65 mm.
6. Wave soldering is suitable for SSOP and TSSOP packages with a pitch (e) equal to or larger than 0.65 mm; it is definitely not suitable for packages with a pitch (e) equal to or smaller than 0.5 mm.

DATA SHEET STATUS

DATA SHEET STATUS[1]	PRODUCT STATUS[2]	DEFINITIONS
Objective data	Development	This data sheet contains data from the objective specification for product development. Philips Semiconductors reserves the right to change the specification in any manner without notice.
Preliminary data	Qualification	This data sheet contains data from the preliminary specification. Supplementary data will be published at a later date. Philips Semiconductors reserves the right to change the specification without notice, in order to improve the design and supply the best possible product.
Product data	Production	This data sheet contains data from the product specification. Philips Semiconductors reserves the right to make changes at any time in order to improve the design, manufacturing and supply. Changes will be communicated according to the Customer Product/Process Change Notification (CPCN) procedure SNW-SQ-650A.

Notes

1. Please consult the most recently issued data sheet before initiating or completing a design.
2. The product status of the device(s) described in this data sheet may have changed since this data sheet was published. The latest information is available on the Internet at URL http://www.semiconductors.philips.com.

DEFINITIONS

Short-form specification — The data in a short-form specification is extracted from a full data sheet with the same type number and title. For detailed information see the relevant data sheet or data handbook.

Limiting values definition — Limiting values given are in accordance with the Absolute Maximum Rating System (IEC 60134). Stress above one or more of the limiting values may cause permanent damage to the device. These are stress ratings only and operation of the device at these or at any other conditions above those given in the Characteristics sections of the specification is not implied. Exposure to limiting values for extended periods may affect device reliability.

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NOTES

NOTES

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DATA SHEET

For a complete data sheet, please also download:

- The IC06 74HC/HCT/HCU/HCMOS Logic Family Specifications
- The IC06 74HC/HCT/HCU/HCMOS Logic Package Information
- The IC06 74HC/HCT/HCU/HCMOS Logic Package Outlines

74HC/HCT11
Triple 3-input AND gate

Product specification
File under Integrated Circuits, IC06

December 1990

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Triple 3-input AND gate 74HC/HCT11

FEATURES

- Output capability: standard
- I_{CC} category: SSI

GENERAL DESCRIPTION

The 74HC/HCT11 are high-speed Si-gate CMOS devices and are pin compatible with low power Schottky TTL (LSTTL). They are specified in compliance with JEDEC standard no. 7A. The 74HC/HCT11 provide the 3-input AND function.

QUICK REFERENCE DATA

GND = 0 V; T_{amb} = 25 °C; $t_r = t_f$ = 6 ns

SYMBOL	PARAMETER	CONDITIONS	TYPICAL		UNIT
			HC	HCT	
t_{PHL}/ t_{PLH}	propagation delay nA, nB, nC to nY	C_L = 15 pF; V_{CC} = 5 V	10	11	ns
C_I	input capacitance		3.5	3.5	pF
C_{PD}	power dissipation capacitance per gate	notes 1 and 2	18	20	pF

Notes

1. C_{PD} is used to determine the dynamic power dissipation (P_D in μW):

   $P_D = C_{PD} \times V_{CC}^2 \times f_i + \sum (C_L \times V_{CC}^2 \times f_o)$ where:

   f_i = input frequency in MHz

   f_o = output frequency in MHz

   C_L = output load capacitance in pF

   V_{CC} = supply voltage in V

   $\sum (C_L \times V_{CC}^2 \times f_o)$ = sum of outputs

2. For HC the condition is V_I = GND to V_{CC}
   For HCT the condition is V_I = GND to V_{CC} – 1.5 V

ORDERING INFORMATION

See *"74HC/HCT/HCU/HCMOS Logic Package Information"*.

PIN DESCRIPTION

PIN NO.	SYMBOL	NAME AND FUNCTION
1, 3, 9	1A to 3A	data inputs
2, 4, 10	1B to 3B	data inputs
7	GND	ground (0 V)
12, 6, 8	1Y to 3Y	data outputs
13, 5, 11	1C to 3C	data inputs
14	V_{CC}	positive supply voltage

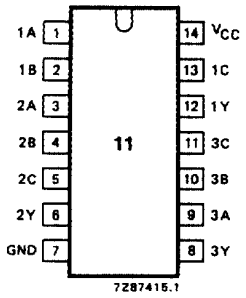


Fig.1 Pin configuration.

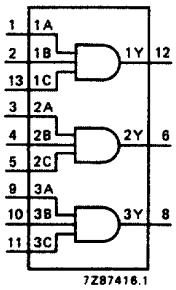


Fig.2 Logic symbol.

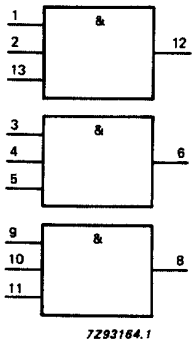


Fig.3 IEC logic symbol.

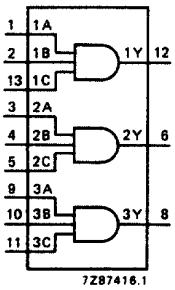


Fig.4 Functional diagram.

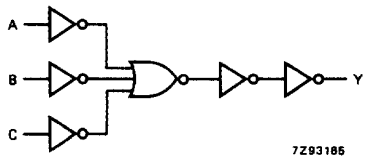


Fig.5 Logic diagram (one gate).

FUNCTION TABLE

INPUTS			OUTPUT
nA	nB	nC	nY
L	L	L	L
L	L	H	L
L	H	L	L
L	H	H	L
H	L	L	L
H	L	H	L
H	H	L	L
H	H	H	H

Notes

1. H = HIGH voltage level
   L = LOW voltage level

DC CHARACTERISTICS FOR 74HC

For the DC characteristics see *"74HC/HCT/HCU/HCMOS Logic Family Specifications"*.

Output capability: standard
I_{CC} category: SSI

AC CHARACTERISTICS FOR 74HC

GND = 0 V; $t_r = t_f$ = 6 ns; C_L = 50 pF

SYMBOL	PARAMETER	T_{amb} (°C)							UNIT	TEST CONDITIONS	
		74HC								V_{CC} (V)	WAVEFORMS
		+25			–40 to +85		–40 to +125				
		min.	typ.	max.	min.	max.	min.	max.			
t_{PHL}/ t_{PLH}	propagation delay nA, nB, nC to nY		32	100		125		150	ns	2.0	Fig.6
			12	20		25		30		4.5	
			10	17		21		26		6.0	
t_{THL}/ t_{TLH}	output transition times		19	75		95		110	ns	2.0	Fig.6
			7	15		19		22		4.5	
			6	13		16		19		6.0	

DC CHARACTERISTICS FOR 74HCT

For the DC characteristics see *"74HC/HCT/HCU/HCMOS Logic Family Specifications"*.

Output capability: standard
I_{CC} category: SSI

Note to HCT types

The value of additional quiescent supply current (ΔI_{CC}) for a unit load of 1 is given in the family specifications.
'To determine ΔI_{CC} per input, multiply this value by the unit load coefficient shown in the table below.

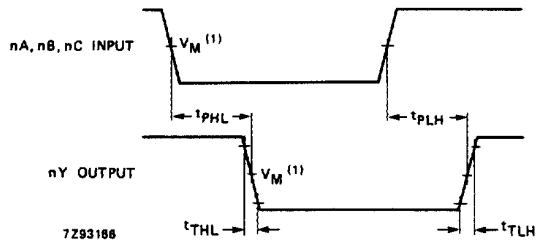
INPUT	UNIT LOAD COEFFICIENT
nA, nB, nC	1.00

AC CHARACTERISTICS FOR 74HCT

GND = 0 V; $t_r = t_f$ = 6 ns; C_L = 50 pF

SYMBOL	PARAMETER	T_{amb} (°C)							UNIT	TEST CONDITIONS	
		74HCT								V_{CC} (V)	WAVEFORMS
		+25			–40 to +85		–40 to +125				
		min.	typ.	max.	min.	max.	min.	max.			
t_{PHL}/ t_{PLH}	propagation delay nA, nB, nC to nY		16	24		30		36	ns	4.5	Fig.6
t_{THL}/ t_{TLH}	output transition times		7	15		19		22	ns	4.5	Fig.6

AC WAVEFORMS



(1) HC : V_M = 50%; V_I = GND to V_{CC}
HCT: V_M = 1.3 V; V_I = GND to 3 V.

Fig.6 Waveforms showing the input (nA, nB, nC) to output (nY) propagation delays and the output transition times.

PACKAGE OUTLINES

See *"74HC/HCT/HCU/HCMOS Logic Package Outlines"*.

DATA SHEET

For a complete data sheet, please also download:

- The IC06 74HC/HCT/HCU/HCMOS Logic Family Specifications
- The IC06 74HC/HCT/HCU/HCMOS Logic Package Information
- The IC06 74HC/HCT/HCU/HCMOS Logic Package Outlines

74HC/HCT4075
Triple 3-input OR gate

Product specification
File under Integrated Circuits, IC06

December 1990

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Triple 3-input OR gate 74HC/HCT4075

FEATURES

- Output capability: standard
- I_{CC} category: SSI

GENERAL DESCRIPTION

The 74HC/HCT4075 are high-speed Si-gate CMOS devices and are pin compatible with the “4075” of the “4000B” series. They are specified in compliance with JEDEC standard no. 7A.

The 74HC/HCT4075 provide the 3-input OR function.

QUICK REFERENCE DATA

GND = 0 V; T_{amb} = 25 °C; $t_r = t_f$ = 6 ns

SYMBOL	PARAMETER	CONDITIONS	TYPICAL		UNIT
			HC	HCT	
t_{PHL}/ t_{PLH}	propagation delay nA, nB, nC to nY	C_L = 15 pF; V_{CC} = 5 V	8	10	ns
C_I	input capacitance		3.5	3.5	pF
C_{PD}	power dissipation capacitance per gate	notes 1 and 2	28	32	pF

Notes

1. C_{PD} is used to determine the dynamic power dissipation (P_D in µW):

   $P_D = C_{PD} \times V_{CC}^2 \times f_i + \sum (C_L \times V_{CC}^2 \times f_o)$ where:

   f_i = input frequency in MHz

   f_o = output frequency in MHz

   $\sum (C_L \times V_{CC}^2 \times f_o)$ = sum of outputs

   C_L = output load capacitance in pF

   V_{CC} = supply voltage in V

2. For HC the condition is V_I = GND to V_{CC}
   For HCT the condition is V_I = GND to V_{CC} – 1.5 V

ORDERING INFORMATION

See *“74HC/HCT/HCU/HCMOS Logic Package Information”*.

PIN DESCRIPTION

PIN NO.	SYMBOL	NAME AND FUNCTION
3, 1, 11	1A to 3A	data inputs
4, 2, 12	1B to 3B	data inputs
5, 8, 13	1C to 3C	data inputs
6, 9, 10	1Y to 3Y	data outputs
7	GND	ground (0 V)
14	V_{CC}	positive supply voltage

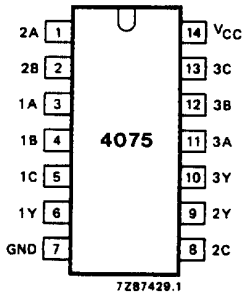


Fig.1 Pin configuration.

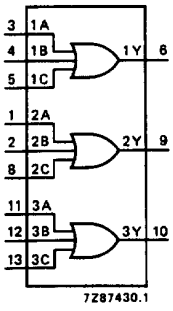


Fig.2 Logic symbol.

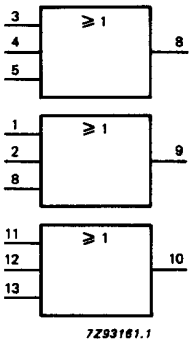


Fig.3 IEC logic symbol.

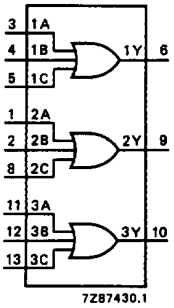


Fig.4 Functional diagram.

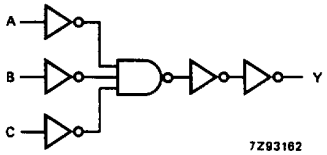


Fig.5 Logic diagram (one gate).

FUNCTION TABLE

INPUTS			OUTPUT
nA	nB	nC	nY
L	L	L	L
H	X	X	H
X	H	X	H
X	X	H	H

Notes

1. H = HIGH voltage level
   L = LOW voltage level
   X = don't care

DC CHARACTERISTICS FOR 74HC

For the DC characteristics see *"74HC/HCT/HCU/HCMOS Logic Family Specifications"*.

Output capability: standard
I_{CC} category: SSI

AC CHARACTERISTICS FOR 74HC

GND = 0 V; $t_r = t_f$ = 6 ns; C_L = 50 pF

SYMBOL	PARAMETER	T_{amb} (°C)							UNIT	TEST CONDITIONS	
		74HC									
		+25			−40 to +85		−40 to +125			V_{CC} (V)	WAVEFORMS
		min.	typ.	max.	min.	max.	min.	max.			
t_{PHL}/ t_{PLH}	propagation delay nA, nB, nC to nY		28 10 8	100 20 17		125 25 21		150 30 26	ns	2.0 4.5 6.0	Fig.6
t_{THL}/ t_{TLH}	output transition time		19 7 6	75 15 13		95 19 16		110 22 19	ns	2.0 4.5 6.0	Fig.6

DC CHARACTERISTICS FOR 74HCT

For the DC characteristics see *"74HC/HCT/HCU/HCMOS Logic Family Specifications"*.

Output capability: standard
I_{CC} category: SSI

Note to HCT types

The value of additional quiescent supply current (ΔI_{CC}) for a unit load of 1 is given in the family specifications. To determine ΔI_{CC} per input, multiply this value by the unit load coefficient shown in the table below.

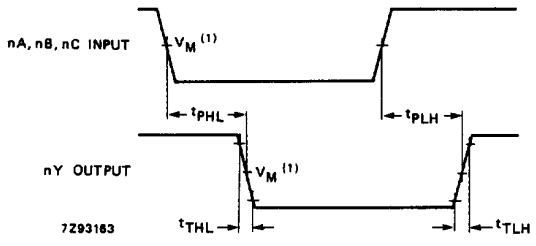
INPUT	UNIT LOAD COEFFICIENT
nA, nB, nC	1.50

AC CHARACTERISTICS FOR 74HCT

GND = 0 V; $t_r = t_f$ = 6 ns; C_L = 50 pF

SYMBOL	PARAMETER	T_{amb} (°C)							UNIT	TEST CONDITIONS	
		74HCT								V_{CC} (V)	WAVEFORMS
		+25			−40 to +85		−40 to +125				
		min.	typ.	max.	min.	max.	min.	max.			
t_{PHL}/ t_{PLH}	propagation delay nA, nB, nC to nY		12	24		30		36	ns	4.5	Fig.6
t_{THL}/ t_{TLH}	output transition time		7	15		19		22	ns	4.5	Fig.6

AC WAVEFORMS



(1) HC : V_M = 50%; V_I = GND to V_{CC}.
HCT: V_M = 1.3 V; V_I = GND to 3 V.

Fig.6 Waveforms showing the input (nA, nB, nC) to output (nY) propagation delays and the output transition times.

PACKAGE OUTLINES

See *"74HC/HCT/HCU/HCMOS Logic Package Outlines"*.