Embedded systems course
Flash memory device specification

Your device is equipped with a NOR flash memory.

The FLASH memory has a default capacity of 64Kbytes with a block size of 4Kbytes.

The FLASH memory is accessed using SPI (Serial Peripheral Interface).

The SPI asserts the CPU on IRQ5.

SPI registers

The SPI is accessed using the I/O bus. Its registers base address is **0x150**.

The following registers are supported:

Address	Symbol	Name
0x150	SR	Status register
0x151	CR	Control register
0x152	FADDR	Flash Address
0x153	FDATA00	Flash Data 0
0x154 – 0x162	FDATA01...FDATA0F	Flash Data 01-0F

SR - Status register definition

Bit	Type	Reset	Description
31:2	RO	0	Reserved
1	RWC	0	Cycle Done Status: this bit is set to 1 when the SPI Cycle completes (i.e., SCIP bit is 0) after software sets the GO bit. This bit remains asserted until cleared by software writing a 1 or hardware reset.
0	RO	0	SPI Cycle In Progress (SCIP): Hardware sets this bit when software sets the SPI Cycle Go bit in the Command register. This bit remains set until the cycle

			completes on the SPI interface. Hardware automatically sets and clears this bit so that software can determine when read data is valid and/or when it is safe to begin programming the next command. Software must only program the next command if this bit is 0.

CR – Control register definition

Bit	Type	Reset	Description
31:22	RO	0	Reserved
21:16	RW	0	Flash Data Byte Count (FDBC): This field specifies the number of bytes to use from the FDATA [00..0F] registers during the SPI cycle. The contents of this register are 0's based with 0b representing 1 byte and 111111b representing 64 bytes. The number of bytes transferred is the value of this field plus 1. This field is ignored for the Block Erase command.
15:8	RW	0	Command (CMD): this is the command code to be sent to the device. The list of possible commands is listed in the command table below. The command will be executed when the SCGO bit will be set to 1. If the command requires address or data settings they will be taken from the FADDR and/or FDATA registers.
7:2	RO	0	Reserved
1	RW	0	SPI interrupt Enable (SME): When set to 1, the SPI asserts an interrupt request whenever the Cycle Done Status bit is 1.
0	RWS	0	SPI Cycle Go (SCGO): This bit always returns 0 on reads. However, a write to this register with a '1' in this bit starts the SPI cycle defined by the other bits of this register and the FADDR/FDATA registers. The "SPI Cycle in Progress" (SCIP) bit gets set by this action. Hardware must ignore writes to this bit while the Cycle In Progress bit is set. Hardware allows other bits in this register to be programmed for the same transaction when writing this bit to 1.

			This saves an additional memory write.

SPI commands

The possible command types (for the CMD field in the control register) are:

Command	Code	Description
Read Data	03h	Read data from flash. The address to read from is set in FADDR. The data will be read into FDATA[00..0F].
Page Program	05h	Write data to flash. The address to write to is set in FADDR. The data will be read from FDATA[00..0F].
Block Erase	D8h	Erase a 4Kb block from flash. The device will erase the block in which the address set in FADDR resides.
Bulk Erase	C7h	Erase the whole flash device

The values in FDATA and FADDR should be programmed according to the command executed.

The byte order in the FDATA and FADDR registers is little-endian.

Note: you should always consider the FLASH write restrictions when writing to the FLASH device. The “page program” command will not give any indication if it has failed to write a value to the flash in case the command tried to change a bit value from 0 to 1.

FLASH image file

A file named “embsys_flash.img” will be created in your path that will keep an image of your FLASH memory, so that any changes you made to the flash persist the next time you run the simulator environment.

You can use an HEX editor or viewer to read the content of your FLASH memory.

If you need a new empty flash (besides using the bulk erase command), you can just delete the image and a new empty image (all bytes initialized to 0xFF) will be created the next time you’ll run the simulator.

Configurable number of block

You can change the amount of banks (a 4Kbytes blocks) used by your device by passing an argument to the simulator in the following way: ***/dlls_path/*embsys_flash.so,size=*flash_units***

The default is a 16 banks memory, i.e. 64Kbytes.