Embedded systems course
Network interface specification

Your device is equipped with a network interface which handles all the communication with the cellular base station. The network interface can cope with most communication errors autonomously such that messages are guaranteed to arrive correctly or not to arrive at all.

The network interface base address is **0x20 0000**.

Device Description

The network device is used to send and receive packets. It has no internal buffers, thus all of the memory which is needed for storing incoming and outgoing packets should be supplied by the hosting system.

The network card will automatically detect the closest antenna and will communicate with it, so basically – it eliminated the need for you to handle network-layer routing.

Circular buffers

The hosting device must initialize the NTXBP and NRXBP registers with pointers to some memory. This memory will contain an "array" of records (called **descriptors**) which look like this:

Length (bits)	Description
32	TX/RX Buffer Pointer
8	Buffer Size
8	Used size
8	Status. Must be set to 0 when descriptor is put in the TX fifo. When transaction completed and interrupt occurs, this field will contain the same value as the interrupt reason

The device has an MTU (Maximum Transmission Unit) of 161 bytes, meaning that 161 bytes is the largest packet length you can send or receive.

To manage the buffer as circular, each of the buffers (Tx, Rx) has a corresponding pair of 'tail' and 'head' registers. Read the 'Tx Registers' and 'Rx Registers' sections below for more details.

Keep in mind, that when the buffers are full, the head will point to the descriptor before the tail (both in Rx and Tx buffers). In this case, no buffers will be free, although the buffer pointed by head is not in use. Therefore, circular buffers must be at least of the size of 2 descriptors.

Tx Registers

When there are no packets to be sent (the network device is idle), the NTXFH and NTXFT must have the same value.

In order to send a packet, a **descriptor** should be stored in the memory pointed by NTXFH. Then NTXFH should be increased by `1`. Note that the TX buffer is cyclic and the hosting system must handle all the corner cases.

Once the NTXFH register is changed (and thus NTXFH != NTXFT), the HW will read any descriptors starting from NTXFT. For each descriptor, the network device will send 'Used Bytes' of the content of the buffer to the network. For instance – if UsedBytes field in the descriptor is 28, the network device will send 28 bytes to the network. The 'Buffer Size' is used by the hosting system to manage the memory.

After each packet is sent, the Tx Complete interrupt line will be asserted (either with reason TX_SUCCESS or an error). Acknowledging the interrupt, this is done by writing the status field to NIRE in Network Status Register, will cause the HW to handle the next descriptor (it's host system's responsibility to advance the NTXFT register).

Rx Registers

When no packets have been received (network device is idle), the NRXFH and NRXFT will have the same value.
Before the host system deasserts the NBSY bit, it must set the Rx Registers to point to a legal cyclic buffer with legal descriptors. It is the host system's responsibility to allocate any memory needed.

When a packet received, the descriptor pointed by NRXFH is filled, and the received packet is copied to the buffer pointer. Then, NRXFH is increased by 1 and the Rx Complete interrupt is asserted.

The host system should then read the content of the buffer, and increase the NRXFT by 1.

If another packet is received before the interrupt was acknowledged, the descriptor pointed by NRXFH will be filled, NRXFH will be increased, and the RX_COMPLETE interrupt will assert again.

Any illegal values in the Rx Registers (for example: buffer of size 0, etc') – will cause the NROR and NBSY bits to assert.

Device Memory Map

Offset	Symbol	Description
0x0000	NTXBP	Network Transmit Circular Buffer Pointer
0x0004	NTXBL	Network Transmit Circular Buffer Length
0x0008	NTXFH	Network Transmit FIFO Head Index
0x000C	NTXFT	Network Transmit FIFO Tail Index
0x0010	NRXBP	Network Receive Circular Buffer Pointer
0x0014	NRXBL	Network Receive Circular Buffer Length
0x0018	NRXFH	Network Receive FIFO Head Index
0x001C	NRXFT	Network Receive FIFO Tail Index
0x0020	NCTRL	Network Control Register
0x0024	NSTAT	Network Status Register

NTXBP - Network Transmit Circular Buffer Pointer

Bit	Type	Default Value	Description
31:0	RW	0	Base address of the circular transmit buffer.

NTXBL - Network Transmit Circular Buffer Length

Bit	Type	Default Value	Description
31:0	RW	0	Number of octets (bytes) in the allocated buffer, divided by sizeof(descriptor)

NTXFH - Network Transmit FIFO Head Index

Bit	Type	Default Value	Description
31:0	RW	0	Index of the next free (unused) packet descriptor.

NTXFT - Network Transmit FIFO Tail Index

Bit	Type	Default Value	Description
31:0	RW	0	Index of the next packet descriptor to be sent by the HW.

NRXBP - Network Receive Circular Buffer Pointer

Bit	Type	Default Value	Description
31:0	RW	0	First address of the receive buffer. Received data will be written to memory starting from this address.

NRXL - Network Receive Circular Buffer Length

Bit	Type	Default Value	Description
31:0	RW	0	Number of octets (bytes) in the allocated buffer, divided by sizeof(descriptor)

NRXFH - Network Receive FIFO Head Index

Bit	Type	Default	Description
31:0	RW	0	Index of the next free (unused) packet descriptor.

NRXFT - Network Receive FIFO Tail Index

Bit	Type	Default	Description
31:0	RW	0	Index of the next packet descriptor which was not yet read from the FIFO.

NCTRL - Network Control Register

<table>
<tr><th>Bit</th><th>Type</th><th>Default Value</th><th>Description</th></tr>
<tr><td>31:29</td><td>RW</td><td>001</td><td>Network Operating Mode (NOM): these bits should be set by the hosting system to determine the operating mode of the network card:
<table>
<tr><td>001</td><td>Normal, asynchronous mode
Send/receive raw packets from the cellular network</td></tr>
<tr><td>010</td><td>SMSC connectivity mode
Optimized mode for sending/receiving SMS messages from SMSC.</td></tr>
<tr><td>100</td><td>Internal Loopback
Send messages are not sent to the network, but are looped back inside the network card and are returned to the RX buffers. If no RX descriptors are available, TX_FAILED_NETWORK_ERROR interrupt will be raised. If there is a free RX buffer, RX_COMPLETE interrupt will be raised.</td></tr>
<tr><td></td><td>Reserved
Setting different values will result in unspecified behavior</td></tr>
</table></td></tr>
<tr><td>28:5</td><td></td><td>0</td><td>Reserved</td></tr>
<tr><td>4</td><td>RW</td><td>0</td><td>Enable Transmit Error Interrupt (due to bad descriptor or network error).

Setting this bit will cause the device to assert IRQ14 upon transition error.</td></tr>
<tr><td>3</td><td>RW</td><td>0</td><td>Enable packet dropped interrupt (due to small buffer or insufficient buffers)

Setting this bit will cause the device to assert IRQ14 upon packet drop.</td></tr>
<tr><td>2</td><td>RW</td><td>0</td><td>Enable RX completion interrupt

Setting this bit will cause the device to assert IRQ14 upon packet RX completion.</td></tr>
<tr><td>1</td><td>RW</td><td>0</td><td>Enable TX completion interrupt

Setting this bit will cause the device to assert IRQ14 upon packet TX completion.</td></tr>
<tr><td>0</td><td>RW</td><td>1</td><td>Network Busy Bit (NBSY): this bit should be set to 1 in order to block any receive activity on the network device.

While this bit is asserted new packets arriving at the hardware are dropped,</td></tr>
</table>

			(without packet dropped interrupt).

NSTAT - Network Status Register

Bit	Type	Default Value	Description
31:16	RO	0	Reserved
15:8	RO	0	Network Interrupt Reason (NIRE): hosting system can read the value of this register upon interrupt, to determine the reason for the interrupt: 00000000 None 00000001 Rx Complete (Successfully) 00000010 Tx Complete (Successfully) 00000100 Rx Packet dropped because Rx buffer was too small 00001000 Rx Packet dropped because Circular Buffer was fulll 00010000 Tx failed due to bad descriptor 00100000 Tx failed due to network error Reserved
7:4	RO	0	Reserved
3	RO	0	Network Receive buffer Over-Run (NROR): this bit is set to 1 when new packet was dropped because the Circular Buffer was full or too small.
2	RO	0	Network Receive In Progress (NRIP): Hardware automatically asserts this bit when a data packet receiving is in progress.
1	RO	0	Reserved
0	RO	0	Network Transmit In Progress (NTIP): Hardware sets this bit when software sets the NTXL register. This bit remains set until the data transmission completes. Hardware automatically sets and clears this bit so that software can determine when the buffer is safe to be reused and/or new transfer can be started.