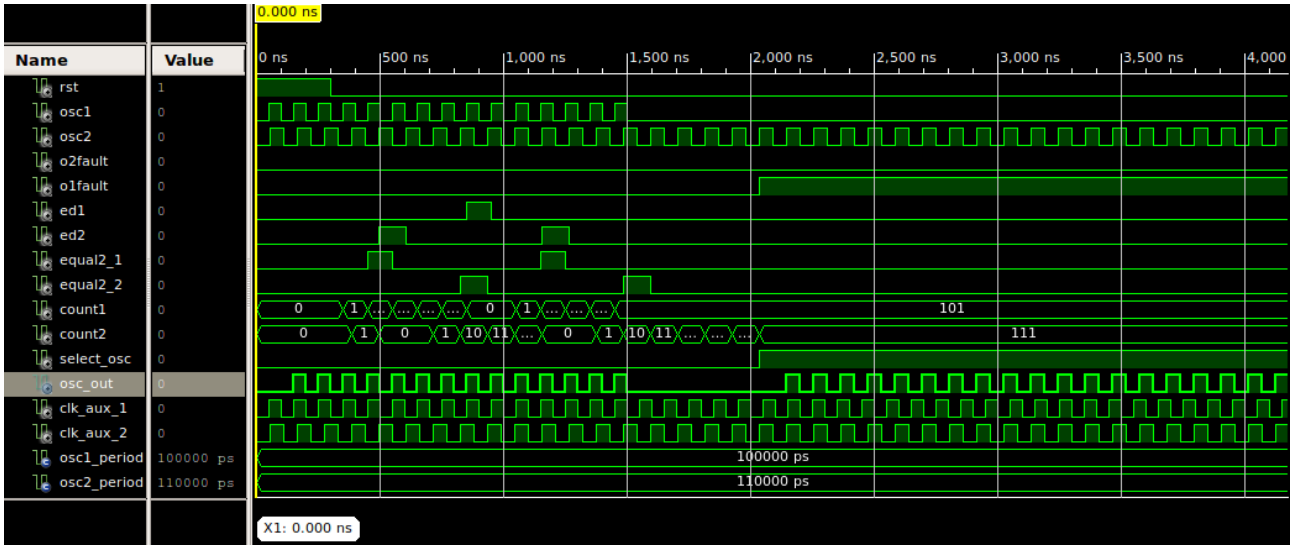
Actividad 8.2

1) Con el siguiente código se realizó lo propuesto en la filmina 34 de la presentación de Módulo 8.

```
begin

  syn1 <= '0' when RST = '1' else equal2_2 when rising_edge(OSC1);
  syn2 <= '0' when RST = '1' else equal2_1 when rising_edge(OSC2);

  syn1_ant <= syn1 when rising_edge(OSC1);
  syn2_ant <= syn2 when rising_edge(OSC2);

  ed1 <= syn1 and not syn1_ant;
  ed2 <= syn2 and not syn2_ant;

  count1 <= 0 when RST = '1' or ed1 = '1' else 7 when count1 = 7 else count1 + 1 when rising_edge(OSC1);
  count2 <= 0 when RST = '1' or ed2 = '1' else 7 when count2 = 7 else count2 + 1 when rising_edge(OSC2);

  equal2_1 <= '1' when count1 = 2 else '0';
  equal2_2 <= '1' when count2 = 2 else '0';

  sO2Fault <= '1' when count1 = 7 else '0';
  sO1Fault <= '1' when count2 = 7 else '0';

  Select_OSC <= '0' when sO2Fault = '1' else '1' when sO1Fault = '1' else '0';

  O1Fault <= sO1Fault;
  O2Fault <= sO2Fault;

  BUFGCTRL_inst : BUFGCTRL
   generic map (
      INIT_OUT => 0,          -- Initial value of BUFGCTRL output ($VALUES;)
      PRESELECT_I0 => FALSE, -- BUFGCTRL output uses I0 input ($VALUES;)
      PRESELECT_I1 => FALSE   -- BUFGCTRL output uses I1 input ($VALUES;)
   )
   port map (
      O => OSC_OUT,              -- 1-bit output: Clock output
      CE0 => not Select_OSC,          -- 1-bit input: Clock enable input for I0
      CE1 => Select_OSC,          -- 1-bit input: Clock enable input for I1
      I0 => OSC1,            -- 1-bit input: Primary clock
      I1 => OSC2,            -- 1-bit input: Secondary clock
      IGNORE0 => '0', -- 1-bit input: Clock ignore input for I0
      IGNORE1 => '0', -- 1-bit input: Clock ignore input for I1
      S0 => '1',             -- 1-bit input: Clock select for I0
      S1 => '1'              -- 1-bit input: Clock select for I1
   );
end Arq_Head;
```

A continuación se expone una captura de la simulación propuesta



Donde los mayores problemas del sistema se visualizan en la transición de relojes, donde lo dependiente del reloj queda sin transiciones hasta que el detector habilite el cambio.