Measuring Deep Metastability

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Outline of presentation

- Why measure
- How to measure
- Results
- Conclusions

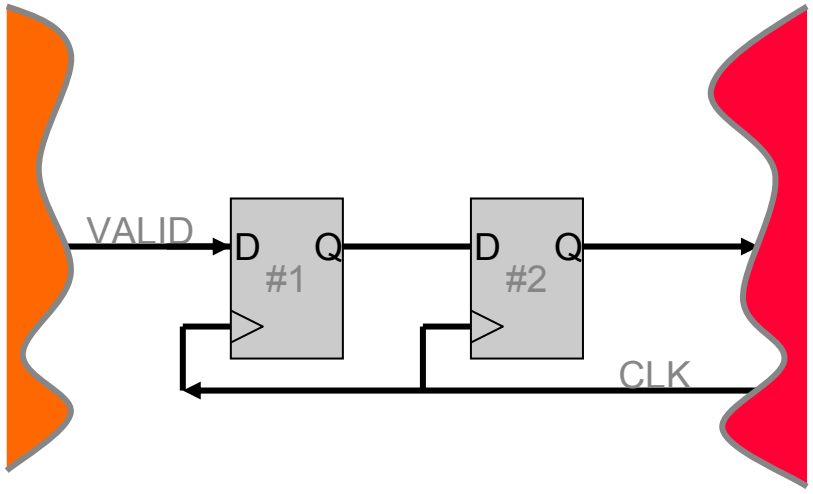
Why

- Systems are Globally Asynchronous
  - 4 x increase in global asynchronous signalling by 2012
  - 8 x by 2020 [ITRS 2005]

- And Locally Synchronous
  - Many different clocks
  - Many synchronizers
  - Need to know the reliability of the synchronizers

Synchronizer

- Handles asynchronous to synchronous interfaces
- Supports synchronous to synchronous interfaces with multiple clocks

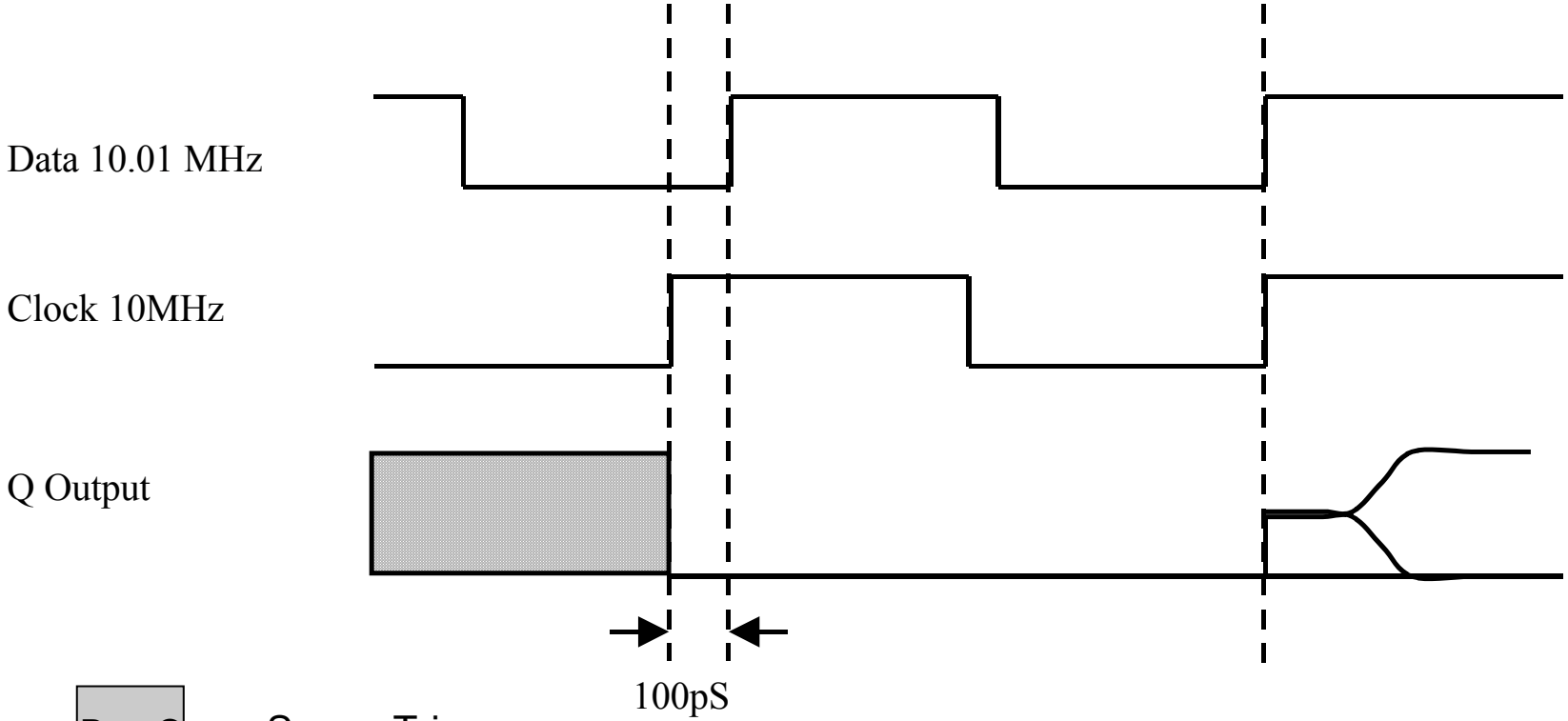


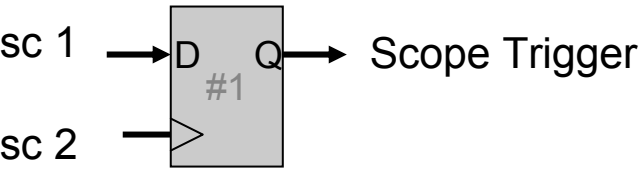
$$MTBF = \frac{e^{t/\tau}}{T_w \cdot f_c \cdot f_d}$$

What we know

- Things we know
  - Synchronizers are unreliable, the more there are the more unreliable the system
  - How to measure reliability up to a few hours
- Things we know we don't know
  - What reliability is at 3 years
  - How to measure it
  - Complex circuits give complex results, the simple MTBF formula may not apply
- Things we don't know we don't know
  - What happens on the back edge of the clock

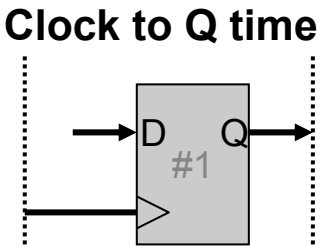
Testing synchronizers

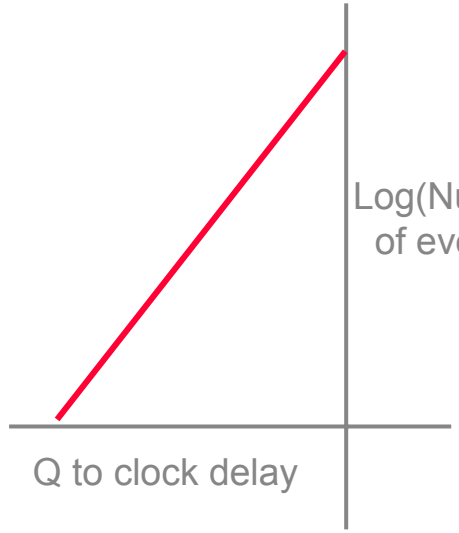




- **Data and Clock are asynchronous**
- **Q only changes if Data and clock edges are within 100ps (1 in 1000)**

Event histogram

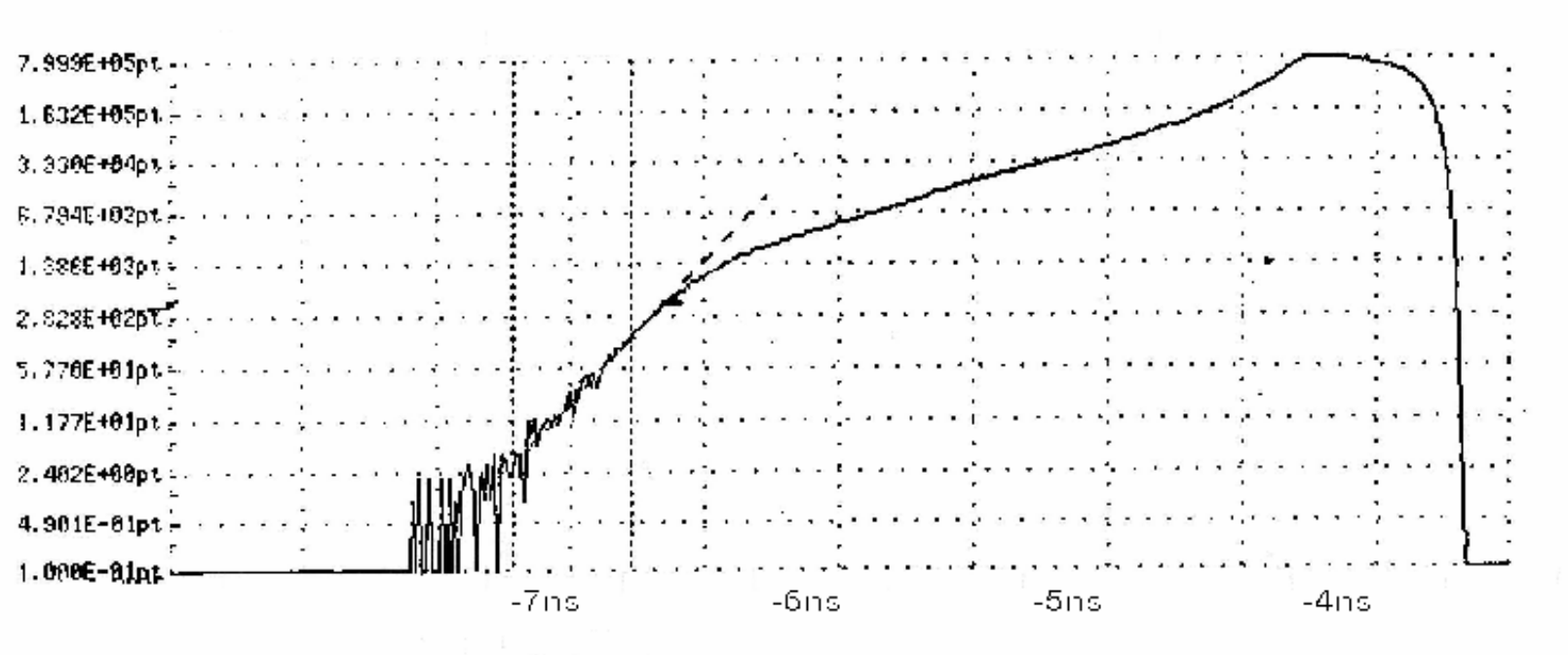




- Trigger from Q going high
- Observe clock, so scale is negative
- Log scale of events because

$$Events = \frac{T_{Elapsed}}{MTBF} = T_{Elapsed}.T_w f_c f_d e^{-t/\tau}$$

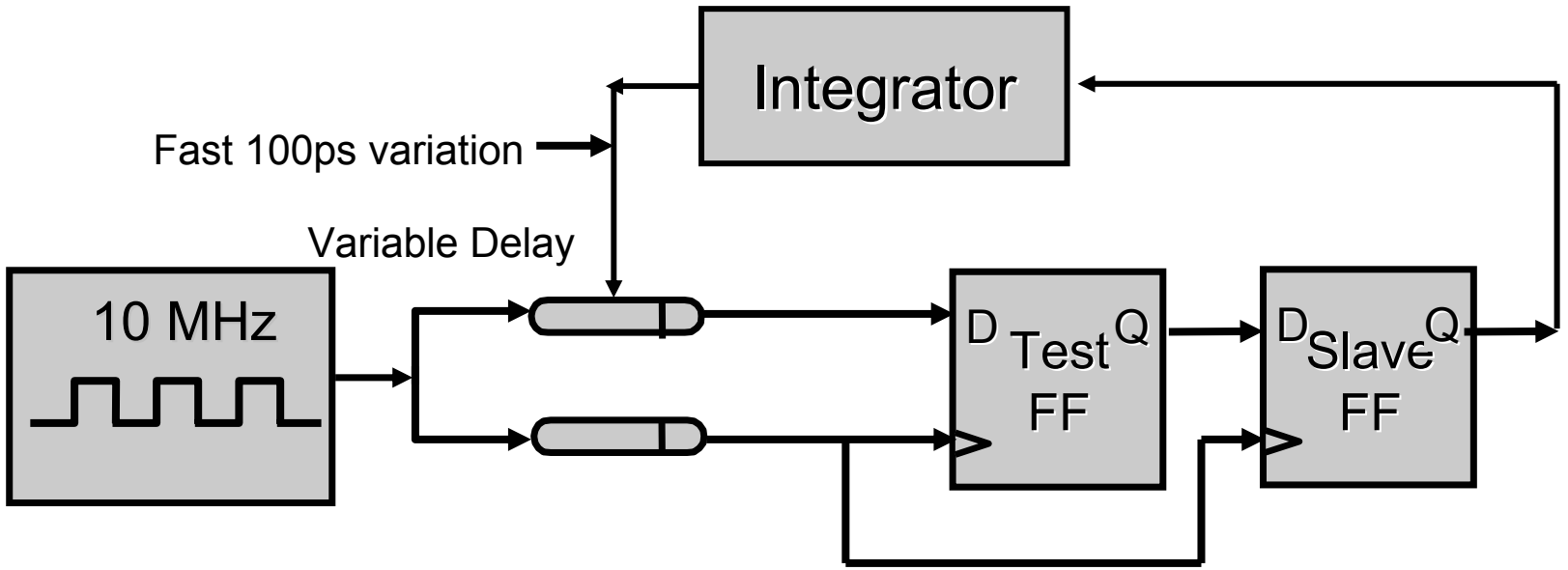
74F5074 Histogram



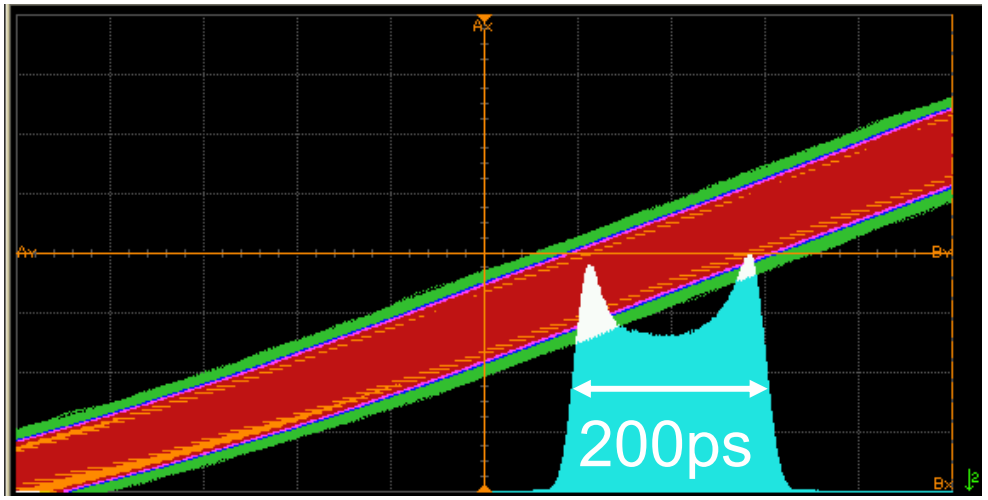
- Slope, τ, is about 120ps (in fast region)
- Typical delay time (most events) is 4ns
- 99.9% of clock cycles do not cause useful events
- To get 1 event at 7ns requires hours

Increasing the number of events

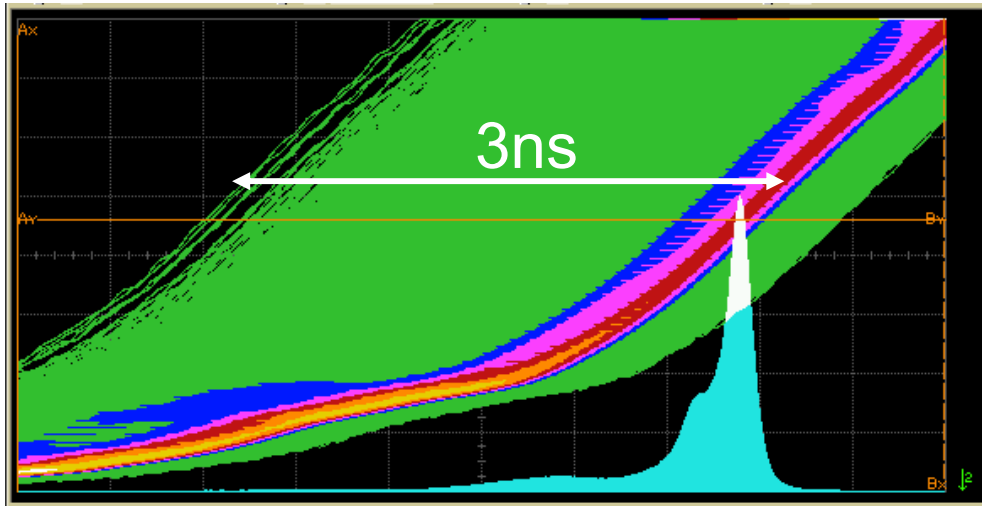
- Test FF is driven to metastability
- Every clock produces a metastable response



What you get

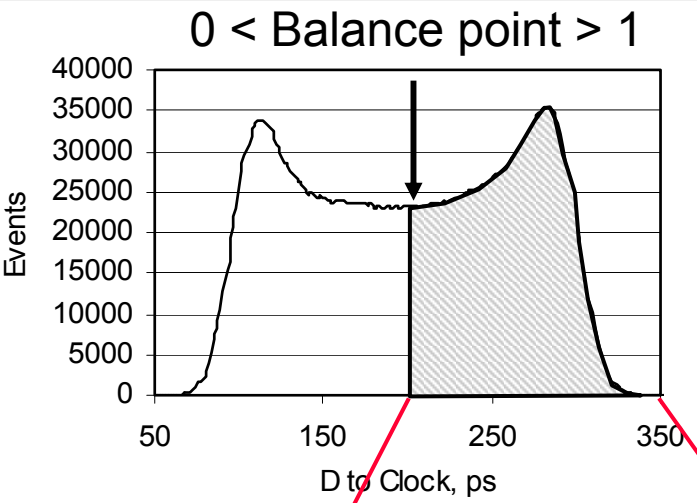


- Clock to D (Input) histogram



- Q to Clock (Output) histogram

Interpreting results

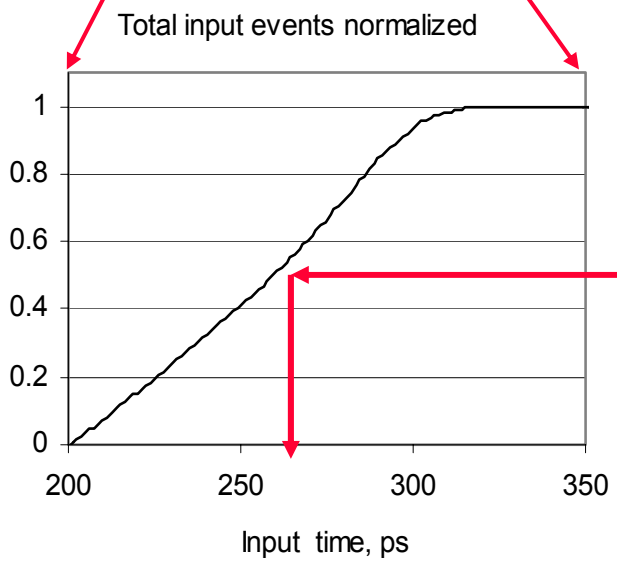


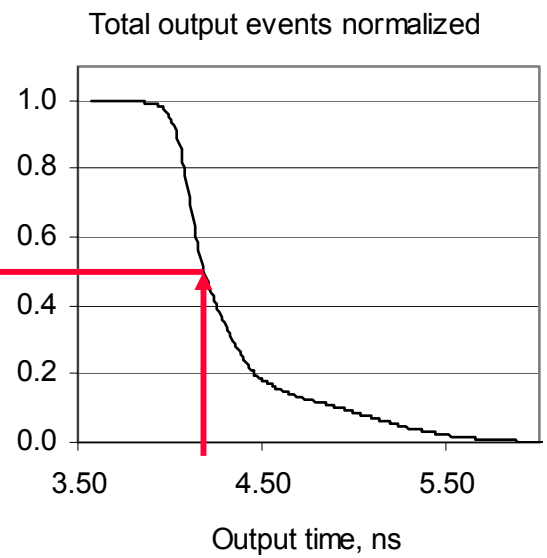
Input time distribution is not flat

Proportion of total inputs causing events vs input time

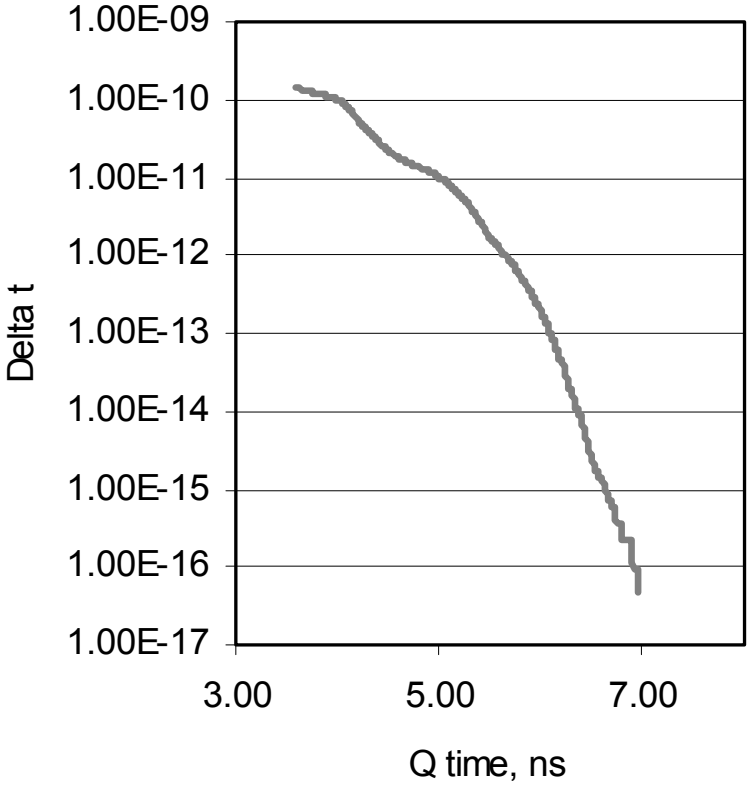
Proportion of total output events vs output time

Mapping output times to input times





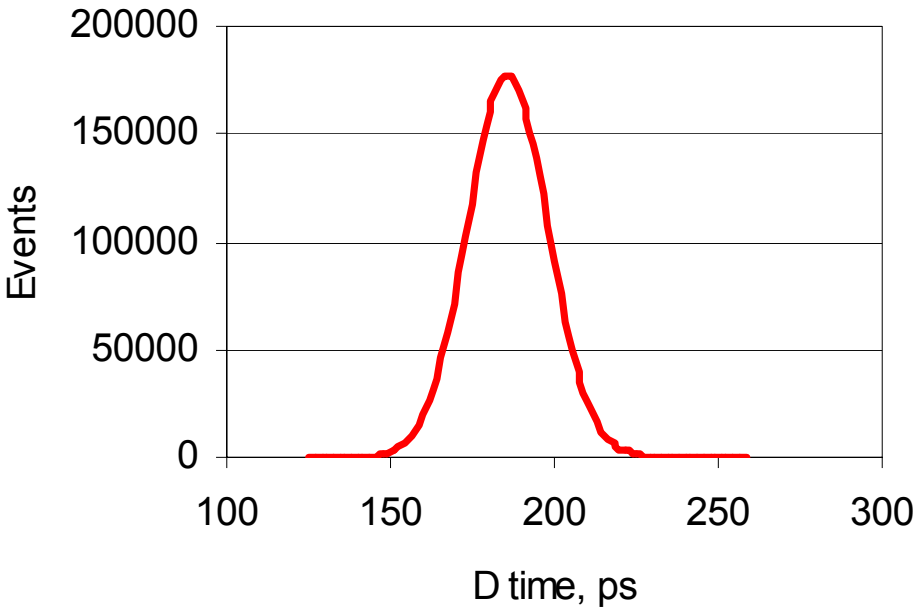
100ps variation



- Δt is the time from the "balance point" of ~200ps
- Similar to original graph BUT Δt not events
- Much quicker to gather data
- Δt does not depend on f_c and f_d or measurement time. Events do

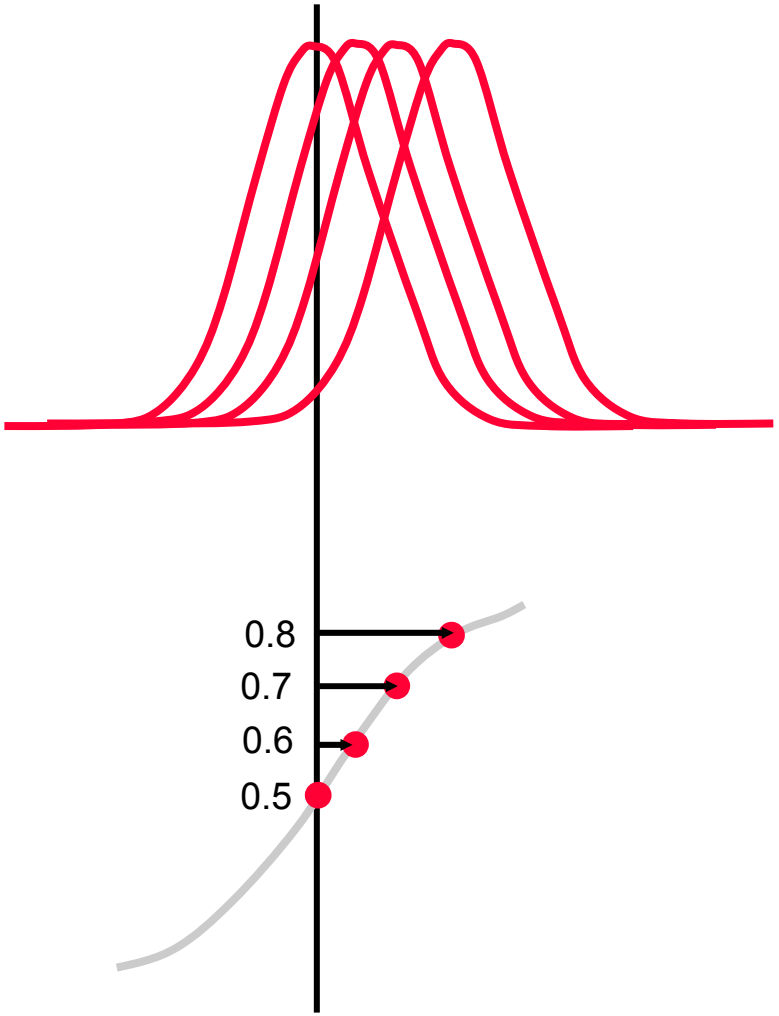
$$MTBF = \frac{1}{\Delta_t f_c f_d}$$

No input variation



- Deviation 12ps
- Noise and jitter at inputs of FF under test
- Noise and jitter in measurement
- Oscilloscope specification 9ps

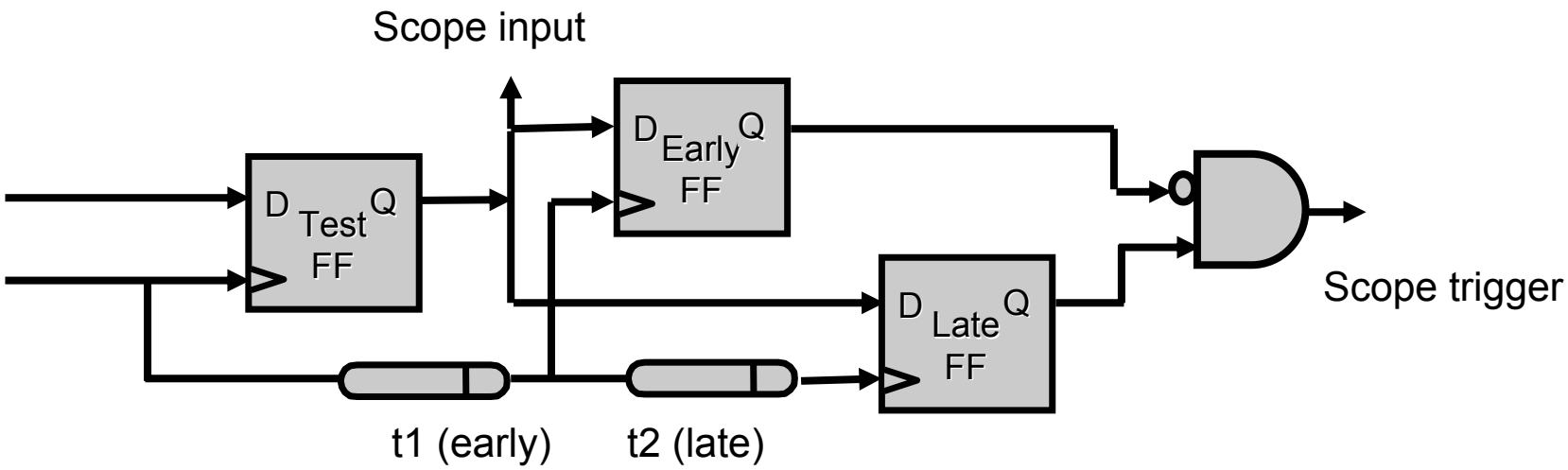
Eliminating measurement noise



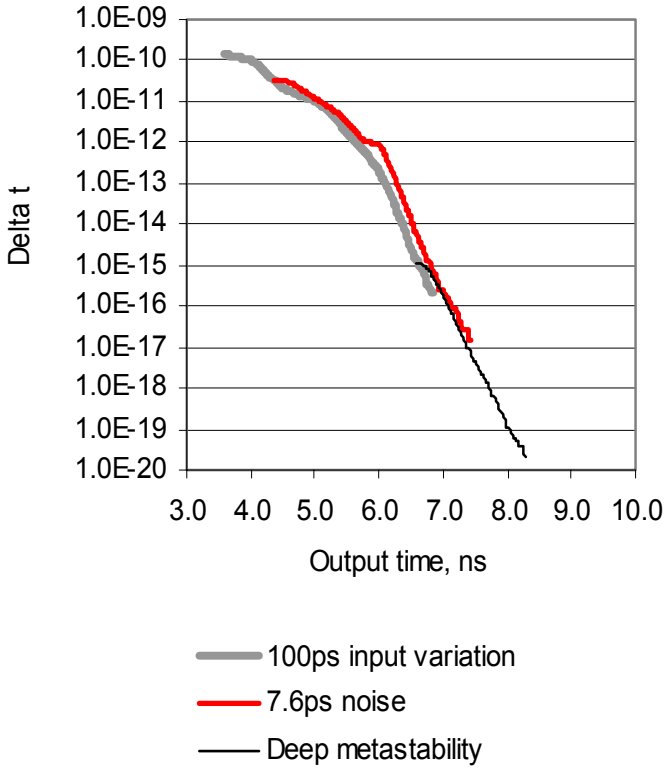
- +5 for a low and –5 for a high gives 0.5 probability of a high output
- + 4 for a high and –6 for a low gives 0.6 probability
- Observed distribution is shifted
- We can plot the cumulative probability against shift
- This is the integral of the actual distribution.
- Deviation 7.6ps.
- $7.6^2 + 9.2^2 = 11.9^2$

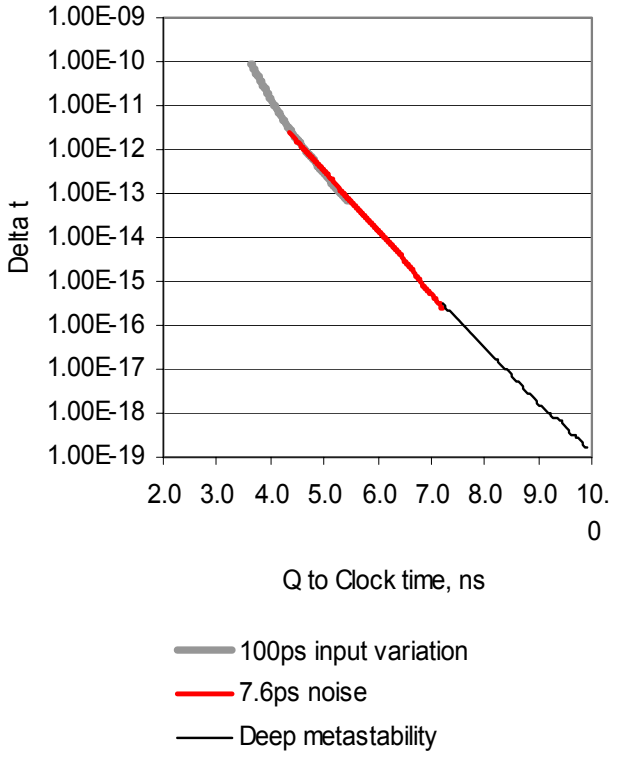
Deep metastability

- 100/7.6 = 13 times as many events with small input times
- They occur every 100ns, too fast for the scope
- Only 1 in 1000 captured
- Most events still produce early output times
- Filter them out so that the event rate is much slower



Results of all methods





74F5074 Schottky bipolar

74ACT74 CMOS

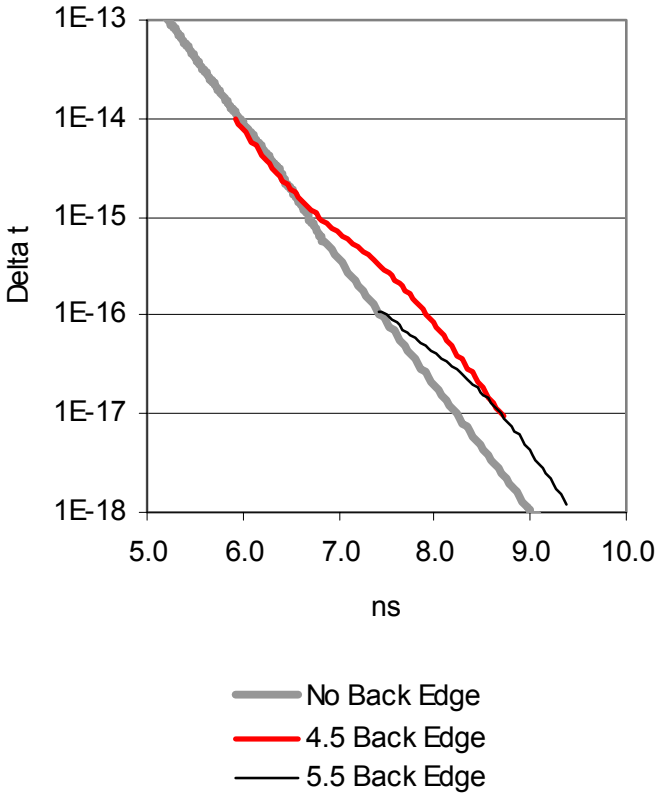
- Reliability measurements to 10^{-20} seconds (MTBF ~ 11days)
- Done in 3 minutes

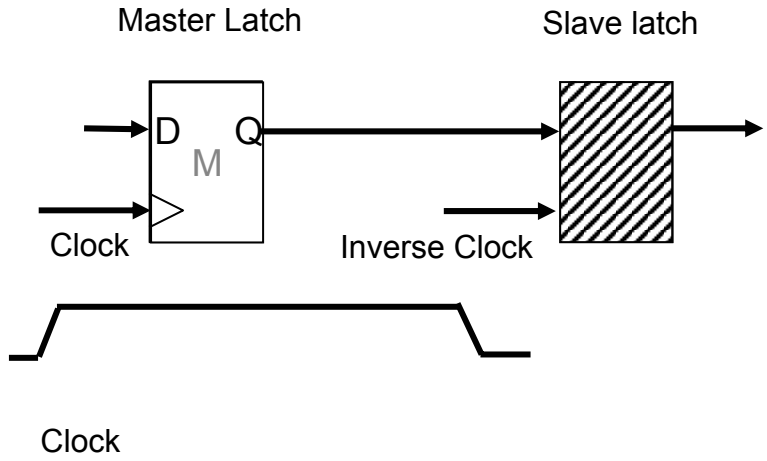
Results

$$MTBF = \frac{1}{\Delta_t f_c f_d} = \frac{1}{10^{-20}.10^7.10^7} = 11 days$$

- We can measure reliabilities of days not hours in 3 minutes
- To get to 3 years reliability (10^{-22} seconds) the experiment is run for 5 hours
- More than two slopes on one sample, 350ps, 120ps and 140ps
- We can see output events at up to 10 ns

When the clock goes low

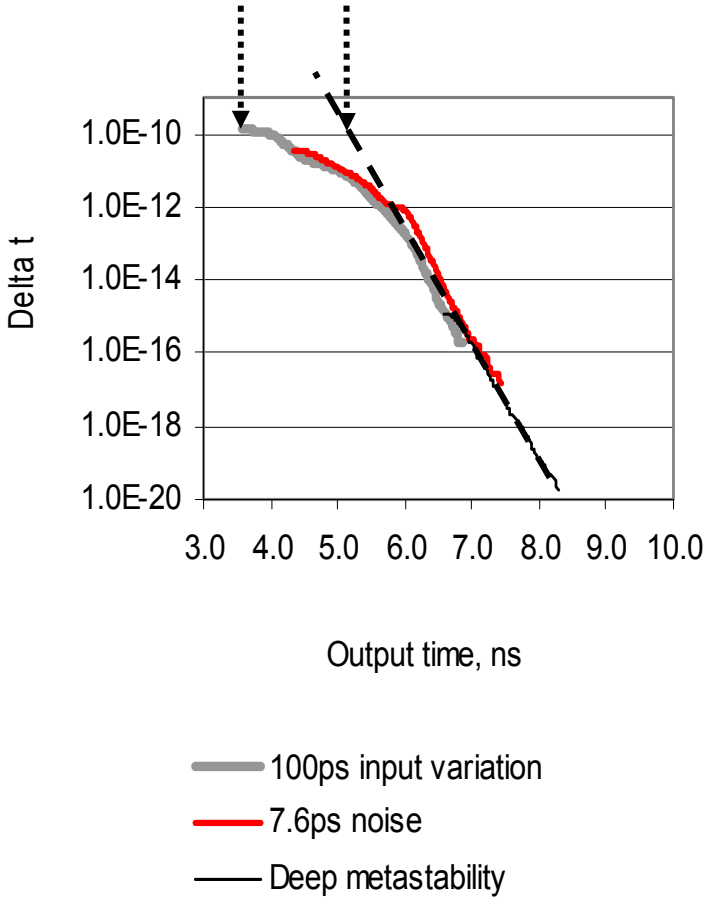




- Clock goes high, master goes metastable
- Master output arrives at slave
  - Before slave clock high: transparent delay
  - As slave clock goes high: metastable

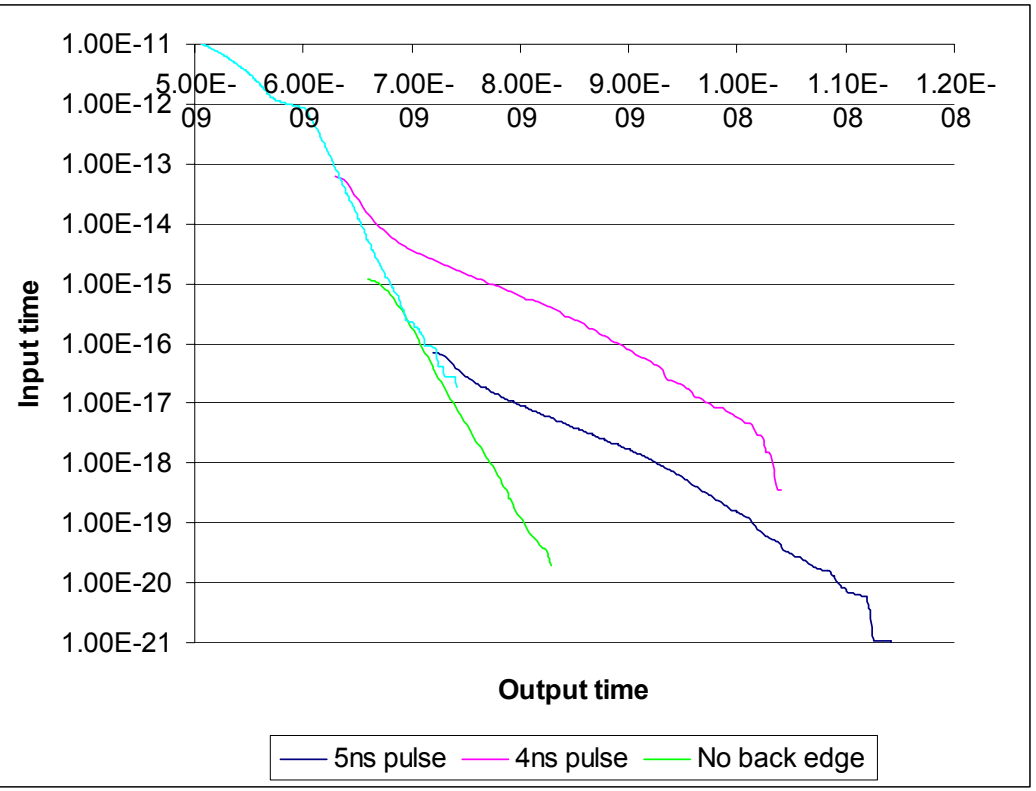
Back edge of clock causes increased delay

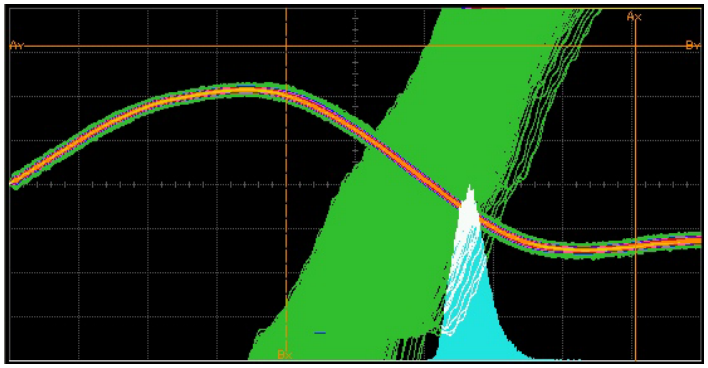
Effect of Clock low on 74F5074



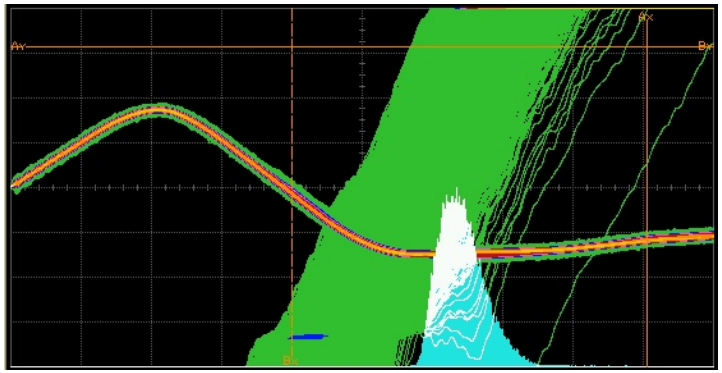
- Step is the difference between slave transparent and metastable
- Master + Slave transparent delay ~ 3.5 ns
- Master metastable + Slave transparent delay ~ 5.5 ns
- Step here is ~ 2 ns, around 15τ

Effect of clock low on 74F5074





6 ns pulse



4 ns pulse

- 1 – 3 ns additional delay

Conclusions

- Reliability measurements extended from
  - 10^{-15} s or MTBF = 16 min at 10MHz, to
  - 10^{-22} s or MTBF = 3 years
- We can see variations in τ not previously seen
- Results can be presented in a form independent of clock frequency
- On-chip and measurement noise can be eliminated
- Back edge of clock pulse is seen to be an important effect, can be 0 – 15τ