APPLICATION NOTE

AN053
The Philips metastable immune ABT22V10-7

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Introduction

Most digital systems are designed to be synchronous in operation, meaning that the timing of all internal signals is coordinated with the system clock. The timing of a synchronous design can be accurately predicted, allowing propagation delays and setup times to be calculated precisely. Unfortunately, in the real world of system design, not all signals are synchronous—so no such timing guarantees are possible. Whenever a signal violates a device's setup or hold timing requirements, the output might go high, low, or temporarily hang between high and low. This undesirable phenomena is known as metastability and wreaks havoc for many designers. The Philips ABT22V10-7 solves this problem.

Metastability

Simply put, metastability is a flip-flop's inability to decide which state it is in. It occurs when a signal level changes at about the same time the latch of a flip-flop is clocked, causing an input signal that falls within the invalid linear region between logic zero (<0.8 Volts) and logic one (>2.0 Volts). This can result in the output of the flip-flop glitching, going into an undefined state somewhere between a high and low, possibly oscillating between high and low delayed for some indeterminable amount of time, or perhaps, having no effect on the output at all.

The problems that can occur due to a metastable condition differ on how the output of the register is used, either for combinatorial logic or pipelined to another register. If the output is used for combinatorial logic, the fact that the output may glitch, oscillate or remain in the linear region for an indefinite period of time will produce erroneous results in the combinatorial logic that may result in system failure. If the output is presented to the next register that is invalid, in the linear region, or oscillating. As a result, the setup and/or hold timing for this second register may also be violated, which can result in it going into a metastable failure mode as well. This failure having propagated further into the system could have catastrophic effects if the register in question resides in the system control logic or CPU.

Due to the fact that random errors caused by metastability increase with higher clock rates, designers may find that the old rules and design practices are no longer sufficient in preventing failures associated with metastability. Some engineers may be surprised to discover that the dependable two-state flip-flop is not as reliable in some of today's higher-clock-speed designs, as it was in yesterday's applications.

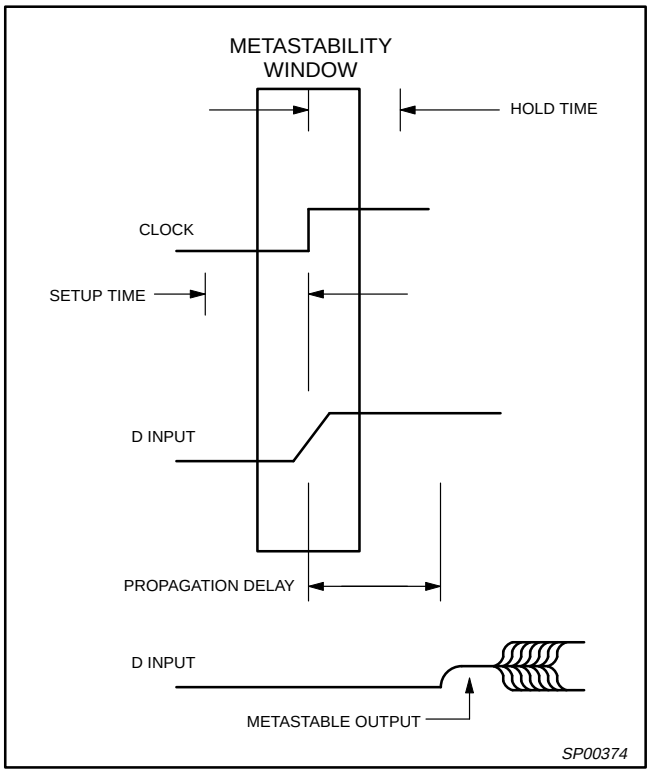

Figure 1. Metastability Window

Metastable Resistant vs. Metastable Immune

Many methods of reducing the possibility of metastability have been introduced. One method is to avoid it by reducing the number of situations where flip-flops use a non-asynchronous signal. Another, more practical, method is based on the belief that metastability is best solved though a double-clocking technique of having two flip-flops in series to filter metastable failures from propagating further into the system (see Figure 2). However, with this method the first flip-flop must resolve any metastable condition within the setup time of the second flip-flop, and that's not always possible. Another, less elegant, method is to simple extend the amount of time after each event in order to allow adequate settling of signals. This adds to the total propagation delay while improving the metastable reliability, but it is a high price to pay. While is is true that these methods aid in resisting or hardening the possibility of a flip-flop entering into a metastable state, there is no guarantee that any of these techniques will prevent metastable-related errors.

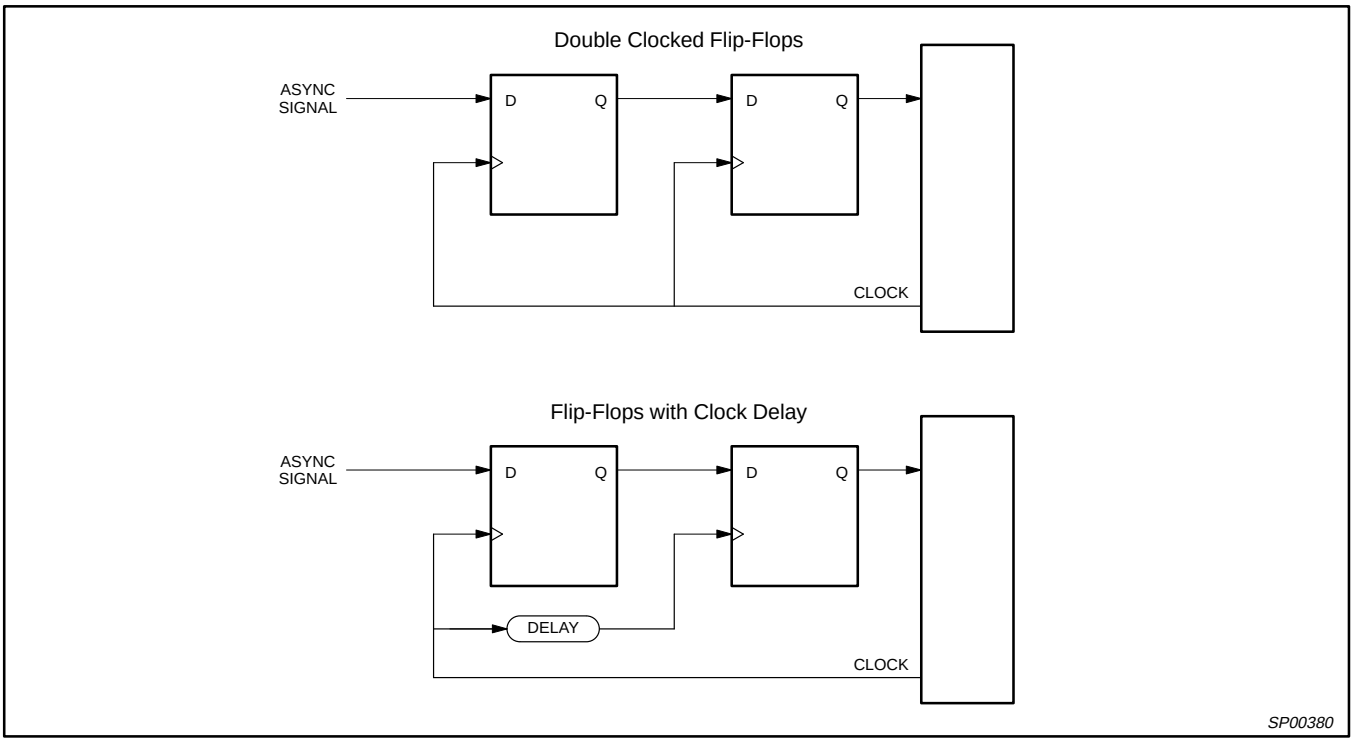

Figure 2. Double Clocked Flip-Flops

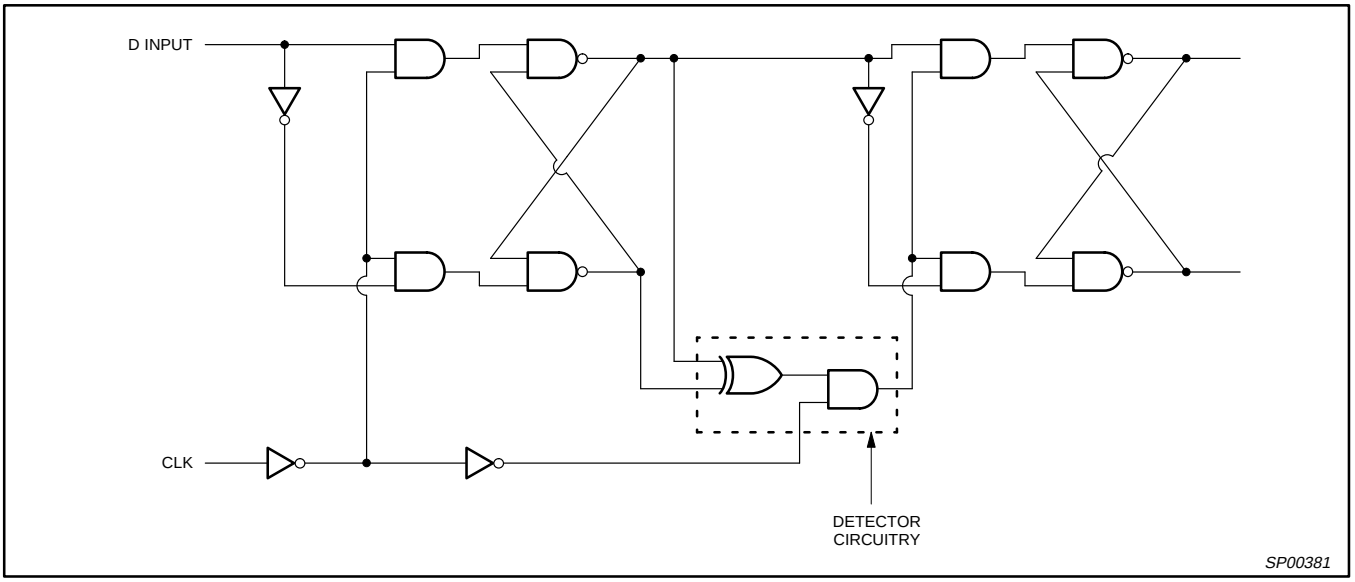

Figure 3. Philips Patented Metastable Gate Arrangement

Table 1. ABT22V10-7 Values for τ and T_0

	T_{amb} = 0°C		T_{amb} = +25°C		T_{amb} = +70°C	
V_{CC}	τ	T_0	τ	T_0	τ	T_0
5.5V	83 ps	8.1×10^{18} sec	82 ps	7.5×10^{18} sec	101 ps	3.0×10^{12} sec
5.0V	80 ps	4.0×10^{18} sec	83 ps	2.2×10^{17} sec	98 ps	4.4×10^{11} sec
4.5V	85 ps	3.4×10^{14} sec	91 ps	2.5×10^{12} sec	106 ps	1.1×10^{8} sec

The Solution

The Philips ABT22V10-7 uses a patented circuit that prevents the outputs from glitching, oscillating, or remaining in the linear region under any circumstances, including setup and hold time violations. While most 22V10s utilize only one flip-flop, the Philips ABT22V10 utilizes two latches along with a patented detector circuitry (US Patent 4963772) to prevent metastable conditions. Philips' patented circuitry, interposed between the first and second latch, literally blocks any metastable condition that may occur in the first latch from propagating into the second latch. This circuitry consists of a detector circuit that gates the clock to the second latch. Whenever the first latch goes metastable, the clock edge to the second clock is inhibited until the metastable condition resolves to the correct state. When this occurs, the clock is enabled and allows data to enter the second latch and propagate to the output pins. While this approach is most effective at preventing a metastable state in the first latch circuit from propagating an unknown state signal to the second latch circuit, it is important to realize that, other than the time delay, this technique is transparent to the end user. Furthermore, the ABT22V10-7 is designed to minimize the likelihood that the first latch circuit will ever enter into a metastable state.

Since the outputs never glitch, oscillate, or remain in the linear region, the only metastable failure that can propagate further into the system is when the next flip-flop in the system samples the ABT22V10-7's output at precisely the same time it is making a logic transition. By allowing sufficient time for any increased clock-to-Q delay, propagation of metastable failures can be avoided. The following design example illustrates this concept.

Design Example: Determining MTBF

Suppose a designer wants to use the ABT22V10 for synchronizing asynchronous data that is arriving at 10MHz (as measured by a frequency counter), in a 5V system that has a clock frequency of 50MHz, at an ambient temperature of 25°C. She has decided that she would like to sample the output of the ABT22V10 8.5ns after the clock edge to ensure that any clock-to-Q delays that were the result of the ABT22V10 internal metastability resolution circuitry have completed and the outputs have transitioned. The MTBF for this situation can be calculated by using the equation below:

$$MTBF = e(t'/\tau)/T_0 F_C F_1$$

In this formula, F_C is the frequency of the clock, F_1 is the average input event frequency, and t' is the time after the clock pulse that the output is sampled ($t' > T_{CO}$). T_0 and τ are device parameters provided by the semiconductor manufacturer (refer to the table for the ABT22V10-7 metastability specifications). T_0 and τ are derived from tests and can be most nearly be defined as follows: τ is a function of the rate at which a latch in a metastable state resolves that condition. T_0 is a function of the measurement of the propensity of a latch to enter a metastable state. T_0 is also a normalization constant which is a very strong function of the normal propagation dely of the device.

In this situation, the F_1 will be twice that data frequency, or 20MHz, because input events consist of both low and high transitions. Thus in this case F_C is 50MHz, F_1 is 20MHz, τ is 83ps, t' is 8.5ns, and T_0 is 2.2×10^{17} seconds. Using the above formula, the actual MTBF for this situation is 1.36×10^{12} seconds, or 43,095 years for the ABT22V10-7.

Summary

The Philips ABT22V10-7 has on-chip circuitry that completely eliminates any output glitches, oscillations, or other output anomalies associated with metastable conditions. For outputs that are then used to generate clocks, control signals or other asynchronous data this represents an unparalleled level of reliability in a PLD. In addition, a complete set of metastability data is provided, that allows designers the ability to design extremely robust systems where data is synchronously pipelined.

NOTES

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