SONY

Diagonal 2.59 mm (Type 1/6.95) 2.4 Mega-Pixel CMOS Image Sensor with Square Pixel for Color Cameras

IMX132TQH5-C

Description

The IMX132TQH5-C is a diagonal 2.59 mm (Type 1/6.95) back-illuminated type CMOS image sensor with a square pixel array and approx. 2.4 M effective pixels. Adoption of column parallel A/D converter realized high-speed processing and changing fundamental structure to back-illuminated type enhanced imaging characteristics including sensitivity and low noise. R, G, and B pigment primary color mosaic filter is emproyed. High sensitivity, low dark current features are achieved. It equips an electronic shutter with variable integration time. It operates with three power supply voltages: analog 2.7 V, digital 1.2 V and 1.8 V for input/output interface and achieves low power consumption.

Features

- ◆ Back-illuminated CMOS image sensor “Exmor R”
- ◆ 2-wire serial communication circuit on chip
- ◆ CSI2 serial data output (selection of 1 Lane/2 Lane) on chip
- ◆ Timing generator, H and V driver circuits on chip
- ◆ CDS/PGA on chip
- ◆ 10-bit A/D converter on chip
- ◆ Automatic optical black (OB) clamp circuit on chip
- ◆ PLL on chip (rectangular wave/sine wave)
- ◆ High sensitivity, low dark current, no smear, excellent anti-blooming characteristics
- ◆ Variable-speed shutter function (Minimum unit: One horizontal sync signal period)
- ◆ R, G, B primary color pigment mosaic filters on chip
- ◆ Supports external mechanical shutter
- ◆ Xenon/LED Flash control function
- ◆ Max. 58.88 frame/s in all-pixel scan mode
- ◆ Pixel rate: 162.0 MHz (all pixels, 2 Lane, 30 frame/s)
- ◆ Supports 720/60 p, 1080/30 p, 1080/60 p drive *NOTE
- ◆ Up/down and/or right/left inversion function
- ◆ Pixel subsampling readout function
- ◆ Image cutout function
- ◆ Power-on reset function
- ◆ Power-on sequence free

NOTE) Please ask about the details of a required register.

Exmor R™

* “Exmor R” is a trademark of Sony Corporation. The “Exmor R” is a Sony's CMOS image sensor with significantly enhanced imaging characteristics including sensitivity and low noise by changing fundamental structure of “Exmor” pixel adopted column parallel A/D converter to back-illuminated type.

Device Structure

- ◆CMOS image sensor
- ◆Image size : Diagonal 2.59 mm (Type 1/6.95)
- ◆Total number of pixels : 1992 (H) × 1256 (V) approx. 2.50 M pixels
- ◆Number of effective pixels : 1992 (H) × 1216 (V) approx. 2.42 M pixels
- ◆Number of active pixels : 1976 (H) × 1200 (V) approx. 2.37 M pixels
- ◆Chip size : 3.818 mm (H) × 3.082 mm (V)
- ◆Unit cell size : 1.12 µm (H) × 1.12 µm (V)
- ◆Substrate material : Silicon

Absolute Maximum Ratings

Item	Symbol	Ratings	Unit	notes
Supply voltage (analog)	VANA	-0.3 to +3.3	V	refer to Vss level
Supply voltage (digital)	VDIG	-0.3 to +2.0	V	
Supply voltage (interface)	VIF	-0.3 to +3.3	V	
Input voltage (digital)	VI	-0.3 to +3.3	V	
Output voltage (digital)	VO	-0.3 to +3.3	V	
Operating temperature	TOPR	-20 to +75	˚C	
Storage guarantee temperature	TSTG	-30 to +80	˚C	
Performance guarantee temperature	TSPEC	-20 to +60	˚C	

Recommended Operating Conditions

Item	Symbol	Ratings	Unit	notes
Supply voltage (analog)	VANA	2.7 +0.2/-0.1	V	refer to Vss level
Supply voltage (digital)	VDIG	1.2 ± 0.1	V	
Supply voltage (interface)	VIF	1.8 ± 0.1	V	

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Contents

Chip Center and Optical Center

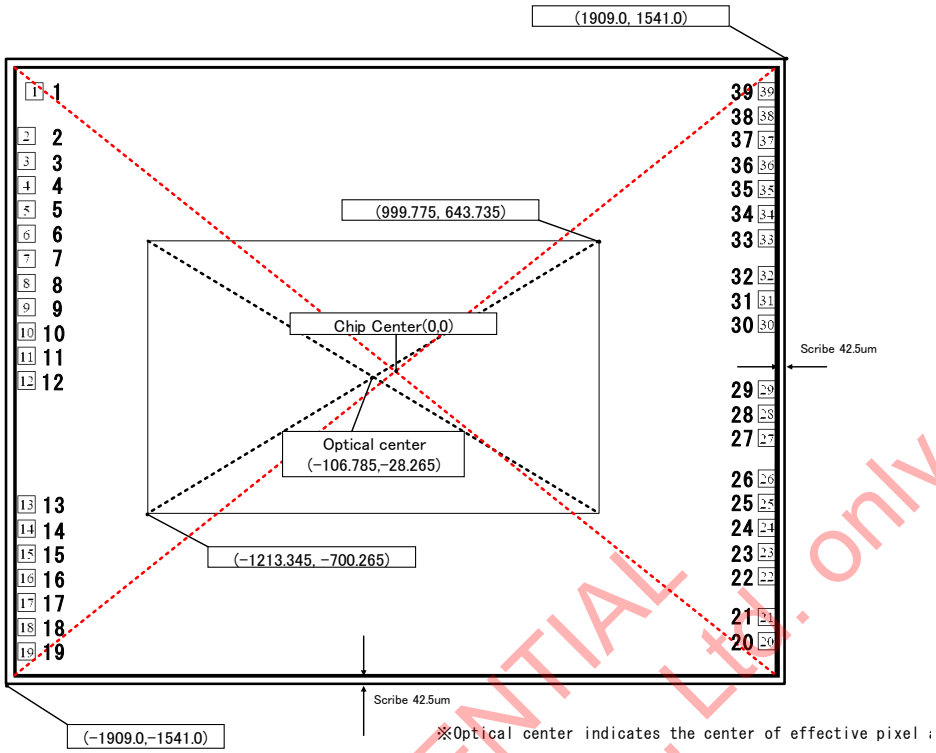


Fig 1. Chip Center and Optical Center (μm, μm)

Pin Coordinates

Table 1. Pin Coordinates

No.	Symbol	X	Y
1	VDDLCN	-1771.50	1379.50
2	VSSLCN	-1811.50	1158.50
3	VDDLIO1	-1811.50	1036.50
4	DMO1P	-1811.50	916.50
5	DMO1N	-1811.50	796.50
6	VSSLIO1	-1811.50	676.50
7	DCKP	-1811.50	556.50
8	DCKN	-1811.50	436.50
9	VSSLIO2	-1811.50	316.50
10	DMO2P	-1811.50	196.50
11	DMO2N	-1811.50	76.50
12	VDDLIO2	-1811.50	-43.50
13	VPO	-1811.50	-654.50
14	VDDHSN1	-1811.50	-774.50
15	VSSHSN1	-1811.50	-894.50
16	VDDSUBD	-1811.50	-1014.50
17	VDDLSC1	-1811.50	-1136.50
18	VSSLSC1	-1811.50	-1256.50
19	VDDHFIL	-1811.50	-1378.50

No.	Symbol	X	Y
20	VSSLSC2	1811.50	-1327.50
21	VDDLSC2	1811.50	-1207.50
22	INCK	1811.50	-1007.50
23	XVS	1811.50	-887.50
24	TMASTER	1811.50	-767.50
25	TENABLE	1811.50	-647.50
26	SDA	1811.50	-527.50
27	SCL	1811.50	-327.50
28	XCLR	1811.50	-207.50
29	VDDMCO	1811.50	-87.50
30	TVMON	1811.50	234.50
31	VSSHAN	1811.50	354.50
32	VDDHAN	1811.50	474.50
33	VSSHSN2	1811.50	654.50
34	VDDHSN2	1811.50	774.50
35	VSSHCM	1811.50	896.50
36	VDDHCM	1811.50	1016.50
37	VSSHCP	1811.50	1138.50
38	VDDHCP	1811.50	1258.50
39	VRL	1811.50	1378.50

Pin Configuration

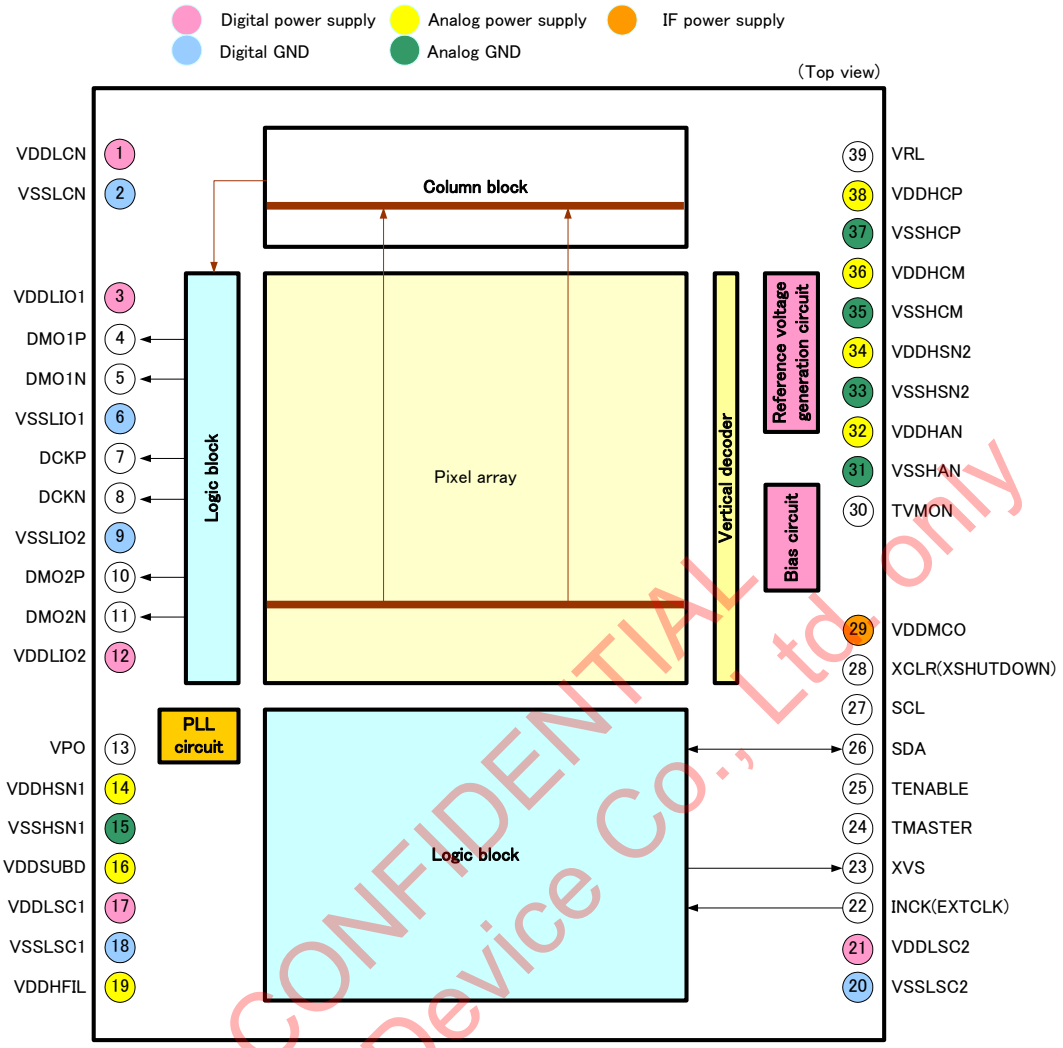


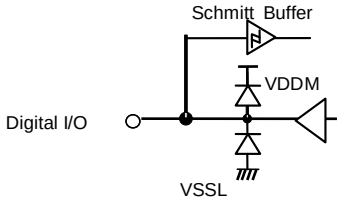
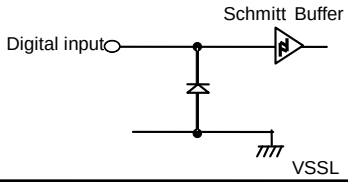
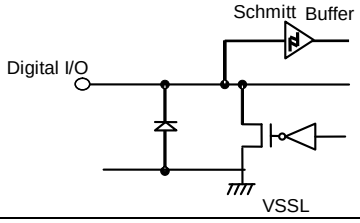
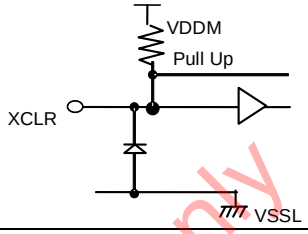
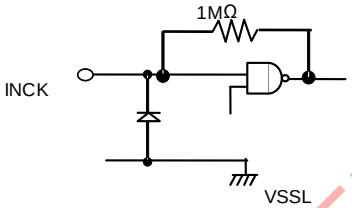
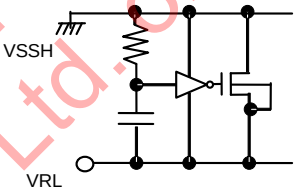
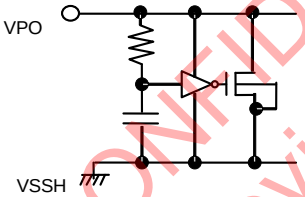
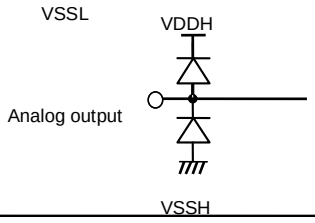
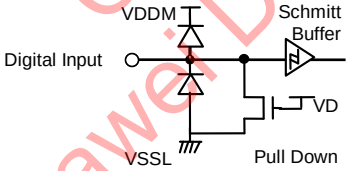
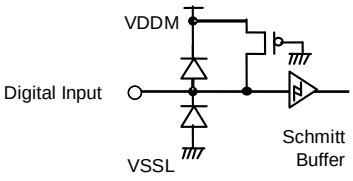
Fig 2. Block Diagram and Pin Configuration

Pin Description

Table 2. Pin Description

No.	Symbol	I/O	A/D	Description	Remarks
1	VDDLCN	Power	D	1.2 V power supply	
2	VSSLCN	GND	D	1.2 V GND	
3	VDDLIO1	Power	D	1.2 V power supply	
4	DMO1P	O	D	Digital output	MIPI output (DATA+)
5	DMO1N	O	D	Digital output	MIPI output (DATA–)
6	VSSLIO1	GND	D	1.2 V GND	
7	DCKP	O	D	Digital output	MIPI output (CLK+)
8	DCKN	O	D	Digital output	MIPI output (CLK-)
9	VSSLIO2	GND	D	1.2 V GND	
10	DMO2P	O	D	Digital output	MIPI output (DATA+)
11	DMO2N	O	D	Digital output	MIPI output (DATA–)
12	VDDLIO2	Power	D	1.2 V power supply	
13	VPO	O	A	Analog output	
14	VDDHSN1	Power	A	2.7 V power supply	
15	VSSHSN1	GND	A	2.7 V GND	
16	VDDSUBD	Power	A	2.7 V power supply	
17	VDDLSC1	Power	D	1.2 V power supply	
18	VSSLSC1	GND	D	1.2 V GND	
19	VDDHFIL	Power	A	2.7 V power supply	Power supply for OTP
20	VSSLSC2	GND	D	1.2 V GND	
21	VDDLSC2	Power	D	1.2 V power supply	
22	INCK	I	D	Digital input	Clock input (EXTCLK)
23	XVS	I/O	D	Digital I/O	
24	TMASTER	I	D	Digital input	NC (with pull-up for test)
25	TENABLE	I	D	Digital input	NC (with pull-down for test)
26	SDA	I/O	D	Digital I/O	I^2C data
27	SCL	I	D	Digital input	I^2C clock
28	XCLR	I	D	Digital input	Chip clear signal (XSHUTDOWN; with pull-up
29	VDDMCO	Power	D	1.8 V power supply	
30	TVMON	O	A	Analog output	NC
31	VSSHAN	GND	A	2.7 V GND	
32	VDDHAN	Power	A	2.7 V power supply	
33	VSSHSN2	GND	A	2.7 V GND	
34	VDDHSN2	Power	A	2.7 V power supply	
35	VSSHCM	GND	A	2.7 V GND	
36	VDDHCM	Power	A	2.7 V power supply	
37	VSSHCP	GND	A	2.7 V GND	
38	VDDHCP	Power	A	2.7 V power supply	
39	VRL	O	A	Analog output	

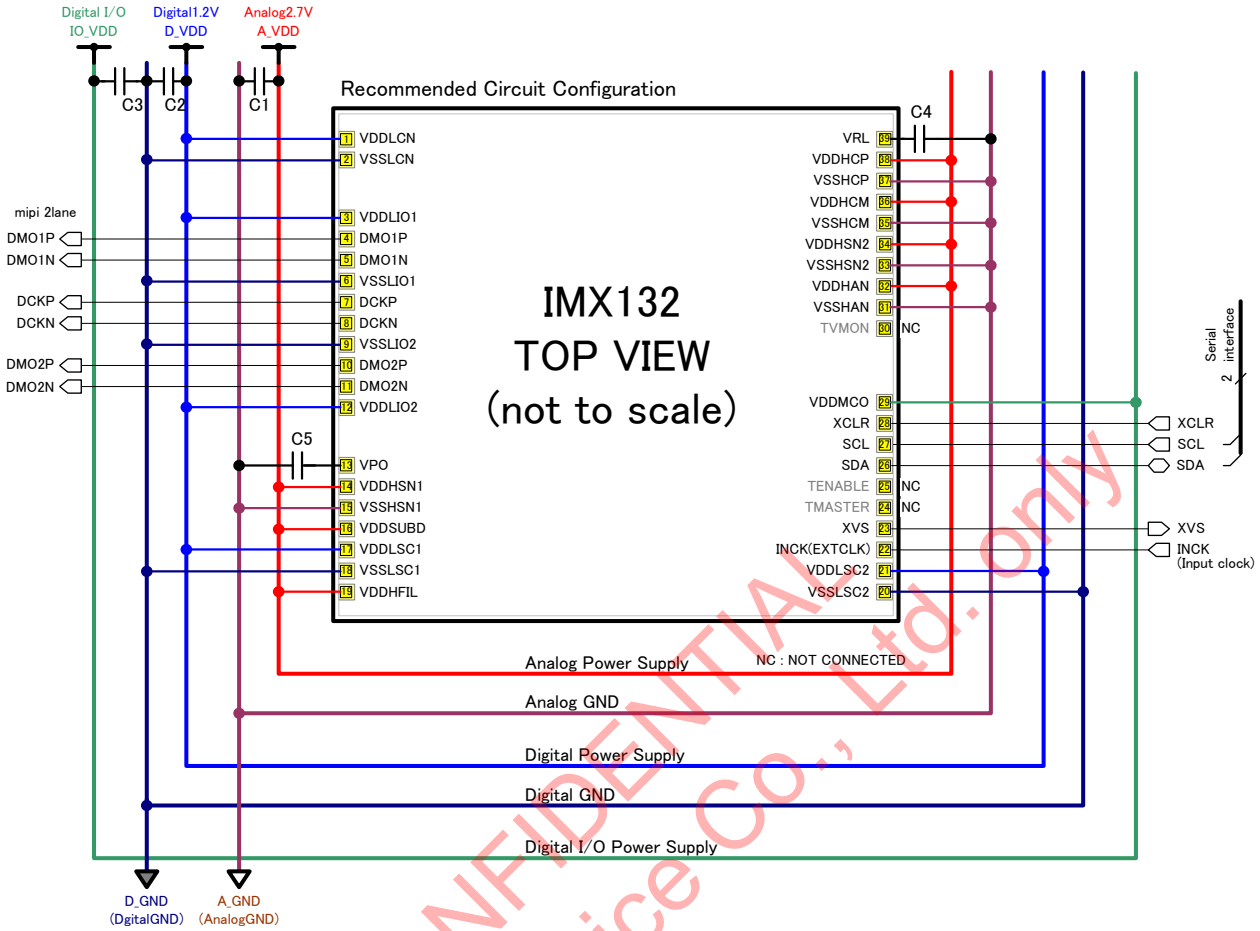
I/O Equivalent Circuit Diagram

Symbol	Equivalent circuit	Symbol	Equivalent circuit
XVS		SCL	
SDA		XCLR	
INCK		VRL	
VPO		TVMON (NC Pin)	
TENABLE (NC Pin)		TMASTER (NC Pin)	

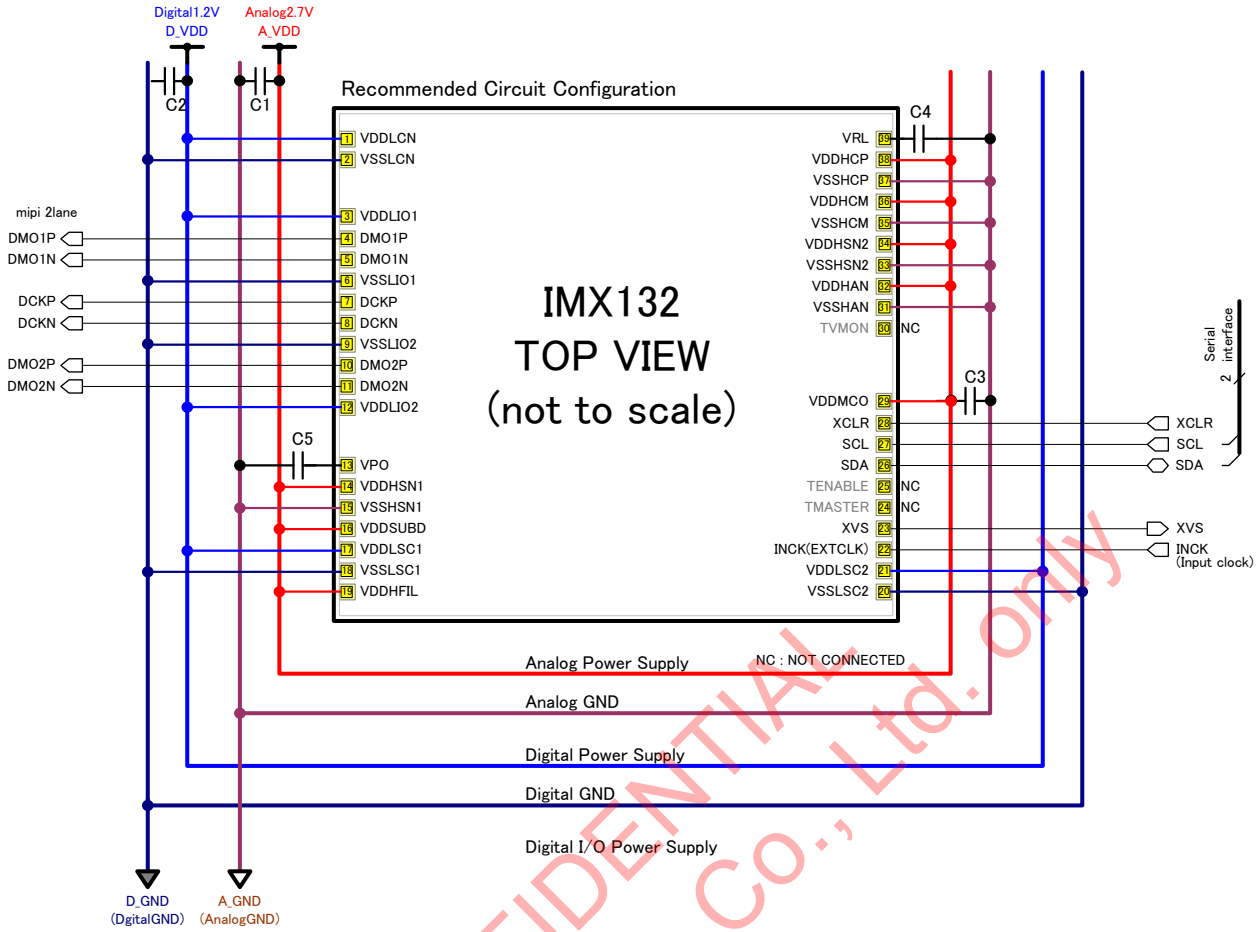
VDDH : 2.7V power supply VDDM : 1.8V power supply VDDL : 1.2V power supply
VSSH : 2.7V GND VSSL : 1.2V GND

Fig 3. Input/Output Equivalent Circuit

Peripheral Circuit



(1) Recommended Circuit



(2) Recommended Circuit (When 2 power supplies)

Fig 4. Reference circuit schematics

Capacitor value	Supplement
C1: 2.2 µF C2: 2.2 µF C3: 0.22 µF C4: 1.0 µF C5: 0.22 µF	♦ XVS It's possible to use XVS as MPO (Multi-purpose Output). If this I/O is not used, nothing is connected with this PAD. ♦ Digital I/O power supply (IO_VDD) Please connect the same power supply as communicated IC with this I/O (Digital I/O power supply)
When fixing the potential of the chip back side, fix it to VDDSUBD potential.	

Functional Description

System Outline

IMX132TQH5-C is a CMOS active pixel type image sensor which adopts the Exmor R technology to achieve high sensitivity, low noise, and high speed image capturing. It is embedded with backside illuminated imaging pixel, low noise analog amplifier, column parallel A/D converters which enables high speed capturing, digital amplifier, image sub-sampling/binning circuit, timing control circuit for imaging size and frame rate, CSI2 image data high speed serial interface, PLL oscillatotr, and serial communication interface to control these functions.
Several binningal image processing functions and peripheral circuits are also included for easy system optimization by the users.

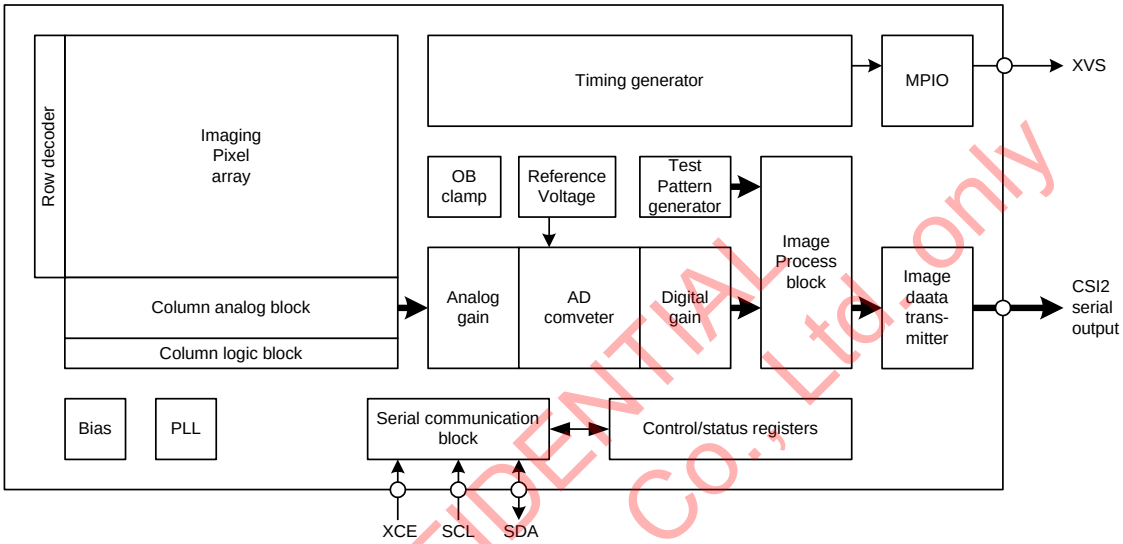


Fig 5. Overview of functional block diagram

Setting Registers Using Serial Communication

Two kinds of serial communication circuit are implemented in IMX132TQH5-C. They are 2-wire serial communication. Data and strobe (clock) wires are shared by those 2 communication circuits. We explain how to use 2-wire serial communication in this product specification sheet.

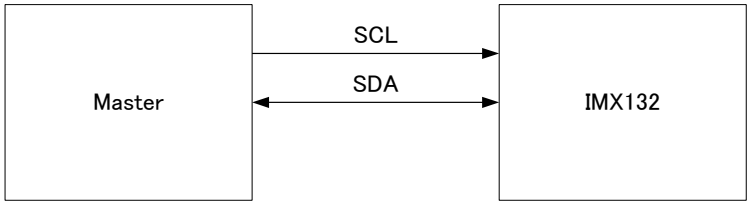


Fig 6. 2-wire serial communication connection instruction

2-wire Serial Communication Operation Specifications

The communication protocol of the 2-wired serial communication is based on the SMIA1.0 Part2 CCP2 Specification Camera Control Interface (CCI) . CCI is the compatible interface of the I²C Fast-mode. The Data transfer protocol follows I²C standard. IMX132TQH5-C should be operated as the slave device of I²C standard. The internal control registers and status registers can be accessed trough 2-wire serial communication.
In power off state, IMX132TQH5-C can be isolated electrically from the 2-wire serial bus by supplying “low” level to XCLR (XSHUTDOWN) . 2-wire serial bus can not be commonly used by the other devices for the case that “low” level cannot be supplied to XCLR (XSHUTDOWN) in power of state.

Table 3. Terminals for 2-wire serial communication

pin name	description
SDA	Serial data input/output pin
SCL	Serial clock input pin

The control registers and status registers of IMX132TQH5-C are mapped on the 16-bit address space and following SMIA standard for the register categories shown as below. Detail regisrter information is shown in RegisterMap

Table 4. Specification of register address map for 2-wire serial communication

	address range	description
I²C register	0x0000 - 0x0fff	Configuration register Read Only and Read/Write Dynamic register
	0x1000 - 0x1fff	Parameter limit register Read Only static resister
	0x2000 - 0x2fff	Reserved for Image statistics register
	0x3000 - 0x3fff	Manufacture specific register
	0x4000 – 0xffff	Reserved

Communication Protocol

2-wire serial communication supports a 16-bit register address and 8-bit data message type.

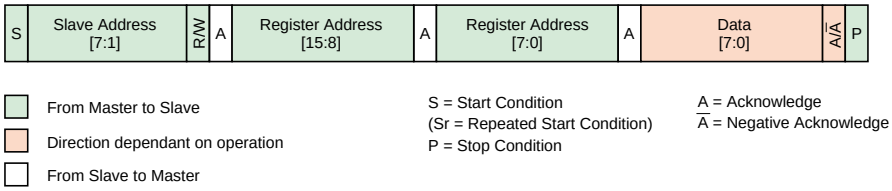


Fig 7. 2-wire serial communication protocol

When called by slave addresses shown as below , Serial communication interface is activated.
Dupplication of the address on the same bus must be prevented.

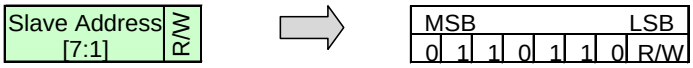


Fig 8. Slave address

R/W shows the direction of communication.

Table 5. R/W bit

R/W bit	direction of communication
0	Write (Master→Sensor)
1	Read (Sensor →Master)

Specification of communication bus state

Idle state

Idle state is specified as follows; Neither master nor slave device does not drive the SDA and SCL, and these bus lines are pulled up to Vdd via resister.

Issue “Start condition”

While idle state of 2-wire communication bus, master device (ex. subsequent Image processing LSI, etc.) issues the communication-start; “start condition; S” by driving SDA from “high” to “low” level. Serial data are transmitted in 8-bit-unit MSB first format. Every 8-bit data transmittion, slave device issues acknowledge or negative acknowledge (explained later) : A (Acknowledge) /Ā (NegativeAcknowledge).
Data (SDA) are tranmitted in time with SCL cycle. SDA shall toggle while SCL is “low” and hold the value while SCL is “high”.

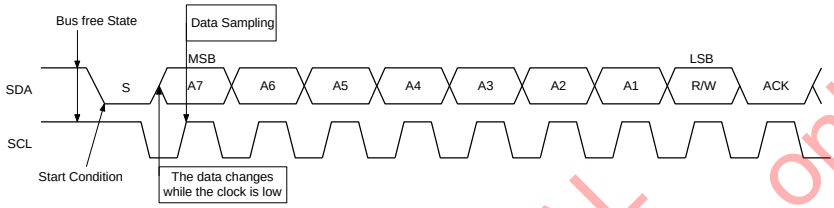


Fig 9. Start Condition

Issue “Stop condition”

After A(Acknowledge)/Ā(NegativeAcknowledge), and while SCL is “high”, master device issues communication-stop; “stop conditon; P” by driving SDA from “low” to “high” level. After issuing “stop”, master release 2-wire serial bus to idle state.

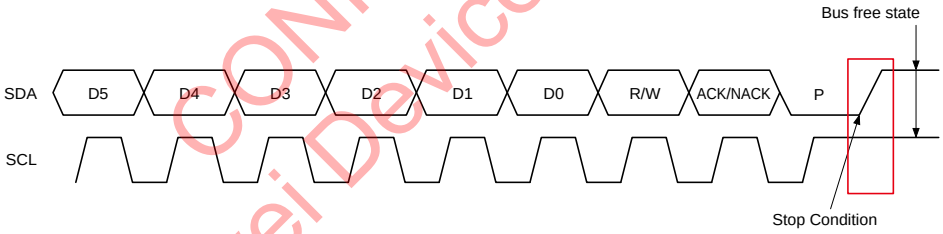


Fig 10. Stop Condition

Issue “Repeated start condition”

Master device does not issue “stop” in previous transmission and can issue “start” instead. In this case this “start condition” is recognized as the “repeated started condition; Sr”.

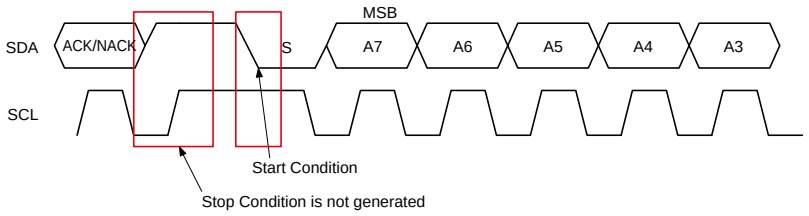


Fig 11. Repeated Start Condition

Issue “Acknowledge/Negative acknowledge”

After transmitting each byte, master or slave device issue “acknowledge/negative acknowledge” and can release the bus to idle state. When negative acknowledge is issued, master must issue the “stop” and terminates the communication immediately.

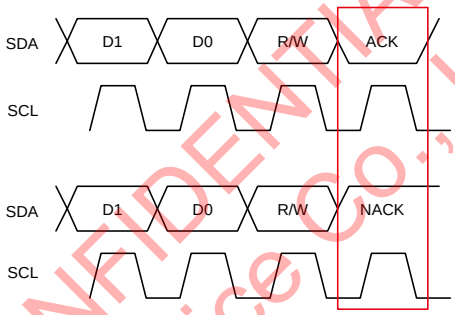


Fig 12. Acknowledge and Negative Acknowledge

Read/Write operation of 2-wire serial communication

IMX132TQH5-C has an index function that indicates which address to be accessed. When reading/writing the value from/to an asked address, the Master must set the address value to the index. Index value is designated by 2-byte of dummy write operation after the slave address transmission. The index value is automatically incremented “one” by the “Acknowledge/Negative Acknowledge” for data transfer.

IMX132TQH5-C supports for of read modes and two of write modes being compliant to SMIA 1.0 Part2 Specification; Camera Control Interface (CCI).

Table 6. Operations Supported by 2-wire Serial Communication

Access mode	1	CCI Single read from random location (Single read from an arbitrary address)
	2	CCI Single read from current location (Single read from the held address)
	3	CCI sequential read starting from random location (Sequential read starting from an arbitrary address)
	4	CCI sequential read starting from current location (Sequential read starting from the held address)
	5	CCI single write to random location (Single write to an arbitrary address)
	6	CCI sequential write starting from random location (Sequential write starting from an arbitrary address)

CCI single read from random location

The upper level of the figure below shows the sensor internal index value, and the lower level shows the SDA I/O data flow. The master sets the sensor index value to M by designating the sensor slave address with a write request,
and then designating the address (M). After that the Master generates the Start condition. The Start condition is generated without generating the Stop condition, so it becomes the Repeated Start condition. Next, when the Master sends the slave address with a read request, the sensor outputs an Acknowledge followed immediately by the index address data on SDA. After the Master receives the data, it generates a Negative Acknowledge and the Stop condition to end the communication.

When reading single datum from asked address register, the master device starts write-operation with the slave address of IMX132TQH5-C and by making 2-bytes of dummy write master sets the address value (M) to the index. After that master issue the “start condition” again instead of issuing “stop condition”. This “start condition” is recognized as “repeated start condition”. Then transmitting the read request with the slave address, IMX132TQH5-C issues the “Acknowledge” and start transmitting the register value from indexed address (M) . Master issue the “Negative Acknowledge” and “stop condition” after receiving the transmission.
The figure below indicates the transition of index value and data on SDA line.

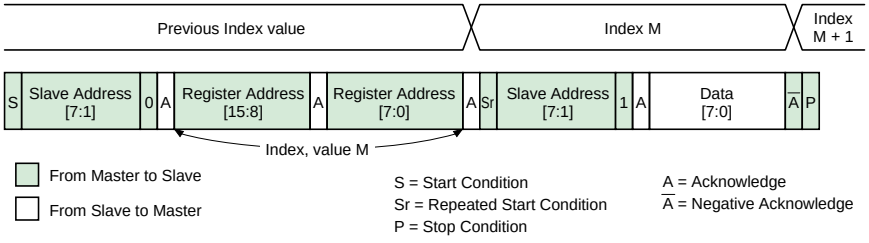


Fig 13. CCI single read from random location

CCI single read from current location

When master transmits slave address, and does not designate index, index value is held. And the inde value is incremented at the “Acknowledge/NegativeAcknowledge” after reading/writeing the register value. When master knows the current index value is set to the asked address, master transmits the slave address and read request, then the value from the register transmitted right after the “Acknowledge” issued by IMX132TQH5-C. Master issues the “Negative Acknowledge” and “Stop” and terminate the communication. Since the index value is incremented one by this “Negative Acknowledge”, master can read the register value of next address with the same procedure.

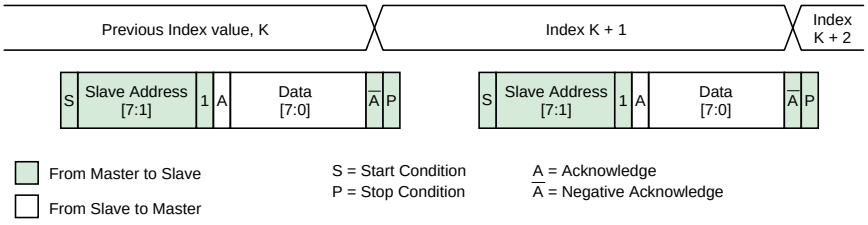


Fig 14. CCI single read from current location

CCI sequential read starting from random location

When reading the data from arbitrary address sequencially, master read the first data by the similar procedure to “CCI single read from random location” but issues the “Acknowledge” instead of “Negative Acknowledge”, the index is incremented one by theis “Acknowledge” then master can repeat the read operation. This operation is terminated when master issues the “Negative Acknowledge”, “Stop condition”, the communication is terminated.

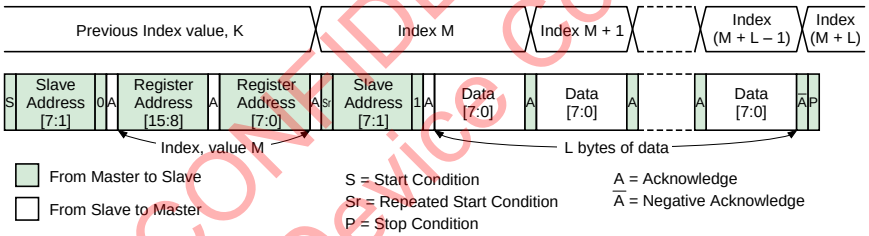


Fig 15. CCI sequential read starting from random location

CCI sequential read starting from current location

When master knows the current index value is set to the asked address, master transmits the slave address and read request, then the value from the register transmitted right after the “Acknowledge” issued by IMX132TQH5-C. Master issues the “Acknowledge” after receiving 1-byte of the data and IMX132TQH5-C continuously tranmits the data from the next address of register since the index value is incremented one by this “Acknowledge”. By repeating to issue the “Acknowledge” for evey 1-byte reading, master can read the data sequentially. After reading necessary bytes of data, master issues “Negative Acknowledge” and “stop condition” and then terminates the communication.

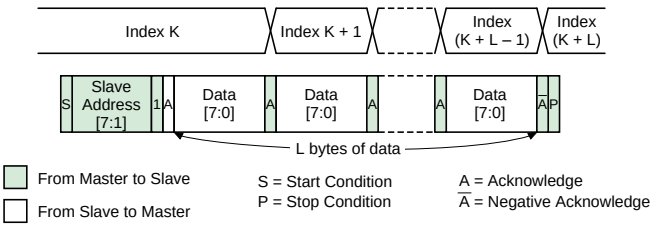


Fig 16. CCI sequential read starting from current location

CCI single write to random location

When writing single datum to asked address register, the master device starts write-operation with the slave address of IMX132TQH5-C and by making 2-bytes of dummy write master sets the address value (M) to the index. And then master transmits the data to be written to the register addressed by index value. Master issue “stop condirion” after transmits the data and terminates the communication.

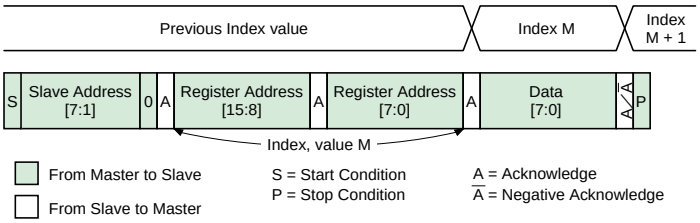


Fig 17. CCI single write to random location

CCI sequential write starting from random location

When master writes the data sequentially from asked address, master takes similar procedure to “CCI single write torandom location” and without issuing “stop condition” and continuously transmits the data after each “Acknowledge” issued by. IMX132TQH5-C.IMX132TQH5-C issues “Acknowledge”s each 1-byte write operation. After transmitting necessary data, master issues “stop condition” and terminates the communication.

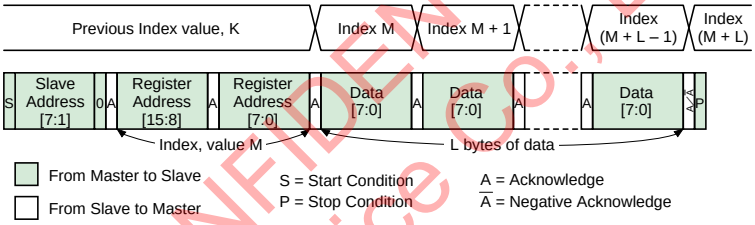


Fig 18. CCI sequential write starting from random location

2-wire serial communication register update timing

There are two types of registers in terms of the update timing of the transmitted data: the immediate type and the double buffered type. For immediate type registers, the tramsmitted data will be written to the registers immediately. As for the double buffered type registers, the actual update timing of the register contents are controlled to the proper timing and become valid in next frame. Users can transmit the commands regardless of the internal update timing of IMX132TQH5-C. The registers of double buffered type are indicated in the “upfdate”column of the register table.

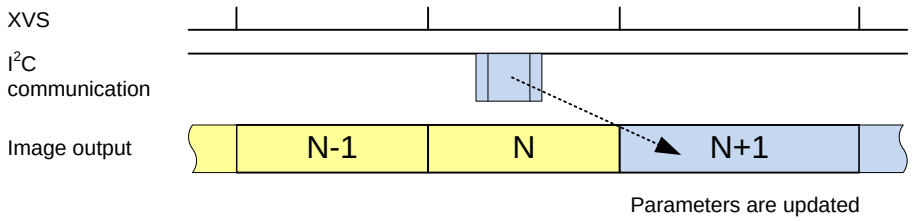


Fig 19. 2-wire serial communication register update timing diagram

Grouped parameter hold function

The image shooting parameters are assigned to many registers and they need to be changed within one frame period of the image. However the communication speed is limited and might not be completed setting all of necessary registers. So the double buffered type registers have the “grouped parameter hold” function to behave to be upfated at once.While “grouped parameter hold” register is set to “1” the transmitted data are hold in the buffer registers and after reset “grouped parameter hold” register to “0”, imaging parameter register values are updated as if they are transmitted at the same time and realize smooth transition of changing the imaging condition.

Table 7. grouped_parameter_hold

I²C register	address	Bit	name	description	notes
	0x0104	[0]	grouped_parameter_hold	0 : Normal operation (No hold) 1 : Hold the value of registers indicated in “update timing” column.	

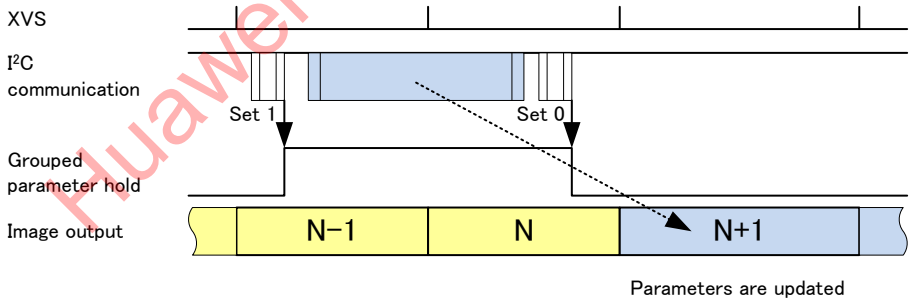


Fig 20. Grouped parameter hold function timing diagram

Mode transition sequence

Integrationtime change sequence

Set the value 1 to “grouped_parameter_hold” register and set the integration duration value to “coarse_integration_time” register. Then reset 0 to “grouped_parameter_hold” register. The integration time is changed from next frame and the image shooted with new integration time is output from 2nd frame after reset “grouped_parameter_hold” register.

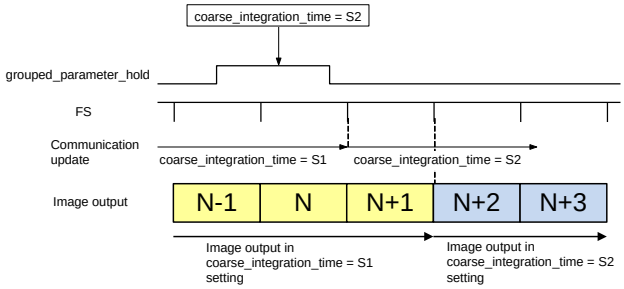


Fig 21. Integration time change sequence

Gain change sequence

Set the values to analogue_gain_code_global/digital_gain_greenR/digital_gain_red/digital_gain_blue/digital_gain_greenB registers. Then reset 0 to “grouped_parameter_hold” register. The gain values are changed from next frame and the image shooted with new gains is output from 2nd frame after reset “grouped_parameter_hold” register.

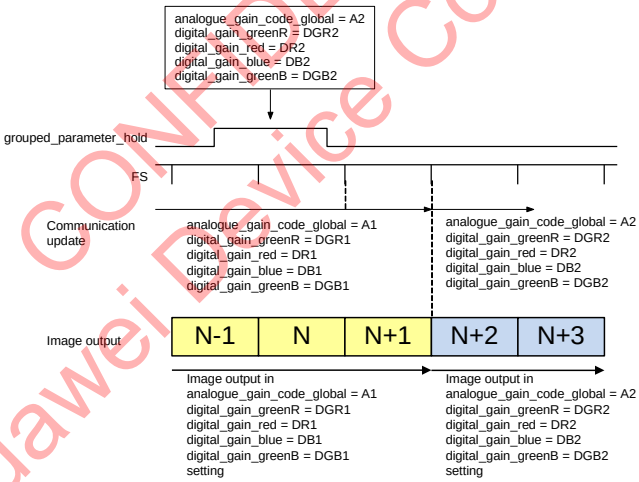


Fig 22. Gain change sequence

Vertical direction readout parameter change sequence

Vertical direction mode change sequence

When changing the mode with vertical direction parameters, photo-electron charge integration operation becomes irregular for one frame after updating of the register. This frame shall be treated as invalid frame.

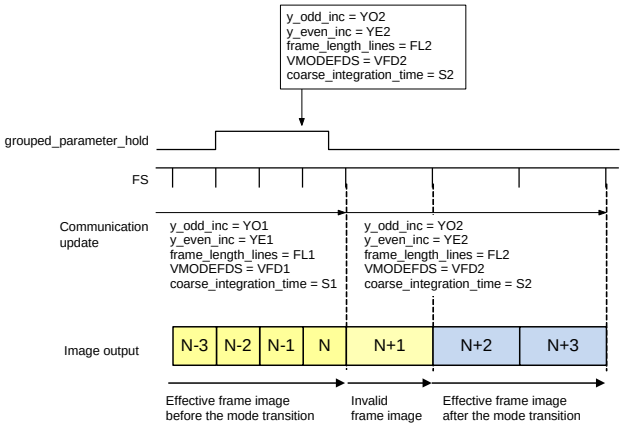


Fig 23. Vertical direction mode change sequence

Vertical flip sequence

When vertically flipping the readout direction, photo-electron charge integration operation becomes irregular for one frame after mode transition. This frame shall be treated as invalid frame.

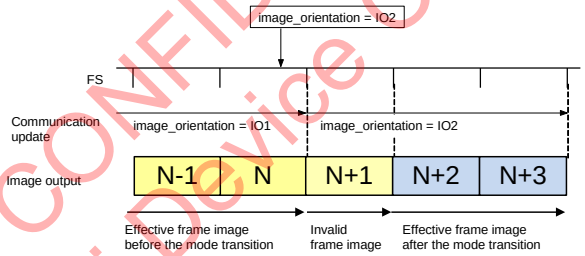


Fig 24. Vertical flip sequence

Clock and PLL

IMX132TQH5-C equips embedded PLL to generate the necessary internal clocks and CSI2 tranmission clocks. Set the related registers according to the operation condition.

Structure of PLLblock

The PLL circuit of IMX132TQH5-C can generate a clock signal at a frequency ranging from 384 MHz up to 1,000 MHz based on an input clock of 6 MHz to 60 MHz.
PLL block contains pre divider circuit with ratio 1, 1/2, 1/4 and 1/8 at the input side of the PLL, post divider circuit with ratio 1, 1/2 and 1/4 at the output side, and the feedback divider with a multiplier of 8 to 183 times which can be set as long as the PLL oscillator frequency is kept within the specified range.

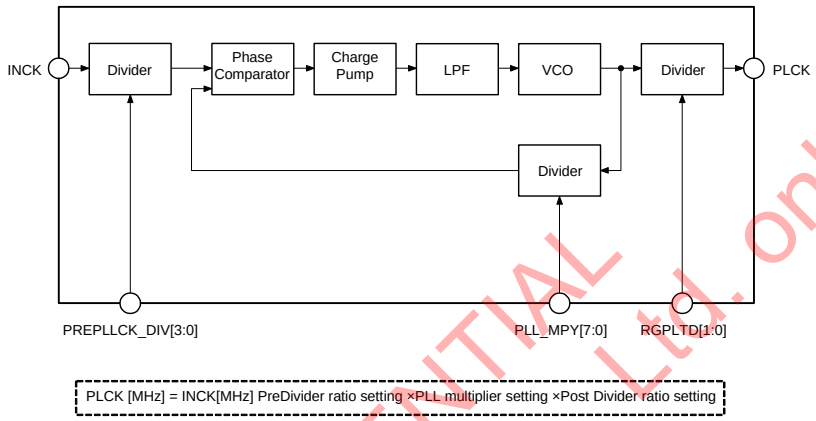


Fig 25. Structure of PLL block

Table 8. PLL pre divider setting

	address	Bit	name	description	notes
I²C register	0x0305	[3:0]	PREPLLCK_DIV	1 (dec) : 1/1 2 (dec) : 1/2 4 (dec) : 1/4 8 (dec) : 1/8 *Setting other than the above is forbidden	

Table 9. PLL post divider setting

	address	Bit	name	description	notes
I²C register	0x30a4	[1:0]	RGPLTD	0 (dec) : 1/2 1 (dec) : 1/4 2 (dec) : 1 3 (dec) : 1	

Table 10. PLL multiplier setting

	address	Bit	name	description	notes
I²C register	0x0307	[7:0]	PLL_MPY	equal or less than 7 (dec) : inhibited value 8 (dec) : 8 9 to 182 (dec) : 9 to 182 183 (dec) :183 equal of greater than 184 (dec) : inhibited value	

Clock frequency setting examples

Table 11. PLL frequency table

Mode	Input Clock (INCK (EXTCLK))	Pre division	Multiple	Post division	PLL Input frequency	VCO Oscillation frequency	PLL Oscillation frequency
Raw10 Mipi 2 Lane	6 MHz	1	135	1	6.0 MHz	810.0 MHz	810.0 MHz
	12 MHz	2	135	1	6.0 MHz	810.0 MHz	810.0 MHz
	13.5 MHz	1	60	1	13.5 MHz	810.0 MHz	810.0 MHz
	18 MHz	1	45	1	18.0 MHz	810.0 MHz	810.0 MHz
	24 MHz	4	135	1	6.0 MHz	810.0 MHz	810.0 MHz
	27 MHz	2	60	1	13.5 MHz	810.0 MHz	810.0 MHz
	36 MHz	2	45	1	18.0 MHz	810.0 MHz	810.0 MHz

Table 12. Output mode and PLL frequency

Mode	Frame Rate	PLCK	Data Rate	Pixel Rate
Raw10-2Lane All-pix	60 fps	810 MHz	810 [Mbps/Lane]	162.0 MHz
Raw10-2Lane V/H 1/2 (elimination)	120 fps	810 MHz	405 [Mbps/Lane]	81.0 MHz
Raw10-2Lane V/H 1/3 (elimination)	120 fps	810 MHz	270 [Mbps/Lane]	54.0 MHz
Raw10-2Lane V/H 1/4 (elimination)	240 fps	810 MHz	203 [Mbps/Lane]	40.5 MHz
Raw10-2Lane V 1/6, H 1/4 (elimination)	240 fps	810 MHz	203[Mbps/Lane]	40.5 MHz
Raw10-2Lane V 1/8, H 1/4 (elimination)	474fps	810 MHz	203[Mbps/Lane]	40.5 MHz
Raw10-2Lane V/H 2/3	60 fps	540 MHz	540 [Mbps/Lane]	108.0 MHz

Supplemental description of operation clocks

PLCK : PLL output

This clock is the root of all the operation clocks in IMX132TQH5-C and it designates the data rate. DCKP/DCKN; CSI2 interface clock is generated from PLCK by dividing into 1/2 frequency since the interface is operated in double data rate format.

PLCK = EXTCLK frequency × PreDivider setting × PLL multiple setting × PostDivider setting

Logic Clock

The clock for intenalimage processing is generated by dividing into 1/10 or 1/8 frequency according to the word length of the CSI2 interface. This clock is designating the pixel rate and used as the base of integration time, frame rate, and etc.

Logic clock frequency = PLCK × Logic clock division ratio

Table 13. Logic clock division ratio

	2 Lane		1 Lane	
Logic clock division ratio	RAW8	RAW10	RAW8	RAW10
	1/8	1/10	1/16	1/20

* Logic clock division ratio is decided by a lane number.

Image Readout Operation

By settimg the parameters of PLL, image size, start/end position of the imaging area, direction of reading image, sub-sampling/binning, shutter mode, integration time, gain, and ooutput format via 2-wire serial communication, IMX132TQH5-C outputs the image data.

Phyical alignment of imaging pixel array

The figure below shoes the physical alignment of the imaging pixel array with Pin #1 located at the upper left corner.

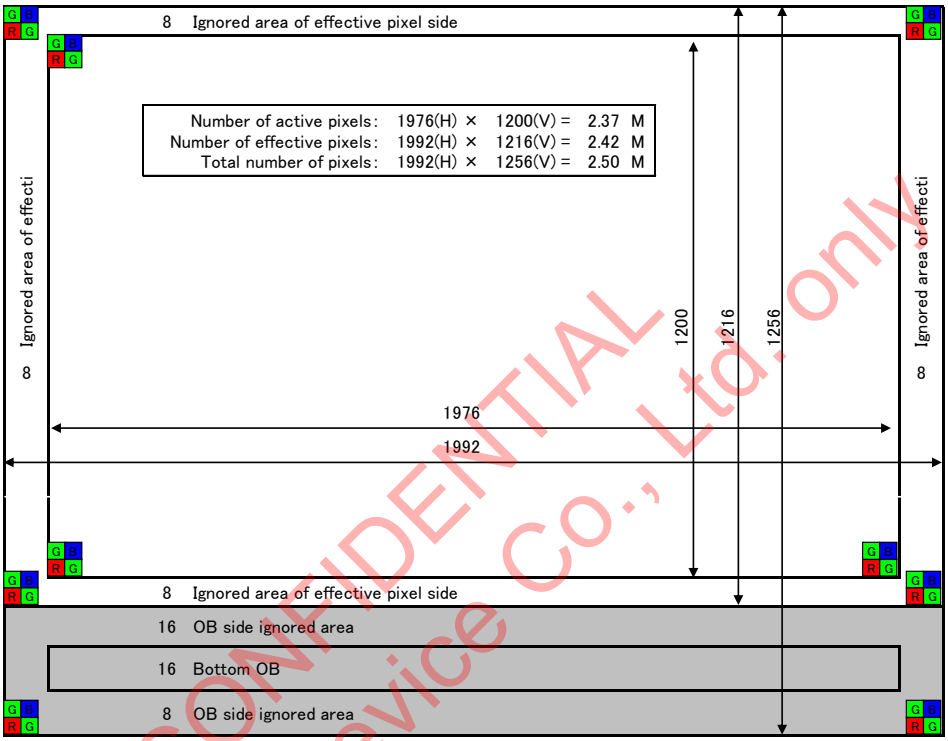


Fig 26. physical alignment of the imaging pixel array

Color coding and order of reading image date

The original color filter arrangement of the sensor is shown in the figure below. Gr and Gb are the G signals shown at the same line as R signals and B signals, respectively. The line with R & Gr signals and the line with Gb & B signals are output one after the other alternatively.

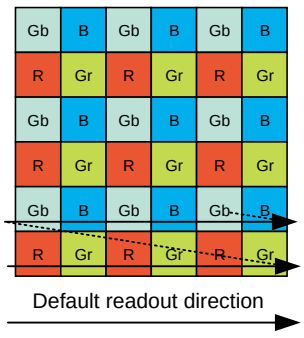


Fig 27. Color coding alignment

Imaging area determination

Imaging area is specified on the physical pixel array and determined by registers shown as below.

Table 14. Imaging area determining registers

	address	Bit	name	description	notes
I²C register	0x0344	[4:0]	x_addr_start[12:8]	Readout start position in horizontal direction	
	0x0345	[7:0]	x_addr_start[7:0]		
	0x0346	[4:0]	y_addr_start[12:8]	Readout start position in vertical direction	
	0x0347	[7:0]	y_addr_start[7:0]		
	0x0348	[4:0]	x_addr_end[12:8]	Readout end position in horizontal direction	
	0x0349	[7:0]	x_addr_end[7:0]		
	0x034A	[4:0]	y_addr_end[12:8]	Readout end position in vertical direction	
	0x034B	[7:0]	y_addr_end[7:0]		
	0x034C	[4:0]	x_output_size[12:8]	Readout size in horizontal direction	
	0x034D	[7:0]	x_output_size[7:0]		
	0x034E	[4:0]	y_output_size[12:8]	Readout size in vertical direction	
	0x034F	[7:0]	y_output_size[12:8]		

Frame structure

Each line of each image frame will be output complying with the General Frame Format of CSI2.
The period from line end sync code; Packet Footer (PF) to line start sync code; Packet Header (PH) of the next line is called “line blanking”.
Similarly, the period from frame end sync code; Frame End (FE) to frame start sync code; Frame Start (FS) of the next frame is called “frame blanking”.
Frame size is determined by “frame_length_line” in vertical direction and “line_length_pck” in horizontal direction.

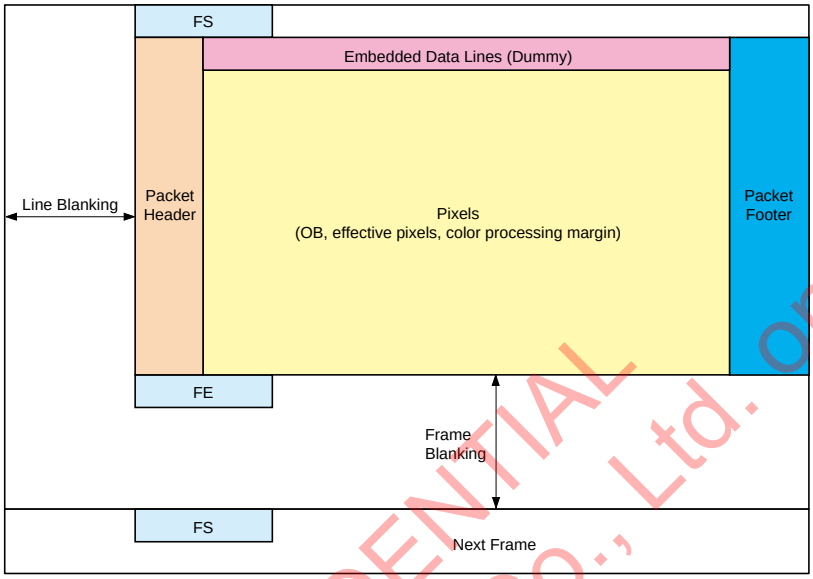


Fig 28. 2 Lane Frame format of serial image output

Table 15. frame size determining registers

	address	Bit	name	description	notes
I²C register	0x0340	[7:0]	frame_length_line[15:8]	Total line number of the frame	
	0x0341	[7:0]	frame_length_line[7:0]		
	0x0342	[7:0]	line_length_pck[15:8]	Total pixel number of the line	
	0x0343	[7:0]	line_length_pck[7:0]		

Output Image Format

This is the output image diagram of full pixel output mode, Image data is output from the upper left corner of the diagram.

Fig 29. Full pixel output mode data structure

Contents of packet header

The contents of the first byte in the packet header (Data Identifier) and the corresponding register settings are described in the table below.

Table 16. Data Identifier

	Bit assignment	value	name	Corresponding registers (IIC)	description
Packet header	[7:6]	CCP2_CH_ID [1:0]	Virtual Channel Indentifier	I^2C address:0x 0110 CCP2_CH_ID[2:0]	Refers LSB 2 bits
	[5:0] Synch Short Packet Data types	6'h00	Frame Start Code	NA	
		6'h01	Frame End Code	NA	
		6'h10	Null	NA	For invalid data and dummy data
		6'h12	Embedded Data	NA	For embedded data line
		6'h13	OPB Data	NA	For OPB lines
		6'h2A	RAW8	Addr : 0113, 0112 CCP_DT_FMT[15:0]	16'h0808
		6'h2B	RAW10		16'h0A0A

Data type

Data types of each line are shown as below.

Table 17. Image pixel area and data type

image pixel area	Data Type
Embedded Data Lines	Embedded Data
OBside ineffective area	Null
OB area for internal use	Null
effective OB	OPB Data
Effective area side ineffective area	Null
effective pixel	RAW10 or RAW8

Embedded Data Line control

It is possible to output certain 2-wire serial register contents on the 2 lines just after the FS sync code of the frame.
The corresponding registers are indicated by “Embd DL” column of the register table.
An unfixed value is outputted when not outputting embedded data.

Table 18. Embedded Data Line output control

	address	Bit	name	description	notes
I^2C register	0x30f6	[5]	EBDMASK	0 : Enable output of Embedded data 1 : Disable output of Embedded data	

Output data sequence is designated by data format of CSI2 IF. In RAW10 mode, dummy bytes “55h” are inserted after 4-bytes or Tag bytes.

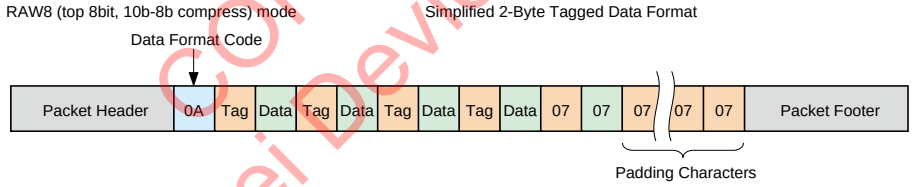


Fig 30. Embedded data lines alignment in RAW8 mode

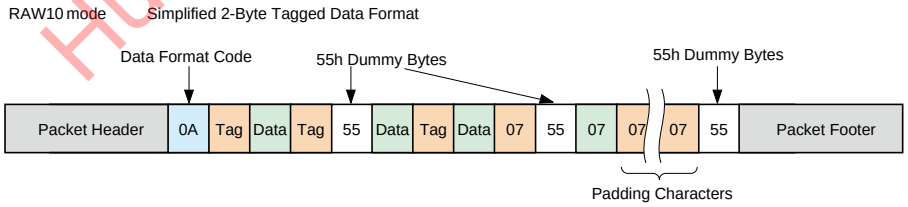


Fig 31. Embedded data lines alignment in RAW10 mode

The addresses and the end of register value are distinguished by “Tags” embedded in the data sequence.

Table 19. Embedded Data Line Tag

Tag	Data Byte Description
00h	Illegal Tag. If found treat as end of Data
07h	End of Data (Data Byte Value = 07H)
aah	CCI Register Index MSB [15:8]
a5h	CCI Register Index LSB [7:0]
5ah	Auto increment the CCI index after the data byte – valid data Data byte contains valid CCI register data
55h	Auto increment the CCI index after the data byte – null data A CCI register does NOT exist for the current CCI index. The data byte value is the 07H
ffh	Illegal Tag. If found treat as end of Data

The definite data sequence is described in the table in Appnedix.

Image size of each sub-sampling mode

By setting the registers for line and pixel skipping factors for sub-sampling, IMX132TQH5-C outputs various re-sized (shrunk) image. Examples are shown in the table below.

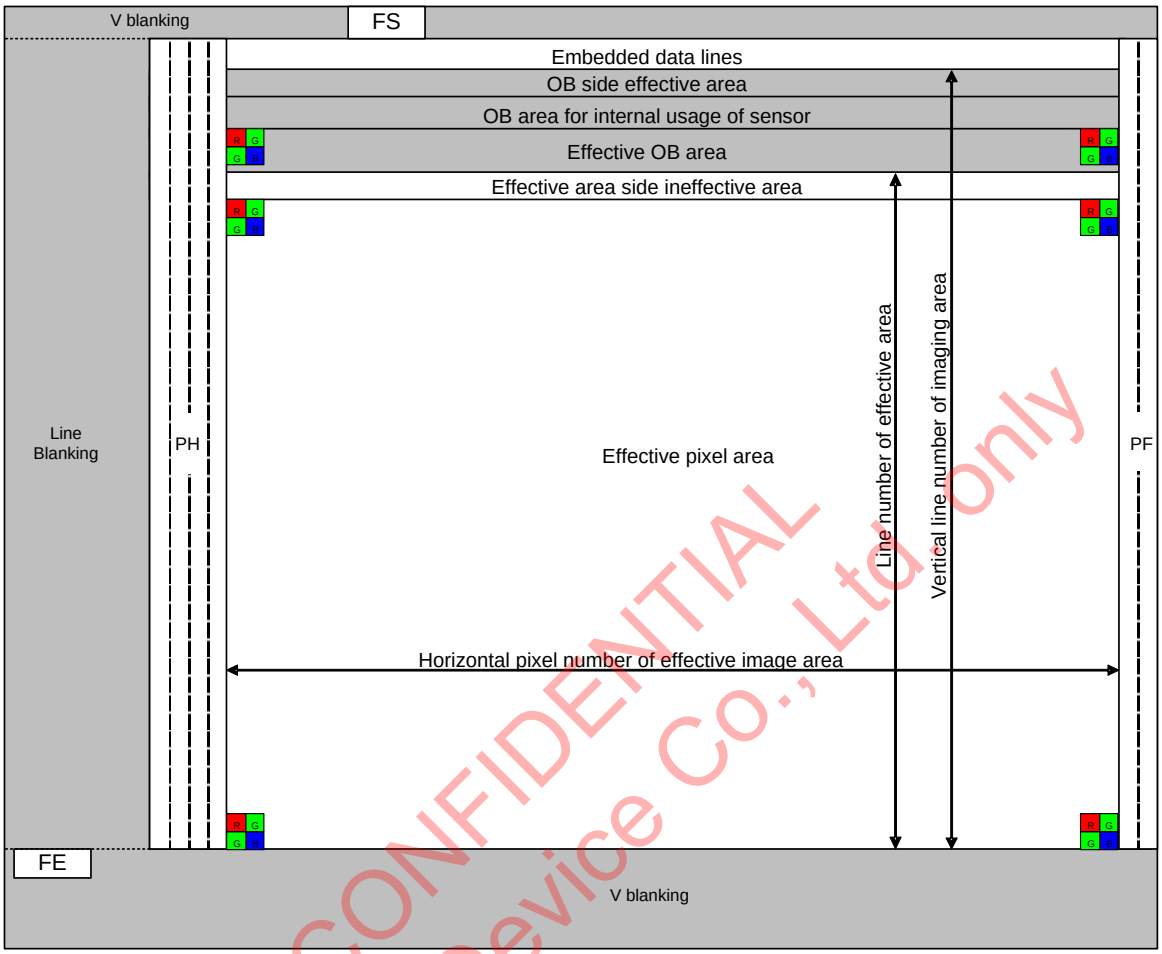


Fig 32. Image size parameter definition

Table 20. Sub-sampling modes and image sizes

		All-pixel Full HD		Sub-sampling modes											
				V:1/2, H:1/2		V:1/3, H:1/3		V:1/4, H:1/4		V:1/6, H:1/4		V:1/8, H:1/4		V:2/3, H:2/3	
Vertical line number of imaging area		1164		584		388		294		196		148		778	
Horizontal pixel number of imaging area		1976		748		500		376		376		376		1316	
Number of lines and start position		Number of lines	start position	Number of lines	start position	Number of lines	start position	Number of lines	start position	Number of lines	start position	Number of lines	start position	Number of lines	start position
name of the areas	Frame Start	1	1	1	1	1	1	1	1	1	1	1	1	1	1
	Embedded data lines	2	2	2	2	2	2	2	2	2	2	2	2	2	2
	OB side Ineffective area	2	4	2	4	2	4	2	4	2	4	2	4	2	4
	OB area for internal usage of sensor	2	6	2	6	2	6	2	6	2	6	2	6	2	6
	Effective OB area	14	8	6	8	2	8	2	8	0	8	0	8	10	8
	Effective area side Ineffective area	2	22	2	14	2	10	2	10	2	8	2	8	2	18
	Line number of effective pixel area	1144	24	572	16	380	12	286	12	190	10	142	10	762	20
	Frame End	1	1168	1	588	1	392	1	298	1	200	1	152	1	782

Description about Sub-sampling and Binning operation

IMX132TQH5-C has both vertical and horizontal sub-sampling function. And the sub-sampling interval can be independently set for vertical and horizontal direction.
In binning, IMX132TQH5-C has the binning function both vertically and horizontally.
By combined methods of sub-sampling and binning, and setting the positions of start pixel and end pixel, it is possible to output the expected image of smaller size. Also, by methods of vertical and horizontal binning, high sensitivity output can be achieved.

Table 21. Sub-sampling mode interval setting

	address	Bit	name	description	notes
I²C register	0x3281	[3:0]	x_even_inc	Horizontal direction skipping factor for even turn	
	0x0383	[3:0]	x_odd_inc	Horizontal direction skipping factor for odd turn	
	0x0385	[3:0]	y_even_inc	Vertical direction skipping factor for even turn	
	0x0387	[3:0]	y_odd_inc	Vertical direction skipping factor for odd turn	

In vertical direction, there are analog binning mode accomplished by shared FD and digital binning mode. In horizontal direction, it is possible to add upto 8 pixels as the digital processing.

Table 22. Binning mode setting

	address	Bit	name	description	notes
I²C register	0x3048	[0]	VMODEFDS	Binning operation by Analog addition average	
		[1]	VMODEADD	Binning operation by Digital addition average	
		[4:2]	Reserved	Reserrved	
		[7:5]	VMODEADDJMP[2:0]	Vertical binning line select	
	0x306A	[5]	Y_SP_ELIMINATION	2/3 verticall special binning mode enable	
	0x30D5	[0]	HADDEN	select sub-sample/binning mode	
		[1]	HADDMODE	horizontal binning mode select	
		[2]	HDSMPLMODE	HD mode horizontal sub-sampling mode select	
		[3]	HADCONFIG	coefficient select	
		[4]	Reserved	Rewrite inhibitted	
		[5]	X_SP_ELIMINATION	2/3 horizontal special binning mode enable	
		[6]	Reserved	Rewrite inhibitted	
		[7]	HDIV_AUTOCKSEL	Auto clock control	

The example of combination of sub sampling mode and binning mode

The example below combines the V (1,3) sub sampling vertical analog binning combined with H (1,3) sub sampling weighed binning-averaging. This sub sampling mode eliminates pixels other than the pixels enclosed by bold lines, but high sensitivity sub sampling can be obtained without degrading the image quality by performing vertical analog binning-averaging and horizontal binning-averaging. Binning is performed in vertical direction, so the pixel signal output is doubled (×2) and the random noise level becomes √2 times. In binning, binning-averaging are performed in the horizontal direction, so the pixel signal output does not change, but the random noise level becomes 1/√2 times. As a result, the total output sensitivity is doubled (×2) , and the random noise level remains the same (×1) .

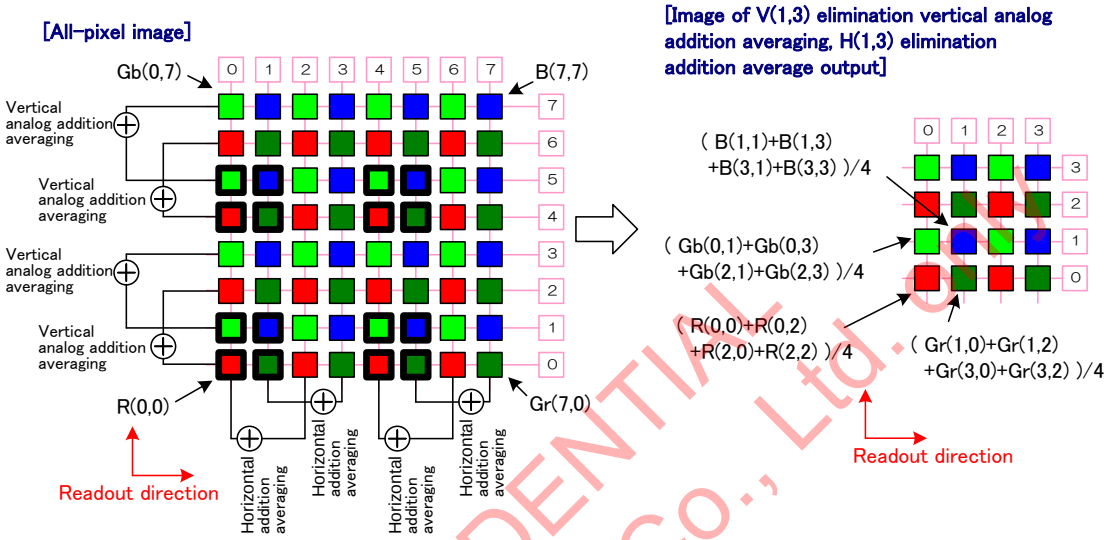


Fig 33. Outline of vertical sub-sampling with analog binning-averaging and horizontal sub-sampling with binning-averaging

Numbers enclosed in pink line rectangles in the figure represent addresses in the format “color-type (x,y) ”. The R pixel in the lower left corner is expressed as R (0,0) .
When performing V (1,3) sub sampling binning and H (1,3) sub sampling binning-averaging,R (0,0) after sub sampling is obtained by the following equation.

$$R\ (0,0)\ \text{after sub sampling} = R\ (0,0) = (\ R\ (0,0) + R\ (0,2) + R\ (2,0) + R\ (2,2)\ ) / 4$$

1/2 sub sampling is performed in the horizontal direction, so the total number of pixels after sub sampling is 1/4 of the original number.

The other example and detail behavior of sub-sample, binning, and combinations of them are described in APPENDIX.

Notes when applying vertical analog binning-averaging

When vertical analog binning-averaging is performed at a luminous under which standard output can be obtained without performing vertical analog binning-averaging, the input range of A/D comverter is exceeded. In this case the input luminous intensity can be limited by the electric shutter, but this means that the signal level is kept within the A/D range by reducing the electrons generated in the photodiode, which is undesirable in terms of the relationship between the signal and light shot noise (*) .
Therefore, the IMX132TQH5-C has a operation mode that widens the A/D input range by ×2 to support the signal increase during vertical analog binning-averaging. When applying analog binning-averaging, usually this operation mode is selected.

(*) Light shot noise…It's derived from fluctuation of the number of injected photons explained by quantum mechanics. it is in proportion to squre-root of number of injected photons.

Table 23. Widen input range of A/D Converter

	address	Bit	name	description	notes
I^2C register	0x309B	[3]	RGDAFDSUMEN	0 : Normal input range of AD converter 1 : Widen input range of AD converter double	

List of pixel binning modes and settings in vertical direction

Possible register settings of sub-sampling mode in vertical direction for IMX132TQH5-C are shown as below.

Table 24. Vertical direction sub-sampling mode

	Mode list				Register settings							
Vertical direction	Communication method	Operation mode	Subsampling ratio	Binning	y_evn_inc	y_odd_inc	VMODEFDS	VMODE ADD	VMODE ADDJMP	Y_SP_ELIMINATION	RGV2 BITEN	RGDAFD SUMEN
					0x0385[3:0]	0x0387[3:0]	0x3048[0]	0x3048[1]	0x3048[7:5]	0x306A[5]	0x309B[2]	0x309B[3]
	I²C	Normal mode	(1, 1) subsampling = All pixcels	—	1	1	0	0	0	0	0	0
			(1, 3) subsampling = 1/2	—	1	3	0					0
				○ (vertical analog binning averaging)			1					1
			(3, 1) subsampling = 1/2	—	3	1	0					0
				○ (vertical analog binning averaging)			1					1
			(3, 3) subsampling = 1/3	—	3	3	0					0
			(3, 5) subsampling = 1/4	—	3	5	0					0
				○ (vertical analog binning averaging)			1					1
			(5, 3) subsampling = 1/4	—	5	3	0					0
				○ (vertical analog binning averaging)			1					1
			(5, 7) subsampling = 1/6	—	5	7	0					0
			(7, 5) subsampling = 1/6	—	7	5	0					0
			(7, 9) subsampling = 1/8	—	7	9	0					0
				○ (vertical analog binning averaging)			1					1
			(9, 7) subsampling = 1/8	—	9	7	0					0
				○ (vertical analog binning averaging)			1					1
	Communication method	Operation mode	Subsampling ratio	Binning	y_evn_inc	y_odd_inc	VMODEFDS	VMODE ADD	VMODE ADDJMP	Y_SP_ELIMINATION	RGV2 BITEN	RGDAFD SUMEN
					0x0385[3:0]	0x0387[3:0]	0x3048[0]	0x3048[1]	0x3048[7:5]	0x306A[5]	0x309B[2]	0x309B[3]
	I²C	Vertical digital binning averaging mode	(1, 3) subsampling = 1/2	○ (vertical digital binning averaging)	1	3	0	1	1	0	1	0
			(3, 1) subsampling = 1/2	○ (vertical digital binning averaging)	3	1	0		1	0		0
			(3, 3) subsampling = 1/3	○ (vertical digital binning averaging)	3	3	0		1~2	0		0
			(3, 5) subsampling = 1/4	○ (vertical digital binning averaging)	3	5	0		1~3	0		0
				○ (vertical digital +analog binning averaging)			1		2	0		1
			(5, 3) subsampling = 1/4	○ (vertical digital binning averaging)	5	3	0		1~3	0		0
				○ (vertical digital +analog binning averaging)			1		2	0		1
			(5, 7) subsampling = 1/6	○ (vertical digital binning averaging)	5	7	0		1~5	0		0
			(7, 5) subsampling = 1/6	○ (vertical digital binning averaging)	7	5	0		1~5	0		0
			(7, 9) subsampling = 1/8	○ (vertical digital binning averaging)	7	9	0		1~7	0		0
				○ (vertical digital +analog binning averaging)			1		2~6	0		1
			(9, 7) subsampling = 1/8	○ (vertical digital binning averaging)	9	7	0		1~7	0		0
				○ (vertical digital +analog binning averaging)			1		2~6	0		1
			2/3	○ (vertical special binning averaging)	2	3	0		1	1		0

Note) ◆ The odd subsampling (including 1/6 V subsampling) does not support the vertical analog binning averaging.
Therefore, vertical digital binning averaging setting is recommended for binning setting.
◆ VMODEADDJMP setting range of vertical digital binning averaging: 1 or more
(V subsampling ratio -1)
VMODEADDJMP setting range during vertical digital binning averaging + vertical analog binning averaging: 2 or more (V subsampling ratio -2)
◆ The minimum setting value is 2 because it does not overlap the vertical analog binning averaged line.

List of pixel binning modes and settings in horizontal direction

Possible register settings of sub-sampling mode in horizontal direction for IMX132TQH5-C are shown as below.

Table 25. Horizontal direction sub-sampling mode

	Mode list			Register settings						
	Communication method	Subsampling ratio	Binning	x_evn_inc	x_odd_inc	HADDEN	HADCONFIG	X_SP_ELIMINATION	HADCOEF0-7	HADCOEF8
				0x0381[3:0]	0x0383[3:0]	0x30D5[0]	0x30D5[3]	0x30D5[5]	0x30D6[7:0]-0x30DD[7:0]	0x30DE[7:0]
Horizontal direction	I^2C	(1,1) subsampling = All pixcels		1	1	0	0	0	-	-
		(1,3) subsampling = 1/2		1	3	0	0	0	-	-
			○ (Horizontal binning averaging)			1	1	0	1 ※	2
		(3,1) subsampling = 1/2		3	1	0	0	0	-	-
			○ (Horizontal binning averaging)			1	1	0	1 ※	2
		(3,3) subsampling = 1/3		3	3	0	0	0	-	-
			○ (Horizontal binning averaging)			1	1	0	0	3
		(3,5) subsampling = 1/4		3	5	0	0	0	-	-
			○ (Horizontal binning averaging)			1	1	0	0	4
		(5,3) subsampling = 1/4		5	3	0	0	0	-	-
			○ (Horizontal binning averaging)			1	1	0	0	4
		2/3	○ (Horizontal special binning averaging)	2	3	1	0	1	-	-

Note) ◆ H (1,3) subsampling or H (3,1) subsampling register setting:
HADCOEF0 = 1d, HADCOEF1 = 1d, The other register (HADCOEF2-7) recommends a setup to 0d

Readout Start Position

Default readout position of IMX132TQH5-C starts from the lower left while PIN1 is placed at the upper left corner. Because the lens will invert the image both vertically and horizontally, the proper image can be archived when PIN1 is placed in the upper left corner.

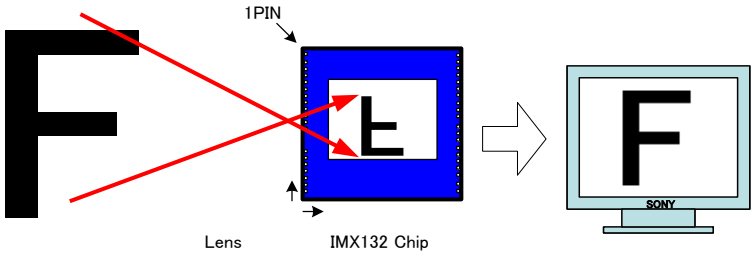


Fig 34. Readout start position

Vertical flip and horizontal mirror readout modes can be specified by the register below. And when readout start and end positions are matching the readout size, the same area is displayed when flipping/mirroring the image. When changing the readout direction, the color of first readout pixel (R/Gr/Gb/B) also changeswith it.

Table 26. Vertical flip and horizontal mirror

	address	Bit	name	description	notes
I^2C register	0x0101	[1]	image_ orientation	0 : V Nomal (Readout from bottom with Pin #1 at upper left corner) 1 : V Flip (Readout from top with Pin #1 at upper left corner)	
		[0]		0 : H Nomal (Readout from left with Pin #1 at upper left corner) 1 : H Mirror (Readout from right with Pin #1 at upper left corner)	

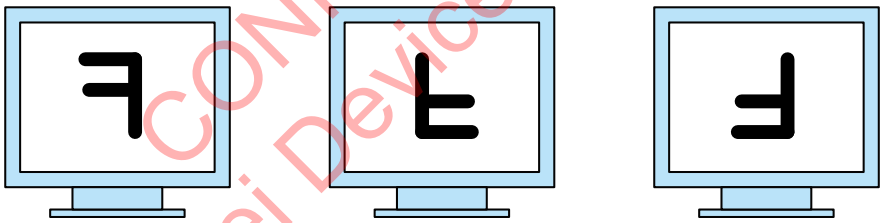


Fig 35. Read out image for each combination of flip and mirror

Output Data Timing Diagram

The IMX132TQH5-C output data alignment changes according to the sub sampling settings. The number of image lines (Embedded data lines+ OB+image pixels) changes according to the vertical sub sampling setting. If the number of vertical lines per frame does not change, the frame rate remains unchanged but the V blanking period length increases. If “the number of vertical lines per frame” changes, the “frame rate” also changes.

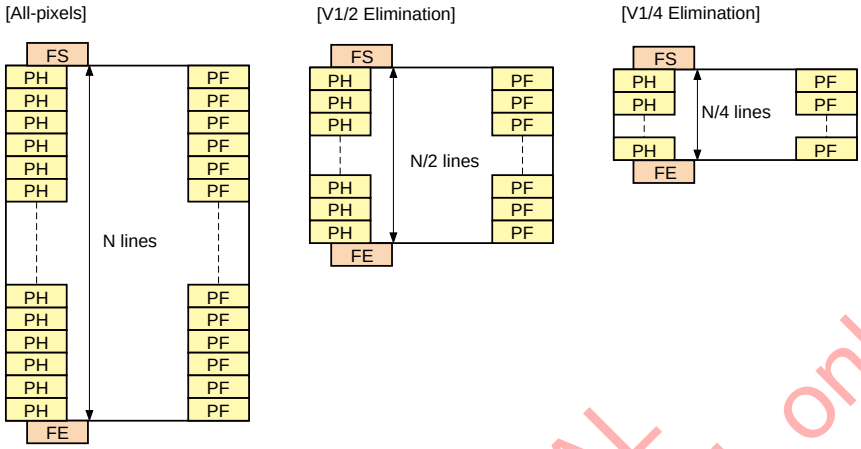


Fig 36. Vertical sub-sampling mode and number of image lines

When sub-sampling is set in the horizontal direction, the output data rate changes.
As data is processed in parallel line-by-line, time to output one line doesn't change regardless of applying horizontal sub-sampling or not. Therefore, time for one byte data output is extended when applying horizontal sub-sampling so that time for transmitting one line is kept unchanged.

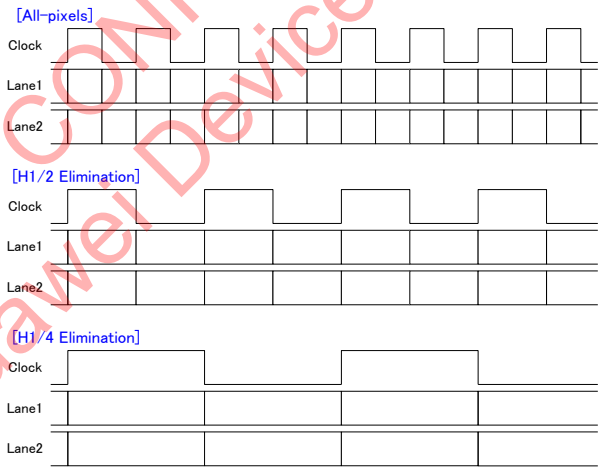


Fig 37. Horizontal sub-sampling mode and output data rate

Frame Rate Calculation Formula

The frame rate of the output image of IMX132TQH5-C can be calculated by the formula below.

Frame Rate[frame/s] = CK_PIXEL / Total number of output data

Where, CK_PIXEL is the internal image processing clock,

CK_PIXEL
= PLCK (PLLoutput clock frequency) × (Output lane number) / (output word length per pixel)
= (EXTCLK frequency ×PreDivider ratio setting ×PLL multiplier setting ×Post Divider ratio setting× Output lane number) / CCP2_data_format setting

Total number of output data
= (total line number per one frame × total pixel number per one line)
= frame_length_lines × line_length_pck

And duration of one line; Tline is calculated as below

T_{line} = line_length_pck / (2×LogicClock) …(Formula 1)

Table 27. Registers to calculate frame rate

	address	Bit	name	description	notes
I^2C register	0x0305	[7:0]	PREPLLCK_DIV	PreDividers setting	1, 1/2, 1/4, 1/8
	0x0307	[7:0]	PLL_MPY	PLLmultiplication setting	8 to 183 (dec)
	0x30A4	[1:0]	RGPLTD	PostDividersetting	1, 1/2, 1/4
	0x0113	[7:0]	CCP2_data_format	output word length per pixel	8, 10 (dec)
	0x0340	[7:0]	frame_length_lines	total line number per one frame	
	0x0341	[7:0]			
	0x0342	[7:0]	line_length_pck	total pixel clock number per one line	
	0x0343	[7:0]			

Electronic shutter and integration time settings

Registers related to Integration time (electronic shuttuer setting

The integration time setting registers are shown below. The set ting value of coarse_integration_time value indicates the number of lines for the integration time. The duration of one line is decided by number of Logic Clock per line multiply by 2 and designated by line_length_pck register. It can be converted into time (sec) by formular (*) in previous page.
The maximum integration time value is obtained by subtracting “five” from the number of lines per frame (set by frame_length_lines) including the blanking period.

Table 28. integration time setting register

	address	Bit	name	description	notes
I^2C register	0x304A	[0]	SMD	0:Rolling shutter mode (normal mode) 1:Global shutter mode (with mechanical shutter)	
	0x0202 0x0203	[7:0] [7:0]	coarse_integration_time	Integration time (unit; line) 0x0202 = coarse_integration_time[15:8] 0x0203 = coarse_integration_time[7:0]	1 to (frame_length_lines- 5)

Integration time calculation

The integration time (T_{SH}) can be obtained from the following relational equation. Define duration of one line as Tline (Formula 1 Reference) ,

$$T_{SH} = T_{line} \times (coarse\_integration\_time+0.160)$$

In other words, the minimum storage time is “Tline ×1.160”. This relationship stands up regardless of the operating mode (sub sampling, etc) except vertical digital addition average mode.

In vertical digital addition average mode the integration time (T_{SH}) can be obtained from the following equation.

$$T_{SH} = T_{line} \times (coarse\_integration\_time+0.095)$$

Alike above, the minimum integration time is “Tline × 1.095”.
Example settings and storage times are shown below.

Table 29. Integration time setting

	Total line number	frame_length_lines [15:0]	coarse_integration_time [15:0]	Integration time (H stands for the duration of one line)	
	dec	dec	dec	Full size/Sub sampling mode	vertical digital addition average mode
Regular frame rate	2400	2400	1	1.160H	1.095H
			2	2.160H	2.095H
			:	:	:
			N	(N+0.160) H	(N+0.095) H
			:	:	:
			2395	2395.160H	2395.095H
Low frame rate (long exposure time)	2401	2401	2396	2396.160H	2396.095H
	2402	2402	2397	2397.160H	2397.095H
	:	:	:	:	:
	M+5	M+5	M	(M+0.160) H	(M+0.095) H
	:	:	:	:	:
	65535	65535	65530	65530.160H	65530.095H

Optical Black level clamping

IMX132TQH5-C has the optical black level clamping function to make the black level stable against to the change of operating condition adaptively. The average value of black level is adjusted to the target level designated by register; BLKLEVEL.
In case of selecting RAW8 (non-compression) format, the clamping level becomes 1/4 following the output format internally.

Table 30. OB clamping target level setting register

	address	Bit	name	description	notes
I^2C register	0x3032	[7:0]	BLKLEVEL	OB clamping target level	Initial value 60 (0x3C)

Gain setting

IMX132TQH5-C can apply analog gain on photo-electron signal and digital gain on digital signal after ADC. According to the gain setting method in the SMIA specification, parameters of analog gain can be set by registers. Analog gain and digital gain can be set independently.

Analog gain setting

Analog gain is designated by the formula below according to SMIA specification.

$$Gain\_analog = (m0 \times X + c0) / (m1 \times X + c1)$$

The variables are specified in the table below.

Table 31. Variables of analog gain setting

	address	Bit	name	description	notes
I^2C register	0x008C 0x008D	[7:0] [7:0]	ana_gain_m0	m0: fixed to 0	Read Only static
	0x0090 0x0091	[7:0] [7:0]	ana_gain_m1	m1: fixed to -1	Read Only static
	0x008E 0x008F	[7:0] [7:0]	ana_gain_c0	c0: fixed to 256	Read Only static
	0x0092 0x0093	[7:0] [7:0]	ana_gain_c1	c1: fixed to 256	Read Only static
	0x0205	[7:0]	ana_gain_global	X: Analog gain setting value	0 to 240

As the result, analog gain is calculated by the formula below.

$$Gain\_analog = 256 / (256 - X)$$

The relationship between the setting values X of ana_gain_global and the gain is shown on the following table. The ana_gain_global value is normally set in the range from 0 to 224 [0 dB to 18 dB]. When AD input range is doubled for vertical analog binning-averaging mode, ana_gain_global value can be set from 0 to 240 [0 dB to 24 dB].

Table 32. Analog gain setting reference for “Setting method 2”

ana_gain_global	Gain [times]	Gain [dB]
0	1.00	0.00
1	1.00	0.03
2	1.01	0.07
3	1.01	0.10
4	1.02	0.14
5	1.02	0.17
6	1.02	0.21
7	1.03	0.24
8	1.03	0.28
9	1.04	0.31
10	1.04	0.35
11	1.04	0.38
12	1.05	0.42
13	1.05	0.45
14	1.06	0.49
15	1.06	0.52
16	1.07	0.56
17	1.07	0.60
18	1.08	0.63
19	1.08	0.67
20	1.08	0.71
21	1.09	0.74
22	1.09	0.78
23	1.10	0.82
24	1.10	0.86
25	1.11	0.89
26	1.11	0.93
27	1.12	0.97
28	1.12	1.01
29	1.13	1.04
30	1.13	1.08
31	1.14	1.12
32	1.14	1.16
33	1.15	1.20
34	1.15	1.24
35	1.16	1.28
36	1.16	1.32
37	1.17	1.36
38	1.17	1.40
39	1.18	1.44
40	1.19	1.48
41	1.19	1.52
42	1.20	1.56
43	1.20	1.60
44	1.21	1.64
45	1.21	1.68
46	1.22	1.72
47	1.22	1.76
48	1.23	1.80
49	1.24	1.85
50	1.24	1.89
51	1.25	1.93
52	1.25	1.97
53	1.26	2.01
54	1.27	2.06
55	1.27	2.10
56	1.28	2.14
57	1.29	2.19
58	1.29	2.23
59	1.30	2.28
60	1.31	2.32
61	1.31	2.36
62	1.32	2.41
63	1.33	2.45
64	1.33	2.50
65	1.34	2.54
66	1.35	2.59
67	1.35	2.64
68	1.36	2.68
69	1.37	2.73
70	1.38	2.77
71	1.38	2.82
72	1.39	2.87
73	1.40	2.92
74	1.41	2.96
75	1.41	3.01
76	1.42	3.06
77	1.43	3.11
78	1.44	3.16
79	1.45	3.21
80	1.45	3.25
81	1.46	3.30
82	1.47	3.35
83	1.48	3.40
84	1.49	3.45
85	1.50	3.50
86	1.51	3.56
87	1.51	3.61
88	1.52	3.66
89	1.53	3.71
90	1.54	3.76
91	1.55	3.82
92	1.56	3.87
93	1.57	3.92
94	1.58	3.97
95	1.59	4.03
96	1.60	4.08
97	1.61	4.14
98	1.62	4.19
99	1.63	4.25
100	1.64	4.30
101	1.65	4.36
102	1.66	4.41
103	1.67	4.47
104	1.68	4.53
105	1.70	4.59
106	1.71	4.64
107	1.72	4.70
108	1.73	4.76
109	1.74	4.82
110	1.75	4.88
111	1.77	4.94
112	1.78	5.00
113	1.79	5.06
114	1.80	5.12
115	1.82	5.18
116	1.83	5.24
117	1.84	5.30
118	1.86	5.37
119	1.87	5.43
120	1.88	5.49
121	1.90	5.56
122	1.91	5.62
123	1.92	5.69
124	1.94	5.75
125	1.95	5.82
126	1.97	5.89
127	1.98	5.95
128	2.00	6.02
129	2.02	6.09
130	2.03	6.16
131	2.05	6.23
132	2.06	6.30
133	2.08	6.37
134	2.10	6.44
135	2.12	6.51
136	2.13	6.58
137	2.15	6.65
138	2.17	6.73
139	2.19	6.80
140	2.21	6.88
141	2.23	6.95
142	2.25	7.03
143	2.27	7.10
144	2.29	7.18
145	2.31	7.26
146	2.33	7.34
147	2.35	7.42
148	2.37	7.50
149	2.39	7.58
150	2.42	7.66
151	2.44	7.74
152	2.46	7.82
153	2.49	7.91
154	2.51	7.99
155	2.53	8.08
156	2.56	8.16
157	2.59	8.25
158	2.61	8.34
159	2.64	8.43
160	2.67	8.52
161	2.69	8.61
162	2.72	8.70
163	2.75	8.80
164	2.78	8.89
165	2.81	8.98
166	2.84	9.08
167	2.88	9.18
168	2.91	9.28
169	2.94	9.37
170	2.98	9.47
171	3.01	9.58
172	3.05	9.68
173	3.08	9.78
174	3.12	9.89
175	3.16	10.00
176	3.20	10.10
177	3.24	10.21
178	3.28	10.32
179	3.32	10.43
180	3.37	10.55
181	3.41	10.66
182	3.46	10.78
183	3.51	10.90
184	3.56	11.02
185	3.61	11.14
186	3.66	11.26
187	3.71	11.39
188	3.76	11.51
189	3.82	11.64
190	3.88	11.77
191	3.94	11.91
192	4.00	12.04
193	4.06	12.18
194	4.13	12.32
195	4.20	12.46
196	4.27	12.60
197	4.34	12.75
198	4.41	12.90
199	4.49	13.05
200	4.57	13.20
201	4.65	13.36
202	4.74	13.52
203	4.83	13.68
204	4.92	13.84
205	5.02	14.01
206	5.12	14.19
207	5.22	14.36
208	5.33	14.54
209	5.45	14.72
210	5.57	14.91
211	5.69	15.10
212	5.82	15.30
213	5.95	15.50
214	6.10	15.70
215	6.24	15.91
216	6.40	16.12
217	6.56	16.34
218	6.74	16.57
219	6.92	16.80
220	7.11	17.04
221	7.31	17.28
222	7.53	17.54
223	7.76	17.79
224	8.00	18.06
225	8.26	18.34
226	8.53	18.62
227	8.83	18.92
228	9.14	19.22
229	9.48	19.54
230	9.85	19.87
231	10.24	20.21
232	10.67	20.56
233	11.13	20.93
234	11.64	21.32
235	12.19	21.72
236	12.80	22.14
237	13.47	22.59
238	14.22	23.06
239	15.06	23.56
240	16.00	24.08

Digital gain setting

Digital gain of IMX132TQH5-C can be set by color. The registers for digital gain setting are shown in the table below.

Table 33. Digital gain setting

	address	Bit	name	description	notes
I²C register	0x020E	[7:0]	digital_gain_greenR[15:8]	MSB side digital gain code for Gr	range: 1 to 15
	0x020F	[7:0]	digital_gain_greenR[7:0]	LSB side digital gain code for Gr	range: 0 to 255
	0x0210	[7:0]	digital_gain_red[15:8]	MSB side digital gain code for R	range: 1 to 15
	0x0211	[7:0]	digital_gain_red[7:0]	LSB side digital gain code for R	range: 0 to 255
	0x0212	[7:0]	digital_gain_blue[15:8]	MSB side digital gain code for B	range: 1 to 15
	0x0213	[7:0]	digital_gain_blue[7:0]	LSB side digital gain code for B	range: 0 to 255
	0x0214	[7:0]	digital_gain_greenB[15:8]	MSB side digital gain code for Gb	range: 1 to 15
	0x0215	[7:0]	digital_gain_greenB[7:0]	LSB side digital gain code for Gb	range: 0 to 255

Each register is comprised of 2 bytes with the upper byte[15:8] setting the integer portion and the lower byte[7:0] setting the decimal portion of the gain. The gain for each color is obtained by the following formula.

$$Gain\_digital = upper\_byte + lower\_byte/256$$

The unit of Gain_digital is [times]. The upper byte can be set to a value ranging from 1 to 15 and the lower byte to a value ranging from 0 to 255. Therefore, the range of digital gain is shown as follows.

$$1 + 0/256 \text{ [times]} (0 \text{ dB}) \leq Gain\_digital \leq 15 + 255/256 \text{ [times]} (24 \text{ dB})$$

When representing the gain by log-linear scale [dB], lower gain takes coarse step and high gain takes fine step for the incrementation of the register value. The table below indicates the register values in 0.1 dB step for reference.

Table 34. Digital gain setting reference

Upper byte		Lower byte		Gain [times]	Gain [dB]
dec	hex	dec	hex		
1	1	0	0	1.00	0.00
1	1	3	3	1.01	0.10
1	1	6	6	1.02	0.20
1	1	9	9	1.04	0.30
1	1	12	C	1.05	0.40
1	1	15	F	1.06	0.49
1	1	18	12	1.07	0.59
1	1	21	15	1.08	0.68
1	1	25	19	1.10	0.81
1	1	28	1C	1.11	0.90
1	1	31	1F	1.12	0.99
1	1	35	23	1.14	1.11
1	1	38	26	1.15	1.20
1	1	41	29	1.16	1.29
1	1	45	2D	1.18	1.41
1	1	48	30	1.19	1.49
1	1	52	34	1.20	1.61
1	1	55	37	1.21	1.69
1	1	59	3B	1.23	1.80
1	1	63	3F	1.25	1.91
1	1	66	42	1.26	1.99
1	1	70	46	1.27	2.10
1	1	74	4A	1.29	2.21
1	1	78	4E	1.30	2.31
1	1	81	51	1.32	2.39
1	1	85	55	1.33	2.49
1	1	89	59	1.35	2.59
1	1	93	5D	1.36	2.69
1	1	97	61	1.38	2.79
1	1	101	65	1.39	2.89
1	1	106	6A	1.41	3.01
1	1	110	6E	1.43	3.10
1	1	114	72	1.45	3.20
1	1	118	76	1.46	3.29
1	1	123	7B	1.48	3.41
1	1	127	7F	1.50	3.50
1	1	131	83	1.51	3.59
1	1	136	88	1.53	3.70
1	1	140	8C	1.55	3.79
1	1	145	91	1.57	3.90
1	1	150	96	1.59	4.01
1	1	154	9A	1.60	4.09
1	1	159	9F	1.62	4.20
1	1	164	A4	1.64	4.30
1	1	169	A9	1.66	4.40
1	1	174	AE	1.68	4.50
1	1	179	B3	1.70	4.60
1	1	184	B8	1.72	4.70
1	1	189	BD	1.74	4.80
1	1	194	C2	1.76	4.90
1	1	199	C7	1.78	5.00
1	1	205	CD	1.80	5.11
1	1	210	D2	1.82	5.20
1	1	215	D7	1.84	5.30
1	1	221	DD	1.86	5.41
1	1	226	E2	1.88	5.50
1	1	232	E8	1.91	5.60
1	1	237	ED	1.93	5.69
1	1	243	F3	1.95	5.80
1	1	249	F9	1.97	5.90
1	1	255	FF	2.00	6.00
2	2	5	5	2.02	6.11
2	2	11	B	2.04	6.21
2	2	17	11	2.07	6.30
2	2	23	17	2.09	6.40
2	2	29	1D	2.11	6.50
2	2	35	23	2.14	6.59
2	2	42	2A	2.16	6.71
2	2	48	30	2.19	6.80
2	2	55	37	2.21	6.91
2	2	61	3D	2.24	7.00
2	2	68	44	2.27	7.10
2	2	74	4A	2.29	7.19
2	2	81	51	2.32	7.30
2	2	88	58	2.34	7.40
2	2	95	5F	2.37	7.50
2	2	102	66	2.40	7.60
2	2	109	6D	2.43	7.70
2	2	116	74	2.45	7.79
2	2	124	7C	2.48	7.90
2	2	131	83	2.51	8.00
2	2	138	8A	2.54	8.09
2	2	146	92	2.57	8.20
2	2	154	9A	2.60	8.30
2	2	161	A1	2.63	8.40
2	2	169	A9	2.66	8.50
2	2	177	B1	2.69	8.60
2	2	185	B9	2.72	8.70
2	2	193	C1	2.75	8.80
2	2	201	C9	2.79	8.90
2	2	210	D2	2.82	9.01
2	2	218	DA	2.85	9.10
2	2	226	E2	2.88	9.20
2	2	235	EB	2.92	9.30
2	2	244	F4	2.95	9.41
2	2	252	FC	2.98	9.50
3	3	5	5	3.02	9.60
3	3	14	E	3.05	9.70
3	3	23	17	3.09	9.80
3	3	32	20	3.13	9.90
3	3	42	2A	3.16	10.00
3	3	51	33	3.20	10.10
3	3	60	3C	3.23	10.20
3	3	70	46	3.27	10.30
3	3	80	50	3.31	10.40
3	3	90	5A	3.35	10.50
3	3	99	63	3.39	10.60
3	3	109	6D	3.43	10.70
3	3	120	78	3.47	10.80
3	3	130	82	3.51	10.90
3	3	140	8C	3.55	11.00
3	3	151	97	3.59	11.10
3	3	161	A1	3.63	11.20
3	3	172	AC	3.67	11.30
3	3	183	B7	3.71	11.40
3	3	194	C2	3.76	11.50
3	3	205	CD	3.80	11.60
3	3	217	D9	3.85	11.70
3	3	228	E4	3.89	11.80
3	3	239	EF	3.93	11.90
3	3	251	FB	3.98	12.00
4	4	7	7	4.03	12.10
4	4	19	13	4.07	12.20
4	4	31	1F	4.12	12.30
4	4	43	2B	4.17	12.40
4	4	56	38	4.22	12.50
4	4	68	44	4.27	12.60
4	4	81	51	4.32	12.70
4	4	93	5D	4.36	12.80
4	4	106	6A	4.41	12.90
4	4	120	78	4.47	13.00
4	4	133	85	4.52	13.10
4	4	146	92	4.57	13.20
4	4	160	A0	4.63	13.30
4	4	173	AD	4.68	13.40
4	4	187	BB	4.73	13.50
4	4	201	C9	4.79	13.60
4	4	215	D7	4.84	13.70
4	4	230	E6	4.90	13.80
4	4	244	F4	4.95	13.90
5	5	3	3	5.01	14.00
5	5	18	12	5.07	14.10
5	5	33	21	5.13	14.20
5	5	48	30	5.19	14.30
5	5	64	40	5.25	14.40
5	5	79	4F	5.31	14.50
5	5	95	5F	5.37	14.60
5	5	111	6F	5.43	14.70
5	5	127	7F	5.50	14.80
5	5	143	8F	5.56	14.90
5	5	160	A0	5.63	15.00
5	5	176	B0	5.69	15.10
5	5	193	C1	5.75	15.20
5	5	210	D2	5.82	15.30
5	5	227	E3	5.89	15.40
5	5	245	F5	5.96	15.50
6	6	7	7	6.03	15.60
6	6	24	18	6.09	15.70
6	6	42	2A	6.16	15.80
6	6	61	3D	6.24	15.90
6	6	79	4F	6.31	16.00
6	6	98	62	6.38	16.10
6	6	117	75	6.46	16.20
6	6	136	88	6.53	16.30
6	6	155	9B	6.61	16.40
6	6	175	AF	6.68	16.50
6	6	195	C3	6.76	16.60
6	6	215	D7	6.84	16.70
6	6	235	EB	6.92	16.80
7	7	0	0	7.00	16.90
7	7	20	14	7.08	17.00
7	7	41	29	7.16	17.10
7	7	63	3F	7.25	17.20
7	7	84	54	7.33	17.30
7	7	106	6A	7.41	17.40
7	7	128	80	7.50	17.50
7	7	150	96	7.59	17.60
7	7	172	AC	7.67	17.70
7	7	195	C3	7.76	17.80
7	7	218	DA	7.85	17.90
7	7	241	F1	7.94	18.00
8	8	9	9	8.04	18.10
8	8	33	21	8.13	18.20
8	8	57	39	8.22	18.30
8	8	81	51	8.32	18.40
8	8	106	6A	8.41	18.50
8	8	131	83	8.51	18.60
8	8	156	9C	8.61	18.70
8	8	182	B6	8.71	18.80
8	8	207	CF	8.81	18.90
8	8	234	EA	8.91	19.00
9	9	4	4	9.02	19.10
9	9	31	1F	9.12	19.20
9	9	58	3A	9.23	19.30
9	9	85	55	9.33	19.40
9	9	113	71	9.44	19.50
9	9	141	8D	9.55	19.60
9	9	169	A9	9.66	19.70
9	9	198	C6	9.77	19.80
9	9	227	E3	9.89	19.90
10	A	0	0	10.00	20.00
10	A	30	1E	10.12	20.10
10	A	60	3C	10.23	20.20
10	A	90	5A	10.35	20.30
10	A	121	79	10.47	20.40
10	A	152	98	10.59	20.50
10	A	183	B7	10.71	20.60
10	A	215	D7	10.84	20.70
10	A	247	F7	10.96	20.80
11	B	23	17	11.09	20.90
11	B	56	38	11.22	21.00
11	B	90	5A	11.35	21.10
11	B	123	7B	11.48	21.20
11	B	157	9D	11.61	21.30
11	B	192	C0	11.75	21.40
11	B	227	E3	11.89	21.50
12	C	6	6	12.02	21.60
12	C	41	29	12.16	21.70
12	C	77	4D	12.30	21.80
12	C	114	72	12.45	21.90
12	C	151	97	12.59	22.00
12	C	188	BC	12.73	22.10
12	C	226	E2	12.88	22.20
13	D	8	8	13.03	22.30
13	D	47	2F	13.18	22.40
13	D	86	56	13.34	22.50
13	D	125	7D	13.49	22.60
13	D	165	A5	13.64	22.70
13	D	206	CE	13.80	22.80
13	D	247	F7	13.96	22.90
14	E	32	20	14.13	23.00
14	E	74	4A	14.29	23.10
14	E	116	74	14.45	23.20
14	E	159	9F	14.62	23.30
14	E	203	CB	14.79	23.40
14	E	246	F6	14.96	23.50
15	F	35	23	15.14	23.60
15	F	80	50	15.31	23.70
15	F	125	7D	15.49	23.80
15	F	171	AB	15.67	23.90
15	F	217	D9	15.85	24.00

Miscellaneous functions

Test signal output

IMX132TQH5-C can output test pattern of SMIA specification by build-in pattern generator.

Types of test pattern

IMX132TQH5-C has the function to output fixed video signal from build-in test pattern generator by setting related registers.
While related register must be set to output test pattern, there is no restriction on the sequence for setting the registers. The required test pattern can be output by setting the related registers when the IMX132TQH5-C is in image shooting operation.

Table 35. Test pattern related registers and description

	address	Bit	name	description	notes
I^2C register	0x3032	[7:0]	BLKLEVEL	Black level for OB level clamping target	initial value = 60 (dec)
	0x3282	[0]	DPUOFF	Skipping all the signal processing 0 : Normal operation 1 : Skipping signal processing	
	0x0600	[7:0]	test_pattern_mode [15:8]	Pattern generator mode setting 0x0000: Disables the pattern generator. 0x0001: Solid Color 0x0002: 100 % Color Bar 0x0003: Fade to grey Color Bar 0x0004: PN9 0x0100: FIX pattern 1 (fixed pattern 1) (0x3FF*4 → 0x000*4) 0x0101: FIX pattern 2 (fixed pattern 2) (0x3FF → 0x180 → 0x100 → 0x060) 0x0102: FIX pattern 3 (setting pattern 1) (td_r*4 → td_gr*4 → td_b*4 → td_gb*4) 0x0103: FIX pattern 4 (setting pattern 2) (td_r→td_gr→td_r→td_gr→td_b→ td_gb→td_b→td_gb) 0x0104: FIX pattern 5 (setting pattern 3) (td_r*2 → td_gr*2 → td_b*2 → td_gb*2) 0x0105: FIX pattern 6 (setting pattern 4) (td_r → td_gr → td_b → td_gb) Other than above: Setting prohibited	
	0x6001	[7:0]	test_pattern_mode [7:0]		
	0x0602	[1:0]	test_data_red[9:8]	R data value for Solid Color mode	
	0x0603	[7:0]	test_data_red[7:0]		
	0x0604	[1:0]	test_data_greenR[9:8]	Gr data value for Solid Color mode	
	0x0605	[7:0]	test_data_greenR[7:0]		
	0x0606	[1:0]	test_data_blue[9:8]	B data value for Solid Color mode	
	0x0607	[7:0]	test_data_blue [7:0]		
	0x0608	[1:0]	test_data_greenB[9:8]	Gb data value for Solid Color mode	
	0x0609	[7:0]	test_data_greenB[7:0]		

While test pattern can be output in Sub-sampling mode, the output might be different from the set pattern. In binning, when DPUOFF = 0, the output is after applying signal processing. Therefore, to output the accurate value which are set to the registers on test pattern, please set DPUOFF = 1 and select full-pixel mode for both vertical and horizontal directions.
If black level clamping is not required, please set register BLKLEVEL = 0.

Please refer to Appendix for details on test pattern.

Image signal interface

MIPI transmitter

IMX132TQH5-C outputs image signal by CSI2 high speed serial interface consisted of one pair of clock line and two pairs of data line. Please refer to MIPI Alliance Standard for Camera Serial Interface2 (CSI-2) version 1.00 and MIPI Alliance Specification for D-PHY version 0.90.00 for details. Because signal is transmitted by differential pair, resistance (generally 100 Ω) between differential pair near the receiver side is required. Otherwise, please select receiver with build-in resistance between differential pair. Different delay time of differential pairs may reduce the input timing margin of ISP device, which leads to malfunction. Therefore, delay time within and among differential pairs must be as similar as possible in layout.

Supplemental function for camera feature

Flash light control sequence

IMX132TQH5-C can internally generate the control pulse assuming to trigger the flash light emission and output from the external pins. There are 2 modes to control Xenon flash light and LED light.
The flash light trigger pulse width and output timming can be controlled by registers shown in table 38. Flush control pulse can be output both from XVS pins. By setting register: XVSSEL[1:0] = 2'h3, it is output from XVS pis.
Detail control sequence is described in APPENDIX.

Global reset and mechanical shutter control pulse

IMX132TQH5-C has the simultaneous reset function of integration start timing for all lines, called "global reset", assuming the mechanical shutter to determine the exposure time. This function is enabled by control registers shown in table 38. Global reset timing pulse can be output both from XVS pins. By setting register: XVSSEL[1:0] = 2'h2, it is output from XVS pis. It is also possible outputting flash control pulse from XVS pin at the same time with global reset timing pulse for simultaneous use of global reset and speed light.
Detail control sequence is described in APPENDIX.

Table 36. Flash pulse and global reset operation control registers

	address	Bit	name	description	notes
I^2C registe	0x304A	[7]	FLASH_SMDMODE	Enable interlocked flash control pulse to SMD 0: disable interlocking with global reset operation (default) 1: enable interlocking with global reset operation	
		[6]	PRE_ FLASH_EN	Enable Pre Flash Control Pulse generation 0: disable pre flash control pulse (default) 1: enable pre flash control pulse	
		[5]	LED_FLASH_EN	Enable LED Flash Control Pulse generation 0: disable LED flash control pulse (default) 1: enable LED flash control pulse	
		[4]	FLASH_EN	Enable Flash Control Pulse generation 0: disable flash control pulse (default) 1: enable flash control pulse	
		[0]	SMD	Select Shutter mode 0: rolling shutter mode 1: global reset mode	
	0x3240	[3:2]	XVSSEL	Select output signal to XVS pin 0: fixed 0 value (default) 1: for test (inhibited setting) 2: mechanical shutter control pulse 3: flash control pulse	
	0x307B	[7:4]	GRRLVL	Global reset applied timing 0000: next frame 0001: 2 frames later : 0111: 8 frames later 1xxx: 9 frames later	
		[3]	FLASH_STR	Rise timing of Flash Control Pulse 0: Top of next frame of communication frame (default) 1: The end of effective image of communication frame	
		[2]	FLASH_REP	Repeat control of Flash Control Pulse 0: output control pulse for one frame only after communiocation frame (default) 1: output every frame	
		[1:0]	FLASH_DLY	Controls delay of the flash control pulse generation timing. 0: Generates after 1 frame of communication frame. 1: Generates after 2 frames of communication frame. 2: Generates after 3 frames of communication frame. 3: Generates after 4 frames of communication frame.	
	0x307C	[2:0]	FLASH_PL_STEP_GAIN	Magnifying factor of Flash Control Pulse width (gain)	
	0x307D	[5:0]	FLASH_PL_STEP	Flash Control Pulse width (step)	

Operation

Power on Reset

IMX132TQH5-C has the built in “Power On Reset” function.
IMX132TQH5-C automatically initializes the internal circuit by itself when XCLR (XSHUTDOWN) pin is open and the power supplies are brought up. In binning, if XCLR (XSHUTDOWN) pin is set to low and the power supplies are bring up. The sensor will skip executing the “Power On Reset” function.

Power-on sequense

Start up sequence with 2-wire serial communication

Please follow the power supply start up sequence below.

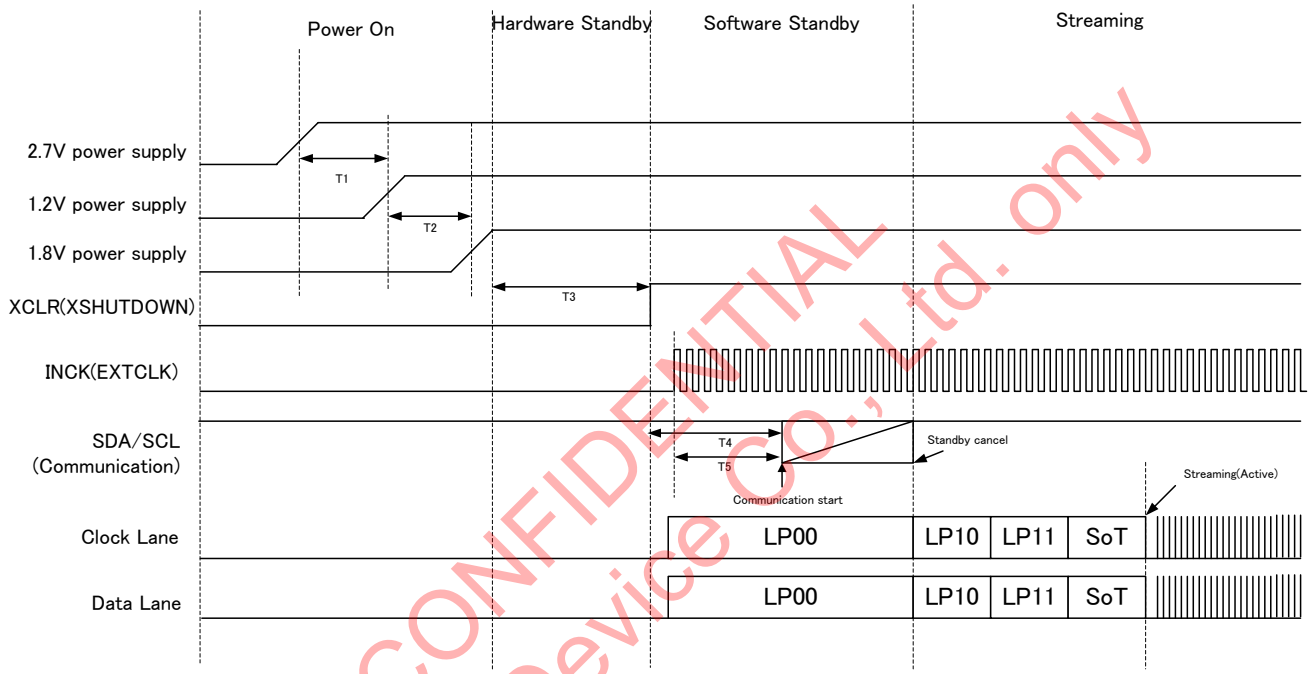


Fig 38. Start up sequence with 2-wire serial communication (external reset)

Table 37. Start up sequence timing constraints (2-wire serial communication mode with external reset)

Item	Label	Min	Max	Unit
2.7 V power supply rising → 1.2 V power supply rising	T1	Rise in any order		—
1.2 V power supply rising → 1.8 V power supply rising	T2	Rise in any order		—
All power supply UP (90 %) → XCLR (XSHUTDOWN) rising	T3	500		ns
XCLR (XSHUTDOWN) rising → Communication start	T4	300		µs
INCK (EXTCLK) applied → Communication start	T5	76		EXTCLK cycle

Note) ◆ EXTCLK can rise before XSHUTDOWN is set to High.
◆ XSHUTDOWN needs to be Low until all power supplies complete power-on.

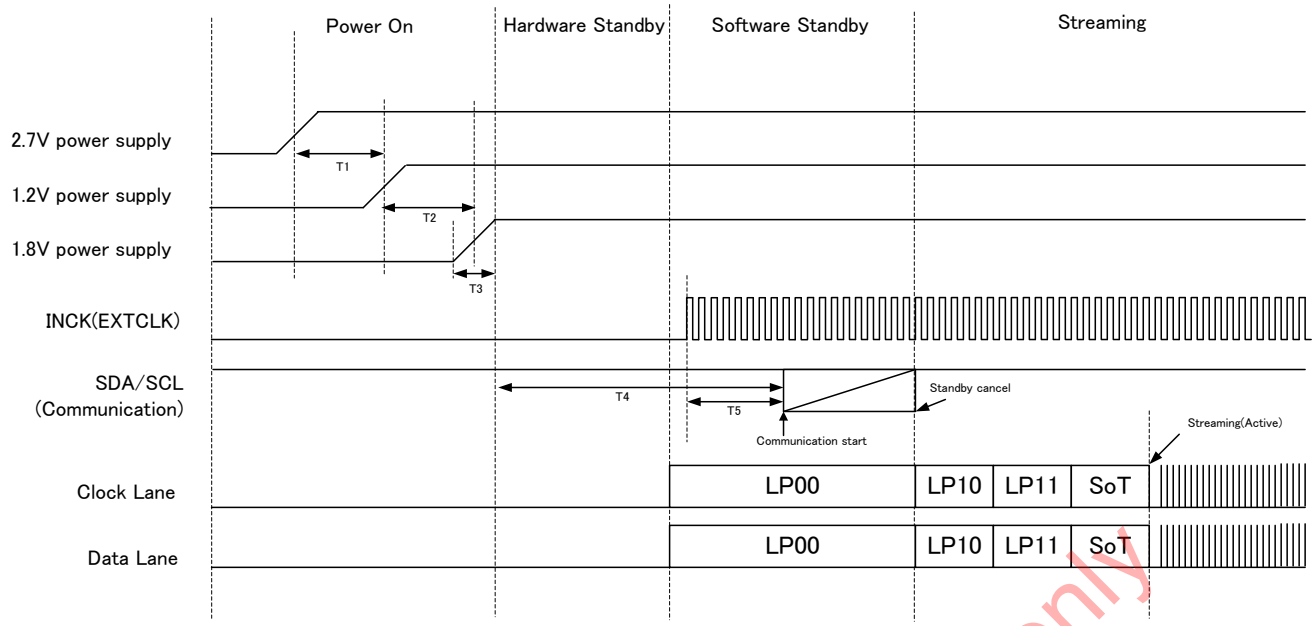


Fig 39. Start up sequence with 2-wire serial communication (power on reset)

Table 38. Start up sequence timing constraints (2-wire serial communication mode with power on reset)

Item	Label	Min	Max	Unit
2.7 V power supply rising → 1.2 V power supply rising	T1	Rise in any order		—
1.2 V power supply rising → 1.8 V power supply rising	T2	Rise in any order		—
Rising time of the lastest power supply (10 %→90 %)	T3		1	ms
All power supply rising (90 %)→Communication start	T4	300		µs
INCK (EXTCLK) applied → Communication start	T5	76		EXTCLK cycle

Start streaming sequence with 2-wire serial communication

IMX132TQH5-C requires the command sequence below to output image data.

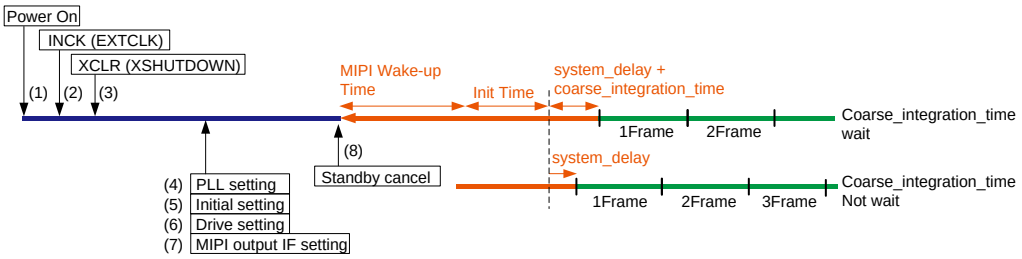


Fig 40. Start streaming sequence with 2-wire serial communication (external reset)

Table 39. Initialization sequence with XCLR

(1) to (3)	Refer power up sequence timing diagram
(4)	Set PLL parameters
(5)	Basic setting (operation-critical setting)
(6)	Set Readout mode (start/end position, size, sub-sampling mode, integration time, and gain)
(7)	Set MIPI interface parameters
(8)	Start streaming with 0x0100 (mode_select = 1)
	After “Wake Up Time” + “Init Time”, 1st frame starts and images come out

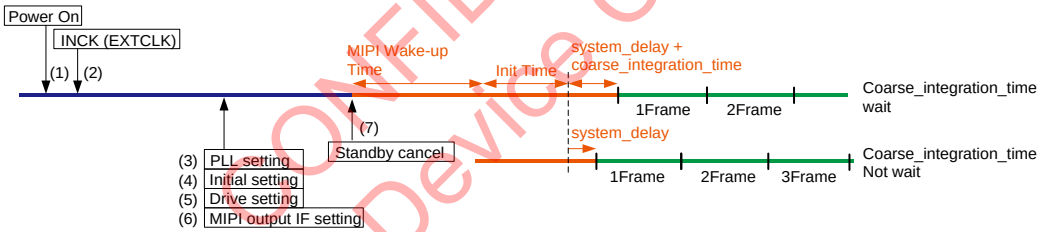


Fig 41. Start streaming sequence with 2-wire serial communication (Power On Reset)

Table 40. Initialization sequence with power on reset

(1) to (2)	Refer power up sequence timing diagram
(3)	Wait for longer than 300µs afte power on, set PLL parameters
(4)	Basic setting (operation-critical setting)
(5)	Set Readout mode (start/end position, size, sub-sampling mode, integration time, and gain)
(6)	Set MIPI interface parameters
(7)	Start streaming with 0x0100 (mode_select = 1)
	After “Wake Up Time” + “Init Time”, 1st frame starts and images come out

Regular image output (required duration to make OB level stable)

After starting streaming, OB level clamping circuit operates with using the shooted images. It takes at least 2 frames to adjust the OB level and make the images stable. We recommend to use the images from third frame and after for recording.

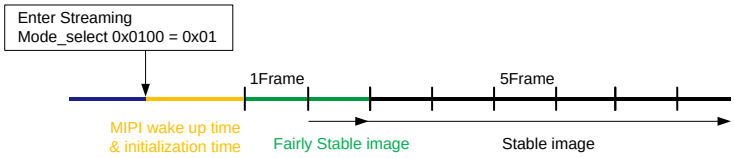


Fig 42. Regular image output

Waiting duration setting for PLLsettling time

When starting streaming, PLL starts operating. The internal control circuit of IMX132TQH5-C needs to wait for settling time of PLL. The waiting duration is designated by PLSTM register. Waiting duration calculation formula is shown as below.

Waiting duration for PLL settling time[μs] = ((PLSTATIM × 64) + 63) × (1 / EXTCLK frequency[MHz])

PLL settling time is 200 μs, then set the value to be longer than 200 μs to PLSTATIM register.
Examples for each EXTCLK frequency are shown in the table below.

Table 41. Example setting of waiting time for PLL settling time

EXTCLK frequency	PLSTATIM[7:0] (0x303C[7:0])	Waiting duration for PLLsettling gtime
MHz	dec	μs
27	84	201.444
24	75	202.625
18	56	202.611
6	18	202.500

Power-off sequence

Power off sequence with 2-wire serial communication

Please follow the power off sequence below.

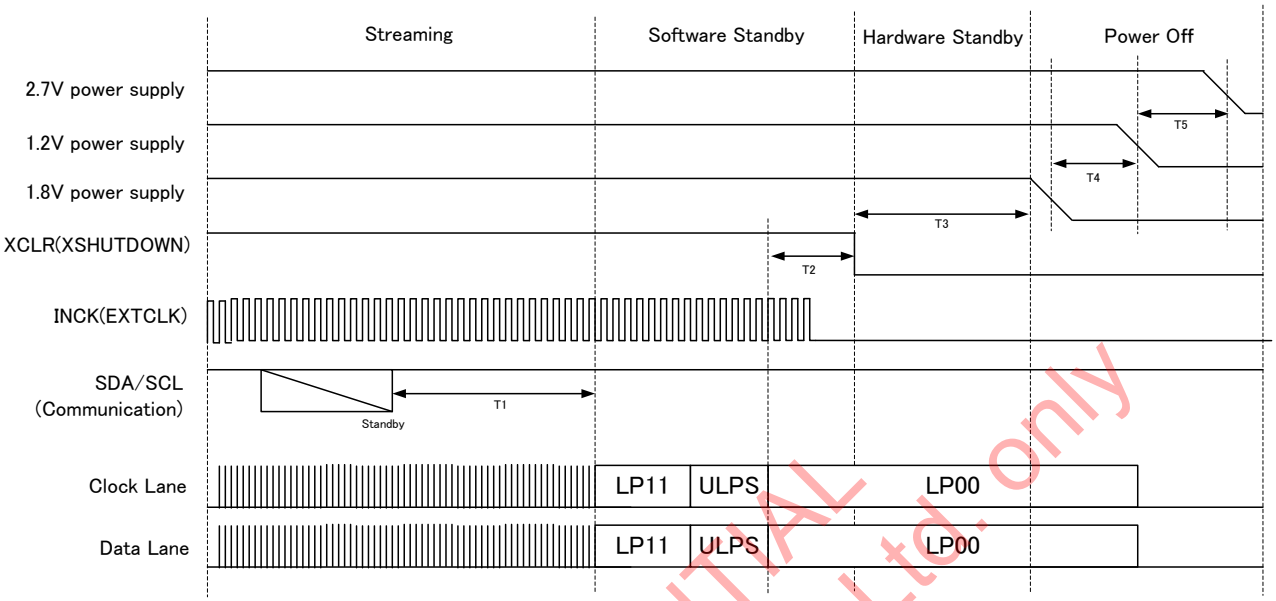


Fig 43. Power off sequence with 2-wire serial communication (external reset)

Table 42. Power off sequence timing constraints (2-wire serial communication mode with external reset)

Item	Label	Min	Max	Unit
Communication end→Software standby	T1	Until frame output		—
Frame output end→XCLR (XSHUTDOWN) falling Frame output end→INCK (EXTCLK) end	T2	128		EXTCLK cycle
XCLR (XSHUTDOWN) falling→First power supply down (90 %)	T3	500		ns
1.8 V power supply down→1.2 V power supply down	T4	Fall in any order		—
1.2 V power supply down→2.7 V power supply down	T5	Fall in any order		—

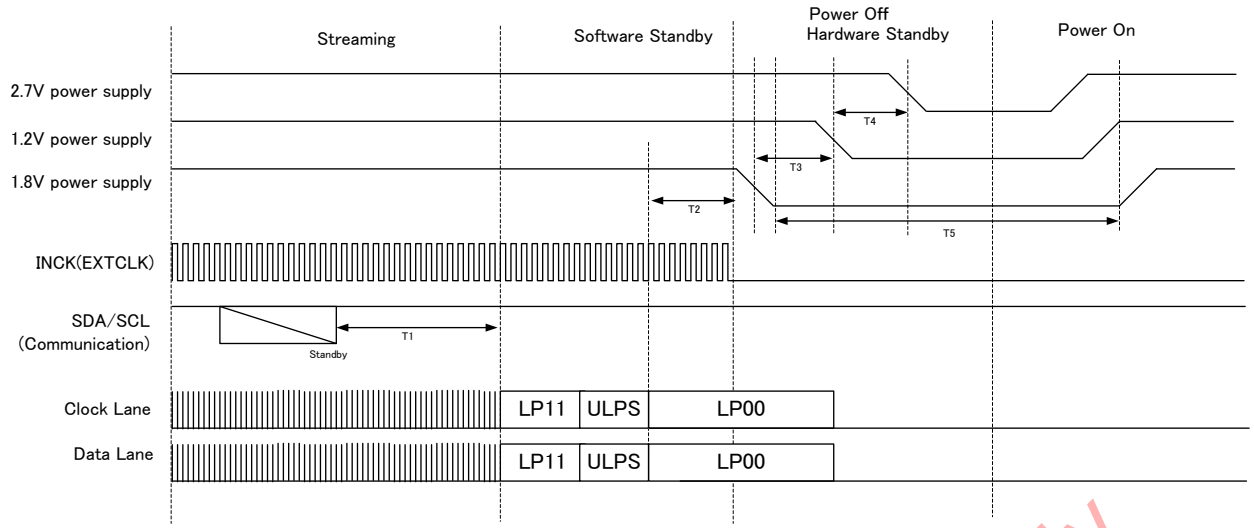


Fig 44. Power off sequence with 2-wire serial communication (power on reset)

Table 43. Power off sequence timing constraints (2-wire serial communication mode with power on reset)

Item	Label	Min	Max	Unit
Communication end→Software standby	T1	Until frame output		—
Frame output→First power supply down (90 %)	T2	500		ns
1.8 V power supply down→1.2 V power supply down	T3	Fall in any order		—
1.2 V power supply down→2.7 V power supply down	T4	Fall in any order		—
First power supply Down (10 %)→Last power supply Up (10 %)	T5	400		μs

T1 (Communication end→Software standby constraint time) in Power off sequence is determined according to the timing to issue “standby”command with 2-wire serial copmmunication.

(1) In case of software standby command is issued in between “FS” and “FE”, IMX132TQH5-C completes outputting the image data and transits to standby state.

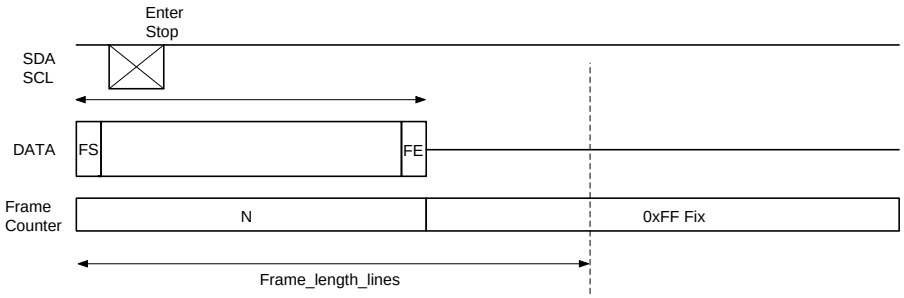


Fig 45. Software standby transition pattern 1

(2) In case of software standby command is issued within “Frame Blanking” period, IMX132TQH5-C immediately transits to software standby state.

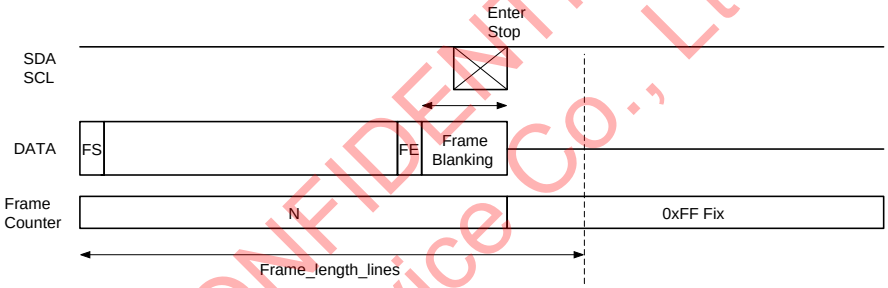


Fig 46. Software standby transition pattern 2

Register Map

Description of Register

Registers with the description “Reserved”,” ManufactureResister” and bit assignment without description are inhibited rewiting.
Registers which have the internal update iming are indicated with “○” description in the “update Timming” columns.
Registers output their address and values on “Embedded data lines” are indicated with “○” description in the “Embd DL” columns.

NOTE) The register required for optimization of operation is contained in the register of a ManufactureResister Please ask about the details of a required register.

2-wire serial communication register map (Configuration register 0x0000 to 0x0FFF)

Address (hex)	Bit	Register Name	initial values (hex)	RW	Description	Update Timing	Embd DL
0x0000	[7:0]	model_id[15:8]	01	RO static	Model No. specified to sensor		○
0x0001	[7:0]	model_id[7:0]	32	RO static			
0x0002	[7:0]	revision_number	—	RO static	Rev. No of silicon (+1 when revised)		○
0x0003	[7:0]	manufacturer_id	0B	RO static	ID specified to manufacturer		○
0x0004	[7:0]	smia_version	0A	RO static	Supported Version of SMIA standard		○
0x0005	[7:0]	frame_count	FF	RO dynamic	Frame counter Value		○
0x0006	[7:0]	pixel_order	01	RO dynamic	Bayer array specification 0h : Horizontal mirror 1h : Normal 2h : Horizontal mirror/Vertical flip 3h : Vertical flip		○
0x0007	[7:0]	Reserved	—	—	Rewrite inhibited	—	—
0x0008	[7:0]	data_pedestal[15:8]	00	RO dynamic	Black level output value of sensor		○
0x0009	[7:0]	data_pedestal[7:0]	40	RO dynamic			
0x000A - 0x003F	[7:0]	Reserved	—	—	Rewrite inhibited	—	—
0x0040	[7:0]	frame_format_model_type	01	RO static	2 byte format = 1		○
0x0041	[7:0]	frame_format_model_subtype	15	RO static	Number of frame_format_descriptor_s* upper 4bits = col side, lower 4bits = raw side		○
0x0042	[7:0]	frame_format_descriptor_0[15:8]	57	RO dynamic	[15:12] = 5 (Visible Pixel Data *Horizontal direction)		○
0x0043	[7:0]	frame_format_descriptor_0[7:0]	B8	RO dynamic	[11: 0] = The number of pixels (x_output_size)		
0x0044	[7:0]	frame_format_descriptor_1[15:8]	10	RO dynamic	[15:12] = 1 (Embedded Data)		○
0x0045	[7:0]	frame_format_descriptor_1[7:0]	02	RO dynamic	[11: 0] = The number of lines		
0x0046	[7:0]	frame_format_descriptor_2[15:8]	20	RO dynamic	[15:12] = 2 (Dummy Pixel Data)		○
0x0047	[7:0]	frame_format_descriptor_2[7:0]	04	RO dynamic	[11: 0] = The number of lines		
0x0048	[7:0]	frame_format_descriptor_3[15:8]	40	RO dynamic	[15:12] = 4 (Dark Pixel Data)		○
0x0049	[7:0]	frame_format_descriptor_3[7:0]	0E	RO dynamic	[11: 0] = The number of lines		
0x004A	[7:0]	frame_format_descriptor_4[15:8]	20	RO dynamic	[15:12] = 2 (Dummy Pixel Data)		○
0x004B	[7:0]	frame_format_descriptor_4[7:0]	02	RO dynamic	[11: 0] = The number of lines		
0x004C	[7:0]	frame_format_descriptor_5[15:8]	54	RO dynamic	[15:12] = 5 (Visible Pixel Data *Vertical direction)		○
0x004D	[7:0]	frame_format_descriptor_5[7:0]	78	RO dynamic	[11: 0] = The number of lines (y_output_size)		
0x004E - 0x007F	[7:0]	Reserved	—	—	Rewrite inhibited	—	—
0x0080	—	analogue_gain_capabiltiy[15:8]	00	RO dynamic	Indicates state in Analog gain mode (not applicable to SIMA specification)		○
0x0081	[0]	analogue_gain_capabiltiy[7:0]	00	RO dynamic	0 : Global gain 1 : Separate Bayer Gains		
0x0082	[7:0]	Reserved	—	—	Rewrite inhibited	—	—
0x0083	[7:0]	Reserved	—	—	Rewrite inhibited	—	—
0x0084	[7:0]	analogue_gain_code_min[15:8]	00	RO static	Analog Gain code		○
0x0085	[7:0]	analogue_gain_code_min[7:0]	00	RO static	Min.		
0x0086	[7:0]	analogue_gain_code_max[15:8]	00	RO static	Analog Gain code		○
0x0087	[7:0]	analogue_gain_code_max[7:0]	E0	RO static	Max.		
0x0088	[7:0]	analogue_gain_code_step[15:8]	00	RO static	Analog gain code		○
0x0089	[7:0]	analogue_gain_code_step[7:0]	01	RO static	Step		
0x008A	[7:0]	analogue_gain_type[15:8]	00	RO static	Analog gain Type		○
0x008B	[7:0]	analogue_gain_type[7:0]	00	RO static	*Fixed to 0 in baseline SMIA		
0x008C	[7:0]	analogue_gain_m0[15:8]	00	RO static	Analog gain m0 constant		○
0x008D	[7:0]	analogue_gain_m0[7:0]	00	RO static	Gain = (m0 * X + c0) / (m1 * X + c1) = 256/ (256-X) *X = analogue_gain_code_global		
0x008E	[7:0]	analogue_gain_c0[15:8]	01	RO static	Analog gain c0 constant		○
0x008F	[7:0]	analogue_gain_c0[7:0]	00	RO static	Gain = (m0 * X + c0) / (m1 * X + c1) = 256/ (256-X) *X = analogue_gain_code_global		
0x0090	[7:0]	analogue_gain_m1[15:8]	FF	RO static	Analog gain m1 constant		○
0x0091	[7:0]	analogue_gain_m1[7:0]	FF	RO static	Gain = (m0 * X + c0) / (m1 * X + c1) = 256/ (256-X) *X = analogue_gain_code_global		
0x0092	[7:0]	analogue_gain_c1[15:8]	01	RO static	Analog gain c1 constant		○
0x0093	[7:0]	analogue_gain_c1[7:0]	00	RO static	Gain = (m0 * X + c0) / (m1 * X + c1) = 256/ (256-X) *X = analogue_gain_code_global		
0x0094 - 0x00BF	[7:0]	Reserved	—	—	Rewrite inhibited	—	—
0x00C0	[7:0]	data_format_model_type	01	RO static	2 byte format = 1		○
0x00C1	[7:0]	data_format_model_subtype	03	RO static	Number of data_format_descriptor_s*		○
0x00C2	[7:0]	data_format_descriptor_0[15:8]	08	RO static	[15:8]:Bit width before compression (= 08h)		○
0x00C3	[7:0]	data_format_descriptor_0[7:0]	08	RO static	[7:0] :Bit width after compression (= 08h)		
0x00C4	[7:0]	data_format_descriptor_1[15:8]	0A	RO static	[15:8]:Bit width before compression (= 0Ah)		○
0x00C5	[7:0]	data_format_descriptor_1[7:0]	08	RO static	[7:0] :Bit width after compression (= 08h)		
0x00C6	[7:0]	data_format_descriptor_2[15:8]	0A	RO static	[15:8]:Bit width before compression (= 0Ah)		○
0x00C7	[7:0]	data_format_descriptor_2[7:0]	0A	RO static	[7:0] :Bit width after compression (= 0Ah)		
0x00C8 - 0x00FF	[7:0]	Reserved	—	—	Rewrite inhibited	—	—
0x0100	[5:0]	mode_select	00	RW	Switching of Software Standby ⇔ Streaming 00h : Software Standby 01h : Streaming 10h : Data output mask (Logic: Standby, Custom: Sreaming Setting other than the above is forbidden.		○
0x0101	[1:0]	image_orientation	00	RW	Switching of horizontal/vertical direction and inverted horizontal/vertical direction [0] Inverted horizontal direction 0 : normal 1 : H Mirror [1] Inverted vertical direction 0 : normal 1 : V Flip	○	○
0x0102	[7:0]	Reserved	—		Rewrite inhibited	—	—
0x0103	[0]	software_reset	00	RW	Resets all F/F. (Software reset) 0: normal operation 1: reset * Automatically returns to 0 after setting to 1. * Transitions to Software Standby mode when set to 1. * CCI communication is not performed during Software reset.		○

Address (hex)	Bit	Register Name	initial values (hex)	RW	Description	Update Timing	Embd DL
0x0104	[0]	grouped_parameter_hold	00	RW	Register sync setting control (1) Sets register to 1. (2) Writes to register. (3) Sets to 0. → This time, the register is reflected .		○
0x0105	[0]	mask_corrupted_frames	00	RW	Mask control switching for corrupted frame 0: Don't mask corrupted frame (outputs corrupted frames) 1: Mask corrupted frame. (Fixed output to High.)		○
0x0110	[2:0]	CCP2_channel_identifier	00	RW	Channel ID	○	○
0x0111	[0]	CCP2_signalling_mode	01	RO static	Output format Selection of Data/Clock and Data/Strobe Change should be performed during Software Standby.		○
0x0112	[7:0]	CCP_data_format[15:8]	0A	RW	Data output format switching register 0x0808 : RAW8 (upper 8bits) 0x0A08 : RAW8 + 10 bit to 8 bit (compression), 0x0A0A : RAW10 Setting other than the above is forbidden. Setting should be performed during Software Standby.		○
0x0113	[7:0]	CCP_data_format[7:0]	0A	RW			
0x0114 - 0x011F	[7:0]	Reserved	—	—	Rewrite inhibited	—	—
0x0120	[0]	gain_mode	00	RW	Analog Gain mode switching 0h: All color global Analog Gain mode 1h: Analog Gain mode by cplor		○
0x0121 - 0x0201	[7:0]	Reserved	—	—	Rewrite inhibited	—	—
0x0202	[7:0]	coarse_integration_time[15:8]	03	RW	Coarse integration time setting	○	○
0x0203	[7:0]	coarse_integration_time[7:0]	20	RW			
0x0204	—	analogue_gain_code_global[15:8]	00	RW	Global Analog Gain Code setting *Valid register when ANA_GAIN_MODE = 0 Sets code value calculated by equation of (Gain = 256 / (256-ANA_GAIN_GLOBAL)).	○	○
0x0205	[7:0]	analogue_gain_code_global[7:0]	00	RW			
0x0206	[7:0]	analogue_gain_code_greenR[15:8]	00	RW	Analog Gain Code setting by color (Gr) *Sets code value calculated by equation of (Gain = 256 / (256-ANA_GAIN_GR)). (conforms to SIMA)	○	○
0x0207	[7:0]	analogue_gain_code_greenR[7:0]	00	RW			
0x0208	[7:0]	analogue_gain_code_red[15:8]	00	RW	Analog Gain Code setting by color (R) *Sets code value calculated by equation of (Gain = 256 / (256-ANA_GAIN_R)). (conforms to SIMA)	○	○
0x0209	[7:0]	analogue_gain_code_red[7:0]	00	RW			
0x020A	[7:0]	analogue_gain_code_blue[15:8]	00	RW	Analog Gain Code setting by color (B) *Sets code value calculated by equation of (Gain = 256 / (256-ANA_GAIN_B)). (conforms to SIMA)	○	○
0x020B	[7:0]	analogue_gain_code_blue[7:0]	00	RW			
0x020C	[7:0]	analogue_gain_code_greenB[15:8]	00	RW	Analog Gain Code setting by color (Gb) *Sets code value calculated by equation of (Gain = 256 / (256-ANA_GAIN_GB)). (conforms to SIMA)	○	○
0x020D	[7:0]	analogue_gain_code_greenB[7:0]	00	RW			
0x020E	[7:0]	digital_gain_greenR[15:8]	01	RW	Digital Gain Code setting by color (Gr) *Sets code value calculated by equation of (Gain = DIG_GAIN_GR[15:8]+DIG_GAIN_GR[7:0]/256). (conforms to SIMA)	○	○
0x020F	[7:0]	digital_gain_greenR[7:0]	00	RW			
0x0210	[7:0]	digital_gain_red[15:8]	01	RW	Digital Gain Code setting by color (R) *Sets code value calculated by equation of (Gain = DIG_GAIN_R[15:8]+DIG_GAIN_R[7:0]/256). (conforms to SIMA)	○	○
0x0211	[7:0]	digital_gain_red[7:0]	00	RW			
0x0212	[7:0]	digital_gain_blue[15:8]	01	RW	Digital Gain Code setting by color (B) *Sets code value calculated by equation of (Gain = DIG_GAIN_B[15:8]+DIG_GAIN_B[7:0]/256) . (conforms to SIMA)	○	○
0x0213	[7:0]	digital_gain_blue[7:0]	00	RW			
0x0214	[7:0]	digital_gain_greenB[15:8]	01	RW	Digital Gain Code setting by color (Gb) *Sets code value calculated by equation of (Gain = DIG_GAIN_GB[15:8]+DIG_GAIN_GB[7:0]/256. (conforms to SIMA)	○	○
0x0215	[7:0]	digital_gain_greenB[7:0]	00	RW			
0x0216 - 0x02FF	[7:0]	Reserved	—	—	Rewrite inhibited	—	—
0x0300	—	vt_pix_clk_div[15:8]	00	RO static	vt_pix_clk_div frequency divider setting * Fixed to 10 because it does not match actual configuration.(default) *Register RW only		○
0x0301	[7:0]	vt_pix_clk_div[7:0]	0A	RO static			
0x0302	—	vt_sys_clk_div[15:8]	00	RO static	vt_sys_clk_div frequency divider setting * Fixed to 1 because it does not match actual configuration.(default) *Register RW only		○
0x0303	[7:0]	vt_sys_clk_div[7:0]	01	RO static			
0x0304	—	pre_pll_clk_div[15:8]	00	RW	PLL Pre-divider frequency divider setting 1h : 1/1 2h : 1/2 4h : 1/4 8h : 1/8 *Setting other than the above is forbidden.		○
0x0305	[3:0]	pre_pll_clk_div[7:0]	01	RW			
0x0306	—	pll_multiplier[15:8]	00	RW	PLL multiplier setting Setting range : 8 to 183d *Setting other than the left is forbidden. (Example) Sets 108d when multiplied 108. *Set the number of multiply as it is.		○
0x0307	[7:0]	pll_multiplier[7:0]	2D	RW			
0x0308 - 0x033F	[7:0]	Reserved	—	—	Rewrite inhibited	—	—
0x0340	[7:0]	frame_length_lines[15:8]	04	RW	Number of lines in vertical direction setting *Set count number from 1.	○	○
0x0341	[7:0]	frame_length_lines[7:0]	B0	RW			
0x0342	[7:0]	line_length_pck[15:8]	08	RW	Number of pixel clocks in horizontal direction setting *Set count number from 1.	○	○
0x0343	[7:0]	line_length_pck[7:0]	CA	RW			
0x0344	[4:0]	x_addr_start[15:8]	00	RW	Holizontal cropping start address setting *Holizontal cropping start address when not inverted	○	○
0x0345	[7:0]	x_addr_start[7:0]	00	RW			
0x0346	[3:0]	y_addr_start[15:8]	00	RW	Vertical cropping start address setting *Vertical cropping start address when not inverted	○	○
0x0347	[7:0]	y_addr_start[7:0]	1C	RW			
0x0348	[4:0]	x_addr_end[15:8]	07	RW	Holizontal cropping end address setting *Holizontal cropping start address when inverted	○	○
0x0349	[7:0]	x_addr_end[7:0]	B7	RW			
0x034A	[3:0]	y_addr_end[15:8]	04	RW	Vertical cropping end address setting *Vertical cropping start address when inverted	○	○
0x034B	[7:0]	y_addr_end[7:0]	93	RW			
0x034C	[4:0]	x_output_size[15:8]	07	RW	Holizontal cropping size setting Sets cropping size from X_ADD_STA when not inverted. Sets cropping size from X_ADD_END when inverted.	○	○
0x034D	[7:0]	x_output_size[7:0]	B8	RW			
0x034E	[3:0]	y_output_size[15:8]	04	RW	Vertical cropping size setting Sets cropping size from Y_ADD_STA when not inverted. Sets cropping size from Y_ADD_END when inverted.	○	○
0x034F	[7:0]	y_output_size[7:0]	78	RW			
0x0350 - 0x037F	[7:0]	Reserved	—	—	Rewrite inhibited	—	—
0x0380	—	x_even_inc[15:8]	00	RW	Horizontal direction subsampling setting (even position)	○	○
0x0381	[3:0]	x_even_inc[7:0]	01	RW			
0x0382	—	x_odd_inc[15:8]	00	RW	Horizontal direction subsampling setting (odd position)	○	○
0x0383	[3:0]	x_odd_inc[7:0]	01	RW			
0x0384	—	y_even_inc[15:8]	00	RW	Vertical direction subsampling setting (even position)	○	○
0x0385	[3:0]	y_even_inc[7:0]	01	RW			
0x0386	—	y_odd_inc[15:8]	00	RW	Vertical direction subsampling setting (odd position)	○	○
0x0387	[3:0]	y_odd_inc[7:0]	01	RW			
0x0388 - 0x03FF	[7:0]	Reserved	—	—	Rewrite inhibited	—	—
0x0400	—	scaling_mode[15:8]	00	RW	Scaler mode setting 0h : No scaling 1h : Horizontal Scaling only 2h : Full Scaling (both horizontal and vertical) 3h : Setting inhibited	○	○
0x0401	[1:0]	scaling_mode[7:0]	00	RW			
0x0402	—	spatial_sampling[15:8]	00	RW	Spatial sample setting 0h : Bayer 1h : co-sited *Setting other than the above is forbidden.	○	○
0x0403	[1:0]	spatial_sampling[7:0]	00	RW			
0x0404	—	scale_m[15:8]	00	RW	Scaling factor M setting Setting Range ： 1 to 16d *Setting other than the above is forbidden.	○	○
0x0405	[7:0]	scale_m[7:0]	1B	RW			
0x0406	—	scale_n[15:8]	00	RO static	Scaling factor N setting Setting Range ： 16d fixed		○
0x0407	[4:0]	scale_n[7:0]	10	RO static			

Address (hex)	Bit	Register Name	initial values (hex)	RW	Description	Update Timing	Embd DL
0x0408 - 0x04FF	[7:0]	Reserved	—	—	Rewrite inhibited	—	—
0x0500	—	compression_mode[15:8]	00	RW	Compression algorithm setting 1 : Simple predictor 2 : Advanced predictor		○
0x0501	[1:0]	compression_mode[7:0]	01	RW			
0x0502 - 0x05FF	[7:0]	Reserved	—	—	Rewrite inhibited	—	—
0x0600	[7:0]	test_pattern_mode[15:8]	00	RW	Test Pattern Mode 0000h : Normal operation 0001h : Solid Color 0002h : 100 % Color Bar 0003h : Fade to grey Color Bar 0004h : PN9 0100h : Fixed Pattern1 (fixed pattern 1) (3FF*4→000*4) 0101h : Fixed Pattern2 (fixed pattern 2) (3FF→180→100→060) 0102h : Fixed Pattern3 (fixed pattern 1) (td_r*4→td_gr*4→td_b*4→td_gb*4) 0103h : Fixed Pattern4 (fixed pattern 2) (td_r→td_gr→td_r→td_gr →td_b→td_gb→td_b→td_gb) 0104h : Fixed Pattern5 (fixed pattern 3) (td_r*2→td_gr*2→td_b*2→td_gb*2) 0105h : Fixed Pattern6 (fixed pattern 4) (td_r→td_gr→td_b→td_gb) *Setting other than the above is forbidden.	○	○
0x0601	[7:0]	test_pattern_mode[7:0]	00	RW			
0x0602	[1:0]	test_data_red[15:8]	00	RW	R data in Solid Color Mode	○	○
0x0603	[7:0]	test_data_red[7:0]	00	RW			
0x0604	[1:0]	test_data_greenR[15:8]	00	RW	GR data in Solid Color Mode	○	○
0x0605	[7:0]	test_data_greenR[7:0]	00	RW			
0x0606	[1:0]	test_data_blue[15:8]	00	RW	B data in Solid Color Mode	○	○
0x0607	[7:0]	test_data_blue[7:0]	00	RW			
0x0608	[1:0]	test_data_greenB[15:8]	00	RW	GB data in Solid Color Mode	○	○
0x0609	[7:0]	test_data_greenB[7:0]	00	RW			
0x060A	[7:0]	horizontal_cursor_width[15:8]	00	RW	Test-cursor output setting Specifies horizontal direction width.		○
0x060B	[7:0]	horizontal_cursor_width[7:0]	00	RW			
0x060C	[7:0]	horizontal_cursor_position[15:8]	00	RW	Test-cursor output setting Specifies horizontal direction insertion position.		○
0x060D	[7:0]	horizontal_cursor_position[7:0]	00	RW			
0x060E	[7:0]	vertical_cursor_width[15:8]	00	RW	Test-cursor output setting Specifies vertical direction width.		○
0x060F	[7:0]	vertical_cursor_width[7:0]	00	RW			
0x0610	[7:0]	vertical_cursor_position[15:8]	00	RW	Test-cursor output setting Specifies vertical direction insertion position.		○
0x0611	[7:0]	vertical_cursor_position[7:0]	00	RW			
0x0612 - 0x0fff	[7:0]	Reserved	—	—	Rewrite inhibited	—	—

Address (hex)	Bit	Register Name	initial values (hex)	RW	Description	Update Timing	Embd DL
0x1000	—	integration_time_capability[15:8]	00	ROstatic	Integration time supported coarse: line units fine: pixel units * Only coarse setting supported		
0x1001	[0]	integration_time_capability[7:0]	00	ROstatic			
0x1002	[7:0]	Reserved	—	—	Rewrite inhibited	—	—
0x1003	[7:0]	Reserved	—	—	Rewrite inhibited	—	—
0x1004	[7:0]	coarse_integration_time_min[15:8]	00	ROstatic	Integration time coarse setting Min.		
0x1005	[7:0]	coarse_integration_time_min[7:0]	01	ROstatic			
0x1006	[7:0]	coarse_integration_time_max_margin[15:8]	00	ROstatic	Integration time coarse setting Margin value when setting Max.		
0x1007	[7:0]	coarse_integration_time_max_margin[7:0]	05	ROstatic			
0x1008 - 0x107F	[7:0]	Reserved	—	—	Rewrite inhibited	—	—
0x1080	—	digital_gain_capability[15:8]	00	ROstatic	Digital gain supported 0: Not supported 1: Supported by color		
0x1081	[0]	digital_gain_capability[7:0]	01	ROstatic			
0x1082	[7:0]	Reserved	—	—	Rewrite inhibited	—	—
0x1083	[7:0]	Reserved	—	—	Rewrite inhibited	—	—
0x1084	[7:0]	digital_gain_min[15:8]	01	ROstatic	Digital Gain code Min.		
0x1085	[7:0]	digital_gain_min[7:0]	00	ROstatic			
0x1086	[7:0]	digital_gain_max[15:8]	0F	ROstatic	Digital Gain code Max.		
0x1087	[7:0]	digital_gain_max[7:0]	FF	ROstatic			
0x1088	[7:0]	digital_gain_step_size[15:8]	00	ROstatic	Digital gain step size		
0x1089	[7:0]	digital_gain_step_size[7:0]	01	ROstatic			
0x108A - 0x10FF	[7:0]	Reserved	—	—	Rewrite inhibited	—	—
0x1100	[7:0]	min_ext_clk_freq_mhz[31:24]	40	ROstatic	INCK (external clock) input frequency Min. *6 MHz		
0x1101	[7:0]	min_ext_clk_freq_mhz[23:16]	C0	ROstatic			
0x1102	[7:0]	min_ext_clk_freq_mhz[15:8]	00	ROstatic			
0x1103	[7:0]	min_ext_clk_freq_mhz[7:0]	00	ROstatic			
0x1104	[7:0]	max_ext_clk_freq_mhz[31:24]	42	ROstatic	INCK (external clock) input frequency Max. *60 MHz		
0x1105	[7:0]	max_ext_clk_freq_mhz[23:16]	70	ROstatic			
0x1106	[7:0]	max_ext_clk_freq_mhz[15:8]	00	ROstatic			
0x1107	[7:0]	max_ext_clk_freq_mhz[7:0]	00	ROstatic			
0x1108	[7:0]	min_pre_pll_clk_div[15:8]	00	ROstatic	Pre PLL divider frequency divider Min.		
0x1109	[7:0]	min_pre_pll_clk_div[7:0]	01	ROstatic			
0x110A	[7:0]	max_pre_pll_clk_div[15:8]	00	ROstatic	Pre PLL divider frequency divider Max.		
0x110B	[7:0]	max_pre_pll_clk_div[7:0]	08	ROstatic			
0x110C	[7:0]	min_pll_ip_freq_mhz[31:24]	40	ROstatic	PLL input clock frequency Min. *6 MHz *Same as MIN_EXCK_FREQ		
0x110D	[7:0]	min_pll_ip_freq_mhz[23:16]	C0	ROstatic			
0x110E	[7:0]	min_pll_ip_freq_mhz[15:8]	00	ROstatic			
0x110F	[7:0]	min_pll_ip_freq_mhz[7:0]	00	ROstatic			
0x1110	[7:0]	max_pll_ip_freq_mhz[31:24]	42	ROstatic	PLL input clock frequency Max. *60 MHz *Same as MAX_EXCK_FREQ		
0x1111	[7:0]	max_pll_ip_freq_mhz[23:16]	70	ROstatic			
0x1112	[7:0]	max_pll_ip_freq_mhz[15:8]	00	ROstatic			
0x1113	[7:0]	max_pll_ip_freq_mhz[7:0]	00	ROstatic			
0x1114	[7:0]	min_pll_multiplier[15:8]	00	ROstatic	PLL multiplier value Min.		
0x1115	[7:0]	min_pll_multiplier[7:0]	08	ROstatic			
0x1116	[7:0]	max_pll_multiplier[15:8]	00	ROstatic	PLL multiplier value Max.		
0x1117	[7:0]	max_pll_multiplier[7:0]	B7	ROstatic			
0x1118	[7:0]	min_pll_op_freq_mhz[31:24]	43	ROstatic	PLL output frequency Min. *PLL output frequency in use range = 384 MHz		
0x1119	[7:0]	min_pll_op_freq_mhz[23:16]	C0	ROstatic			
0x111A	[7:0]	min_pll_op_freq_mhz[15:8]	00	ROstatic			
0x111B	[7:0]	min_pll_op_freq_mhz[7:0]	00	ROstatic			
0x111C	[7:0]	max_pll_op_freq_mhz[31:24]	42	ROstatic	PLL output frequency Max. *PLL output frequency in use range = 1 GHz		
0x111D	[7:0]	max_pll_op_freq_mhz[23:16]	98	ROstatic			
0x111E	[7:0]	max_pll_op_freq_mhz[15:8]	00	ROstatic			
0x111F	[7:0]	max_pll_op_freq_mhz[7:0]	00	ROstatic			
0x1120	[7:0]	min_vt_sys_clk_div[15:8]	00	ROstatic	vt_sys_clk_div frequency divider Min. *Fixed to 1 because mismatched to actual configuration. (default)		
0x1121	[7:0]	min_vt_sys_clk_div[7:0]	01	ROstatic			
0x1122	[7:0]	max_vt_sys_clk_div[15:8]	00	ROstatic	vt_sys_clk_div frequency divider Max. *Fixed to 1 because mismatched to actual configuration. (default)		
0x1123	[7:0]	max_vt_sys_clk_div[7:0]	01	ROstatic			
0x1124	[7:0]	min_vt_sys_clk_freq_mhz[31:24]	00	ROstatic	vt_sys_clk frequency Min. * Mismatched to actual configuration.		
0x1125	[7:0]	min_vt_sys_clk_freq_mhz[23:16]	00	ROstatic			
0x1126	[7:0]	min_vt_sys_clk_freq_mhz[15:8]	00	ROstatic			
0x1127	[7:0]	min_vt_sys_clk_freq_mhz[7:0]	00	ROstatic			
0x1128	[7:0]	max_vt_sys_clk_freq_mhz[31:24]	00	ROstatic	vt_sys_clk frequency Max. * Mismatched to actual configuration.		
0x1129	[7:0]	max_vt_sys_clk_freq_mhz[23:16]	00	ROstatic			
0x112A	[7:0]	max_vt_sys_clk_freq_mhz[15:8]	00	ROstatic			
0x112B	[7:0]	max_vt_sys_clk_freq_mhz[7:0]	00	ROstatic			
0x112C	[7:0]	min_vt_pix_clk_freq_mhz[31:24]	00	ROstatic	vt_pix_clk frequency Min. * Mismatched to actual configuration.		
0x112D	[7:0]	min_vt_pix_clk_freq_mhz[23:16]	00	ROstatic			
0x112E	[7:0]	min_vt_pix_clk_freq_mhz[15:8]	00	ROstatic			
0x112F	[7:0]	min_vt_pix_clk_freq_mhz[7:0]	00	ROstatic			
0x1130	[7:0]	max_vt_pix_clk_freq_mhz[31:24]	00	ROstatic	vt_pix_clk frequency Max. * Mismatched to actual configuration.		
0x1131	[7:0]	max_vt_pix_clk_freq_mhz[23:16]	00	ROstatic			
0x1132	[7:0]	max_vt_pix_clk_freq_mhz[15:8]	00	ROstatic			
0x1133	[7:0]	max_vt_pix_clk_freq_mhz[7:0]	00	ROstatic			
0x1134	[7:0]	min_vt_pix_clk_div[15:8]	00	ROstatic	vt_pix_clk_div frequency divider Min. *Fixed to 0xA because mismatched to actual configuration. (default)		
0x1135	[7:0]	min_vt_pix_clk_div[7:0]	0A	ROstatic			
0x1136	[7:0]	max_vt_pix_clk_div[15:8]	00	ROstatic	vt_pix_clk_div frequency divider Max. * Fixed to 0xA because mismatched to actual configuration. (default)		
0x1137	[7:0]	max_vt_pix_clk_div[7:0]	0A	ROstatic			
0x1138 - 0x113F	[7:0]	Reserved	—	—	Rewrite inhibited	—	—
0x1140	[7:0]	min_frame_length_lines[15:8]	00	ROstatic	Number of lines per frame Min.		
0x1141	[7:0]	min_frame_length_lines[7:0]	CA	ROstatic			
0x1142	[7:0]	max_frame_length_lines[15:8]	FF	ROstatic	Number of lines per frame Max.		
0x1143	[7:0]	max_frame_length_lines[7:0]	FF	ROstatic			
0x1144	[7:0]	min_line_length_pck[15:8]	02	ROstatic	Number of pixel clocks per frame Min.		
0x1145	[7:0]	min_line_length_pck[7:0]	30	ROstatic			
0x1146	[7:0]	max_line_length_pck[15:8]	FF	ROstatic	Number of pixel clocks per frame Max.		
0x1147	[7:0]	max_line_length_pck[7:0]	F0	ROstatic			
0x1148	[7:0]	min_line_blanking_pck[15:8]	00	ROstatic	Number of horizontal blanking pixel clocks Min.		
0x1149	[7:0]	min_line_blanking_pck[7:0]	2D	ROstatic			
0x114A	[7:0]	min_frame_blanking_lines[15:8]	00	ROstatic	Number of vertical blanking lines Min.		
0x114B	[7:0]	min_frame_blanking_lines[7:0]	02	ROstatic			
0x114C - 0x115F	[7:0]	Reserved	—	—	Rewrite inhibited	—	—
0x1160	[7:0]	min_op_sys_clk_div[15:8]	00	ROstatic	op_sys_clk_div frequency divider Min. *Not supported		
0x1161	[7:0]	min_op_sys_clk_div[7:0]	00	ROstatic			
0x1162	[7:0]	max_op_sys_clk_div[15:8]	00	ROstatic	op_sys_clk_div frequency divider Max. *Not supported		
0x1163	[7:0]	max_op_sys_clk_div[7:0]	00	ROstatic			
0x1164	[7:0]	min_op_sys_clk_freq_mhz[31:24]	00	ROstatic	op_sys_clk frequency Min. *Not supported		
0x1165	[7:0]	min_op_sys_clk_freq_mhz[23:16]	00	ROstatic			
0x1166	[7:0]	min_op_sys_clk_freq_mhz[15:8]	00	ROstatic			
0x1167	[7:0]	min_op_sys_clk_freq_mhz[7:0]	00	ROstatic			

Address (hex)	Bit	Register Name	initial values (hex)	RW	Description	Update Timing	Embd DL
0x1168	[7:0]	max_op_sys_clk_freq_mhz[31:24]	00	ROstatic	op_sys_clk frequency Max. *Not supported		
0x1169	[7:0]	max_op_sys_clk_freq_mhz[23:16]	00	ROstatic			
0x116A	[7:0]	max_op_sys_clk_freq_mhz[15:8]	00	ROstatic			
0x116B	[7:0]	max_op_sys_clk_freq_mhz[7:0]	00	ROstatic			
0x116C	[7:0]	min_op_pix_clk_div[15:8]	00	ROstatic	op_pix_clk_div frequency divider Min. *Not supported		
0x116D	[7:0]	min_op_pix_clk_div[7:0]	00	ROstatic			
0x116E	[7:0]	max_op_pix_clk_div[15:8]	00	ROstatic	op_pix_clk_div frequency divider Max. *Not supported		
0x116F	[7:0]	max_op_pix_clk_div[7:0]	00	ROstatic			
0x1170	[7:0]	min_op_pix_clk_freq_mhz[31:24]	00	ROstatic	op_pix_clk frequency Min. *Not supported		
0x1171	[7:0]	min_op_pix_clk_freq_mhz[23:16]	00	ROstatic			
0x1172	[7:0]	min_op_pix_clk_freq_mhz[15:8]	00	ROstatic			
0x1173	[7:0]	min_op_pix_clk_freq_mhz[7:0]	00	ROstatic			
0x1174	[7:0]	max_op_pix_clk_freq_mhz[31:24]	00	ROstatic	op_pix_clk frequency Max. *Not supported		
0x1175	[7:0]	max_op_pix_clk_freq_mhz[23:16]	00	ROstatic			
0x1176	[7:0]	max_op_pix_clk_freq_mhz[15:8]	00	ROstatic			
0x1177	[7:0]	max_op_pix_clk_freq_mhz[7:0]	00	ROstatic			
0x1178 - 0x117F	[7:0]	Reserved	—	—	Rewrite inhibited	—	—
0x1180	[7:0]	x_addr_min[15:8]	00	ROstatic	Croppingt setting Address X direction Min.		
0x1181	[7:0]	x_addr_min[7:0]	00	ROstatic			
0x1182	[7:0]	y_addr_min[15:8]	00	ROstatic	Cropping setting Address Y direction Min.		
0x1183	[7:0]	y_addr_min[7:0]	00	ROstatic			
0x1184	[7:0]	x_addr_max[15:8]	07	ROstatic	Cropping setting Address X direction Max.		
0x1185	[7:0]	x_addr_max[7:0]	B7	ROstatic			
0x1186	[7:0]	y_addr_max[15:8]	04	ROstatic	Cropping setting Address Y direction Max.		
0x1187	[7:0]	y_addr_max[7:0]	AF	ROstatic			
0x1188	[7:0]	min_x_output_size[15:8]	01	ROstatic	Cropping setting Size X direction Min.		
0x1189	[7:0]	min_x_output_size[7:0]	00	ROstatic			
0x118A	[7:0]	min_y_output_size[15:8]	00	ROstatic	Cropping setting Size Y direction Min.		
0x118B	[7:0]	min_y_output_size[7:0]	C0	ROstatic			
0x118C	[7:0]	max_x_output_size[15:8]	07	ROstatic	Cropping setting Size X direction Max.		
0x118D	[7:0]	max_x_output_size[7:0]	B8	ROstatic			
0x118E	[7:0]	max_y_output_size[15:8]	04	ROstatic	Cropping setting Size Y direction Max.		
0x118F	[7:0]	max_y_output_size[7:0]	B0	ROstatic			
0x11C0	[7:0]	min_even_inc[15:8]	00	ROstatic	Subsampling setting even position Min.		
0x11C1	[7:0]	min_even_inc[7:0]	01	ROstatic			
0x11C2	[7:0]	max_even_inc[15:8]	00	ROstatic	Subsampling setting even position Max.		
0x11C3	[7:0]	max_even_inc[7:0]	0F	ROstatic			
0x11C4	[7:0]	min_odd_inc[15:8]	00	ROstatic	Subsampling setting odd position Min.		
0x11C5	[7:0]	min_odd_inc[7:0]	01	ROstatic			
0x11C6	[7:0]	max_odd_inc[15:8]	00	ROstatic	Subsampling setting odd position Max.		
0x11C7	[7:0]	max_odd_inc[7:0]	0F	ROstatic			
0x11C8 - 0x11FF	[7:0]	Reserved	—	—	Rewrite inhibited	—	—
0x1200	—	scaling_capability[15:8]	00	ROstatic	Scaler setting 0 : Not supported 1 : Horizontal 2 : Horizontal & Vertical		
0x1201	[1:0]	scaling_capability[7:0]	01	ROstatic			
0x1202	[7:0]	Reserved	—	—	Rewrite inhibited	—	—
0x1203	[7:0]	Reserved	—	—	Rewrite inhibited	—	—
0x1204	—	scaler_m_min[15:8]	00	ROstatic	Down scale factor : Mini. M value		
0x1205	[7:0]	scaler_m_min[7:0]	10	ROstatic			
0x1206	—	scaler_m_max[15:8]	00	ROstatic	Down scale factor : Max. M value		
0x1207	[7:0]	scaler_m_max[7:0]	80	ROstatic			
0x1208	—	scaler_n_min[15:8]	00	ROstatic	Down scale factor : Min. N value		
0x1209	[4:0]	scaler_n_min[7:0]	10	ROstatic			
0x120A	—	scaler_n_max[15:8]	00	ROstatic	Down scale factor : Max. N value		
0x120B	[4:0]	scaler_n_max[7:0]	10	ROstatic			
0x120C - 0x12FF	[7:0]	Reserved	—	—	Rewrite inhibited	—	—
0x1300	—	compression_capability[15:8]	00	ROstatic	Data compression 0 : Not supported 1 : DPCM/PCM		
0x1301	[0]	compression_capability[7:0]	01	ROstatic			
0x1302 - 0x13FF	[7:0]	Reserved	—	—	Rewrite inhibited	—	—
0x1400	[7:0]	matrix_element_RedInRed[15:8]	00	ROstatic	Color matrix parameter *Not supported		
0x1401	[7:0]	matrix_element_RedInRed[7:0]	00	ROstatic			
0x1402	[7:0]	matrix_element_GreenInRed[15:8]	00	ROstatic	Color matrix parameter *Not supported		
0x1403	[7:0]	matrix_element_GreenInRed[7:0]	00	ROstatic			
0x1404	[7:0]	matrix_element_BlueInRed[15:8]	00	ROstatic	Color matrix parameter *Not supported		
0x1405	[7:0]	matrix_element_BlueInRed[7:0]	00	ROstatic			
0x1406	[7:0]	matrix_element_RedInGreen[15:8]	00	ROstatic	Color matrix parameter *Not supported		
0x1407	[7:0]	matrix_element_RedInGreen[7:0]	00	ROstatic			
0x1408	[7:0]	matrix_element_GreenInGreen[15:8]	00	ROstatic	Color matrix parameter *Not supported		
0x1409	[7:0]	matrix_element_GreenInGreen[7:0]	00	ROstatic			
0x140A	[7:0]	matrix_element_BlueInGreen[15:8]	00	ROstatic	Color matrix parameter *Not supported		
0x140B	[7:0]	matrix_element_BlueInGreen[7:0]	00	ROstatic			
0x140C	[7:0]	matrix_element_RedInBlue[15:8]	00	ROstatic	Color matrix parameter *Not supported		
0x140D	[7:0]	matrix_element_RedInBlue[7:0]	00	ROstatic			
0x140E	[7:0]	matrix_element_GreenInBlue[15:8]	00	ROstatic	Color matrix parameter *Not supported		
0x140F	[7:0]	matrix_element_GreenInBlue[7:0]	00	ROstatic			
0x1410	[7:0]	matrix_element_BlueInBlue[15:8]	00	ROstatic	Color matrix parameter *Not supported		
0x1411	[7:0]	matrix_element_BlueInBlue[7:0]	00	ROstatic			
0x1412 - 0x1fff	[7:0]	Reserved	—	—	Rewrite inhibited	—	—

2-wire serial communication register map (Manufacture specific register 0x3000 to 0x30FF)

Address (hex)		Bit	Register Name	initial values (hex)	RW	Description	Update Timing
3000 - 3017	0	[7:0]	ManufactureRegister	—	—	Rewrite inhibited	—
	1						
	2						
	3						
	4						
	5						
	6						
	7						
3018	0	[0]	ManufactureRegister	04	R/W	Rewrite inhibited	
	1	[0]	FMCEN		R/W	Fast mode Transition Setting [1] : Fast mode transition setting [0] : Normal mode (includes ignored frame)	○
	2	[0]	MASK_SHORT_FRM		R/W	Frame mask control switching during Fast mode transition 0 : Masks invalid frames. 1 : Don't mask invalid frames.	
	3						
	4						
	5						
	6						
	7						
3019 - 3031	0	[7:0]	ManufactureRegister	—	—	Rewrite inhibited	—
	1						
	2						
	3						
	4						
	5						
	6						
	7						
3032	0	[7:0]	BLKLEVEL[0]	40	R/W	Black level setting input Sets black level to the pixel data after signal processing. The LSB unit is “1”.	
	1		BLKLEVEL[1]		R/W		
	2		BLKLEVEL[2]		R/W		
	3		BLKLEVEL[3]		R/W		
	4		BLKLEVEL[4]		R/W		
	5		BLKLEVEL[5]		R/W		
	6		BLKLEVEL[6]		R/W		
	7		BLKLEVEL[7]		R/W		
3033	0	[7:0]	ManufactureRegister	—	—	Rewrite inhibited	—
	1						
	2						
	3						
	4						
	5						
	6						
	7						
3034	0	[0]	IMGORICTRL	00	R/W	Inverted and not inverted switching of IMG_ORIENTATION 0 : As Register IMG_ORIENTATION setting is. 1 : Register IMG_ORIENTATION setting inverted internally	
	1						
	2						
	3						
	4						
	5						
	6						
	7						
3035	0				R/W		
	1						
	2						
	3						
	4	[0]	SW_RESET_DI	00	R/W	Resets all F/F other than registers (function reset) 0: Normal operation 1: Reset * Don't return to 0 automatically after setting to 1.	
	5						
	6						
	7						
3036	0	[0]	ManufactureRegister	00	R/W	Rewrite inhibited	
	1						
	2						
	3						
	4						
	5						
	6						
	7						
3037 - 3038	0	[7:0]	ManufactureRegister	—	—	Rewrite inhibited	—
	1						
	2						
	3						
	4						
	5						
	6						
	7						
3039	0	[0]	EC_AGAIN_MODE	00	R/W	Output gain value by color = gain by color + ANA_GAIN_GLOBAL binning flag 0: ANA_GAIN_GLOBAL + gain by color 1: Only gain by color	
	1	[1:0]	ManufactureRegister		R/W	Rewrite inhibited	
	2		ManufactureRegister		R/W		
	3						
	4						
	5						
	6						
	7						
303A - 303B	0	[7:0]	ManufactureRegister	—	—	Rewrite inhibited	—
	1						
	2						
	3						
	4						
	5						
	6						
	7						

Address (hex)		Bit	Register Name	Initial values (hex)	RW	Description	Update Timing
303C	0	[7:0]	PLSTATIM[0]	38	R/W	PLL oscillation stable wait timer setting (Maximum count value in INCK) Recommended value (Setting value that count value in INCK exceeds 200 µs a little in each setting.) INCK = 27 MHz: 54h (84d) INCK = 18 MHz: 38h (56d) INCK = 6 MHz: 12h (18d) (Designates the upper 8bits of the 14-bit down counter. *The lower 6bits are fixed to 3Fh internally. PLL oscillation stable wait time = PLSTATIM * INCK < < 6 | 3Fh))	
	1		PLSTATIM[1]		R/W		
	2		PLSTATIM[2]		R/W		
	3		PLSTATIM[3]		R/W		
	4		PLSTATIM[4]		R/W		
	5		PLSTATIM[5]		R/W		
	6		PLSTATIM[6]		R/W		
	7		PLSTATIM[7]		R/W		
303D	0	[3:0]	ManufactureRegister	10	R/W	Rewrite inhibited	
	1		ManufactureRegister		R/W		
	2		ManufactureRegister		R/W		
	3		ManufactureRegister		R/W		
	4	[0]	FRMSTAMODE		R/W	Setting of period from software standby cancel until start frame output 0 : Waits integration time 1 : Don't wait integration time	
	5						
	6						
	7						
303E - 303F	0	[7:0]	ManufactureRegister	—	—	Rewrite inhibited	—
	1						
	2						
	3						
	4						
	5						
	6						
	7						
3040	0	[5:0]	Y_OPBADD_STA[0]	08	R/W	Effective OPB start address in vertical direction	○
	1		Y_OPBADD_STA[1]		R/W		
	2		Y_OPBADD_STA[2]		R/W		
	3		Y_OPBADD_STA[3]		R/W		
	4		Y_OPBADD_STA[4]		R/W		
	5		Y_OPBADD_STA[5]		R/W		
	6						
	7						
3041	0	[5:0]	Y_OPBADD_END[0]	97	R/W	Effective OPB end address in vertical direction	○
	1		Y_OPBADD_END[1]		R/W		
	2		Y_OPBADD_END[2]		R/W		
	3		Y_OPBADD_END[3]		R/W		
	4		Y_OPBADD_END[4]		R/W		
	5		Y_OPBADD_END[5]		R/W		
	6						
	7	[0]	Y_AUTOSTART		R/W	Selection of adding two lines of ignored OPB and aperture ignored 0: Use Y_OPBADD_STA/y_addr_start as the start address 1: Automatic calculation : The start address is calculated from Y_OPBADD_STA/y_addr_start	○
3042 - 3047	0	[7:0]	ManufactureRegister	—	—	Rewrite inhibited	—
	1						
	2						
	3						
	4						
	5						
	6						
	7						
3048	0	[0]	VMODEFDS	00	R/W	Vertical analog addition operation setting 0: No Vertical analog addition 1: Vertical analog addition operates	○
	1	[0]	VMODEADD		R/W	Vertical digital addition setting 0 : No addition 1 : Vertical digital addition operates	○
	2	[0]	ManufactureRegister		R/W	Rewrite inhibited	
	3	[1:0]	ManufactureRegister		R/W	Rewrite inhibited	
	4		ManufactureRegister		R/W		
	5	[2:0]	VMODEADDJMP[0]		R/W	Selection of addition lines by vertical digital addition 0 : No addition 1 : +2 lines 2 : +4 lines 3 : +6 lines 4 : +8 lines 5 : +10 lines 6 : +12 lines 7 : +14 lines	○
	6		VMODEADDJMP[1]		R/W		
	7		VMODEADDJMP[2]		R/W		
3049	0	[0]	SUMFDCN	00	R/W	Selection of the number of addition pixels by Vertical digital addition + Vertical analog addition 0 : 4 pixels addition 1 : 3 pixels addition	○
	1						
	2						
	3						
	4						
	5						
	6						
	7						
304A	0	[0]	SMD	04	R/W	Shutter mode switching 0: Rolling shutter mode 1: Global reset mode	○
	1	[0]	MECHSHR_EN		R/W	Mechanical shutter pulse enable 0 : OFF 1 : ON	○
	2	[0]	MECHSHR_SMDMODE		R/W	Selection of interlock mode with register SMD in Mechanical shutter function 0 : Interlock with register SMD Disable 1 : Interlock with register SMD Enable	
	3						
	4	[0]	FLASH_EN		R/W	Xenon flash function ON/OFF selection 0 : Xenon flash function Disable 1 : Xenon flash function Enable	○
	5	[0]	LED_FLASH_EN		R/W	LED flash function ON/OFF selection 0 : LED flash function Disable 1 : LED flash function Enable	○
	6	[0]	PRE_FLASH_EN		R/W	Preflash function ON/OFF selection 0 : Preflash function Disable 1 : Preflash function Enable	
	7	[0]	FLASH_SMDMODE		R/W	Selection of interlock mode with register SMD in Xenon flash function 0 : Interlock with register SMD Disable 1 : Interlock with register SMD Enable	
304B	0	[0]	SHR_FORBK	20	R/W	Mode selection of integration/sweep time 0: Integration time 1: Sweep time	
	1	[1:0]	ManufactureRegister		0	Rewrite inhibited	
	2		ManufactureRegister		0		
	3	[1:0]	ManufactureRegister		0	Rewrite inhibited	
	4		ManufactureRegister		R/W		
	5	[1:0]	ManufactureRegister		R/W	Rewrite inhibited	
	6		ManufactureRegister		R/W		
	7						

Address (hex)		Bit	Register Name	Initial values (hex)	RW	Description	Update Timing
304C	0	[10:0]	HCNTHALF[0]	2F	R/W	Number of readout pixels *It counts from 0. *unit : H	○
	1		HCNTHALF[1]		R/W		
	2		HCNTHALF[2]		R/W		
	3		HCNTHALF[3]		R/W		
	4		HCNTHALF[4]		R/W		
	5		HCNTHALF[5]		R/W		
	6		HCNTHALF[6]		R/W		
	7		HCNTHALF[7]		R/W		
304D	0		HCNTHALF[8]	02	R/W		
	1		HCNTHALF[9]		R/W		
	2		HCNTHALF[10]		R/W		
	3						
	4						
	5						
	6						
	7						
304E 305C	0 1 2 3 4 5 6 7	[7:0]	ManufactureRegister	—	—	Rewrite inhibited	—
305D	0	[0]	ManufactureRegister	00	R/W	Rewrite inhibited	
	1	[0]	ManufactureRegister		R/W	Rewrite inhibited	
	2	[0]	ManufactureRegister		R/W	Rewrite inhibited	
	3						
	4	[1:0]	ManufactureRegister		R/W	Rewrite inhibited	
	5		ManufactureRegister		R/W		
	6	[0]	MECHSHR_PL_STEP0		R/W	Pulse width setting 2 for Mechanical shutter formula (1) : mechanical shutter pulse width[H] = MECHSHR_PL_STEP[15:0]+ 1/2 × MECHSHR_PL_STEP0 formula (2) : mechanical shutter pulse width[μs] = 1/ (CK_PIXEL) × 64 × 2^ (MECHSHR_PL_STEP[9:8]) × (MECHSHR_PL_STEP[5:0]+1)	
	7	[0]	MECHSHR_PL_MODE		R/W	Selection of unit for Mechanical shutter pulse 0 : H *formula (1) 1 : μs *formula (2) formula (1) : mechanical shutter pulse width[H] = MECHSHR_PL_STEP[15:0] + 1/2 × MECHSHR_PL_STEP0 formula (2) : mechanical shutter pulse width[μs] = 1/ (CK_PIXEL) × 64 × 2^(MECHSHR_PL_STEP[9:8]) × (MECHSHR_PL_STEP[5:0]+1)	
305E	0	[15:0]	MECHSHR_PL_STEP[0]	0B	R/W	Pulse width setting 1 for Mechanical shutter formula (1) : mechanical shutter pulse width[H] = MECHSHR_PL_STEP[15:0] + 1/2 × MECHSHR_PL_STEP0 formula (2) : mechanical shutter pulse width[μs] = 1/ (CK_PIXEL) × 64 × 2^ (MECHSHR_PL_STEP[9:8]) × (MECHSHR_PL_STEP[5:0] + 1)	
	1		MECHSHR_PL_STEP[1]		R/W		
	2		MECHSHR_PL_STEP[2]		R/W		
	3		MECHSHR_PL_STEP[3]		R/W		
	4		MECHSHR_PL_STEP[4]		R/W		
	5		MECHSHR_PL_STEP[5]		R/W		
	6		MECHSHR_PL_STEP[6]		R/W		
	7		MECHSHR_PL_STEP[7]		R/W		
305F	0		MECHSHR_PL_STEP[8]	0C	R/W		
	1		MECHSHR_PL_STEP[9]		R/W		
	2		MECHSHR_PL_STEP[10]		R/W		
	3		MECHSHR_PL_STEP[11]		R/W		
	4		MECHSHR_PL_STEP[12]		R/W		
	5		MECHSHR_PL_STEP[13]		R/W		
	6		MECHSHR_PL_STEP[14]		R/W		
	7		MECHSHR_PL_STEP[15]		R/W		
3060	0	[13:0]	MECHSHR_STR[0]	00	R/W	Rise position setting for Mechanical Shutter Pulse 0 : OPB start 1 : OPB start + 4 lines 2 : OPB start + 8 lines …….. *Setting range : 0 to frame_length_lines/4 by 4H	
	1		MECHSHR_STR[1]		R/W		
	2		MECHSHR_STR[2]		R/W		
	3		MECHSHR_STR[3]		R/W		
	4		MECHSHR_STR[4]		R/W		
	5		MECHSHR_STR[5]		R/W		
	6		MECHSHR_STR[6]		R/W		
	7		MECHSHR_STR[7]		R/W		
3061	0		MECHSHR_STR[8]	00	R/W		
	1		MECHSHR_STR[9]		R/W		
	2		MECHSHR_STR[10]		R/W		
	3		MECHSHR_STR[11]		R/W		
	4		MECHSHR_STR[12]		R/W		
	5		MECHSHR_STR[13]		R/W		
	6						
	7						
3062	0 1 2 3 4 5 6 7	[7:0]	ManufactureRegister	—	—	Rewrite inhibited	—
3063	0	[2:0]	3DMODE[0]	00	R/W	3D mode setting 0: 3D mode Off (default) 1: 3D mode1 2: 3D mode2 3: 3D mode3 4: 3D mode4	
	1		3DMODE[1]		R/W		
	2		3DMODE[2]		R/W		
	3						
	4						
	5						
	6						
	7						
3064	0	[0]	ManufactureRegister	92	R/W	Rewrite inhibited	
	1	[0]	ManufactureRegister		R/W	Rewrite inhibited	
	2	[0]	ManufactureRegister		R/W	Rewrite inhibited	
	3	[0]	ManufactureRegister		R/W	Rewrite inhibited	
	4	[0]	AGAIN_SEL		R/W	Global Analog Gain Code setting method switching 0 : log linear mode (0.3 dB steps) 1 : Sets the gain code value calculated by the formula (Gain = 256/(256 - analogue_gain_code_global).	○
	5						
	6						
	7	[0]	SMIA_SW		R/W	Global switching of Register setting method Setting method of analog gain, cropping address and black level. 0 : Not conformed to SMIA standard 1 : Conformed to SMIA standard	
3065	0	[0]	MASK_DMY	10	R/W	Trigger setting of mask control for corrupted frame →When register MASK_DMY is changed from 0 to 1 , or from 1 to 0, the Mask flag for corrupted frame is outputted for frame set by from register MASK_CORR_FRM_STA to register MASK_CORR_FRM_END.	○
	1	[2:0]	MASK_CORR_FRM_STA[0]		R/W	Mask control setting for corrupted frame Setting of the frame which starts mask control	
	2		MASK_CORR_FRM_STA[1]		R/W		
	3		MASK_CORR_FRM_STA[2]		R/W		
	4	[3:0]	MASK_CORR_FRM_END[0]		R/W	Mask control setting for corrupted frame Setting of the frame which ends mask control	
	5		MASK_CORR_FRM_END[1]		R/W		
	6		MASK_CORR_FRM_END[2]		R/W		
	7		MASK_CORR_FRM_END[3]		R/W		

Address (hex)		Bit	Register Name	Initial values (hex)	RW	Description	Update Timing
3066 - 3069	0 to 7	[7:0]	ManufactureRegister	—	—	Rewrite inhibited	—
306A	0	[0]	ManufactureRegister	10	—	Rewrite inhibited	
	1	[0]	ManufactureRegister		—	Rewrite inhibited	
	2	[0]	ManufactureRegister		—	Rewrite inhibited	
	3	[0]	ManufactureRegister		—	Rewrite inhibited	
	4	[0]	ManufactureRegister		—	Rewrite inhibited	
	5	[0]	Y_SP_ELIMINATION		R/W	2/3 subsampling ON/OFF control 0 : 2/3 subsampling OFF 1 : 2/3 subsampling ON	
	6	[0]	ManufactureRegister		—	Rewrite inhibited	
	7	[0]	ManufactureRegister		—	Rewrite inhibited	
306B - 307A	0 to 7	[7:0]	ManufactureRegister	—	—	Rewrite inhibited	—
307B	0	[1:0]	FLASH_DLY[0]	00	R/W	Xenon Flash pulse delay setting 0: Next Frame to communication (default): 1: 1 frame after default setting 2: 2 frames after default setting 3: 3 frames after default setting	
	1		FLASH_DLY[1]		R/W		
	2	[0]	FLASH_REP		R/W	Xenon Flash pulse repeat setting 0: Single frame output 1: Every frame output	
	3	[0]	FLASH_STR		R/W	Xenon Flash pulse Start Position setting 0 : XVS reference 1 : Following V blanking reference	
	4	[3:0]	GRRLVL[0]		R/W	Reflection timing for Global Reset 0000 : Next frame 0001 : 2 frames after 0010 : 3 frames after : 0111 : 8 frames after 1xxx : 9 frames after	
	5		GRRLVL[1]		R/W		
	6		GRRLVL[2]		R/W		
	7		GRRLVL[3]		R/W		
307C	0	[2:0]	FLASH_PL_STEP_GAIN[0]	00	R/W	Pulse width setting for Xenon Flash Pulse width = 64 × Pixel clocks cycle × FLASH_PL_STEP × 2^FLASH_PL_STEP_GAIN	○
	1		FLASH_PL_STEP_GAIN[1]		R/W		
	2		FLASH_PL_STEP_GAIN[2]				
	3 to 7						
307D	0	[5:0]	FLASH_PL_STEP[0]	00	R/W	Pulse width setting for Xenon Flash Pulse width = 64 × Pixel clocks cycle × FLASH_PL_STEP × 2^FLASH_PL_STEP_GAIN	○
	1		FLASH_PL_STEP[1]		R/W		
	2		FLASH_PL_STEP[2]		R/W		
	3		FLASH_PL_STEP[3]		R/W		
	4		FLASH_PL_STEP[4]		R/W		
	5		FLASH_PL_STEP[5]		R/W		
	6 to 7						
307E - 309A	0 to 7	[7:0]	ManufactureRegister	—	—	Rewrite inhibited	—
309B	0	[0]	ManufactureRegister	20	R/W	Rewrite inhibited	
	1	[0]	ManufactureRegister		R/W	Rewrite inhibited	
	2						
	3	[0]	RGDAFDSUMEN		R/W	PGA-DAC initial current value setting 0 : default 1 : Vertical analog addition (double current)(normally not used)	○
	4	[0]	ManufactureRegister		R/W	Rewrite inhibited	
	5	[1:0]	ManufactureRegister		R/W	Rewrite inhibited	
	6		ManufactureRegister		R/W		
	7						
309C - 309F	0 to 7	[7:0]	ManufactureRegister	—	—	Rewrite inhibited	—
30A0	0	[0]	RGSPV2ADDEN	10	R/W	Vertical digital addition for HD mode 0 : Normal operation 1 : Vertical digital addition for HD mode	○
	1	[0]	ManufactureRegister		R/W	Rewrite inhibited	
	2	[0]	ManufactureRegister		R/W	Rewrite inhibited	
	3	[0]	ManufactureRegister		R/W	Rewrite inhibited	
	4	[0]	ManufactureRegister		R/W	Rewrite inhibited	
	5	[0]	ManufactureRegister		R/W	Rewrite inhibited	○
	6	[0]	ManufactureRegister		R/W	Rewrite inhibited	
	7						
30A1 - 30A3	0 to 7	[7:0]	ManufactureRegister	—	—	Rewrite inhibited	—
30A4	0	[1:0]	RGPLTD[0]	02	R/W	PLL frequency division setting (Linked to the register pll_multiplier) 0: 1/2 frequency division 1: 1/4 frequency division 2: 1/1 frequency division 3: Not used	○
	1		RGPLTD[1]		R/W		
	2						
	3	[0]	ManufactureRegister		R/W	Rewrite inhibited	
	4	[0]	ManufactureRegister		R/W	Rewrite inhibited	
	5	[0]	ManufactureRegister		R/W	Rewrite inhibited	
	6	[0]	ManufactureRegister		R/W	Rewrite inhibited	
	7	[0]	ManufactureRegister		R/W	Rewrite inhibited	
30A5 - 30AA	0 to 7	[7:0]	ManufactureRegister	—	—	Rewrite inhibited	—

Address (hex)		Bit	Register Name	Initial values (hex)	R/W	Description	Update Timing
30AB	0	[0]	ACLPMODE	01	R/W	Analog clamp mode switching control register 0: All color feedback control 1: Direct control *When using direct control, ACLPCODEDIR [6:0] setting is needed. The setting value results code input of clamp DAC.	
	1						
	2	[0]	ManufactureRegister		R/W	Rewrite inhibited	
	3	[0]	ManufactureRegister		R/W	Rewrite inhibited	
	4	[0]	ManufactureRegister		R/W	Rewrite inhibited	
	5	[0]	ManufactureRegister		R/W	Rewrite inhibited	
	6	[1:0]	ManufactureRegister		R/W	Rewrite inhibited	
	7		ManufactureRegister		R/W		
30AC	0	[7:0]	ManufactureRegister	—	—	Rewrite inhibited	—
	1						
	2						
	3						
	4						
	5						
	6						
	7						
30AD	0	[6:0]	ACLPCODEDIR[0]	08	R/W	Clamp DAC code setting register in Direct control mode *Valid when ACLPMODE = 1 (Direct control mode)	
	1		ACLPCODEDIR[1]		R/W		
	2		ACLPCODEDIR[2]		R/W		
	3		ACLPCODEDIR[3]		R/W		
	4		ACLPCODEDIR[4]		R/W		
	5		ACLPCODEDIR[5]		R/W		
	6		ACLPCODEDIR[6]		R/W		
	7	[0]	ManufactureRegister		R/W	Rewrite inhibited	
30AE - 30AF	0	[7:0]	ManufactureRegister	—	—	Rewrite inhibited	—
	1						
	2						
	3						
	4						
	5						
	6						
	7						
30B0	0	[1:0]	DCLPMODE[0]	32	R/W	Digital clamp mode selection register 0 : No digital clamp (digital clamo OFF) 1 : Global digital clamp by average of all color 2 : Digital clamp by color by average of color 3 : Same as 0	
	1						
	2		DCLPMODE[1]		R/W		
	3						
	4	[0]	ManufactureRegister		R/W	Rewrite inhibited	
	5	[0]	ManufactureRegister		R/W	Rewrite inhibited	
	6	[1:0]	ManufactureRegister		R/W	Rewrite inhibited	
	7		ManufactureRegister		R/W		
30B1 - 30D4	0	[7:0]	ManufactureRegister	—	—	Rewrite inhibited	—
	1						
	2						
	3						
	4						
	5						
	6						
	7						
30D5	0	[0]	HADDEN	00	R/W	Horizontal direction binning mode setting 0 : Sub sampling mode (Horizontal direction) 1 : Addition mode (Operation is decided by HADDMODE.)	○
	1	[0]	HADDMODE		R/W	Horizontal direction binning operation setting 0 : Horizontal weighted addition mode 1 : Horizontal 2 pixels addition mode	○
	2	[0]	ManufactureRegister		R/W	Rewrite inhibited	○
	3	[0]	HADCONFIG		R/W	Coefficient selection for Horizontal weighted binning 0 : Hardware preset values Others : Used HADCOEF0 to HADCOEF8	○
	4	[0]	ManufactureRegister		R/W	Rewrite inhibited	
	5	[0]	X_SP_ELIMINATION		R/W	2/3 subsampling ON/OFF control 0 : 2/3 subsampling OFF 1 : 2/3 subsampling ON	○
	6						
	7	[0]	HDIV_AUTOCKSEL		R/W	Automatic clock control when changing Horizontal subsampling mode 0 : Normal operation 1 : Automatic clock control	
30D6	0	[3:0]	HADCOEF0[0]	00	R/W	・Horizontal weighted binning Horizontal weighted binning coefficient 0	○
	1		HADCOEF0[1]		R/W		
	2		HADCOEF0[2]		R/W		
	3		HADCOEF0[3]		R/W		
	4						
	5						
	6						
	7						
30D7	0	[3:0]	HADCOEF1[0]	00	R/W	・Horizontal weighted binning Horizontal weighted binning coefficient 1	○
	1		HADCOEF1[1]		R/W		
	2		HADCOEF1[2]		R/W		
	3		HADCOEF1[3]		R/W		
	4						
	5						
	6						
	7						
30D8	0	[3:0]	HADCOEF2[0]	00	R/W	・Horizontal weighted binning Horizontal weighted binning coefficient 2	○
	1		HADCOEF2[1]		R/W		
	2		HADCOEF2[2]		R/W		
	3		HADCOEF2[3]		R/W		
	4						
	5						
	6						
	7						
30D9	0	[3:0]]	HADCOEF3[0]	00	R/W	・Horizontal weighted binning Horizontal weighted binning coefficient 3	○
	1		HADCOEF3[1]		R/W		
	2		HADCOEF3[2]		R/W		
	3		HADCOEF3[3]		R/W		
	4						
	5						
	6						
	7						
30DA	0	[3:0]	HADCOEF4[0]	00	R/W	・Horizontal weighted binning Horizontal weighted binning coefficient 4	○
	1		HADCOEF4[1]		R/W		
	2		HADCOEF4[2]		R/W		
	3		HADCOEF4[3]		R/W		
	4						
	5						
	6						
	7						
30DB	0	[3:0]	HADCOEF5[0]	00	R/W	・Horizontal weighted binning Horizontal weighted binning coefficient 5	○
	1		HADCOEF5[1]		R/W		
	2		HADCOEF5[2]		R/W		
	3		HADCOEF5[3]		R/W		
	4						
	5						
	6						
	7						

Address (hex)		Bit	Register Name	Initial values (hex)	R/W	Description	Update Timing
30DC	0	[3:0]	HADCOEF6[0]	00	R/W	・Horizontal weighted binning Horizontal weighted binning coefficient 6	○
	1		HADCOEF6[1]		R/W		
	2		HADCOEF6[2]		R/W		
	3		HADCOEF6[3]		R/W		
	4						
	5						
	6						
	7						
30DD	0	[3:0]	HADCOEF7[0]	00	R/W	・Horizontal weighted binning Horizontal weighted binning coefficient 7	○
	1		HADCOEF7[1]		R/W		
	2		HADCOEF7[2]		R/W		
	3		HADCOEF7[3]		R/W		
	4						
	5						
	6						
	7						
30DE	0	[7:0]	HADCOEF8[0]	00	R/W	Horizontal weighted addition divisor	○
	1		HADCOEF8[1]		R/W		
	2		HADCOEF8[2]		R/W		
	3		HADCOEF8[3]		R/W		
	4		HADCOEF8[4]		R/W		
	5		HADCOEF8[5]		R/W		
	6		HADCOEF8[6]		R/W		
	7		HADCOEF8[7]		R/W		
30DF - 30E7	0	[7:0]	ManufactureRegister	—	—	Rewrite inhibited	—
	1						
	2						
	3						
	4						
	5						
	6						
	7						
30E8	0	[3:0]	ManufactureRegister	0F	R/W	Rewrite inhibited	
	1		ManufactureRegister		R/W		
	2		ManufactureRegister		R/W		
	3		ManufactureRegister		R/W		
	4	[1:0]	CLPOWERMODE[0]		R/W	Column Low power ON/OFF selection 0 : Column Low power OFF (full OFF) 1 : Column Low power ON (Horizontal subsampling linked mode) 2 : Column Low power ON (optional setting mode by register)	○
	5		CLPOWERMODE[1]		R/W		
	6	[1:0]	ManufactureRegister		R/W	Rewrite inhibited	
	7		ManufactureRegister		R/W		
30E9 - 30F5	0	[7:0]	ManufactureRegister	—	—	Rewrite inhibited	—
	1						
	2						
	3						
	4						
	5						
	6						
	7						
30F6	0			20			
	1						
	2						
	3						
	4						
	5	[0]	EBDMASK		R/W	Embedded Data output mask setting 0: Outputs Embedded Data Line 1: Don't output Embedded Data Line	
	6						
	7						
30F7 - 30F8	0	[7:0]	ManufactureRegister	—	—	Rewrite inhibited	—
	1						
	2						
	3						
	4						
	5						
	6						
	7						
30F9	0	[1:0]	XVSLNG[0]	00	R/W	XVS pulse width setting in master mode 0 : 1 line, 1 : 2 line, 2 : 4 line, 3 : Dummy period	
	1		XVSLNG[1]		R/W		
	2	[1:0]	XHSLNG[0]		R/W	XHS pulse width setting in master mode 0 : 4 clocks, 1 : 8 clocks, 2 : 16 clocks, 3 : 32 clocks	
	3		XHSLNG[1]		R/W		
	4						
	5						
	6						
	7						
30FA	0			00			
	1						
	2						
	3						
	4	[0]	XVSINV		R/W	XVS output polarity setting 0 : Low Active 1 : High Active.	
	5	[0]	XHSINV		R/W	XHS output polarity setting 0 : Low Active 1 : High Active Sets in sensor master mode.	
	6						
	7						
30FB	0	[7:0]	ManufactureRegister	—	—	Rewrite inhibited	—
	1						
	2						
	3						
	4						
	5						
	6						
	7						
30FC	0			06			
	1	[0]	ManufactureRegister		R/W	Rewrite inhibited	
	2	[0]	XVSOUTEN		R/W	XVS output setting 0 : Don't output XVS (Fixed XVS output to High) 1 : Outputs XVS. Sets in sensor master mode.	
	3						
	4	[1:0]	ManufactureRegister		R/W	Rewrite inhibited	
	5		ManufactureRegister		R/W		
	6	[0]	ManufactureRegister		R/W	Rewrite inhibited	
	7						
30FD - 30FF	0	[7:0]	ManufactureRegister	—	—	Rewrite inhibited	—
	1						
	2						
	3						
	4						
	5						
	6						
	7						

2-wire serial communication register map (Manufacture specific register 0x3100 to 0x31FF)

Address (hex)		Bit	Register Name	initial values (hex)	RW	Description	Update Timming
3100 - 31FF	0	[7:0]	ManufactureRegister	—	—	Rewrite inhibited	—
	1						
	2						
	3						
	4						
	5						
	6						
	7						

2-wire serial communication register map (Manufacture specific register 0x3200 to 0x32FF)

Address (hex)		Bit	Register Name	initial values (hex)	RW	Description	Update Timming
3200 - 3235	0	[7:0]	ManufactureRegister	—	—	Rewrite inhibited	—
	1						
	2						
	3						
	4						
	5						
	6						
	7						
3236	0	[14:0]	3DADJPCK[0]	00	R/W	3D mode Sensor sync timing setting Set by H direction pixel clock units.	
	1		3DADJPCK[1]		R/W		
	2		3DADJPCK[2]		R/W		
	3		3DADJPCK[3]		R/W		
	4		3DADJPCK[4]		R/W		
	5		3DADJPCK[5]		R/W		
	6		3DADJPCK[6]		R/W		
	7		3DADJPCK[7]		R/W		
3237	0		3DADJPCK[8]	00	R/W		
	1		3DADJPCK[9]		R/W		
	2		3DADJPCK[10]		R/W		
	3		3DADJPCK[11]		R/W		
	4		3DADJPCK[12]		R/W		
	5		3DADJPCK[13]		R/W		
	6		3DADJPCK[14]		R/W		
	7						
3238	0	[15:0]	3DADJLINE[0]	00	R/W	3D mode Sensor sync timing setting Set by H-line units.	
	1		3DADJLINE[1]		R/W		
	2		3DADJLINE[2]		R/W		
	3		3DADJLINE[3]		R/W		
	4		3DADJLINE[4]		R/W		
	5		3DADJLINE[5]		R/W		
	6		3DADJLINE[6]		R/W		
	7		3DADJLINE[7]		R/W		
3239	0		3DADJLINE[8]	00	R/W		
	1		3DADJLINE[9]		R/W		
	2		3DADJLINE[10]		R/W		
	3		3DADJLINE[11]		R/W		
	4		3DADJLINE[12]		R/W		
	5		3DADJLINE[13]		R/W		
	6		3DADJLINE[14]		R/W		
	7		3DADJLINE[15]				
323A - 323F	0	[7:0]	ManufactureRegister	—	—	Rewrite inhibited	—
	1						
	2						
	3						
	4						
	5						
	6						
	7						
3240	0	[1:0]	ManufactureRegister	10	R/W	Rewrite inhibited	
	1						
	2	[1:0]	XVSSEL[0]		R/W	XVS Monitor output setting 0 : Fixed L *When CNBISTEN=1 or OTPTEST=1, Result of Counter BIST or OTP Test is outputted. 1 : Test Monitor Output selected by TESTXVCU 2 : Mechanical shutter Control Pulse Output 3 : Flash Control Pulse Output	
	3		XVSSEL[1]		R/W		
	4						
	5	[0]	ManufactureRegister		R/W	Rewrite inhibited	
	6						
	7						
3241	0	[7:0]	ManufactureRegister	—	—	Rewrite inhibited	—
	1						
	2						
	3						
	4						
	5						
	6						
	7						
3242	0	[7:0]	TESTXVSCU[0]	00	R/W	XVS monitor output pulse selection (Sensor control block)	
	1		TESTXVSCU[1]		R/W		
	2		TESTXVSCU[2]		R/W		
	3		TESTXVSCU[3]		R/W		
	4		TESTXVSCU[4]		R/W		
	5		TESTXVSCU[5]		R/W		
	6		TESTXVSCU[6]		R/W		
	7		TESTXVSCU[7]		R/W		
3243 - 3281	0	[7:0]	ManufactureRegister	—	—	Rewrite inhibited	—
	1						
	2						
	3						
	4						
	5						
	6						
	7						
3282	0	[0]	DPUOFF	00	R/W	DUTOP signal processing function OFF (for test) 0h : Normal operation 1h : All signal processing OFF	
	1						
	2						
	3						
	4						
	5						
	6						
	7						
3283 - 32FF	0	[7:0]	ManufactureRegister	—	—	Rewrite inhibited	—
	1						
	2						
	3						
	4						
	5						
	6						
	7						

2-wire serial communication register map (Manufacture specific register 0x3300 to 0x33FF)

Address (hex)		Bit	Register Name	initial values (hex)	RW	Description	Update Timing
3300	0	[7:0]	ManufactureRegister	—	—	Rewrite inhibited	—
	1						
	2						
	3						
	4						
	5						
	6						
	7						
3301	0	[1:0]	RGLANESEL[0]	01	R/W	Number of output lanes setting. 00: 2 Lane output 01: 1 Lane output 10: Reserved 11: 4 Lane output	○
	1		RGLANESEL[1]		R/W		
	2	[0]	ManufactureRegister		R/W	Rewrite inhibited	
	3	[0]	ManufactureRegister		R/W	Rewrite inhibited	
	4	[1:0]	ManufactureRegister		0	Rewrite inhibited	
	5		ManufactureRegister		0		
	6						
	7	[0]	ManufactureRegister		R/W	Rewrite inhibited	
3302 - 33FF	0	[7:0]	ManufactureRegister	—	—	Rewrite inhibited	—
	1						
	2						
	3						
	4						
	5						
	6						
	7						

2-wire serial communication register map (Manufacture specific register 0x3400 to 0x34FF)

Address (hex)		Bit	Register Name	initial values (hex)	RW	Description	Update Timing
3400 - 34FF	0	[7:0]	ManufactureRegister	—	—	Rewrite inhibited	—
	1						
	2						
	3						
	4						
	5						
	6						
	7						

2-wire serial communication register map (Manufacture specific register 0x3500 to 0x35FF)

Address (hex)		Bit	Register Name	initial values (hex)	RW	Description	Update Timing
3500 - 35FF	0	[7:0]	ManufactureRegister	—	—	Rewrite inhibited	—
	1						
	2						
	3						
	4						
	5						
	6						
	7						

2-wire serial communication register map (Manufacture specific register 0x3600 to 0x36FF)

Address (hex)		Bit	Register Name	initial values (hex)	RW	Description	Update Timing
3600 - 36FF	0	[7:0]	ManufactureRegister	—	—	Rewrite inhibited	—
	1						
	2						
	3						
	4						
	5						
	6						
	7						

Electrical Characteristics

The Electrical Characteristics of the IMX132TQH5-C is shown below

DC Characteristics

Table 44. DC characteristics

Item	Pins	Symbol	Conditions	Min.	Typ.	Max	Unit
Supply voltage	VDDSUBD VDDHCM VDDHSN1,2 VDDHAN VDDHCP	VANA		2.6	2.7	2.9	V
	VDDLCN VDDLSC1,2 VDDLIO1,2	VDIG		1.1	1.2	1.3	V
	VDDMCO	VIF		1.7	1.8	2.9	V
Digital input voltage	XCLR (XSHUTDOWN) SDA SCL XCE INCK (EXTCLK)	VIH		0.7VIF		2.9	V
		VIL				0.3VIF	V
Digital output voltage	SDA XVS	VOH		VIF-0.4			V
		VOL				0.4	V

AC Characteristics

Master Clock Waveform Diagram

INCK (EXTCLK) Square Waveform Input Specifications

Input specifications are shown below when square-wave signal is input directly into the external pin INCK (EXTCLK).

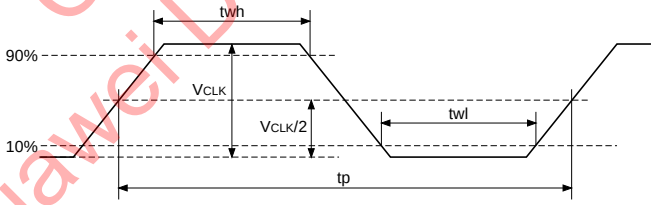


Fig 47. Master Clock Square Waveform Input Diagram

Table 45. Master Clock Square Waveform Input Characteristics

PARAMETER	SYMBOL	MIN.	TYP	MAX.	UNIT
INCK (EXTCLK) clock frequency	f_{SCK}	6	18	60	MHz
INCK (EXTCLK) amplitude	V_{CLK}	1.0	1.8	2.9	V
INCK (EXTCLK) clock period	t_p	166.7	55.0	16.6	ns
INCK (EXTCLK) low level width	t_{wl}	0.4tp		0.6tp	ns
INCK (EXTCLK) high level width	t_{wh}	0.4tp		0.6tp	ns
INCK (EXTCLK) jitter	Tjitter			200	ps

INCK (EXTCLK) Sine Waveform Input Specifications

Input specifications are shown below when sine wave signal is input into INCK (EXTCLK) with AC coupled connection.

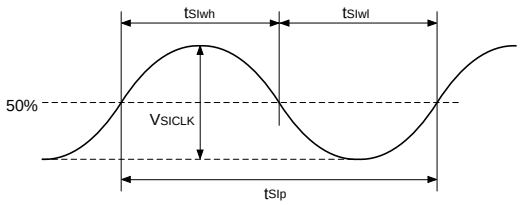


Fig 48. Master Clock Sine Waveform Diagram

Table 46. Master Clock Sine Waveform Input Characteristics

PARAMETER	SYMBOL	MIN.	TYP	MAX.	UNIT
INCK (EXTCLK) clock frequency	f_{SISCK}	6	18	27	MHz
INCK (EXTCLK) amplitude	V_{SICLK}	0.5	1.0	1.2	V
INCK (EXTCLK) clock period	t_{SIp}	166.7	55.0	37.0	ns
INCK (EXTCLK) low level width	t_{SIwl}	0.4tp		0.6tp	ns
INCK (EXTCLK) high level width	t_{SIwh}	0.4tp		0.6tp	ns
INCK (EXTCLK) jitter	Tjitter			200	ps

PLL block characteristics

Electrical characteristics of PLL block is shown below.

Table 47. PLL block characteristics

Item	Min	Typ	Max	Unit	Note
Input frequency range	6.0		60.0	MHz	
Input frequency range of phase comparator	6.0		60.0	MHz	
VCO frequency range	384.0		1000.0	MHz	
Output frequency range	96.0		1000.0	MHz	
Settling time		100.0	200.0	µs	

Definition of settling time of PLL block

After start operation, the oscillation frequency of PLL output transits from 0 Hz to target frequency then gradually become stable. The duration for oscillation frequency becomes within 5 % of the target frequency is defined as “settling time”.

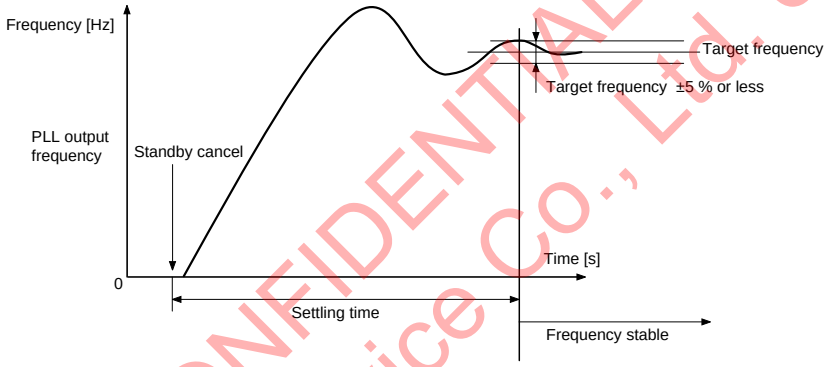


Fig 49. Definition of settling time

2-wire serial communication block characteristics

2-wire serial communication characteristics are shown below.

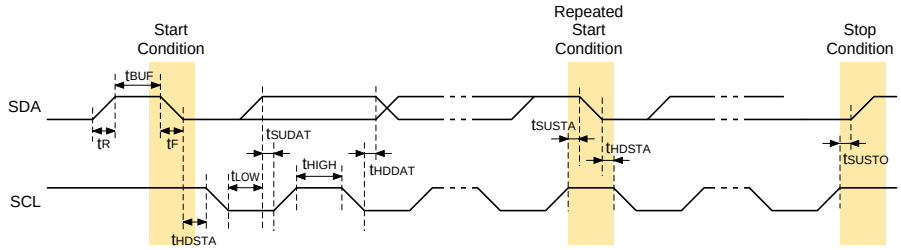


Fig 50. 2-wire serial communication block specification

Table 48. 2-wire serial communication block specification

Parameter	Symbol	Conditions	Min	Max	Unit
Low level input voltage	V_{IL}		-0.3	$0.3V_{IF}$	V
High level input voltage	V_{IH}		$0.7V_{IF}$	2.9	V
Low level output voltage	V_{OL1}	VIF > 2 V,Sink 3 mA	0	0.4	V
	V_{OL2}	VIF < 2 V,Sink 3 mA	0	$0.2\ V_{IF}$	V
High level output voltage	V_{OH}		$0.8V_{IF}$		V
Output fall time	t_{of}	Load 10 pF – 400 pF, 0.7 VIF→0.3 VIF		250	ns
Input current	I_I	0.1 VIF→0.9 VIF	-10	10	µA
SDA I/O capacitance	$C_{I/O}$			8	pF
SCL Input capacitance	C_I			6	pF

Table 49. 2-wire serial communication block AC specification

Parameter	Symbol	Min	Max	Unit
SCL clock frequency	f_{SCL}	0	400	kHz
Rise time (SDA and SCL)	t_R	—	300	ns
Fall time (SDA and SCL)	t_F	—	300	ns
Hold time (start condition)	t_{HDSTA}	0.6	—	µs
Setup time (rep.-start condition)	t_{SUSTA}	0.6	—	µs
Setup time (stop condition)	t_{SUSTO}	0.6	—	µs
Data setup time	t_{SUDAT}	100	—	ns
Data hold time	t_{HDDAT}	0	0.9	µs
Bus free time between Stop and Start	t_{BUF}	1.3		µs
Low period of the SCL clock	t_{LOW}	1.3		µs
High period of the SCL clock	t_{HIGH}	0.6		µs

Current consumption and standby current

Table 50. Current consumption and standby current

(30 frame/s, V_{ANA} = 2.7 V, V_{DIG} = 1.2 V, V_{IF} = 1.8 V, Tj = 60 ˚C)

Item	Symbol	Min.	Typ.	Max.	Unit	Remarks
Current consumption (analog)	I_{ANA}		21	37	mA	
Current consumption (digital)	I_{DIG}		56	85	mA	
Standby current (analog)	I_{STBANA}			37	μA	XCLR (XSHUTDOWN) :High fixed INCK (EXTCLK) :stop
Standby current (digital)	I_{STBDIG}			2100	μA	XCLR (XSHUTDOWN) :High fixed INCK (EXTCLK) :stop
Standby current (IF)	I_{STBIF}			2	μA	XCLR (XSHUTDOWN) :Highfixed INCK (EXTCLK) :stop

(*)Current consumption (IF) is not specified because it is depend on amount of 2-wire serial communication that the host transmits.

Spectral Sensitivity Characteristic

(Excludes neither lens characteristics nor light source characteristics.)

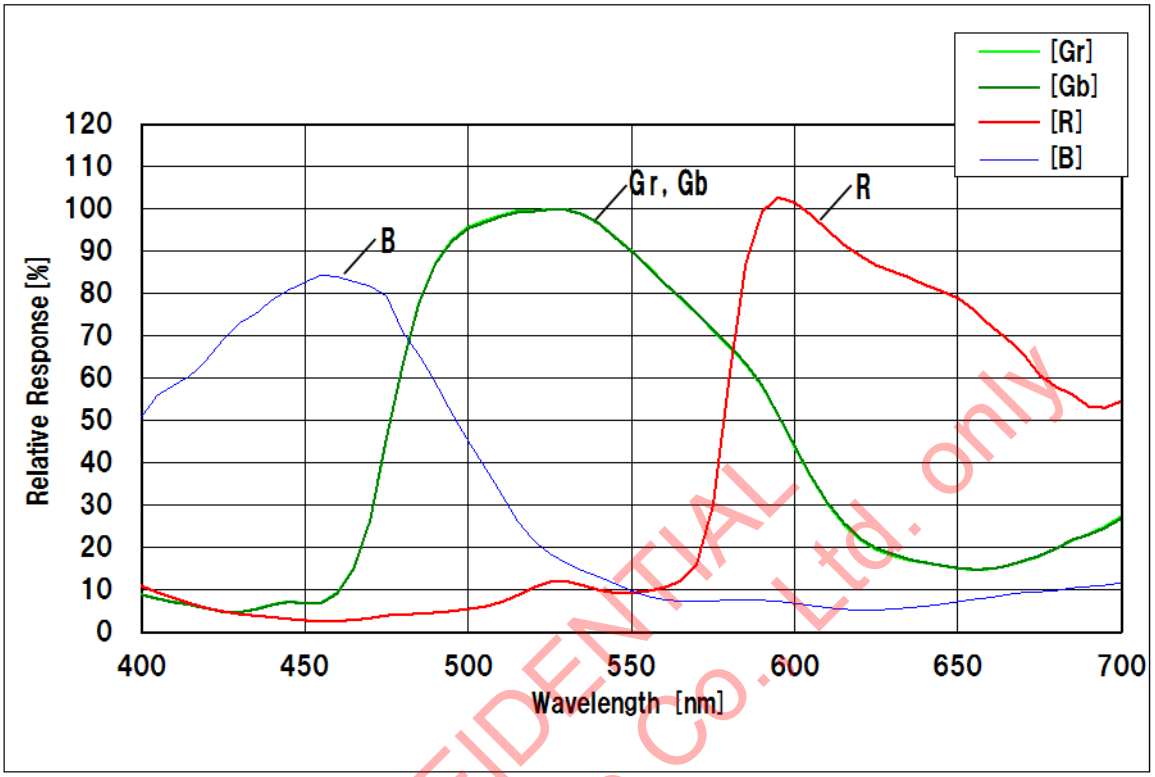


Fig 51. Spectral sensitivity characteristics

Image Sensor Characteristics

Image Sensor Characteristics

Table 51. Image Sensor Characteristics

(30 frame/s, V_{ANA} = 2.7 V, V_{DIG} = 1.2 V, V_{IF} = 1.8 V,Tj = 60 ˚C)

Item	Symbol	Min. *2	Typ. *1	Max. *2	Unit	Range	Measurement method	Remarks
Sensitivity	S	205			LSB	Center	1	1/120 s storage
Sensitivity ratio	RG	0.45	0.51	0.57		Center	2	
	BG	0.40	0.46	0.52				
Saturation signal	Vsat	820			LSB	Zone1	3	
Video signal shading	SH			60	%	Zone2D	4	Design assurance
Dark signal	Vdt			0.5	LSB	Zone2D	5	When operation at 30 frame/s

*1 The above estimated values are calculated based on prototype samples; thus, it does not indicate the center distribution values for the final MP.

*2 The above estimated values are calculated based on prototype samples; variances from testing environment and/or final MP distributions are not considered.

LSB is the abbreviation of Least Significant Bit. 10 bits = 1023 digital is the maximum output code for the output unit. The gain setting (base gain setting) in which the saturation signal output matches with 1023 LSB requires 1.8[dB] when the OB level is 60 LSB (standard recommended value). The data described at this image sensor characteristics are the measurement standard without base gain setting, and indicates the results evaluated with OB as a reference.

Zone Definition of Video Signal Shading

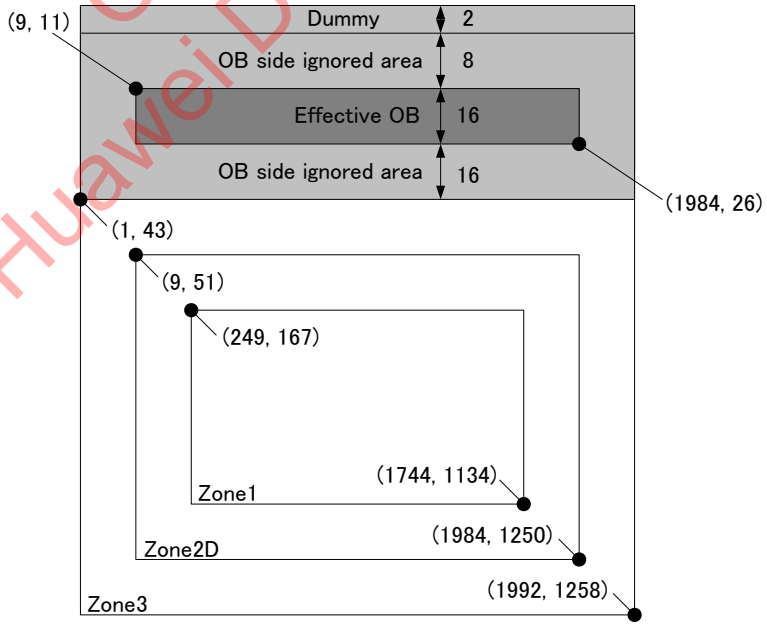


Fig 52. Zone Definition Diagram

Image Sensor Characteristics Measurement Method

Measurement Conditions

The device operation conditions are at the typical values of the bias and clock voltage.

Table 52. Measurement Conditions

Supply voltage	Analog 2.7 V, digital 1.2 V, IF 1.8 V
Clock	INCK (EXTCLK) 18 MHz

In the following measurements, spot pixels are excluded and, unless otherwise specified, the optical black (OB) level is used as the reference for the signal output, which is taken as the value of the Gr, Gb, R and B digital signal outputs of the measurement system.
As an example of 1 LSB, the typical value is 1 LSB ≈ 0.335 mV in all-pixel output 10-bit operation mode. The minimum value is 0.31 mV and the maximum value is 0.36 mV.

Color Coding of this Image Sensor and Readout

The primary color filters of this image sensor are arranged in the layout shown in the figure below. Gr and Gb denote the G signals on the same line as the R signal and the B signal, respectively. The R signal and Gr signal lines and the Gb signal and B signal lines are output successively.
All pixel signals are output successively in a 1/15 s period.

Fig 53. Color coding alignment

Definition of Standard Imaging Conditions

Standard imaging condition I

Use a pattern box (luminance: 706 cd/m2, color temperature of 3200 K halogen source) as a subject. (Pattern for evaluation is not applicable.) Use a testing standard lens with CM500S (t = 1.0 mm) as an IR cut filter and image at F2.8. The luminous intensity to the sensor receiving surface at this point is defined as the standard sensitivity testing luminous intensity.

Standard imaging condition II

A testing lens with CM500S (t = 1.0 mm) is used as an IR cut filter for light source with 3200 K color temperature. The luminous intensity to the sensor receiving surface is adjusted to the luminous intensity level shown in each measurement item by the light source output, lens aperture or storage time control by the electronic shutter.

Standard imaging condition III

A recommended testing lens with CM500S (t = 1.0 mm) is used as an IR cut filter for light source with 3200 K color temperature. The luminous intensity to the sensor receiving surface is adjusted to the luminous intensity level shown in each measurement item by the light source output or storage time control by the electronic shutter.

Measurement method

1.Sensitivity

Set the measurement condition to the standard imaging condition I. After setting the luminous intensity of 10 times that of the standard imaging condition and the electronic shutter mode with a shutter speed of 1/300 s, measure the Gr and Gb signal outputs (VGr, VGb) at the center of imaging area, and substitute the values into the following formula.

$$S = \{ ((VGr + VGb) /2) \times (1/10) \times (300/120) \} \text{ [LSB]}$$

2.Sensitivity ratio

Set the measurement condition to the standard imaging condition II. After adjusting so that the average value of the Gr and Gb signal output is 380LSB, measure the R signal output (VR [LSB]) , the Gr and Gb signal outputs (VGr, VGb [LSB]) and the B signal output (VB [LSB]) at the imaging area Center in frame readout mode, and substitute the values into the following formulas.

$$VG = (VGr + VGb) /2$$

$$RG = VR/VG$$

$$RB = VB/VG$$

3.Saturation signal

Set the measurement condition to the standard imaging condition II. After adjusting the luminous Intensity to 20 times the intensity with the average value of the Gr, Gb signal outputs, 380 [LSB], measure the average value of the Gr, Gb, R and B signal outputs.

4.Video signal shading

Set the measurement condition to the standard imaging condition III. With the lens diaphragm at F2.8, adjust the luminous intensity so that the average value of the Gr and Gb signal outputs is 380 [LSB]. Then measure the maximum value (Gmax [LSB]) and minimum value (Gmin [LSB]) of the Gr and Gb signal outputs, and substitute the values into the following formula.

$$SH = ((Gmax – Gmin) /Gmax) \times 100 [\%]$$

5.Dark signal

Measure the output difference between 1/30 [s] signal output (Va) and 1/15000 or less [s] signal output (Vb) at the device ambient temperature of 60 ˚C and the device in the light-obstructed state, and calculate the signal output at 1/30 [s] storage by them using the following approximate formula. Then, this is Vdt [LSB].

$$Vdt = (Va – Vb) \times (1 / 30) / ((1 / 30) – (1 / 15000)) \approx (Va –Vb) \text{ [LSB]}$$

Spot Pixel Specifications

Table 53. Spot Pixel Specifications
(30 frame/s, VANA = 2.7 V, VDIG = 1.2 V, VIF = 1.8 V, Tj = 60 ˚C)

Type of distortion	Level Note 1)	Maximum distorted pixels in each zone				Measurement method	Remarks
		Zone2D	Zone3	Ineffective OB	Effective OB		
Black or white pixels at high ight	30 % ≤ D	12	No evaluation criteria applied			2	Base gain 1.8[db] Setting Note 2)
White pixels in the dark	28 (LSB) ≤ D	180	No evaluation criteria applied			2	Base gain 1.8[db] Setting 1/30[s] storage Note 2)

Note) 1. D...Spot pixel level.
2. Continuous same color pixels in the horizontal or vertical direction or Oblique direction are NG.
3. The above chart (hereinafter referred to as the “White and Black Pixel Specifications”) is the standard only for sorting image sensor products in this specification book (hereinafter referred to as the “PRODUCTS”) before shipment from a manufacturing factory. Sony Corporation and its distributors (collectively hereinafter referred to as the “Seller”) disclaim and will not assume any liability even if actual number of distorted pixels of the PRODUCTS delivered to you exceeds the maximum number set forth in the White and Black Pixel Specifications. You are solely liable for any claim, damage or liability arising from or in connection with such distorted pixels. If the Seller separately has its own product warranty program for the PRODUCTS (the “Program”), the conditions in this specification book shall prevail over the Program and the Seller shall not assume any liability under the Program to the extent there is contradiction.

Spot Pixel Zone Definition

Zone Definition of Video Signal Shading is applied.

Notice on White Pixels Specifications

After shipment inspection of CMOS image sensors, pixels of CMOS image sensors may be distorted and then distorted pixels may cause white point effects in dark signals in picture images. (Such white point effects shall be hereinafter referred to as "White Pixels.") Cosmic radiation is one of the causes of White Pixels. Unfortunately, it is not possible with current scientific technology for CMOS image sensors to prevent such distorted pixels. It is recommended that when you use CMOS image sensors, you should consider taking measures against White Pixels, such as adoption of automatic compensation systems for White Pixels and establishment of quality assurance standards.
White Pixels may be also caused by alpha radiation, which will be emitted in a process of decay of radioactive isotopes which inevitably exist in the air in minute amounts and may exist in materials or parts of CMOS image sensor devices (e.g. packaging materials, seal glass, wiring materials and IC chips). It is recommended that you should use materials or parts which do not include radioactive isotopes, which are sources of alpha radiation, and consider taking measures, such as adoption of vacuum packaging technologies in order to ensure that the PRODUCTS are not exposed to the air. As the density of radioactive isotopes in the air of the underground space may become thicker than that on the ground, it is highly recommended to ensure the PRODUCTS are not exposed to the air in using or storing the PRODUCTS at the underground space.

[For Your Reference] The Annual number of White Pixels Occurrence Caused by Cosmic Radiation
The data in the below chart shows the estimated annual number of White Pixels occurrence caused by cosmic radiation in a single-story building in Tokyo at an altitude of 0 meters. The data shows estimated number of White Pixels based on records of past field tests calculated taking structures and electrical properties of each device into account. However, the data in the chart is for your reference purpose only, and shall not be construed as part of any CMOS image sensor product specifications which the Seller warrants.

Example of Annual Number of Occurrence

White Pixel Level (in case of integration time = 1/30 s) (Tj = 60 ℃)	Annual number of occurrence
5.6 mV or higher	0.2 pcs
10.0 mV or higher	0.1 pcs
24.0 mV or higher	0.1 pcs
50.0 mV or higher	0 pcs
72.0 mV or higher	0 pcs

Note 1) The above data indicates the number of White Pixels occurrence when a CMOS image sensor is left for a year.

Note 2) The annual number of White Pixels occurrence fluctuates depending on the CMOS image sensor storage environment (such as altitude, geomagnetic latitude and building structure), time (solar activity effects) and so on. Moreover, there may be statistic errors. Please take notice and understand that this is an example of test data with experiments that have being conducted over a specific time period and in a specific environment.

Note 3) This data does not guarantee the upper limits of the annual number of White Pixels occurrence.

Note 4) As this data does not take occurrence of White Pixels caused by alpha radiation into account, White Pixels are likely to occur at higher value than the rate set forth in such data.

For Your Reference:
The annual number of White Pixels occurrence caused by cosmic radiation at an altitude of 3,000 meters will be from 5 to 10 times higher than that at an altitude of 0 meters because of the density of the cosmic rays. In addition, in high latitude geographical areas such as London and New York, the density of cosmic rays increases due to a difference in the geomagnetic density, so the annual number of White Pixels occurrence caused by cosmic radiation in such areas approximately doubles when compared with that in Tokyo.

Measurement Method for Spot Pixels

Measure under the standard imaging condition II.

Spot Pixel Pattern Specifications

Black or white pixels at high light

After adjusting the average value of the Gr/Gb/R/B signal output to 380 LSB, measure the local dip point (black pixel at high light, VXB) and peak point (white pixel at high light, VXK) in the Gr/Gb/R/B signal output Vx (x = Gr/Gb/R/B) , and substitute the values into the following formula.

$$D_K \text{ (White pixel level)} = (\overline{V_{XK}}/\overline{V_X}) \times 100 \text{ [\%]}$$

$$D_B \text{ (Black pixel level)} = (\overline{V_{XB}}/\overline{V_X}) \times 100 \text{ [\%]}$$

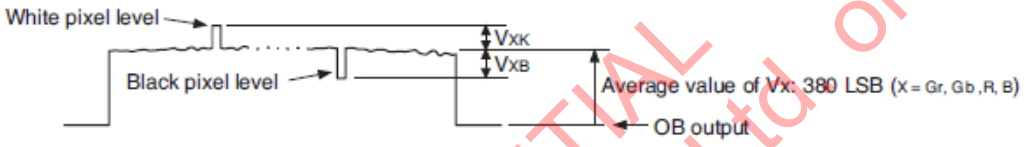


Fig 54. Measurement Method for Spot Pixels

White pixels in the dark

Set the device to a dark setting and measure the local peak point of the signal output waveform using the average value of the dark signal output as a reference.

CRA Characteristics of Recommended Lens

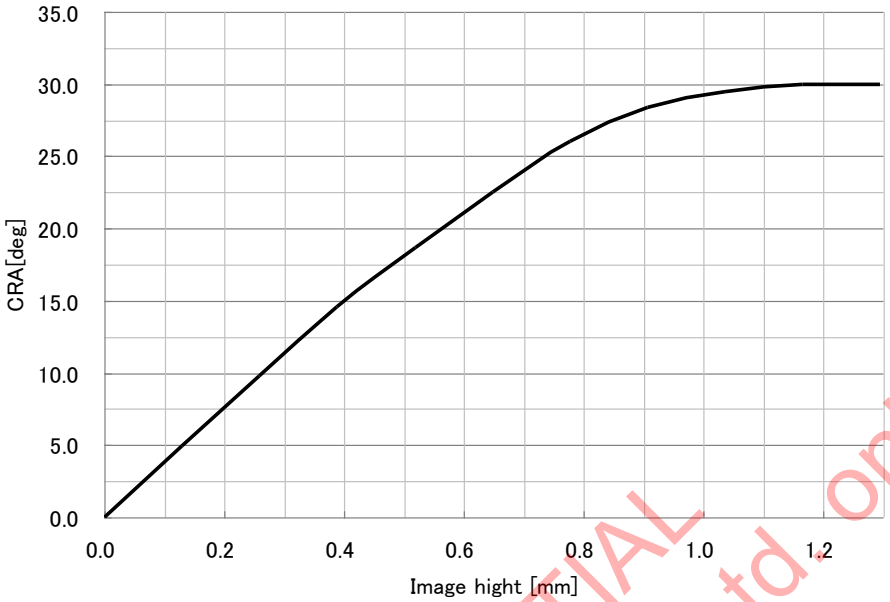


Fig 55. CRA characteristics

Notes On Handling

1. Static charge prevention

Image sensors are easily damaged by static discharge. Before handling be sure to take the following protective measures.

(1) Either handle bare handed or use non-chargeable gloves, clothes or material.
Also use conductive shoes.
(2) Use a wrist strap when handling directly.
(3) Install grounded conductive mats on the floor and working table to prevent the generation of static electricity.
(4) Ionized air is recommended for discharge when handling image sensors.
(5) For the shipment of mounted boards, use boxes treated for the prevention of static charges.

2. Protection from dust and dirt

(1) Perform all work in a clean environment.
(2) Do not touch the chip surface with hand and make any object contact with it.
(3) Keep in a dedicated case to protect from dust and dirt. To prevent dew condensation, preheat or precool when moving to a room with great temperature differences.

3. Others

(1) Do not expose to strong light (sun rays) for long periods, as the color filters of color devices will be discolored.
(2) Exposure to high temperature or humidity will affect the characteristics. Accordingly avoid storage or use in such conditions.
(3) This product is precision optical parts, so care should be taken not to apply excessive mechanical shocks or force.
(4) Reliability assurance of this product should be ignored because it is a bare chip.
(5) Note that imaging characteristics of the sensor may be affected when approaching strong electromagnetic wave or magnetic field during operation.
(6) Note that X-ray inspection may damage characteristics of the sensor.
(7) Note that the sensor may be damaged when using ultraviolet ray and infrared ray on mounting it.
(8) Note that image may be affected by the light leaked to optical black when using an infrared cut filter that has transparency in near infrared ray area during shooting subjects with high luminance.

APPENDIX

Embedded Data Lines

Contents and output sequence of Embedded Data Lines are shown as below.

LINE	Pixel	2Wire Register Name	Output value
1	1	data format	0x0a
1	2	address	0xaa
1	3		0x00
1	4		0xa5
1	5		0x00
1	6	model_id	0x5a
1	7		0x00
1	8		0x5a
1	9		0x91
1	10	revision_number	0x5a
1	11		—
1	12	manufacturer_id	0x5a
1	13		0x0b
1	14	smia_version	0x5a
1	15		0x0a
1	16	frame_count	0x5a
1	17		[7:0]
1	18	pixel_order	0x5a
1	19		[7:0]
1	20	NULL	0x55
1	21		0x07
1	22	data_pedestal	0x5a
1	23		0x00
1	24		0x5a
1	25		[7:0]
1	26	address	0xa5
1	27		0x40
1	28	frame_format_model_type	0x5a
1	29		0x01
1	30	frame_format_model_subtype	0x5a
1	31		0x15
1	32	frame_format_descriptor_0	0x5a
1	33		[15:8]
1	34		0x5a
1	35		[7:0]
1	36	frame_format_descriptor_1	0x5a
1	37		0x10
1	38		0x5a
1	39		0x02
1	40	frame_format_descriptor_2	0x5a
1	41		0x20
1	42		0x5a
1	43		0x04

LINE	Pixel	2Wire Register Name	Output value
1	44	frame_format_descriptor_3	0x5a
1	45		0x40
1	46		0x5a
1	47		[7:0]
1	48	frame_format_descriptor_4	0x5a
1	49		0x20
1	50		0x5a
1	51		0x02
1	52	frame_format_descriptor_5	0x5a
1	53		[15:8]
1	54		0x5a
1	55		[7:0]
1	56	address	0xa5
1	57		0x80
1	58	analogue_gain_capabiltiy	0x5a
1	59		0x00
1	60		0x5a
1	61		{7'd0,[0]}
1	62	address	0xa5
1	63		0x84
1	64	analogue_gain_code_min	0x5a
1	65		0x00
1	66		0x5a
1	67		0x00
1	68	analogue_gain_code_max	0x5a
1	69		0x00
1	70		0x5a
1	71		0xE0
1	72	analogue_gain_code_step	0x5a
1	73		0x00
1	74		0x5a
1	75		0x01
1	76	analogue_gain_type	0x5a
1	77		0x00
1	78		0x5a
1	79		0x00
1	80	analogue_gain_m0	0x5a
1	81		0x00
1	82		0x5a
1	83		0x00

LINE	Pixel	2Wire Register Name	Output
1	84	analogue_gain_c0	0x5a
1	85		0x01
1	86		0x5a
1	87		0x00
1	88	analogue_gain_m1	0x5a
1	89		0xff
1	90		0x5a
1	91		0xff
1	92	analogue_gain_c1	0x5a
1	93		0x01
1	94		0x5a
1	95		0x00
1	96	address	0xa5
1	97		0xc0
1	98	data_format_model_type	0x5a
1	99		0x01
1	100	data_format_model_subtype	0x5a
1	101		0x03
1	102	data_format_descriptor_0	0x5a
1	103		0x08
1	104		0x5a
1	105		0x08
1	106	data_format_descriptor_1	0x5a
1	107		0x0a
1	108		0x5a
1	109		0x08
1	110	data_format_descriptor_2	0x5a
1	111		0x0a
1	112		0x5a
1	113		0x0a
1	114	address	0xaa
1	115		0x01
1	116		0xa5
1	117		0x00
1	118	mode_select	0x5a
1	119		0x01
1	120	image_orientation	0x5a
1	121		{6'd0,[1:0]}
1	122	NULL	0x55
1	123		0x07
1	124	software_reset	0x5a
1	125		{7'd0,[0]}

LINE	Pixel	2Wire Register Name	Output value
1	126	grouped_parameter_hold	0x5a
1	127		{7'd0,[0]}
1	128	mask_corrupted_frames	0x5a
1	129		{7'd0,[0]}
1	130	address	0xa5
1	131		0x10
1	132	CCP2_channel_identifier	0x5a
1	133		{5'd0,[2:0]}
1	134	CCP2_signalling_mode	0x5a
1	135		0x01
1	136	CCP_data_format	0x5a
1	137		[15:8]
1	138		0x5a
1	139		[7:0]
1	140	address	0xa5
1	141		0x20
1	142	gain_mode	0x5a
1	143		{7'd0,[0]}
1	144	address	0xaa
1	145		0x02
1	146		0xa5
1	147		0x02
1	148	coarse_integration_time	0x5a
1	149		[15:8]
1	150		0x5a
1	151		[7:0]
1	152	analogue_gain_code_global	0x5a
1	153		0x00
1	154		0x5a
1	155		[7:0]
1	156	analogue_gain_code_greenR	0x5a
1	157		[15:8]
1	158		0x5a
1	159		[7:0]
1	160	analogue_gain_code_red	0x5a
1	161		[15:8]
1	162		0x5a
1	163		[7:0]
1	164	analogue_gain_code_blue	0x5a
1	165		[15:8]
1	166		0x5a
1	167		[7:0]

LINE	Pixel	2Wire Register Name	Output
1	168	analogue_gain_code_greenB	0x5a
1	169		[15:8]
1	170		0x5a
1	171		[7:0]
1	172	End of Data	0x07
1	173		0x07
1	174		0x07
2	1	Data format	0x0a
2	2	address	0xaa
2	3		0x02
2	4		0xa5
2	5		0x0e
2	6	Digital_gain_greenR	0x5a
2	7		[15:8]
2	8		0x5a
2	9		[7:0]
2	10	Digital_gain_red	0x5a
2	11		[15:8]
2	12		0x5a
2	13		[7:0]
2	14	Digital_gain_blue	0x5a
2	15		[15:8]
2	16		0x5a
2	17		[7:0]
2	18	Digital_gain_greenB	0x5a
2	19		[15:8]
2	20		0x5a
2	21		[7:0]
2	22	address	0xaa
2	23		0x03
2	24		0xa5
2	25		0x00
2	26	vt_pix_clk_div	0x5a
2	27		0x00
2	28		0x5a
2	29		0x0a
2	30	vt_sys_clk_div	0x5a
2	31		0x00
2	32		0x5a
2	33		0x01
2	34	pre_pll_clk_div	0x5a
2	35		0x00
2	36		0x5a
2	37		{4'd0,[3:0]}
2	38	pll_multiplier	0x5a
2	39		0x00
2	40		0x5a
2	41		[7:0]

LINE	Pixel	2Wire Register Name	Output value
2	42	address	0xaa
2	43		0x03
2	44		0xa5
2	45		0x40
2	46	frame_length_lines	0x5a
2	47		[15:8]
2	48		0x5a
2	49		[7:0]
2	50	line_length_pck	0x5a
2	51		[15:8]
2	52		0x5a
2	53		[7:0]
2	54	x_addr_start	0x5a
2	55		{3'd0,[12:8]}
2	56		0x5a
2	57		[7:0]
2	58	y_addr_start	0x5a
2	59		{4'd0,[11:8]}
2	60		0x5a
2	61		[7:0]
2	62	x_addr_end	0x5a
2	63		{3'd0,[12:8]}
2	64		0x5a
2	65		[7:0]
2	66	y_addr_end	0x5a
2	67		{4'd0,[11:8]}
2	68		0x5a
2	69		[7:0]
2	70	x_output_size	0x5a
2	71		{3'd0,[12:8]}
2	72		0x5a
2	73		[7:0]
2	74	y_output_size	0x5a
2	75		{4'd0,[11:8]}
2	76		0x5a
2	77		[7:0]
2	78	address	0xa5
2	79		0x80
2	80	x_even_inc[15:8]	0x5a
2	81		0x00
2	82		0x5a
2	83		{4'd0,[3:0]}
2	84	x_odd_inc[15:8]	0x5a
2	85		0x00
2	86		0x5a
2	87		{4'd0,[3:0]}

LINE	Pixel	2Wire Register Name	Output
2	88	y_even_inc[15:8]	0x5a
2	89		0x00
2	90		0x5a
2	91		{4'd0,[3:0]}
2	92	y_odd_inc[15:8]	0x5a
2	93		0x00
2	94		0x5a
2	95		{4'd0,[3:0]}
2	96	address	0xaa
2	97		0x04
2	98		0xa5
2	99		0x00
2	100	Scaling_mode[15:8]	0x5a
2	101		0x00
2	102		0x5a
2	103		{6'd0,[1:0]}
2	104	Spatial_samiling[15:8]	0x5a
2	105		0x00
2	106		0x5a
2	107		[7:0]
2	108	Scale_m[15:8]	0x5a
2	109		0x00
2	110		0x5a
2	111		[7:0]
2	112	Scale_n[15:8]	0x5a
2	113		0x00
2	114		0x5a
2	115		{3'd0,[4:0]}
2	116	address	0xaa
2	117		0x05
2	118		0xa5
2	119		0x00
2	120	Compession_mode[15:8]	0x5a
2	121		0x00
2	122		0x5a
2	123		{6'd0,[1:0]}
2	124	address	0xaa
2	125		0x06
2	126		0xa5
2	127		0x00
2	128	test_pattern_mode	0x5a
2	129		[15:8]
2	130		0x5a
2	131		[7:0]
2	132	test_data_red	0x5a
2	133		[15:8]
2	134		0x5a
2	135		[7:0]

LINE	Pixel	2Wire Register Name	Output value
2	136	test_data_greenR	0x5a
2	137		[15:8]
2	138		0x5a
2	139		[7:0]
2	140	test_data_blue	0x5a
2	141		[15:8]
2	142		0x5a
2	143		[7:0]
2	144	test_data_greenB	0x5a
2	145		[15:8]
2	146		0x5a
2	147		[7:0]
2	148	horizontal_cursor_width	0x5a
2	149		[15:8]
2	150		0x5a
2	151		[7:0]
2	152	horizontal_cursor_position	0x5a
2	153		[15:8]
2	154		0x5a
2	155		[7:0]
2	156	vertical_cursor_width	0x5a
2	157		[15:8]
2	158		0x5a
2	159		[7:0]
2	160	Vertical_cursor_position	0x5a
2	161		[15:8]
2	162		0x5a
2	163		[7:0]
2	164	End of data	0x07
2	165		0x07
2	166		0x07

Detail description of Sub-sampling and Binning operation

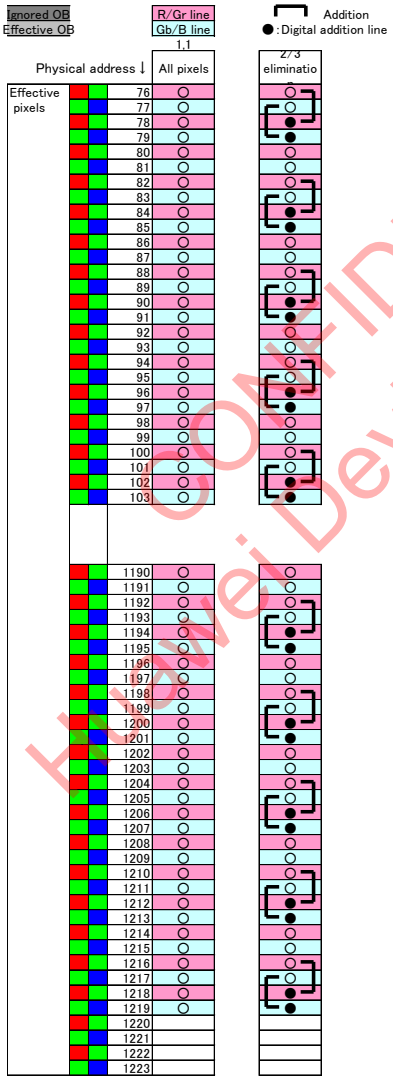
Operation diagram in vertical direction, Image Aspect Ratio of 16:9 (Default readout direction)

【Conversion formula (Vertical direction. normal)】
Physical address of resdout starting position = y_addr_start + 48※
※48 = (Effective and Ignored OB(40)) + (Ignored area of effective pixels(8))

(Example : Image Aspect Ratio of 16:9)
Physical address of resdout starting position = 28 + 48 = 76

【Vertical direction. normal】 **※Hex(Dec)**

Setting register name	Address	Image Aspect Ratio of 16:9		
		All pixels		Special addition average
		(1,1) All pixels		2/3 elimination
image_orientation	0x0101[1]	0x0(0)		0x0(0)
frame_length_lines	0x0340[7:0] 0x0341[7:0]	0x04B0(1200)		0x0320(800)
y_addr_start	0x0346[3:0] 0x0347[7:0]	0x01C(28)		0x01C(28)
y_output_size	0x034E[3:0] 0x034F[7:0]	0x478(1144)		0x2FA(762)
y_even_inc	0x0385[3:0]	0x1(1)		0x2(2)
y_odd_inc	0x0387[3:0]	0x1(1)		0x3(3)
Y_OPBADD_STA	0x3040[5:0]	0x08(8)		0x08(8)
Y_OPBADD_END	0x3041[5:0]	0x17(23)		0x17(23)
Y_AUTOSTART	0x3041[7]	0x1(1)		0x1(1)
VMODEFDS	0x3048[0]	0x0(0)		0x0(0)
VMODEADD	0x3048[1]	0x0(0)		0x1(1)
VMODEADDJMP	0x3048[7:5]	0x0(0)		0x1(1)
Y_SP_ELIMINATION	0x306A[5]	0x0(0)		0x1(1)
RGDAFDSUMEN	0x309B[3]	0x0(0)		0x0(0)
RGV2BITEN	0x309E[2]	0x0(0)		0x1(1)



Operation diagram in horizontal direction, Image Aspect Ratio of 16:9 (Default readout direction)

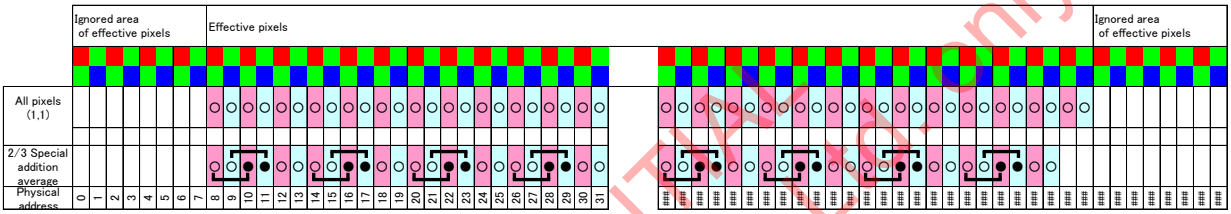
【Conversion formula (Horizontal direction. normal)】
Physical address of resdout starting position = X_ADD_STA + 8※
※8 = Ignored area of effective pixels(8)

(Example : Image Aspect Ratio of 16:9)
Physical address of resdout starting position = 0 + 8 = 8

[Horizontal direction. normal]
※Hex(Dec)

Setting register name	Address	Image Aspect Ratio of 16:9	
		All pixels (1,1)	2/3 Special addition average (2,3)
image_orientation	0x0101[7:0]	0(0)	0(0)
line_length_pck	0x0342[7:0] 0x0343[7:0]	8CA(2250)	D2F(3375)
x_addr_start	0x0344[7:0] 0x0345[7:0]	0(0)	0(0)
x_output_size	0x034C[7:0] 0x034D[7:0]	7B8(1976)	524(1316)
x_even_inc	0x0381[3:0]	1(1)	2(2)
x_odd_inc	0x0383[3:0]	1(1)	3(3)
HADDEN	0x30D5[0]	0(0)	1(1)
HADDMODE	0x30D5[1]	0(0)	0(0)
HADCONFIG	0x30D5[3]	0(0)	0(0)
X_SP_ELIMINATION	0x30D5[5]	0(0)	1(1)
HADCOEF0	0x30D6[7:0]	0(0)	0(0)
HADCOEF1	0x30D7[7:0]	0(0)	0(0)
HADCOEF2	0x30D8[7:0]	0(0)	0(0)
HADCOEF3	0x30D9[7:0]	0(0)	0(0)
HADCOEF8	0x30DE[7:0]	0(0)	0(0)
CLPOWERMODE	0x30E8[5:4]	0(0)	0(0)

R/Gb line
Gr/B line
Addition
●:Horizontal addition pixel



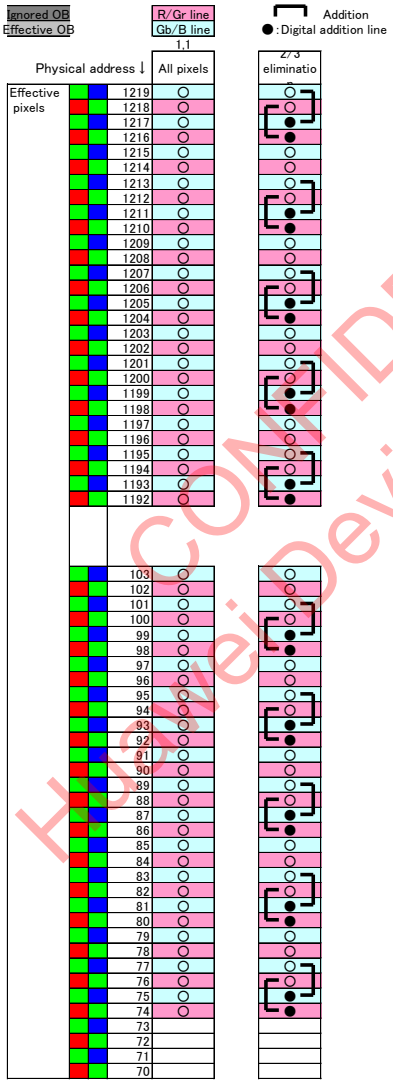
Operation diagram in vertical direction, Image Aspect Ratio of 16:9 (Flipped readout direction)

【Conversion formula (Vertical direction, inverted)】
Physical address of resdout starting position = y_addr_end + 48※
※48 = (Effective and Ignored OB(40)) + (Ignored area of effective pixels(8))

(Example : Image Aspect Ratio of 16:9)
Physical address of resdout starting position = 1171 + 48 = 1219

【Vertical direction, inverted】 **※Hex(Dec)**

Setting register name	Address	Image Aspect Ratio of 16:9		
		All pixels		Special addition average
		(1,1)	All pixels	2/3 elimination
image_orientation	0x0101[1]		0x1(1)	0x1(1)
frame_length_lines	0x0340[7:0] 0x0341[7:0]		0x04B0(1200)	0x0320(800)
y_addr_end	0x034A[3:0] 0x034B[7:0]		0x493(1171)	0x493(1171)
y_output_size	0x034E[3:0] 0x034F[7:0]		0x478(1144)	0x2FA(762)
y_even_inc	0x0385[3:0]		0x1(1)	0x2(2)
y_odd_inc	0x0387[3:0]		0x1(1)	0x3(3)
Y_OPBADD_STA	0x3040[5:0]		0x08(8)	0x08(8)
Y_OPBADD_END	0x3041[5:0]		0x17(23)	0x17(23)
Y_AUTOSTART	0x3041[7]		0x1(1)	0x1(1)
VMODEFDS	0x3048[0]		0x0(0)	0x0(0)
VMODEADD	0x3048[1]		0x0(0)	0x1(1)
VMODEADDJMP	0x3048[7:5]		0x0(0)	0x1(1)
Y_SP_ELIMINATION	0x306A[5]		0x0(0)	0x1(1)
RGDAFDSUMEN	0x309B[3]		0x0(0)	0x0(0)
RGV2BITEN	0x309E[2]		0x0(0)	0x1(1)



Operation diagram in horizontal direction, Image Aspect Ratio of 16:9 (Flipped readout direction)

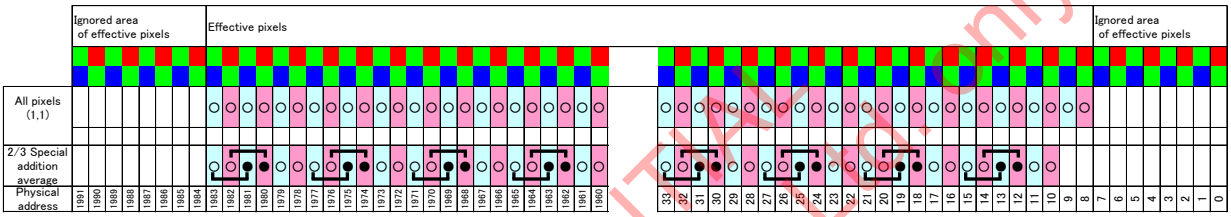
【Conversion formula (Horizontal direction. inverted)】
Physical address of resdout starting position = X_ADD_END + 8※
※8 = Ignored area of effective pixels(8)

(Example : Image Aspect Ratio of 16:9)
Physical address of resdout starting position = 1975 + 8 = 1983

【Horizontal direction. inverted】
※Hex(Dec)

Setting register name	Address	Image Aspect Ratio of 16:9	
		All pixels (1,1)	2/3 Special addition average (2,3)
image_orientation	0x0101[7:0]	1(1)	1(1)
line_length_pck	0x0342[7:0] 0x0343[7:0]	8CA(2250)	D2F(3375)
x_addr_end	0x0348[7:0] 0x0349[7:0]	7B7(1975)	7B7(1975)
x_output_size	0x034C[7:0] 0x034D[7:0]	7B8(1976)	524(1316)
x_even_inc	0x0381[3:0]	1(1)	2(2)
x_odd_inc	0x0383[3:0]	1(1)	3(3)
HADDEN	0x30D5[0]	0(0)	1(1)
HADDMODE	0x30D5[1]	0(0)	0(0)
HADCONFIG	0x30D5[3]	0(0)	0(0)
X_SP_ELIMINATION	0x30D5[5]	0(0)	1(1)
HADCOEF0	0x30D6[7:0]	0(0)	0(0)
HADCOEF1	0x30D7[7:0]	0(0)	0(0)
HADCOEF2	0x30D8[7:0]	0(0)	0(0)
HADCOEF3	0x30D9[7:0]	0(0)	0(0)
HADCOEF8	0x30DE[7:0]	0(0)	0(0)
CLPOWERMODE	0x30E8[5:4]	0(0)	0(0)

R/Gb line
Gr/B line
Addition
●:Horizontal addition pixel



Operation diagram in vertical direction, Image Aspect Ratio of 4:3 (Default readout direction)

【Conversion formula (Vertical direction, normal)】
Physical address of resdout starting position = y_addr_start + 48※
※48 = (Effective and Ignored OB(40)) + (Ignored area of effective pixels(8))

(Example : Image Aspect Ratio of 4:3)
Physical address of resdout starting position = 28 + 48 = 76

[Vertical direction, normal] **※Hex(Dec)**

Setting register name	Address	Image Aspect Ratio of 4:3 Elimination (1/3)	1/2 elimination	(3,3)	1/3 elimination	(5,3)	1/4 elimination	(5,7)	1/6 elimination	(9,7)	1/8 elimination
image_orientation	0x0101[1:0]	0x0(0)		0x0(0)		0x0(0)		0x0(0)		0x0(0)	
frame_length_lines	0x0340[7:0] 0x0341[7:0]	0x0258(600)		0x0190(400)		0x012C(300)		0x00C8(200)		0x0098(152)	
y_addr_start	0x0346[3:0] 0x0347[7:0]	0x01C(28)		0x01E(30)		0x01C(28)		0x01E(30)		0x020(32)	
y_output_size	0x034E[3:0] 0x034F[7:0]	0x23C(572)		0x17C(380)		0x11E(286)		0x0BE(190)		0x08E(142)	
y_even_inc	0x0385[3:0]	0x1(1)		0x3(3)		0x5(5)		0x5(5)		0x9(9)	
y_odd_inc	0x0387[3:0]	0x3(3)		0x3(3)		0x3(3)		0x7(7)		0x7(7)	
Y_OPBADD_STA	0x3040[5:0]	0x08(8)		0x08(8)		0x08(8)		0x08(8)		0x08(8)	
Y_OPBADD_END	0x3041[5:0]	0x17(23)		0x17(23)		0x17(23)		0x13(19)		0x17(23)	
Y_AUTOSTART	0x3041[7]	0x1(1)		0x1(1)		0x1(1)		0x1(1)		0x1(1)	
VMODEFDS	0x3048[0]	0x0(0)		0x0(0)		0x0(0)		0x0(0)		0x0(0)	
VMODEADD	0x3048[1]	0x0(0)		0x0(0)		0x0(0)		0x0(0)		0x0(0)	
VMODEADDJMP	0x3048[7:5]	0x0(0)		0x0(0)		0x0(0)		0x0(0)		0x0(0)	
Y_SP_ELIMINATION	0x306A[5]	0x0(0)		0x0(0)		0x0(0)		0x0(0)		0x0(0)	
RGDAFDSUMEN	0x309B[3]	0x0(0)		0x0(0)		0x0(0)		0x0(0)		0x0(0)	
RGV2BITEN	0x309E[2]	0x0(0)		0x0(0)		0x0(0)		0x0(0)		0x0(0)	

Image Aspect Ratio of 4:3 Vertical digital addition average	(1,3)	1/2 elimination	(3,3)	1/3 elimination	(5,3)	1/4 elimination	(5,7)	1/6 elimination	(9,7)	1/8 elimination
	0x0(0)		0x0(0)		0x0(0)		0x0(0)		0x0(0)	
	0x0258(600)		0x0190(400)		0x012C(300)		0x00C8(200)		0x0098(152)	
	0x01C(28)		0x01E(30)		0x01C(28)		0x01E(30)		0x020(32)	
	0x23C(572)		0x17C(380)		0x11E(286)		0x0BE(190)		0x08E(142)	
	0x1(1)		0x3(3)		0x5(5)		0x5(5)		0x9(9)	
	0x3(3)		0x3(3)		0x3(3)		0x7(7)		0x7(7)	
	0x08(8)		0x08(8)		0x08(8)		0x08(8)		0x08(8)	
	0x17(23)		0x17(23)		0x17(23)		0x13(19)		0x17(23)	
	0x1(1)		0x1(1)		0x1(1)		0x1(1)		0x1(1)	
	0x0(0)		0x0(0)		0x0(0)		0x0(0)		0x0(0)	
	0x1(1)		0x1(1)		0x1(1)		0x1(1)		0x1(1)	
	0x1(1)		0x1(1)		0x1(1)		0x1(1)		0x1(1)	
	0x0(0)		0x0(0)		0x0(0)		0x0(0)		0x0(0)	
	0x0(0)		0x0(0)		0x0(0)		0x0(0)		0x0(0)	
	0x1(1)		0x1(1)		0x1(1)		0x1(1)		0x1(1)	

Image Aspect Ratio of 4:3 Vertical analog addition average	(1,3)	1/2 elimination	(5,3)	1/4 elimination	(9,7)	1/8 elimination
	0x0(0)		0x0(0)		0x0(0)	
	0x0258(600)		0x012C(300)		0x0098(152)	
	0x01C(28)		0x01C(28)		0x020(32)	
	0x23C(572)		0x11E(286)		0x08E(142)	
	0x1(1)		0x5(5)		0x9(9)	
	0x3(3)		0x3(3)		0x7(7)	
	0x08(8)		0x08(8)		0x08(8)	
	0x17(23)		0x17(23)		0x17(23)	
	0x1(1)		0x1(1)		0x1(1)	
	0x1(1)		0x1(1)		0x1(1)	
	0x0(0)		0x0(0)		0x0(0)	
	0x0(0)		0x0(0)		0x0(0)	
	0x1(1)		0x1(1)		0x1(1)	
	0x0(0)		0x0(0)		0x0(0)	

Image Aspect Ratio of 4:3 Vertical digital + analog addition average	(5,3)	1/4 elimination	(9,7)	1/8 elimination
	0x0(0)		0x0(0)	
	0x012C(300)		0x0098(152)	
	0x01C(28)		0x020(32)	
	0x11E(286)		0x08E(142)	
	0x5(5)		0x9(9)	
	0x3(3)		0x7(7)	
	0x08(8)		0x08(8)	
	0x17(23)		0x17(23)	
	0x1(1)		0x1(1)	
	0x1(1)		0x1(1)	
	0x0(0)		0x0(0)	
	0x2(2)		0x2(2)	
	0x0(0)		0x0(0)	
	0x1(1)		0x1(1)	
	0x1(1)		0x1(1)	

Operation diagram in horizontal direction, Image Aspect Ratio of 4:3 (Default readout direction)

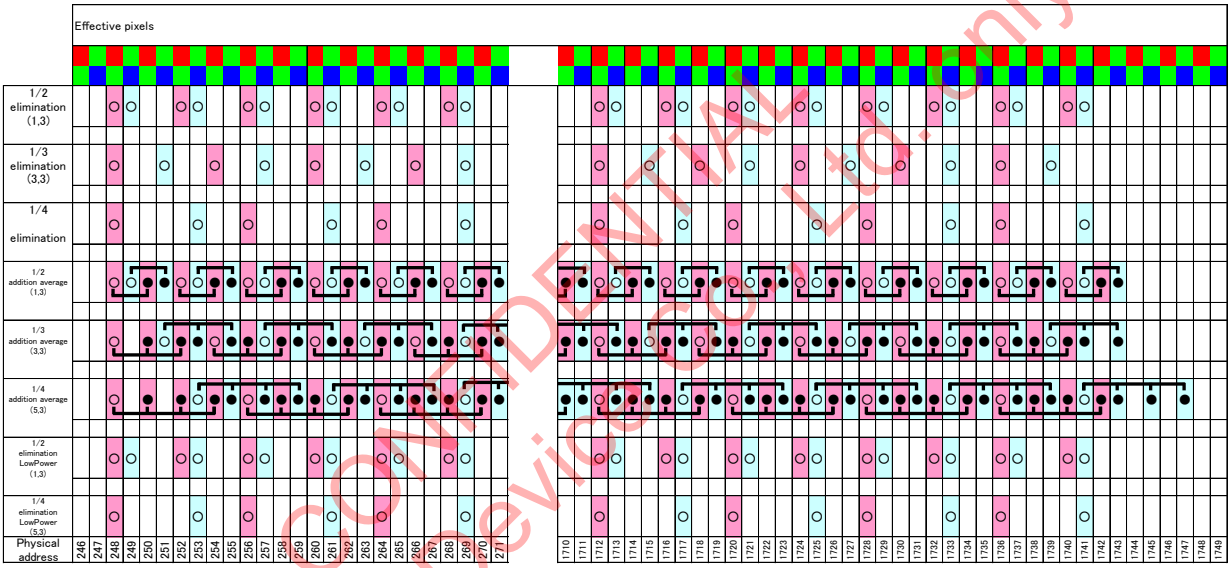
【Conversion formula (Horizontal direction. normal)】
Physical address of resdout starting position = X_ADD_STA + 8※
※8 = Ignored area of effective pixels(8)

(Example : Image Aspect Ratio of 4:3)
Physical address of resdout starting position = 240 + 8 = 248

[Horizontal direction. normal]
※Hex(Dec)

Setting register name	Address	Image Aspect Ratio of 4:3							
		1/2 elimination (1,3)	1/3 elimination (3,3)	1/4 elimination (5,3)	1/2 addition average (1,3)	1/3 addition average (3,3)	1/4 addition average (5,3)	1/2 elimination LowPower (1,3)	1/4 elimination LowPower (5,3)
image_orientation	0x0101[7:0]	0(0)	0(0)	0(0)	0(0)	0(0)	0(0)	0(0)	0(0)
line_length_pck	0x0342[7:0] 0x0343[7:0]	8CA(2250)	8CA(2250)	8CA(2250)	8CA(2250)	8CA(2250)	8CA(2250)	8CA(2250)	8CA(2250)
x_addr_start	0x0344[7:0] 0x0345[7:0]	F0(240)	F0(240)	F0(240)	F0(240)	F0(240)	F0(240)	F0(240)	F0(240)
x_output_size	0x034C[7:0] 0x034D[7:0]	2EC(748)	1F2(498)	176(374)	2EC(748)	1F2(498)	176(374)	2EC(748)	176(374)
x_even_inc	0x0381[3:0]	1(1)	3(3)	5(5)	1(1)	3(3)	5(5)	1(1)	5(5)
x_odd_inc	0x0383[3:0]	3(3)	3(3)	3(3)	3(3)	3(3)	3(3)	3(3)	3(3)
HADDEN	0x30D5[0]	0(0)	0(0)	0(0)	1(1)	1(1)	1(1)	0(0)	0(0)
HADDMODE	0x30D5[1]	0(0)	0(0)	0(0)	0(0)	0(0)	0(0)	0(0)	0(0)
HADCONFIG	0x30D5[3]	0(0)	0(0)	0(0)	1(1)	1(1)	1(1)	0(0)	0(0)
X_SP_ELIMINATION	0x30D5[5]	0(0)	0(0)	0(0)	0(0)	0(0)	0(0)	0(0)	0(0)
HADCOEF0	0x30D6[7:0]	0(0)	0(0)	0(0)	1(1)	0(0)	0(0)	0(0)	0(0)
HADCOEF1	0x30D7[7:0]	0(0)	0(0)	0(0)	1(1)	0(0)	0(0)	0(0)	0(0)
HADCOEF2	0x30D8[7:0]	0(0)	0(0)	0(0)	0(0)	0(0)	0(0)	0(0)	0(0)
HADCOEF3	0x30D9[7:0]	0(0)	0(0)	0(0)	0(0)	0(0)	0(0)	0(0)	0(0)
HADCOEF8	0x30DE[7:0]	0(0)	0(0)	0(0)	2(2)	3(3)	4(4)	0(0)	0(0)
CLPOWERMODE	0x30E8[5:4]	0(0)	0(0)	0(0)	0(0)	0(0)	0(0)	1(1)	1(1)

R/Gb line
Gr/B line
Addition
●:Horizontal addition pixel



Operation diagram in vertical direction, Image Aspect Ratio of 4:3 (Flipped readout direction)

【Conversion formula (Vertical direction, inverted)】
Physical address of readout starting position = y_addr_end + 48※
※48 = (Effective and Ignored OB(40)) + (Ignored area of effective pixels(8))

(Example : Image Aspect Ratio of 4:3)
Physical address of readout starting position = 1171 + 48 = 1219

【Vertical direction, inverted】 **※Hex(Dec)**

Setting register name	Address	Image Aspect Ratio of 4:3 Elimination							
		(1,3)	1/2 elimination	(3,3)	1/3 elimination	(5,3)	1/4 elimination	(5,7)	1/6 elimination	(9,7)	1/8 elimination
image_orientation	0x0101[1:0]		0x1(1)		0x1(1)		0x1(1)		0x1(1)		0x1(1)
frame_length_lines	0x0340[7:0] 0x0341[7:0]		0x0258(600)		0x01960(400)		0x012C(300)		0x00C8(200)		0x0098(152)
y_addr_end	0x034A[3:0] 0x034B[7:0]		0x493(1171)		0x491(1169)		0x493(1171)		0x491(1169)		0x48F(1167)
y_output_size	0x034E[3:0] 0x034F[7:0]		0x23C(572)		0x17C(380)		0x11E(286)		0x0BE(190)		0x08E(142)
y_even_inc	0x0385[3:0]		0x1(1)		0x3(3)		0x5(5)		0x5(5)		0x9(9)
y_odd_inc	0x0387[3:0]		0x3(3)		0x3(3)		0x3(3)		0x7(7)		0x7(7)
Y_OPBADD_STA	0x3040[5:0]		0x08(8)		0x08(8)		0x08(8)		0x0C(12)		0x08(8)
Y_OPBADD_END	0x3041[5:0]		0x17(23)		0x17(23)		0x17(23)		0x17(23)		0x17(23)
Y_AUTOSTART	0x3041[7]		0x1(1)		0x1(1)		0x1(1)		0x1(1)		0x1(1)
VMODEFDS	0x3048[0]		0x0(0)		0x0(0)		0x0(0)		0x0(0)		0x0(0)
VMODEADD	0x3048[1]		0x0(0)		0x0(0)		0x0(0)		0x0(0)		0x0(0)
VMODEADDJMP	0x3048[7:5]		0x0(0)		0x0(0)		0x0(0)		0x0(0)		0x0(0)
Y_SP_ELIMINATION	0x306A[5]		0x0(0)		0x0(0)		0x0(0)		0x0(0)		0x0(0)
RGDAFDSUMEN	0x309B[3]		0x0(0)		0x0(0)		0x0(0)		0x0(0)		0x0(0)
RGV2BITEN	0x309E[2]		0x0(0)		0x0(0)		0x0(0)		0x0(0)		0x0(0)

Setting register name	Address	Image Aspect Ratio of 4:3 Vertical digital addition average							
		(1,3)	1/2 elimination	(3,3)	1/3 elimination	(5,3)	1/4 elimination	(5,7)	1/6 elimination	(9,7)	1/8 elimination
image_orientation	0x0101[1:0]		0x1(1)		0x1(1)		0x1(1)		0x1(1)		0x1(1)
frame_length_lines	0x0340[7:0] 0x0341[7:0]		0x0258(600)		0x01960(400)		0x012C(300)		0x00C8(200)		0x0098(152)
y_addr_end	0x034A[3:0] 0x034B[7:0]		0x493(1171)		0x491(1169)		0x493(1171)		0x491(1169)		0x48F(1167)
y_output_size	0x034E[3:0] 0x034F[7:0]		0x23C(572)		0x17C(380)		0x11E(286)		0x0BE(190)		0x08E(142)
y_even_inc	0x0385[3:0]		0x1(1)		0x3(3)		0x5(5)		0x5(5)		0x9(9)
y_odd_inc	0x0387[3:0]		0x3(3)		0x3(3)		0x3(3)		0x7(7)		0x7(7)
Y_OPBADD_STA	0x3040[5:0]		0x08(8)		0x08(8)		0x08(8)		0x0C(12)		0x08(8)
Y_OPBADD_END	0x3041[5:0]		0x17(23)		0x17(23)		0x17(23)		0x17(23)		0x17(23)
Y_AUTOSTART	0x3041[7]		0x1(1)		0x1(1)		0x1(1)		0x1(1)		0x1(1)
VMODEFDS	0x3048[0]		0x0(0)		0x0(0)		0x0(0)		0x0(0)		0x0(0)
VMODEADD	0x3048[1]		0x1(1)		0x1(1)		0x1(1)		0x1(1)		0x1(1)
VMODEADDJMP	0x3048[7:5]		0x0(0)		0x0(0)		0x0(0)		0x0(0)		0x0(0)
Y_SP_ELIMINATION	0x306A[5]		0x0(0)		0x0(0)		0x0(0)		0x0(0)		0x0(0)
RGDAFDSUMEN	0x309B[3]		0x0(0)		0x0(0)		0x0(0)		0x0(0)		0x0(0)
RGV2BITEN	0x309E[2]		0x1(1)		0x1(1)		0x1(1)		0x1(1)		0x1(1)

Setting register name	Address	Image Aspect Ratio of 4:3 Vertical analog addition average					
		(1,3)	1/2 elimination	(5,3)	1/4 elimination	(9,7)	1/8 elimination
image_orientation	0x0101[1:0]		0x1(1)		0x1(1)		0x1(1)
frame_length_lines	0x0340[7:0] 0x0341[7:0]		0x0258(600)		0x012C(300)		0x0098(152)
y_addr_end	0x034A[3:0] 0x034B[7:0]		0x493(1171)		0x493(1171)		0x48F(1167)
y_output_size	0x034E[3:0] 0x034F[7:0]		0x23C(572)		0x11E(286)		0x08E(142)
y_even_inc	0x0385[3:0]		0x1(1)		0x5(5)		0x9(9)
y_odd_inc	0x0387[3:0]		0x3(3)		0x3(3)		0x7(7)
Y_OPBADD_STA	0x3040[5:0]		0x08(8)		0x08(8)		0x08(8)
Y_OPBADD_END	0x3041[5:0]		0x17(23)		0x17(23)		0x17(23)
Y_AUTOSTART	0x3041[7]		0x1(1)		0x1(1)		0x1(1)
VMODEFDS	0x3048[0]		0x1(1)		0x1(1)		0x1(1)
VMODEADD	0x3048[1]		0x0(0)		0x0(0)		0x0(0)
VMODEADDJMP	0x3048[7:5]		0x0(0)		0x0(0)		0x0(0)
Y_SP_ELIMINATION	0x306A[5]		0x0(0)		0x0(0)		0x0(0)
RGDAFDSUMEN	0x309B[3]		0x1(1)		0x1(1)		0x1(1)
RGV2BITEN	0x309E[2]		0x0(0)		0x0(0)		0x0(0)

Setting register name	Address	Image Aspect Ratio of 4:3 Vertical digital + analog addition average			
		(5,3)	1/4 elimination	(9,7)	1/8 elimination
image_orientation	0x0101[1:0]		0x1(1)		0x1(1)
frame_length_lines	0x0340[7:0] 0x0341[7:0]		0x012C(300)		0x0098(152)
y_addr_end	0x034A[3:0] 0x034B[7:0]		0x493(1171)		0x48F(1167)
y_output_size	0x034E[3:0] 0x034F[7:0]		0x11E(286)		0x08E(142)
y_even_inc	0x0385[3:0]		0x5(5)		0x9(9)
y_odd_inc	0x0387[3:0]		0x3(3)		0x7(7)
Y_OPBADD_STA	0x3040[5:0]		0x08(8)		0x08(8)
Y_OPBADD_END	0x3041[5:0]		0x17(23)		0x17(23)
Y_AUTOSTART	0x3041[7]		0x1(1)		0x1(1)
VMODEFDS	0x3048[0]		0x1(1)		0x1(1)
VMODEADD	0x3048[1]		0x1(1)		0x1(1)
VMODEADDJMP	0x3048[7:5]		0x2(2)		0x2(2)
Y_SP_ELIMINATION	0x306A[5]		0x0(0)		0x0(0)
RGDAFDSUMEN	0x309B[3]		0x1(1)		0x1(1)
RGV2BITEN	0x309E[2]		0x1(1)		0x1(1)

Operation diagram in horizontal direction, Image Aspect Ratio of 4:3 (Flipped readout direction)

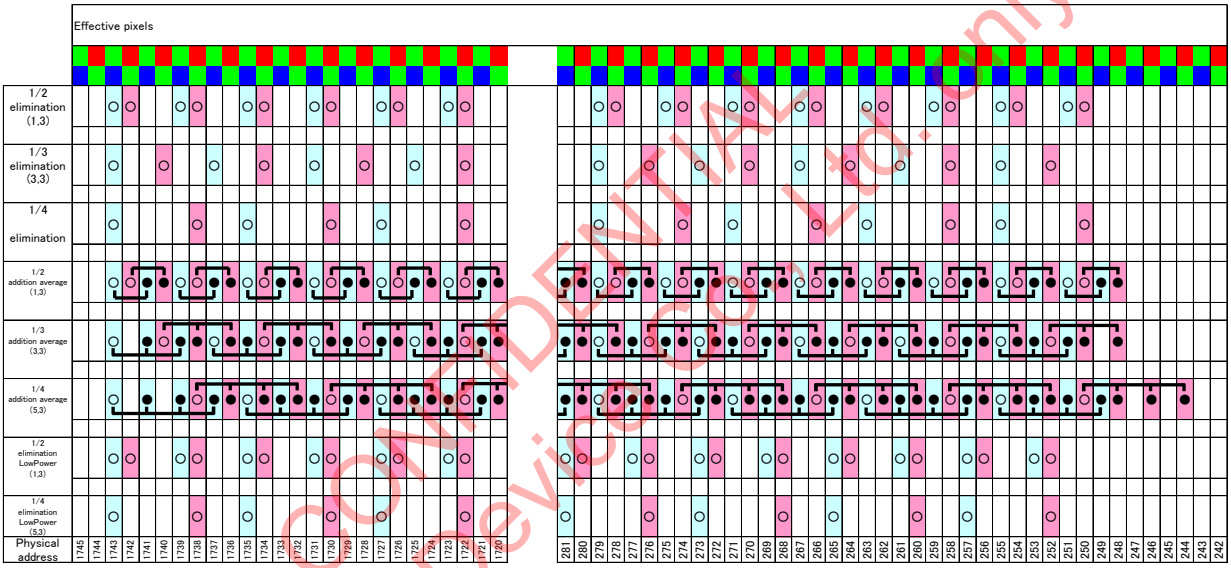
【Conversion formula (Horizontal direction. normal)】
Physical address of resdout starting position = X_ADD_END + 8※
※8 = Ignored area of effective pixels(8)

(Example : Image Aspect Ratio of 4:3)
Physical address of resdout starting position = 1735 + 8 = 1743

【Horizontal direction. inverted】
※Hex(Dec)

Setting register name	Address	Image Aspect Ratio of 4:3							
		1/2 elimination (1,3)	1/3 elimination (3,3)	1/4 elimination (5,3)	1/2 addition average (1,3)	1/3 addition average (3,3)	1/4 addition average (5,3)	1/2 elimination LowPower (1,3)	1/4 elimination LowPower (5,3)
image_orientation	0x0101[7:0]	1(1)	1(1)	1(1)	1(1)	1(1)	1(1)	1(1)	1(1)
line_length_pck	0x0342[7:0] 0x0343[7:0]	8CA(2250)	8CA(2250)	8CA(2250)	8CA(2250)	8CA(2250)	8CA(2250)	8CA(2250)	8CA(2250)
x_addr_end	0x0348[7:0] 0x0349[7:0]	6C7(1735)	6C7(1735)	6C7(1735)	6C7(1735)	6C7(1735)	6C7(1735)	6C7(1735)	6C7(1735)
x_output_size	0x034C[7:0] 0x034D[7:0]	2EC(748)	1F2(498)	176(374)	2EC(748)	1F2(498)	176(374)	2EC(748)	176(374)
x_even_inc	0x0381[3:0]	1(1)	3(3)	5(5)	1(1)	3(3)	5(5)	1(1)	5(5)
x_odd_inc	0x0383[3:0]	3(3)	3(3)	3(3)	3(3)	3(3)	3(3)	3(3)	3(3)
HADDEN	0x30D5[0]	0(0)	0(0)	0(0)	1(1)	1(1)	1(1)	0(0)	0(0)
HADDMODE	0x30D5[1]	0(0)	0(0)	0(0)	0(0)	0(0)	0(0)	0(0)	0(0)
HADCONFIG	0x30D5[3]	0(0)	0(0)	0(0)	1(1)	1(1)	1(1)	0(0)	0(0)
X_SP_ELIMINATION	0x30D5[5]	0(0)	0(0)	0(0)	0(0)	0(0)	0(0)	0(0)	0(0)
HADCOEF0	0x30D6[7:0]	0(0)	0(0)	0(0)	1(1)	0(0)	0(0)	0(0)	0(0)
HADCOEF1	0x30D7[7:0]	0(0)	0(0)	0(0)	1(1)	0(0)	0(0)	0(0)	0(0)
HADCOEF2	0x30D8[7:0]	0(0)	0(0)	0(0)	0(0)	0(0)	0(0)	0(0)	0(0)
HADCOEF3	0x30D9[7:0]	0(0)	0(0)	0(0)	0(0)	0(0)	0(0)	0(0)	0(0)
HADCOEF8	0x30DE[7:0]	0(0)	0(0)	0(0)	2(2)	3(3)	4(4)	0(0)	0(0)
CLPOWERMODE	0x30E8[5:4]	0(0)	0(0)	0(0)	0(0)	0(0)	0(0)	1(1)	1(1)

R/Gb line
Gr/B line
Addition
●:Horizontal addition pixel



2-wire serial communication setting example; 1/2 sub-sampling and its output image diagram

2-wire serial communication regiser setting for verticaland horizontal 1/2 sub-sampling operation is shown below. Image size becomes 1/4 since sub-sampling ratios are 1/2 in both direction.
Pixel skipping factors; (even-turn factor, odd- turn factor) are (1, 3) in vertical direction, (1, 3) in horizontal direction.

Table 54. 2-wire serial communication register setting for V (1,3) and H (1,3) sub-sampling

Setting item	Description of peration	Register name	Address	Setting value
Communication mode	I^2C			
Readout direction	V, H inverted	IMG_ORIENTATION[1:0]	0x0101 [1:0]	0 (0)
Vertical subsampling setting	1/2 V subsampling vertical analog binning averaging (1,3)	Y_EVN_INC[3:0]	0x0385 [3:0]	1 (1)
		Y_ODD_INC[3:0]	0x0387 [3:0]	3 (3)
		Y_OUT_SIZE[11:8] [7:0]	0x034E [3:0] 0x034F [7:0]	618 (1560)
		VMODEFDS	0x3048[0]	1 (1)
Horizontal subsampling setting	1/2 H subsampling binning averaging (1,3)	X_EVN_INC[3:0]	0x0381 [3:0]	1 (1)
		X_ODD_INC[3:0]	0x0383 [3:0]	3 (3)
		X_OUT_SIZE[12:8] [7:0]	0x034C [4:0] 0x034D [7:0]	838 (2104)
		HADDEN	0x30D5[0]	1 (1)
		HADCONFIG	0x30D5[3]	1 (1)
		HADCOEF0[7:0]	0x30D6[7:0]	1 (1)
		HADCOEF1[7:0]	0x30D7[7:0]	1 (1)
		HADCOEF2[7:0]	0x30D8[7:0]	0 (0)
		HADCOEF3[7:0]	0x30D9[7:0]	0 (0)
		HADCOEF4[7:0]	0x30DA[7:0]	0 (0)
		HADCOEF5[7:0]	0x30DB[7:0]	0 (0)
		HADCOEF6[7:0]	0x30DC[7:0]	0 (0)
		HADCOEF7[7:0]	0x30DD[7:0]	0 (0)
		HADCOEF8[7:0]	0x30DE[7:0]	2 (2)

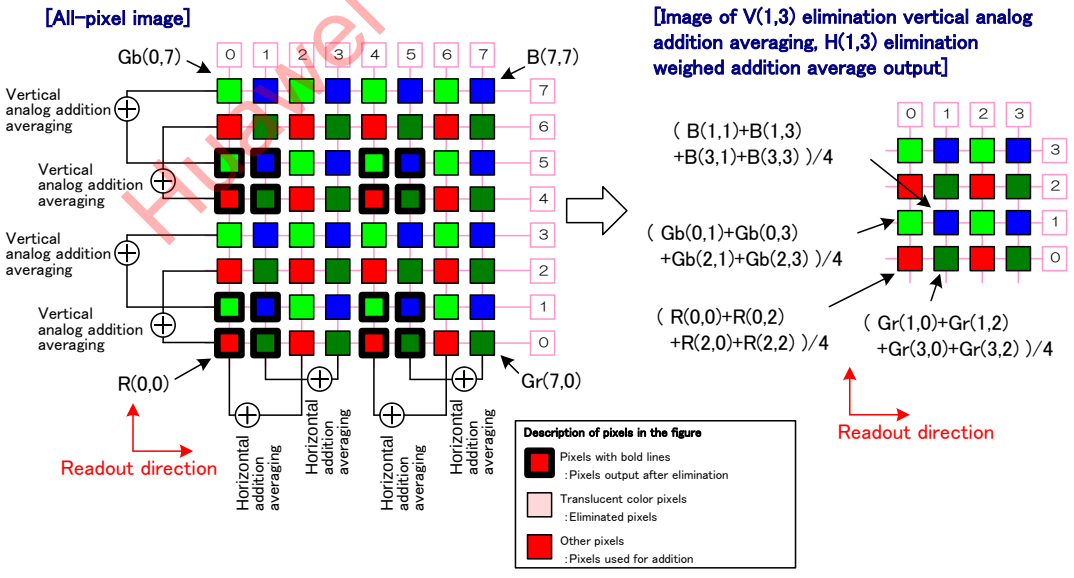


Fig 56. 2-wire serial communication V (1,3) , H (1,3) sub-sampling operation

2-wire serial communication setting example; 1/4 sub-sampling and its output image diagram

2-wire serial communication regiser setting for verticaland horizontal 1/4 sub-sampling operation is shown below. Image size becomes 1/16 since sub-sampling ratios are 1/4 in both direction.
Pixel skipping factors; (even-turn factor, odd- turn factor) are (5, 3) in vertical direction, (5, 3) in horizontal direction.

Table 55. 2-wire serial communication register setting for V (5,3) and H (5,3) sub-sampling

Setting item	Description of operation	Register name	Address	Setting value
Communication mode	I^2C			
Readout direction	V, H inverted	IMG_ORIENTATION[1:0]	0x0101 [1:0]	0 (0)
Vertical subsampling setting	1/4 V subsampling vertical analog binning averaging (5,3)	Y_EVN_INC[3:0]	0x0385 [3:0]	5 (5)
		Y_ODD_INC[3:0]	0x0387 [3:0]	3 (3)
		Y_OUT_SIZE[11:8] [7:0]	0x034E [3:0] 0x034F [7:0]	30A (778)
		VMODEFDS	0x3048[0]	1 (1)
Horizontal subsampling setting	1/4 H subsampling binning averaging (5,3)	X_EVN_INC[3:0]	0x0381 [3:0]	5 (5)
		X_ODD_INC[3:0]	0x0383 [3:0]	3 (3)
		X_OUT_SIZE[12:8] [7:0]	0x034C [4:0] 0x034D [7:0]	41C (1052)
		HADDEN	0x30D5[0]	1 (1)
		HADCONFIG	0x30D5[3]	1 (1)
		HADCOEF0[7:0]	0x30D6[7:0]	0 (0)
		HADCOEF1[7:0]	0x30D7[7:0]	0 (0)
		HADCOEF2[7:0]	0x30D8[7:0]	0 (0)
		HADCOEF3[7:0]	0x30D9[7:0]	0 (0)
		HADCOEF4[7:0]	0x30DA[7:0]	0 (0)
		HADCOEF5[7:0]	0x30DB[7:0]	0 (0)
		HADCOEF6[7:0]	0x30DC[7:0]	0 (0)
		HADCOEF7[7:0]	0x30DD[7:0]	0 (0)
		HADCOEF8[7:0]	0x30DE[7:0]	4 (4)

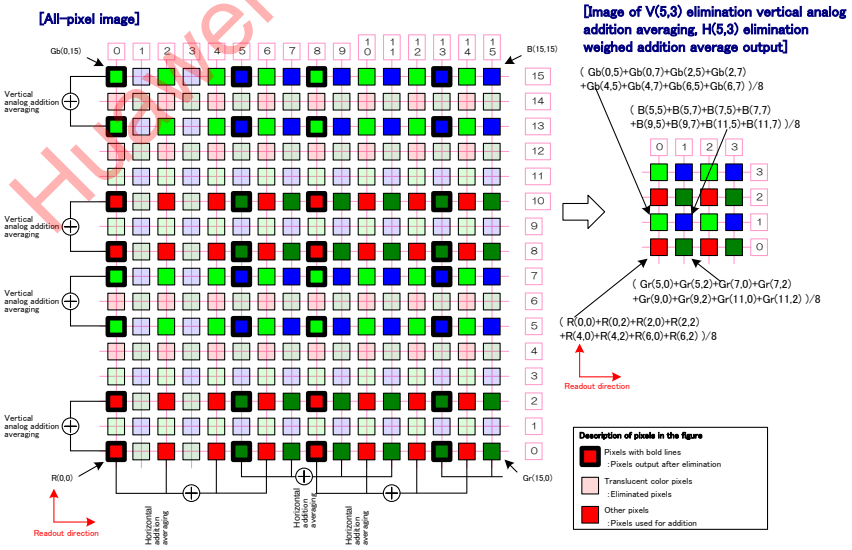
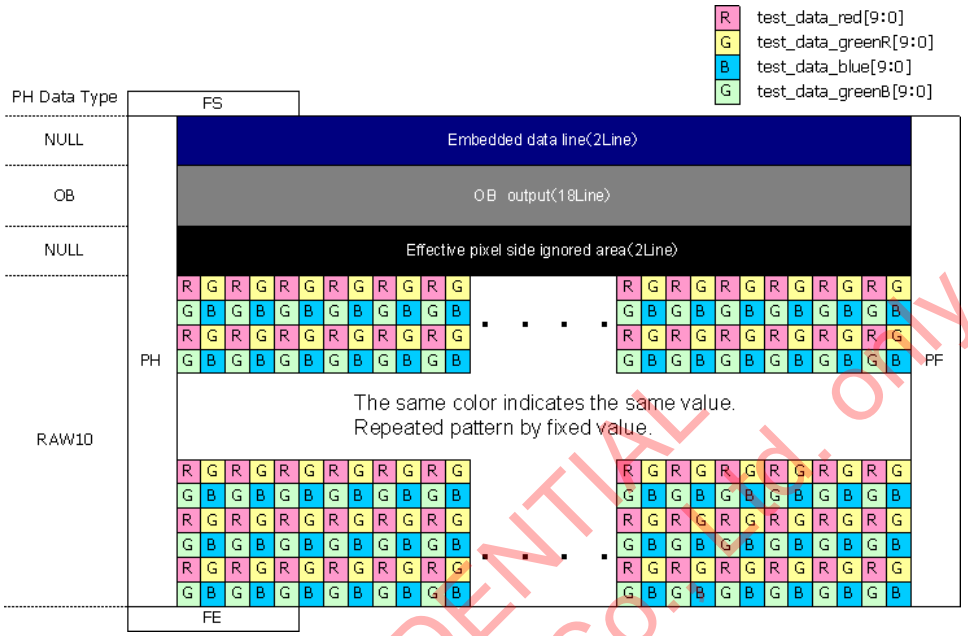


Fig 57. 2-wire serial communication V (5,3) , H (5,3) sub-sampling operation

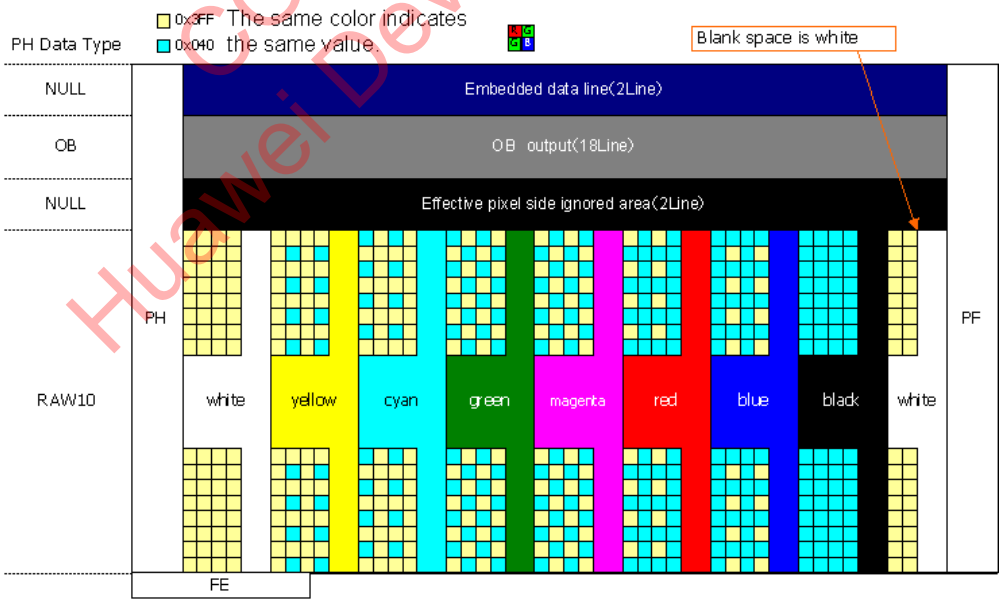
Test Pattern Generator Detail Information

Table 56. Test Pattern Description

Solid Color
test_pattern_mode = 1
test_data_red/test_data_greenR/test_data_blue/test_data_greenB = Arbitrary value

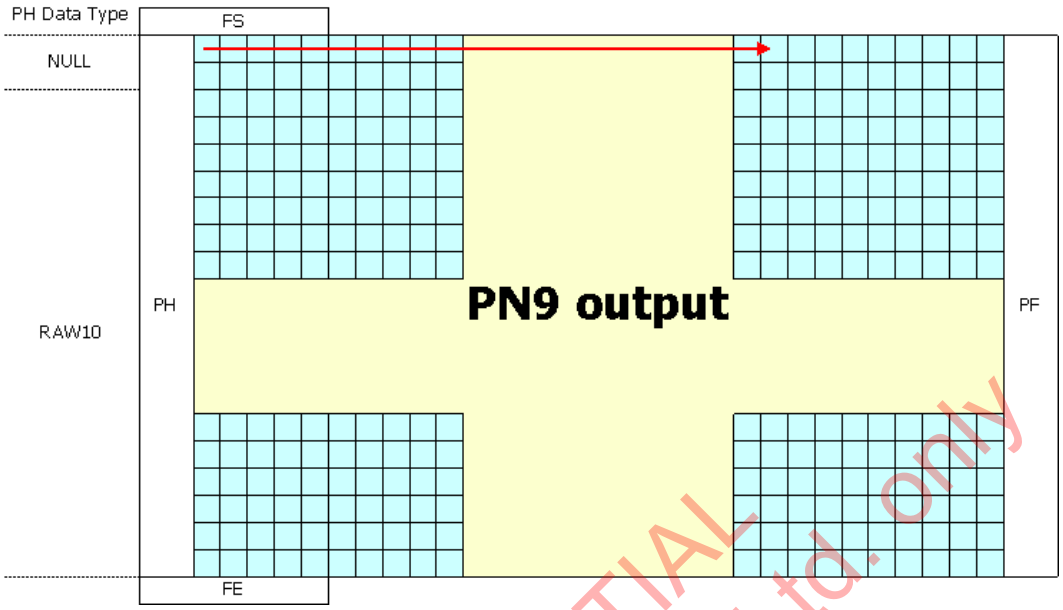


100 % color bars
test_pattern_mode = 2



Fade to grey color bar
test_pattern_mode = 3

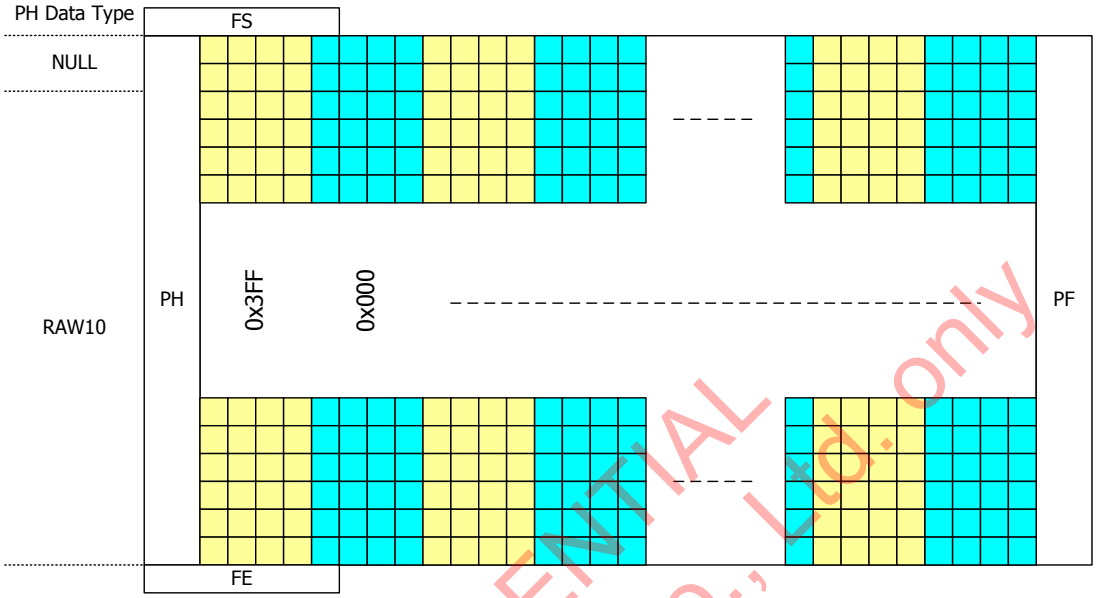
PN9 (512 bits pseudorandom data)
test_pattern_mode = 4



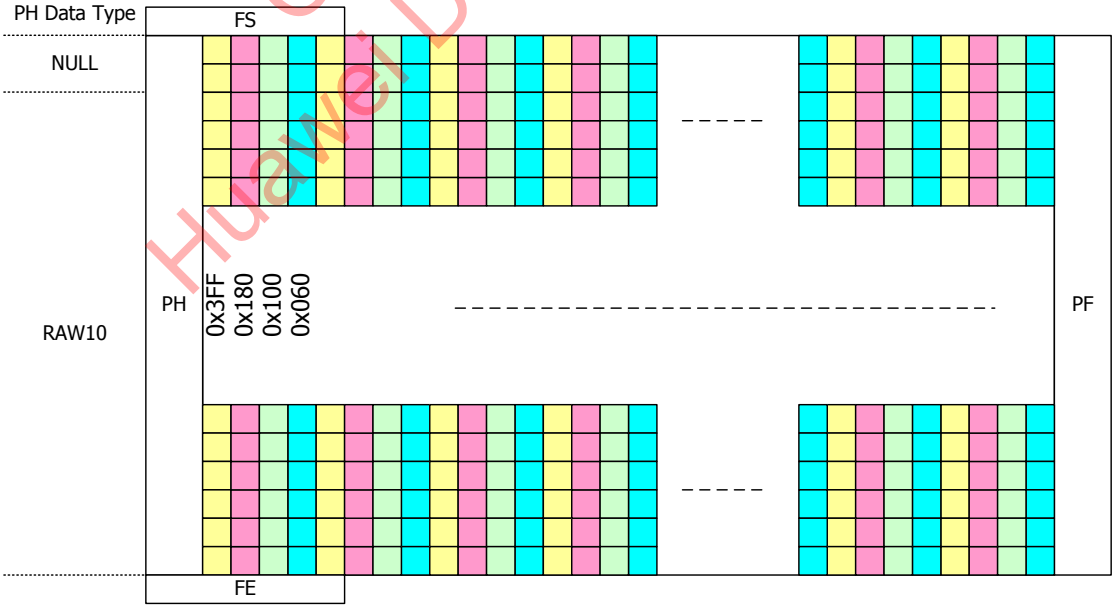
PN9 is generated by the generator polynomial of $X_9 + X_5 + 1$ as the initial value = 1.

Fix Pattern

Fix Pattern 1
test_pattern_mode = 0x0100
Pattern that repeats fixed values in 4-column units

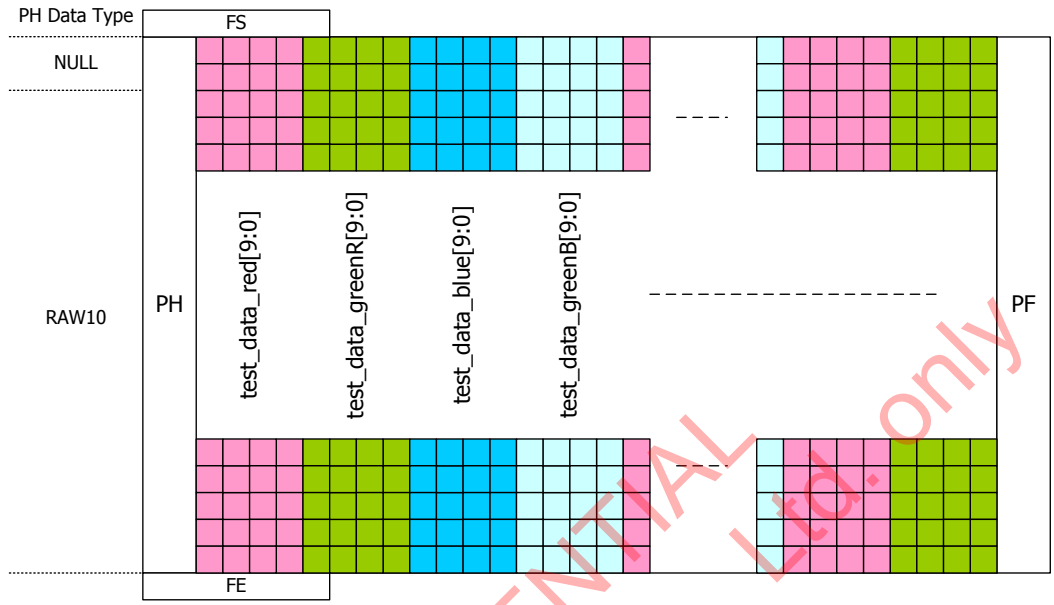


Pattern 2
test_pattern_mode = 0x0101
Pattern that repeats the setting values in 1-column units

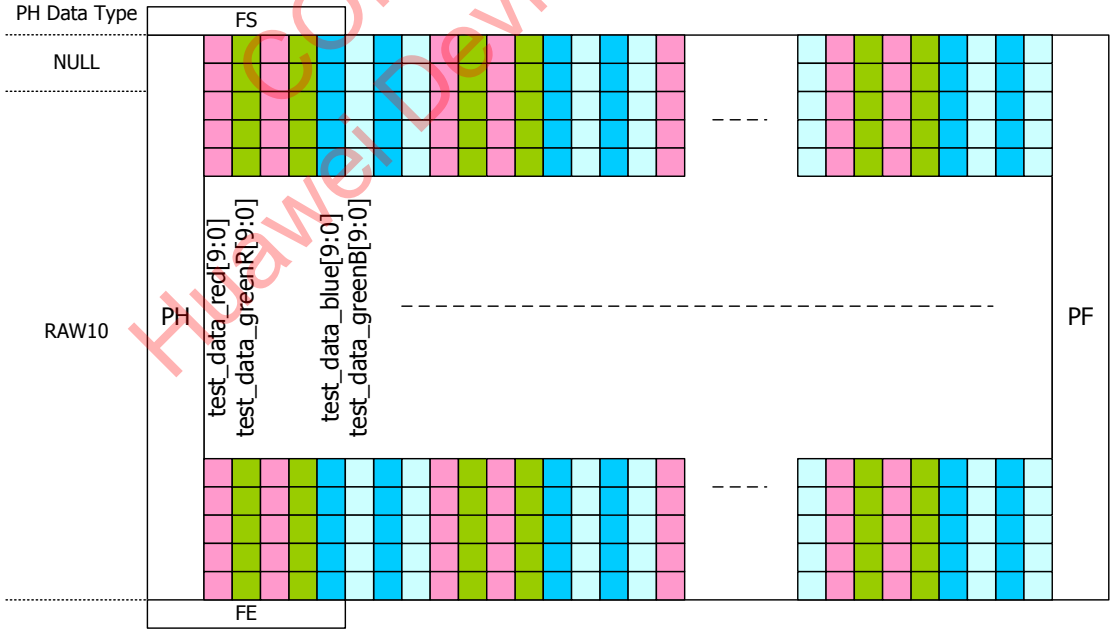


Arbitrary Pattern

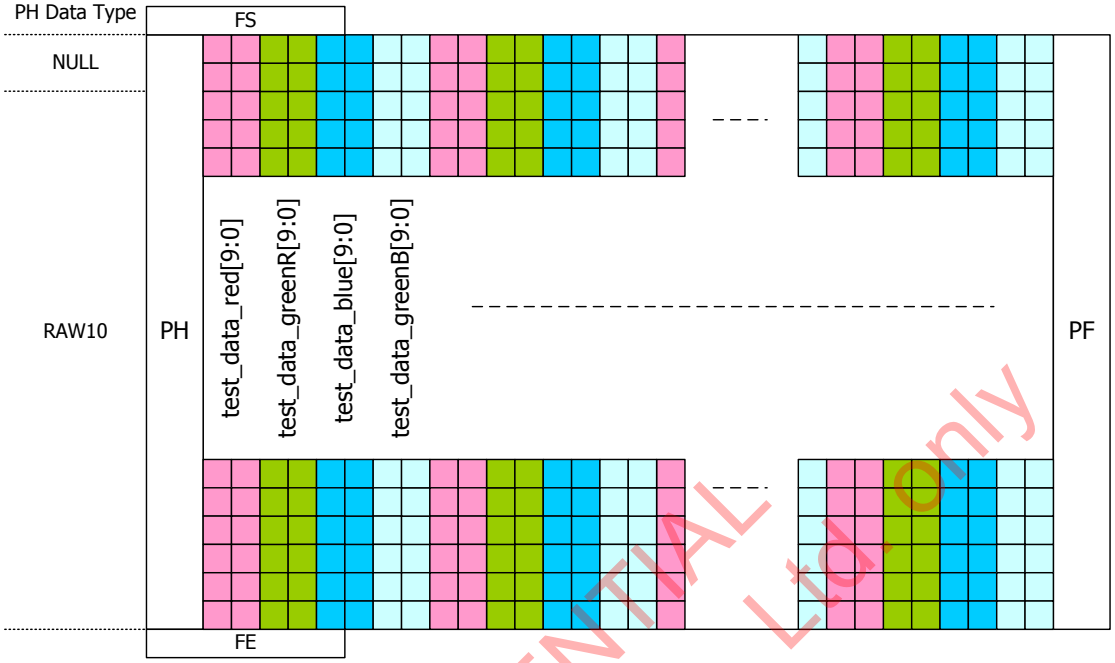
Arbitrary Pattern 1
test_pattern_mode = 0x0102
Pattern that repeats setting values in 4-column units



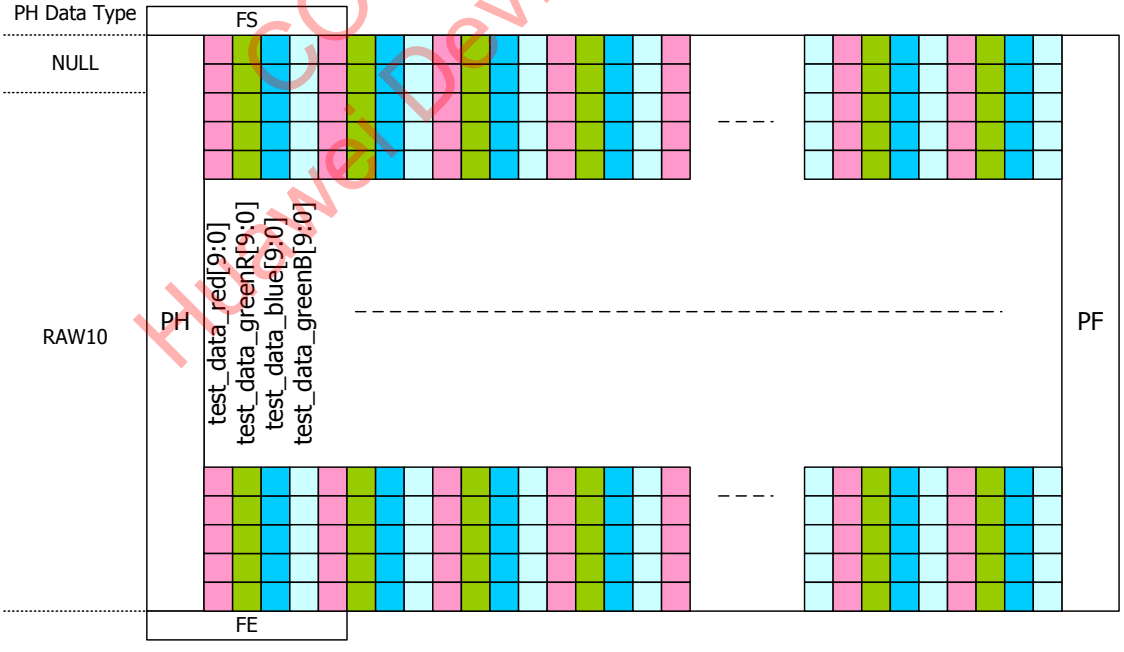
Arbitrary Pattern 2
test_pattern_mode = 0x0103
Pattern that repeats the setting values in 1-column units



Arbitrary Pattern 3
test_pattern_mode = 0x0104
Pattern that repeats fixed values in 2-column units



Arbitrary Pattern 4
test_pattern_mode = 0x0105
Pattern that repeats the fixed values in 1-column units



Detailed description of flash pulse timing control registers

FLASH_STR

This register controls the flash pulse riseing time point. When [FLASH_STR = 1], the flash pulse is output from the external pin XVS at the effective pixel end time point of the next frame of communication frame. When [FLASH_STR = 0], the flash pulse is output at the start time point of the next frame of communication frame. When [SMD = 1; global reset mode], use with [FLASH_STR = 1] is assumed. When [SMD = 0; rolling shutter mode], use with [FLASH_STR = 0] is assumed.

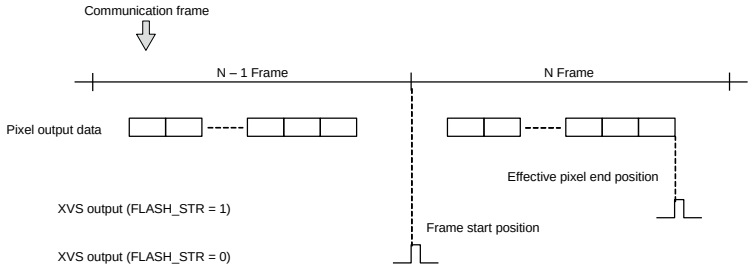


Fig 58. FLASH_STR

FLASH_REP

This register controls to repeat the flashe pulse. When [FLASH_REP = 1], IMX132TQH5-C outputs flash pulses repeatedly until
[FLASH_EN = 0] is issued. When [FLASH_REP = 0], the flash pulse is output once, however, [FLASH_EN] must be returned to “0” in the same manner as when [FLASH_REP = 1] to reset the flash pulse function for the next use of it.

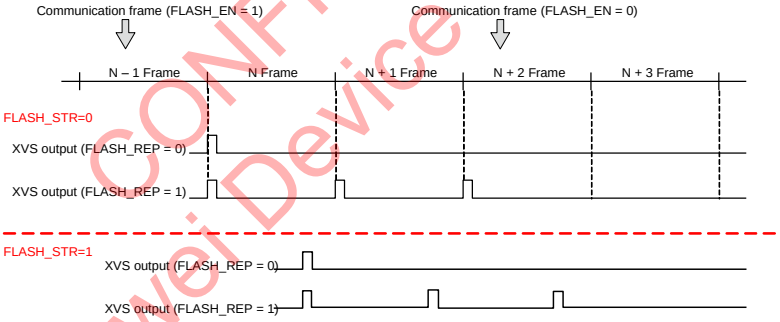


Fig 59. FLASH_REP

FLASH_DLY

The flash pulse generation timing can be delayed in frame units. This function can be used when FLASH_SMDMODE = 0 (SMD interlock disabled) .
When FLASH_SMDMODE = 1 (SMD interlock is enabled) , flash pulse delay is controlled by the GRRLVL register, so FLASH_DLY shall be set to 0 because GRRLVL and FLASH_DLY cannot be used simultaneously.

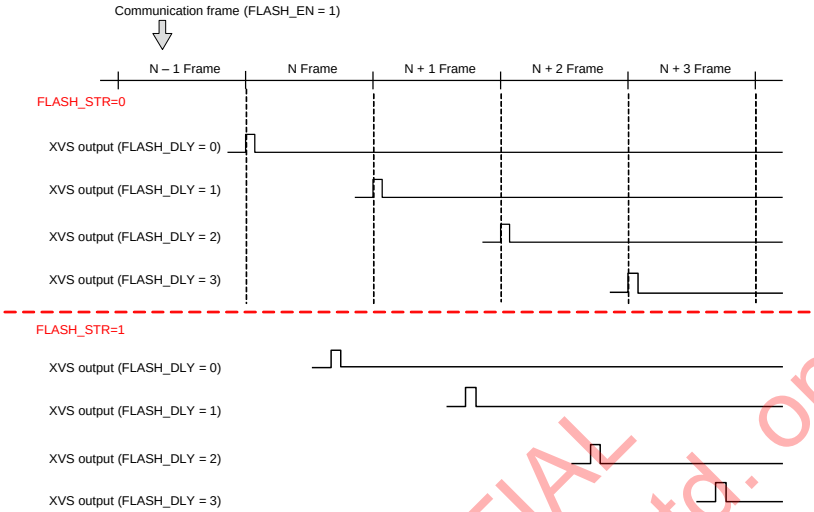


Fig 60. FLASH_DLY

FLASH_PL_STEP, FLASH_PL_STEP_GAIN

Flash pulse width is determined by flash_pl_step and flash_pl_gain registers.

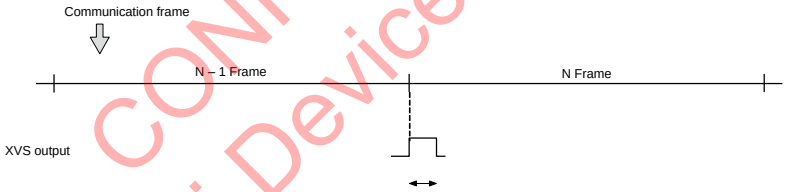


Fig 61. FLASH_PL_STEP and FLASH_PL_STEP_GAIN

The pulse width is determined from Logic clock and these two registers using following formula.

$$\text{Pulse width[sec]} = \frac{1}{\text{Logic clock frequency}} \times 64 \times 2^{\text{FLASH\_PL\_STEP\_GAIN}} \times (\text{FLASH\_PL\_STEP} + 1)$$

Setting examples are shown on the following page.

Flush pulse width setting table

Table 57. Flush pulse width setting table (1/2)

FLASH_PL_STEP_GAIN[2:0]	FLASH_PL_SETP[5:0]	Example of setting width : 1lane/RAW10/18.5fps dataRate=1000Mbps/lane logic clock=50MHz	Example of setting width : 2lane/RAW10/30fps dataRate=810Mbps/lane logic clock=81.0MHz	Example of setting width : 1lane/RAW8/23.1fps dataRate=1000Mbps/lane logic clock=62.5MHz
		us	us	us
0	0	1.3	0.8	1.0
	1	2.6	1.6	2.0
	2	3.8	2.4	3.1
	3	5.1	3.2	4.1
	4	6.4	4.0	5.1
	5	7.7	4.7	6.1
	6	9.0	5.5	7.2
	7	10.2	6.3	8.2
	8	11.5	7.1	9.2
	9	12.8	7.9	10.2
	10	14.1	8.7	11.3
	11	15.4	9.5	12.3
	12	16.6	10.3	13.3
	13	17.9	11.1	14.3
	14	19.2	11.9	15.4
	15	20.5	12.6	16.4
	16	21.8	13.4	17.4
	17	23.0	14.2	18.4
	18	24.3	15.0	19.5
	19	25.6	15.8	20.5
	20	26.9	16.6	21.5
	21	28.2	17.4	22.5
	22	29.4	18.2	23.6
	23	30.7	19.0	24.6
	24	32.0	19.8	25.6
	25	33.3	20.5	26.6
	26	34.6	21.3	27.6
	27	35.8	22.1	28.7
	28	37.1	22.9	29.7
	29	38.4	23.7	30.7
	30	39.7	24.5	31.7
	31	41.0	25.3	32.8
	32	42.2	26.1	33.8
	33	43.5	26.9	34.8
	34	44.8	27.7	35.8
	35	46.1	28.4	36.9
	36	47.4	29.2	37.9
	37	48.6	30.0	38.9
	38	49.9	30.8	39.9
	39	51.2	31.6	41.0
	40	52.5	32.4	42.0
	41	53.8	33.2	43.0
	42	55.0	34.0	44.0
	43	56.3	34.8	45.1
	44	57.6	35.6	46.1
	45	58.9	36.3	47.1
	46	60.2	37.1	48.1
	47	61.4	37.9	49.2
	48	62.7	38.7	50.2
	49	64.0	39.5	51.2
	50	65.3	40.3	52.2
	51	66.6	41.1	53.2
	52	67.8	41.9	54.3
	53	69.1	42.7	55.3
	54	70.4	43.5	56.3
	55	71.7	44.2	57.3
	56	73.0	45.0	58.4
	57	74.2	45.8	59.4
	58	75.5	46.6	60.4
	59	76.8	47.4	61.4
	60	78.1	48.2	62.5
	61	79.4	49.0	63.5
	62	80.6	49.8	64.5
	63	81.9	50.6	65.5
1	0	2.6	1.6	2.0
	1	5.1	3.2	4.1
	2	7.7	4.7	6.1
	3	10.2	6.3	8.2
	4	12.8	7.9	10.2
	5	15.4	9.5	12.3
	6	17.9	11.1	14.3
	7	20.5	12.6	16.4
	8	23.0	14.2	18.4
	9	25.6	15.8	20.5
	10	28.2	17.4	22.5
	11	30.7	19.0	24.6
	12	33.3	20.5	26.6
	13	35.8	22.1	28.7
	14	38.4	23.7	30.7
	15	41.0	25.3	32.8
	16	43.5	26.9	34.8
	17	46.1	28.4	36.9
	18	48.6	30.0	38.9
	19	51.2	31.6	41.0
	20	53.8	33.2	43.0
	21	56.3	34.8	45.1
	22	58.9	36.3	47.1
	23	61.4	37.9	49.2
	24	64.0	39.5	51.2
	25	66.6	41.1	53.2
	26	69.1	42.7	55.3
	27	71.7	44.2	57.3
	28	74.2	45.8	59.4
	29	76.8	47.4	61.4
	30	79.4	49.0	63.5
	31	81.9	50.6	65.5
	32	84.5	52.1	67.6
	33	87.0	53.7	69.6
	34	89.6	55.3	71.7
	35	92.2	56.9	73.7
	36	94.7	58.5	75.8
	37	97.3	60.0	77.8
	38	99.8	61.6	79.9
	39	102.4	63.2	81.9
	40	105.0	64.8	84.0
	41	107.5	66.4	86.0
	42	110.1	68.0	88.1
	43	112.6	69.5	90.1
	44	115.2	71.1	92.2
	45	117.8	72.7	94.2
	46	120.3	74.3	96.3
	47	122.9	75.9	98.3
	48	125.4	77.4	100.4
	49	128.0	79.0	102.4
	50	130.6	80.6	104.4
	51	133.1	82.2	106.5
	52	135.7	83.8	108.5
	53	138.2	85.3	110.6
	54	140.8	86.9	112.6
	55	143.4	88.5	114.7
	56	145.9	90.1	116.7
	57	148.5	91.7	118.8
	58	151.0	93.2	120.8
	59	153.6	94.8	122.9
	60	156.2	96.4	124.9
	61	158.7	98.0	127.0
	62	161.3	99.6	129.0
	63	163.8	101.1	131.1
2	0	5.1	3.2	4.1
	1	10.2	6.3	8.2
	2	15.4	9.5	12.3
	3	20.5	12.6	16.4
	4	25.6	15.8	20.5
	5	30.7	19.0	24.6
	6	35.8	22.1	28.7
	7	41.0	25.3	32.8
	8	46.1	28.4	36.9
	9	51.2	31.6	41.0
	10	56.3	34.8	45.1
	11	61.4	37.9	49.2
	12	66.6	41.1	53.2
	13	71.7	44.2	57.3
	14	76.8	47.4	61.4
	15	81.9	50.6	65.5
	16	87.0	53.7	69.6
	17	92.2	56.9	73.7
	18	97.3	60.0	77.8
	19	102.4	63.2	81.9
	20	107.5	66.4	86.0
	21	112.6	69.5	90.1
	22	117.8	72.7	94.2
	23	122.9	75.9	98.3
	24	128.0	79.0	102.4
	25	133.1	82.2	106.5
	26	138.2	85.3	110.6
	27	143.4	88.5	114.7
	28	148.5	91.7	118.8
	29	153.6	94.8	122.9
	30	158.7	98.0	127.0
	31	163.8	101.1	131.1
	32	169.0	104.3	135.2
	33	174.1	107.5	139.3
	34	179.2	110.6	143.4
	35	184.3	113.8	147.5
	36	189.4	116.9	151.6
	37	194.6	120.1	155.6
	38	199.7	123.3	159.7
	39	204.8	126.4	163.8
	40	209.9	129.6	167.9
	41	215.0	132.7	172.0
	42	220.2	135.9	176.1
	43	225.3	139.1	180.2
	44	230.4	142.2	184.3
	45	235.5	145.4	188.4
	46	240.6	148.5	192.5
	47	245.8	151.7	196.6
	48	250.9	154.9	200.7
	49	256.0	158.0	204.8
	50	261.1	161.2	208.9
	51	266.2	164.3	213.0
	52	271.4	167.5	217.1
	53	276.5	170.7	221.2
	54	281.6	173.8	225.3
	55	286.7	177.0	229.4
	56	291.8	180.1	233.5
	57	297.0	183.3	237.6
	58	302.1	186.5	241.7
	59	307.2	189.6	245.8
	60	312.3	192.8	249.9
	61	317.4	196.0	254.0
	62	322.6	199.1	258.0
	63	327.7	202.3	262.1
3	0	10.2	6.3	8.2
	1	20.5	12.6	16.4
	2	30.7	19.0	24.6
	3	41.0	25.3	32.8
	4	51.2	31.6	41.0
	5	61.4	37.9	49.2
	6	71.7	44.2	57.3
	7	81.9	50.6	65.5
	8	92.2	56.9	73.7
	9	102.4	63.2	81.9
	10	112.6	69.5	90.1
	11	122.9	75.9	98.3
	12	133.1	82.2	106.5
	13	143.4	88.5	114.7
	14	153.6	94.8	122.9
	15	163.8	101.1	131.1
	16	174.1	107.5	139.3
	17	184.3	113.8	147.5
	18	194.6	120.1	155.6
	19	204.8	126.4	163.8
	20	215.0	132.7	172.0
	21	225.3	139.1	180.2
	22	235.5	145.4	188.4
	23	245.8	151.7	196.6
	24	256.0	158.0	204.8
	25	266.2	164.3	213.0
	26	276.5	170.7	221.2
	27	286.7	177.0	229.4
	28	297.0	183.3	237.6
	29	307.2	189.6	245.8
	30	317.4	196.0	254.0
	31	327.7	202.3	262.1
	32	337.9	208.6	270.3
	33	348.2	214.9	278.5
	34	358.4	221.2	286.7
	35	368.6	227.6	294.9
	36	378.9	233.9	303.1
	37	389.1	240.2	311.3
	38	399.4	246.5	319.5
	39	409.6	252.8	327.7
	40	419.8	259.2	335.9
	41	430.1	265.5	344.1
	42	440.3	271.8	352.3
	43	450.6	278.1	360.4
	44	460.8	284.4	368.6
	45	471.0	290.8	376.8
	46	481.3	297.1	385.0
	47	491.5	303.4	393.2
	48	501.8	309.7	401.4
	49	512.0	316.0	409.6
	50	522.2	322.4	417.8
	51	532.5	328.7	426.0
	52	542.7	335.0	434.2
	53	553.0	341.3	442.4
	54	563.2	347.7	450.6
	55	573.4	354.0	458.8
	56	583.7	360.3	466.9
	57	593.9	366.6	475.1
	58	604.2	372.9	483.3
	59	614.4	379.3	491.5
	60	624.6	385.6	499.7
	61	634.9	391.9	507.9
	62	645.1	398.2	516.1
	63	655.4	404.5	524.3

Table 58. Flush pulse width setting table (2/2)

FLASH_PL_STEP_GAIN[2:0]	FLASH_PL_SETP[5:0]	Example of setting width: 1lane/RAW10/18.5ps dataRate=1000Mbps/lane logic clock=50MHz	Example of setting width: 2lane/RAW10/30fps dataRate=810Mbps/lane logic clock=81.0MHz	Example of setting width: 1lane/RAW8/23.1fps dataRate=1000Mbps/lane logic clock=62.5MHz
		us	us	us
4	0	20.5	12.6	16.4
	1	41.0	25.3	32.8
	2	61.4	37.9	49.2
	3	81.9	50.6	65.5
	4	102.4	63.2	81.9
	5	122.9	75.9	98.3
	6	143.4	88.5	114.7
	7	163.8	101.1	131.1
	8	184.3	113.8	147.5
	9	204.8	126.4	163.8
	10	225.3	139.1	180.2
	11	245.8	151.7	196.6
	12	266.2	164.3	213.0
	13	286.7	177.0	229.4
	14	307.2	189.6	245.8
	15	327.7	202.3	262.1
	16	348.2	214.9	278.5
	17	368.6	227.6	294.9
	18	389.1	240.2	311.3
	19	409.6	252.8	327.7
	20	430.1	265.5	344.1
	21	450.6	278.1	360.4
	22	471.0	290.8	376.8
	23	491.5	303.4	393.2
	24	512.0	316.0	409.6
	25	532.5	328.7	426.0
	26	553.0	341.3	442.4
	27	573.4	354.0	458.8
	28	593.9	366.6	475.1
	29	614.4	379.3	491.5
	30	634.9	391.9	507.9
	31	655.4	404.5	524.3
	32	675.8	417.2	540.7
	33	696.3	429.8	557.1
	34	716.8	442.5	573.4
	35	737.3	455.1	589.8
	36	757.8	467.8	606.2
	37	778.2	480.4	622.6
	38	798.7	493.0	639.0
	39	819.2	505.7	655.4
	40	839.7	518.3	671.7
	41	860.2	531.0	688.1
	42	880.6	543.6	704.5
	43	901.1	556.2	720.9
	44	921.6	568.9	737.3
	45	942.1	581.5	753.7
	46	962.6	594.2	770.0
	47	983.0	606.8	786.4
	48	1003.5	619.5	802.8
	49	1024.0	632.1	819.2
	50	1044.5	644.7	835.6
	51	1065.0	657.4	852.0
	52	1085.4	670.0	868.4
	53	1105.9	682.7	884.7
	54	1126.4	695.3	901.1
	55	1146.9	708.0	917.5
	56	1167.4	720.6	933.9
	57	1187.8	733.2	950.3
	58	1208.3	745.9	966.7
	59	1228.8	758.5	983.0
	60	1249.3	771.2	999.4
	61	1269.8	783.8	1015.8
	62	1290.2	796.4	1032.2
	63	1310.7	809.1	1048.6

FLASH_PL_STEP_GAIN[2:0]	FLASH_PL_SETP[5:0]	Example of setting width: 1lane/RAW10/18.5ps dataRate=1000Mbps/lane logic clock=50MHz	Example of setting width: 2lane/RAW10/30fps dataRate=810Mbps/lane logic clock=81.0MHz	Example of setting width: 1lane/RAW8/23.1fps dataRate=1000Mbps/lane logic clock=62.5MHz
		us	us	us
5	0	41.0	25.3	32.8
	1	81.9	50.6	65.5
	2	122.9	75.9	98.3
	3	163.8	101.1	131.1
	4	204.8	126.4	163.8
	5	245.8	151.7	196.6
	6	286.7	177.0	229.4
	7	327.7	202.3	262.1
	8	368.6	227.6	294.9
	9	409.6	252.8	327.7
	10	450.6	278.1	360.4
	11	491.5	303.4	393.2
	12	532.5	328.7	426.0
	13	573.4	354.0	458.8
	14	614.4	379.3	491.5
	15	655.4	404.5	524.3
	16	696.3	429.8	557.1
	17	737.3	455.1	589.8
	18	778.2	480.4	622.6
	19	819.2	505.7	655.4
	20	860.2	531.0	688.1
	21	901.1	556.2	720.9
	22	942.1	581.5	753.7
	23	983.0	606.8	786.4
	24	1024.0	632.1	819.2
	25	1065.0	657.4	852.0
	26	1105.9	682.7	884.7
	27	1146.9	708.0	917.5
	28	1187.8	733.2	950.3
	29	1228.8	758.5	983.0
	30	1269.8	783.8	1015.8
	31	1310.7	809.1	1048.6
	32	1351.7	834.4	1081.3
	33	1392.6	859.7	1114.1
	34	1433.6	884.9	1146.9
	35	1474.6	910.2	1179.6
	36	1515.5	935.5	1212.4
	37	1556.5	960.8	1245.2
	38	1597.4	986.1	1278.0
	39	1638.4	1011.4	1310.7
	40	1679.4	1036.6	1343.5
	41	1720.3	1061.9	1376.3
	42	1761.3	1087.2	1409.0
	43	1802.2	1112.5	1441.8
	44	1843.2	1137.8	1474.6
	45	1884.2	1163.1	1507.3
	46	1925.1	1188.3	1540.1
	47	1966.1	1213.6	1572.9
	48	2007.0	1238.9	1605.6
	49	2048.0	1264.2	1638.4
	50	2089.0	1289.5	1671.2
	51	2129.9	1314.8	1703.9
	52	2170.9	1340.0	1736.7
	53	2211.8	1365.3	1769.5
	54	2252.8	1390.6	1802.2
	55	2293.8	1415.9	1835.0
	56	2334.7	1441.2	1867.8
	57	2375.7	1466.5	1900.5
	58	2416.6	1491.8	1933.3
	59	2457.6	1517.0	1966.1
	60	2498.6	1542.3	1998.8
	61	2539.5	1567.6	2031.6
	62	2580.5	1592.9	2064.4
	63	2621.4	1618.2	2097.2

FLASH_PL_STEP_GAIN[2:0]	FLASH_PL_SETP[5:0]	Example of setting width: 1lane/RAW10/18.5ps dataRate=1000Mbps/lane logic clock=50MHz	Example of setting width: 2lane/RAW10/30fps dataRate=810Mbps/lane logic clock=81.0MHz	Example of setting width: 1lane/RAW8/23.1fps dataRate=1000Mbps/lane logic clock=62.5MHz
		us	us	us
6	0	81.9	50.6	65.5
	1	163.8	101.1	131.1
	2	245.8	151.7	196.6
	3	327.7	202.3	262.1
	4	409.6	252.8	327.7
	5	491.5	303.4	393.2
	6	573.4	354.0	458.8
	7	655.4	404.5	524.3
	8	737.3	455.1	589.8
	9	819.2	505.7	655.4
	10	901.1	556.2	720.9
	11	983.0	606.8	786.4
	12	1065.0	657.4	852.0
	13	1146.9	708.0	917.5
	14	1228.8	758.5	983.0
	15	1310.7	809.1	1048.6
	16	1392.6	859.7	1114.1
	17	1474.6	910.2	1179.6
	18	1556.5	960.8	1245.2
	19	1638.4	1011.4	1310.7
	20	1720.3	1061.9	1376.3
	21	1802.2	1112.5	1441.8
	22	1884.2	1163.1	1507.3
	23	1966.1	1213.6	1572.9
	24	2048.0	1264.2	1638.4
	25	2129.9	1314.8	1703.9
	26	2211.8	1365.3	1769.5
	27	2293.8	1415.9	1835.0
	28	2375.7	1466.5	1900.5
	29	2457.6	1517.0	1966.1
	30	2539.5	1567.6	2031.6
	31	2621.4	1618.2	2097.2
	32	2703.4	1668.7	2162.7
	33	2785.3	1719.3	2228.2
	34	2867.2	1769.9	2293.8
	35	2949.1	1820.4	2359.3
	36	3031.0	1871.0	2424.8
	37	3113.0	1921.6	2490.4
	38	3194.9	1972.1	2555.9
	39	3276.8	2022.7	2621.4
	40	3358.7	2073.3	2687.0
	41	3440.6	2123.9	2752.5
	42	3522.6	2174.4	2818.0
	43	3604.5	2225.0	2883.6
	44	3686.4	2275.6	2949.1
	45	3768.3	2326.1	3014.7
	46	3850.2	2376.7	3080.2
	47	3932.2	2427.3	3145.7
	48	4014.1	2477.8	3211.3
	49	4096.0	2528.4	3276.8
	50	4177.9	2579.0	3342.3
	51	4259.8	2629.5	3407.9
	52	4341.8	2680.1	3473.4
	53	4423.7	2730.7	3538.9
	54	4505.6	2781.2	3604.5
	55	4587.5	2831.8	3670.0
	56	4669.4	2882.4	3735.6
	57	4751.4	2932.9	3801.1
	58	4833.3	2983.5	3866.6
	59	4915.2	3034.1	3932.2
	60	4997.1	3084.6	3997.7
	61	5079.0	3135.2	4063.2
	62	5161.0	3185.8	4128.8
	63	5242.9	3236.3	4194.3

FLASH_PL_STEP_GAIN[2:0]	FLASH_PL_SETP[5:0]	Example of setting width: 1lane/RAW10/18.5ps dataRate=1000Mbps/lane logic clock=50MHz	Example of setting width: 2lane/RAW10/30fps dataRate=810Mbps/lane logic clock=81.0MHz	Example of setting width: 1lane/RAW8/23.1fps dataRate=1000Mbps/lane logic clock=62.5MHz
		us	us	us
7	0	163.8	101.1	131.1
	1	327.7	202.3	262.1
	2	491.5	303.4	393.2
	3	655.4	404.5	524.3
	4	819.2	505.7	655.4
	5	983.0	606.8	786.4
	6	1146.9	708.0	917.5
	7	1310.7	809.1	1048.6
	8	1474.6	910.2	1179.6
	9	1638.4	1011.4	1310.7
	10	1802.2	1112.5	1441.8
	11	1966.1	1213.6	1572.9
	12	2129.9	1314.8	1703.9
	13	2293.8	1415.9	1835.0
	14	2457.6	1517.0	1966.1
	15	2621.4	1618.2	2097.2
	16	2785.3	1719.3	2228.2
	17	2949.1	1820.4	2359.3
	18	3113.0	1921.6	2490.4
	19	3276.8	2022.7	2621.4
	20	3440.6	2123.9	2752.5
	21	3604.5	2225.0	2883.6
	22	3768.3	2326.1	3014.7
	23	3932.2	2427.3	3145.7
	24	4096.0	2528.4	3276.8
	25	4259.8	2629.5	3407.9
	26	4423.7	2730.7	3538.9
	27	4587.5	2831.8	3670.0
	28	4751.4	2932.9	3801.1
	29	4915.2	3034.1	3932.2
	30	5079.0	3135.2	4063.2
	31	5242.9	3236.3	4194.3
	32	5406.7	3337.5	4325.4
	33	5570.6	3438.6	4456.4
	34	5734.4	3539.8	4587.5
	35	5898.2	3640.9	4718.6
	36	6062.1	3742.0	4849.7
	37	6225.9	3843.2	4980.7
	38	6389.8	3944.3	5111.8
	39	6553.6	4045.4	5242.9
	40	6717.4	4146.6	5374.0
	41	6881.3	4247.7	5505.0
	42	7045.1	4348.8	5636.1
	43	7209.0	4450.0	5767.2
	44	7372.8	4551.1	5898.2
	45	7536.6	4652.2	6029.3
	46	7700.5	4753.4	6160.4
	47	7864.3	4854.5	6291.5
	48	8028.2	4955.7	6422.5
	49	8192.0	5056.8	6553.6
	50	8355.8	5157.9	6684.7
	51	8519.7	5259.1	6815.7
	52	8683.5	5360.2	6946.8
	53	8847.4	5461.3	7077.9
	54	9011.2	5562.5	7209.0
	55	9175.0	5663.6	7340.0
	56	9338.9	5764.7	7471.1
	57	9502.7	5865.9	7602.2
	58	9666.6	5967.0	7733.2
	59	9830.4	6068.1	7864.3
	60	9994.2	6169.3	7995.4
	61	10158.1	6270.4	8126.5
	62	10321.9	6371.6	8257.5
	63	10485.8	6472.7	8388.6

LED_FLASH_EN

This register controls LED flash pulse generation. By setting [LED_FLASH_EN = 1], XVS pin output High level in unit of fram until [LED_FLASH_EN = 0] is issued. This function cannot be enabled at the same time with FLASH_EN.

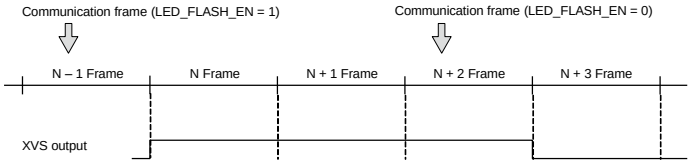


Fig 62. LED_FLASH_EN

FLASH_SMDMODE

This register controls the flash pulse generation timing interlocking with global reset operation frame. (Hereinafter the mode interlocking with the global reset operation frame is described as “global reset interlock mode”.) When FLASH_SMDMODE = 1, the flash pulse is output from the XVS pin at the frame in global reset operation.
In this mode, the FLASH_EN register is automatically cleared.
(When FLASH_SMDMODE = 0, the flash pulse is output at the frame which FLASH_EN register is updated. In this case, FLASH_EN register is not cleared.)

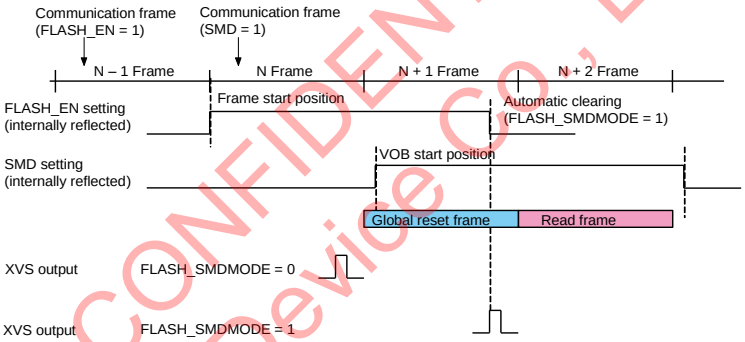


Fig 63. FLASH_SMDMODE

PRE_ FLASH_EN

As a countermeasure to red eyes phenomena, PRE_FLASH_EN register controls to generate the pulses for pre-flash light emission before the main flash pulse. When PRE_FLASH_EN = 1, the pulse is output from XVS pin. When used with FLASH_SMDMODE =1 (global reset interlock mode) , PRE_FLASH_EN register is automatically cleared after the pulse is output.
The pulse width of pre-flash pulse is the same as that of main flash pulse.

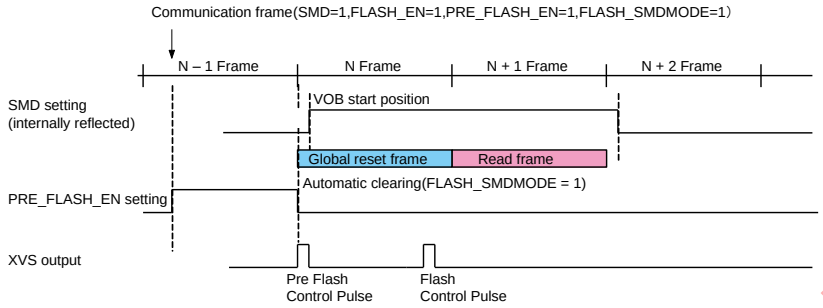


Fig 64. PRE_ FLASH_EN

When setting [PRE_ FLASH_EN = 1] with [FLASH_SMDMODE = 0], no interlock with global reset mode, pre-flash pulse is generated at the same time with this register setting. In this case, PRE_FLASH_EN register is not cleared automattically, then it is necessary to reset [PRE_FLASH_EN = 0] and set [FLASH_EN = 1] to generate the main flash pulse. The time interval between pre-flash and main flash emission can be controlled by command issuing timing of PRE_FLASH_EN and FLASH_EN.

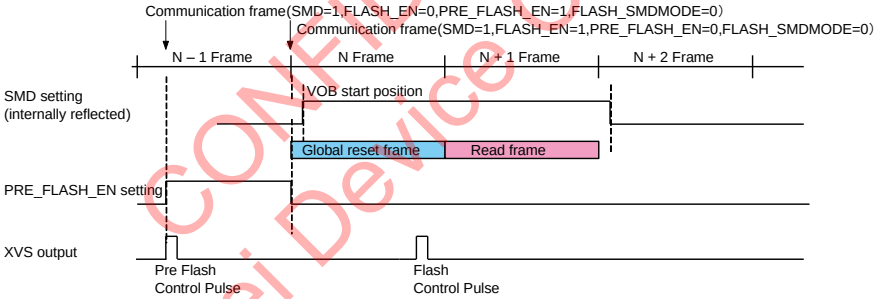


Fig 65. PRE_ FLASH_EN (2)

GRRLVL

This register is effective when FLASH_SMDMODE = 1 (global reset interlock mode) and determins the period from pre-flash pulse to main flash pulse in unit of frame from “zero” to “eight”. “0” means the pre-flash pulse and main flash pulse are generated in the same frame, “eight” means main flash pulse is generated “eight” frames after the pre-flash pulse frame. GRRLVL has 4 bit, however the values from “zero” to “eight” are significant, 8 and greater values take the maximum duration of “eight” frames.

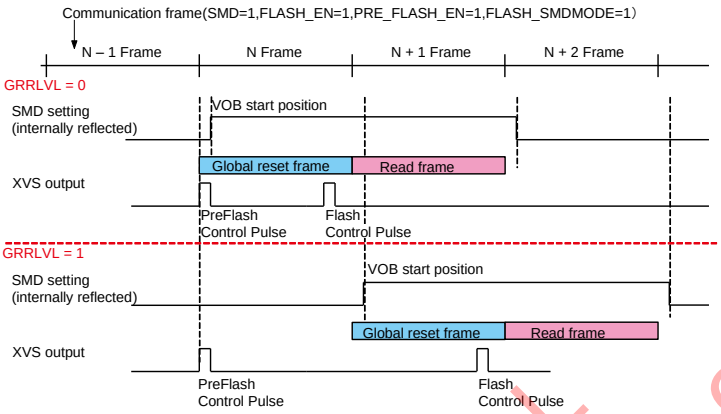


Fig 66. GRRLVL

Global Reset and Mechanical Shutter Control Pulse

XVS and XHS output

IMX132TQH5-C can output the vertical and horizontal synchronous pulse; XVS and XHS from XVS pin.
IMX132TQH5-C has the global reset fundtion assuming the use of the mechanical shutter.
Though the global reset operation can be performed by the register access, the mechanical shutter timing signal can be output from XVS pin.

First of all, we explain how to output these synchronous pulses. As the common setting for XVS pin, set the drivability of these pins considering the loading for them on the bvoard. Please set the value ather than 3h. When set the value 3h, they become high impedance state.

Table 59. XVS,XHS common setting for drive current

I²C register	address	Bit	name	description	notes
	0x30F8	[1:0]	OUTCUR	0h : 4 mA@2.7 V 2 mA@1.8 V 1h : 2 mA@2.7 V 1 mA@1.8 V 2h : 1 mA@2.7 V 0.5 mA@1.8 V 3h : High-Z	Select drive strength

Set registers in the table below to output XVS pulse from XVS pin.

Table 60. XVS output mode select

I²C register	address	Bit	name	description	notes
	0x30FC	[2]	XVSOUTEN	Setting value : 1h	
	0x3240	[3:2]	XVSSEL	Setting value : 1h	
	0x3242	[7:0]	TESTXVSCU	Setting value : 12h	

Set registers in the table below to output XHS pulse from XVS pin.

Table 61. XHS output mode select

I²C register	address	Bit	name	description	notes
	0x30FC	[1]	XHSOUTEN	Setting value : 1h	
	0x3240	[3:2]	XVSSEL	Setting value : 1h	
	0x3241	[7:0]	TESTTGCU	Setting value : 11h	

As the result of setting the registers above, XVS and XHS are output as following timimg diagram. XVS is only pin that can output sync signals.So V sync signal(XVS) and H sync signal(XHS) can be sent out from pin XVS once at a time.

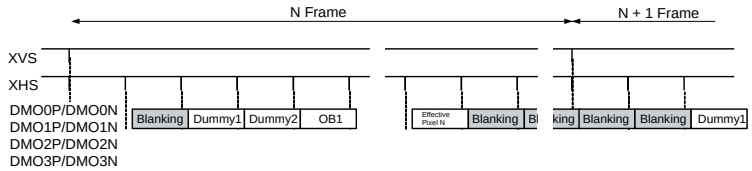


Fig 67. XVS, XHSoutput timing diagram

Pulse width and polarity of XVS and XHS are programmable with the registers in below table.

Table 62. XVS,XHS pulse width and polarity setting

	address	Bit	name	Description	notes
I2C register	0x30F9	[3:2]	XHSLNG	0h : 4 Logic clock width (Def.) 1h : 8 Logic clock width 2h : 16 Logic clock width 3h : 32 Logic clock width	XHS pulse width
		[1:0]	XVSLNG	0h : 1H width (Def.) 1h : 2H width 2h : 4H width 3h : 8H width	XVS pulse width setting
	0x30FA	[5]	XHSINV	0h : LowActive (Def.) 1h : HighActive	XHS output polarity setting
		[4]	XVSINV	0h : LowActive (Def.) 1h : HighActive	XVS output polarity setting

Logic clock width[sec] = 1 / Logic clock frequency

XVS is only pin that can output sync signals.So V sync signal(XVS) and H sync signal(XHS) can be sent out from pin XVS once at a time.

Examples are shown below.

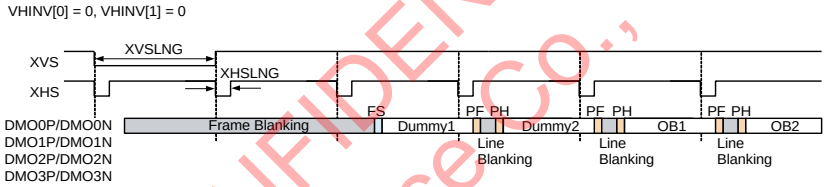


Fig 68. XVSLNG = 0h (1H width) , XHSLNG = 1h (8 Logic clock width) , CVHINV [1:0] = 0h (LowActive)

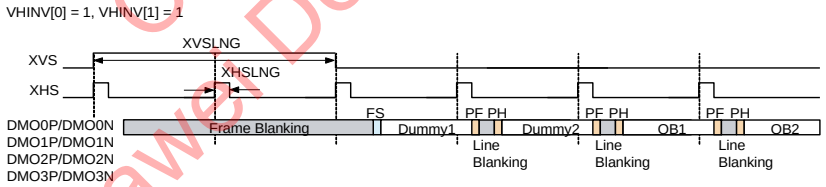


Fig 69. XVSLNG =1 h (2H width) , XHSLNG = 1h (8 Logic clock width) , VHINV [1:0] = 3h (HighActive)

Method to determin the mechanical shutter control timimg by XVS, XHS, and globa reset mode setting timing

IMX132TQH5-C indicates the border of frames by XVS and border of lines by XHS. By using these pulses for the trigger of global reset setting, user can recognize the readout frame position, more precisely, these pulses can be used for the trigger for mechanical shutter operation.

Set the XVS and XHS output mode register in initialize sequence of before “communicarion 1” in the diagram below. Set global reset mode; [SMD = 1] in “communication 1” and reset the mode; [SMD = 0] in “communication 2”. With these communications, IMX132TQH5-C operates the the sequence below. (Please refere the section of integration time setting for SMD and related registers.)

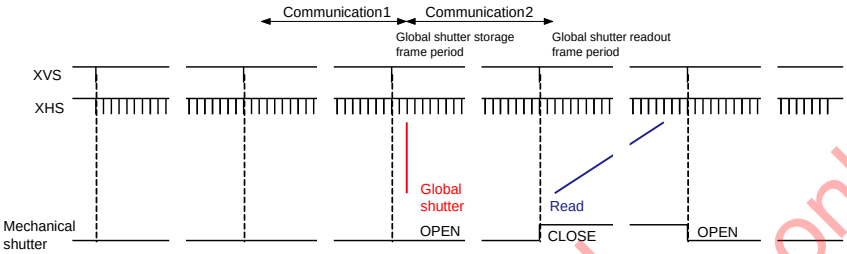


Fig 70. Timing diagram of global reset operation and XVS/XHS output

Example 1: Falling Pulse Output at Mechanical Shutter Timing, and Global Reset Non-linkage Mode

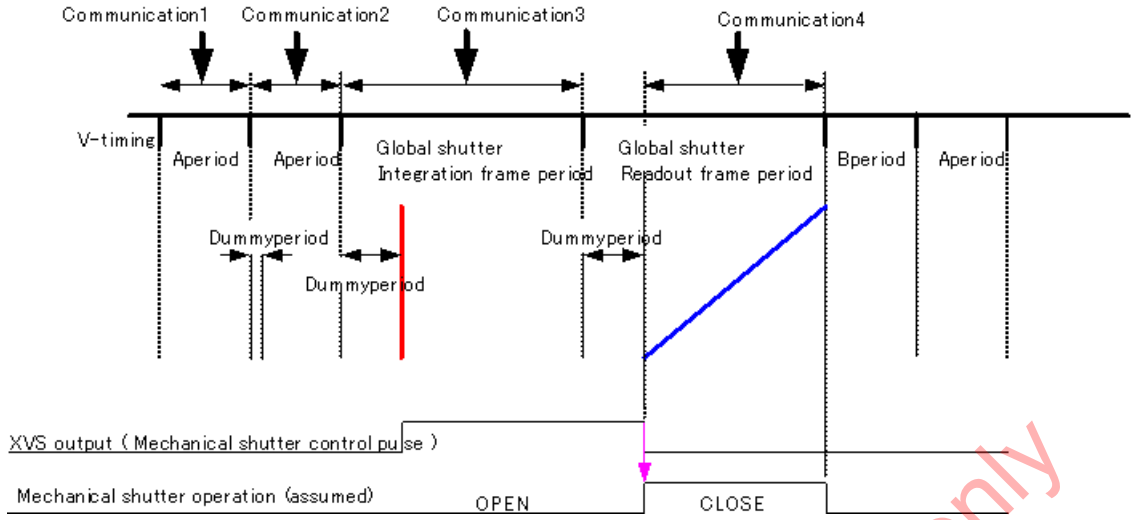


Fig 1. Global Reset and Mechanical Shutter Control 1

Mechanical shutter control pulse can be output from the XVS pin only. XVS signal and XHS signal cannot be output at the same time.

Table 1. Global Reset and Mechanical Shutter Control 1

Communication 1	Mechanical shutter control pulse timing setting	MECHSHR_STR = 0
	Mechanical shutter control pulse output setting	XVSSEL = 2 (Possible for the initial setting after power On)
	Mechanical shutter control pulse width setting	As required
	Global reset linkage setting of mechanical shutter control pulse	MECHSHR_SMDMODE = 0
Communication 2	Mechanical shutter control pulse enable setting	MECHSHR_EN = 1
	Global reset enable setting	SMD = 1
	Mode change	x_odd_inc=1,x_even_inc=1 y_odd_inc=1,y_even_inc=1
	Frame length change	frame_length_lines = all pixels setting
	Gain setting	As required
Communication 3	none	
Communication 4	Mechanical shutter control pulse output stop setting	XVSSEL = 0
	Mode, frame and gain setting	As required

Example 2 : Short Falling Pulse Output at Mechanical Shutter Timing, and Global Reset Non-linkage Mode

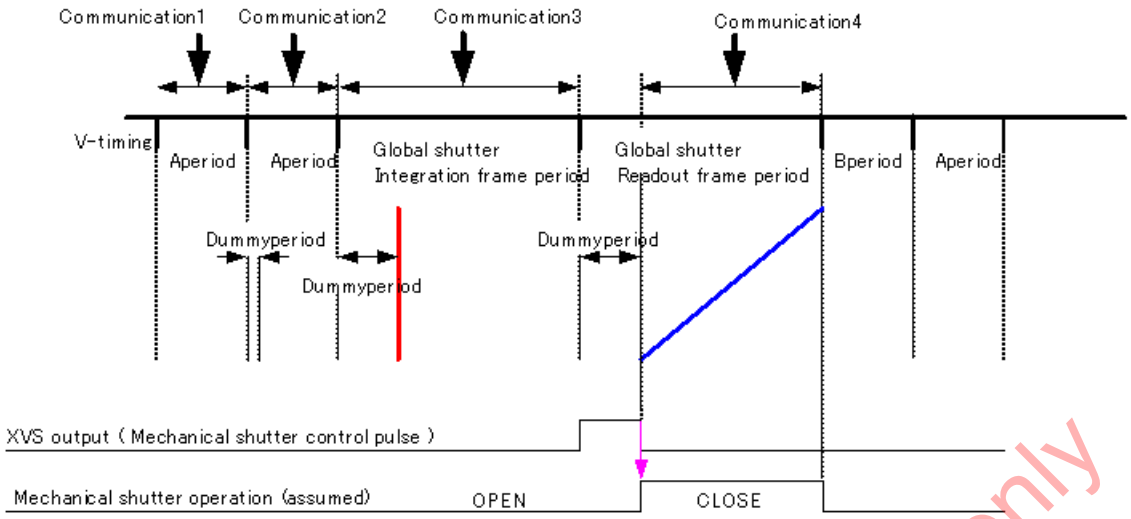


Fig 2. Global Reset and Mechanical Shutter Control 2

Mechanical shutter timing pulse can be output from the XVS pin only. XVS signal and XHS signal cannot be output at the same time.

Table 2. Global Reset and Mechanical Shutter Control 2

Communication 1	Mechanical shutter control pulse timing setting	MECHSHR_STR (According to frame length)
	Mechanical shutter control pulse output setting	XVSSEL = 2 (Possible for the initial setting after power On)
	Mechanical shutter control pulse width setting	As required
	Global reset linkage setting of mechanical shutter control pulse	MECHSHR_SMDMODE = 0
Communication 2	Mechanical shutter control pulse enable setting	MECHSHR_EN = 1
	Global reset enable setting	SMD = 1
	Mode change	x_odd_inc=1,x_even_inc=1 y_odd_inc=1,y_even_inc=1
	Frame length change	frame_length_lines = all pixels setting
	Gain setting	As required
Communication 3	none	
Communication 4	Mechanical shutter control pulse output stop setting	XVSSEL = 0
	Mode, frame and gain setting	As required

Example 3: Rising Pulse Output at Mechanical Shutter Timing, and Global Reset Non-linkage Mode

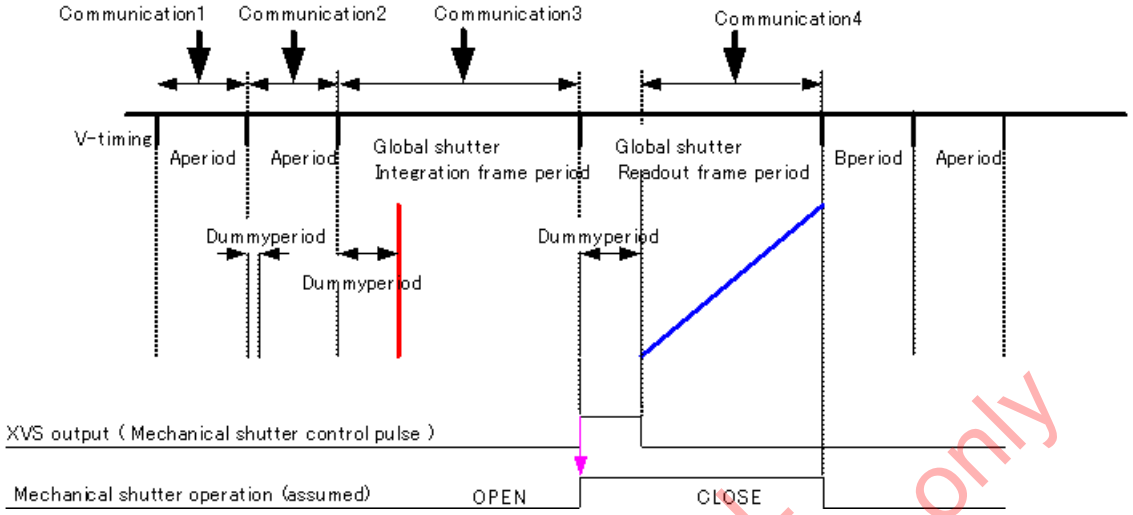


Fig 3. Global Reset and Mechanical Shutter Control 3

Table 3. Global Reset and Mechanical Shutter Control 3

Communication 1	Mechanical shutter control pulse timing setting	MECHSHR_STR (According to frame length)
	Mechanical shutter control pulse output setting	XVSSEL = 2 (Possible for the initial setting after power On)
	Mechanical shutter control pulse width setting	As required
	Global reset linkage setting of mechanical shutter control pulse	MECHSHR_SMDMODE = 0
Communication 2	Mechanical shutter control pulse enable setting	MECHSHR_EN = 1
	Global reset enable setting	SMD = 1
	Mode change	x_odd_inc=1,x_even_inc=1 y_odd_inc=1,y_even_inc=1
	Frame length change	frame_length_lines = all pixels setting
	Gain setting	As required
Communication 3	none	
Communication 4	Mechanical shutter control pulse output stop setting	XVSSEL = 0
	Mode, frame and gain setting	As required

Example 4: Rising Pulse Output at Mechanical Shutter Timing, and Global Reset Linkage Mode

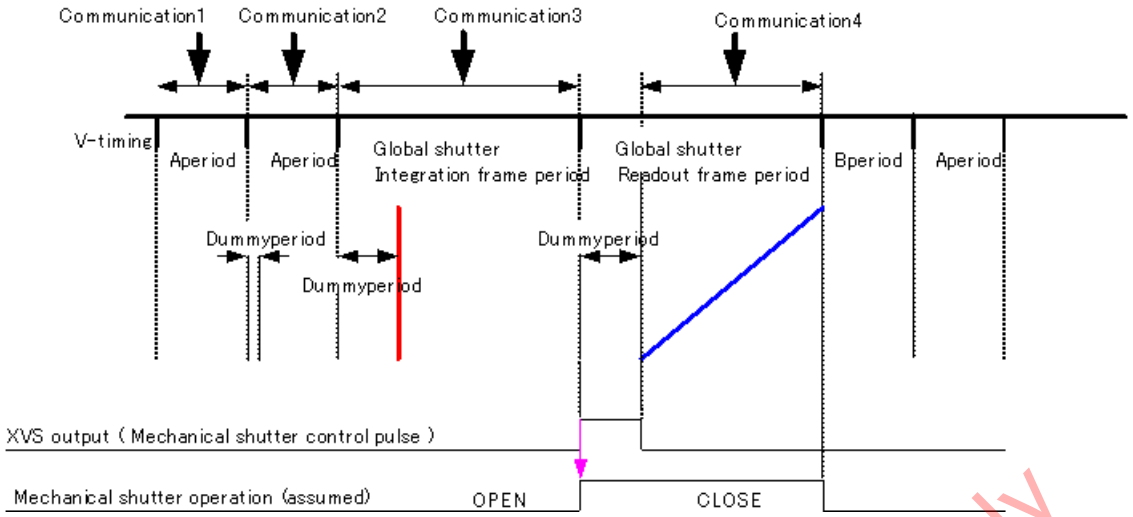


Fig 4. Global Reset and Mechanical Shutter Control 4

Table 4. Global Reset and Mechanical Shutter Control 4

Communication 1	Mechanical shutter control pulse timing setting	MECHSHR_STR (According to frame length)
	Mechanical shutter control pulse output setting	XVSSEL = 2 (Possible for the initial setting after power On)
	Mechanical shutter control pulse width setting	As required
	Global reset linkage setting of mechanical shutter control pulse	MECHSHR_SMDMODE = 1
Communication 2	Mode change	x_odd_inc=1,x_even_inc=1 y_odd_inc=1,y_even_inc=1
	Frame length change	frame_length_lines = all pixels setting
	Gain setting	As required
	Timing setting of global reset enable reflection	As required
	Mechanical shutter control pulse enable setting	MECHSHR_EN = 1
	Global reset enable setting	SMD = 1
Communication 3	none	
Communication 4	Mechanical shutter control pulse output stop setting	XVSSEL = 0
	Mode, frame and gain setting	As required

Example 5: Flash Control Pulse Output at Frame Start, and Global Reset Non-linkage Mode

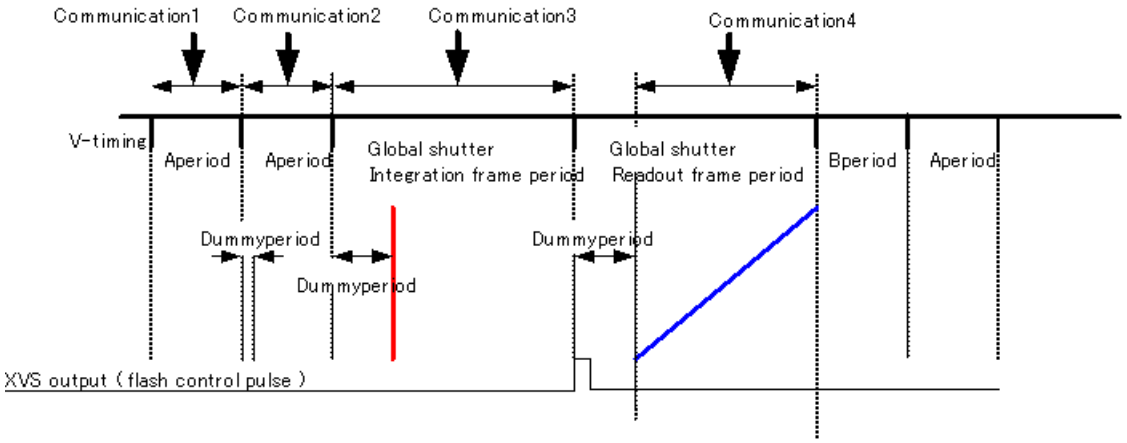


Fig 5. Global Reset and Flash Control 5

Flash control pulse can be output from the XVS pin only. XVS signal and XHS signal cannot be output at the same time.

Table 5. Global Reset and Flash Control 5

Communication 1	Flash control pulse timing setting	FLASH_DLY = 1
	Flash control pulse output position setting	FLASH_STR = 0
	Flash control pulse repeat setting	FLASH_REP = 0
	Flash control pulse output setting	XVSSEL = 3 (Possible for the initial setting after power On)
	Flash control pulse width setting	As required
	Global reset linkage setting of flash control pulse	FLASH_SMDMODE = 0
Communication 2	Global reset enable setting	SMD = 1
	Mode change	x_odd_inc=1,x_even_inc=1 y_odd_inc=1,y_even_inc=1
	Frame length change	frame_length_lines = all pixels setting
	Gain setting	As required
Communication 3	Flash control pulse enable setting	FLASH_EN = 1
Communication 4	Flash control pulse disable setting	FLASH_EN = 0
	Flash control pulse output stop setting	XVSSEL = 0
	Mode, frame and gain setting	As required

Example 6: Flash Control Pulse Output at Effective Pixel End Position, and Global Reset Non-linkage Mode

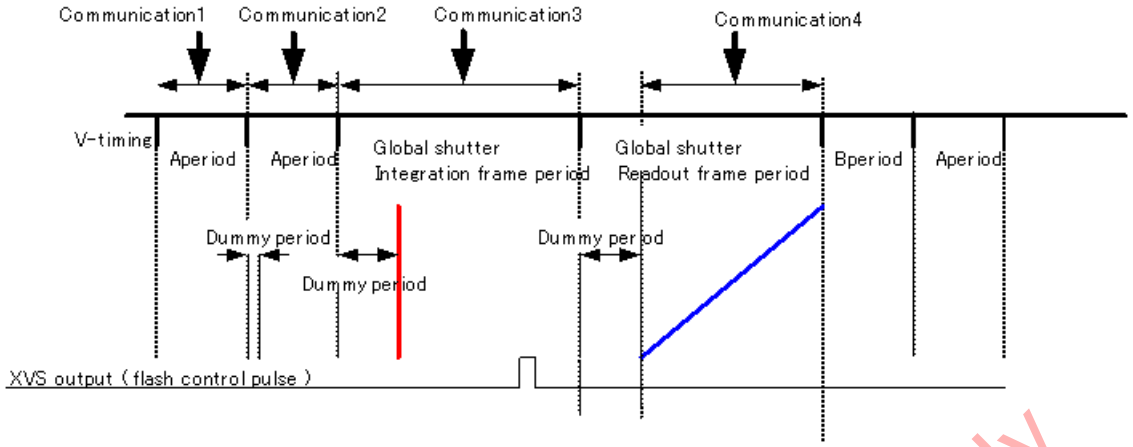


Fig 6. Global Reset and Flash Control 6

Table 6. Global Reset and Flash Control 6

Communication 1	Flash control pulse timing setting	FLASH_DLY = 0
	Flash control pulse output position setting	FLASH_STR = 1
	Flash control pulse repeat setting	FLASH_REP = 0
	Flash control pulse output setting	XVSSEL = 3
	Flash control pulse width setting	As required
	Global reset linkage setting of flash control pulse	FLASH_SMDMODE = 0
Communication 2	Flash control pulse enable setting	FLASH_EN = 1
	Global reset enable setting	SMD = 1
	Mode change	x_odd_inc=1,x_even_inc=1 y_odd_inc=1,y_even_inc=1
	Frame length change	frame_length_lines = all pixels setting
	Gain setting	As required
Communication 3	none	
Communication 4	Flash control pulse disable setting	FLASH_EN = 0
	Flash control pulse output stop setting	XVSSEL = 0
	Mode, frame and gain setting	As required

Example 7: Flash Control Pulse Output, and Global Reset Linkage Mode

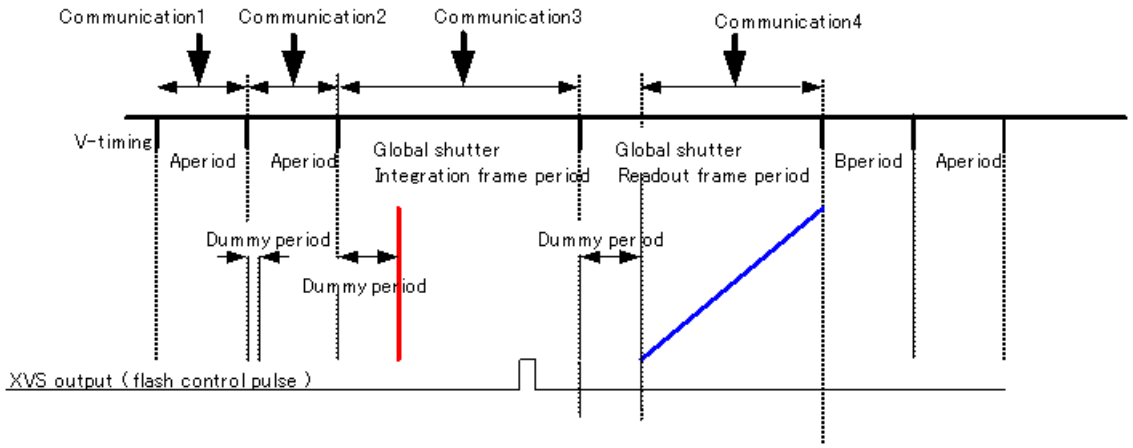


Fig 7. Global Reset and Flash Control 7

Table 7. Global Reset and Flash Control 7

Communication 1	Flash control pulse timing setting	FLASH_DLY = 0
	Flash control pulse output position setting	FLASH_STR = 1
	Flash control pulse repeat setting	FLASH_REP = 0
	Flash control pulse output setting	XVSSEL = 3 (Possible for the initial setting after power On)
	Flash control pulse width setting	As required
	Global reset linkage setting of flash control pulse	FLASH_SMDMODE = 1
Communication 2	Mode change	x_odd_inc=1,x_even_inc=1 y_odd_inc=1,y_even_inc=1
	Frame length change	frame_length_lines = all pixels setting
	Gain setting	As required
	Timing setting of global reset enable reflection	As required
	Flash control pulse enable setting	FLASH_EN = 1
	Global reset enable setting	SMD = 1
Communication 3	none	
Communication 4	Flash control pulse output stop setting	XVSSEL = 0
	Mode, frame and gain setting	As required

In global reset linkage mode, the flash control pulse or mechanical shutter control pulse is output at the timing of global reset frame after the flash control pulse enable and mechanical shutter control pulse enable are set in advance, and then the global reset enable is set. Only one pulse can be output because destination is only the XVS pin. In addition, each enable setting is automatically cleared after the pulse is output.

In global reset linkage mode, after communicating the global reset enable setting, the timing which actually becomes a global reset frame can be set up. (GRRVL register)
The timing when the reflection timing of global reset enable is delayed by 2 frames (GRRLVL = 2) is shown below.

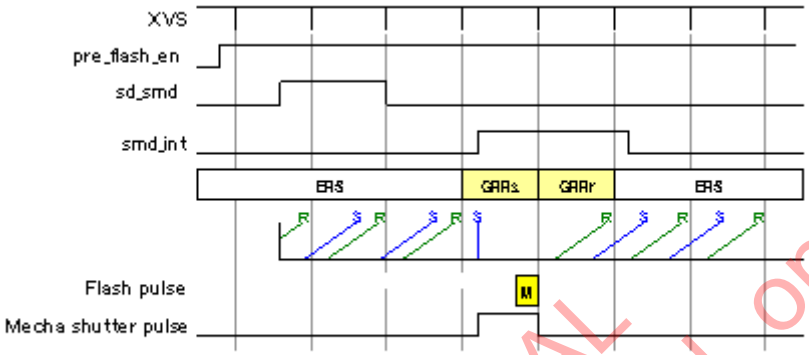


Fig.78. Global Reset Timing

Example 8: Pre-flash Control Pulse Output, and Global Reset Linkage Mode

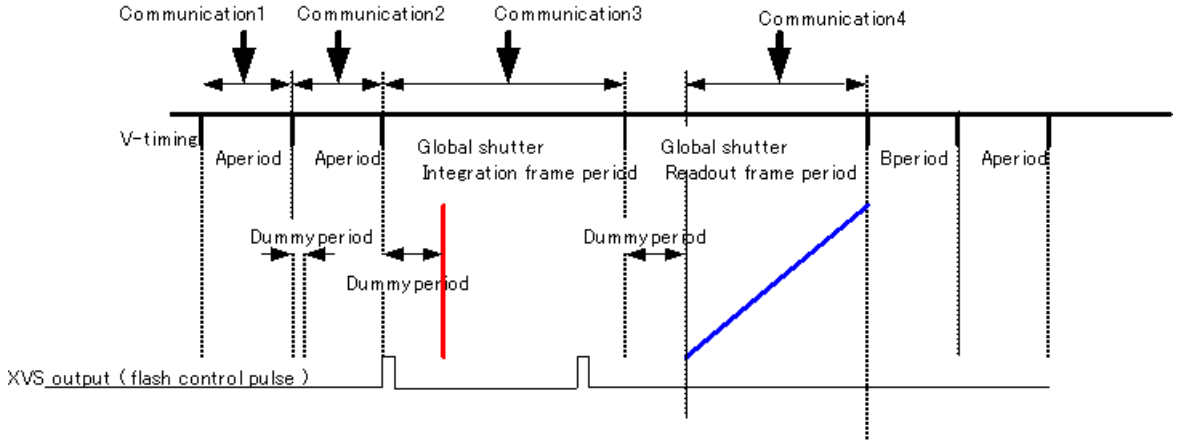


Fig 8. Global Reset and Flash Control 8

Table 8. Global Reset and Flash Control 8

Communication 1	Flash control pulse timing setting	FLASH_DLY = 0
	Flash control pulse output position setting	FLASH_STR = 1
	Flash control pulse repeat setting	FLASH_REP = 0
	Flash control pulse output setting	XVSSEL = 3 (Possible for the initial setting after power On)
	Flash control pulse width setting	As required
	Global reset linkage setting of flash control pulse	FLASH_SMDMODE = 1
Communication 2	Mode change	x_odd_inc=1,x_even_inc=1 y_odd_inc=1,y_even_inc=1
	Frame length change	frame_length_lines = all pixels setting
	Gain setting	As required
	Timing setting of global reset enable reflection	As required
	Pre-flash control pulse enable setting	PRE_FLASH_EN = 1
	Flash control pulse enable setting	FLASH_EN = 1
	Global reset enable setting	SMD = 1
Communication 3	none	
Communication 4	Flash control pulse output stop setting	XVSSEL = 0
	Mode, frame and gain setting	As required

The pre-flash control pulse can be output for a countermeasure to red eyes. The period from pre-flash control pulse to main flash pulse can be expanded by the GRRLVL register up to 9 frames.
The timing when the reflection timing of global reset enable is delayed by 2 frames (GRRLVL = 2) is shown below.

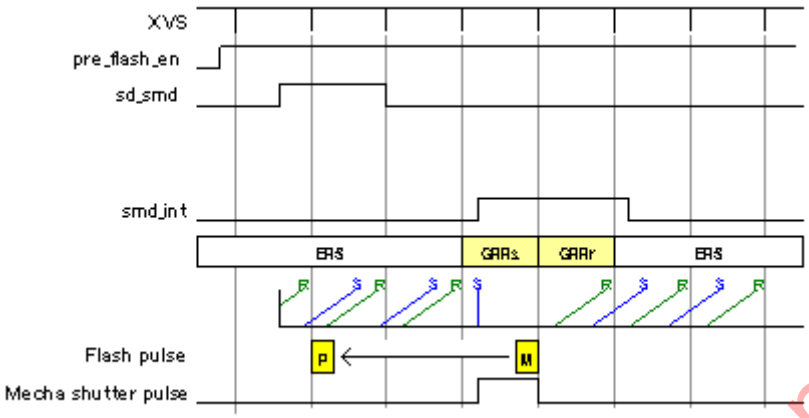


Fig 9. Global Reset Timing