S5K3H7YX EVT0.2

1/3.2" 8M / FHD 30 fps CMOS Image Sensor

Revision 0.23

June 2012

Data Sheet

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Chip Handling Guide

Precaution against Electrostatic Discharge

When using semiconductor devices, ensure that the environment is protected against static electricity:

1. Wear antistatic clothes and use earth band.
2. All objects that are in direct contact with devices must be made up of materials that do not produce static electricity.
3. Ensure that the equipment and work table are earthed.
4. Use ionizer to remove electron charge.

Contamination

Do not use semiconductor products in an environment exposed to dust or dirt adhesion.

Temperature/Humidity

Semiconductor devices are sensitive to:

- Environment
- Temperature
- Humidity

High temperature or humidity deteriorates the characteristics of semiconductor devices. Therefore, do not store or use semiconductor devices in such conditions.

Mechanical Shock

Do not to apply excessive mechanical shock or force on semiconductor devices.

Chemical

Do not expose semiconductor devices to chemicals because exposure to chemicals leads to reactions that deteriorate the characteristics of the devices.

Light Protection

In non- Epoxy Molding Compound (EMC) package, do not expose semiconductor IC to bright light. Exposure to bright light causes malfunctioning of the devices. However, a few special products that utilize light or with security functions are exempted from this guide.

Radioactive, Cosmic and X-ray

Radioactive substances, cosmic ray, or X-ray may influence semiconductor devices. These substances or rays may cause a soft error during a device operation. Therefore, ensure to shield the semiconductor devices under environment that may be exposed to radioactive substances, cosmic ray, or X-ray.

EMS (Electromagnetic Susceptibility)

Strong electromagnetic wave or magnetic field may affect the characteristic of semiconductor devices during the operation under insufficient PCB circuit design for Electromagnetic Susceptibility (EMS).

Revision History

Revision No.	Date	Description	Author (s)
0.01	August 11, 2011	• Initial Release	Yoel Yaffe
0.02	August 22, 2011	• External clock frequency updated to 54Mhz-6Mhz • Power-up timing updated • Analog gain control and ADC resolution description • Add note on PLL_S	Yoel Yaffe
0.03	August 22, 2011	• Device operating modes updated (3.1) • SPI Max frequency updated to 18 MHz • ISP functional description updated (11.5) • Mechanical shutter figures updated	Yoel Yaffe
0.04	Sep 7, 2011	• Important Notice updated • Trademark page added • *Figure 4*: Pixel Array Information – updated • *Table 18*: Absolute max rating updated • Receiver characteristics removed • SPI section updated • Analog gain control updated • MCLK timing description format updated • Parallel I/F AC spec updated • Color Matrix read only registers removed • Added few missing registers	Yoel Yaffe
0.05	Sep 20, 2011	• Operation Modes updated • Power-up sequence updated • Power consumption updated based on updated simulations • Add frame timing change examples	Yoel Yaffe
0.06	Sep 21, 2011	• Formatting updates	Yoel Yaffe
0.07	Oct 30, 2011	• Typo update for context switch • Register address correction • Figure 26: remove corrupted frame	Yoel Yaffe
0.08	Oct 30, 2011	• Limit spec to FHD 30fps for EVT0 • Operating conditions: Power supply limits changes.	Yoel Yaffe
0.09	Nov 6, 2011	• Unit fix in DC Characteristics • AC Characteristics updated • Update power-up/down sequence in case POR_PWDN is High • Update *5.5.1 Integration Time Control (Electronic Shutter Control)*	Yoel Yaffe
0.10	Nov 13, 2011	• Update VDDA range 2.7-3V, VDDD range 1.15-1.3V	Yoel Yaffe
0.11	Dec 22, 2011	• Model id description updated • Update *8.1.1.2 Mechanical Shutter Frame Timing*	Yoel Yaffe

Revision No.	Date	Description	Author (s)
		Configuration Change • Description updated for pin #84, #85, #95	
0.12	Dec 27, 2011	• nvm_charge_pump_lvl register description for NVM x1.5 charge pump setting added to *11.1.2 Configuration Registers 2 [0xD0003000 to 0xD0003FFF]*	Yoel Yaffe
0.13	Dec 28, 2011	• Formatting updates	Yoel Yaffe
0.14	Jan 6, 2012	• Context switch feature removed	Yoel Yaffe
0.15	Jan 8, 2012	• Figures 26-30 updated	Yoel Yaffe
0.16	Feb 12, 2012	• *6.1.2 SPI Sequences* updated • *7.1 Power-Up Sequence* updated	Yoel Yaffe
0.17	Mar 7, 2012	• *10.3 DC Characteristics* updated with max current • *11.1.1 Configuration Registers 1 [0xD0000000 to 0xD0001FFF]* updated for EVT0.2 • *11.1.2 Configuration Registers 2 [0xD0003000 to 0xD0003FFF]* updated for EVT0.2	Yoel Yaffe
0.18	Apr 30, 2012	• *10.3 DC Characteristics* – Dynamic power updated based on mass-production data	Yoel Yaffe
0.19	Apr 30, 2012	• *Table 9 I2C Fast Mode Timing Specifications* – Note on MCLK frequency limitation removed	Yoel Yaffe
0.20	May 3, 2012	• *Table 9 I2C Fast Mode Timing Specifications* – Updated for MCLK < 12.8Mhz	Yoel Yaffe
0.21	May 8, 2012	• *Table 9 I2C Fast Mode Timing Specifications* – Updated for MCLK < 12.8Mhz	Yoel Yaffe
0.22	May 10, 2012	• *Table 9 I2C Fast Mode Timing Specifications* – Updated for MCLK < 12Mhz	Yoel Yaffe
0.23	June 7, 2012	• *10.3 DC Characteristics* – Updated VDDA max current spec	Yoel Yaffe

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List of Conventions

Register RW Access Type Conventions

Type	Definition	Description
R	Read Only	The application has permission to read the Register field. Writes to read-only fields have no effect.
W	Write Only	The application has permission to write in the Register field.
RW	Read & Write	The application has permission to read and writes in the Register field. The application sets this field by writing 1'b1 and clears it by writing 1'b0.

Register Value Conventions

Expression	Description
x	Undefined bit
X	Undefined multiple bits
?	Undefined, but depends on the device or pin status
Device dependent	The value depends on the device
Pin value	The value depends on the pin status

Reset Value Conventions

Expression	Description
0	Clears the register field
1	Sets the register field
x	Don't care condition

Warning: Some bits of control registers are driven by hardware or write operation only. As a result the indicated reset value and the read value after reset might be different.

1 Product Overview

1.1 Introduction

The S5K3H7YX is a highly integrated 8M pixel camera chip that includes a CMOS image sensor (CIS), image correction functionality and serial transmission using 4-lane MIPI. It is designed for fast yet low power operation, delivering full resolution capture at 30 frames per second (fps) and full field of view (16:9) FHD video at 30fps. It is fabricated by the SAMSUNG 90 nm back side illumination (BSI) CMOS image sensor process developed for imaging applications to realize a high-efficiency and low-power photo sensor. The sensor consists of 3264 × 2448 effective pixels that meet with the 1/3.2-inch optical format.

The CIS has on-chip 10-bit ADC arrays to digitize the pixel output and on-chip Correlated Double Sampling (CDS) to drastically reduce Fixed Pattern Noise (FPN). It incorporates on-chip camera functions such as lens shading correction, defect correction, exposure setting, white balance setting, image scaling and image data compression.

It is programmable through a CCI or SPI serial interface and includes on-chip one-time programmable (OTP) none-volatile memory (NVM).

The S5K3H7YX is suitable for a low-power camera module with a 2.8 V/1.2 V power supply.

1.2 Features

- 8Mp sensor with 1/3.2"optics
- Pixel size: 1.4 μm
- Effective resolution: 3264 (H) × 2448 (V)
- Electronic rolling shutter and global reset
- Support digital video stabilization margins in FHD/HD video modes
- Frame rate:
  - Capture: 8M-4:3 30 fps (2640 Mbps)
  - FHD video: 6M-16:9 30 fps (1980 Mbps)/2.7M (16:9) 30 fps (990 Mbps)
  - HD video: 1.5M-16:9 120 fps
  - High speed: QVGA 240 fps
- Interfaces:
  - Fine interface frequency control using additional dedicated PLL for EMI avoidance and integration flexibility.
  - MIPI CSI2 – four lanes (1Gbps per lane)
  - 10-bit parallel video interface, with reduced frame rate
  - Output formats: RAW8 (using DPCM/PCM compression), RAW10, RAW12 (for test only)
- Control interface:
  - SPI interface – Three-wire serial communication circuit up to 18 MHz.
  - I2C-compatible – Two-wire serial communication circuit up to 400 kHz.
- Xenon/LED flash
- Mechanical shutter
- 8 Kbit on-chip OTP memory to support defect corrections, chip ID and module-to-module compensation.
- Analog gain x16
- Vertical and horizontal flip mode
- Continuous frame capture mode
- 2/2, 4/4 – average/average sub sampling readout
- Pixel elimination readout function
- x1.5, x2, x3, x4 Bayer downscaler function
- Lens shading correction function
- Bad pixel correction
- On-chip temperature sensor
- Built-in test pattern generation
- Supply voltage: 2.8 V for analog and 2.8 V or 1.8 V for I/O, 1.2 V for digital core supply
- Operating temperature: – 30 °C to + 70 °C

1.3 Block Diagram

The S5K3H7YX is a progressive-scan sensor that generates a stream of pixel data at a constant frame rate. It uses an on-chip phase-locked loop (PLL) to generate all internal clocks from a single master input clock running between 6 MHz and 54 MHz. Output interface clocks may be generated by dedicated PLL for maximal flexibility in interface frequency and for EMI avoidance. The maximum pixel rate is 3960 Mbps at MIPI 4-lane, corresponding to the pixel rate of 396 MHz at CSI-2 RAW10.

The block diagram of the sensor is shown in *Figure 1*.

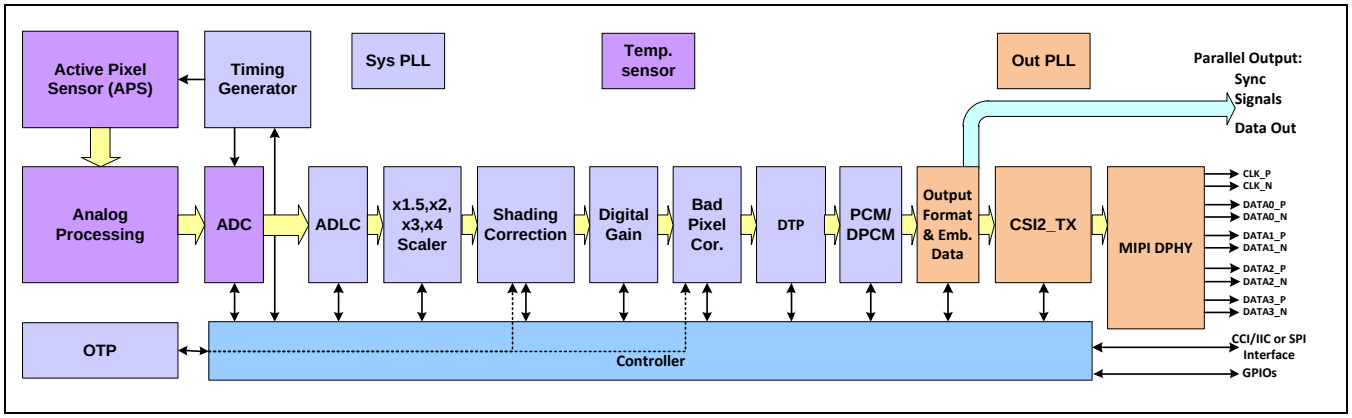


Figure 1 Function Block Diagram

The image sensor has an on-chip ADC. A column parallel ADC scheme is used for low-power analog processing.

The analog output signal of each pixel includes some temporal random noise caused by the pixel reset action and some fixed pattern noise caused by the in-pixel amplifier offset deviation. To eliminate these noise components, a Correlated Double Sampling (CDS) circuit is used before converting to digital.

The output from the ADC is a 10-bit value for each pixel in the array. The ADC output passes through a digital processing signal chain, which provides further data path corrections and applies digital gain. Digital scaling is performed before most digital processing to allow quadratic scale power reduction for core power in video modes. A shading correction block is used to compensate for color/brightness shading introduced by the lens or CRA curve mismatch. Low power, bad pixel correction block is used to fix pre-defined defects that are not handled perfectly by the host ISP bad pixel correction block such as bad pixel clusters and small level outliers. Additional functionality is provided that includes a deterministic pattern generator, a PCM/DPCM compressor and a MIPI CSI-2 frame formatter with embedded line support.

The sensor is interfaced using a set of control and status registers that can be used to control many aspects of the sensor behavior, including frame size, exposure and gain setting. These registers can be accessed through a CCI interface.

1.4 Device Operating Modes

The Sensor module has four operating modes (*Table 1*). Moving from one mode to another is achieved by issuing the appropriate mode command via the CCI serial control interface, the RSTN (XSHUTDOWN) signal changing state and the power supplies. By default, S5K3H7YX powers up with the CSI-2 serial data interface enabled. *Figure 2* defines the valid mode changes for the sensor module.

Table 1 Operating Mode Summary

Power State	Description
Power-off	Power supplies are turned off.
Hardware Standby	No communication with the sensor is possible. Internal core power shut-off by external VDDD power down.
Software Standby	CCI/SPI communication with sensor is possible. Core power is on. Entry to SW standby mode is either by mode_select or by software_reset CCI commands.
Streaming	The sensor module is fully powered and is streaming image data on the CSI-2 bus.

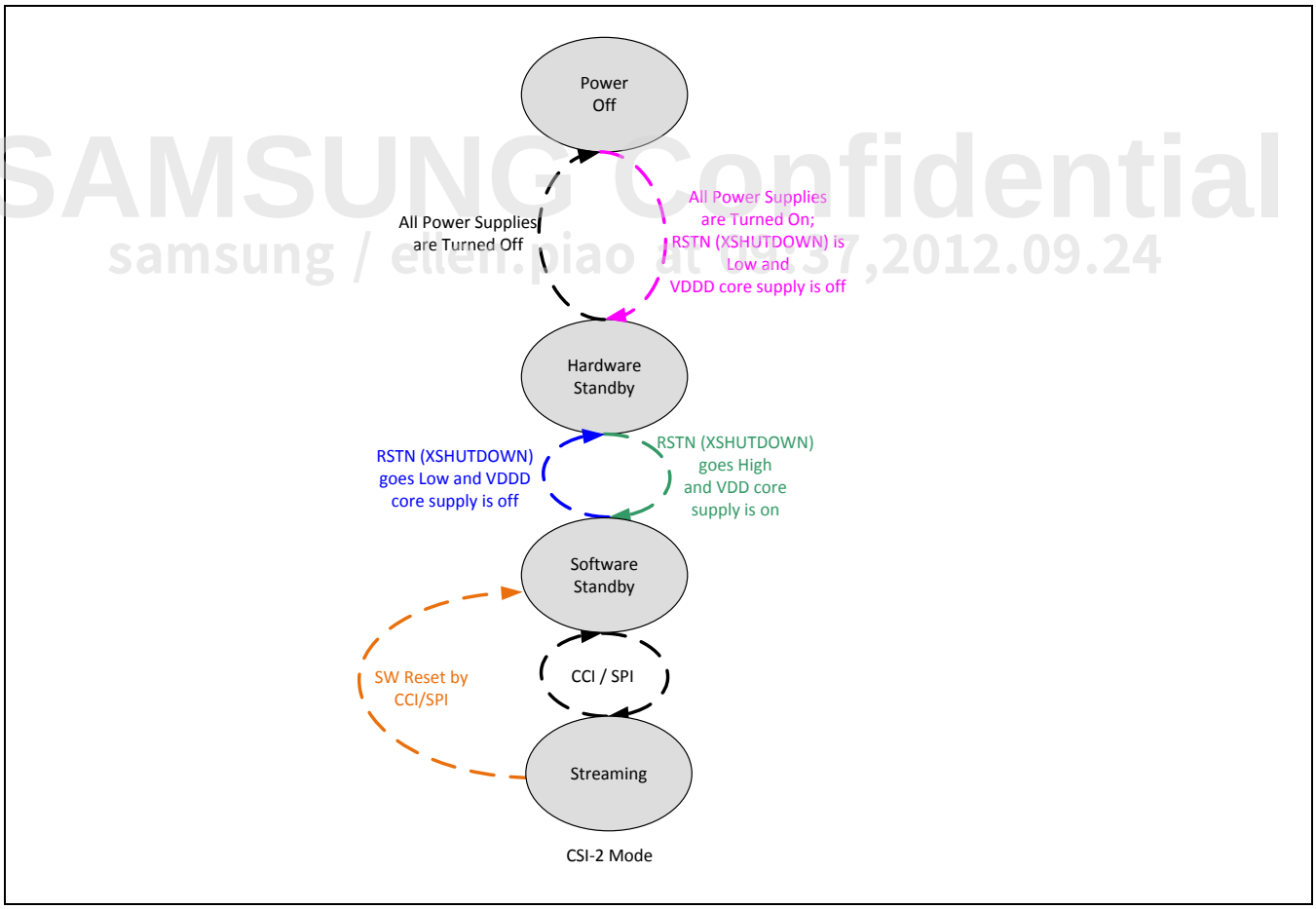


Figure 2 System State Diagram

2 Pad Configuration

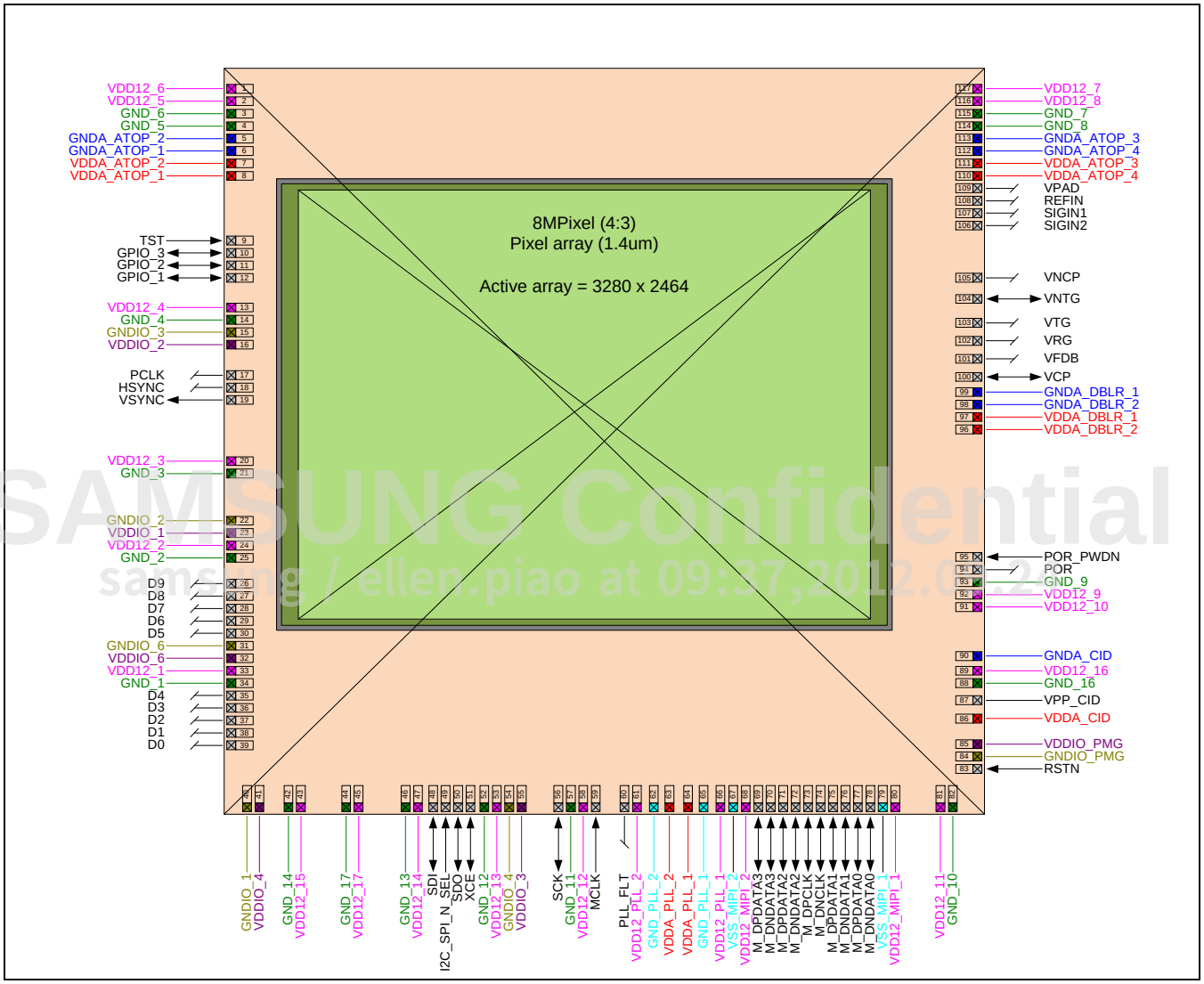


Figure 3 Pad Configuration

2.1 Pad Description

Table 2 Pad Description

Pad No	Pad Name	I/O	Description
83	RSTN	I	Master Reset, Active low (XSHUTDOWN)
59	MCLK	I	Input external 6-54Mhz clock
49	I2C_SPI_N_SEL	I	SPI/IIC Select (1: IIC, 0: SPI)
51	XCE	IOD	SPI mode: Serial communication enable / IIC mode: IIC slave address selection (0: 20h/21h 1: 5Bh/5Ah)
50	SDO	IOZ	SPI mode: Serial Data output (SPI) / IIC mode: leave open
48	SDI	IOD	SPI mode: Serial communication data input / IIC mode: IIC data
56	SCK	IOD	SPI mode: Serial communication clock input (SPI) / IIC mode: IIC input clock
12	GPIO_1	IOZ	General purpose I/Os: Input function: STRB_IN / GPI, Output function: STRB_OUT / Xenon / GPO / Pixel Data Output [1] in RAW 12
11	GPIO_2	IOZ	General purpose I/Os: Input function: STRB_IN / GPI, Output function: STRB_OUT / Xenon / GPO / Pixel Data Output [0] (LSB) in RAW 12
10	GPIO_3	IOZ	General purpose I/Os: Input function: STRB_IN / GPI, Output function: STRB_OUT / Xenon / GPO
73	M_DPCLK	AIO	MIPI clock lane positive
74	M_DNCLK	AIO	MIPI clock lane negative
77	M_DPDATA0	AIO	MIPI data lane 0 positive
78	M_DNDATA0	AIO	MIPI data lane 0 negative
75	M_DPDATA1	AIO	MIPI data lane 1 positive
76	M_DNDATA1	AIO	MIPI data lane 1 negative
71	M_DPDATA2	AIO	MIPI data lane 2 positive
72	M_DNDATA2	AIO	MIPI data lane 2 negative
69	M_DPDATA3	AIO	MIPI data lane 3 positive
70	M_DNDATA3	AIO	MIPI data lane 3 negative
60	PLL_FLT	AIO	Test: PLL Monitor PAD
87	VPP_CID	AIO	OTP Input Power mode: Programming Voltage (6.5V External VPP option); For read, VPP is tied to 2.8V or floating. Output Monitor mode: VPP monitors output during test mode.
109	VPAD	AIO	Test: Voltage monitoring
108	REFIN	AIO	Test: Reference signal of ADC sat test

Pad No	Pad Name	I/O	Description
107	SIGIN1	AIO	Test: Signal 1 of ADC sat test
106	SIGIN2	AIO	Test: Signal 2 of ADC sat test
105	VNCP	AIO	Test: Voltage doubler negative power
104	VNTG	AIO	Test: Boosted negative TG voltage
103	VTG	AIO	Test: Boosted TG voltage
102	VRG	AIO	Test: Boosted RG voltage
101	VFDB	AIO	Test: Boosted FD voltage
100	VCP	AIO	Voltage doubler positive power. Connect to 0.1uF cap.
19	VSYNC	IOZ	Vertical sync output for parallel and MIPI interface (optional)
18	HSYNC	IOZ	Horizontal sync output
17	PCLK	IOZ	Pixel clock output
39	D0	IOZ	Pixel Data Output (LSB in 10-bit mode)
38	D1	IOZ	Pixel Data Output (LSB in 9-bit mode)
37	D2	IOZ	Pixel Data Output (LSB in 8-bit mode)
36	D3	IOZ	Pixel Data Output
35	D4	IOZ	Pixel Data Output
30	D5	IOZ	Pixel Data Output
29	D6	IOZ	Pixel Data Output
28	D7	IOZ	Pixel Data Output
27	D8	IOZ	Pixel Data Output
26	D9	IOZ	Pixel Data Output (MSB in all modes)
9	TST	I	Test: EDS test configuration pin. Tie low in normal operation
95	POR_PWDN	I	POR circuit power down (low - POR is active, high - POR is disabled). From EVT0.1: Analog Ground. (Pin is disabled - POR off)
94	POR	AO	Test: POR monitor
33	VDD12_1	P	Digital Core Power (1.2V)
24	VDD12_2	P	Digital Core Power (1.2V)
20	VDD12_3	P	Digital Core Power (1.2V)
13	VDD12_4	P	Digital Core Power (1.2V)
2	VDD12_5	P	Digital Core Power (1.2V)
1	VDD12_6	P	Digital Core Power (1.2V)
117	VDD12_7	P	Digital Core Power (1.2V)
116	VDD12_8	P	Digital Core Power (1.2V)
92	VDD12_9	P	Digital Core Power (1.2V)
91	VDD12_10	P	Digital Core Power (1.2V)

Pad No	Pad Name	I/O	Description
81	VDD12_11	P	Digital Core Power (1.2V)
58	VDD12_12	P	Digital Core Power (1.2V)
53	VDD12_13	P	Digital Core Power (1.2V)
47	VDD12_14	P	Digital Core Power (1.2V)
43	VDD12_15	P	Digital Core Power (1.2V)
89	VDD12_16	P	Digital Core Power (1.2V)
45	VDD12_17	P	Digital Core Power (1.2V)
80	VDD12_MIPI_1	P	Mipi Digital Power (1.2V)
68	VDD12_MIPI_2	P	Mipi Digital Power (1.2V)
66	VDD12_PLL_1	P	PLL Digital Power (1.2V)
61	VDD12_PLL_2	P	PLL Digital Power (1.2V)
64	VDDA_PLL_1	P	PLL Analog Power (2.8V)
63	VDDA_PLL_2	P	PLL Analog Power (2.8V)
8	VDDA_ATOP_1	P	Analog Power (2.8V)
7	VDDA_ATOP_2	P	Analog Power (2.8V)
111	VDDA_ATOP_3	P	Analog Power (2.8V)
110	VDDA_ATOP_4	P	Analog Power (2.8V)
97	VDDA_DBLR_1	P	Analog Power (2.8V)
96	VDDA_DBLR_2	P	Analog Power (2.8V)
86	VDDA_CID	P	OTP Analog Power Read: 2.8V / Write (charge pump x1.5): 2.6V-2.9V / Write (charge pump x1): 3V-3.3V
23	VDDIO_1	P	IO Voltage (1.8V / 2.8V)
16	VDDIO_2	P	IO Voltage (1.8V / 2.8V)
55	VDDIO_3	P	IO Voltage (1.8V / 2.8V)
41	VDDIO_4	P	IO Voltage (1.8V / 2.8V)
32	VDDIO_6	P	IO Voltage (1.8V / 2.8V)
85	VDDIO_PMG	P	IO Voltage (1.8V / 2.8V)
34	GND_1	G	Digital Ground
25	GND_2	G	Digital Ground
21	GND_3	G	Digital ground
14	GND_4	G	Digital Ground
4	GND_5	G	Digital Ground
3	GND_6	G	Digital Ground
115	GND_7	G	Digital Ground

Pad No	Pad Name	I/O	Description
114	GND_8	G	Digital Ground
93	GND_9	G	Digital Ground
82	GND_10	G	Digital Ground
57	GND_11	G	Digital Ground
52	GND_12	G	Digital Ground
46	GND_13	G	Digital Ground
42	GND_14	G	Digital Ground
88	GND_16	G	Digital Ground
44	GND_17	G	Digital Ground
79	VSS_MIPI_1	G	MIPI Ground
67	VSS_MIPI_2	G	MIPI Ground
65	GND_PLL_1	G	MIPI Ground
62	GND_PLL_2	G	PLL Ground
6	GNDA_ATOP_1	G	Sensor Analog Ground
5	GNDA_ATOP_2	G	Sensor Analog Ground
113	GNDA_ATOP_3	G	Sensor Analog Ground
112	GNDA_ATOP_4	G	Sensor Analog Ground
90	GNDA_CID	G	Sensor Analog Ground (for OTP)
99	GNDA_DBLR_1	G	Sensor Analog Ground
98	GNDA_DBLR_2	G	Sensor Analog Ground
40	GNDIO_1	G	IO Ground
22	GNDIO_2	G	IO Ground
15	GNDIO_3	G	IO Ground
54	GNDIO_4	G	IO Ground
31	GNDIO_6	G	IO Ground
84	GNDIO_PMG	G	IO Ground

3 Pixel Array Information

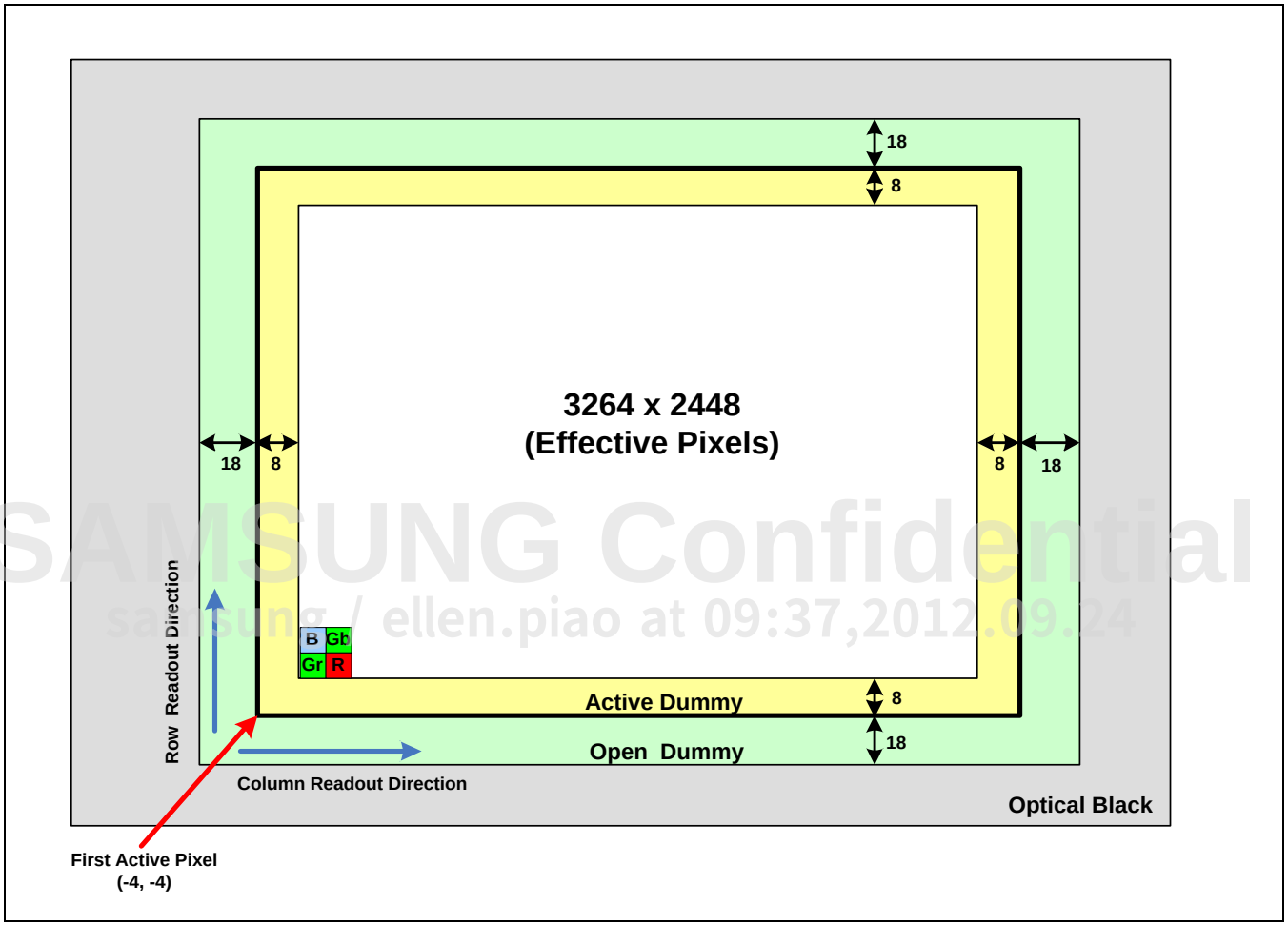


Figure 4 Pixel Array Information

NOTE: Top view on chip.
Displayed image will be flipped.

4 Functional Operation Modes

S5K3H7YX can support a wide range of operation modes.

Operation mode is function of several mode parameters such as:

- Interface bandwidth
- Requested sensor output size and sensor operation mode
- CIS output size and number of bits per pixel e.g. RAW10, RAW8+ (8 bit in DPCM/PCM compression)
- Required VBlank time
- Power consumption limitations e.g. use single PLL, limited MIPI lanes, system lower power modes.

Typical operation modes and related typical settings are presented in this table.

Table 3 Typical Functional Operation Modes

Mode	Best Frame Rate	Horizontal FOV loss	CiS Output		Output Parameters			Sensor Output						MIPI Parameters	
			Output Width	Output Height	VBlank [uS]	Output Bittage	Bit Clk [Mhz]	WOI Width	H Analog Scale	H Dig Scale	WOI Height	V Analog Scale	V Dig Scale	Num. Lanes	Cont. Clk
8M 4:3	30.00	0%	3264	2448	3000	10	940	3264	1	1	2448	1	1	3	Yes
6M 16:9	60.12	0%	3264	1836	250	10	1000	3264	1	1	1836	1	1	4	Yes
6M 16:9	30.02	0%	3264	1836	9500	10	880	3264	1	1	1836	1	1	4	Yes
2.7M 16:9 (D.I.S)	60.06	0%	2176	1224	570	10	1000	3264	1	1.5	1836	1	1.5	2	Yes
2.7M 16:9 (No D.I.S)	60.06	12%	1920	1080	2500	10	1000	2880	1	1.5	1620	1	1.5	2	Yes
FHD (Win)	60.09	41%	1920	1080	2500	10	1000	1920	1	1	1080	1	1	2	Yes
HD 1.5M (D.I.S)	120.11	0%	1632	918	250	10	880	3264	2	1	1836	2	1	3	Yes
VGA+	120.73	0%	816	612	250	10	880	3264	4	1	2448	4	1	1	Yes
VGA (Win)	120.36	22%	640	480	1990	10	880	2560	4	1	1920	4	1	1	Yes
QVGA+	240.23	0%	400	306	1390	10	880	3264	8	1	2448	8	1	1	Yes
QVGA (Win)	240.23	22%	320	240	1960	10	880	2560	8	1	1920	8	1	1	Yes

In case of constraint such as for example use of max MIPI 660Mbits/lane modes will be different;

Table 4 Typical Functional Operation Modes for MIPI @ 660Mbits/lane

Mode	Best Frame Rate	Horizontal FOV loss	CiS Output		Output Parameters			Sensor Output						MIPI Parameters	
			Output Width	Output Height	VBlank [uS]	Output Bittage	Bit Clk [Mhz]	WOI Width	H Analog Scale	H Dig Scale	WOI Height	V Analog Scale	V Dig Scale	Num. Lanes	Cont. Clk
8M 4:3	30.06	0%	3264	2448	1000	10	660	3264	1	1	2448	1	1	4	Yes
6M 16:9	60.12	0%	3264	1836	250	10	1000	3264	1	1	1836	1	1	4	Yes
6M 16:9	30.12	0%	3264	1836	9000	10	660	3264	1	1	1836	1	1	4	Yes
2.7M 16:9 (D.I.S)	60.06	0%	2176	1224	570	10	660	3264	1	1.5	1836	1	1.5	3	Yes
2.7M 16:9 (No D.I.S)	60.06	12%	1920	1080	2500	10	660	2880	1	1.5	1620	1	1.5	3	Yes
FHD (Win)	60.09	41%	1920	1080	2500	10	660	1920	1	1	1080	1	1	3	Yes
HD 1.5M (D.I.S)	120.11	0%	1632	918	250	10	660	3264	2	1	1836	2	1	4	Yes
VGA+	120.73	0%	816	612	250	10	660	3264	4	1	2448	4	1	2	Yes
VGA (Win)	120.36	22%	640	480	1990	10	660	2560	4	1	1920	4	1	1	Yes
QVGA+	240.23	0%	400	306	1390	10	660	3264	8	1	2448	8	1	1	Yes
QVGA (Win)	240.23	22%	320	240	1960	10	660	2560	8	1	1920	8	1	1	Yes

NOTE: 16:9 60 fps modes are not supported in EVT0. Please contact SEC for more information.

5 Video Timing

5.1 Overview

The output image size is a function of the size of the addressed region of the pixel array and the sub-sampling programmed factor. *Figure 5* shows the video timing overview.

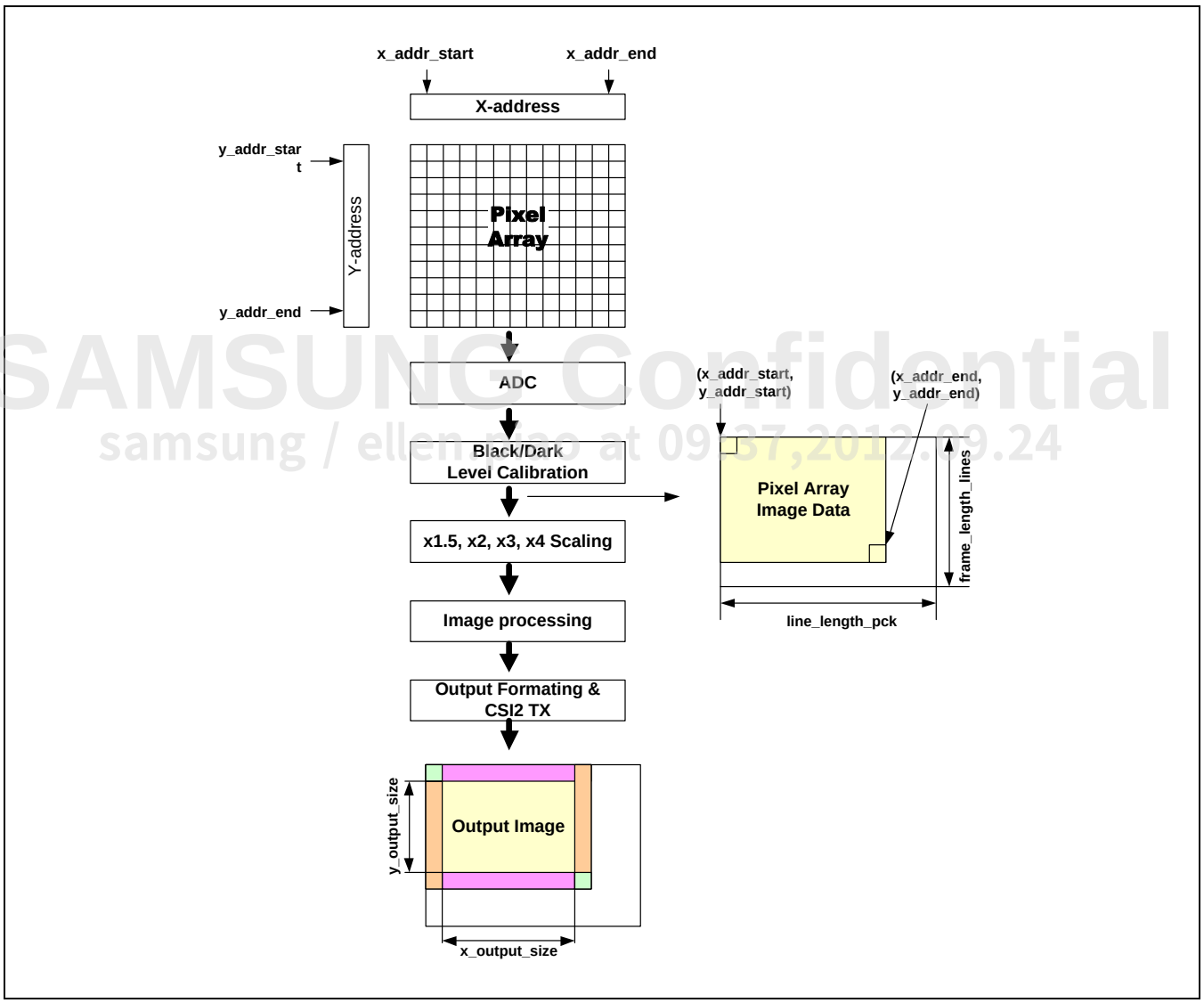


Figure 5 Video Timing Overview

5.2 Pixel Array Addresses

Addressable pixel array is defined as the pixel address range to be read. The addressable pixel array can be assigned anywhere on the pixel array. The addressed region of the pixel array is controlled by the h_addr_start, v_addr_start, h_addr_end and v_addr_end register.

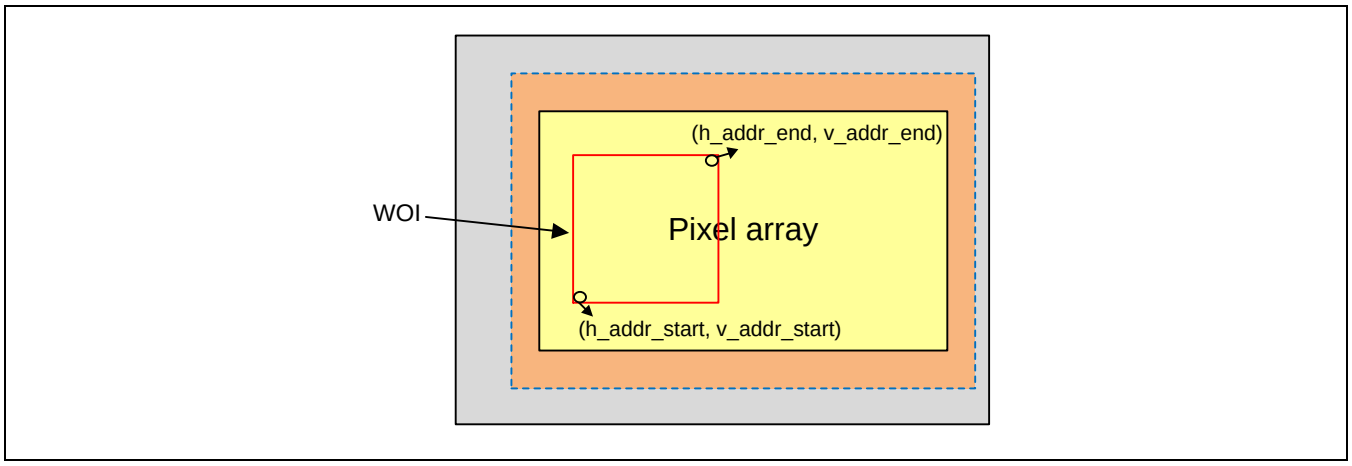


Figure 6 Window of Interest on Pixel Array

5.3 Horizontal Mirror and Vertical Flip

The pixel data is normally read out from left to right in the horizontal direction and from top to bottom in the vertical direction. By changing the mirror/flip mode, the read-out sequence can be reversed, and the resulting image can be flipped like a mirror image. Pixel data is then read out from right to left in horizontal mirror mode and from bottom to top in vertical flip mode. The horizontal mirror and the vertical flip mode can be programmed by the image orientation register.

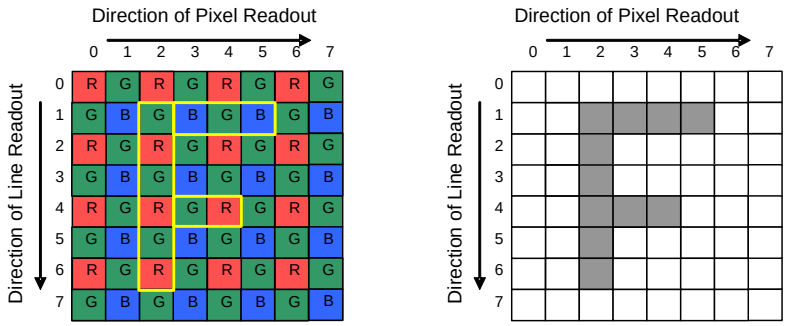
The sensor module supports four possible pixel readout orders, as described in the sections below:

a) Standard Readout
The addressed region of the horizontal pixel data output is controlled by the x_addr_start and x_output_width registers. The addressed region of the vertical pixel data output is controlled by the y_addr_start and y_output_depth registers.

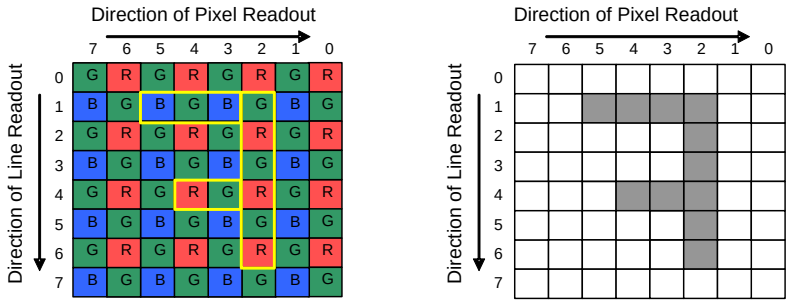
b) Horizontally Mirrored Readout
The addressed region of the horizontal pixel data output is controlled by the x_addr_end, and x_output_width registers, and the vertical pixel data output is the same as that of the standard readout.

c) Vertical Flipped Readout
The horizontal pixel data output is same as that of the standard readout, and the addressed region of the vertical pixel data output is controlled by the y_addr_end and y_output_depth registers.

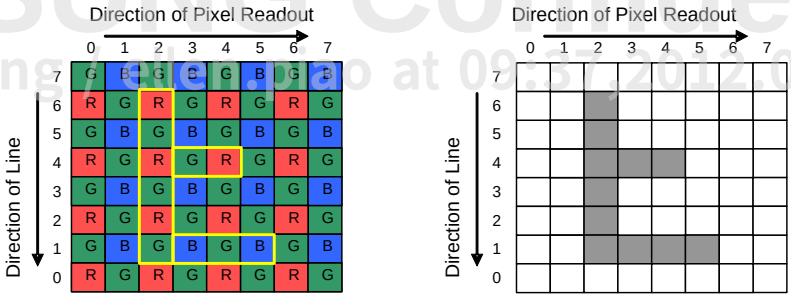
d) Horizontally Mirrored and Vertically Flipped Readout
The addressed region of the horizontal pixel data output is controlled by the x_addr_end and x_output_width registers. The addressed region of the vertical pixel data output is controlled by the y_addr_end and y_output_depth registers.



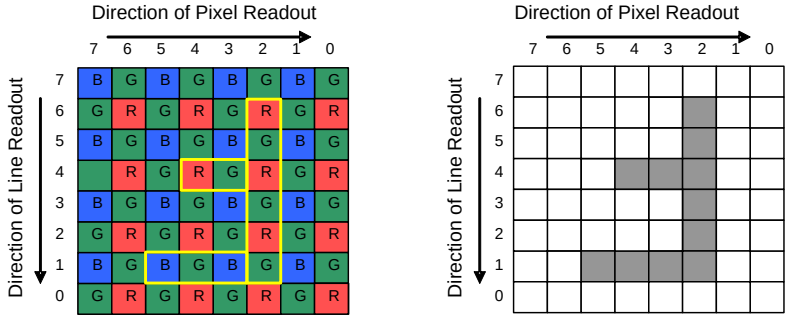
a) Standard Readout



b) Horizontally Mirrored Readout



c) Vertically Flipped Readout



d) Horizontally Mirrored and Vertically Flipped Readout

Figure 7 Horizontal Mirror and Vertical Flip

5.4 Sub-Sampled Readout

By programming the x and y odd and even increment registers (x_even_inc, x_odd_inc, y_even_inc, y_odd_inc), the sensor can be configured to read out sub-sampled pixel data.

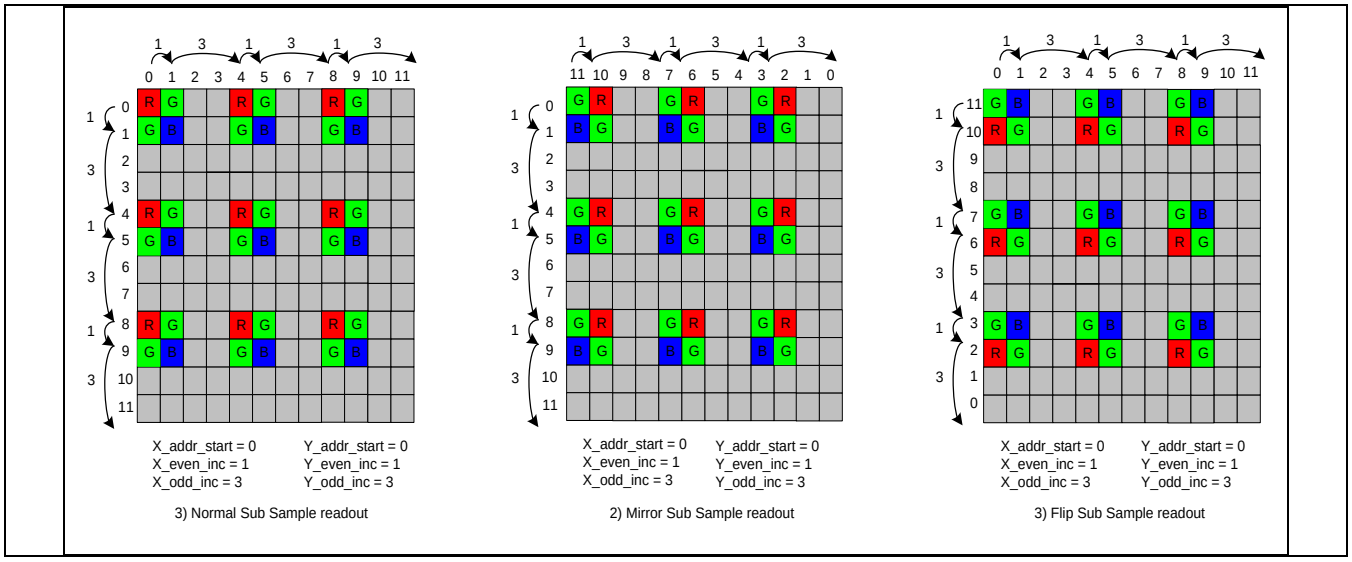


Figure 8 Example of Sub-Sampled Readout

5.4.1 Averaged Sub-sampled Readout

By programming the averaged sub-sampling enable register, the sensor can be configured to read out pixel data that has been averaged with adjacent pixels.

5.5 Frame Rate Control (Virtual Frame)

The line rate and the frame rate can be changed by varying the size of the virtual frame. The virtual frame's width and depth are controlled by the line_length_pck and frame_length_lines register. The horizontal and vertical blanking times (horizontal blanking time: line_length_pck – x_output_size, vertical blanking time: frame_length_lines – y_output_size) should meet system requirements.

Frame rate = vt_pix_clk/(frame_length_lines × line_length_pck)

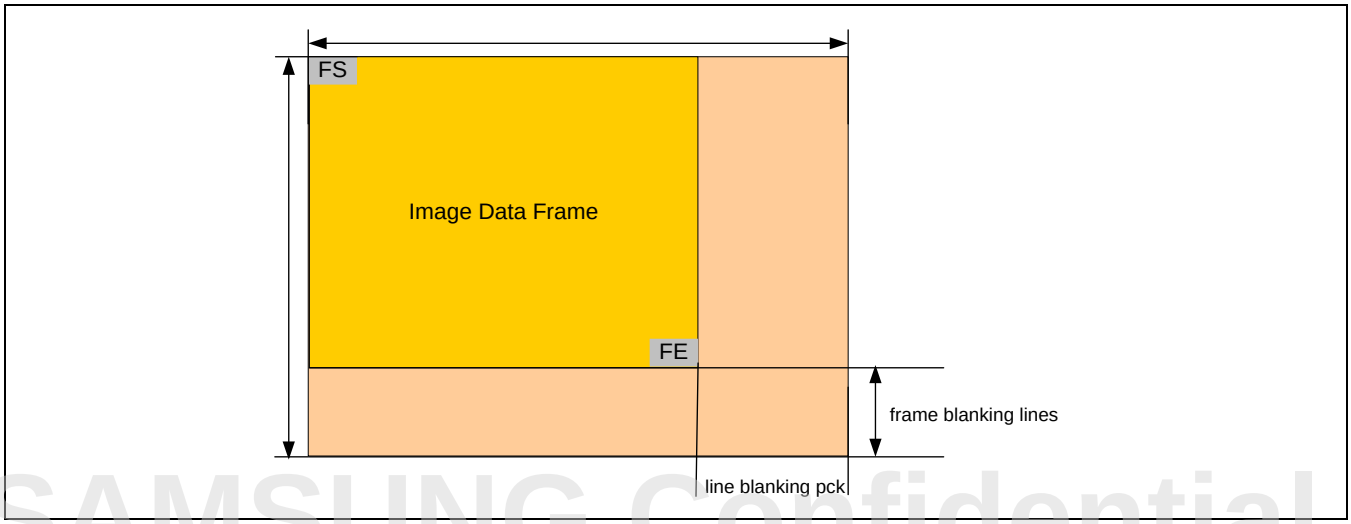


Figure 9 Virtual Frame Format Example

5.5.1 Integration Time Control (Electronic Shutter Control)

The pixel integration time is controlled by the shutter operation. During the shutter operation, the amount of time – integration time – is determined by the column Step Integration Time Control Register (fine_integration_time) and the line Step Integration Time Control Register (coarse_integration_time). The total integration time of the sensor module can be calculated using the following formula:

Total_integration_time = {coarse_integration_time × line_length_pck + fine_integration_time + const} × pclk period[sec]

const parameter is calculated internally according to sensor settings and is fixed per sensor configuration. const parameter can be checked for any configuration by read of reg_gtg_aig_tx_ptr1 register (0xF470).

5.6 PLL and Clock Generator

The S5K3H7YX clock system uses system phase-locked loop (PLL), system clock dividers, output PLL, and output clock dividers to generate all internal clocks from a single master input clock running between 6 MHz and 54 MHz.

Output interface clocks may be generated by the System PLL. In this case the Output PLL will be powered-down and overall system power reduced.

Alternatively dedicated Output PLL may be used for maximal flexibility in interface frequency and for EMI avoidance. The maximum PLL VCO frequency is 1 GHz.

Clock dividers are used to generate all system clocks from one or two PLL sources.

The charge pump clock and the ADC clock are used for A/D conversion circuits, pixel clock and pixel clock/2 are used for pixel processing and sensor control. Bit clock and output clock are set according to the required output rate.

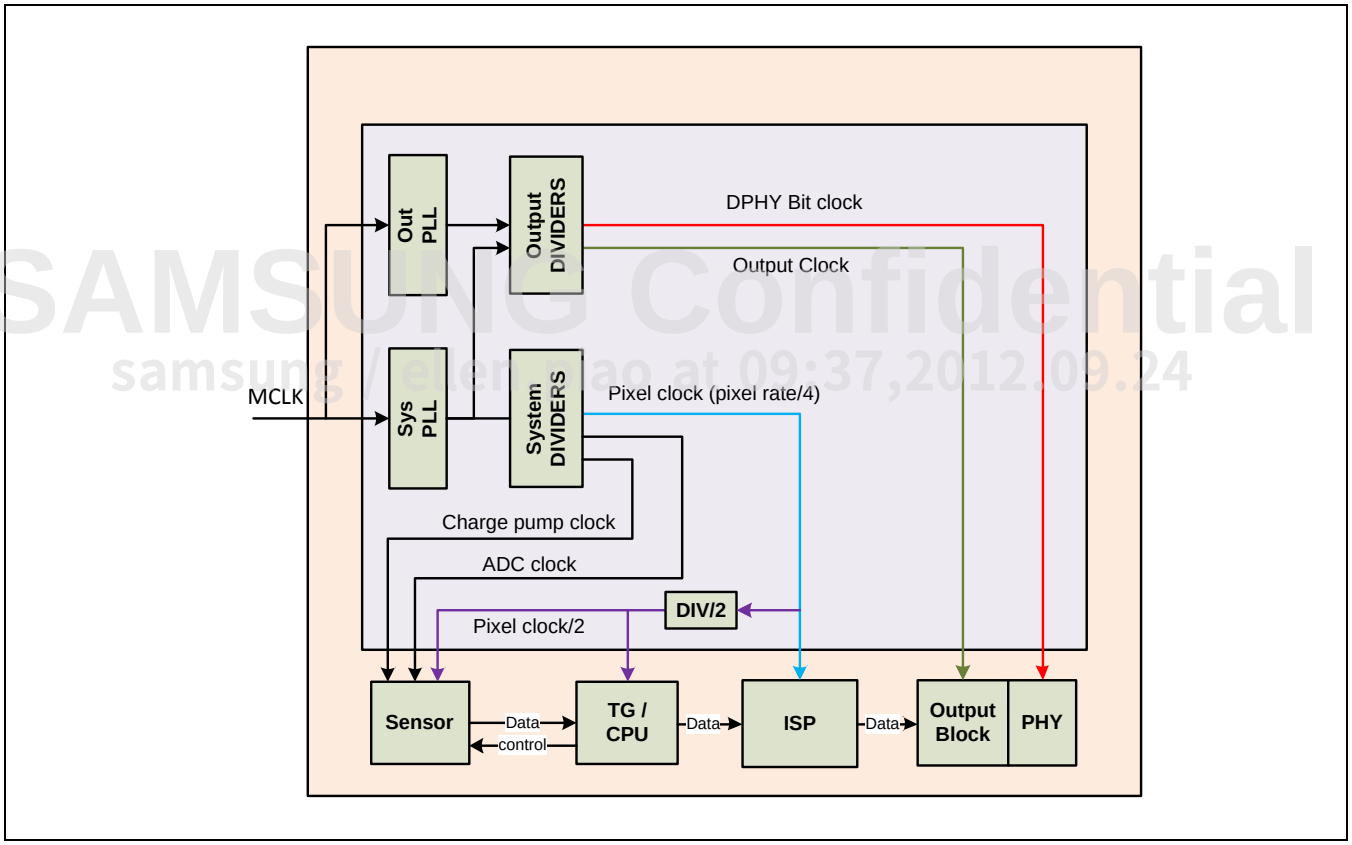


Figure 10 Clock System Block Diagram

5.6.1 Clock Relationships

The host provides the external input clock (with values varying between 6-54 MHz) in addition to setting dividers and multipliers in order to get the required video timing and output pixel clocks.

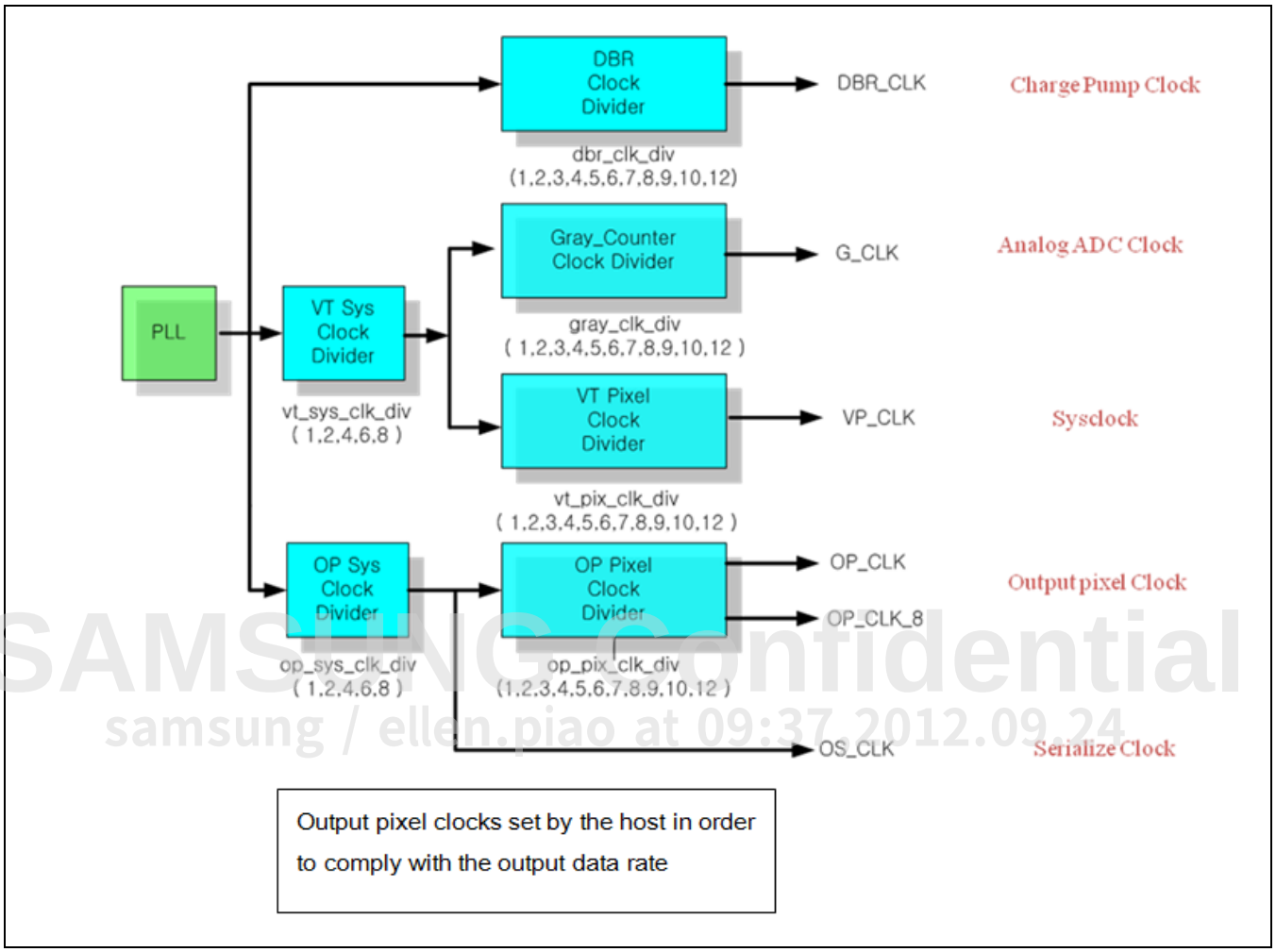


Figure 11 Clock Relationships

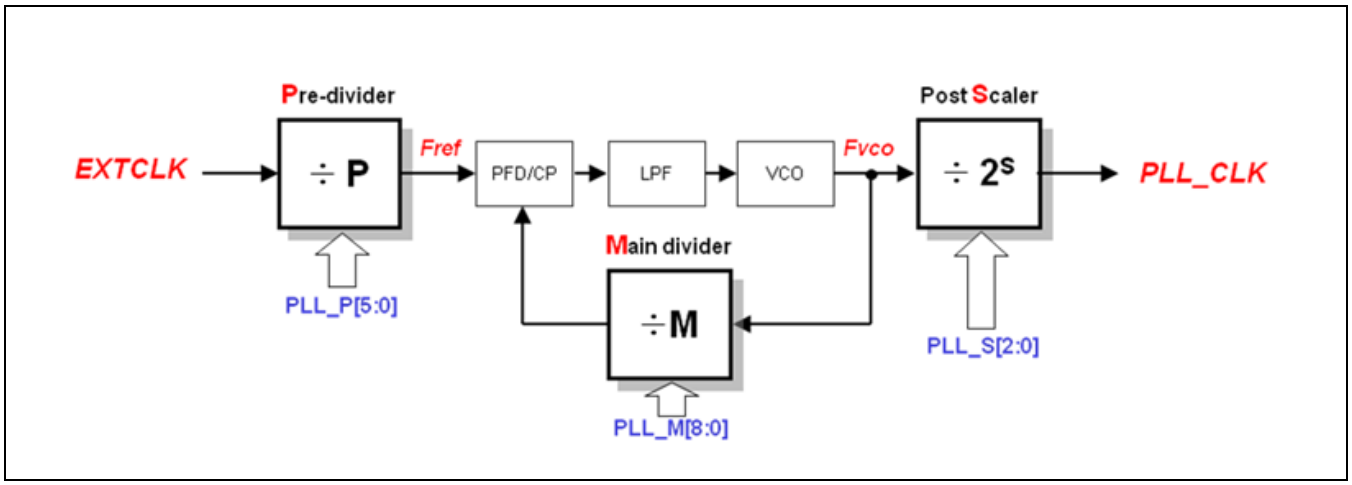


Figure 12 PLL Frequency Synthesis

$$PLL\_CLK = EXTCLK \times \left[\frac{M}{P} \times \frac{1}{2^S}\right]$$

NOTE: PLL_S = 0 and is not controllable. Post dividers are used for lower frequency synthesis.

Table 5 PLL Component Output Frequency

Parameter	Min.	Typ.	Max.	Unit	Remarks
Input frequency range	6	–	54	MHz	EXTCLK frequency range
Reference frequency range	3	–	6	MHz	Output of pre-divider (Fref)
VCO frequency range	500	–	1000	MHz	Output of PLL multiplier VCO oscillation range (Fvco)
PLL output frequency range	31.25	–	1000	MHz	Output of PLL post scaler. Minimum value is just for test. (S ≥ 4)

NOTE: For more information about the PLL and clock system control, refer to the application note.

5.6.2 Master Clock Waveform Diagram

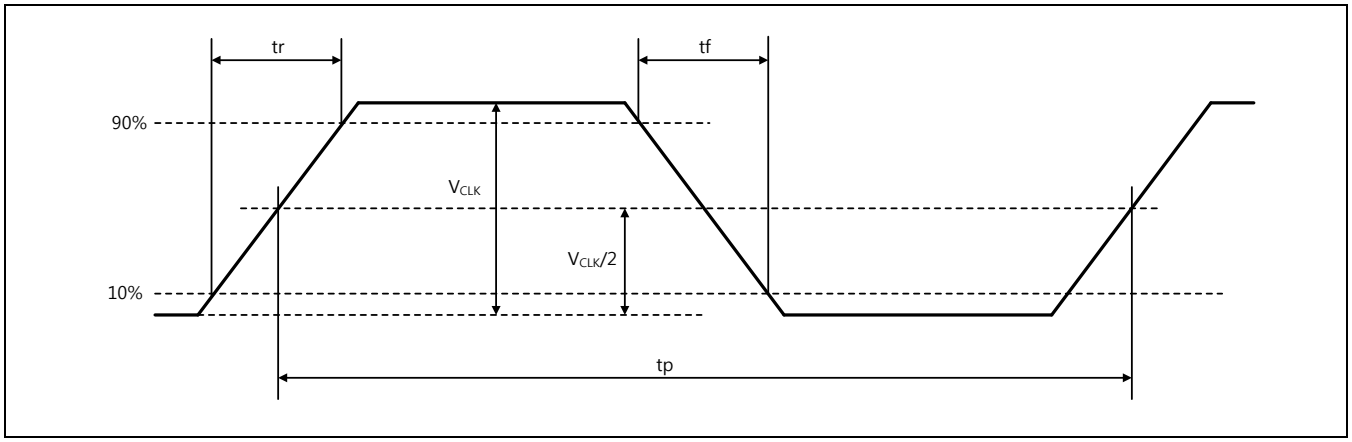


Figure 13 Master Clock Waveform Diagram

MCLK is the input clock to the S5K3H7YX sensor, sometimes refer as EXTCLK.

Parameter	Symbol	Min.	Typ.	Max.	Unit	Comment
MCLK clock frequency	EXTCLK	6	–	54	MHz	–
MCLK period	tp	18.52	41.6	166.6	ns	–
MCLK rise/fall time	tr/tf	–	–	6		–
MCLK jitter (periodic)	Tjitter	–	–	200	ps	–
MCLK jitter (peak-to-peak)	–	–	–	0.1 V_{CLK}	V	–

6 Control Interface

S5K3H7YX control is done using register writes.

S5K3H7YX can be configured using the I2C_SPI_N_SEL pin, to be controlled using the Camera Control Interface (CCI) or SPI control interface.

Table 6 SPI/I2C PAD Sharing

SPI	I2C
SDI	SDA
SCK	SCL
XCE	I2C_ID
SDO	–
I2C_SPI_N_SEL	

6.1 SPI Control Interface

The S5K3H7YX may use the SPI interface for control registers communication.

SPI interface is described in the diagram below.

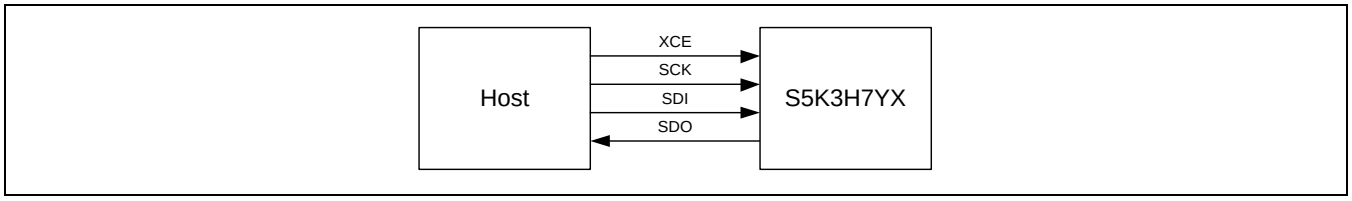


Figure 14 SPI Control Interface

The following table describes SPI signals:

Pin Name	Description
XCE	Serial communication enable
SCK	Serial communication clock input
SDI	Serial data input
SDO	Serial data output

If it is not necessary to read the control registers and chip ID, the SDO pad can be left unconnected.

The SPI control interface implemented in S5K3H7YX will be presented in detail in the next section.

6.1.1 SPI Timing Definitions

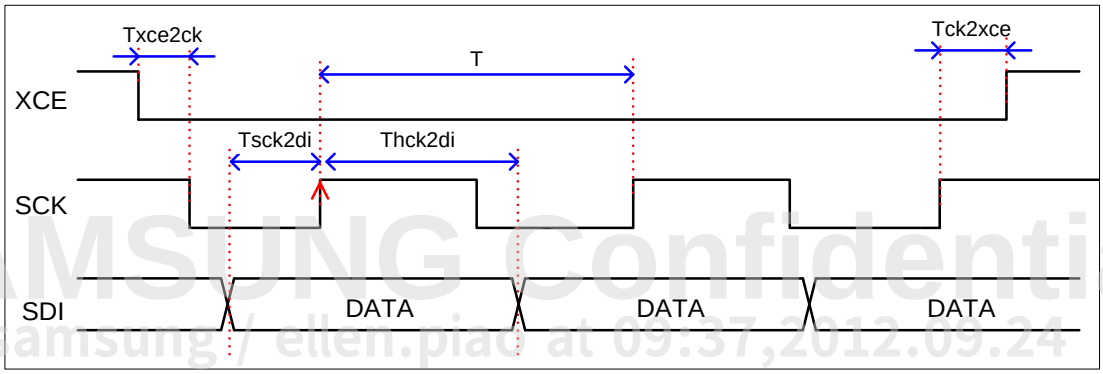


Figure 15 SPI WRITE Timing Diagram Mode 11

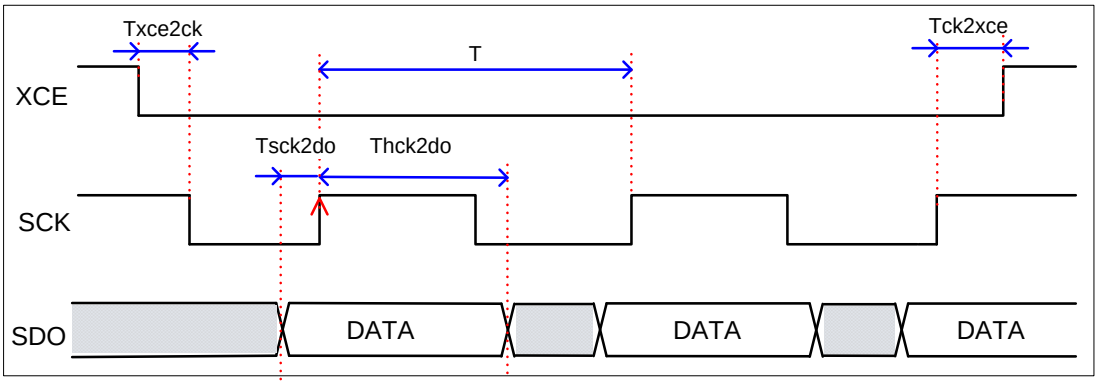


Figure 16 SPI READ Timing Diagram Mode 11

Table 7 SPI WRITE/READ Timing Specification

Description	Symbol	Min.	Typ.	Max.	Unit
MCLK (external clock) Frequency	Fext	6	–	54	MHz
SPI clock frequency	F (1)	–	–	Fext/3	
	F (2)	–	–	10	
	F (3)	–	–	18	
SPI clock period	T	1/F	–	–	nSec
SPI clock duty cycle	Tdc	45	–	55	%
XCE negedge to SCK edge	Txce2ck	T	–	–	nSec
SCK posedge to XCE edge	Tck2xce	2T	–	–	
SCK to SDI setup time	Tsck2di	7	–	–	
SCK to SDI hold time	Thck2di	5	–	–	
SCK to SDO setup time	Tsck2do	T/2-20	–	–	
SCK to SDO hold time	Thck2do	T/2	–	–	

NOTE:

1. External clock is used
2. PLL stable. Internal system clock set to > 60 MHz.
3. PLL stable. Internal system clock set to max 110 MHz

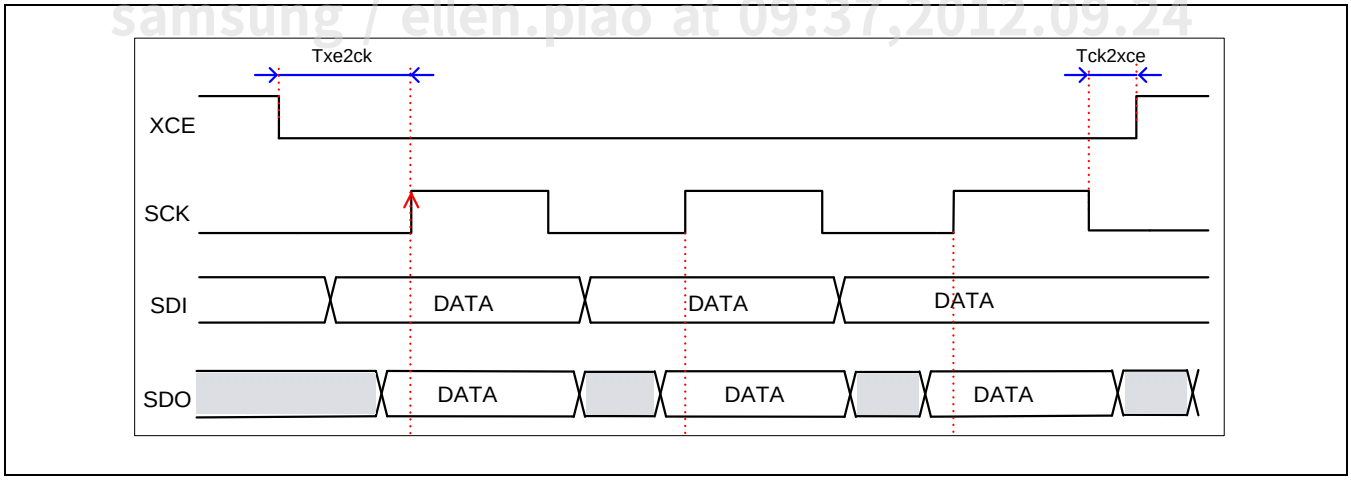


Figure 17 SPI WRITE/READ Mode 00

6.1.2 SPI Sequences

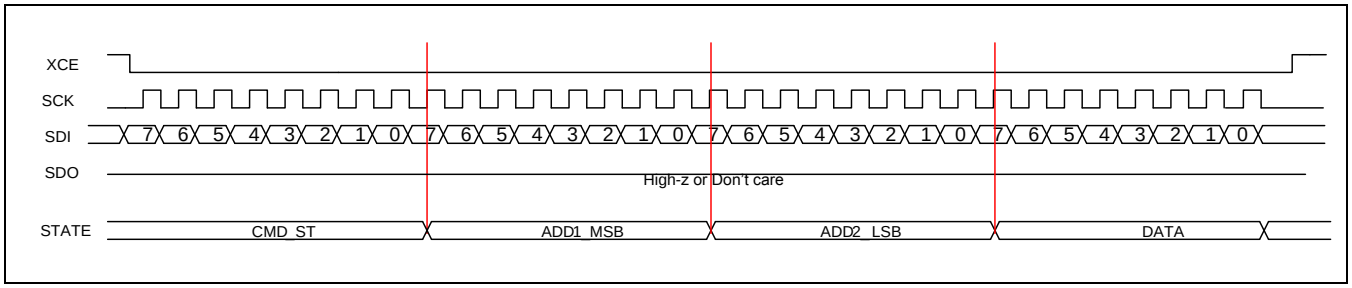


Figure 18 SPI WRITE sequence (1 cycle)

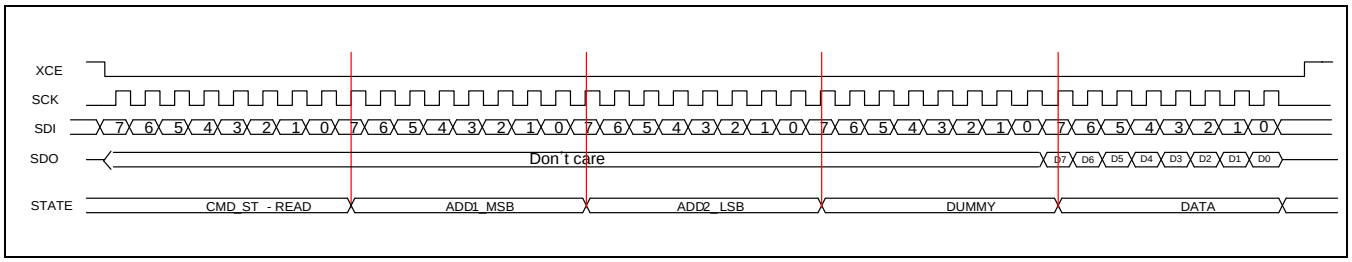


Figure 19 SPI READ

6.2 Camera Control Interface (CCI)

S5K3H7YX supports the Camera Control Interface (CCI), which is an I2C fast-mode compatible interface for controlling the transmitter. S5K3H7YX always acts as a slave in the CCI bus. CCI is capable of handling several slaves in the bus, but multi-master mode is not supported. Typically, only the receiver and transmitter are connected to the CCI bus. This makes a pure SW implementation possible.

Typically the CCI is separate from the system I2C bus, but I2C-compatibility ensures that it is also possible to connect the transmitter to the system I2C bus. CCI is a subset of the I2C protocol, including the minimum combination of obligatory features for the I2C slave device specified in the I2C specification. Therefore, transmitters complying with the CCI specification can also be connected to the system I2C bus. However, it is important to ensure that the I2C masters do not try to utilize these I2C features, which are not supported in transmitters complying with the CCI specification. Each transmitter conformed to the CCI specification may have additional features implemented to support I2C.

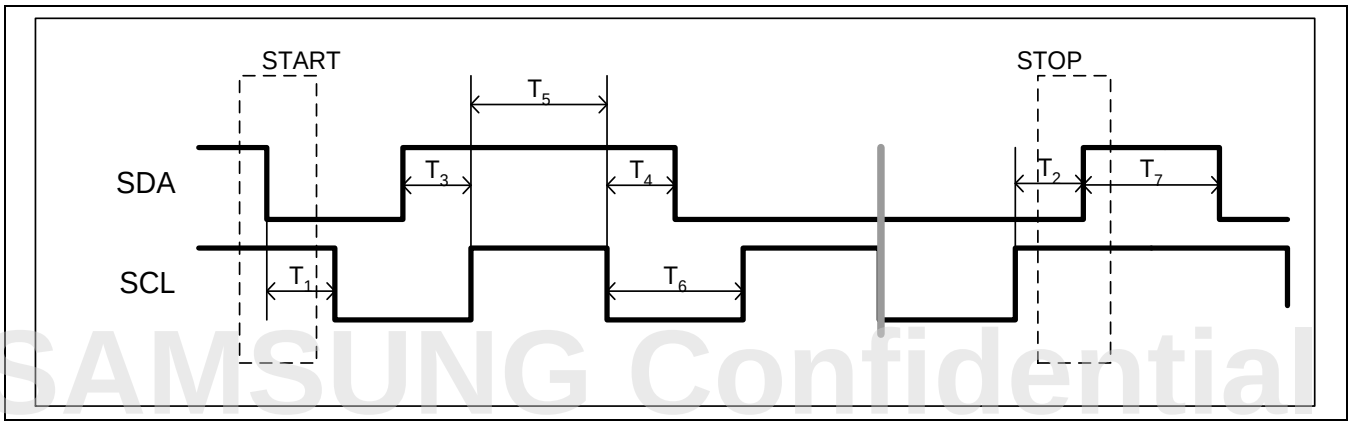


Figure 20 I2C Timing

Table 8 I2C Standard Mode Timing Specifications

Symbol	Parameter	Min.	Max.	Unit
–	SCL clock frequency	0	100	kHz
T1	Hold time for START condition	4.0	–	µs
T2	Setup time for STOP condition	4.0	–	
T3	Data setup time	250	–	ns
T4	Data hold time	0	3.45	µs
T5	High period of the SCL clock	4.0	–	
T6	Low period of the SCL clock	4.7	–	
T7	Bus free time between STOP and START conditions	4.7	–	
–	Rise time for both SDA and SCL signals	–	1000	ns
–	Fall time for both SDA and SCL signals	–	300	
CB	Capacitive load for each bus line	–	400	pF

Table 9 I2C Fast Mode Timing Specifications

Symbol	Parameter	Min.	Max.	Unit
–	SCL clock frequency	0	400	kHz
T1	Hold time for START condition	0.6	–	µs
T2	Setup time for STOP condition	0.6	–	
T3	Data setup time, external clock (MCLK) 12 Mhz and above	0.1	–	µs
	Data setup time, external clock (MCLK) below 12 Mhz	0.25	–	µs
T4	Data hold time	0	0.9	µs
T5	High period of the SCL clock	0.6	–	
T6	Low period of the SCL clock	1.3	–	
T7	Bus free time between STOP and START conditions	1.3	–	
–	Rise time for both SDA and SCL signals	–	300	ns
–	Fall time for both SDA and SCL signals	–	300	
CB	Capacitive load for each bus line	–	400	pF

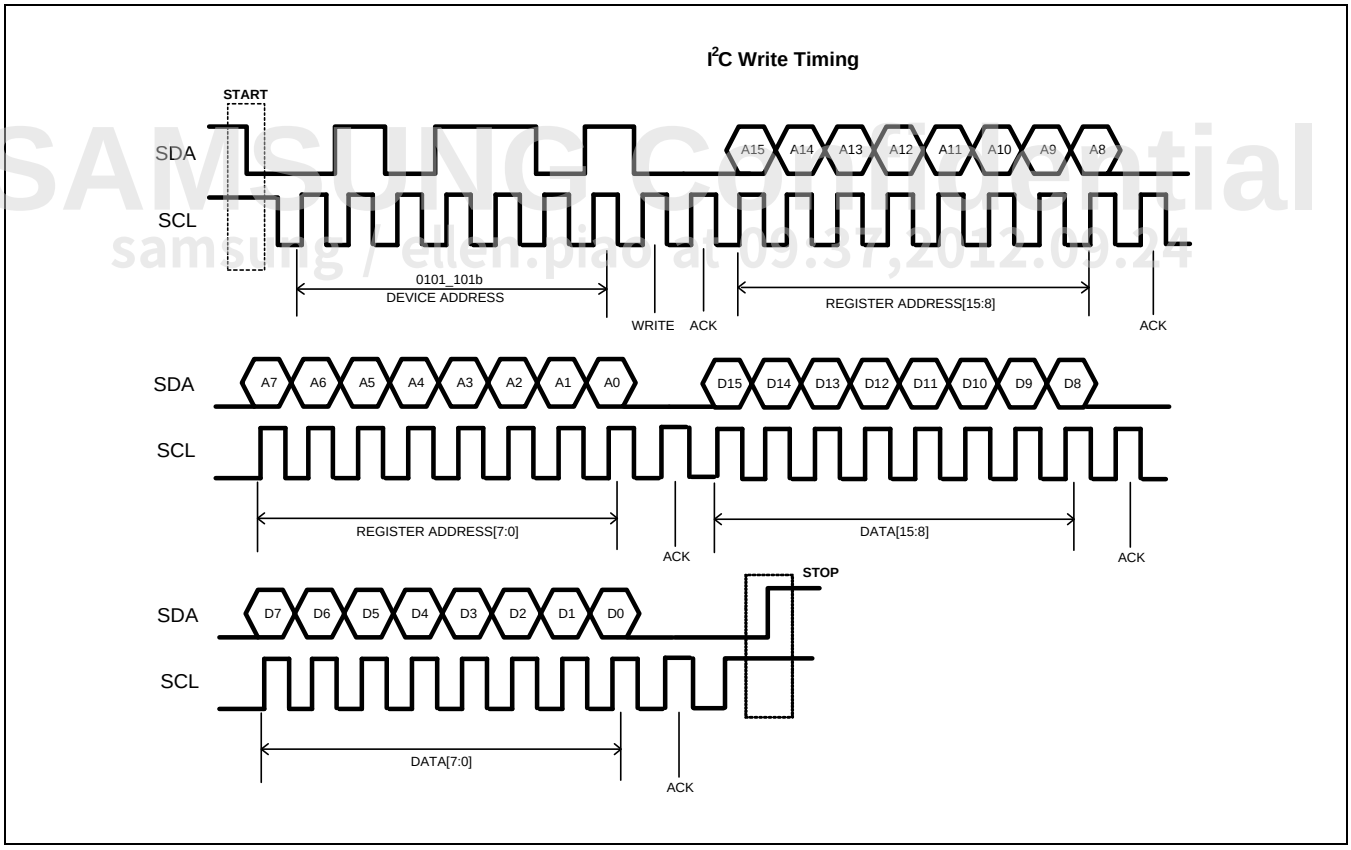


Figure 21 I2C Write Timing Example

NOTE: The device address can be changed by pin configuration of I2C_ID, as described in the pad description.

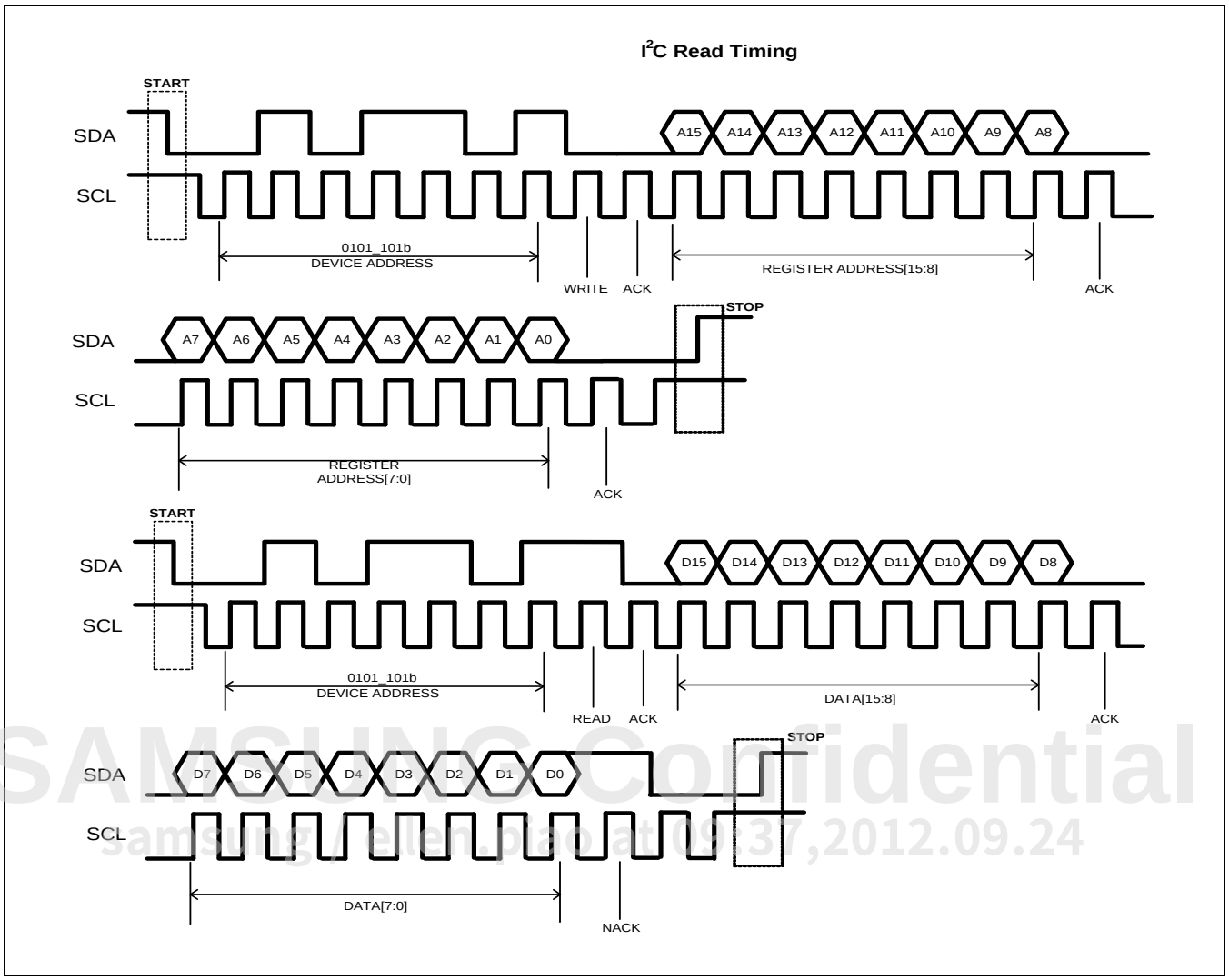


Figure 22 I2C Read Timing Example

NOTE: The device address can be changed by the pin configuration of I2C_ID, as described in the pad description.

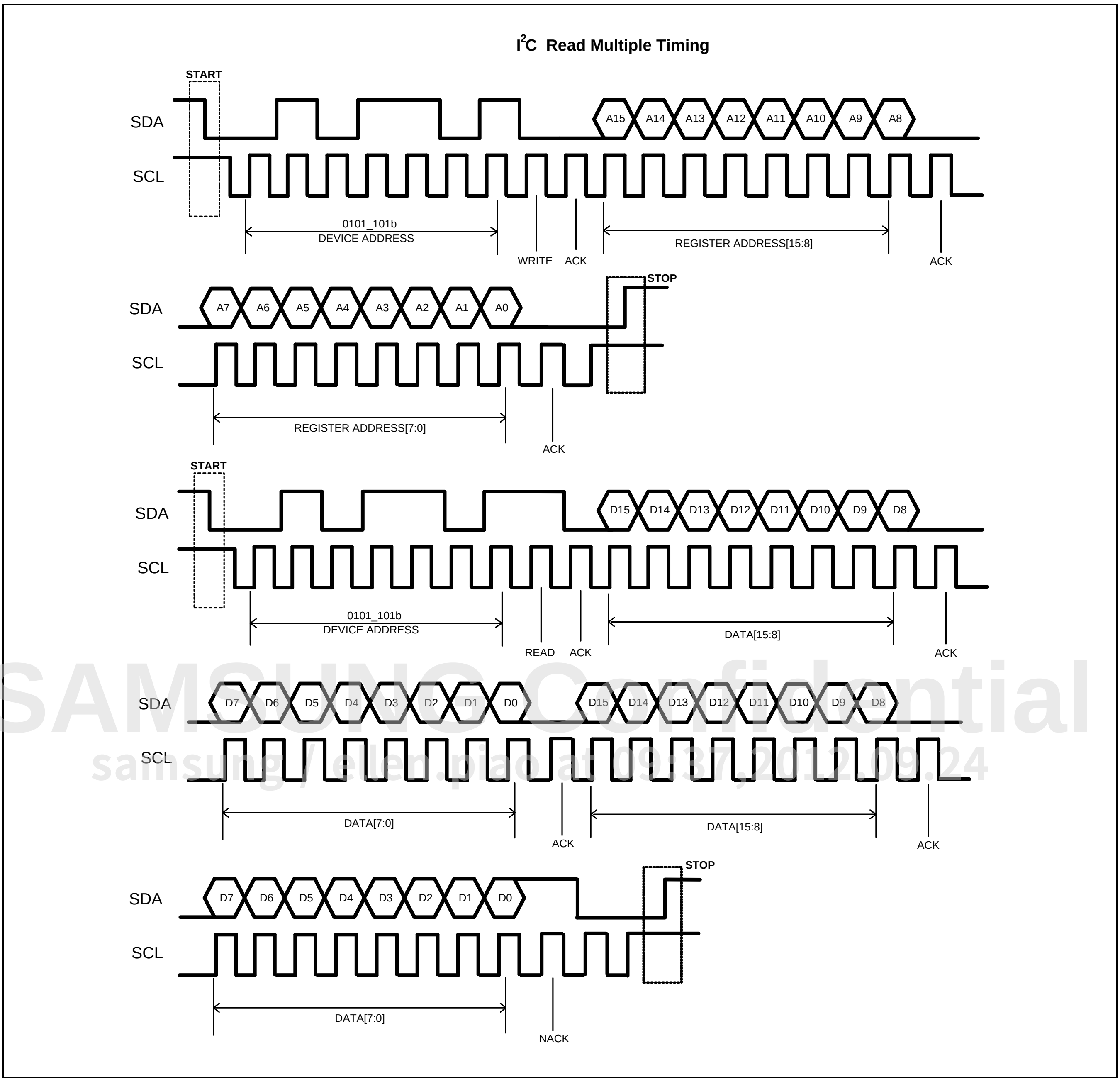


Figure 23 I2C Read Multiple Timing Example

NOTE: The device address can be changed by the pin configuration of I2C_ID, as described in the pad description.

It is possible to configure up to two I2C slave addresses using I2C_ID pins.

Table 10 I2C ID Address (XCE Pad)

XCE	Slave Address (7-bit + Read Mode)	Slave Address (7-bit + Write Mode)	Comment
0	0010_0001b/21h	0010_0000b/20h	Address 1
1	0101_1011b/5Bh	0101_1010b/5Ah	Address 2

7 Power Up/Down Sequence

7.1 Power-Up Sequence

The digital and analog supply voltages can be powered up in any order, e.g., VDDD/VDDIO then VDDA or VDDA/VDDIO then VDDD.

On power up, RSTN (XSHUTDOWN) should be low when the power supplies are brought up, then the sensor module will go into hardware standby mode.

The assertion of RSTN ensures that the CCI/SPI register values are initialized correctly to their default values. The MCLK clock can either be initially low and then enabled during software standby mode or MCLK can be a free running clock.

NOTE: (1) At hardware standby mode external VDDD should be OFF.
(2) For minimal SW standby power external clock (MCLK) should be off
(3) In case Software standby mode is desired after power up it should be initiated by register configuration (see S5K3H7YX application notes for details)

Table 11 Power-Up Sequence Timing Constraints (Serial Output Case)

Constant	Label	Min.	Max.	Unit
VDDA/VDDD/VDDIO rising time	t0	VDDA/VDDD/VDDIO may rise in any order. The rising separation can vary from 0ns to indefinite. If RSTN is high during VDDD rising then VDDD max rising time is 2000 ns		ns
RSTN (XSHUTDOWN) rising to VDDD rising	t1	0.0	VDDD rising and RSTN rising can be in any order	
VDDD rising to RSTN (XSHUTDOWN) rising	t2	0.0		
RSTN (XSHUTDOWN) rising and VDDD rising to first I2C transaction (1)	t3	9600 (2) 12,500 (3)	–	MCLK cycles
Minimum No. of MCLK (EXTCLK) cycles prior to the first I2C transaction	t4	9600 (2) 12,500 (3)	–	
PLL startup/lock time	t5	–	1	ms
Entering streaming mode – first frame start sequence (fixed part)	t6	–	10	
Entering streaming mode – first frame start sequence (variable part)	t7	The delay is the coarse integration time value		lines
DPHY Recovery Time (TWAKEUP)	t8	1	–	ms
DPHY Initialization Period (TINIT)	t9	0.1	–	

NOTE:

1 In case Software standby mode is desired after power up it should be initiated by register configuration (see S5K3H7YX application notes for details)

2. I2C/SPI access to tuning registers and T&P memory: t3, t4 = 9600 MCLK cycles.

3. I2C/SPI access to Chip ID from NVM, tuning registers and T&P memory: t3, t4 = 12,500 MCLK cycles.

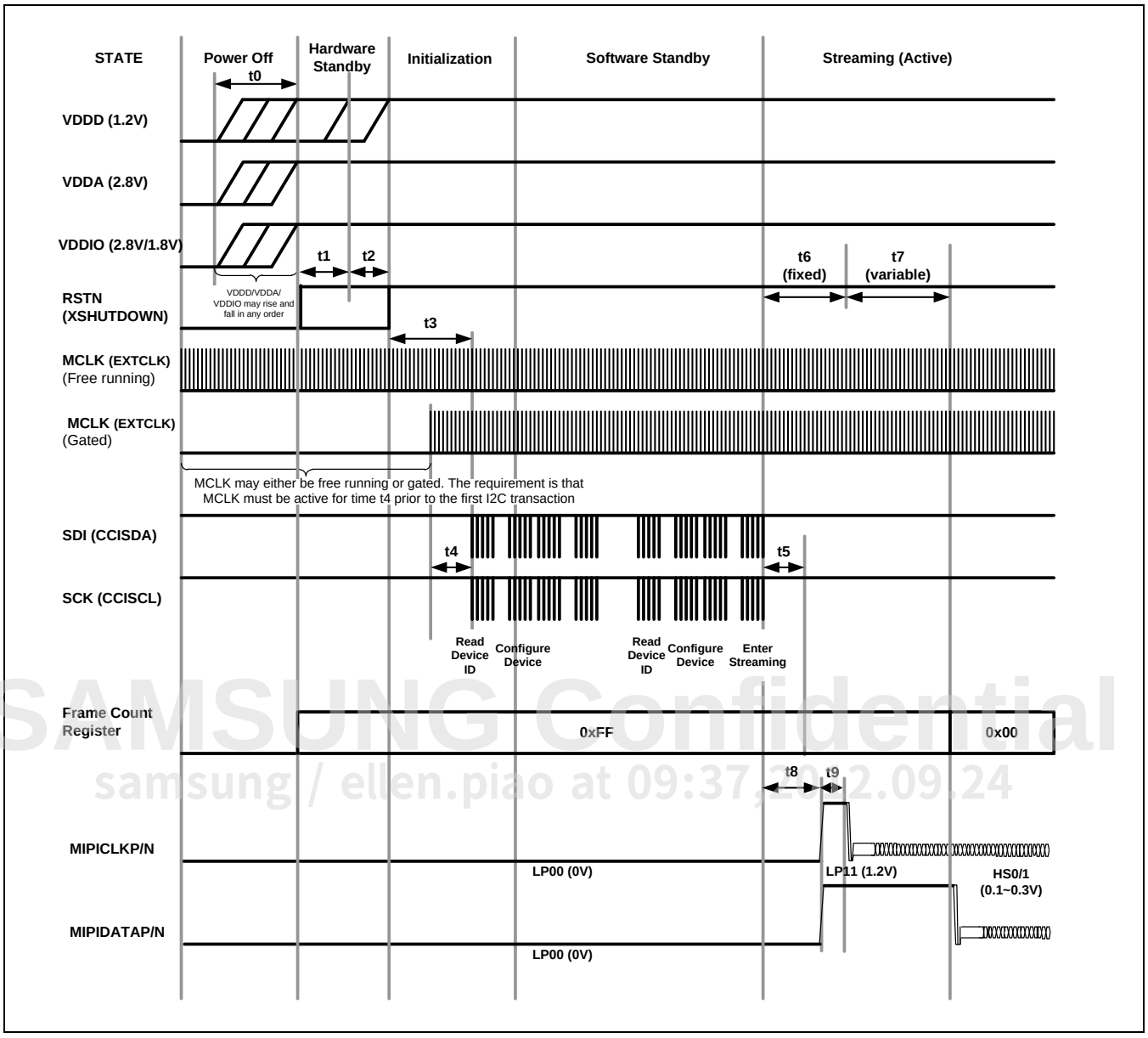


Figure 24 Power-Up Sequence (Serial Output Case)

7.2 Power-Down Sequence

The digital and analog supply voltages can be powered down in any order, e.g., VDDD/VDDIO then VDDA or VDDA/VDDIO then VDDD.

Similar to the power-up sequence, the MCLK (EXTCLK): input clock may be either gated or continuous.

If the CCI/SPI command to exit streaming is received while a frame of valid active data is being output, then the sensor module must wait for the frame end code before entering software standby mode.

If the CCI/SPI command to exit streaming mode is received during the inter frame time, then the sensor module must enter software standby mode immediately.

Table 12 Power-Down Sequence Timing Constraints (Serial Output Case)

Constant	Label	Min.	Max.	Unit
Enter Software Standby CCI command – Device in Software Standby mode	t0	If outputting a frame of MIPI, the data waits for the MIPI frame end code before entering software standby; otherwise enter software standby mode immediately.		–
Minimum number of MCLK (EXTCLK) cycles after the last I2C transaction or MIPI frame end code.	t1	512	–	MCLK cycles
Last I2C Transaction or MIPI frame end code – RSTN (XSHUTDOWN) falling	t2	512	–	
RSTN (XSHUTDOWN) falling to VDDD falling	t3	0.0	RSTN falling and VDDD falling can be in any order	ns
VDDD falling to RSTN (XSHUTDOWN) falling	t4	0.0		
VDDA/VDDD/VDDIO falling time	t5	VDDA/VDDD/VDDIO may fall in any order. The rising separation can vary from 0 ns to indefinite		

NOTE: For minimal power at hardware standby mode external VDDD should be OFF.

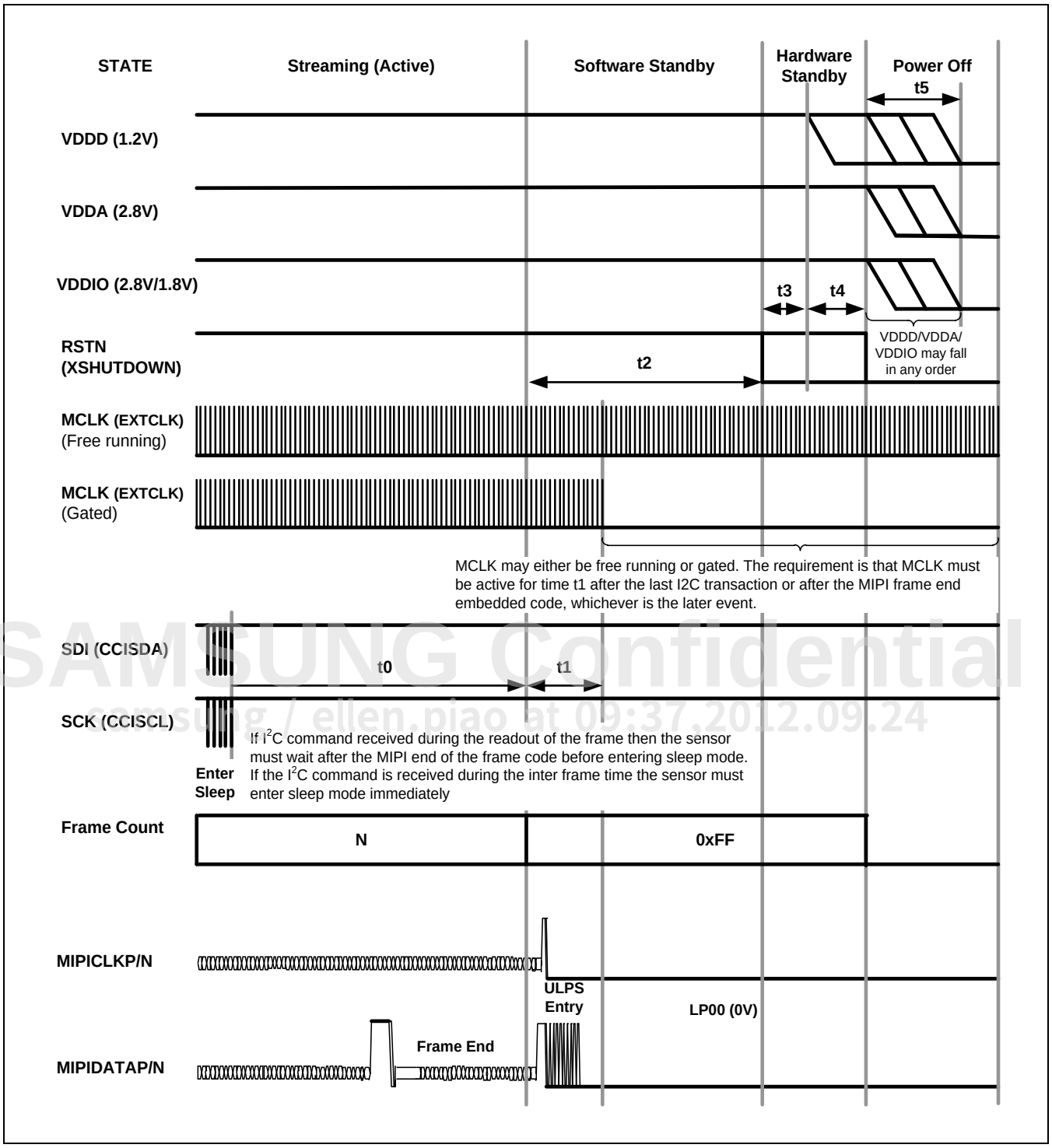


Figure 25 Power-Down Sequence (Serial Output Case)

7.3 Software Standby Mode Sequence

Entering software standby mode is the same as entering hardware standby mode but without RSTN (XSHUTDOWN) assertion to low and without applying external VDDD power down.

8 Functional Features

8.1 Frame Timing Control

When sensor frame timing configuration change is requested by host (Refer to section 8.1.1.3 Settings Affecting Frame Timing) by register setting with "group parameter hold" request, S5K3H7YX firmware detects the change and forces frame timing change in one of the following options:

a) Preserve frame timing without outputting the corrupted frame to host (skip frame)

b) Preserve frame timing and output corrupted frame

c) Timing abort: After end of readout and VBLANK (14,000 system cycles – 254.5uSec @55Mhz before a new frame starts).

d) Timing abort: After frame readout ends but before VBLANK time.

e) Timing abort: Immediate abort (including during frame read out).

Frame timing examples may be found in the following figures;

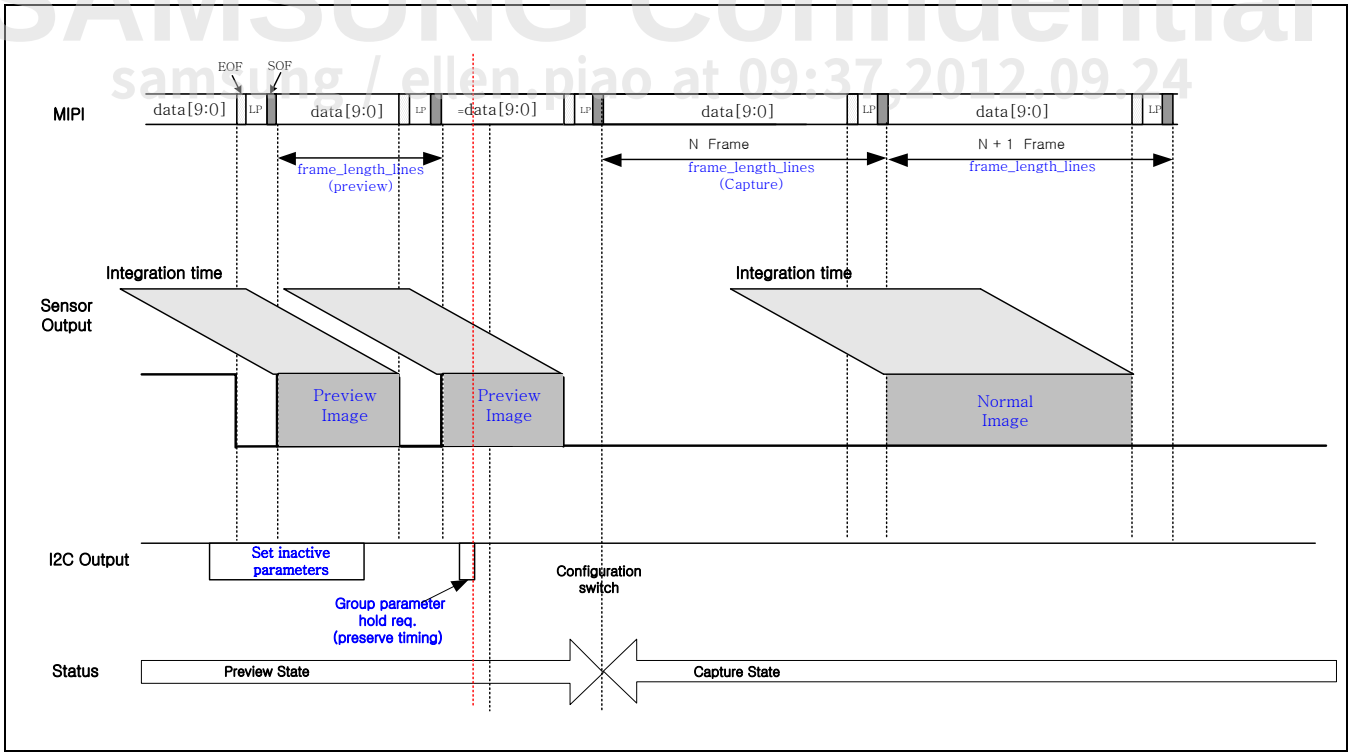


Figure 26 Example - case (a); Preserve frame timing without outputting the corrupted frame to host

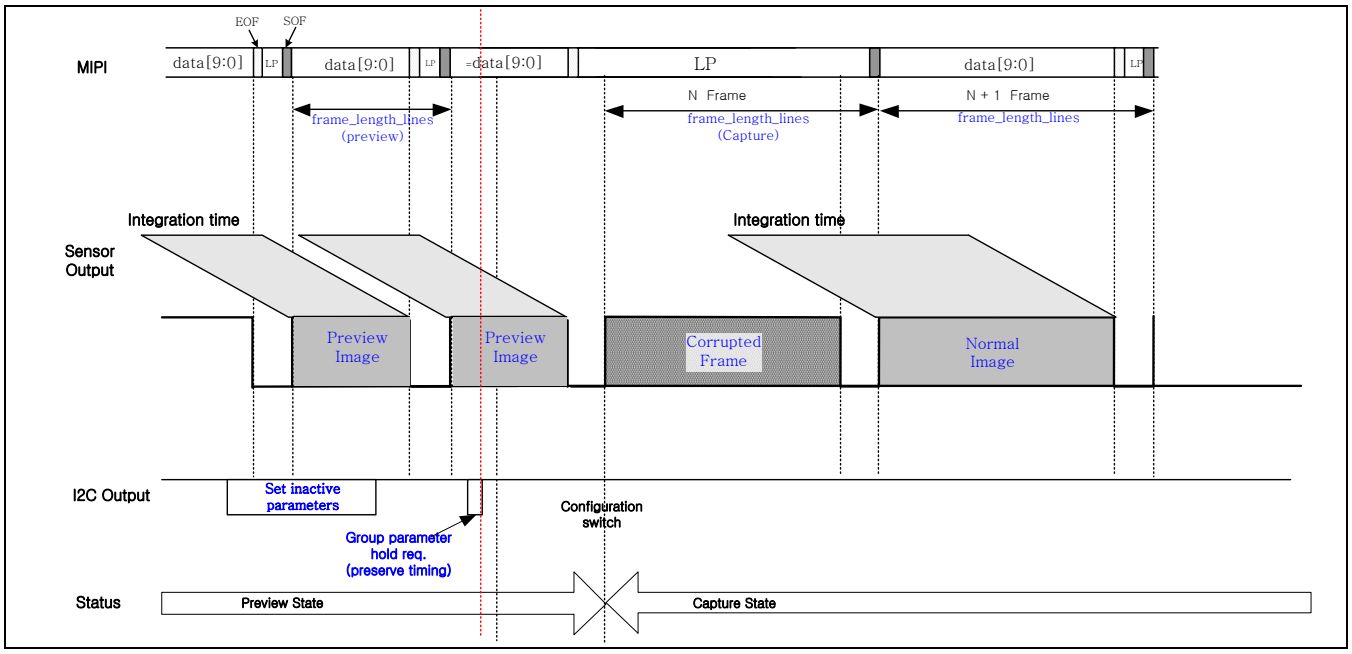


Figure 27 Example - case (b); Preserve frame timing and output corrupted frame

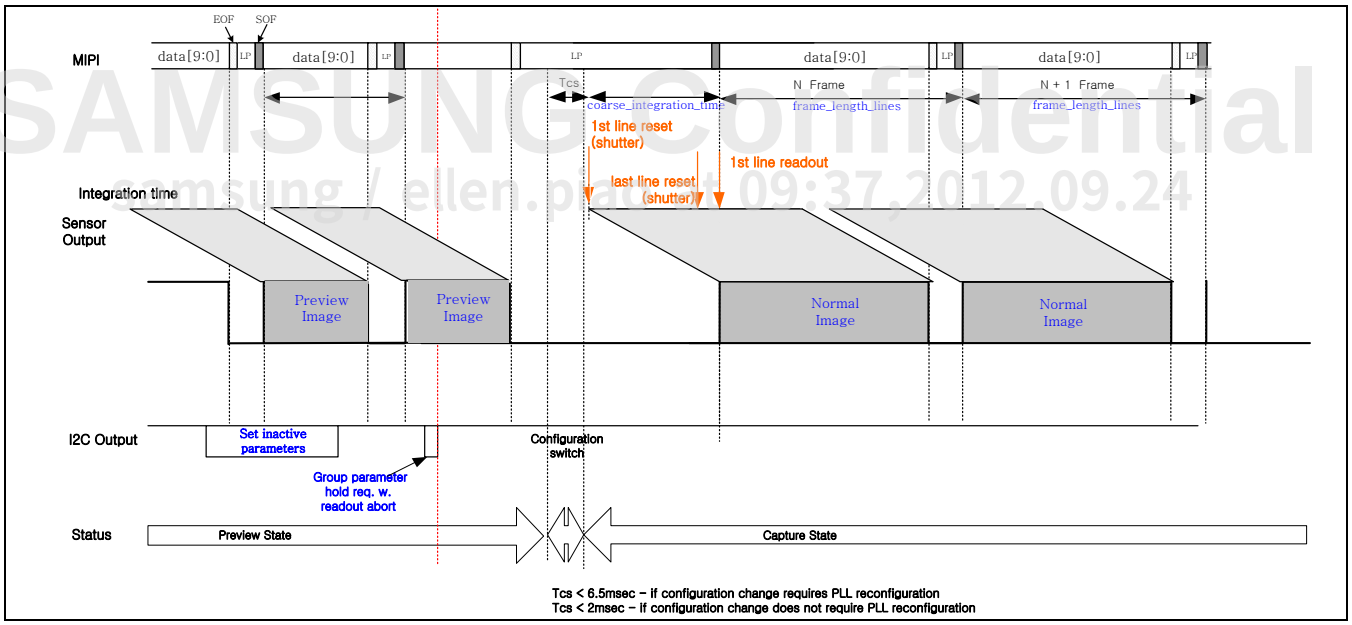


Figure 28 Example - case (c); Timing abort: After end of readout and VBLANK

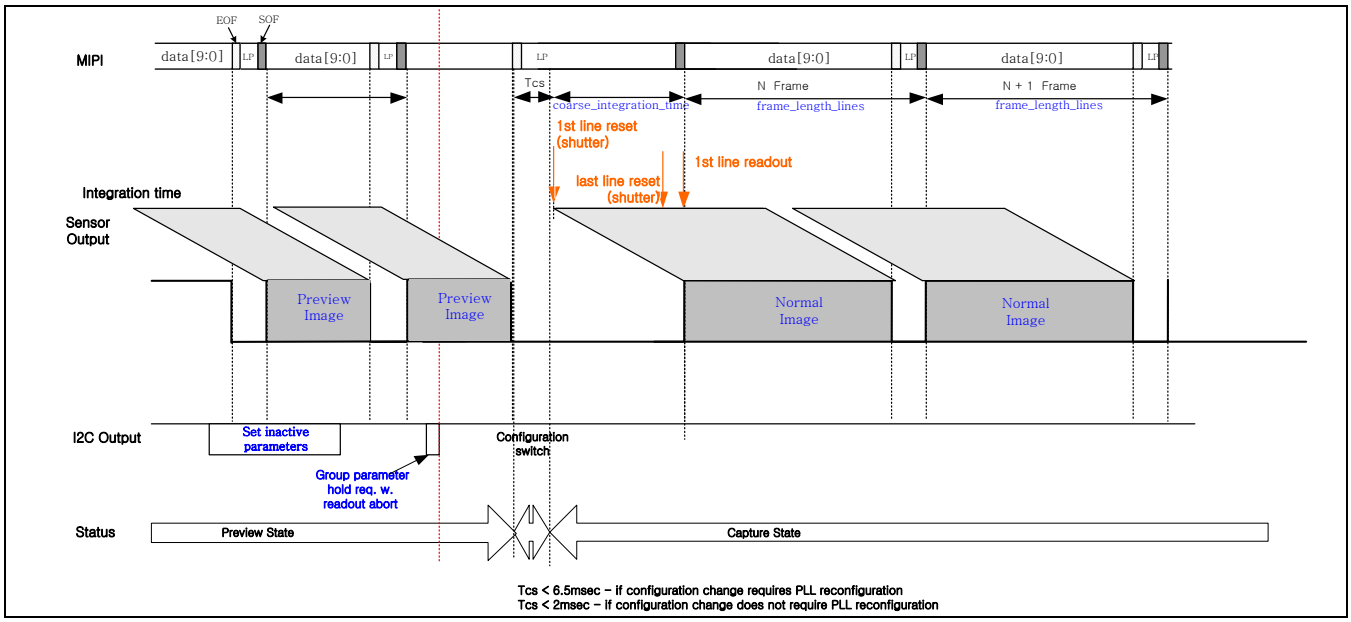


Figure 29 Example - case (d);
Timing abort: After frame readout ends but before VBLANK time

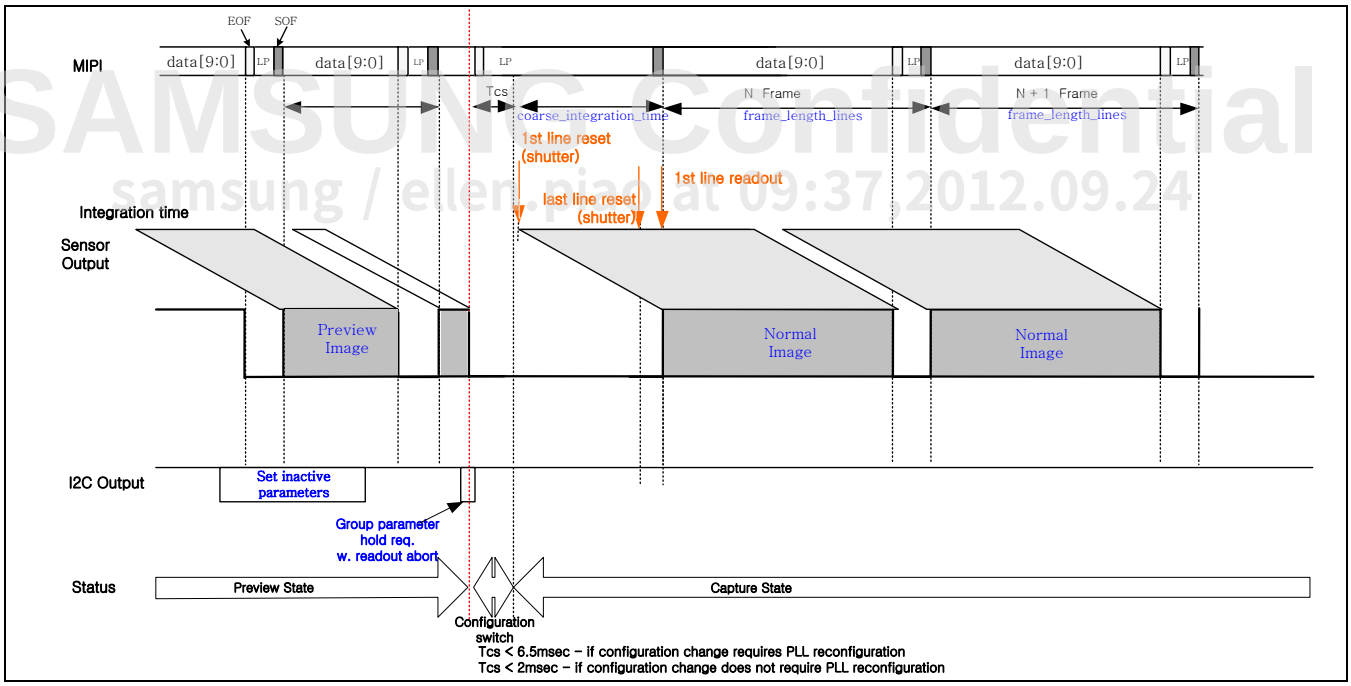


Figure 30 Example - case (e);
Timing abort: Immediate abort (including during frame read out).

8.1.1 Frame Timing Control Configuration

Table 13 Frame Timing Transition Options

	Timing Transition Type	Description
1	REQ_NO_ABORT_CORRUP_FRAME	Preserve timing and output the corrupted frame
2	REQ_NO_TIMING_ABORT	Preserve timing skip the corrupted frame
3	REQ_ABORT_ON_END_FRAME	Abort after end of timing frame
4	REQ_ABORT_ON_END_RO	Abort after frame read out ends
5	REQ_IMMEDIATE_ABORT	Abort immediately, even during frame read out (NOTE)

NOTE: The abort immediately has 3 exceptions where the command response will be delayed slightly:

a. Command detected during first 10 timing lines: In this case, firmware will delay the actual abort after the dark lines are finished, and OUTIF transmitted the MIPI short packet "frame-start".
b. Command detected during last 10 readout lines: In this case, firmware will delay the actual abort after readout ends (in order to prevent problematic timing of internal firmware interrupts).
c. Command detected during last 10 timing lines (just before frame ends anyway): In this case, firmware will delay the actual abort after normal API registers read that happens anyway around this time.

8.1.1.1 Rolling Shutter Frame Timing Configuration Change

Table 14 Rolling Shutter Frame Timing Transition Options

	Timing Transition Type	Setting
1	REQ_NO_ABORT_CORRUP_FRAME	general_setup_mask_corrupted_frames = 0
2	REQ_NO_TIMING_ABORT	general_setup_mask_corrupted_frames = 1
3	REQ_ABORT_ON_END_FRAME	general_setup_mask_corrupted_frames = 2
4	REQ_ABORT_ON_END_RO	general_setup_mask_corrupted_frames = 3
5	REQ_IMMEDIATE_ABORT	general_setup_mask_corrupted_frames = 4

8.1.1.2 Mechanical Shutter Frame Timing Configuration Change

Table 15 Mechanical Shutter Frame Timing Transition Options

	Timing Transition Type	Setting
1	Reserved	vendor_ms_invoke_method = 0
2	Reserved	vendor_ms_invoke_method = 1
3	REQ_ABORT_ON_END_FRAME	vendor_ms_invoke_method = 2
4	REQ_ABORT_ON_END_RO	vendor_ms_invoke_method = 3
5	REQ_IMMEDIATE_ABORT	vendor_ms_invoke_method = 4

8.1.1.3 Settings Affecting Frame Timing

These are main parameters that if changed will result in frame timing configuration change:

Table 16 Parameters that Cause Frame Timing Change if Modified

Input Size, Mirror, Binning or Line Timing	PLL Modification	If BPC is Enabled
frame_timing_x_addr_start frame_timing_x_addr_end frame_timing_y_addr_start frame_timing_y_addr_end frame_timing_line_length_pck output_data_format sub_sample_x_odd_inc sub_sample_x_even_inc sub_sample_y_odd_inc sub_sample_y_even_inc binning_mode binning_type binning_ver_bin_inc general_setup_image_orientation	clocks_vt_pix_clk_div clocks_vt_sys_clk_div clocks_pre_pll_clk_div clocks_pll_multiplier clocks_op_pix_clk_div clocks_op_sys_clk_div clocks_secnd_pre_pll_clk_div clocks_secnd_pll_multiplier	scaling_scale_m scaling_digital_crop_x_offset scaling_digital_crop_y_offset

8.2 Analog Sensor

8.2.1 Analog to Digital Converter (ADC)

The image sensor has an on-chip ADC. A two-channel column parallel ADC scheme is used for high-speed analog processing.

8.2.2 Analog Gain Control

The user can control the gain of the pixel signal (AG) by using the analog gain control registers.

Analog gain (AG) of up to x16 is supported.

AG precision is determined according to AnalogGainPrecision register (0x37F8).

The analogue_gain_code_global register is used to set the analog gain according to these equations:

Table 17 Analog Gain (AG) Control

AnalogGainPrecision	AG
AnalogGainPrecision = 0 (Default)	AG = analogue_gain_code_global/32
AnalogGainPrecision = 1	AG = analogue_gain_code_global/64
AnalogGainPrecision = 2	AG = analogue_gain_code_global/128
AnalogGainPrecision = 3	AG = analogue_gain_code_global/256

8.2.3 ADC Resolution

The supported ADC effective resolutions are 8/9/10-bit

8.3 Embedded Line

S5K3H7YX may be configured to generate an embedded MIPI header with frame information.

8.4 ISP (Image Signal Processor)

8.4.1 Dual Correlated Double Sampling Statistics

This mechanism of "auto calibration" collects statistical data from the analog circuits and adjusts/keeps optimal analog settings.

8.4.2 Analog Dark Level Correction

This block is responsible for row noise reduction and frame black level recovery by subtracting a weighted sum of optical black pixels. Also, the block collects temperature statistics.

8.4.3 Periodic Offset Mismatch Correction

A difference between analog circuits and channels might produce an undesired position-dependent mismatch (checkers pattern). The algorithms correct additive/offset components of periodic mismatch by adding 4 (2x2) coefficients to appropriate pixels.

8.4.4 Global Offset Correction (GOS)

The GOS compensation model is based on 5x4 grid. Bilinear interpolation is used between grid points.

8.4.5 Lens Shading Correction

The lens shading compensation model is based on Radial polynomial with additional dynamic grid compensation for error minimization. Bilinear interpolation is used between grid points.
Shading correction might change dynamically, according to illumination type.

8.4.6 Module to Module Shading Variation Correction

The shading profile may be different across modules due to variations in relative lens positioning.

During module manufacturing, on-chip OTP memory may be programmed with the shading characteristics of the specific module. The programming is done using the Samsung proprietary shading classification algorithm at the module manufacturing site.

The programmed shading characteristics are matched with the best correction scheme, which is applied to the image in order to cancel specific module shading.

8.4.7 Periodic Gain Mismatch Correction

The difference between analog circuits and channels might produce an undesired position-dependent mismatch (checkers pattern). The algorithms correct the multiplicative/gain component of periodic mismatch by applying 4 (2x2) coefficients to appropriate pixels.

8.4.8 Static Despeckle

This algorithm replaces OTP mapped, bad pixel pairs (clusters) on the raw image data, based on the neighboring pixel pattern. This algorithm prepares the image for perfect bad pixel detection and correction by the host by fixing bad pixels and pixel clusters with characteristics that are harder to detect by host.

8.4.9 Image Downscaling

The image from the sensor can be downscaled by x1.5, x2, x3, x4. Scaling is performed early in processing pipeline for maximal power reduction.

8.4.10 DPCM/PCM Image Compression

10-bit output may be compressed using DPCM/PCM 10-bit to 8-bit compression.

8.4.11 Output Formatting

Raw sensor data in Bayer format is outputted with 8 or 10-bit accuracy.

8-bit output may be uncompressed or compressed.

8.5 Temperature Sensor

S5K3H7YX integrates an on-chip temperature sensor.

The temperature value in degrees (± 5 °C accuracy) may be obtained via register read.

8.6 General Purpose IO Control

Table 18 GPIO Functional Table

	CIS VIA Parallel	Parallel DATA PATH			STROBE OUT	GPI/GPO
		BAYER8	BAYER10	BAYER12		
D9_PAD	CIS[10]	DOUT[7]	DOUT[9]	DOUT[11]	N/A	N/A
D8_PAD	CIS[9]	DOUT[6]	DOUT[8]	DOUT[10]	N/A	N/A
D7_PAD	CIS[8]	DOUT[5]	DOUT[7]	DOUT[9]	N/A	N/A
D6_PAD	CIS[7]	DOUT[4]	DOUT[6]	DOUT[8]	N/A	N/A
D5_PAD	CIS[6]	DOUT[3]	DOUT[5]	DOUT[7]	N/A	N/A
D4_PAD	CIS[5]	DOUT[2]	DOUT[4]	DOUT[6]	N/A	N/A
D3_PAD	CIS[4]	DOUT[1]	DOUT[3]	DOUT[5]	N/A	N/A
D2_PAD	CIS[3]	DOUT[0]	DOUT[2]	DOUT[4]	N/A	N/A
D1_PAD	CIS[2]	0	DOUT[1]	DOUT[3]	N/A	N/A
D0_PAD	CIS[1]	0	DOUT[0]	DOUT[2]	N/A	N/A
GPIO_1_PAD	CIS[0]	NOT USED	NOT USED	DOUT[1]	Flash/M.Shutter	GPI/GPO
GPIO_2_PAD	NOT USED	NOT USED	NOT USED	DOUT[0]	Flash/M.Shutter	GPI/GPO
GPIO_3_PAD	NOT USED	NOT USED	NOT USED	NOT USED	Flash/M.Shutter	GPI/GPO

8.7 System

8.7.1 Clock System

Described in: *5.6 PLL and Clock Generator*

8.7.2 Reset System

Reset is performed after power-up by the on-chip POR (power-on-reset) circuit.

Asynchronous HW reset is possible using the RSTN (XSHUTDOWNB) pin.

SW reset is possible using IIC/SPI register access.

8.7.3 CPU Sub-System

ARM7-based system

8.7.4 I2C Slave/SPI

The I2C and SPI control interface are high priority AHB masters. This allows CPU-independent register access.

8.7.5 Memory System

ROM/RAM on ARM7 AHB bus.

ROM code may be modified using on-chip application for FW function replacement.

8.8 NVM OTP Memory

The NVM memory module is a non-volatile OTP (one-timing programming) memory module. This module enables the saving of unique data to each chip at the production stage.

OTP memory is used to store the following unique information:

- Chip_id data – production history data to be stored during die sorting
- Process-dependent calibration parameters
- Bad clusters and a tiny pixel map for despeckle
- Lens shading data – classified during module production that uses and is stored in the Samsung proprietary algorithm

There are three different ways to access each NVM memory:

- Externally, using IO pads by configuring the chip to a dedicated test mode and performing full OTP memory IP write/read protocol.
- Internally, through the APB bus using the controller.
- Internally, through the APB bus by writing dedicated registers and performing full NVM write/read protocol.

8.8.1 OTP Read/Write Procedure

NOTE: Contact your FAE for more details.

8.9 Global Reset

The S5K3H7YX provides global reset mode. Global reset allows all rows to have the same integration start and end. Global reset mode is used in conjunction with the external mechanical shutter controlled by the host. The host must program following the sequence and restrictions.

There are three options of operation for the mechanical shutter mode.

- **reset_mode = 0:** The TG waits for the end of the read out of the current frame, and then starts the mechanical shutter mode.
- **reset_mode = 1:** The current rolling shutter frame is truncated at the end of the nearest line, and the mechanical shutter mode is started.
- **reset_mode = 2:** The MS mode will wait for the end of the timing frame.
- **reset_mode = 3:** Illegal.

There is 1H time uncertainty from the MS host command. All timings in the sequence are synchronized to the end of the frame (in case of tgr_glb_reset_mode = 1 it is the end of the nearest line).

8.9.1 Global Reset – Single Frame

The Mechanical Shutter mode (MS) is a special mode in the Global Management block. It is used to capture a frame in a non-rolling shutter mode by exposing all of the array lines at a specific time.
The readout process is performed as always in a line-by-line manner.
The following schematic drawing shows the MS mode from preview to MS and back to preview.

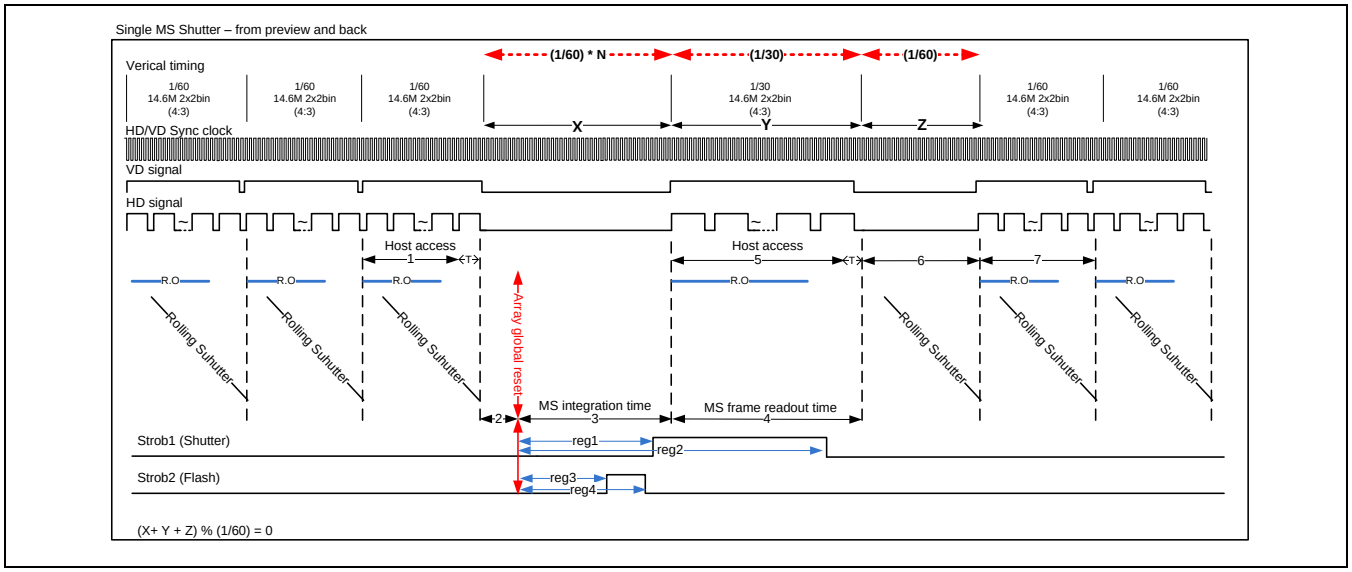


Figure 31 Mechanical Shutter Single Frame

Table 19 Mechanical Shutter Single Frame

Phase	Title	Description
1	Host access for MS	Host access for MS. System at preview mode.
2	Pre global reset	After preview frame is finished, additional time is required for the setting of the array global reset.
3	MS integration time	The entire array is in the integration state until readout starts. Strobe1 and strobe2 for mechanical shutter and xenon are controlled by register pulse generation.
4	MS frame readout	MS configuration frame is output.
5	Host access for preview	Host access for back to preview. Will follow with blank time for integration period.
6	MS frame readout	Integration time for first preview frame.
7	MS frame readout	First preview frame after MS.

1. Timing until the first capture image (X) is a multiple of the preview frame rate.
2. Capture image timing (Y) is a multiple of the preview frame rate.
3. Timing until the first preview image (Z) after capture is a multiple of the preview frame rate.
4. S5K3H7YX maintains a certain time between the HD and VD falling edge to data output under any conditions.
5. S5K3H7YX maintains a certain low period of VD within 1 V time.

8.9.2 Global Reset – with Frame Truncation

The following schematic drawing shows the MS mode from preview to MS with truncated frame:

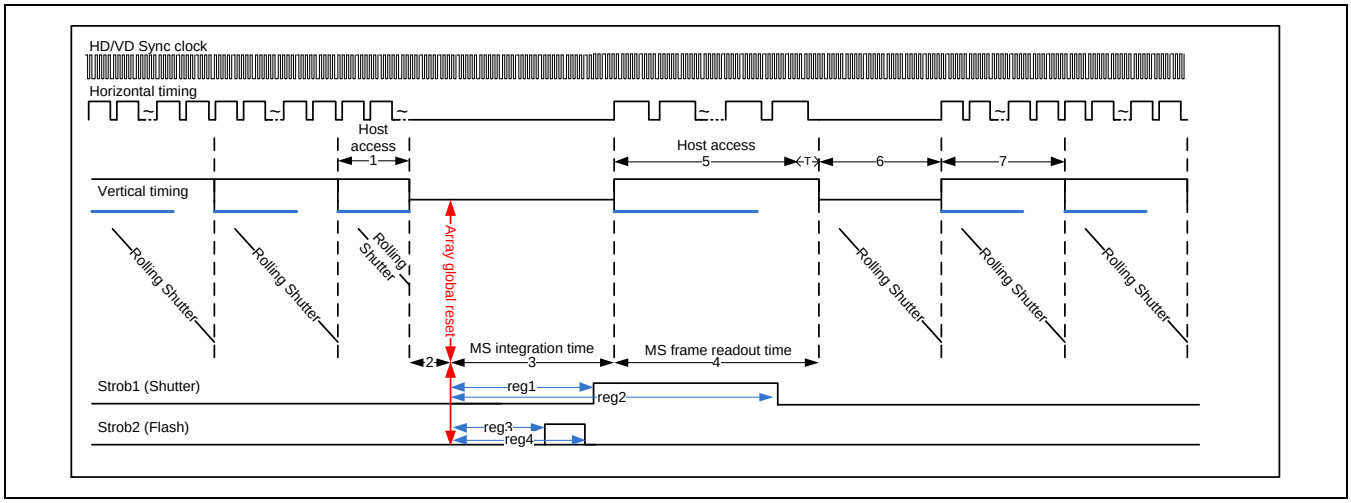


Figure 32 Mechanical Shutter with Frame Truncation

Table 20 Mechanical Shutter with Frame Truncation

Phase	Title	Description
1	Host access for MS	Host access for MS. System in preview mode.
2	Pre global reset	After current frame is immediately truncated, additional time is required for the setting of the array global reset.
3	MS integration time	The entire array is in the integration state until readout starts. Strobe1 and strobe2 are controlled by the register for mechanical shutter and xenon pulses.
4	MS frame readout	MS configuration frame is output.
5	Host access for preview	Host access for back to preview. Will follow with blank time for the integration period.
6	MS frame readout	Integration time for the first preview frame.
7	MS frame readout	First preview frame after MS.

8.10 Test Pattern

S5K3H7YX may be configured to generate deterministic test patterns.

9 Output Data Interface

The S5K3H7YX MIPI CSI-2 interface is a four-lane high-speed serial interface that connects the camera sensor to a host processor. The S5K3H7YX MIPI core IP is compatible with the MIPI Alliance Standards for D-PHY, CSI2 and DSI.

The maximum high speed clock frequency of the MIPI Core is 1 GHz.

Main features:

- Main output frame rates:
- Capture: 8M-4:3 30 fps (2640 Mbps)
- FHD video: 6M-16:9 30 fps (1980 Mbps)/2.7M (16:9) 30 fps (990 Mbps)
- HD video: 1.5M-16:9 120 fps
- High speed: QVGA 240 fps
- MIPI CSI-2: Four lanes with a maximum of 1 GHz (bit clock rate) each (125 MHz byte clock).
- Supported data types: RAW,8 RAW10, RAW12
- Integrated MIPI DPHY v0.90 compatible
- MIPI transmit only
- Support up to four data lanes, one clock lane
- ULPM – ultra low power mode supported

NOTE: RAW12 for test purpose only

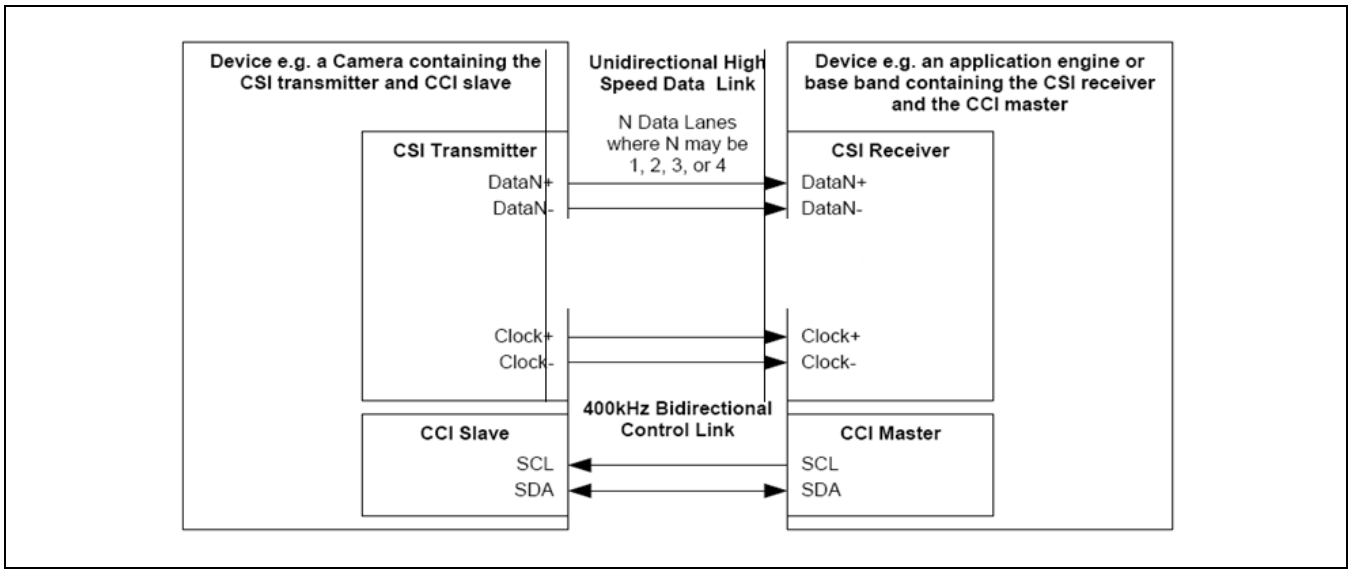


Figure 33 CSI-2 and CCI Transmitter and Receiver Interface

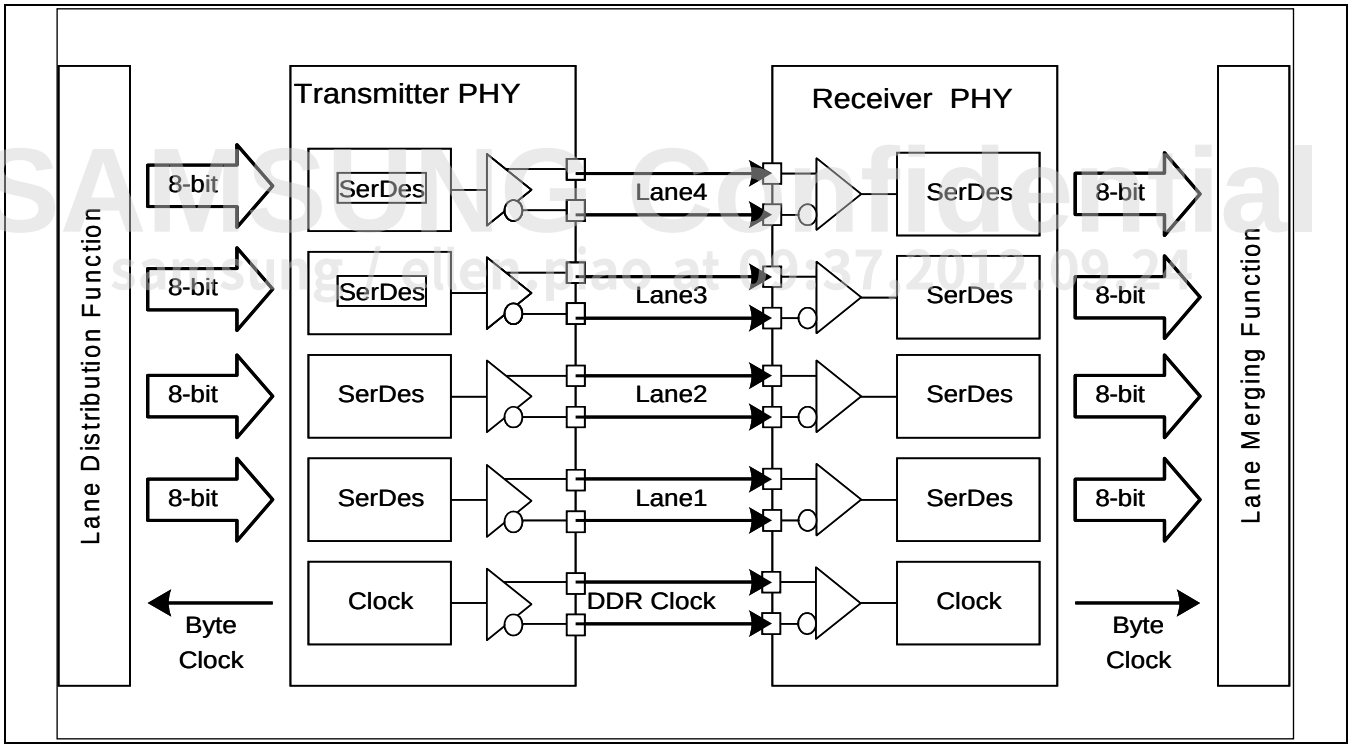


Figure 34 Four Lane Transmitter and Four Lane Receiver Example

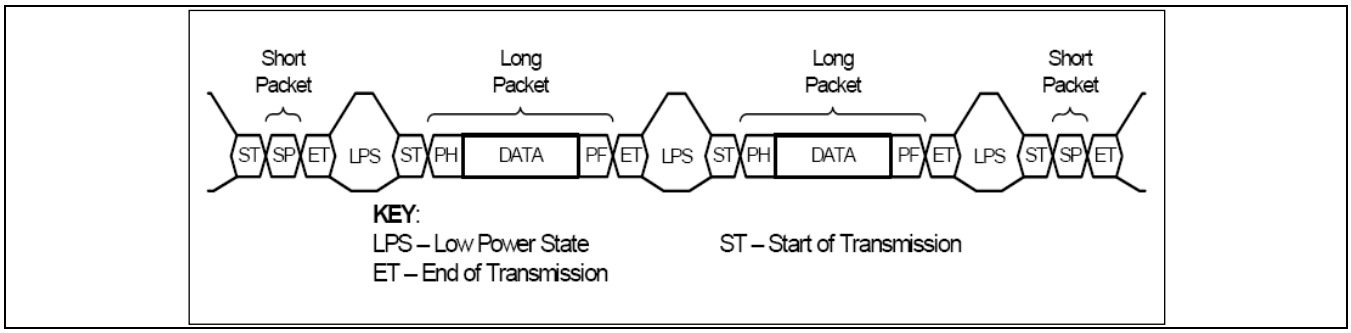


Figure 35 Low Level Protocol Packet Overview

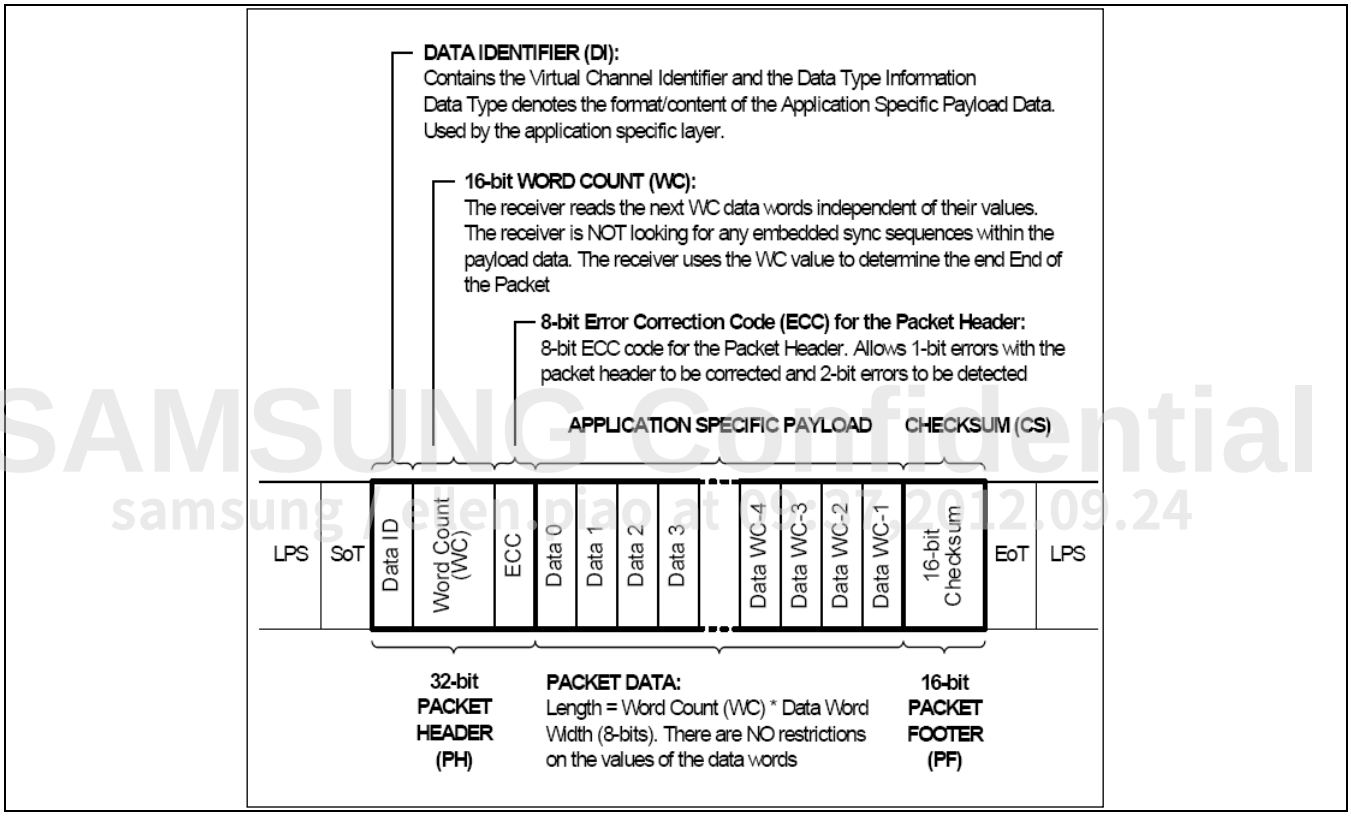


Figure 36 Long Packet Structure

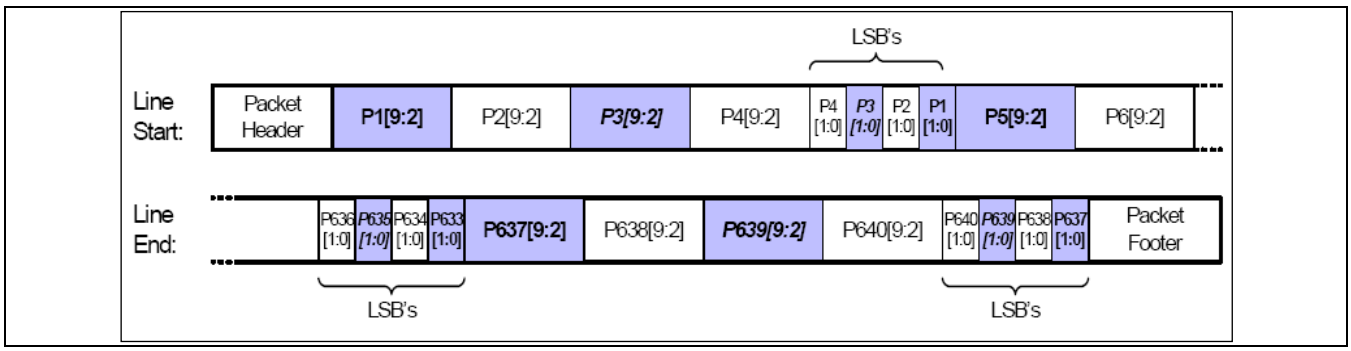


Figure 37 RAW10 Transmission

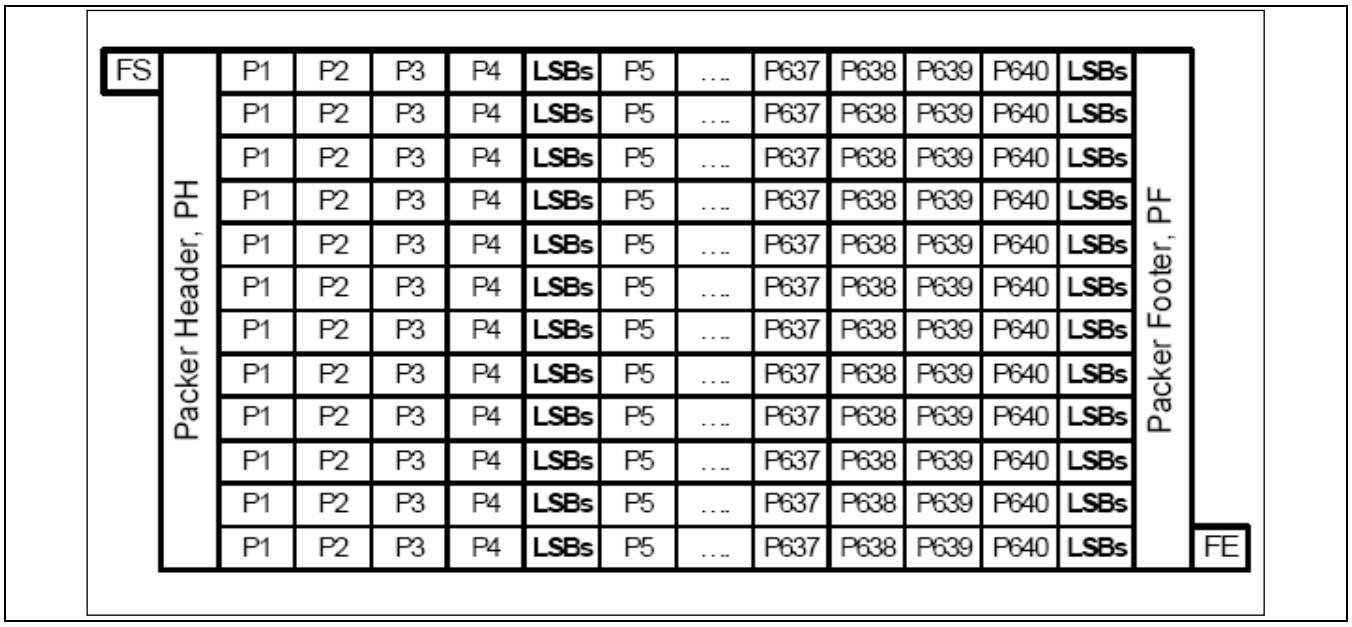


Figure 38 RAW10 Frame Format

10 Electrical Characteristics

10.1 Absolute Maximum Rating

Table 21 Absolute Maximum Rating

Symbol	Description	Min.	Typ.	Max.	Unit
VDDD (MAX)	Digital Absolute Max (1)	– 0.3	–	1.8	V
VDDA (MAX)	Analog Absolute Max (2)	– 0.3	–	4	
VDDIO (MAX)	Parallel IO Absolute Max (3)	– 0.3	–	3.6	
VIP	Digital Input Voltages (4)	– 0.3	–	VDDIO + 0.3	
VCAP	VCAP Analog Voltage (5)	–0.3	–	4.2	
TSTR	Storage Temperature	– 40	–	85	°C

NOTE:

1. Digital Supply 1.3 V + 0.5 V
2. Analog Supply 2.9 V + 1.1 V
3. Parallel IO Supply 2.9 V + 0.7 V
4. Digital Inputs: MCLK, RSTN, I2C_SPI_N_SEL, XCE, SDO, SDI, SCK, GPIO_1/2/3
5. Voltage on external analog capacitors

10.2 Operating Conditions

Table 22 Operating Conditions

Symbol	Description	Min.	Typ.	Max.	Unit
VDDD	Digital Power Supply (1)	1.15	1.2	1.3	V
VDDA	Analog Power Supply (2)	2.7	2.8	3.0	
VDDIO	Parallel IO Supply	1.7	2.8	3.0	
VIP	Digital Input Voltages (3)	0	–	VDDA	
VCAP	VCAP Analog Voltage	0	–	4.2	
TTEST	Test Temperature (4)	21	23	25	°C
TOPT	Optimum Operating Temperature (5)	5	–	40	
TOPR	Normal Operating Temperature (6)	– 25	–	55	
TFUNC	Functional Operating Temperature (7)	– 30	–	70	

NOTE:

1. Digital Supply Tolerances: Lower limit 1.2 V – 50 mV, Upper Limit: 1.2 V + 100 mV
2. Analog Supply Tolerances: Lower limit 2.8 V – 100 mV, Upper Limit: 2.8 V + 200 mV
3. Digital Inputs: MCLK, RSTN (XSHUTDOWN), SCL, SDA
4. Test Temperature – image quality test conditions
5. Optimum Operating Temperature – no visible degradation in image quality
6. Normal Operating Temperature – camera produces acceptable images
7. Functional Operating Temperature – camera fully functional

10.3 DC Characteristics

Table 23 DC Characteristics

(VANA = 2.7 V to 3.0 V, VIP = 1.8 V ± 0.1 V (or 2.6 V to 3.0 V), T_A = – 30 to + 70 °C, CLOAD = 20 pF)

Characteristics	Symbol	Condition	Min.	Typ.	Max.	Unit
Input voltage (1)	VIH	–	0.7 × VIP	–	–	V
	VIL	–	–	–	0.3 × VIP	
Input leakage current (1)	IIL	VIN = VIP or VSS	– 10	–	10	μA
High level output voltage (2)	VOH	IOH = – 100 μA	VDIG – 0.2	–	–	V
		IOH = – 6, – 8 mA	0.7 × VIO	–	–	
Low level output voltage (2)	VOL	IOL = 100 μA	–	–	0.2	
		IOL = 6, 8 mA	–	–	0.3 × VIO	
High-Z output leakage current (3)	IOZ	VOUT = VSS or VDDD	– 10	–	10	μA
Input capacitance (1)	CIN	–	–	–	5	pF
Supply current (4)	IHWSBA	Hardware standby mode Analog (5)	–	25	-	μA
	IHWSBD	Hardware standby mode Digital (5)	–	-	-	
	ISWSB1A	Software standby mode Analog (6)	–	25	-	
	ISWSB1D	Software standby mode Digital (6)	–	800	26000	
	ISWSB2A	Software standby mode Analog (7)	–	–	-	
	ISWSB2D	Software standby mode Digital (7)	–	2000	34000	
	ISTRMA	Streaming mode Analog (8) 2M@30 fps 4:3	–	37	39	mA
		Streaming mode Analog (9) 8M@30 fps 4:3	–	44	47	
	ISTRMD2	Streaming mode Digital (8) 2M@30 fps 4:3	–	92	170	
		Streaming mode Digital (9) 8M@30 fps 4:3	–	126	203	
	ISTRMIO	Streaming mode Digital (9) (10) @30 fps	–	0.4	0.5	

NOTE:

1. Applied to MCLK, RSTN, SCL, SDA pins
2. Applied to SCL, SDA, PVI pins
3. Applied to SCL, SDA, PVI pins when in High-Z output state
4. Summation of currents from VDDD and VDDA
5. At 25deg., external clock active or not switching, External VDDD off
6. External clock not switching, Max @ FF/Vcc+10%,85 °C
7. External clock active (6 MHz)

8. Readout of 1632x1224 binning raw Bayer image at 30 fps (full processing, 2 PLLs, MIPI 2 lane)
9. Readout of 3264x2448 raw Bayer image at 30 fps (full processing, 2 PLLs, MIPI 4 lane)
10. CLOAD = 20 pF

10.4 AC Characteristics

Table 24 AC Characteristics

(V_{ANA} = 2.7 V to 3.0 V, V_{IP} = 1.8 V ± 0.1 V (or 2.6 V to 3.0 V), T_A = – 30 to + 70 °C)

Characteristics	Symbol	Condition	Min.	Typ.	Max.	Unit
External clock frequency (1)	fXCLK	–	6.0	–	54.0	MHz
External clock duty cycle (1)	fXDUTY	–	45	–	55	%
PLL locking time	tLOCK	–	–	200	1000	µs

NOTE:

1. Applied to MCLK pin

10.5 TX Driver Characteristics

Table 25 TX HS Transmitter DC Specifications

Parameter	Description	Min.	Nom.	Max.	Unit	Note
VCMTX	HS transmit static common-mode voltage	150	200	250	mV	(1)
|ΔVCMTX(1,0)|	VCMTX mismatch when output is Differential-1 or Differential-0	–	–	5		(2)
|VOD|	HS transmit differential voltage	140	200	270		(1)
|ΔVOD|	VOD mismatch when output is Differential-1 or Differential-0	–	–	10		(2)
VOHHS	HS output high voltage	–	–	360		(1)
ZOS	Single ended output impedance	40	50	62.5	Ω	–
ΔZOS	Single ended output impedance mismatch	–	–	10	%	–

NOTE:

1. Value when driving into load impedance anywhere in the ZID range.
2. It is recommended that the implementer minimize ΔVOD and ΔVCMTX(1,0) in order to minimize radiation and optimize signal integrity.

Table 26 TX HS Transmitter AC Specifications

Parameter	Description	Min.	Nom.	Max.	Unit	Note
VCMTX (HF)	Common-level variation above 450 MHz	–	–	15	mVRMS	–
VCMTX (LF)	Common-level variation between 50 to 450 MHz	–	–	25	mVPEAK	–
tR and tF	20 % to 80 % rise time and fall time	–	–	0.3	UI	1
		150	–	–	ps	–

NOTE: UI is equal to 1/(2*fh). 'fh' is the highest fundamental frequency for data transmission.

Table 27 TX LP Transmitter DC Specifications

Parameter	Description	Min.	Nom.	Max.	Unit
V_{OH}	Thevenin output high level	1.15	1.2	1.3	V
V_{OL}	Thevenin output low level	– 50	–	50	mV
Z_{OLP}	Output impedance of LP transmitter	110	–	–	Ω

Table 28 TX LP Transmitter AC Specifications

Parameter	Description		Min.	Nom.	Max.	Unit
T_{RLP}/T_{FLP}	15 % to 85 % rise time and fall time		–	–	25	ns
T_{REOT}	30 % to 85 % rise time and fall time		–	–	35	
$T_{LP-PULSE-TX}$	Pulse width of the LP exclusive-OR clock	First LP exclusive-OR clock pulse after Stop state or last pulse before Stop state	40	–	–	
		All other pulses	20	–	–	
$T_{LP-PER-TX}$	Period of the LP exclusive-OR clock		90	–	–	–
–	Slew rate @ CLOAD = 20 pF		30	–	150	mV/ns
	Slew rate @ CLOAD = 70 pF		30	–	100	
C_{LOAD}	Load capacitance		0	–	70	pF

10.6 Parallel DATA IO Characteristics

Table 29 AC Characteristics (Parallel Mode)

(V_{DDA} = 2.7 V to 3.0 V, V_{DDIO} = 1.8 V ± 0.1 V (or 2.6 V to 3.0 V), V_{DDD} = 1.15 V to 1.3 V, T_A = – 30 to + 70 °C)

Characteristic	Symbol	Condition	Min.	Typ.	Max.	Unit
Data output clock frequency	f_{PCLK}	–	–	–	110	MHz
Parallel Interface setup time (1) (2)	t_{VSSUR}	VSYNC output	–	–	3	nsec
	t_{HSSUR}	HSYNC output	–	–	3	
	t_{VSSUF}	VSYNC output	–	–	3	
	t_{HSSUF}	HSYNC output	–	–	3	
	t_{DSU}	DATA output	–	–	3	
Parallel Interface hold time (1) (2)	t_{DH}	DATA output	–	–	3	
RSTN input pulse width	t_{WSHB}	RSTN = low (active)	200	–	–	µsec

NOTE:

1. When max PCLK is 110 MHz
2. Not considered external circuit loading

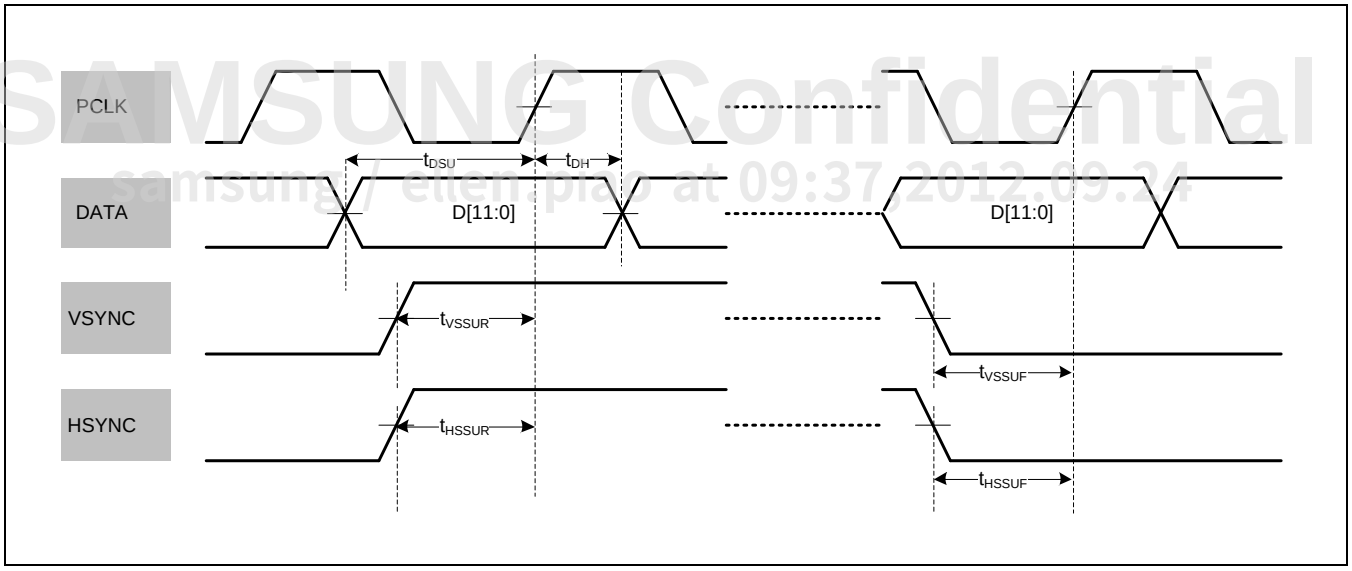


Figure 39 Setup and Hold Time for Data, VSYNC and HSYNC with Reference to PCLK

11 Register Description

This section describes the S5K3H7YX register map.

Vendor registers are defined for extended functionality control.

11.1 Configuration Registers

11.1.1 Configuration Registers 1 [0xD0000000 to 0xD0001FFF]

Start	Finish	Size	Reset Value Hex	Reset Value Dec	Name	Type	Width	Description
General Status Registers								
0x0000	0x0001	2	0x3087	###	model_id	RO	[15:0]	Camera module model identification number
0x0002	0x0002	1	0x00A2	162	revision_number_major	RO	[7:0]	Revision identifier of the camera module for DCC change
0x0003	0x0003	1	0x0001	1	manufacturer_id	RO	[7:0]	Module manufacturers code Refer to the Manufacturer Codes Document
0x0004	0x0004	1	0x0010	16	Reserved	RO	[7:0]	Reserved
0x0005	0x0005	1	0x00FF	255	frame_count	ROD	[7:0]	8-bit (0-255) Frame counter value
0x0006	0x0006	1	0x0000	0	pixel_order	RO	[7:0]	Colour Pixel Order
0x0007	0x0007	1		0	Reserved			
0x0008	0x0009	2	0x0040	64	data_pedestal	RO	[15:0]	Data pedestal – typically code 64 for 10-bit systems
0x000A	0x000B	2	0x0000	0	general_temperature	ROD	[15:0]	Sensor temperature
0x000C	0x000C	1	0x000C	12	pixel_depth	RO	[7:0]	Data pedestal – typically code 64 for 10-bit systems
0x0010	0x0010	1	0x0000	0	revision_number_minor	RO	[7:0]	Refer to the Data Format Chapter
0x001	0x001	1	0x000	6	Reserved	RO	[7:0]	Reserved

Start	Finish	Size	Reset Value Hex	Reset Value Dec	Name	Type	Width	Description
1	1		6					
0x0012	0x0012	1	0x0000	0	module_date_year	RO	[7:0]	Bits [3:0] - Last digit of manufacturing year.
0x0013	0x0013	1	0x0000	0	module_date_month	RO	[7:0]	Bits [3:0] - manufacturing month
0x0014	0x0014	1	0x0000	0	module_date_day	RO	[7:0]	Bits [4:0] - manufacturing day
0x0015	0x0015	1	0x0001	1	module_date_phase	RO	[7:0]	Bits [2:0] • 0=TS • 1=ES • 2=CS • 3=MP
0x0016	0x0017	2	0x0000	0	sensor_model_id	RO	[15:0]	
0x0018	0x0018	1	0x0000	0	sensor_revision_number	RO	[7:0]	
0x0019	0x0019	1	0x0000	0	sensor_manufacturer_id	RO	[7:0]	Running number, starting at 0
0x001A	0x001A	1	0x0000	0	sensor_firmware_version	RO	[7:0]	Running number, starting at 0
0x001C	0x001D	2	0x0000	0	serial_number	RO	[15:0]	Silicon revision number
0x001E	0x001F	2	0x0000	0	serial_number	RO	[15:0]	Silicon firmware version
Frame Format Description								
0x0040	0x0040	1	0x0001	1	frame_format_model_type	RO	[7:0]	
0x0041	0x0041	1	0x0013		frame_format_model_subtype_row	RO	[3:0]	
					frame_format_model_subtype_col	RO	[7:4]	
0x0042	0x0043	2	0x5788		frame_format_descriptor_0_n	RO	[11:0]	
					frame_format_descriptor_0_pix_code	RO	[15:12]	
0x0044	0x0045	2	0x1004		frame_format_descriptor_1_n	RO	[11:0]	
					frame_format_descriptor_1_pix_code	RO	[15:12]	
0x0046	0x0047	2	0x5440		frame_format_descriptor_2_n	RO	[11:0]	

Start	Finish	Size	Reset Value Hex	Reset Value Dec	Name	Type	Width	Description
					frame_format_descriptor_2_pix_code	RO	[15:12]	
0x0048	0x0049	2	0x1004		frame_format_descriptor_3_n	RO	[11:0]	
					frame_format_descriptor_3_pix_code	RO	[15:12]	
0x004A	0x004B	2	0x0000		frame_format_descriptor_4_n	RO	[11:0]	
					frame_format_descriptor_4_pix_code	RO	[15:12]	
0x004C	0x004D	2	0x0000		frame_format_descriptor_5_n	RO	[11:0]	
					frame_format_descriptor_5_pix_code	RO	[15:12]	
0x004E	0x004F	2	0x0000		frame_format_descriptor_6_n	RO	[11:0]	
					frame_format_descriptor_6_pix_code	RO	[15:12]	
0x0050	0x0051	2	0x0000		frame_format_descriptor_7_n	RO	[11:0]	
					frame_format_descriptor_7_pix_code	RO	[15:12]	
0x0052	0x0053	2	0x0000		frame_format_descriptor_8_n	RO	[11:0]	
					frame_format_descriptor_8_pix_code	RO	[15:12]	
0x0054	0x0055	2	0x0000		frame_format_descriptor_9_n	RO	[11:0]	
					frame_format_descriptor_9_pix_code	RO	[15:12]	
0x0056	0x0057	2	0x0000		frame_format_descriptor_10_n	RO	[11:0]	
					frame_format_descriptor_10_pix_code	RO	[15:12]	
0x0058	0x0059	2	0x0000		frame_format_descriptor_11_n	RO	[11:0]	
					frame_format_descriptor_11_pix_code	RO	[15:12]	
0x005A	0x005B	2	0x0000		frame_format_descriptor_12_n	RO	[11:0]	
					frame_format_descript	RO	[15:1	

Start	Finish	Size	Reset Value Hex	Reset Value Dec	Name	Type	Width	Description
					or_12_pix_code		2]	
0x005C	0x005D	2	0x0000		frame_format_descriptor_13_n	RO	[11:0]	
					frame_format_descriptor_13_pix_code	RO	[15:12]	
0x005E	0x005F	2	0x0000		frame_format_descriptor_14_n	RO	[11:0]	
					frame_format_descriptor_14_pix_code	RO	[15:12]	
Analogue Gain Description Registers								
0x0080	0x0081	2	0x0001	1	analogue_gain_capabiltiy	RO	[0:0]	0 - single global alanlogue gain only, 1 - separate channel alanlogue gains only
0x0082	0x0083	2	0x0000	0	RESERVED			
0x0084	0x0085	2	0x0020	32	analogue_gain_code_min	RO	[15:0]	Minimum recommended analogue gain code (dec: 32)
0x0086	0x0087	2	0x0200	512	analogue_gain_code_max	RO	[15:0]	Maximum recommended analogue gain code (dec: 512)
0x0088	0x0089	2	0x0001	1	analogue_gain_code_step	RO	[15:0]	Analogue gain code step size (dec:1)
0x008A	0x008B	2	0x0000	0	analogue_gain_type	RO	[0:0]	Analogue gain type (dec:0)
0x008C	0x008D	2	0x0001	1	analogue_gain_m0	RO	[15:0]	Analogue gain m0 constant (dec:m0=1)
0x008E	0x008F	2	0x0000	0	analogue_gain_c0	RO	[15:0]	Analogue gain c0 constant (dec:m0=1)
0x0090	0x0091	2	0x0000	0	analogue_gain_m1	RO	[15:0]	Analogue gain m1 constant (dec:m0=1)
0x0092	0x0093	2	0x0020	32	analogue_gain_c1	RO	[15:0]	Analogue gain c1 constant (dec:c1=32)
Data Format Description								
0x00C0	0x00C0	1	0x0001	1	data_format_model_type	ROD	[7:0]	0x01: 2-Byte Data Format
0x00C1	0x00C1	1	0x0004	4	data_format_model_subtype	ROD	[7:0]	Contains the number of data format descriptors used
0x00C2	0x00C3	2	0x0A0A	###	data_format_descriptor_0	ROD	[15:0]	ex) 0x0A0A: top 10-bit
0x00C4	0x00C5	2	0x0A08	###	data_format_descriptor_1	ROD	[15:0]	ex) 0x0A08: top 10-bit compressed to 8-bit, and

Start	Finish	Size	Reset Value Hex	Reset Value Dec	Name	Type	Width	Description
0x00C6	0x00C7	2	0x0808	###	data_format_descriptor_2	ROD	[15:0]	ex) 0x0808: top 8-bit
0x00C8	0x00C9	2	0x0C0C	###	data_format_descriptor_3	ROD	[15:0]	ex) 0x0C0C: top 12-bit
0x00CA	0x00CB	2	0x0000	0	data_format_descriptor_4	ROD	[15:0]	
0x00CC	0x00CD	2	0x0000	0	data_format_descriptor_5	ROD	[15:0]	
0x00CE	0x00CF	2	0x0000	0	data_format_descriptor_6	ROD	[15:0]	
General Set-up Registers								
0x0100	0x0100	1	0x0000	0	mode_select	RW	[7:0]	0 – Software Standby 1 - Streaming
0x0101	0x0101	1	0x0000	0	image_orientation	RW	[7:0]	Image orientation i.e. horizontal mirror and vertical flip
0x0102	0x0102	1	0x0000	0	Reserved	RW		
0x0103	0x0103	1	0x0000	0	software_reset	RW	[7:0]	Software reset
0x0104	0x0104	1	0x0000	0	grouped_parameter_hold	RW	[0:0]	The grouped parameter hold register disables the consumption of integration, gain and video timing parameters 0 – consume as normal 1 - hold
0x0105	0x0105	1	0x0003	3	mask_corrupted_frames	RW	[0:0]	Refer to Integration Time and Gain Control Chapter
0x0106	0x0106	1	0x0000	0	fast_standby_ctrl	RW	[0:0]	0 - Frame completes before mode entry. 1 - Frame may be truncated before mode entry
0x0107	0x0107	1	0x0020	32	cci_address_control	RW	[7:0]	Expressed as 8 bit (e.g. 0x20 write, 0x21 read is entered as 0x20)
Output Set-up Registers								
0x0110	0x0110	1	0x0000	0	channel_identifier	RW	[3:0]	Valid Range : 0-7 for CCP2 Valid Range : 0-3 for CSI-2 Default Value = 0
0x0111	0x0111	1	0x0002	2	signalling_mode	RW	[1:0]	0 : CCP2 Data/Clock Signalling 1 : CCP2 Data/Strobe Signalling

Start	Finish	Size	Reset Value Hex	Reset Value Dec	Name	Type	Width	Description
								2 : CSI-2(MIPI)
0x0112	0x0113	2	0x0A0A	###	data_format	RW	[15:0]	CCP Data Format: 0x0808: Top 8-b of pixel data,RAW8 0x0A08: 10-b to 8-b compression, RAW8 0x0A0A: Top 10-b of pixel data, RAW10
0x0114	0x0114	1	0x0003	3	lane_mode	RW	[7:0]	Number of CSI-2 lanes to be used Valid range: 0 (1-lane) to 3 (4-lane) Number of SLVS lanes to be used Valid only odd numbers: 1(2-lanes) to 11(12-lanes)
Integration Time and Gain Set-up Registers								
0x0120	0x0120	1	0x0000	0	gain_mode	RW	[0:0]	0 – Global Analogue Gain (Default) 1 – Per Channel Analogue Gain
Integration Time and Gain Set-up Registers								
0x0130	0x0131	2	0x0028	40	vana_voltage		[15:0]	Typical supplied VANA voltage
0x0132	0x0133	2	0x0012	18	vdig_voltage		[15:0]	Typical supplied VDIG voltage
0x0134	0x0135	2	0x0018	24	vio_voltage		[15:0]	Typical IO voltage
0x0136	0x0137	2	0x1800	###	extclk_frequency_mhz		[15:0]	Nominal Extclk frequency in MHz
Integration Time and Gain Registers								
Integration Time Registers								
0x0200	0x0201	2	0x0BEF	###	fine_integration_time	RW	[15:0]	Fine integration time (pixels) (dec:1000)
0x0202	0x0203	2	0x09D9	###	coarse_integration_time	RW	[15:0]	Coarse integration time (lines) (dec:800)
Analogue Gain Registers								
0x0204	0x0205	2	0x0020	32	analogue_gain_code_global	RW	[15:0]	Global Analogue Gain Code (dec:1x)
0x0206	0x0207	2	0x0020	32	analogue_gain_code_greenR	RW	[15:0]	Analogue Gain Code (dec:1x)
0x0208	0x0209	2	0x0020	32	analogue_gain_code_red	RW	[15:0]	Red Channel Analogue Gain Code

Start	Finish	Size	Reset Value Hex	Reset Value Dec	Name	Type	Width	Description
0x020A	0x020B	2	0x0020	32	analogue_gain_code_blue	RW	[15:0]	Blue Channel Analogue Gain Code
0x020C	0x020D	2	0x0020	32	analogue_gain_code_greenB	RW	[15:0]	Green (Blue Row) Analogue Gain Code
Digital Gain Registers								
0x020E	0x020F	2	0x0100	256	digital_gain_greenR	RW	[15:0]	Green (Red Row) channel digital gain value (1x)
0x0210	0x0211	2	0x0100	256	digital_gain_red	RW	[15:0]	Red channel digital gain value (1x)
0x0212	0x0213	2	0x0100	256	digital_gain_blue	RW	[15:0]	Blue channel digital gain value (1x)
0x0214	0x0215	2	0x0100	256	digital_gain_greenB	RW	[15:0]	Green (Blue Row) channel digital gain value (1x)
Clock Set-up Registers								
0x0300	0x0301	2	0x0002	2	vt_pix_clk_div	RW	[15:0]	Video Timing Pixel Clock Divider (dec:10)
0x0302	0x0303	2	0x0001	1	vt_sys_clk_div	RW	[15:0]	Video Timing System Clock Divider Value (dec:4)
0x0304	0x0305	2	0x0006	6	pre_pll_clk_div	RW	[15:0]	Pre PLL clock Divider Value (dec:4)
0x0306	0x0307	2	0x008C	140	pll_multiplier	RW	[15:0]	PLL multiplier Value (dec:144)
0x0308	0x0309	2	0x0008	8	op_pix_clk_div	RW	[15:0]	Output Pixel Clock Divider (dec:10)
0x030A	0x030B	2	0x0001	1	op_sys_clk_div	RW	[15:0]	Output System Clock Divider Value (dec:4)
0x030C	0x030D	2	0x0006	6	secnd_pre_pll_clk_div	RW	[15:0]	2nd PLL Pre PLL clock Divider Value (dec:4)
0x030E	0x030F	2	0x00A6	166	secnd_pll_multiplier	RW	[15:0]	2nd PLL multiplier Value (dec:144)
Frame Timing Registers								
0x0340	0x0341	2	0x09E8	###	frame_length_lines	RW	[15:0]	Frame Length (dec:1618)
0x0342	0x0343	2	0x0E60	###	line_length_pck	RW	[15:0]	Line Length (dec:2256)
Image Size Registers								
0x0344	0x0345	2	0x0004	4	x_addr_start	RW	[11:0]	X-address of the top left corner of the visible pixel data (dec:0)
0x0346	0x0347	2	0x0004	4	y_addr_start	RW	[10:0]	Y-address of the top left corner of the visible pixel data

Start	Finish	Size	Reset Value Hex	Reset Value Dec	Name	Type	Width	Description
								(dec:0)
0x0348	0x0349	2	0x0CC3	###	x_addr_end	RW	[11:0]	X-address of the bottom right corner of the visible pixel data (dec:2079)
0x034A	0x034B	2	0x0993	###	y_addr_end	RW	[10:0]	Y-address of the bottom right corner of the visible pixel data (dec:1567)
0x034C	0x034D	2	0x0CC0	###	x_output_size	RW	[15:0]	Width of image data output from the sensor module (dec:2080)
0x034E	0x034F	2	0x0990	###	y_output_size	RW	[15:0]	Height of image data output from the sensor module (dec:1568)
Sub-Sampling Registers								
0x0380	0x0381	2	0x0001	1	x_even_inc	RW	[15:0]	Increment for even pixels – 0, 2, 4 etc (dec:1)
0x0382	0x0383	2	0x0001	1	x_odd_inc	RW	[15:0]	Increment for odd pixels – 1, 3, 5 etc (dec:1)
0x0384	0x0385	2	0x0001	1	y_even_inc	RW	[15:0]	Increment for even pixels – 0, 2, 4 etc (dec:1)
0x0386	0x0387	2	0x0001	1	y_odd_inc	RW	[15:0]	Increment for odd pixels – 1, 3, 5 etc (dec:1)
Image Scaling Registers								
0x0400	0x0401	2	0x0002	2	Scaling_mode	RW	[15:0]	0 – No scaling,1 – Horizontal Scaling, 2 – Full Scaling (both horizontal and vertical)
0x0402	0x0403	2	0x0000	0	Spatial_sampling	RW	[15:0]	0 – Bayer Sampling, 1 – Co-sited, 2 – Reserved
0x0404	0x0405	2	0x0010	16	scale_m	RW	[15:0]	Down scale factor: M component Range: 1 to 4 upwards (dec:16) (1,1.5,2,3,4)->(16,24,32,48,64)
0x0406	0x0407	2	0x0010	16	scale_n	RW	[15:0]	Down scale factor: N component, Value: 16 (fixed) (dec:16)
0x0408	0x0409	2	0x0000	0	digital_crop_x_offset	RW	[15:0]	Offset from X-address of the top left corner of the visible pixel data after analog crop, bin and subsample
0x040A	0x040B	2	0x0000	0	digital_crop_y_offset	RW	[15:0]	Offset from Y-address of the top left corner of the visible

Start	Finish	Size	Reset Value Hex	Reset Value Dec	Name	Type	Width	Description
								pixel data after analog crop, bin and subsample
0x040C	0x040B	0	0x0000	0	digital_crop_image_width	RW	[15:0]	Image width after digital crop
0x040E	0x040F	2	0x0000	0	digital_crop_image_height	RW	[15:0]	Image height after digital crop
Image Compression Registers								
0x0500	0x0501	2	0x0001	1	compression_mode	RW	[15:0]	1 – DPCM/PCM Compression - Simple Predictor, 2 – DPCM/PCM – Advanced Predictor (dec:0 – no compression)
Test Pattern Registers								
0x0600	0x0601	2	0x0000	0	test_pattern_mode	RW	[15:0]	
0x0602	0x0603	2	0x0000	0	test_data_red	RW	[15:0]	(dec:512)
0x0604	0x0605	2	0x0000	0	test_data_greenR	RW	[15:0]	(dec:512)
0x0606	0x0607	2	0x0000	0	test_data_blue	RW	[15:0]	(dec:512)
0x0608	0x0609	2	0x0000	0	test_data_greenB	RW	[15:0]	(dec:512)
0x060A	0x060B	2	0x0000	0	horizontal_cursor_width	RW	[15:0]	(dec:0 – no h-cursor)
0x060C	0x060D	2	0x0000	0	horizontal_cursor_position	RW	[15:0]	(dec:256)
0x060E	0x060F	2	0x0000	0	vertical_cursor_width	RW	[15:0]	(dec:0 – no v-cursor)
0x0610	0x0611	2	0x0000	0	vertical_cursor_position	RW	[15:0]	(dec:256)
0x0612	0x0612	1	0x0000	0	pattern_crc	RW	[7:0]	
0x0613	0x0613	1	0x0000	0	pattern_fade_aux	RW	[7:0]	
0x0614	0x0614	1	0x0000	0	pattern_fade_factor	RW	[7:0]	
0x0615	0x0615	1	0x0000	0	pattern_fedtp_gradient_enable	RW	[7:0]	
0x0616	0x0616	1	0x0000	0	pattern_fedtp_gradient_invert	RW	[7:0]	

Start	Finish	Size	Reset Value Hex	Reset Value Dec	Name	Type	Width	Description
0x0617	0x0617	1	0x0000	0	pattern_fedtp_gradient_hor_shift	RW	[7:0]	
0x0618	0x0618	1	0x0000	0	pattern_fedtp_gradient_ver_shift	RW	[7:0]	
0x0619	0x0619	1	0x0000	0	pattern_fedtp_address_noise	RW	[7:0]	
0x061A	0x061A	1	0x0000	0	pattern_fedtp_hor_addr_noise_shift	RW	[7:0]	
0x061B	0x061B	1	0x0000	0	pattern_fedtp_ver_addr_noise_shift	RW	[7:0]	
0x061C	0x061C	1	0x0000	0	pattern_fedtp_random_noise_right	RW	[7:0]	
0x061D	0x061D	1	0x0000	0	pattern_fedtp_mode56_shift_rigth	RW	[7:0]	
FIFO Configuration Registers								
0x0700	0x0701	2	0x0000	0	fifo_water_mark_pixels	RW	[15:0]	FIFO usage level triggering CCP line output
D-PHY related timings								
0x0800	0x0800	1	0x0000	0	tclk_post	RW	[7:0]	Time that the transmitter shall continue sending HS clock after the Data Lane has transitioned to LP mode. The host will ensure that a suitable value is used
0x0801	0x0801	1	0x0000	0	ths_prepare	RW	[7:0]	The time to drive LP-00 before starting the HS transmission on the Data Lane.
0x0802	0x0802	1	0x0000	0	ths_zero_min	RW	[7:0]	The time to send HS-0, i.e. turn on the line termination and drive the interconnect with the HS driver, prior to sending the SoT sync sequence.
0x0803	0x0803	1	0x0000	0	ths_trail	RW	[7:0]	The time the transmitter must drive the flipped last data bit after sending the last payload data bit of an HS transmission burst. This time is required by the receiver to determine EOT.
0x0804	0x0804	1	0x0000	0	tclk_trail_min	RW	[7:0]	Time to drive the HS differential state after the last payload clock bit of an HS

Start	Finish	Size	Reset Value Hex	Reset Value Dec	Name	Type	Width	Description
								transmission burst
0x0805	0x0805	1	0x0002	2	tclk_prepare	RW	[7:0]	Time to drive LP-00 to prepare for HS clock transmission
0x0806	0x0806	1	0x0000	0	tclk_zero_zero	RW	[7:0]	Time for lead HS-0 drive period before starting the clock.
0x0807	0x0807	1	0x0000	0	tlpx	RW	[7:0]	Length of any low-power state period
0x0808	0x0808	1	0x0000	0	dphy_ctrl	RW	[7:0]	Value 0: Automatic in use Value 1: UI control in use Value 2: register control in use
CSI-2 Bitrate Negotiation Registers								
0x0820	0x0823	4	0x0000 00000	0	requested_link_bit_rate_mbps	RW	[31:0]	Target bitrate for CSI-2 transmission
Binning Configuration Registers								
0x0900	0x0900	1	0x0000	0	binning_mode	RW	[7:0]	0 – Disabled 1 - Enabled
0x0901	0x0901	1	0x0011	17	binning_type	RW	[7:0]	High nibble specifies Column Binning factor Low nibble specifies Row Binning factor
0x0902	0x0902	1	0x0001	1	binning_weighting	RW	[7:0]	Bit 0 = 1 : Averaged Bit 1 = 1 : Summed (for low light) Bit 2 = 1 : Bayer-corrected Bit 3 = 1 : User-defined weighting
Data Transfer Control & Data Registers								
0x0A00	0x0A00	1	0x0000	0	data_transfer_if_1_ctrl	RW	[7:0]	Bit 0: 1- enable. 0 - disable Bit 1: 1- write enable. 0 - read enable Bit 2: 1- clear error bits. Default value 0x00
0x0A01	0x0A01	1	0x0000	0	data_transfer_if_1_status	RW	[7:0]	Bit 0: 1 - read_if_ready Bit 1: 1 - write_if_ready Bit 2: 1- data corrupted Bit 3: 1 – improper if usage
0x0A02	0x0A02	1	0x0000	0	data_transfer_if_1_page_select	RW	[7:0]	Pages from 0 – 255. Default value 0x00
0x0A0	0x0A0	1	0x000	0	data_transfer_if_1_res	RW	[7:0]	

Start	Finish	Size	Reset Value Hex	Reset Value Dec	Name	Type	Width	Description
3	3		0		erved			
0x0A04	0x0A43	64	0x00000000	0	data_transfer_if_1_data	RW	64x[7:0]	64 x 8-bit register for read or write accesses
0x0A44	0x0A44	1	0x0000	0	data_transfer_if_2_ctrl	RW	[7:0]	Bit 0: 1- enable. 0 - disable Bit 1: 1- write enable. 0 - read enable Bit 2: 1- clear error bits. Default value 0x00
0x0A45	0x0A45	1	0x0000	0	data_transfer_if_2_status	RW	[7:0]	Bit 0: 1 - read_if_ready Bit 1: 1 - write_if_ready Bit 2: 1- data corrupted Bit 3: 1 – improper if usage
0x0A46	0x0A46	1	0x0000	0	data_transfer_if_2_page_select	RW	[7:0]	Pages from 0 – 255. Default value 0x00
0x0A47	0x0A47	1	0x0000	0	data_transfer_if_2_reserved	RW	[7:0]	
0x0A48	0x0A87	64	0x00000000	0	data_transfer_if_2_data	RW	64x[7:0]	64 x 8-bit register for read or write accesses
Internal Defect Correction								
0x0B00	0x0B00	1	0x0000	0	shading_correction_enable	RW	[7:0]	0 = shading correction disabled 1 = shading correction enabled
0x0B01	0x0B01	1	0x0080	128	luminance_correction_level	RW	[7:0]	Range 0 – 255 default = 128
0x0B02	0x0B02	1	0x0000	0	green_imbalance_filter_enable	RW	[7:0]	0 – Green imbalance filter disabled 1 – Green imbalance filter enabled default = 1
0x0B03	0x0B03	1	0x0000	0	green_imbalance_filter_weight	RW	[7:0]	Range 0 – 255 default = 128
0x0B04	0x0B04	1	0x0001	1	black_level_correction_enable	RW	[7:0]	0 – Black level correction disabled 1 – black level correction enabled default = 1
0x0B05	0x0B05	1	0x0001	1	mapped_couplet_correct_enable	RW	[7:0]	0 = correction disabled 1 = correction enabled default = 1
0x0B06	0x0B06	1	0x0000	0	single_defect_correct_enable	RW	[7:0]	0 = correction disabled 1 = correction enabled default = 1

Start	Finish	Size	Reset Value Hex	Reset Value Dec	Name	Type	Width	Description
0x0B07	0x0B07	1	0x0040	64	single_defect_correct_weight	RW	[7:0]	0x80 to 0xFF = limited auto 0x01 to 0x7F = manual 0x00 = bypass Default = 0x40 (mid-range)
0x0B08	0x0B08	1	0x0000	0	dynamic_couplet_correct_enable	RW	[7:0]	0 = correction disabled 1 = correction enabled default = 1
0x0B09	0x0B09	1	0x0040	64	dynamic_couplet_correct_weight	RW	[7:0]	0x80 to 0xFF = limited auto 0x01 to 0x7F = manual 0x00 = bypass Default = 0x40 (mid-range)
0x0B0A	0x0B0A	1	0x0000	0	combined_defect_correct_enable	RW	[7:0]	0 – combined defect correction disabled 1 – combined defect correction enabled default = 1 in case of that there is no dedicated corrections (i.e. dyn. Couplet or dyn. Singlet)
0x0B0B	0x0B0B	1	0x0000	0	combined_defect_correct_weight	RW	[7:0]	80 - FF = limited auto 1 – 7F = manual 0 = bypass Default = 0x40 (mid-range)
0x0B0C	0x0B0C	1	0x0000	0	module_specific_correction_enable	RW	[7:0]	0 = correction disabled 1 = correction enabled default = 1
0x0B0D	0x0B0D	1	0x0000	0	module_specific_correction_weight	RW	[7:0]	0x80 to 0xFF = limited auto 0x01 to 0x7F = manual 0x00 = bypass Default = 0x40 (mid-range)
0x0B0E	0x0B0E	1	###	###	mapped_line_defect_correct_enable	RW	[7:0]	0 – mapped line defect correction disabled 1 - mapped line defect correction enabled
0x0B0F	0x0B0F	1	###	###	mapped_line_defect_correct_adjust	RW	[7:0]	0x80 to 0xFF = limited auto 0x01 to 0x7F = manual 0x00 = bypass Default = 0x40 (mid-range)
0x0B10	0x0B10	1	###	###	mapped_couplet_correct_adjust	RW	[7:0]	0 – combined defect correction disabled 1 – combined defect correction enabled default = 1 in case of that there is no dedicated corrections (i.e. dyn.

Start	Finish	Size	Reset Value Hex	Reset Value Dec	Name	Type	Width	Description
								Couplet or dyn. Singlet)
0x0B11	0x0B11	1	###	###	mapped_triplet_defect_correct_enable	RW	[7:0]	80 - FF = limited auto 1 – 7F = manual 0 = bypass Default = 0x40 (mid-range)
0x0B12	0x0B12	1	###	###	mapped_triplet_defect_correct_adjust	RW	[7:0]	0 = correction disabled 1 = correction enabled default = 1
0x0B13	0x0B13	1	###	###	dynamic_triplet_defect_correct_enable	RW	[7:0]	0 – mapped triplet defect correction disabled 1 – mapped triplet defect correction enabled
0x0B14	0x0B14	1	###	###	dynamic_triplet_defect_correct_adjust	RW	[7:0]	80 - FF = limited auto 1 – 7F = manual 0 = bypass Default = 0x40 (mid-range)
0x0B15	0x0B15	1	###	###	dynamic_line_defect_correct_enable	RW	[7:0]	0 – dynamic line defect correction disabled 1 - dynamic line defect correction enabled
0x0B16	0x0B16	1	###	###	dynamic_line_defect_correct_adjust	RW	[7:0]	0x80 to 0xFF = limited auto 0x01 to 0x7F = manual 0x00 = bypass Default = 0x40 (mid-range)
EDOF Control								
0x0B80	0x0B80	1	0x0001	1	edof_mode	RW	[7:0]	Bit 0 – 0 EDOF disabled (default) Bit 1 – EDOF estimation type 1 enabled Bit 2 – EDOF enabled Bit 3 to 7 - reserved for future use
0x0B81	0x0B81	1	0x0000	0	est_depth_of_field	ROD	[7:0]	This represents the estimated depth of field measured 'outwards' from the nearest focus point (mapping to distance in cm)
0x0B82	0x0B82	1	0x0000	0	est_focus_distance	ROD	[7:0]	This represents the estimated nearest focus point (mapping

Start	Finish	Size	Reset Value Hex	Reset Value Dec	Name	Type	Width	Description
								to distance in cm)
0x0B83	0x0B83	1	0x0080	128	sharpness	RW	[7:0]	Host EDOF sharpness control :- 0x80 to 0xFF = limited auto 0x01 to 0x7F = manual 0x00 = bypass
0x0B84	0x0B84	1	0x0080	128	denoising	RW	[7:0]	Host EDOF denoising control :- 0x80 to 0xFF = limited auto 0x01 to 0x7F = manual 0x00 = bypass
0x0B85	0x0B85	1	0x0080	128	module_specific	RW	[7:0]	Slider which can be used for any specific tuning of EDOF block not covered by the above 0x80 to 0xFF = limited auto 0x01 to 0x7F = manual 0x00 = bypass
0x0B86	0x0B87	2	0x0000	0	depth_of_field	RW	[7:0]	This represents the depth of field measured 'outwards' from the nearest focus point (mapping to distance in cm) 0x8000 to 0xFFFF = limited auto 0x0000 to 0x7FFF = manual
0x0B88	0x0B89	2	0x0000	0	focus_distance	RW	[7:0]	This represents the depth of field measured 'outwards' from the nearest focus point (mapping to distance in cm) 0x8000 to 0xFFFF = limited auto 0x0000 to 0x7FFF = manual
Host AWB feedback								
0x0B8C	0x0B8D	2	0x0C80	###	colour_temperature	RW	[15:0]	Scene colour temperature in Kelvin
0x0B8E	0x0B8F	2	0x0000	0	absolute_gain_greenr	RW	[15:0]	Calculated gain for green-red channel
0x0B90	0x0B91	2	0x0000	0	absolute_gain_red	RW	[15:0]	Calculated gain for red channel
0x0B92	0x0B93	2	0x0000	0	absolute_gain_blue	RW	[15:0]	Calculated gain for blue channel
0x0B94	0x0B95	2	0x0000	0	absolute_gain_greenb	RW	[15:0]	Calculated gain for greenb channel
Integration Time Parameter Limit Registers								

Start	Finish	Size	Reset Value Hex	Reset Value Dec	Name	Type	Width	Description
0x1000	0x1001	2	0x0000	0	integration_time_capability	ROS	[0:0]	0 – coarse integration but NO fine integration 1 – course and smooth (1 pixel) fine integration
0x1002	0x1002	1	0x0000	0	Reserved	ROS		
0x1003	0x1003	1	0x0000	0		ROS		
0x1004	0x1005	2	0x0000	0	coarse_integration_time_min	ROS	[15:0]	Lines (dec:0)
0x1006	0x1007	2	0x0004	4	coarse_integration_time_max_margin	ROS	[15:0]	(Current frame length – current max coarse exp) (dec:2)
0x1008	0x1009	2	0x0000	0	fine_integration_time_min	ROS	[15:0]	Pixels (dec:266)
0x100A	0x100B	2	0x0000	0	fine_integration_time_max_margin	ROS	[15:0]	(Current line length – current max fine exp) (dec:466)
Digital Gain Parameter Limit Registers								
0x1080	0x1081	2	0x0000	0	digital_gain_capability	ROS	[0:0]	0 – none 1 – per channel digital gain
0x1082	0x1083	2	0x0000	0	Reserved	ROS		
0x1084	0x1085	2	0x0100	256	digital_gain_min	ROS	[15:0]	Minimum recommended digital gain value
0x1086	0x1087	2	0xFFFF	###	digital_gain_max	ROS	[15:0]	Maximum recommended digital gain value
0x1088	0x1089	2	0x0100	256	digital_gain_step_size	ROS	[15:0]	Defines the resolution of the digital gain control parameters.
Pre-PLL and PLL Clock Set-up Capability Registers								
0x1100	0x1103	4	0x40C00000	0	min_ext_clk_freq_mhz	ROS	[31:0]	Minimum external clock frequency
0x1104	0x1107	4	0x42800000	0	max_ext_clk_freq_mhz	ROS	[31:0]	Maximum external clock frequency
0x1108	0x1109	2	0x0001	1	min_pre_pll_clk_div	ROS	[15:0]	Minimum Pre PLL divider value
0x110A	0x110B	2	0x003F	63	max_pre_pll_clk_div	ROS	[15:0]	Maximum Pre PLL divider value
0x110C	0x110F	4	0x40400000	0	min_pll_ip_freq_mhz	ROS	[31:0]	Minimum PLL input clock frequency
0x111	0x111	4	0x40C	0	max_pll_ip_freq_mhz	RO	[31:0]	Maximum PLL input clock

Start	Finish	Size	Reset Value Hex	Reset Value Dec	Name	Type	Width	Description
0	3		00000			S		frequency
0x1114	0x1115	2	0x0001	1	min_pll_multiplier	ROS	[15:0]	Minimum PLL multiplier
0x1116	0x1117	2	0x01FF	511	max_pll_multiplier	ROS	[15:0]	Maximum PLL multiplier
0x1118	0x111B	4	0x43FA0000	0	min_pll_op_freq_mhz	ROS	[31:0]	Minimum PLL output clock frequency
0x111C	0x111F	4	0x447A0000	0	max_pll_op_freq_mhz	ROS	[31:0]	Maximum PLL output clock frequency
Video Timing Clock Set-up Capability Registers								
0x1120	0x1121	2	0x0001	1	min_vt_sys_clk_div	ROS	[15:0]	Minimum video timing system clock divider value
0x1122	0x1123	2	0x0008	8	max_vt_sys_clk_div	ROS	[15:0]	Maximum video timing system clock divider value
0x1124	0x1127	4	0x43FA0000	0	min_vt_sys_clk_freq_mhz	ROS	[31:0]	Minimum video timing system clock frequency
0x1128	0x112B	4	0x447A0000	0	max_vt_sys_clk_freq_mhz	ROS	[31:0]	Maximum video timing system clock frequency
0x112C	0x112F	4	0x42F00000	0	min_vt_pix_clk_freq_mhz	ROS	[31:0]	Minimum video timing pixel clock frequency
0x1130	0x1133	4	0x43DC0000	0	max_vt_pix_clk_freq_mhz	ROS	[31:0]	Maximum video timing pixel clock frequency
0x1134	0x1135	2	0x0001	1	min_vt_pix_clk_div	ROS	[15:0]	Minimum video timing pixel clock divider value
0x1136	0x1137	2	0x000A	10	max_vt_pix_clk_div	ROS	[15:0]	Maximum video timing pixel clock divider value
Frame Timing Parameter Limit Registers								
0x1140	0x1141	2	0x0064	100	min_frame_length_lines	ROS	[15:0]	Minimum Frame Length allowed.
0x1142	0x1143	2	0xFFFF	###	max_frame_length_lines	ROS	[15:0]	Maximum possible number of lines per Frame.
0x1144	0x1145	2	0x1028	###	min_line_length_pck	ROS	[15:0]	Minimum Line Length allowed.
0x1146	0x1147	2	0xFFFF	###	max_line_length_pck	ROS	[15:0]	Maximum possible number of pixel clocks per line.
0x1148	0x1149	2	0x011C	284	min_line_blanking_pck	ROS	[15:0]	Minimum line blanking time in pixel clocks
0x114A	0x114B	2	0x0036	54	min_frame_blanking_lines	ROS	[15:0]	Minimum frame blanking in video tming lines

Start	Finish	Size	Reset Value Hex	Reset Value Dec	Name	Type	Width	Description
0x114C	0x114D	2	0x0008	8	min_line_length_pck_step_size	ROS	[15:0]	Minimum step size of line length pck. Typical value may be 1,2 or 4. Units: Pixel Clocks
Output Clock Set-up Capability Registers								
0x1160	0x1161	2	0x0001	1	min_op_sys_clk_div	ROS	[15:0]	Minimum output system clock divider value
0x1162	0x1163	2	0x0008	8	max_op_sys_clk_div	ROS	[15:0]	Maximum output system clock divider value
0x1164	0x1167	4	0x42800000	0	min_op_sys_ck_clk_freq_mhz	ROS	[31:0]	Minimum output system clock frequency
0x1168	0x116B	4	0x44840000	0	max_op_sys_clk_freq_mhz	ROS	[31:0]	Maximum output system clock frequency
0x116C	0x116D	2	0x0004	4	min_op_pix_clk_div	ROS	[15:0]	Minimum output pixel clock divider value
0x116E	0x116F	2	0x000C	12	max_op_pix_clk_div	ROS	[15:0]	Maximum output pixel clock divider value
0x1170	0x1173	4	0x41000000	0	min_op_pix_clk_freq_mhz	ROS	[31:0]	Minimum output pixel clock frequency
0x1174	0x1177	4	0x43040000	0	max_op_pix_clk_freq_mhz	ROS	[31:0]	Maximum output pixel clock frequency
Image Size Parameter Limit Registers								
0x1180	0x1181	2	0x0000	0	x_addr_min	ROS	[15:0]	Minimum X-address of the addressable pixel array
0x1182	0x1183	2	0x0000	0	y_addr_min	ROS	[15:0]	Minimum Y-address of the addressable pixel array
0x1184	0x1185	2	0x0CC8	###	x_addr_max	ROS	[15:0]	Maximum X-address of the addressable pixel array
0x1186	0x1187	2	0x0998	###	y_addr_max	ROS	[15:0]	Maximum Y-address of the addressable pixel array
0x1188	0x1189	2	0x0100	256	min_x_output_size	ROS	[15:0]	Minimum x output size in pixels
0x118A	0x118B	2	0x0090	144	min_y_output_size	ROS	[15:0]	Minimum y output size in pixels
0x118C	0x118D	2	0x0CC8	###	max_x_output_size	ROS	[15:0]	Maximum x output size in pixels
0x118E	0x118F	2	0x0998	###	max_y_output_size	ROS	[15:0]	Maximum y output size in pixels
Sub-Sampling Parameter Limit Registers								
0x11C0	0x11C1	2	0x0001	1	min_even_inc	ROS	[15:0]	Minimum Increment for even pixels

Start	Finish	Size	Reset Value Hex	Reset Value Dec	Name	Type	Width	Description
0x11C2	0x11C3	2	0x0009	9	max_even_inc	ROS	[15:0]	Maximum increment for even pixels
0x11C4	0x11C5	2	0x0001	1	min_odd_inc	ROS	[15:0]	Minimum Increment for odd pixels
0x11C6	0x11C7	2	0x001D	29	max_odd_inc	ROS	[15:0]	Maximum Increment for odd pixels
Image Scaling Parameter Limit Registers								
0x1200	0x1201	2	0x0002	2	scaling_capability	ROS	[15:0]	0 – None 1 – Horizontal 2 – Full (Horizontal & Vertical)
0x1202	0x1203	2	0x0000	0	reserved	ROS	[15:0]	
0x1204	0x1205	2	0x0010	16	scaler_m_min	ROS	[15:0]	Down scale factor: Minimum M value
0x1206	0x1207	2	0x0080	128	scaler_m_max	ROS	[15:0]	Down scale factor: Maximum M value
0x1208	0x1209	2	0x0010	16	scaler_n_min	ROS	[15:0]	Down scale factor: Minimum N value
0x120A	0x120B	2	0x0010	16	scaler_n_max	ROS	[15:0]	Down scale factor: Maximum N value
0x1208	0x1209	2	0x0001	1	spatial_sampling_capability	ROS	[15:0]	
0x120A	0x120B	2	0x0001	1	digital_crop_capability	ROS	[15:0]	
Image Compression Capability Registers								
0x1300	0x1301	2	0x0002	2	compression_capability	ROS	[15:0]	0 – No Compression 1 – DPCM/PCM Compression
Colour Matrix Registers								
0x1400	0x1401	2	0x0000	0	matrix_element_RedInRed	ROS	[15:0]	Colour matrix parameter for Red in Red (dec:2.055)
0x1402	0x1403	2	0x0000	0	matrix_element_GreenInRed	ROS	[15:0]	Colour matrix parameter for Green in Red (dec:-0.555)
0x1404	0x1405	2	0x0000	0	matrix_element_BlueInRed	ROS	[15:0]	Colour matrix parameter for Blue in Red (dec:-0.148)
0x1406	0x1407	2	0x0000	0	matrix_element_RedInGreen	ROS	[15:0]	Colour matrix parameter for Red in Green (dec:-0.359)
0x1408	0x1409	2	0x0000	0	matrix_element_GreenInGreen	ROS	[15:0]	Colour matrix parameter for Green in Green (dec:1.578)
0x140A	0x140B	2	0x0000	0	matrix_element_BlueInGreen	ROS	[15:0]	Colour matrix parameter for Blue in Green (dec:-0.949)
0x140	0x140	2	0x000	0	matrix_element_RedIn	RO	[15:0]	Colour matrix parameter for

Start	Finish	Size	Reset Value Hex	Reset Value Dec	Name	Type	Width	Description
C	D		0		Blue	S		Red in Blue (dec:0.246)
0x140E	0x140F	2	0x0000	0	matrix_element_GreennInBlue	ROS	[15:0]	Colour matrix parameter for Green in Blue (dec:-0.324)
0x1410	0x1411	2	0x0000	0	matrix_element_BluelnBlue	ROS	[15:0]	Colour matrix parameter for Blue in Blue (dec:2.250)
FIFO Capability Registers								
0x1500	0x1501	2	0x0000	0	fifo_size_pixels	ROS	[15:0]	FIFO size in pixels (0 = no FIFO present)
0x1502	0x1503	2	0x0000	0	fifo_support_capability	ROS	[15:0]	Value 0 – not supported Value 1 – supports derating Value 2 – supports VT/OP domain decoupling
CSI Capability Registers								
0x1600	0x1600	1	0x0000	0	dphy_ctrl_capability	ROS	[2:0]	Bit 0 (Only UI capability) 0 : UI enough. 1 : register control is needed Bit 1 (Time and UI capability) 0 : UI enough. 1 : register control is needed Bit 2 (Time capability) 0 : UI enough. 1 : register control is needed
0x1601	0x1601	1	###	###	CSI_lane_mode_capability	ROS	[2:0]	Bit 0 :- 1 : 1-lane supported 0 : 1-lane not supported Bit 1 :- 1 : 2-lane supported 0 : 2-lane not supported Bit 2 :- 1 : 3-lane supported 0 : 3-lane not supported Bit 2 :- 1 : 4-lane supported 0 : 4-lane not supported
0x1602	0x1602	1	###	###	CSI_signalling_mode_capability	ROS	[2:0]	Bit 0 :- 1 - CCP2 Data/Clock supported 0 - not supported Bit 1 :- 1 - CCP2 Data/Strobe Signalling supported 0 - not supported Bit 2 :- 1 - CSI-2 supported 0 - not supported

Start	Finish	Size	Reset Value Hex	Reset Value Dec	Name	Type	Width	Description
0x1603	0x1603	1	0x0000	0	fast_standby_capability	ROS	[1:0]	0 – Frame truncation not supported for rolling shutter 1 – Frame truncation supported for rolling shutter
0x1605	0x1605	1	###	###	reserved	ROS		
0x1606	0x1606	1	###	###	reserved	ROS		
0x1607	0x1607	1	###	###	reserved	ROS		
0x1608	0x160B	4	###	###	max_per_lane_bitrate_1_lane_mode_mbps	ROS	[7:0]	32-bit unsigned iReal
0x160C	0x160F	4	###	###	max_per_lane_bitrate_2_lane_mode_mbps	ROS	[7:0]	32-bit unsigned iReal
0x1610	0x1613	4	###	###	max_per_lane_bitrate_3_lane_mode_mbps	ROS	[7:0]	32-bit unsigned iReal
0x1614	0x1617	4	###	###	max_per_lane_bitrate_4_lane_mode_mbps	ROS	[7:0]	32-bit unsigned iReal
Binning Capability Registers								
0x1700	0x1701	2	0x0064	100	min_frame_length_lines_bin	ROD	[15:0]	Minimum Frame Length allowed in binning mode
0x1702	0x1703	2	0xFFFF	###	max_frame_length_lines_bin	ROD	[15:0]	Maximum possible number of lines per Frame in binning mode
0x1704	0x1705	2	0x0ED8	###	min_line_length_pck_bin	ROD	[15:0]	Minimum Line Length allowed in binning mode Value: sensor dependent Units : Pixel Clocks
0x1706	0x1707	2	0xFFFF	###	max_line_length_pck_bin	ROD	[15:0]	Maximum possible number of pixel clocks per line in binning mode Value: sensor dependent Units : Pixel Clocks
0x1708	0x1709	2	0x011C	284	min_line_blanking_pck_bin	ROD	[15:0]	Minimum line blanking time in pixel clocks in binning mode Units : Pixel Clocks
0x170A	0x170B	2	0x0000	0	fine_integration_time_min_bin	ROD	[15:0]	Minimum fine integration time allowed in binning mode Value: sensor dependent Units: Pixels
0x170C	0x170D	2	0x0000	0	fine_integration_time_max_margin_bin	ROD	[15:0]	Margin used to determine the maximum fine integration time allowed in binning mode.

Start	Finish	Size	Reset Value Hex	Reset Value Dec	Name	Type	Width	Description
								Value: sensor dependent Units: Pixels
0x170E	0x170F	2	0x0000	0	fine_integration_time_max_margin_bin	ROD	[15:0]	Margin used to determine the maximum fine integration time allowed in binning mode. Value: sensor dependent Units: Pixels
0x1710	0x1710	1	0x0001	1	binning_capability	ROS	[7:0]	0 – None 1 - Yes
0x1711	0x1711	1	0x0003	3	binning_weighting_capability	ROS	[7:0]	0x00: averaged weighting 0x01: summed weighting 0x02: bayer weighting 0x03: module-specific weighting
0x1712	0x1712	1	0x000C	12	binning_sub_types	ROS	[7:0]	N - Number of Binning subtypes available
0x1713	0x1713	1	0x0042	66	binning_type_1	ROS	[7:0]	Example : 0x21 = Column x 2, Row x 1
0x1714	0x1714	1	0x0044	68	binning_type_2	ROS	[7:0]	Example : 0x22 = Column x 2, Row x 2
0x1715	0x1715	1	0x0048	72	binning_type_3	ROS	[7:0]	Example : 0x31 = Column x 3, Row x 1
0x1716	0x1716	1	0x0022	34	binning_type_4	ROS	[7:0]	Example : 0x33 = Column x 3, Row x 3
0x1717	0x1717	1	0x0024	36	binning_type_5	ROS	[7:0]	Example : 0x41 = Column x 4, Row x 1
0x1718	0x1718	1	0x0028	40	binning_type_6	ROS	[7:0]	Example : 0x42 = Column x 4, Row x 2
0x1719	0x1719	1	0x0012	18	binning_type_7	ROS	[7:0]	Example : 0x44 = Column x 4, Row x 4
0x171A	0x171A	1	0x0014	20	binning_type_8	ROS	[7:0]	Example : 0x42 = Column x 4, Row x 2
0x171B	0x171B	1	0x0018	24	binning_type_9	ROS	[7:0]	Example : 0x44 = Column x 4, Row x 4
0x171C	0x171C	1	0x0021	33	binning_type_10	ROS	[7:0]	Example : 0x42 = Column x 4, Row x 2
0x171D	0x171D	1	0x0041	65	binning_type_11	ROS	[7:0]	Example : 0x44 = Column x 4, Row x 4
0x171E	0x171E	1	0x0081	129	binning_type_12	ROS	[7:0]	Example : 0x42 = Column x 4, Row x 2
0x171	0x171	1	0x000	0	binning_type_13	RO	[7:0]	Example : 0x44 = Column x 4,

Start	Finish	Size	Reset Value Hex	Reset Value Dec	Name	Type	Width	Description
F	F		0			S		Row x 4
Data Upload/Download Interface Capability								
0x1800	0x1800	1	0x000F	15	data_transfer_if_capability	ROS	[7:0]	Bit 0: 1 – interface 1 supported Bit 1: 1 – interface 2 supported Bit 2: 0 – polling not needed in reading Bit 3: 0 – polling not needed in writing 1 = internal module shading correction present
Ideal raw and EDOF Capability Registers								
0x1900	0x1900	1	0x0003	3	shading_correction_capability	ROS	[7:0]	0 = internal module shading correction NOT present 1 = internal module shading correction present
0x1901	0x1901	1	0x0000	0	green_imbalance_capability	ROS	[7:0]	b0=1: on-module green imbalance filtering
0x1902	0x1902	1	0x0001	1	black_level_capability	ROS	[7:0]	b0=1: black level correction available
0x1903	0x1903	1	0x0000	0	module_specific_correction_capability	ROS	[7:0]	Bit 0: 0 – not supported. 1 – Manual supported Bit 1: 0 – not supported. 1 – Limited auto supported

Start	Finish	Size	Reset Value Hex	Reset Value Dec	Name	Type	Width	Description
0x1904	0x1905	2	0x0000	0	defect_correction_capability	ROS	[15:0]	b0=1: internal module mapped couplet correction available B1=1: internal module mapped couplet correction weight available B2=1: internal module dynamic couplet correction available B3=1: manual dynamic couplet correction weight adjust available B4=1: limited auto dynamic couplet correction weight adjust available B5=1: internal module dynamic single pixel defect correction available B6=1: manual dynamic single pixel defect correction weight adjust available B7=1: limited auto dynamic single pixel defect correction weight adjust available B8=1: combined internal module dynamic couplet & single pixel defect correction available B9=1: manual dynamic couplet & single pixel defect correction weight adjust available B10=1: limited auto dynamic couplet & single pixel defect correction weight adjust available

Start	Finish	Size	Reset Value Hex	Reset Value Dec	Name	Type	Width	Description
0x1906	0x1907	2	0x0000	0	module_specific_correction_capability	ROS	[15:0]	B0=1: internal module mapped triplet correction available B1=1: manual mapped triplet correction weight adjust available B2=1: limited auto mapped triplet correction weight adjust available B3=1: internal module dynamic triplet correction available B4=1: manual dynamic triplet correction weight adjust available B5=1: limited auto dynamic triplet correction weight adjust available B6=1: internal module dynamic line correction available B7=1: manual dynamic line correction weight ajust available B8=1: limited auto dynamic line correction weight adjust available Other bits: reserved for future extensions
EDOF Capability								
0x1980	0x1980	1	0x0001	1	edof_capability	ROS	[1:0]	0 – None 1 – EDOF present
0x1981	0x1981	1	0x0000	0	estimation_frames	ROS	[1:0]	0 – No estimation frames are required Other value – the number of estimation frames required
0x1982	0x1982	1	0x0000	0	supports_sharpness_adj	ROS	[1:0]	0 – Not supported 1 – Supported
0x1983	0x1983	1	0x0000	0	supports_denoising_adj	ROS	[1:0]	0 – Not supported 1 – Supported
0x1984	0x1984	1	0x0000	0	supports_module_specific_adj	ROS	[1:0]	0 – Not supported 1 – Supported
0x1985	0x1985	1	0x0000	0	supports_depth_of_field_adj	ROS	[1:0]	Bit 0 :-0 – not supported.1 – manual supported Bit 1 : -0 – not supported.1 – limited auto supported

Start	Finish	Size	Reset Value Hex	Reset Value Dec	Name	Type	Width	Description
0x1986	0x1986	1	0x0000	0	supports_focus_distance_adj	ROS	[1:0]	Bit 0 :- 0 – not supported. 1 – manual supported Bit 1 : -0 – not supported. 1 – limited auto supported
0x1987	0x1987	1	0x0001	1	colour_feedback_capability	ROS	[1:0]	Bit 0 – module requires Kelvin feedback Bit 1 – module requires AWB gain feedback
0x1988	0x1988	1	0x0000	0	edof_support_AB_nxm	ROD	[1:0]	Bit 0 = 0 – EDOF not supported in n x m binned mode Bit 0 = 1 - EDOF supported in n x m binned mode Bit 1 = 0 – new coefficient/patch download required. Bit 1 = 1 – no coefficient/patch download required (or download has taken place)

11.1.2 Configuration Registers 2 [0xD0003000 to 0xD0003FFF]

Start	Finish	Size	Reset Value Hex	Reset Value Dec	Name	Type	Width	Description
0x3000	0x3000	1	0x0000	0	vendor_error_type	RW	[7:0]	System level error: 0 no error 1 external clock is not defiend 2 external clock is defined, but out of range 3 pre_pll_clk_div is out of range 4 pll_ip_freq is out of range 5 pll_multiplier is out of range 6 pll_op_freq is out of range 7 vt_sys_div is out of range 8 vt_pix_div is out of range 9 vt_sys_freq is out of range 10 vt_pix_freq is out of range 11 op_sys_div is out of range 12 op_pix_div is out of range 13 op_sys_freq is out of range 14 op_pix_freq is out of range 15 bad_div_vt_sys is out of range 16 bad_div_op is out of range 17 dclk_div is out of range 18 smiaRegs_rw_clocks_secnd_pre_pll_clk_div is out of range 19 smiaRegs_rw_clocks_secnd_pll_multiplier is out of range 20 Second PLL VCO is is out of range 32 two or more functions are assigned to same GPIO 40 failed to allocate BPC tables
0x3001	0x3001	1	0x0000	0	vendor_pll_bypass	RW	[7:0]	Locked on enable streaming 0 PLL is operational 1 PLL is bypass
0x3002	0x3002	1	0x0000	0	vendor_pll_use_exact_vt_pix_clk_div	RW	[7:0]	Locked on enable streaming 0 vt_pix_clk_div is multiplied by 4 1 vt_pix_clk_div is used "as is" (this option is useful for deviders not equal to 4,8,12)

Start	Finish	Size	Reset Value Hex	Reset Value Dec	Name	Type	Width	Description
0x3003	0x3003	1	0x0000	0	vendor_pll_use_fixed_dclk_div	RW	[7:0]	Determine whether searching for the minimal dclk divider possible per current state
0x3004	0x3004	1	0x0002	2	vendor_pll_dclk_min_ratio_numer	RW	[7:0]	Numer/denum – the minimal frequency ratio between Dclk/SysClk
0x3005	0x3005	1	0x0001	1	vendor_pll_dclk_min_ratio_denum	RW	[7:0]	Numer/denum – the minimal frequency ratio between Dclk/SysClk
0x3006	0x3006	1	0x0000	0	vendor_pll_scale_up_ext_clock	RW	[7:0]	Allows using input clock higher than 255.99MHz. For example, input clock 260MHz will be set as 0x8200 on smia register smiaRegs_rw_op_cond_extclk_frequency_mhz, and as 0x01 on this vendor register (130MHz << 1 = 260MHz).
0x3007	0x3007	1	0x0000	0	vendor_pll_reserved	RW	[7:0]	#N/A
0x3008	0x3009	2	0x0000	0	vendor_sensor_offset_x	RW	[15:0]	Allow to cut off left side of output image
0x300A	0x300B	2	0x0000	0	vendor_sensor_offset_y	RW	[15:0]	Allow to cut off top side of output image
0x300C	0x300C	1	0x0001	1	vendor_sensor_abort_timing_on_sw_stby	RW	[7:0]	When entering sw stby: 0 – Wait till end of timing frame before entering sw stby 1 – Abort timing frame on end of readout and enter sw stby
0x300D	0x300D	1	0x0000	0	vendor_sensor_physical_pixel_order	RW	[7:0]	Defines color of physical pixel 0,0: 0: Gr Rg / Bg Gb 1: Rg Gr / Gb Bg 2: Bg Gb / Gr Rg 3: Gb Bg / Rg Gr
0x300E	0x300E	1	0x0001	1	vendor_sensor_dynamic_aac	RW	[7:0]	Reserved.
0x300F	0x300F	1	0x0000	0	vendor_sensor_disabl	RW	[7:0]	Disable Ladlc according fadlc

Start	Finish	Size	Reset Value Hex	Reset Value Dec	Name	Type	Width	Description
					e_ladlc_with_fadlc			state
0x3010	0x3010	1	0x0000	0	vendor_sensor_out_type	RW	[7:0]	0 - SMIA_OUT_VISIBLE_ONLY 1 - SMIA_OUT_VISIBLE_AND_DARK 2 - SMIA_OUT_ALL
0x3011	0x3011	1	0x0001	1	vendor_sensor_dig_hor_bin_scale_fact	RW	[7:0]	1 - No Binning 2 - Use digital binning 1:2 instead of analog binning (on the horizontal axis) 4 - Use digital binning 1:4 instead of analog binning (on the horizontal axis)
0x3012	0x3012	1	0x0000	0	vendor_sensor_emb_use_header	RW	[7:0]	0 Disable heading embedded line 1 Enable heading embedded line
0x3013	0x3013	1	0x0004	4	vendor_sensor_emb_header_lines	RW	[7:0]	Defines the number of embedded lines (1-4). Default value is 4.
0x3014	0x3014	1	0x0000	0	vendor_sensor_emb_footer_lines	RW	[7:0]	0 Disable footering embedded line 1 Enable footering embedded line
0x3015	0x3015	1	0x0000	0	vendor_sensor_enable_immediate_exp	RW	[7:0]	0 Disable immidiate update for integration time and analog gain 1 Enable immidiate update for integration time and analog gain
0x3016	0x3016	1	0x0000	0	vendor_dyn_opt_dummy	RW	[7:0]	Reserved
0x3017	0x3017	1	0x0000	0	vendor_isp_reinit	RW	[7:0]	Enable reinit of GRAS, GOS, DADLC tables 1 Update GRAS tables 2 Update GOS tables 4 Update DADLC tables 8 Prepare GRAS tables

Start	Finish	Size	Reset Value Hex	Reset Value Dec	Name	Type	Width	Description
0x3018	0x3018	1	0x0003	3	vendor_isp_close_clock	RW	[7:0]	0 - CLOSE_ISP_CLOCK_NEVER 1 - CLOSE_ISP_CLOCK_ALWAYS 2 - CLOSE_ISP_CLOCK_AUTO 3 - CLOSE_ISP_CLOCK_AUTO_POWER_SAVE
0x3019	0x3019	1	0x0011	17	vendor_isp_afit_gain_channel_mask	RW	[7:0]	Msb - Dgain channel , Lsb - Agsin Channel
0x301A	0x301A	1	0x0001	1	vendor_isp_resizer_keep_ds_rate	RW	[7:0]	Not applicable
0x301B	0x301B	1	0x0000	0	vendor_isp_resizer_aligned	RW	[7:0]	If align is on then row length rounding up to 16 pixels for 10bit Bayer,to 8 for 12 bit and to 4 pixels for 8 bit creating line size which divide 32 bits. 14 bits are extended to 16 => 2 pixels for 32 bits -> always exist.
0x301C	0x301D	2	0x0000	0	vendor_gras_nvm_address	RW	[15:0]	NVM address of beginning GRAS data
0x301E	0x301F	2	0x0000	0	vendor_gras_load_from	RW	[15:0]	0 Fill up GRAS tables with zero 1 Prevent FW acess to GRAS tables, allow to load GRAS tables directly into HW regs 2 Using tables and parabolas from RAM 3 Using tables and parabolas from NVM 4 Using incremental tables from NVM
0x3020	0x3023	4	0x0000	0	vendor_gras_reserved	RW	[31:0]	#N/A
0x3024	0x3027	4	0x0000 0000	0	vendor_gras_grid	RW	[31:0]	Pointer to GRAS grids

Start	Finish	Size	Reset Value Hex	Reset Value Dec	Name	Type	Width	Description
0x3028	0x302B	4	0x00000000	0	vendor_gras_para	RW	[31:0]	Pointer to GRAS parameters and matrices
0x302C	0x302F	4	0x00000000	0	vendor_gras_buffer	RW	[31:0]	0
0x3030	0x3031	2	0x0000	0	vendor_gos_nvm_address	RW	[15:0]	address of GRAS data in NVM
0x3032	0x3033	2	0x0000	0	vendor_gos_load_from	RW	[15:0]	0 Fill up GOS tables with zero 1 Prevent FW acess to GOS tables, allow to load GOS tables directly into HW regs 2 Using tables and parabolas from RAM 3 Using tables and parabolas from NVM
0x3034	0x3037	4	0x0000	0	vendor_gos_reserved	RW	[31:0]	#N/A
0x3038	0x303B	4	0x00000000	0	vendor_gos_address	RW	[31:0]	address of GOS data in NVM
0x303C	0x303F	4	0x00000000	0	vendor_gos_buffer	RW	[31:0]	Pointer to GOS grids
0x3040	0x3043	4	0x00000000	0	vendor_offs_gain_buffer	RW	[31:0]	Reserved.
0x3044	0x3044	1	0x0001	1	vendor_bpc_halt_when_dynamic_allocation_failed	RW	[7:0]	When true, Cause FW to halt (endless loop) if it failed to allocate all required memory for BPC tables
0x3045	0x3045	1	0x0000	0	vendor_bpc_reserved	RW	[7:0]	#N/A
0x3046	0x3047	2	0x0028	40	vendor_bpc_max_clusters_in_nvm	RW	[15:0]	Maximum number of clusters in NVM (option to modify projects defaults)
0x3048	0x3048	1	0x0000	0	vendor_oif_ccp2	RW	[7:0]	Enable(1)/Disable(0) CCP2 frame packing on PVI
0x3049	0x3049	1	0x0000	0	vendor_oif_vsync_pulse_width	RW	[7:0]	Defines width of vsync pulse in PVI clocks
0x304A	0x304A	1	0x0000	0	vendor_oif_mipi_over_	RW	[7:0]	Enable(1)/Disable(0) MIPI

Start	Finish	Size	Reset Value Hex	Reset Value Dec	Name	Type	Width	Description
					pvi			output over PVI
0x304B	0x304B	1	0x0000	0	vendor_oif_slvs_over_pvi	RW	[7:0]	Enable(1)/Disable(0) SLVS output over PVI
0x304C	0x304D	2	0x0008	8	vendor_oif_pvi_bits	RW	[15:0]	[1:1] invert polarity of VSYNC signal [2:2] invert polarity of HSYNC signal [3:3] invert polarity of PCLK signal [12:12] outputs 8.2 or 8.4 format
0x304E	0x304E	1	0x0000	0	vendor_oif_vsync_on_frame_start	RW	[7:0]	0 VSYNC toggles on first pixel 1 VSYNC toggles on frame start
0x304F	0x304F	1	0x0000	0	vendor_oif_qual_mode	RW	[7:0]	0 // 000 Legacy mode of continuous clock - PCLK always on 1 // 001 Qualified clock - on VSYNC rise and fall and on HSYNC valid - Legacy qualified clock 2 // 010 Qualified clock - on VSYNC rise and fall and on overlap HSYNC valid - Legacy qualified clock + new overlap HSYNC 5 // 101 Qualified clock - on HSYNC valid but no clock on VSYNC. Only on data. 6 // 110 Qualified clock - on overlap HSYNC valid but no clock on VSYNC. Only on data + overlap HSYNC.
0x3050	0x3050	1	0x0001	1	vendor_oif_disable_pads_on_stdby	RW	[7:0]	Enable(1)/Disable(0) High-Z on PVI pads while in standby.

Start	Finish	Size	Reset Value Hex	Reset Value Dec	Name	Type	Width	Description
0x3051	0x3051	1	0x0000	0	vendor_oif_pvi_CIS_bits	RW	[7:0]	Equvalent to HW register outregs_cis_via_pvi_vclkout_inv_pol [0:0] Enable OUTIF cis_via_pvi testbus. This testbus is special testbus output that transmit ISP line directly from OUTIF RAM working with sys_clk. outregs_cis_via_pvi_vclkout_inv_pol – [4:4] 0 cis_via_pvi_validv is active low/ 1 cis_via_pvi_validv is active high [5:5] 0 cis_via_pvi_validh is active low/ 1 cis_via_pvi_validh is active high [6:6] 0 cis_via_pvi_vclkout = sys_clk/ 1 cis_via_pvi_vclkout = !sys_clk
0x3052	0x3052	1	0x0001	1	vendor_mipi_ulpm_on_stby	RW	[7:0]	Enable(1)/Disable(0) ULPM sequence MIPI on standby
0x3053	0x3053	1	0x0000	0	vendor_mipi_use_extra_packets	RW	[7:0]	Enable(1)/Disable(0) generation line start/end short packets for MIPI protocol
0x3054	0x3054	1	0x002C	44	vendor_mipi_user_type	RW	[7:0]	If set, MIPI data type will be set accordingly.
0x3055	0x3055	1	0x0001	1	vendor_mipi_emb_equal_to_data	RW	[7:0]	Keep embedded line same length as pixels line: 0 - Embedded line length is shorter then data line length 1 - Embedded line length is equal to data line length

Start	Finish	Size	Reset Value Hex	Reset Value Dec	Name	Type	Width	Description
0x3056	0x3056	1	0x0001	1	vendor_mipi_emb_in_bytes	RW	[7:0]	Keep embedded line same length as pixels line: 0 - Each embedded line pixel is byte 1 - Each embedded line pixel is equal to data pixel
0x3057	0x3057	1	0x0004	4	vendor_mipi_dphy_max_lanes	RW	[7:0]	Limits maximal number of enabled MIPI lines
0x3058	0x3058	1	0x0001	1	vendor_mipi_vsync_on	RW	[7:0]	Enable(1)/Disable(0) Vsync pad signal activity when in MIPI mode. Allows user to output Vsync pad when in MIPI.
0x3059	0x3059	1	0x0064	100	vendor_mipi_t_init	RW	[7:0]	uSec delay after dphy enable
0x305A	0x305A	1	0x0000	0	vendor_mipi_elg_mode	RW	[7:0]	0 - Embedded data is presented on the MSBs of the pixel (when pixel bits is higher then 8). 1 - Embedded data is presented on the LSBs of the pixel.
0x305B	0x305B	1	0x0000	0	vendor_gpios_use_12bit_pvi	RW	[7:0]	connect D1 to GPIO1 and D0 to GPIO2
0x305C	0x305C	1	0x0001	1	vendor_gpios_ms_index	RW	[7:0]	defines GPIO number for mechanical shautter strobe out. Values: 0,1,2
0x305D	0x305D	1	0x0002	2	vendor_gpios_flash_index	RW	[7:0]	defines GPIO number for flash strobe out. Values: 0,1,2
0x305E	0x305E	1	0x0000	0	vendor_gpios_cmnd_gpi_index	RW	[7:0]	defines GPIO number for mechanical shutter strobe in. Values: 0,1,2
0x305F	0x305F	1	0x0000	0	vendor_gpios_reserved	RW	[7:0]	#N/A
0x3060	0x3060	1	0x0000	0	vendor_dphy_reserved_0_	RW	[7:0]	#N/A
0x3061	0x3061	1	0x0000	0	vendor_dphy_reserved_1_	RW	[7:0]	#N/A

Start	Finish	Size	Reset Value Hex	Reset Value Dec	Name	Type	Width	Description
0x3062	0x3062	1	0x0000	0	vendor_dphy_reserved_2_	RW	[7:0]	#N/A
0x3063	0x3063	1	0x0000	0	vendor_dphy_reserved_3_	RW	[7:0]	#N/A
0x3064	0x3064	1	0x0000	0	vendor_ms_enable	RW	[7:0]	enable/disable mechanical shutter
0x3065	0x3065	1	0x0001	1	vendor_ms_with_global_reset	RW	[7:0]	enable/disable mechanical shutter with global reset
0x3066	0x3066	1	0x0000	0	vendor_ms_exp_shifter	RW	[7:0]	Allows very long exposures when in mechanical shutter.
0x3067	0x3067	1	0x0003	3	vendor_ms_invoke_method	RW	[7:0]	0 Mechanical shutter abort readout/timing of current frame. 1 Mechanical shutter abort timing of current frame. 2 Mechanical shutter preserve timing of current frame.
0x3068	0x306B	4	0x00000000	0	vendor_ms_close_bef_exp_end_pixels	RW	[31:0]	offset from global reset event to closing mechanical shutter
0x306C	0x306F	4	0x00000000	0	vendor_ms_open_bef_fr_end_pixels	RW	[31:0]	offset from global reset event to opening mechanical shutter
0x3070	0x3073	4	0x00000000	0	vendor_ms_open_flash_ofs_pixels	RW	[31:0]	offset from global reset event to flash pulse
0x37F8	0x37F8	1	0x0000	0	AnalogGainPrecision	RW	[1:0]	Analog gain resolution control. AG = analogue_gain_code_global/ $2^{(AnalogGainPrecision + 5)}$
0x3972	0x3972	1	0x0000	0	nvm_charge_pump_lvl	RW	[0]	0 = NVM: Set x1 charge pump mode 1= NVM: Set x1.5 charge pump mode

11.1.3 Configuration Registers 3 [0xD000F000 to 0xD000FFFF]

Start	Finish	Size	Reset Value Hex	Reset Value Dec	Name	Type	Width	Description
0xF470	0xF472	2	0x00C5	197	reg_gtg_aig_tx_ptr1	RW	[13:0]	Timing generator pointer. Holding calculated exposure offset. FW controlled, do not overwrite

12 Mechanical

12.1 Package Specification

Refer to S5K3H7YX_Assembly_Guide