SMARTSENS

SmartSens™
SC2336 Datasheet

Preliminary V0.7

2021.9.13

■ Applications

- ◆ Security cameras
- ◆ Home security surveillance systems
- ◆ IoT cameras

■ Features

- ◆ High sensitivity
- ◆ High signal to noise ratio
- ◆ 32× analog gain, 4× digital gain
- ◆ High speed DPC
- ◆ External control frame rate, multiple sensors synchronization
- ◆ Horizontal/vertical windowing
- ◆ 2 × 2 binning mode
- ◆ Programmable I2C port register

■ Specifications

Parameters	Description
Resolution	2 MP
Pixel array	1928H x 1088V
Pixel size	2.7 μm x 2.7 μm
Optical format	1/3”
Maximum frame rate	1920H x 1080V@30fps 10bit
Output interface	10/8-bit 1/2Lane MIPI, 10-bit DVP
Output format	RAW RGB
CRA	12°
Sensitivity	6594 mV/lux • s
Dynamic range	74 dB
SNR	36 dB
Operation temperature range	-30°C ~ +85°C
Best IQ temperature	-20°C ~ +60°C
Power supply	AVDD = 2.8V ± 0.1V, DVDD (internal power supply recommended), DOVDD = 1.8V ± 0.1V
Package	CSP, 5.718 mm x 3.663 mm, 35-pin
ESD rank	TBD

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1. System Description

1.1. General Description

SC2336 is an advanced digital CMOS image sensor for automotive fields, supporting a maximum resolution of 1920H × 1080V@30fps. It outputs raw images with an effective pixel array of 1928H × 1088V and supports complex on-chip operations such as windowing, horizontal or vertical mirroring, and so on. It can be configured via the standard I²C interface. It can achieve external control of frame rate and multiple sensor synchronization via the EFSYNC/FSYNC pin.

1.2. System Framework

Figure 1-1 shows the block diagram of SC2336. SC2336 supports the Mobile Industry Processor Interface (MIPI) and Digital Video Port (DVP). Figure 1-2 shows a typical configuration example using the MIPI.

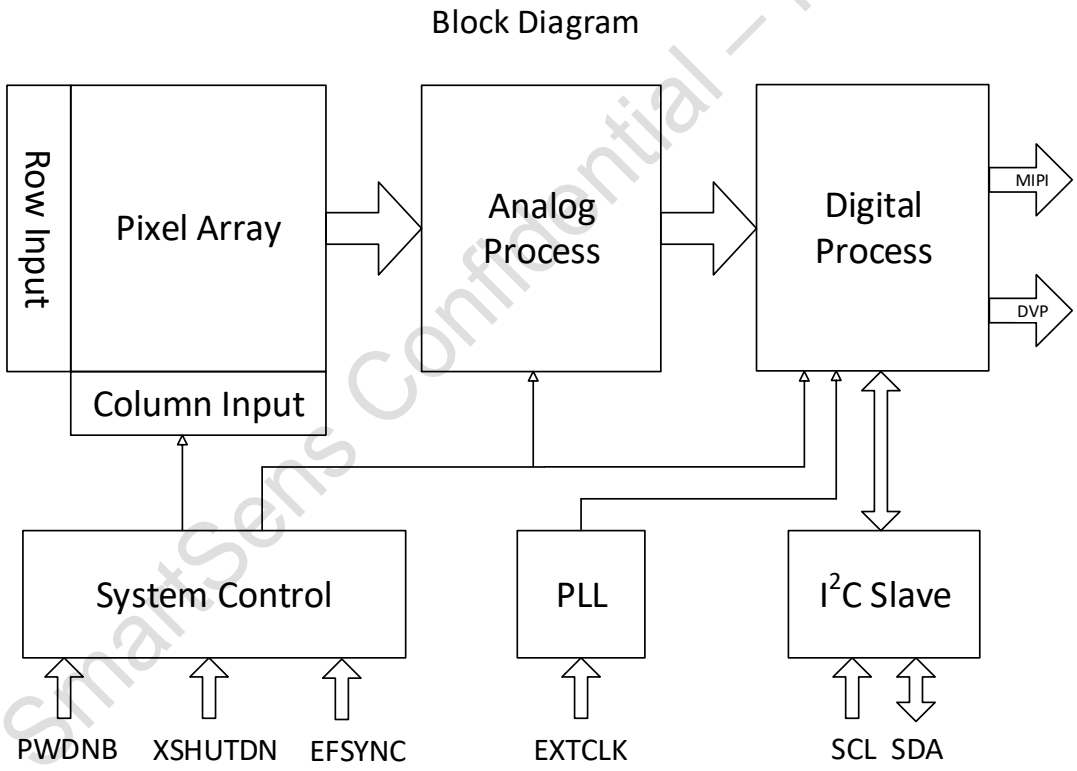

Figure 1-1 Block diagram

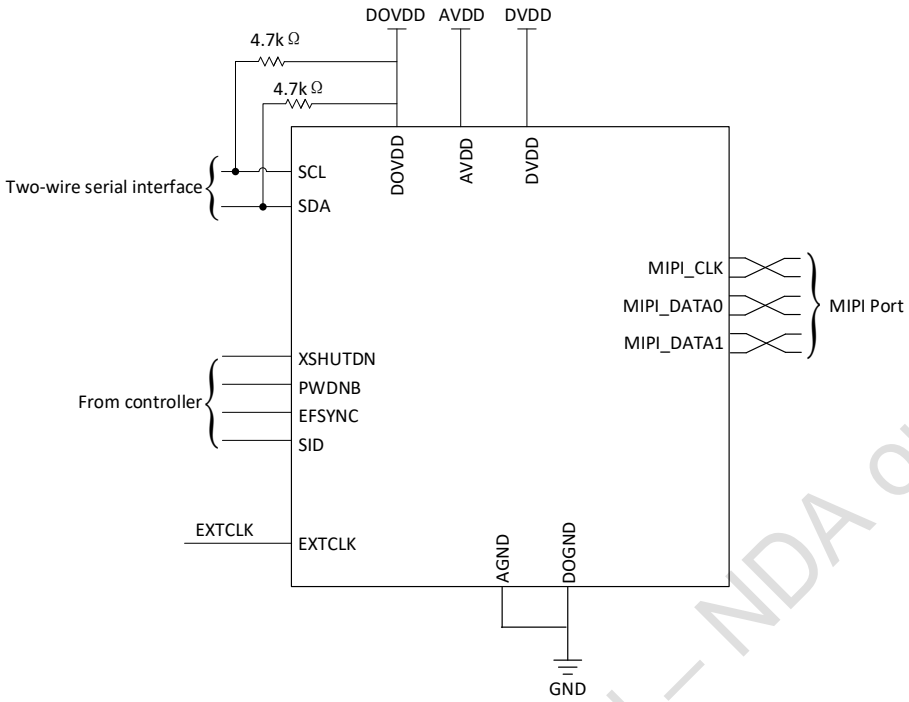

Figure 1-2 Typical configuration diagram

1.3. Pin Description

The table below lists the pin information and related description of SC2336.

Table 1-1 Pin description

No.	Pin No.	Pin Name	Pin Type	Description
1	A1	AGND	GND	Analog Ground
2	A2	LREF	Output	DVP Row SYNC
3	A3	EXTCLK	Input	Clock Input
4	A4	SDA	Input / Output	I^2C Data Line (open drain)
5	A5	SCL	Input	I^2C Clock Line
6	A6	XSHUTDN	Input	Reset Signal Input (internal pull-up, active low)
7	A7	EFSYNC	Input	External frame synchronization signal
8	B1	AVDD	Power	2.8V Analog Power Supply
9	B2	DOGND	GND	I/O Ground
10	B3	FSYNC	Output	As an external frame synchronization signal when input As a DVP frame synchronization signal when output
11	B4	DVDD	Power	Digital Power Supply (internal power supply by LDO)
12	B5	SID	Input	I^2C Device ID (internal pull-down, device ID = 7'h30)
13	B6	DVDD	Power	Digital Power Supply (internal power supply by LDO)
14	B7	AVDD	Power	2.8V Analog Power Supply
15	C1	DVDD	Power	Digital Power Supply (internal power supply by

No.	Pin No.	Pin Name	Pin Type	Description
				LDO)
16	C2	DOVDD	Power	1.8V I/O Power Supply
17	C3	DOVDD	Power	1.8V I/O Power Supply
18	C4	D<6>/MCP	Output	DVP Output Bit [6]/MIPI Clock Positive
19	C5	D<9>	Output	DVP Output Bit [9]
20	C6	PWDNB	Input	Power Down (internal pull-up, active low)
21	C7	AGND	GND	Analog Ground
22	D1	D<1>	Output	DVP Output Bit [1]
23	D2	D<3>/MD1N	Output	DVP Output Bit [3]/MIPI Data 1 Negative
24	D3	D<4>/MD1P	Output	DVP Output Bit [4]/MIPI Data 1 Positive
25	D4	PCLK/MCN	Output	DVP Clock/ MIPI Clock Negative
26	D5	D<7>/MD0N	Output	DVP Output Bit [7]/MIPI Data 0 Negative
27	D6	DOGND	GND	I/O Ground
28	D7	VREFN	Output	Internal Reference Voltage (connect an external capacitor to the AGND pin)
29	E1	D<0>	Output	DVP Output Bit [0]
30	E2	D<2>	Output	DVP Output Bit [2]
31	E3	D<5>	Output	DVP Output Bit [5]
32	E4	DVDD	Power	Digital Power Supply (internal power supply by LDO)
33	E5	D<8>/MD0P	Output	DVP Output Bit [8]/ MIPI Data 0 Positive
34	E6	NC	-	NC
35	E7	NC	-	NC

Top View

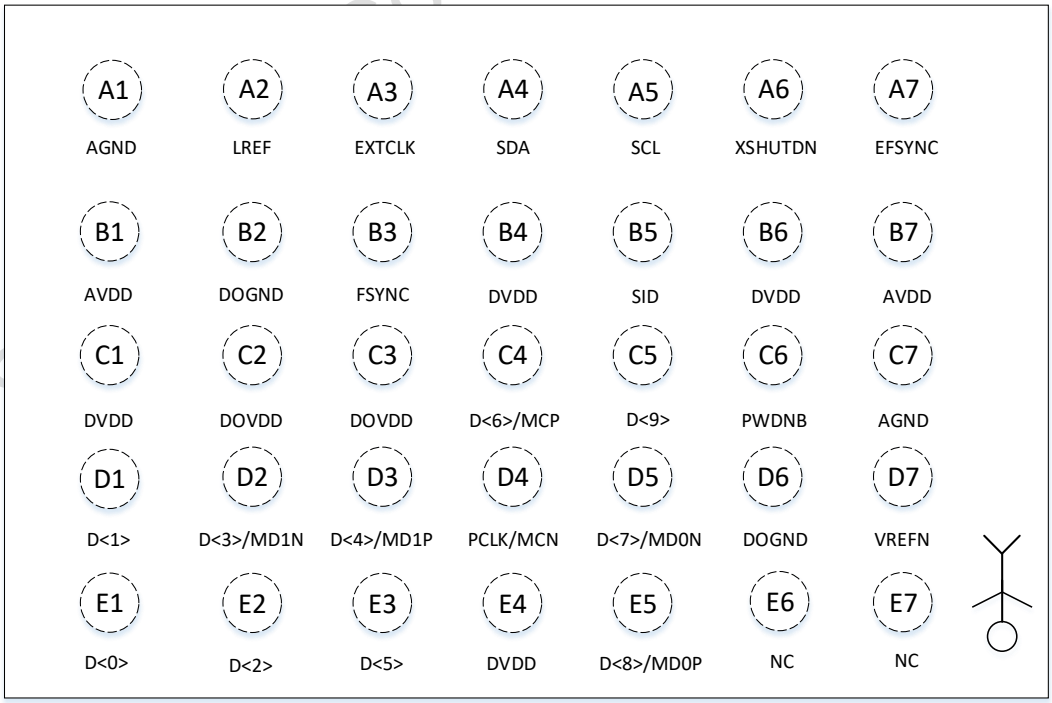

Figure 1-3 Top view of package pin assignment

1.4. Chip Initialization

1.4.1. Power-up Timing

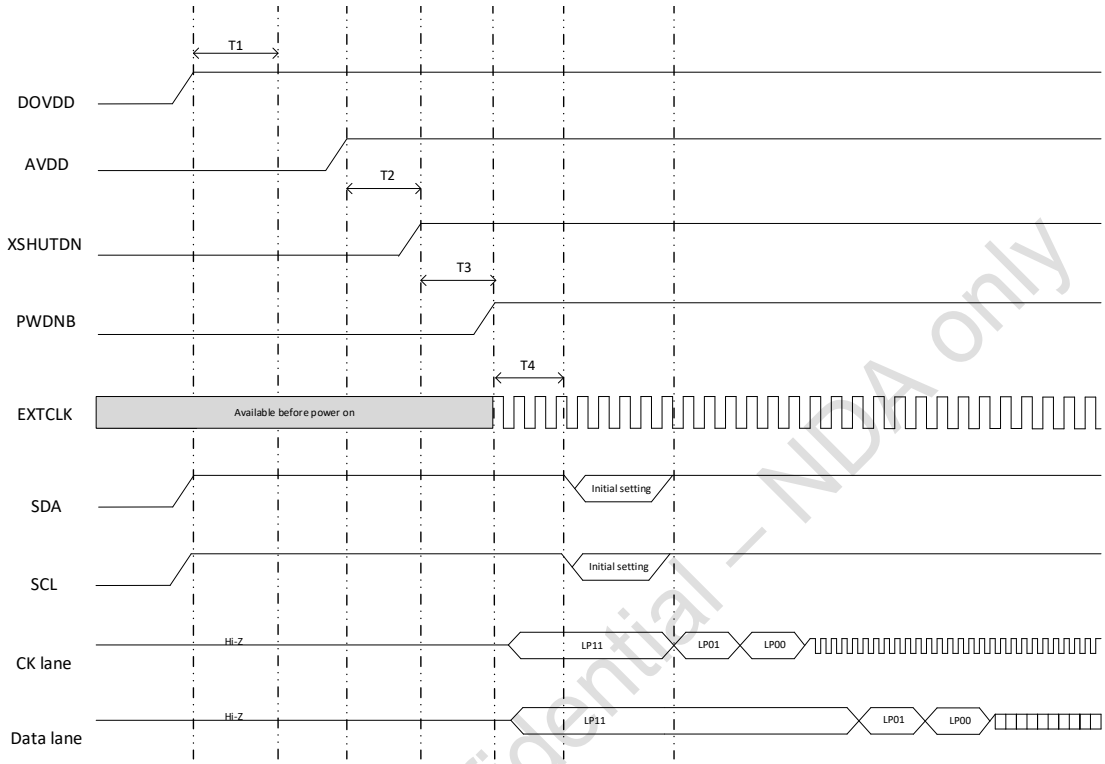

Figure 1-4 Power-up timing

Note: T1≥0ms, T2≥0ms, T3≥0ms, T4≥4ms.

1.4.2. Sleep Mode

Under sleep mode, this chip stops outputting data, works in a low power status, and keeps registers unchanged. This chip offers two approaches to enter sleep mode:

1. Pull the PWDNB pin low, I^{2}C read and write not supported.
2. Write register 16'h0100 [0] to 0, I^{2}C access remains active.

Table 1-2 Sleep mode control register

Function	Address	Default Value	Description
Sleep mode by the software approach	16'h0100	8'h0	Bit[0]: manual sleep mode control 1: sleep mode disable 0: sleep mode enable

1.4.3. Reset Mode

During reset, this chip stops outputting data, works in a low power status, and resets its registers to their default values. This chip offers two approaches to reset:

1. Hard reset: pull the XSHUTDN pin low, registers access through I²C is not supported.
2. Soft reset: write 1 to register 16'h0103[0], reset mode lasts for 150 ns.

Table 1-3 Soft reset control register

Function	Address	Default Value	Description
Soft reset	16'h0103	8'h0	Bit[0]: soft reset

1.5. Configuration Interface

Registers of this chip can be read and written via the standard I²C bus. The I²C bus device address of the I²C interface is 7'h30. The first line of Figure 1-5 shows a standard I²C communication protocol for 7-bit slave address, 16-bit sub address and 8-bit data. The slave address is the I²C bus device address, which is 7-bit. The R/W bit is either 1 for read or 0 for write. The 2 sub address bytes are the high byte and low byte of the 16-bit address of the register to be accessed. The second line of Figure 1-5 shows a write operation. The third line of Figure 1-5 shows a read operation. A dummy write operation is required to set the sub address (i.e. register address) before the read operation. Figure 1-6 shows the I²C timing diagram.

Standard I2C communication protocol:

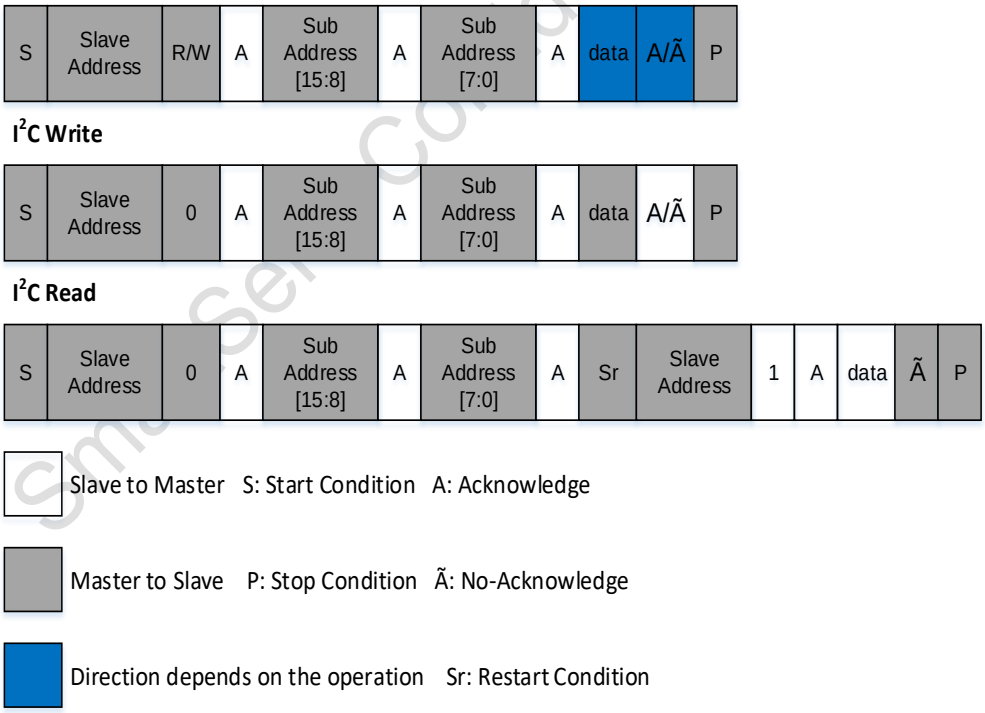

Figure 1-5 I²C standard protocol

I²C interface timing

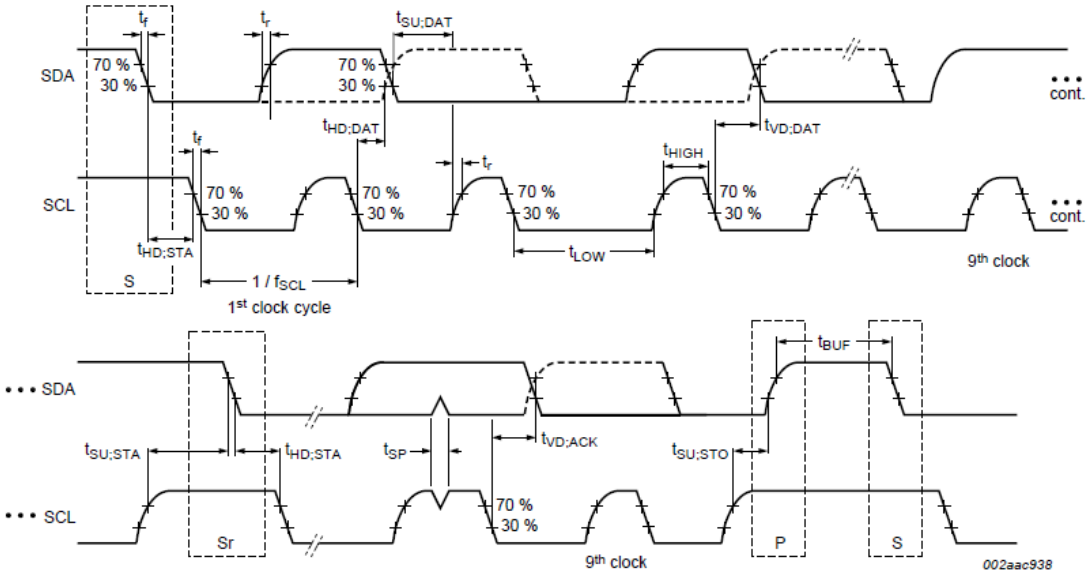

Figure 1-6 I²C interface timing

Table 1-4 I²C interface timing parameter

Symbol	Parameter	Standard-mode		Fast-mode		Unit
		Min	Max	Min	Max	
f_{SCL}	SCL clock frequency	0	100	0	400	kHz
$t_{HD;STA}$	hold time (repeated) START condition	4.0	-	0.6	-	μs
t_{LOW}	LOW period of the SCL clock	4.7	-	1.3	-	μs
t_{HIGH}	HIGH period of the SCL clock	4.0	-	0.6	-	μs
$t_{SU;STA}$	set-up time for a repeated START condition	4.7	-	0.6	-	μs
$t_{HD;DAT}$	data hold time	0	-	0	-	μs
$t_{SU;DAT}$	data set-up time	250	-	100	-	ns
t_r	rise time of both SDA and SCL signals	-	1000	20	300	ns
t_f	fall time of both SDA and SCL signals	-	300	20	300	ns
$t_{SU;STO}$	set-up time for STOP condition	4.0	-	0.6	-	μs
t_{BUF}	bus free time between a STOP and START condition	4.7	-	1.3	-	μs
$t_{VD;DAT}$	data valid time	-	3.45	-	0.9	μs
$t_{VD;ACK}$	data valid acknowledge time	-	3.45	-	0.9	μs
t_{SP}	pulse width of spikes that must be suppressed by the input filter	-	-	0	50	ns

Note: The beginning of a rising edge and the end of a falling edge are at 30% of the amplitude of the signal. The end of a rising edge and the beginning of a falling edge are at 70% of the amplitude of the signal.

1.6. Sensor ID

Table 1-5 Sensor ID control register

Function	Register	Default Value	Description
SENSOR ID high	16'h3107	8'hcb	SENSOR ID[15:8]
SENSOR ID low	16'h3108	8'h3a	SENSOR ID[7:0]

1.7. Data Interface

There are 2 types of data interfaces in this chip: the Digital Video Port (DVP) and the Mobile Industry Processor Interface (MIPI).

1.7.1. Digital Video Port (DVP)

This chip provides a Digital Video Port (DVP) that outputs 10-bit parallel data. A pulse signal indicating the start of data of a new frame is outputted from the FSYNC pin, line synchronization signals are outputted from the LREF pin, and the data clock signal is outputted from the PCLK pin. The period of the data clock signal equals to the period of the pixel clock T_{PCLK} (given by FAEs). Figure 1-7 shows the DVP timing diagram.

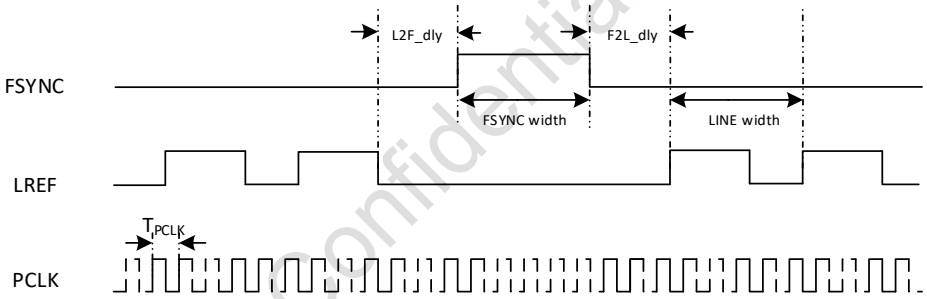

Figure 1-7 DVP timing diagram

Notes:

1) T_{PCLK} is the period of the PCLK signal.
2) L2F_dly is the delay between the falling edge of the last LREF signal and the rising edge of the FSYNC signal.
3) F2L_dly is the delay between the falling edge of the FSYNC signal and the rising edge of the first LREF signal.
4) Line width indicates the line width in the unit of number of T_{PCLK}, which is controlled by register {16'h320c, 16h'320d}.
5) FSYNC width is in the unit of number of lines. It equals to one line by default and is adjusted by register 16'h3d01.

Table 1-6 DVP timing control register

Function	Address	Default Value	Description
FSYNC output enable	16'h300a	8'h20	Bit[2]: FSYNC output en 1 ~ FSYNC as output PAD 0 ~ FSYNC as input PAD
FSYNC signal width	16'h3d01	8'h01	FSYNC length
DVP signal polarity	16'h3d08	8'h01	Bit[2]: LREF polarity Bit[1]: FSYNC polarity Bit[0]: PCLK polarity
PAD driving capability	16'h3641	8'h00	Bit[1:0]: adjust PAD driver capability
PCLK delay	16'h3640	8'h00	Bit[1:0]: PCLK DLY 2ns/step

1.7.2. Mobile Industry Processor Interface (MIPI)

This chip provides a Mobile Industry Processor Interface (MIPI) which supports 8/10-bit, 1/2lane data serial output with a speed of lower than 1.0 Gbps on each lane. Figure 1-8 shows the MIPI block diagram.

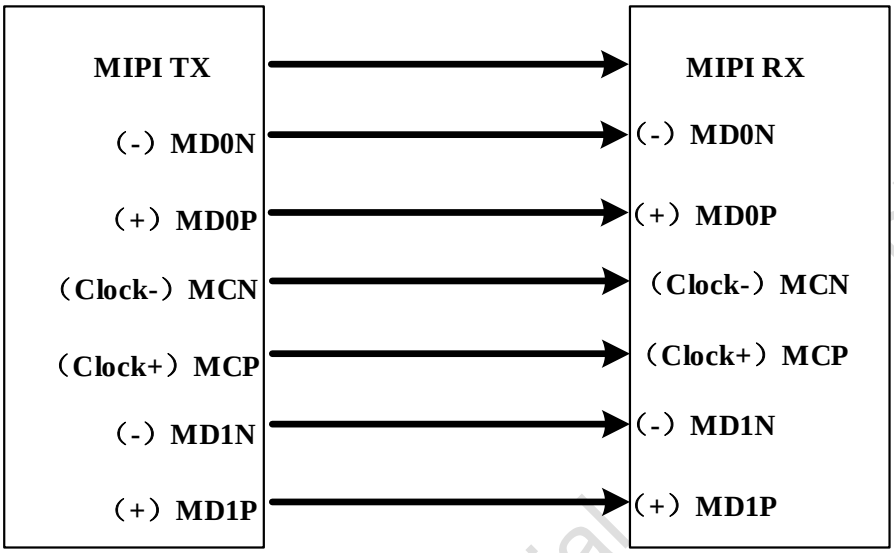

Figure 1-8 MIPI block diagram

Figure 1-9 is a brief diagram of an MIPI low level data packet, showing the transmission process of a short packet and a long packet. Figure 1-10 shows MIPI data packet structure diagrams for long and short packets. The Data Identifier (DI) is used to distinguish different packet types. Figure 1-11 shows the data packet transmission diagram of MIPI working in 1/2 lane. In Figure 1-12, DI consists of two parts, Virtual Channel (VC) and Data Type (DT). By default, the VC value of MIPI data given by this chip is 0, and the DT values are shown in Table 1-7.

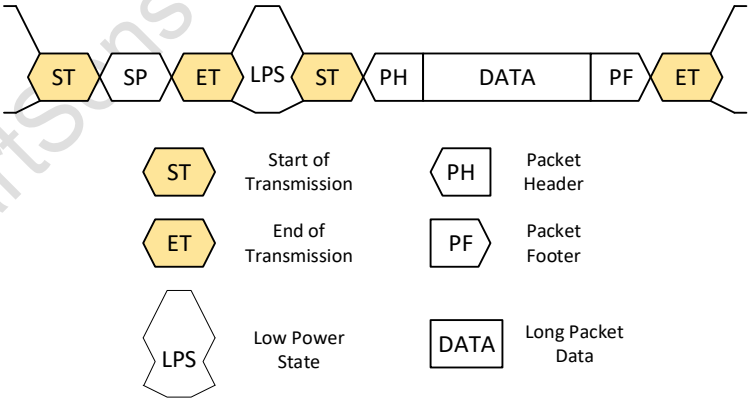

Figure 1-9 MIPI data packet

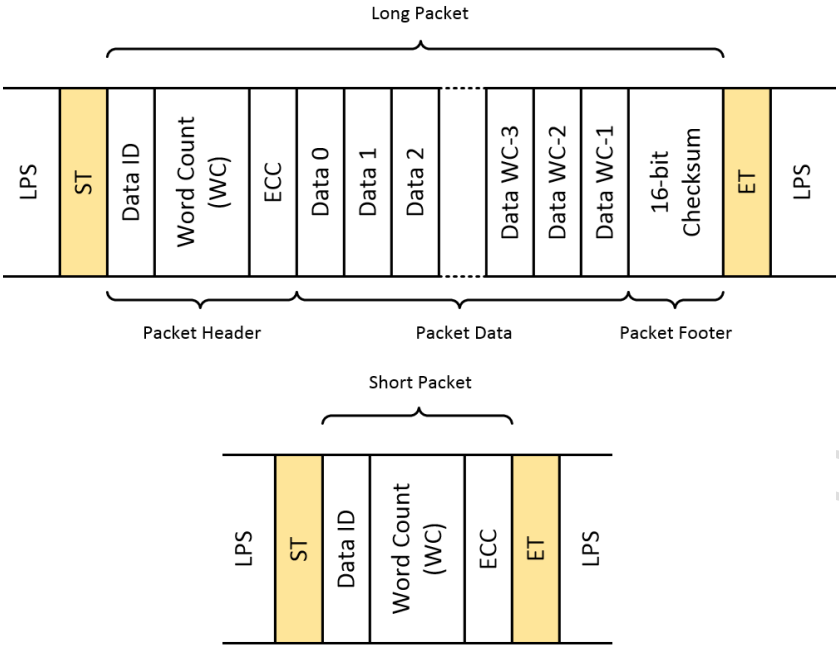

Figure 1-10 MIPI long/short packet structure diagram

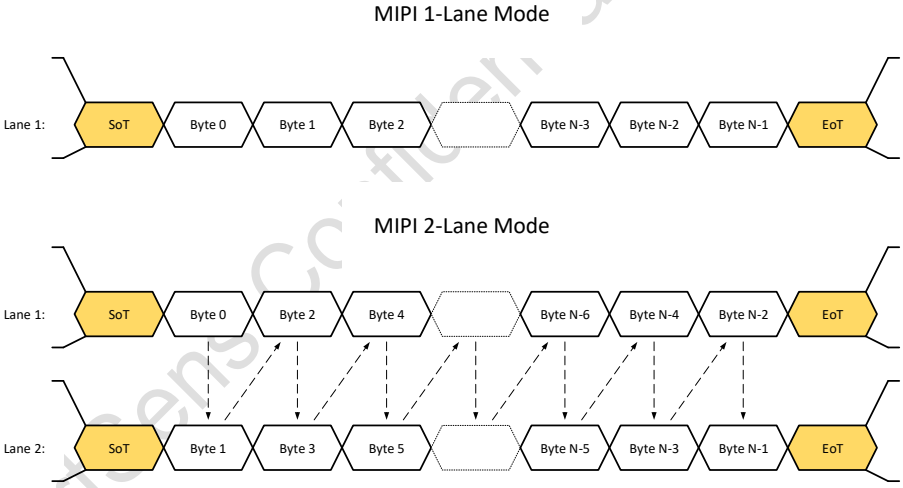

Figure 1-11 MIPI 1/2-lane data package transmission diagram

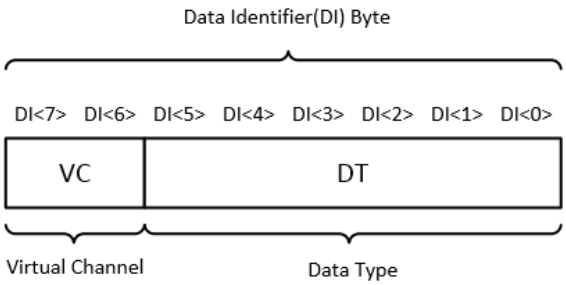

Figure 1-12 MIPI data packet DI structure

Table 1-7 MIPI data type

DT	Description
6'h00	Frame start short packet
6'h01	Frame end short packet
6'h02	Row start short packet
6'h03	Row end short packet
6'h2a	8-bit data long packet
6'h2b	10-bit data long packet

Table 1-8 MIPI control registers

Function	Address	Default Value	Description
MIPI lane number	16'h3018	8'h32	Bit[7:5]: MIPI lane num-1 3'h0 ~ 1 lane mode 3'h1 ~ 2 lane mode
MIPI output data mode	16'h3031	8'h0a	Bit[3:0]: MIPI bit mode 4'h8 ~ raw8 mode 4'ha ~ raw10 mode
PHY data mode	16'h3037	8'h20	Bit[6:5]: phy bit mode 2'h0 ~ 8bit mode 2'h1 ~ 10bit mode
MIPI clock setting	16'h303f	8'h01	Bit[7]: pclk sel 1'h0 ~ sel MIPI_pclk 1'b1 ~ sel DVP_pclk
MIPI data enabling	16'h4603	8'h00	Bit[0]: MIPI read 1'h1 ~ disable 1'h0 ~ enable
MIPI LP driving	16'h3651	8'h7d	Bit[2:1]: MIPI LP driving capability adjustment, the default value is 3'h1
MIPI Lane 0 delay	16'h3652	8'h00	Bit[3]: data lane0 invert, the default value is 1'h0 Bit[2:0]: data lane delay, 40 ps/step, the default value is 3'h0
MIPI Lane 1 delay	16'h3652	8'h00	Bit[7]: data lane1 invert, the default value is 1'h0 Bit[6:4]: data lane1 delay, 40 ps/step, the default value is 3'h0
MIPI Clock delay	16'h3654	8'h00	Bit[3]: clock lane invert, the default value is 1'h0 Bit[2:0]: clock delay, 40 ps/step, the default value is 3'h0

1.8. Phase Locked Loop (PLL)

The input clock frequency of the PLL module ranges from 6 MHz to 40 MHz, while the VCO output frequency (F_{VCO}) ranges from 400 MHz to 1200 MHz. The PLL block diagram is shown in Figure 1-13.

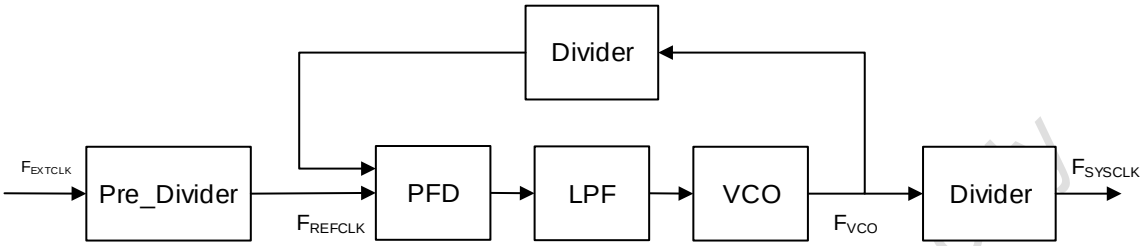

Figure 1-13 PLL control diagram

2. Function Introduction

2.1. Slave Mode

In the slave mode, data output of this chip is triggered by an external signal applied to the EFSYNC pin or FSYNC to achieve synchronization of multiple sensors. The frame rate is determined by the triggering signal. Figure 2-1 shows the timing diagram of the slave mode which consists of the following time intervals: Active State, RB Rows, Active Rows, Blank Rows, and Extra Delays. The exposure implementation in the slave mode is shown in Figure 2-2.

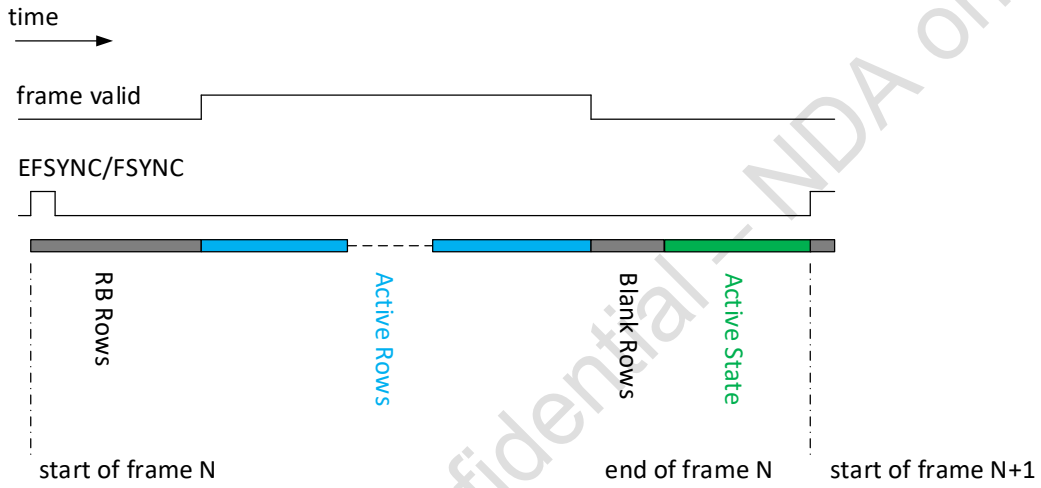

Figure 2-1 Slave mode timing diagram

From Figure 2-1, the slave mode workflow can be detailed as follows:

1) When the chip operates in the slave mode, the chip automatically enters Active State and waits for a trigger from the EFSYNC/FSYNC pin.
2) EFSYNC/FSYNC is active after triggering the rising edge, the duration of EFSYNC high level is not less than 4 EXTCLK cycles.
3) Upon triggering through EFSYNC/FSYNC, the chip enters RB Rows, which is the waiting time before the reading of valid data. The waiting time is controlled by registers. The value of the registers is in the unit of row.
4) During Active Rows, image data can be read. The value of the registers is in the unit of row.
5) During Blank Rows, blanking time after the image data can be read. The first and last rows to be read are controlled by registers. The value of the registers is in the unit of row.
6) During Active State, the chip waits for next triggering through the EFSYNC/FSYNC pin. The Active State should be as minimum as possible, which is proposed to be 0;
7) The rising edge interval of EFSYNC/FSYNC is one frame, and 40 ns deviation is allowed for EFSYNC/FSYNC rising edge interval.

Notes:

1) Triggering through the EFSYNC/FSYNC pin is valid only when the chip enters Active State.

2) The chip will withdraw from Blank Rows 40 ns in advance and enter into Active State

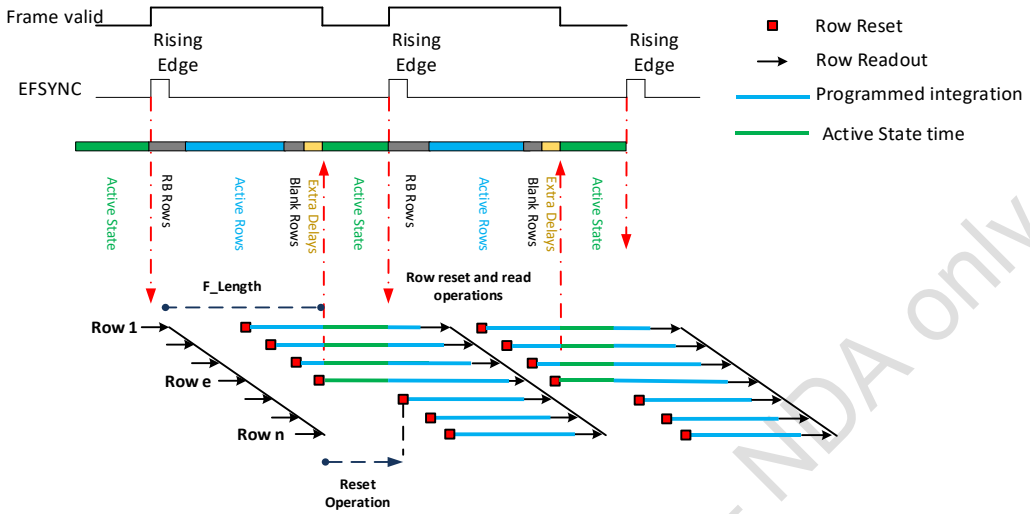

Figure 2-2 Slave mode exposure implementation chart

The exposure in the slave mode is shown in Figure 2-2.

Notes:

1) Row Reset starts exposure operation, ends exposure operation before Row Readout starts, including Active State time;

2) VTS represents frame length, VTS= RB Rows + Active Rows + Blank Rows;

3) During Active State, the chip stops output and stops the Row reset operation, as shown in Figure 2-2. This will result in exposure time being different in a frame image such that the exposure Row 1 to Row e and Row (e + 1) to Row n having different integration time, resulting in the top e rows exposure time being larger than the bottom of n-e rows. The time difference is Active State time as shown as Reset Operation time in the diagram. In order to avoid this exposure difference, the external high precision control EFSYNC/FSYNC is required to keep the Active State within 40ns, ensuring the exposure time of each row in one frame is basically consistent.

4) When RB Rows is greater than the exposure time, the inconsistencies in the in-frame exposure time in Note 3) do not occur, and the exposure time in each row in one frame is the same. At this time, the EFSYNC/FSYNC pin can achieve simultaneous exposure.

Table 2-1 Slave mode control register

Function	Register Address	Default Value	Description
Slave mode enable	16'h3222	8'h00	Bit[1]:Slave mode enable control 1~slave mode 0~master mode
Merge enable	16'h3225	8'h10	Bit[4]: Active Rows Blank Rows merge enable
Trigger Pad sel	16'h3224	8'h82	Bit[4]: trigger pad sel 1 ~ sel FSYNC 0 ~ sel EFSYNC
FSYNC OEN	16'h300a	8'h20	Bit[2]: FSYNC output en 1 ~ FSYNC as output PAD 0 ~ FSYNC as input PAD
RB rows	{16'h3230,16'h3231}	16'h0004	Rows Before Read control register

Function	Register Address	Default Value	Description
Active Rows, Blank Rows	{16'h322e,16'h322f}	16'h04de	Active Rows + Blank Rows = VTS – RB Rows
VTS	{16'h320e,16'h320f}	16'h0465	Frame length

2.2. AEC/AGC

The AEC/AGC adjustment is based on the brightness. AEC adjusts the exposure time while AGC adjusts the gain value so that the image's brightness can fall within the target range of a given brightness threshold.

2.2.1. AEC/AGC adjustment strategy

This chip does not have the AEC/AGC function, so a back-end platform is needed in order to achieve AEC/AGC.

During the AEC/AGC adjustment process, sensor exposure time or gain should not be adjusted independently. A recommended adjustment strategy is as follows: adjust the exposure time first, and then the gain if the exposure time has reached its maximum.

For example, when adjusting a dark scene, the sequence of adjustment is: 1) do not turn on any gain until the exposure time reaches its maximum; 2) when the exposure time reaches its maximum, automatic gain control can be adjusted. It is important to note that when the gain is applied, the average image noise also increases. But when the exposure time increases, the signal-to-noise ratio will improve.

On the other hand, when the image is too bright, the gain should be reduced first. If all gains are disabled and the image is still too bright, the exposure time can be reduced to properly expose the scene.

The exposure time and gain are interrelated. They should be considered at the same time during system adjustment.

2.2.2. AEC control registers

AEC control registers are listed in Table 2-2.

Table 2-2 Manual control registers

Function	Register Address	Description	Adjustment Step	Min.	Max.
Exposure time	{16'h3e00[3:0] 16'h3e01[7:0], 16'h3e02[7:4]}	Manual exposure time, in the unit of one line	1	1	{16'h320e, 16'h320f} – 'd4

For AEC control, please refer to the following instructions:

1) The adjustment step of AEC is calculated in the unit of one line, and the calculation method of one-line time is referred to Section 2.6;

2) If the exposure time and gain are written in the N^{th} frame, they are effective on the $(N+2)^{th}$ frame.

3) Writing point of exposure time and gain: writing is recommended after the start of the frame.

2.2.3. AGC control registers

AGC control registers are listed in Table 2-3.

Table 2-3 Gain control registers

ANA GAIN register	DIG GAIN register	DIG FINE GAIN register
16'h3e09	16'h3e06	16'h3e07

For AGC control, the register 16'h3e03[3:0] is set to 4'hb.

The values of the analog gain and the digital gain are shown in Table 2-4 and Table 2-5 respectively. In general, the analog gain should be increased first. If the brightness is required to be further increased when the analog gain is increased to the maximum, the digital gain can be increased. The accuracy of the DIG FINE gain of this chip is 1/32. The digital gain is listed in Table 2-5.

Because the analog gain only has coarse gain, and no fine gain, so in the adjustment of analog gain, DIG FINE GAIN (1 ~ 2 times) needs to replace analog fine gain for smooth transition, so as to avoid AGC oscillation.

Table 2-4 Analog gain control registers

ANA GAIN	GAIN Value	dB Value
8'h00	1.000	0.00
8'h08	2.000	6.02
8'h09	4.000	12.04
8'h0b	8.000	18.06
8'h0f	16.000	24.08
8'h1f	32.000	30.10

Table 2-5 Digital gain control registers

DIG GAIN	DIG FINE GAIN	GAIN Value	dB Value	DIG GAIN	DIG FINE GAIN	GAIN Value	dB Value
8'h00	8'h80	1.000	0.00	8'h01	8'h84	2.063	6.29
8'h00	8'h84	1.031	0.27	8'h01	8'h88	2.125	6.55
8'h00	8'h88	1.063	0.53	8'h01	8'h8c	2.188	6.80
8'h00	8'h8c	1.094	0.78	8'h01	8'h90	2.250	7.04
8'h00	8'h90	1.125	1.02	8'h01	8'h94	2.313	7.28
8'h00	8'h94	1.156	1.26	8'h01	8'h98	2.375	7.51
8'h00	8'h98	1.188	1.49	8'h01	8'h9c	2.438	7.74
8'h00	8'h9c	1.219	1.72	8'h01	8'ha0	2.500	7.96
8'h00	8'ha0	1.250	1.94	8'h01	8'ha4	2.563	8.17
8'h00	8'ha4	1.281	2.15	8'h01	8'ha8	2.625	8.38
8'h00	8'ha8	1.313	2.36	8'h01	8'hac	2.688	8.59
8'h00	8'hac	1.344	2.57	8'h01	8'hb0	2.750	8.79
8'h00	8'hb0	1.375	2.77	8'h01	8'hb4	2.813	8.98
8'h00	8'hb4	1.406	2.96	8'h01	8'hb8	2.875	9.17
8'h00	8'hb8	1.438	3.15	8'h01	8'hbc	2.938	9.36
8'h00	8'hbc	1.469	3.34	8'h01	8'hc0	3.000	9.54
8'h00	8'hc0	1.500	3.52	8'h01	8'hc4	3.063	9.72
8'h00	8'hc4	1.531	3.70	8'h01	8'hc8	3.125	9.90
8'h00	8'hc8	1.563	3.88	8'h01	8'hcc	3.188	10.07
8'h00	8'hcc	1.594	4.05	8'h01	8'hd0	3.250	10.24
8'h00	8'hd0	1.625	4.22	8'h01	8'hd4	3.313	10.40
8'h00	8'hd4	1.656	4.38	8'h01	8'hd8	3.375	10.57
8'h00	8'hd8	1.688	4.54	8'h01	8'hdc	3.438	10.72
8'h00	8'hdc	1.719	4.70	8'h01	8'he0	3.500	10.88
8'h00	8'he0	1.750	4.86	8'h01	8'he4	3.563	11.04
8'h00	8'he4	1.781	5.01	8'h01	8'he8	3.625	11.19
8'h00	8'he8	1.813	5.17	8'h01	8'hec	3.688	11.33
8'h00	8'hec	1.844	5.31	8'h01	8'hf0	3.750	11.48
8'h00	8'hf0	1.875	5.46	8'h01	8'hf4	3.813	11.62
8'h00	8'hf4	1.906	5.60	8'h01	8'hf8	3.875	11.77
8'h00	8'hf8	1.938	5.74	8'h01	8'hfc	3.938	11.90
8'h00	8'hfc	1.969	5.88	8'h03	8'h80	4.000	12.04
8'h01	8'h80	2.000	6.02				

2.3. Group Hold

Group hold refers to the packing of a group of registers to be effective at a specific time within a frame. In this chip, the maximum number of registers within the group is 10. Frame delay is supported and can be controlled by a register.

The procedure of packing a group is as follows. First, set register 16'h3812 to 8'h00 to start packing the group. Then write the required values to registers of the group. Finally set register 16'h3812 to 8'h30 to end packing the group. Registers in the group are effective with a delay of N frames when setting register 16'h3812 to 8'h30, where N is the value of register 16'h3802. N = 0 means the current frame. N = 1 means the next frame and so on.

Table 2-6 Group hold control registers

Function	Address	Default Value	Description
Frame delay control	16'h3802	8'h00	Bit [3:0]: Determine the number of frames to be delayed before the group of registers is effective. Setting to 0 implies the current frame. Setting to N implies a delay of N frames.

2.4. Defective Pixel Correction (DPC)

This chip supports the Defective Pixel Correction (DPC) feature. A pixel is regarded as defective if the value of the pixel is greater (or smaller) than its surrounding pixels with the same color, and the difference is greater than the set threshold. A defective pixel may be classified as a white pixel or a black pixel. The corresponding control registers are shown in Table 2-7.

Table 2-7 DPC registers

Function	Address	Default Value	Description
White pixel correction	16'5000[2]	1'b1	white pixel cancellation enable 1 ~ enable 0 ~ disable
Black pixel correction	16'5000[1]	1'b1	black pixel cancellation enable 1 ~ enable 0 ~ disable

2.5. Video output Mode

2.5.1. Read Order

Below figure shows the location of the first read pixel as well as the entire array structure. This figure shows the top view when the A1 pin is placed in the upper left corner. Figure 2-4 shows the first pixel data color format.

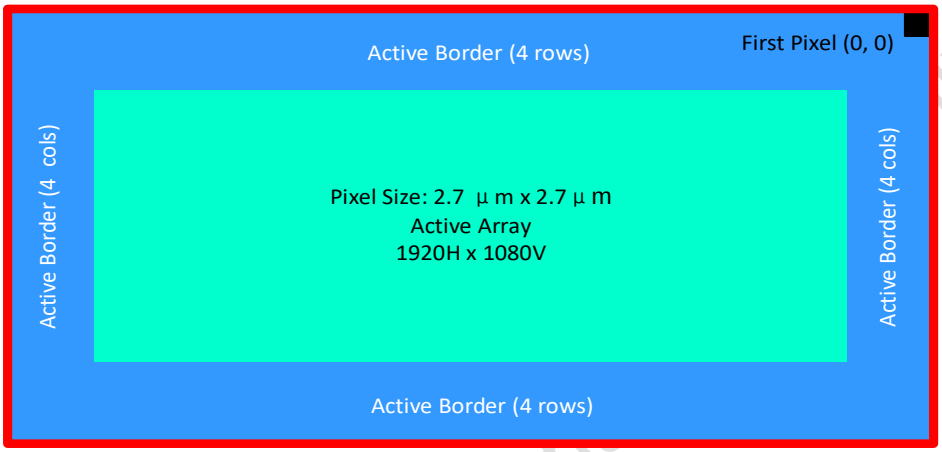

Figure 2-3 Pixel array 1

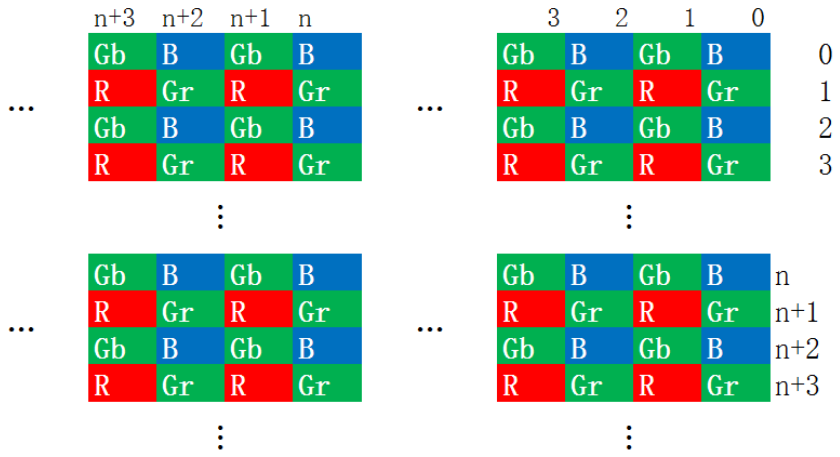

Figure 2-4 Pixel array 2

This chip supports the mirror mode and the flip mode. The mirror mode reverses the sensor data read out order, and the flip mode vertically reverses the sensor readout order, as shown in Figure 2-5.

Figure 2-5 Mirror/flip example

Table 2-8 Mirror and flip control registers

Function	Address	Default Value	Description
Mirror	16'h3221	8'h00	Bit[2:1]: mirror ctrl
			2'b00 ~ mirror off
			2'b11 ~ mirror on
Flip	16'h3221	8'h00	Bit[6:5]: flip ctrl
			2'b00 ~ flip off
			2'b11 ~ flip on

2.5.2. Output Window

Table 2-9 Output window registers

Function	Address	Default Value	Description
Window width	{16'h3208, 16'h3209}	16'h0780	Output window width
Window height	{16'h320a, 16'h320b}	16'h0438	Output window height
Column start	{16'h3210, 16'h3211}	16'h0004	Output window column start
Row start	{16'h3212, 16'h3213}	16'h0004	Output window row start

2.6. Frame Rate Calculator

The frame rate of this chip is provided by FAEs. For simplicity, the duration of one row can be calculated as 1 ÷ (frame rate × frame length).

Table 2-10 Frame rate related registers

Function	Address	Default Value	Description
Frame length	{16'h320e[7:0],16'h320f}	16'h0465	Frame length={16'h320e[7:0],16'h320f}

2.7. Test Mode

For the ease of testing, this chip provides an incremental test mode as shown in Figure 2-6.

Figure 2-6 Test mode

Table 2-11 Test mode control registers

Function	Address	Register value	Default Value	Description
Grey ramp mode	16'h4501	8'hac	8'hc4	Bit[3]: incremental pattern enable 0 ~ normal image 1 ~ incremental pattern

3. Electrical Characteristics

Table 3-1 Absolute maximum ratings (to pad)

Item	Symbol	Absolute Maximum Ratings	Unit
Analog supply voltage	V_{AVDD}	-0.3~3.4	V
I/O supply voltage	V_{DOVDD}	-0.3~2.2	V
I/O input voltage	V_I	-0.3 ~ V_{DOVDD} +0.3	V
I/O output voltage	V_O	-0.3 ~ V_{DOVDD} +0.3	V
Operating temperature	T_{OPR}	-30~+85	℃
Functional temperature	T_{SPEC}	-20~+60	℃
Storage temperature	T_{STG}	-40~+85	℃

Table 3-2 DC electrical characteristics (to pad)

Item	Symbol	Min	Typical	Max	Units
Power Supply					
Analog supply voltage	V_{AVDD}	2.7	2.8	2.9	V
I/O supply voltage	V_{DOVDD}	1.7	1.8	1.9	V
Supply Current (Operating current: linear mode, 30fps, MIPI 2-lane output)					
Analog supply current	I_{AVDD}	-	26.3	-	mA
I/O supply current	I_{DOVDD}	-	37.4	-	mA
Total power consumption	Power (*)	-	140.96	-	mW
Digital Input					
Input low level	V_{IL}	-	-	0.3 × DOVDD	V
Input high level	V_{IH}	0.7 × DOVDD	-	-	V
Input capacitor	C_{IN}	-	-	10	pF
Digital Output (25 pF standard load)					
Output high level	V_{OH}	0.9 × DOVDD	-	-	V
Output low level	V_{OL}	-	-	0.1 × DOVDD	V
Serial Interface Input (SCL and SDA)					
Input low level	V_{IL}	- 0.5	0	0.3 × DOVDD	V
Input high level	V_{IH}	0.7 × DOVDD	DOVDD	DOVDD + 0.5	V

Note: Operating current: (Typ.) Supply voltage 2.8V/1.8V, T_j=25℃;

The light condition: luminous intensity when the sensor outputs 1/3 of the maximum output.

Table 3-3 AC characteristics (TA = 25°C, AVDD = 2.8V, DOVDD = 1.8V)

Item	Symbol	Min	Typical	Max	Unit
AC Parameters					
DC differential linearity deviation	DLE	-	< 1	-	LSB
DC integral linearity deviation	ILE	-	< 2	-	LSB
Crystal and Clock Input					
Input clock frequency	f_{EXTCLK}	6	-	40	MHz
Input clock high pulse width	t_{WH}	5	-	-	ns
Input clock low pulse width	t_{WL}	5	-	-	ns
Input clock duty cycle	-	45	50	55	%

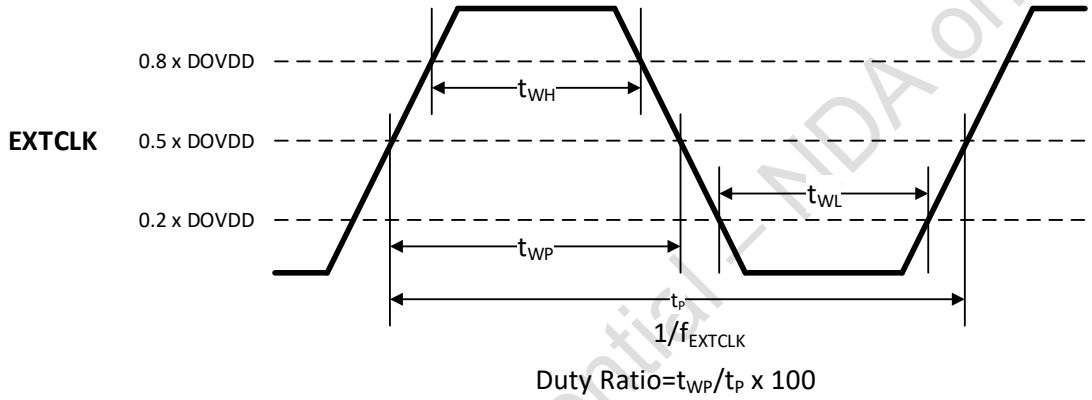

Figure 3-1 Input clock waveform

4. Optical Characteristic

4.1. QE Curve

SC2336 QE curve is shown in Figure 4-1.

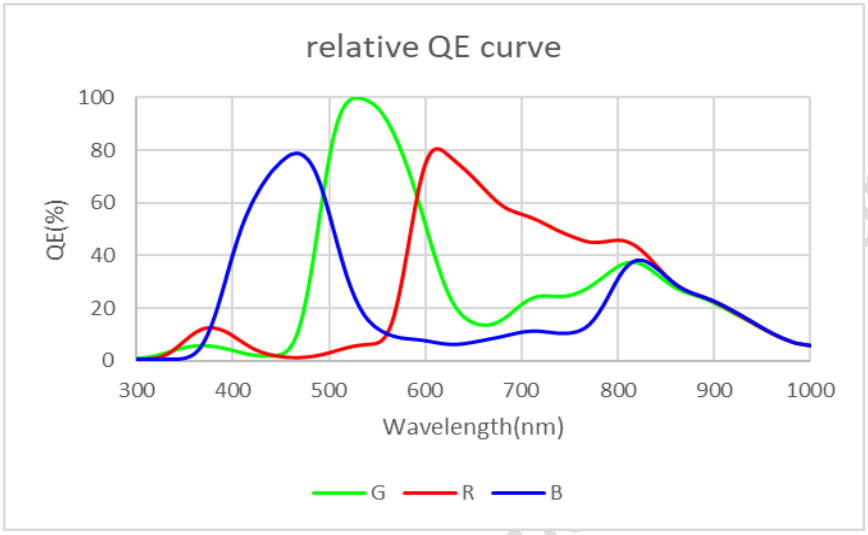

Figure 4-1 QE curve

4.2. Chief Ray Angle (CRA)

SC2336 CRA curve is shown in Figure 4-2.

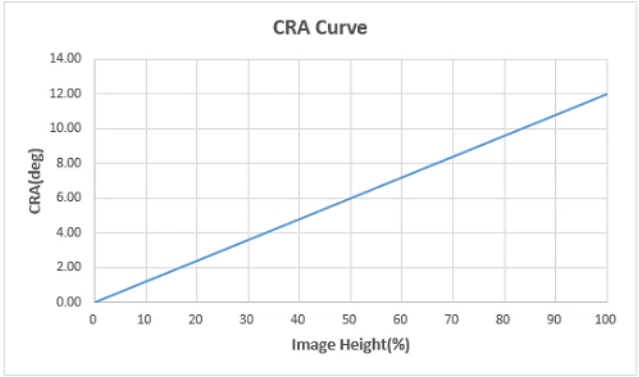

Image Height		CRA
%	mm	deg.
0	0.000	0.00
10	0.292	1.20
20	0.584	2.40
30	0.876	3.60
40	1.168	4.80
50	1.459	6.00
60	1.751	7.20
70	2.043	8.40
80	2.335	9.60
90	2.627	10.80
100	2.919	12.00

Figure 4-2 CRA curve

5. Packaging Information

SC2336 provides a 41-pin CSP package. The package drawing is shown in Figure 5-1.

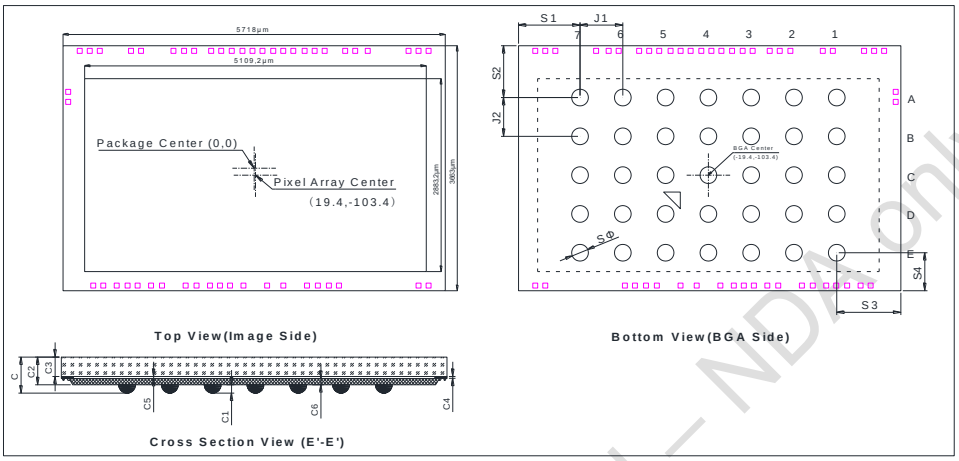

Figure 5-1 Package drawing

Note: Package Center (Chip Center) is not coincident with Array Center (Optical Center), BGA Center is coincident with Optical Center. Taking Chip Center as the origin, the BGA Center / Optical Center is (19.4, - 103.4), the unit is μm.

Table 5-1 Package dimensions

Parameter	Symbol	Nominal	Min	Max	Nominal	Min	Max
		Millimeters			Inches		
Package Body Dimension X	A	5.7180	5.6930	5.7430	0.22512	0.22413	0.22610
Package Body Dimension Y	B	3.6630	3.6380	3.6880	0.14421	0.14323	0.14520
Package Height	C	0.6650	0.6100	0.7200	0.02618	0.02402	0.02835
Cavity wall height	C4	0.0410	0.0370	0.0450	0.00161	0.00146	0.00177
Cavity wall + epoxy thickness (glass to the wafer bonding top point)	C5	0.0435	0.0385	0.0485	0.00171	0.00152	0.00191
Si Thickness	C6	0.1500	0.1400	0.1600	0.00591	0.00551	0.00630
Glass Thickness	C3	0.3000	0.2900	0.3100	0.01181	0.01142	0.01220
Package Body Thickness	C2	0.5350	0.5000	0.5700	0.02106	0.01969	0.02244
Ball Height	C1	0.1300	0.1000	0.1600	0.00512	0.00394	0.00630
Ball Diameter	SΦ	0.2500	0.2200	0.2800	0.00984	0.00866	0.01102
Total Ball Count	N	34	-	-	-	-	-
Ball Count X axis	N1	7	-	-	-	-	-
Ball Count Y axis	N2	5	-	-	-	-	-
Pins Pitch X axis1	J1	0.6400	0.6300	0.6500	0.0252	0.02480	0.02559
Pins Pitch X axis2	J2	0.5800	0.5700	0.5900	0.02283	0.02244	0.02323
BGA ball center to package center offset in X-direction	X	0.0194	-0.0056	0.0444	0.00076	-0.00022	0.00175
BGA ball center to package center offset in Y-direction	Y	0.1034	0.0784	0.1284	0.00407	0.00309	0.00506
Edge to Ball Center Distance	S1	0.91960	0.88960	0.94960	0.03620	0.03502	0.03739

Parameter	Symbol	Nominal	Min	Max	Nominal	Min	Max
		Millimeters			Inches		
along X							
Edge to Ball Center Distance along Y	S2	0.77490	0.74490	0.80490	0.03051	0.02933	0.03169
Edge to Ball Center Distance along X2	S3	0.95840	0.92840	0.98840	0.03773	0.03655	0.03891
Edge to Ball Center Distance along Y2	S4	0.56810	0.53810	0.59810	0.02237	0.02119	0.02355

6. Order Information

Table 6-1 Order information

Product code	Package	Description
SC2336-CSBNN00	35-pin CSP	2.0 Megapixel, RAW/RGB, DVP/MIPI output
SC2336-CSBNF00	35-pin CSP	2.0 Megapixel, RAW/RGB, DVP/MIPI output

7. Revision History

Version	Description	Owner and date
0.2	Initial version	Vicky Song/2021.6.29
0.5	• Section 2.2.3: Table 2-4: updated Ana gain register • Updated pixel size • Section 2.2.2: Table 2-2: updated min. exposure value	Vicky Song/2021.8.20
0.6	Chapter 3: Table 3-2: updated operating current typical value	Vicky Song/2021.8.30
0.7	Chapter 6: added a new order number: SC2336-CSBNF00	Vicky Song/2021.9.13

Contact us:

Headquarters:

Address: 11/F, Chuang Xin Building, No. 1009 Yishan Road, Shanghai, China.

Tel: 021-64853570

Fax: 021-64853572-8004

E-mail: sales@smartsenstech.com

Website: http://www.smartsenstech.com

American Branch:

Address: 4340 Stevens Creek Blvd. Suite 280, San Jose, CA 95129.

Tel: +1(408)981-6626

Shenzhen Branch:

Address: B2908B, Building B, Galaxy WORLD, No. 1 Yabao Road, Bantian Street, Longgang District, Shenzhen, China.

Tel: 0755-23739713

SmartSens Technical Support E-mail:

support@smartsenstech.com