1/5” UXGA CMOS Image Sensor

GC2235

DataSheet

V1.1

2013-07-15

GalaxyCore Inc.

Content

1. Sensor Overview

1.1 General Description

GC2235 is a high quality 2Mega CMOS image sensor, for mobile phone camera applications and digital camera products. GC2235 incorporates a 1616V x 1232H pixel array, on-chip 10-bit ADC, and image signal processor.

The full scale integration of high-performance and low-power functions makes the GC2235 best fit the design, reduce implementation process, and extend the battery life of cell phones, PDAs, and a wide variety of mobile applications.

It provides RAW10 and RAW8 data formats with MIPI interface. It has a commonly used two-wire serial interface for host to control the operation of the whole sensor.

1.2 Features

- Standard optical format of 1/5 inch
- BSI process
- Output formats: Raw Bayer 10bit/8bit
- Power supply requirement: AVDD28: 2.7~3.0V
  DVDD18: 1.7~1.9V
  IOVDD: 1.7~3.0V
- PLL support
- Windowing support
- MIPI interface support
- Horizontal/Vertical mirror
- Image processing module
- Package: CSP/wafer

1.3 Application

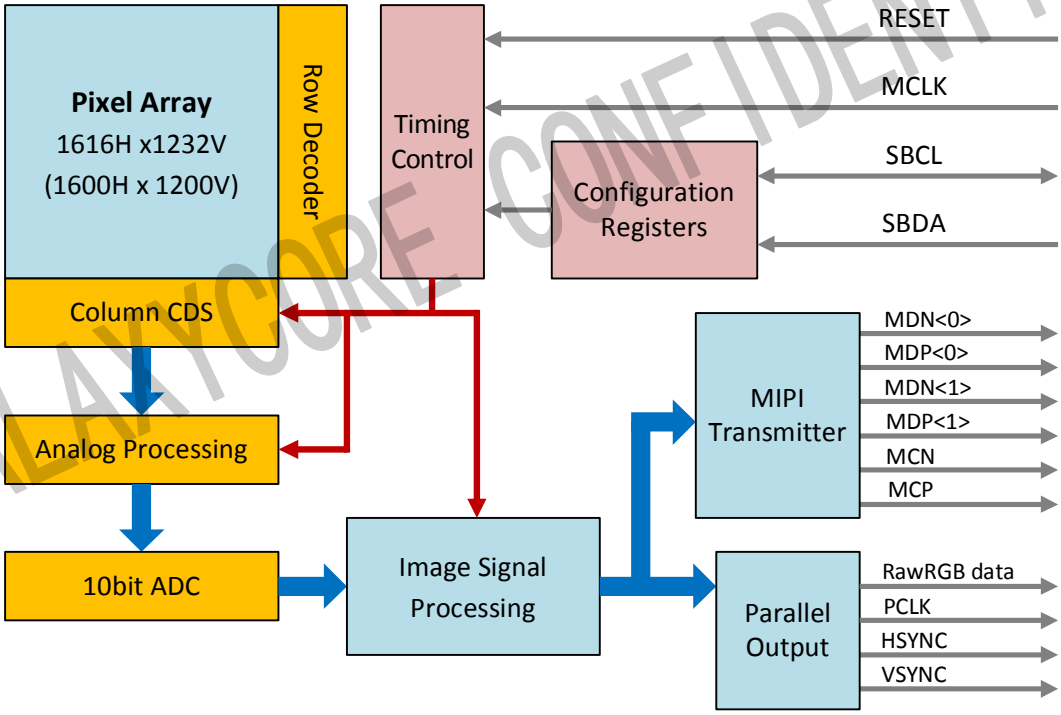
- Cellular Phone Cameras
- Notebook and desktop PC cameras
- PDAs
- Toys
- Digital still cameras and camcorders
- Video telephony and conferencing equipments
- Security systems
- Industrial and environmental systems

1.4 Technical Specifications

Parameter	Typical value
Optical Format	1/5 inch
Pixel Size	1.75um x 1.75um(BSI)
Active pixel array	1616 x 1232
ADC resolution	10 bit ADC
Max Frame rate	Full resolution@30fps
Power Supply	AVDD28: 2.7~3.0V DVDD18: 1.7~1.9V IOVDD: 1.7~3.0V
Power Consumption	140mW(Active) <100uA(Standby)
SNR	37.4 dB
Dark Current	60 e-/sec@60℃
Sensitivity	6700 e-/lux • sec
Operating temperature:	-20~70℃
Stable Image temperature	0~50℃
Optimal lens chief ray angle(CRA)	25° (non-linear)
Package type	CSP/wafer

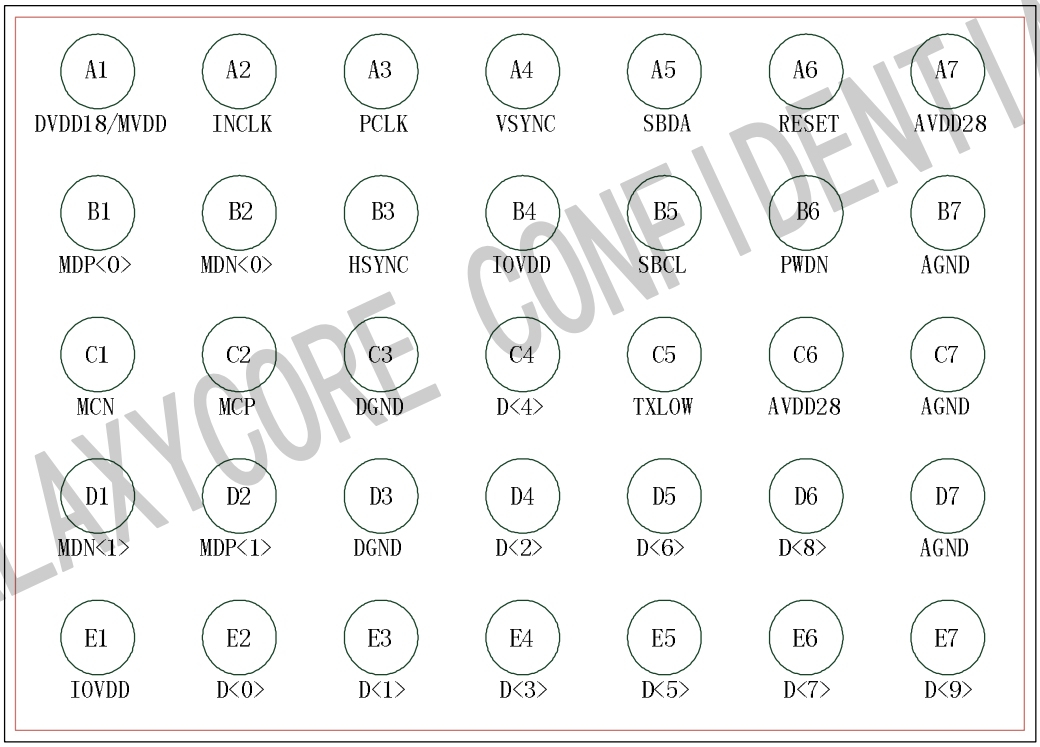
2. Block Diagram

2.1 Block Diagram



GC2235 has an active image array of 1616x1232 pixels. The active pixels are read out progressively through column/row driver circuits. In order to reduce fixed pattern noise, CDS circuits are adopted. The analog signal is transferred to digital signal by 10 bit A/D converter. The digital signals are processed in the ISP Block. Users can easily control these functions via two-wire serial interface bus.

2.2 Pin Diagram



Top View

2.3 Signal Descriptions

Pin	Name	Pin Type	Function
A1	**DVDD18/MVDD**	Power	Digital (MIPI) power supply pin: 1.7~1.9V, please connect 0.1μF or 1μF capacity to ground.
A2	**INCLK**	Input	Main clock
A3	**PCLK**	Output	Pixel clock output
A4	**VSYNC**	Output	VSYNC output
A5	**SBDA**	I/O	Two-wire serial bus, data
A6	**RESET**	Input	Chip reset control: 0: chip reset 1: normal work
A7	**AVDD28**	Power	Main power supply pin: 2.7~3.0V, Please connect 0.1μF or 1μF capacity to ground.
B1	**MDP<0>**	Output	MIPI data<0> (+)
B2	**MDN<0>**	Output	MIPI data<0> (-)
B3	**HSYNC**	Output	HSYNC output

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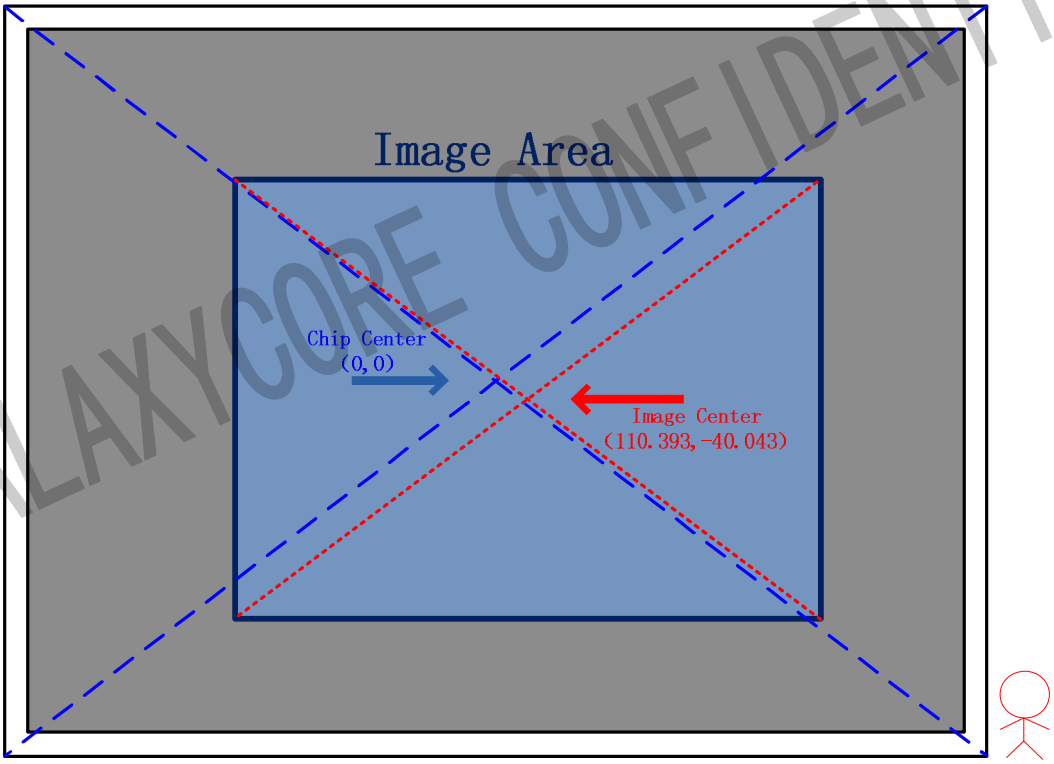
B4	**IOVDD**	Power	Power supply for I/O circuits: 1.7~3.0V, Please connect 0.1μF or 1μF capacity to ground.
B5	**SBCL**	Input	Two-wire serial bus, clock
B6	**PWDN**	Input	Sensor power down control: 0: normal work 1: standby
B7	**AGND**	Ground	AGND
C1	**MCN**	Output	MIPI clock (-)
C2	**MCP**	Output	MIPI clock (+)
C3	**DGND**	Ground	DGND
C4	**D<4>**	Output	Raw RGB data output bit[4]
C5	**TXLOW**	Power	Internal power supply, please connect 0.1μF or 1μF capacity to ground.
C6	**AVDD28**	Power	Main power supply pin: 2.7~3.0V, Please connect 0.1μF or 1μF capacity to ground.
C7	**AGND**	Ground	AGND
D1	**MDN<1>**	Output	MIPI data<1> (-)
D2	**MDP<1>**	Output	MIPI data<1> (+)
D3	**DGND**	Ground	DGND
D4	**D<2>**	Output	Raw RGB data output bit[2]
D5	**D<6>**	Output	Raw RGB data output bit[6]
D6	**D<8>**	Output	Raw RGB data output bit[8]
D7	**AGND**	Ground	AGND
E1	**IOVDD**	Power	Power supply for I/O circuits: 1.7~3.0V, Please connect 0.1μF or 1μF capacity to ground.
E2	**D<0>**	Output	Raw RGB data output bit[0]
E3	**D<1>**	Output	Raw RGB data output bit[1]
E4	**D<3>**	Output	Raw RGB data output bit[3]
E5	**D<5>**	Output	Raw RGB data output bit[5]
E6	**D<7>**	Output	Raw RGB data output bit[7]
E7	**D<9>**	Output	Raw RGB data output bit[9]

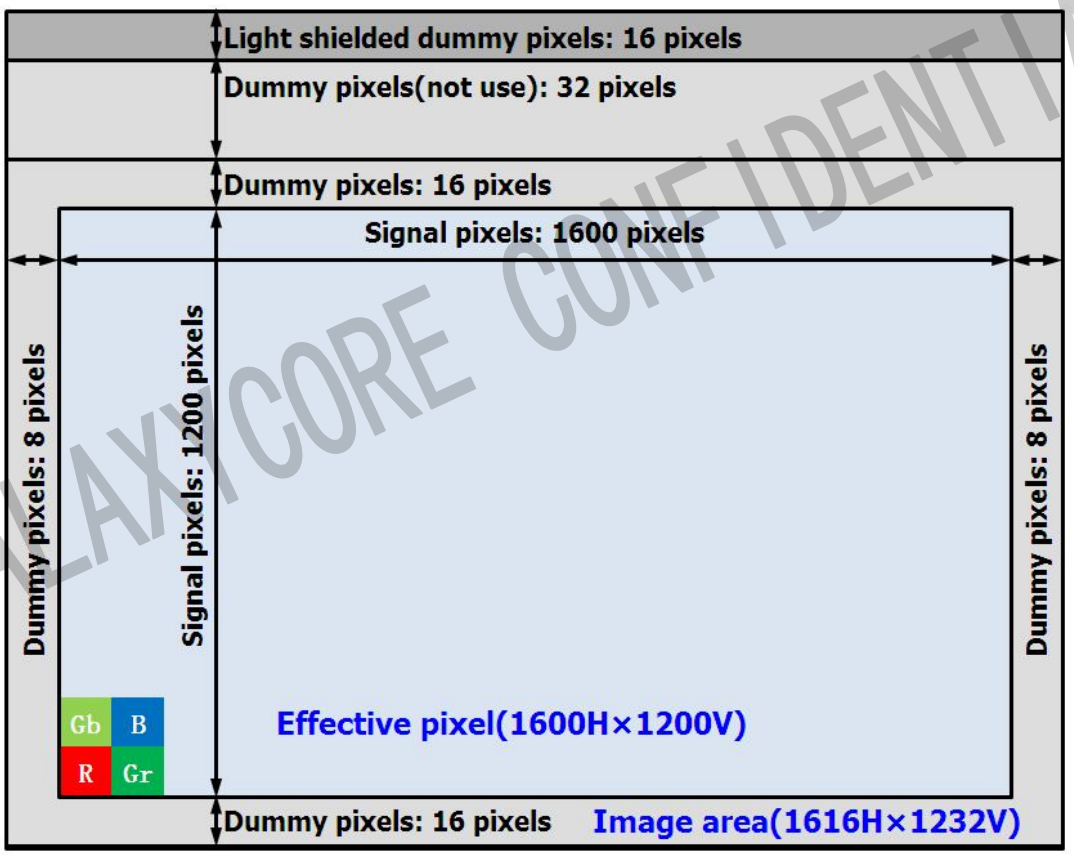
- **10-bit output (RAW): D<9>~D<0>.**
- **8-bit output (RAW): D<9>~D<2>.**

3. Optical Specifications

3.1 Sensor Array Center



3.2 Pixel Array



Pixel array is covered by Bayer pattern color filters. The primary color BG/GR array is arranged in line-alternating way.

If no flip in column, column is read out from 0 to 1615. If flip in column, column is read out from 1615 to 0.

If no flip in row, row is read out from 0 to 1231.If flip in row, row is read out from 1231 to 0.

3.3 Lens Chief Ray Angle (CRA)

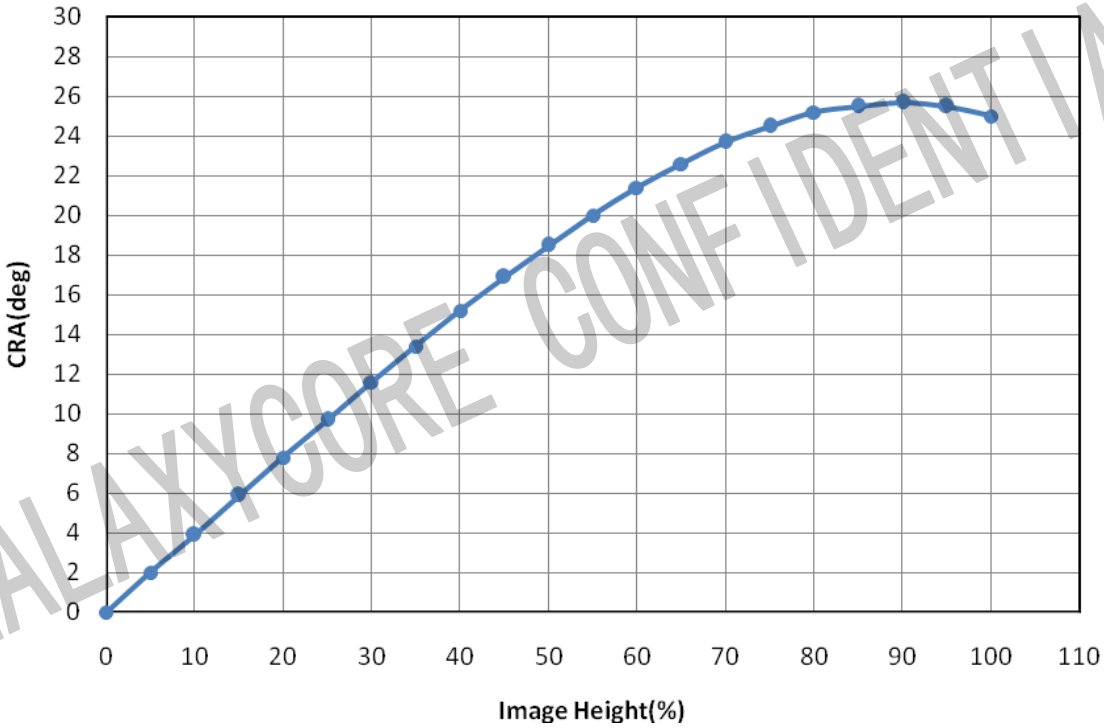
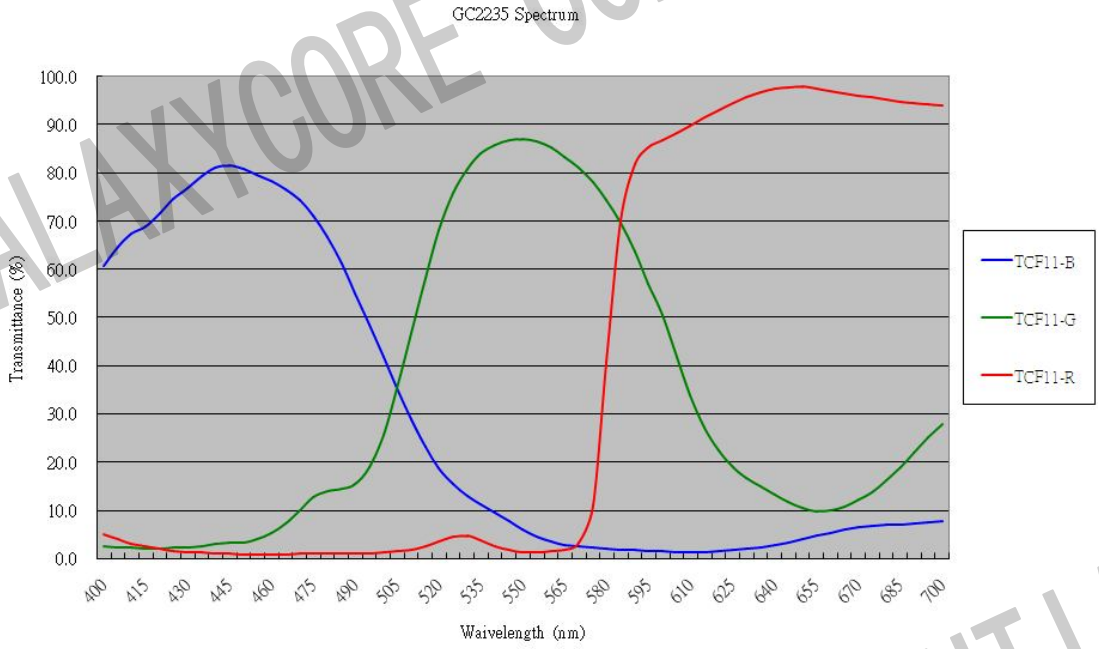


Image Height		CRA
（%）	（mm）	(deg)
0	0.000	0.0
5	0.087	2.0
10	0.175	3.9
15	0.263	5.9
20	0.350	7.8
25	0.438	9.7
30	0.525	11.6
35	0.613	13.4
40	0.700	15.2
45	0.787	16.9
50	0.875	18.5
55	0.963	20.0
60	1.050	21.4
65	1.138	22.6
70	1.225	23.7
75	1.313	24.5
80	1.400	25.2
85	1.488	25.5

90	1.575	25.7
95	1.663	25.5
100	1.750	25.0

3.4 Color Filter Spectral Characteristics

The optical spectrum of color filters is shown below



4. Two-wire Serial Bus Communication

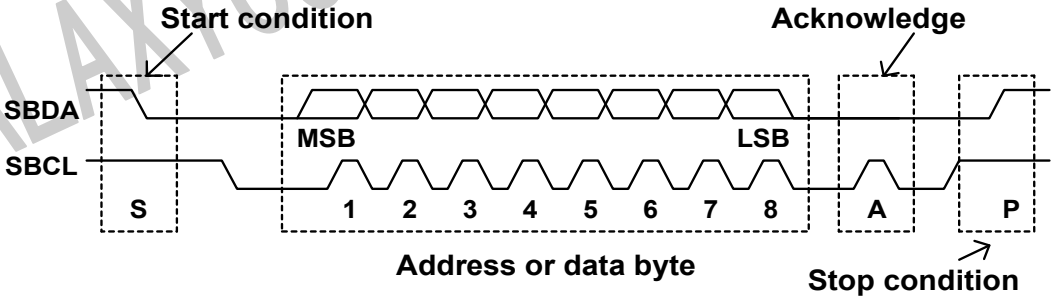
GC2235 Device Address:

serial bus write address = 0x78, serial bus read address = 0x79

4.1 Protocol

The host must perform the role of a communications master and GC2235 acts as either a slave receiver or transmitter. The master must do

- Generate the **Start(S)/Stop(P)** condition
- Provide the serial clock on **SBCL**.



Single Register Writing:

S	78H	A	Register Address	A	Data	A	P

Incremental Register Writing:

S	78H	A	Register Address	A	Data(1)	A	.....	Data(N)	A	P

Single Register Reading:

S	79H	A	Register Address	A	S	79H	A	Data	NA	P

Notes:

From master to slave From slave to master

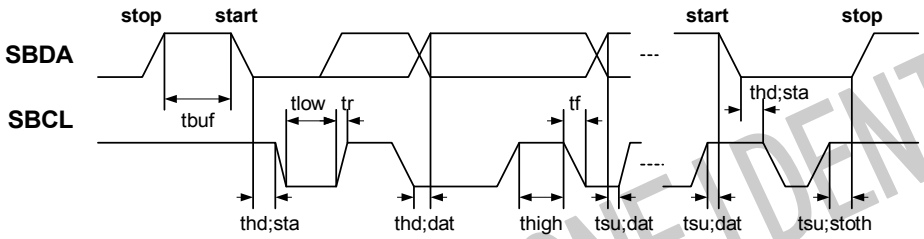
S: Start condition **P:** Stop condition

A: Acknowledge bit **NA:** No acknowledge

Register Address: Sensor register address

Data: Sensor register value

4.2 Serial Bus Timing

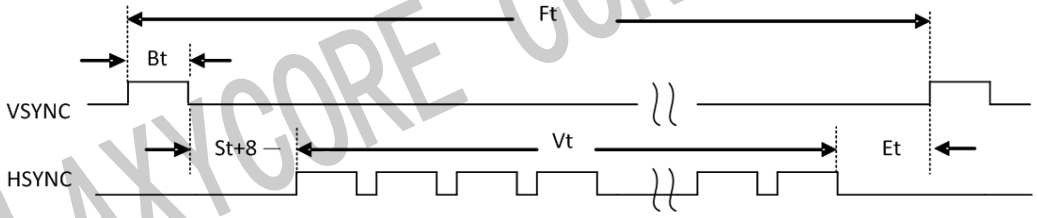


Parameter	Symbol	Min.	Max.	Unit
SBCL clock frequency	fscl	0	400	KHz
Bus free time between a stop and a start	tbuf	1.2	*	μs
Hold time for a repeated start	thd;sta	1.0	*	μs
LOW period of SBCL	tlow	1.2	*	μs
HIGH period of SBCL	thigh	1.0	*	μs
Set-up time for a repeated start	tsu;sta	1.2	*	ns
Data hold time	thd;dat	1.3	*	ns
Data Set-up time	tsu;dat	250	*	ns
Rise time of SBCL, SBDA	tr	*	250	ns
Fall time of SBCL, SBDA	tf	*	300	ns
Set-up time for a stop	tsu;sto	1.2	*	μs
Capacitive load of bus line (SBCL, SBDA)	Cb	*	*	pf

5. Applications

5.1 DVP Timing

Suppose Vsync is low active and Hsync is high active, and output format is RAW Bayer 10bit/8bit, then the timing of Vsync and Hsync is bellowing (take capture mode for example, preview mode is the same):



Ft =VB+ Vt +8 (unit is row_time)

VB = Bt + St + Et, Vblank/Dummy line, setting by register P0:0x07 and P0:0x08.

Ft -> Frame time, one frame time.

Bt -> Blank time, Vsync no active time.

St -> Start time, setting by register P0:0x13.

Et –> End time, setting by register P0:0x14.

Vt -> valid line time. UXGA is 1200, Vt = win_height-32, win_height is setting by register P0:0x0d and P0:0x0e.

When exp_time ≤ win_height + VB, Bt = VB – St - Et. Frame rate is controlled by window_height + VB.

When exp_time > win_height + VB, Bt = exp_time - win_height – St - Et. Frame rate is controlled by exp_time.

The following is row_time calculate:

row_time = (Hb + Sh_delay + win_width /2+ 4)/HPCLK.

Hb –> HBlank or dummy pixel，Setting by register P0:0x05 and P0:0x06.

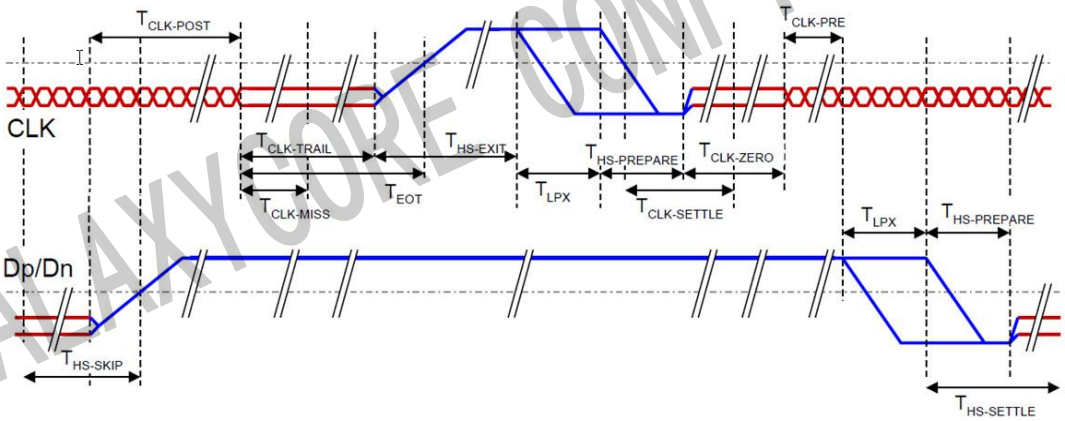
Sh_delay -> Setting by register P0:0x11, P0:0x12.

win_width -> Setting by register P0:0x0f and P0:0x10, win_width = final_output_width + 16. So for UXGA, we should set win_width as 1616.

HPCLK -> half PCLK.

5.2 MIPI

5.2.1 Clock lane low-power



Notice:

- Clock must be reliable during high speed transmission and mode-switching.
- Clock can go to LP only if data lanes are in LP (and nothing relies on it).
- In Low-Power data lanes are conceptually asynchronous (independent of the high speed clock).

  T_{CLK_PRE}: setting by Register P3: 0x24

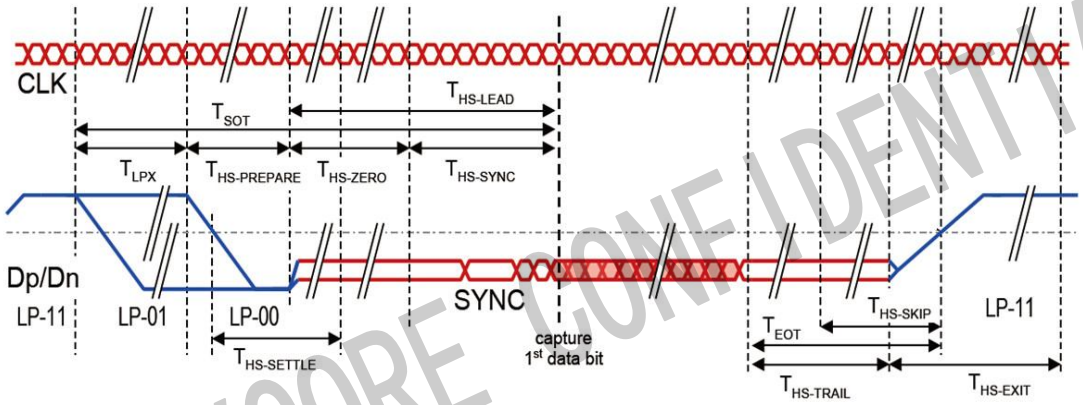
  $T_{CLK\_HS\_PRE}$: setting by Register P3: 0x22

  T_{CLK_POST} : setting by Register P3: 0x25

  T_{CLK_ZERO}: setting by Register P3: 0x23

  T_{CLK_TRAIL}: setting by Register P3: 0x26

5.2.2 Data Burst



Notice:

- Clock keeps running and samples data lanes (except for lanes in LPS).
- Unambiguous leader and trailer sequences required to distill real bits.
- Trailer is removed inside PHY (a few bytes).
- Time-out to ignore line values during line state transition.

  T_{LPX}: setting by Register P3:0x21

  $T_{HS\_PREPARE}$: setting by Register P3: 0x29

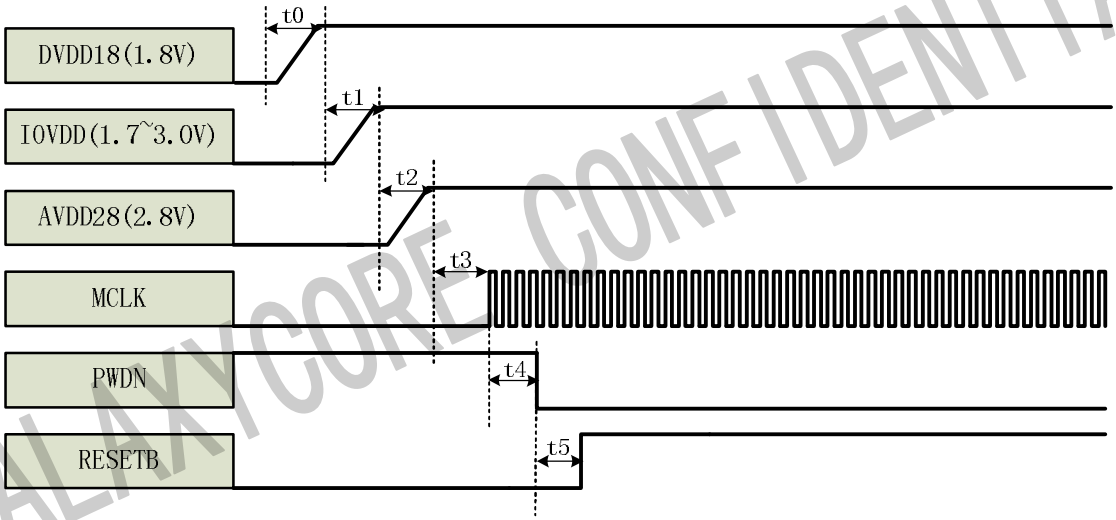
  T_{HS_ZERO}: setting by Register P3: 0x2a

  T_{HS_TRAIL}: setting by Register P3: 0x2b

  T_{HS_EXIT}: setting by Register P3: 0x27

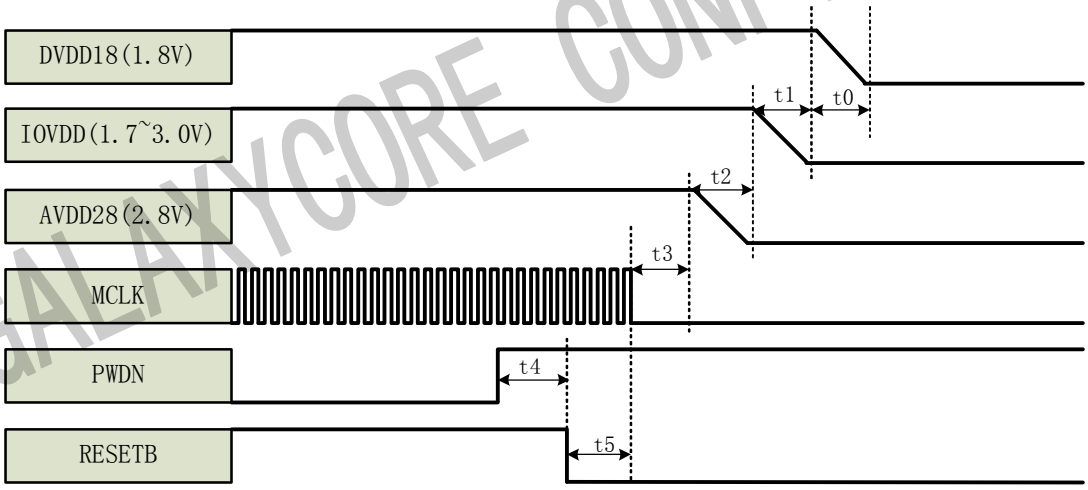
5.3 Power On/Off Sequence

5.3.1 Power On Sequence



Parameter	Description	Min.	Max.	Unit
t0	DVDD18 rising time	100		us
t1	From DVDD18 to IOVDD	50		us
t2	From IOVDD to AVDD28	50		us
t3	From AVDD28 to MCLK applied	>0		us
t4	From MCLK applied to Sensor enable	>0		us
t5	From PWDN pull low to RESET pull high	>0		us

5.3.2 Power Off Sequence



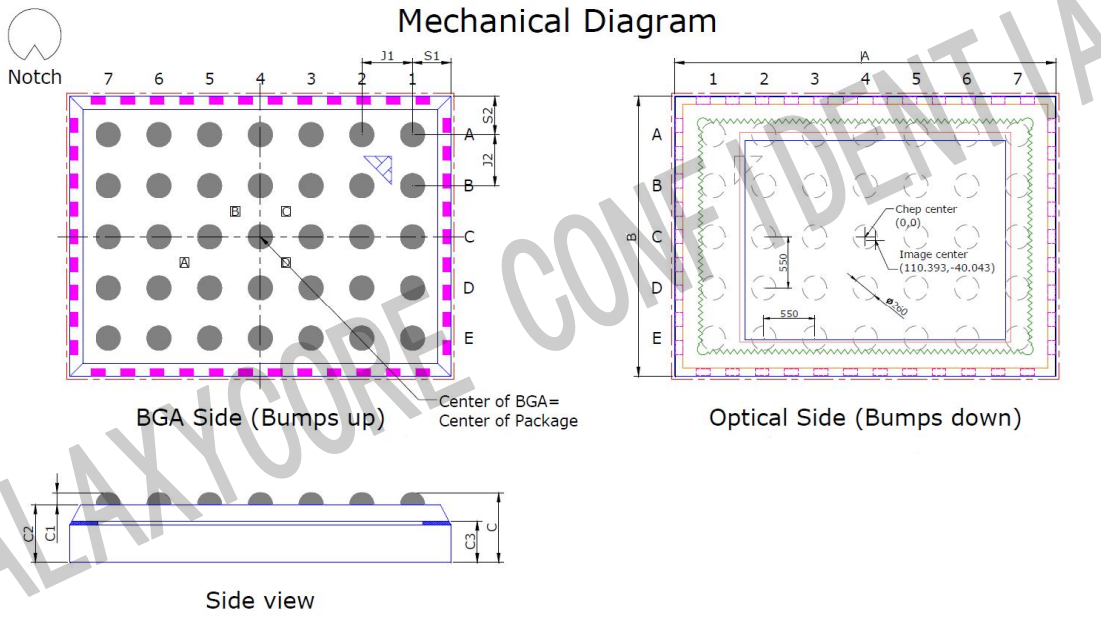
Parameter	Description	Min.	Max.	Unit
t0	From IOVDD to DVDD18 falling time	>0		us
t1	From AVDD28 to IOVDD falling time	>0		us
t2	AVDD28 falling time	>0		us
t3	From MCLK disable to sensor AVDD28 power down	>0		us
t4	From sensor disable to RESET pull low	>0		us
t5	From sensor RESET pull low to MCLK disable	>0		us

- **Recommended power on/off sequence is above.**
- **If you have special requirements in application, please contact with us to confirm.**

5.4 DC Parameters

Symbol		Parameter	Min	Typ	Max	Unit
Supply						
V_{AVDD28}		Power supply	2.7	2.8	3.0	V
V_{DVDD18}		Supply voltage(digital core)	1.7	1.8	1.9	V
V_{IOVDD}		Supply voltage(digital I/O)	1.7	1.8	3.0	V
I_{AVDD28}		Active(operating) current		30	60	mA
I_{DVDD18}				20	40	mA
I_{IOVDD}	1.8V			10	20	mA
	2.8V			15	30	mA
I_{DDS_PWD}		Standby Current	30	60	100	uA
Digital Input(Typical conditions: AVDD28 = 2.8V，DVDD = 1.8V，IOVDD = 1.8V)						
V_{IH}		Input voltage HIGH	1.4			V
V_{IL}		Input voltage LOW			0.6	V
Digital Output(AVDD28 = 2.8V，standard Loading 25PF，IOVDD = 1.8V)						
V_{OH}		Output voltage HIGH	1.6			V
V_{OL}		Output voltage LOW			0.2	V

6. Package Specification



Parameter	Symbol	Nominal	Min.	Max.
		μ m		
Package Body Dimension X	A	4130	4105	4155
Package Body Dimension Y	B	3022	2997	3047
Package Height	C	760	700	820
Ball Height	C1	130	100	160
Package Body Thickness	C2	630	585	675
Thickness of Glass surface to wafer	C3	445	425	465
Ball Diameter	D	260	230	290
Total Pin Count	N	35		
Pins Count X axis	N1	7		
Pins Count Y axis	N2	5		
Pins Pitch X axis	J1	550		
Pins Pitch Y axis	J2	550		
Edge to Pin Center Distance along X	S1	415	385	445
Edge to Pin Center Distance along Y	S2	411	381	441

7. Register List

System Register

Address	Name	Width	Default Value	R/W	Description
0xf0	**Sensor_ID_highbit**	**8**	**0x22**	**RO**	**Sensor_ID**
0xf1	**Sensor_ID_low**	**8**	**0x35**	**RO**	**Sensor_ID**
0xf2	pad_vb_hiz_mode data_pad_io sync_pad_io	5	0x00	RW	[7:5] NA [4] pad_vb_hiz_mode [3] data_pad_IO [2:0] sync_pad_io_ebi
0xf6	Up_down Pwd_dn	6	0x00	RW	[7:6] NA [5:4] up_dn 00: not pull 01:pull down 10: pull up 11: illegal [3:1] NA [0] PWD dn 0: pull down 1: not pull
0xf7	PLL_mode1	6	0x00	RW	[7:6] NA [5:4] serial_clk_double [3] clk_double [2] Mode 24MHz 1: MCLK x32(MCLK 24MHz) 0: MCLK x48(MCLK 12MHz) [1] div2en 1: divider MCLK 1/2 0: not divider [0] PLL_en 1: enable 0: disable
0xf8	PLL_mode2	8	0x00	RW	[7] PLL dgdiv enable [6] NA [5:0] div MIPI:MCLK*(div+1)*4 DVP: MCLK*(div+1)/4
0xf9	Cm_mode	8	0x00	RW	[7] super clk enable [6] 2pclk enable

					[5] pclk enable [4] hpclk enable [3] ISP all clock enable [2] serial clock enable [1] re-lock PLL [0] not use PLL
0xfa	clk_div_mode	8	0x00	RW	[7:4] +1 represent the frequency division number [3:0] represent the high level in one pulse after frequency division MCLK by Div duty 0x11 2 1:1 0x21 3 1:2 0x22 3 2:1 0x31 4 1:3 0x32 4 2:2 0x33 4 3:1 …
0xfb	i2c_device_id	8	0x78	RW	[7:1] I2C device ID, can write once [0] NA
0xfc	analog_pwc	3	0x01	RW	[7:3] NA [2] vpix_en [1] NA [0] apwd
0xfe	Reset related	8	0x00	RW	[7] soft_reset [6] cm_reset [5] mipi_reset [4] CISCTL_restart_n, restart CISCTL, effective low [3] spi_reset [2:0] page_select

Analog & CISCTL

Address	Name	Width	Default Value	R/W	Description
P0:0x03	Exposure[12:8]	5	0x00	RW	[7:5] NA [4:0] exposure[12:8], use line processing time as the unit.
P0:0x04	Exposure[7:0]	8	0x10	RW	Exposure[7:0]
P0:0x05	HB[11:8]	4	0x01	RW	H Blanking

P0:0x06	HB[7:0]	8	0x2a	RW	
P0:0x07	VB[12:8]	5	0x00	RW	Vertical blanking, if current exposure < (Vb + window Height) , frame rate will be (Vb + window Height); otherwise frame rate will be determined by exposure
P0:0x08	VB[7:0]	8	0x10	RW	
P0:0x09	Row_start[10:8]	3	0x00	RW	Row Start
P0:0x0a	Row_start[7:0]	8	0x00	RW	
P0:0x0b	Col_start[10:8]	3	0x00	RW	Col start
P0:0x0c	Col_start[7:1]	8	0x04	RW	
P0:0x0d	win_height[10:8]	3	0x04	RW	[7:3] NA [2:0] Window height[10:8]
P0:0x0e	win_height[7:0]	8	0xd0	RW	Window height[7:0]
P0:0x0f	win_width[10:8]	3	0x06	RW	[7:3] NA [2:0] Window width[10:8]
P0:0x10	win_width[7:1]	8	0x50	RW	window width[7:0]
P0:0x11	Sh_delay[9:8]	2	0x00	RW	Sh_delay[9:8]
P0:0x12	Sh_delay[7:0]	8	0x0a	RW	Sh_delay[7:0]
P0:0x13	Vs_st	8	0x02	RW	Vs_st
P0:0x14	Vs_et	8	0x02	RW	Vs_et
P0:0x15	Reserved	8	0x00	RW	Reserved
P0:0x16	Reserved	8	0xc1	RW	Reserved
P0:0x17	Mirror & Flip	8	0X00	RW	[7:2] Reserved [1] Flip [0] mirror
P0:0x18	Reserved	8	0x0a	RW	Reserved
P0:0x19	Reserved	8	0x05	RW	Reserved
P0:0x1a	Reserved	8	0x0c	RW	Reserved
P0:0x1b	Reserved	8	0x44	RW	Reserved
P0:0x1c	Reserved	8	0x11	RW	Reserved
P0:0x1d	Reserved	8	0x00	RW	Reserved
P0:0x1e	Reserved	8	0x93	RW	Reserved
P0:0x1f	Reserved	8	0x18	RW	Reserved
P0:0x20	Reserved	8	0x00	RW	Reserved
P0:0x21	Reserved	8	0x40	RW	Reserved
P0:0x22	Reserved	8	0xb2	RW	Reserved
P0:0x23	Reserved	8	0x05	RW	Reserved
P0:0x24	Analog_PAD_d	8	0x15	RW	[7:6] NA

	rv				[5:4] sync_drv 00: 4mA 01: 8mA 10: 12mA 11: 16mA [3:2] data_drv 00: 8mA 01: 12mA 10: 16mA 11: 20mA [1:0] pclk_drv 00: 8mA 01: 12mA 10: 16mA 11: 20mA
P0:0x25	Reserved	8	0x00	RW	Reserved
P0:0x26	Reserved	8	0x00	RW	Reserved
P0:0x27	Reserved	6	0x35	RW	Reserved
P0:0x3f	Reserved	8	0x11	RW	Reserved

CSI/PHY1.0

Address	Name	Width	Default Value	R/W	Description
P3:0x01	DPHY_analog_mode1	8	0x00	RW	[6] CTD_lan1 [5] CTD_lane0 [4] CTD_clk [2] PHY_lane1_en [1] PHY_lane0_en [0] PHY_clk_en
P3:0x02	DPHY_analog_mode2	8	0x00	RW	[6:4] lane0_diff [2:0] clk_diff
P3:0x03	DPHY_analog_mode3	8	0x00	RW	[6] lane1_delay [5] lane0_delay [4] clk_delay [2:0] lane1_diff
P3:0x04	FIFO_prog_full_level[7:0]	8	0xa0	RW	FIFO_prog_full_level[7:0]
P3:0x05	FIFO_prog_full_level[11:8]	8	0x00	RW	FIFO_prog_full_level[11:8]
P3:0x06	FIFO_mode	8	0x00	RW	[7] MIPI_clk_Module

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					[6] manual CSI2_up_mode [5] NA [4] FIFO_rst_mode [3] use_SRAM1_mode [2] NA [1] FIFO switch read [0] FIFO switch write
P3:0x10	buf_CSI2_mode	8	0x00	RW	[7] lane_en [6] NA [5] ULP_mode [4] MIPI_en [3] bit10_switch [2] RAW8 [1] line_sync_mode [0] double_lane
P3:0x11	LDI_set	8	0x2b	RW	RAW10
P3:0x12	LWC_set[7:0]	8	0x20	RW	Long packet WC set
P3:0x13	LWC_set[15:8]	8	0x03	RW	Long packet WC set
P3:0x14	SYNC_set	8	0xb8	RW	SYNC
P3:0x15	DPHY_mode	8	0x00	RW	[7:4] trigger mode [7] read_ready [6] half [5] full [4] prog [3] PP_mode , XOL mode [2] NA [1:0] clklane_mode 1X: frames keep 01: clock lane sync with data lane 00: every frame stop clk lane mode
P3:0x16	LP_set	8	0x09	RW	[7:6] HIGH-Z [3:2] 1 [1:0] 0
P3:0x17	MIPI_wdiv_set	4	0x01	RW	MIPI_wdiv_set, default 1/2
P3:0x20	T_init_set	8	0x80	RW	Timing of initial setting
P3:0x21	T_LPX_set	8	0x10	RW	Timing of LP setting
P3:0x22	T_CLK_HS_PREPARE_set	8	0x05	RW	Timing of COCLK HS PREPARE setting
P3:0x23	T_CLK_zero_set	8	0x30	RW	Timing of COCLK HS zero setting
P3:0x24	T_CLK_PRE_set	8	0x02	RW	Timing of COCLK HS PRE of Data setting

P3:0x25	T_CLK_POST_set	8	0x10	RW	Timing of COCLK HS Post of Data setting
P3:0x26	T_CLK_TRAIL_set	8	0x08	RW	Timing of COCLK tail setting
P3:0x27	T_HS_exit_set	8	0x10	RW	Timing of HS exit setting
P3:0x28	T_wakeup_set	8	0xa0	RW	Timing of wakeup setting
P3:0x29	T_HS_PREPARE_set	8	0x06	RW	Timing of data HS PREPARE setting
P3:0x2a	T_HS_Zero_set	8	0x0a	RW	Timing of data HS zero setting
P3:0x2b	T_HS_TRAIL_set	8	0x08	RW	Timing of data HS trail setting
P3:0x3f	FIFO_error_valid	1		RO	Fifo_error

ISP Related

Address	Name	Width	Default Value	R/W	Description
P0:0x8a	Reserved	8	0x9d	RW	Reserved
P0:0x8b	debug_mode1	8	0xa3	RW	[7] update gain mode [6] close exp protection [5] not smooth 2 frame when gain switch [4] test image in OUT [3] output round for 8bits [2] INBF_en [1] OUT gate mode [0] BLK_for_PRC_mode
P0:0x8c	debug_mode2	8	0x07	RW	[7] data delay half 2pclk [6] hsync delay half 2pclk [5] test image when in VGA,UXGA 1: UXGA 0: VGA [4] input test image [3] bypass_mode [2] opclk polarity 0: invert of isp_2pclk(isp_pclk) 1: same as isp_2pclk(isp_pclk) [1] hsync polarity 0: low valid 1: high valid

					[0] vsync polarity 0: low valid 1: high valid
P0:0x8d	Debug_mode3	8	0x03	RW	[7:4] test image fix value, [3] test image fix value mode [2] NA [1: 0] low byte mode
P0:0x90	Crop_win_mode	1	0x00	RW	[7:1] NA [0] Crop out Window mode
P0:0x91	Crop_win_y1[10:8]	3	0x00	RW	[7:3] NA [2:0] Crop _win_y1[10:8]
P0:0x92	Crop_win_y1[7:0]	8	0x00	RW	Crop _win_y1[7:0]
P0:0x93	Crop_win_x1[10:8]	3	0x00	RW	[7:3] NA [2:0] Crop _win_x1[10:8]
P0:0x94	Crop_win_x1[7:0]	8	0x00	RW	Crop _win_x1[7:0]
P0:0x95	out_win_height[10:8]	3	0x04	RW	[7:3] NA [2:0] Out window height[10:8]
P0:0x96	out_win_height[7:0]	8	0xb0	RW	Out window height[7:0]
P0:0x97	out_win_width[10:8]	3	0x06	RW	[7:3] NA [2:0] Out window width[10:8]
P0:0x98	out_win_width[7:0]	8	0x40	RW	Out window width[7:0]
P0:0x7b	Reserved	8	0x00	RW	
P0:0x7c	Reserved	8	0x00	RW	
P0:0x7d	Reserved	8	0x00	RW	

BLK

Address	Name	Width	Default Value	R/W	Description
P0:0x40	Blk_mode1	8	0xa3	RW	[7] not smooth [6:4] BLK_smooth_speed [3] BLK after GAIN [2] dark_current_mode [1] dark_current_en [0] offset_en
P0:0x41	BLK_mode2	8	0x82	RW	Reserved

P0:0x42	BLK_limit_value	8	0xff	RW	When Dark data big than it, while get this to replace it for protect dark data. low align 11bits
P0:0x43	global_offset	7	0x00	RW	[7] NA [6:0] global offset
P0:0x44	current_G1_offset_odd_offset[7:0]	8		RO	current_G1_offset_odd_offset[7:0]
P0:0x45	current_G1_offset_even_offset[7:0]	8		RO	current_G1_offset_even_offset[7:0]
P0:0x46	current_R1_offset_odd_offset[7:0]	8		RO	current_R1_offset_odd_offset[7:0]
P0:0x47	current_R1_offset_even_offset[7:0]	8		RO	current_R1_offset_even_offset[7:0]
P0:0x48	current_B2_offset_odd_offset[7:0]	8		RO	current_B2_offset_odd_offset[7:0]
P0:0x49	current_B2_offset_even_offset[7:0]	8		RO	current_B2_offset_even_offset[7:0]
P0:0x4a	current_G2_offset_odd_offset[7:0]	8		RO	current_G2_offset_odd_offset[7:0]
P0:0x4b	current_G2_offset_even_offset[7:0]	8		RO	current_G2_offset_even_offset[7:0]
P0:0x54	current_G1_offset_odd_dark_current[7:0]	8		RO	current_G1_offset_odd_dark_current[7:0]
P0:0x55	current_G1_offset_even_dark_current[7:0]	8		RO	current_G1_offset_even_dark_current[7:0]
P0:0x56	current_R1_offset_odd_dark_current[7:0]	8		RO	current_R1_offset_odd_dark_current[7:0]
P0:0x57	current_R1_offset_even__dark_current[7:0]	8		RO	current_R1_offset_even__dark_current[7:0]
P0:0x58	current_B2_off	8		RO	current_B2_offset_odd_dark_current[7:0

	set_odd_dark_current[7:0]				]
P0:0x59	current_B2_offset_even_dark_current[7:0]	8		RO	current_B2_offset_even_dark_current[7:0]
P0:0x5a	current_G2_offset_odd_dark_current[7:0]	8		RO	current_G2_offset_odd_dark_current[7:0]
P0:0x5b	current_G2_offset_even_dark_current[7:0]	8		RO	current_G2_offset_even_dark_current[7:0]
P0:0x5c	Exp_rate_darkc	8	0x04	RW	Exp_rate_darkc
P0:0x5d	Offset_submode Darkc_submode	8	0x00	RW	[7:4] Offset_submode [3:0] Darkc_submode
P0:0x5e	current_G1_offset_odd_ratio	6	0x18	RW	[7:6] NA [5:0] 1.5bits offset_ratio_G1_odd
P0:0x5f	current_G1_offset_even_ratio	6	0x18	RW	[7:6] NA [5:0] 1.5bits offset_ratio_G1_even
P0:0x60	current_R1_offset_odd_ ratio	6	0x18	RW	[7:6] NA [5:0] 1.5bits offset_ratio_R1_odd
P0:0x61	current_R1_offset_even__ratio	6	0x18	RW	[7:6] NA [5:0] 1.5bits offset_ratio_R1_even
P0:0x62	current_B2_offset_odd_ ratio	6	0x18	RW	[7:6] NA [5:0] 1.5bits offset_ratio_B2_odd
P0:0x63	current_B2_offset_even_ratio	6	0x18	RW	[7:6] NA [5:0] 1.5bits offset_ratio_B2_even
P0:0x64	current_G2_offset_odd_ ratio	6	0x18	RW	[7:6] NA [5:0] 1.5bits offset_ratio_G2_odd
P0:0x65	current_G2_offset_even_ratio	6	0x18	RW	[7:6] NA [5:0] 1.5bits offset_ratio_G2_even
P0:0x66	Dark_current_G1_ ratio	6	0x18	RW	[7:6] NA [5:0] 1.5bits dark_current_ratio_G1
P0:0x67	Dark_current_R1_ ratio	6	0x18	RW	[7:6] NA [5:0] 1.5bits dark_current_ratio_R1
P0:0x68	Dark_current_	6	0x18	RW	[7:6] NA

	B2_ ratio				[5:0] 1.5bits dark_current_ratio_B2
P0:0x69	Dark_current_G2_ ratio	6	0x18	RW	[7:6] NA [5:0] 1.5bits dark_current_ratio_G2
P0:0x6A	manual_G1_odd_offset	6	0x00	RW	[7:6] NA [5:0] S5, aligned to lower 8 of 11 bits data
P0:0x6B	manual_G1_even_offset	6	0x00	RW	[7:6] NA [5:0] S5, aligned to lower 8 of 11 bits data
P0:0x6C	manual_R1_odd_offset	6	0x00	RW	[7:6] NA [5:0] S5, aligned to lower 8 of 11 bits data
P0:0x6D	manual_R1_even_offset	6	0x00	RW	[7:6] NA [5:0]S5, aligned to lower 8 of 11 bits data
P0:0x6E	manual_B2_odd_offset	6	0x00	RW	[7:6] NA [5:0] S5, aligned to lower 8 of 11 bits data
P0:0x6F	manual_B2_even_offset	6	0x00	RW	[7:6] NA [5:0] S5, aligned to lower 8 of 11 bits data
P0:0x70	manual_G2_odd_offset	6	0x00	RW	[7:6] NA [5:0] S5, aligned to lower 8 of 11 bits data
P0:0x71	manual_G2_even_offset	6	0x00	RW	[7:6] NA [5:0] S5, aligned to lower 8 of 11 bits data
P0:0x72	Reserved	3	0x00	RW	Reserved
P0:0x73	Reserved	8	0x10	RW	Reserved
P0:0x74	Reserved	8	0x10	RW	Reserved
P0:0x75	Reserved	8	0x00	RW	Reserved
P0:0x76	Reserved	8	0x00	RW	Reserved
P0:0xc4	current_G1_offset_odd_offset[10:8]	3		RO	[7:3] NA [2:0] current_G1_offset_odd_offset[10:8]
P0:0xc5	current_G1_offset_even_offset[10:8]	3		RO	[7:3] NA [2:0] current_G1_offset_even_offset[10:8]
P0:0xc6	current_R1_offset_odd_offset[10:8]	3		RO	[7:3] NA [2:0] current_R1_offset_odd_offset[10:8]
P0:0xc7	current_R1_offset_even_offse	3		RO	[7:3] NA [2:0]

	t[10:8]				current_R1_offset_even_offset[10:8]
P0:0xc8	current_B2_offset_odd_offset[10:8]	3		RO	[7:3] NA [2:0] current_B2_offset_odd_offset[10:8]
P0:0xc9	current_B2_offset_even_offset[10:8]	3		RO	[7:3] NA [2:0] current_B2_offset_even_offset[10:8]
P0:0xca	current_G2_offset_odd_offset[10:8]	3		RO	[7:3] NA [2:0] current_G2_offset_odd_offset[10:8]
P0:0xcb	current_G2_offset_even_offset[10:8]	3		RO	[7:3] NA [2:0] current_G2_offset_even_offset[10:8]
P0:0xd4	current_G1_offset_odd_dark_current[10:8]	3		RO	[7:3] NA [2:0]current_G1_offset_odd_dark_current[10:8]
P0:0xd5	current_G1_offset_even_dark_current[10:8]	3		RO	[7:3] NA [2:0]current_G1_offset_even_dark_current[10:8]
P0:0xd6	current_R1_offset_odd_dark_current[10:8]	3		RO	[7:3] NA [2:0]current_R1_offset_odd_dark_current[10:8]
P0:0xd7	current_R1_offset_even_dark_current[10:8]	3		RO	[7:3] NA [2:0]current_R1_offset_even_dark_current[10:8]
P0:0xd8	current_B2_offset_odd_dark_current[10:8]	3		RO	[7:3] NA [2:0]current_B2_offset_odd_dark_current[10:8]
P0:0xd9	current_B2_offset_even_dark_current[10:8]	3		RO	[7:3] NA [2:0]current_B2_offset_even_dark_current[10:8]
P0:0xda	current_G2_offset_odd_dark_current[10:8]	3		RO	[7:3] NA [2:0]current_G2_offset_odd_dark_current[10:8]
P0:0xdb	current_G2_offset_even_dark_current[10:8]	3		RO	[7:3] NA [2:0]current_G2_offset_even_dark_current[10:8]

GLOBAL/PREGAIN

Address	Name	Width	Default Value	R/W	Description

P0:0xa3	channel_gain_G1_odd	8	0x80	RW	G1 odd Channel gain
P0:0xa4	channel_gain_G1_even	8	0x80	RW	G1 even Channel gain
P0:0xa5	channel_gain_R1_odd	8	0x80	RW	R1 odd Channel gain
P0:0xa6	channel_gain_R1_even	8	0x80	RW	R1 even Channel gain
P0:0xa7	channel_gain_B2_odd	8	0x80	RW	B2 odd channel gain
P0:0xa8	channel_gain_B2_even	8	0x80	RW	B2 even channel gain
P0:0xa9	channel_gain_G2_odd	8	0x80	RW	G2 odd channel gain
P0:0xaa	channel_gain_G2_even	8	0x80	RW	G2 even channel gain
P0:0xb0	Global_gain	8	0x40	RW	Global gain
P0:0xb1	Auto_pregain	8	0x40	RW	Auto_pregain
P0:0xb2	Exp_gain_buf_mode	1	0x01	RW	[7:1] NA [0] Update exp and gain as whole
P0:0xb3	AWB_R_gain	8	0x40	RW	AWB_R_gain
P0:0xb4	AWB_G_gain	8	0x40	RW	AWB_G_gain
P0:0xb5	AWB_B_gain	8	0x40	RW	AWB_B_gain

Revision History

Version TBD 2013.02.22

- Document Release

Version V1.0 2013.02.26

- Update 5.3 Power On/Off Sequence
- Update 5.4 DC Parameters

Version V1.1 2013.07.15

- Update 1.4 Technical Specifications
- Update 5.4 DC Parameters