GC2607 CSP

1/7.3’’ 2Mega CMOS Image Sensor

Datasheet

V1.0

2022-05-07

Ordering Information

◆ **GC2607-C20YA**

(Colored, 20PIN-CSP)

GENERATION REVISION HISTORY

Version.	Effective Date	Description of Changes	Prepared by
V1.0	2022-05-07	Document Release	DSC-AE Dept.

Galaxycore Incorporation

Galaxycore Inc. reserves the right to change the contents in this document without prior notice

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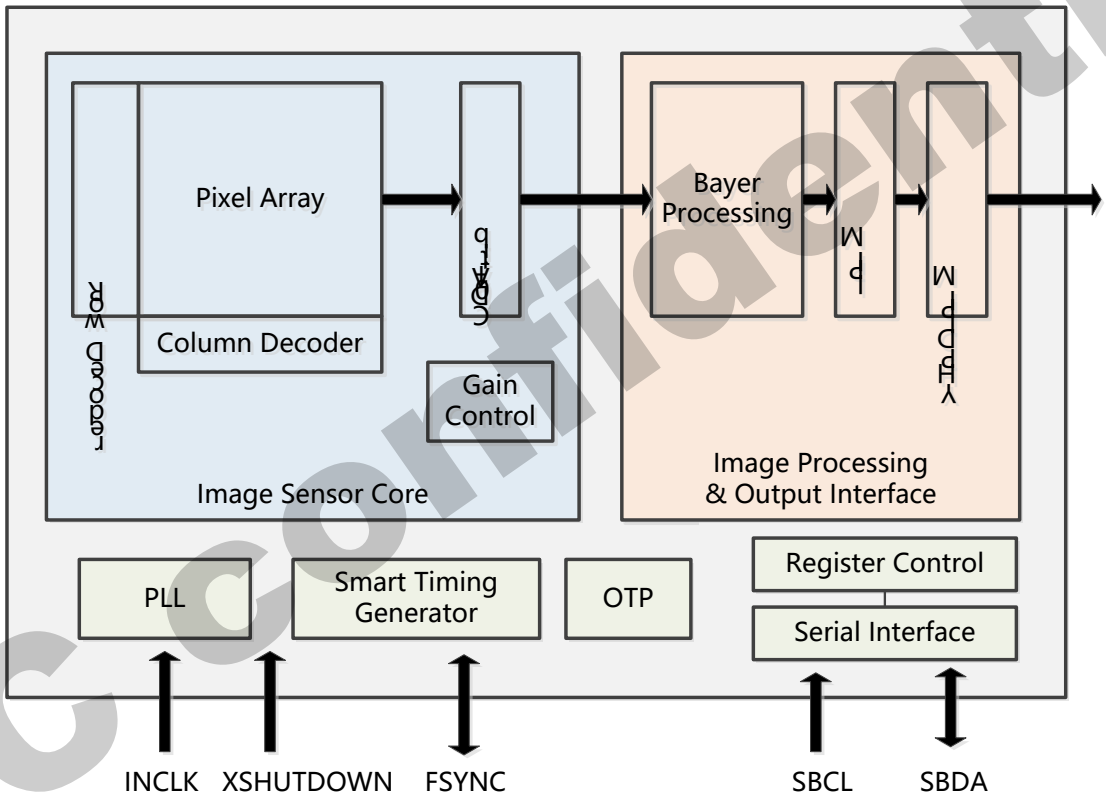
1. Sensor Overview

1.1 General Description

GC2607 is a high quality 2Mega CMOS image sensor, for notebook camera digital camera and mobile phone camera applications. GC2607 incorporates a 1920H x 1080V active pixel array, on-chip 10-bit ADC, and image signal processor. It is programmable through a simple two-wire serial interface and has very low power consumption. It provides RAW10 data formats with MIPI interface.

Figure 1: Block Diagram



1.2 Features

- Optical size: 1/7.3 inch
- Pixel size: 1.12μm x 1.12μm FSI
- Active image size: 1920 x 1080
- Color Filter: RGB Bayer
- Output formats: Raw Bayer 10bit
- Power supply requirement: AVDD28: 2.7~2.9V (Typ. 2.8V)
  DVDD: 1.15~1.25V (Typ. 1.2V)
  IOVDD: 1.7~1.9V (Typ. 1.8V)
- Power Consumption: 76.5mW @Full Size @30fps
- Max Frame rate: 60fps@Full Size
- PLL support
- Frame sync support (master/slave)
- Windowing support
- Mirror and Flip support
- Binning Mode support
- HDR support
- OTP support
- Analog Gain: 32X(Max)
- Sensitivity: 1.97 V/lux.s
- Dynamic range: 72 dB
- MAX SNR: 38 dB
- Dark Current: 8 e-/s @60℃
- Micro lens chief ray angle (CRA): 33.658°(non-linear)
- Operation Temperature: -30~85℃
- Stable Image temperature: -20~60℃
- Storage temperature: -40~125℃
- Package: CSP

2. Electrical Characteristics

2.1 Absolute Maximum Ratings

Table 1: Absolute Maximum Ratings

Description	Symbol	Rating	Unit	Note
Analogue absolute max	V_{AVDD_MAX}	-0.3~3.9	V	Refer to GND
Digital absolute voltages	V_{DVDD_MAX}	-0.3~1.8	V	
IO absolute max	V_{IOVDD_MAX}	-0.3~3.6	V	
Digital input voltages	V_{IF_MAX}	-0.3~V_{IOVDD}+0.3	V	

Note: Digital input voltage: XCLK, SBCL, SBDA, XSHUTDOWN, FSYNC

2.2 Operation Conditions

Table 2: Operation Conditions

Description	Symbol	Min.	Typical	Max.	Unit
Analog power supply	V_{AVDD}	2.7	2.8	2.9	V
Digital power supply	V_{DVDD}	1.15	1.2	1.25	V
IO power supply	V_{IOVDD}	1.7	1.8	1.9	V
Digital input voltages	V_{IF}	0		IOVDD	V
Test temperature	T_{TEST}	21	25	27	℃

Note: 1. Digital input voltage: XCLK, SBCL, SBDA, XSHUTDOWN, FSYNC.
2. Test temperature: image quality test condition.

2.3 DC Characteristics

Table 3: DC Characteristics

Characteristics	Symbol	Min.	Typical	max	Unit
Input voltage HIGH	V_{IH}	0.7 x V_{IF}	-	-	V
Input voltage Low	V_{IL}	-	-	0.3 x V_{IF}	V
Output voltage HIGH	V_{OH}	0.7 x V_{IOVDD}	-	-	V
Output voltage LOW	V_{OL}	-	-	0.3 x V_{IOVDD}	V

Note: Input voltage apply to XCLK, SBCL, SBDA, XSHUTDOWN, FSYNC.

2.4 AC Characteristics

Figure 2: AC Characteristics

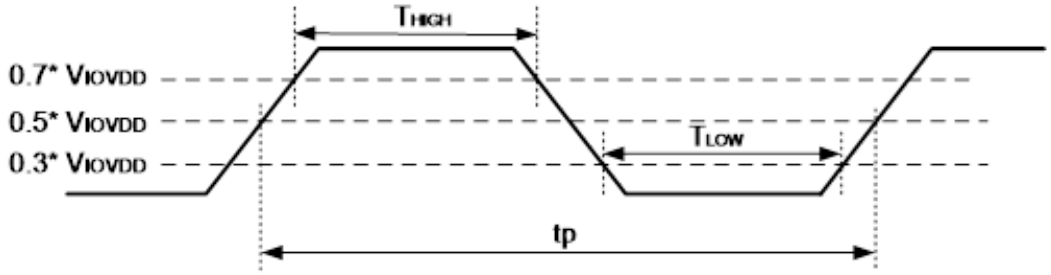


Table 4: AC Characteristics

Item	Symbol	Min.	Typ.	max	unit
Frequency	f_{SCK}	6	24	36	MHz
jitter (period, peak-to-peak)	T_{jitter}			600	ps
High level width	T_{HIGH}	0.4tp		0.6tp	ns
Low level width	T_{LOW}	0.4tp		0.6tp	ns
Duty Cycle	f_{DUTY}	40		60	%

2.5 Power Consumption

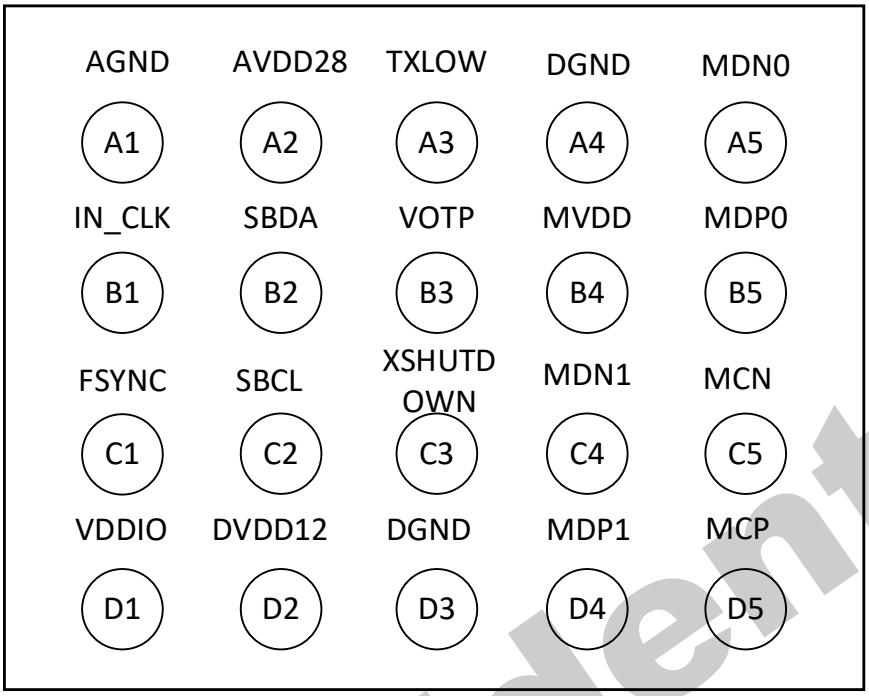
Table 5: Power Consumption

Item	Symbol	Min	Typ	Max	Unit
Full size @30fps MIPI 2lane	I_{AVDD}	-	17.53	-	mA
	I_{DVDD}		18.1		mA
	I_{IOVDD}	-	3.15	-	mA
Full size @60fps MIPI 2lane	I_{AVDD}	-	**TBD**	-	mA
	I_{DVDD}		**TBD**		mA
	I_{IOVDD}	-	**TBD**	-	mA
Standby current	I_{AVDD}	-	77.7	-	μA
	I_{DVDD}		41.9		μA
	I_{IOVDD}	-	13.5	-	μA
Power off current	I_{total}	-	-	0	μA

Note: 1. All operate current are measured at 24MHz XCLK.
2. Standby current is measured at XSHUTDOWN = L, XCLK=24MHz.
3. We recommend that power should be turned off, when lower power consumption is required.

3. CSP Package Specifications

Figure 3: CSP Pin Top View



3.1 Pin Descriptions

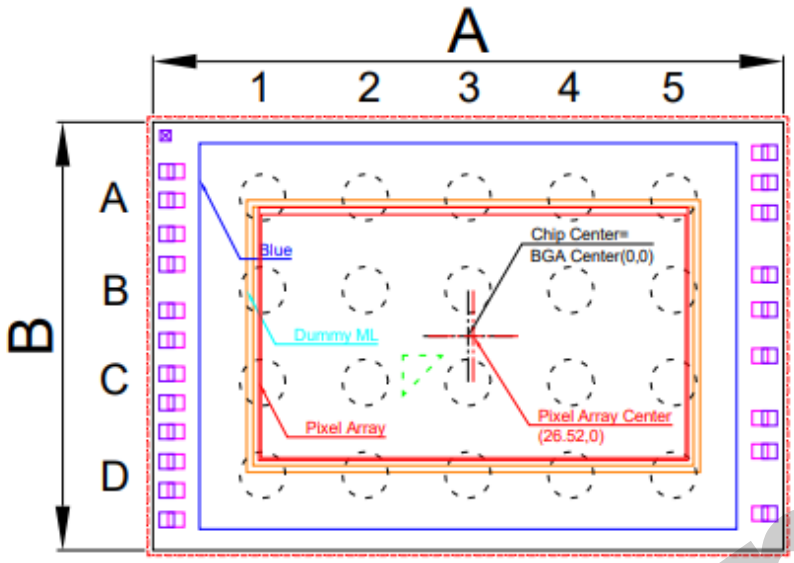
Table 6: Pin Descriptions

Pin	Name	Type	A/D	Description
A1	AGND	Ground	A	Ground for analog
A2	AVDD28	Power	A	Analog power supply: 2.8V
A3	TXLOW	Power	A	Internal power supply.
A4	DGND	Ground	D	Ground for digital
A5	MDN0	Output	D	MIPI data<0> (-)
B1	IN_CLK	Input	D	Sensor input clock
B2	SBDA	Input	D	Two-wire serial bus, data.
B3	VOTP	Power	D	OTP power supply: 7V (floating available)
B4	MVDD	Power	D	MIPI Power supply: 1.2V
B5	MDP0	Output	D	MIPI data <0> (+)
C1	FSYNC	I/O	D	Frame sync control
C2	SBCL	Input	D	Two-wire serial bus, clock.
C3	XSHUTDOWN	Input	D	Sensor power down control: (Floating forbidden) 0: reset & standby; 1: normal work
C4	MDN1	Output	D	MIPI data <1> (-)
C5	MCN	Output	D	MIPI clock (-)
D1	VDDIO	Power	D	I/O Power supply: 1.8V

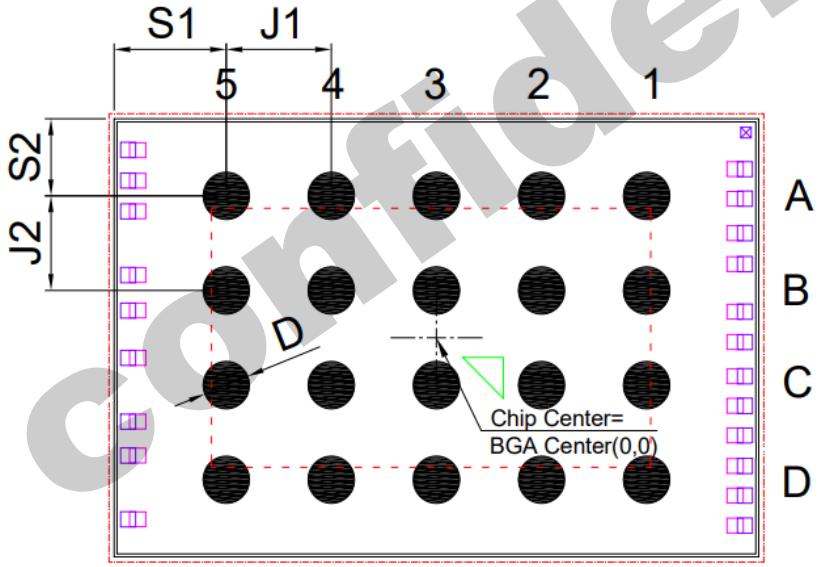
Pin	Name	Type	A/D	Description
D2	DVDD12	Power	D	Digital power supply: 1.2V
D3	DGND	Ground	D	Ground for Digital.
D4	MDP1	Output	D	MIPI data <1> (+)
D5	MCP	Output	D	MIPI clock (+)

3.2 Package Specification

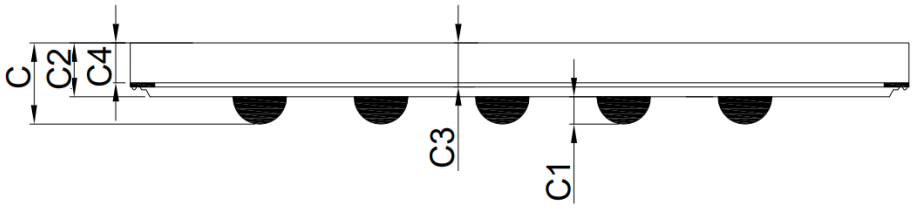
Figure 4: Mechanical Drawing View(μ m)



Top View(Bumps Down)



Back View(Bumps Up)



Side View

Table 7: Package Specifications

Description	symbol	Nominal	Min	Max
		Millimeters		
Package Body Dimension X	A	3.190	3.165	3.215
Package Body Dimension Y	B	2.130	2.105	2.155
Package Height	C	0.660	0.605	0.715
Ball Height	C1	0.130	0.100	0.160
Package Body Thickness	C2	0.530	0.495	0.565
Thickness from top glass surface to wafer	C3	0.345	0.325	0.365
Glass Thickness	C4	0.300	0.290	0.305
Ball Diameter	D	0.230	0.200	0.260
Total Ball Count	N	20		
Ball Count X axis	N1	5		
Ball Count Y axis	N2	4		
Pins pitch X axis	J1	0.520		
Pins pitch Y axis	J2	0.460		
BGA ball center to package center offset in X-direction	X	0.0000	-0.0250	0.0250
BGA ball center to package center offset in Y-direction	Y	0.0000	-0.0250	0.0250
BGA ball center to chip center offset in X-direction	X1	0.0000	-0.0250	0.0250
BGA ball center to chip center offset in Y-direction	Y1	0.0000	-0.0250	0.0250
Edge to Pin Center Distance along X	S1	0.555	0.525	0.585
Edge to Pin Center Distance along Y	S2	0.375	0.345	0.405

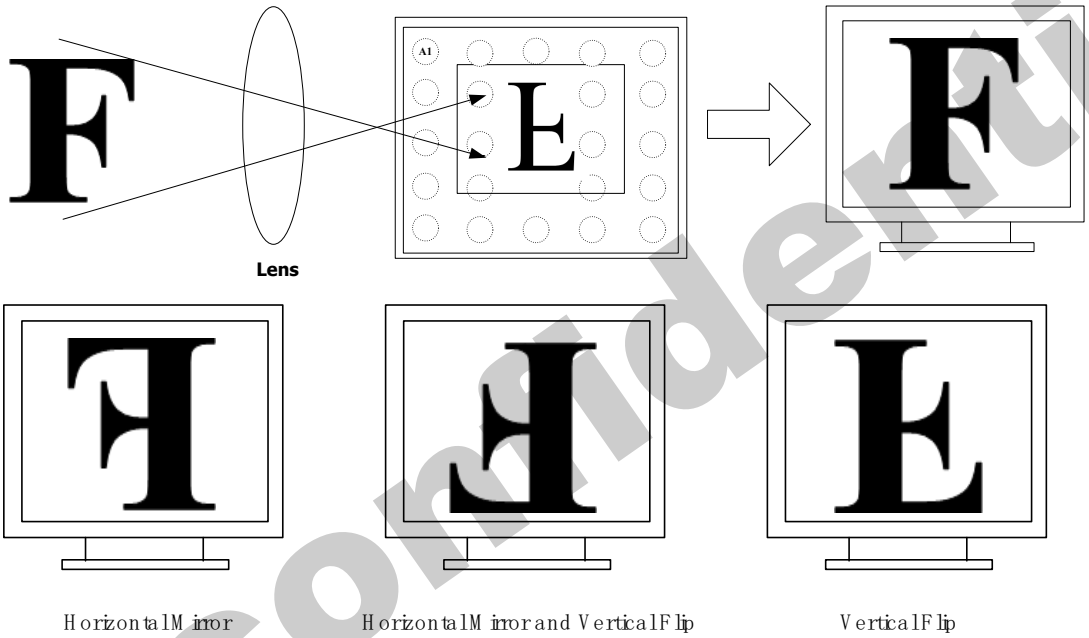
Note: The package center, optical center, and BGA center of the chip are not coincident. If setting the package center as the origin (0, 0), the BGA center coordinate is (0, 0), the optical center coordinate is (26.52, 0), with μm unit

4. Optical Specifications

4.1 Readout Position

GC2607 default status is readout from the lower left corner with pin A1 located in the upper left corner. The image is inverted vertically and horizontally by the lens, so proper image output results when Pin A1 is located in the upper left corner.

Figure 5: Readout Position



Readout direction can be set by the registers.

Table 8: Mirror and Flip Information

Function	Register Address	Register Value	First Pixel
Normal	0x0101[1:0]	00	Gr
Horizontal mirror	0x0101[1:0]	01	R
Vertical Flip	0x0101[1:0]	10	B
Horizontal Mirror and Vertical Flip	0x0101[1:0]	11	Gb

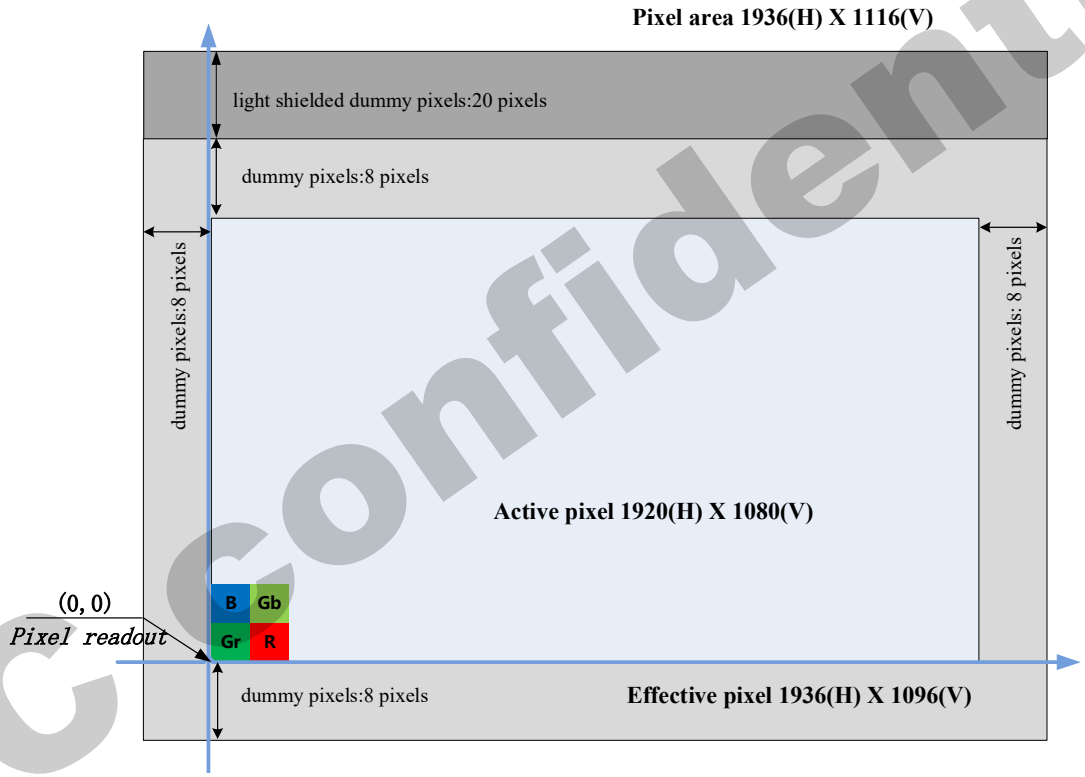
4.2 Pixel Array

Pixel array is covered by Bayer pattern color filters. The primary color GR/BG array is arranged in line-alternating way.

If no flip in column, column is read out from 0 to 1919. If flip in column, column is read out from 1919 to 0.

If no flip in row, row is read out from 0 to 1079.If flip in row, row is read out from 1079 to 0.

Figure 6: Pixel Array



4.3 Lens Chief Ray Angle (CRA)

Figure 7 CRA Information

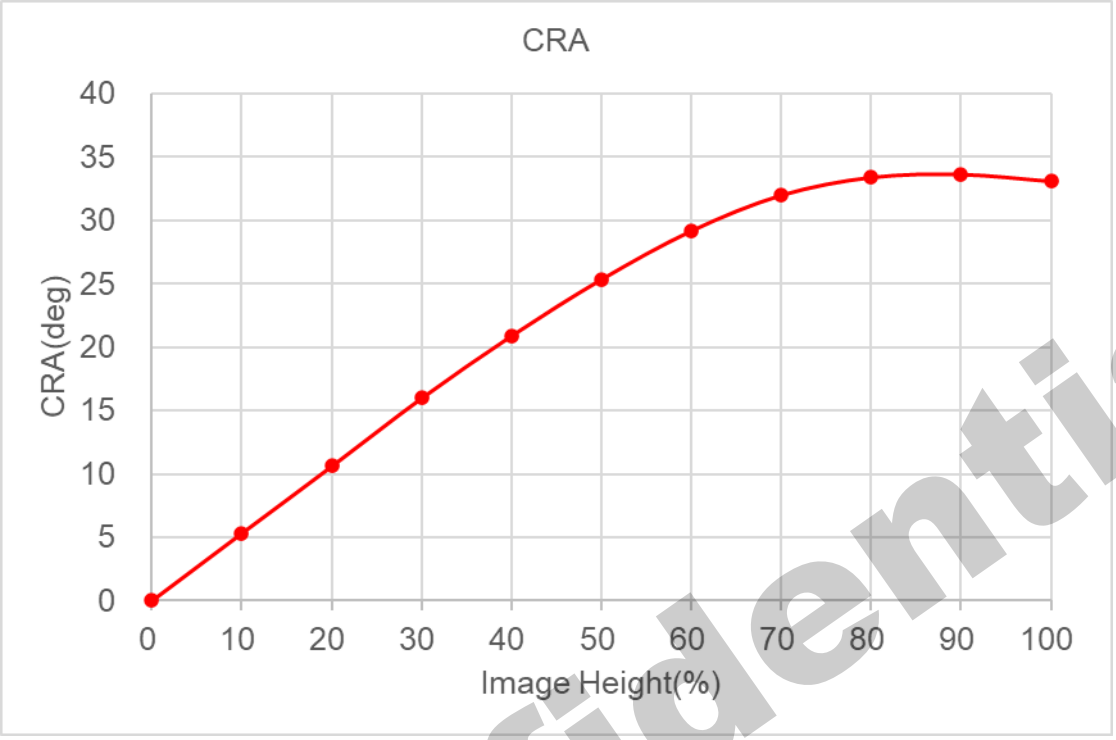


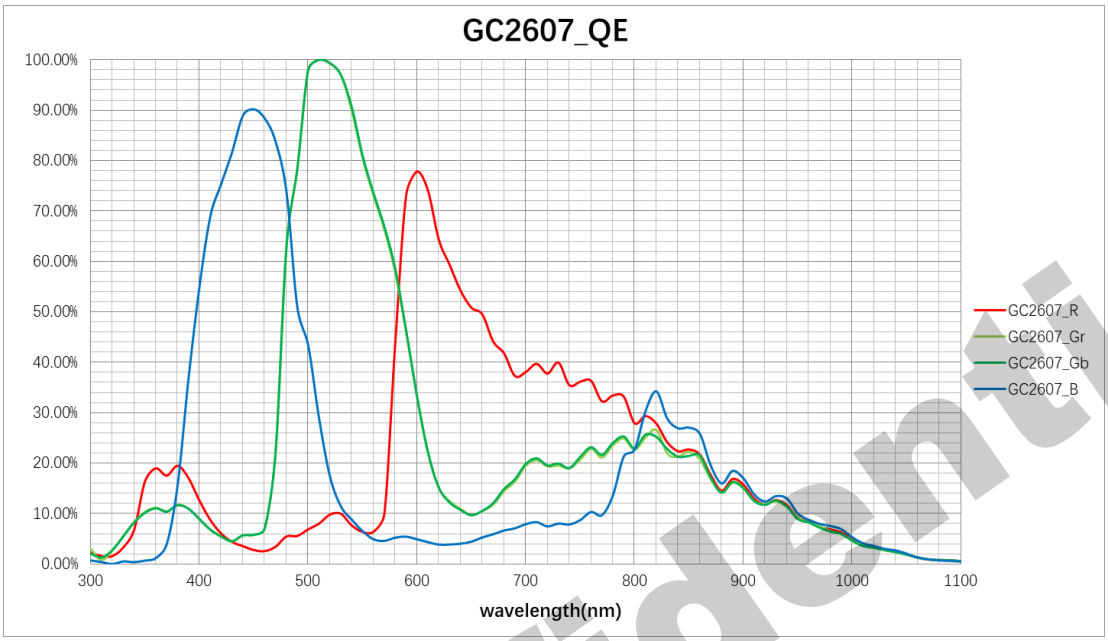
Table 9: CRA Information

Image Heigh (%)	Image Height (mm)	CRA (degree)
00	0.000	0.000
10	0.123	5.327
20	0.247	10.621
30	0.370	15.988
40	0.493	20.910
50	0.617	25.368
60	0.740	29.198
70	0.864	32.015
80	0.987	33.420
90	1.110	33.658
100	1.234	33.115

4.4 QE Spectral Characteristics

The optical spectrum of QE is below:

Figure 8 QE curve



5. Two-wire Serial Bus Communication

GC2607 Device Address:

Table 10: Device ID

Slave address write mode	Slave address read mode
0x6e	0x6f

5.1 Protocol

The host must perform the role of a communications master and GC2607 acts as either a slave receiver or transmitter. The master must do:

- Generate the **Start(S)/Stop(P)** condition
- Provide the serial clock on **SBCL**

Figure 9: Write operate (2 bytes address –1byte data format)

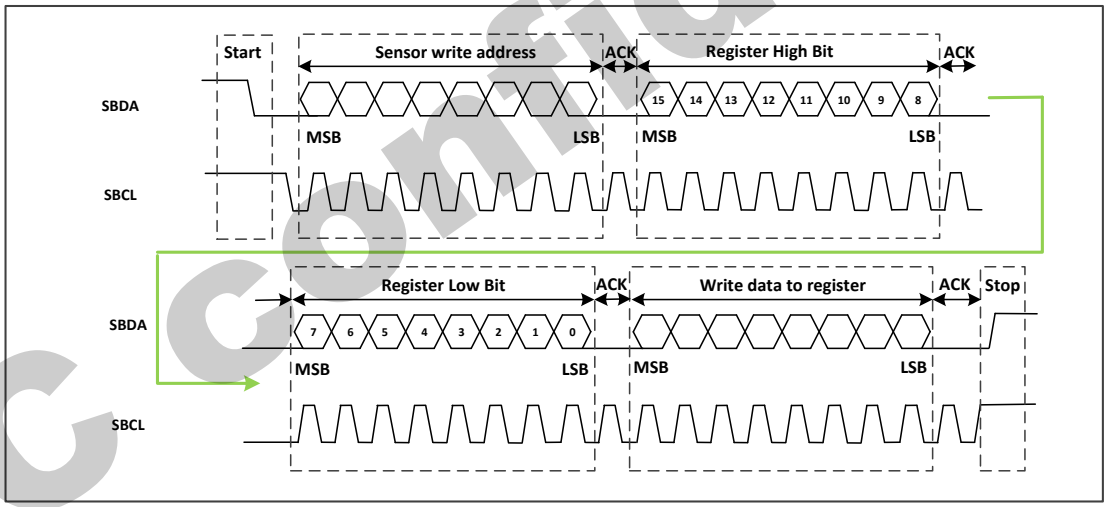
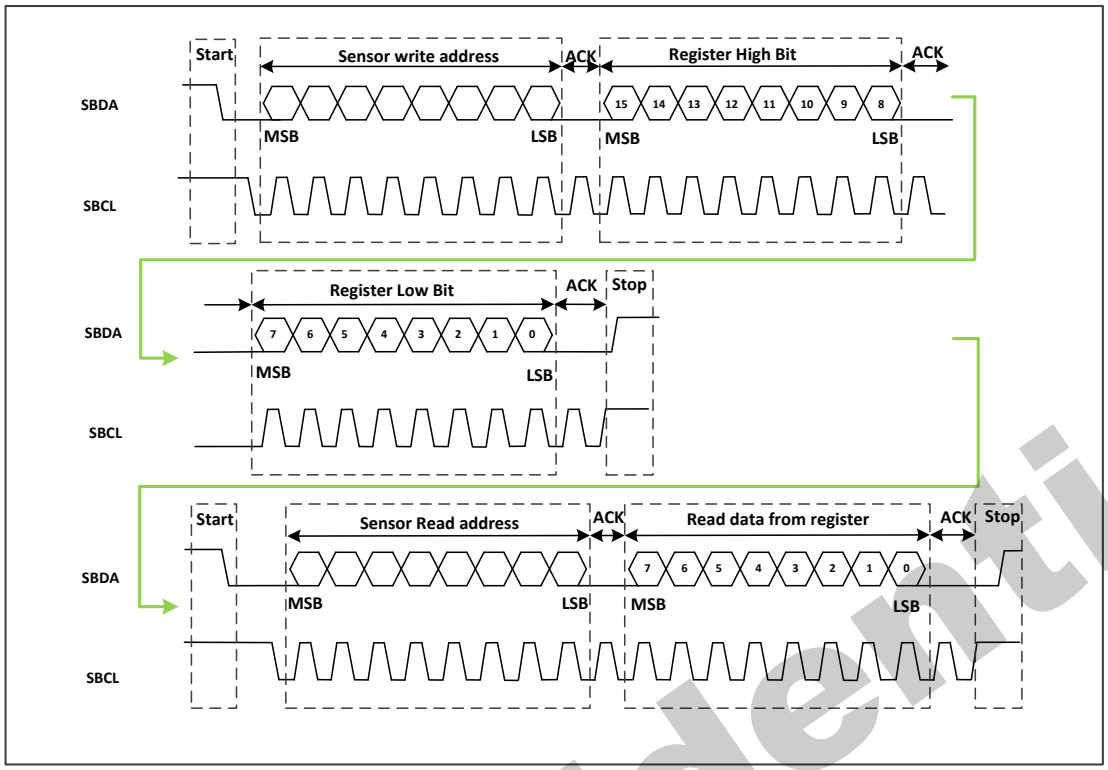


Figure 10: Read Operate (2 bytes address –1byte data format)



5.2 Serial Bus Timing

Figure 11: Serial Bus Timing

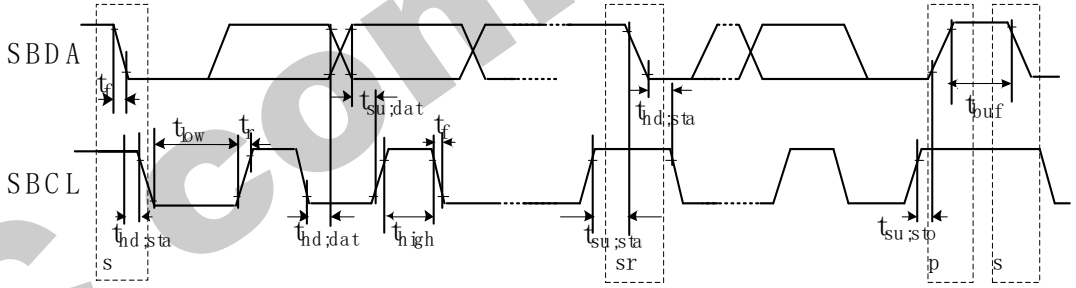


Table 11: Serial Bus Timing

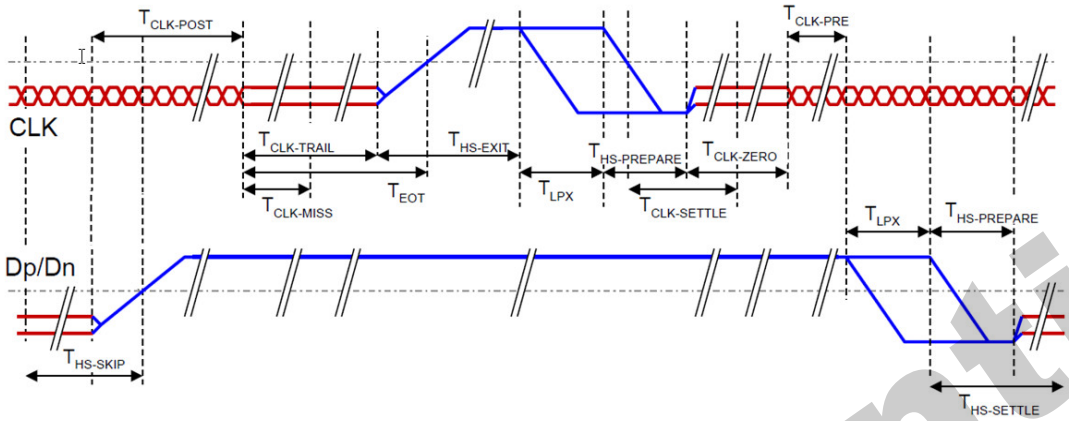
Parameter	Symbol	Min	Typ.	Max	Unit
SBCL clock frequency	F_{scl}	0	--	400	KHz
Bus free time between a stop and a start	t_{buf}	1.3	--	--	μs
Hold time for a repeated start	$t_{hd;sta}$	0.6	--	--	μs
LOW period of SBCL	t_{low}	1.3	--	--	μs
HIGH period of SBCL	t_{high}	0.6	--	--	μs
Set-up time for a repeated start	$t_{su;sta}$	600	--	--	ns
Data hold time	$t_{hd;dat}$	0	--	900	ns

Data Set-up time	$t_{su;dat}$	100	--	--	ns
Rise time of SBCL, SBDA	t_r	--	--	300	ns
Fall time of SBCL, SBDA	t_f	--	--	300	ns
Set-up time for a stop	$t_{su;sto}$	0.6	--	--	μs
Capacitive load of bus line (SBCL, SBDA)	C_b	--	--	100	pf

6. MIPI Timing

6.1 Clock Lane Low-power

Figure 12: MIPI Clock Lane Time

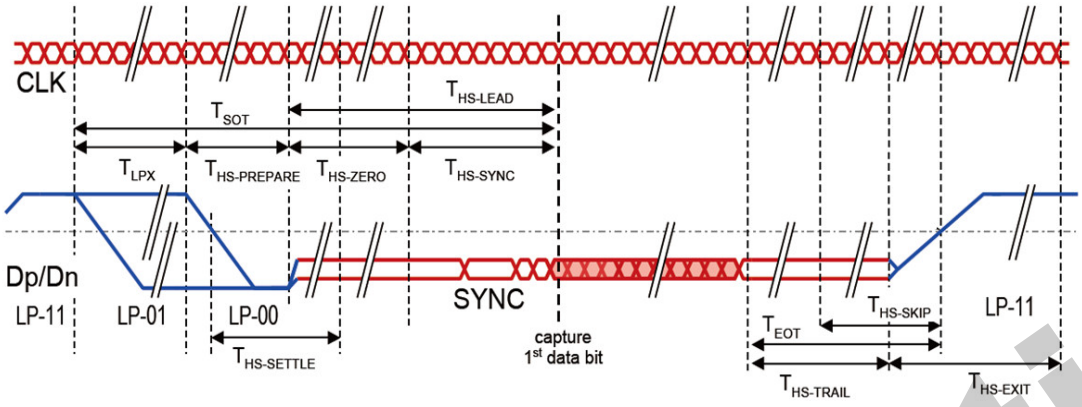


Notice:

- Clock must be reliable during high speed transmission and mode-switching.
- Clock can go to LP only if data lanes are in LP (and nothing relies on it).
- In Low-Power data lanes are conceptually asynchronous (independent of the high speed clock).
  - $T_{CLK\_HS\_PREPARE}$: setting by Register 0x0db4
  - T_{CLK_ZERO}: setting by Register 0x0db5
  - T_{CLK_PRE}: setting by Register 0x0db6
  - T_{CLK_POST}: setting by Register 0x0db8
  - T_{CLK_TRAIL}: setting by Register 0x0db9

6.2 Data Burst

Figure 13: MIPI Data Lane Time



Notice:

- Clock keeps running and samples data lanes (except for lanes in LPS).
- Unambiguous leader and trailer sequences required to distill real bits.
- Trailer is removed inside PHY (a few bytes).
- Time-out to ignore line values during line state transition.
  - T_{LPX}: setting by Register 0x0d93
  - $T_{HS\_PREPARE}$: setting by Register 0x0d94
  - T_{HS_ZERO}: setting by Register 0x0d95
  - T_{HS_TRAIL}: setting by Register 0x0d99
  - T_{HS_EXIT}: setting by Register 0x0d9b

7. Function Description

7.1 Operation Mode

Figure 14: Operation Mode

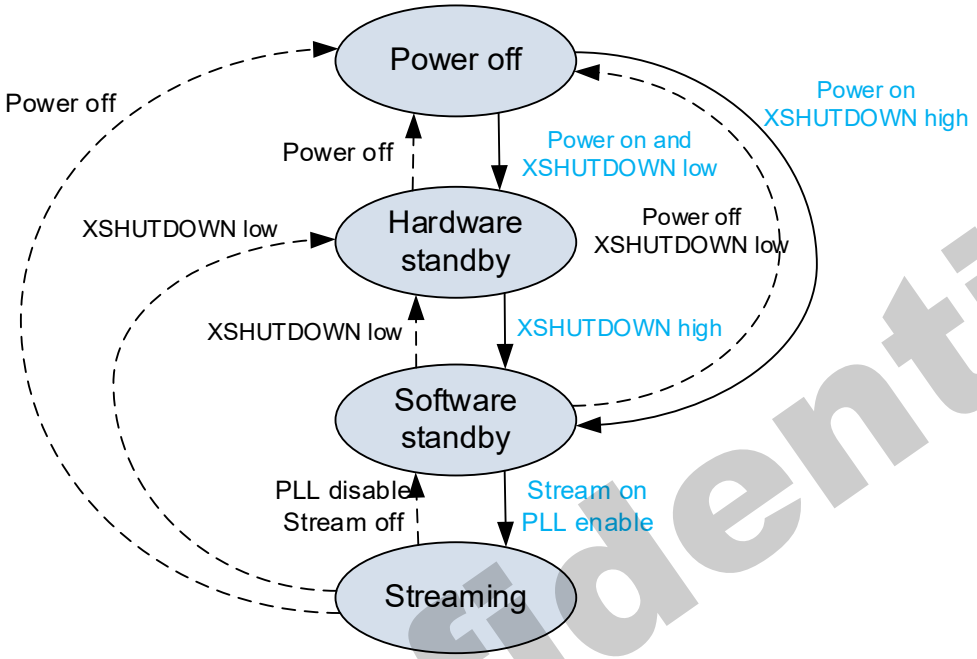


Table 12: Operate State

Power state	Description	Activate
Power off	Power supplies are turned off	None
Hardware standby	No communication with sensor, low level on XSHUTDOWN	XSHUTDOWN low
Software standby	Two- wire serial communication with sensor is possible, pll is ready for fast return to streaming mode	Stream mode off PLL disable XSHUTDOWN high
Streaming	Sensor is fully powered and streaming image data on the MIPI CSI-2 bus	All Pad Enabled

7.2 Power on Sequence

Figure 15: Power on Timing

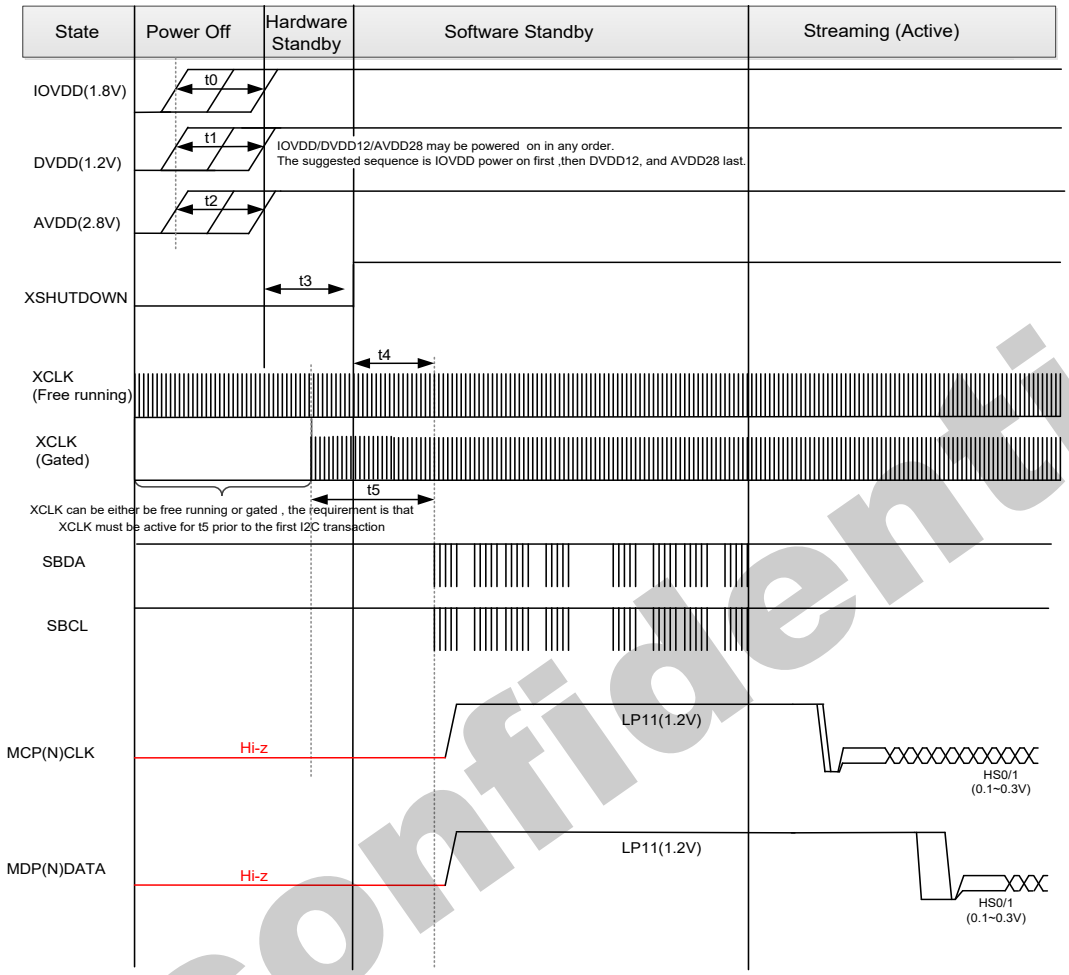


Table 13: Power on Timing

Parameter	Description	Min.	Max.	Unit
t0	IOVDD/DVDD12/AVDD28 may rise in any order. The rising separation can vary from 0μs to indefinite.	0	-	μs
t1				
t2				
t3	From power on to XSHUTDOWN pull high	0	-	μs
t4	XSHUTDOWN rising to first I2C transaction	50	-	μs
t5	Minimum No. of XCLK cycles prior to the first I2C transaction	1200	-	XCLK

Note: 1. IOVDD/DVDD12/AVDD28 may rise in any order.
2. The suggested sequence is IOVDD powered on first, then DVDD12, and AVDD28 last.
3. Register should be reloaded before works.

7.3 Power off Sequence

Figure 16: Power off Timing

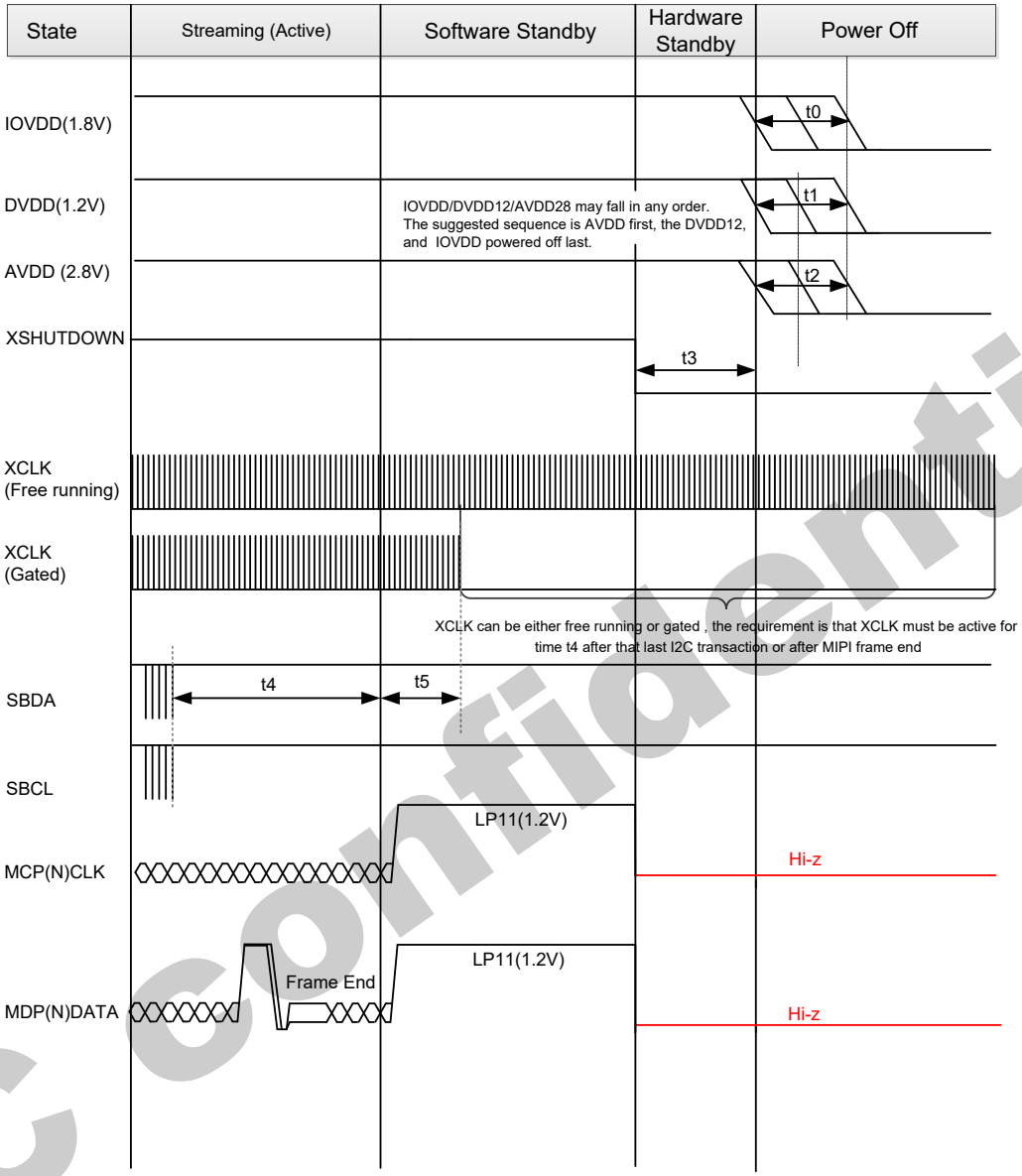


Table 14: Power off Timing

Parameter	Description	Min.	Max.	Unit
t0	IOVDD/DVDD12/AVDD28 may fall in any order. The fall separation can Vary from 0μs to indefinite.	0	-	μs
t1				
t2				
t3	From XSHUTDOWN pull down to power off	0		μs
t4	Enter Software Standby command – Device in Software Standby mode	0	-	μs
t5	Minimum number of XCLK cycles after the	2000		XCLK

	last transaction or MIPI frame end code.			

Note: 1. IOVDD/DVDD12/AVDD28 may fall in any order. The suggested sequence is AVDD first, the DVDD12, and IOVDD powered off last.
2. If the sensor’s power cannot be cut off, please keep power supply, then set XSHUTDOWN pin low. It will make sensor standby.
3. If the standby sequence needs to be modified, please contact FAE of *Galaxycore Inc*.

7.4 Black Level Calibration

Black level is caused by pixel characteristics and analog channel offset, which makes poor image quality in dark condition and color balance, to reduce these, sensor automatically calibrates the black level every frame with light shield pixel array.

7.5 Integration Time

The integration time is controlled by the shutter time registers. When you want to set an exposure value that is bigger than the current frame length value, you should first set a new frame length and make sure that it’s bigger than the exposure value you’d like to set.

Table 15: Shutter Time Register

Addr.	Register name	Description
0x0202	Shutter time	[5:0] shutter time[13:8]
0x0203		[7:0] shutter time[7:0]

7.6 Windowing

GC2607 has a rectangular pixel array 1920 x 1080, it can be windowed by output size control, the output image windowing can be used to adjust output size, and it will affect field angle.

Figure 17: Windowing Mode

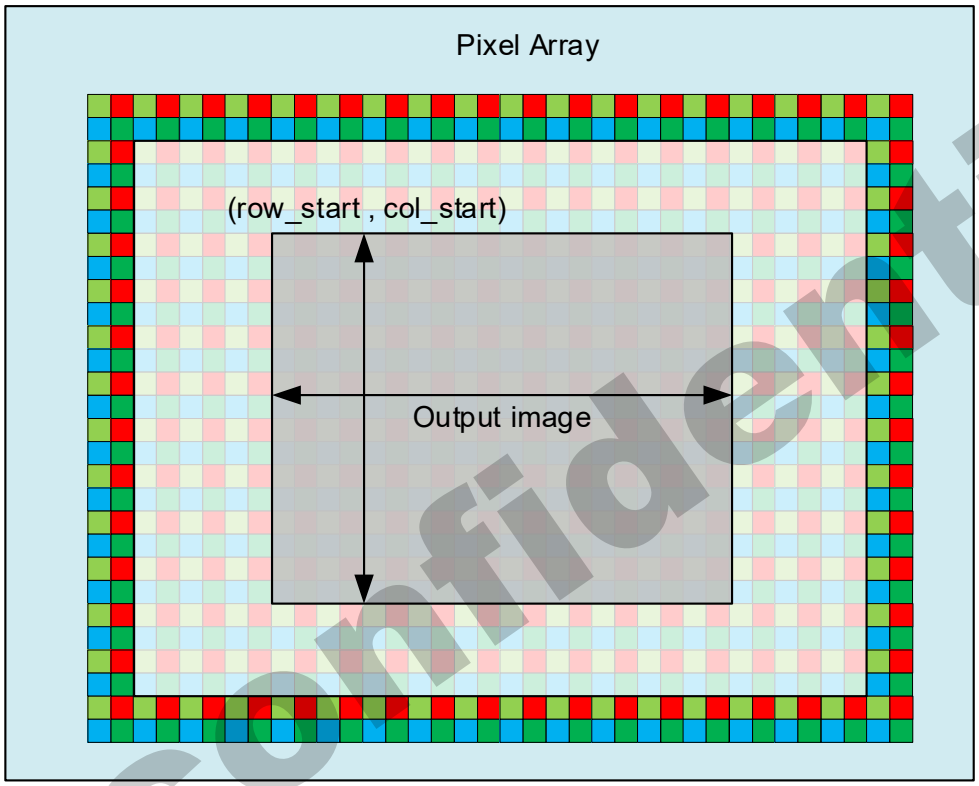


Table 16: Window Set Register

Addr.	Register name	Description
0x00c0	win_height	[2:0]win_height[10:8]
0x00c1		[7:0]win_height[7:0]
0x034a	win_width	[3:0]win_width[11:8]
0x034b		[7:0]win_width[7:0]
0x0346	Row start	[2:0]row_start[10:8]
0x0347		[7:0]row_start [7:0]

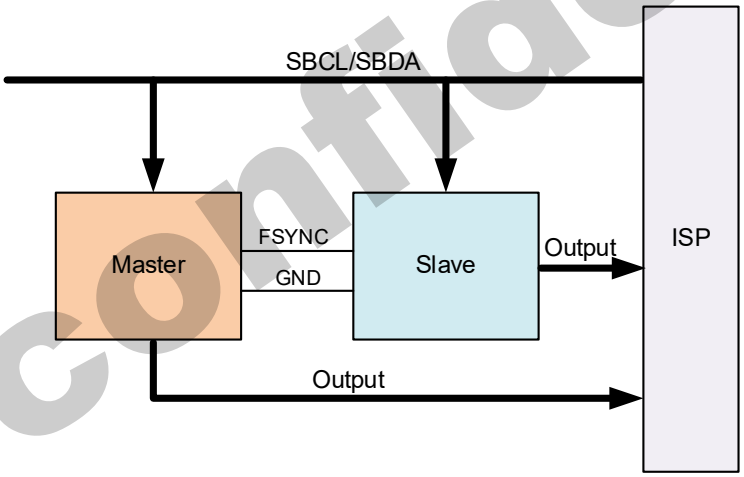
Table 17: Out Window Set Register

Addr.	Register name	Description
0x0353	out_win_x1	[3:0] out_win_x1[11:8]
0x0354		[7:0] out_win_x1[7:0]
0x021f	out_win_y1	[7:0] out_win_y1[3:0]
0x034c	out_win_width	[3:0] out_win_width[11:8]
0x034d		[7:0] out_win_width[7:0]

7.7 Frame Sync Mode

GC2607 can support hardware frame sync for dual camera application. It can be set both master and slave sensor. When use this mode, the two sensor’s FSYNC pin must connect to each other.

Figure 18: Frame Sync Configuration



Master Mode:

When GC2607 operates as a master device, it controls vertical synchronous timings and outputs synchronous signal called Vsync signal or Fsync signal from the FSYNC pin.

Slave Mode:

GC2607 can be worked as a slave and automatically synchronized within a certain VSYNC time period. It is important to control two image sensors’ rolling shutters with the same timing.

7.8 Binning Mode

GC2607 has Binning mode which support a lower resolution output with high frame rate. The row or col can be independent controlled. However, only the row binning can increase frame rate.

Table 18: Binning mode Register

Addr.	Register name	Description
0x0218	Row Binning	[7] Row Binning enable
0x005e	Col Binning	[0] Col Binning enable

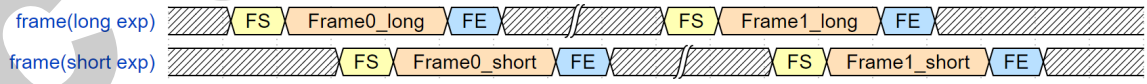
7.9 HDR mode

GC2607 has HDR function. If the function is enabled, by setting 2 different exposure times (always called long and short exposure), user can get 2 frame data in staggered output mode, and can combine two frames into one picture to improve dynamic range and avoid smearing.

When user choose MIPI protocol as output format, different exposure time line can be distinguished by virtual channel according to MIPI protocol. By default, long exposure line’ ID is 00, and short exposure line’s ID is 01.

The MIPI output timing as following (virtual channel mode):

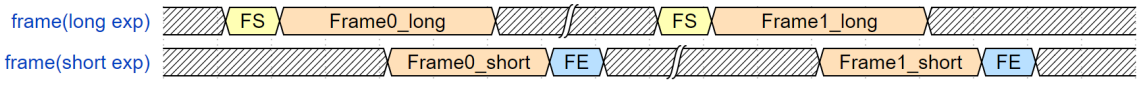
Figure 19: Virtual Channel Mode



Additionally, User can distinguish different exposure time line without virtual channel. In this mode, Short exposure time line has fixed offset lines with Long exposure time line.

The MIPI output timing as following (no virtual channel mode):

Figure 20: No Virtual Channel Mode



7.10 OTP memory

GC2607 sensor has 16K bits embedded OTP(One Time Programmable) memory and 11K bits for customer which is used for store module calibration date, etc.

7.11 Frame Structure

Frame structure is controlled by line length, frame length, window height, window width.

Frame length control:

Frame length is controlled by window height, and shutter time.

◆ Frame length depend shutter time.

- Minimum frame length = window height + 80
- If shutter time < minimum frame length: Actual frame length = minimum frame length
- If shutter time > minimum frame length: Actual frame length = shutter time + 16 (recommended).

Table 19: Frame Length Register

Addr.	Register name	Description
0x0340	Frame length	[7:0] frame length[15:8]
0x0341		[7:0] frame length[7:0]

Line length control:

Line length control for internal set, and not recommended to be modified.

Table 20: Line Length Register

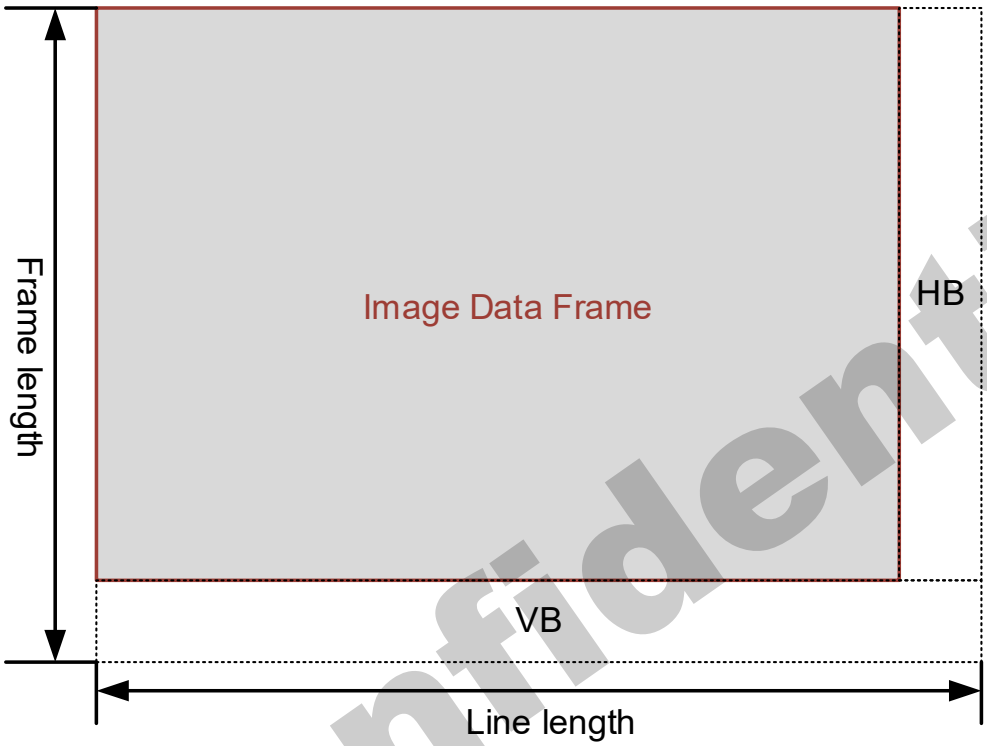
Addr.	Register name	Description
0x0342	Line length	[3:0] Line length[11:8]
0x0343		[7:0] Line length[7:0]

Blank time control:

Line blank time is controlled by line length.

Frame blank time = frame length – out window height

Figure 21: Frame Structure



8. Register List

System Register:

Address	Name	Default	R/W	Description
0x03f0	Sensor_ID_HIGH	0x26	RO	Sensor_ID
0x03f1	Sensor_ID_LOW	0x07	RO	Sensor_ID

Analog & CISCTL:

Address	Name	Default	R/W	Description
0x0202	Exposure time[14:8]	0x04	RW	[7] NA [6:0] exposure time[14:8]
0x0203	Exposure time [7:0]	0x48	RW	[7:0] exposure time[7:0]
0x0342	CISCTL_HB[13:8]	0x08	RW	CISCTL_HB
0x0343	CISCTL_HB [7:0]	0x00	RW	
0x0346	CISCTL_row_start[10:8]	0x00	RW	[7:3] reserved [2:0] Row Start[10:8]
0x0347	CISCTL_row_start [7:0]	0x02	RW	Row Start[7:0]
0x034a	CISCTL_ win_height[10:8]	0x04	RW	[7:3] NA [2:0] Window height[10:8]
0x034b	CISCTL_ win_height [7:0]	0x40	RW	[7:0] Window height
0x00c0	CISCTL_win_width [10:8]	0x07	RW	[7:3] NA [2:0] Window width[11:8]
0x00c1	CISCTL_win_width [7:0]	0x80	RW	[7:0] window width
0x0220	Framelength_RW	0x04	RW	[5:0]: framelength[13:8]
0x0221		0x37	RW	[7:0]: framelength[7:0]
0x0340	Framelength_RO	0x04	RW	Framelegth = frameledgth_RW+32
0x0341		0x57	RW	
0x0213	CISCTL_vs_st	0x10	RW	vs_st
0x0214	CISCTL_vs_et	0x04	RW	vs_et

CSI/PHY1.0

Address	Name	Default	R/W	Description
0x0d80	DPHY_Lane_en	0x00	RW	[2] dphy_clk_en [1] dphy_data1_en [0] dphy_data0_en
0x0d81	DPHY_mode	0x00	RW	[4]DATA lane gate [3:2]clane_data_mode [1:0]clklane_mode

0x0d82	MIPI_DPHY_Test	0x00	RW	[4] DoubleLane_en_DPHY [3] DPHY_read_en [2] dphy_clkX_enable [1] clklane off [0] mipi_test
0x0d83	LDI_set_IMG	0x08	RW	Default RAW10
0x0d84	LWC_set_manual_DPHY	0x04	RW	LWC_set_manual_DPHY[7:1]
0x0d85		0xb0	RW	
0x0d86	LANE_cnt_num_DPHY	0x04	RW	(LWC+2)/lane_num
0x0d87		0xb2	RW	
0x0db1	T_init_set	0x80	RW	
0x0db3	T_LPX_set	0x12	RW	
0x0db4	T_CLK_HS_PREPARE	0x0d	RW	
0x0db5	T_CLK_zero_set	0x4b	RW	
0x0db6	T_CLK_PRE_set	0x02	RW	
0x0db8	T_CLK_POST_set	0x16	RW	
0x0db9	T_CLK_TRAIL_set	0x0f	RW	
0x0dbb	T_HS_exit_set	0x10	RW	
0x0dbe	T_wakeup_set	0x80	RW	
0x0d91	T_init_set	0x80	RW	
0x0d93	T_LPX_set	0x12	RW	
0x0d94	T_HS_PREPARE_set	0x0d	RW	
0x0d95	T_HS_Zero_set	0x11	RW	
0x0d99	T_HS_TRAIL_set	0x10	RW	
0x0d9b	T_HS_exit_set	0x10	RW	
0x0da9	T_HS_ULP_set	0x12	RW	
0x0dae	T_wakeup_set	0x80	RW	

OUT

Address	Name	Default	R/W	Description
0x008c	Test image	0x10	RW	[2] input test image
0x021f	out_win_y1[3:0]	0x00	RW	Out_win_y1 [7:4]NA [3:0] out_win_y1[3:0]
0x0353	out_win_x1[11:8]	0x00	RW	Out_win_y1 [7:4]NA [3:0]out_win_x1[11:8]
0x0354	Out_win_x1[7:0]	0x00	RW	Out_win_y1 [7:0]out_win_x1[7:0]

0x034c	Out_win_width[11:8]	0x07	RW	[7:4]NA [3:0]out_win_width[11:8]
0x034d	Out_win_width[7:0]	0x80	RW	Out_win_width[7:0] must be 8X when raw10
0x021f	Out_win_offset_updown	0x00	RW	for auto_updown[4] out_offset_y1=2
0x0087	Out_win_offset_mirror	0x00	RW	for auto_mirror[0] out_offset_x1=2

OB OFFSET

Address	Name	Default	R/W	Description
0x0070	WB_offset_G1	0x40	RW	WB_offset_G1
0x0071	WB_offset_R1	0x40	RW	WB_offset_R1
0x0072	WB_offset_B1	0x40	RW	WB_offset_B1
0x0073	WB_offset_G2	0x40	RW	WB_offset_G2

Gain

Address	Name	Default	R/W	Description
0x0208	auto_pregain_sync[13:8]	0x04	RW	[7:6] NA [5:0] Auto_pregain[13:8]
0x0209	auto_pregain[7:0]	0x00	RW	[7:0] Auto_pregain[7:0]
0x02b3	Analog_PGA_gain[15:8]	0x00	RW	analog_gain
0x02b4	Analog_PGA_gain[7:0]	0x00	RW	
0x020c	Col_gain[11:8]	0x00	RW	[7:4]NA [3:0]col_gain[11:8]
0x020d	Col_gain[7:0]	0x00	RW	[7:0]col_gain[7:0]
0x009e	Global gain[11:8]	0x04	RW	[3:0] global_gain[11:8]
0x009f	Global gain[7:0]	0x00	RW	[7:0] global_gain[7:0]

HDR

Address	Name	Default	R/W	Description
0x0202	Exposure time_T1[14:8]	0x04	RW	[7] NA [6:0] exposure time_T1[14:8]
0x0203	Exposure time_T1[7:0]	0x48	RW	[7:0] exposure time_T1[7:0]
0x0240	Exposure time_T2[14:8]	0x04	RW	[7] NA [6:0] exposure time_T2[14:8]
0x0241	Exposure time_T2 [7:0]	0x48	RW	[7:0] exposure time_T2[7:0]
0x020c	Col_gain_T1[11:8]	0x00	RW	[7:4]NA [3:0]col_gain_T1[11:8]

0x020d	Col_gain_T1[7:0]	0x40	RW	[7:0]col_gain_T1[7:0]
0x020e	Col_gain_T2[11:8]	0x00	RW	[7:4]NA [3:0]col_gain_T2[11:8]
0x020f	Col_gain_T2[7:0]	0x40	RW	[7:0]col_gain_T2[7:0]
0x0208	auto_pregain_T1[13:8]	0x04	RW	[7:6] NA [5:0] Auto_pregain_T1[13:8]
0x0209	auto_pregain_T1[7:0]	0x00	RW	[7:0] Auto_pregain_T1[7:0]
0x020a	auto_pregain_T2[13:8]	0x04	RW	[7:6] NA [5:0] Auto_pregain_T2[13:8]
0x020b	auto_pregain_T2[7:0]	0x00	RW	[7:0] Auto_pregain_T2[7:0]
0x02b3	Analog_PGA_gain_T1[15:8]	0x00	RW	analog_gain_T1
0x02b4	Analog_PGA_gain_T1[7:0]	0x00	RW	
0x02b5	Analog_PGA_gain_T2[15:8]	0x00	RW	analog_gain_T2
0x02b6	Analog_PGA_gain_T2[7:0]	0x00	RW	
0x0218	HDR enable	0x00	RW	[4] HDR enable
0x0107	Virtual Channal	0x00	RW	[1] Virtual Channal
0x0242	exp2_position[10:8]	0x00	RW	[7:3] NA [2:0] exp2_position[10:8]
0x0243	exp2_position[7:0]	0x40	RW	[7:0] exp2_position[7:0]