GC5035 CSP

1/5” 5Mega CMOS Image Sensor

Datasheet

V1.2

2019-11-06

Ordering Information

◆ **GC5035-C31Y0**

(Colored, 31 PIN - CSP)

GENERATION REVISION HISTORY

REV.	EFFECTIVE DATE	DESCRIPTION OF CHANGES	AUTHOR
V1.0	2018-10-24	Document Release	Teddy Yin
V1.1	2019-09-26	Modify first pixel & dual sync explanation	Teddy Yin
V1.2	2019-11-06	Modify power on/off sequence	Teddy Yin

Galaxycore Incorporation

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Content

1. Sensor Overview

1.1 General Description

GC5035 is a high quality 5Mega CMOS image sensor, for mobile phone camera applications and digital camera products. GC5035 incorporates a 2592H x 1944V pixel array, on-chip 10-bit ADC, and image signal processor.

The full-scale integration of high-performance and low-power functions makes the GC5035 fit the design, reduce implementation process, and extend the battery life of cell phones, PDAs, and a wide variety of mobile applications.

It provides RAW10 and RAW8 data formats with MIPI interface. It has a commonly used two-wire serial interface for host to control the operation of the whole sensor.

1.2 Features

- Optical format : 1/5 inch
- Pixel size : 1.12μmx1.12μm BSI
- Output formats : Raw Bayer 10bit/8bit
- Power supply requirement : 2.70~3.00V for AVDD28 (typical 2.80V)
  : 1.15~1.30V for DVDD12 (typical 1.20V)
  : 1.70~3.00V for IOVDD (typical 1.80V)
- OTP support (4K for customers) : Module information/WB
- Package : CSP
- PLL support
- Binning mode support
- MIPI(2_lane) interface support
- Horizontal/Vertical mirror
- Image processing module

1.3 Application

- Cellular Phone Cameras
- Notebook and desktop PC cameras
- PDAs
- Toys
- Digital still cameras and camcorders
- Video telephony and conferencing equipment

1.4 Technical Specifications

Parameter	Typical value
Optical Format	1/5 inch
Pixel Size	1.12μm x 1.12μm(BSI)
Active pixel array	2592 x 1944
Shutter type	Electronic rolling shutter
ADC resolution	10-bit ADC
Max Frame rate	30fps@full size 876Mbps/lane
Power Supply	AVDD28: 2.8 V DVDD: 1.2V IOVDD: 1.8V
Power Consumption	100mW
SNR	37dB
Dark Current	3e-/s(60℃)
Sensitivity	2368 e-/lux*s
Dynamic range	64.7dB
Operating temperature:	-20 ~ 70℃
Stable Image temperature	0~60℃
Max Optimal lens chief ray angle(CRA)	31.90°(non-linear)
Package type	CSP
D-PHY version	V1.1

2. DC Characteristics

2.1 Standby Current

Item	Symbol	Min	Typ	Max	Unit
Analog	I_{AVDD}	—	10	100	μA
Digital	I_{DVDD}	—	500	5000	μA
I/O	I_{IOVDD}	—	20	300	μA

RST: L, PWDN: L

Typ. Analog: 2.8V, Digital: 1.2V, I/O:1.8V, T_j=25℃

2.2 Power off Current

Item	Symbol	Min	Typ	Max	Unit
Analog	I_{AVDD}	—	0	0	μA
Digital	I_{DVDD}	—	0	0	μA
I/O	I_{IOVDD}	—	0	0	μA

Power off, T_j=25℃

2.3 Operation Current

Full size (MIPI 2 lane @876Mbps/Lane)

Item	Symbol	Min	Typ	Max	Unit
Analog	I_{AVDD}	—	12.5	35	mA
Digital	I_{DVDD}	—	45	80	mA
I/O	I_{IOVDD}	—	1.8	3	mA

INCLK: 24MHz, Frame rate: 30fps, Raw 10

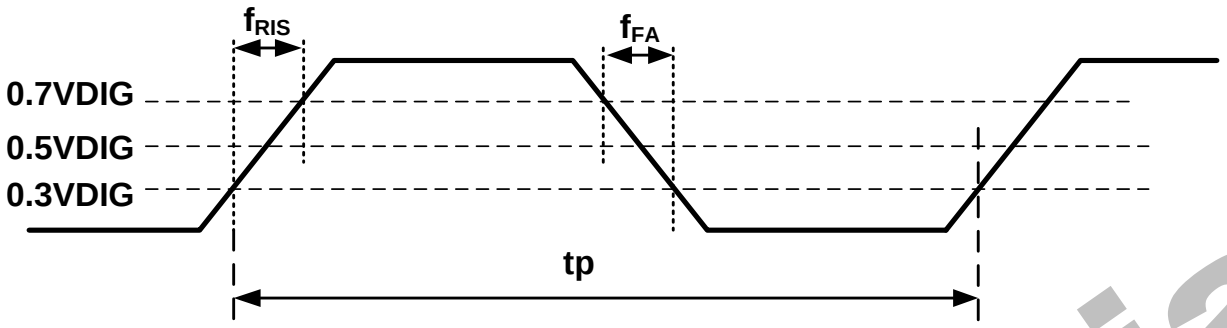
Typ. Analog: 2.8V, Digital: 1.2V, I/O:1.8V, T_j=25℃

2.4 DC Characteristics

Item	Symbol	Min	Typ	Max	Unit
Power supply	V_{AVDD}	2.7	2.8	3.0	V
	V_{DVDD}	1.15	1.2	1.3	V
	V_{IOVDD}	1.7	1.8	3.0	V
Digital Input (Conditions: AVDD = 2.8V, DVDD = 1.2V, IOVDD = 1.8V)					
Input voltage HIGH	**V_{IH}**	0.7*VIF	-		V
Input voltage LOW	**V_{IL}**		-	0.3*VIF	V
Input leakage current	**I_{IL}**	-10	-	10	μA
Digital Output (Conditions: AVDD = 2.8V, IOVDD = 1.8V, standard Loading 25PF)					
Output voltage HIGH	**V_{OH}**	0.8*VIF	-		V
Output voltage LOW	**V_{OL}**		-	0.2*VIF	V
High-Z output leakage current	**I_{OZ}**	-10	-	10	μA

3. AC Characteristics

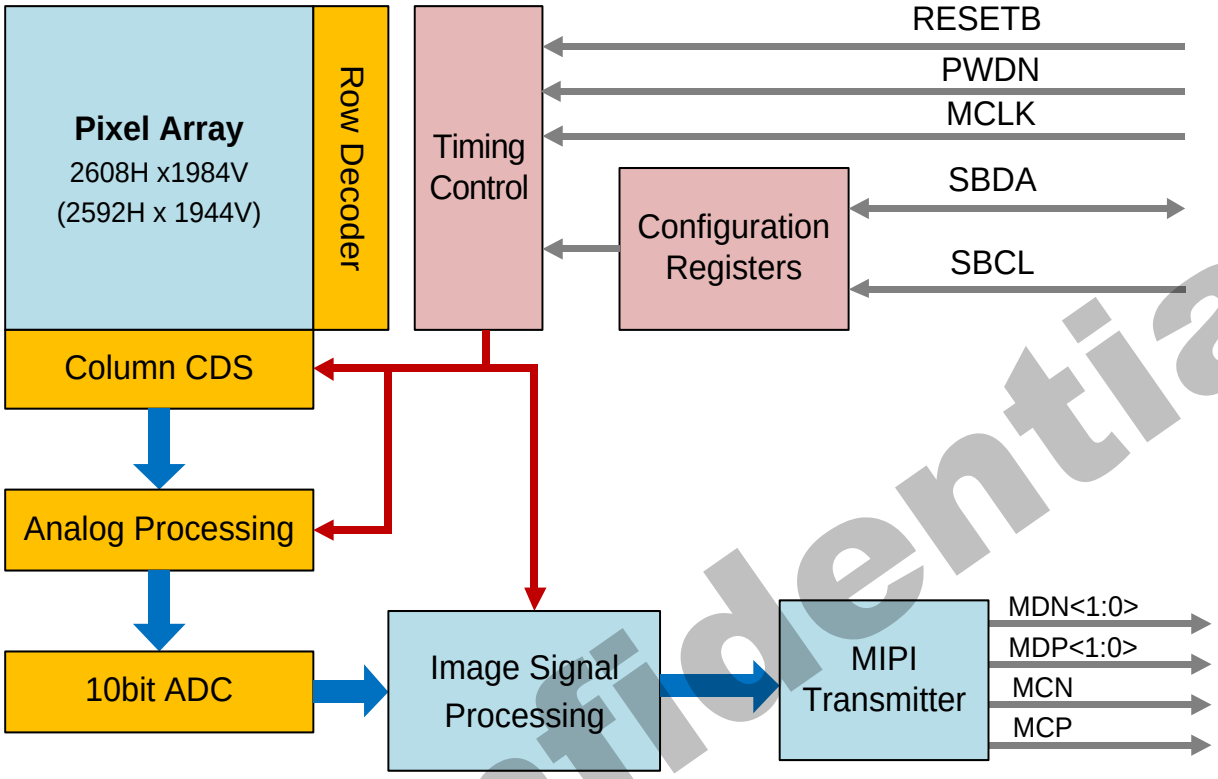
Master clock wave diagram



Input clock square waveform specifications：

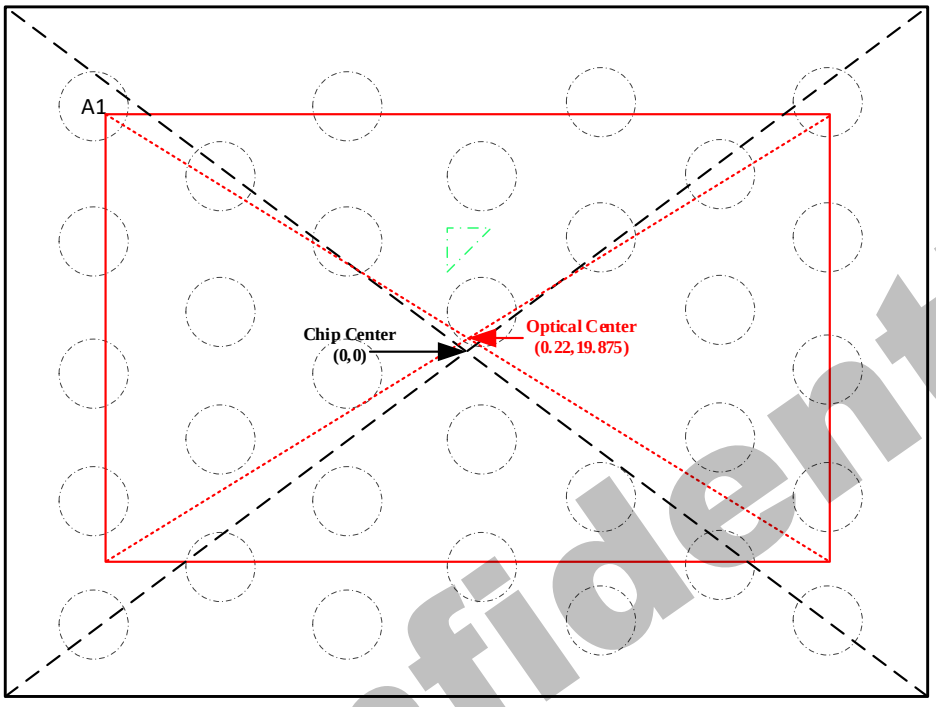
Item	Symbol	Min.	Typ.	max	unit
Frequency	f_{SCK}	6	24	27	MHz
jitter (period, peak-to-peak)	T_{jitter}			600	ps
Rise Time	f_{RISE}			15	ns
Fall Time	f_{FALL}			15	ns
Duty Cycle	f_{DUTY}	40		60	%

4. Block Diagram

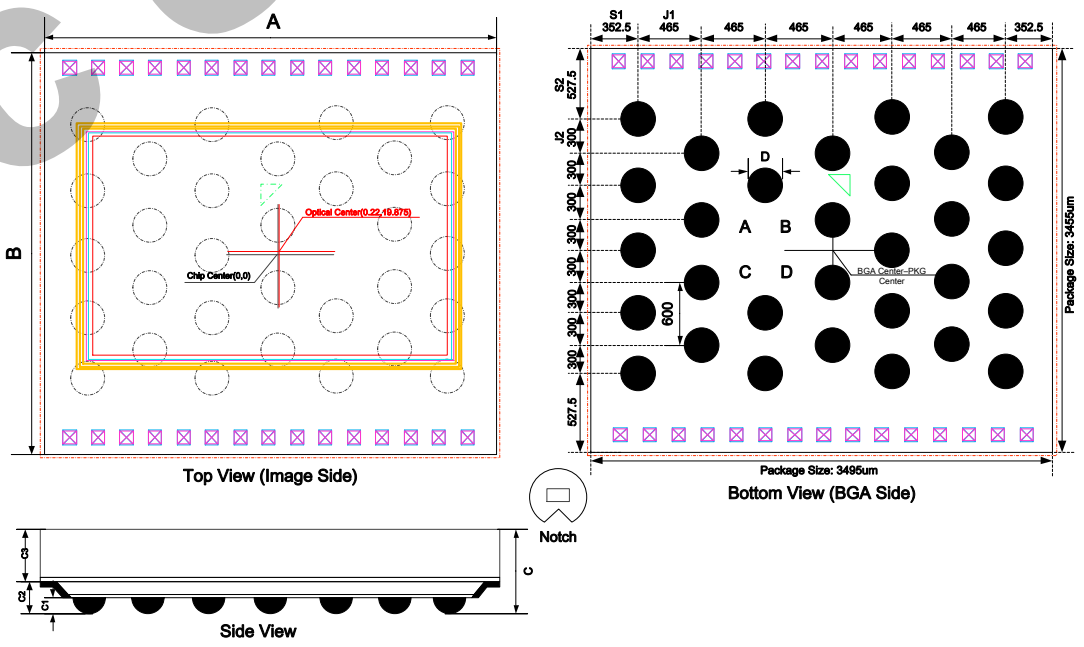


5. Chip Information

5.1 Optical center

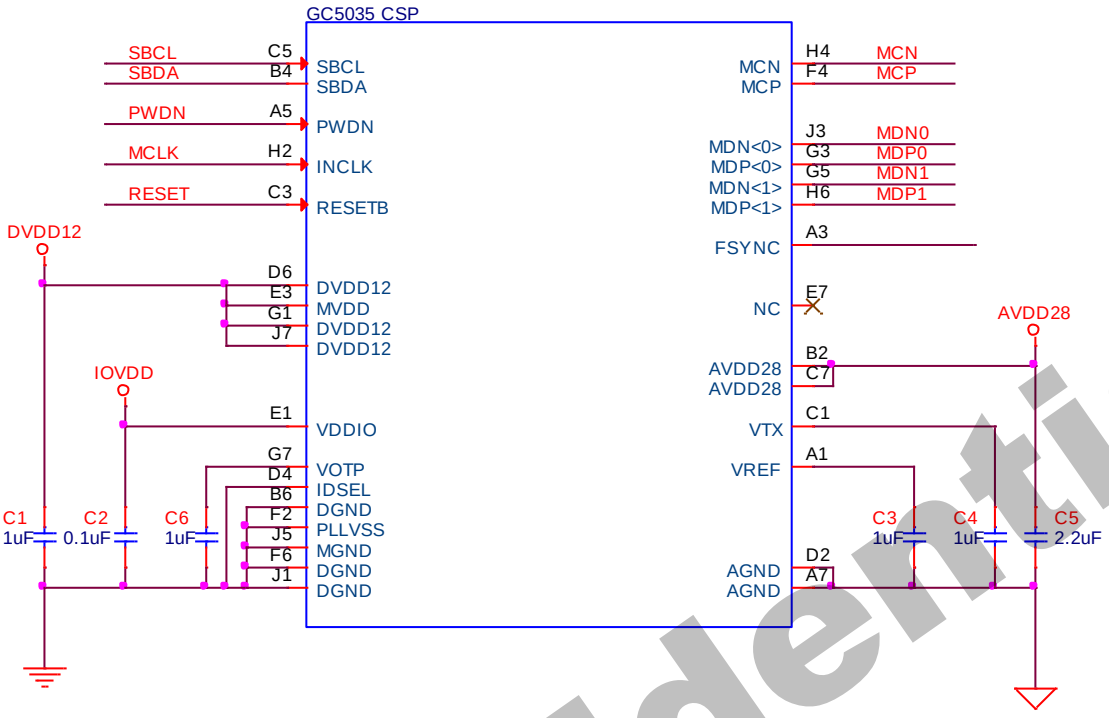


5.2 Package Specifications

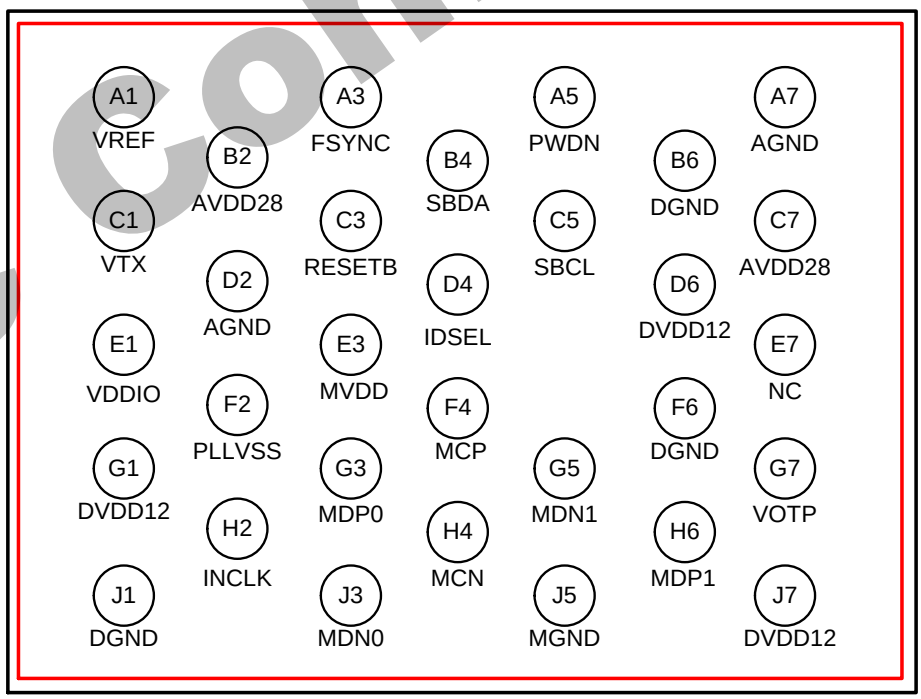


Description	Symbol	Nominal	Min.	Max.
		Millimeters		
Package Body Dimension X	A	3.495	3.470	3.520
Package Body Dimension Y	B	3.455	3.430	3.480
Package Height	C	0.600	0.545	0.655
Ball Height	C1	0.120	0.090	0.150
Thickness from ball to wafer surface	C2	0.255	0.180	0.330
Thickness from top glass surface to wafer surface	C3	0.345	0.325	0.365
Ball Diameter	D	0.230	0.200	0.260
Total Ball Count	N	31(1 NC)		
Ball Count X axis	N1	7		
Ball Count Y axis	N2	9		
Pins Pitch X axis	J1	0.465		
Pins Pitch Y axis	J2	0.300		
BGA ball center to package center offset in X-direction	X	0.0000	-0.025	0.025
BGA ball center to package center offset in Y-direction	Y	0.0000	-0.025	0.025
BGA ball center to chip center offset in X direction	X1	0.0000	-0.025	0.025
BGA ball center to chip center offset in Y direction	Y1	0.0000	-0.025	0.025
Edge to Pin Center Distance along X	S1	0.3525	0.3225	0.3825
Edge to Pin Center Distance along Y	S2	0.5275	0.4975	0.5575

5.3 Peripheral Circuit Diagram



5.4 Pin Coordinates and Description



Top View (See through)

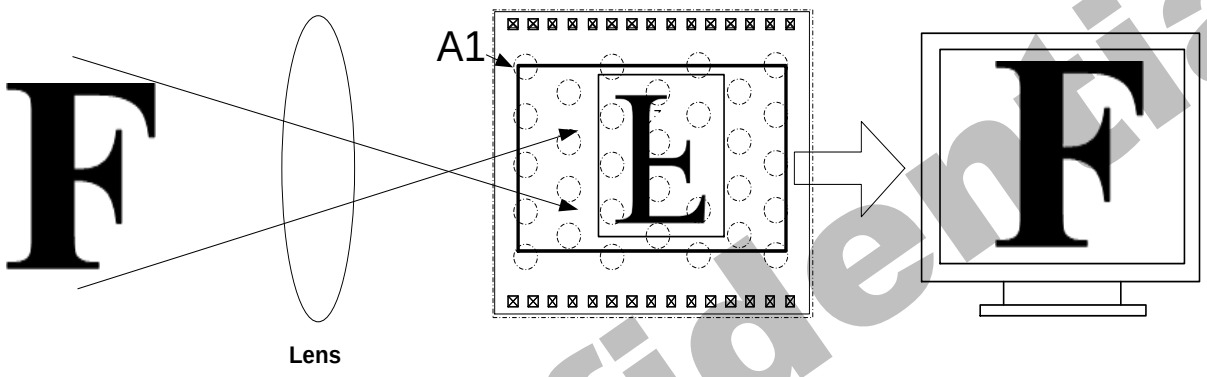
Pin	Name	Pin Type	Description
A1	VREF	POWER	Internal power supply, please connect capacitor to analog ground.
A3	FSYNC (strobe)	I/O	Frame sync control / Strobe control
A5	PWDN	Input	Sensor power down control: 0: standby 1: normal work
A7	AGND	Ground	Ground for analog
B2	AVDD28	POWER	Main power supply pin:2.7~3.0V, please connect capacitor to digital ground
B4	SBDA	I/O	I2C Data
B6	DGND	Ground	Ground for digital
C1	VTX	POWER	Internal power supply, please connect capacitor to analog ground.
C3	RESETB	Input	Chip reset control: 0: chip reset 1: normal work
C5	SBCL	Input	I2C Data
C7	AVDD28	POWER	Main power supply pin:2.7~3.0V, please connect 2.2μF capacitor to digital ground
D2	AGND	Ground	Ground for analog
D4	IDSEL	Input	Sensor I2C address ID select ***0: 0x6e/0x6f (default)*** 1: 0x7e/0x7f
D6	DVDD12	Power	Digital power supply pin: 1.15~1.3V, please connect capacitor to digital ground.
E1	VDDIO	POWER	Power supply for I/O circuits: 1.7~3.0V, please connect capacitor to digital ground.
E3	MVDD	Power	Digital power supply pin: 1.15~1.3V， please connect capacitor to digital ground.
E7	NC		
F2	PLLVSS	Ground	Ground for PLL
F4	MCP	Output	MIPI clock (+)
F6	DGND	Ground	Ground for digital
G1	DVDD12	Power	Digital power supply pin: 1.15~1.3V, please connect capacitor to digital ground.
G3	MDP0	Output	MIPI data <0> (+)
G5	MDN1	Output	MIPI data <1> (-)
G7	VOTP	POWER	For OTP power supply Please connect capacitor to digital ground.
H2	INCLK	Input	Sensor input clock

H4	MCN	Output	MIPI clock (-)
H6	MDP1	Output	MIPI data <1> (+)
J1	DGND	Ground	Ground for digital
J3	MDN0	Output	MIPI data <0> (-)
J5	MGND	Ground	Ground for MIPI
J7	DVDD12	Power	Digital power supply pin: 1.15~1.3V, please connect capacitor to digital ground.

6. Optical Specifications

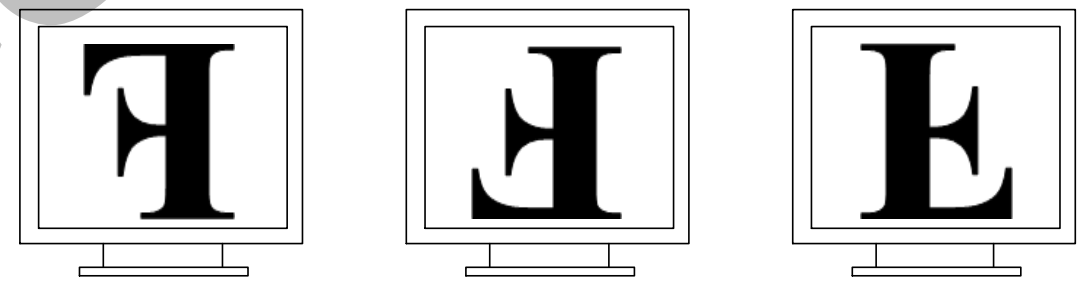
6.1 Readout Position

In default status, the first pixel to read out of GC5035 is located at the lower left corner. The image is inverted vertically and horizontally by the lens, which results in a mirrored image output.



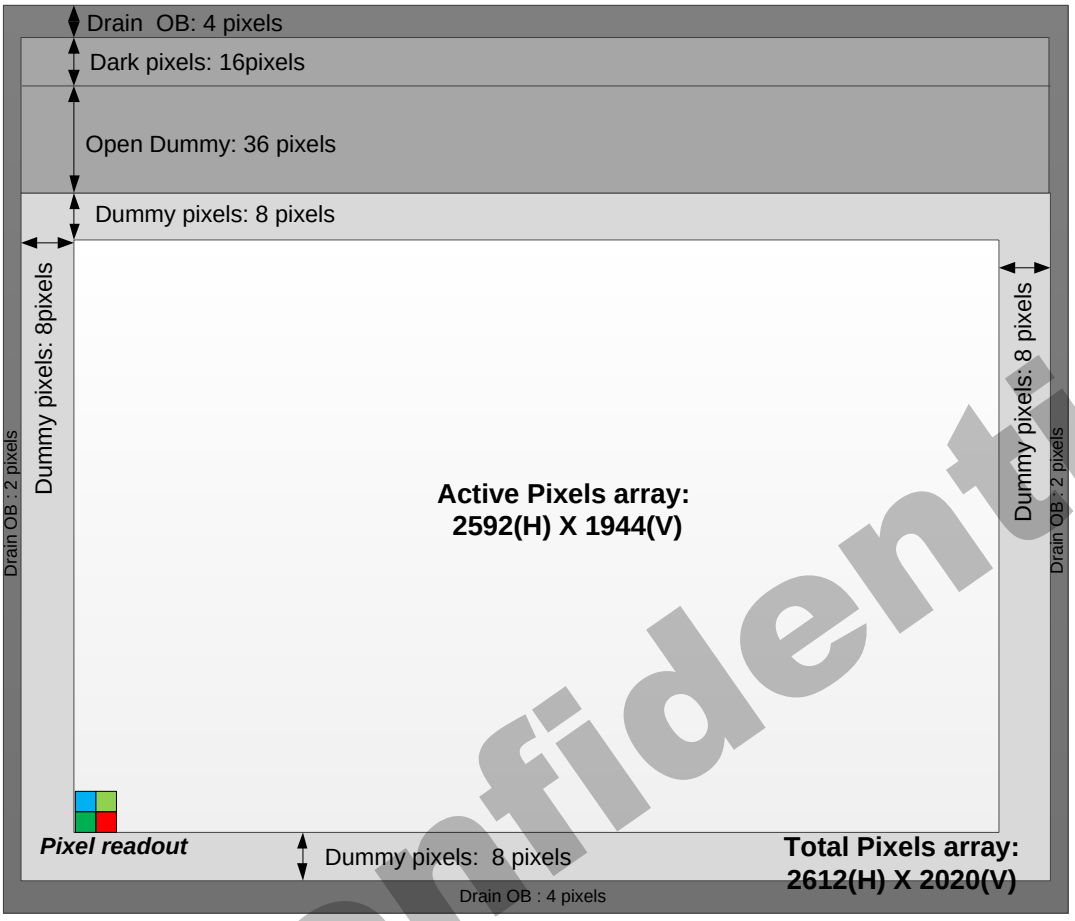
Readout direction can be set by the registers.

Function	Register Address	Register Value	First Pixel
Normal	P0:0x17[1:0]	00	R
Horizontal mirror	P0:0x17[1:0]	01	Gr
Vertical Flip	P0:0x17[1:0]	10	Gb
Horizontal Mirror and Vertical Flip	P0:0x17[1:0]	11	B



Horizontal Mirror Horizontal Mirror and Vertical Flip Vertical Flip

6.2 Pixel Array



Pixel array is covered by Bayer pattern color filters. The primary color BG/GR array is arranged in line-alternating way.

If no flip in column, column is read out from 0 to 2591. If flip in column, column is read out from 2591 to 0.

If no flip in row, row is read out from 0 to 1943. If flip in row, row is read out from 1943 to 0.

- *Notice: The first out pixel depends on col start setting. In current set file, first out pixel is R.*

6.3 Lens Chief Ray Angle (CRA)

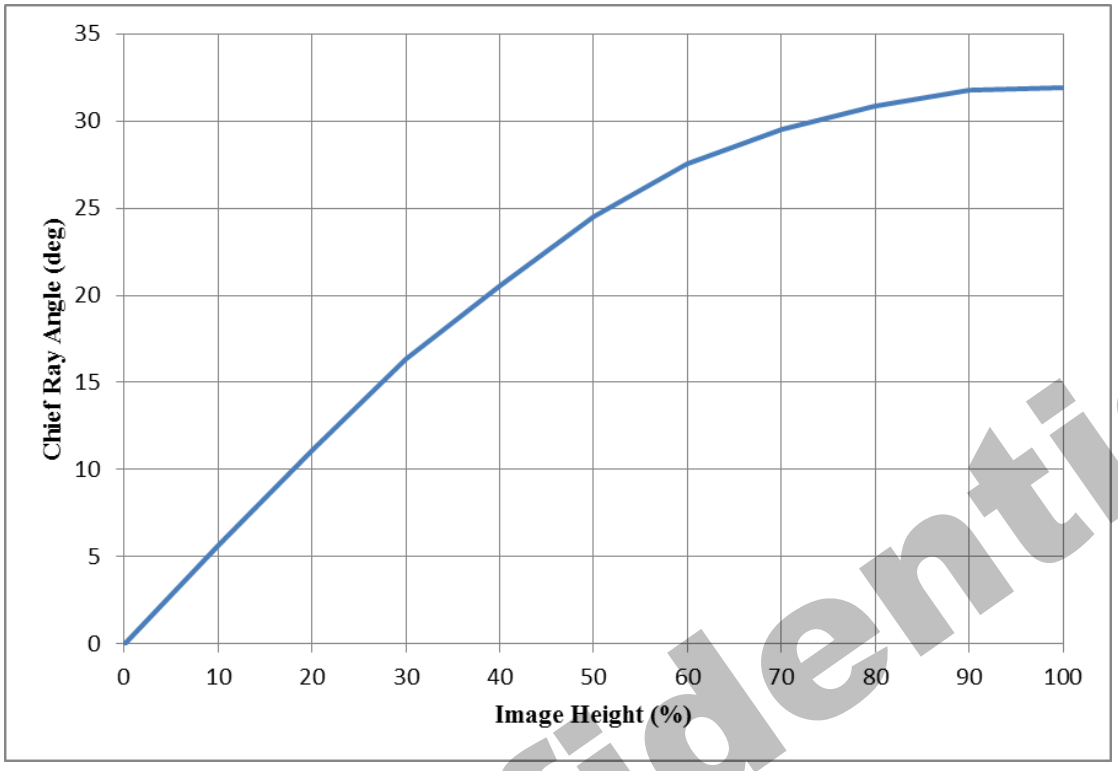
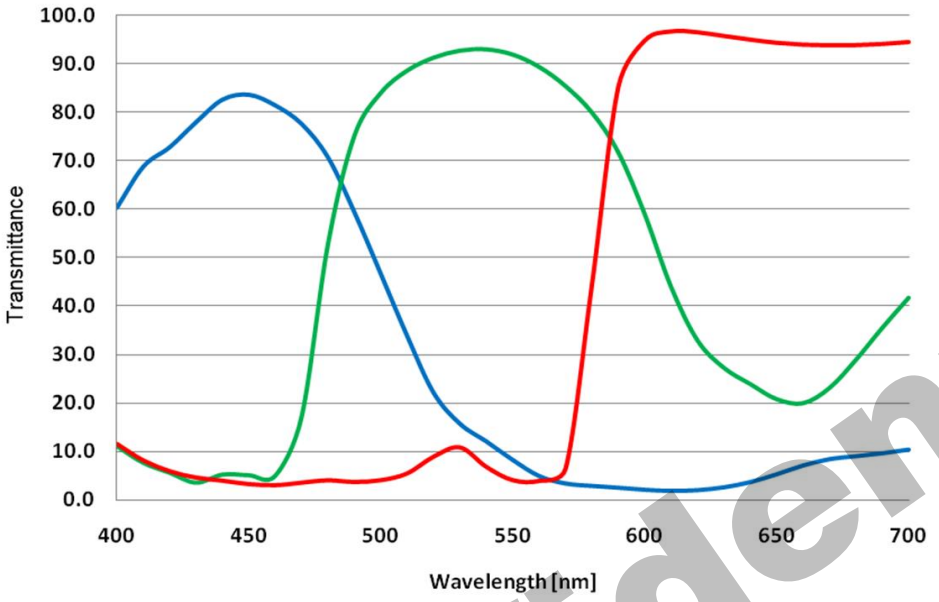


Image Height (%)	Image Height (mm)	CRA (degree)
00	0.000	0.00
10	0.181	5.65
20	0.363	11.09
30	0.544	16.32
40	0.726	20.59
50	0.907	24.53
60	1.088	27.54
70	1.270	29.53
80	1.451	30.87
90	1.633	31.80
100	1.814	31.90

6.4 Color Filter Spectral Characteristics

The optical spectrum of color filters is shown below:



7. Two-wire Serial Bus Communication

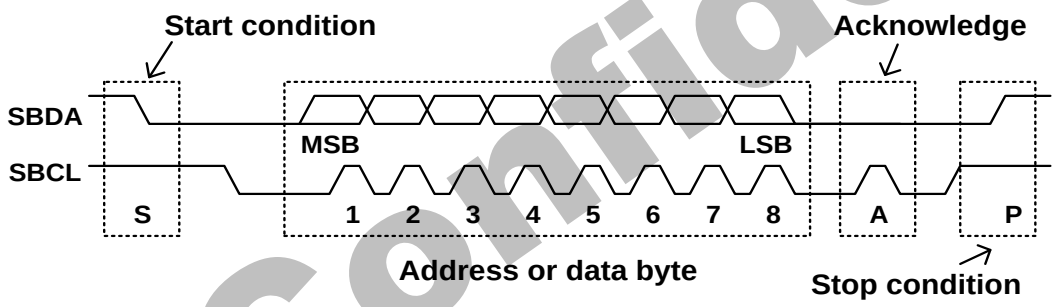
GC5035 Device Address:

IDSEL	Slave address write mode	Slave address read mode
0(default)	0x6e	0x6f
1	0x7e	0x7f

7.1 Protocol

The host must play the role of a communication master and GC5035 acts as either a slave receiver or transmitter. The master must do

- Generate the **Start(S)/Stop(P)** condition
- Provide the serial clock on **SBCL.**



Single Register Writing:

S	6EH	A	Register Address	A	Data	A	P

Incremental Register Writing:

S	6EH	A	Register Address	A	Data(1)	A	.....	Data(N)	A	P

Single Register Reading:

S	6EH	A	Register Address	A	S	6FH	A	Data	NA	P

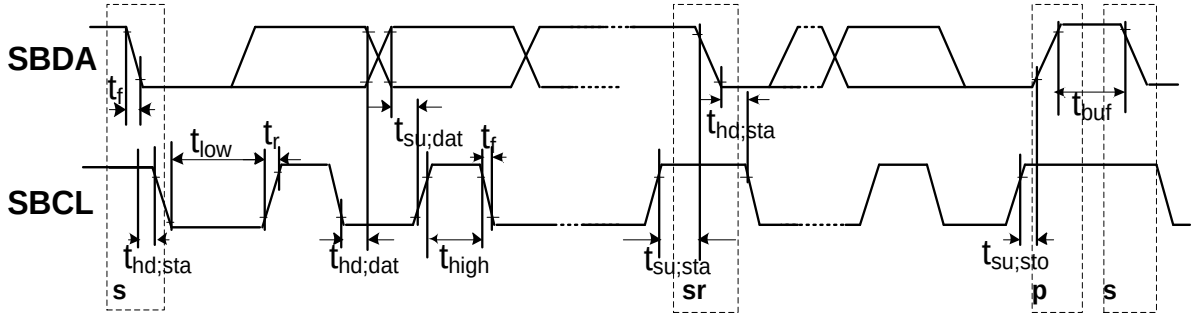
S: Start condition **P:** Stop condition

A: Acknowledge bit **NA:** No acknowledge

Register Address: Sensor Register Address

Data: Sensor Register Value

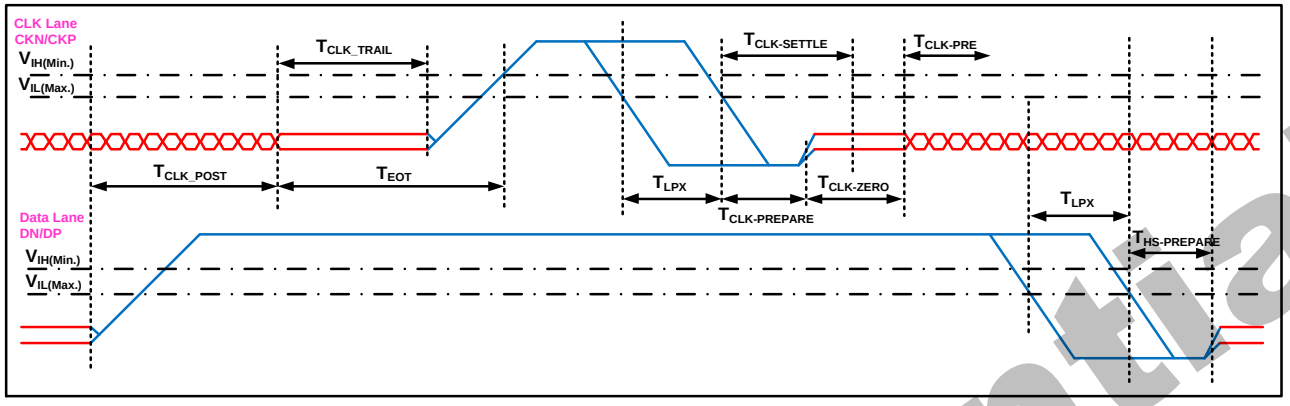
7.2 Serial Bus Timing



Parameter	Symbol	Min.	Typ.	Max.	Unit
SBCL clock frequency	F_{scl}	0	--	400	KHz
Bus free time between a stop and a start	t_{buf}	1.3	--	--	μs
Hold time for a repeated start	$t_{hd;sta}$	0.6	--	--	μs
LOW period of SBCL	t_{low}	1.3	--	--	μs
HIGH period of SBCL	t_{high}	0.6	--	--	μs
Set-up time for a repeated start	$t_{su;sta}$	600	--	--	ns
Data hold time	$t_{hd;dat}$	0	--	900	ns
Data Set-up time	$t_{su;dat}$	100	--	--	ns
Rise time of SBCL, SBDA	t_r	--	--	300	ns
Fall time of SBCL, SBDA	t_f	--	--	300	ns
Set-up time for a stop	$t_{su;sto}$	0.6	--	--	μs
Capacitive load of bus line (SBCL, SBDA)	C_b	--	--	--	pf

8. Applications

8.1 Clock lane low-power



Notice:

- Clock must be reliable during high speed transmission and mode-switching.
- Clock can go to LP only if data lanes are in LP (and nothing relies on it).
- In Low-Power data lanes are conceptually asynchronous (independent of the high speed clock).

$T_{CLK\_HS\_PREPARE}$: setting by Register P3: 0x22

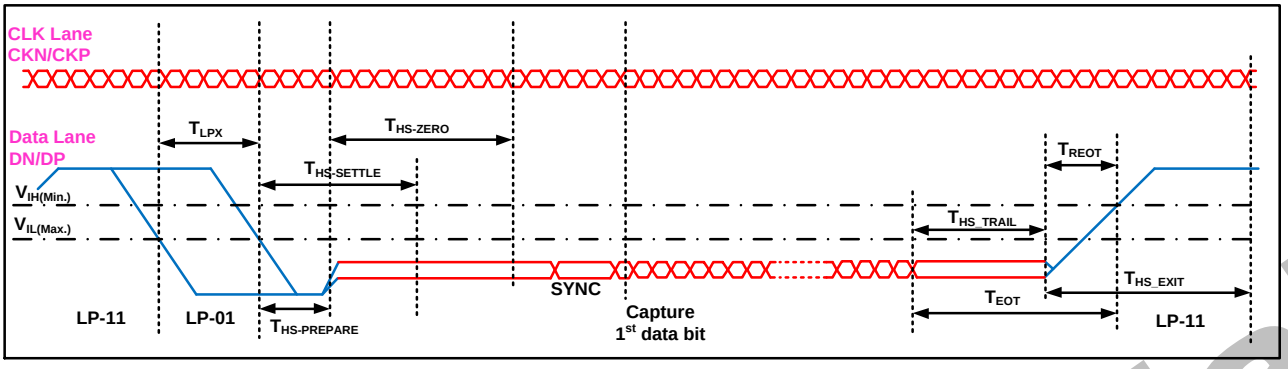
T_{CLK_ZERO} : setting by Register P3: 0x23

T_{CLK_PRE} : setting by Register P3: 0x24

T_{CLK_POST} : setting by Register P3: 0x25

T_{CLK_TRAIL} : setting by Register P3: 0x26

8.2 Data Burst



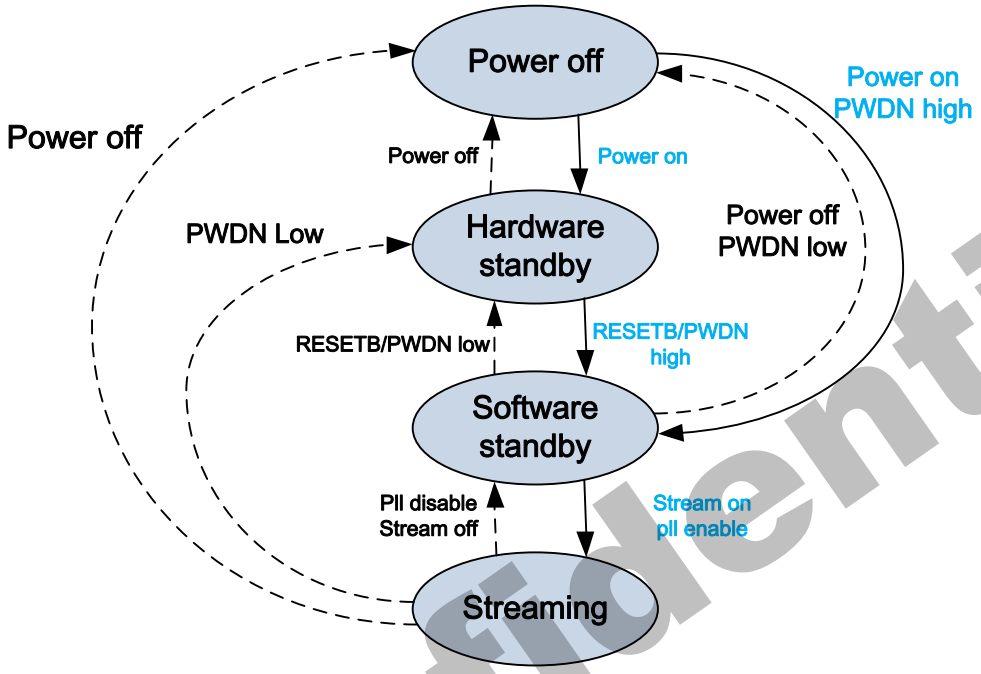
Notice:

- Clock keeps running and samples data lanes (except for lanes in LPS).
- Unambiguous leader and trailer sequences required to distill real bits.
- Trailer is removed inside PHY (a few bytes).
- Time-out to ignore line values during line state transition.

T_{LPX}	: setting by Register P3: 0x21
$T_{HS\_PREPARE}$	: setting by Register P3: 0x29
T_{HS_ZERO}	: setting by Register P3: 0x2a
T_{HS_TRAIL}	: setting by Register P3: 0x2b
T_{HS_EXIT}	: setting by Register P3: 0x27

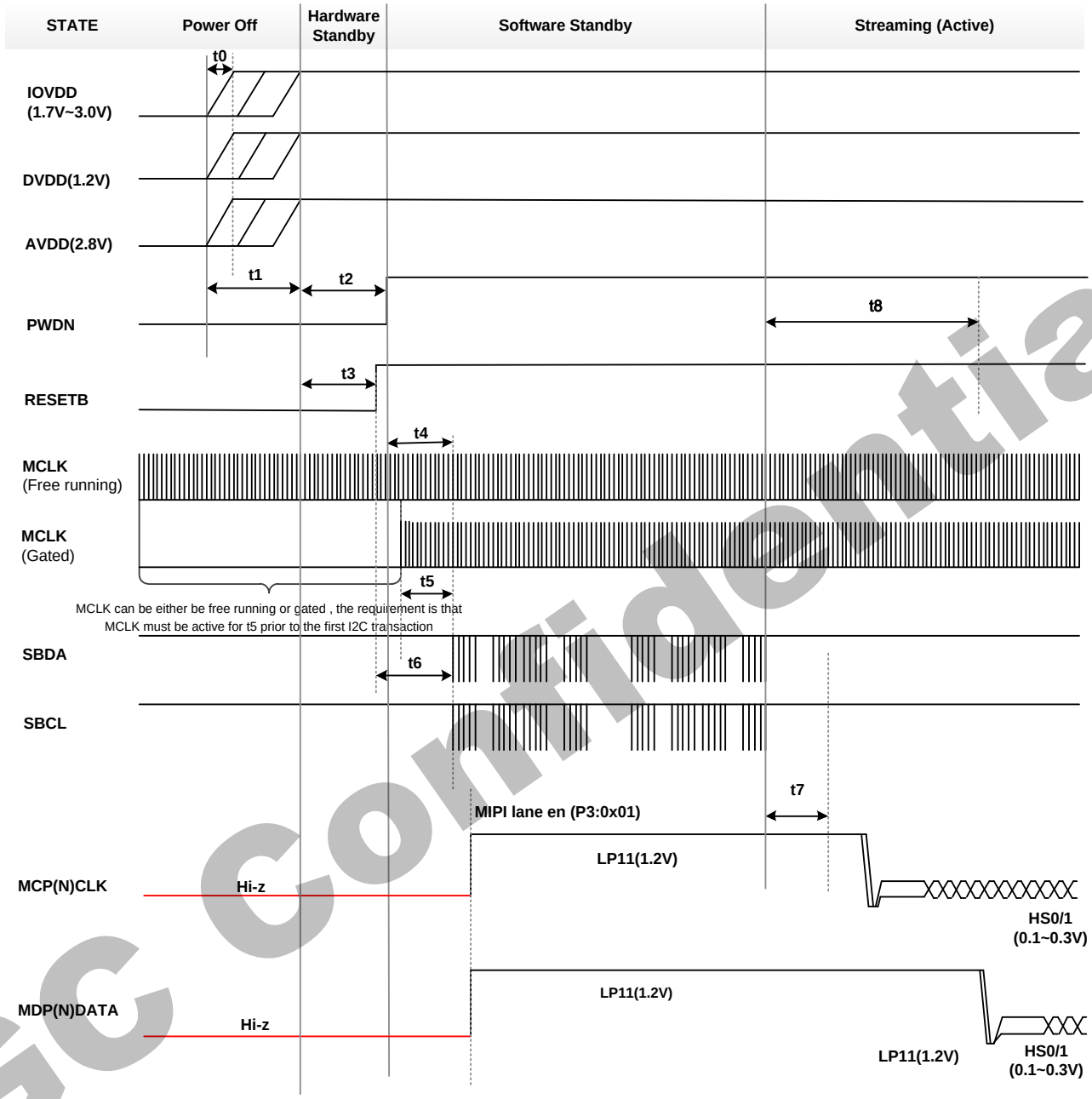
9. Function description

9.1 Operation mode



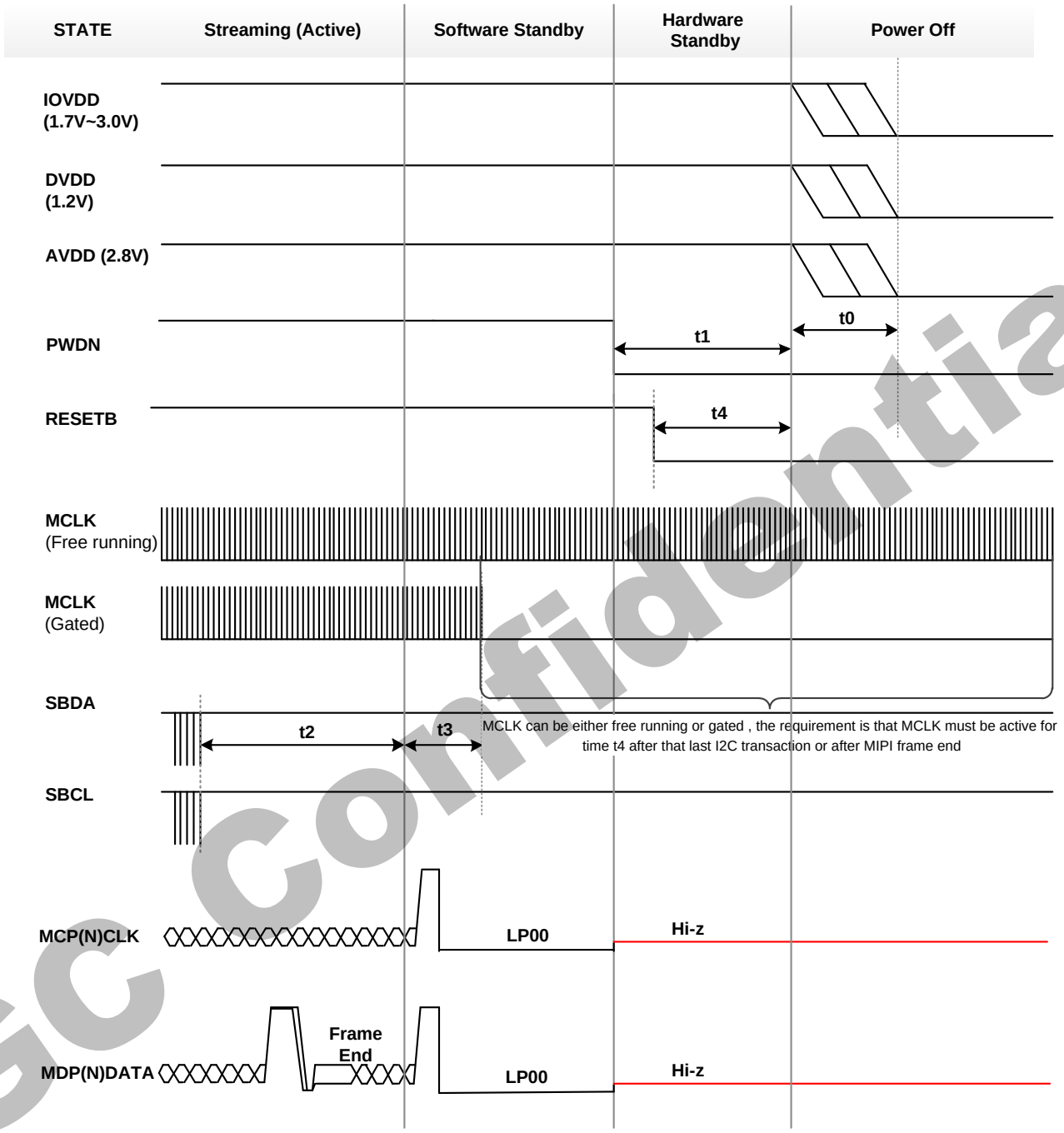
Power state	Description	Activate
Power off	Power supplies are turned off	None
Hardware standby	No communication with sensor, low level on PWDN and RESETB, and stop MCLK	PWDN low
Software standby	Two- wire serial communication with sensor, pll is ready for fast return to streaming mode	Stream mode off PLL disable RESETB high PWDN high
Streaming	Sensor is fully powered and is streaming image data on the MIPI CSI-2 bus	All

9.2 Power on Sequence



Parameter	Description	Min.	Max.	Unit
t0	IOVDD/DVDD12/AVDD28 rising time	50	-	μs
t1	IOVDD, DVDD12 and AVDD28 may rise in any order so the rising separation time can vary from 0μs to indefinite	0		μs
t2	From power on to PWDN pull high	0	-	μs
t3	From power on to RESETB pull high	0	-	μs
t4	From PWDN to first I2C transaction	50	-	μs
t5	Minimum No. of MCLK cycles prior to the first I2C transaction	1200	-	MCLK
t6	From RESETB to first I2C transaction	50	-	μs
t7	PLL start up/lock time	-	1	ms
t8	Entering streaming mode – First frame start sequence	Depend on the setting		ms

9.3 Power off Sequence



Parameter	Description	Min.	Max.	Unit
t0	IOVDD, DVDD12 and AVDD28 may pull down in any order, so the falling separation time can vary from 0μs to indefinite	0	-	μs
t1	From PWDN pull low to AVDD28/DVDD12 pull down	0		μs
t2	Enter Software Standby CCI command – Device in Software Standby mode	0	-	μs
t3	Minimum number of MCLK cycles after the last CCI transaction or MIPI frame end code.	2000		MCLK
t4	From RESETB pull low to AVDD28/DVDD12 pull down	0	-	μs

- Recommended power on/off sequence is above.
- If the sensor’s power cannot be cut off, please keep power supply, then set PWDN pin low. It will make sensor standby
- Register should be reloaded before works.
- If the standby sequence needs to be modified, please contact FAE of *Galaxycore Inc.*

9.4 Black level calibration

Black level is caused by pixel characteristics and analog channel offset, which makes poor image quality in dark condition and color balance, to reduce these, sensor automatically calibrates the black level every frame with light shield pixel array.

9.5 Integration time

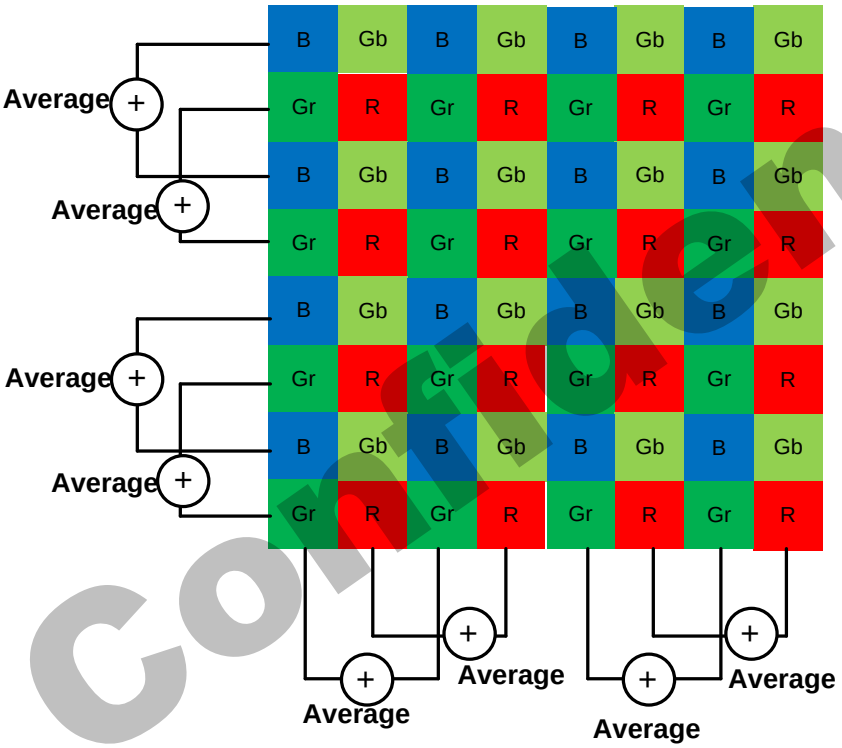
The integration time is controlled by the integration time registers

Address	Register name	Description
P0:0x03	Shutter time	[5:0] shutter time[13:8]
P0:0x04		[7:0] shutter time[7:0]
P0:0x41	Frame length	[5:0] frame length[13:8]
P0:0x42		[7:0] frame length[7:0]

9.6 Binning mode

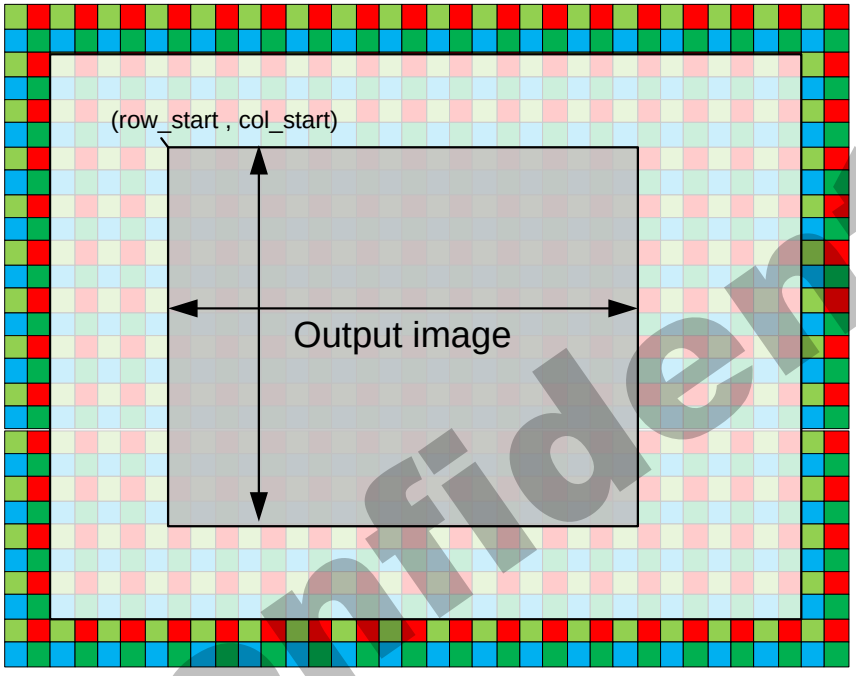
Binning read out mode can be used to obtain an image of lower resolution for full field of view, with lower output rate.

The following diagram describe on 2x2 averaged binning operations, pixels of two adjacent rows and columns are averaged, read out as one pixel.



9.7 Windowing

GC5035 has a rectangular pixel array 2608 x 1960, it can be windowed by output size control, the output image windowing can be used to adjust output size, and it will affect field angle.

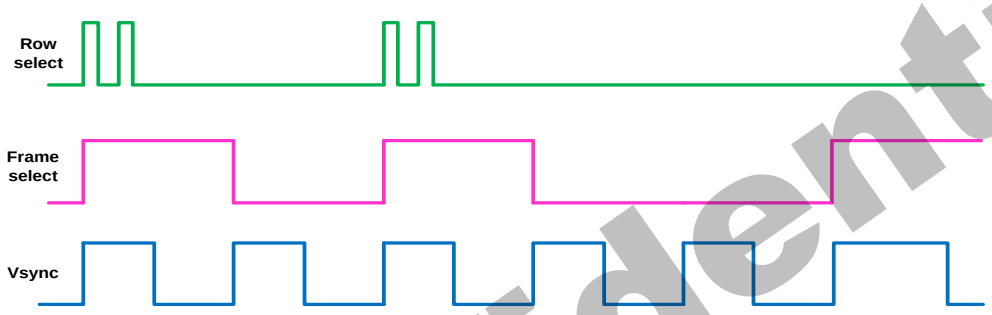


Address	Register name	Description
P0:0x0d	win_height	[2:0]win_height[10:8]
P0:0x0e		[7:0]win_height[7:0]
P0:0x0f	win_width	[3:0]win_width[11:8]
P0:0x10		[7:0]win_width[7:0]
P0:0x09	Row start	[2:0]row_start[10:8]
P0:0x0a		[7:0]row_start [7:0]
P0:0x0b	Col start	[2:0]col_start[10:8]
P0:0x0c		[7:0]col_start[7:0]

9.8 Strobe timing

The strobe function of GC5035 is controlled by strobe request (P2:0x84[0]), which is level triggered. The beginning and the end of the request should not within the same frame.

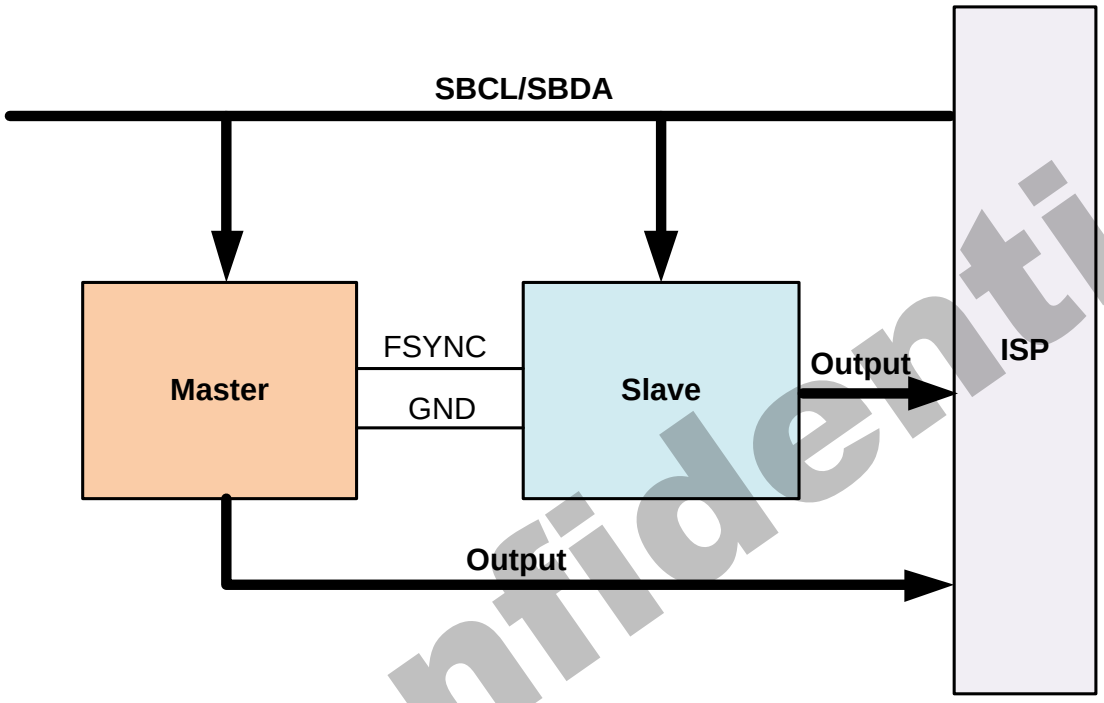
As the strobe request begins, there are two sub-patterns we can use. The first is row_sel (P2:0x8a[2]), which means we can choose several rows to determine the duration of the request. Second is frame_sel (P2:0x8a[1]), the meaning of which is similar to the first one.



Address	Register name	Description
P2:0x84	strobe_request	[0]strobe_request
P2:0x85	strobe_mode2	[3]strobe output [2]strobe_frame_times_mode
P2:0x86	strobe_exp_th	[7:0]strobe_exp_th[7:0]
P2:0x87		[5:0]strobe_exp_th[13:8]
P2:0x88	strobe_lasts_th	[7:0]strobe_lasts_th[7:0]
P2:0x89		[5:0]strobe_lasts_th[13:8]
P2:0x8a	strobe_mode	[7] pre_exp_mode [6] out 2frame [5] startl sel used in allout [4] edge trigger mode [3] fsync_strobe_allout [2] row sel [1] frame sel [0] exp sel
P2:0x8b	strobe_delay_mode	[7:6] strobe_delay_mode [5:3] strobe_frame_interval [2:0] strobe_frame_times

9.9 Frame sync mode

GC5035 can support hardware frame sync for dual camera application. It can be set both master and slave sensor. When use this mode, the two sensor’s FSYNC pin must connect to each other.



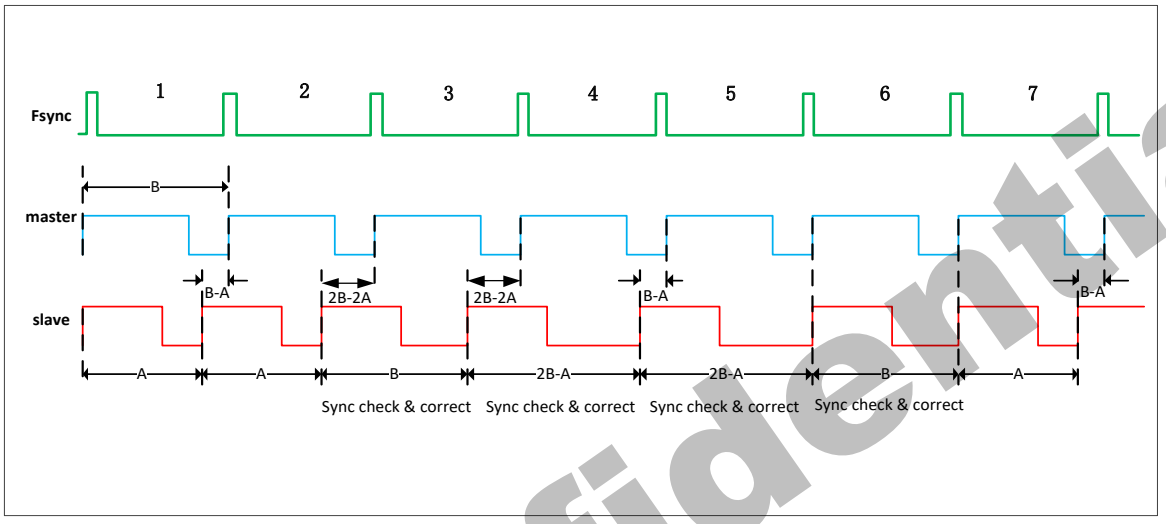
The following figure shows the mechanism of dual sync function of GC5035 in slave mode. It comes down to four steps with the dual sync operation.

(1) After enabling the dual sync function of GC5035, the internal row counter of GC5035 would be set to a specific value (either 0 or controlled by P0:0x83[6:0]) compulsively as the first sync pulse comes. This operation determines the align position of the dual sync process.

(2) As the second sync pulse comes, the slave will record the row counter value at the moment it receives the sync pulse, then calculate the value that the frame length should be extended (which is B-A) and add that value to the initial frame length of slave.

(3) The new frame length value will be written to frame length register as soon as the calculation finishes. Since the frame length update timing is N+1, the new frame length (A+B-A=B) will take effect in the third frame, as shown in the figure.

(4) Step (2) & (3) will continue in following frames.



Address	Register name	Description
P0:0x00	fsync_mode	[4]fsync_clear_counter [3]clock en [1]1 master or 0 slave [0]fsync_en
P0:0x82	fsync_mode_new2	[3] row count mode
P0:0x83	fsync_mode_new3	[7] gpio_value (gpio_mode on) or Fsync_diff_always_mode (gpio_mode off) [6:0] fsync out position
P0:0x84	Fsync row time	[7] position_FS_D [3] position_FS_A [2] position_FE_D [1] fsync_out_polarity [0] fsync_in_polarity
P0:0x85	fsync_mode_new4	[6] first vb clear [5] fsync_row_diff_mode
P0:0x86	fsync_row_diff_th	[5:0] fsync_row_diff_th

P0:0x87	Debug_mode4	[5:4] fsync_vb_gap
P0:0x88	fsync_row_diff_big[13:8]	[5:0] fsync_row_diff_big[13:8]
P0:0x89	fsync_row_diff_big [7:0]	[7:0] fsync_row_diff_big [7:0]
P0:0x8a	fsync_row_diff_big2[13:8]	[5:0] fsync_row_diff_big2[13:8]
P0:0x8b	fsync_row_diff_big2 [7:0]	[7:0] fsync_row_diff_big2[7:0]

9.10 OTP memory

GC5035 sensor has 8K bits embedded OTP (One Time Programmable) memory, 4K bits are for customers, which is for storing camera module calibration data.

9.11 Frame structure

Frame structure is controlled by HB, frame length, window start, window height, window width and VB.

Frame length control

Frame length is controlled by window height, minimum VB and shutter time.

- Minimum frame length = window height + 24 +12
- If shutter time < minimum frame length:

  Actual frame length = minimum frame length
- If shutter time > minimum frame length:

  Actual frame length = shutter time + 16 (recommended).

Line length control

Line length = 2920 (not recommended to be modified)

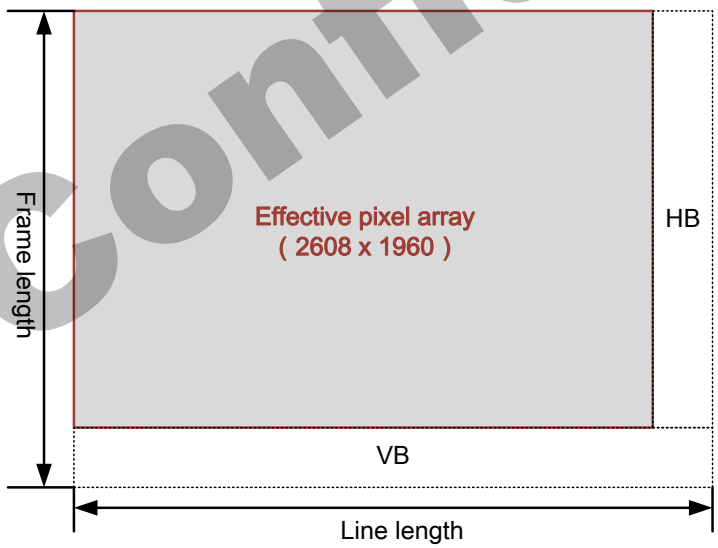
Address	Register name	Description
P0:0x05	Line length	[3:0] Line length[11:8] X4
P0:0x06		[7:0] Line length[7:0] X4
P0:0x41	Frame length	[5:0] frame length[13:8]
P0:0x42		[7:0] frame length[7:0]

Output window array control

Address	Register name	Description
P1:0x91	Out_window_y1	[2:0] Out_window_y1[10:8]
P1:0x92		[7:0] Out_window_y1[7:0]
P1:0x93	Out_window_x1	[3:0] Out_window_x1[11:8]
P1:0x94		[7:0] Out_window_x1[7:0]
P1:0x95	Out window height	[2:0] Out window height[10:8]
P1:0x96		[7:0] Out window height[7:0]
P1:0x97	Out window width	[3:0] Out window width[11:8]
P1:0x98		[7:0] Out window width[7:0]

Blank time control

1. line blank time is controlled by HB
2. frame blank time
   - frame blank time = frame length[Reg(P0:0x41, 0x42)] – window height – 24



10. Register List

System Register

Address	Name	Default Value	R/W	Description
0xf0	**Sensor_ID_high**	**0x50**	**RO**	**Sensor_ID**
0xf1	**Sensor_ID_low**	**0x35**	**RO**	**Sensor_ID**
0xf2	I2C_open_ena pwd_dn	0x00	RW	[5] I2C_open_ena [4] pwd_dn 0: pulldown 1: not pull
0xf3	OTP_mode_new	0x00	WR	[6] OTP write pulse [5] OTP read pulse [4] read speed up [3] write speed up [2] OTP write 1: bit 0: byte [1] OTP_acc_enable [0] OTP read 1: bit 0: byte
0xf4	reduce_power_mode PLL_mode3	0x00	RW	[7] reduce_power_mode [6:4] pll_ldo_set
0xf5	cp_clk_mode	0x80	RW	[7] soc_mclk_enable [6] pll_ldo_en [5:4] cp_clk_sel [3:0] cp_clk_div
0xf6	wpllclk_div refmp_div	0x15	RW	[7:3] wpllclk_div [2:0] refmp_div
0xf7	PLL_mode1	0x00	RW	[7]refdiv2d5_en [6]refdiv1d5_en [5:4]scaler_mode(dvpmode) [3] refmp_enb [2] freq div2 switch delay mode(need vs_st>0x10) [1] div2en [0] pll_en
0xf8	PLL_mode2	0x5a	RW	[7:0]pllmp_div
0xf9	rpllclk_div	0x83	RW	[7:3] rpllclk_div

	pllmp_prediv analog_pwc			[2:1] pllmp_prediv [0] analog_pwc
0xfa	clk_div_mode	0x00	RW	[7] div2 enable [6] close div2_frame mode [5] divmp_enb 0: en 1: off [4] mdclk_en [3] NA [2] NA [1] div2 [0] div1
0xfb	I2c_device_id	0x74	RW	[7:1] I2C device id: 6e [0] NA
0xfc	cm_mode	0x00	RW	[7] regf clk enable [6] sys_rclk sel [5] div2_mode [4] bypass_clk_auto_switch [3] NA [2] serial clk enable [1] re_lock_pll [0] not_use_pll
0xfd	regf_buf_mode	0x00	RW	[5] regf_buf_clk_en [4] cen_mode [3] buf_en [2] page mode [1:0] sel_flag 1: buf2 0: buf1
0xfe	Reset related	0x00	RW	[7] soft_reset [6] cm_reset clock manager [5] mipi_reset [4] CISCTL_reset_n [2:0] page_select

Analog & CISCTL

Address	Name	Default Value	R/W	Description
P0:0x03	Exposure[13:8]	0x04	RW	[7:6] NA [5:0] exposure[13:8]
P0:0x04	Exposure[7:0]	0x10	RW	Exposure[7:0]

P0:0x05	Line length[11:8]	0x02	RW	Line length
P0:0x06	Line length[7:0]	0xda	RW	
P0:0x09	Row_start[10:8]	0x00	RW	[2:0] CISCTL_row_start[10:8]
P0:0x0a	Row_start[7:0]	0x00	RW	Row start[7:0]
P0:0x0b	Col_start[11:8]	0x00	RW	[3:0]CISCTL_col_start[11:8]
P0:0x0c	Col_start[7:1]	0x00	RW	Col start[7:0]
P0:0x0d	win_height[10:8]	0x07	RW	[7:3] NA [2:0] Window height[10:8]
P0:0x0e	win_height[7:0]	0xa8	RW	Window height[7:0]
P0:0x0f	win_width[11:8]	0x0a	RW	[7:4] NA [3:0] Window width[11:8]
P0:0x10	win_width[7:0]	0x34	RW	[7:0] window width[7:0]
P0:0x13	CISCTL_vs_st	0x1c	RW	[7:0] CISCTL_vs_st
P0:0x14	CISCTL_vs_et	0x04	RW	[7:0] CISCTL_vs_et
P0:0x17	CISCTL_mode1	0X80	RW	[7:2] reserved [1] updown [0] mirror
P0:0x41	frame length [13:8]	0x0b	RW	[5:0] frame length[13:8]
P0:0x42	frame length [7:0]	0xc8	RW	[7:0] frame length[7:0]

CSI/PHY1.0

Address	Name	Default Value	R/W	Description
P3:0x01	DPHY_analog_mode1	0x00	RW	[7] disable_set[1] [6:5] clkctr [4] NA [3] disable_set[0] [2] dphy_lane1_en [1] dphy_lane0_en [0] dphy_clk_en
P3:0x02	DPHY_analog_mode2	0x00	RW	[7:6] data1ctr [5:4] data0ctr [3:0] mipi_diff
P3:0x03	DPHY_analog_mode3	0x00	RW	[7] clklane_p2s_sel [6] NA [5] data1delay1s [4] data0delay1s [3] clk_delay1s [2] mipi_en [1:0] clkhs_ph
P3:0x04	FIFO_prog_full_level[7:0]	0x08	RW	[7:0] FIFO_prog_full_level[7:0]

P3:0x05	FIFO_prog_full_level[11:8]	0x00	RW	[7:4] NA [3:0] FIFO_prog_full_level[11:8]
P3:0x06	FIFO_mode	0x00	RW	[7] NA [6] RF2 32X32 cen [5] mipi write gate mode [4] FIFO_rst_mode [3] bit10_swich [2] NA [1] write fifo gate mode [0] read fifo gate mode
P3:0x10	LDI_set_dummy	0x32	RW	dummy LDI
P3:0x11	LDI_set	0x2b	RW	RAW8：0x2a RAW10：0x2b
P3:0x12	LWC_set[7:0]	0xa8	RW	Raw8：2592
P3:0x13	LWC_set[15:8]	0x0c	RW	Raw10：2592x5/4
P3:0x14	SYNC_set	0xb8	RW	SYNC_set
P3:0x15	DPHY_mode	0x10	RW	[7] NA [6] mipi para invar when div2 [5] DATA lane gate mode [4] all_lane_open_mode [3:2] switch_msb_mode [1:0] clklane_mode
P3:0x16	LP_set	0x29	RW	[7:6] hi-z [5:4] use define [3:2] 1 [1:0] 0
P3:0x18	DPHY_analog_mode4	0x00	RW	[7:4] mp_reserve [3:2] data0hs_ph [1:0] data1hs_ph
P3:0x1b	Fifo2_prog_full_level	0x0c	RW	[5:0] Fifo2_prog_full_level
P3:0x1c	Fifo2_push_prog_full_level	0x10	RW	[5:0] Fifo2_push_prog_full_level
P3:0x1d	Sram_test_mode	0x02	RW	[3] 1:write_fifo_gate mode [2] 1:read_fifo_gate mode [1] 1:sram gate [0] sram test mode
P3:0x20	T_init_set	0x80	RW	Timing of initial setting, more than 100 us
P3:0x21	T_LPX_set	0x10	RW	Timing of LP setting, more than 50ns
P3:0x22	T_CLK_HS_PREPARE_set	0x05	RW	Timing of COCLK HS PREPARE setting, 38ns ~95ns LP00
P3:0x23	T_CLK_zero_set	0x20	RW	Timing of COCLK HS zero setting, more than 300ns
P3:0x24	T_CLK_PRE_set	0x02	RW	Timing of COCLK HS PRE of Data setting, more than 8UI

P3:0x25	T_CLK_POST_set	0x10	RW	Timing of COCLK HS Post of Data setting, 60ns +52UI
P3:0x26	T_CLK_TRAIL_set	0x08	RW	Timing of COCLK tail setting, 60ns
P3:0x27	T_HS_exit_set	0x10	RW	Timing of HS exit setting, more than 100ns
P3:0x28	T_wakeup_set	0xa0	RW	Timing of wakeup setting, 1ms
P3:0x29	T_HS_PREPARE_set	0x06	RW	Timing of data HS PREPARE setting, 45+4UI~85+5UI
P3:0x2a	T_HS_Zero_set	0x0a	RW	Timing of data HS zero setting, 140ns
P3:0x2b	T_HS_TRAIL_set	0x08	RW	Timing of data HS trail setting, 60ns
P3:0x30	MIPI_test	0x00	RW	[7:2] NA [1:0] MIPI_test [1] clk [0] data
P3:0x35	OUT_pad_test_data	0x00	RW	OUT_pad_test_data
P3:0x36	clkp_drv	0x00	RW	[7:3] NA [2:0] clkp_drv
P3:0x37	data1lp_drv data0lp_drv	0x00	RW	[5:3] data1lp_drv [2:0] data0lp_drv
P3:0x38	prbs_mode	0x20	RW	[7]NA [6]prbs11 [5]prbs_9 [4]clane prbs en [3]dlane3 prbs en [2]dlane2 prbs en [1]dlane1 prbs en [0]dlane0 prbs en
P3:0x39	prbs_LDI	0x3d	RW	prbs_LDI
P3:0x4a	prbs_seed[7:0]	0x9a	RW	[7:0] prbs_seed[7:0]
P3:0x4b	prbs_seed[15:8]	0x78	RW	[7:0] prbs_seed[15:8]
P3:0x4c	MIPI_TSEL	0x01	RW	[7:2] NA [1:0] MIPI_TSEL
P0:0x3f	fifo_pop_error fifo_push_error fif01_full fifo1_error	0x00	RW	[3]fifo1_error_valid [2] fifo1_full_valid [1] fifo_pop_error_valid [0] fifo_push_error_valid
P0:0x3e	CIS2_mode	0x00	RW	[7] lane_en [6] Four lane [5] ULP_en [4] MIPI_en [3]mipi_set_auto_disable [2]RAW8_mode [1] line_sync_mode [0] double_lane_en

ISP Related

Address	Name	Default Value	R/W	Description
P1:0x60	WB_offset	0x40	RW	[7:0] WB_offset
P1:0x8c	debug_mode2	0x10	RW	[7:3] reserved [2] input test image [1] pregain test image [0] out test image
P1:0x91	out_win_y1[10:8]	0x00	RW	[2:0] out_win_y1[10:8]
P1:0x92	out_win_y1 [7:0]	0x00	RW	[7:0] out_win_y1 [7:0]
P1:0x93	out_win_x1[11:8]	0x00	RW	[3:0] out_win_x1[11:8]
P1:0x94	out_win_x1 [7:0]	0x00	RW	[7:0] out_win_x1[7:0]
P1:0x95	out_win_height[10:8]	0x07	RW	[2:0] out_win_height[10:8]
P1:0x96	out_win_height[7:0]	0x98	RW	[7:0] out_win_height[7:0]
P1:0x97	out_win_width[11:8]	0x0a	RW	[3:0] out_win_width[11:8]
P1:0x98	out_win_width[7:0]	0x20	RW	[7:0] out_win_width[7:0]

BLK

Address	Name	Default Value	R/W	Description
P4:0x50	colgain_offset_CH0_G1[7:0]	0x00	RW	[7:0] colgain_offset_ CH0_G1[7:0]
P4:0x58	colgain_offset_CH0_G1[12:8]	0x00	RW	[3:0] colgain_offset_ CH0_G1[11:8] S7.4
P4:0x51	colgain_offset_CH0_R1[7:0]	0x00	RW	[7:0] colgain_offset_ CH0_R1[7:0]
P4:0x59	colgain_offset_CH0_R1[12:8]	0x00	RW	[3:0] colgain_offset_ CH0_R1[11:8] S7.4
P4:0x52	colgain_offset_CH0_B2[7:0]	0x00	RW	[7:0] colgain_offset_ CH0_B2[7:0]
P4:0x5a	colgain_offset_CH0_B2[12:8]	0x00	RW	[3:0] colgain_offset_ CH0_B2[11:8] S7.4
P4:0x53	colgain_offset_CH0_G2[7:0]	0x00	RW	[7:0] colgain_offset_ CH0_G2[7:0]
P4:0x5b	colgain_offset_CH0_G2[12:8]	0x00	RW	[3:0] colgain_offset_ CH0_G2[11:8] S7.4
P4:0x54	colgain_offset_CH1_G1[7:0]	0x00	RW	[7:0] colgain_offset_ CH1_G1[7:0]
P4:0x5c	colgain_offset_CH1_G1[12:8]	0x00	RW	[3:0] colgain_offset_ CH1_G1[11:8] S7.4
P4:0x55	colgain_offset_CH1_R1[7:0]	0x00	RW	[7:0] colgain_offset_ CH1_R1[7:0]
P4:0x5d	colgain_offset_CH1_R1[12:8]	0x00	RW	[3:0] colgain_offset_ CH1_R1[11:8] S7.4
P4:0x56	colgain_offset_CH1_B2[7:0]	0x00	RW	[7:0] colgain_offset_ CH1_B2[7:0]
P4:0x5e	colgain_offset_CH1_B2[12:8]	0x00	RW	[3:0] colgain_offset_ CH1_B2[11:8] S7.4
P4:0x57	colgain_offset_CH1_G2[7:0]	0x00	RW	[7:0] colgain_offset_ CH1_G2[7:0]
P4:0x5f	colgain_offset_CH1_G2[12:8]	0x00	RW	[3:0] colgain_offset_ CH1_G2[11:8] S7.4

Gain control

Address	Name	Default Value	R/W	Description	
P0:0xb1	auto_pregain[9:6]	0x01	RW	[3:0] auto_pregain[9:6]	
P0:0xb2	auto_pregain[5:0]	0x00	RW	[7:2] auto_pregain[5:0]	4.6
P0:0xb6	col_code	0x00	RW	[7:5]NA [4:0]code	
P4:0x40	channel_gain_CH0_G1[7:0]	0x00	RW	[7:0] channel_gain_CH0_G1[7:0]	
P4:0x48	channel_gain_CH0_G1[10:8]	0x04	RW	[2:0] channel_gain_CH0_G1[10:8]	1.10
P4:0x41	channel_gain_CH0_R1[7:0]	0x00	RW	[7:0] channel_gain_CH0_R1[7:0]	
P4:0x49	channel_gain_CH0_R1[10:8]	0x04	RW	[2:0] channel_gain_CH0_R1[10:8]	1.10
P4:0x42	channel_gain_CH0_B2[7:0]	0x00	RW	[7:0] channel_gain_CH0_B2[7:0]	
P4:0x4a	channel_gain_CH0_B2[10:8]	0x04	RW	[2:0] channel_gain_CH0_B2[10:8]	1.10
P4:0x43	channel_gain_CH0_G2[7:0]	0x00	RW	[7:0] channel_gain_CH0_G2[7:0]	
P4:0x4b	channel_gain_CH0_G2[10:8]	0x04	RW	[2:0] channel_gain_CH0_G2[10:8]	1.10
P4:0x44	channel_gain_CH1_G1[7:0]	0x00	RW	[7:0] channel_gain_CH1_G1[7:0]	
P4:0x4c	channel_gain_CH1_G1[10:8]	0x04	RW	[2:0] channel_gain_CH1_G1[10:8]	1.10
P4:0x45	channel_gain_CH1_R1[7:0]	0x00	RW	[7:0] channel_gain_CH1_R1[7:0]	
P4:0x4d	channel_gain_CH1_R1[10:8]	0x04	RW	[2:0] channel_gain_CH1_R1[10:8]	1.10
P4:0x46	channel_gain_CH1_B2[7:0]	0x00	RW	[7:0] channel_gain_CH1_B2[7:0]	
P4:0x4e	channel_gain_CH1_B2[10:8]	0x04	RW	[2:0] channel_gain_CH1_B2[10:8]	1.10
P4:0x47	channel_gain_CH1_G2[7:0]	0x00	RW	[7:0] channel_gain_CH1_G2[7:0]	
P4:0x4f	channel_gain_CH1_G2[10:8]	0x04	RW	[2:0] channel_gain_CH1_G2[10:8]	1.10

STROBE

Address	Name	Default Value	R/W	Description
P2:0x80	long_exp_position	0x4c	RW	[7:6] long_exp_turn [5:0] long_exp_position
P2:0x81	long_exp[19:16]	0x00	RW	[3:0] long_exp[19:16]
P2:0x82	long_exp[15:8]	0x00	RW	[7:0] long_exp[15:8]
P2:0x83	long_exp[7:0]	0x00	RW	[7:0] long_exp[7:0]
P2:0x84	strobe_request	0x00	RW	[0] strobe_request
P2:0x85	strobe_mode2	0x00	RW	[3]strobe output [2]strobe_frame_times_mode
P2:0x86	strobe_exp_th[7:0]	0x50	RW	[7:0] strobe_exp_th[7:0]
P2:0x87	strobe_exp_th[13:8]	0x00	RW	[5:0] strobe_exp_th[13:8]
P2:0x88	strobe_lasts_th[7:0]	0x04	RW	[7:0] strobe_lasts_th[7:0]
P2:0x89	strobe_lasts_th[13:8]	0x00	RW	[5:0] strobe_lasts_th[13:8]

P2:0x8a	strobe_mode	0x00	RW	[7] pre_exp_mode [6] out 2frame [5] start sel used in all out [4] edge trigger mode [3] fsync_strobe_allout [2] row sel [1] frame sel [0] exp sel
P2:0x8b	strobe_delay_mode strobe_frame_interval strobe_frame_times	0x09	RW	[7:6] strobe_delay_mode [5:3] strobe_frame_interval [2:0] strobe_frame_times
P2:0x8c	strobe_pre_exp_num	0x08	RW	strobe_pre_exp_num

FSYNC

Address	Name	Default Value	R/W	Description
P0:0x00	Fsync_en	0x08	RW	[3] clock_en [2:1] fsync old mode 2’b10: slave old mode 2’b01: master old mode 2’b00: new mode, determined byP0:0x82 as master or slave [0] fsync_en
P0:0x81	fsync_mode_new	0x13	RW	[7:2] fsync_time x4+3 [1:0] fsync_mode_new 2'b11:old mode 2'b10:clear_start 2'b01:clear_stop 2'b00:update_flop
P0:0x82	fsync_mode_new2	0x00	RW	[7] gpio_mode [6] vsync_out_mode [5] co-work with old [4] 0: disable aec delay mode using fsync [3] row count mode [2] delay to row gap [1] every frame slave en [0] every frame master en
P0:0x83	fsync_mode_new3	0x04	RW	[7] gpio_value [6:0] fsync out position
P0:0x84	fsync_rowtime	0x00	RW	[1] fsync_out_polarity [0] fsync_in_polarity
P0:0x85	fsync_mode_new4	0x01	RW	[7] fsync_vb_gap_mode_tmp [6] fsync_vb_first_mode_tmp

				[5] fsync_row_diff_mode [4] fsync_vb_mode [3:0] vb_lowbits_disable
P0:0x86	fsync_row_diff_th	0x02	RW	[7] fsync_vb_diff_rnd [6] fsync_exp_change_mode [5:0] fsync_row_diff_th
P0:0x87	debug_mode4	0x58	RW	[7] exp_3T_mode2 [6] AEC_delay_mode [5:4] fsync_vb_gap [3:2] gain switch mode [1:0] fsync vb old
P0:0x88	fsync_row_diff_big[13:8]	0x00	RW	[5:0] fsync_row_diff_big[13:8]
P0:0x89	fsync_row_diff_big [7:0]	0x04	RW	[7:0] fsync_row_diff_big [7:0]
P0:0x8a	fsync_row_diff_big2[13:8]	0x00	RW	[5:0] fsync_row_diff_big2[13:8]
P0:0x8b	fsync_row_diff_big2[7:0]	0x10	RW	[7:0] fsync_row_diff_big2[7:0]
P0:0x8d	debug_mode2	0x92	RW	[7] fsync_vb_gap_lasts [2]NA [0]NA
P0:0xec	fsync_row_diff[14:8]	--	RW	[6:0] fsync_row_diff[14:8]
P0:0xed	fsync_row_diff[7:0]	--	RW	[7:0] fsync_row_diff[7:0]