Muhammed YILMAZ
150150149

20.05.2020

BLG 322E – Computer Architecture
Assigment 4

a) All signals are active low (0).

BR_1	BR_2	BR_3	BR_4	BG	BR	BG_1	BG_2	BG_3	BR_4
0	X	X	X	0	0	0	1	1	1
0	X	X	X	1	0	1	1	1	1
1	0	X	X	0	0	1	0	1	1
1	0	X	X	1	0	1	1	1	1
1	1	0	X	0	0	1	1	0	1
1	1	0	X	1	0	1	1	1	1
1	1	1	0	0	0	1	1	1	0
1	1	1	0	1	0	1	1	1	1
1	1	1	1	1	1	1	1	1	1

b) Minimized logical expressions are

$$BR = BR_1 \cdot BR_2 \cdot BR_3 \cdot BR_4$$

$$BG_1 = BR_1 + BG$$

$$BG_2 = \neg BR_1 + BR_2 + BG$$

$$BG_3 = \neg BR_1 + \neg BR_2 + BR_3 + BG$$

$$BG_4 = \neg BR_1 + \neg BR_2 + \neg BR_3 + BR_4 + BG$$

Muhammed YILMAZ
150150149

20.05.2020

c)

DMAC$_1$		Data Transfer						Data Transfer	
DMAC$_2$			Data Transfer (5 words)						
DMAC$_3$									
DMAC$_4$									
CPU	Instruction Fetch								
Time(ns)	0	40	90	140	190	240	290	340	390

DMAC$_1$		Data Transfer		Data Transfer		Data Transfer			
DMAC$_2$									
DMAC$_3$	Data Transfer		Data Transfer		Data Transfer		Data Transfer		
DMAC$_4$								Data Transfer	
CPU									
Time(ns)	390	440	490	540	590	640	690	740	790

DMAC$_1$							
DMAC$_2$							
DMAC$_3$	Data Transfer						
DMAC$_4$		Data Transfer		Data Transfer			
CPU			Operand Fetch	Execution		Operand Write	
Time(ns)	790	840	890	950	970	1000	1040 completion of the first instruction

d)

i. CPU(IF) – DMAC$_1$ transfer a word - DMAC$_2$ transfer 2 word

40ns + (50+50)ns + 2*(50+50)ns = 340ns

Clock is 340ns when DMAC 2 complete the transfer of the second word.

ii. CPU(IF)
DMAC$_1$ (1st word)
DMAC$_2$ (1st-5th words)
DMAC$_1$ (2nd word)
DMAC$_3$ (1st word)
DMAC$_1$ (3rd word)
DMAC$_3$ (2nd word)
DMAC$_1$ (4th word)
DMAC$_3$ (3rd word)
DMAC$_1$ (5th word)
DMAC$_3$ (4th word)
DMAC$_4$ (1st-5th words)
DMAC$_3$ (5th words)
CPU(OF)
CPU(EX)
CPU(OW)

40ns + 20*(50+50)ns + 60ns + 20ns + 40ns = 2160ns

Clock is 2160ns when the CPU complete the first instruction cycle.