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Istanbul Technical University
Department of Computer Engineering

BLG 322E – Computer Architecture
Assignment 5 Solutions

1.

a.i.

Data is transferred in blocks of 16 words: 16 = 2^4 => w=4 bits
4K cache memory => 2^12 / 2^4 = 2^8 => f=8 bits
Tag bits => t = a - (w + f) => 20 - (4+8) = 8 => t=8 bits

a.ii.

Data	Tag	Frame	Word	Hit / Miss
$00050	0000 0000	0000 0101	0000	Miss
$0005C	0000 0000	0000 0101	1100	Hit
$01052	0000 0001	0000 0101	0010	Miss
$00057	0000 0000	0000 0101	0111	Miss
$01054	0000 0001	0000 0101	0100	Miss

b.i.

Data is transferred in blocks of 8 words: 8 = 2^3 => w=3 bits
4K cache memory => 2^12 / 2^4 = 2^8 => s=8 bits
Tag bits => t = a - (w + s) => 20 - (8+3) = 9 => t=9 bits

b.ii.

Data	Tag	Set	Word	Hit / Miss
$00050	0000 0000 0	000 0101 0	000	Miss
$0005C	0000 0000 0	000 0101 1	100	Miss
$01052	0000 0001 0	000 0101 0	010	Miss
$00057	0000 0000 0	000 0101 0	111	Hit
$01054	0000 0001 0	000 0101 0	100	Hit

2.

512k Word Main-> 2^19

16 K Word Cache -> 2^14

Blocks -> 16 Words -> 2^4 -> 4 bit offset

Cache contains 256 sets -> 2^8 -> 8 bit index

14 – 8 – 4 = 2 bit -> 4 Way associative

7 bit tag – 8 bit index – 4 bit offset

a.i.

000 0000 0000 1000 1110 A start -> Set numbers: 8, 9, 10, Frame 0

000 0000 0000 1010 0001 A end

Because of No Write Allocate, only A will be cached. No need to calculate set numbers for B and C since they are always used for writing and are never cached.

Address	Tag	Set Number	Frame	A
$00080 - $0008F	0	8	0	A[0]-A[1]
$00090 - $0009F	0	9	0	A[2]-A[17]
$000A0 - $000AF	0	10	0	A[18]-A[19]

a.ii&iii.

For loop 1:

3 read miss, 17 read hit for A

3 block transfer for A

20 write miss for B (C didn't allocate to cache)

20 write to main memory

For loop2:

10 read hit for A

10 write miss for C (C didn't allocate to cache)

10 write to main memory for C (Write through)

0 block transfer

Total: ReadMiss: 3, ReadHits:27, WriteMiss: 30, WriteHits:0, Write-to-main-mem:30, BlockTransfer:3

b.i&ii.

For loop 1:

Read -> 3 miss, 17 hit for A

3 block transfer for A, 3 block transfer for replacement

Write -> 2 miss , 18 hit for B

2 block transfer for B, 2 block transfer for replacement

5*16 word write to the memory (Because replacement algorithm was used.)

2 word write to the memory (write miss – write to the memory)

For loop 2:

10 read hit for A

1 write miss, 9 write hit for C

1 block transfer for C, 1 block transfer for replacement.

16 word write to the memory (Because replacement algorithm was used.)

1 word write to the memory (write miss)

Total: ReadMiss: 3, ReadHits:27, WriteMiss: 3, WriteHits:27, Write-to-main-mem:99, BlockTransfer:12