İTÜ Computer Engineering Department
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COMPUTER ARCHITECTURE FINAL EXAMINATION SOLUTIONS

QUESTION 1: (30 Points)

a)

i) (10 points)

	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15
ADD R8,R6,R7	F	O	A												
LD 0(R10),R1		F	O	A	M										
LD 0(R11),R2			F	O	A	M									
NOP				F	O	A									
NOP					F	O	A								
ADD R1,R2,R3						F	O	A							
NOP							F	O	A						
ADD R0,R3,R4								F	O	A					
ST 0(R12),R3									F	O	A	M			
BA L2										F	O	A			
NOP											F	O	A		
NOP												F	O	A	
L2: ADD R0,0,R3													F	O	A

Arrows show the operations, which must be performed in different clock cycles.
Since the instruction ADD R0, 0, R4 cannot enter the pipeline, it is not shown in the diagram.

ii) (5 points)
Total amount of penalty is 5 clock cycles.

b)

i) (10 points)

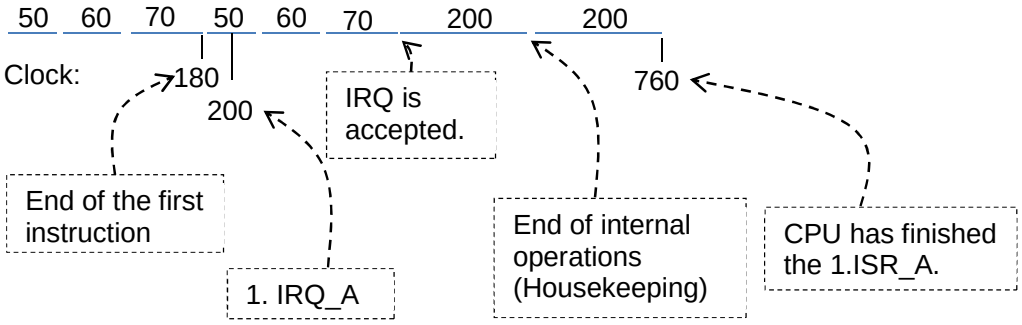
	1	2	3	4	5	6	7	8	9	10	11	12
LD 0(R10),R1	F	O	A	M								
LD 0(R11),R2		F	O	A	M							
ADD R8,R6,R7			F	O	A							
NOP				F	O	A						
ADD R1,R2,R3					F	O	A					
BA L2						F	O	A				
ADD R0,R3,R4							F	O	A			
ST 0(R12),R3								F	O	A	M	
NOP									F	O	A	
L2: ADD R0,0,R3										F	O	A

Since the instruction ADD R0, 0, R4 cannot enter the pipeline, it is not shown in the diagram.

ii) (5 points)
Total amount of penalty is 2 clock cycles.

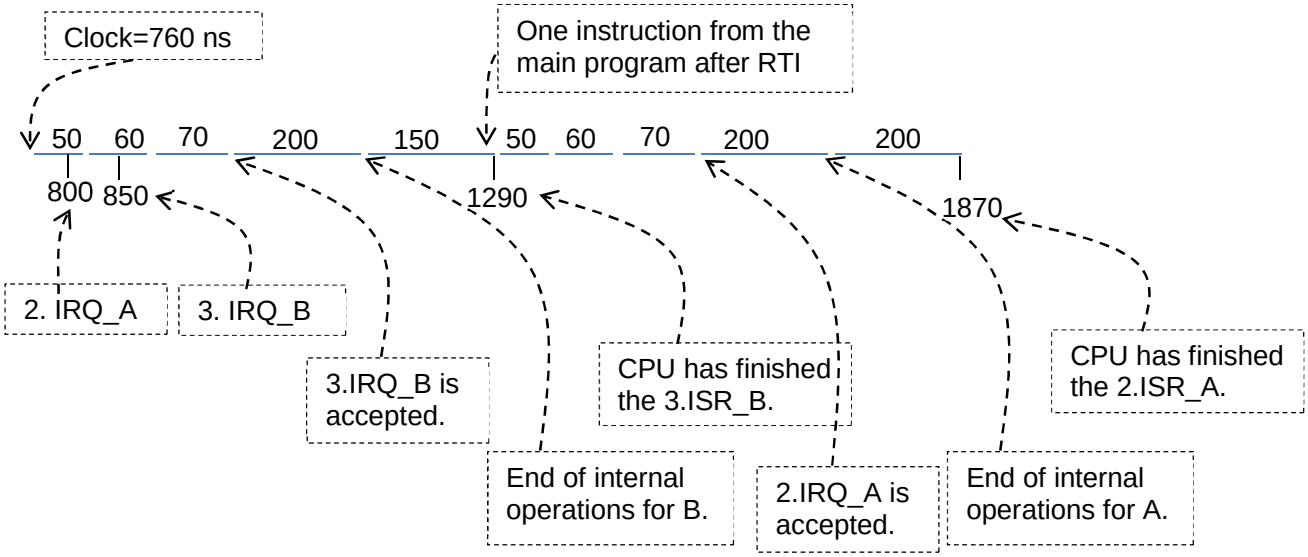
QUESTION 2: (25 Points)

a) Remember, interrupts are accepted and processed after the execution of the current instruction.



Answer: 760 ns. **5 points**

b) We continue from the end of a), Clock=760 ns.



Answer: 1870 ns. **10 points**

c) Explanation is in b).
Answer: 1290 ns. **10 points**

QUESTION 3: (25 Points)

a)

i) In the best case all variables are in the same block of the main memory and in the same cache frame. Same set number and same tag value. (5 points)

For example;

A: 0000 0000 0000 0000 = $0000
B: 0000 0000 0000 0001 = $0001
C: 0000 0000 0000 0010 = $0002

Or

A: 0000 0000 0000 1000 = $0008
B: 0000 0000 0000 1001 = $0009
C: 0000 0000 0000 1010 = $000A

ii) Generate address of A, miss, transfer block from main to cache memory at the same time get A. Read B, hit. Write C, hit, write to cache and main memory (because of WT). (5 points)

$t_a = t_B + t_c + t_m = 100 + 10 + 50 = 160$ ns

b)

i) In the worst case all variables try to share the same set but they are in different blocks of the main memory. Set numbers are same bur their tags are different. (5 points)

16-bit

Tag	set num.	word num.
7-bit	6-bit	3-bit

For example;

A: 0000 000**0 0000 0**000 = $0000
B: 0000 001**0 0000 0**000 = $0200
C: 0000 010**0 0000 0**000 = $0400

ii) Generate address of A, miss, transfer block from main to cache memory, at the same time get A (set:0, frame=0). Generate address of B, miss, transfer block from main to cache memory, at the same time get B (set:0, frame=1). Generate address of C, miss, transfer block from main to cache memory (because of WA) (set:0, frame=0), write to cache and main memory (because of WT). (10 points)

$t_a = t_B + t_B + t_B + t_m = 100 + 100 + 100 + 50 = 350$ ns

QUESTION 4: (20 Points)

a) In a symmetric multiprocessor (SMP) system CPUs use the same memory space, therefore the variable A has the same address in both spaces of CPU1and CPU2. If it is in set:1, frame:0 in the cache of CPU1, then it must be also in set:1 of the cache of CPU2. But we cannot know which frame in set 1. (5 Points)

b) It must be in state "invalid". (5 Points)

c) (10 Points)
CPU2: Write miss, issues the signal *read-with-intent-to-modify*.
CPU1 signals the requesting CPU2 "*Main memory is not valid*".
CPU1 writes the modified cache frame back to main memory, and transitions the state of the cache from "modified" to "invalid".
CPU2 issues the signal *read-with-intent-to-modify* again and reads the frame from main memory.
CPU2 modifies the word in the frame and transitions the state of the frame to "modified".