Istanbul Technical University

Department of Computer Engineering

BLG 322E - COMPUTER ARCHITECTURE

Assignment 1

Due Date: Wednesday, March 16, 2022, 23:00.

- Please **write and draw neatly**.
- You may draw the circuits by hand. Please use a ruler and draw neatly. PLEASE BE NEAT! If we cannot read or follow your solution, no partial credit will be given.
- Please **write your full name** (first name and last name) **and Student ID** at the top of your solution.
- Please show ALL your work. Answers with no supporting explanations or work will not receive any partial credit. Your homework is not just a final report of your results; we want to see your steps. Upload all the papers you worked on to get to the solution.
- **Submissions:** Submit your solution as a PDF file to Ninova before the deadline.
- **No late submissions** will be accepted. Do not send your solutions by e-mail. We will only accept files that have been uploaded to the official Ninova e-learning system before the deadline. Do not risk leaving your submission to the last few minutes.
- **Consequences of plagiarism/cheating:** Assignments have to be done individually. Any cheating will be subject to disciplinary action.

If you have any questions, please e-mail **Abdullah Akgül (akgula15@itu.edu.tr).**

QUESTION:

A task **T** that will be executed on integers consists of seven suboperations X_i (i =1,2,3,4,5) and Y_i (i=1,2).
These suboperations are implemented using combinational digital circuits with the following propagation delays:

X_1=**25ns**,X_2=**15ns**, X_3=**20ns**, X_4=**20ns**, X_5=**45ns**, Y_1=**15ns**, Y_2=**15ns**

Fig. 1 on the right shows the block diagram of the circuit.

- The suboperations should be executed in the given order indicated by the dependency arrows between them.
- Suboperation Y_1 can execute in parallel with X_3 or X_4.
- Similarly, suboperation Y_2 can also execute in parallel with X_3 or X_4.

To execute task **T** faster on elements of an array, we construct pipeline P_A with five stages (S1, S2, S3, S4, S5) as shown in Fig. 2 below. After each stage, we place a register with a delay of 5ns.

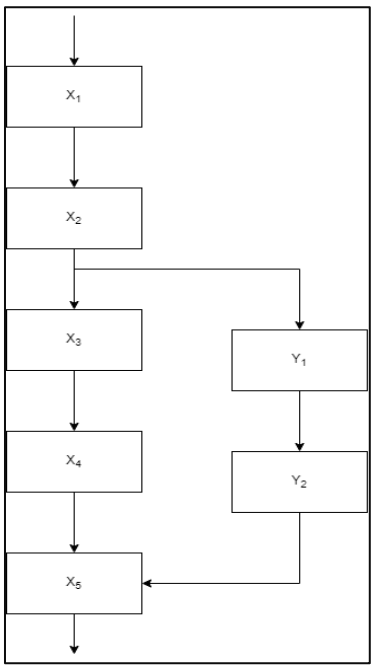

Figure 1: Task T with 7 suboperations

a) How long does it take to execute the task only on the first element of array using the pipeline P_A? (**T_1** = ?) **[10pt]**

b) What is the duration for executing task **T** on one element without a pipeline? (t_n = ?) **[10pt]**

c) What is the minimum number of elements the array should have to achieve any speedup with this pipeline? **[10pt]**

d) Calculate the highest possible speedup pipeline P_A can achieve when it executes a task **T** on an array with an *infinite* number of elements. **[10pt]**

e) Design an alternative pipeline P_B that executes task **T** and meets the following constraints: **[40pt]**

- The speedup P_B achieves on an array with an *infinite* number of elements should not be lower than that achieved by P_A.
- Use as few registers as possible.
- Use the units given in the original circuit (X_i (i=1,2,3,4,5) and Y_i (i=1,2)).
  Do not submit incomprehensible, unreadable, or sloppy drawings. These will incur a **-5pt penalty.**

f) How long does it take to execute the task only on the first element using pipeline P_B you designed in **Part (e)** (**T_1** = ?)? **[10pt]**

g) When executing task **T** on an array with an *infinite* number of elements, what speedup does the pipeline P_B you designed in **Part (e)** achieve? **[10pt]**

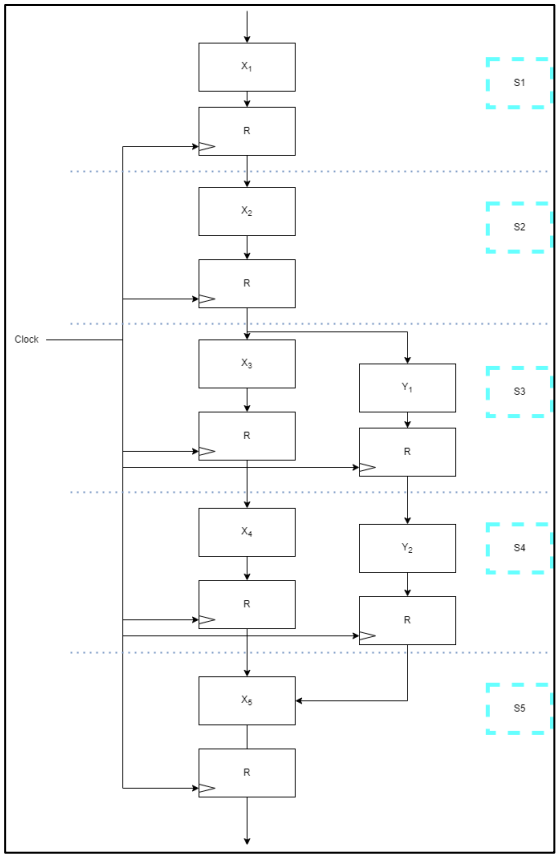

Figure 2: Pipeline P_A with 5 stages