Istanbul Technical University
Department of Computer Engineering

04.04.2019

BLG 322E – Computer Architecture
Assignment 3 – Interrupt

Due Date: 17.04.2019, **Wednesday,** 23.59.

A CPU with 8-bit data bus, has two Interrupt Request inputs (**IRQ1, IRQ2**) and only one Interrupt Acknowledgement output (**INTA**). All signals are active at "1". If the CPU receives a request from IRQ1, it works with vectored interrupts and reads the interrupt vector number after the acknowledgement (**INTA**=1) of the interrupt when its Data acknowledgement input (**DACK**) is "1". If the request comes from **IRQ2**, the CPU does not read a vector number and works in auto vectored mode. There is not an Interrupt acknowledge output related to **IRQ2**. **IRQ1** has higher priority than the **IRQ2**.

In this system there are 5 interrupt sources (*A1, A2, A3, B1, B2*) of two different types (A, B).

- Type **A**: These devices (*A1, A2, A3*) have an Interrupt Request output (**IRQ**), an Interrupt Acknowledgement input (INTA), and 8-bit vector number output (**VN**). 20 ns after the interrupt has been acknowledged (**INTA**=1) the device outputs its vector number at the **VN** and removes its request (**IRQ**=0). The devices A1, A2 and A3 are connected over a serial priority controller (daisy chain) to the CPU.
- Type **B**: These devices (*B1, B2*) have an Interrupt Request output (**IRQ**). They don't have an interrupt acknowledge input.

Priority (precedence) order of the devices: *A1 > A2 > A3 > B1 > B2*

a) (50 points) Design and draw the system with the CPU, 5 devices (*A1, A2, A3, B1, B2*) and the necessary circuitry. You have to decide how and to which input (**IRQ1** or **IRQ2**) of the CPU should be the interrupt sources connected. First, show the links of the daisy chain as a box. Then design and draw the internal structure of one link (stage) of the daisy chain using logical gates.

b) (20 points) How does the CPU determine the start address of the interrupt service routine to be run if the interrupt source is a device of type **A** or of type **B**?

c) (30 points) Assume that the devices *A3* and *B2* assert their interrupt requests at the same time. Show step by step all the signals that are sent in the system until the requests of both devices has been fulfilled.

Submission: Draw the diagrams using a computer program. You should type your name and student ID at the top of the paper. You must submit your homework in PDF format through the Ninova system before the due date.

Late submissions are not accepted. Assignments have to be made individually. If any plagiarism issue is detected, disciplinary regulations of the university are applied.

Note: If you have a problem about the homework, you may make contact with the research assistants of the course (daltan@itu.edu.tr or bakkoca@itu.edu.tr).