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Istanbul Technical University
Department of Computer Engineering

BLG 322E – Computer Architecture
Assignment 4 Solutions

1.

All signals are zero-active.

BR1	BR2	BR3	BR4	BG	BR	BG1	BG2	BG3	BG4
0	X	X	X	0	0	0	1	1	1
0	X	X	X	1	0	1	1	1	1
1	0	X	X	0	0	1	0	1	1
1	0	X	X	1	0	1	1	1	1
1	1	0	X	0	0	1	1	0	1
1	1	0	X	1	0	1	1	1	1
1	1	1	0	0	0	1	1	1	0
1	1	1	0	1	0	1	1	1	1
1	1	1	1	1	1	1	1	1	1

2.

BR= BR1.BR2.BR3.BR4

BG1 = BR1 + BG

BG2 = BR1’ + BR2 + BG

BG3 = BR1’ + BR2’ + BR3 + BG

BG4 = BR1’ + BR2’ + BR3’ + BR4 + BG

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3.

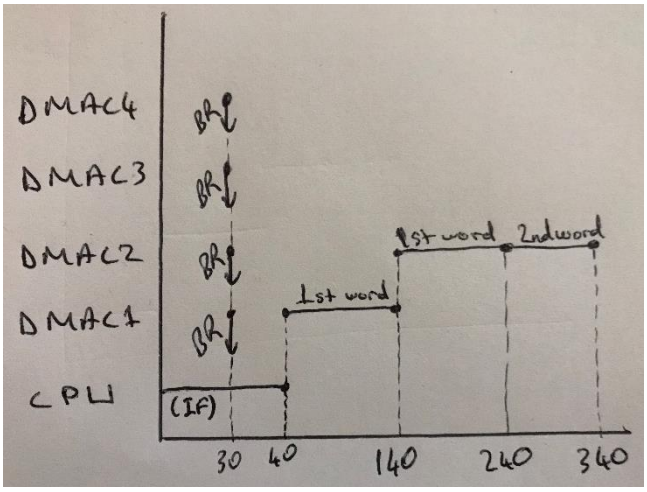
Cycles	CPU	$DMAC_1$	$DMAC_2$	$DMAC_3$	$DMAC_4$
1	IF				
2		1st word			
3			1st word		
4			2nd word		
5			3rd word		
6			4th word		
7			5th word		
8		2nd word			
9				1st word	
10		3rd word			
11				2nd word	
12		4th word			
13				3rd word	
14		5th word			
15				4th word	
16					1st word
17				5th word	
18					2nd word
19	OF				
20	EX				3rd word
21	OW				
22					4th word

4.

A flow-through (explicit) DMAC first reads a word from the I/O interface then writes it to the memory. Therefore, the transfer of one word takes *2 x 50 = 100ns.*

i. DMAC2 completes transfer of the second word at: 340ns

CPU (IF cycle) + DMAC1 (1st word) + DMAC2 (1st and 2ns words) = 40 + 100 + 200 = 340ns



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ii. CPU completes the first instruction cycle at: 2160ns

CPU completes first instruction cycle after all DMACs completes transfer of their words and leave the bus to the CPU.

CPU completes the IF cycle: 40ns

DMACs completes the transfer of all words:

4 x 5 x 100 = 2000ns (# of DMACs x # of words x time to transfer a word)

CPU completes OF, EX, OW cycles: 60 + 20 + 40 = 120ns

In total: 40 + 2000 + 120 = 2160ns

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