18.04.2019

Istanbul Technical University
Department of Computer Engineering

BLG 322E – Computer Architecture
Assignment 4

Due Date: 24.04.2019, **Wednesday,** 23.59.

QUESTION:

Three 3-wire DMACs ($DMAC_1$, $DMAC_2$, $DMAC_3$, and $DMAC_4$) are connected to the 68000-like processor over a bus arbiter (see lecture notes slide 5.23).

The order of precedence is $DMAC_1 > DMAC_2 > DMAC_3 > DMAC_4$.

The CPU has the following properties.

- No Pipelining
- 16-bit Data Bus
- 4 cycles:
  - Instruction Fetch
  - Operand Fetch
  - Execution
  - Operand Write
- Only execution cycle does not need memory.

a) Construct the truth table for the bus arbiter. BR_i represents the BR output of the $DMAC_i$, and BG_i represents the BG input of the $DMAC_i$.

b) Write the minimized logic expressions for the outputs of the bus arbiter.

c) $DMAC_1$, $DMAC_2$, and $DMAC_4$ are in the cycle-stealing mode, and $DMAC_3$ is in the burst mode. All DMACs are programmed to transfer 5 words. Assume that $DMAC_1$, $DMAC_2$, $DMAC_3$, and $DMAC_4$ issue bus requests at the same time as the processor is in the instruction fetch cycle. Write step by step operations performed by the DMACs and the CPU from the beginning of the instruction fetch until the end of the completion of the first instruction.

Submission: You should type your name and student ID at the top of the paper. You must submit your homework through the Ninova system before the due date.

Late submissions are not accepted.

Assignments have to be made individually. If any plagiarism issue is detected, disciplinary regulations of the university are applied.

Note: If you have a problem about the homework, you may make contact with the responsible research assistant of the assignment (esengun@itu.edu.tr).