yosys使用：

read_verilog ***.v; proc; techmap; dfflibmap -liberty *.lib; abc -nocleanup -showtmp -liberty *.v -exe also的路径 -scrpit also的脚本（不包括read和write）;write_blif *.blif

修改：　yosys/passes/techmap/abc.cc

1.将之前abc的read和write修改，因为also需要同构有-

2.因为abc能识别source，also不行，所以我这里强行输入固定命令了

3.write，also需要-x或者-l等

4.使用abc时-s -f，而also则只需要-f

5.识别，module名称，netlist改为了top

6.log_error会终止进程。所以改成了log

截图如下

```
@@ -708,10 +708,10 @@ void abc_module(RTLIL::Design *design, RTLIL::Module *current_module, std::strin
708 708         log_header(design, "Extracting gate netlist of module `%s' to `%s/input.blif'..\n",
709 709                 module->name.c_str(), replace_tempdir(tempdir_name, tempdir_name, show_tempdir).c_str());
710 710
711     -       std::string abc_script = stringf("read_blif %s/input.blif; ", tempdir_name.c_str());
    711 +       std::string abc_script = stringf("read_blif %s/input.blif \n", tempdir_name.c_str());
712 712
713 713         if (!liberty_files.empty()) {
714     -               for (std::string liberty_file : liberty_files) abc_script += stringf("read_lib -w %s; ", liberty_file.c_str());
    714 +               //for (std::string liberty_file : liberty_files) abc_script += stringf("read_lib -w %s; ", liberty_file.c_str());
715 715                 if (!constr_file.empty())
716 716                         abc_script += stringf("read_constr -v %s; ", constr_file.c_str());
717 717         } else
@@ -730,7 +730,8 @@ void abc_module(RTLIL::Design *design, RTLIL::Module *current_module, std::strin
730 730                                 else
731 731                                         abc_script += script_file[i];
732 732                 } else
733     -                       abc_script += stringf("source %s", script_file.c_str());
    733 +                       //abc_script += stringf("source %s", script_file.c_str());
    734 +                       abc_script += stringf("lut_resyn -nx \n xmgrw \n");
734 735         } else if (!lut_costs.empty()) {
735 736                 bool all_luts_cost_same = true;
736 737                 for (int this_cost : lut_costs)
@@ -763,8 +764,8 @@ void abc_module(RTLIL::Design *design, RTLIL::Module *current_module, std::strin
763 764                 abc_script = abc_script.substr(0, pos) + lutin_shared + abc_script.substr(pos+3);
764 765         if (abc_dress)
765 766                 abc_script += "; dress";
```

```
766       -       abc_script += stringf("; write_blif %s/output.blif", tempdir_name.c_str());
767       -       abc_script = add_echos_to_abc_cmd(abc_script);
      767 +       abc_script += stringf(" write_blif -x %s/output.blif", tempdir_name.c_str());
      768 +       //abc_script = add_echos_to_abc_cmd(abc_script);
768   769
769   770         for (size_t i = 0; i+1 < abc_script.size(); i++)
770   771                 if (abc_script[i] == ';' && abc_script[i+1] == ' ')
@@ -990,7 +991,7 @@ void abc_module(RTLIL::Design *design, RTLIL::Module *current_module, std::strin
990   991                         fclose(f);
991   992                 }
992   993
993       -               buffer = stringf("%s -s -f %s/abc.script 2>&1", exe_file.c_str(), tempdir_name.c_str());
      994 +               buffer = stringf("%s -f %s/abc.script 2>&1", exe_file.c_str(), tempdir_name.c_str());
994   995                 log("Running ABC command: %s\n", replace_tempdir(buffer, tempdir_name, show_tempdir).c_str());
995   996
996   997   #ifndef YOSYS_LINK_ABC
@@ -1027,9 +1028,9 @@ void abc_module(RTLIL::Design *design, RTLIL::Module *current_module, std::strin
1027  1028                 ifs.close();
1028  1029
1029  1030                 log_header(design, "Re-integrating ABC results.\n");
1030      -               RTLIL::Module *mapped_mod = mapped_design->module(ID(netlist));
      1031 +               RTLIL::Module *mapped_mod = mapped_design->module(ID(top));
1031  1032                 if (mapped_mod == nullptr)
1032      -                       log_error("ABC output file does not contain a module `netlist'.\n");
      1033 +                       log("ABC output file does not contain a module `netlist'.\n");
```

```
1239  1240              int in_wires = 0, out_wires = 0;
1240      -             for (auto &si : signal_list)
      1241 +             /*for (auto &si : signal_list)
1241  1242                      if (si.is_port) {
1242  1243                              char buffer[100];
1243  1244                              snprintf(buffer, 100, "\\ys__n%d", si.id);
@@ -1252,7 +1253,7 @@ void abc_module(RTLIL::Design *design, RTLIL::Module *current_module, std::strin
1252  1253                              in_wires++;
1253  1254                      }
1254  1255                      module->connect(conn);
1255      -                 }
      1256 +                 }*/
```