Fei Wu

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EDUCATION

University of Exeter, United Kingdom Oct. 2023 – Present
Ph.D. in Computer Science
- Fully funded by the China Scholarship Council and University of Exeter (**CSC-Exeter**)

University of Electronic Science and Technology of China (UESTC), China Sept. 2019 – July 2022
M.Eng. in Electronic and Communication Engineering (Ranked 23/332)
- Ranked **23rd** out of 332 students (**Top 7%**)

Chengdu University of Technology (CDUT), China Sept. 2015 – July 2019
B.Eng. in Electronic and Information Engineering
- Ranked **1st** out of 135 students (**Top 1%**), admitted to master's program without entrance examination.

RESEARCH PUBLICATIONS

[1] **F. Wu**, J. Hu, G. Min, S. Wang, "Efficient Orthogonal Fine-Tuning with Principal Subspace Adaptation," *The Fourteenth International Conference on Learning Representations (ICLR)*, April, 2026.
[2] **F. Wu**, J. Hu, G. Min, S. Wang, "Adaptive Rank Allocation for Federated Parameter-Efficient Fine-Tuning of Language Models," *IEEE Transactions on Computers (TC)*, Accepted, Jan. 2026.
[3] Y. Liu, **F. Wu**, N. Zhao et al., "NVP: A Flexible and Efficient Processor Architecture for Accelerating Diverse Computer Vision Tasks including DNN," *IEEE Transactions on Circuits and Systems II: Express Briefs (TCAS-II)*, vol. 70, no. 1, pp. 271-275, Jan. 2023.

INDUSTRIAL PROJECTS

Pedestrian Tracking and Following for Mobile Robot SLAM (*RuiXinXing Co., Ltd.***)** 2022 – 2023
Objective: Enable reliable tracking and following of a designated pedestrian for mobile robot SLAM.
Responsibilities: 1. Implement PySOT on Jetson Xavier; 2. Develop a tracking method via LiDAR-vision fusion.

NVP: Neural Visual Processor (*SenseTime Co., Ltd.*) 2020 – 2022
Objective: design a general-purpose image processor supporting CNN inference, filtering, and stereo matching.
Responsibilities: 1. Design of hardware architecture and multi-core Segmented Ring Bus; 2. Verification and test of single-core prototype on FPGA; 3. PPA evaluation of the multi-core design using a 40 nm CMOS technology.

FPGA Hardware Accelerator for MRI Segmentation (*West China Hospital of Sichuan Hospital*) 2019 – 2020
Objective: accelerate MRI segmentation using a level-set method on FPGA.
Responsibilities: 1. Design of parallel hardware; 2. UART implementation; 3. FPGA-based demo development

Weightel: Vehicle Intelligent Weighing System (*Griffith-Elder Co., Ltd. & Camrong Co., Ltd.*) 2020 – 2022
Objective: Enable real-time in-vehicle weight measurement for industrial vehicles.
Responsibilities: 1. Design of weighing and aggregation nodes for measurement; 2. In-vehicle communication protocol design using CAN bus; 3. System integration and validation in real-world operating environments.

AWARDS & HONORS

Competitions
- National Third Prize, The China Graduate Circuit Design Contest 2021
- **National Second Prize** and Third Prize, The China Graduate Electronics Design Contest 2020 – 2021
- **National Second Prize**, Huawei Special Competition, The China Graduate Electronics Design Contest 2020

Honors
- Outstanding Graduate of Sichuan Province, China 2022
- Outstanding Graduate of University of Electronic Science and Technology of China 2022

Scholarships
- CSC-Exeter Scholarship and the additional Limetree Capital PhD Scholarship 2023 – 2027
- First-Class Academic Scholarship of University of Electronic Science and Technology of China 2021
- Outstanding Student Scholarship of Chengdu University of Technology 2016 – 2018

SKILLS

Certifications	AMD training on *Accelerating Your Application with AMD GPUs* NVIDIA training on *Efficient Large Language Model (LLM) Customization*.
Technical Skills	Software: PyCharm, Vivado, MATLAB, VS Code; Libraries: PEFT, Flower, Transformers; Programming Languages: Python, C, C++, Verilog, SystemVerilog, VHDL
Language Skills	Native Mandarin speaker; fluent in English