

## Registers

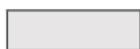
Address	Bit 7	6	5	4	3	2	1	Bit 0	Name
\$0000	PA7	PA6	PA5	PA4	PA3	PA2	PA1	PA0	PORTA <sup>(1)</sup>
\$0001	PB7	PB6	PB5	PB4	PB3	PB2	PB1	PB0	PORTB <sup>(1)</sup>
\$0002	DDA7	DDA6	DDA5	DDA4	DDA3	DDA2	DDA1	DDA0	DDRA <sup>(1)</sup>
\$0003	DDB7	DDB6	DDB5	DDB4	DDB3	DDB2	DDB1	DDB0	DDRB <sup>(1)</sup>
\$0004	0	0	0	0	0	0	0	0	Reserved <sup>(3)</sup>
\$0005	0	0	0	0	0	0	0	0	Reserved <sup>(3)</sup>
\$0006	0	0	0	0	0	0	0	0	Reserved <sup>(3)</sup>
\$0007	0	0	0	0	0	0	0	0	Reserved <sup>(3)</sup>
\$0008	PE7	PE6	PE5	PE4	PE3	PE2	PE1	PE0	PORTE <sup>(2)</sup>
\$0009	DDE7	DDE6	DDE5	DDE4	DDE3	DDE2	0	0	DDRE <sup>(2)</sup>
\$000A	NDBE	CGMTE	PIPOE	NECLK	LSTRE	RDWE	CALE	DBENE	PEAR <sup>(3)</sup>
\$000B	SMODN	MODB	MODA	ESTR	IVIS	EBSWAI	0	EME	MODE <sup>(3)</sup>
\$000C	PUPH	PUPG	0	PUPE	0	0	PUPB	PUPA	PUCR <sup>(3)</sup>
\$000D	0	RDPH	RDPG	0	RDPE	0	RDPB	RDPA	RDRIV <sup>(3)</sup>
\$000E	0	0	0	0	0	0	0	0	Reserved <sup>(3)</sup>
\$000F	0	0	0	0	0	0	0	0	Reserved <sup>(3)</sup>
\$0010	RAM15	RAM14	RAM13	RAM12	RAM11	0	0	0	INITRM
\$0011	REG15	REG14	REG13	REG12	REG11	0	0	0	INITRG
\$0012	EE15	EE14	EE13	EE12	0	0	0	EEON	INITEE
\$0013	MAPROM	NDRF	RFSTR1	RFSTR0	EXSTR1	EXSTR0	ROMON28	ROMON32	MISC
\$0014	RTIE	RSWAI	RSBCK	Reserved	RTBYP	RTR2	RTR1	RTR0	RTICL
\$0015	RTIF	0	0	0	0	0	0	0	RTIFLG
\$0016	CME	FCME	FCMCOP	WCOP	DISR	CR2	CR1	CR0	COPCTL
\$0017	Bit 7	6	5	4	3	2	1	Bit 0	COPRST
\$0018	0	0	0	0	0	0	0	0	Reserved
\$0019	0	0	0	0	0	0	0	0	Reserved
\$001A	0	0	0	0	0	0	0	0	Reserved
\$001B	0	0	0	0	0	0	0	0	Reserved
\$001C	0	0	0	0	0	0	0	0	Reserved
\$001D	0	0	0	0	0	0	0	0	Reserved
\$001E	IRQE	IRQEN	DLY	0	0	0	0	0	INTCR
\$001F	1	1	PSEL5	PSEL4	PSEL3	PSEL2	PSEL1	0	HPRIO
\$0020	BKEN1	BKEN0	BKPM	0	BK1ALE	BK0ALE	0	0	BRKCT0

= Reserved or unimplemented bits.

Table 4-1. MC68HC912D60A Register Map (Sheet 1 of 9)

Registers  
Register Block

Address	Bit 7	6	5	4	3	2	1	Bit 0	Name
\$0021	0	BKDBE	BKMBH	BKMLB	BK1RWE	BK1RW	BK0RWE	BK0RW	BRKCT1
\$0022	Bit 15	14	13	12	11	10	9	Bit 8	BRKAH
\$0023	Bit 7	6	5	4	3	2	1	Bit 0	BRKAL
\$0024	Bit 15	14	13	12	11	10	9	Bit 8	BRKDH
\$0025	Bit 7	6	5	4	3	2	1	Bit 0	BRKDL
\$0026	0	0	0	0	0	0	0	0	reserved
\$0027	0	0	0	0	0	0	0	0	reserved
\$0028	PG7	PG6	PG5	PG4	PG3	PG2	PG1	PG0	PORTG
\$0029	PH7	PH6	PH5	PH4	PH3	PH2	PH1	PH0	PORTH
\$002A	DDG7	DDG6	DDG5	DDG4	DDG3	DDG2	DDG1	DDG0	DDRG
\$002B	DDH7	DDH6	DDH5	DDH4	DDH3	DDH2	DDH1	DDH0	DDRH
\$002C	WI2CE	KWIEG6	KWIEG5	KWIEG4	KWIEG3	KWIEG2	KWIEG1	KWIEG0	KWIEG
\$002D	KWIEH7	KWIEH6	KWIEH5	KWIEH4	KWIEH3	KWIEH2	KWIEH1	KWIEH0	KWIEH
\$002E	0	KWIFG6	KWIFG5	KWIFG4	KWIFG3	KWIFG2	KWIFG1	KWIFG0	KWIFG
\$002F	KWIFH7	KWIFH6	KWIFH5	KWIFH4	KWIFH3	KWIFH2	KWIFH1	KWIFH0	KWIFH
\$0030-\$0037	Unimplemented <sup>(4)</sup>								Reserved
\$0038	0	0	SYN5	SYN4	SYN3	SYN2	SYN1	SYN0	SYNR
\$0039	0	0	0	0	0	REFDV2	REFDV1	REFDV0	REFDV
\$003A	0	0	0	0	0	0	0	0	Reserved
\$003B	LOCKIF	LOCK	0	0	0	0	LHIF	LHOME	PLLFLG
\$003C	LOCKIE	PLLON	AUTO	ACQ	0	PSTP	LHIE	NOLHM	PLLCR
\$003D	0	BCSP	BCSS	0	0	MCS	0	0	CLKSEL
\$003E	0	0	SLDV5	SLDV4	SLDV3	SLDV2	SLDV1	SLDV0	SLOW
\$003F	0	0	0	0	0	0	0	0	Reserved
\$0040	CON23	CON01	PCKA2	PCKA1	PCKA0	PCKB2	PCKB1	PCKB0	PWCLK
\$0041	PCLK3	PCLK2	PCLK1	PCLK0	PPOL3	PPOL2	PPOL1	PPOL0	PWPOL
\$0042	0	0	0	0	PWEN3	PWEN2	PWEN1	PWEN0	PWEN
\$0043	0	Bit 6	5	4	3	2	1	Bit 0	PWPRES
\$0044	Bit 7	6	5	4	3	2	1	Bit 0	PWSCAL0
\$0045	Bit 7	6	5	4	3	2	1	Bit 0	PWSCNT0
\$0046	Bit 7	6	5	4	3	2	1	Bit 0	PWSCAL1
\$0047	Bit 7	6	5	4	3	2	1	Bit 0	PWSCNT1
\$0048	Bit 7	6	5	4	3	2	1	Bit 0	PWCNT0
\$0049	Bit 7	6	5	4	3	2	1	Bit 0	PWCNT1
\$004A	Bit 7	6	5	4	3	2	1	Bit 0	PWCNT2



= Reserved or unimplemented bits.

**Table 4-1. MC68HC912D60A Register Map (Sheet 2 of 9)**

## Registers

Address	Bit 7	6	5	4	3	2	1	Bit 0	Name
\$004B	Bit 7	6	5	4	3	2	1	Bit 0	PWCNT3
\$004C	Bit 7	6	5	4	3	2	1	Bit 0	PWPER0
\$004D	Bit 7	6	5	4	3	2	1	Bit 0	PWPER1
\$004E	Bit 7	6	5	4	3	2	1	Bit 0	PWPER2
\$004F	Bit 7	6	5	4	3	2	1	Bit 0	PWPER3
\$0050	Bit 7	6	5	4	3	2	1	Bit 0	PWDTY0
\$0051	Bit 7	6	5	4	3	2	1	Bit 0	PWDTY1
\$0052	Bit 7	6	5	4	3	2	1	Bit 0	PWDTY2
\$0053	Bit 7	6	5	4	3	2	1	Bit 0	PWDTY3
\$0054	0	0	0	PSWAI	CENTR	RDPP	PUPP	PSBCK	PWCTL
\$0055	DISCR	DISCP	DISCAL	0	0	0	0	0	PWTST
\$0056	PP7	PP6	PP5	PP4	PP3	PP2	PP1	PP0	PORTP
\$0057	DDP7	DDP6	DDP5	DDP4	DDP3	DDP2	DDP1	DDP0	DDRP
\$0058	0	0	0	0	0	0	0	0	Reserved
\$0059	0	0	0	0	0	0	0	0	Reserved
\$005A	0	0	0	0	0	0	0	0	Reserved
\$005B	0	0	0	0	0	0	0	0	Reserved
\$005C	0	0	0	0	0	0	0	0	Reserved
\$005D	0	0	0	0	0	0	0	0	Reserved
\$005E	0	0	0	0	0	0	0	0	Reserved
\$005F	0	0	0	0	0	0	0	0	Reserved
\$0060	Reserved								ATD0CTL0
\$0061	Reserved								ATD0CTL1
\$0062	ADPU	AFFC	ASWAI	DJM	R	R	ASCIE	ASCIF	ATD0CTL2
\$0063	0	0	0	0	S1C	FIFO	FRZ1	FRZ0	ATD0CTL3
\$0064	RES10	SMP1	SMP0	PRS4	PRS3	PRS2	PRS1	PRS0	ATD0CTL4
\$0065	0	S8C	SCAN	MULT	SC	CC	CB	CA	ATD0CTL5
\$0066	SCF	0	0	0	0	CC2	CC1	CC0	ATD0STAT0
\$0067	CCF7	CCF6	CCF5	CCF4	CCF3	CCF2	CCF1	CCF0	ATD0STAT1
\$0068	SAR9	SAR8	SAR7	SAR6	SAR5	SAR4	SAR3	SAR2	ATD0TESTH
\$0069	SAR1	SAR0	RST	TSTOUT	TST3	TST2	TST1	TST0	ATD0TESTL
\$006A-\$006E	0	0	0	0	0	0	0	0	Reserved
\$006F	PAD07	PAD06	PAD05	PAD04	PAD03	PAD02	PAD01	PAD00	PORTAD0
\$0070	Bit 15	14	13	12	11	10	9	Bit 8	ADR00H
\$0071	Bit 7	Bit 6	0	0	0	0	0	0	ADR00L

= Reserved or unimplemented bits.

**Table 4-1. MC68HC912D60A Register Map (Sheet 3 of 9)**

Registers  
Register Block

Address	Bit 7	6	5	4	3	2	1	Bit 0	Name
\$0072	Bit 15	14	13	12	11	10	9	Bit 8	ADR01H
\$0073	Bit 7	Bit 6	0	0	0	0	0	0	ADR01L
\$0074	Bit 15	14	13	12	11	10	9	Bit 8	ADR02H
\$0075	Bit 7	Bit 6	0	0	0	0	0	0	ADR02L
\$0076	Bit 15	14	13	12	11	10	9	Bit 8	ADR03H
\$0077	Bit 7	Bit 6	0	0	0	0	0	0	ADR03L
\$0078	Bit 15	14	13	12	11	10	9	Bit 8	ADR04H
\$0079	Bit 7	Bit 6	0	0	0	0	0	0	ADR04L
\$007A	Bit 15	14	13	12	11	10	9	Bit 8	ADR05H
\$007B	Bit 7	Bit 6	0	0	0	0	0	0	ADR05L
\$007C	Bit 15	14	13	12	11	10	9	Bit 8	ADR06H
\$007D	Bit 7	Bit 6	0	0	0	0	0	0	ADR06L
\$007E	Bit 15	14	13	12	11	10	9	Bit 8	ADR07H
\$007F	Bit 7	Bit 6	0	0	0	0	0	0	ADR07L
\$0080	IOS7	IOS6	IOS5	IOS4	IOS3	IOS2	IOS1	IOS0	TIOS
\$0081	FOC7	FOC6	FOC5	FOC4	FOC3	FOC2	FOC1	FOC0	CFORC
\$0082	OC7M7	OC7M6	OC7M5	OC7M4	OC7M3	OC7M2	OC7M1	OC7M0	OC7M
\$0083	OC7D7	OC7D6	OC7D5	OC7D4	OC7D3	OC7D2	OC7D1	OC7D0	OC7D
\$0084	Bit 15	14	13	12	11	10	9	Bit 8	TCNT
\$0085	Bit 7	6	5	4	3	2	1	Bit 0	TCNT
\$0086	TEN	TSWAI	TSBCK	TFFCA	Reserved				TSCR
\$0087	Reserved								TQCR
\$0088	OM7	OL7	OM6	OL6	OM5	OL5	OM4	OL4	TCTL1
\$0089	OM3	OL3	OM2	OL2	OM1	OL1	OM0	OL0	TCTL2
\$008A	EDG7B	EDG7A	EDG6B	EDG6A	EDG5B	EDG5A	EDG4B	EDG4A	TCTL3
\$008B	EDG3B	EDG3A	EDG2B	EDG2A	EDG1B	EDG1A	EDG0B	EDG0A	TCTL4
\$008C	C7I	C6I	C5I	C4I	C3I	C2I	C1I	C0I	TMSK1
\$008D	TOI	0	PUPT	RDPT	TCRE	PR2	PR1	PR0	TMSK2
\$008E	C7F	C6F	C5F	C4F	C3F	C2F	C1F	C0F	TFLG1
\$008F	TOF	0	0	0	0	0	0	0	TFLG2
\$0090	Bit 15	14	13	12	11	10	9	Bit 8	TC0
\$0091	Bit 7	6	5	4	3	2	1	Bit 0	TC0
\$0092	Bit 15	14	13	12	11	10	9	Bit 8	TC1
\$0093	Bit 7	6	5	4	3	2	1	Bit 0	TC1
\$0094	Bit 15	14	13	12	11	10	9	Bit 8	TC2
\$0095	Bit 7	6	5	4	3	2	1	Bit 0	TC2

= Reserved or unimplemented bits.

**Table 4-1. MC68HC912D60A Register Map (Sheet 4 of 9)**

## Registers

Address	Bit 7	6	5	4	3	2	1	Bit 0	Name
\$0096	Bit 15	14	13	12	11	10	9	Bit 8	TC3
\$0097	Bit 7	6	5	4	3	2	1	Bit 0	TC3
\$0098	Bit 15	14	13	12	11	10	9	Bit 8	TC4
\$0099	Bit 7	6	5	4	3	2	1	Bit 0	TC4
\$009A	Bit 15	14	13	12	11	10	9	Bit 8	TC5
\$009B	Bit 7	6	5	4	3	2	1	Bit 0	TC5
\$009C	Bit 15	14	13	12	11	10	9	Bit 8	TC6
\$009D	Bit 7	6	5	4	3	2	1	Bit 0	TC6
\$009E	Bit 15	14	13	12	11	10	9	Bit 8	TC7
\$009F	Bit 7	6	5	4	3	2	1	Bit 0	TC7
\$00A0	0	PAEN	PAMOD	PEDGE	CLK1	CLK0	PAOVI	PAI	PACTL
\$00A1	0	0	0	0	0	0	PAOVF	PAIF	PAFLG
\$00A2	Bit 7	6	5	4	3	2	1	Bit 0	PACN3
\$00A3	Bit 7	6	5	4	3	2	1	Bit 0	PACN2
\$00A4	Bit 7	6	5	4	3	2	1	Bit 0	PACN1
\$00A5	Bit 7	6	5	4	3	2	1	Bit 0	PACN0
\$00A6	MCZI	MODMC	RDMCL	ICLAT	FLMC	MCEN	MCPR1	MCPR0	MCCTL
\$00A7	MCZF	0	0	0	POLF3	POLF2	POLF1	POLF0	MCFLG
\$00A8	0	0	0	0	PA3EN	PA2EN	PA1EN	PA0EN	ICPACR
\$00A9	0	0	0	0	0	0	DLY1	DLY0	DLYCT
\$00AA	NOVW7	NOVW6	NOVW5	NOVW4	NOVW3	NOVW2	NOVW1	NOVW0	ICOVW
\$00AB	SH37	SH26	SH15	SH04	TFMOD	PACMX	BUFEN	LATQ	ICSYS
\$00AC	0	0	0	0	0	0	0	0	Reserved
\$00AD	0	0	0	0	0	0	TCBYP	0	TIMTST
\$00AE	PT7	PT6	PT5	PT4	PT3	PT2	PT1	PT0	PORTT
\$00AF	DDT7	DDT6	DDT5	DDT4	DDT3	DDT2	DDT1	DDT0	DDRT
\$00B0	0	PBEN	0	0	0	0	PBOVI	0	PBCTL
\$00B1	0	0	0	0	0	0	PBOVF	0	PBFLG
\$00B2	Bit 7	6	5	4	3	2	1	Bit 0	PA3H
\$00B3	Bit 7	6	5	4	3	2	1	Bit 0	PA2H
\$00B4	Bit 7	6	5	4	3	2	1	Bit 0	PA1H
\$00B5	Bit 7	6	5	4	3	2	1	Bit 0	PA0H
\$00B6	Bit 15	14	13	12	11	10	9	Bit 8	MCCNTH
\$00B7	Bit 7	6	5	4	3	2	1	Bit 0	MCCNTL
\$00B8	Bit 15	14	13	12	11	10	9	Bit 8	TC0H
\$00B9	Bit 7	6	5	4	3	2	1	Bit 0	TC0H

= Reserved or unimplemented bits.

Table 4-1. MC68HC912D60A Register Map (Sheet 5 of 9)

Registers  
Register Block

Address	Bit 7	6	5	4	3	2	1	Bit 0	Name
\$00BA	Bit 15	14	13	12	11	10	9	Bit 8	TC1H
\$00BB	Bit 7	6	5	4	3	2	1	Bit 0	TC1H
\$00BC	Bit 15	14	13	12	11	10	9	Bit 8	TC2H
\$00BD	Bit 7	6	5	4	3	2	1	Bit 0	TC2H
\$00BE	Bit 15	14	13	12	11	10	9	Bit 8	TC3H
\$00BF	Bit 7	6	5	4	3	2	1	Bit 0	TC3H
\$00C0	BTST	BSPL	BRLD	SBR12	SBR11	SBR10	SBR9	SBR8	SC0BDH
\$00C1	SBR7	SBR6	SBR5	SBR4	SBR3	SBR2	SBR1	SBR0	SC0BDL
\$00C2	LOOPS	WOMS	RSRC	M	WAKE	ILT	PE	PT	SC0CR1
\$00C3	TIE	TCIE	RIE	ILIE	TE	RE	RWU	SBK	SC0CR2
\$00C4	TDRE	TC	RDRF	IDLE	OR	NF	FE	PF	SC0SR1
\$00C5	SCSWAI	MIE	MDL1	MDL0	0	0	0	RAF	SC0SR2
\$00C6	R8	T8	0	0	0	0	0	0	SC0DRH
\$00C7	R7/T7	R6/T6	R5/T5	R4/T4	R3/T3	R2/T2	R1/T1	R0/T0	SC0DRL
\$00C8	BTST	BSPL	BRLD	SBR12	SBR11	SBR10	SBR9	SBR8	SC1BDH
\$00C9	SBR7	SBR6	SBR5	SBR4	SBR3	SBR2	SBR1	SBR0	SC1BDL
\$00CA	LOOPS	WOMS	RSRC	M	WAKE	ILT	PE	PT	SC1CR1
\$00CB	TIE	TCIE	RIE	ILIE	TE	RE	RWU	SBK	SC1CR2
\$00CC	TDRE	TC	RDRF	IDLE	OR	NF	FE	PF	SC1SR1
\$00CD	SCSWAI	0	0	0	0	0	0	RAF	SC1SR2
\$00CE	R8	T8	0	0	0	0	0	0	SC1DRH
\$00CF	R7/T7	R6/T6	R5/T5	R4/T4	R3/T3	R2/T2	R1/T1	R0/T0	SC1DRL
\$00D0	SPIE	SPE	SWOM	MSTR	CPOL	CPHA	SSOE	LSBF	SP0CR1
\$00D1	0	0	0	0	0	0	SPSWAI	SPC0	SP0CR2
\$00D2	0	0	0	0	0	SPR2	SPR1	SPR0	SP0BR
\$00D3	SPIF	WCOL	0	MODF	0	0	0	0	SP0SR
\$00D4	0	0	0	0	0	0	0	0	Reserved
\$00D5	Bit 7	6	5	4	3	2	1	Bit 0	SP0DR
\$00D6	PS7	PS6	PS5	PS4	PS3	PS2	PS1	PS0	PORTS
\$00D7	DDS7	DDS6	DDS5	DDS4	DDS3	DDS2	DDS1	DDS0	DDRS
\$00D8	0	0	0	0	0	0	0	0	Reserved
\$00D9	0	RDPS2	RDPS1	RDPS0	0	PUPS2	PUPS1	PUPS0	PURDS
\$00DA-\$00DF	0	0	0	0	0	0	0	0	Reserved
\$00E0-\$00ED	Unimplemented <sup>(4)</sup>								Reserved
\$00EE	0	0	0	0	0	0	EEDIV9	EEDIV8	EEDIVH

= Reserved or unimplemented bits.

**Table 4-1. MC68HC912D60A Register Map (Sheet 6 of 9)**

## Registers

Address	Bit 7	6	5	4	3	2	1	Bit 0	Name
\$00EF	EEDIV7	EEDIV6	EEDIV5	EEDIV4	EEDIV3	EEDIV2	EEDIV1	EEDIV0	EEDIVL
\$00F0	NOBDM <sub>L</sub>	NOSH <sub>B</sub>	Reserved	FPOOPEN <sup>(5)</sup>	1	EESWAI	PROTLCK	DMY	EEMCR
\$00F1	SHPROT	1	1	BPROT4	BPROT3	BPROT2	BPROT1	BPROT0	EEPROT
\$00F2	0	0	0	0	0	0	0	0	Reserved
\$00F3	BULKP	0	AUTO	BYTE	ROW	ERASE	EELAT	EEPGM	EEPROG
\$00F4	0	0	0	0	0	0	0	LOCK	FEE32LCK
\$00F5	0	0	0	0	0	0	0	BOOTP	FEE32MCR
\$00F6	0	0	0	0	0	0	0	0	Reserved
\$00F7	0	0	0	FEESWAI	HVEN	0	ERAS	PGM	FEE32CTL
\$00F8	0	0	0	0	0	0	0	LOCK	FEE28LCK
\$00F9	0	0	0	0	0	0	0	BOOTP	FEE28MCR
\$00FA	0	0	0	0	0	0	0	0	Reserved
\$00FB	0	0	0	FEESWAI	HVEN	0	ERAS	PGM	FEE28CTL
\$00FC-\$00FF	Unimplemented <sup>(4)</sup>								Reserved
\$0100	0	0	CWSWAI	SYNCH	TLNKEN	SLPAK	SLPRQ	SFTRES	CMCR0
\$0101	0	0	0	0	0	LOOPB	WUPM	CLKSRC	CMCR1
\$0102	SJW1	SJW0	BRP5	BRP4	BRP3	BRP2	BRP1	BRP0	CBTR0
\$0103	SAMP	TSEG22	TSEG21	TSEG20	TSEG13	TSEG12	TSEG11	TSEG10	CBTR1
\$0104	WUPIF	RWRNIF	TWRNIF	RERRIF	TERRIF	BOFFIF	OVRIF	RXF	CRFLG
\$0105	WUPIE	RWRNIE	TWRNIE	RERRIE	TERRIE	BOFFIE	OVRIE	RXFIE	CRIER
\$0106	0	ABTAK2	ABTAK1	ABTAK0	0	TXE2	TXE1	TXE0	CTFLG
\$0107	0	ABTRQ2	ABTRQ1	ABTRQ0	0	TXEIE2	TXEIE1	TXEIE0	CTCR
\$0108	0	0	IDAM1	IDAM0	0	IDHIT2	IDHIT1	IDHITO	CIDAC
\$0109-\$010D	Unimplemented <sup>(4)</sup>								Reserved
\$010E	RXERR7	RXERR6	RXERR5	RXERR4	RXERR3	RXERR2	RXERR1	RXERR0	CRXERR
\$010F	TXERR7	TXERR6	TXERR5	TXERR4	TXERR3	TXERR2	TXERR1	TXERR0	CTXERR
\$0110	AC7	AC6	AC5	AC4	AC3	AC2	AC1	AC0	CIDAR0
\$0111	AC7	AC6	AC5	AC4	AC3	AC2	AC1	AC0	CIDAR1
\$0112	AC7	AC6	AC5	AC4	AC3	AC2	AC1	AC0	CIDAR2
\$0113	AC7	AC6	AC5	AC4	AC3	AC2	AC1	AC0	CIDAR3
\$0114	AM7	AM6	AM5	AM4	AM3	AM2	AM1	AM0	CIDMR0
\$0115	AM7	AM6	AM5	AM4	AM3	AM2	AM1	AM0	CIDMR1
\$0116	AM7	AM6	AM5	AM4	AM3	AM2	AM1	AM0	CIDMR2
\$0117	AM7	AM6	AM5	AM4	AM3	AM2	AM1	AM0	CIDMR3
\$0118	AC7	AC6	AC5	AC4	AC3	AC2	AC1	AC0	CIDAR4

= Reserved or unimplemented bits.

Table 4-1. MC68HC912D60A Register Map (Sheet 7 of 9)

Registers  
Register Block

Address	Bit 7	6	5	4	3	2	1	Bit 0	Name
\$0119	AC7	AC6	AC5	AC4	AC3	AC2	AC1	AC0	CIDAR5
\$011A	AC7	AC6	AC5	AC4	AC3	AC2	AC1	AC0	CIDAR6
\$011B	AC7	AC6	AC5	AC4	AC3	AC2	AC1	AC0	CIDAR7
\$011C	AM7	AM6	AM5	AM4	AM3	AM2	AM1	AM0	CIDMR4
\$011D	AM7	AM6	AM5	AM4	AM3	AM2	AM1	AM0	CIDMR5
\$011E	AM7	AM6	AM5	AM4	AM3	AM2	AM1	AM0	CIDMR6
\$011F	AM7	AM6	AM5	AM4	AM3	AM2	AM1	AM0	CIDMR7
\$0120–\$013C	Unimplemented <sup>(4)</sup>								Reserved
\$013D	0	0	0	0	0	0	PUPCAN	RDPCAN	PCTLCAN
\$013E	PCAN7	PCAN6	PCAN5	PCAN4	PCAN3	PCAN2	TxCAN	RxCAN	PORTCAN
\$013F	DDCAN7	DDCAN6	DDCAN5	DDCAN4	DDCAN3	DDCAN2	0	0	DDRCAN
\$0140–\$014F	RECEIVE BUFFER								RxFG
\$0150–\$015F	TRANSMIT BUFFER 0								Tx0
\$0160–\$016F	TRANSMIT BUFFER 1								Tx1
\$0170–\$017F	TRANSMIT BUFFER 2								Tx2
\$0180–\$01DF	Unimplemented <sup>(4)</sup>								Reserved
\$01E0	Reserved								ATD1CTL0
\$01E1	Reserved								ATD1CTL1
\$01E2	ADPU	AFFC	ASWAI	DJM	R	R	ASCIE	ASCIF	ATD1CTL2
\$01E3	0	0	0	0	S1C	FIFO	FRZ1	FRZ0	ATD1CTL3
\$01E4	RES10	SMP1	SMP0	PRS4	PRS3	PRS2	PRS1	PRS0	ATD1CTL4
\$01E5	0	S8C	SCAN	MULT	SC	CC	CB	CA	ATD1CTL5
\$01E6	SCF	0	0	0	0	CC2	CC1	CC0	ATD1STAT0
\$01E7	CCF7	CCF6	CCF5	CCF4	CCF3	CCF2	CCF1	CCF0	ATD1STAT1
\$01E8	SAR9	SAR8	SAR7	SAR6	SAR5	SAR4	SAR3	SAR2	ATD1TESTH
\$01E9	SAR1	SAR0	RST	TSTOUT	TST3	TST2	TST1	TST0	ATD1TESTL
\$01EA–\$01EE	0	0	0	0	0	0	0	0	Reserved
\$01EF	PAD17	PAD16	PAD15	PAD14	PAD13	PAD12	PAD11	PAD10	PORTAD1

= Reserved or unimplemented bits.

**Table 4-1. MC68HC912D60A Register Map (Sheet 8 of 9)**

## Registers

Address	Bit 7	6	5	4	3	2	1	Bit 0	Name
\$01F0	Bit 15	14	13	12	11	10	9	Bit 8	ADR10H
\$01F1	Bit 7	Bit 6	0	0	0	0	0	0	ADR10L
\$01F2	Bit 15	14	13	12	11	10	9	Bit 8	ADR11H
\$01F3	Bit 7	Bit 6	0	0	0	0	0	0	ADR11L
\$01F4	Bit 15	14	13	12	11	10	9	Bit 8	ADR12H
\$01F5	Bit 7	Bit 6	0	0	0	0	0	0	ADR12L
\$01F6	Bit 15	14	13	12	11	10	9	Bit 8	ADR13H
\$01F7	Bit 7	Bit 6	0	0	0	0	0	0	ADR13L
\$01F8	Bit 15	14	13	12	11	10	9	Bit 8	ADR14H
\$01F9	Bit 7	Bit 6	0	0	0	0	0	0	ADR14L
\$01FA	Bit 15	14	13	12	11	10	9	Bit 8	ADR15H
\$01FB	Bit 7	Bit 6	0	0	0	0	0	0	ADR15L
\$01FC	Bit 15	14	13	12	11	10	9	Bit 8	ADR16H
\$01FD	Bit 7	Bit 6	0	0	0	0	0	0	ADR16L
\$01FE	Bit 15	14	13	12	11	10	9	Bit 8	ADR17H
\$01FF	Bit 7	Bit 6	0	0	0	0	0	0	ADR17L



= Reserved or unimplemented bits.

**Table 4-1. MC68HC912D60A Register Map (Sheet 9 of 9)**

1. Port A, port B and data direction registers DDRA, DDRB are not in map in expanded and peripheral modes.
2. Port E and DDRE not in map in peripheral mode; also not in map in expanded modes with EME set.
3. Registers also not in map in peripheral mode.
4. Data read at these locations is undefined.
5. The FPOpen bit is available only on the 1L02H and later mask sets. For previous masks, this bit is reserved.