Dissertation Preparation

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Abbreviations and Symbols

ANN   Artificial Neural Networks
BPTT   Backpropagation Through Time
CNN   Convolutional Neural Network
CPU   Central Processing Unit
FPGA   Field-Programmable Gate Array
LSTM   Long Short-Term Memory
RNN   Recursive Neural Networks
SPSA   Simultaneous Perturbation Stochastic Approximation

Chapter 1

Introduction

Brief overview of the report:

In Chapter 1, I will present a conceptual background to the problem at hand, exposing the background that surrounds it 1.1, the motivation for the desired solution 1.2, its objectives 1.3 and, lastly, the people that will help me achieve them 1.4.

In Chapter 2, the theoretical foundations will be layed out. Section 2.1.1 presents the basic concepts of Machine Learning, and in the following sections, the theoretical details of ANNs, RNNs and LSTMs. Section 2.1.4.2 provides a quick explanation of the training algorithm that will be used in the final solution, which will be outlined in Section 2.2.

In Chapter 3, the state of the art of LSTMs, their applications 3.1, their hardware implementations 3.2 and the current work regarding the chosen training algorithm 3.3 are presented.

In Chapter 4 I will present some of the work that I have already concluded.

Finally, in Chapter 5, the work plan for the Dissertation work is detailed as *tasks* in Section 5.1.1, and their temporal arrangement is pictured in a Gantt chart in Section 5.1.2. Furthermore, the description of the Hardware and Software resources that I will be utilizing during the course of my work is done in Section 5.2

1.1 Background

Artificial Neural Networks are one of the most popular models in the field of Machine Learning. As the name suggests, their operation is inspired by the operation of the building blocks of our brain, the **neurons**. In spite of its high performance, one of their shortcomings is the fact that they cannot retain temporal dependences among incoming data samples, thus not being suitable to process time-series data, such as audio, video or other kinds of time-varying data streams, where current inputs have a high temporal dependence with previous and future inputs.

To address this issue, several algorithms have been used, such as Hidden Markov Models (HMM) or Recurrent Neural Networks (RNN), but both of these methods fail to recall temporal dependences that extend over an large period of time, for the reasons that we will understand in Sections 2.1.3 and 2.1.4.Thus, in 1997 Hochreiter et al. proposed a novel RNN structure [3],

the Long Short-Term Network (LSTM), where a memory cell was introduced, and the input/output/read/write access is controlled by individual gates that are activated both by the incoming data samples, but also by the outputs from the previous time-step (it is an RNN after all). They are one of the state of the art methods in Deep Learning nowadays, as we can attest in Section 3.1.

1.2 Motivation

Hitherto, and to the best of my knowledge, all of the published applications that use LSTM are software based, but the parallel nature of the structure hollers for a dedicated hardware realization that can dramatically increase its performance, something that has only recently been done once [4] (see Section 3.2 for further details), and although it improves the processing time when compared to a naïve software solution, it still lacks the ability to perform on-chip learning, and the learning process is performed offline, in a normal CPU, when it also could be sped up by a dedicated hardware structure.

All these techniques are generally implemented in mainstream processors, making use of general high-level or low-level languages, where all the real parallelism is limited to the number of simultaneous threads that we can run on each physical core, which up to now generally have between 2-8 cores (mobile devices and general use personal computers),

In order to parallelize the computations to the fullest extent, a solution is to port it both to a Graphics Processing Unit (GPU) or even a Field-Programmable Gate Array (FPGA), but the porting process is not entierely automatic and to have the least performance drop possible, it has to be explicitly programmed in CUDA/OpenCL for GPUs, and a Hardware Description Language for FPGAs, with an increasing level of complexity and low-level details. Therefore, it is necessary to provide frameworks that can allow an FPGA to quickly reconfigure itself to run these kind of networks on demand, for a particular task that requires them, achieving a lower computation time, and unburdening the CPU from running it, thus saving performance for running other tasks related with the Operating System, for instance. Furthermore, when processing an incoming stream of highly dimensional data, or with high throughput, a CPU solution might not be scalable, and could benefit greatly from a dedicated hardware implementation.

1.3 Objectives

Taking into account the considerations done in 1.2, I propose to develop a hardware implementation of an LSTM Network, *with on-chip learning*, improving the performance, capability and flexibility of the existing solution of [4]. Moreover, I also propose to benchmark this solution and try to compare it with the software performance results of [5] and, as a secondary objective, try to use my developed structure to replicate some of the applications portrayed in 3.1. Lastly, I will work to make this structure reconfigurable on the go, and trying to minimize the reconfiguration time.

1.4   People Involved

Besides me, the candidate to the Master's Degree, there are two more people involved, namely

- **Supervisor** – The Professor João Canas Ferreira, auxiliary professor at the Faculty of Engineering of the University of Porto.

- **Second Supervisor** – Ivo Timóteo, MSc, a Computer Science PhD candidate at Cambridge University, UK, in the field of Artificial Inteligence.

Chapter 2

Problem Characterization

2.1 Theoretical Background

2.1.1 Basic Concepts of Machine Learning

Machine Learning is a field of Computer Science that studies the development of mathematical techniques that allow software to learn autonomously, without an explicit description of each rule of operation. Its goal is to extract latent features from the data that allow an immediate classification of each input data into a particular class – the catch is that there is no previous rule formulation, but instead we have an adaptive model that adjusts is parameters according to the input data it receives, improving the estimates it yields as it receives new input samples.

Let us consider a practical example. For instance, suppose we want to build a program that given an input audio waveform representation of a spoken word, it matches it into a particular word of a dictionary. We could, of course, devise a set of rules and exceptions for each word analysing some of its features (perhaps the Fourier representation of each one, and, from it, manually finding the appropriate rules for each), but apart from being a very complex task, it wouldn't be a scalable solution, given the enormous number of words in each language. The approach taken by Machine Learning is different, and instead of manually processing each waveform, we build a large dataset, of size N, containing the waveforms of several words $[\mathbf{x}_1, \mathbf{x}_2, \mathbf{x}_2, \ldots, \mathbf{x}_N]$ – we call this dataset the **training dataset** – and we feed it to our model. Each of the i-th data point was previously labelled, and in fact we feed each training data point $\mathbf{x}_i$ *along* with its corresponding label t_i, so that the model can adapt its parameters accordingly to the *target value* it is supposed to classify. This set of labels $\mathbf{t} = [t_1, t_2, t_3, \ldots, t_N]$ is called the **target vector**.

We are, then, left with the following question: how can the model quantitatively evaluate the quality of its current set of parameters? That could be achieved in a number of ways, but the most usual is using a **Cost Function** that, as the name suggests, measures the cost of each wrong classification of the model. The model then evolves in a way that minimizes the cost function. A usual choice for the cost function is the **sum of squares error**, given the Gaussian

Noise assumption. Mathematically, if $y_\theta^i = y_\theta(x_i)$ is the prediction for the input data point x_i with label t_i, given the current set of parameters θ, the cost function using this metric is given by

$$J(\theta) = \frac{1}{2} \sum_{i=1}^{N} \left(y_\theta^i - t_i\right)^2.$$

(2.1)

Sometimes, instead of applying the raw data to the model, we can apply some sort of *preprocessing* to the data to extract the relevant features from it. For instance, instead of just feeding a raw image, we can perform several operations like edge detection or low-pass filtering, and apply them in parallel. In cases of highly dimensional data (i.e. each data vector has a very high number of features), we can apply techniques like **Principal Component Analysis** to reduce the feature space to a smaller dimension one, where the previous features were combined into two or three new features that pose themselves as the most relevant.

The problems described above are, in fact, a subset of the problems that Machine Learning tries to address. These problems are called **classification problems**, because for each input data point, our model tries to fit it into the most appropriate class. But we can also address **regression problems** where the output is not limited to a discrete set of values but rather a continuous interval. On the other hand, the Neural Network that this work will implement addresses a special kind of classification problem, where the classification decision is influenced not only by the current input sample, but also by a given *window of samples* that trail the current sample.

In summary, the most typical setting for a Machine Learning problem is having a large *input dataset* which we use to *train* our model (i.e. allowing him to dynamically adapt its set of parameters θ), in order to produce an output label y_i for each of them that minimizes a quality metric, the *Cost Funcion*, which can be chosen to the sum of squared differences, the log-loss, or any other appropriate mathematical relationship between the estimate y_i and the correct label t_i.

Now that the basic Machine Learning concepts have been presented, I will discuss, henceforth, one of the most important algorithms that address the supervised classification problems, the *Artificial Neural Networks* that will be discussed in Section 2.1.2 as a contextual introduction to the main theme of the thesis, which will be Recurrent Neural Networks (Section 2.1.3), namely the **Long Short-Term Memory Networks** (Section 2.1.4), both of which are improvements over the initial formulation of the ANNs. These two last networks branch even further from these set of problems, and are usually employed in *Deep Learning* tasks, where we try to extract even higher level information from data at the expense of increased model complexity.

2.1.2   Artificial Neural Networks

Artificial Neural Networks (ANN) are mathematical structures that, as the name suggests, try to mimic the basic way of how a human brain works. ANN's building blocks, like their biological counterpart, model the high-level behaviour of biological neurons, in the sense that they neglect unnecessary biological aspects (such as modeling all the voltages across the neuron and all its electromagnetic interactions), and only retain its fundamental underlying mathematical function,

which is a weighted linear combination of its inputs subject to a *activation function*, i.e. a function that outputs a decision value depending on its inputs. Mathematically, we have

$$y = f(\mathbf{w}^T \mathbf{x}) \tag{2.2}$$

where $\mathbf{w} = [w_0 \ w_1 \ w_2 \ w_3 \ \dots \ w_n]$ is the input weight vector, $\mathbf{x} = [x_0 \ x_1 \ x_2 \ x_3 \ \dots \ x_n]$ the input vector, b_0 is the bias factor and $f(\cdot)$ is the chosen activation function. Furthermore, we call the scalar quantity $a = \mathbf{w}^T \mathbf{x}$ the **activation**, since its value determines how the activation function will behave. Figure 2.1 exemplifies the roles of these variables within our neuron model, and compares each part of it with the biological counterpart.
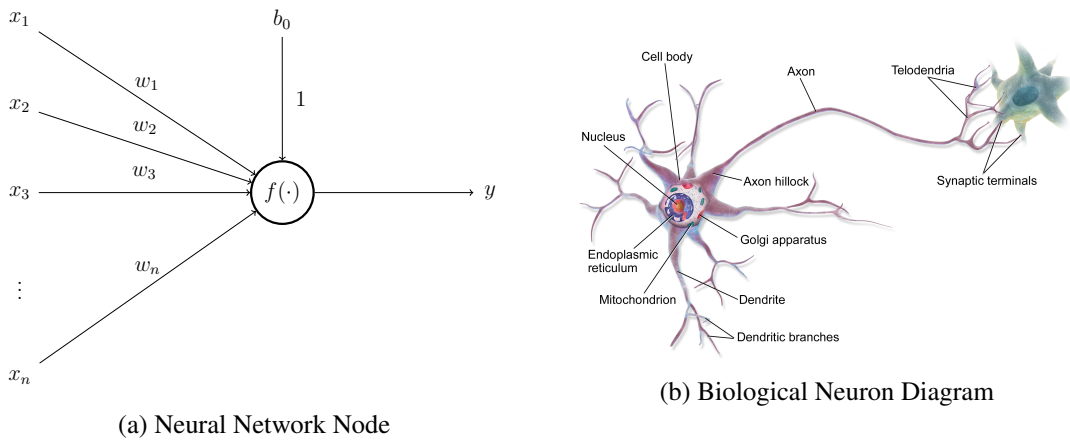

(a) Neural Network Node

(b) Biological Neuron Diagram

Figure 2.1: In Figure 2.1a. each input feature x_i is weighted by its corresponding weight w_i. During the training procedure, these weights are adjusted so that the output y approaches the target value. In Figure 2.1b, we see the diagram of an actual multi polar neuron. The dendrites, where the stimuli are received, plays a role similar to that of the input nodes. The axon transmits the signal to the synaptic terminals, that are similar to the y output. Source: Wikipedia

As far as the activation function is concerned, we can have several types. An immediate choice would be the **Binary Step Function** that outputs -1 if the activation is **below** a given threshold and 1 otherwise. There can also be **real valued activation functions**, whose output is not binary, but rather that of a continuously differentiable function, such as the logistic sigmoid $\sigma(a) = \frac{1}{1+e^{-a}}$ or the hyperbolic tangent $\tanh(a)$. This aspect will prove useful for the usual training methods, that involve the computation of derivatives. In Figure 2.2 these activation functions are plotted.
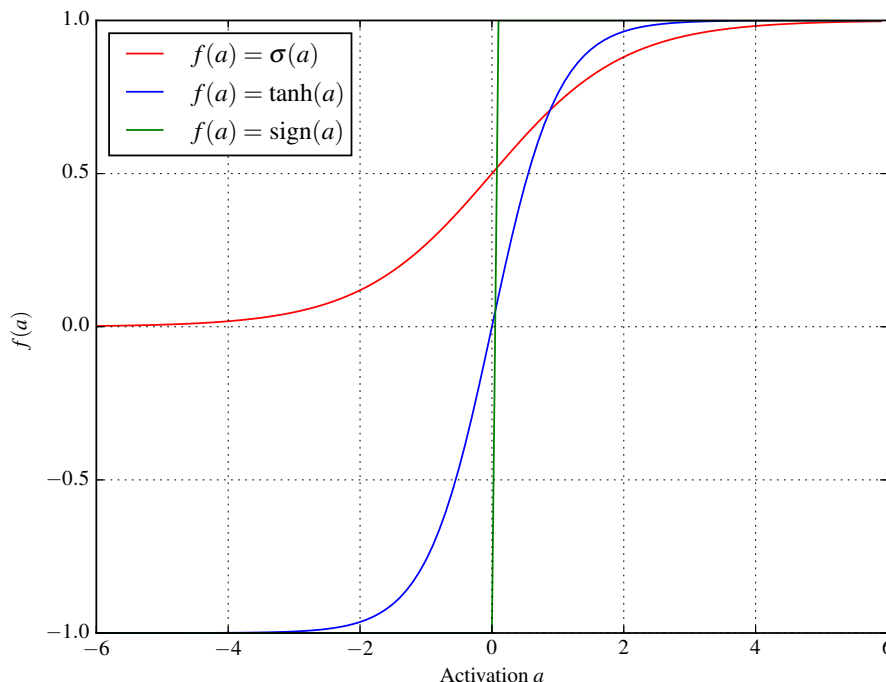
Figure 2.2: Three different activation functions. As you can see, the hyperbolic tangent has the same extreme values as the sign step function, but has a smooth transition between them, which can be interpreted as a *soft decision* in the more ambiguous middle region, reflecting the degree of uncertainty on the decision. On the other hand, the sigmoid function goes from zero to one, and is also smooth like the hyperbolic tangent.

A neuron by itself can be thought of as a simple linear regression, where we optimize the weight of each feature according to a target value, or function. While important in some applications, the main interest in ANN is to evaluate increasingly more complex models, and not a simple linear regression. This is achieved by *chaining* nodes to one another, connecting the output of a given node to one of the inputs of another. We call *layers* to a group of these nodes that occupy the same hierarchical position. There can be any number of layers, with any number of nodes, but most implementations generally have 3 layers: the *input* layer, the *hidden* layer (in the middle) and the *output* layer. Figure 2.3 suggests a possible structure for a 3 layer ANN.

Figure 2.3: A three layer ANN. We have omitted some of the connections in the hidden layer, for simplification purposes. $\mathbf{w}_1$ represents the weight matrix of the input layer, $\mathbf{w}_2$ the weight matrix of the connections between the input layer and the hidden layer, and $\mathbf{w}_3$ the weight connections between the hidden and the output layer. $f_{ij}(\dots)$ is the activation function of the j-th neuron of the i-th layer. Since they can be different, I chose different indexes to each.

Regarding the training of ANNs, it is performed through a two-step process: first, a **feedforward** step where the input is applied, and the activations are evaluated in succession up to the output neurons; then, we perform the **backpropagation** step, where we calculate the errors in each of the nodes (the so-called **deltas** of equation 2.5), but now from the output to the input: the weights are updated and optimized using an iterative method called *Gradient Descent*, where if τ is the current time step, the next update on the weight matrix $\mathbf{w}^{(\tau+1)}$ is given by

$$\mathbf{w}^{(\tau+1)} = \mathbf{w}^{(\tau)} - \eta \nabla E(\mathbf{w}^{(\tau)}) \tag{2.3}$$

where $E(\cdot)$ is the error function. As we can see, the weight matrix is moved in the direction that minimizes the error function the most, and η controls how fast this is achieved, being the reason why it is called the **learning rate**.

The computation of gradient of the error function comprises the evaluation of its derivatives with respect to each weight of all network connections, w_{ij}. They are

$$\frac{\partial E}{\partial w_{ji}} = \delta_j f(a_i) \tag{2.4}$$

where $f(\cdot)$ is the activation function of the neuron and

$$\delta_j = f'(a_j) \sum_k w_{kj} \delta_k. \tag{2.5}$$

The interpretation of these equations is simple. If w_{ji} is the weight of the connection between the neuron j we are considering and a neuron i in a previous layer, then the sum over k relates to all the neurons in the *next* layer to which j connects: this way, since the update of w_{ji}, according to 2.3, is given by

$$w_{ji}^{(\tau+1)} = w_{ji}^{(\tau)} - \eta \frac{\partial E}{\partial w_{ji}} \tag{2.6}$$

we see that, from 2.4 it simply is the product of the error of the current neuron, δ_j, with the output of the previous neuron $f(a_i)$. In turn, from 2.5, we see the recurrence relationship between it and the weighted sum of all posterior neurons that connect to it. Hence, the name backpropagation is now clear: we are, in fact, propagating the errors backwards into the neuron of interest, weighted by the corresponding weight, but now *backwards* instead of forward, as before. For the output units, the δ_j is simply the difference between the produced output and the corresponding label for that sample. This two-step process is performed for every data point in out dataset. For a complete proof of the above formulas, see [6, chap. 5.3.1].

2.1.3   Recurrent Neural Networks

A Recurrent Neural Network (RNN) is, essentially, a regular ANN where some neurons (especially in the hidden layer) have *feedback connections* to themselves, i.e. their outputs are fed as inputs. The relevance of this different structure is the possibility to retain *sequence* information about the data. Before, each incoming data point only contributed to the training of the network, but the information about the correlation between themselves and the data points that preceded them did not influence the training step. Temporal relationship is disregarded and each data point considered conditionally independent of any other. This is obviously not necessarily true, and in fact there are many cases where the correlation between data points is high for those closely spaced in time, such as in video signals, audio signals, or other kinds of *temporal sequences* of data. Therefore, the feedback connection of the neuron to himself acts as a kind of *memory element* that takes into account in the present decision, the history of decisions previously taken, and hence the previous data.

Figure 2.4 suggests a possible structure for a neuron of a hidden layer in an RNN, and also an alternate representation, where the structure is unfold through time.
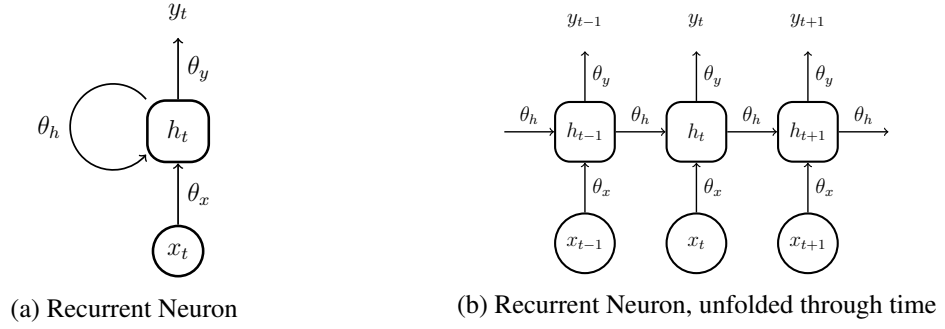
(a) Recurrent Neuron

(b) Recurrent Neuron, unfolded through time

Figure 2.4: In Figure 2.4a, a recurrent neuron is depicted, where the output is fed back to the input, weighted by θ_h. Figure 2.4b, an unfolding through time of that same neuron is performed. The basic idea is that feeding the output back to the input is similar to feeding the output to the input of the neuron *at a previous time step*: this way, we linearize the structure. Considering a training epoch of T samples, corresponds to having T unfolded neurons/layers

The training of an RNN is usually performed using a variation of Backpropagation, called **Backpropagation Through Time** (BPTT), that as the name implies, performs the same back-propagation procedure discussed for the ANNs, but now taking into account the unfolding of the network through a fixed training epoch T like Figure 2.4b. Due to this very fact, this training procedure is memory and performance consuming, and so it will not be used in my final work, but instead a novel approach, the **Simultaneous Perturbation Stochastic Approximation** will be evaluated.

Even though RNNs outperform static ANNs in sequence recognition problems [7], they fail to retain long-term dependencies. Of course that the weight training process is itself a form of memory, but the problem is that the weight update is much slower than the activations [8], and therefore this memory only retains short-term dependencies. This is because of the so-called **Vanishing Gradients Problem** [9, 8], where the error decays exponentially through time, and the impact of previous incoming data points on the training of the weights, and thus the current decision, quickly decreases.

2.1.4 Long Short-Term Memory Networks

To overcome the issue of failing to remember long-term dependencies, Hochreiter and Schmid-hüber proposed, in 1997, a novel approach to the RNNs called the *Long-Short Term Network* [3]. This section explains the main idea of this approach (Section 2.1.4.1), and also how it is trained (Section 2.1.4.2), serving as a support for the work of this thesis. Although originally formulated in 1997, its formulation has been incrementally updated in [10] and [11], and the most current version is the one in [1]. One of the inital proposers of LSTM, Prof. Jürgen Schmidhüber, did a survey on the most common variations of the model last year [2], and this will the basis of this short theoretical presentation, as well as the work that will be developed in this thesis.

2.1.4.1 Structure, Operation and Equations

A single LSTM neuron is presented in Figure 2.5. As we can see from the picture, we still have the recurrent connections from the regular RNNs, but now there are multiple entry points that control the flow of information through the network. Although omitted from the picture, all the gates are biased, as is suggested in Equations 2.7. The main components, their role and relevance, are explained as follows
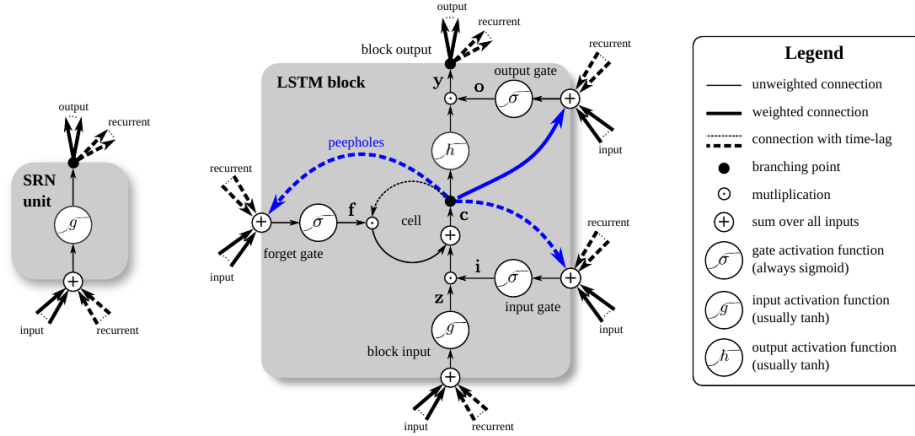

Figure 2.5: A complete LSTM neuron, with all the features as described in [1]. Source: [2]

- **Input Gate** – this is the input gate, where the importance of each feature of the input vector at time t, $\mathbf{x}^t$, and the output vector at the previous time step $\mathbf{y}^{t-1}$ is weighed in, producing an output $\mathbf{i}^t$.

- **Block Input Gate** – as the name implies, this gate controls the flow of information from the input gate to the memory cell. It also receives the input vector and the previous output vector as inputs, but it does not have peephole connections and its dynamics are controlled by a different set of weights. The **activation function of this gate can be either**, but the most common choice is the **Hyperbolic Tangent**.

- **Forget Gate** – its role is to control the contents of the Memory Cell, either to set them or reset them, using the *Hadamard Elementwise* matrix multiplication of its output at time t, $\mathbf{c}^{(t)}$, with the contents of the memory unit at the previous time step, $\mathbf{c}^{(t-1)}$. The activation function of this gate is **always sigmoid**.

- **Output Block Gate** – this gate has a role very similar to that of the Block Input Gate, but now it controls the information flow *out* of the LSTM neuron, namely the activated Memory Cell output.

- **Memory Cell** – the cornerstone of the LSTM neuron. This is the memory element of the neuron, where the previous state is kept, and updated accordingly to the dynamics of the gates that connect to it. Also, this is where the peephole connections come from.

- **Output Activation** – the output of the Memory Cell goes through this activation function that, as the gate activation function, can be any, but the *hyperbolic tangent* is the most common choice.

- **Peepholes** – direct connections *from* the memory cell that allow for gates to 'peep' at the states of the memory cell. They were added after the initial 1997 formulation, and their absence was proven to have a minimal performance impact [2].

After these small conceptual definitions, that allow us to grasp some intuition on the operation of a *single* LSTM cell, I can present the overview of a *layer* of LSTM neurons and their formal mathematical formulation, that will be needed both for the high-level model and the HDL description. The operation of each set of gates of the layer is given by the following set of equations

$$\mathbf{z}^{(t)} = g(\mathbf{W}_z\mathbf{x}^{(t)} + \mathbf{R}_z\mathbf{y}^{(t-1)} + \mathbf{b}_z)$$
$$\mathbf{i}^{(t)} = \sigma(\mathbf{W}_i\mathbf{x}^{(t)} + \mathbf{R}_i\mathbf{y}^{(t-1)} + \mathbf{p}_i \odot \mathbf{c}^{(t-1)} + \mathbf{b}_i)$$
$$\mathbf{f}^{(t)} = \sigma(\mathbf{W}_f\mathbf{x}^{(t)} + \mathbf{R}_f\mathbf{y}^{(t-1)} + \mathbf{p}_f \odot \mathbf{c}^{(t-1)} + \mathbf{b}_f)$$
$$\mathbf{c}^{(t)} = \mathbf{i}^{(t)} \odot \mathbf{z}^{(t)} + \mathbf{f}^{(t)} \odot \mathbf{c}^{(t-1)}$$
$$\mathbf{o}^{(t)} = \sigma(\mathbf{W}_o\mathbf{x}^{(t)} + \mathbf{R}_o\mathbf{y}^{(t-1)} + \mathbf{p}_o \odot \mathbf{c}^{(t)} + \mathbf{b}_o)$$
$$\mathbf{c}^{(t)} = \mathbf{o}^{(t)} \odot h(\mathbf{z}^{(t)}) \tag{2.7}$$

where $\odot$ is the Hadamard multiplication. The *i*-th element of the previous vectors in bold corresponds to the value of the gate of the *i*-th neuron of the layer, which is a very convenient and compact representation of the whole layer. Furthermore, if the layer has *N* LSTM neurons and *M* inputs (i.e. the size of the layer that precedes this), we see that the input weight matrices $\mathbf{W}_*$ and the recurrent weight matrices $\mathbf{R}_*$ all have size $N \times M$, and that the bias weight matrices $\mathbf{b}_*$, the peephole weight matrices $\mathbf{p}_*$ and the matrices $\mathbf{z}^{(t)}$ through $\mathbf{c}^{(t)}$ have size $N \times 1$. Although useful for a high-level description in a programming language, the matrix representation may not be suitable for a direct HDL port. In that case, in order to represent the operation of the *i-single neuron*, all the above equations still hold, but instead of *vectors* of outputs, we will have a single scalar output, and we only use the appropriate row in the weight matrices $\mathbf{W}_*$, $\mathbf{R}_*$ and the remaining.

2.1.4.2 Training – SPSA

Since this work aims to perform on-chip learning, it is important to find a suitable learning scheme. Since I am aiming at an hardware implementation, and although the memory resources of current FPGAs are abundant, one must find an algorithm that uses the less memory as possible (at the smallest performance cost possible), in order to use the additional memory, for instance, to add additional LSTM cells that can improve the performance of our system. That being said, we see that the usual training algorithms for LSTM cells – i.e. Real-Time Recurrent Learning (RTRL),

Truncated Backpropagation Through Time (BPTT) or a mixture of both [1] [3] [2] – usually involve the storage of the deltas of each layer for every time instant in the training epoch (from 0 to T), which is a highly non-scalable solution both in terms of memory and performance. A most efficient approach to training times series dependant structures like LSTM is the use of **Simultaneous Perturbation Stochastic Approximation** (SPSA) [12]. The main idea of this technique is, instead of explicitly evaluating the gradients for the cost function at each time step, to perform a random walk in the neighbourhood of the current weight matrix, in the weight space, and approximate the new weight update by the approximation of the gradient of the cost function that resulted from that random walk. The weight update for the i-th weight at the time step t is given by

$$\Delta w_i^{(t)} = \frac{J(\mathbf{w}^{(t)} + \beta \mathbf{s}^{(t)}) - J(\mathbf{w}^{(t)})}{\beta s_i^{(t)}} \tag{2.8}$$

where β is the magnitude of the perturbation to be introduced, $\mathbf{s}^{(t)}$ is a *sign vector* whose i-th element, $s_i^{(t)}$, is either -1 or 1. This way, we see that every weight is **randomly** incremented either by $-\beta$ or β, and we only need to keep a duplicate of the weight matrix with the perturbations, and we only need to evaluate the cost function twice per incoming sample. As for the *update rule*, we have

$$w_i^{(t+1)} = w_i^{(t)} - \eta \Delta w_i^{(t)} \tag{2.9}$$

where η is the learning rate, and $\Delta w_i^{(t)}$ is the update for the i-th weight evaluated in 2.8. According to the analysis performed in [13], performing a two-term Taylor expansion at $\mathbf{w} = \mathbf{w}^{(t)}$, and taking the expected value of the equation, we get that there is a $\mathbf{w}_{S1}$ so that

$$\Delta w_i^{(t)} = s_i^{(t)} (\mathbf{s}^{(t)})^T \frac{\partial J(\mathbf{w}^{(t)})}{\partial \mathbf{w}} + \frac{c s_i^{(t)}}{2} (\mathbf{s}^{(t)})^T \frac{\partial^2 J(\mathbf{w}^{(t)})}{\partial \mathbf{w}^2} (\mathbf{s}^{(t)}) \tag{2.10}$$

If the random sign vector $\mathbf{s}^{(t)}$ is chosen carefully so that the expected value of the vector at the i-th position is zero, $E(s_i^{(t)})$, and the signs of two different components i and j, at different time-steps, are independent (i.e. $E(s_i^{(t_1)} s_j^{(t_2)}) = \delta_{ij} \delta_{t_1 t_2}$, where δ is the Kronecker fuction), taking the *Expected Value* of equation 2.10 yields

$$E(\Delta w_i^{(t)}) = \frac{\partial J(\mathbf{w}^{(t)})}{\partial w_i^{(t)}} \tag{2.11}$$

that is, the *expected value* of the weight update approximates the gradient of the cost function relative to that weight, and so the learning rule is a special form of *Stochastic Gradient Descent*.

One last comment to be made concerning the update rule, is the hypothetical need for **limits** to the weight values, when the update rule exceeds $|w_{\max}|$ (in that case, we set $w_i^{(t+1)} = \pm w_{\max}$), which sometimes might be needed if the behaviour of the weight update is not appropriate [13].

2.2   Proposed Solution

Given the previous discussion of how LSTM neurons work and their benefits when compared to other RNN architectures, this work aims to conceive and design an efficient dedicated FPGA implementation with on-chip learning that, surpasses the training/testing time of an equivalent CPU implementation in a general high-level language or of a framework (see Section 5.2).

As discussed in Chapter 3, up to now there is only one FPGA implementation of LSTM cells [4], but there is no on-chip learning on the architecture (the weights are learned offline, and loaded in the FPGA before operation, and they are not changed while the FPGA system is operating), and my proposed work will implement an efficient LSTM implementation *with* the ability to learn on-chip, which is an innovative and useful feature for the LSTM architecture on a dedicated hardware implementation. I will achieve that using the SPSA method described in 2.1.4.2, and inspired in the previous work of [13].

This solution will combine the benefits of a dedicated hardware implementation, where the inherent parallelism so obviously visible in the network architecture can be fully exploited something that, predominantly, yields a much higher performance in terms of computation time than a naïve CPU implementation (as in [13] where a $21\times$ speed-up against an ARM CPU was acheived) with the flexibility that a reconfigurable platform such as an FPGA provides.

Chapter 3

State of the Art

Over the course of this chapter, I am going to present an overview of the most recent developments related to the work of this thesis, both in terms of existing dedicated hardware implementations 3.2, the most relevant work in adapting suitable training algorithms to hardware 3.3 and also some of the most relevant applications of LSTM 3.1, which are not FPGA-based, but demonstrate how LSTM are useful by themselves, and how well it competes with other Machine Learning algorithms in terms of long time-series dependences in data.

3.1 LSTM Applications (non-FPGA related)

LSTM Networks are nowadays one of the state of the art algorithms in deep-learning, and their performance is superior to that of other kinds of RNNs and Hidden Markov Models, both of which are generally used to address the same set of problems where LSTM are employed, namely predicting and producing classification decisions from time-series data. A very comprehensive description of applications can be found in one of the initial authors webpage dedicated to the subject [1]. I will now enumerate some of the leading edge applications of LSTM.

- **Handwriting Recognition** – an LSTM-based network [14], submitted by a team of the Technische Universität München, won the 2009 ICDAR Handwriting Recognition Contest, achieveing a recognition rate of up to 91% [15]. LSTMs have also proven to surpass HMM-based models in terms of optical character recognition of printed text, as [16] suggests.

- **Speech Recognition** – an architecture[17] proposed by Graves et al. in 2013 achieved an astonishing 17.7% of accuracy on the TIMT Phoneme Recognition Benchmark, which up to the date is a new record. Furthermore, it has also been used for large scale acoustic modelling of speech [18].

- **Handwriting Synthesis** – a comprehensive study by Graves shows, among other sequence generation tasks such as Text Prediction, that use of LSTM to produce synthetic handwriting, that looks incredibly similar to human-produced handwriting [19].

---

[1]http://people.idsia.ch/ juergen/rnn.html

- **Translation** – LSTM was used by Sutskever et al. (Google) to perform sequence-to-sequence translation on the WMT'14 dataset, translating English to French with a close to state of the art score [20].

- **Biomedical Applications** – this network architecture was used in a protein homology detection scheme [21] using the SCOP 1.53 benchmark dataset, displaying a good performance when compared to other methods. Similarly, a recent article from 2015 by Sønderby et al. suggested the use of standalone LSTM and also Convolutional LSTM to perform sub cellular localization of proteins, given solely their protein sequence, with an astounding accuracy of 0.902 [22]

- **Music Analysis and Composition** – Lehner et al. proposed a low-latecy solution based on LSTM, suitable for real-time detection of a singing voice in music recordings [23] whose performance surpassed other baseline methods, with lower latency. In terms of music transcription from audio data, there is a study that proposes the use of LSTM cells to perform a transcription of piano recordings to musical notes [24], in order to automate music transcription. The model was trained with recordings of both acoustic pianos and synthesized pianos, and the labelling was performed using an associated MIDI file for each piece that was used in the training, showing promising results. [25] suggests the use of LSTM to perform autonomous computer music composition, and Eck and Schmidhüber proposed LSTM to perform Blues improvisation in [26].

- **Video and Image Analysis** – Vinyals et al., at Google, proposed an LSTM network for **image captioning**, preceded by a Convolutional Neural Network (CNN) to apply preprocessing to the images [27]. The LSTM works as *sentence generator*, that captions the images with state of the art performance. Besides image captioning, video captioning is also an interesting topic. Venugopalan et al. recently proposed a CNN + LSTM architecture to translate video sequences to natural language [28], using the Microsoft Research Video Description Corpus as a dataset.There are other similar studies that combine image and video captioning [29].

3.2 Hardware Implementations of LSTM

Hitherto, there is but one actual implementation of an LSTM network in hardware, published recently (November 2015) by Chang et al. [4] in the Computing Research Repository (CoRR). It consists on the proposal of an LSTM cell architecture for dedicated hardware, targeting a Xilinx® Zedboard implementation. It uses a character-level language model from Andrej Karpathy [2], written in Lua using the Torch7 framework [3] (the Lua calls are implemented in C, so no performance is lost).

---

[2]https://github.com/karpathy/char-rnn
[3]http://torch.ch/

Although the article is not clear on whether there is active learning by the ARM CPU – the authors refer that the CPU loads the weights before operation, and that it changes them during operation, although how and why that change is done is not even clearly explained, neither mathematically nor conceptually –, **there is no on-chip learning module** in the FPGA according to the description provided.

The implementation itself makes an extensive use of the Multiply-and-Accumulate units (MAC) of the FPGA, which since they are limited in number in the target platform, limits the number of neurons that we can deploy in parallel. The authors report a nearly 75% usage for only 8 LSTM neurons. Although an apparently excessive number, I am left to scrutinize whether the usage of MACs is compulsory to obtain a better performance than a CPU or if it can be discarded, allowing for smaller cells. This way, we can have a layer of more neurons occupying the same area and, hopefully, the same, or even fewer, resources within the FPGA.

3.3   Training Algorithms and Implementation

As stated in 3.2, the work of [4] does not feature on-chip learning at FPGA level, although there are a handful proposed solutions for it in recent literature. I will particularly look into the ones that use SPSA (see Section 2.1.4.2), since that is the training algorithm of choice for my proposed solution, and also to the ones that particularly apply SPSA to the training of Neural Networks.

The SPSA algorithm was initially published by Spall in [12], and its theoretical details are outlined in Section 2.1.4.2. As to its applications to the training of general Neural Networks, the earliest examples come from 1995 and 1996 in [30, 31] where SPSA is used to train a VLSI *Analog* Neural Networks, a time where the memory resources of digital circuitry were limited, and so most of these structures were analog-based. Its adequacy was also established for **control problems**, such as those proposed in [32], where a Time Delay Neural Network is used to control an unknown plant in a linear feedback system.

In 2005, Maeda and Wakamura published a proposed SPSA hardware implementation [13] to train an Hopfield Neural Network in an FPGA (and thus a digital system), achieving promising results in an Altera FPGA. The article carefully delineates the approach taken, and also the hardware architecture designed, so it is a very good reference for the design that I will have to implement.

Furthermore, a 2013 article by Tavear et al. [5] proposes, for the first time, using SPSA to train LSTM Neurons, although the article focuses on proving the suitability of SPSA to LSTM, and no actual hardware implementation is done or proposed. The authors simply demonstrate the suitability using conceptual arguments and by building a software model of an SPSA-trained LSTM network, and by comparing both the performance and computing speed of their model with the results achieved by Hochreiter et al. in [21]. Since the forward phase in both regular LSTM and SPSA-trained LSTM is the same, the computation time suffers no performance penalty whatsoever and the learning ability is preserved to a high degree, showing that SPSA is a valid alternative do BPTT and other similar and more common training schemes.

3.4   Final Overview

As we could attest from this small literature survey, although there is already an hardware imple-
mentation of LSTM, there is still a good deal of room for improvement by adding on chip-learning
to the system, and also to restrict it to a smaller use of the FPGA resources, allowing it to acco-
modate a more complex network. Furthermore, [5] shows that, at least for that particular case, the
LSTM network doesn't suffer a great performance impact from using SPSA training, as opposed
to the more common BPTT, and [13] showed that an SPSA hardware implementation is feasi-
ble. These three conclusions combined indicate that the idea of a hardware LSTM network with
on-chip learning using SPSA is viable.

Besides the proposed hardware implementation, it would be advantageous to perform *bench-
marking* to see how well it compares with software solutions, and Section 3.1 suggests a handful
of examples to test my final solution.

Chapter 4

Early Work

In order to better undesrtand LSTM, gain some useful insight on their operation, and to have a software implementation, that is not part of any framework, with which I can validate in the future my FPGA implementation, I have developed a fully functional LSTM Layer in Python and Numpy, that still uses BPTT as a training algorithm (the governing equations are in appendix A of [2]). The idea is to adapt it to use SPSA in the beginning of my Master's work. The code is present in

```python
1  # -*- coding: utf-8 -*-
2  """
3  LSTM Layer Class
4  @author: Jose Pedro Castro Fonseca, University of Porto, PORTUGAL
5  """
6  import numpy as np
7  import time
8
9  # Defines the seed for random() as the current time in seconds
10 np.random.seed(round(time.time()))
11
12 # Evaluates the Sigmoid Function
13 def sigmoid(x):
14     output = 1/(1+np.exp(-x))
15     return output
16
17 # Evaluates the derivative of the Sigmoid Func, based on a previous sigmoid() call
18 def sigmoidPrime(output):
19     return output*(1-output)
20
21 # Evaluates the derivative of the TanH Func, based on a previous np.tanh() call
22 def tanhPrime(output):
23     return (1-output**2)
24
25 class LSTMlayer :
26
27     def __init__(self, inputUnits, hiddenUnits, learnRate, T):
28         # The Network Parameters, passed by the user
29         self.inputUnits  = inputUnits
30         self.hiddenUnits = hiddenUnits
31         self.learnRate   = learnRate
32         self.T           = T
```

```
33          self.t           = 0
34
35          # Initializing the matrix weights
36          #LSTM Block
37          self.Wz = np.random.random((hiddenUnits, inputUnits)) - 0.5
38          self.Wi = np.random.random((hiddenUnits, inputUnits)) - 0.5
39          self.Wf = np.random.random((hiddenUnits, inputUnits)) - 0.5
40          self.Wo = np.random.random((hiddenUnits, inputUnits)) - 0.5
41
42          self.Rz = np.random.random((hiddenUnits, hiddenUnits)) - 0.5
43          self.Ri = np.random.random((hiddenUnits, hiddenUnits)) - 0.5
44          self.Rf = np.random.random((hiddenUnits, hiddenUnits)) - 0.5
45          self.Ro = np.random.random((hiddenUnits, hiddenUnits)) - 0.5
46
47          self.pi = np.random.random((hiddenUnits)) - 0.5
48          self.pf = np.random.random((hiddenUnits)) - 0.5
49          self.po = np.random.random((hiddenUnits)) - 0.5
50
51          self.bz = np.random.random((hiddenUnits)) - 0.5
52          self.bi = np.random.random((hiddenUnits)) - 0.5
53          self.bo = np.random.random((hiddenUnits)) - 0.5
54          self.bf = np.random.random((hiddenUnits)) - 0.5
55
56          # Updates
57          self.Wz_update = np.zeros_like(self.Wz)
58          self.Wi_update = np.zeros_like(self.Wi)
59          self.Wf_update = np.zeros_like(self.Wf)
60          self.Wo_update = np.zeros_like(self.Wo)
61
62          self.Rz_update = np.zeros_like(self.Rz)
63          self.Ri_update = np.zeros_like(self.Ri)
64          self.Rf_update = np.zeros_like(self.Rf)
65          self.Ro_update = np.zeros_like(self.Ro)
66
67          self.po_update = np.zeros_like(self.po)
68          self.pf_update = np.zeros_like(self.pf)
69          self.pi_update = np.zeros_like(self.pi)
70
71          self.bz_update = np.zeros_like(self.bz)
72          self.bi_update = np.zeros_like(self.bi)
73          self.bf_update = np.zeros_like(self.bf)
74          self.bo_update = np.zeros_like(self.bo)
75
76          # State vars
77          self.y_prev = np.zeros((hiddenUnits,self.T))
78          self.x_prev = np.zeros((inputUnits,self.T))
79          self.o_prev = np.zeros((hiddenUnits,self.T))
80          self.f_prev = np.zeros((hiddenUnits,self.T))
81          self.c_prev = np.zeros((hiddenUnits,self.T))
82          self.z_prev = np.zeros((hiddenUnits,self.T))
83          self.i_prev = np.zeros((hiddenUnits,self.T))
84
85          self.delta_y_list = np.zeros((hiddenUnits,self.T))
86          self.delta_o_list = np.zeros((hiddenUnits,self.T))
87          self.delta_c_list = np.zeros((hiddenUnits,self.T))
88          self.delta_f_list = np.zeros((hiddenUnits,self.T))
89          self.delta_i_list = np.zeros((hiddenUnits,self.T))
```

```
90          self.delta_z_list = np.zeros((hiddenUnits,self.T))
91
92          self.future_y = np.zeros_like(self.y_prev[:,1])
93          self.future_c = np.zeros_like(self.c_prev[:,1])
94
95          # Delta vectors for a previous layer
96          self.delta_x = np.zeros((inputUnits,self.T))
97
98      def forwardPropagate(self, X):
99
100         # Note that in a list, accessing [-1] corresponds to the last element appended. so
        y_prev[-1] == y^(t-1)
101         if (self.t != 0):
102             self.z_prev[:,self.t] = np.tanh( np.dot(self.Wz,X) + np.dot(self.Rz,self.y_prev
        [:,self.t-1]) + self.bz.T )
103             self.i_prev[:,self.t] = sigmoid( np.dot(self.Wi,X) + np.dot(self.Ri,self.y_prev
        [:,self.t-1]) + np.multiply(self.pi,self.c_prev[:,self.t-1]) + self.bi.T )
104             self.f_prev[:,self.t] = sigmoid( np.dot(self.Wf,X) + np.dot(self.Rf,self.y_prev
        [:,self.t-1]) + np.multiply(self.pf,self.c_prev[:,self.t-1]) + self.bf.T )
105             self.c_prev[:,self.t] = np.multiply(self.z_prev[:,self.t],self.i_prev[:,self.t])
        + np.multiply(self.c_prev[:,self.t-1],self.f_prev[:,self.t])
106             self.o_prev[:,self.t] = sigmoid( np.dot(self.Wo,X) + np.dot(self.Ro,self.y_prev
        [:,self.t-1]) + np.multiply(self.po,self.c_prev[:,self.t]) + self.bo.T )
107             self.y_prev[:,self.t] = np.multiply(np.tanh(self.c_prev[:,self.t]), self.o_prev
        [:,self.t])
108         else:
109             self.z_prev[:,self.t] = np.tanh( np.dot(self.Wz,X) + np.dot(self.Rz,self.future_y
        ) + self.bz.T )
110             self.i_prev[:,self.t] = sigmoid( np.dot(self.Wi,X) + np.dot(self.Ri,self.future_y
        ) + self.bi.T )
111             self.f_prev[:,self.t] = sigmoid( np.dot(self.Wf,X) + np.dot(self.Rf,self.future_y
        ) + self.bf.T )
112             self.c_prev[:,self.t] = np.multiply(self.z_prev[:,self.t],self.i_prev[:,self.t])
        + np.multiply(self.future_c,self.f_prev[:,self.t])
113             self.o_prev[:,self.t] = sigmoid( np.dot(self.Wo,X) + np.dot(self.Ro,self.future_y
        ) + np.multiply(self.po, self.c_prev[:,self.t]) + self.bo.T )
114             self.y_prev[:,self.t] = np.multiply(np.tanh(self.c_prev[:,self.t]), self.o_prev
        [:,self.t])
115
116         self.x_prev[:,self.t] = X
117
118         if (self.t == self.T-1) :
119             self.future_y = self.y_prev[:,self.t]  # Saving the state of these variables
        between iterations, otherwise y_prev will be zero!
120             self.future_c = self.c_prev[:,self.t]
121             self.t = 0                              # Reset the time pointer within time frame
122             return self.y_prev[:,self.T-1]
123         else:
124             self.t += 1
125             return self.y_prev[:,self.t-1]
126
127
128
129     def backPropagate_T(self, upperLayerDeltas):
130         # EVALUATING THE DELTAS
131         for t in reversed(range(self.T)):
132             if (t == self.T-1):
```

```
133                self.delta_y_list[:,t] = (upperLayerDeltas[:,t])
134                self.delta_o_list[:,t] = (np.multiply( np.multiply(upperLayerDeltas[:,t],np.
      tanh(self.c_prev[:,t])), sigmoidPrime(self.o_prev[:,t])))
135                self.delta_c_list[:,t] = (np.multiply(np.multiply(self.delta_y_list[:,t],
      tanhPrime(np.tanh(self.c_prev[:,t]))), self.o_prev[:,t]))
136            else:
137                self.delta_y_list[:,t] = (upperLayerDeltas[:,t] + np.dot(self.Rz,self.
      delta_z_list[:,t+1]) + np.dot(self.Ri,self.delta_i_list[:,t+1]) + np.dot(self.Rf,self.
      delta_f_list[:,t+1]) + np.dot(self.Ro,self.delta_o_list[:,t+1]))
138                self.delta_o_list[:,t] = (np.multiply( np.multiply(upperLayerDeltas[:,t],np.
      tanh(self.c_prev[:,t])), sigmoidPrime(self.o_prev[:,t])))
139                self.delta_c_list[:,t] = (np.multiply(np.multiply(self.delta_y_list[:,t],
      tanhPrime(np.tanh(self.c_prev[:,t]))), self.o_prev[:,t]) + np.multiply(self.delta_c_list
      [:,t+1],self.f_prev[:,t+1]))
140
141            if (t != 0) :
142                self.delta_f_list[:,t] = (np.multiply(np.multiply(self.delta_c_list[:,t],self
      .c_prev[:,t-1]), sigmoidPrime(self.f_prev[:,t])))
143
144            self.delta_i_list[:,t] = (np.multiply( np.multiply(self.delta_c_list[:,t],self.
      z_prev[:,t]), sigmoidPrime(self.i_prev[:,t])))
145            self.delta_z_list[:,t] = (np.multiply( np.multiply(self.delta_c_list[:,t],self.
      i_prev[:,t]), tanhPrime(self.z_prev[:,t])))
146            self.delta_x[:,t] = np.dot(self.Wz.T,self.delta_z_list[:,t]) + np.dot(self.Wi.T,
      self.delta_i_list[:,t]) + np.dot(self.Wf.T,self.delta_f_list[:,t]) + np.dot(self.Wo.T,
      self.delta_o_list[:,t])
147
148        # EVALUATING THE UPDATES
149        for t in range(self.T):
150            self.Wz += self.learnRate * np.outer(self.delta_z_list[:,t],self.x_prev[:,t])
151            self.Wi += self.learnRate * np.outer(self.delta_i_list[:,t],self.x_prev[:,t])
152            self.Wf += self.learnRate * np.outer(self.delta_f_list[:,t],self.x_prev[:,t])
153            self.Wo += self.learnRate * np.outer(self.delta_o_list[:,t],self.x_prev[:,t])
154            self.po += self.learnRate * np.multiply(self.c_prev[:,t],self.delta_o_list[:,t])
155            self.bz += self.learnRate * self.delta_z_list[:,t]
156            self.bi += self.learnRate * self.delta_i_list[:,t]
157            self.bf += self.learnRate * self.delta_f_list[:,t]
158            self.bo += self.learnRate * self.delta_o_list[:,t]
159
160            if(t < self.T-1):
161                self.Rz += self.learnRate * np.outer(self.delta_z_list[:,t+1],self.y_prev[:,t
      ])
162                self.Ri += self.learnRate * np.outer(self.delta_i_list[:,t+1],self.y_prev[:,t
      ])
163                self.Rf += self.learnRate * np.outer(self.delta_f_list[:,t+1],self.y_prev[:,t
      ])
164                self.Ro += self.learnRate * np.outer(self.delta_o_list[:,t+1],self.y_prev[:,t
      ])
165                self.pi += self.learnRate * np.multiply(self.c_prev[:,t],self.delta_i_list[:,
      t+1])
166                self.pf += self.learnRate * np.multiply(self.c_prev[:,t],self.delta_f_list[:,
      t+1])
167
168        return  self.delta_x
```

Listing 4.1: Implementation of a LSTM Layer

Chapter 5

Work Plan

5.1 Approach and Main Tasks

Dwight Eisenhower, United States' President from 1953 to 1961 and Army Officer, said that 'no battle was ever won according to plan, but no battle was ever won without one'. Hence, although this initial planning draft might not be religiously followed in all its extent, it is important to break down the work in **tasks** so that I and my supervisors can keep track of what has to be done, and establishing deadlines for the small achievements that, together, will build up to the successful completion of the proposed work of this thesis. The detailed explanation of each task is provided in Section 5.1.1 and the **schedule** for them, where their estimated begin and end weeks are marked, is represented by a *Gantt Chart* in Section 5.1.2.

5.1.1 Task Description

The work will be partitioned in *five* large groups of tasks, and each of these groups will be further partitioned in smaller subtasks which are the actual assignments that I will be completing. We can think of the group of task as a sort of *logical* grouping of the subtasks, according both to their relatedness and also to their precedence relationships. The task groups, and their related subtasks, are as follows:

- **T1 – Preparation** – This stage is the initial phase of the work, where I will essentially setup my working environment and finish the Python modules for the LSTM network that will be used in the validation of my Verilog modules

    - **T1.1 – Complete Python Implementation with SPSA** – here I will finish the Python modules that I have already developed as a preparation for this work, whose details are presented in Section 4, by adding the SPSA training algorithm, as opposed to the current Backpropagation Through Time version.

    - **T1.2 – Reproduce the Benchmark Results with the Python Implementation** – after developing and testing the Python Class with SPSA, I will try to reproduce with it

the results of [5], in order for me to have a high-level model whose performance is comparable to [5, 21], and thus provide a good performance baseline for this and other future benchmark tests that I would like to run in order to compare my FPGA solution with a software solution.

– **T1.3 – Setup FPGA Development Board** – this is a fairly technical step, where I setup my working environment, and make sure that everything is working correctly and is properly configured. As will be pointed out in Section 5.2, the FPGA development board of choice will be Xilinx ®Zedboard.

– **T1.4 – Familiarize with the Zedboard** – before any actual use, I should synthesize and run some sample designs, and perhaps write a small Verilog design, and go through the full design flow, from behavioural simulation, to synthesis. This will allow me to know exactly what steps to take when I will need to develop and test my Dissertation related modules, and focus more on the solving the problem at hand rather than solving technical details.

• **T2 – HDL Module Development** – this is where I will port the ideas from Section 2 to fully functional HDL blocks, using Verilog and targeting a Zedboard technology.

– **T2.1 – Design Planning** – before performing and HDL coding, it is desirable first assemble the system design strategy in paper. This is where, together with my supervisor, I will outline the internal organization of my system, and make the fundamental design decisions. Of course, this task will continue during the entire of **T2** extent, since some design changes to the original plan will have to be performed as I find *bugs* in my early Verilog implementations that force a design correction.

– **T2.2 – Design SPSA Module** – this task comprises the Verilog description of the module that will update the network weights using SPSA, and also the development of a testbench to validate my description. Furthermore, I will compare the output of this model with the golden output produced by a standalone SPSA Python Class previously developed in **T1**.

– **T2.3 – Design LSTM Neuron/Layer Module** – similarly to the previous task, but now I am aiming to implement the actual LSTM Neuron or a layer of LSTM Neurons. This is a design decision that will need to be set in **T2.1**, to assess whether it is justifiable to have dedicated multiplication units assigned to each neuron, or we can perform matrix-like batch multiplications and treat the LSTM as a batch of Neurons, i.e. as a layer. Like in the previous task, a testbench will also be developed, and the module validate both with it and the Python golden output.

– **T2.4 – Integrate and Validate both LSTM and SPSA modules** – here, after the modules designed in **T2.2** and **T2.3** are validated individually, I will integrate them together in a higher level module, and perform a behavioural simulations of the new

integrated module, as well as a verification procedure where the results from [5] will hopefully be reproduced and compared against the Python golden output.

- **T3 – FPGA Synthesis of the Verilog Code** – after having Verilog code that passed all the validation tests and whose correct functionality is, therefore, ensured, I will synthesize the Verilog modules to FPGA RTL blocks, and perform a new simulation on these RTL syntesized code, that unlike the previous behavioural simulation, now has timing information resulting from the FPGA block mapping, and the place and routing of those mapped blocks.

    - **T3.1 – Synthesis of the SPSA Module** – the module developed in **T2.2** is now synthesized and validated.

    - **T3.2 – Synthesis of the LSTM Neuron/Layer Module** – same as the previous task, but now on the module of **T2.3**

    - **T3.3 – Integration of the Modules and Validation** – the modules synthesized in the previous tasks are integrated and validated using the same testbench as in **T2.4**.

- **T4 – Benchmarking the Design** – at this stage, we have a fully functional FPGA design of an LSTM network with SPSA on-chip training. Henceforth, we will need to benchmark its performance by comparing it to [5, 21], and prove its usefulness by using it in one or two use-cases from 3, which are interesting uses of Deep Learning techniques such as these.

    - **T4.1 – Benchmark the Performance/Computing Time** – perform a side-by-side comparison of our model with the software counterpart of [5, 21] and with the only hardware implementation of LSTM of [4].

    - **T4.2 – Reproduce some of the state of the art applications of LSTM** – in order to be able to show real-life, user-oriented, applications, I understand it is a good idea to try to reproduce some of the state of the art usages of LSTM, outlined in Section 3.1. It is too early to commit myself to which of these applications I will use, and how many, because that will depend on how well the work on tasks **T2** and **T3** is flowing. Nevertheless, I intend to at least implement one or two of them.

- **T5 – Write the Dissertation Final Report** – while all the stages of work are progressing, this task will obviously be active, by documenting all the design decisions, milestones achieved and logging all the results that come from the implementation. A couple of weeks before the deadline, this will be the only active task, since producing a clear and well-written document requires concentration and undivided attention.

5.1.2 Tentative Task Scheduling

Here is the Gantt Chart that depicts the temporal extension of the tasks described in Section 5.1.1.
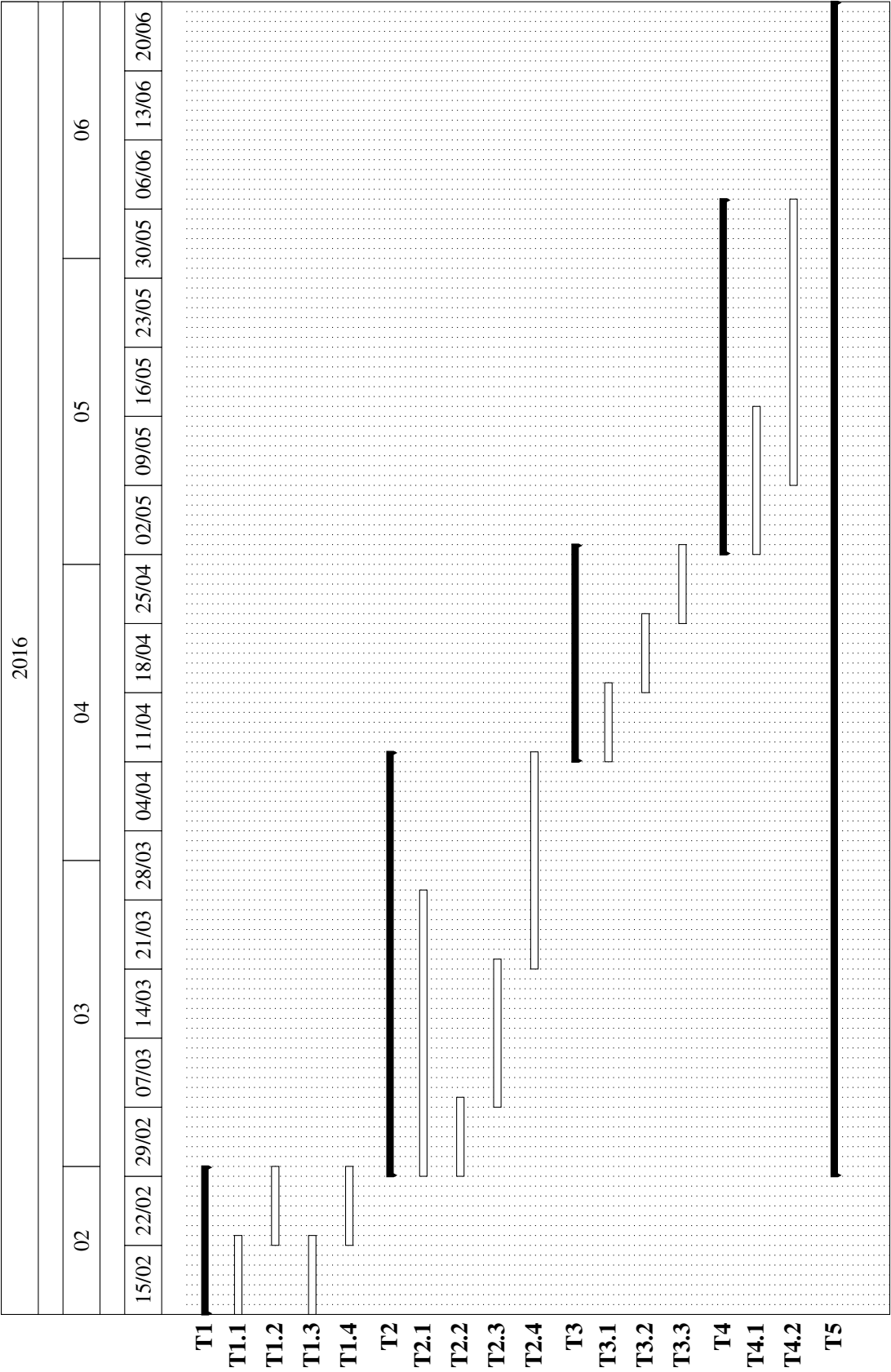
5.2   Software and Hardware resources to be used

5.2.1   Hardware Resources

The main hardware resource that I will use for my solution is the **Xilinx® Zedboard** (Figure 5.1), whose core is a Zynq-7000 System-on-Chip that features both an FPGA core and two ARM ® Cortex™ -A9 processors. It is an FPGA development board that features several I/O interfaces such as Ethernet, HDMI output, VGA output, Audio IOs, USB and UART, among other capabilities, making it easy to prototype additional features to the core design (i.e. for building the note transcription system of [24], and to make it operate in real-time, I would need an audio input, which I can easily get from the Audio IO, without investing time in connecting the codec and programming the FPGA to interface it).

5.2.2   Software Resources

In terms of software resources related to the FPGA development, I will need an **HDL simulation tool** to simulate and verify the Verilog code that I will develop, and a **Synthesis tool** to synthesize the Verilog files into RTL code, and to map that description into the resources available in the FPGA. The simulation tool used will be Questasim™, the successor of the well-known Modelsim™, which is an industry-standard tool in the area. For the synthesis tool, I will use Xilinx®Vivado Suite, also an industry-standard tool, and that is the only alternative, since the Zedboard is also produced by Xilinx®. These two tools are proprietary, but there are licenses available at FEUP. Furthermore, I am planning to use FloPoCo [1] to generate some of the modules that perform arithmetic operations, to hasten the developing effort/time, and to ensure that they are the most efficient possible, and don't pose a performance bottleneck to my design; this software is freeware, and a standard in Academia.

For the Python implementation, I will make use of the 3.3 version of the Python distribution, the high-performance numerical computation library Numpy[2], which is a standard in scientific computing, and the Matplotlib[3] plotting library. All of this software is also free to use, and open-source. I may also need to use the PyBrain[4] framework, since it has an LSTM implementation.

To write the final Dissertation report, I will use LaTeX (this report itself was also written in LaTeX), and mostly use Tikz, Inkscape and Matplotlib to produce figures and drawings. Once again, all of these are free to use.

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[1] http://flopoco.gforge.inria.fr/
[2] http://www.numpy.org/
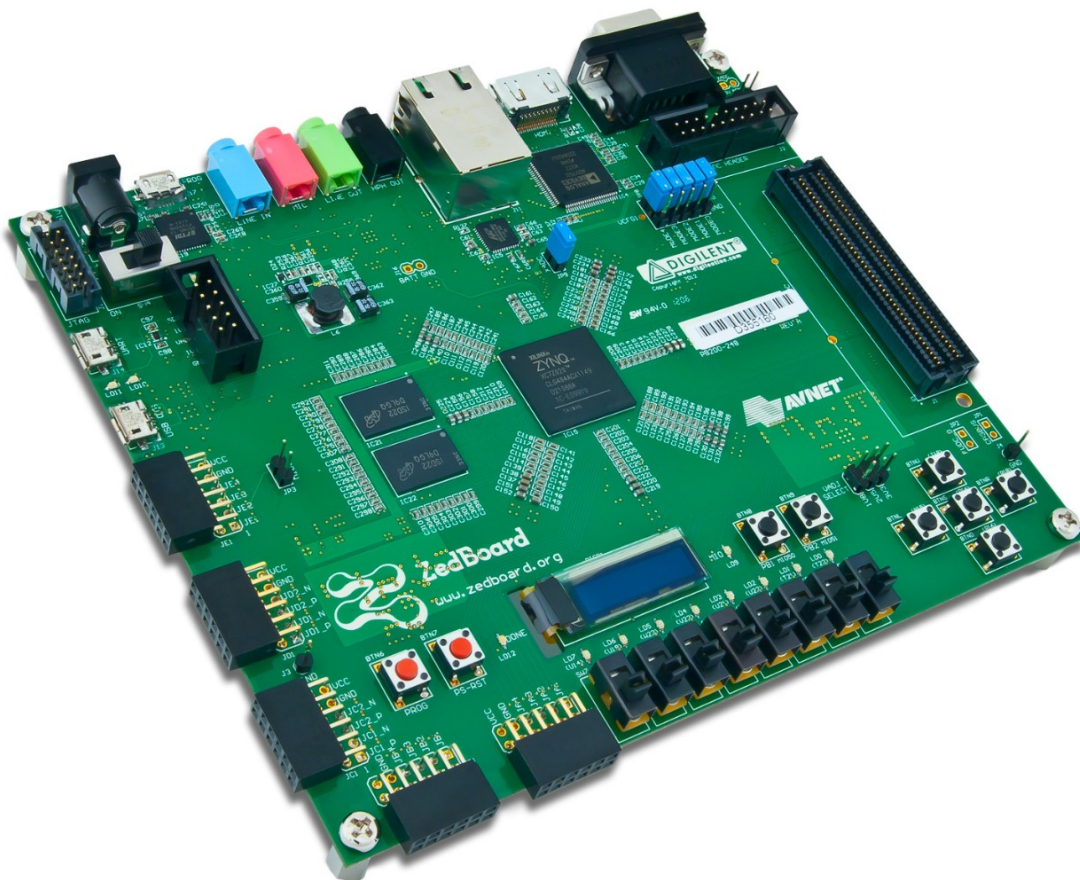[3] http://matplotlib.org/
[4] http://pybrain.org/

Figure 5.1: The Zedboard FPGA Development Board. Source: Xilinx

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