RABBIT 2000™ PROCESSOR

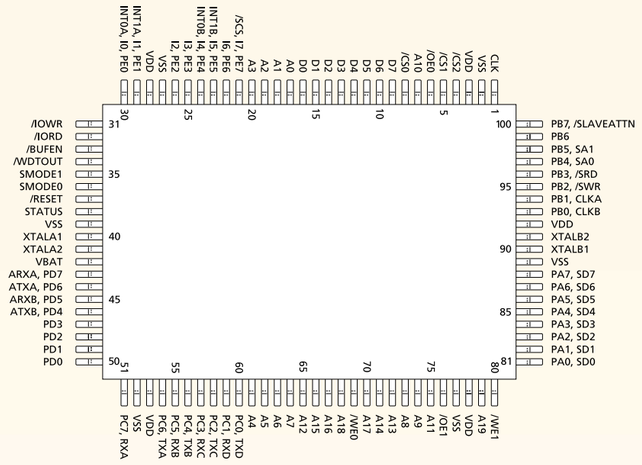
EASY REFERENCE

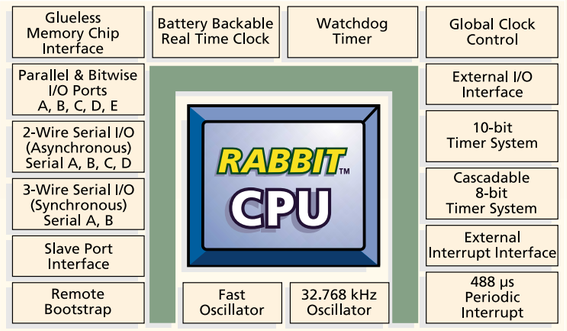
Pin Chart

PIN	NAME	ALT FUNCTION OUTPUT	ALT FUNCTION INPUT
1	CLK		
2	VSS		
3	VDD		
4	/CS2		
5	/CS1		
6	/OE0		
7	A10		
8	/CS0		
9	D7		
10	D6		
11	D5		
12	D4		
13	D3		
14	D2		
15	D1		
16	D0		
17	A0		
18	A1		
19	A2		
20	A3		
21	PE7	I7	/SCS
22	PE6	I6	
23	PE5	I5	INT1B
24	PE4	I4	INT0B
25	PE3	I3	
26	PE2	I2	
27	VSS		
28	VDD		
29	PE1	I1	INT1A
30	PE0	I0	INT0A
31	/IOWR		
32	/IORD		
33	/BUFEN		
34	/WDTOUT		
35	SMODE1		
36	SMODE0		
37	/RESET		
38	STATUS		
39	VSS		
40	XTALA1		
41	XTALA2		
42	VBAT		
43	PD7		ARXA
44	PD6	ATXA	
45	PD5		ARXB
46	PD4	ATXB	
47	PD3		
48	PD2		
49	PD1		
50	PD0		
51	PC7		RXA
52	VSS		
53	VDD		
54	PC6	TXA	
55	PC5		RXB
56	PC4	TXB	
57	PC3		RXC
58	PC2	TXC	
59	PC1		RXD
60	PC0	TXD	
61	A4		
62	A5		
63	A6		
64	A7		
65	A12		
66	A15		
67	A16		
68	A18		
69	/WE0		
70	A17		
71	A14		
72	A13		
73	A8		
74	A9		
75	A11		
76	/OE1		
77	VSS		
78	VDD		
79	A19		
80	/WE1		
81	PA0	SD0	SD0
82	PA1	SD1	SD1
83	PA2	SD2	SD2
84	PA3	SD3	SD3
85	PA4	SD4	SD4
86	PA5	SD5	SD5
87	PA6	SD6	SD6
88	PA7	SD7	SD7
89	VSS		
90	XTALB1		
91	XTALB2		
92	VDD		
93	PB0	CLKB	CLKB
94	PB1	CLKA	CLKA
95	PB2		/SWR
96	PB3		/SRD
97	PB4		SA0
98	PB5		SA1
99	PB6		
100	PB7	/SLAVEATTN	

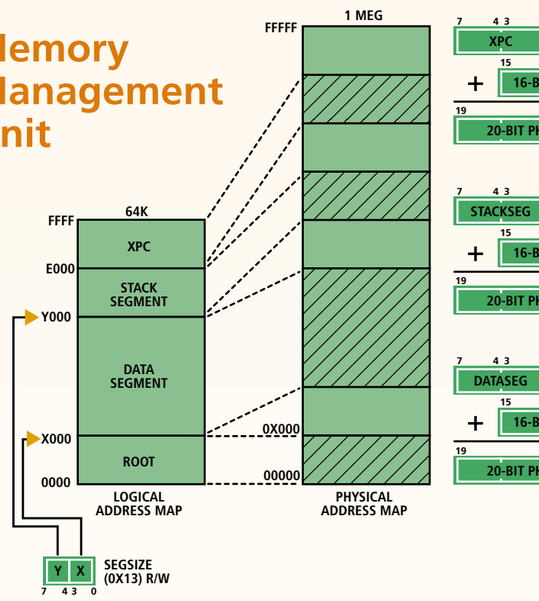
Processor Mode Select

SMODE1	SMODE0	BOOTSTRAP OPERATION
0	0	BOOTSTRAP DISABLED. NORMAL PROCESSOR OPERATION (CODE FETCHED FROM MEMORY)
0	1	SLAVE PORT. SPDOR USED FOR BOOTSTRAP OPERATION
1	0	SYNCHRONOUS SERIAL. CLOCKED SERIAL PORT A ON PARALLEL PORT C USED FOR BOOTSTRAP OPER. MAX EXTERNAL CLOCK RATE = PCLK/6
1	1	ASYNCHRONOUS SERIAL. ASYNCH SERIAL PORT A ON PARALLEL PORT C USED FOR BOOTSTRAP OPER. REQUIRED BAUD RATE = 2400





Memory Management Unit



XPC — EXTENDED PROGRAM COUNTER REGISTER
+ 16-BIT LOGICAL ADDRESS (15 … 0)
= 20-BIT PHYSICAL ADDRESS (19 … 0)

STACKSEG — STACK SEGMENT REGISTER (0x11) R/W
+ 16-BIT LOGICAL ADDRESS (15 … 0)
= 20-BIT PHYSICAL ADDRESS (19 … 0)

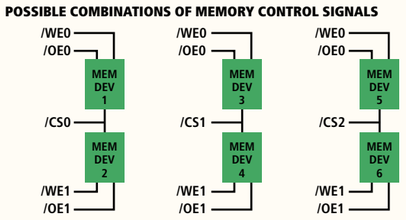
DATASEG — DATA SEGMENT REGISTER (0x12) R/W
+ 16-BIT LOGICAL ADDRESS (15 … 0)
= 20-BIT PHYSICAL ADDRESS (19 … 0)

A[19:18]	CONTROL REGISTER USED	ADDRESS
00	MB0CR	(0x14) W
01	MB1CR	(0x15) W
10	MB2CR	(0x16) W
11	MB3CR	(0x17) W

MBXCR
- 00 = 4 WAITS (5 FOR WRITES)
- 01 = 2 WAITS (3 FOR WRITES)
- 10 = 1 WAITS (2 FOR WRITES)
- 11 = 0 WAITS (1 FOR WRITES)
- 0 = PASS A[19]; 1 = INVERT A[19]
- 0 = PASS A[18]; 1 = INVERT A[18]
- 00 USE /OE0 & /WE0; 01 USE /OE1 & /WE1; 10 USE /OE0 (READ ONLY); 11 USE /OE1 (READ ONLY)
- 00 USE /CS0; 01 USE /CS1; 1X USE /CS2

MMIDR (0x10) R/W
- X X X 0 0 0 0 0
- 0 = NORMAL /CS1 OPERATION; 1 = FORCE /CS1 ALWAYS ACTIVE
- MUST WRITE 0 TO THESE

POSSIBLE COMBINATIONS OF MEMORY CONTROL SIGNALS



Timer A

TIMER A CONTROL/STATUS REGISTER TACSR (0xA0) R/W

TMRA7 TMRA6 TMRA5 TMRA4 0 0 TMRA1

(WRITE)
- 0 = CORRESPONDING TIMER A INTERRUPT IS DISABLED; 1 = CORRESPONDING TIMER A INTERRUPT IS ENABLED

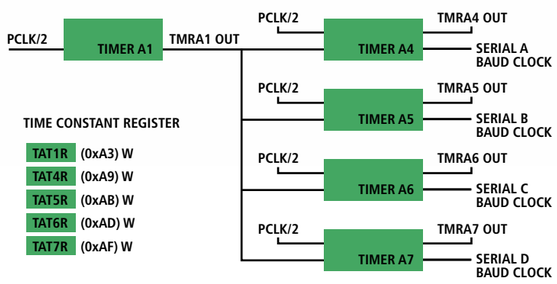
(READ)
- 0 = CORRESPONDING TIMER A HAS NOT REACHED TERM. COUNT; 1 = CORRESPONDING TIMER A HAS REACHED TERM. COUNT

0 = MAIN CLOCK FOR TIMER A DISABLED; 1 = MAIN CLOCK (PCLK/2) FOR TIMER A ENABLED

TIMER A CONTROL REGISTER / TACR (0xA4) W

TMRA7 TMRA6 TMRA5 TMRA4 X X

- 0 = CORRESPONDING TIMER CLOCKED BY (PCLK/2); 1 = CORRESPONDING TIMER CLOCKED BY TIMER A1
- 00 = INTERRUPTS DISABLED; 01 = PRIORITY 1 INTERRUPT; 10 = PRIORITY 2 INTERRUPT; 11 = PRIORITY 3 INTERRUPT



TIME CONSTANT REGISTER

TAT1R	(0xA3) W
TAT4R	(0xA9) W
TAT5R	(0xAB) W
TAT6R	(0xAD) W
TAT7R	(0xAF) W

Timer B

TIMER B CONTROL/STATUS REGISTER TBCSR (0xB0) R/W

0 0 0 0 0

(WRITE)
- 0 = CORRESPONDING TIMER B INTERRUPT IS DISABLED; 1 = CORRESPONDING TIMER B INTERRUPT IN ENABLED

(READ)
- 0 = CORRESPONDING TIMER B HAS NOT ENCOUNTERED A MATCH; 1 = CORRESPONDING TIMER B HAS ENCOUNTERED A MATCH (STATUS BIT/INTERRUPTS STATUS IS CLEARED BY READ OF THIS REGISTER

0 = MAIN CLOCK (PCLK/2) IS DISABLED; 1 = MAIN CLOCK (PCLK/2) IS ENABLED

TIMER B CONTROL REGISTER TBCR (0xB1) W

X X X X

- BITS [7:4] IGNORED
- 00 = TIMER B CLOCKED BY PCLK/2; 01 = TIMER B CLOCKED BY TIMER A1; 1X = TIMER B CLOCKED BY PCLK/16
- 00 = TIMER B INTERRUPT DISBALED; 01 = PRIORITY 1 INTERRUPT; 10 = PRIORITY 2 INTERRUPT; 11 = PRIORITY 3 INTERRUPT

TIMER B MATCH 1 REGISTER

(MSB) BIT9 BIT8 X X X X X X — TBM1R (0xB2) W
(LSB) BIT7 BIT6 BIT5 BIT4 BIT3 BIT2 BIT1 BIT0 — TBL1R (0xB3) W

TIMER B MATCH 2 REGISTER

(MSB) BIT9 BIT8 X X X X X X — TBM2R (0xB4) W
(LSB) BIT7 BIT6 BIT5 BIT4 BIT3 BIT2 BIT1 BIT0 — TBL2R (0xB5) W

TIMER B COUNT REGISTER

(MSB) BIT9 BIT8 0 0 0 0 0 0 — TBCMR (0xBE) RD
(LSB) BIT7 BIT6 BIT5 BIT4 BIT3 BIT2 BIT1 BIT0 — TBCLR (0xBF) RD

External Interrupt

INTERUPT 0 CONTROL REGISTER I0CR (0x98) W

X X
- INT0 AT PORT E[4]: 00 DISABLE; 01 FALLING EDGE; 10 RISING EDGE; 11 BOTH EDGES
- INT0 AT PORT E[0]: 00 DISABLE; 01 FALLING EDGE; 10 RISING EDGE; 11 BOTH EDGES
- 00 INT0 DISABLED; 01 INT0 PRIORITY 1; 10 INT0 PRIORITY 2; 11 INTO PRIORITY 3

INTERUPT 1 CONTROL REGISTER I1CR (0x99) W

X X
- INT1 AT PORT E[5]: 00 DISABLE; 01 FALLING EDGE; 10 RISING EDGE; 11 BOTH EDGES
- INT1 AT PORT E[1]: 00 DISABLE; 01 FALLING EDGE; 10 RISING EDGE; 11 BOTH EDGES
- 00 INT1 DISABLED; 01 INT1 PRIORITY 1 = LOWEST; 10 INT1 PRIORITY 2; 11 INT1 PRIORITY 3 = HIGHEST

** EXTERNAL INTERRUPT HOLD TIME MUST BE AT LEAST THREE PERIPHERAL CLOCK CYCLES*

** SEE USERS MANUAL FOR DETAILS ON EXTERNAL INTERRUPT INTERFACE*

External I/O

I/O ADDRESS A15 A14 A13	I/O BANK CTL REGISTER		PORT E
1 1 1	IB7CR	(0x87) W	I7
1 1 0	IB6CR	(0x86) W	I6
1 0 1	IB5CR	(0x85) W	I5
1 0 0	IB4CR	(0x84) W	I4
0 1 1	IB3CR	(0x83) W	I3
0 1 0	IB2CR	(0x82) W	I2
0 0 1	IB1CR	(0x81) W	I1
0 0 0	IB0CR	(0x80) W	I0

IBxCR — X X X

- WAITS: 00 = 15 WAITS; 01 = 7 WAITS; 10 = 3 WAITS; 11 = 1 WAIT
- 1 = WRITES ALLOWED; 0 = WRITES NOT ALLOWED
- Ix FUNCTIONS: 00 = I/O /CS; 01 = I/O /RD STROBE; 10 = I/O /WR STROBE; 11 = I/O DATA (/RD OR /WR) STROBE

Parallel Ports

PARALLEL PORT DATA REGISTERS

PADR (0x30) R/W — A
PBDR (0x40) R/W — B
PCDR (0x50) R/W — C
PDDR (0x60) R/W — D
PEDR (0x70) R/W — E

PARALLEL PORT A (PPA)

PIN NAME	PRIMARY FUNCTION OUTPUT	PRIMARY FUNCTION INPUT	ALTERNATE FUNCTION OUTPUT	ALTERNATE FUNCTION INPUT
PA7	PARALLEL I/O		SD7	SD7
PA6			SD6	SD6
PA5			SD5	SD5
PA4			SD4	SD4
PA3			SD3	SD3
PA2			SD2	SD2
PA1			SD1	SD1
PA0			SD0	SD0

PARALLEL PORT A/ SLAVE PORT CONTROL REGISTER SPCR (0x24) R/W

- SEE SECTION ON SLAVE PORT FOR DETAILS ON THESE BITS IN THE SPCR
- 00 = DISABLE SLAVE PORT, PORT A: BYTEWIDE INPUT
- 01 = DISABLE SLAVE PORT, PORT A: BYTEWIDE OUTPUT
- SEE SECTION ON SLAVE PORT FOR DETAILS ON THESE BITS IN THE SPCR

PARALLEL PORT B (PPB)

PIN NAME	PRIMARY FUNCTION OUTPUT	PRIMARY FUNCTION INPUT	ALTERNATE FUNCTION OUTPUT	ALTERNATE FUNCTION INPUT
PB7	OUTPUT		/SLAVEATTN	
PB6	OUTPUT			
PB5		INPUT		SA1
PB4		INPUT		SA0
PB3		INPUT		/SRD
PB2		INPUT		/SWR
PB1		INPUT	*CLKA	CLKA
PB0		INPUT	*CLKB	CLKB

*OUTPUT FUNCTION ACTIVE ONLY WHEN USED AS CLOCK OUTPUT IN CLOCKED SERIAL MODE

PARALLEL PORT C (PPC)

PIN NAME	PRIMARY FUNCTION OUTPUT	PRIMARY FUNCTION INPUT	ALTERNATE FUNCTION OUTPUT	ALTERNATE FUNCTION INPUT
PC7		INPUT		RXA
PC6	OUTPUT		TXA	
PC5		INPUT		RXB
PC4	OUTPUT		TXB	
PC3		INPUT		RXC
PC2	OUTPUT		TXC	
PC1		INPUT		RXD
PC0	OUTPUT		TXD	

PARALLEL PORT C FUNCTION REGISTER PCFR (0x55) W

TXA TXB TXC TXD
- 0 = CORRESPONDING BIT FUNCTIONS NORMALLY AS OUTPUT
- 1 = CORRESPONDING BIT CARRIES ALTERNATE SIGNAL AS OUTPUT

PARALLEL PORT D (PPD)

PIN NAME	PRIMARY FUNCTION OUTPUT	PRIMARY FUNCTION INPUT	ALTERNATE FUNCTION OUTPUT	ALTERNATE FUNCTION INPUT
PD7				ARXA
PD6			ATXA	
PD5	PARALLEL AND BITWISE I/O			ARXB
PD4			ATXB	
PD3				
PD2				
PD1				
PD0				

PARALLEL PORT D FUNCTION REGISTER PDFR (0x65) W

ATXA ATXB
- 0 = CORRESPONDING BIT FUNCTIONS NORMALLY AS I/O
- 1 = CORRESPONDING BIT CARRIES ALTERNATE SIGNAL AS OUTPUT

PARALLEL PORT E (PPE)

PIN NAME	PRIMARY FUNCTION OUTPUT	PRIMARY FUNCTION INPUT	ALTERNATE FUNCTION OUTPUT	ALTERNATE FUNCTION INPUT
PE7			I7	/SCS
PE6			I6	
PE5	PARALLEL AND BITWISE I/O		I5	INT1B
PE4			I4	INT0B
PE3			I3	
PE2			I2	
PE1			I1	INT1A
PE0			I0	INT0A

PARALLEL PORT E FUNCTION REGISTER PEFR (0x75) W

I7 I6 I5 I4 I3 I2 I1 I0
- 0 = CORRESPONDING BIT FUNCTIONS NORMALLY AS I/O
- 1 = CORRESPONDING BIT CARRIES EXTERNAL I/O CONTROL SIGNAL

PARALLEL PORTS D & E CONTROL REGISTER PDCR (0x64) W, PECR (0x74) W

- 00 = UPPER NIBBLE PORT TRANSFER CLOCK IS PCLK/2
- 01 = UPPER NIBBLE PORT TRANSFER CLOCK IS TIMER_A1
- 10 = UPPER NIBBLE PORT TRANSFER CLOCK IS TIMER_B1
- 11 = UPPER NIBBLE PORT TRANSFER CLOCK IS TIMER_B2
- 00 = LOWER NIBBLE PORT TRANSFER CLOCK IS PCLK/2
- 01 = LOWER NIBBLE PORT TRANSFER CLOCK IS TIMER_A1
- 10 = LOWER NIBBLE PORT TRANSFER CLOCK IS TIMER_B1
- 11 = LOWER NIBBLE PORT TRANSFER CLOCK IS TIMER_B2

PARALLEL PORT D BIT REGISTERS

A WRITE TO THE CORRESPONDING BIT CHANGES THAT BIT

PDB7R (0x6F) W
PDB6R (0x6E) W
PDB5R (0x6D) W
PDB4R (0x6C) W
PDB3R (0x6B) W
PDB2R (0x6A) W
PDB1R (0x69) W
PDB0R (0x68) W

PARALLEL PORT D DATA DIRECTION REGISTER PDDDR (0x67) W

- 0 = CORRESPONDING BIT IS INPUT
- 1 = CORRESPONDING BIT IS OUTPUT

PARALLEL PORT D DRIVE CONTROL REGISTER PDDCR (0x66) W

- 0 = CORRESPONDING BIT AS OUTPUT IS DRIVEN HIGH OR LOW
- 1 = CORRESPONDING BIT AS OUTPUT IS OPEN DRAIN

PARALLEL PORT E DATA DIRECTION REGISTER PEDDR (0x77) W

- 0 = CORRESPONDING BIT IS INPUT
- 1 = CORRESPONDING BIT IS OUTPUT

PARALLEL PORT E BIT REGISTERS

A WRITE TO THE CORRESPONDING BIT CHANGES THAT BIT

PEB7R (0x7F) W
PEB6R (0x7E) W
PEB5R (0x7D) W
PEB4R (0x7C) W
PEB3R (0x7B) W
PEB2R (0x7A) W
PEB1R (0x79) W
PEB0R (0x78) W

Serial Ports

SERIAL x PORT STATUS REGISTER (SxSR)

SASR (0xC3) R/W, SBSR (0xD3) R/W, SCSR (0xE3) R/W, SDSR (0xF3) R/W

- RCV DATA REG. — 0 = EMPTY; 1 = FULL. SER PORT REQUESTS INTERRUPT. INTERRUPT CLEARED WHEN RCV BUF READ
- RCV BUF — 0 = BYTE IN RCV BUF IS DATA; 1 = BYTE IN RCV BUF IS ADDRESS
- RCV BUF — 0 = RCV BUF NOT OVERRUN; 1 = RCV BUF OVERRUN. CLEARED WHEN RVC BUF READ
- ALWAYS ZERO
- XMIT DATA REG — 0 = EMPTY. SER PORT REQUESTS INTERRUPT; 1 = FULL.
- XMIT — 0 = IDLE. SER PORT REQUESTS INTERRUPT; 1 = SENDING BYTE
- ALWAYS ZERO

SERIAL PORT x CONTROL REGISTER (SxCR)

SACR (0xC4) W, SCCR (0xE4) W, SBCR (0xD4) W, SDCR (0xF4) W

- 00 = NO OPERATION. IGNORED IN ASYNCH MODE; 01 = CLOCKED MODE: START BYTE RCV OPERATION; 10 = CLOCKED MODE: START BYTE XMIT OPERATION
- 00 = PARALLEL PORT C USED FOR INPUT; 01 = PARALLEL PORT D USED FOR INPUT; 10 = DISBALE RCV INPUT
- 00 = ASYNCH MODE: 8-BITS PER CHAR.; 01 = ASYNCH MODE: 7-BITS PER CHAR.; 10 = CLOCKED MODE: EXTERNAL CLOCK (INPUT); 11 = CLOCKED MODE: INTERNAL CLOCK (OUTPUT)
- INTERRUPT — 00 = DISABLED; 01 = PRIORITY 1; 10 = PRIORITY 2; 11 = PRIORITY 3

SERIAL PORT x DATA REGISTER (SxDR)

SADR (0xC0) R/W, SBDR (0xD0) R/W, SCDR (0xE0) R/W, SDDR (0xF0) R/W

RD = RETURNS CONTENTS OF RCV BUFFER
W = LOADS XMIT BUF WITH DATA BYTE FOR TRANSMISSION

SERIAL PORT x ADDRESS REGISTER

SAAR (0xC1) R/W, SBAR (0xD1) R/W, SCAR (0xE1) R/W, SDAR (0xF1) R/W

RD = RETURNS CONTENTS OF RCV BUFFER
W = LOADS XMIT BUF WITH ADDRESS BYTE FOR TRANSMISSION (9TH BIT=0)

Slave Port

SLAVE PORT CONTROL REGISTER SPCR (0x24) R/W

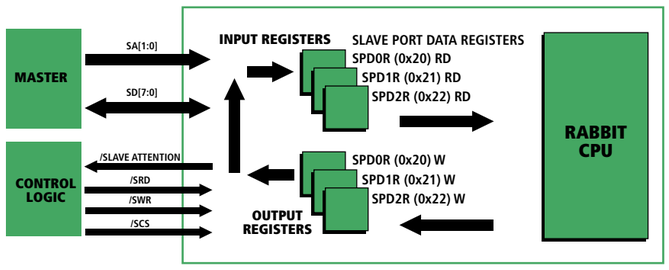
X
- 0 = PROGRAM FETCH AS A FUNCTION OF SMODE PINS; 1 = IGNORE SMODE PINS
- (RD) = REPORT STATE OF SMODE PINS; (WR) = IGNORED FOR WRITE
- (WR) 00 = DISABLE SLAVE PORT. PORT A IS BYTE WIDE INPUT; 01 = DISABLE SLAVE PORT. PORT A IS BYTE WIDE OUTPUT; 1X = ENABLE SLAVE PORT
- (WR) 00 = SLAVE PORT INTERRUPT DISABLED; 01 = PRIORITY 1 INTERRUPT; 10 = PRIORITY 2 INTERRUPT; 11 = PRIORITY 3 INTERRUPT

SLAVE PORT STATUS REGISTER SPSR (0x23) RD

- 0 = PROCESSOR WROTE TO SPSR; 1= MASTER WROTE TO SPDOR
- READ PORT STATUS: 0 = EMPTY; 1 = FULL
- 0 = MASTER WROTE TO STATUS REG; 1 = PROCESSOR WROTE TO SPDOR
- WRITE PORT STATUS: 0 = EMPTY; 1 = FULL

SLAVE PORT INTERFACE SIGNALS

PORT A: SD7 SD6 SD5 SD4 SD3 SD2 SD1 SD0
PORT B: /SLAVE ATTN; SA1; SA0; /SRD; /SWR
PORT E: /SCS



Global Control/Status

GCSR (0x00) R/W

- RD ONLY: 00 = NO RESET OR WD TIMEOUT; 01 = WATCHDOG TIMEOUT; 10 = NOT POSSIBLE; 11 = RESET OCCURRED
- WRITE 1 = FORCE A PERIODIC INTERRUPT TO BE PENDING
- OSC: 000 PROC=OSC/8: PCLK = OSC/8; 001 PROC=OSC/8: PCLK = OSC; 01X PROC=OSC: PCLK = OSC; 1X0 PROC=32kHz: PCLK = 32kHz, MAIN OSC ON; 1X1 PROC=32kHz: PCLK = 32kHz, MAIN OSC OFF
- PERIODIC INTERRUPT: 00 PERIODIC INTERRUPT = DISABLE; 01 PERIODIC INTERRUPT = PRIORITY 1 (LOWEST); 10 PERIODIC INTERRUPT = PRIORITY 2; 11 PERIODIC INTERRUPT = PRIORITY 3 (HIGHEST)

PERIODIC INTERRUPT = 32kHz/16 (488µs)
PCLK = PERIPHERAL CLOCK
PROC = CPU CLOCK

Global Output Control Register

GOCR (0x0E) W

- CLK OUTPUT: 00 = CLK DRIVEN WITH PCLK; 01 = CLK DRIVEN BY PCLK/2; 10 = CLK = LOW; 11 = CLK = HIGH
- STATUS OUTPUT: 00 = LOW DURING FIRST OPCODE FETCH; 01 = LOW DURING FIRST INTERRUPT ACKNOWLEDGE; 10 = LOW; 11 = HIGH
- /WDTOUB OUTPUT: 0 = FUNCTIONS NORMALLY, 30.5µs LOW (WATCHDOG TIMEOUT); 1 = LOW PULSE FOR DURATION OF 30.5 - 61µs
- /BUFEN OUTPUT: 00 = LOW FOR EXTERNAL I/O CYCLE; 01 = LOW FOR DATA MEMORY CYCLE; 10 = LOW; 11 = HIGH

Global Clock Double Register

GCDR (0x0F) W

X X X X X

000		DISABLE CLOCK DOUBLER
001	8ns LOW TIME	(BEST FOR 30MHz)
010	10ns LOW TIME	(25MHz)
011	12ns LOW TIME	(20MHz)
100	14ns LOW TIME	(18MHz)
101	16ns LOW TIME	(16MHz)
110	18ns LOW TIME	(14MHz)
111	20ns LOW TIME	(12MHz)

Real Time Clock Control Register

REAL TIME CLOCK x REGISTER

RTC0R (0x02) R/W
RTC1R (0x03) RD
RTC2R (0x04) RD
RTC3R (0x05) RD
RTC4R (0x06) RD
RTC5R (0x07) RD

RD = CURRENT VALUE OF 48bit RTC HOLDING REGISTER IS RETURNED
W = A WRITE TO RTC0R TRANSFERS CURRENT COUNT OF RTC TO HOLDING REGISTERS

REAL TIME CLOCK CONTROL REGISTER RTCCR (0x01) W

RTC5B RTC4B RTC3B RTC2B RTC1B RTC0B
- 01 = THIS BIT COMBINATION MUST BE USED WITH EVERY BYTE INCREMENT WRITE
- 0 = NO EFFECT ON RTC COUNTER; 1 = INCREMENT CORRESPONDING BYTE OF RTC (RTCxB)

RTCCR (SHORTCUTS)

- 00h = NO EFFECT ON RTC COUNTER DISABLE BYTE INCREMENT CANCEL RTC COMMAND
- 40h = ARM RTC FOR RESET OR BYTE INCREMENT. THIS COMMAND MUST BE WRITTEN PRIOR TO RTC RESET OR FIRST BYTE RESET
- 80h = RESET ALL SIX BYTES OF RTC TO 00h. RESET MUST BE PRECEDED BY WRITING 40h TO ARM RESET FUNCTION
- C0h = RESET ALL SIX BYTES IN RTC COUNTER TO 00H AND REMAIN IN BYTE INCREMENT MODE

Watchdog Timer

WATCHDOG TIMER CONTROL REG WDTCR (0x08) W

- 5Ah = RESET WDT WITH 2 SECOND TIMEOUT
- 57h = RESET WDT WITH 1 SECOND TIMEOUT
- 59h = RESET WDT WITH .5 SECOND TIMEOUT
- 53h = RESET WDT WITH .25 SECOND TIMEOUT
- OTHER = NO EFFECT

WATCHDOG TIMER TEST REG WDTTR (0x09) W

- 51h = CLOCK LSB OF WDT WITH PERIPHERAL CLOCK
- 52h = CLOCK MSB OF WDT WITH PERIPHERAL CLOCK
- 53h = CLOCK LSB & MSB OF WDT WITH PERIPHERAL CLOCK
- 54h = DISABLE WDT (MUST BE PRECEDED BY A WRITE OF 51h,52h, 0R 53h)
- OTHER = NORMAL, WATCHDOG TIMER IS CLOCKED BY 32kHz CLOCK

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