

## EMC Test Report

# DRAFT

## Index

<b>1</b>	<b>ELECTRO MAGNETIC COMPATIBILITY (EMC) SETUP AND DEFINITION .....</b>	<b>4</b>
	EMC TEST STANDARDS.....	4
	IC PERFORMANCE CLASSES .....	4
	DEVICE UNDER TEST .....	4
	PIN DEFINITION .....	5
	PIN SELECTION FOR IMMUNITY AND EMISSION TEST .....	5
	GENERAL TEST SETUP .....	6
	TEST CONDITIONS .....	7
	OPERATION MODES.....	7
	RESET ROUTINE.....	8
	PASS/FAIL CRITERIA FOR IMMUNITY TESTS.....	9
<b>2</b>	<b>CONDUCTED IMMUNITY – TRANSIENT DISTURBANCES (ISO) .....</b>	<b>10</b>
	TEST-/SIMULATION SETUP FOR TRANSIENT DISTURBANCES.....	10
	GENERAL REQUIREMENTS FOR TRANSIENT DISTURBANCES.....	11
<b>3</b>	<b>CONDUCTED IMMUNITY – DIRECT POWER INJECTION (DPI).....</b>	<b>13</b>
	HARDWARE TEST SETUP .....	13
	TEST-/ SIMULATION SETUP FOR DPI.....	14
	SUSCEPTIBILITY LEVEL AREA DEFINITION .....	15
	PASS/FAIL REQUIREMENTS FOR DPI .....	16
	TEST RESULT .....	17
	<i>RF-VS</i> .....	17
	<i>RF-OUT0</i> .....	18
	<i>RF-OUT1</i> .....	19
	<i>RF-OUT2</i> .....	20
	<i>RF-LIN-M</i> .....	21
	<i>RF-LIN-S</i> .....	22
<b>4</b>	<b>CONDUCTED EMISSION - 150Ω DIRECT COUPLING METHOD .....</b>	<b>23</b>
	HARDWARE TEST SETUP .....	23
	TEST-/ SIMULATION SETUP FOR CONDUCTED EMISSION .....	23
	EMISSION LEVELS AREA DEFINITION.....	24
	TEST RESULT .....	25
	<i>RF-VS</i> .....	25
	<i>RF-OUT0</i> .....	25
	<i>RF-OUT1</i> .....	26
	<i>RF-OUT2</i> .....	26
	<i>RF-LIN</i> .....	27
<b>5</b>	<b>CONDUCTED EMISSION - LISN METHOD.....</b>	<b>28</b>
	HARDWARE TEST SETUP .....	28
	TEST-/ SIMULATION SETUP FOR CONDUCTED EMISSION .....	28
	EMISSION LEVELS CLASSIFICATION .....	29
	REQUIREMENTS FOR CONDUCTED EMISSION (LISN) .....	29
	TEST RESULT .....	30
	<i>Emission on Vbat</i> .....	30
<b>6</b>	<b>RADIATED EMISSION (RE)- ALSE METHOD .....</b>	<b>31</b>
	HARDWARE TEST SETUP .....	31
	GENERAL TEST-SETUP FOR RADIATED EMISSION.....	31
	HARDWARE TEST-SETUP FOR RADIATED EMISSION.....	32
	REQUIREMENTS FOR RADIATED EMISSION (ALSE).....	32
	TEST RESULT .....	33
	<i>Emission on Vbat</i> .....	33
	<b>APPENDIX .....</b>	<b>34</b>



---

TEST PULSE DEFINITION FOR THE 12V SYSTEM .....	34
DEFINITION FOR LIN COMMUNICATION SIGNALS .....	37
EMC TESTBOARD SCHEMATIC .....	38
EMC TESTBOARD LAYOUT.....	39
RX-TX ADAPTER.....	40
<b>REVISION HISTORY: .....</b>	<b>41</b>

# 1 Electro Magnetic Compatibility (EMC) Setup and Definition

## EMC Test Standards

Overview about all required measurement methods and respective standards.

**Table 1** General information about the measurement standards as off 2022-05-16

Measurement method	Coupling mode	Reference to the standard	Abbreviation
-	-	IEC 62215-3: 2013	IC Performance Class
<a href="#">Transient disturbance</a>	Conducted	ISO 7637-1: 2015 ISO 7637-2: 2011 ISO 7637-3: 2016 ISO 16750-2: 2012	ISO
<a href="#">Direct Power Injection (DPI)</a>	Conducted	IEC 62132-1: 2015 IEC 62132-4: 2006	DPI
<a href="#">Emission direct coupling</a>	Conducted	IEC 61967-1: 2018 IEC 61967-4: 2021	150Ohm
<a href="#">Emission with artificial Network</a>	Conducted	IEC CISPR 25 : 2021	LISN
<a href="#">Radiated Emission ALSE</a>	Radiated	IEC CISPR 25 : 2021	ALSE Absorbed Lined Shielded Enclosure

## IC Performance Classes

[According to](#) Table 1

The test results are classified from A<sub>IC</sub> to E<sub>IC</sub>. Table 2 shows the definition for each Class.

**Table 2** Definition of the IC Performance classes used for [Transient-](#) and [RF- Immunity testing](#)

Class	Content
A <sub>IC</sub>	all monitored functions of the IC perform within the defined tolerances during and after exposure to disturbance.
B <sub>IC</sub> <sup>1</sup>	short time degradation of one or more monitored signals during exposure to disturbance is not evaluable for IC only. Therefore this classification may not be applicable for ICs
C <sub>IC</sub>	at least one of the monitored functions of the IC is out of the defined tolerances during the disturbance but returns automatically to the defined tolerances after the exposure to disturbance;
D1 <sub>IC</sub> D2 <sub>IC</sub>	at least one monitored function of the IC does not perform within the defined tolerances during exposure and does not return to normal operation by itself. The IC returns to normal operation by manual intervention Class D1IC: the IC returns to normal operation by manual intervention: (e.g. reset); Class D2IC: the IC returns to normal operation by power cycling the device
E <sub>IC</sub>	at least one monitored function of the IC does not perform within the defined tolerances after exposure and cannot be returned to proper operation.

## Device Under Test

**Table 3** Device Under Test Information

Sales Code	Date Code	Design Step
TLD4020-3ET		A11

<sup>1</sup> Short time degradation of one or more monitored signals can be tolerable in the application by its error handling. This error handling is unknown in most cases for IC test.

## Pin Definition

**Table 4** General pin classification

Class	Definition
global pin	A 'global' pin carries a signal or power, which enters or leaves the application board.
local pin	A 'local' pin carries a signal or power, which does not leave the application board. It remains on the application PCB as a signal between two components with or without additional EMC components.

## Pin Selection for Immunity and Emission Test

The following Table lists all IC Pins in order to classify and to select the required EMC-test.

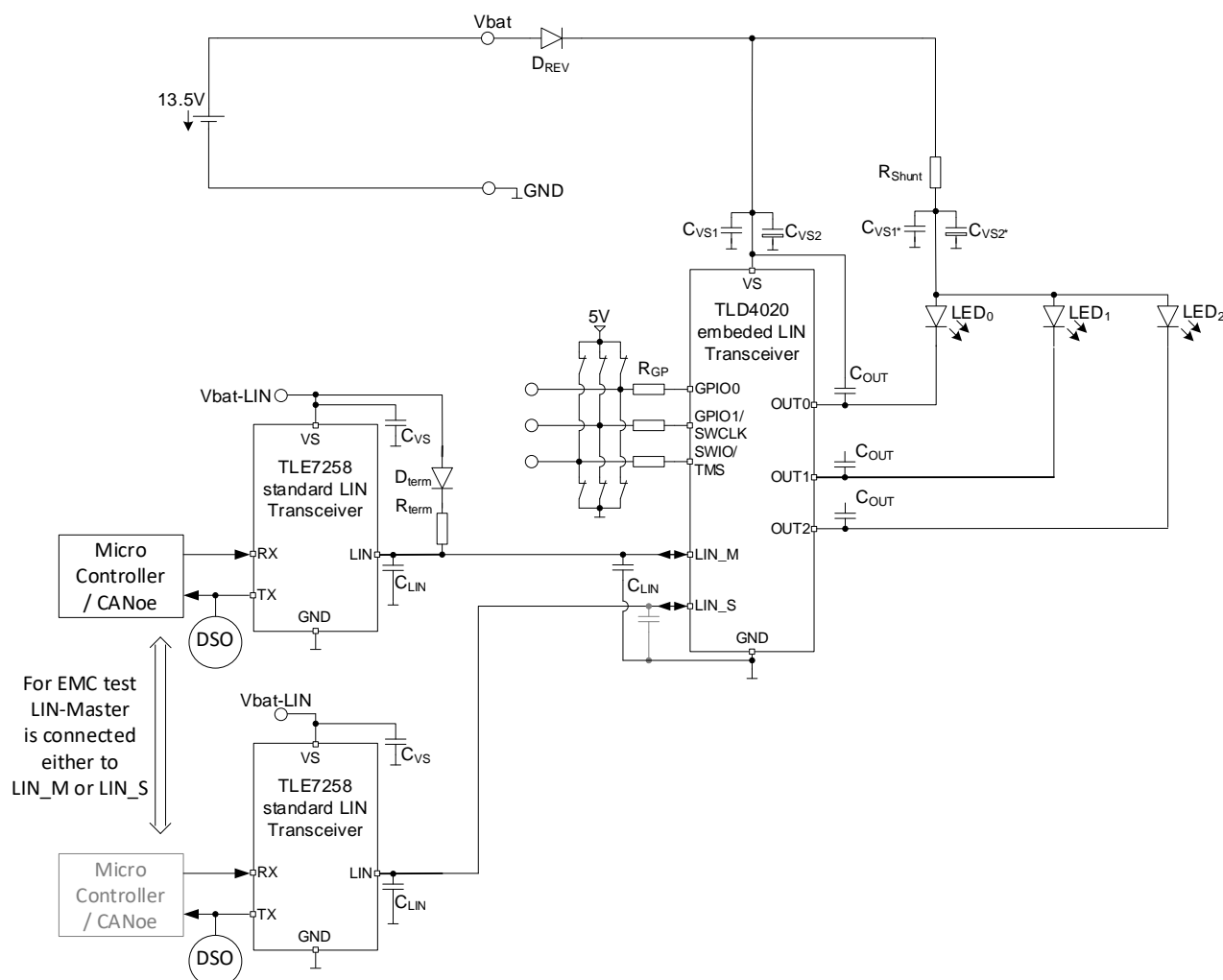
The requirement listing for [RF-immunity](#), [RF-Emission-150R](#) and [RF-Emission-LISN](#) are based on Table 5 .

**Table 5** IC-Pin definition considering Pin-class and required EMC test/simulation. Listing all IC Pins.

Pin		class	Immunity		Emission
			<u>Electrical transients (ISO)</u>	<u>Conducted Immunity (DPI)</u>	<u>Conducted Emission (150Ω)</u>
1	VS	global	X	RF-VBAT	RF-VBAT
2	NC	—	—	—	—
3	NC	—	—	—	—
4	GND	global	—	—	—
5	NC	—	—	—	—
6	NC	—	—	—	—
7	LIN_M	global	X	RF-LIN_M	RF-LIN_M
8	LIN_S	global	—	RF-LIN_S	RF-LIN_S
9	GPIO0	local	—	RF-GPIO0	RF-GPIO0
10	GPIO1/SWCLK	local	—	RF-GPIO1	RF-GPIO1
11	SWIO/TMS	local	—	—	—
12	NC	—	—	—	—
13	NC	—	—	—	—
14	OUT0	global	—	RF-OUT0	RF-OUT0
15	OUT1	global	—	RF-OUT1	RF-OUT1
16	OUT2	global	—	RF-OUT2	RF-OUT2

## General Test Setup

Figure 1 outlines all needed external components to operate the DUT under application conditions. These components can influence the final EMC result. They are treated as inherent part of the DUT during the EMC characterization.



**Figure 1** Device under Test including the applicative external components that are needed to bring the DUT into its normal operation mode as well as the allowed additional components.

**Table 6** Part listing for normal operation mode

Reference	Value	Type	Comment
Drev	1A 200V	RB168MM200TFTR	to low reverse voltage!
Cvs1	100nF	X7R, 50V, 0805	
Cvs21	4.7uF	X7R, 50V, 1210	
COUT		X7R, 50V, 0805	
CLIN	Open / 110pF	X7R, 50V, 0805	IEC 62228-2 specifies limits with and without CLIN
DTerm		BYD17K	Optional
RTerm	1kR	X7R, 50V, 0805	Master Termination
LED		OVSTRGBB1CR8	one color on each 50mA
Rshunt,on/active	10Ohm		51mA per channel
Rshunt,off/sleep	1kOhm		<100uA per channel

## Test Conditions

All general EMC-Test conditions are listed in Table 7 .

**Table 7** General EMC-Test conditions

Parameter	Symbol	Value	Unit	Remark
Voltage reference	—	—	—	All voltages are referred to PCB-GND
Temperature	T <sub>A</sub>	23 +/-5	°C	—
Supply voltage	V <sub>s</sub>	13.5 ± 0.5 12 ± 0.5	V	All test but not Starting Profile Only for Starting Profile
Input voltage high level	V <sub>IN,high</sub>	5 ± 5%	V	—
Input voltage low level	V <sub>IN,low</sub>	0 + 5%	V	—

## Operation Modes

**Table 8** Pin setting or/and alternatively SPI register in order to bring the device in the desired operation mode for [Transient-](#) and [RF-Immunity](#) test as well as for the [RF-Emission test150R](#) and [Emission test LISN](#) .

Test Case	Operation Mode	Standard Test	LIN Test	Comment
TC1	Off-all	X	—	All channels off
TC2	On-all	X	—	All channels on, d=100% 10mA each , no PWM
TC3	Pwm-all	X	—	All channels pwm 300Hz, d=50% 10mA each
TC4	ADC-check	X	—	Read OUT1 voltage in ON Mode
TC5	Sleep, unwanted wake up	—	X	Check OUT0 on/off
TC6	Sleep, wanted wake up	—	X	Check OUT0 on/off sending <a href="#">LIN Pattern TX3</a>
TC7	LIN-respond	—	X	Device has to respond on this pattern. GPIO-PWM by <a href="#">LIN Pattern TX2</a> .
TC8		—	X	Interoperability test check that LIN communication with additional standard LIN Transceiver is not affected by DUT. Sending <a href="#">0xA5A5</a> and read RX Master on LIN_M Receiver on LIN_S Master on LIN_S Receiver on LIN_M

Note :

**TC4** ADC Check : Average ( milli s range ) of ADC under normal undisturbed condition ADC result is internally stored as reference Value by sending a dedicated command. During EMC test average ADC readout is internally compared with previous stored reference value, readout within tolerance is pass result otherwise fail result. Readout is extern triggered by rising edge on GPIO1. GPIO0 indicate pass / fail result by digital high / low output value.

**TC5 & TC6:** special device Firmware for this test. If device wakes up OUT0 is turned on. After 1ms device returns automatically into sleep mode.

## Reset Routine

Before performing any EMC test the device is to be set into a defined functional state. This is done by the reset routine.

**Table 9** Reset routine

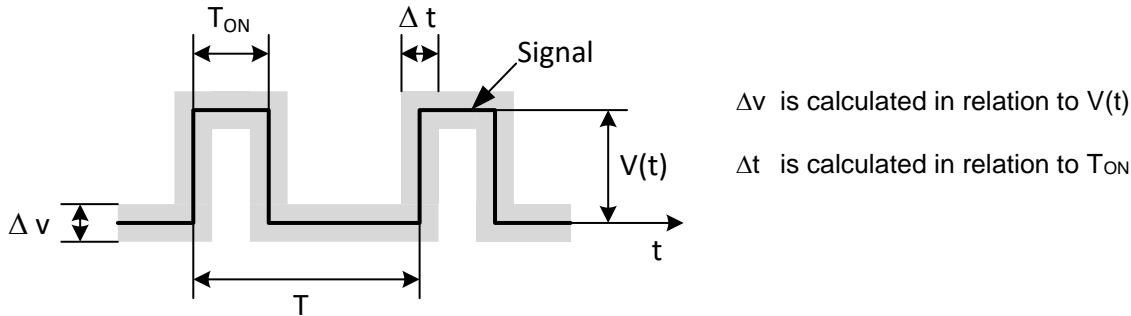
Action	Pin -action	comment
1	Turn off Vs	No dedicated reset requirement defined
2	Wait 1sec	
3	Turn on Vs	



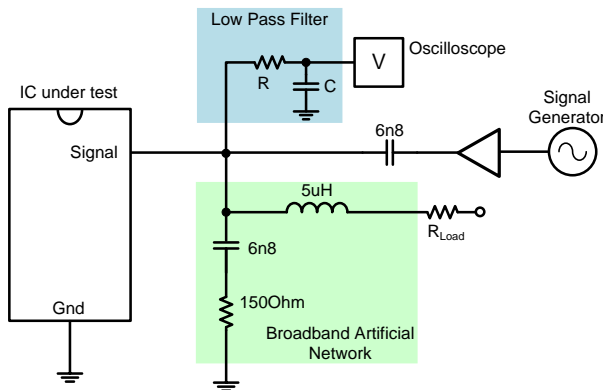
## Pass/Fail Criteria for Immunity Tests

For evaluating the device behavior during Transient-Immunity and RF-Immunity tests monitoring criteria have to be defined. The device functionality is monitoring by checking required signals by an oscilloscope. Therefore a tolerance band for the nominal behavior is defined in amplitude and time. A signal within this specified tolerance band is a pass signal. For register readouts the nominal pass value for the register content is defined. For RF-immunity tests the monitoring is done with powered RF signal. The monitoring signal should not be superimposed by RF-signals therefore a low pass filter is inserted for RF-immunity tests.

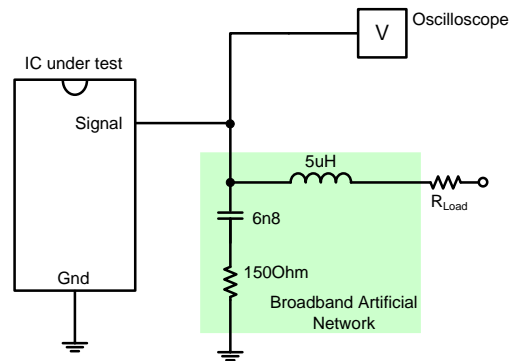
Table 10 defines the tolerance band for different monitor Pins as well as the nominal register values.



**Figure 2** Tolerance band specification



**Figure 3** Signal probing with low-pass filter used for RF-Immunity test



**Figure 4** Signal probing without Low Pass Filter used for Transient-Immunity test

**Table 10** Pass / Fail Criteria for [Transient](#)- and [RF](#)-Immunity test.

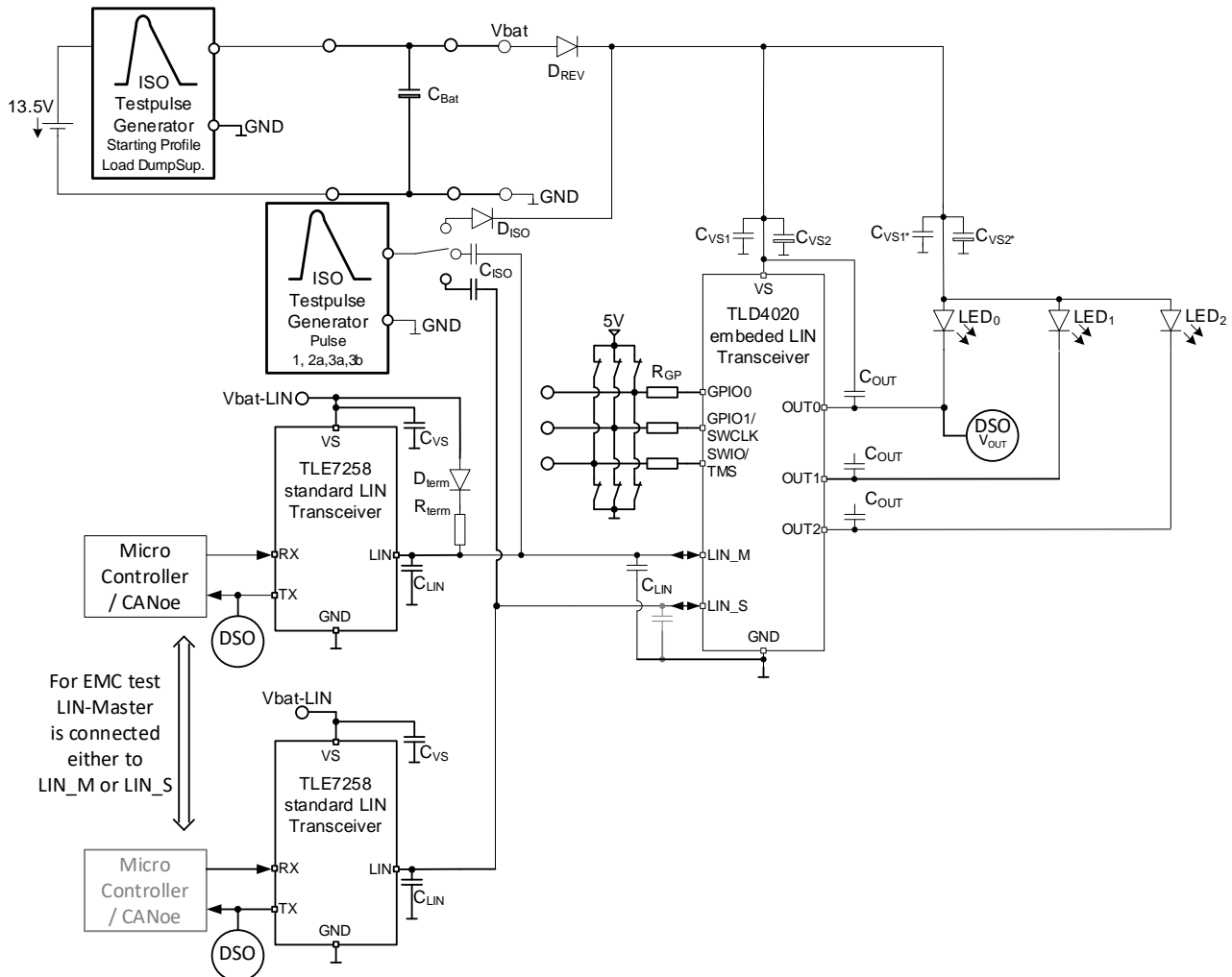
Monitoring	Monitoring Pin/register	Operation mode	Failure Criteria		
			Tolerance Band		Value
			Amplitude	Time	
M0	—	PWM	—	—	—
M1	$I_{LED}$	OFF	$< 100\mu A$	—	High/Low level
M2	$I_{LED}$	ON / PWM	$\pm 10\%$	$\pm 10\%$	Voltage within tolerance band
M3	ADC readout	ON	$\pm 20\%$	—	Average value compare to undisturbed readout
M4	$V_{OUT0}$	SLEEP	$\Delta V_{out0}$	—	Out0 stays off (Auto Trigger)
M5	$V_{OUT0}$	Wake up	$\Delta V_{out0}$	—	OUT0: off=>on
M6	RX readout		$\pm 10\%$	$\pm 10\%$	Voltage within tolerance band

## 2 Conducted Immunity – Transient Disturbances (ISO)

“Conducted Immunity – Transient Disturbances” examines electrical transient conduction along supply lines according to Table 1, plus special electrical transients based on customer requirements.

### Test-/Simulation Setup for Transient Disturbances

Figure 5 shows the basic transient immunity test- simulation-setup for the injection of the standardized ISO pulses. For the pulse definition refer to the Appendix 5.



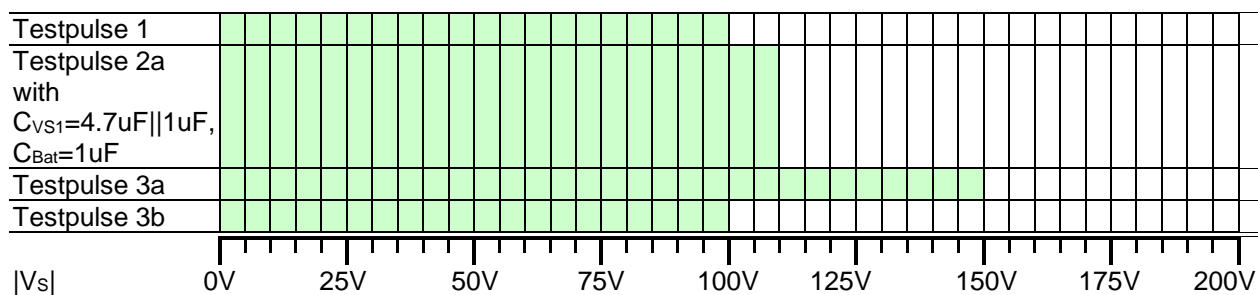
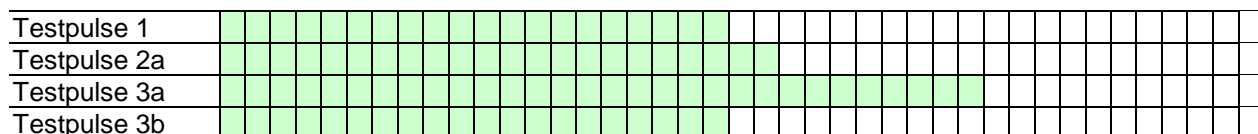
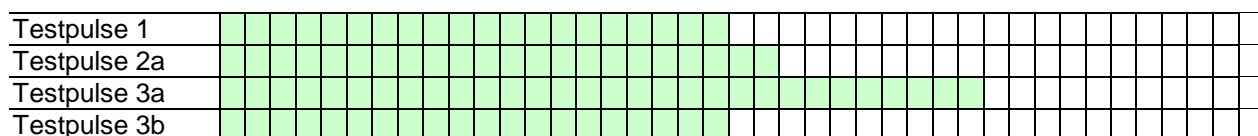
**Figure 5** Transient immunity test/simulation setup for injection into Vbat, ISO pulses 1, 2a, 3a, 3b, Starting Profile and Load Dump Suppression Pulse

## General Requirements for Transient Disturbances

The following tables outline the absolute minimum and target value for transient immunity of 12V system.

**Table 11** Transient immunity requirements [IC Performance Class A<sub>IC</sub>](#)

Test Pulse	Test Pulse voltage		Injection	Coup- ling	BUS Filter	<a href="#">IC Performance Class Requirement Operation mode</a>					
	Absolute min. requirement	Target value				TC1	TC2	TC5	TC6	TC7	TC8
<a href="#">1</a>	-100V	-100V	Vbat	direct	X	—	—	—	—	—	—
					—	—	—	—	M2	—	
			LIN_M	1nF	X	—	—	M4	M5	M2	M6
					—	—	—	M4	M5	M2	M6
<a href="#">2a</a>	+75V	+112V	Vbat	direct	X	—	—	—	—	—	—
					—	—	—	—	M2	—	
			LIN_M	1nF	X	—	—	M4	M5	M2	M6
					—	—	—	M4	M5	M2	M6
<a href="#">3a</a>	-150V	-150V	Vbat	direct	X	—	—	—	—	—	—
					—	—	—	—	M2	—	
			LIN_M	1nF	X	—	—	M4	M5	M2	M6
					—	—	—	M4	M5	M2	M6
<a href="#">3b</a>	+100V	+100V	Vbat	direct	X	—	—	—	—	—	—
					—	—	—	—	M2	—	
			LIN_M	1nF	X	—	—	M4	M5	M2	M6
					—	—	—	M4	M5	M2	M6
<a href="#">Starting Profile</a>	+5.5V	+5.5V	Vbat	direct	X	M1	—	—	—	—	—
<a href="#">Load Dump Suppression</a>	+35V	+39V	Vbat	direct	X	M1	M2	—	—	—	—

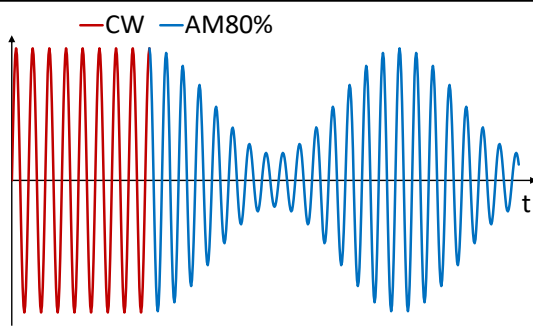
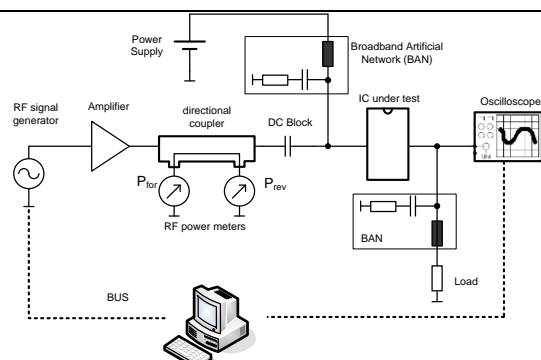
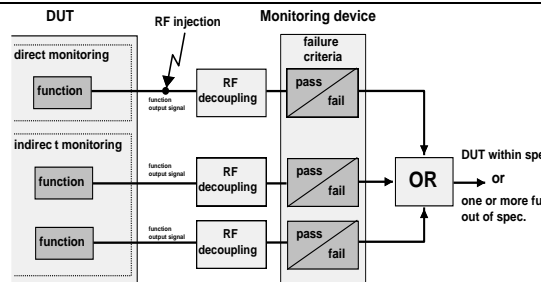
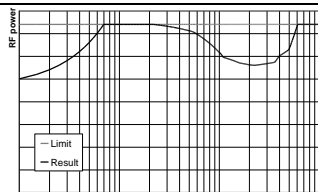
**Table 12** Transient Disturbance Result injected to Vbat Line, Operation mode TC7 = Lin respond**Table 13** Transient Disturbance Result injected to LIN-M, Operation mode TC7 = Lin respond**Table 14** Transient Disturbance Result injected to LIN-M, Operation mode TC5 and TC6

### 3 Conducted Immunity – Direct Power Injection (DPI)

“Conducted Immunity – Direct power Injection” examines the RF susceptibility level [according to](#) Table 1

#### Hardware test setup

**Table 15** Disturbance signal, Test bench and Presentation

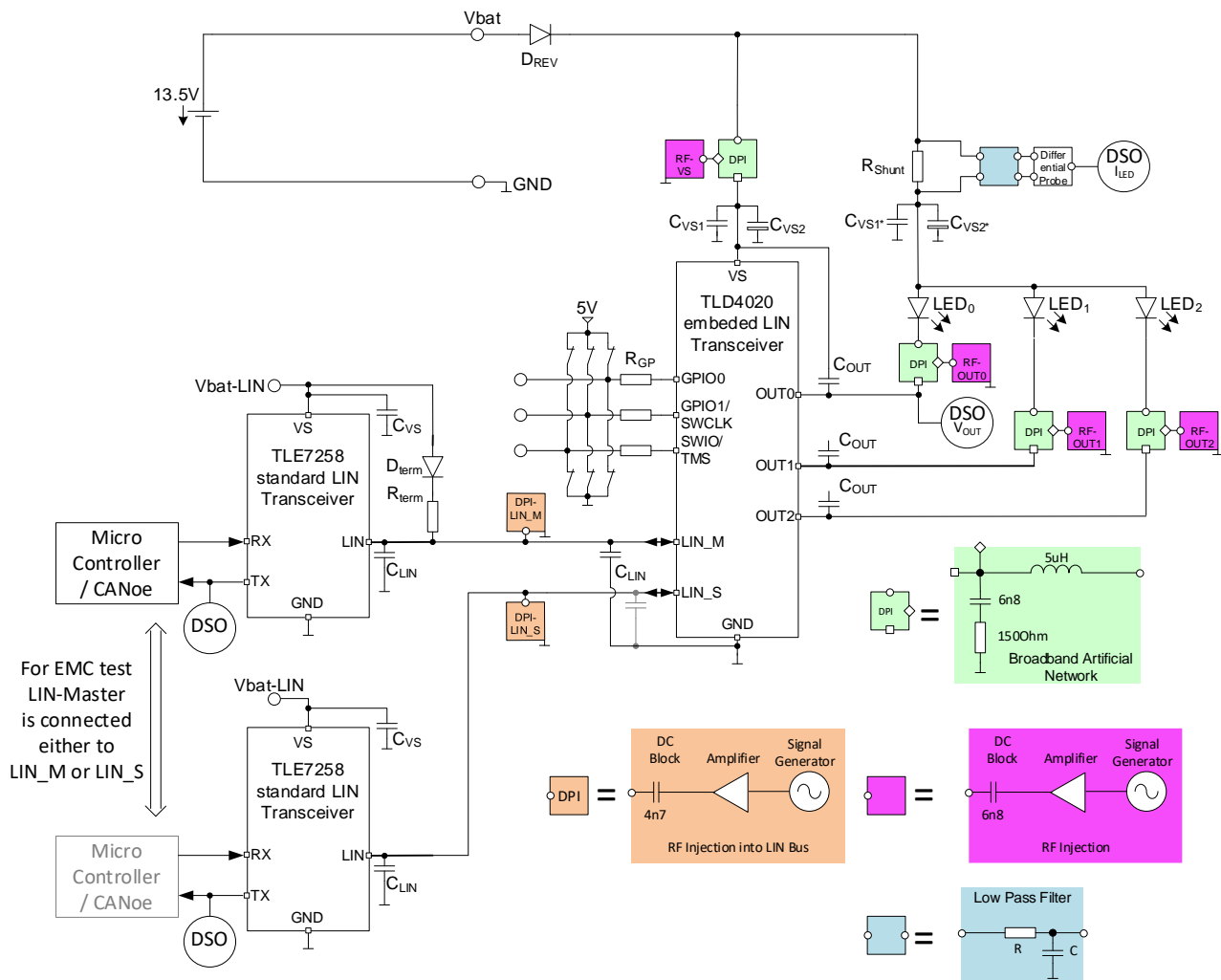
Forward power:	17 dBm (local pin) 37 dBm (global pin)	
Modulation:	CW (no modulation) AM (80%, 1kHz sine wave, $P_{PEAK,AM} = P_{PEAK,CW}$ )	
Dwell time:	$t_D = 1s$ *) can be increased in order to do current averaging for monitoring	
Monitoring time:	$t_M = 0.5s$ )	
Test Bench	A signal generator is used to provide the disturbance signal that is further amplified. A directional coupler and a power meter are used to measure the actual forward power that is coupled to the IC under test. The DC supply and the load are connected to broadband artificial networks. To monitor the behaviour of the IC measurement devices (e.g. oscilloscopes) are used	
DUT monitoring	The monitored signals are combined to a logical sum "within specification or out of specification" as shown in the figure. As monitoring device an oscilloscope with a programmable signal tolerance mask is used. To prevent the monitoring device from the disturbance a RF decoupling filter is necessary	
Typical diagram	The graph in the immunity diagram shows the value of the maximum injected RF power to a pin up to that the DUT operates without any failure. The maximum RF power to apply is defined by the limit line.	

**Table 16** Frequency ranges for direct power injection test

Method	Frequency range			Frequency step	RF power step
DPI	1 MHz	to	10 MHz	0.5 MHz	0.2 dB
	10 MHz	to	100 MHz	1 MHz	0.2 dB
	100 MHz	to	200 MHz	2 MHz	0.2 dB
	200 MHz	to	400 MHz	4 MHz	0.2 dB
	400 MHz	to	1000 MHz	10 MHz	0.2 dB

## Test-/ Simulation Setup for DPI

Below picture show the conducted immunity test/simulation setup.



**Figure 6** Conducted RF-Immunity test/simulation setup

## Susceptibility Level Area Definition

The following figure shows the susceptibility level scheme for the DPI- classification of global and local pins.

### Above Class III:

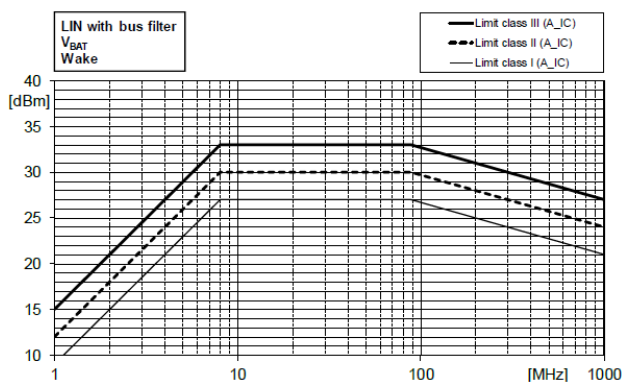
The Class III defines a range where usually no susceptibility issues occur on device level. The test Limit represents the design target. The Class III level itself represents the absolute minimum requirement.

### Class I:

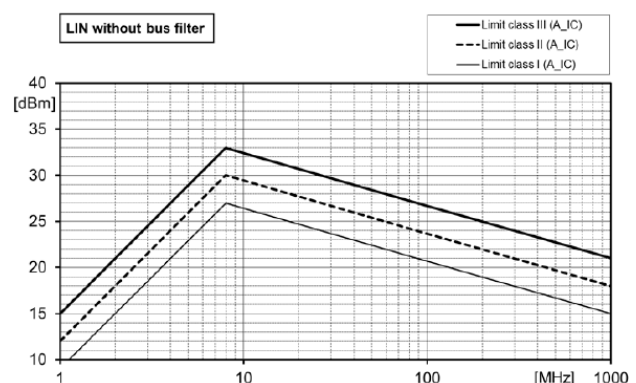
A result between Class III and Class I defines a range where additional simple external filtering/decoupling components usually improves the susceptibility level back to the Class III range. In the unlikely event that the susceptibility level is within the Class III and Class I although external components are used, please align with the EMC and AE colleagues on the further proceeding.

### Below Class I:

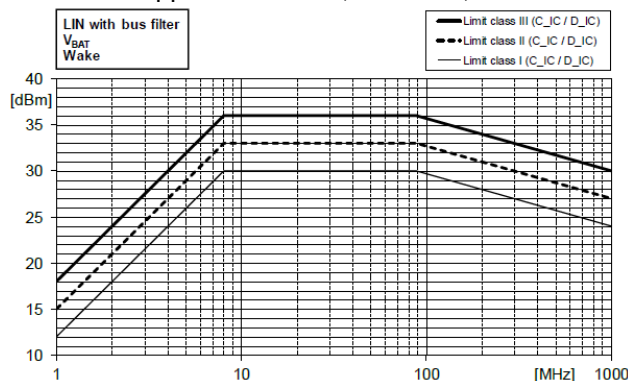
A result below Class I is a severe and non-acceptable susceptibility level for the DUT with and without additional external components.



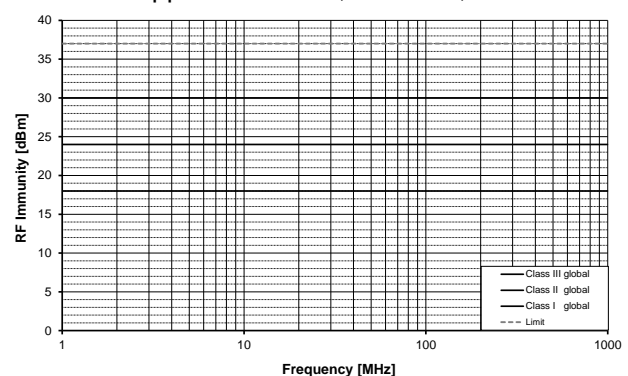
**Figure 7** “LIN with bus filter”  
[Functional Status](#)  $A_{IC}$   
 Applicable for VS, LIN-BUS, Wake



**Figure 8** “LIN without bus filter”  
[Functional Status](#)  $A_{IC}$   
 Applicable for VS, LIN-BUS, Wake



**Figure 9** “LIN with bus filter”  
[Functional Status](#)  $C_{IC}$  or  $D_{IC}$   
 Applicable for VS, LIN-BUS, Wake



**Figure 10** “DPI global Pins”  
 Susceptibility level for DPI global Pins

## Pass/Fail Requirements for DPI

In general the green area has to be reached. If the test without external components results in the yellow area then a second test with external components needs to result in the green area.

**Table 17** Conducted immunity requirements (test levels), [Pin selection regarding](#) Table 5

RF-injection into Pin	Target value	IC Performance Class & Limit	BUS Filter	Modulation, Pass / Fail Criteria and Operation Mode							
				TC1	TC2	TC3	TC4	TC5	TC6	TC7	TC8
RF-VS	37dBm	A <sub>IC</sub> , DPI Global	X	CW M1	CW M2	CW M2	CW M3	—	—	—	—
	36dBm	A <sub>IC</sub> , LIN with BUS filter	X	—	—	—	—	—	—	—	—
		A <sub>IC</sub> , LIN without BUS filter	—	—	—	—	—	CW,AM M4	—	CW,AM M2	—
		D <sub>IC</sub> , LIN without BUS filter	—	—	—	—	—	—	—	CW M0	—
RF-OUT0,1,2	37dBm	A <sub>IC</sub> , DPI Global	—	CW M1	CW M2	—	—	—	—	—	—
RF-LIN_M	36dBm	A <sub>IC</sub> , LIN with BUS filter	X	—	—	—	—	CW M4	CW M5	CW M2	CW M6
		A <sub>IC</sub> , LIN without BUS filter	—	—	—	—	—	CW,AM M4	CW,AM M5	CW,AM M2	CW,AM M6
		D <sub>IC</sub> , LIN with BUS filter	X	—	—	—	—	—	—	CW M0	—
RF-LIN_S	36dBm	A <sub>IC</sub> , LIN with BUS filter	X	—	—	—	—	CW M4	CW M5	CW M2	CW M6
		A <sub>IC</sub> , LIN without BUS filter	—	—	—	—	—	CW,AM M4	CW,AM M5	CW,AM M2	CW,AM M6
		D <sub>IC</sub> , LIN with BUS filter	X	—	—	—	—	—	—	CW M0	—

Note: Bus Filter always only to the LIN Bus used for RF injection.





Test Result

RF-VS

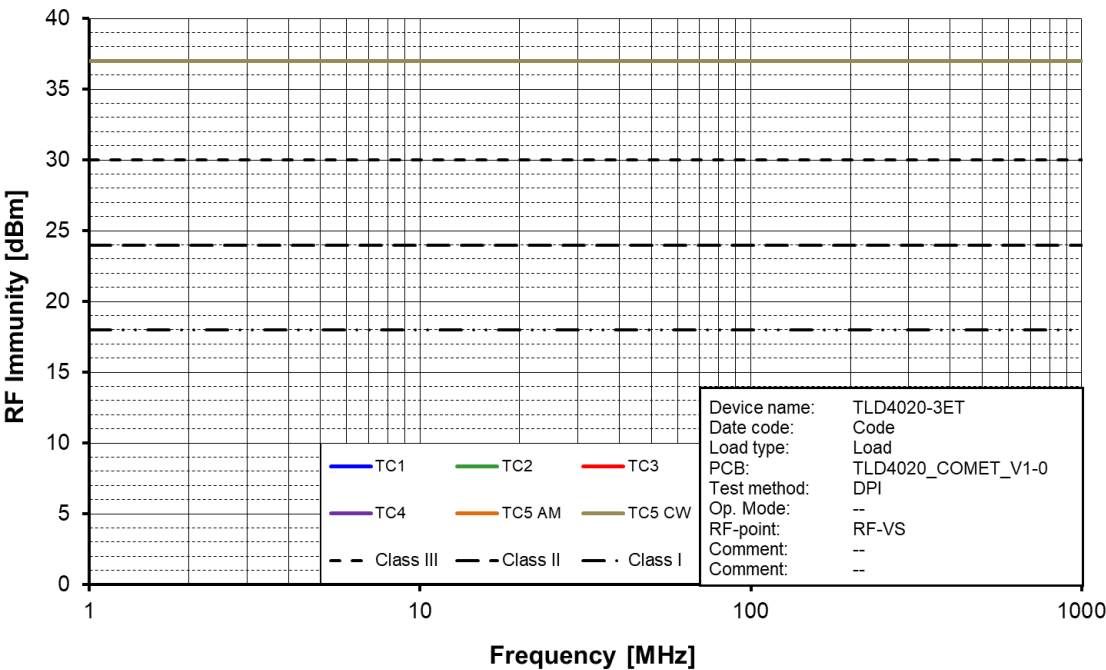


Figure 11 Conducted RF-Immunity into VS.

## RF-OUT0

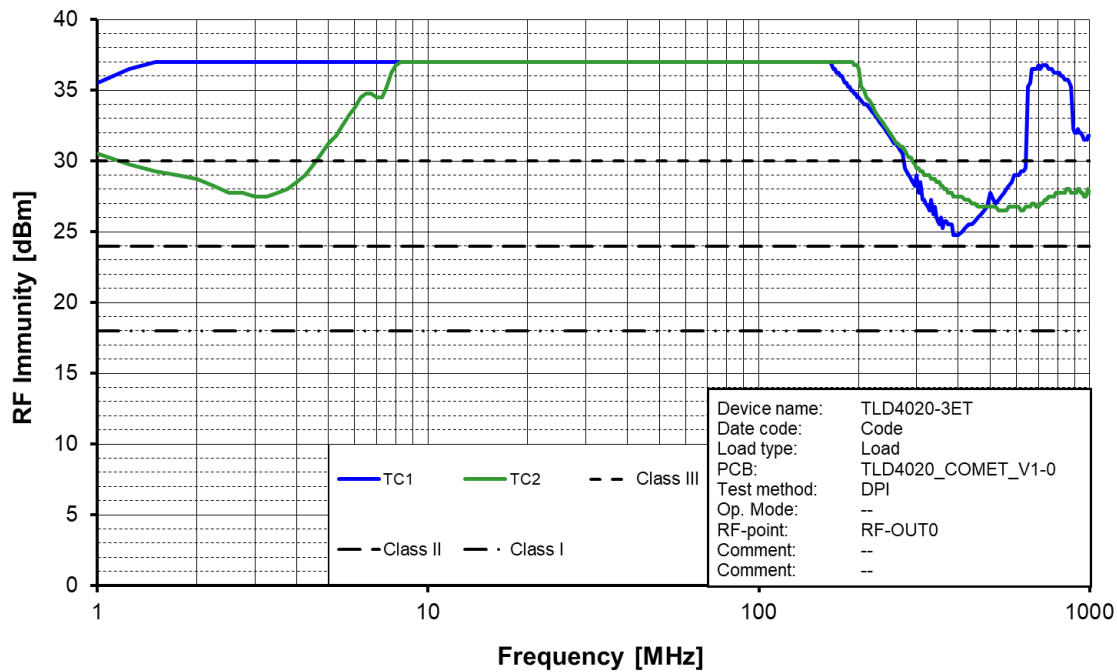


Figure 12 Conducted RF-Immunity into OUT0.

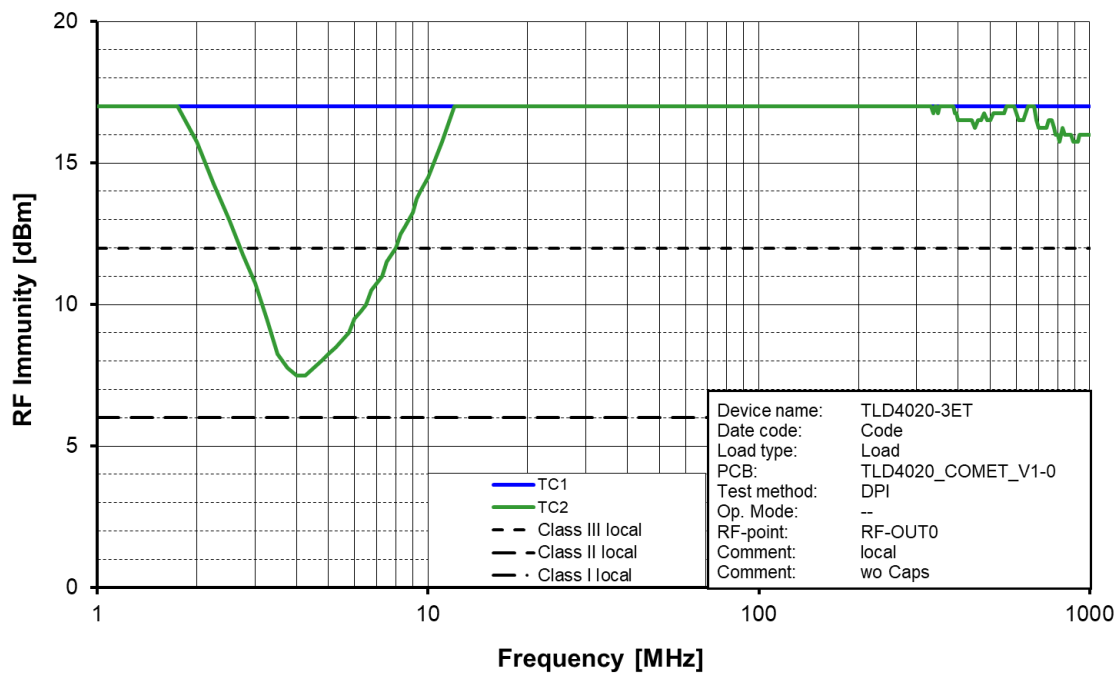


Figure 13 Conducted RF-Immunity into OUT0 for local limits with Cout left open.

## RF-OUT1

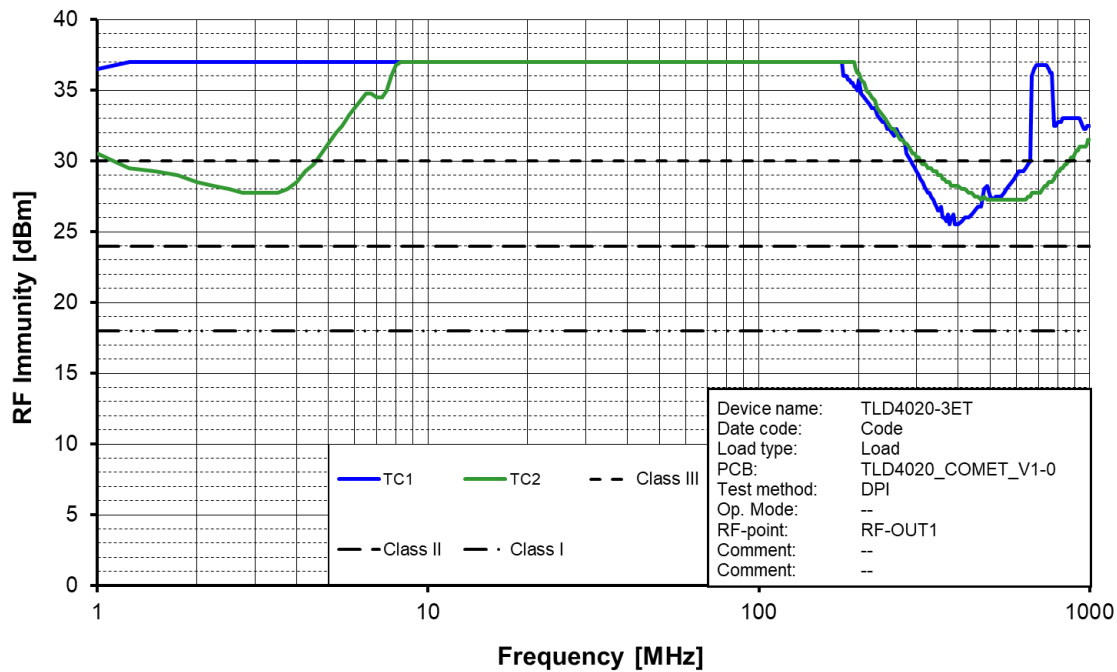


Figure 14 Conducted RF-Immunity into OUT1.

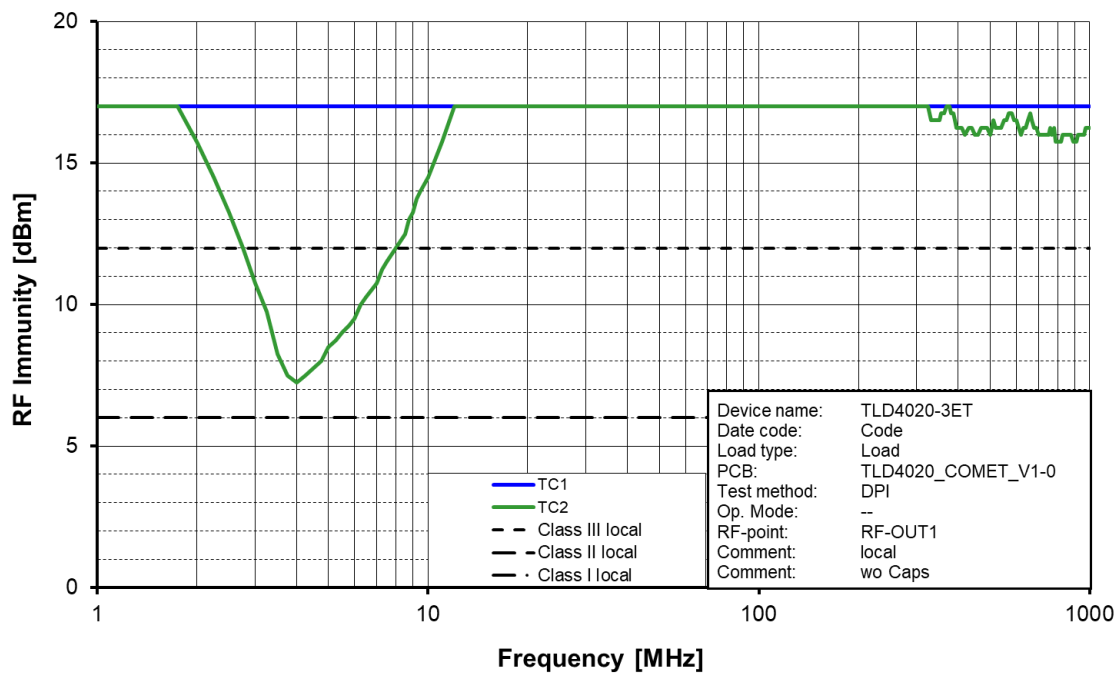


Figure 15 Conducted RF-Immunity into OUT1 for local limits with Cout left open.

## RF-OUT2

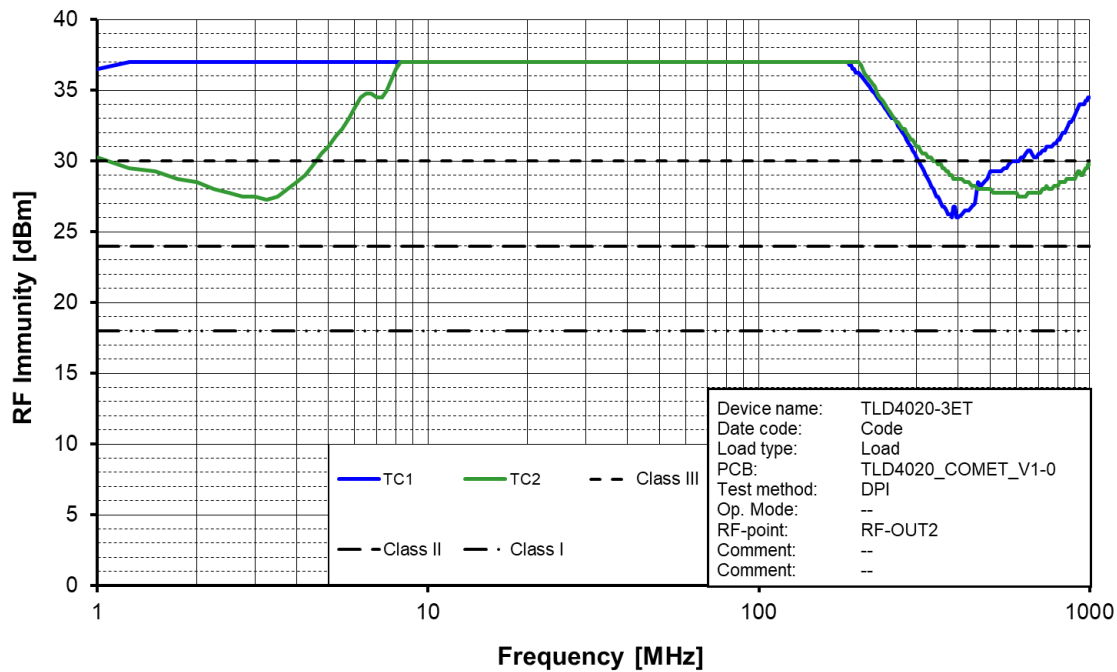


Figure 16 Conducted RF-Immunity into OUT2.

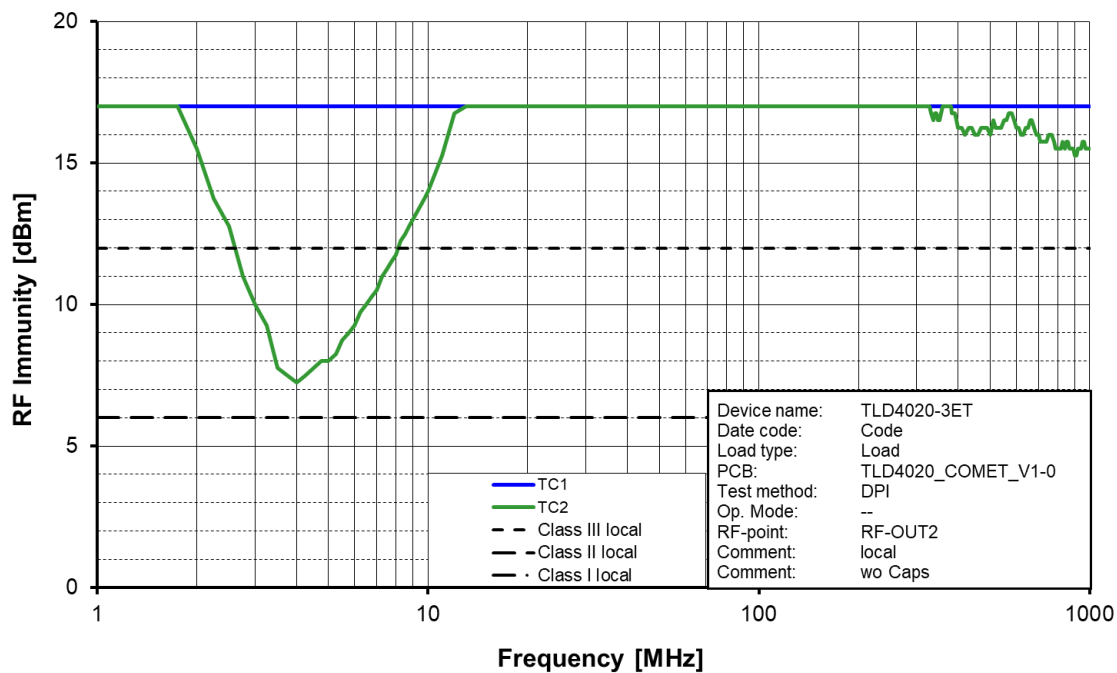
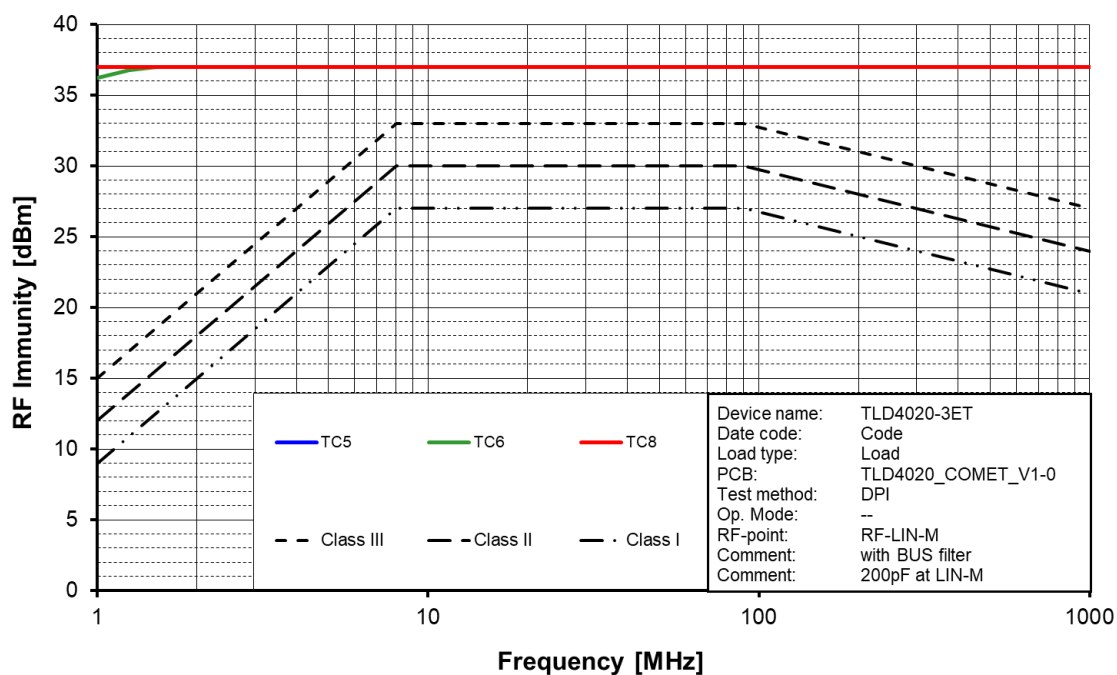


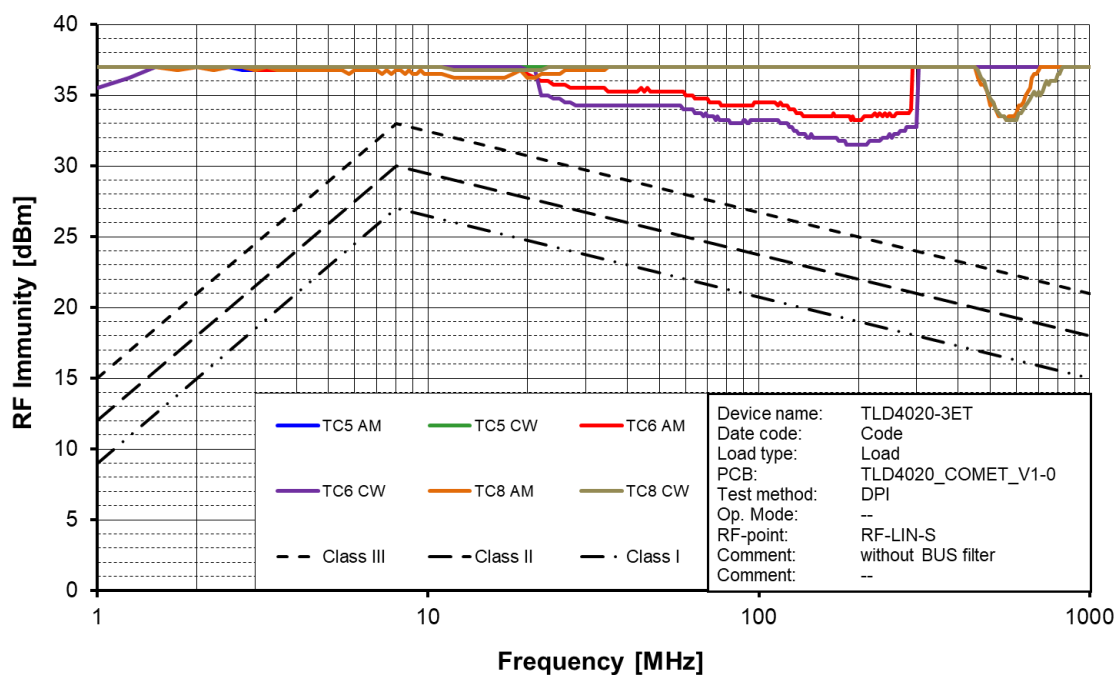
Figure 17 Conducted RF-Immunity into OUT2 for local limits with Cout left open.

## RF-LIN-M



**Figure 18** Conducted RF-Immunity into LIN-M with BUS filter.

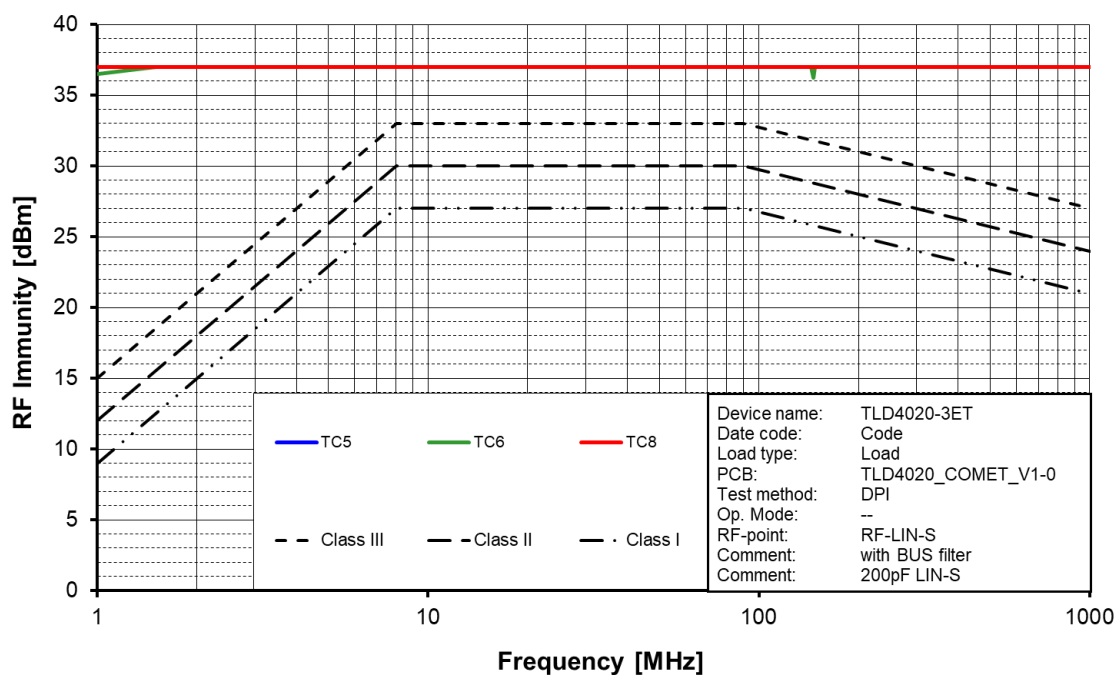
TC5 = sleep unwanted wake, TC5 = sleep wanted wake, TC8 = interoperability check



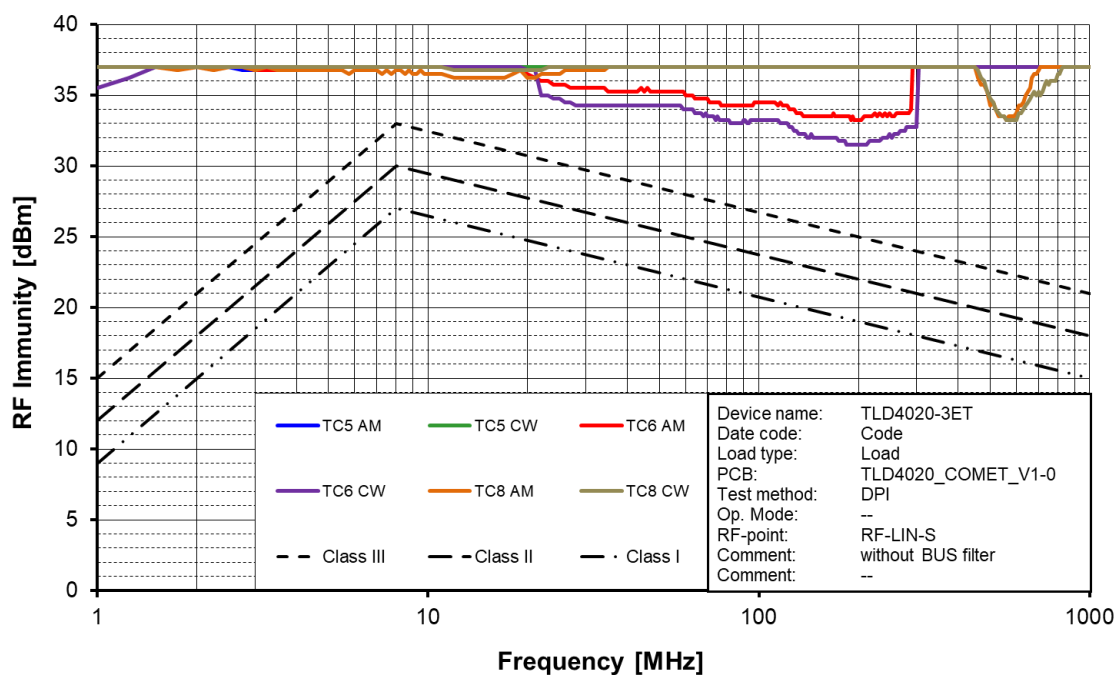
**Figure 19** Conducted RF-Immunity into LIN-M without BUS filter.

TC5 = sleep unwanted wake, TC5 = sleep wanted wake, TC8 = interoperability check

## RF-LIN-S



**Figure 20** Conducted RF-Immunity into LIN-M with BUS filter, 200pF at LIN-S.  
 TC5 = sleep unwanted wake, TC5 = sleep wanted wake, TC8 = interoperability check



**Figure 21** Conducted RF-Immunity into LIN-M without BUS filter.  
 TC5 = sleep unwanted wake, TC5 = sleep wanted wake, TC8 = interoperability check

## 4 Conducted Emission - 150Ω direct coupling method

“Conducted Emission – 150Ω direct coupling” examines conducted emissions [according to](#) Table 1

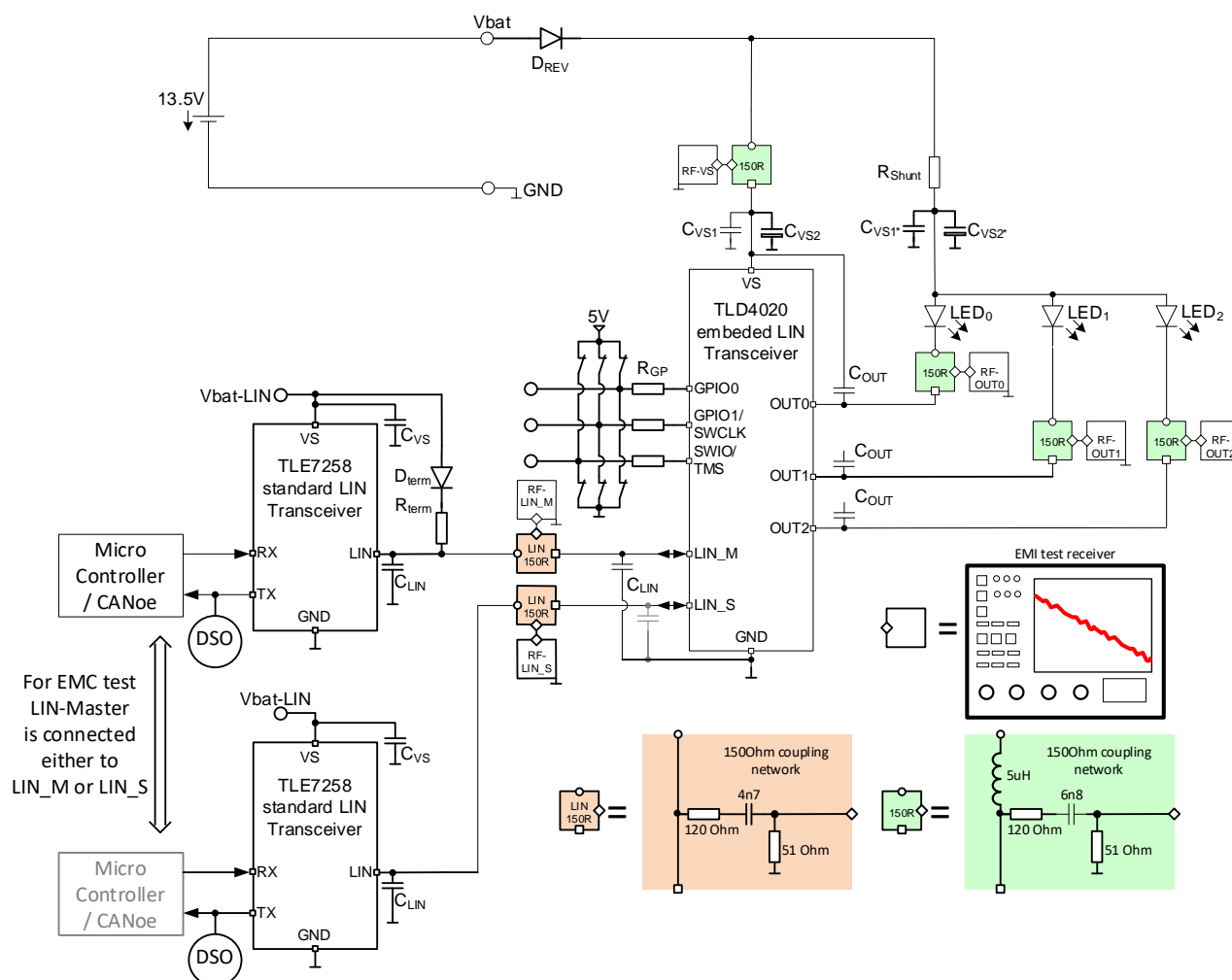
### Hardware Test Setup

**Table 18** Frequency range and settings for the EMI test receiver

Frequency range			Receiver			
			RBW	step size	Meas. time	Detector
150 kHz	to	30 MHz	9 kHz	5 kHz	$\geq 10$ ms	Max. Peak
30 MHz	to	1 GHz	120 kHz	50 kHz	$\geq 10$ ms	

### Test-/ Simulation Setup for Conducted Emission

Below picture show the conducted emission test/simulation setup.



**Figure 22** Conducted RF-Emission test/simulation setup

## Emission Levels Area Definition

Below Figure shows the emission level scheme for the 150Ω classification for global and local pins.

### Below Class III:

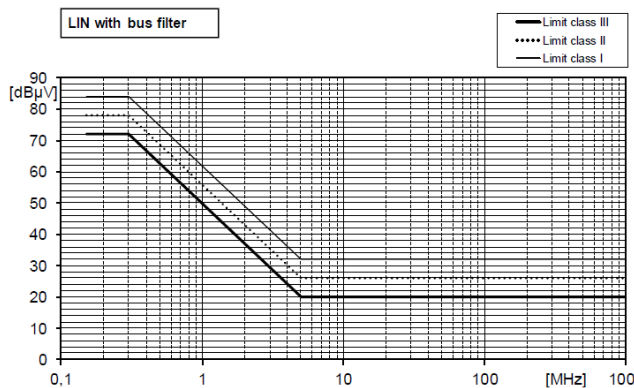
The area below Class III defines a range where usually no emission issues occur on device level. The Class III value itself represents the internal design target.

### Class I:

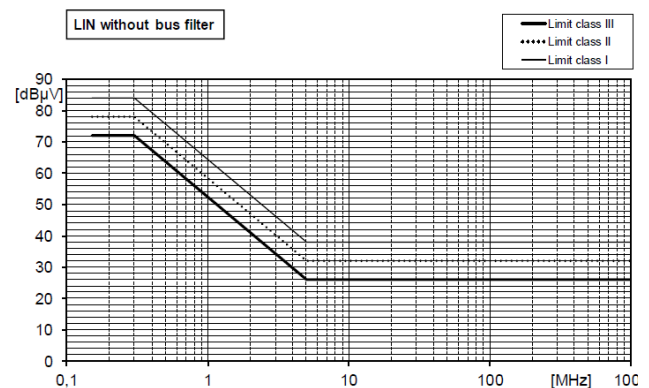
A result between **Class III** and **Class I** defines a range where additional simple external filtering/decoupling components usually improve the emission level back to the **Class III** range. In the unlikely event that the emission level is within **Class III** and **Class I** range although external components are used, please align with the EMC and AE colleagues on the further proceeding.

### Above Class I

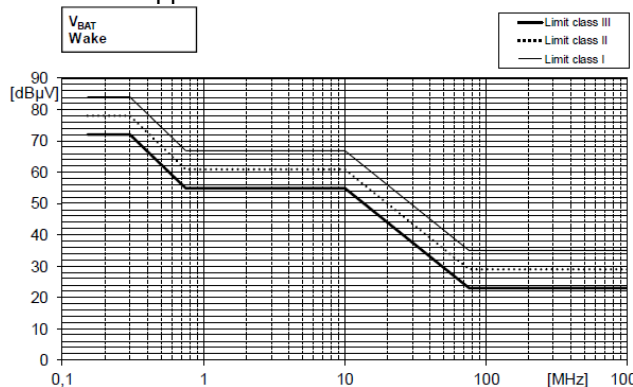
The result above **Class I** is not-acceptable.



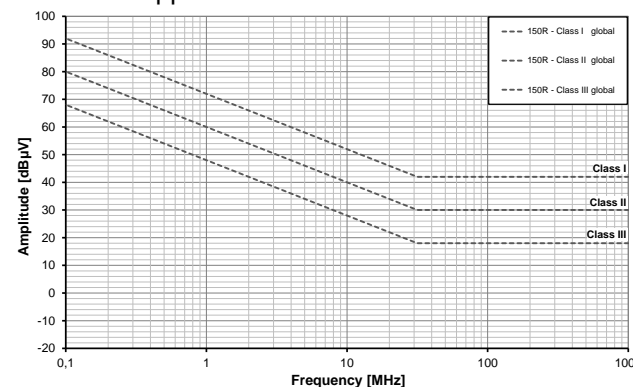
**Figure 23** “LIN with bus filter”  
Applicable for LIN-BUS



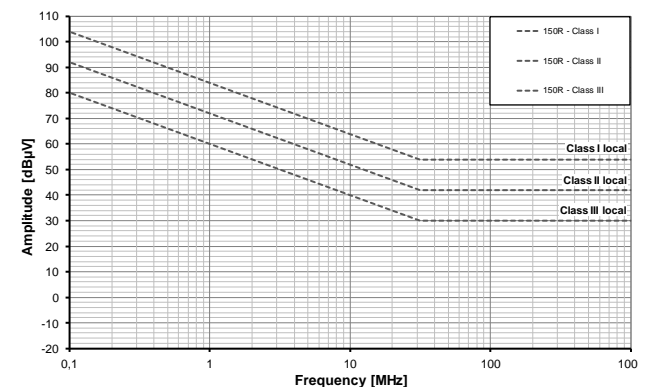
**Figure 24** “LIN without bus filter”  
Applicable for LIN-BUS



**Figure 25** “LIN device”  
Applicable for VS and Wake



**Figure 26** “150R global”  
Emission Limit for OUT



**Figure 27** “150R local”  
Emission Limit for OUT



## Test Result

### RF-VS

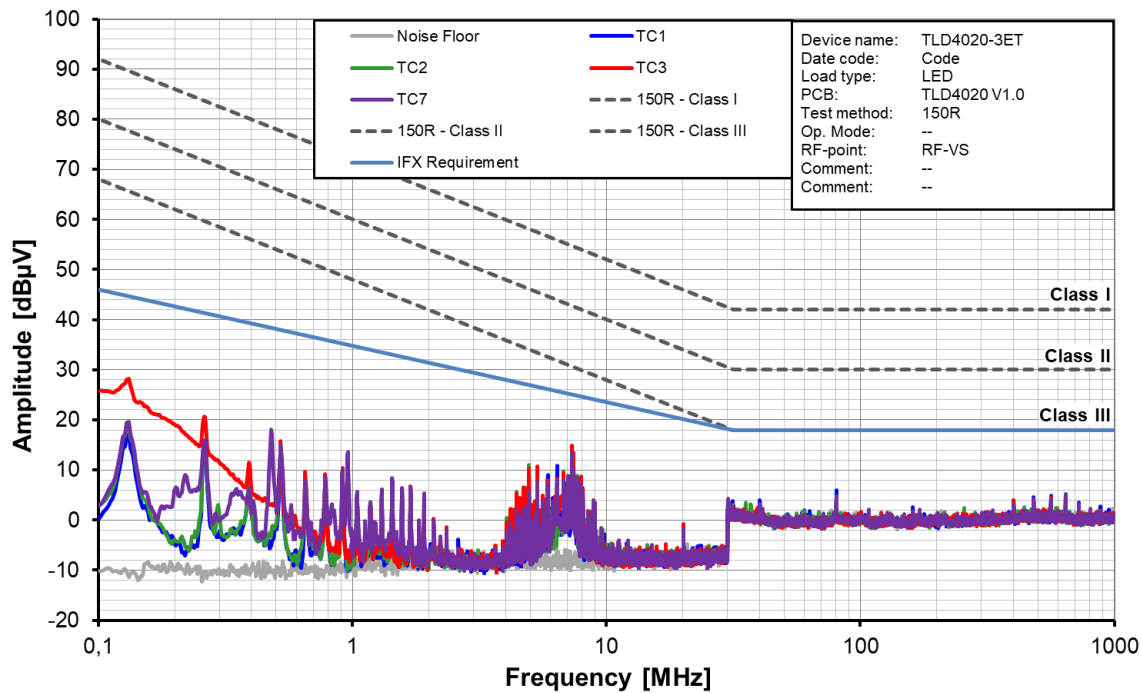


Figure 28 Conducted Emission 150R method RF-VS

### RF-OUT0

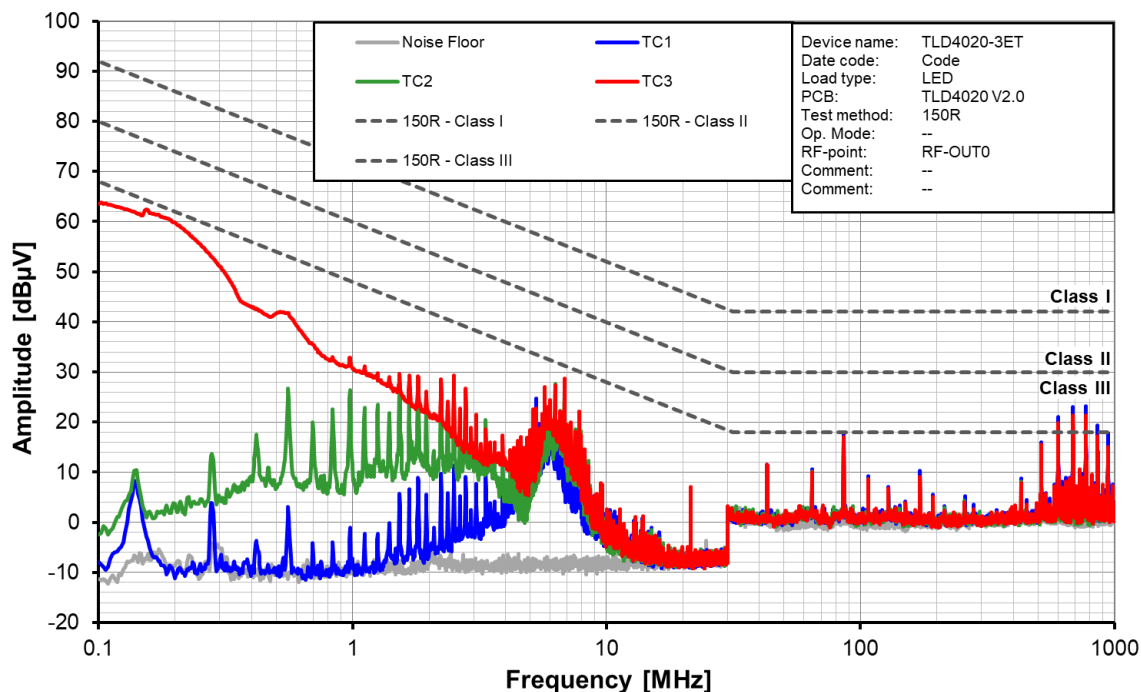


Figure 29 Conducted Emission 150R method RF-OUT0

## RF-OUT1

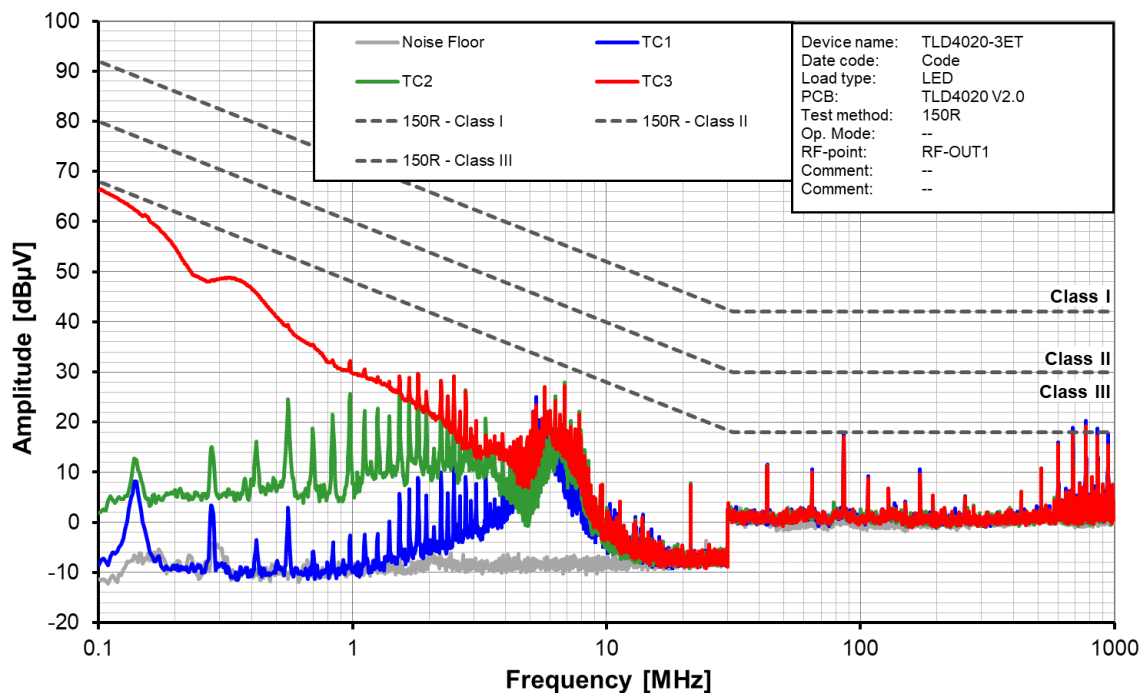


Figure 30 Conducted Emission 150R method RF-OUT1

## RF-OUT2

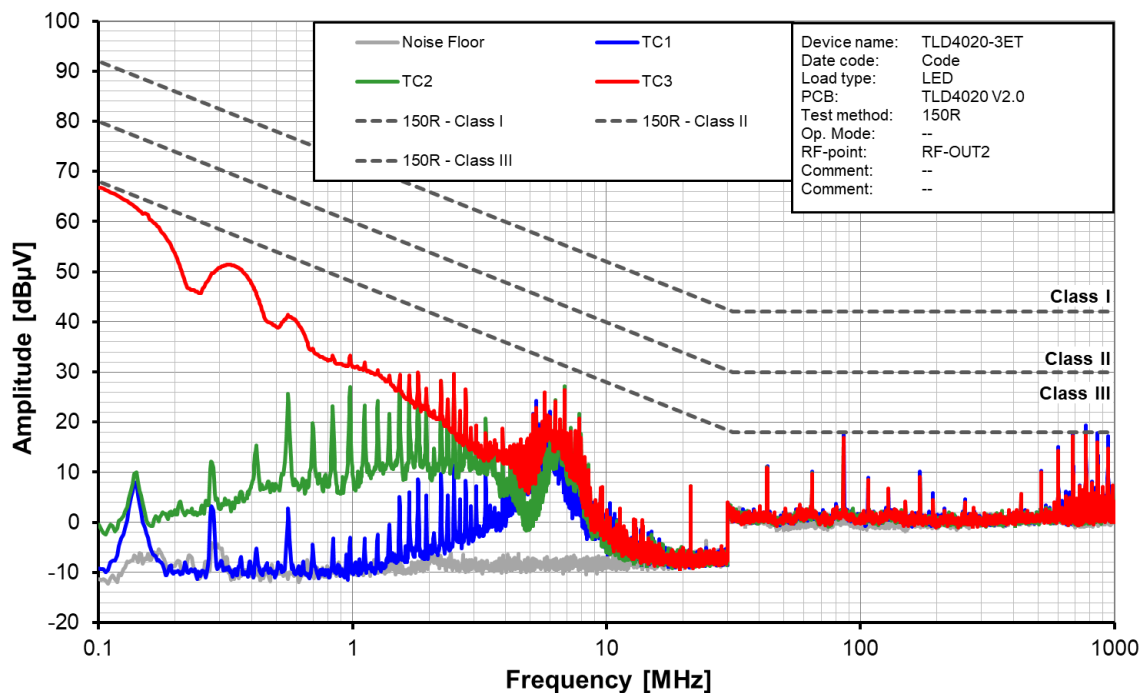


Figure 31 Conducted Emission 150R method RF-OUT2

## RF-LIN

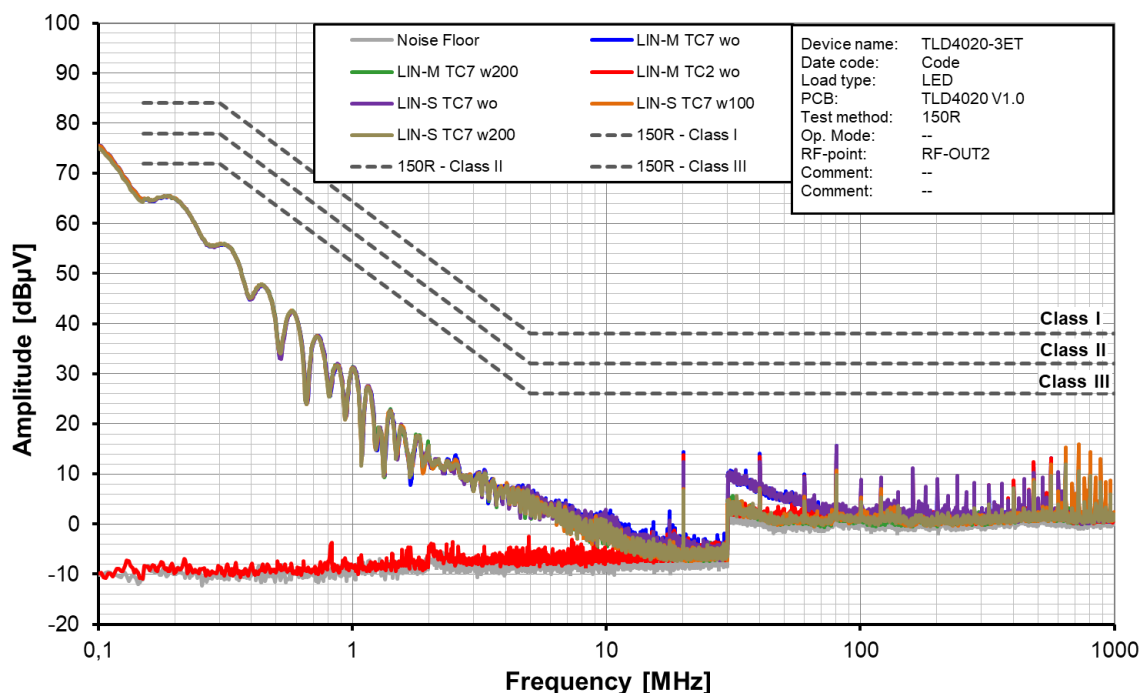


Figure 32 Conducted Emission 150R method RF-LIN. LIN without Bus Filter

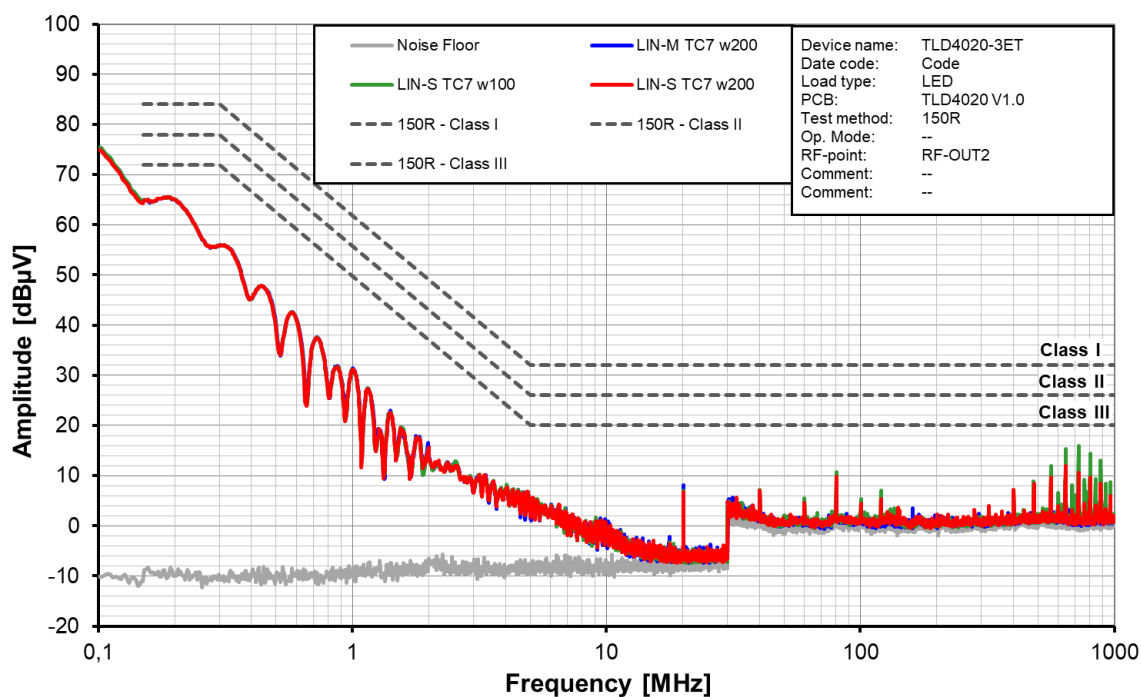


Figure 33 Conducted Emission 150R method RF-LIN. LIN with Bus Filter

## 5 Conducted Emission - LISN method

“Conducted Emission – LISN method “examines conducted emissions [according to](#) Table 1

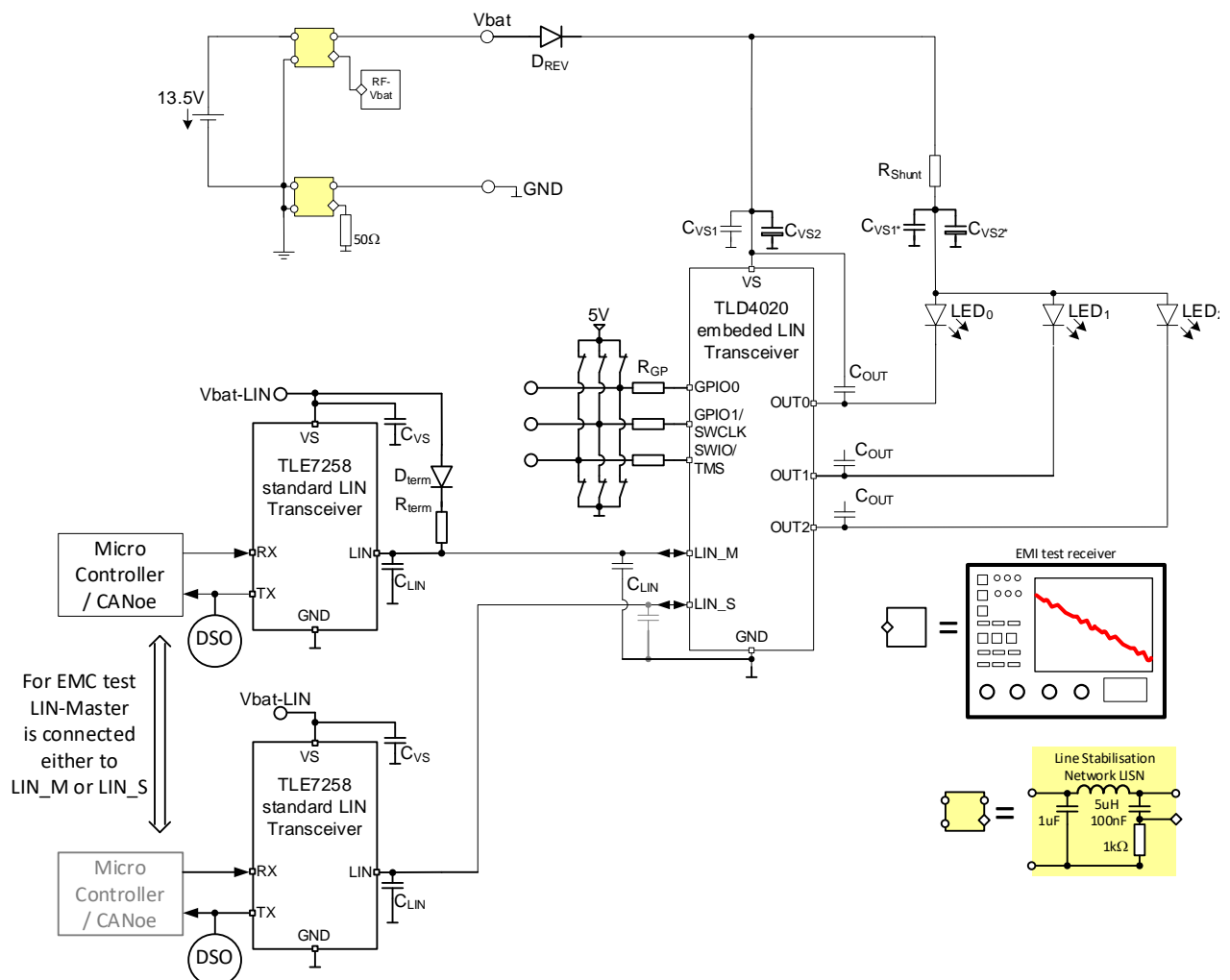
## Hardware Test Setup

**Table 19** Frequency range and settings for the EMI test receiver

Frequency range			Receiver			
			RBW	step size	Meas. time	Detector
150 kHz	to	30 MHz	9 kHz	5 kHz	>= 10 ms	Max. Peak & Average
30 MHz	to	108 MHz	120 kHz	50 kHz	>= 10 ms	

## Test-/ Simulation Setup for Conducted Emission

Conducted Emission test setup for the Line Impedance Stabilization Network (LISN) method.



**Figure 34** Conducted emission test/simulation setup for the Battery Line.

## Emission Levels Classification

Emission Levels Class-I to Class-V for peak and average detector.

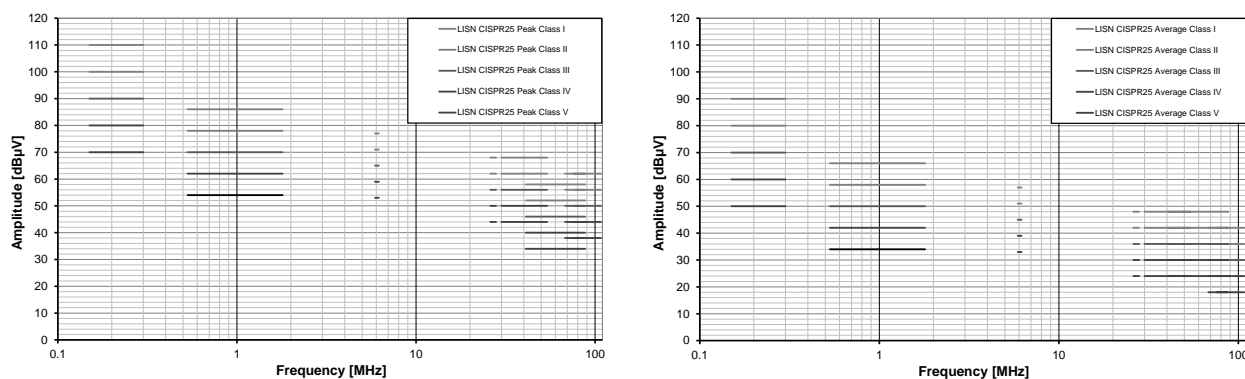


Figure 35 Emission level characterization for peak and average detector.

## Requirements for Conducted Emission (LISN)

Table 20 show the requirements for the conducted emission test.

Table 20 Conducted emission requirements, [Pin selection regarding](#) Table 5

Pin	Bus Filter	Required Target Value for	
		<a href="#">Operation Mode</a>	requirement
Vbat	X	TC1, TC2, TC3, TC7	< Class V peak & average

## Test Result

### Emission on Vbat

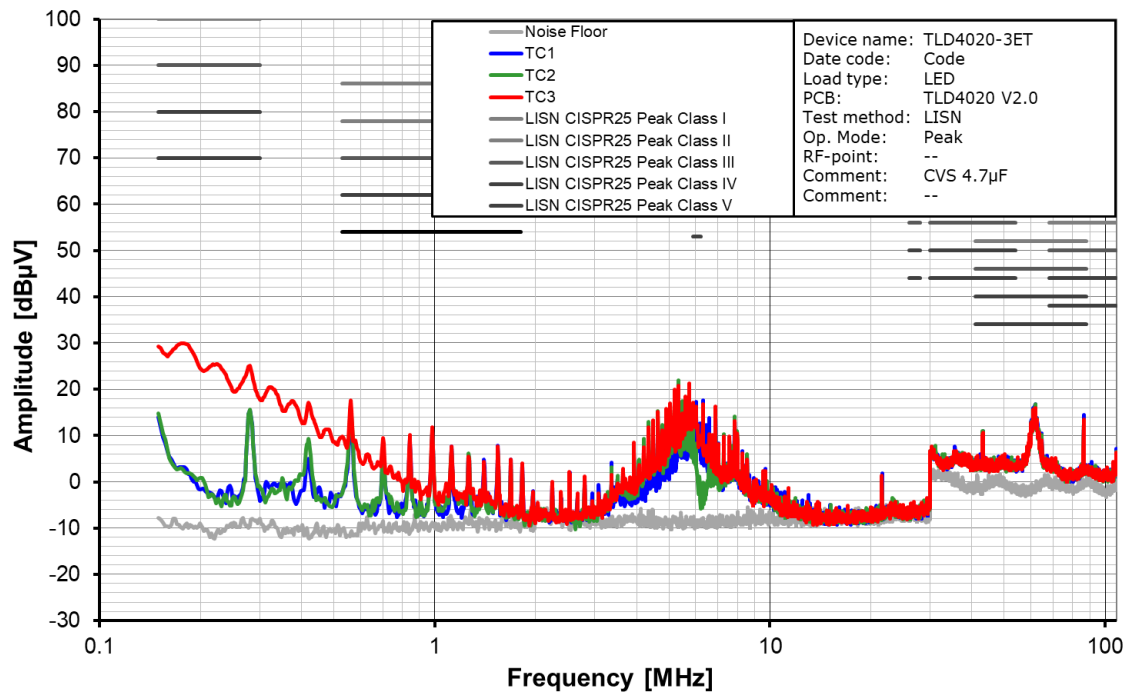


Figure 36 RF peak emissions on the Battery Line.

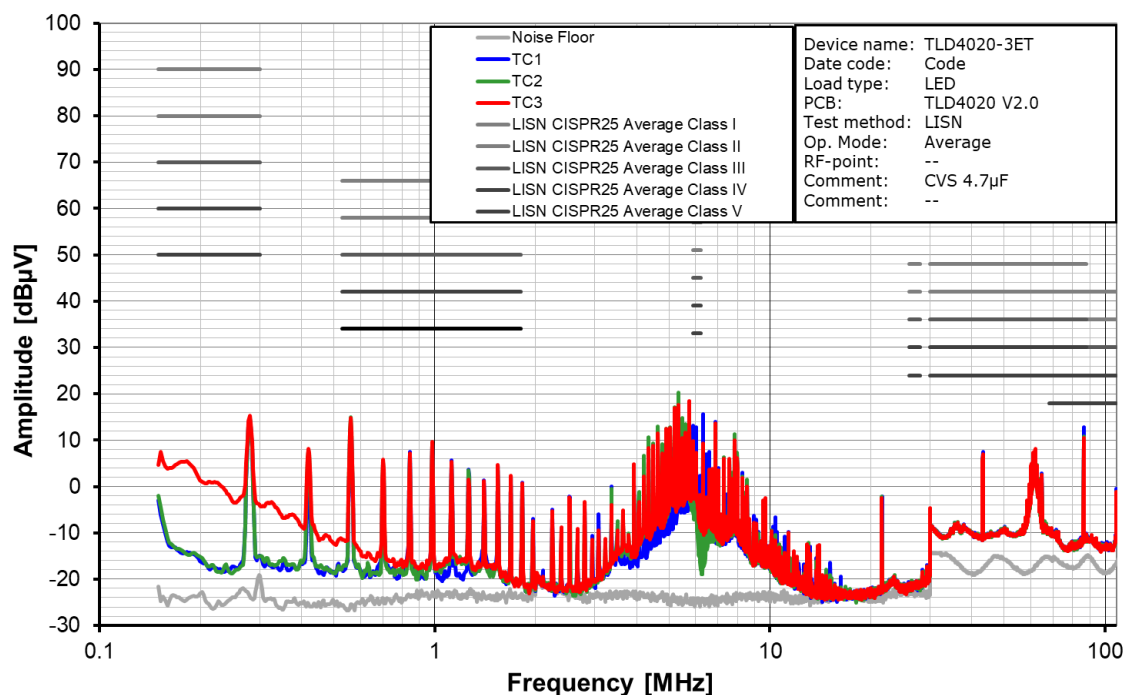


Figure 37 RF average emissions on the Battery Line.

## 6 Radiated Emission (RE)- ALSE method

“Radiated Emission – Antenna methode“ examines radiated emissions [according to](#) Table 1

### Hardware test setup

**Table 21** Frequency range and settings for the EMI test receiver

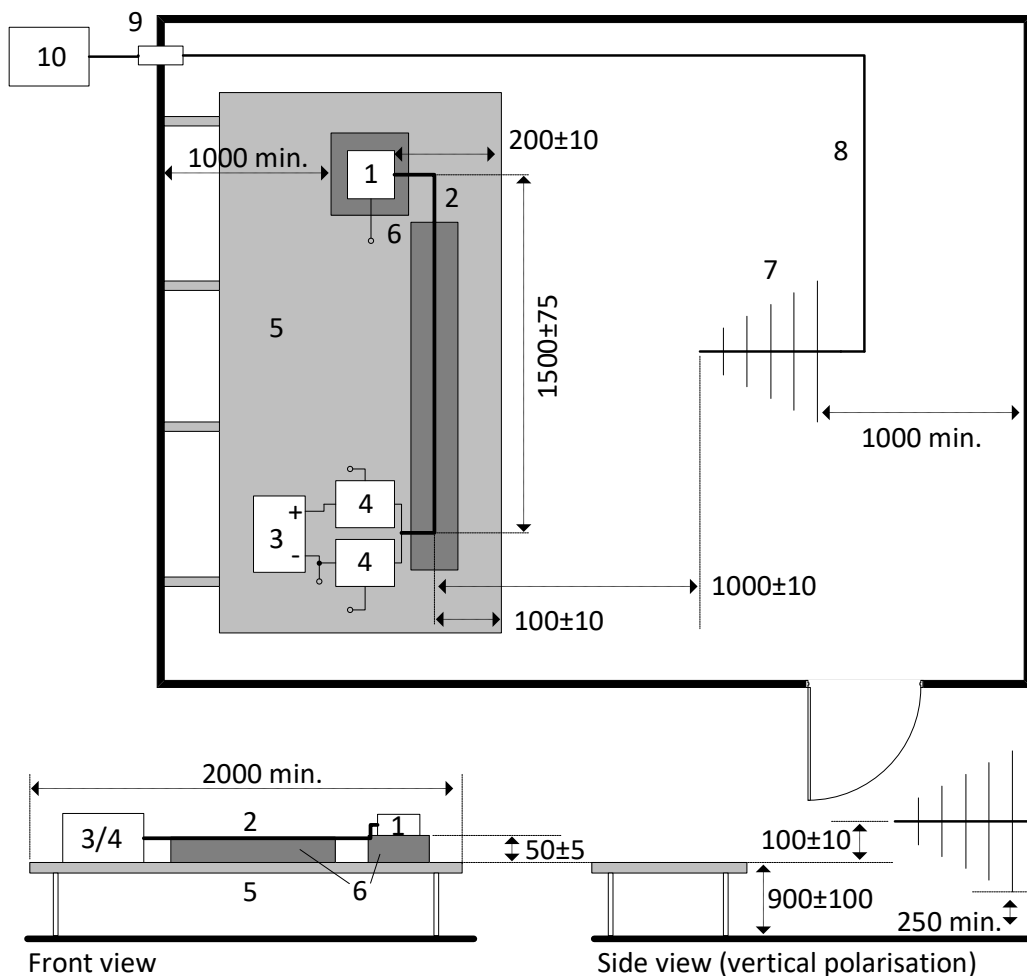
Frequency range	Receiver setting for radiated emission - ALSE				
	Antenna	RBW	Step size	Meas time	detector
150 kHz to 30 MHz	Rod	9 kHz	5 kHz	$\geq 5\text{ms}$	peak, average
30 MHz to 200 MHz	Biconical	120 kHz	50 kHz	$\geq 5\text{ms}$	peak, average
200 MHz to 1000 MHz	Log-Periodic	120 kHz	50 kHz	$\geq 5\text{ms}$	peak, average

### General Test-Setup for Radiated Emission

The RE test setup as shown in the net picture, Antenna type and polarization needs to be adapted.

Top view (horizontal polarisation)

Dimensions in millimeters – not to scale



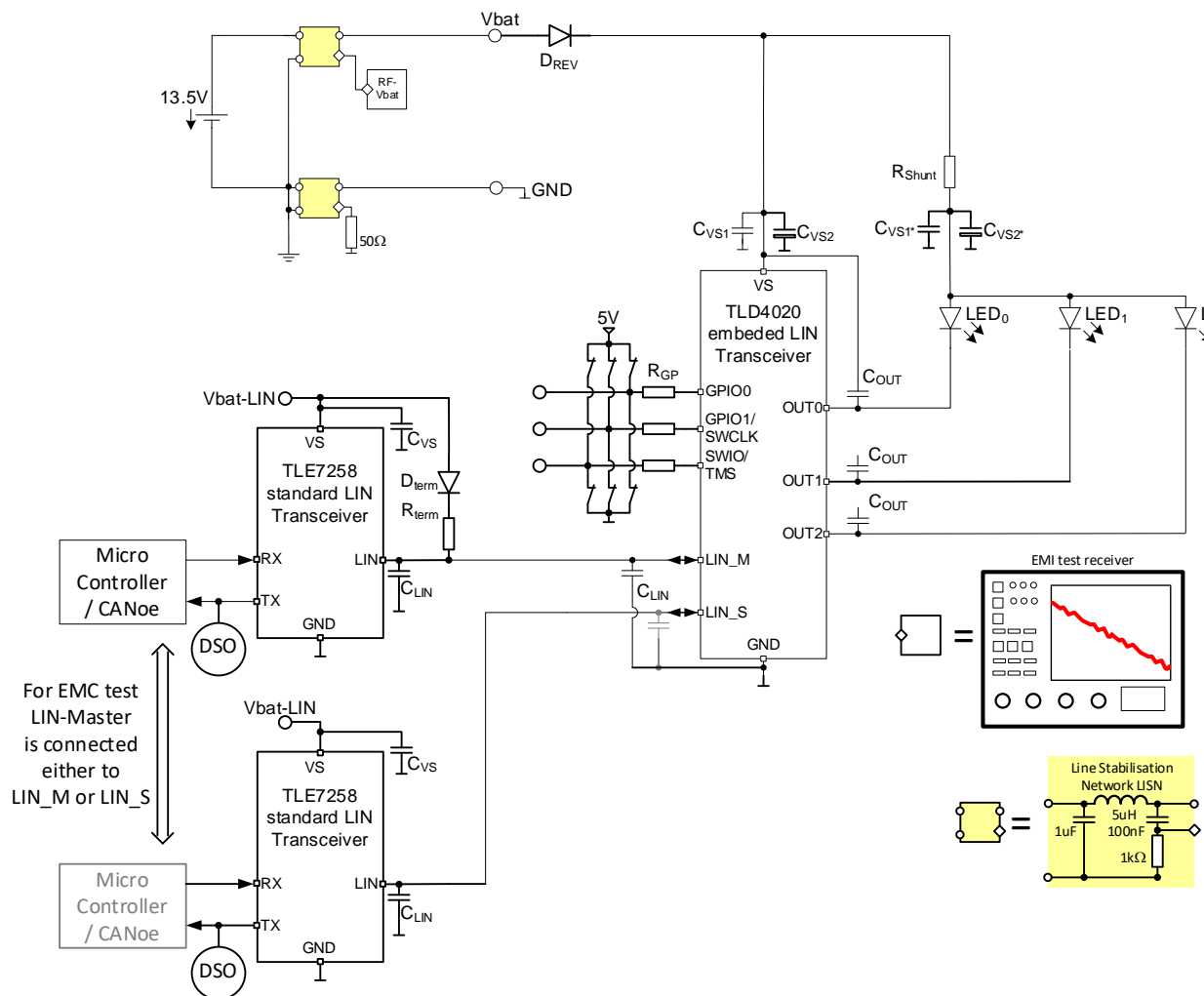
Key:

- |   |  |
|---|--|
| 1 EUT (grounded locally if required in test plan) | 6 Low relative permittivity support ( $\epsilon_r < 1.4$ )       |
| 2 Test harness                                    | 7 Log-periodic antenna   |
| 3 Power supply (location optional)                | 8 High-quality coaxial cable e.g. double-shielded (50 $\Omega$ ) |
| 4 Artificial network (AN)                         | 9 Bulkhead connector   |
| 5 Ground plane (bonded to shielded enclosure)     | 10 Measuring instrument  |

**Figure 38** General Test Setup Radiated Emission ALSE method.

## Hardware Test-Setup for Radiated Emission

The RE test setup is the same as for the CE



**Figure 39** Radiated Emission test/simulation setup according to CISPR-25 ALSE.

## Requirements for Radiated Emission (ALSE)

Table 22 show the requirements for the conducted emission test.

**Table 22** Radiated emission requirements.

Pin	Input Pi-Filter	Input Common Mode Choke	Load	Required Target Value for <u>Operation Mode</u>	
				ON	Spread Spectrum
VBAT	No	No	Load1	< Class-V for peak & average	



## Test Result

### Emission on Vbat

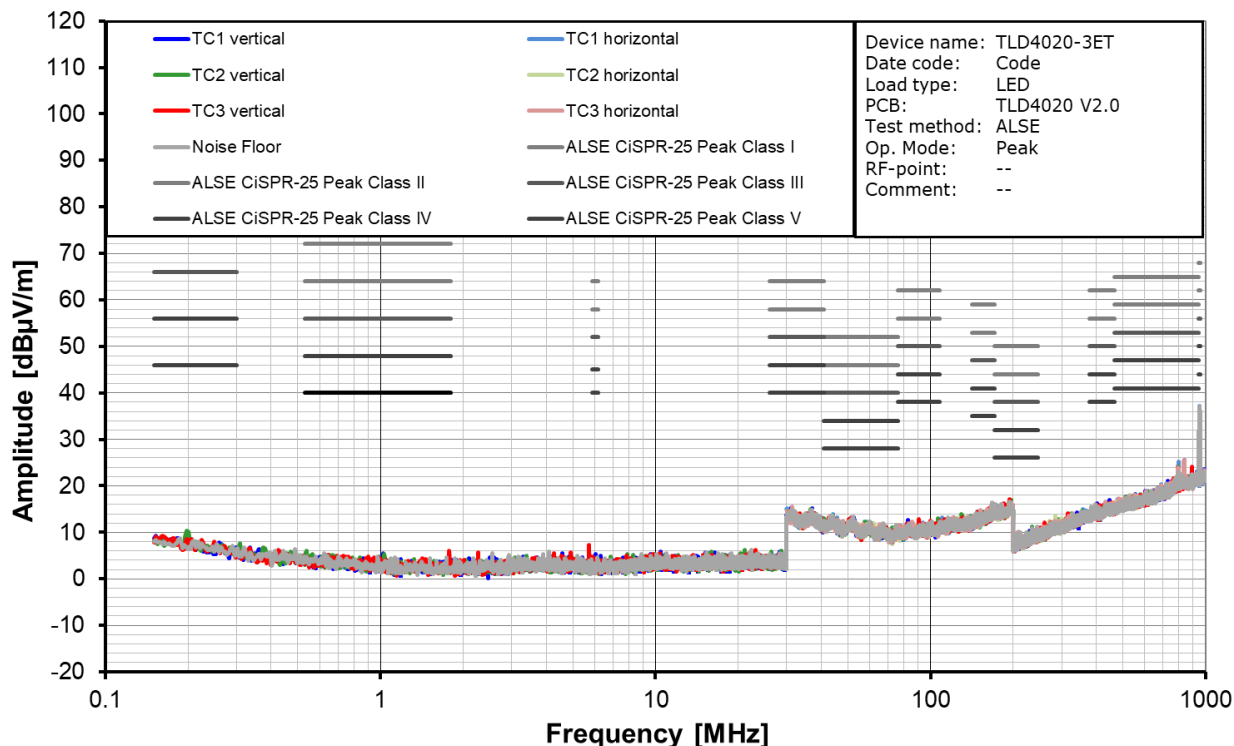


Figure 40 Radiated peak emissions on battery line.

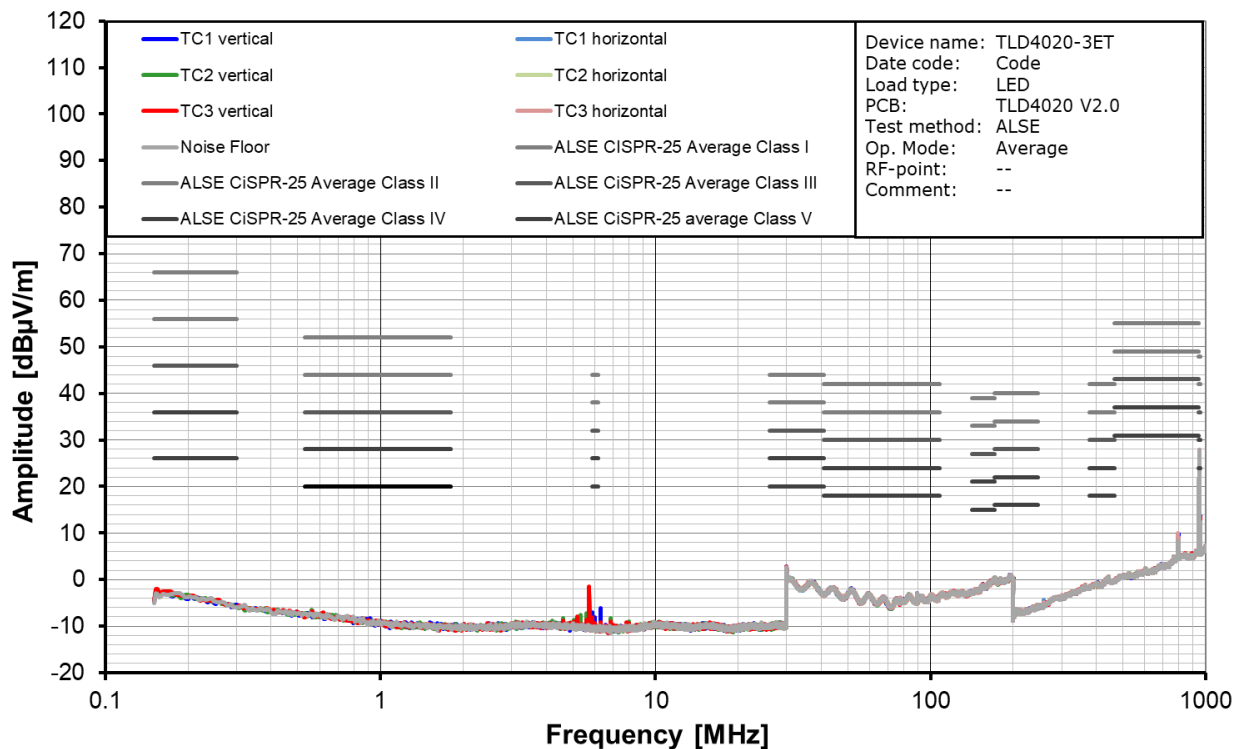


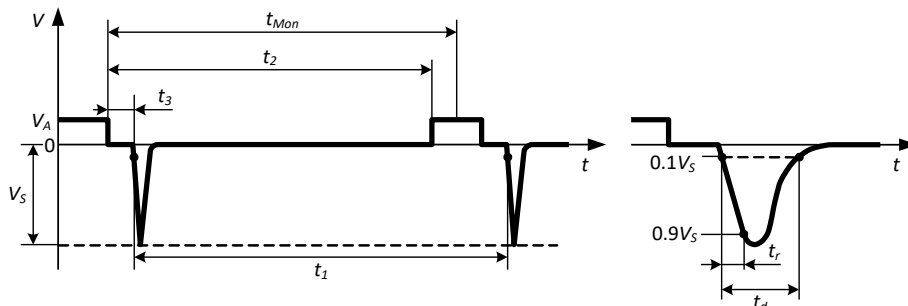
Figure 41 Radiated average emissions on battery line.

## Appendix

### Test Pulse Definition for the 12V System<sup>12</sup>

**Table 23** Test Pulse 1

$V_A$	13.5V
$V_{Smax}$	-75V to -150V
$R_i$	10 $\Omega$
$t_d$	2ms
$t_r$	1 $\mu$ s (+0 $\mu$ s, -0.5 $\mu$ s)
$t_1$	$\geq 0.5$ s
$t_2$	As short as possible
$t_3$	<100 $\mu$ s
# of pulses	5000
$t_{Mon}$	Time between 2 pulses
Standard	ISO7637-2: 2010

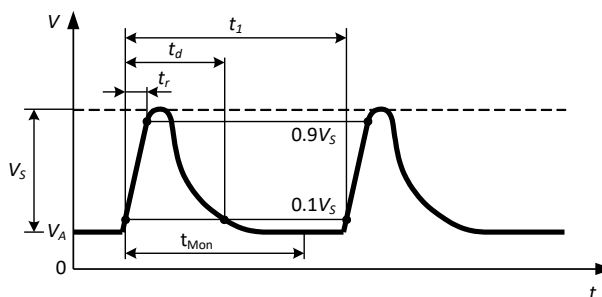


[back to requirement](#)

Test Pulse1 simulates the turn-of for inductive loads parallel to the DUT. Battery voltage is turned-off for 200ms.

**Table 24** Test Pulse 2a

$V_A$	13.5V
$V_{Smax}$	+37V to +112V
$R_i$	2 $\Omega$
$t_d$	50 $\mu$ s
$t_r$	1 $\mu$ s (+0 $\mu$ s, -0.5 $\mu$ s)
$t_1$	0.2s to 5s
# of pulses	5000
$t_{Mon}$	Time between 2 pulses
Standard	ISO7637-2: 2010



[back to requirement](#)

Test Pulse 2a simulates transients due to sudden interruption of currents in a device connected in parallel with the DUT generated in the inductance of the wiring harness.

<sup>1</sup> The peak voltage  $V_S$  shall be adjusted to the test levels with a tolerance of +10%, -0%.

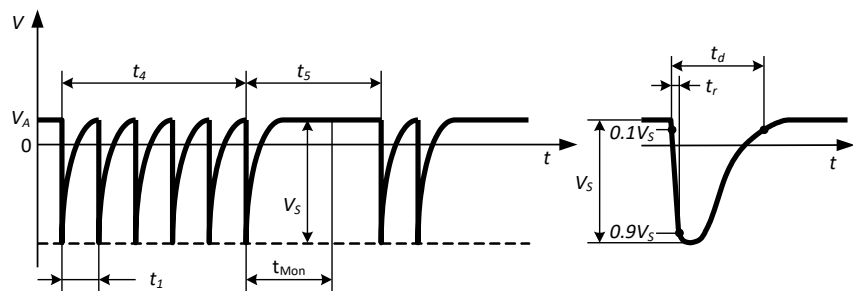
The timing tolerances and internal resistance  $R_i$  tolerance shall be  $\pm 20\%$ , unless otherwise specified.

<sup>2</sup> The pulse voltage- amplitude and waveform are specified for the idle pulse.

Table 25 Pulse 3a

[back to requirement](#)

$V_A$	13.5V
$V_{Smax}$	-112V to -220V
$R_i$	<b>50Ω</b>
$t_d$	150ns $\pm$ 45ns
$t_r$	5ns $\pm$ 1.5ns
$t_1$	100μs
$t_4$	10ms
$t_5$	90ms
test time	1h
$t_{Mon}$	between burst package
Standard	ISO7637-2: 2010

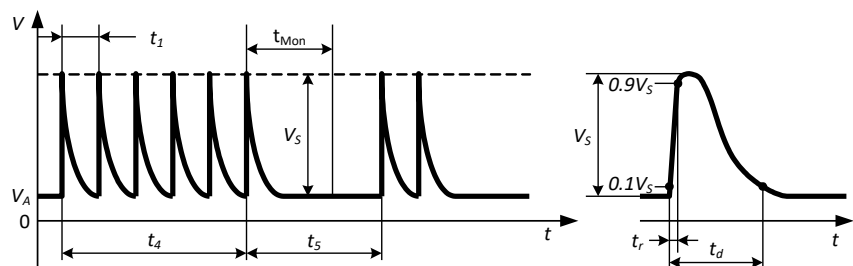


Test Pulse 3a simulates a switching process.

**Table 26** Pulse 3b

[back to requirement](#)

$V_A$	13.5V
$V_{Smax}$	+75V to +150V
$R_i$	<b>50Ω</b>
$t_d$	150ns ± 45ns
$t_r$	5ns ± 1.5ns
$t_i$	100μs
$t_4$	10ms
$t_5$	90ms
test time	1h
$t_{Mon}$	between burst package
Standard	ISO7637-2: 2010

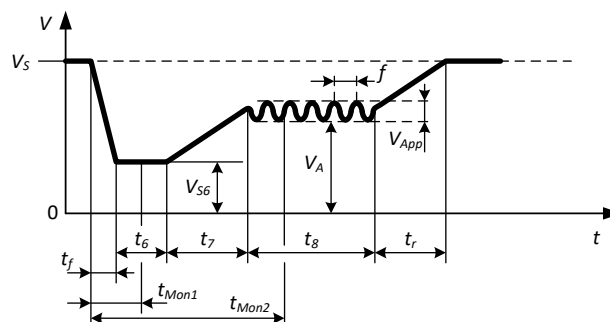


Test Pulse 3b simulates a switching process.

**Table 27** Pulse Starting Profile

[back to requirement](#)

$V_S$	+12V
$V_{S6}$	<b>5.5V</b>
$V_A$	<b>7.5V</b>
$V_{APP}$	2.0V
$R_i$	0.01 $\Omega$
$t_i$	5ms
$t_6$	15ms
$t_7$	50ms
$t_8$	10s
$t_i$	100ms
$f$	20Hz
# of pulses	1
$t_{Mon1}$	during $t_6$
$t_{Mon2}$	during $t_8$
Standard	ISO 16750-2: 2010

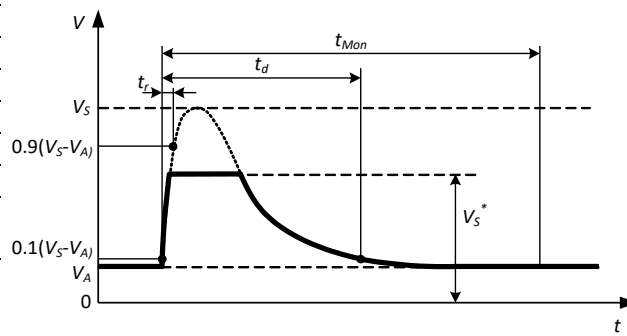


The starting Profile simulates the battery voltage during the ignition process

$V_{S6}$  and  $V_A$  depend on device requirement

**Table 28** Pulse Load Dump Suppression[back to requirement](#)

$V_A$	+13.5V
$V_{Smax}$	+79V to +101V
$V_S^*$	+35V
$R_i$	0.5Ω to 4Ω <b>2Ω</b>
$t_d$	40ms to 400ms
$t_r$	10ms(+0ms, -5ms)
# of pulses	10 pulses at intervals of 1 min
$t_{Mon}$	between burst package
Standard	ISO16750-2: 2010



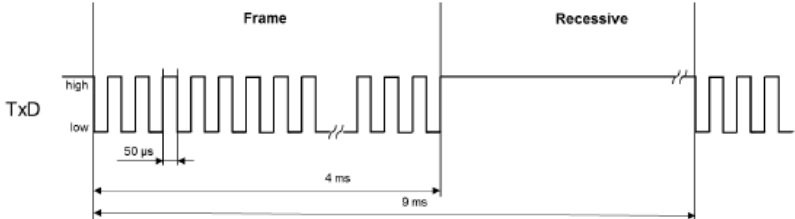
This pulse simulates the load dump pulse in case of suppressor diodes integrated into the generator.

$V_S^*$  depend on device requirement

## Definition for LIN Communication signals

**Table 29** LIN test pattern TX1

[return to Operation Modes](#)

Test Signal	LIN Communication test signal TX1
Signal Type	Standard test signal (periodic)
	 <p>source: IEC 62228-2</p>
Frequency	10kHz
Cycle time	9 ms
Frame length	4 ms
Amplitude	$V_{CC} \pm 0,1V$
Standard	IEC 62228-2 chapter 5.4

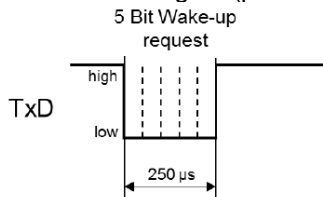
**Table 30** LIN test pattern TX2

[return to Operation Modes](#)

Test Signal	LIN Communication test signal TX2
Signal Type	LIN frame
Protocol	ISO 17987-6-2
Data bit rate	19,2 kB/s
PID and Data	Depending on designed or programmed functionality
Cycle time	9 ms(default)
Amplitude	$V_{CC} \pm 0,1V$
Standard	IEC 62228-2 chapter 5.4
TLD4020 GPIO-PWM	Insert LIN Pattern which will show PWM on GPIO

**Table 31** LIN Test Pattern TX3

[return to Operation Modes](#)

Test Signal	Wake up from sleep mode
Signal Type	Standard test signal (periodic)
	 <p>source: IEC 62228-2</p>
Amplitude	$V_{CC} \pm 0,1V$
Standard	IEC 62228-2 chapter 5.4

Note : TX3 is send only once during each wake request.  
 Apply RF, wait for 1second (dwell time) then send TX3 and evaluate respond.  
 TX3 is 250us low signal.

## EMC Testboard Schematic

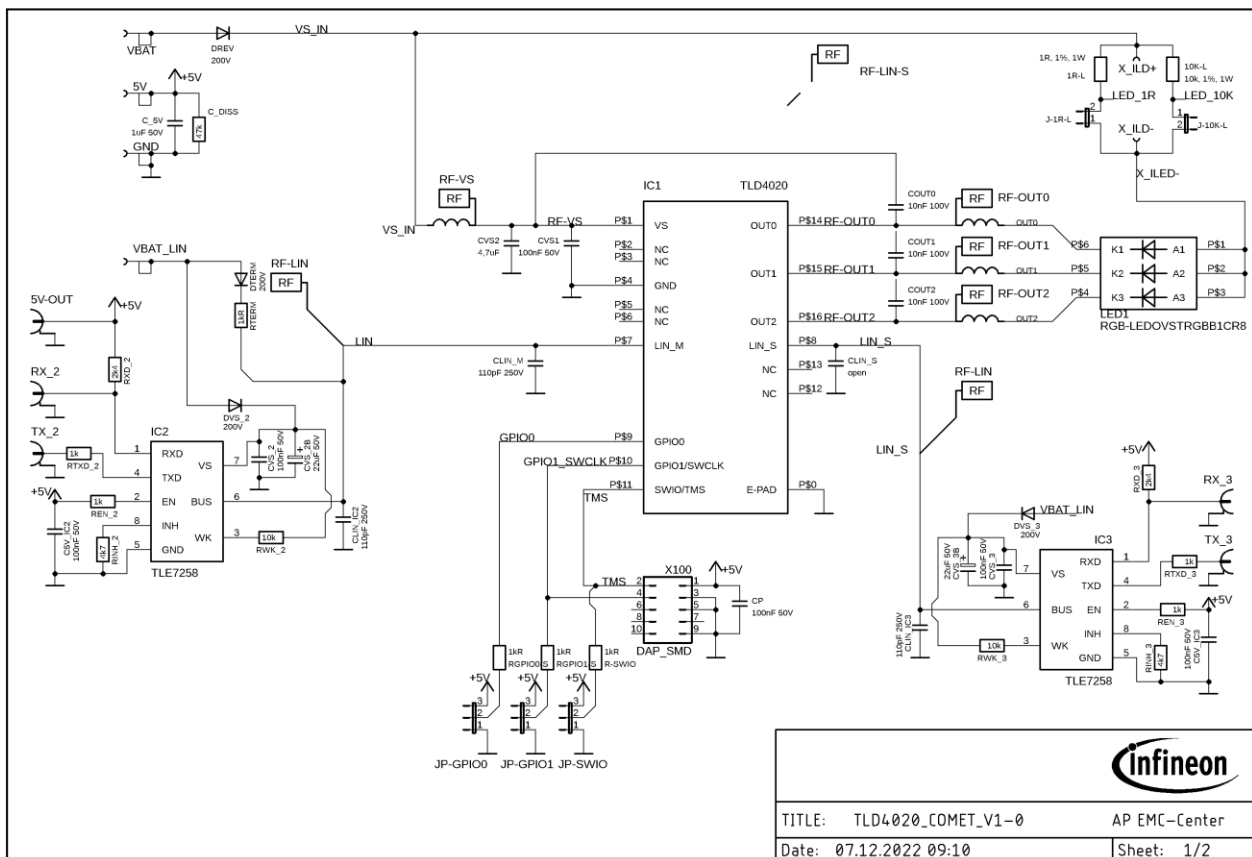


Figure 42 EMC Testboard Schematic Page 1 of 2

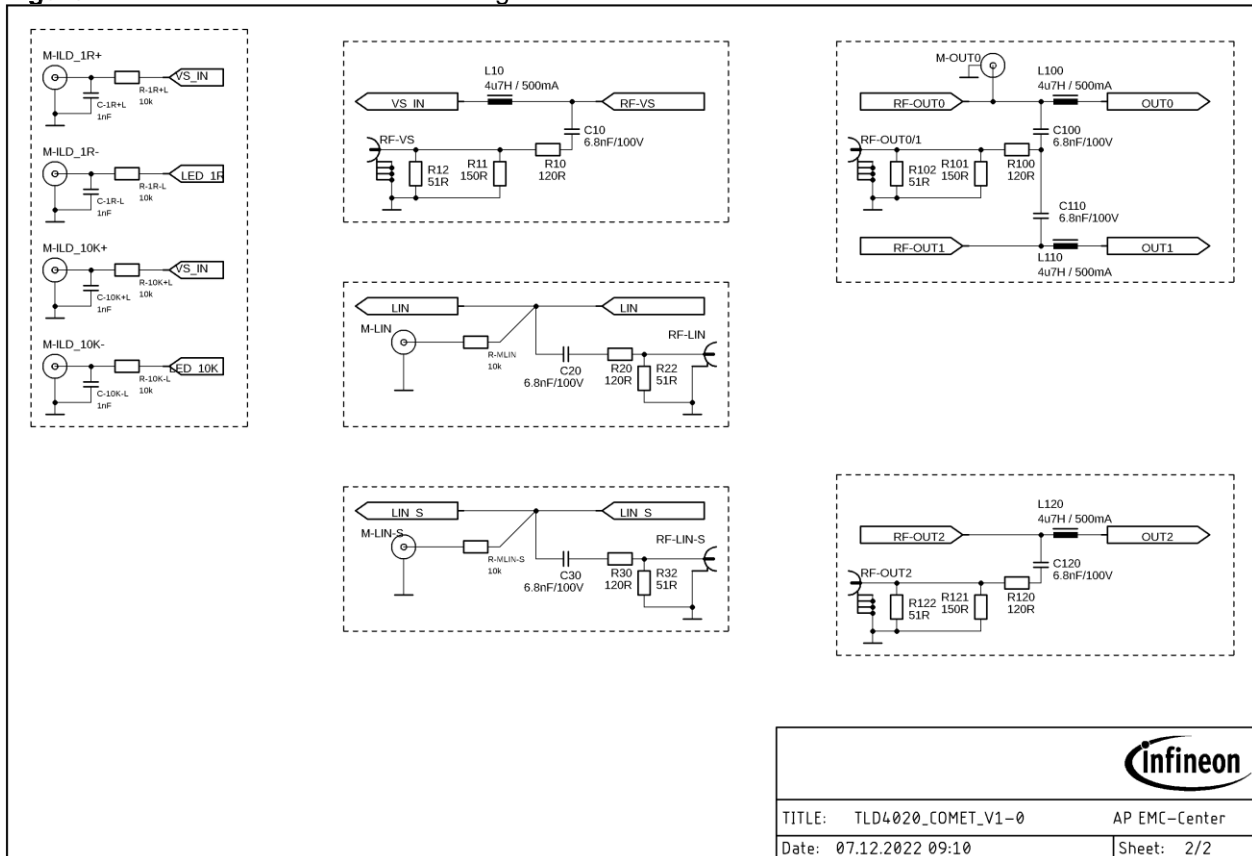
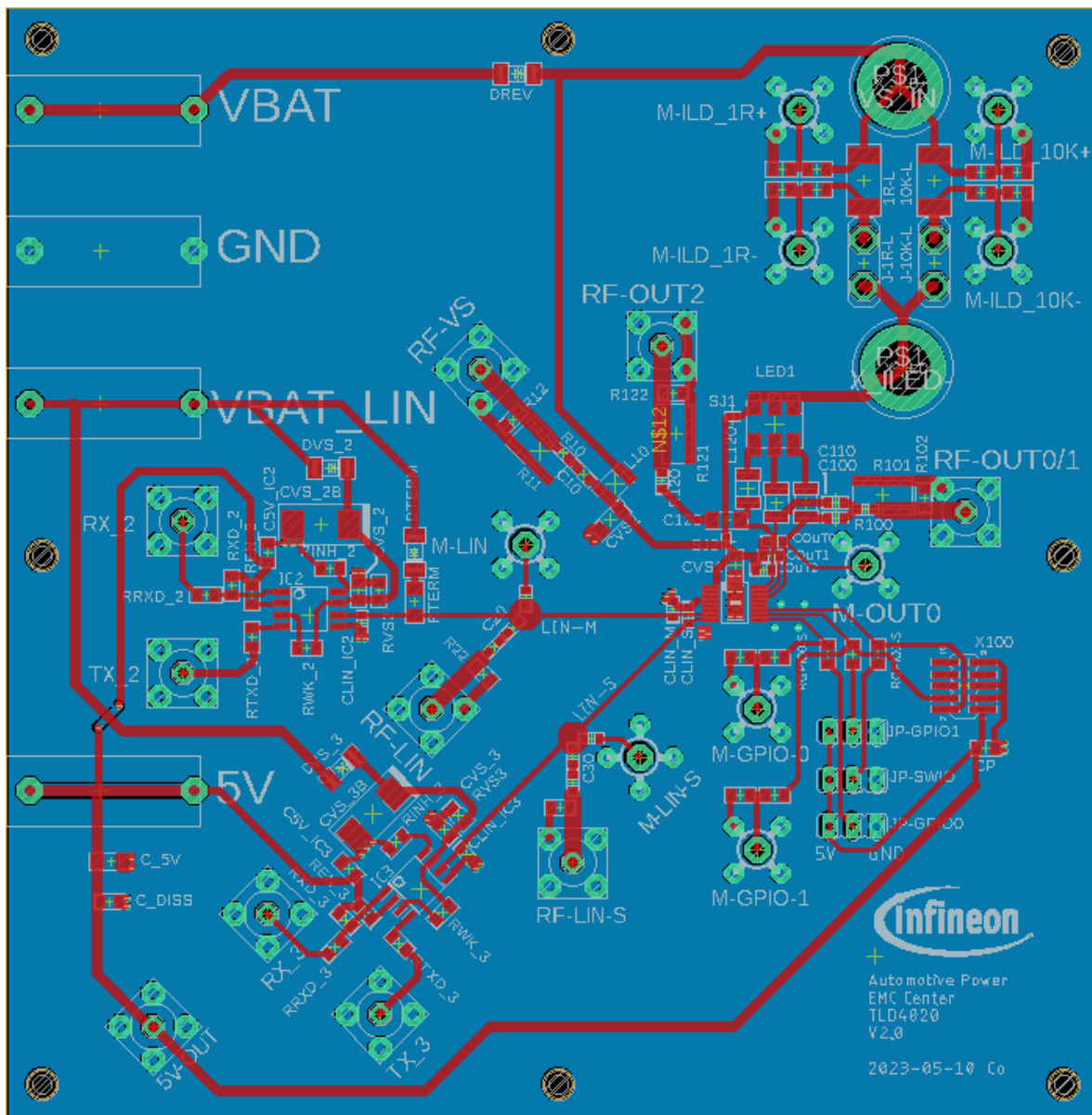


Figure 43 EMC Testboard Schematic Page 2 of 2

## EMC Testboard Layout



**Figure 44** EMC Testboard Top(red) and Bottom(blue) Layer

## RX-TX Adapter

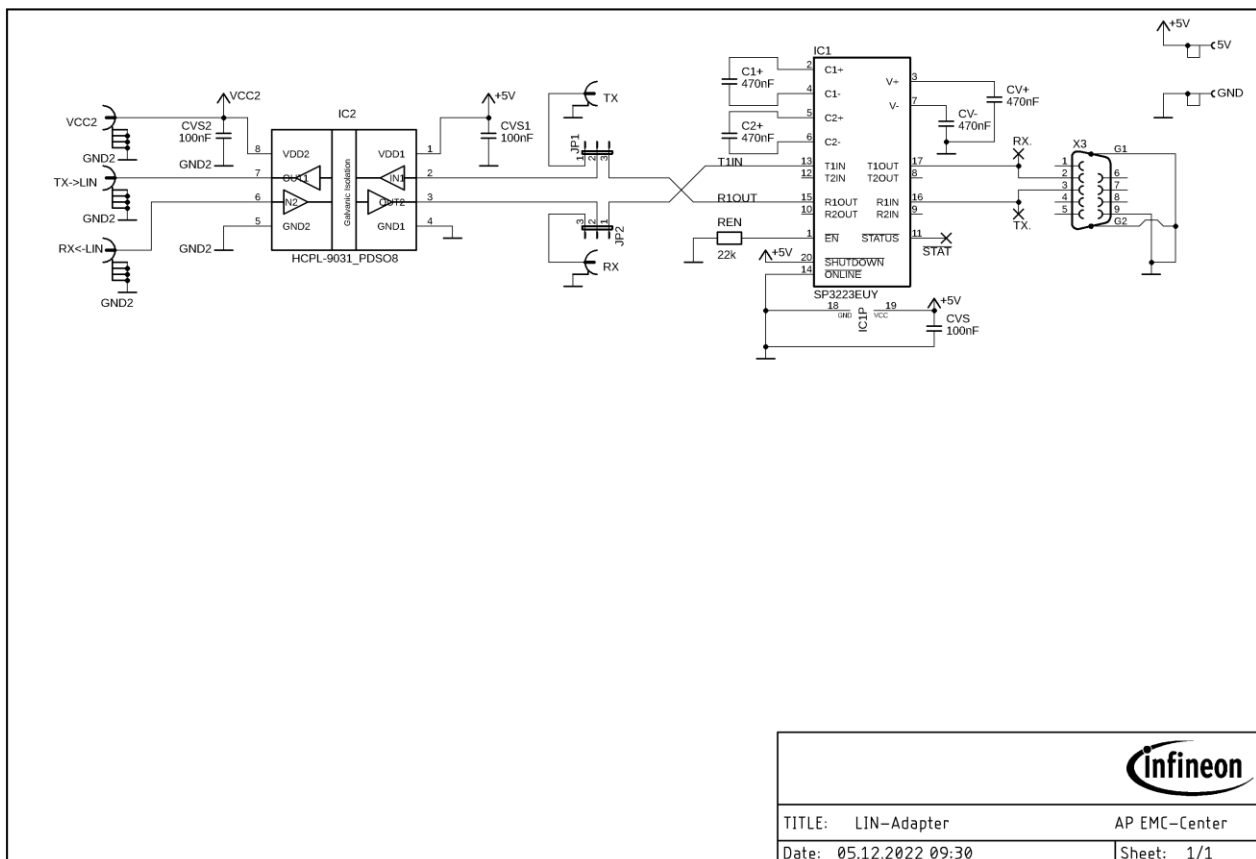


Figure 45 EMC RX-TX Coupler Page 1 of 1

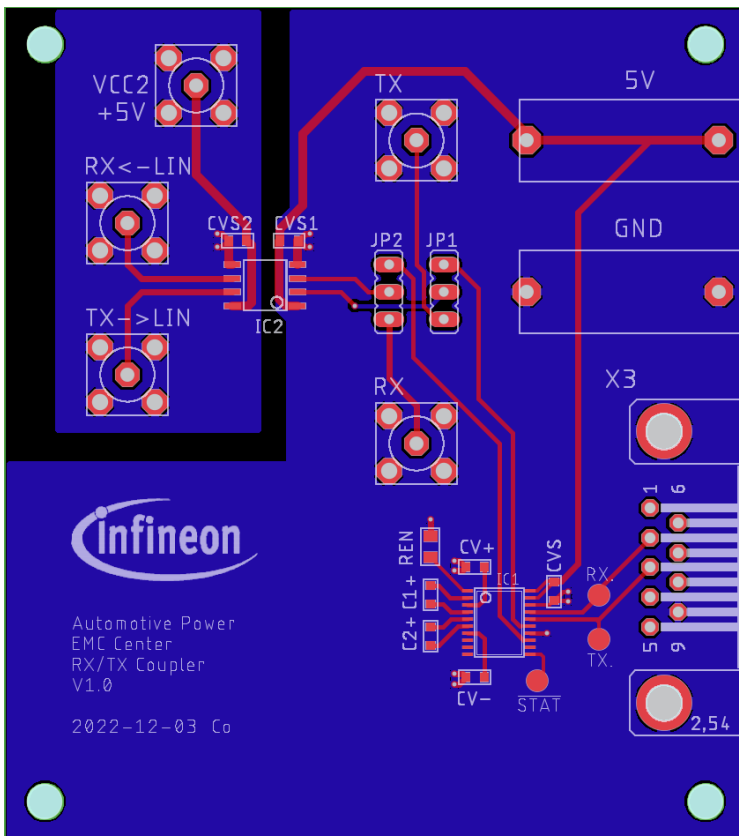


Figure 46 EMC RX-TX Coupler Top(red) and Bottom(blue) Layer



## Revision History:

Revision	Date	Description of change
1.3	2023-06	EMC test results on 1 <sup>st</sup> silicon
1.4	2023-08	DPI Out local results added

#### Trademarks

All referenced product or service names and trademarks are the property of their respective owners.

**Published by**  
**Infineon Technologies AG**  
**81726 Munich, Germany**

**© 2023 Infineon Technologies AG.**  
**All Rights Reserved.**

**Do you have a question about this document?**

**Email:** [erratum@infineon.com](mailto:erratum@infineon.com)

**Document reference**  
**EMC Test Report**

#### IMPORTANT NOTICE

The information contained in this application note is given as a hint for the implementation of the product only and shall in no event be regarded as a description or warranty of a certain functionality, condition or quality of the product. Before implementation of the product, the recipient of this application note must verify any function and other technical information given herein in the real application. Infineon Technologies hereby disclaims any and all warranties and liabilities of any kind (including without limitation warranties of non-infringement of intellectual property rights of any third party) with respect to any and all information given in this application note.

The data contained in this document is exclusively intended for technically trained staff. It is the responsibility of customer's technical departments to evaluate the suitability of the product for the intended application and the completeness of the product information given in this document with respect to such application.

For further information on the product technology, delivery terms and conditions and prices please contact your nearest Infineon Technologies office ([www.infineon.com](http://www.infineon.com)).

#### WARNINGS

Due to technical requirements products may contain dangerous substances. For information on the types in question please contact your nearest Infineon Technologies office.

Except as otherwise explicitly approved by Infineon Technologies in a written document signed by authorized representatives of Infineon Technologies, Infineon Technologies' products may not be used in any applications where a failure of the product or any consequences of the use thereof can reasonably be expected to result in personal injury.