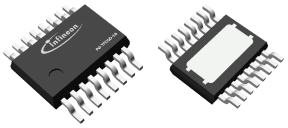
TLD4020-3ET

Target datasheet

LITIX™ Interior

Features



- 32-bit Arm® Cortex®-M23 core
  - One clock per machine cycle architecture
  - Single cycle multiplier
  - Hardware divider
- On-chip memory
  - 32 kB Flash (including 1000 TP memory)
  - 576 Bytes 1000TP memory
  - 3 kB SRAM
  - 16 kB Boot ROM for startup firmware and Flash routines
- On-chip oscillator and on-chip debug support via 2-wire SWD

AEC Qualified

RoHS

ISO 26262 compliant

Potential applications

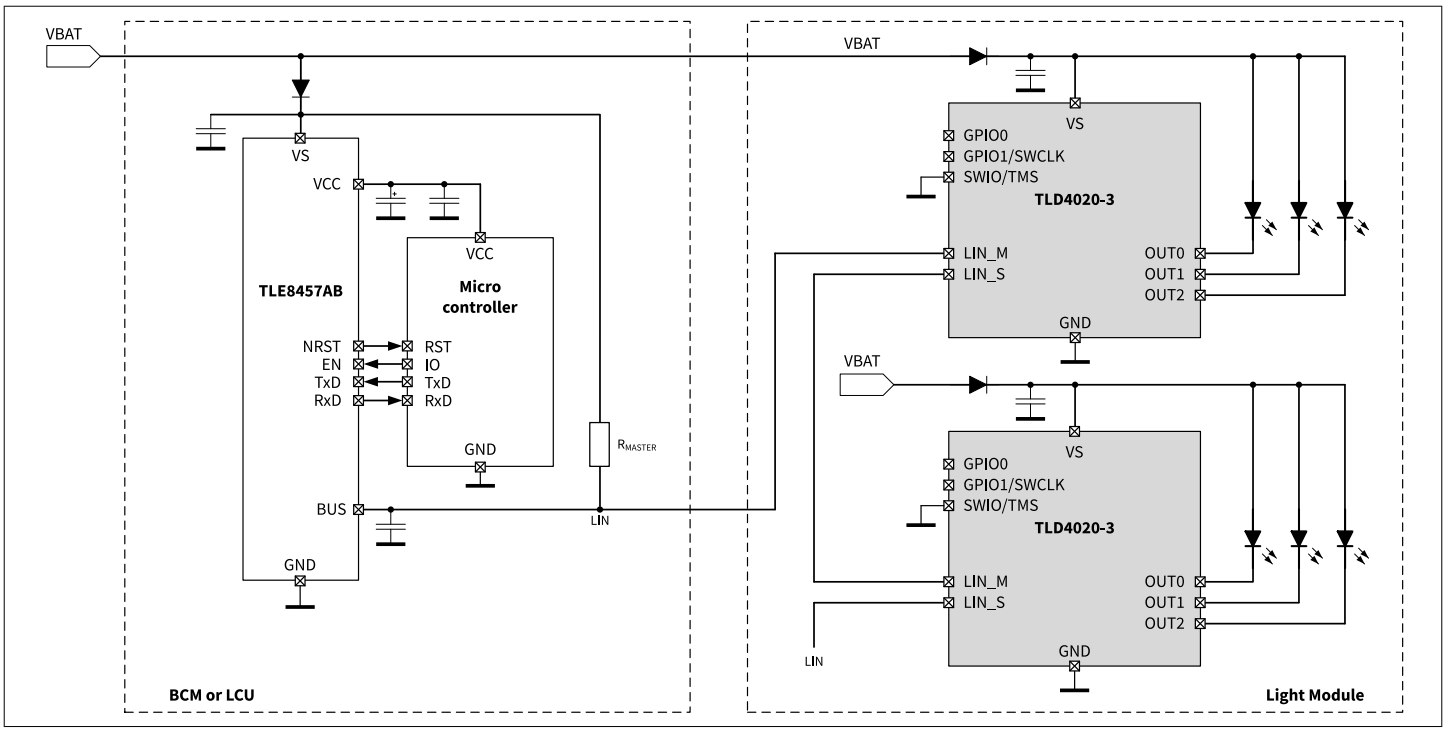
- Three channel LED driver for interior lighting with LIN interface
- Contour lighting using a single light source with constant or slowly changing light patterns
- Functional and switch illumination
- Surface lighting requiring single LED

Product validation

Qualified for automotive applications. Product validation according to AEC-Q100, Grade 1.

Description

The TLD4020-3ET is a 3 channel device with integrated and protected output stages. It is designed to control RGB LEDs with a current up to 50 mA as linear current sink (LCS). The power stages can be configured in parallel for higher load currents. Each individual power output stage is configurable via a 5-bit current set value. In total 3 independent and individual PWM configurations can be set. A LIN interface is used for programming (via bootloader), control and diagnostic feedback.



Product type	Package	Marking
TLD4020-3ET	PG-TFDSO-16	–

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1 Product description

1.1 Product summary

Table 1 Product summary

Parameter	Symbol	Values
Power supply operating voltage	$V_{S(OP)}$	5.5 V ... 29 V
Maximum output voltage	V_{OUT_max}	35 V
Nominal load current (Linear current sink)	I_{L_nom}	50 mA, V_s = 13.5 V
Output current accuracy T_J = 25°C	A_{IOUT_25}	±5%
Minimum dropout voltage	$V_{DR,all}$	1.2 V, I_{OUT} ≥ 90% of 50 mA

1.2 Additional features

- Optimized for electromagnetic compatibility (EMC)
- Optimized for low electromagnetic emission (EME)
- Optimized for high immunity against electromagnetic interference (EMI)
- Green product (RoHS compliant)
- Automotive temperature range of -40°C to 125°C
- One full duplex serial interface (UART), with LIN support
- One ISO 17987 series LIN transceiver
- LIN bootstrap loader to program the flash via LIN (LIN BSL)
- Three integrated low-side current sinks
- 11-bit differential A/D converter
- Integrated 10-bit digital temperature sensor (DTS)

2 Block diagram and terms

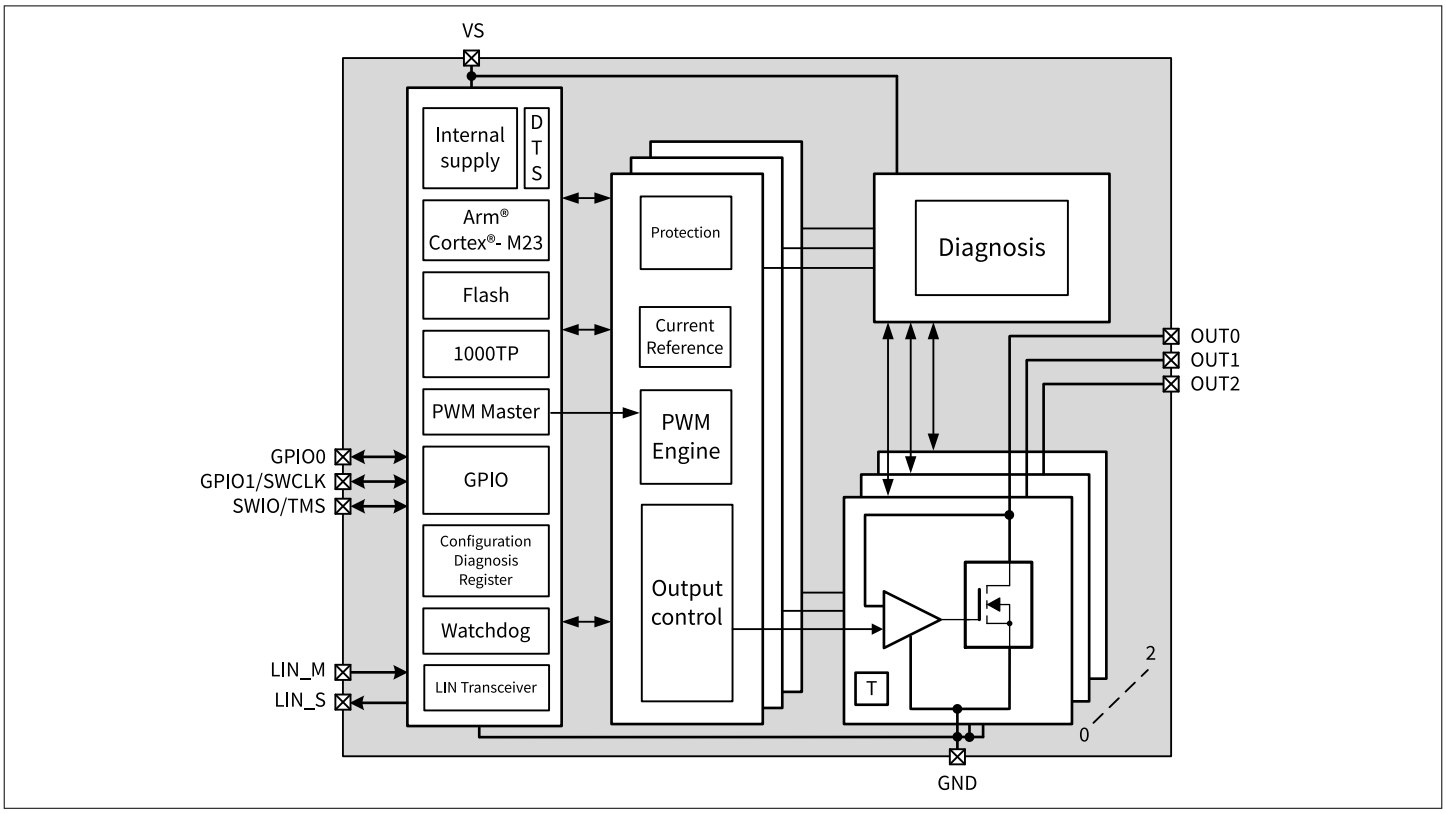

Figure 1 Block diagram of TLD4020-3ET

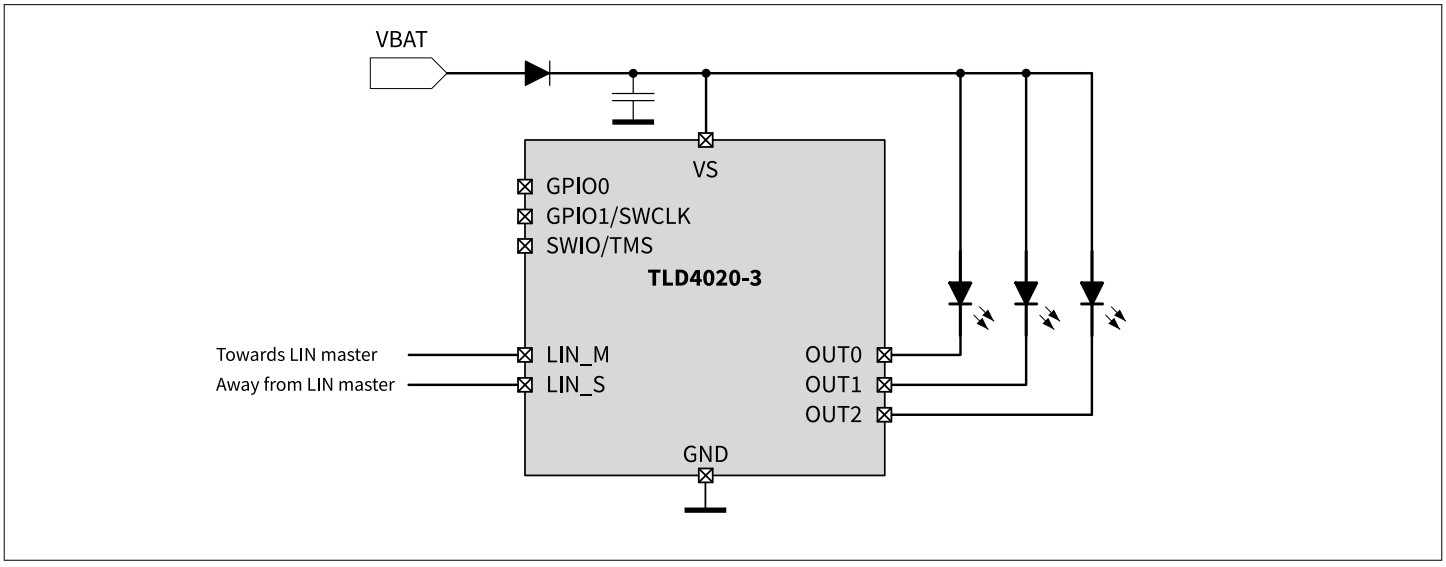

Figure 2 Application block diagram (simplified)

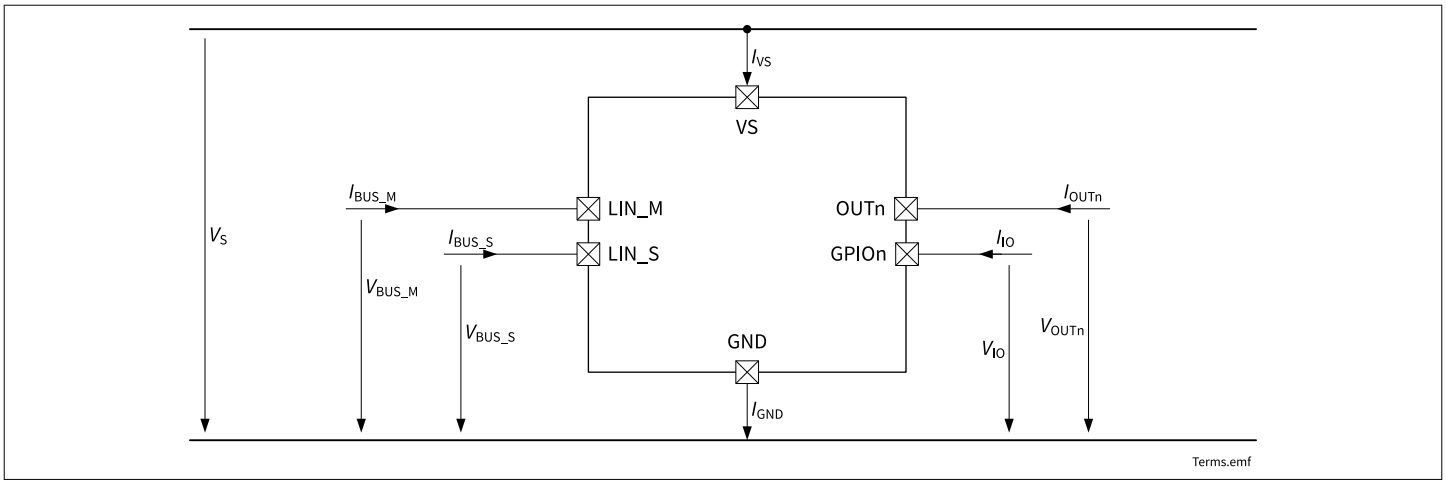

Figure 3 Terms and definitions

OUTn: n denotes the channel number from 0 to 2
GPIOn: n denotes the GPIO number from 0 to 1

3 Pin configuration

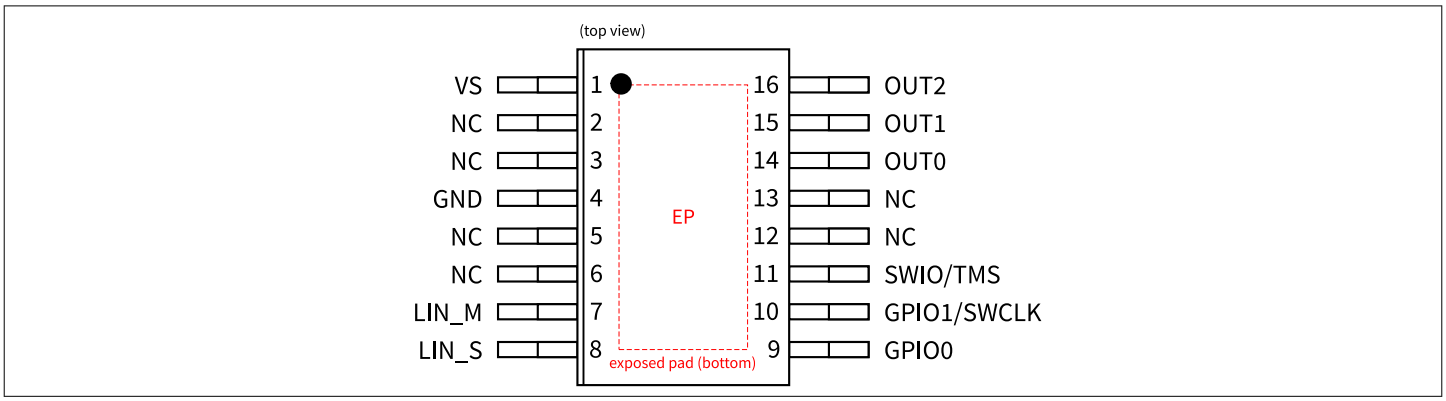

Figure 4 Pin configuration

Table 2 Pin definitions and functions

Pin	Symbol	Function
1	VS	**Power supply voltage** Battery supply input
2, 3	NC	Not connected
4	GND	**Ground** Ground potential. Connect externally close to the chip
5, 6	NC	Not connected
7	LIN_M	**LIN master** LIN connection towards direction of the master device
8	LIN_S	**LIN slave** LIN connection away from master device
9	GPIO0	**GPIO** Can be used for voltage measurements or as general-purpose input/output. Can be used as a wake-up source from sleep mode
10	GPIO1/SWCLK	**GPIO/SWD clock** Can be used for voltage measurements or as general-purpose input/output. Can be used as a wake-up source from sleep mode. Serial Wire Debug clock
11	SWIO/TMS	**SWD IO/TMS** Serial Wire Debug input/output Test mode select input
12...13	NC	Not connected
14...16	OUT0...OUT2	**Output channel** Open-drain linear current sink. Connect to the target load

(table continues...)

Table 2 (continued) Pin definitions and functions

Pin	Symbol	Function
–	EP	**Exposed pad** Connect to external heat spreading Cu area connected to electrical GND. Recommendation is to use the GND layer of a PCB with thermal vias. The exposed pad does not replace the electrical GND pin

4 General product characteristics

4.1 Absolute maximum ratings

Table 3 Absolute maximum ratings

T_J = -40°C to +150°C; all voltages with respect to ground, positive currents flowing as described in Chapter 2 (unless otherwise specified).

Parameter	Symbol	Values			Unit	Note or condition	P-Number
		Min.	Typ.	Max.			
Supply pins							
Power supply voltage	V_S	-0.3	–	29	V	–	PRQ-142
Power supply load dump voltage	$V_{S(LD)}$	–	–	35	V	Suppressed load dump acc. to ISO16750-2 (2010). R_i = 2 Ω	PRQ-143
Output pins							
Power output voltage	V_{OUT}	-0.3	–	35	V	–	PRQ-896
Power output current	I_{OUT}	0	–	56.65	mA	–	PRQ-495
GPIO pins							
Voltage at pin GPIO0, GPIO1	V_{IO}	-0.3	–	5.5	V	–	PRQ-898
Current at pin GPIO0, GPIO1	I_{IO}	0	–	2	mA	–	PRQ-497
LIN							
Voltage at pin LIN_M, LIN_S	V_{BUS}	-27	–	35	V	–	PRQ-1138
Temperatures							
Junction temperature	T_J	-40	–	150	°C	–	PRQ-144
Ambient temperature	T_A	-40	–	125	°C	–	PRQ-145
ESD susceptibility							
ESD susceptibility all pins (HBM)	$V_{ESD(HBM)}$	-2	–	2	kV	ESD susceptibility, Human Body Model "HBM" according to AEC Q100-002	PRQ-150
ESD susceptibility LIN vs GND (HBM)	$V_{ESD(HBM)}$	-8	–	8	kV	ESD susceptibility, Human Body Model "HBM" according to AEC Q100-002	PRQ-151
ESD susceptibility all pins (CDM)	$V_{ESD(CDM)}$	-500	–	500	V	ESD susceptibility, Charged Device Model "CDM" according to AEC Q100-011 Rev D	PRQ-152

(table continues...)

Table 3 (continued) Absolute maximum ratings

T_J = -40°C to +150°C; all voltages with respect to ground, positive currents flowing as described in Chapter 2 (unless otherwise specified).

Parameter	Symbol	Values			Unit	Note or condition	P-Number
		Min.	Typ.	Max.			
ESD susceptibility corner pins (CDM)	$V_{ESD(CDM)\_CR}$	-750	–	750	V	ESD susceptibility, Charged Device Model "CDM" according to AEC Q100-011 Rev D	PRQ-153

Note: *1. Stresses above the ones listed here may cause permanent damage to the device. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.*

2. Integrated protection functions are designed to prevent IC destruction under fault conditions described in the data sheet. Fault conditions are considered as "outside" normal operating range. Protection functions are not designed for continuous repetitive operation.

4.2 Functional range

Table 4 Functional range

T_J = -40°C to +150°C, all voltages with respect to ground, positive currents flowing as described in Chapter 2 (unless otherwise specified).

Parameter	Symbol	Values			Unit	Note or condition	P-Number
		Min.	Typ.	Max.			
Supply pins							
Supply voltage at VS	V_S	5.5	13.5	29	V	–	PRQ-162
Supply voltage for LIN transceiver	V_{S_LIN}	5.5	13.5	18	V	–	PRQ-967
VS capacitor range	C_{VS}	2	–	–	µF	X7R	PRQ-164
Temperatures							
Junction temperature	T_J	-40	–	150	°C	–	PRQ-529
Power stage pins							
Output voltage operating range	$V_{OUT(OP)}$	0	–	29	V	–	PRQ-897
Output current per channel	I_{OUT}	0	–	51.5	mA	–	PRQ-532
Output capacitor range	C_{OUT}	0	–	10	nF	–	PRQ-534
Output inductance range	L_{OUT}	0	–	0.5	µH	C_{OUT} < 10 nF	PRQ-536

4.3 Thermal resistance

Table 5 Thermal resistance

Parameter	Symbol	Values			Unit	Note or condition	P-Number
		Min.	Typ.	Max.			
Thermal resistance junction to top	Ψ_{JTOP}	–	30	35	K/W	1)	PRQ-538
Thermal resistance junction to soldering point	R_{thJSP}	–	30	–	K/W	1) Simulated at exposed pad	PRQ-539
Thermal resistance junction to ambient	R_{thJA}	–	70	–	K/W	1)	PRQ-1125

1) Specified by design, not subject to production test

Note: Specified R_{th} values are according to Jedec JESD51-2,-5,-7 at natural convection on FR4 2s2p board; the product (chip + package) was simulated on a 76.2 x 114.3 x 1.5 mm board with 2 inner copper layers (2 x 70 µm Cu, 2 x 35 µm Cu). Where applicable a thermal via array under the exposed pad contacted the first inner copper layer. Simulation done at T_{AMB} = 85°C with all channels on, $P_{DISSIPATION}$ = 1.5 W and a homogeneous temperature distribution across the device.

5 Power management unit (PMU)

5.1 Features overview

- Power management control with diagnosis
- System mode control (startup, sleep, active, and failsleep in case of severe system failures)
- Wake configuration and management
- Reset management according to the system modes
- Windowed watchdog providing a highly reliable and safe way to recover from software or hardware failures
- Configurable with SFRs. Supports error condition signaling to the MCU via interrupt
- Data retention registers available in all PMU modes
- Immune to ISO pulses. Compliant with the LV124 specification

5.2 Block diagram

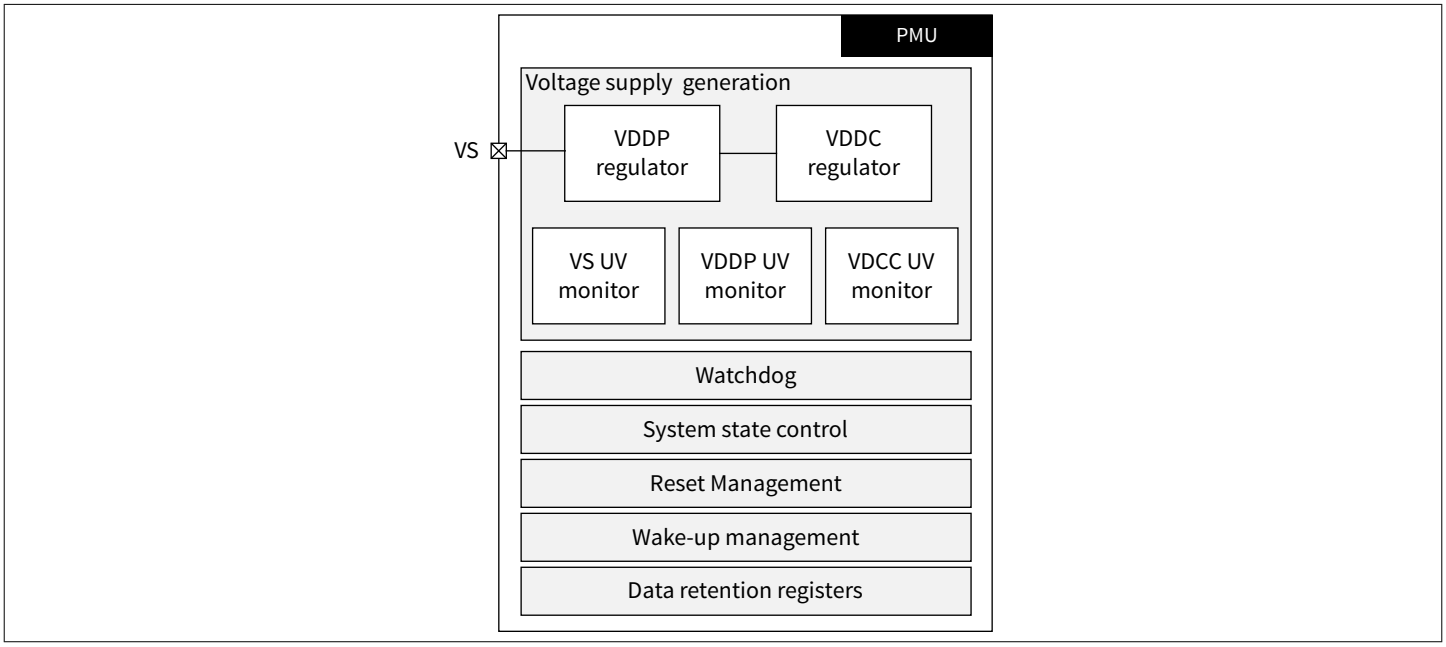

Figure 5 PMU block diagram

5.3 Voltage supply generation

5.3.1 VDDC 1V5 Source

As soon as the VDDC supply voltage is under $V_{DDCUVFALL}$ for more than 1 µs (nominal) a VDDC undervoltage event is detected. The VDDC undervoltage is requesting a reset and it is reported via a status register.

Similar to the VDDC undervoltage, as soon as the VDDC supply voltage is above $V_{DDCOVRISE}$ for more than *2* µs (nominal) a VDDC overvoltage event is detected. The VDDC overvoltage is requesting an interrupt and it is reported via a status register.

5.3.2 VS undervoltage monitor

As soon as the VS supply voltage is under V_{SUV} for more than 1 µs (nominal) a VS undervoltage event is detected. The VS undervoltage is requesting a reset and it is reported via a status register.

5.4 Watchdog

A window watchdog mechanism is available to safeguard user software timing.

The incorrect servicing of the watchdog triggers a reset which is reported in a status register. After five times consecutive incorrect services a failsleep is entered.

The watchdog is serviced by toggling a trigger bit.

The watchdog is clocked with a clock source independent of the system clock.

The watchdog period is programmable.

5.5 System state control

5.5.1 PMU system modes overview

The device has the following operating modes:

- unsupplied (reset)
- startup
- active
- sleep
- failsleep

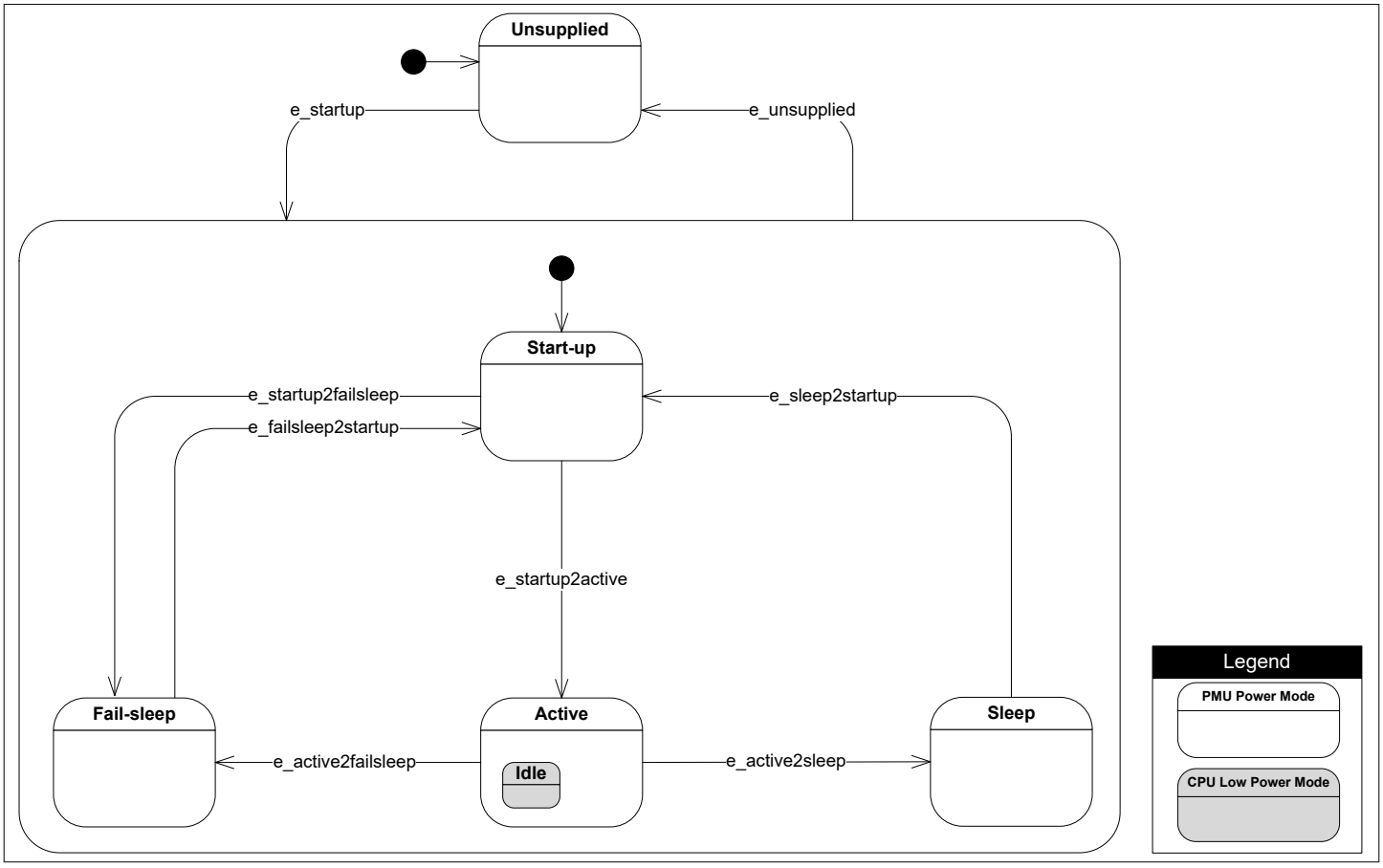

Figure 6 Power mode state diagram

5.5.2 PMU mode transitions

Table 6 Power mode transitions

From\To	unsupplied	startup	active	sleep	failsleep
unsupplied	–	e_startup	–	–	–
startup	e_unsupplied	–	e_startup2active	–	e_startup2failsleep
active	e_unsupplied	–	–	e_active2sleep	e_active2failsleep
sleep	e_unsupplied	e_sleep2startup	–	–	–
failsleep	e_unsupplied	e_failsleep2startup	–	–	–

Table 7 Power mode transition conditions

Transition	Condition
e_unsupplied	Power supply voltage $V_S < V_{S\_PD}$
e_startup	Power supply voltage $V_S > V_{S(min)}$
e_sleep2startup	Wake-up event occurred
e_failsleep2startup	The failure is not permanent AND a wake-up event occurred
e_startup2active	Internal supplies are stable
e_active2sleep	Sleep request by CPU
e_startup2failsleep	Unrecoverable hardware fault detected
e_active2failsleep	Five consecutive watchdog timeout events occurred OR unrecoverable hardware fault detected

5.6 Reset management

The PMU provides register for inspecting the reset sources allowing to determine the reason for the last reset. This register can be cleared by the user software only.

5.7 Wake-up management

The PMU accepts wake-up requests from the following sources:

- LIN
- GPIO

5.8 Data retention registers

The PMU provides dedicated registers to store 96 bits of data. The content is retained in all the PMU operation modes except unsupplied mode.

5.9 Electrical characteristics PMU

5.9.1 PMU operating conditions

Table 8 PMU operating conditions

V_S = 5.5 V to 29 V, T_J = -40°C to +150°C, all voltages with respect to ground, positive currents flowing as described in Chapter 2 (unless otherwise specified). Typical values: V_S = 13.5 V, T_J = 25°C

Parameter	Symbol	Values			Unit	Note or condition	P-Number
		Min.	Typ.	Max.			
Input voltage	V_S	5.5	13.5	29	V	–	PRQ-2871
Input capacitor	C_{VS}	2	–	–	µF	*1) 2) 3)*	PRQ-2872
Power supply undervoltage monitor	V_{SUV_MON}	4.8	–	5.5	V	V_S voltage falling	PRQ-2853
Power-down voltage	V_{S_PD}	–	–	3.6	V	V_S voltage falling	PRQ-479

1) Ceramic capacitor is recommended
2) When DC voltage is applied to a ceramic capacitor, the effective capacitance is reduced due to DC bias effect. The table above therefore lists the minimum value as capacitance. In order to meet the minimum capacitance requirement, the nominal value of the capacitor may have to be scaled accordingly to take the drop of capacitance into account for a given DC voltage at the outputs of regulators.
3) Specified by design, not subject to production test

5.9.2 Current consumption

Table 9 Current consumption

V_S = 5.5 V to 29 V, T_J = -40°C to +150°C, all voltages with respect to ground, positive currents flowing as described in Chapter 2 (unless otherwise specified). Typical values: V_S = 13.5 V, T_J = 25°C

Parameter	Symbol	Values			Unit	Note or condition	P-Number
		Min.	Typ.	Max.			
Active mode current consumption	$I_{VS(ACTIVE)}$	–	12	15	mA	Active mode: SYS0_CLK = 40 MHz, CPU_CLK = 20 MHz. MCU executing code from NVM, MCU subsystem only, all other external peripherals disabled	PRQ-481
Active mode current consumption at reduced frequency	$I_{VS(ACTIVE)}$	–	1.5	2	mA	Active mode, slow-down operation: SYS0_CLK = CPU_CLK = 1 MHz. MCU executing code from NVM, MCU subsystem only, all other external peripherals disabled	PRQ-2890

(table continues...)

Table 9 (continued) Current consumption

V_S = 5.5 V to 29 V, T_J = -40°C to +150°C, all voltages with respect to ground, positive currents flowing as described in Chapter 2 (unless otherwise specified). Typical values: V_S = 13.5 V, T_J = 25°C

Parameter	Symbol	Values			Unit	Note or condition	P-Number
		Min.	Typ.	Max.			
Idle mode current consumption	$I_{VS(IDLE)}$	–	10	12	mA	Idle mode operation: SYS0_CLK = 40 MHz. CPU_CLK = stopped. No DMA, bus system stopped. MCU idle. MCU subsystem only, all other external peripherals disabled	PRQ-2891
Sleep mode current consumption	$I_{VS(SLEEP)}$	–	20	30	µA	T_J = -40°C to 85°C; V_S = 7.3 V to 18 V; sleep mode; $V_{BUS} = V_{BUS\_REC}$	PRQ-480
Sleep mode current consumption	$I_{VS(SLEEP)}$	–	150	200	µA	T_J = -40°C to 85°C V_S = 3.6 V to 7.3 V sleep mode	PRQ-2893
Failsleep mode current consumption	$I_{VS(SLEEP)}$	–	20	30	µA	T_J = -40°C to 85°C failsleep mode V_S = 7.3 V to 18 V	PRQ-2894

5.9.3 VDDC linear regulator

Table 10 VDDC linear regulator

V_S = 5.5 V to 29 V, T_J = -40°C to +150°C, all voltages with respect to ground, positive currents flowing as described in Chapter 2 (unless otherwise specified). Typical values: V_S = 13.5 V, T_J = 25°C

Parameter	Symbol	Values			Unit	Note or condition	P-Number
		Min.	Typ.	Max.			
VDDC DC voltage	V_{DDC}	1.4	1.5	1.6	V	$V_S \geq V_{S\_EXT(min)}$	PRQ-2897
VDDC monitor undervoltage falling threshold	$V_{VDDCUVFALL}$	1.2	1.25	1.3	V	–	PRQ-2898
VDDC monitor overvoltage rising threshold	$V_{VDDCOVRISE}$	1.65	1.72	1.79	V	–	PRQ-2900
VDDC monitor overvoltage hysteresis	$V_{VDDCOVHYS}$	20	30	40	mV	1)	PRQ-2901
VDDC monitor undervoltage hysteresis	$V_{VDDCUVHYS}$	20	30	40	mV	1)	PRQ-2903

1) Specified by design, not subject to production test

5.9.4 VDDP linear regulator

Table 11 VDDP linear regulator

V_S = 5.5 V to 29 V, T_J = -40°C to +150°C, all voltages with respect to ground, positive currents flowing as described in Chapter 2 (unless otherwise specified). Typical values: V_S = 13.5 V, T_J = 25°C

Parameter	Symbol	Values			Unit	Note or condition	P-Number
		Min.	Typ.	Max.			
VDDP DC output voltage	V_{VDDP}	4.75	5.0	5.25	V	–	PRQ-2904
VDDP monitor undervoltage hysteresis	$V_{VDDPUVHYS}$	250	300	350	mV	1)	PRQ-2906

1) Specified by design, not subject to production test

5.9.5 Power supply DC specification

Table 12 Power supply DC specification

V_S = 5.5 V to 29 V, T_J = -40°C to +150°C, all voltages with respect to ground, positive currents flowing as described in Chapter 2 (unless otherwise specified). Typical values: V_S = 13.5 V, T_J = 25°C

Parameter	Symbol	Values			Unit	Note or condition	P-Number
		Min.	Typ.	Max.			
Power-up voltage	V_{S_PU}	–	–	4.7	V	V_S voltage rising	PRQ-921

5.9.6 Watchdog

Table 13 Watchdog

V_S = 5.5 V to 29 V, T_J = -40°C to +150°C, all voltages with respect to ground, positive currents flowing as described in Chapter 2 (unless otherwise specified). Typical values: V_S = 13.5 V, T_J = 25°C

Parameter	Symbol	Values			Unit	Note or condition	P-Number
		Min.	Typ.	Max.			
Watchdog timer clock period	t_{WDTCLK}	40	50	60	ns	1)	PRQ-2953
Long open window (LOW) duration	t_{LOW}	160	200	240	ms	1)	PRQ-2310
Short open window (SOW) duration	t_{SOW}	24	30	36	ms	1)	PRQ-2311

1) Specified by design, not subject to production test

5.9.7 System state control

Table 14 System state control

V_S = 5.5 V to 29 V, T_J = -40°C to +150°C, all voltages with respect to ground, positive currents flowing as described in Chapter 2 (unless otherwise specified). Typical values: V_S = 13.5 V, T_J = 25°C

Parameter	Symbol	Values			Unit	Note or condition	P-Number
		Min.	Typ.	Max.			
Unsupplied to active mode	$t_{UNSUP2ACT}$	–	–	2.5	ms	Time power-up event to first instruction execution in user software or BSL ready	PRQ-2474
Active to sleep mode	$t_{ACTIVE2SLEEP}$	–	–	250	µs	Triggered by WFE command	PRQ-835
Sleep to active mode	$t_{SLP2ACT}$	–	–	2.5	ms	Triggered by a wake-up event	PRQ-2316
Failsleep to active mode	$t_{FSLP2ACT}$	–	–	2.5	ms	Triggered by wake-up event	PRQ-2318

6 System control unit (SCU)

- The SCU provides a flexible clock management
- The SCU synchronizes the reset signals
- The SCU provides interrupt mapping features
- The SCU provides power control for load stepping

6.1 Clock control

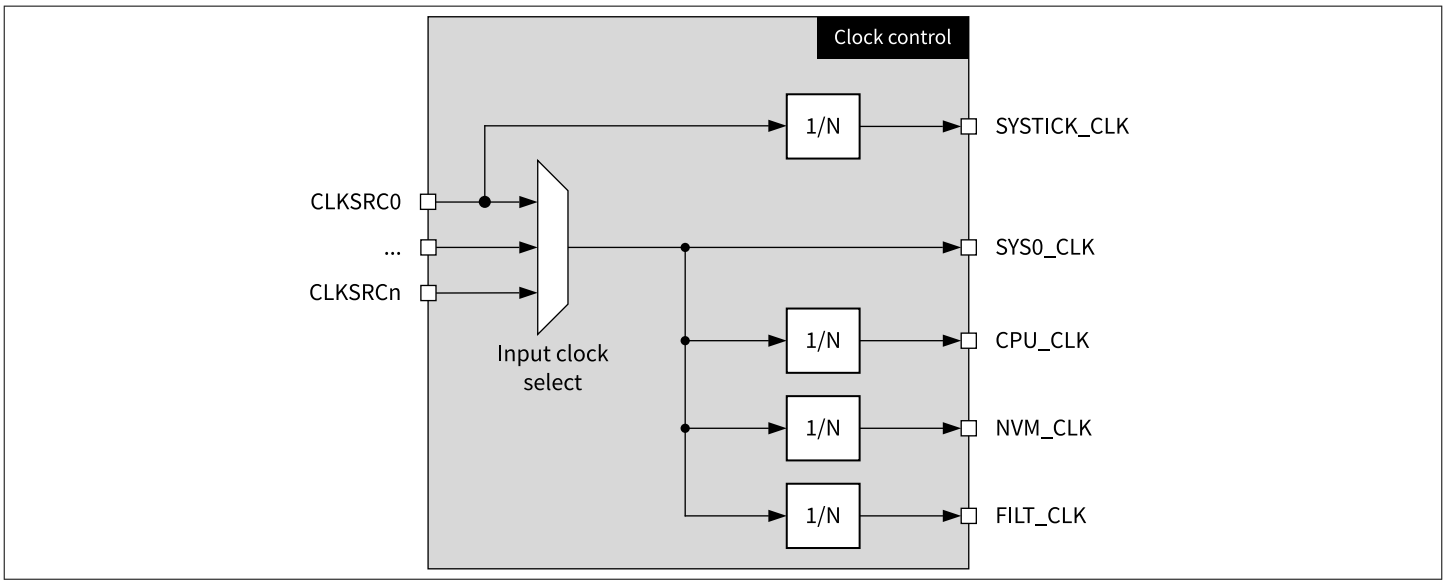

Figure 7 Clock generation

The SCU is able to select a configurable input clock source for SYS0_CLK.

6.1.1 Clock source inputs

The following clock sources can be selected:

- Clock source 0 with a frequency of $f_{CLKSRC0}$
- Clock source 1 which is generated from clock source 0 by a P/Q divider

6.1.2 Clock generation

The SCU generates clock NVM_CLK for the NVM from SYS0_CLK.

The SCU generates clock CPU_CLK for the CPU subsystem from SYS0_CLK.

The SCU generates clock FILT_CLK from SYS0_CLK. The selected input clock source and 1/N divider setting must ensure that the FILT_CLK frequency is within the range of f_{FILT_CLK}.

The frequency *f* of clocks generated from system clock SYSn_CLK is done via individual 1/N dividers according to the following formula:

$$f = \frac{f_{SYSn\_CLK}}{N} \quad (1)$$

Unless otherwise specified, the programmable values for N are listed in Table 15.

Table 15 Programmable 1/N scaling values

Scaling value
1
2
3
4
6
8
16
20

Table 16 Programmable 1/N scaling values for NVM_CLK

Scaling value
1
2

The SCU generates clock SYSTICK_CLK from CLKSRC0 as input for the CPU. The SYSTICK_CLK frequency $f_{SYSTICK\_CLK}$ is configurable via a dedicated 1/N divider according to the following formula:

$$f_{SYSTICK\_CLK} = \frac{f_{CLKSRC0}}{N} \quad (2)$$

The programmable values for N are from 1 to 511.

6.2 Peripheral control

Peripheral control performs power-up/power-down sequencing for individual peripherals according to power steps limits of the supply system. The power-up/power-down time for individual modules is t_{POWSEQ}.

Idle mode and sleep mode entry sequence is applied upon POWAVE_REQ mode request input signal from CPU.

The POWAVE_REQ is triggered with Arm® Cortex®-M sleep mode request with WFE/WFI instruction.

The selection between idle mode and sleep mode is performed with a dedicated register in SCU.

The default is idle mode.

6.3 Interrupt control

The interrupt control collects the interrupt sources of the peripherals and maps to the CPU input vector using configuration registers.

6.4 Electrical characteristics SCU

6.4.1 Clock control

Table 17 Electrical characteristics

V_S = 5.5 V to 29 V, T_J = -40°C to +150°C, all voltages with respect to ground, positive currents flowing as described in Chapter 2 (unless otherwise specified). Typical values: V_S = 13.5 V, T_J = 25°C

Parameter	Symbol	Values			Unit	Note or condition	P-Number
		Min.	Typ.	Max.			
SYS0_CLK frequency	f_{SYS0_CLK}	39.6	40	40.6	MHz	–	PRQ-2471
Filter clock frequency	f_{FILT_CLK}	1.9	2	2.1	MHz	To be ensured by user configuration [1)]	PRQ-3103

1) It must be ensured that the frequency resulting from combined configuration of SYS0_CLK and relevant 1/N clock divider lies within the specified range

6.4.2 Clock monitoring

Table 18 Electrical characteristics clock monitoring

V_S = 5.5 V to 29 V, T_J = -40°C to +150°C, all voltages with respect to ground, positive currents flowing as described in Chapter 2 (unless otherwise specified). Typical values: V_S = 13.5 V, T_J = 25°C

Parameter	Symbol	Values			Unit	Note or condition	P-Number
		Min.	Typ.	Max.			
Reference clock (REFCLK) failure detection time	$t_{REFCLKFD}$	11	14	17	µs	Timing is referred to the master clock (MCLK) [1)]	PRQ-2971
Master clock (MCLK) watchdog timeout to device reset time	$t_{M\_CLKLOSS}$	25	30	35	µs	Timing is referred to the standby clock (REFCLK) [1)]	PRQ-3119

1) Specified by design, not subject to production test

6.4.3 Peripheral control

Table 19 Electrical characteristics peripheral control

V_S = 5.5 V to 29 V, T_J = -40°C to +150°C, all voltages with respect to ground, positive currents flowing as described in Chapter 2 (unless otherwise specified). Typical values: V_S = 13.5 V, T_J = 25°C

Parameter	Symbol	Values			Unit	Note or condition	P-Number
		Min.	Typ.	Max.			
Peripheral control sequencing time	t_{POWSEQ}	–	–	0.2	ms	–	PRQ-2347

7 Clock sources

7.1 Features overview

The master clock (MCLK) is always on, in active mode. It has following use cases:

- Clock source for filters within the PMU
- Clock source for the watchdog timer (WDT)

The device features clock source 0 with a frequency of $f_{CLKSRC0}$.

Clock source 1 is generated from clock source 0 with a P/Q divider according to the following formula:

$$f_{CLKSRC1} = \frac{P}{Q} \times f_{CLKSRC0} \quad (3)$$

The allowed range for P and Q is 1 to 1023, whereby P/Q has to be ≤ 1.

7.2 Block diagram

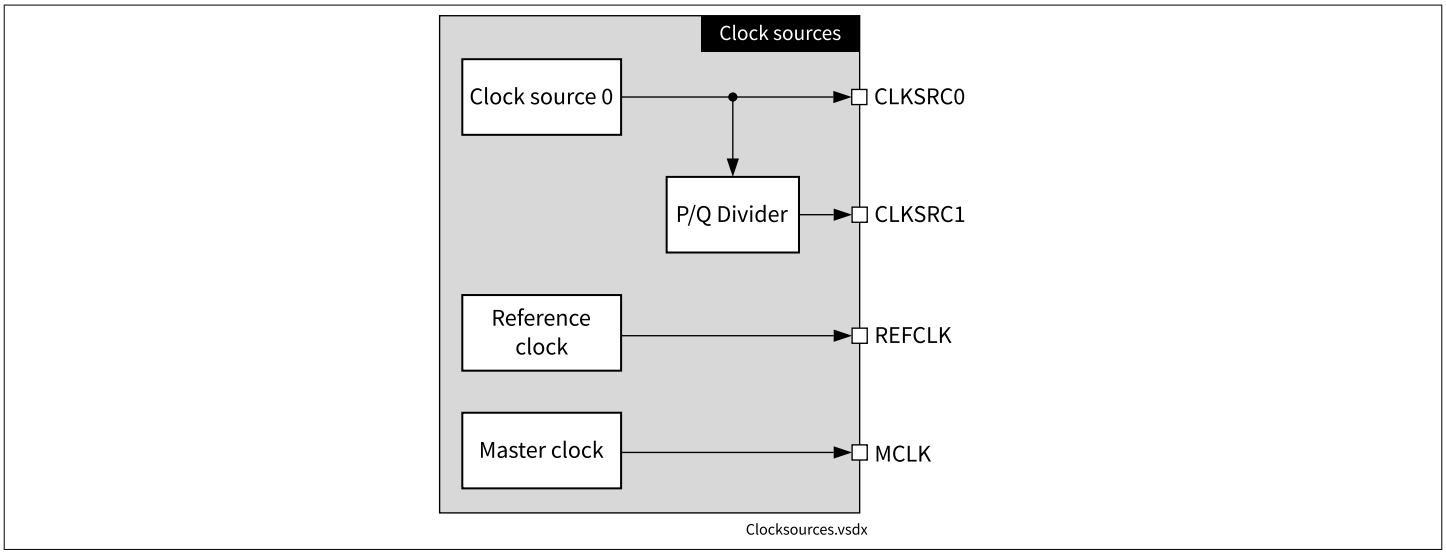

Figure 8 Internal clock sources

7.3 Electrical characteristics clock sources

Table 20 Electrical characteristics

V_S = 5.5 V to 29 V, T_J = -40°C to +150°C, all voltages with respect to ground, positive currents flowing as described in Chapter 2 (unless otherwise specified). Typical values: V_S = 13.5 V, T_J = 25°C

Parameter	Symbol	Values			Unit	Note or condition	P-Number
		Min.	Typ.	Max.			
Clock source 0 frequency	$f_{CLKSRC0}$	39.4	40	40.6	MHz	$T_J \leq 150°C$	PRQ-2828
Master clock frequency	f_{MCLK}	17	20	23	MHz	–	PRQ-482
Reference clock frequency	f_{REFCLK}	85	100	115	kHz	–	PRQ-3132

8 Microcontroller subsystem (MCU)

8.1 Features overview

- Arm® Cortex®-M23 core
- Arm® v8-M architecture
- Arm® Thumb® + Thumb®-2 instruction set
- Fast multiply (one cycle)
- Debug access through debug access port (DAP) via serial wire debug (SWD) connection
- Halt after reset (HAR) support
- The debug access can be disabled
- Four hardware breakpoints
- Four data watchpoints
- ARM® AMBA® 5 AHB interface for code, data, debug and peripheral transactions
- 32 external interrupt inputs, each with four levels of priority
- The system timer (SYSTICK) can be used as general purpose timer, for example, for periodic operating system tick. The SYSTICK event can request an exception at the NVIC. The SYSTICK has following features:
  - 24-bit down counting timer
  - Auto-reload from programmable reload value
  - Selectable clock source
  - CPU exception (system tick)
- Secure usage is programmable

8.2 Block diagram

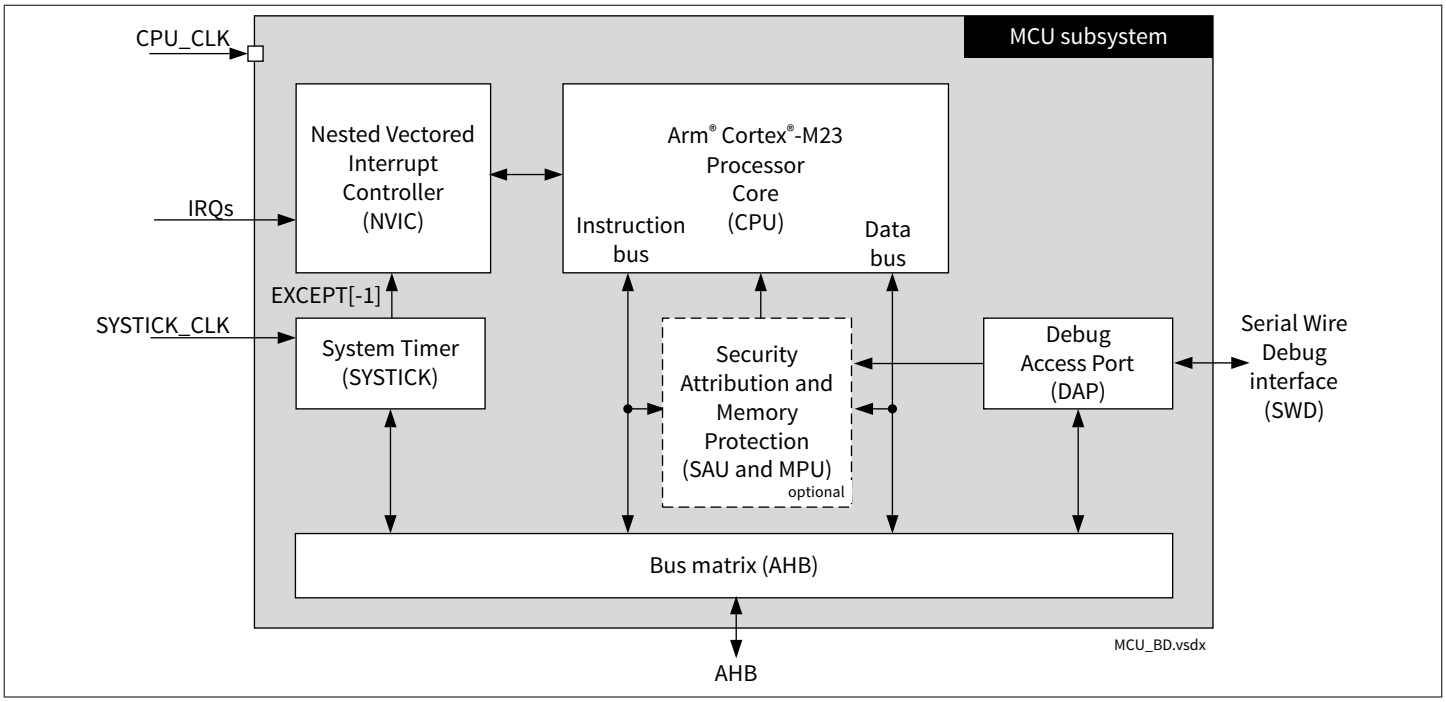

Figure 9 MCU block diagram

8.3 Arm® Cortex® Core

The device integrates a processor with following feature set:

- Arm® Cortex®-M23 core
- Arm®v8-M architecture
- Thumb® + Thumb®-2 instruction set
- SysTick timer
- Hardware divider
- Hardware multiplier

The device integrates a nested vectored interrupt controller (NVIC) with following feature set:

- Configurable number of external interrupts
- Programmable interrupt priority levels
- Dynamic re-prioritization of interrupts

The CPU is connected to an advanced high-performance bus (AHB) as bus master.

The core provides a debug unit with following configuration options:

- Accessible via serial wire debug interface (SWD)
- CPU register can be read and write
- System memory access
- 4 hardware debug breakpoints
- Halt after reset (HAR)
- The debug unit can be disabled to avoid an unintended activation in the final application

The debug mechanism supports up to four data watchpoints.

9 Memory system

The memory subsystem provides

- Access to ROM, RAM, Flash and configuration sectors through the AHB interface
- MBIST for RAM
- MBIST for ROM
- Flash erase and program function

9.1 NVM

The flash has a hardware error correction.

9.1.1 Flash programming

The device offers means for the user to program the NVM.

9.1.2 Flash error correction (ECC)

The hardware error correction (ECC) can correct a single bit error and detect a double bit error (SECDET):

- In case a single bit error is detected, an error flag ECC1 is set
- In case a double bit error is detected, a warning flag ECC2 is set, an NMI can be requested

9.2 SRAM

The hardware error correction (ECC) can correct a single bit error and detect a double bit error (SECDET):

- In case a single bit error is detected an error flag ECC1 is set, an NMI can be requested
- In case a double bit error is detected a warning flag ECC2 is set, an NMI can be requested

9.3 Electrical characteristics

Table 21 Electrical characteristics

V_S = 5.5 V to 29 V, T_J = -40°C to +150°C, all voltages with respect to ground, positive currents flowing as described in Chapter 2 (unless otherwise specified). Typical values: V_S = 13.5 V, T_J = 25°C

Parameter	Symbol	Values			Unit	Note or condition	P-Number
		Min.	Typ.	Max.			
BROM size	n_{BROM}	16	–	–	kB	–	PRQ-140
SRAM size	n_{SRAM}	3	–	–	kB	–	PRQ-137
Flash size	n_{FLASH}	32	–	–	kB	–	PRQ-139
1000TP size	n_{1000TP}	576	–	–	Byte	–	PRQ-141
Initial read access time	t_{RD}	–	–	75	ns	–	PRQ-2810
Write time per page	t_{WR}	–	3	3.5	ms	1)	PRQ-2811
Erase time per sector/ page	t_{ER}	4	4.5	–	ms	1)	PRQ-2813
Endurance	n_{ER}	1000	–	–	cycles	–	PRQ-147
Data retention	t_{RET}	20	50	–	years	–	PRQ-646
Minimum VS programming voltage	V_{VSPROG}	4.95	–	–	V	–	PRQ-3143

(table continues...)

Table 21 (continued) Electrical characteristics

V_S = 5.5 V to 29 V, T_J = -40°C to +150°C, all voltages with respect to ground, positive currents flowing as described in Chapter 2 (unless otherwise specified). Typical values: V_S = 13.5 V, T_J = 25°C

Parameter	Symbol	Values			Unit	Note or condition	P-Number
		Min.	Typ.	Max.			

1) Specified by design, not subject to production test

10 General purpose input / output (GPIO)

The device provides two general purpose input/output pins GPIO0 and GPIO1. The GPIOs can be used as

- Open drain digital input/output for signaling
- Wake-up source from sleep mode
- Analog input connected to the internal ADC multiplexer for external measurements, for example external NTC/PTC measurements

The GPIOn pins integrate an internal pull-down function, where the pull-down current is defined by I_{IO_PD}.

The pull-down current can be activated when the pin is configured as a digital input pin and is disabled if the pin is used as an analog input pin.

The GPIOs can be configured via register as analog input pins for external voltage measurements, for example for external NTC/PTC temperature measurements.

The pull-down function is disabled in case the GPIOn is configured as analog input pin.

10.1 Electrical characteristics

Table 22 Electrical characteristics

V_S = 5.5 V to 29 V, T_J = -40°C to +150°C, all voltages with respect to ground, positive currents flowing as described in Chapter 2 (unless otherwise specified). Typical values: V_S = 13.5 V, T_J = 25°C

Parameter	Symbol	Values			Unit	Note or condition	P-Number
		Min.	Typ.	Max.			
General purpose input / output							
IO low voltage	V_{IO_L}	0	–	0.8	V	–	PRQ-853
IO high voltage	V_{IO_H}	2.0	–	5.5	V	Internally clamped to ≥ 5.5 V if the input current is ≤ I_{IO} and pin is configured as input	PRQ-854
Analog input voltage range	V_{AIN}	0	–	4	V	–	PRQ-855
Digital input voltage range	V_{DIN}	0	–	5	V	–	PRQ-881
Input pull-down current	I_{IO_PD}	3	10	25	µA	V_{IO} = 5 V; configured as digital input	PRQ-856
Input leakage current	I_{IL}	-1	–	1	µA	V_{AIN} = 4 V; configured as analog input	PRQ-857
Output impedance	R_{IO}	1000	2000	3000	Ω	Configured as digital output low. V_{IO} = 0.4 V	PRQ-1131
Time for GPIO wake-up	t_{WK_IO}	30	–	150	µs	[1] Including analog and digital filter time. Digital filter time can be adjusted via register.	PRQ-928

(table continues...)

Table 22 (continued) Electrical characteristics

V_S = 5.5 V to 29 V, T_J = -40°C to +150°C, all voltages with respect to ground, positive currents flowing as described in Chapter 2 (unless otherwise specified). Typical values: V_S = 13.5 V, T_J = 25°C

Parameter	Symbol	Values			Unit	Note or condition	P-Number
		Min.	Typ.	Max.			
Analog filter time for GPIO wake-up	$t_{WK\_IO\_filter}$	3	–	15	µs	1) An additional digital filter is required to achieve the required wake-up time	PRQ-929

1) Specified by design, not subject to production test

11 Measurement unit

- 11-bit ADC with 3 inputs allowing measurement of LED forward voltage
- 2 inputs for GPIO voltage measurement
- 10-bit digital temperature sensor (DTS) for monitoring the chip temperature
- 11-bit supply monitoring

11.1 DTS

The device has an 11-bit digital temperature sensor (DTS) integrated.

11.2 ADC

The device has a differential analog to digital converter integrated to measure LED forward voltages.

ADC measurements can be triggered by other IP blocks, such as the power stage.

11.3 Supply monitoring

The device provides an analog to digital conversion of V_S voltage measurement with a resolution of n_{VRES_Sup}. The device samples the V_S once per PWM period and stores the result in a VS result register. New data is signaled with a dedicated valid flag, which is reset after reading completion.

11.4 LED forward voltage measurement

The LED forward voltage measurements, performed by the ADC, follow a schedule that is configurable via registers.

Schedule configuration consists of the following settings:

- A measurement start value per channel relative to the beginning of the PWM period and independent of the duty cycle configuration (i.e. possible during on and off period).
- A fixed sequential priority ranking in case of equal start values of multiple channels. Channel 0 has the highest priority.

To ensure a reliable measurement result, the time between output activation for each channel and its corresponding forward voltage measurement has to be at least t_{DIAG_DLY} and the output has to be activated during the entire measurement.

The LED forward voltage measurements are performed in every PWM period. After measurements for all channels have been performed in the current PWM period, there are no further forward voltage measurements performed until the next PWM period.

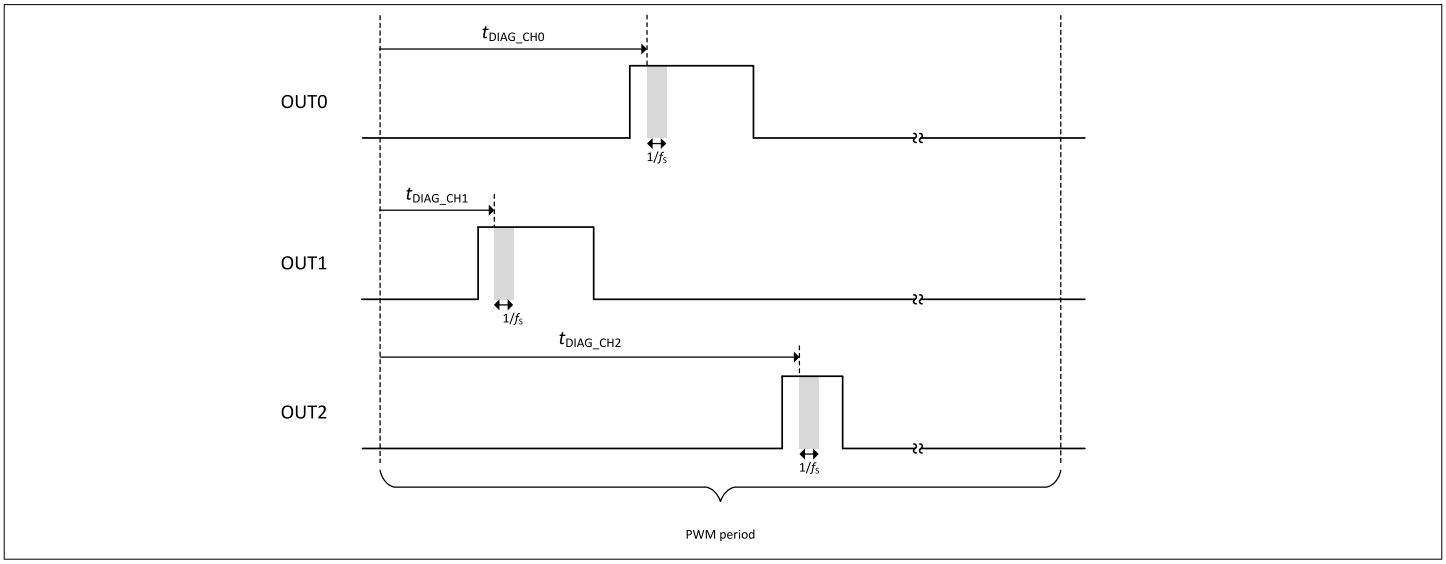

Figure 10 LED forward voltage measurement configuration (sequence = OUT1, OUT0, OUT2)

The input gain for LED forward voltage measurements can be configured to k_{VF1} or k_{VF2} via register.

11.5 Electrical characteristics

Table 23 Electrical Characteristics

V_S = 5.5 V to 29 V, T_J = -40°C to +150°C, all voltages with respect to ground, positive currents flowing as described in Chapter 2 (unless otherwise specified). Typical values: V_S = 13.5 V, T_J = 25°C

Parameter	Symbol	Values			Unit	Note or condition	P-Number
		Min.	Typ.	Max.			
ADC							
Conversion resolution	n_{VRES}	11	–	–	Bit	–	PRQ-900
Supply voltage conversion resolution	n_{VRES_Sup}	11	–	–	Bit	Full scale 20.067 V	PRQ-924
Differential nonlinearity error	*DNL*	-1	–	1	LSB	–	PRQ-902
Integral nonlinearity	*INL*	-2	–	2	LSB	–	PRQ-903
Offset	ADC_{offset}	-2	–	2	LSB	–	PRQ-904
Gain error	ADC_{gain}	-0.5	–	0.5	%	–	PRQ-905
Sampling rate	f_S	250	–	–	kS/s	1)	PRQ-906
Forward voltage measurement gain	k_{VF1}	–	1	–	–	Conversion range 0 V to 4 V	PRQ-2512
Forward voltage measurement gain	k_{VF2}	–	0.5	–	–	Conversion range 0-8 V	PRQ-2513
Forward voltage measurement timing	t_{DIAG_CHn}	0	–	PWM_MAX	–	1) Time in peripheral clock cycles. n = channel number	PRQ-955
DTS							
DTS absolute accuracy	A_{DTS_abs}	-7	–	+7	K	–	PRQ-913

1) Specified by design, not subject to production test

12 Power stage

- Three open-drain linear current sink output power stages
- Three individually configurable start and stop PWM compare registers with 16-bit resolution to configure the duty cycle and phase shift
- One master PWM frequency f_{PWM}
- Output current individually configurable for each channel
- Parallel output operation
- Integrated thermal overload protection

The device integrates 3 output power stages.

The output stages sink an individually configurable current I_{OUT} according to the formula below, where n is a 5-bit value configurable via register.

$$I_{OUT} = 5 + 1.5 \times n \quad (4)$$

Up to all output stages can be used in parallel to achieve a higher output current without any dedicated configuration needs.

The power output stage provides an individual configurable normal and fast switching mode where the turn-on and turn-off timings are defined in PWM output timing and the timing definition is shown in Figure 11.

The normal switching mode is the default configuration and can be changed to fast-mode via registers.

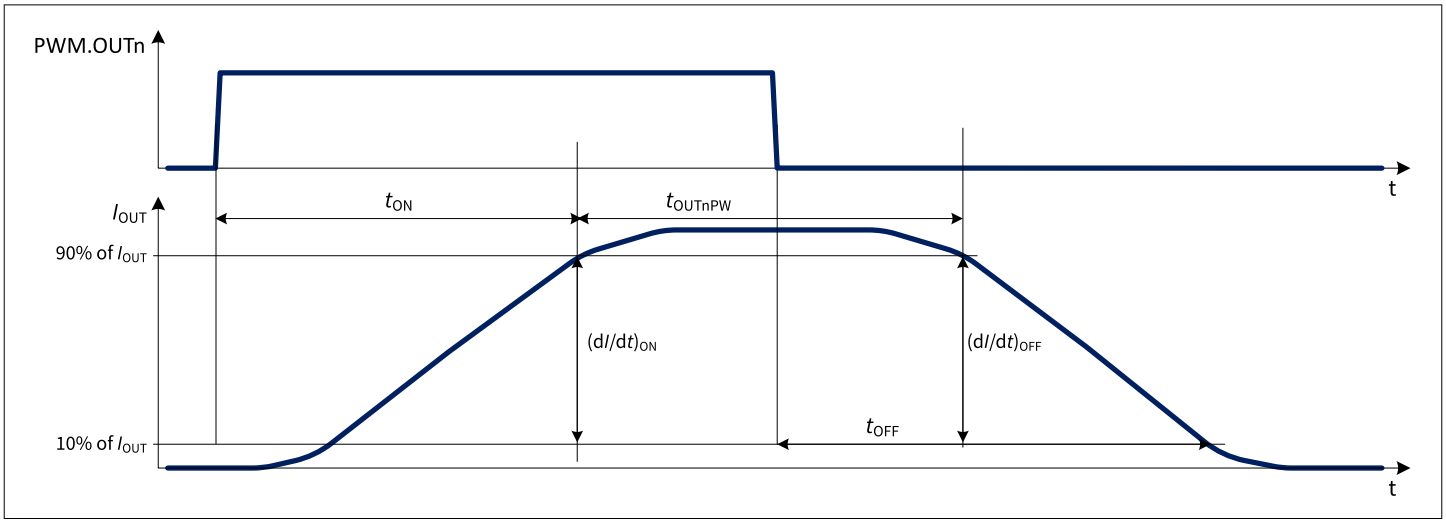

Figure 11 Output stage timing definition

12.1 PWM Generator

The device operates each power output stage with a PWM function containing

- Individually configurable start and stop compare values per output channel
- One global PWM frequency

The PWM engine operates with one master PWM frequency defined by a period value PWM_MAX with resolution n_{PWM} and configurable via register. The PWM frequency is determined by the following formula.

$$f_{PWM} = \frac{f_{SYS0\_CLK}}{n_{PWM\_PS} \times (PWM\_MAX + 1)} \quad (5)$$

The following table lists some examples for PWM_MAX period values and the resulting PWM frequencies.

Table 24 PWM frequency examples (f_{SYS0_CLK} = 40 MHz)

n_{PWM_PS}	PWM_MAX	f_{PWM} in Hz
1	0xFFFF (16 bit)	610
1	0x7FFF (15 bit)	1220
2	0x3FFF (14 bit)	1220
2	0x1FFF (13 bit)	2440
4	0x0FFF (12 bit)	2440

The PWM engine provides a total of 3 individually configurable PWM phase shift values, one per output channel, configurable via register.

The PWM engine provides a total of 3 individually configurable PWM duty cycle values, one per output channel, configurable via register.

Duty cycle and phase shift of the output channels are controlled via the corresponding phase shift and duty cycle registers.

Updated phase shift and duty cycle values of a channel are applied to the power stages synchronously to the internal PWM period, that is, the power output duty cycle and phase shift change is seen the latest after one PWM period ($1/f_{PWM}$).

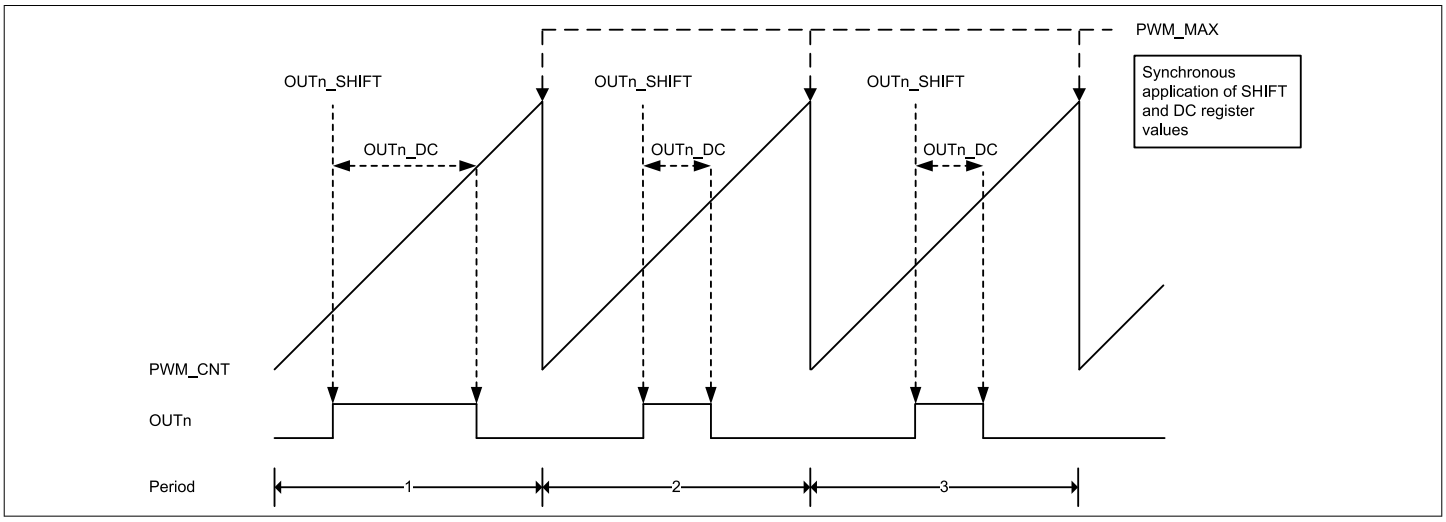

Figure 12 PWM output generation

12.2 Output stage protection

The output stage integrates an individual thermal overload protection.

The output stage turns off if the junction temperature exceeds $T_{J\_SD\_LCS}$ with a hysteresis of $\Delta T_{J\_SD\_LCS}$ and reports the thermal overload event in a fault register.

The output stage contains a configurable protection behavior for the thermal overload fault event. The protection behavior consists of two options, 1) synchronized latch off and 2) latch off.

- All output stages turn off after a thermal overload event if it is configured to 1) synchronized latch off. All output stages remains off as long as the dedicated fault register is not cleared via register AND T_J is lower than $T_{J\_SD\_LCS}$ - $\Delta T_{J\_SD\_LCS}$.
- The output stage remains off after a thermal overload event if it is configured to 2) latch off, which is the default configuration. The output stage remains off as long as the dedicated fault register is not cleared via register AND T_J is lower than $T_{J\_SD\_LCS}$ - $\Delta T_{J\_SD\_LCS}$.

The protection behavior can be configured globally via register.

The output stage integrates a short to ground detection.

The output stage of the corresponding channel is turned off if an external short to ground is detected and the fault event is reported in a fault register.

12.3 Electrical characteristics

Table 25 Electrical Characteristics

V_S = 5.5 V to 29 V, T_J = -40°C to +150°C, all voltages with respect to ground, positive currents flowing as described in Chapter 2 (unless otherwise specified). Typical values: V_S = 13.5 V, T_J = 25°C

Parameter	Symbol	Values			Unit	Note or condition	P-Number
		Min.	Typ.	Max.			
Leakage currents							
Output leakage current	$I_{OUT-LEAK\_85}$	–	–	3	µA	$T_J \le 85°C$	PRQ-365
Output leakage current	$I_{OUT-LEAK}$	–	–	7	µA	$T_J \le 150°C$	PRQ-366
Output current accuracy and drop-out voltage							
Output current accuracy	A_{IOUT_25}	-5	–	5	%	$T_J \ge 25°C$; full scale range, where 5.0 mA ≤ I_{OUT} ≤ 51.5 mA	PRQ-367
Output current accuracy	A_{IOUT}	-10	–	10	%	-40°C ≤ T_J < 150°C; full scale range, where 5.0 mA ≤ I_{OUT} ≤ 51.5 mA	PRQ-369
Output current channel matching	I_{OUTn}, I_{OUTn+1}	-5	–	5	%	$(I_{OUTn} - I_{average})/I_{average}$, full scale range, where 5.0 mA ≤ I_{OUT} ≤ 51.5 mA	PRQ-372
Drop out voltage - all channels active	$V_{DR,all}$	1.2	–	–	V	$T_J \le 105°C$, all channels active, $I_{OUT} \ge 90\%$ of 51.5 mA	PRQ-376
PWM engine							
Number of PWM channels	n_{PWM_CH}	3	–	–	–	–	PRQ-379
PWM clock prescaler	n_{PWM_PS}	1	1	64	–	Integer value	PRQ-2796
PWM resolution	n_{PWM}	16	–	–	Bit	–	PRQ-381
PWM frequency	f_{PWM}	–	–	2500	Hz	1)	PRQ-2979
PWM frequency drift	f_{DRIFT}	-1	–	1	%	1) -20°C ≤ T_J < 125°C	PRQ-382
PWM output timing							
PWM turn on time (fast)	t_{ONfast}	–	300	900	ns	Fast switching mode; I_{OUT} = 90% of 30.0 mA; see Figure 11	PRQ-385

(table continues...)

Table 25 (continued) Electrical Characteristics

V_S = 5.5 V to 29 V, T_J = -40°C to +150°C, all voltages with respect to ground, positive currents flowing as described in Chapter 2 (unless otherwise specified). Typical values: V_S = 13.5 V, T_J = 25°C

Parameter	Symbol	Values			Unit	Note or condition	P-Number
		Min.	Typ.	Max.			
PWM turn off time (fast)	$t_{OFFfast}$	–	300	900	ns	Fast switching mode; I_{OUT} = 10% of 30.0 mA; see Figure 11	PRQ-393
PWM turn on time (normal)	$t_{ONnormal}$	15	20	25	µs	Normal switching mode, I_{OUT} = 90% of 51.5 mA, see Figure 11	PRQ-387
PWM turn off time (normal)	$t_{OFFnormal}$	15	20	25	µs	Normal switching mode; I_{OUT} = 10% of 51.5 mA; see Figure 11	PRQ-395
Current rise slew rate (normal)	dI/dt_{ON}	1.8	2.6	3.34	mA/µs	Normal switching mode, I_{OUT} rising from 10% to 90% of 51.5 mA, see Figure 11	PRQ-389
Current falling slew rate (normal)	dI/dt_{OFF}	-3.34	-2.6	-1.8	mA/µs	I_{OUT} falling from 90% to 10% of 51.5 mA; see Figure 11	PRQ-391
Protection							
Thermal shutdown temperature	$T_{J\_SD\_LCS}$	165	175	200	°C	1)	PRQ-399
Thermal shutdown hysteresis	$\Delta T_{J\_SD\_LCS}$	5	10	15	K	1)	PRQ-400

1) Specified by design, not subject to production test

13 UART

- Full-duplex asynchronous modes
  - 8-bit data frames, LSB first
  - Fixed or variable baud rate
- Receive buffered (1 byte)
- Interrupt generation on the completion of a data transmission or reception
- Baud-rate generator with fractional divider for generating a wide range of baud rates, such as 9.6 kBaud, 19.2 kBaud, 115.2 kBaud, 250.4 kBaud
- LIN support: hardware logic for break and sync byte detection
- LIN support: connected to timer channel for synchronization to LIN baud rate (autobaud)

The following figure shows the standard UART byte field consisting of a start bit, eight data bits and one stop bit. This structure is the basis for data transfer between communication partners. The LSB of the data is transmitted first and the MSB last. The start bit is encoded as a low and the stop bit is encoded as a high bit.

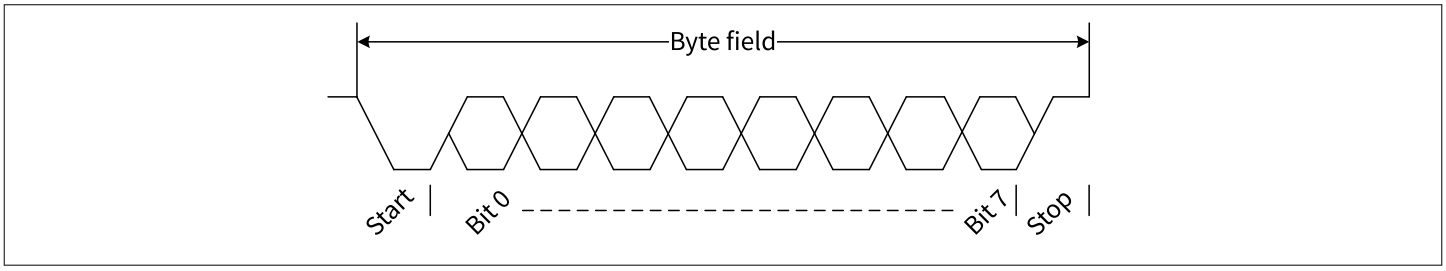

Figure 13 UART byte field

The following baud rates can be configured via register:

Supported baud rates

- 2400
- 4800
- 9600
- 19 200
- 20 000
- 115 200
- 250 400

14 LIN transceiver

The LIN module is a transceiver for the local interconnect network (LIN) compliant with the LIN2.2 standard, backward compatible to LIN1.3, LIN2.0 and LIN2.1. It operates as a bus driver between the protocol controller and the physical network. The LIN bus is a single wire, bi-directional bus typically used for in-vehicle networks, using baud rates between 2.4 kBaud and 20 kBaud. Additionally baud rates up to 250 kBaud are implemented.

The LIN module offers several different operation modes, including a LIN sleep mode and the LIN normal mode. The integrated slope control allows to use several data transmission rates with optimized EMC performance. For data transfer at the end of line, a flash mode up to 115 kBaud is implemented. This flash mode can be used for data transfer under special conditions for up to 250 kbit/s (in production environment, point-to-point communication with reduced wire length and limited supply voltage).

The device implements an LIN transceiver according to ISO 17987 series.

14.1 Features

General functional features

- Compliant to LIN2.2 standard, backward compatible to LIN1.3, LIN2.0 and LIN 2.1
- Compliant to SAE J2602 (slew rate, receiver hysteresis)

Special features

- Measurement of LIN master baudrate via Timer2
- LIN can be used as input/output with SFR bits
- TxD timeout feature (optional, on by default)
- Overcurrent limitation and overtemperature protection
- LIN module fully resettable via global enable bit

Operation modes features

- LIN sleep mode (LSLM)
- LIN receive-only mode (LROM)
- LIN normal mode (LNM)
- High voltage input/output mode (LHVIO)
- Auto-addressing SNPD and NAD via bus shunt method (BSM)

Slope modes features

- Normal slope mode (20 kbit/s)
- Low slope mode (10.4 kbit/s)
- Fast slope mode (62.5 kbit/s)
- Flash mode (115.2 kbit/s)

Wake-up features

- LIN bus wake-up. The wake-up happens on the falling edge of the LIN signal to allow wake-up and decoding of the same frame. It is also possible to enter the sleep mode with LIN dominant (caused by LIN shorted to GND, for example).

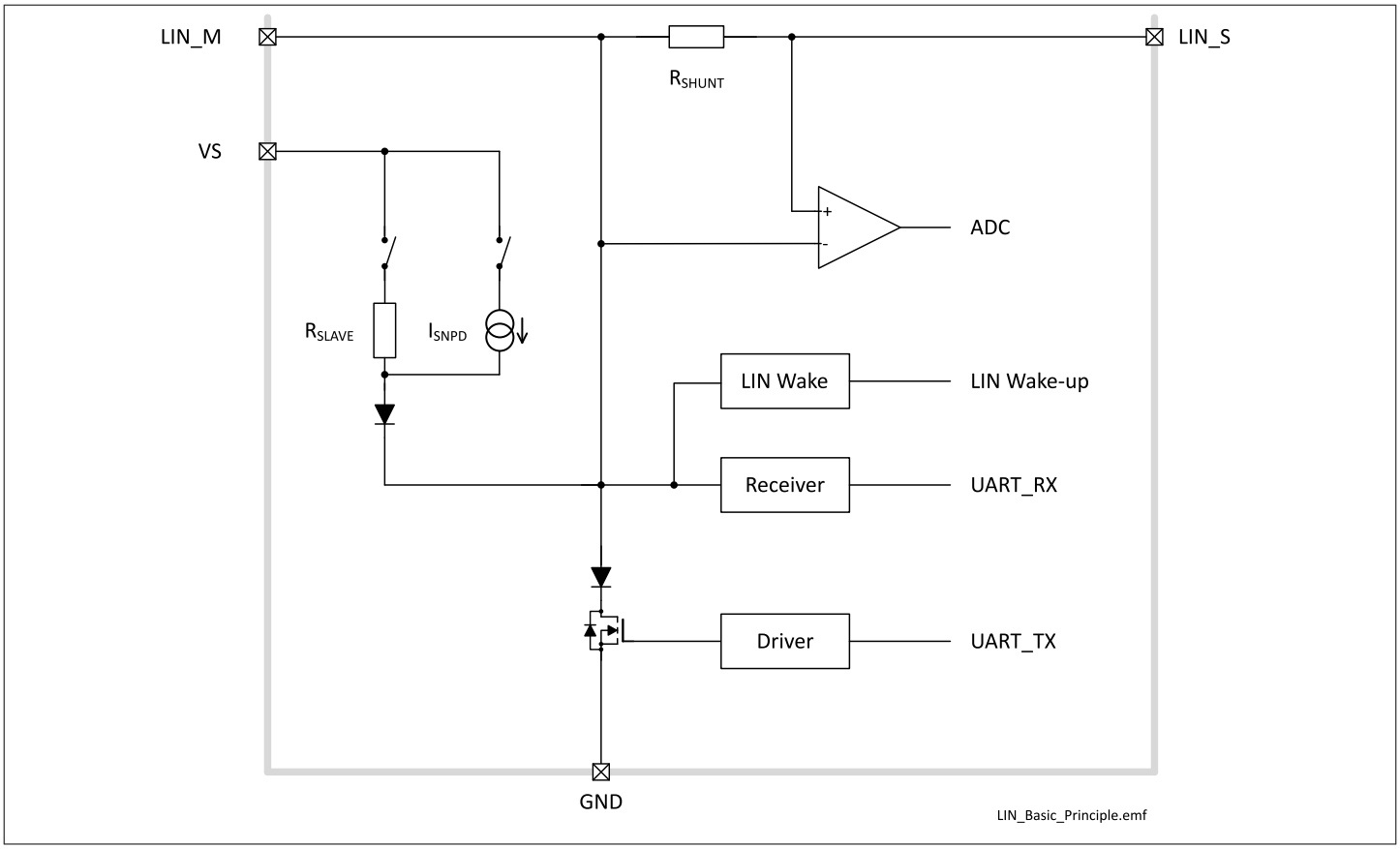

Figure 14 LIN basic principle diagram

14.2 Auto-addressing

The device implements slave node position detection (SNDP) auto-addressing according to the bus shunt method (BSM).

The device performs the following steps in hardware, with the possibility to configure timing and effect reporting:

- Shunt voltage measurement
- Pull-up and current source configuration

Information about any errors as well as the success or failure of the SNPD must be accessible via register.

The decision whether the device is already addressed or not is based on a register flag that can only be modified by the user code.

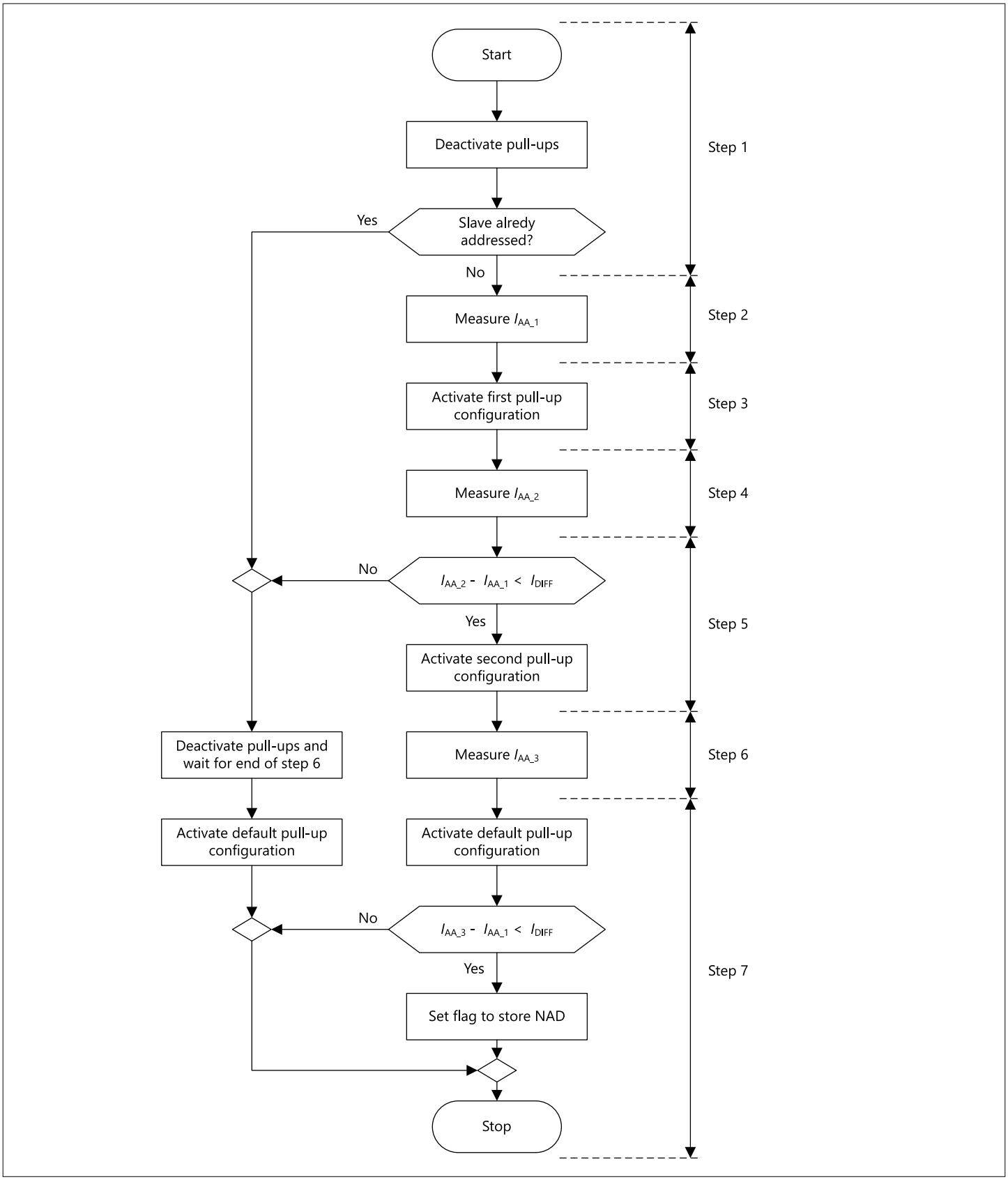

Figure 15 Bus shunt method flow chart

14.3 Electrical characteristics

Table 26 Electrical Characteristic

V_S = 5.5 V to 18 V, T_J = -40°C to +150°C, all voltages with respect to ground, positive currents flowing as described in Chapter 2 (unless otherwise specified). Typical values: V_S = 13.5 V, T_J = 25°C

Parameter	Symbol	Values			Unit	Note or condition	P-Number
		Min.	Typ.	Max.			
Bus receiver interface							
Receiver threshold voltage, recessive to dominant edge	V_{th_dom}	0.4 × V_S	0.45 × V_S	0.53 × V_S	V	SAE J2602	PRQ-644
Receiver dominant state	V_{BUS_DOM}	-27	–	0.4 × V_S	V	ISO 17987-4 (Param 17)	PRQ-645
Receiver threshold voltage, dominant to recessive edge	V_{th_rec}	0.47 × V_S	0.55 × V_S	0.6 × V_S	V	SAE J2602	PRQ-651
Receiver recessive state	V_{BUS_REC}	0.6 × V_S	–	1.15 × V_S	V	1) ISO 17987-4 (Param 18)	PRQ-652
Receiver center voltage	V_{BUS_CNT}	0.475 × V_S	0.5 × V_S	0.525 × V_S	V	2) ISO 17987-4 (Param 19)	PRQ-653
Receiver hysteresis	ΔV_{HYS}	0.07 × V_S	0.12 × V_S	0.175 × V_S	V	3) ISO 17987-4 (Param 20)	PRQ-654
Wake-up threshold voltage	V_{BUS_WK}	0.4 × V_S	0.5 × V_S	0.6 × V_S	V	–	PRQ-655
Bus transmitter interface							
Bus recessive output voltage	V_{BUS_RO}	0.8 × V_S	–	V_S	V	V_{TXD} = high level	PRQ-657
Bus dominant output voltage	V_{BUS_DO}	–	–	2.1	V	V_{TxD} = low level; R_{BUS} = 500 Ω; 10 V < V_S ≤ 18 V	PRQ-3095
Bus dominant output voltage low supply	V_{BUS_DO}	–	–	0.2 × V_S	V	V_{TxD} = low level; R_{BUS} = 500 Ω; 7.3 V ≤ V_S ≤ 10 V	PRQ-3094
Bus dominant output voltage deep supply	V_{BUS_DO}	–	–	0.2 × V_S	V	V_{TxD} = low level; R_{BUS} = 500 Ω; 5.5 V < V_S ≤ 7.3 V	PRQ-3096
Bus short circuit current	I_{BUS_LIM}	40	130	190	mA	Current limitation for driver dominant state; V_{BUS} ≤ 18 V; ISO 17987-4 (Param 12)	PRQ-658
Leakage current löoss of ground	$I_{BUS\_NO\_GND}$	-1000	-70	0	µA	V_S = 0 V; V_{BUS} = -12 V; ISO 17987-4 (Param 15)	PRQ-659

(table continues...)

Table 26 (continued) Electrical Characteristic

V_S = 5.5 V to 18 V, T_J = -40°C to +150°C, all voltages with respect to ground, positive currents flowing as described in Chapter 2 (unless otherwise specified). Typical values: V_S = 13.5 V, T_J = 25°C

Parameter	Symbol	Values			Unit	Note or condition	P-Number
		Min.	Typ.	Max.			
Leakage current loss of battery	$I_{BUS\_NO\_BAT}$	–	10	20	µA	V_S = 0 V; V_{BUS} = 18 V; ISO 17987-4 (Param 16)	PRQ-660
Leakage current driver off	$I_{BUS\_PAS\_dom}$	-1	–	–	mA	V_S = 18 V; V_{BUS} = 0 V; ISO 17987-4 (Param 13)	PRQ-661
Leakage current driver off	$I_{BUS\_PAS\_rec}$	–	–	20	µA	V_S = 8 V; V_{BUS} = 18 V; ISO 17987-4 (Param 14)	PRQ-662
Bus pull-up resistance	R_{SLAVE}	20	30	47	kΩ	Normal mode, also present in sleep mode; ISO 17987-4 (Param 26)	PRQ-663
Auto-addressing specifications							
Pull-up current source	I_{SNPD}	0	–	7.7	mA	Configurable via register	PRQ-797
Shunt resistor	R_{SHUNT}	0.4	0.7	1.0	Ω	–	PRQ-799
Timing							
TXD dominant time out	$t_{TXD\_LIN\_TO}$	20	25	30	ms	V_{TXD} = 0 V	PRQ-685
Dominant time for bus wake-up	t_{WK_BUS}	30	–	150	µs	4) Including analog and digital filter time. Digital filter time can be adjusted via register	PRQ-656
Dominant analog filter time for bus wake-up	$t_{WK\_BUS\_filter}$	3	–	15	µs	4) Analog filter time of transceiver. An additional digital filter is required to achieve the required wake-up time	PRQ-131
AC Characteristics							
Propagation delay bus dominant to RxD LOW	$t_{d(L)\_R}$	0.1	–	6	µs	4) C_L = 20 pF; ISO 17987-4 (Param 31)	PRQ-664
Propagation delay bus recessive to RxD HIGH	$t_{d(H)\_R}$	0.1	–	6	µs	4) ISO 17987-4 (Param 31)	PRQ-665
Receiver delay symmetry	t_{sym_R}	-2	–	2	µs	4) $t_{sym\_R} = t_{d(L)\_R} - t_{d(H)\_R}$; ISO 17987-4 (Param 32)	PRQ-666
AC Characteristics - Low battery supply							
Low ECU battery voltage input	$V_{battECU\_low}$	6.5	–	8	V	5) 4)	PRQ-2973

(table continues...)

Table 26 (continued) Electrical Characteristic

V_S = 5.5 V to 18 V, T_J = -40°C to +150°C, all voltages with respect to ground, positive currents flowing as described in Chapter 2 (unless otherwise specified). Typical values: V_S = 13.5 V, T_J = 25°C

Parameter	Symbol	Values			Unit	Note or condition	P-Number
		Min.	Typ.	Max.			
Low IC battery voltage input	V_{battIC_low}	5.5	–	7	V	–	PRQ-2974
Duty cycle D1 at low battery supply	n_{D1_low}	0.396	–	–	–	[6] Duty cycle 1 at low battery supply. $TH_{Rec(max)}$ = 0.665 × V_{battIC_low}; $TH_{Dom(max)}$ = 0.499 × V_{battIC_low}; V_{battIC_low} = 5.5 V to 7 V; t_{bit} = 50 µs;	PRQ-2975
Duty cycle D2 at low battery supply	n_{D2_low}	–	–	0.581	–	[6] Duty cycle 2 at low battery supply. $TH_{Rec(min)}$ = 0.496 × V_{battIC_low}; $TH_{Dom(max)}$ = 0.361 × V_{battIC_low}; V_{battIC_low} = 6.1 V to 7 V; t_{bit} = 50 µs;	PRQ-2976
Duty cycle D3 at low battery supply	n_{D3_low}	0.417	–	–	–	[6] Duty cycle 3 at low battery supply. $TH_{Rec(max)}$ = 0.665 × V_{battIC_low}; $TH_{Dom(max)}$ = 0.499 × V_{battIC_low}; V_{battIC_low} = 5.5 V to 7 V; t_{bit} = 96 µs;	PRQ-2977
Duty cycle D4 at low battery supply	n_{D4_low}	–	–	0.590	–	[6] Duty cycle 2 at low battery supply. $TH_{Rec(min)}$ = 0.496 × V_{battIC_low}; $TH_{Dom(max)}$ = 0.361 × V_{battIC_low}; V_{battIC_low} = 6.1 V to 7.6 V; t_{bit} = 96 µs;	PRQ-2978

(table continues...)

Table 26 (continued) Electrical Characteristic

V_S = 5.5 V to 18 V, T_J = -40°C to +150°C, all voltages with respect to ground, positive currents flowing as described in Chapter 2 (unless otherwise specified). Typical values: V_S = 13.5 V, T_J = 25°C

Parameter	Symbol	Values			Unit	Note or condition	P-Number
		Min.	Typ.	Max.			
AC Characteristics - Transceiver normal slope mode							
Duty cycle D1 normal slope mode (for worst case at 20 kbit/s)	n_{D1}	0.396	–	–	–	6) Duty cycle 1. $TH_{Rec(max)} = 0.744 \times V_S$; $TH_{Dom(max)} = 0.581 \times V_S$; t_{bit} = 50 µs; $n_{D1} = t_{bus\_rec(min)}/(2 \times t_{bit})$; ISO 17987-4 (Param 27)	PRQ-667
Duty cycle D2 normal slope mode (for worst case at 20 kbit/s)	n_{D2}	–	–	0.581	–	6) Duty cycle 2. $TH_{Rec(max)} = 0.422 \times V_S$; $TH_{Dom(max)} = 0.284 \times V_S$; t_{bit} = 50 µs; $n_{D2} = t_{bus\_rec(max)}/(2 \times t_{bit})$; ISO 17987-4 (Param 28)	PRQ-668
AC Characteristics - Flash mode							
Duty cycle D7 (for worst case at 115 kbit/s)	n_{D7}	0.399	–	–	–	6) Duty cycle 7. $TH_{Rec(max)} = 0.744 \times V_S$; $TH_{Dom(max)} = 0.581 \times V_S$; t_{bit} = 8.7 µs; V_S = 13.5 V; $n_{D7} = t_{bus\_rec(min)}/(2 \times t_{bit})$	PRQ-682
Duty cycle D8 (for worst case at 115 kbit/s)	n_{D8}	–	–	0.578	–	6) Duty cycle 8. $TH_{Rec(max)} = 0.422 \times V_S$; $TH_{Dom(max)} = 0.284 \times V_S$; t_{bit} = 8.7 µs; V_S = 13.5 V; $n_{D8} = t_{bus\_rec(max)}/(2 \times t_{bit})$	PRQ-683
LIN input capacitance	C_{BUS}	–	15	30	pF	4)	PRQ-684
Protection							
Thermal shutdown temperature	$T_{J\_SD\_LIN}$	165	175	200	°C	4)	PRQ-686
Thermal shutdown hysteresis	$\Delta T_{J\_SD\_LIN}$	5	10	15	K	4)	PRQ-687

1) Maximum limit specified by design
2) $V_{BUS\_CNT} = (V_{th\_dom} + V_{th\_rec})/2$
3) $V_{HYS} = V_{th\_rec} - V_{th\_dom}$
4) Specified by design, not subject to production test
5) $V_{battECU}$ is measured at the ECU input power pins. All voltages are referenced to the local ECU ground
6) Bus load concerning LIN Spec 2.2 (C_{BUS}; R_{BUS}):
   Load 1 = 1 nF; 1 kΩ
   Load 2 = 6.8 nF; 660 Ω

Load 3 = 10 nF; 500 Ω

Note: The voltages and currents listed in above table apply to both V_{BUS_M}, V_{BUS_S} and I_{BUS_M}, I_{BUS_S} as shown in Figure 3.

15 Timer2

- 16-bit auto-reload mode
  - Selectable up or down counting
- One channel 16-bit capture mode
- Baud-rate generator for UART

The timer modules are general purpose 16-bit timer. Timer 2 can function as a timer or counter in each of its modes.

The timer module supports LIN autobaud detection by using pin LIN_M as an input for edge detection.

Table 27 Timer2 modes

Mode	Description
Auto-reload up	**Up/down count disabled** • Count up only • Start counting from 16-bit reload value, overflow at $FFFF_{16}$ • Reload event configurable for trigger by overflow condition only, or by negative/positive edge at input pin LIN_M as well • Programmable reload value in register • Interrupt is generated with reload events

Auto-reload up/down	**Up/down count enabled**
	• Count up or down, direction determined by level at input pin LIN_M
	• No interrupt is generated
	• Count up
	  - Start counting from 16-bit reload value, overflow at $FFFF_{16}$
	  - Reload event configurable for trigger by overflow condition
	  - Programmable reload value in register
	• Count down
	  - Start counting from $FFFF_{16}$, underflow at value defined in register
	  - Reload event configurable for trigger by underflow condition
	  - Reload value fixed at $FFFF_{16}$

Channel capture	• Count up only • Start counting from 0000_{16}, overflow at $FFFF_{16}$ • Reload event triggered by overflow condition • Reload value fixed at 0000_{16} • Capture event triggered by falling/rising adge at input pin LIN_M • Captured timer value stored in register • Interrupt is generated with reload or capture event

16 Package dimensions

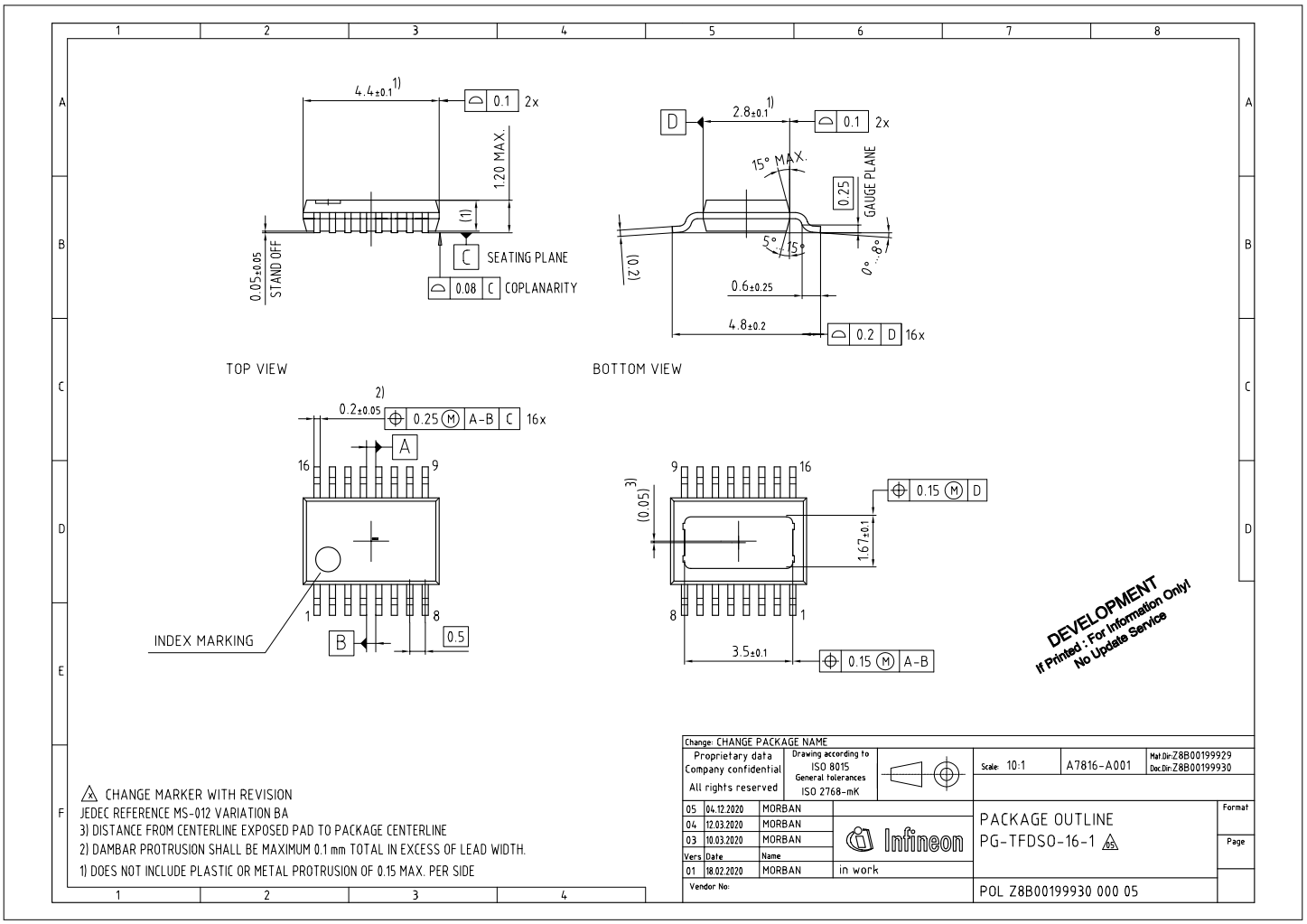

Figure 16 PG-TFDSO-16 package outline

tbd

Figure 17 PG-TFDSO-16 package pads and stencil

Note: ***Green product (RoHS compliant)***

To meet the world-wide customer requirements for environmentally friendly products and to be compliant with government regulations the device is available as a green product. Green products are RoHS-Compliant (i.e. Pb-free finish on leads and suitable for Pb-free soldering according to IPC/JEDEC J-STD-020).
For further information on packages, please visit our website: https://www.infineon.com/packages

17 Revision history

Table 28 Revision history

Document version	Date of release	Description of changes
Rev.0.06	2022-11-27	• Editorial and layout changes • Added family name • Changes Pin descriptions • Rework Power management unit chapter • Rework of System control unit chapter • Rework of Clock sources chapter • Rework of Microcontroller subsystem chapter • Moved Chapter Memory system to new chapter • Added description text to Chapter Output state protection in Power stages • Rework of Auto-addressing in Chapter LIN transceiver
Rev.0.06	2022-11-27	• PRQ-897: Updated min • PRQ-2890: Updated Typ. Max and note • PRQ-480: Updated Typ. and note • PRQ:2893: Updated Typ., Max and note • PRQ: 2894: Updated Typ. and note • PRQ-2471: Updated Parameter description, Max. and note • PRQ-147: Note or condition is removed • PRQ-645: Updated note • PRQ-652: Updated note • PRQ-653: Updated note • PRQ-654: Updated note • PRQ-658: Updated note • PRQ-659: Updated note • PRQ-660: Updated note • PRQ-661: Updated note • PRQ-662: Updated note • PRQ-663: Updated note • PRQ-664: Updated note • PRQ-665: Updated note • PRQ-666: Updated note • PRQ-2471: Updated Max. and note • PRQ-147: Updated note • PRQ-389: Updated Min., Typ. and Max. • PRQ-391: Updated Min., Typ. and Max. • PRQ-797: Updated Min., Max and note • PRQ-799: Updated Min. Typ and Max.

(table continues...)

Table 28 (continued) Revision history

Document version	Date of release	Description of changes
Rev.0.06	2022-11-27	**Added:** PRQ-2890; PRQ-3103; PRQ-2971; PRQ-3119; PRQ-3143 PRQ-3095; PRQ-3094; PRQ-3096; PRQ-164; PRQ-2897; PRQ-2898; PRQ-2900; PRQ-2901; PRQ-2903; PRQ-2904; PRQ-2906; PRQ-3132 **Deleted:** PRQ-2321; PRQ-2315, PRQ-2475; PRQ-2341; PRQ-312; PRQ-2339; PRQ-2453; PRQ-2827; PRQ-2829; PRQ-371; PRQ-2337; PRQ-2794; PRQ-2788; PRQ-1132; PRQ-672; PRQ-673; PRQ-677; PRQ-678: PRQ-2473; PRQ-2314; PRQ-2314; PRQ-2326
Rev.0.05	2021-10-14	Description • Changed EEPROM to 1000TP memory • Changed DTS resolution from 8 to 10 bit • Changed nominal load current from 50 to 51.5 mA in table 1 Chapter 1 - Block diagram and terms • Updated figure 1 Chapter 2 - Pin configuration • Changed device pinout in figure 5 and table 2 Chapter 3 - General product characteristics • Changed PRQ-495 in table 3 • Changed PRQ-532 in table 4 • Removed PRQ-164 in table 4 Chapter 4 - Power management unit (PMU) • Moved PRQ-482 to chapter 6 • Added PRQ-2871, PRQ-2872 to table 11 • Added PRQ-2853 to table 12 • Added PRQ-2891, PRQ-2893, PRQ-2894 to table 13 • Moved PRQ-482 to table 18 in chapter 6 • Removed PRQ-2478 • Added PRQ-2953 to table 14

(table continues...)

Table 28 (continued) Revision history

Document version	Date of release	Description of changes
Rev.0.05	2021-10-14	Chapter 5 - System control unit (SCU) • Updated chapter 5.1 • Removed PRQ-1106 in table 17 • Changed symbol of PRQ-2453, PRQ-2337 • Moved PRQ-2337 to table 18 in chapter 6 Chapter 6 - Clock sources • Added chapter 6 • Added PRQ-2827, PRQ-2828, PRQ-2829, PRQ-2794, PRQ-2788 to table 18 Chapter 7 - Microcontroller subsystem (MCU) • Added PRQ-2810, PRQ-2811, PRQ-2813 to table 19 • Changed symbol of PRQ-141, PRQ-147 in table 19 • Removed PRQ-646 and replaced with PRQ-149 in table 19 Chapter 9 - Measurement unit • Changed chapter 9.4 LED forward voltage measurement • Updated figure 7 in chapter 9.4 • Changed Min. value of PRQ-924 in table 21 • Changed Min., Max. value of PRQ-913 in table 21 • Removed PRQ-956, PRQ-914 in table 21 Chapter 10 - Power stage • Replaced table 16 with formula 2 in chapter 10 • Changed chapter 10.1 PWM Generator • Updated formula 3 in chapter 10.1 • Added PRQ-2796, PRQ-2979 in table 23 Chapter 11 - LIN transceiver • Added PRQ-2973, PRQ-2974, PRQ_2975, PRQ-2976, PRQ-2977, PRQ-2978 to table 25
Rev.0.04	2021-02-22	Titlepage • Changed Arm® Cortex® CPU core from M0+ to M23 • Added package suffix ET to product name Chapter 1 - Block diagram and terms • Changed Arm® Cortex® CPU core from M0+ to M23 in figure 2 • Added package suffix ET to product name in figure 2 caption and figure 3 Chapter 2 - Pin configuration • Changed device pinout in figure 5 and table 2

(table continues...)

Table 28 (continued) Revision history

Document version	Date of release	Description of changes
Rev.0.04	2021-02-22	Chapter 4 - Power management unit (PMU) • Added chapter 4.1 Master clock generation • Renamed Reset operating mode to Unsupplied in chapter 4.2 PMU mode overview • Updated power mode descriptions in chapter 4.2 PMU mode overview • Updated table 7 in chapter 4.4 Power mode transitions • Removed Duration column of table 8 in chapter 4.3 Power mode transitions • Updated condition for e_sleep2startup, e_failsleep2startup in table 8 • Moved wake-up management to chapter 4.4 Wake-up management • Updated and moved watchdog timer description, chapter 7 in Rev.0.03, to chapter 4.5 • Added PRQ-2478, PRQ-2474, PRQ-2314, PRQ-2316, PRQ-2315, PRQ-2475, PRQ-2318, PRQ-2473, PRQ-2326, PRQ-2321, PRQ-2310, PRQ-2311 to table 11 • Removed PRQ-483, PRQ-836, PRQ-834, PRQ-940, PRQ-837, PRQ-838, PRQ-839 from table 11 Chapter 5 - System control unit (SCU) • Added chapter 5.1, 5.2 and 5.3 • Updated PRQ-312, PRQ-1106 in table 12 • Added PRQ-2471, PRQ-2341, PRQ-2339, PRQ-2337, PRQ-2453, PRQ-2347 to table 12 Chapter 6 - Microcontroller subsystem (MCU) • Changed Arm® Cortex® CPU core from M0+ to M23 and updated description in chapter 6.1 • Added chapter 6.2.1, 6.2.2, 6.2.3 • Renamed PRQ-140 from SysROM to BROM and updated parameter symbol in table 13 Chapter 8 - Measurement unit • Added configurable gain description to chapter 8.5 • Removed note from PRQ-900 in table 15 • Added PRQ-2512, PRQ-2513 to table 15 Chapter 9 - Power stage • Changed current configuration from 4 bit to 5 bit • Updated table 16 • Updated note field of PRQ-367, PRQ-369, PRQ-372, PRQ-376, PRQ-385, PRQ-393, PRQ-387, PRQ-395, PRQ-389, PRQ-391
Rev.0.03	2020-10-06	Initial target datasheet

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