# Signal conditioning IC for directly driven ultrasonic sensors — E524.05 / E524.06

PRODUCTION DATA – Apr 27, 2015

RoHS compliant

## Features

- Transformerless direct transducer driver
- Programmable transducer frequencies between 38kHz and 72kHz
- Bi-directional interface in 2-wire & 3-wire variants
- Supply voltage independent performance
- Optimized short & long range performance by:
  - active and passive damping mechanisms
  - sensitivity time control
  - optional automatic threshold generation
- Fully integrated digital signal conditioning
- Programmable transducer voltage & burst length
- Programmable receiver amplifier gain
- Digital envelope and threshold readout via test mode
- Transducer diagnosis information
- Embedded EEPROM for calibration data
- Chip ID for traceability

## Applications

- Ultrasonic park assist systems (USPA, PAS,...)
- Industrial distance measuring
- Robotics

## Ordering Information

| *Product ID* | *Temp. Range* | *Interface* | *Package* |
|---|---|---|---|
| E524.05 | -40°C to +105°C | 2-wire | QFN20L4 |
| E524.06 | -40°C to +105°C | 3-wire | QFN20L4 |

## General Description

The device builds the core for a robust and easy-to-handle distance measurement system, while offering flexibility for customer applications.

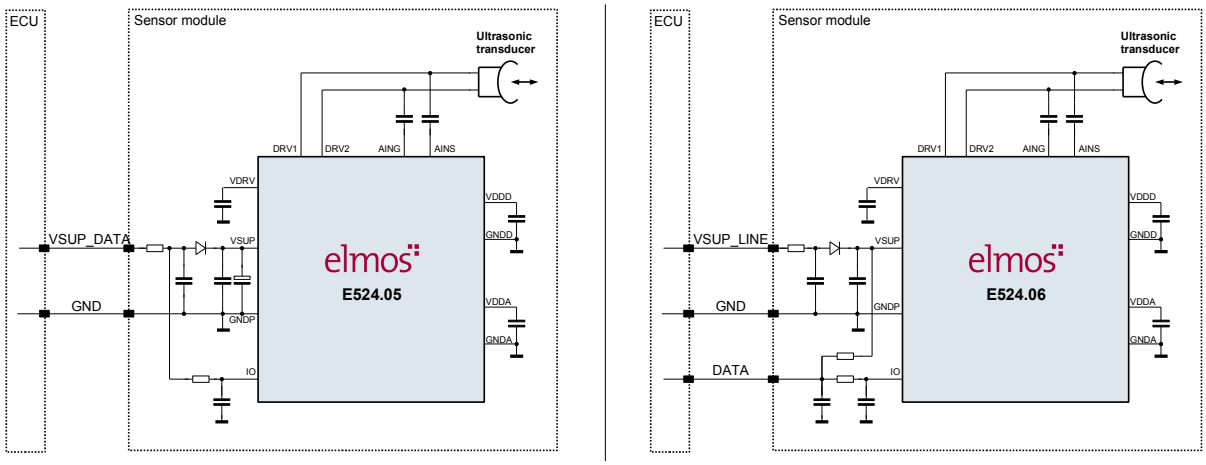
A driver unit stimulates the direct connected ultrasonic transducer. Driver frequency, transducer voltage, burst length, amplifier gain and other parameters are user configurable. Active and passive damping mechanisms combined with STC (Sensitivity Time Control) optimize short and long range performance.

The received echo signal is amplified, converted and digitally processed. Customized obstacle interpretation is feasible by a variable detection threshold. In SEND Mode the circuit triggers the ultrasonic transducer while in RECEIVE ONLY Mode only indirect echo signals are detected.

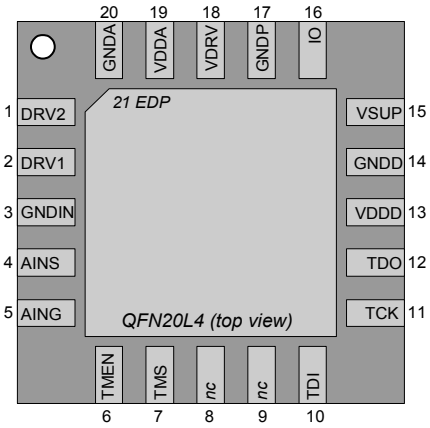
Application relevant settings can be stored in EEPROM during an End-Of-Line calibration by the customer. For evaluation and debugging purposes, envelope and threshold data can be read out via test mode.

Communication with the control unit is possible via 2-wire or 3-wire configuration. The E524.05 supports a bi-directional communication via data modulation on the supply line. The E524.06 supports a dedicated IO-line for data transfer.

## Typical Application Circuit



## Pin Configuration

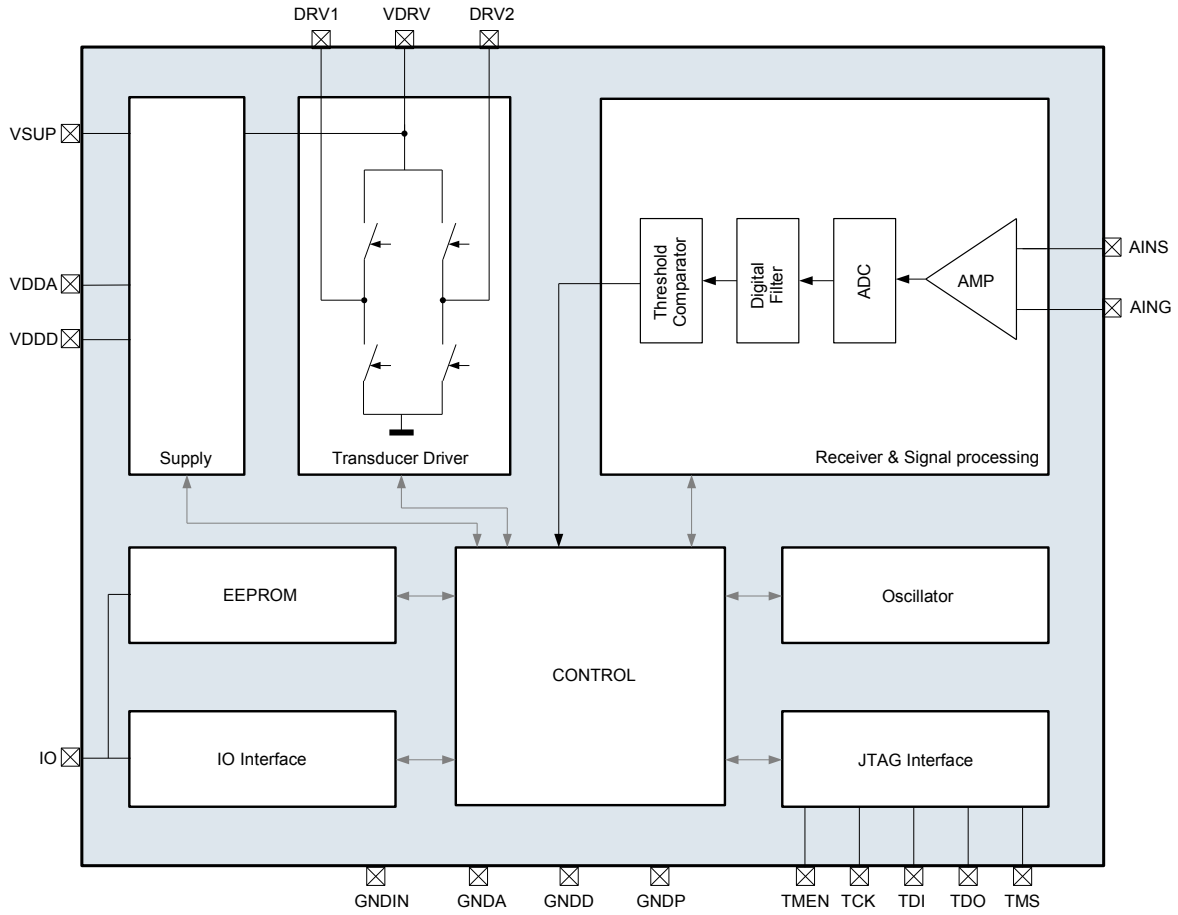



## Pin Description

| *No* | *Name* | *Type* | *Description* |
|---|---|---|---|
| 1 | DRV2 | HV_A_IO | Driver output 2, has to be connected to transducer-GND |
| 2 | DRV1 | HV_A_IO | Driver output 1 |
| 3 | GNDIN | S | Analog ground for optimized EMC performance |
| 4 | AINS | A_I | Positive signal input |
| 5 | AING | A_I | Negative signal input |
| 6 | TMEN | D_I | Test mode enable |
| 7 | TMS | D_I | JTAG test mode select |
| 8 | nc | | not connected to device, should be connected to PCB-GND |
| 9 | nc | | not connected to device, should be connected to PCB-GND |
| 10 | TDI | D_I | JTAG data input |
| 11 | TCK | D_I | JTAG clock |
| 12 | TDO | D_O | JTAG data output |
| 13 | VDDD | A_O | Internal digital supply voltage |
| 14 | GNDD | S | Digital ground |
| 15 | VSUP | S | Supply voltage |
| 16 | IO | HV_A_IO | Bidirectional interface |
| 17 | GNDP | S | Power ground |
| 18 | VDRV | S | Transducer driver output voltage |
| 19 | VDDA | A_O | Internal analog supply voltage |
| 20 | GNDA | S | Analog ground |
| 21 | EDP | | Exposed die pad, has to be connected to PCB-GND |

Explanation of Types:
A = Analog, D = Digital, S = Supply, I = Input, O = Output, B = Bidirectional, HV = High Voltage

# 1 Block Diagram



## 2 Absolute Maximum Ratings

Stresses beyond these absolute maximum ratings listed below may cause permanent damage to the device. **These are stress ratings only; operation of the device at these or any other conditions beyond those listed in the operational sections of this document is not implied.** Exposure to absolute maximum rated conditions for extended periods may affect device reliability. All voltages referred to GNDP. Currents flowing into terminals are positive, those drawn out of a terminal are negative.

| *No.* | *Description* | *Condition* | *Symbol* | *Min* | *Max* | *Unit* |
|---|---|---|---|---|---|---|
| 1 | Supply Voltage | | VSUP | -0.3 | 36 | V |
| 2 | Supply Voltage | t < 500 ms | VSUP | -0.3 | 40 | V |
| 3 | Voltage at pin IO | | $V_{IO}$ | -0.3 | 36 | V |
| 4 | Voltage at pin IO | t < 500 ms | $V_{IO}$ | -0.3 | 40 | V |
| 5 | Voltage at digital pins (TCK, TDO, TDI, TMS, TMEN) | | $V_D$ | -0.3 | 3.6 | V |
| 6 | Voltage at analog pins (AINS, AING) | | $V_A$ | -0.8 | 0.8 | V |
| 7 | Internal digital supply voltage | | VDDD | -0.3 | 3.6 | V |
| 8 | Internal analog supply voltage | | VDDA | -0.3 | 3.6 | V |
| 9 | Voltage at pins DRV1, DRV2 and VDRV | | $V_{DRV1}$, $V_{DRV2}$, VDRV | -0.3 | 16 | V |
| 10 | Ambient temperature | | $T_{AMB}$ | -40 | 105 | °C |
| 11 | Junction Temperature | | $T_J$ | -40 | 125 | °C |
| 12 | Storage Temperature | | $T_{STG}$ | -40 | 125 | °C |

# 3 ESD and Latchup

## 3.1 ESD Protection

| *No.* | *Description* | *Condition* | *Symbol* | *Min* | *Max* | *Unit* |
|---|---|---|---|---|---|---|
| 1 | ESD HBM at pin VSUP, IO[1)] | | $HBM_{VSUP, IO}$ | +/- 4 | | kV |
| 2 | ESD HBM at all other pins[1)] | | $HBM_{PINS\_OTHER}$ | +/- 2 | | kV |
| 3 | ESD CDM at pins near corners (Pins 1,5,6,10,11,15,16,20)[2)] | | $CDM_{PINS\_EDGE}$ | +/- 0.75 | | kV |
| 4 | ESD CDM at all other pins[2)] | | $CDM_{PINS\_OTHER}$ | +/- 0.5 | | kV |

[1)] According to AEC-Q100-002 (HBM) chip level test
[2)] According to AEC-Q100-011 (CDM) chip level test

## 3.2 Latch-up

Latch-up performance is validated according JEDEC standard JESD 78 in its valid revision.

# 4 Recommended Operating Conditions

- Parameters are guaranteed within the range of recommended operating conditions unless otherwise specified.
- The first electrical potential connected to the ASSP must be GND.
- In the operating range from $VSUP_{POR}$ ... 7V and 18V ... 36V function is guaranteed with limited parameters.

| *No.* | *Description* | *Condition* | *Symbol* | *Min* | *Typ* | *Max* | *Unit* |
|---|---|---|---|---|---|---|---|
| 1 | Supply Voltage | | VSUP | 7 | - | 18 | V |
| 2 | Programming voltage for EEPROM at pin IO | | $V_{IO}$ | 23 | 25 | 27 | V |
| 3 | DC Input Voltage | | AINS/AING | -0.8 | - | 0.8 | V |
| 4 | Input Current | | AINS/AING | -20 | - | 20 | mA |
| 5 | Operating Temperature Range | | $T_{OPR}$ | -40 | - | 105 | °C |

# 5 Electrical Characteristics

- $V_{VSUP}$ = +7V to +18V
- $T_{OPR}$=-40°C to + 105°C, unless otherwise noted.
- Typical values are at $V_{VSUP}$=12.0V and $T_{amb}$=+25°C.
- Positive currents flow into the device pins.

## 5.1 Supply and Power-On-Reset

| No. | Description | Condition | Symbol | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|---|
| 1 | Current consumption at VSUP | F_DRV_ADJ=$f_{DRV,ADJ}$, VDRV_CFG='1000', t>$t_{D\_nom}$ | $I_{VSUP}$ | - | 4 | - | mA |
| 2 | Worst case current consumption at VSUP | F_DRV_ADJ='11111111', VDRV_CFG='1111', t>$t_{D\_nom}$ | $I_{VSUP\_WC}$ | - | - | 7 | mA |
| 3 | Internal generated analog supply | external $C_{VDDA}$ connected | VDDA | 3.0 | 3.3 | 3.6 | V |
| 4 | Current out of VDDA in case of short to GND | | $I_{VDDA,SHORT}$ | -30 | - | - | mA |
| 5 | Internal generated digital supply | external $C_{VDDD}$ connected | VDDD | 3.0 | 3.3 | 3.6 | V |
| 6 | Current out of VDDD in case of short to GND | | $I_{VDDD,SHORT}$ | -85 | - | - | mA |
| 7 | Level at VSUP: threshold from operation mode to reset state | $I_{VDDD}$=-10mA | $VSUP_{POR}$ | - | - | 4.5 | V |
| 8 | Start-up time at VDRV for typical settings[1)] | VDRV_CFG='1000', $V_{DRV\_OK}$='1', $C_{DRV}$=2.2µF | $t_{D\_nom}$ | 10 | 15 | 25 | ms |
| 9 | Start-up time at VDRV for VSUP=7V ... 18V and VDRV_CFG=any[1)] | VDRV_CFG=any, $V_{DRV\_OK}$='1', $C_{DRV}$=2.2µF | $t_{D\_7V}$ | - | - | 45 | ms |
| 10 | Start-up time until communication via IO is possible[*)] | | $t_{D\_IO}$ | - | 60 | 450 | µs |

[*)] Not tested in production

[1)] Load conditions different for production test. Doubling $C_{DRV}$ results in doubling the start-up time.

### 5.1.1 Transducer driver output voltage

| No. | Description | Condition | Symbol | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|---|
| 1 | Driver supply voltage for typical setting | VDRV_CFG='1000' | VDRV | 10.5 | 11 | 11.5 | V |
| 2 | Driver supply voltage step size | | $VDRV_{STEP}$ | 0.3 | 0.5 | 0.7 | V |
| 3 | Minimum driver supply voltage | VDRV_CFG='0010' | $VDRV_{MIN}$ | 7.5 | 8 | 8.5 | V |
| 4 | Maximum driver supply voltage | VDRV_CFG='1111' | $VDRV_{MAX}$ | 13.9 | 14.5 | 15.1 | V |
| 5 | Number of steps | | $N_{VDRV}$ | - | 13 | - | |
| 6 | Driver supply voltage ok level, high | VDRV_CFG='1000' | $V_{DRV\_OK\_H}$ | 0.85 | 0.9 | 0.96 | VDRV |
| 7 | Driver supply voltage ok level, low | VDRV_CFG='1000' | $V_{DRV\_OK\_L}$ | 0.75 | 0.8 | 0.85 | VDRV |
| 8 | Short circuit current | | $I_{VDRV\_SHORT}$ | - | - | 12 | mA |

## 5.2 Transducer Driver

| No. | Description | Condition | Symbol | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|---|
| 1 | High-side driver On-Resistance at DRV1*) | common functional test of diode and $R_{ON\_HS\_DRV1}$ | $R_{ON\_HS\_DRV1}$ | - | 25 | - | Ω |
| 2 | High-side driver On-Resistance at DRV2 | | $R_{ON\_HS\_DRV2}$ | 10 | 25 | 50 | Ω |
| 3 | Low-side driver On-Resistance at DRV1*) | common functional test of diode and $R_{ON\_LS\_DRV1}$ | $R_{ON\_LS\_DRV1}$ | - | 50 | - | Ω |
| 4 | Low-side driver On-Resistance at DRV2 | | $R_{ON\_LS\_DRV2}$ | 15 | 50 | 100 | Ω |
| 5 | Damping resistance | | $R_D$ | 1.8 | 2.2 | 2.6 | kΩ |

*) Not tested in production

| No. | Description | Condition | Symbol | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|---|
| 1 | Driver output frequency adjustment range | to be adjusted by F_DRV_ADJ @ 25°C | $f_{DRV}$ | 38 | - | 72 | kHz |
| 2 | Step width of frequency adjustment | Temperature=25°C | $LSB_{f\_DRV}$ | 200 | 300 | 400 | Hz |
| 3 | Temp coefficient of driver output frequency*) | | $TC_{f\_DRV\_L}$ | - | -300 | - | ppm/K |
| 4 | Factory adjusted driver output frequency | Temperature=25°C | $f_{DRV,ADJ}$ | 57.00 | 58.00 | 59.00 | kHz |

*) Not tested in production

## 5.3 Receiving path

### 5.3.1 Analog Amplifier

| No. | Description | Condition | Symbol | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|---|
| 1 | Minimum gain | @ $f_{DRV}$=58 kHz | $G_{MIN}$ | 56 | 60 | 64 | dB |
| 2 | Maximum gain | @ $f_{DRV}$=58 kHz | $G_{MAX}$ | 79 | 83 | 87 | dB |
| 3 | Step size1) | @ $f_{DRV}$=58 kHz, (3) | $\Delta G_C$ | 0.25 | 0.742 | 1.25 | dB |
| 4 | Number of steps | | $N_G$ | - | 31 | - | |
| 5 | Input Impedance<br>AINS to GNDA<br>AING to GNDA | Temperature=25°C | $R_{IN}$ | 75 | 100 | 125 | kΩ |
| 6 | Noise Level*) | @ $f_{DRV}$=58 kHz | $e_N$ | - | 6.9 | - | $nV/\sqrt{Hz}$ |

*) Not tested in production

1) monotony guaranteed by design

### 5.3.2 Digital Filter

| No. | Description | Condition | Symbol | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|---|
| 1 | Center frequency | | $f_{c,filt}$ | - | 1 | - | $f_{DRV}$ |
| 2 | -3dB-Bandwidth | N_PULSES=any | BW,DFILT | - | 0.052 | - | $f_{DRV}$ |

#### 5.3.3 Sensitivity Time Control (STC)

| No. | Description | Condition | Symbol | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|---|
| 1 | Sum of digital STC gain, when off | STC_CFG='0' | $S_{G\_STC\_OFF}$ | - | 0 | - | dB |
| 2 | Sum of digital STC gain | STC_CFG='1' | $S_{G\_STC}$ | - | 12 | - | dB |
| 3 | Number of STC gain steps | STC_CFG='1' | $N_{STEP\_STC}$ | - | 16 | - | |
| 4 | Step durations | | $T_{STEP\_STC}$ | - | 17 | - | $1/f_{DRV}$ |
| 5 | Start of digital gain steps[1)] | | $T_{START\_STC}$ | - | 120 | - | $1/f_{DRV}$ |

[1)] Example: For $f_{DRV}$=58kHz: $T_{START\_STC}$=120*1/$f_{DRV}$=2.069ms

#### 5.3.4 Threshold comparator

| No. | Description | Condition | Symbol | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|---|
| 1 | Time, the comparator output is masked | COMP_MASK='1' | $T_{CMASK}$ | - | 16 | - | $1/f_{DRV}$ |

### 5.4 IO Interface

| No. | Description | Condition | Symbol | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|---|
| 1 | Voltage threshold for pin IO to detect low input signal | | $V_{IO\_IL}$ | 0.29 | 0.33 | 0.36 | VSUP |
| 2 | Voltage threshold for pin IO to detect high input signal | | $V_{IO\_IH}$ | 0.62 | 0.67 | 0.70 | VSUP |
| 3 | Voltage at pin IO to output low level at high current load | $I_{OUT}$ = 16mA [only 524.05] | $V_{IO\_OL,16}$ | - | - | 0.8 | V |
| 4 | Voltage at pin IO to output low level | $I_{OUT}$ = 4mA | $V_{IO\_OL,4}$ | - | - | 0.5 | V |
| 5 | Current limitation for pin IO | $V_{OUT}$ < 18V | $I_{IO\_LIMIT}$ | - | - | 60 | mA |

| No. | Description | Condition | Symbol | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|---|
| 1 | Slew Rate | | $SR_{VIO}$ | 1.0 | 1.7 | 3.0 | V/µs |
| 2 | Input debouncer | | $T_{DEB}$ | 0 | - | 1 | $1/f_{DRV}$ |
| 3 | IO high phase after $T_{CMD}$ | | $T_D$ | 1.08 | 3 | 4.42 | $1/f_{DRV}$ |
| 4 | IO low phase for send request | | $T_{SND}$ | 4.5 | 6 | 8.92 | $1/f_{DRV}$ |
| 5 | IO low phase for receive request | | $T_{REC}$ | 9 | 12 | 14.92 | $1/f_{DRV}$ |
| 6 | IO low phase to enter command mode | | $T_{CMD}$ | 15 | 20 | 24.92 | $1/f_{DRV}$ |
| 7 | Setup time for $V_{PROG}$ | | $T_{VPROG}$ | - | - | 265 | $1/f_{DRV}$ |
| 8 | Programming time | | $T_{PROG}$ | 1000 | 1100 | - | $1/f_{DRV}$ |
| 9 | Bit length, ECU to sensor module | | $T_{BIT\_WR}$ | 9 | 12 | 14.92 | $1/f_{DRV}$ |
| 10 | IO low phase for a logical '0', ECU to sensor module | | $T_{BIT0\_WR}$ | 4.5 | 6 | 8.92 | $1/f_{DRV}$ |
| 11 | IO low phase for a logical '1', ECU to sensor module | | $T_{BIT1\_WR}$ | 1.08 | 3 | 4.42 | $1/f_{DRV}$ |
| 12 | Bit length, sensor module to ECU | | $T_{BIT}$ | - | 12 | - | $1/f_{DRV}$ |
| 13 | IO low phase for a logical '0', sensor module to ECU | | $T_{BIT0}$ | - | 6 | - | $1/f_{DRV}$ |

| No. | Description | Condition | Symbol | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|---|
| 14 | IO low phase for a logical '1', sensor module to ECU[1)] | | $T_{BIT1}$ | - | 3 | - | $1/f_{DRV}$ |
| 15 | Devouncing of echo signal | | $T_{DEB\_ECHO}$ | - | 4 | - | $1/f_{DRV}$ |
| 16 | Pulse width echo event in 2 wire mode | [only 524.05] | $T_{ECHO2WIRE}$ | - | 3 | - | $1/f_{DRV}$ |
| 17 | Pulse width low frequency calibration pulse | | $T_{CAL}$ | - | 288 | - | $1/f_{DRV}$ |
| 18 | Pulse width of calibration pulses | | $T_{CALS}$ | - | 6 | - | $1/f_{DRV}$ |

[1)] Example: For $f_{DRV}$=58kHz, $T_{BIT1}$=3*1/$f_{DRV}$=51.72us

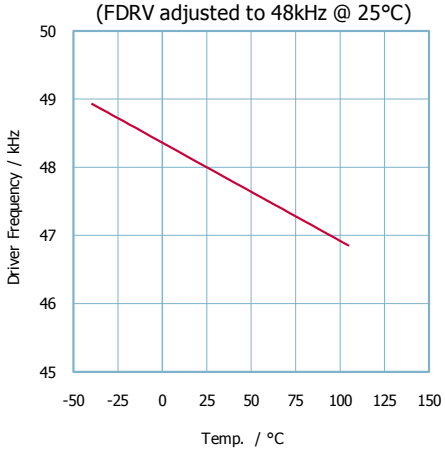
### 5.4.1 EEPROM Programming

#### 5.4.1.1 EEPROM delivery state

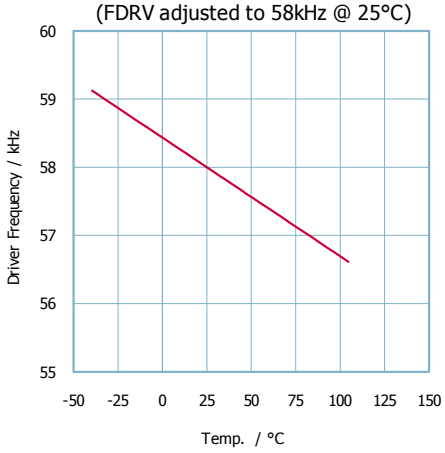
| No. | Description | Condition | Symbol | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|---|
| 1 | Amplifier gain adjustment | | AMP_GAIN | 16 | | 16 | |
| 2 | Transducer driver output voltage configuration | | VDRV_CFG | 8 | | 8 | |
| 3 | Driver frequency | calibrated to $f_{DRV}=f_{DRV,ADJ}$ | F_DRV_ADJ | 0 | | 191 | |
| 4 | Number of burst pulses | | N_PULSES | 1 | | 1 | |
| 5 | Electronic damping setting | | EL_DAMP | 0 | | 0 | |
| 6 | Damping resistor | | RD_CFG | 1 | | 1 | |
| 7 | Comparator masking on IO line | | COMP_MASK | 0 | | 0 | |
| 8 | Automatic threshold generation | | ATG_CFG | 0 | | 0 | |
| 9 | Noise strategy | | NOISE_CFG | 3 | | 3 | |
| 10 | Free configurable by customer | | CUSTOMER BITS | 0 | | 0 | |

# 6 Typical Operating Characteristics

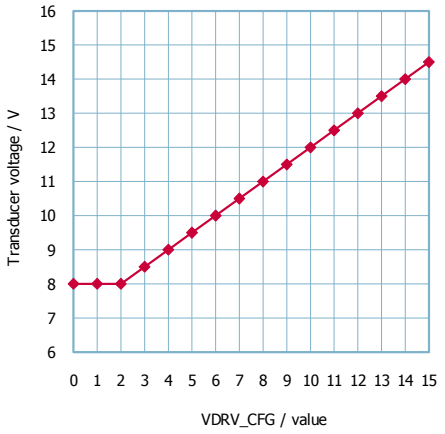
Driver Frequency vs. Temperature
(FDRV adjusted to 48kHz @ 25°C)



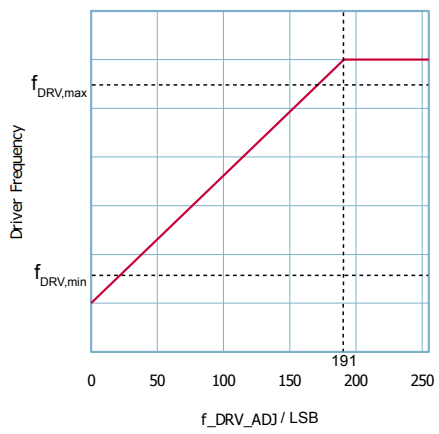

Driver Frequency vs. Temperature
(FDRV adjusted to 58kHz @ 25°C)




Transducer voltage vs. VDRV_CFG




Driver Frequency vs. F_DRV_ADJ



# 7 Functional Description

## 7.1 Overview

The principle of ultrasonic distance measuring is based on transmitting a pulse and measuring the reflection time of the received pulse as shown in Figure 7.1-1. The relationship between the distance from the transducer to the object L and the time T it takes to receive the echo is L = C * T/2, where C is the velocity of sound. The IC requires only one transducer, which acts as a transmitter and receives the reflected pulse with a time delay. The time delay is proportional to the distance to measure.

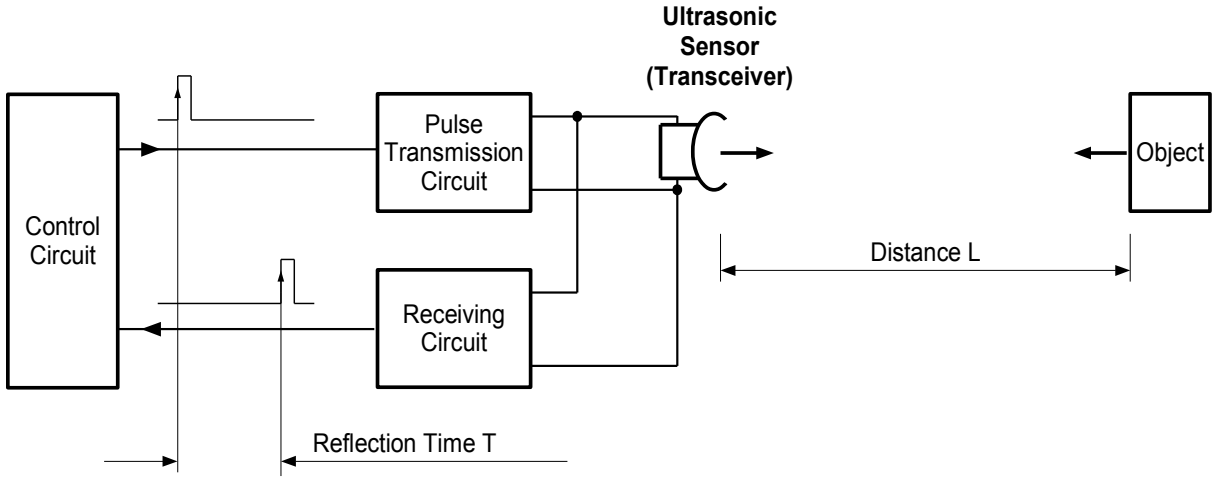



*Figure 7.1-1: Ultrasonic distance measuring*

A measurement is started by a 'SEND' or 'RECEIVE' request by the control unit (ECU). Internal logic generates a burst for the transducer first. Incoming reflected pulses are digitally filtered and compared to programmed threshold levels or to the automatically generated threshold. If the echo pulse exceeds the set threshold level, the comparator is triggered. In SEND / RECEIVE mode, the comparator output drives the single IO pin. The time elapsed from sending out a burst signal to receiving an echo signal from an object is proportional to the distance of the object.

| **E524.05** | **E524.06** |
|---|---|
| The E524.05 requires only two wires for the communication of ultrasonic module and ECU: Ground (GND) and the supply wire (VSUP_DATA). As illustrated in Figure 8.1-1, bidirectional data travels between ultrasonic module and ECU by modulating voltage on the supply wire. | The E524.06 requires three wires to communicate from the ultrasonic module with the ECU. As shown in Figure 8.3-1, the three wires are ground (GND), supply (VSUP) and one signal line (DATA). |

## 7.2 Supply and Power-On-Reset

The IC uses two internal regulators (VDDA and VDDD) as supplies for the internal circuits. An additional regulator generates a stable driver voltage (VDRV) over the complete supply voltage range (VSUP). The relationship of the power supplies is shown in Figure 7.2-1.

For recommended values of the used capacitors see chapter 8.2 or 8.4.

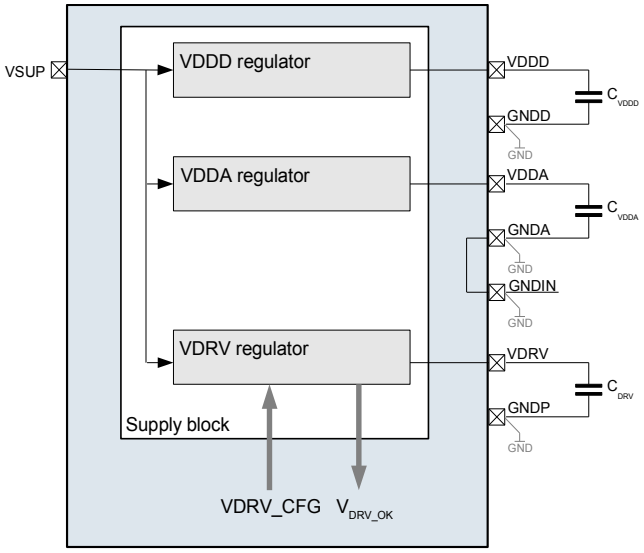



*Figure 7.2-1: Supply block*

### 7.2.1 Analog supply

The analog supply VDDA requires an external blocking capacitor $C_{VDDA}$. It is recommended to place the external capacitor as close as possible to the related pins VDDA and GNDA. VDDA is not intended to supply any external components. In case VDDA is shorted to GND, the output current will be limited to $I_{VDDA,SHORT}$.

An additional analog ground GNDIN is for an improved application EMC behavior. It is internally connected to the GNDA.

### 7.2.2 Digital supply

The digital supply VDDD requires an external blocking capacitor $C_{VDDD}$. It is recommended to place the external capacitor as close as possible to the related pins VDDD and GNDD. In case VDDD is shorted to GND, the output current will be limited to $I_{VDDD,SHORT}$.

VDDD is not intended to supply any external components.

### 7.2.3 Driver supply

The driver supply VDRV requires an external buffer capacitor $C_{DRV}$. It is recommended to place the external capacitor as close as possible to the related pins VDRV and GNDP. This capacitor stores the energy needed during an ultrasonic burst. VDRV is not intended to supply any external components except the transducer.

### 7.2.4 Power up sequence

The IC begins to power up once an external voltage is supplied to the pin VSUP. A power-up diagram is shown in Figure 7.2.4-1. The sequence can be described as follows:

1. An external supply voltage is supplied to pin VSUP.
2. After the Power-on-reset (POR) signal to the digital part is released, the digital part is running and communication via the interface is possible. The receiver path is enabled to receive signals.
3. READ_STATUS bit6 of the VDRV regulator goes high and the transducer driver can be switched on. The start-up time $t_{D\_nom}$ depends on the supply voltage VSUP, the VDRV regulator output voltage (set by VDRV_CFG) and on the external capacitor $C_{DRV}$. Doubling $C_{DRV}$ results in doubling the start-up time.

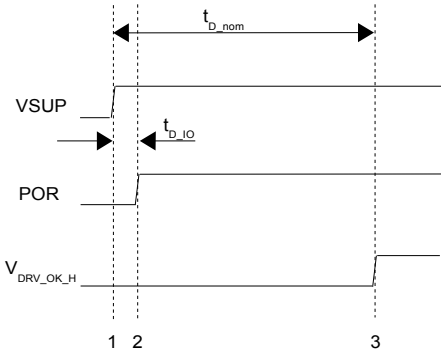



*Figure 7.2.4-1: Power up sequence*

For typical and maximum $C_{DRV}$ (2.2µF and 4.7µF) as well as typical and worst case $V_{VSUP}$ (12V,18V and 7V) the following figure shows the start-up time over VDRV:

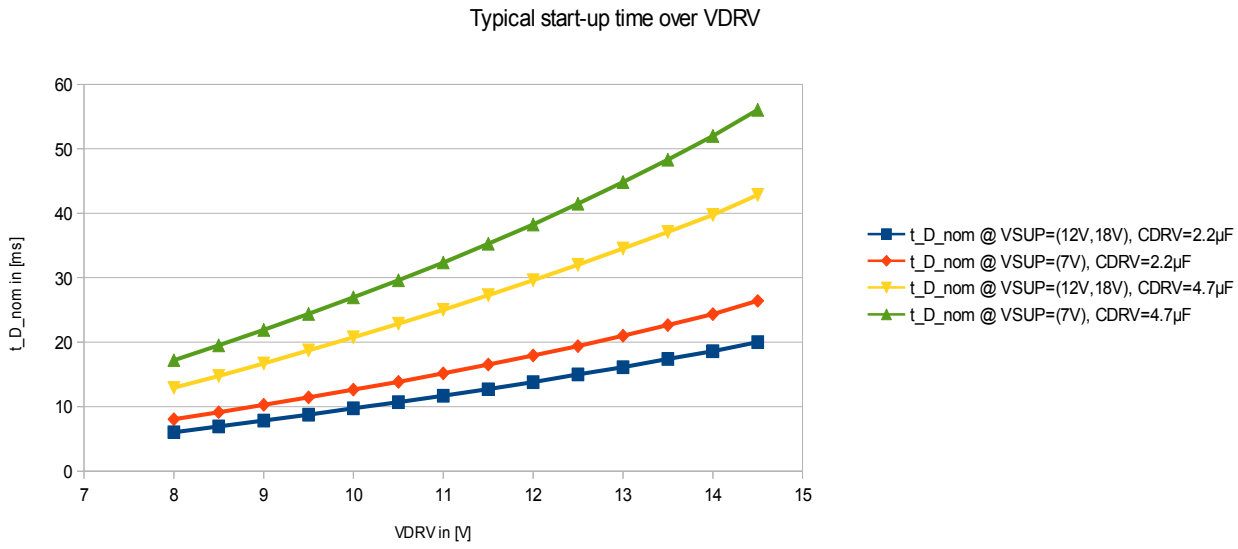



*Figure 7.2.4-2: Typical start-up time over VRDV*

### 7.2.5 Limited performance between $VSUP_{min}$ and $VSUP_{POR}$

The digital part is running, when the power-on-reset is high. When the power-on-reset goes from high to low state, the digital part is in reset state. This results in full functionality down to $VSUP_{min}$ and a still working digital part down to $VSUP_{POR}$. Between $VSUP_{min}$ and $VSUP_{POR}$ the performance is limited, but communication with the control unit is still possible.

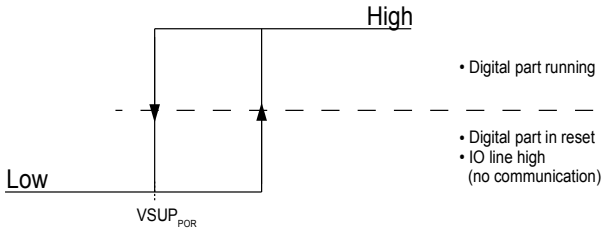



*Figure 7.2.5-1: Power-on-reset functionality*

## 7.3 Transducer Driver

When the transducer driver is activated by the 'SEND', 'SEND4', 'SEND8', 'SEND12', 'SEND24' or 'SEND_WO_DAMP' command, the pins DRV1 and DRV2 are tied towards ground and $V_{DRV}$ respectively by internal switches alternately with the driver output frequency $f_{DRV}$.

Transducer-GND has to be connected to DRV2.

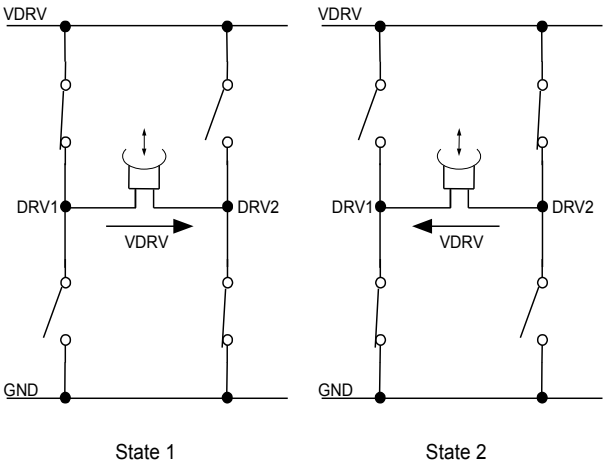



*Figure 7.3-1: Simplified transducer excitation*

The driver can be adjusted to the transducer by performing the following steps.

1. Adjust the driver frequency (F_DRV_ADJ)
2. Select the number of burst pulses (N_PULSES)
3. Adjust the transducer voltage (VDRV_CFG)
4. Adjust the electronic damping (EL_DAMP)

For further details of EEPROM programming functions refer to Table 7.5.10-1.

During receiving DRV2 is directly tied to GND and DRV1 is tied to GND via two antiparallel diodes.

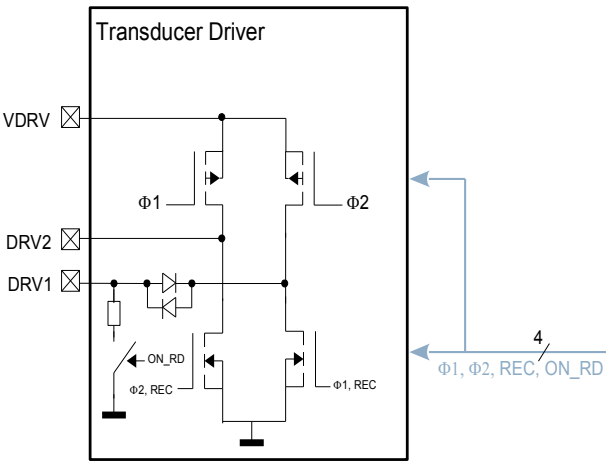



*Figure 7.3-2: Transducer full bridge*

An internal damping resistor is used to decrease the ringing time, which results in an optimized short distance. The damping resistor is switched on during ringing, but switched off during sending the burst and echo detection. The value depends on the electrical parameters of the transducer and is set to a typical value.

If the damping resistor is not used at all (e.g. when using an application with an inductance) it can be switched off by RD_CFG.

#### 7.3.1 Transducer driver frequency

The frequency $f_{DRV}$ can be adjusted by the EEPROM bits F_DRV_ADJ. The guaranteed adjustment range is defined by $f_{DRV,MIN}$ and $f_{DRV,MAX}$. The typical step width is defined as $LSB_{f\_DRV,typ}$. The frequency is strictly monotonic increasing with increasing value of F_DRV_ADJ. Before delivery the frequency is adjusted to $f_{DRV,ADJ}$. The setting F_DRV_ADJ=0 corresponds to the minimum frequency that might be much lower than $f_{DRV,MIN}$.

The frequency can be measured with the 'CAL_PULSES' command.

The procedure for adjusting the frequency should be as following:
1. Read the actual value of F_DRV_ADJ
2. Measure the actual frequency
3. Calculate the difference $f_{DIFF}$=target frequency-actual frequency
4. Calculate the rough number n of steps corresponding to $f_{DIFF}$ by $n=f_{DIFF}/LSB_{f\_DRV,typ}$
5. Adjust F_DRV_ADJ by n
6. Repeat until the target frequency is reached
7. Store the setting for F_DRV_ADJ by EE-Programming command ('EE_WRITE' impacts only the output of the Driver Frequency Calibration command, for all other frequency related functions (e.g. driver output frequency, communication timing), the new setting of F_DRV_ADJ will be activated after EE_PROGRAM command only)

**Remark:** The timing for communication is based on $f_{DRV}$, thus activating another $f_{DRV}$ by 'EE_PROGRAM' changes the timing for communication.

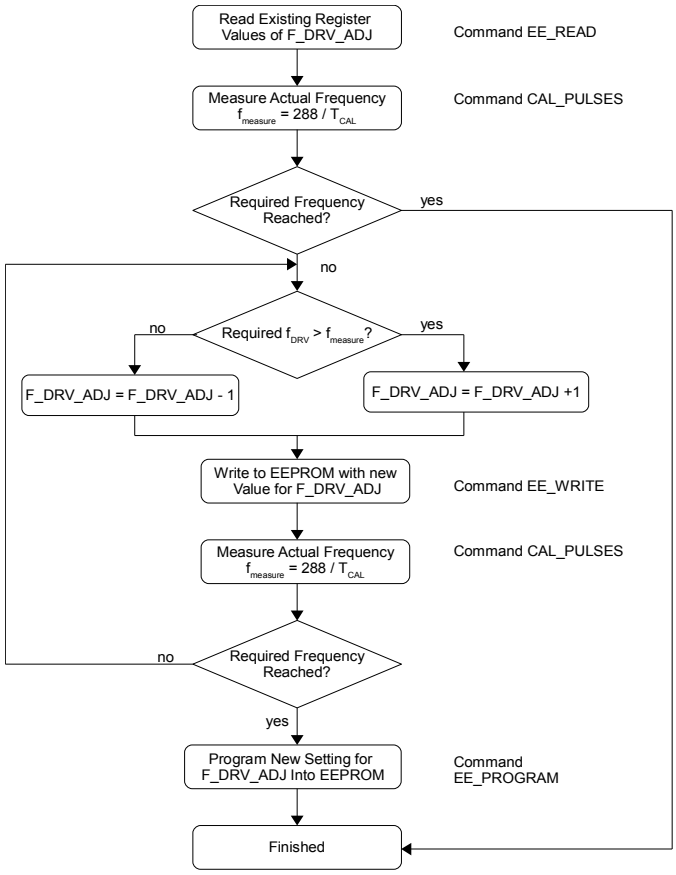



*Figure 7.3.1-1: Flow chart of frequency adjustment*

### 7.3.2 Number of burst pulses

The number of burst pulses is defined by the EEPROM setting N_PULSES. In general a burst with 10 pulses has a better performance in the short range while a burst with 16 pulses has a better performance in the long range.
For most transducers with low driving frequencies (40-48kHz) it is recommended to use 10 pulses and for transducer with higher frequencies (58kHz) it is recommended to use 16 pulses.

Additional commands 'SEND4', 'SEND8', 'SEND12', 'SEND24' can be used to send a burst with different number of pulses other than programmed with N_PULSES.

### 7.3.3 Transducer voltage

The voltage over the transducer is defined by the regulator output voltage VDRV and can be adjusted from $VDRV_{MIN}$ to $VDRV_{MAX}$ in $VDRV_{STEP}$ steps by configuring VDRV_CFG. This configuration can be used to adjust the sound pressure level of the transducer.

Table 7.3.3-1: VDRV for different VDRV_CFG

| *VDRV_CFG* | *Driver voltage VDRV* |
|---|---|
| 0000, 0001, 0010 | 8.0V |
| 0011 | 8.5V |
| 0100 | 9.0V |
| 0101 | 9.5V |
| 0110 | 10.0V |
| 0111 | 10.5V |
| 1000 | 11.0V |
| 1001 | 11.5V |
| 1010 | 12.0V |
| 1011 | 12.5V |
| 1100 | 13.0V |
| 1101 | 13.5V |
| 1110 | 14.0V |
| 1111 | 14.5V |

The start-up time of VDRV mainly depends on VSUP, VDRV_CFG and the external capacitor CDRV.

Figure 7.3.3-1 shows a typical start-up behavior at different VDRV_CFG settings and a discharging with 16 pulses at 30ms. The VDRV_OK_H and VDRV_OK_L thresholds are also depicted for the three voltages.

The 'READ_STATUS' command can be used to check if the VDRV voltage is working properly.

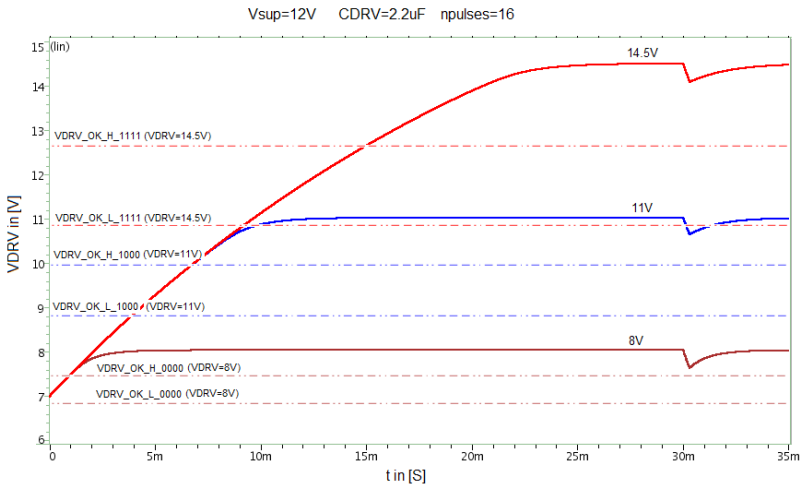



*Figure 7.3.3-1: Example of charging CDRV=2.2µF and discharging with 16 pulses @ VSUP=12V*

#### 7.3.4 Electronic damping

An electronic damping algorithm after the burst pulses reduces the ringing time of the transducer. The optimum setting depends on the transducer characteristics and the EEPROM bits EL_DAMP.

The procedure for adjusting the electronic damping can be done as follows:

1. Measure ringing time with EL_DAMP = 0 and 'SEND' command
2. Increase EL_DAMP
3. Measure ringing time with 'SEND' command
4. Increase EL_DAMP as long as ringing time becomes lower using the 'SEND' command for measurement

If EL_DAMP=0, then no additional damping pulses are sent.

During calibration of EL_DAMP no close obstacle should be in front of the transducer.

## 7.4 Receiving path

Figure 7.4-1 shows the receiver block diagram. The echo signal is picked up from the transducer at pins AINS and AING. The signal goes through a programmable gain stage first. After digitization, the signal is further processed by a digital filter. This reduces the sensitivity to unwanted signals outside the frequency band of the transducer.

The receiver starts to work after $t_{D\_IO}$.

Finally, the filter output goes through a register programmable comparator stage before the evaluated data is sent via pin IO to the control unit.

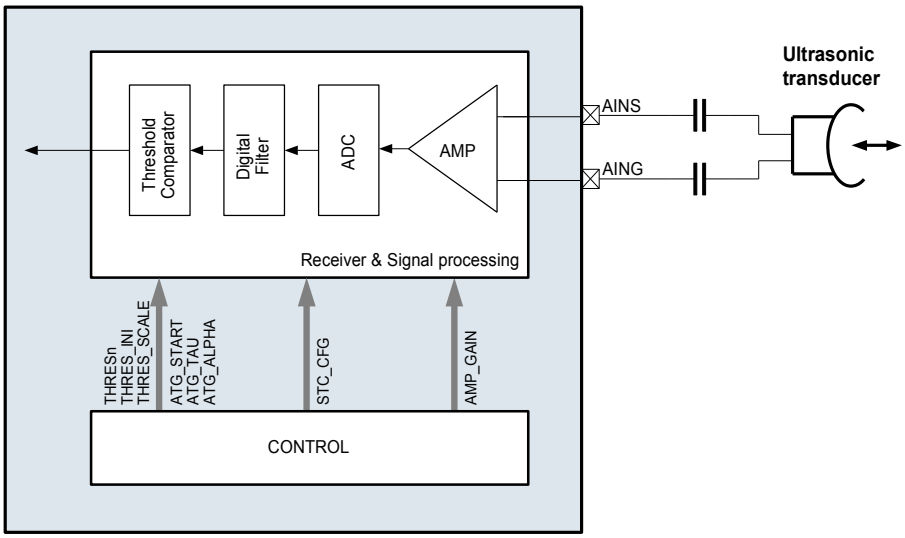



*Figure 7.4-1: Block diagram of receiving path*

### 7.4.1 Analog Amplifier

Transducer output signal levels vary by type and application. The differential input of the amplifier minimizes pickup of unwanted signals. AINS input is typically used as signal input while AING input has to be connected to transducer GND.

The low incoming analog echo signal has to be amplified before it is converted by an ADC. The amplifier gain is programmable with a range between $G_{MIN}$ and $G_{MAX}$ with $\Delta G_C$ resolution to ensure an optimum amplifier output voltage range. Gain settings are programmed with AMP_GAIN and stored in EEPROM. The gain can be calculated using the following formula:

$$Gain = G_{MIN} + \Delta GC \cdot AMP\_GAIN$$

The amplifier output is internally connected to an ADC.

### 7.4.2 Analog to Digital Conversion (ADC)

The analog to digital converter (ADC) converts the analog signal into a digital signal and all further steps are processed digitally.

### 7.4.3 Digital Filter

After an analog to digital conversion the signal is processed by a digital filter.
Since the clock of the transducer driver and the ADC / filter clock are synchronized, the digital filter follows the sending frequency. The output of the digital matched filter (DMF) represents the envelope of the echo signal.

The driver frequency and the frequency of the digital filter together with the timing of the threshold depend on the oscillator frequency. The center frequency of the filter is shifted with the driver frequency temperature dependency. The bandwidth is scaled with frequency.

#### 7.4.3.1 Filter characteristics

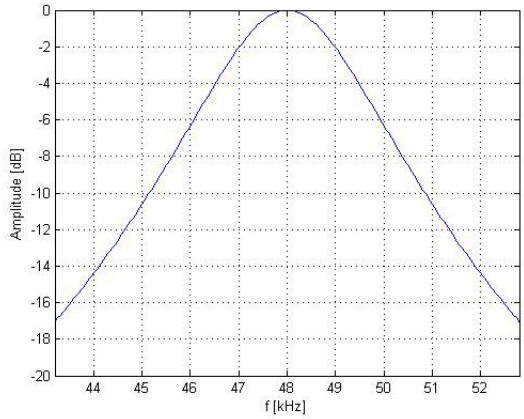



*Figure 7.4.3.1-1: Filter frequency response at 48kHz*

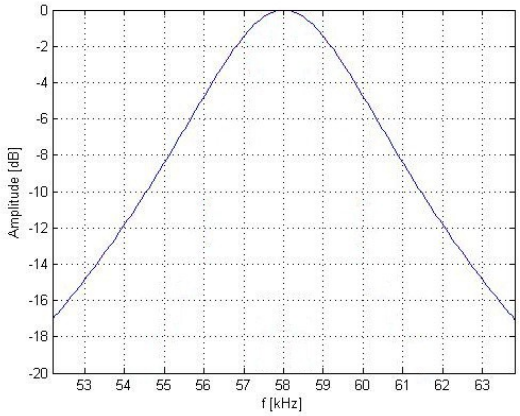



*Figure 7.4.3.1-2: Filter frequency response at 58kHz*

### 7.4.4 Sensitivity Time Control (STC)

Sensitivity time control (STC) increases a digital gain over time, starting at $T_{START\_STC}$ with an increment of ΔG_STC for $N_{STEP\_STC}$ steps every $T_{STEP\_STC}$ time steps. The maximum gain value is fix and results in the final sum of all steps $S_{G\_STC}$ (see Figure 7.4.4-1). The STC can be activated by STC_CFG.

STC combined with a proper threshold setup is useful in:
- Reduction of ground echoes at short range and increased amplitude at long range.
- No overdrive at short range.

**Remark:** The configuration of STC_CFG is written in volatile memory.

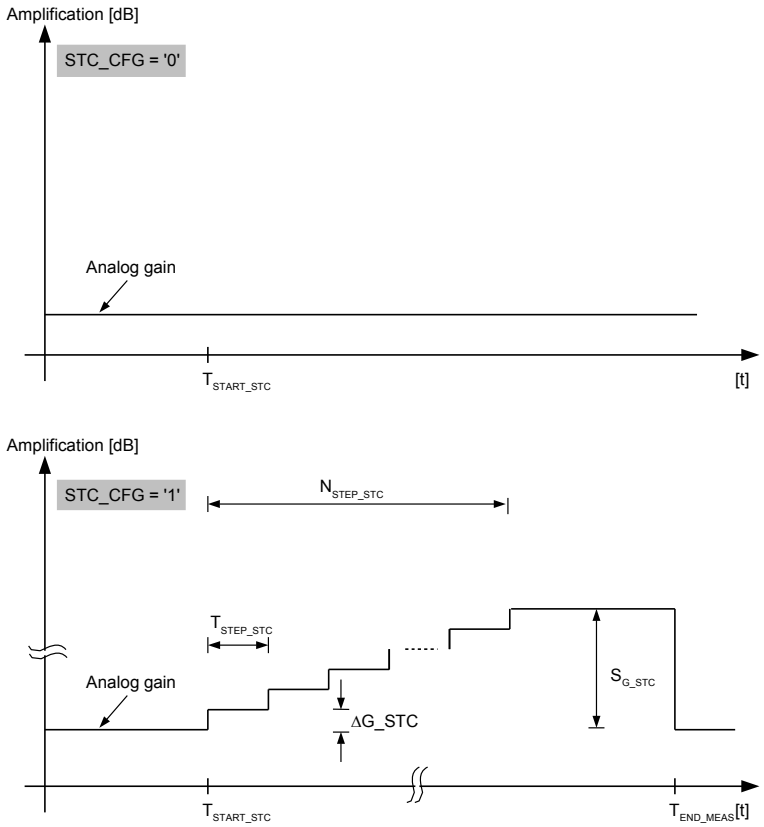



*Figure 7.4.4-1: Sensitivity time control*

After a measurement the STC is switched off (0dB). So that the noise measurement is done without STC.

Table 7.4.4-1: STC calculation table

| ***stc_step*** | ***0*** | ***1*** | ***2*** | ***3*** | ***4*** | ***5*** | ***6*** | ***7*** | ***8*** | ***9*** |
|---|---|---|---|---|---|---|---|---|---|---|
| factor | 1,00 | 1,125 | 1,250 | 1,375 | 1,500 | 1,625 | 1,750 | 1,875 | 2,00 | 2,25 |
| dB | 0,000 | 1,023 | 1,938 | 2,766 | 3,522 | 4,217 | 4,861 | 5,460 | 6,021 | 7,044 |
| dB / step | | 1,023 | 0,915 | 0,828 | 0,756 | 0,695 | 0,644 | 0,599 | 0,561 | 1,023 |
| | | | | | | | | | | |
| stc_step | 10 | 11 | 12 | 13 | 14 | 15 | 16 | | | |
| factor | 2,500 | 2,750 | 3,000 | 3,250 | 3,500 | 3,750 | 4,000 | | | |
| dB | 7,959 | 8,787 | 9,542 | 10,238 | 10,881 | 11,481 | 12,041 | | | |
| dB / step | 0,915 | 0,828 | 0,756 | 0,695 | 0,644 | 0,599 | 0,561 | | | |

### 7.4.5 Threshold comparator

The signal processing and data evaluation is done by comparing the echo envelope signal of the digital filter output with a threshold value. In case of the static threshold generation (ATG_CFG='0') the programmed values are used. In case of the automatic threshold generation (ATG_CFG='1') the combination of static and dynamic threshold generation is used.

The result of the comparator output appears at pin IO in SEND / RECEIVE mode. If the current envelope of the echo signal goes above the threshold for a time $t > t_{DEB\_ECHO}$, pin IO is pulled to GND.

### 7.4.6 Threshold generation

The IC offers two different possibilities of threshold generation, which can be selected by the EEPROM bit ATG_CFG:

- static threshold generation
- automatic threshold generation

In both cases during SEND and RECEIVE mode, a filter output signal exceeding the comparator threshold, indicates a received echo. The threshold passed to the comparator is a function of time.

In case of the static threshold generation, the IC offers several opportunities for individual configuration of the threshold function. This function is defined by:

- Selected transducer frequency
- Up to 14 threshold values which are connected by linear interpolation
- An additional offset value
- A scaling factor (only receive mode)
- Initial threshold (only receive mode)

In case of automatic threshold generation, the IC offers the individual configuration parameters described in chapter 7.4.6.3.

With the example for static threshold generation in Figure 7.4.6-1 the notation of the following chapters is introduced.

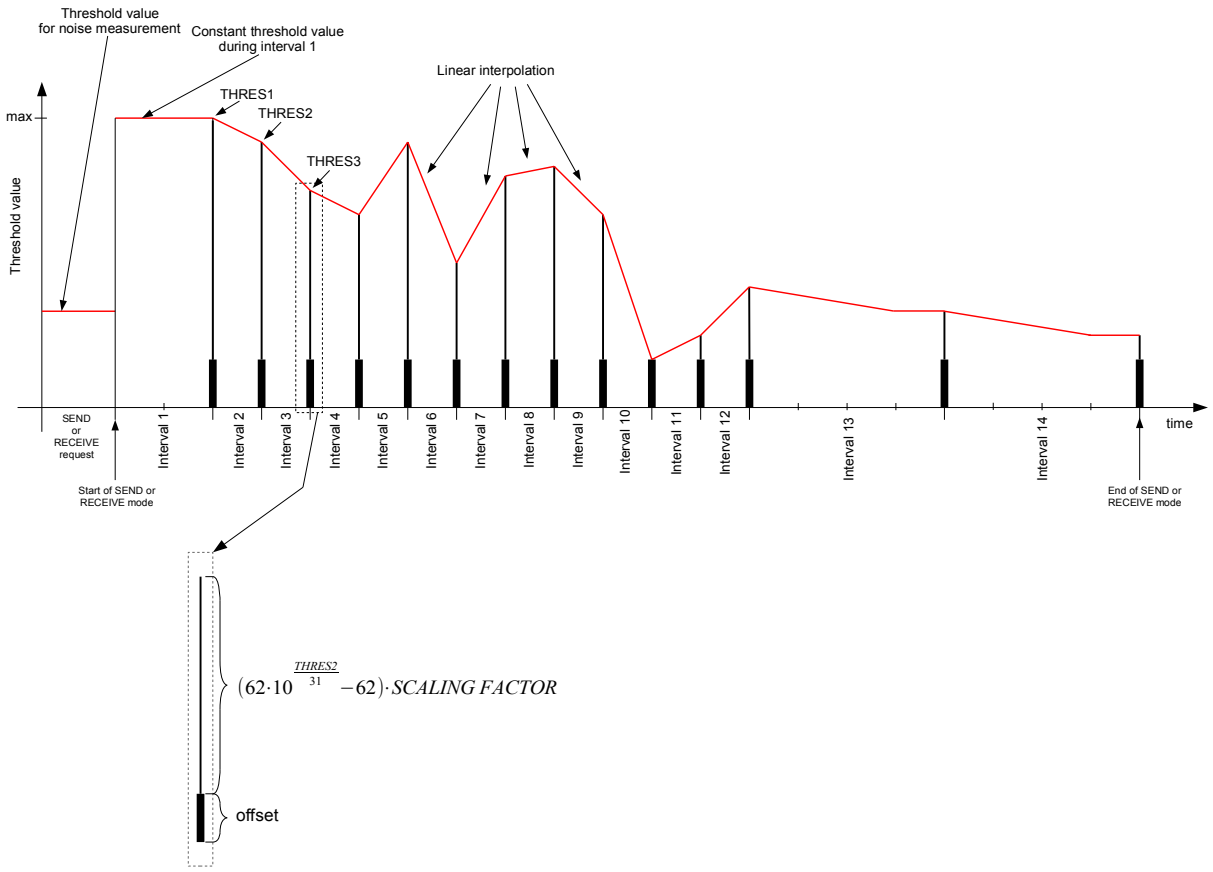



*Figure 7.4.6-1: Intervals of static threshold generation in SEND or RECEIVE mode and related threshold values*

#### 7.4.6.1 Intervals of static threshold generation

The intervals linearly depend on the selected transducer frequency $f_{DRV}$. The programmable threshold values THRES1 - THRES14 are reached at the end of the corresponding interval. During the interval the threshold is evaluated by a linear interpolation. Only the first interval THRES1 is constant during the complete interval 1. Table 7.4.6.1-1 shows the intervals for two different frequencies and gives the corresponding register THRESn to program the exponent of the threshold value.

Table 7.4.6.1-1: Intervals depending on $f_{DRV}$

| *Interval name* | *threshold exponent* | *Interval [ms]* | *Interval [ms]* |
|---|---|---|---|
| | | $f_{DRV}$=48kHz | $f_{DRV}$=58kHz |
| 1 | THRES1 | 0 - 2.0 | 0 - 1.66 |
| 2 | THRES2 | 2.0 -3.0 | 1.66 - 2.48 |
| 3 | THRES3 | 3.0 - 4.0 | 2.48 - 3.31 |
| 4 | THRES4 | 4.0 - 5.0 | 3.31 - 4.14 |
| 5 | THRES5 | 5.0 - 6.0 | 4.14 - 4.97 |
| 6 | THRES6 | 6.0 - 7.0 | 4.97 - 5.79 |
| 7 | THRES7 | 7.0 - 8.0 | 5.79 - 6.62 |
| 8 | THRES8 | 8.0 - 9.0 | 6.62 - 7.45 |
| 9 | THRES9 | 9.0 - 10.0 | 7.45 - 8.28 |
| 10 | THRES10 | 10.0 - 11.0 | 8.28 - 9.10 |
| 11 | THRES11 | 11.0 - 12.0 | 9.10 - 9.93 |
| 12 | THRES12 | 12.0 - 13.0 | 9.93 - 10.76 |
| 13 | THRES13 | 13.0 - 17.0 | 10.76 - 14.07 |
| 14 | THRES14 | 17.0 - 21.0 | 14.07 - 17.38 |

A measurement cycle ('SEND', 'SENDx', 'RECEIVE', 'SEND_WO_DAMP') will be finished between THRES6 and THRES14 depending on the programmed threshold values. The measurement cycle stops, when the value of the current threshold is set to the maximum threshold value and higher than the previous one. If this combination does not occur the measurement cycle stops after the last time interval.

For example at $f_{DRV}$=58kHz the shortest measurement duration of 4.97ms is achieved, when THRES6=31 and THRES5<31 .

#### 7.4.6.2 Values of static threshold generation

In SEND mode the threshold value used for the interpolation algorithm is calculated as follows:

$$threshold\_value\_n = \left(62 \cdot 10^{\frac{THRESn\_dez}{31}} - 62\right) + 62$$

In RECEIVE mode the threshold values can be decreased by a scaling factor. All threshold values are multiplied with this scaling factor. The scaling factor is set by bits THRES_SCALE[1:0] according to Table 7.4.6.2-1 and the threshold value in RECEIVE mode is calculated as follows:

$$threshold\_value\_n = \left(62 \cdot 10^{\frac{THRESn\_dez}{31}} - 62\right) \cdot SCALING\_FACTOR + 62$$

The additional offset is always 62, independent from SEND or RECEIVE mode. Table 7.4.6.2-2 shows the resulting threshold values depending on the threshold component and the scaling factor.

Table 7.4.6.2-1: Scaling for Receive Threshold

| *THRES_SCALE[1]* | *THRES_SCALE[0]* | *SCALING_FACTOR* |
|---|---|---|
| 0 | 0 | 0.25 |
| 0 | 1 | 0.5 |
| 1 | 0 | 0.75 |
| 1 | 1 | 1.0 |

Table 7.4.6.2-2: Threshold values resulting from exponent and scaling factor

| *Threshold exponent* | *Threshold value with scaling 1.0* | *Threshold value with scaling 0.75* | *Threshold value with scaling 0.5* | *Threshold value with scaling 0.25* |
|---|---|---|---|---|
| 0 | 62 | 62 | 62 | 62 |
| 1 | 67 | 65 | 64 | 63 |
| 2 | 72 | 69 | 67 | 64 |
| 3 | 77 | 73 | 69 | 65 |
| 4 | 83 | 77 | 72 | 67 |
| 5 | 90 | 83 | 76 | 69 |
| 6 | 97 | 88 | 79 | 70 |
| 7 | 104 | 93 | 83 | 72 |
| 8 | 112 | 99 | 87 | 74 |
| 9 | 121 | 106 | 91 | 76 |
| 10 | 130 | 113 | 96 | 79 |
| 11 | 140 | 120 | 101 | 81 |
| 12 | 151 | 128 | 106 | 84 |
| 13 | 163 | 137 | 112 | 87 |
| 14 | 175 | 146 | 118 | 90 |
| 15 | 189 | 157 | 125 | 93 |
| 16 | 203 | 167 | 132 | 97 |
| 17 | 219 | 179 | 140 | 101 |
| 18 | 236 | 192 | 149 | 105 |
| 19 | 254 | 206 | 158 | 110 |
| 20 | 274 | 221 | 168 | 115 |
| 21 | 295 | 236 | 178 | 120 |
| 22 | 318 | 254 | 190 | 126 |
| 23 | 342 | 272 | 202 | 132 |
| 24 | 369 | 292 | 215 | 138 |
| 25 | 397 | 313 | 229 | 145 |
| 26 | 428 | 336 | 245 | 153 |
| 27 | 461 | 361 | 261 | 161 |
| 28 | 496 | 387 | 279 | 170 |
| 29 | 534 | 416 | 298 | 180 |
| 30 | 576 | 447 | 319 | 190 |
| 31 | 620 | 480 | 341 | 201 |

**Remark:** The SCALING_FACTOR in SEND mode cannot be modified, SCALING_FACTOR is always 1.0.

#### 7.4.6.3 Automatic threshold generation

The automatic threshold generation (ATG) can be activated by ATG_CFG.

An activation means a combination of static and dynamic threshold, which is depicted in Figure 7.4.6.3-1.

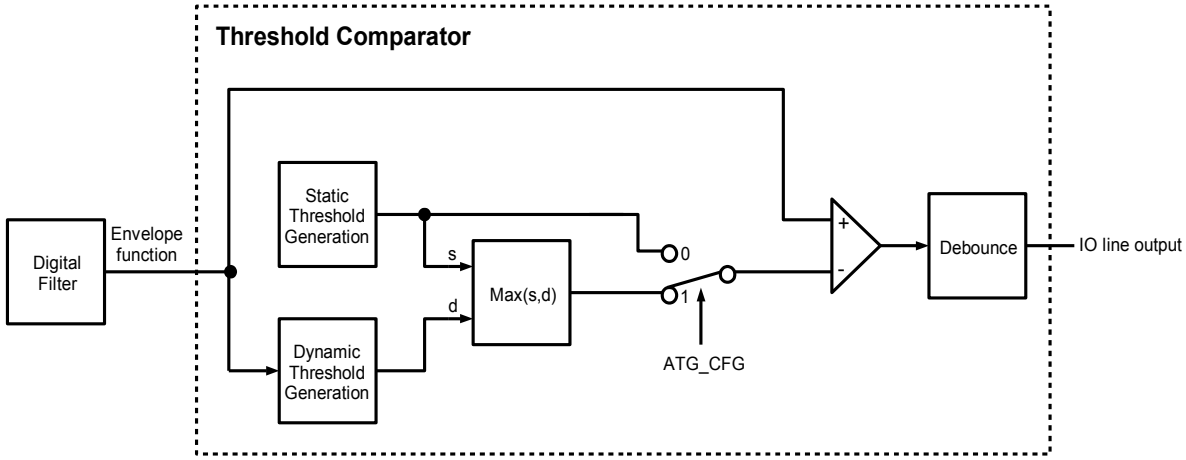



*Figure 7.4.6.3-1: Threshold generation using ATG_CFG*

When ATG_CFG='1' the maximum of the static threshold value and the dynamic calculated value is compared to the envelope function with a comparator.

The dynamic threshold is continuoulsy calculated and depends on the start value (ATG_START), the time constant (ATG_TAU) and the multiplier (ATG_ALPHA).

As soon as the envelope of the echo signal is above the dynamic threshold, the dynamic threshold stays constant.

If ATG_CFG='1' the dynamic threshold parameters can be programmed with the 'THRESHOLD' command within the volatile memory. See chapter 7.5.6 for more details.

The starting value of the dynamic threshold can be set by ATG_START:

Table 7.4.6.3-1: ATG_START[1:0]

| *ATG_START[1]* | *ATG_START[0]* | *value* |
|---|---|---|
| 0 | 0 | 256 |
| 0 | 1 | 384 |
| 1 | 0 | 512 |
| 1 | 1 | 640 |

The figures Figure 7.4.6.3-2 and Figure 7.4.6.3-3 show samples of the dynamic threshold set-up in receive mode.

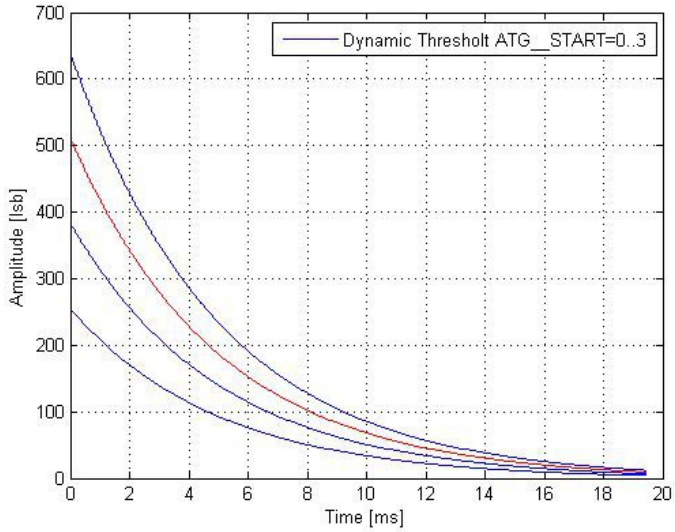



*Figure 7.4.6.3-2: Dynamic threshold @ $f_{DRV}$=48kHz for ATG_TAU=0, ATG_ALPHA=any and ATG_START varied*

The time constant defines the fall time and can be set by ATG_TAU:

Table 7.4.6.3-2: ATG_TAU[2:0]

| *ATG_TAU[2]* | *ATG_TAU[1]* | *ATG_TAU[0]* | *falltime* |
|---|---|---|---|
| 0 | 0 | 0 | slow |
| 0 | 0 | 1 | |
| 0 | 1 | 0 | |
| 0 | 1 | 1 | |
| 1 | 0 | 0 | |
| 1 | 0 | 1 | |
| 1 | 1 | 0 | |
| 1 | 1 | 1 | fast |

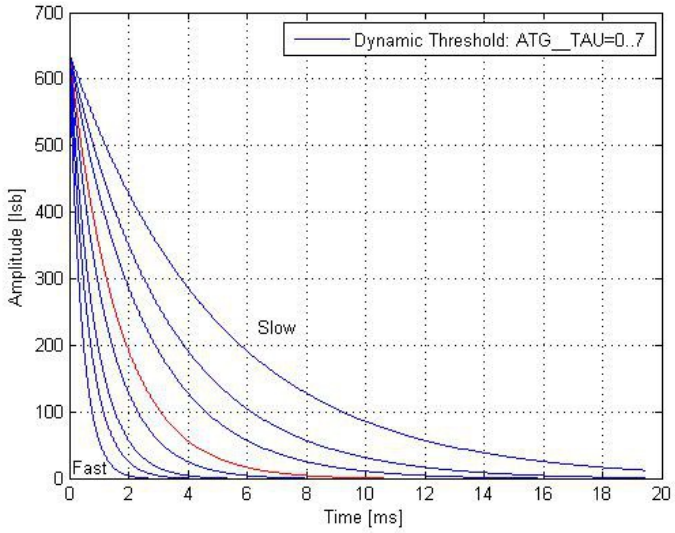



*Figure 7.4.6.3-3: Dynamic threshold @ $f_{DRV}$=48kHz for ATG_TAU=varied, ATG_ALPHA=any and ATG_START=3*

The multiplier sets the signal-to-noise ratio between the envelope function and the used threshold.
It can be defined by ATG_APLHA:

Table 7.4.6.3-3: ATG_ALPHA[1:0]

| *ATG_ALPHA[1]* | *ATG_ALPHA[0]* | *value* |
|---|---|---|
| 0 | 0 | 2.5 |
| 0 | 1 | 3.0 |
| 1 | 0 | 3.5 |
| 1 | 1 | 4.0 |

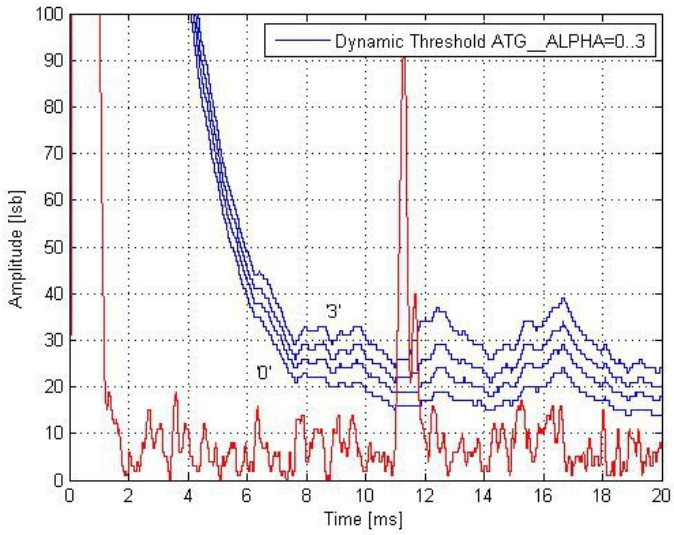



*Figure 7.4.6.3-4: Dynamic threshold for ATG_TAU=3, ATG_ALPHA=varied and ATG_START=2*

A zoom of Figure 7.4.6.3-4 shows the behavior during echo reception:

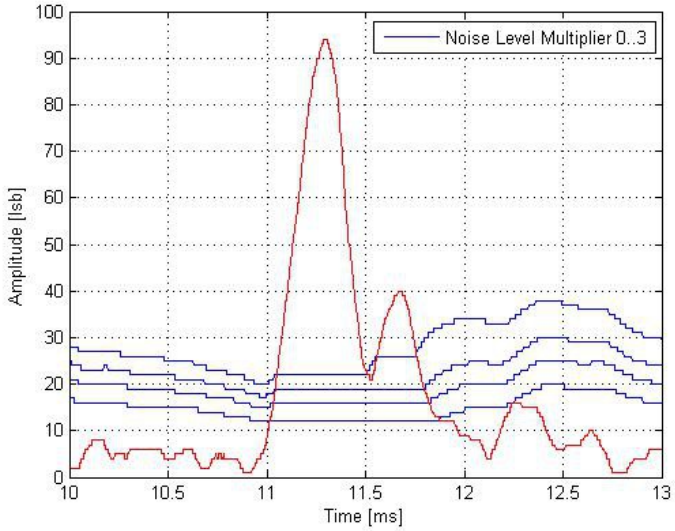



*Figure 7.4.6.3-5: Dynamic threshold behavior during echo*

When ATG_CFG='1':

- As static threshold value for THRES13 and THRES14 the value of THRES12 is used.
- For the threshold exponent = 0 the threshold value can go down to 3 (instead of 62) for every scaling.
- All other threshold values are as depicted in Table 7.4.6.2-2.

To finish a measurement cycle while ATG_CFG=1 after THRES12 or THRES13 the THRES_END option can be used:

Table 7.4.6.3-4: THRES_END[2:0]

| ***THRES_END[2]*** | ***THRES_END[1]*** | ***THRES_END[0]*** | ***Meaning*** |
|---|---|---|---|
| 0 | 0 | 0 | Measurement cycle finished after THRES14 |
| 0 | 0 | 1 | Measurement cycle finished after THRES13 |
| 0 | 1 | 0 | Measurement cycle finished after THRES12 |

#### 7.4.6.4 Initial threshold in receive mode

The initial threshold exponent during RECEIVE mode is defined by bit THRES_INI according to Table 7.4.6.4-1. If this bit is set to '0' THRES1 is valid for the first interval and if this bit is set to '1' THRES2 is valid for the first interval.

Table 7.4.6.4-1: Function of bit THRES_INI

| *THRES_INI* | *Function in receive mode* |
|---|---|
| 0 | initial threshold exponent=THRES1 |
| 1 | initial threshold exponent=THRES2 |

#### 7.4.6.5 Noise measurement during SEND and RECEIVE command

As increased ambient noise might disturb the measurement in SEND or RECEIVE mode, the IC measures the ambient supersonic noise directly before entering SEND or RECEIVE mode. The ambient noise measurement is performed during the low phase of the 'SEND' or 'RECEIVE' command ($T_{SND}$ / $T_{REC}$). The output of the digital filter is compared to a threshold value which can be selected by bits NOISE_CFG[1:0] according to Table 7.4.6.5-1.

The result of the noise measurement is stored each 'SEND' or 'RECEIVE' command and can be read out with the IO command "READ_STATUS" from the status register.

Table 7.4.6.5-1: Threshold value for noise measurement depending of bits NOISE_CFG[1:0]

| *NOISE_CFG[1]* | *NOISE_CFG[0]* | *Threshold value* |
|---|---|---|
| 0 | 0 | ATG_CFG=0: THRES14 (of the previous measurement) and SCALING_FACTOR fixed to 1.0<br>ATG_CFG=1: THRES12 (of the previous measurement) and SCALING_FACTOR fixed to 1.0 |
| 0 | 1 | 62 |
| 1 | 0 | 124 |
| 1 | 1 | 620 |

**Remark:** The threshold value for the first noise measurement after 'power on' is at maximum value of 620.

#### 7.4.6.6 Masking of comparator output

For threshold values < 255 the comparator output can be masked for the time $T_{CMASK}$ after the output signal of the digital filter drops below the comparator threshold. This functionality might be useful if the IC is operated with high gain and low comparator threshold. In this combination even low noise coupling from the IO line to the analog input circuitry can cause an additional echo signal.
The masking can be enabled with bit COMP_MASK according to Table 7.4.6.6-1.

Table 7.4.6.6-1: Comparator masking

| *COMP_MASK* | *Function* |
|---|---|
| 0 | Comparator masking **not** active |
| 1 | Comparator masking active |

Masking of the comparator output is not necessary (COMP_MASK=0), if a clean decoupling between IO-line and receiving part is guaranteed.

## 7.5 IO Interface

The IO interface is used to communicate between the E524.05 or E524.06 and the hosting ECU. A 'SEND' or 'RECEIVE' command is initiated by an ECU pulling pin IO low for $T_{SND}$ or $T_{REC}$. For all other commands, the ECU pulls IO low for $T_{CMD}$ and issues a 4 bit command sequence. A logic '0' is signalized with pulling the line low for $T_{BIT0}$ and a logic '1' with $T_{BIT1}$ as shown in Figure 7.5-1. The bit length and all other timing parameters are proportional to the programmed driver frequency $f_{DRV}$.

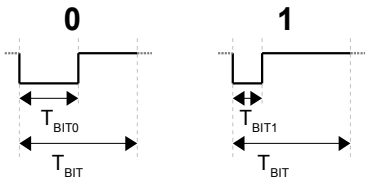



*Figure 7.5-1: IO Pin bit encoding*

**E524.05**

Data is sent between the E524.05 and ECU by modulating voltage on the supply wire VSUP_DATA. The application diagram in Figure 8.1-1 and Table 8.2-1 show the location and size of the external components to ensure secure bidirectional communication. During communication, tank capacitors $C_{SUP3}$ supply the E524.05 at pin VSUP.

To send data to the E524.05, the supply line voltage has to be modulated by the ECU. A voltage at the pin IO below $V_{IO\_IL}$ will be detected as a low level, a voltage above $V_{IO\_IH}$ as a high level. A debouncing circuit suppresses interference shorter than $T_{DEB}$.

Data is transmitted from the E524.05 to the ECU by modulating pull-down current $I_{PD\_IO}$ into pin IO. $I_{PD\_IO}$ increases the supply current coming from the ECU via VSUP_DATA. Increasing $I_{PD\_IO}$ will increase the voltage drop over Ri and decrease the voltage at VI_ECU which is recognized as a low level by the ECU. Consider plug and wire resistances for VSUP_DATA and GND connecting ultrasonic module and ECU to establish proper voltage levels at pin IO.

**E524.06**

Data is sent between the E524.06 and ECU by pulling the single line DATA low for defined periods of time. The application diagram in Figure 8.3-1 and Table 8.4-1 show the location and size of the external components to ensure secure communication via DATA.

Incoming data to the E524.06 is recognized as a low if $V_{IO}$ is below $V_{IO\_IL}$ of the voltage at VSUP. A debouncing circuit suppresses interference shorter than $T_{DEB}$. Outgoing data transmission to the ECU is accomplished by pulling pin IO low overcoming pull-up resistor $R_{IO\_PU\_ECU}$. To reduce EMI, the slew rate pulling low is limited to $SR_{VIO}$. The slew rate of the rising edge is defined by external circuitry.

### 7.5.1 Exchange of commands

The E524.05 and E524.06 support following commands from the hosting ECU.

Table 7.5.1-1: Command structure summary

| *Command* | *Coding* | *Command Description* |
|---|---|---|
| SEND | $T_{SND}$ | Initiates a burst signal via the internal drivers followed by a measurement sequence. |
| RECEIVE | $T_{REC}$ | Initiates a measurement sequence without preceding burst, useful for triangulation in systems with multiple transducers. |
| SEND_WO_DAMP | $T_{CMD}$ + 1010 | Initiates a burst signal without electronic damping, useful for analyzing the ringing time without damping and the frequency deviation between driver frequency and transducer resonance frequency. |
| SEND4 | $T_{CMD}$ + 1011 | Initiates a burst signal with 4 pulses via the internal drivers followed by a measurement sequence. |
| SEND8 | $T_{CMD}$ + 1100 | Initiates a burst signal with 8 pulses via the internal drivers followed by a measurement sequence. |
| SEND12 | $T_{CMD}$ + 1101 | Initiates a burst signal with 12 pulses via the internal drivers followed by a measurement sequence. |
| SEND24 | $T_{CMD}$ + 1110 | Initiates a burst signal with 24 pulses via the internal drivers followed by a measurement sequence. |
| THRESHOLD | $T_{CMD}$ + 0001 | Writes individual threshold values for up to 14 timing intervals and scaling factors into the device. |
| READ_STATUS | $T_{CMD}$ + 0010 | Verifies previous transmission of threshold values, reads current noise status, reads frequency deviation between driver and resonance frequency and reads VDRV status. |
| CAL_PULSES | $T_{CMD}$ + 0011 | Returns 2 pulses with a defined interval of $T_{CAL}$ to the ECU for transducer driver frequency calibration purposes. |
| READ_ECHO | $T_{CMD}$ + 0111 | Returns 8 bit value as information of the echo height of the first detected echo. |
| EE_READ | $T_{CMD}$ + 0100 | Reads the EEPROM contents with three read voltage levels to verify successful programming. |
| EE_WRITE | $T_{CMD}$ + 0101 | Allows to pre-load settings for the driver frequency, amplifier gain, number of pulses, noise strategy, electronic damping, comparator masking, RD and ATG activation into the device. |
| EE_PROGRAM | $T_{CMD}$ + 0110 | Programs settings pre-loaded with EE_WRITE into the internal EEPROM. |
| EE_READ_SHADOW | $T_{CMD}$ + 1000 | Reads the EEPROM shadow registers to verify EE_WRITE. |
| READ_ID | $T_{CMD}$ + 1001 | A 24 bit chip ID is transferred on the IO line. |

### 7.5.2 'SEND' command

The 'SEND' command initiates a burst followed by a measurement sequence. The SEND mode is requested from the ECU by holding Pin IO low for $T_{SND}$ and is entered with the rising edge of the corresponding command. A filter output signal exceeding the comparator threshold indicates a received echo.

As long as the E524.05 and E524.06 operate in SEND mode, no instructions coming over the IO-Interface are accepted. The interface is ready to receive new instructions when a high level remains at pin IO for at least $T_{DEB}$ to debounce after SEND mode has ended.

The E524.05 and E524.06 can diagnose the proper operation of the transducer. After the 'SEND' command, the transducer driver is activated and sends out a burst for the length $T_{TX}$. This also causes high signal levels at the receiving amplifier and triggers the comparator.

**E524.05**

For the E524.05 Figure 7.5.2-1 illustrates the 'SEND' command timing with an example of correct operation.

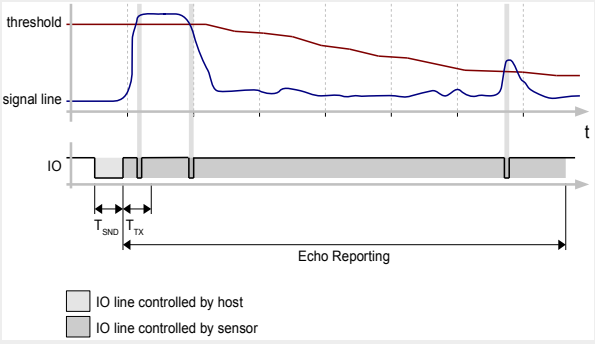



*Figure 7.5.2-1: E524.05 'SEND' command timing*

In the example above the threshold is held at maximum and then programmed to decline slowly.
The example above shows the three different possibilities when the IO line is pulled down.
The first low pulse is reported during burst, the second low pulse indicates the end of ringing time and can be used to verify correct operation and the third pulse in this example is triggered due to a detected echo.

**E524.06**

For the E524.06, the duration of the low phase after $T_{TX}$ can be used for diagnosis puposes. Figure 7.5.2-2 illustrates the 'SEND' command timing for the E524.06 with an example of correct operation.

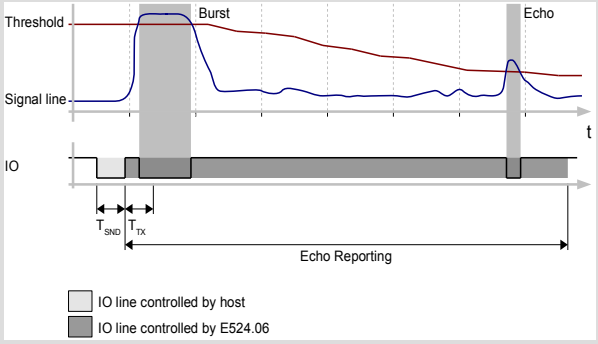



*Figure 7.5.2-2: E524.06 'SEND' command timing*

In the example above, the threshold is held at maximum during and shortly after the burst and then programmed to decline slowly. An echo is detected, when the signal line crosses the threshold line, which means that the comparator is triggered.

**E524.05**

The figure below shows that a crossing between threshold line and envelope will only be recognised on the IO_line if a debounce time of $T_{DEB\_ECHO}$ is maintained.

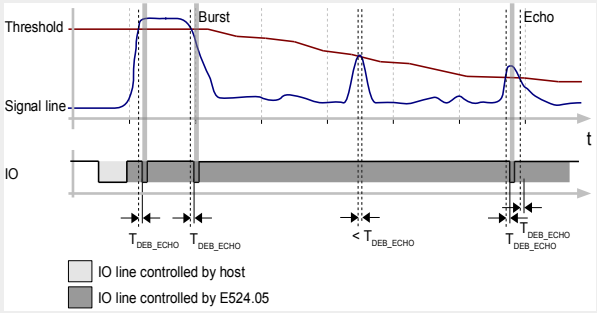



*Figure 7.5.2-3: E524.05 'SEND' command timing with $T_{DEB\_ECHO}$*

**E524.06**

The figure below shows that a crossing between threshold line and envelope will only be recognised on the IO_line if a debounce time of $T_{DEB\_ECHO}$ is maintained.

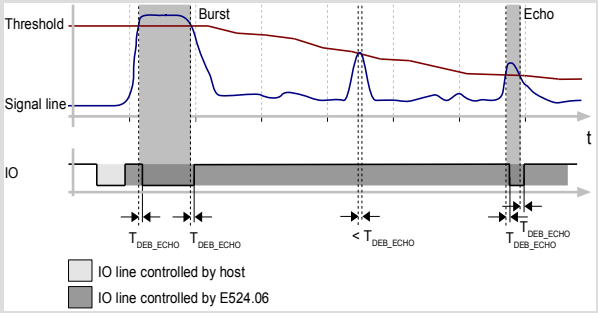



*Figure 7.5.2-4: E524.06 'SEND' command timing with $T_{DEB\_ECHO}$*

### 7.5.3 'RECEIVE' command

A 'RECEIVE' command is identical to the 'SEND' command but skips the burst. The initial threshold value in RECEIVE is defined by bit THRES_INI. The RECEIVE mode is requested from the ECU by holding Pin I/O low for $T_{REC}$ and is entered with the rising edge of the corresponding command. A filter output signal exceeding the comparator threshold indicates a received echo. In RECEIVE mode the threshold sensitivity can be increased by a scaling factor THRES_SCALE.

As long as the E524.05 and E524.06 operate in RECEIVE mode, no instructions coming over the IO-Interface are accepted. The interface is ready to receive new instructions when a high level remains at pin IO for at least $T_{DEB}$ to debounce after RECEIVE mode has ended.

**E524.05**

Figure 7.5.3-1 shows the timing for a E524.05 'RECEIVE' command.

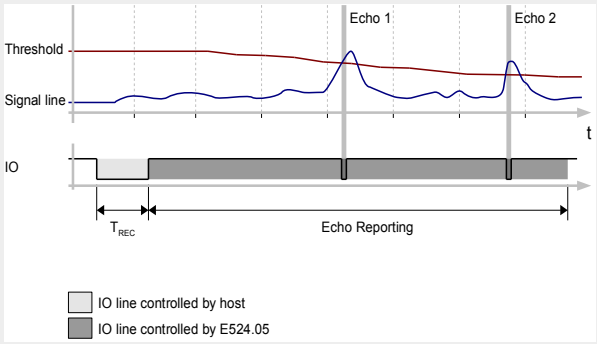



*Figure 7.5.3-1: E524.05 'RECEIVE' command timing*

The E524.05 operates purely in receiving mode for the entire sequence. In the example, two echoes are received and pull Pin IO low for $T_{ECHO2WIRE}$. The thresholds are scalable with the selected scaling factor THRES_SCALE, part of the 'THRESHOLD' command.

**E524.06**

Figure 7.5.3-2 shows the timing for a E524.06 'RECEIVE' command.

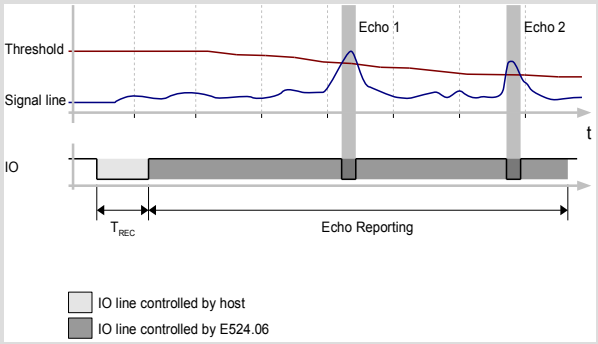



*Figure 7.5.3-2: E524.06 RECEIVE' command timing*

The E524.06 operates purely in receiving mode for the entire sequence. In the example, two echoes are received and pull Pin IO low. The thresholds are scalable with the selected scaling factor THRES_SCALE, part of the 'THRESHOLD' command.

### 7.5.4 'SEND_WO_DAMP' command

The command 'SEND_WO_DAMP' (send request without damping) is functional identical with the 'SEND' command with one exception: after the burst pulses the electronic damping is inactive during this measurement (if enabled in EEPROM) are generated. Without damping the frequency deviation between the driver frequency and transducer resonance frequency can be analyzed. The result is valid after the 'SEND_WO_DAMP' command is finished and is read out with the command 'READ_STATUS'. This command can also be used to check the efficiency of the damping.

**E524.05**

Figure 7.5.4-1 illustrates the 'SEND_WO_DAMP' command timing for the E524.05 with an example.

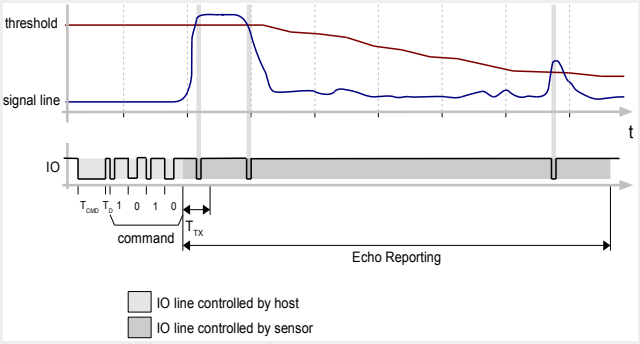



*Figure 7.5.4-1: E524.05 Send without damping timing*

**E524.06**

Figure 7.5.4-2 illustrates the 'SEND_WO_DAMP" command timing for the E524.06 with an example.

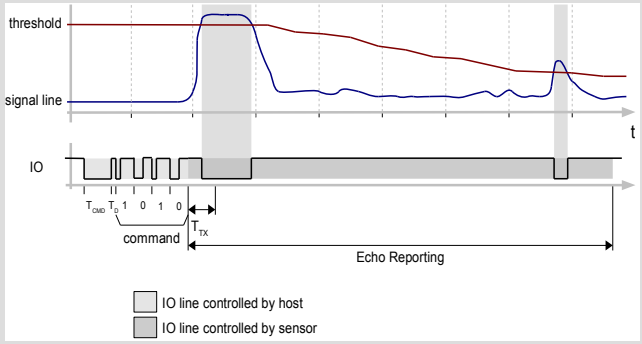



*Figure 7.5.4-2: E524.06 Send without damping timing*

### 7.5.5 'SEND4', 'SEND8', 'SEND12', 'SEND24' commands

The commands 'SEND4' (send request with 4 pulses), 'SEND8' (send request with 8 pulses), 'SEND12' (send request with 12 pulses) and 'SEND24' (send request with 24 pulses) are functional identical with the 'SEND' command with one exception: Independent from the EEPORM setting N_PULSES, all 4 commands use their number of pulses.

These commands can be used to send a burst with different number of pulses for an enhanced short or long range performance without programming of the EEPROM.

### 7.5.6 'THRESHOLD' command

In case of ATG_CFG='0' the 'THRESHOLD' command writes the threshold values of the 14 intervals and several control bits for threshold scaling, noise strategy and the sensitivity time control into the device.

In case of ATG_CFG='1' the 'THRESHOLD' command writes the threshold values of the 12 intervals and several control bits for automatic threshold generation, threshold scaling, noise strategy and the sensitivity time control into the device.

In both cases the programming is secured with parity bits. The successful programming can be verified with the 'READ_STATUS' command.

**Remark:** Threshold data is stored in a volatile memory. Therefore the ECU has to write the threshold data every start up. After power on the default values are active.

**Static Thresholds (ATG_CFG='0')**

| MSB | | | | | | | | | | | | | | | | | | | | | | LSB |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| 78 | 77 | 76 | 75 | 74 | 73 | 72 | 71 | 70 | 69 | 68 ... 19 | 18 | 17 | 16 | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| THRES1 | | | | | THRES2 | | | | | THRES3 ... THRES12 | | | | | THRES13 | | | | THRES14 | | THRES_SCALE | | THRES_INI | STC_CFG | PARITY0 | PARITY1 | PARITY2 | PARITY3 | PARITY4 |

**Automatic Thresholds (ATG_CFG='1')**

| MSB | | | | | | | | | | | | | | | | | | | | | | LSB |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| 78 | 77 | 76 | 75 | 74 | 73 | 72 | 71 | 70 | 69 | 68 ... 19 | 18 | 17 | 16 | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| THRES1 | | | | | THRES2 | | | | | THRES3 ... THRES12 | | THRES_END | | ATG_TAU | | ATG_ALPHA | | ATG_START | | THRES_SCALE | | THRES_INI | STC_CFG | PARITY0 | PARITY1 | PARITY2 | PARITY3 | PARITY4 |

**Parity calculation**

| MSB | | | | | | | | | | | | | | | | | | | | | | LSB |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| 78 ... 69 | | | | | | | | | | 68 ... 53 | | | | | | | | | | | 52 ... 37 | | | | | | | | | 36 ... 21 | | | | | | | | | 20 ... 5 | | | | | | | | | 4 | 3 | 2 | 1 | 0 |
| Calculate even parity bit | | | | | | | | | | Calculate even parity bit | | | | | | | | | | | Calculate even parity bit | | | | | | | | | Calculate even parity bit | | | | | | | | | Calculate even parity bit | | | | | | | | | PARITY0 | PARITY1 | PARITY2 | PARITY3 | PARITY4 |

*Figure 7.5.6-1: Threshold organisation*

The 'THRESHOLD' command timing diagram is shown in Figure 7.5.6-2. The first bit transmitted on the IO line is the MSB of THRES1 and the last bit is the parity bit PARITY4.

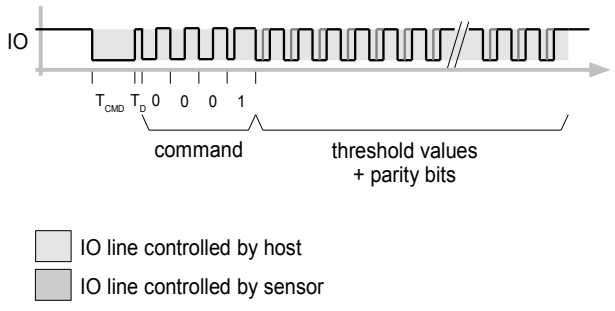



*Figure 7.5.6-2: Write threshold command*

Table 7.5.6-1: Write threshold (ATG_CFG='0')

| *Bit* | *No. of bits* | *Function* | *Name* | *Default (dec)* |
|---|---|---|---|---|
| 78:74 | 5 | 1st threshold value | THRES1 | 31 |
| 73:69 | 5 | 2nd threshold value | THRES2 | 31 |
| 68:64 | 5 | 3rd threshold value | THRES3 | 31 |
| 63:59 | 5 | 4th threshold value | THRES4 | 30 |
| 58:54 | 5 | 5th threshold value | THRES5 | 29 |
| 53:49 | 5 | 6th threshold value | THRES6 | 28 |
| 48:44 | 5 | 7th threshold value | THRES7 | 27 |
| 43:39 | 5 | 8th threshold value | THRES8 | 25 |
| 39:34 | 5 | 9th threshold value | THRES9 | 22 |
| 33:29 | 5 | 10th threshold value | THRES10 | 14 |
| 28:24 | 5 | 11th threshold value | THRES11 | 10 |
| 23:19 | 5 | 12th threshold value | THRES12 | 6 |
| 18:14 | 5 | 13th threshold value | THRES13 | 0 |
| 13:9 | 5 | 14th threshold value | THRES14 | 0 |
| 8:7 | 2 | Scaling for receive operation | THRES_SCALE[1:0] | 2 |
| 6 | 1 | Initial threshold value | THRES_INI | 0 |
| 5 | 1 | Sensitivity time control configuration<br>'0': off<br>'1': on | STC_CFG | 1 |
| 4 | 1 | Even parity bit for bit 20-5 | PARITY0 | - |
| 3 | 1 | Even parity bit for bit 36-21 | PARITY1 | - |
| 2 | 1 | Even parity bit for bit 52-37 | PARITY2 | - |
| 1 | 1 | Even parity bit for bit 68-53 | PARITY3 | - |
| 0 | 1 | Even parity bit for bit 78-69 | PARITY4 | - |

Table 7.5.6-2: Write threshold (ATG_CFG='1')

| *Bit* | *No. of bits* | *Function* | *Name* | *Default (dec)* |
|---|---|---|---|---|
| 78:74 | 5 | 1st threshold value | THRES1 | 31 |
| 73:69 | 5 | 2nd threshold value | THRES2 | 31 |
| 68:64 | 5 | 3rd threshold value | THRES3 | 31 |
| 63:59 | 5 | 4th threshold value | THRES4 | 30 |
| 58:54 | 5 | 5th threshold value | THRES5 | 29 |
| 53:49 | 5 | 6th threshold value | THRES6 | 28 |
| 48:44 | 5 | 7th threshold value | THRES7 | 27 |
| 43:39 | 5 | 8th threshold value | THRES8 | 25 |
| 39:34 | 5 | 9th threshold value | THRES9 | 22 |
| 33:29 | 5 | 10th threshold value | THRES10 | 14 |
| 28:24 | 5 | 11th threshold value | THRES11 | 10 |
| 23:19 | 5 | 12th threshold value | THRES12 | 6 |
| 18:16 | 3 | Finish measurement cycle option | THRES_END | 0 |
| 15:13 | 3 | Time constant of ATG | ATG_TAU | 0 |
| 12:11 | 2 | Multiplier of ATG | ATG_ALPHA | 0 |
| 10:9 | 2 | Start value of ATG | ATG_START | 0 |
| 8:7 | 2 | Scaling for receive oper-ation | THRES_SCALE[1:0] | 2 |
| 6 | 1 | Initial threshold value | THRES_INI | 0 |
| 5 | 1 | Sensitivity time control configuration<br>'0': off<br>'1': on | STC_CFG | 1 |
| 4 | 1 | Even parity bit for bit 20-5 | PARITY0 | - |
| 3 | 1 | Even parity bit for bit 36-21 | PARITY1 | - |
| 2 | 1 | Even parity bit for bit 52-37 | PARITY2 | - |
| 1 | 1 | Even parity bit for bit 68-53 | PARITY3 | - |
| 0 | 1 | Even parity bit for bit 78-69 | PARITY4 | - |

The default threshold values for ATG_CFG=0 and ATG_CFG=1 are the same.

### 7.5.7 'READ_STATUS' command

The command 'READ_STATUS' can be used to verify the last transmission of the threshold values and control bits and to get information about the noise level of the latest send/receive request. The noise level is analyzed during the low phase on the IO line of the send/receive request command.
The frequency deviation measurement of the latest 'SEND_WO_DAMP' measurement or 'SEND' with EL_DAMP=0 is transmitted as well as the status signal of the transducer driver output voltage. The data of Bit0-5 should be evaluated before another 'SEND' with EL_DAMP>0. The meaning of these bits is as follows:

Table 7.5.7-1: Read Status: Bits 0-4

| *Bit 4:0* | *Meaning* |
|---|---|
| 01111 | +11.7% frequency deviation between the transducer driver and its resonance frequency |
| 01110 | +10.92% frequency deviation between the transducer driver and its resonance frequency |
| ... | |
| 00001 | +0.78% frequency deviation between the transducer driver and its resonance frequency |
| 00000 | 0.0% frequency deviation between the transducer driver and its resonance frequency |
| 11111 | -0.78% frequency deviation between the transducer driver and its resonance frequency |
| ... | |
| 10001 | -11.7% frequency deviation between the transducer driver and its resonance frequency |
| 10000 | -12.48% frequency deviation between the transducer driver and its resonance frequency |

The frequency deviation between driver frequency and transducer resonance frequency is transmitted as a complement on two. Each digit equals 0.78% frequency deviation. The value is valid after the 'SEND_WO_DAMP' command as well as after the 'SEND' command with EL_DAMP=0 has been executed.

Table 7.5.7-2: Read Status: Bit 5

| *Bit 5* | *Meaning* |
|---|---|
| 0 | Result of frequency measurement is invalid |
| 1 | Result of frequency measurement is valid |

Table 7.5.7-3: Read Status: Bit 6

| *Bit 6* | *Meaning* |
|---|---|
| 0 | Transducer driver output voltage not above $V_{DRV\_OK\_H}$ |
| 1 | Transducer driver output voltage above $V_{DRV\_OK\_H}$ |

Table 7.5.7-4: Read Status: Bit 7

| *Bit 7* | *Meaning* |
|---|---|
| 0 | Reset state or last threshold data reception incorrect, default data active |
| 1 | Last threshold data reception successful, transmitted threshold data active |

Table 7.5.7-5: Read Status: Bit 8

| *Bit 8* | *Meaning* |
|---|---|
| 0 | No noise detected during last measurement cycle |
| 1 | Noise detected during last measurement cycle |

The 'READ_STATUS' command timing diagram is shown in Figure 7.5.7-1. The transmission starts with bit 8.

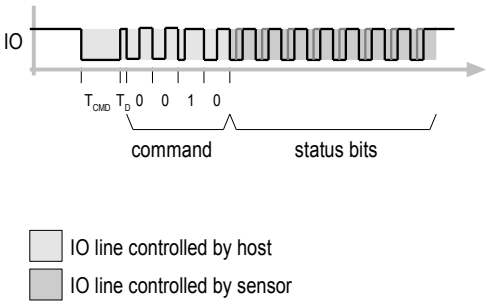



*Figure 7.5.7-1: READ_STATUS command*

### 7.5.8 'CAL_PULSES' command

To calibrate the internal oscillator to the required frequency two pulses with a defined interval of $T_{CAL}$ can be driven on the IO line. The interval starts and stops with a pulse of the width $T_{CALS}$. Due to the controlled slew rate, the ECU should observe the falling edge of the pulses. The following diagram shows the flow:

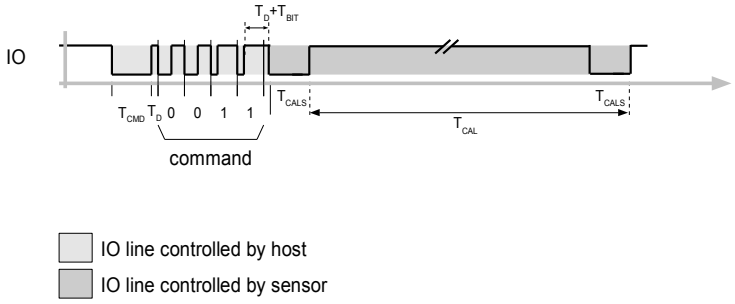



*Figure 7.5.8-1: Oscillator Calibration Pulse*

### 7.5.9 'READ_ECHO' command

The 'READ_ECHO' command returns an 8 bit value of the echo height of the first detected echo. The returned value is the maximum of the region when the signal line is above the threshold.

The returned value is the evaluation of the last 'SENDxx' or 'RECEIVE' command.

No echo results in a value of 0. Maximum echo amplitude results in a value of 255.

The command is depicted in Figure 7.5.9-1:

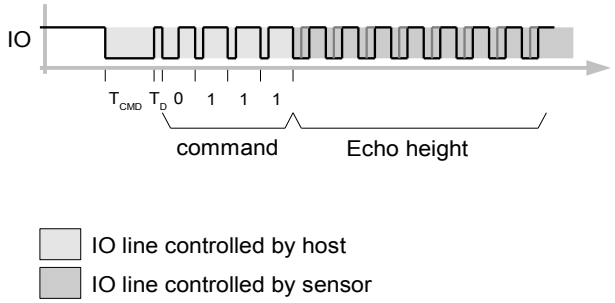



*Figure 7.5.9-1: 'READ_ECHO' command*

Two examples for echo height detection are depicted in the following figures:

**E524.05**

Figure 7.5.9-2 illustrates an example for the detection of the maximum echo for the E524.05. Besides the depicted 'SEND' command, with 'RECEIVE' or any other 'SEND' command the maximum of the first echo will be returned by the 'READ_ECHO' command.

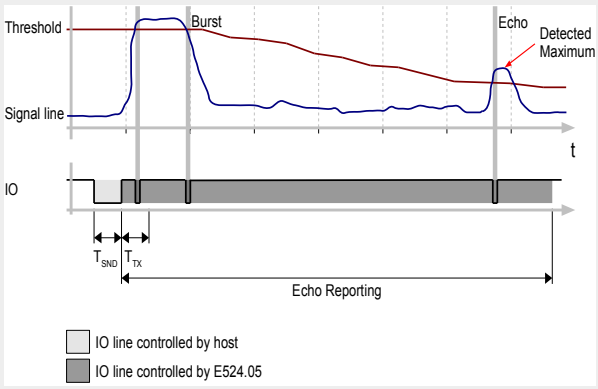



*Figure 7.5.9-2: E524.05 Echo height detection*

**E524.06**

Figure 7.5.9-3 illustrates an example for the detection of the maximum echo for the E524.06. Besides the depicted 'SEND' command, with 'RECEIVE' or any other 'SEND' command the maximum of the first echo will be returned by the 'READ_ECHO' command.

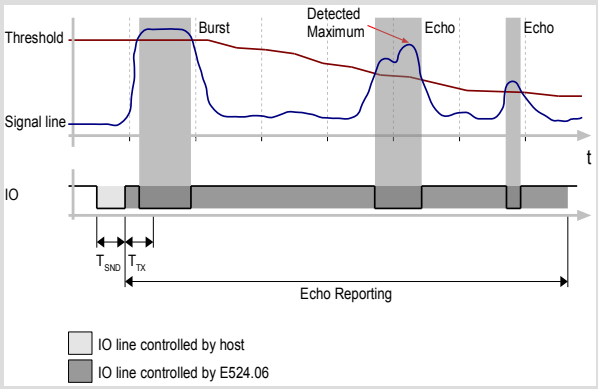



*Figure 7.5.9-3: E524.06 Echo height detection*

### 7.5.10 EEPROM Programming

The internal 32 bit EEPROM holds values for driver frequency, amplifier gain, noise analysis thresholds, electronic damping settings, driver supply voltage, number of pulses, comparator masking, RD and ATG activation. The programming and verification via the single IO pin is done in three steps. 'EE_WRITE' allows to pre-load initial settings. After calibration, 'EE_PROGRAM' stores the final settings in EEPROM. To verify successful programming, 'EE_READ' reads the register content back.
To achieve a valid programming, an 'EE_WRITE' must be sent before an 'EE_PROGRAM'.
Both E524.05 and E524.06 are shipped with factory default settings. After assembly with a transducer, the optimum values for driver frequency, amplifier gain, electronic damping, number of pulses and driver supply voltage are found in functional testing and calibration in the application of the customer. The EEPROM configuration is depicted in the following figure and table. The delivery state can be found in chapter 5.

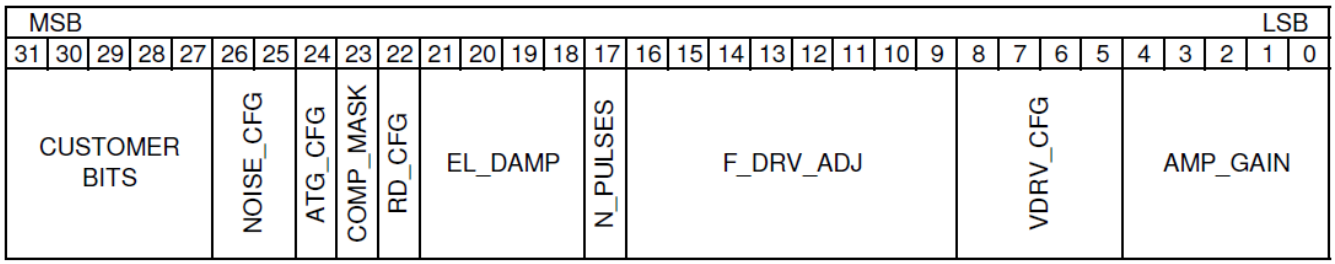



*Figure 7.5.10-1: EEPROM organisation*

Table 7.5.10-1: EEPROM Bits

| *Bit* | *No. Bits* | *Function* | *Description* |
|---|---|---|---|
| 27:31 | 5 | CUSTOMER BITS | free configurable |
| 26:25 | 2 | NOISE_CFG | Noise strategy:<br>'00': THRES14 and THRES_SCALE=3 fixed<br>'01': 62 fixed<br>'10': 124 fixed<br>'11': 620 fixed |
| 24 | 1 | ATG_CFG | Automatic threshold generation:<br>'0': off<br>'1': on |
| 23 | 1 | COMP_MASK | Comparator masking on IO line:<br>'0': not active<br>'1': active |
| 22 | 1 | RD_CFG | Damping resistor during ringing:<br>'0': off<br>'1': on |
| 21:18 | 4 | EL_DAMP | Electronic damping setting (nonlinear increment) |
| 17 | 1 | N_PULSES | Number of burst pulses:<br>'0': 10 pulses<br>'1': 16 pulses |
| 16:9 | 8 | F_DRV_ADJ | Driver frequency |
| 8:5 | 4 | VDRV_CFG | Transducer driver output voltage configuration |
| 4:0 | 5 | AMP_GAIN | Amplifier gain adjustment |

#### 7.5.10.1 'EE_WRITE' Command

As shown in Figure 7.5.10.1-1 in 'EE_WRITE', data bits follow directly after the command bits. The transmitted data bits overwrite previous EEPROM data, the new settings are valid for all functionality execpt the oscillator frequency. A new setting for the oscillator frequency impinge only on the command 'CAL_PULSES' before the command 'EE_PROGRAM' is executed. The first bit transmitted on the IO line is bit 31 (MSB of CUSTOMER BITS) and the last bit is bit 0 (LSB of AMP_GAIN).

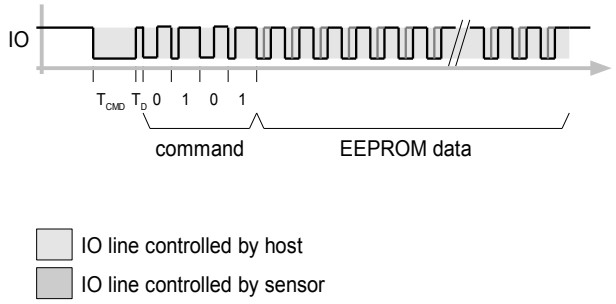



*Figure 7.5.10.1-1: EE_WRITE command*

#### 7.5.10.2 'EE_PROGRAM' Command

With the 'EE_PROGRAM' command, the EEPROM cells are programmed with the current register contents. After sending out the command, the voltage at the IO pin has to be raised to $V_{PROG}$ within $T_{VPROG}$. As shown in Figure 7.5.10.2-1, the programming time at pin IO is $T_{PROG}$.

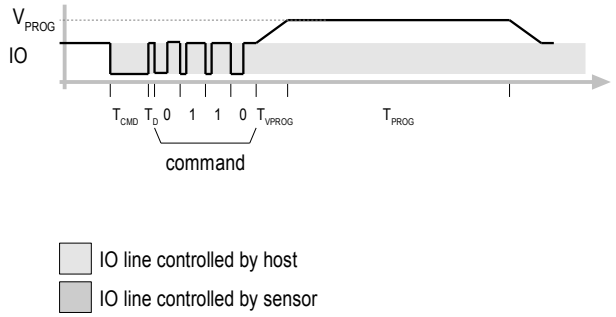



*Figure 7.5.10.2-1: EE_PROGRAM command*

#### 7.5.10.3 'EE_READ' Command

To verify successful programming, the 'EE_READ' command loads EEPROM data into registers and transmits the data at the IO pin, see Figure 7.5.10.3-1. The EEPROM data is read with a nominal, low and high read voltage and presented sequentially at the output IO indicating data integrity. Additionally, one VPROG_Status bit is appended to the end of the 31 EEPROM bits being read each time. The VPROG_Status contains the output of a comparator observing the programming voltage during programming. A high level shows the programming voltage has been within limits, a low levels indicates that the programming was not correct.
After power-on the VPROG_Status bit is '0'.

The first bit transmitted on the IO line is bit 31 (MSB of CUSTOMER BITS), the last bit is bit 0 (LSB of AMP_GAIN) and an additional bit 32 (VPROG_Status) with a nominal read voltage. The sequence is repeated with a low and a high read voltage. All in all 3 times (32+1) bit are transferred.

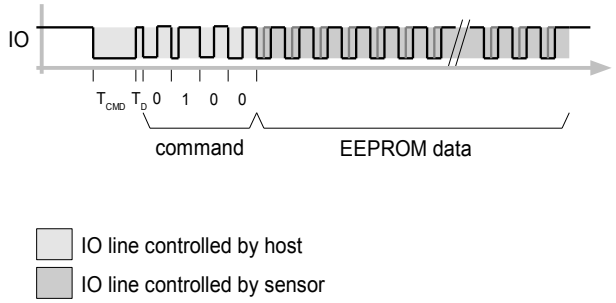



*Figure 7.5.10.3-1: EE_READ command*

#### 7.5.10.4 'EE_READ_SHADOW' command

To verify the data that has been written to the EEPROM shadow registers the 'EE_READ_SHADOW' command can be used. It transfers the contents of the shadow registers on the IO line.

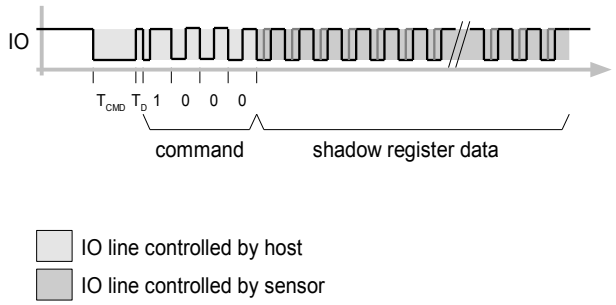



*Figure 7.5.10.4-1: EE_READ_SHADOW command*

#### 7.5.11 'READ_ID' command

A 24 bit chip ID is transferred on the IO line with the command 'READ_ID'. The MSB of the ID is transmitted first.

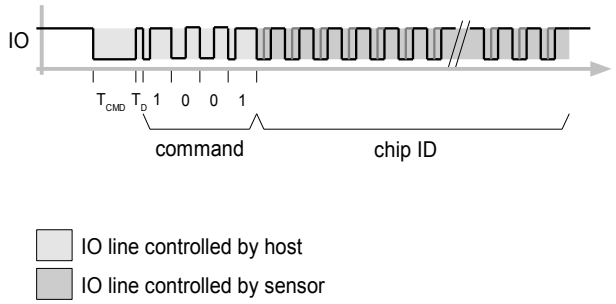



*Figure 7.5.11-1: 'READ_ID' command*

# 8 Typical Applications

## 8.1 Typical Application Circuit E524.05

The E524.05 supports a wide range of ultrasound transducers. Circuit diagrams may contain components not manufactured by Elmos Semiconductor AG, which are included as means of illustrating a typical application. Elmos Semiconductor does not endorse or warrant performance specifications beyond the Electrical Characteristics for the E524.05. Please contact Elmos Semiconductor for further assistance and application notes.

Figure 8.1-1 and Table 8.2-1 show the typical operating circuit and external components for the E524.05. The ECU and transducer assembly are connected with two wires VSUP_DATA and GND. Data is exchanged via shared supply line VSUP_DATA.

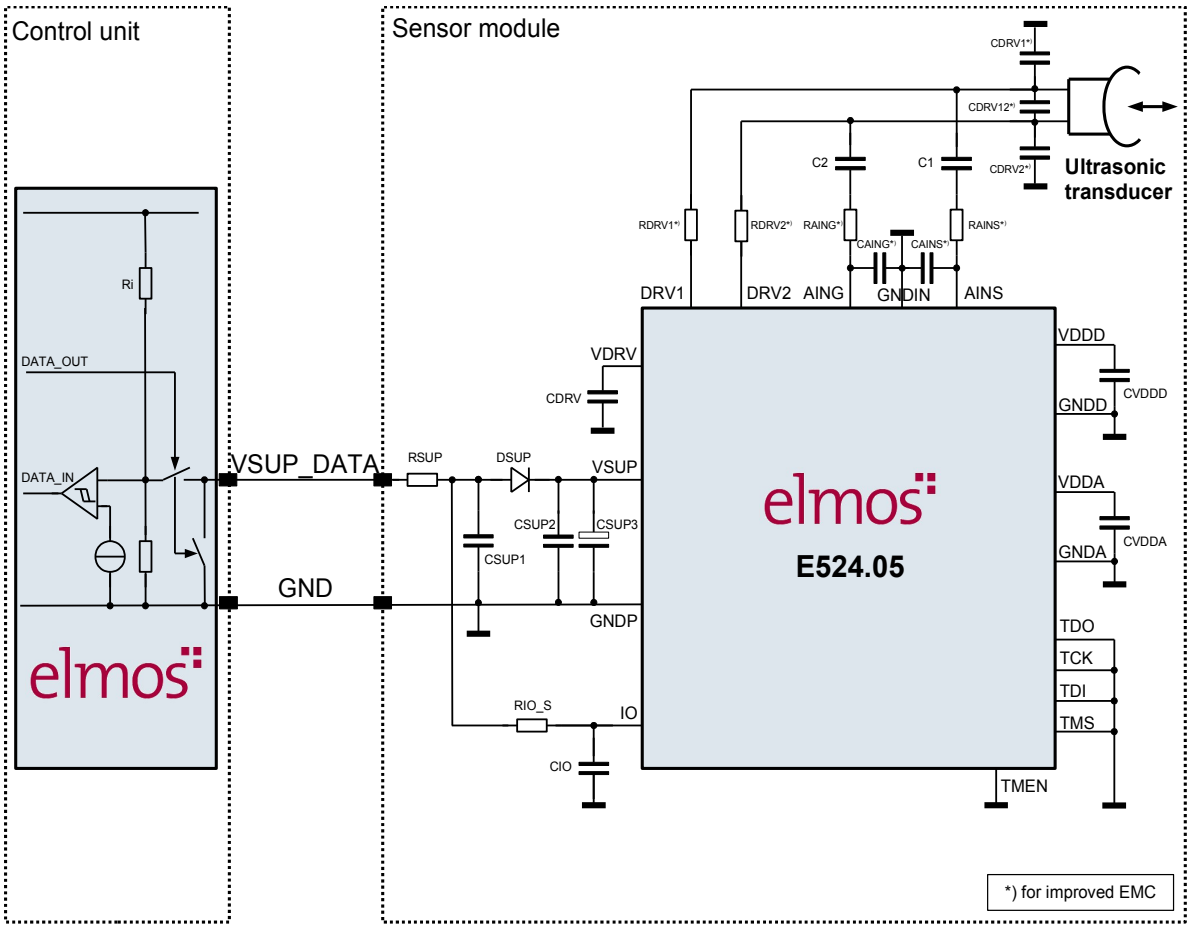



*Figure 8.1-1: Application Circuit E524.05*

## 8.2 External Components E524.05

Table 8.2-1: Device values E524.05

| No. | Description | Condition | Symbol | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|---|
| 1 | Serial resistor in supply line | | RSUP | 90 | 100 | 110 | Ω |
| 2 | Reverse polarity protection diode | BAS321 general purpose diode or equivalent | DSUP | 200 | | | $V_{Reverse}$ |
| 3 | Blocking capacitor for supply line | | CSUP1 | | 2.2 | | nF |
| 4 | Blocking capacitor for supply line | | CSUP2 | | 220 | | nF |
| 5 | Storage capacitor for supply line | | CSUP3 | | 10 | | µF |
| 6 | Storage capacitor for transducer driver | | CDRV | | 2.2 | 4.7 | µF |
| 7 | Serial resistor for IO line | 5%, 1/8W | RIO_S | 135 | 150 | 165 | Ω |
| 8 | Capacitor for IO line | 10% | CIO | 3.2 | 4.7 | 6.2 | nF |
| 9 | Blocking capacitor for analog supply | 10%, 50V, ESR < 0.2Ω at 1MHz | CVDDA | 70 | 100 | 130 | nF |
| 10 | Blocking capacitor for digital supply | 10%, 50V, ESR < 0.2Ω at 1MHz | CVDDD | 70 | 100 | 130 | nF |
| 11 | AC coupling capacitor for transducer signal | | C1 | | 470 | | pF |
| 12 | AC coupling capacitor for transducer signal | | C2 | | 470 | | pF |
| 13 | Filter resistor for improved EMC | depends on PCB layout | RAING | | 47 | | Ω |
| 14 | Filter resistor for improved EMC | depends on PCB layout | RAINS | | 47 | | Ω |
| 15 | Filter capacitor for improved EMC | depends on PCB layout | CAING | | - | | pF |
| 16 | Filter capacitor for improved EMC | depends on PCB layout | CAINS | | - | | pF |
| 17 | Filter capacitor for improved EMC | depends on PCB layout | CDRV1 | | - | | pF |
| 18 | Filter capacitor for improved EMC | depends on PCB layout | CDRV2 | | 220 | | pF |
| 19 | Filter capacitor for improved EMC | depends on PCB layout | CDRV12 | | 220 | | pF |
| 20 | Filter resistor for improved EMC | depends on PCB layout | RDRV1 | | 100 | | Ω |
| 21 | Filter resistor for improved EMC | depends on PCB layout | RDRV2 | | 0 | | Ω |
| 22 | Transducer | e.g. Murata | Ultrasonic transducer | | 58 | | kHz |

## 8.3 Typical Application Circuit E524.06

The E524.06 supports a wide range of ultrasound transducers. Circuit diagrams may contain components not manufactured by Elmos Semiconductor AG, which are included as means of illustrating a typical application. Elmos Semiconductor does not endorse or warrant performance specifications beyond the Electrical Characteristics for the E524.06. Please contact Elmos Semiconductor for further assistance and application notes.

The typical operational circuit for the E524.06 is shown in Figure 8.3-1, Table 8.4-1 lists external components. Three wires (GND, VSUP and DATA) connect ECU and ultrasonic module.

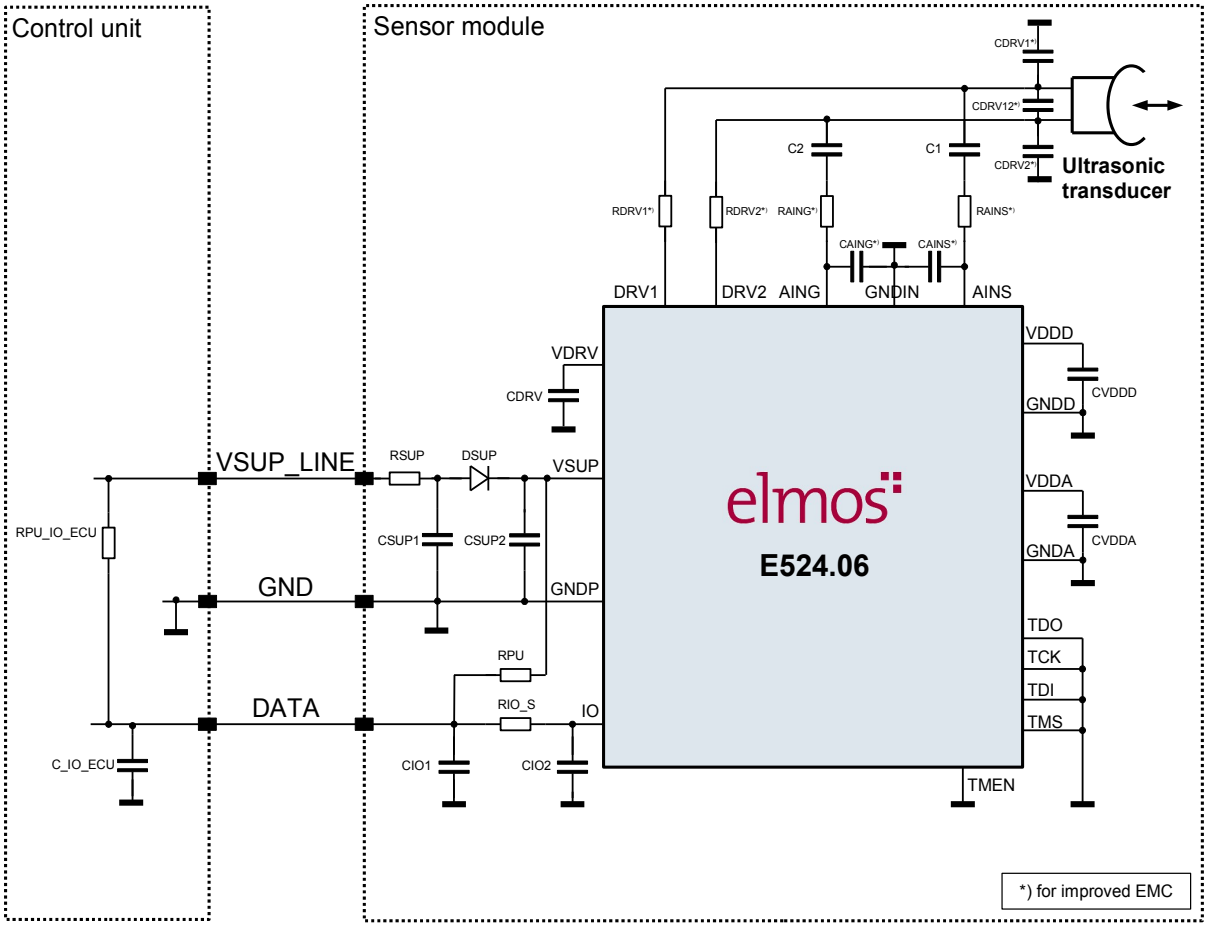



*Figure 8.3-1: Application Circuit E524.06*

## 8.4 External Components E524.06

Table 8.4-1: Device values E524.06

| No. | Description | Condition | Symbol | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|---|
| 1 | Serial resistor in supply line | | RSUP | 90 | 100 | 110 | Ω |
| 2 | Reverse polarity protection diode | BAS321 general purpose diode or equivalent | DSUP | 200 | | | $V_{Reverse}$ |
| 3 | Blocking capacitor for supply line | | CSUP1 | | 2.2 | | nF |
| 4 | Blocking capacitor for supply line | | CSUP2 | | 220 | | nF |
| 5 | Storage capacitor for transducer driver | | CDRV | | 2.2 | 4.7 | µF |
| 6 | Serial resistor for IO line | 5%, 1/8W | RIO_S | 0.9 | 1 | 1.1 | kΩ |
| 7 | Capacitor for IO line | 5% | CIO1 | 230 | 330 | 430 | pF |
| 8 | Capacitor for IO line | 10% | CIO2 | 1.5 | 2.2 | 2.9 | nF |
| 9 | Blocking capacitor for analog supply | 10%, 50V, ESR < 0.2Ω at 1MHz | CVDDA | 70 | 100 | 130 | nF |
| 10 | Blocking capacitor for digital supply | 10%, 50V, ESR < 0.2Ω at 1MHz | CVDDD | 70 | 100 | 130 | nF |
| 11 | AC coupling capacitor for transducer signal | | C1 | | 470 | | pF |
| 12 | AC coupling capacitor for transducer signal | | C2 | | 470 | | pF |
| 13 | Pull up resistor | [1)] | RPU | | 5 | | kΩ |
| 14 | Filter resistor for improved EMC | depends on PCB layout | RAING | | 47 | | Ω |
| 15 | Filter resistor for improved EMC | depends on PCB layout | RAINS | | 47 | | Ω |
| 16 | Filter capacitor for improved EMC | depends on PCB layout | CAING | | - | | pF |
| 17 | Filter capacitor for improved EMC | depends on PCB layout | CAINS | | - | | pF |
| 18 | Filter capacitor for improved EMC | depends on PCB layout | CDRV1 | | - | | pF |
| 19 | Filter capacitor for improved EMC | depends on PCB layout | CDRV2 | | 220 | | pF |
| 20 | Filter capacitor for improved EMC | depends on PCB layout | CDRV12 | | 220 | | pF |
| 21 | Filter resistor for improved EMC | depends on PCB layout | RDRV1 | | 100 | | Ω |
| 22 | Filter resistor for improved EMC | depends on PCB layout | RDRV2 | | 0 | | Ω |
| 23 | Transducer | e.g. Murata | Ultrasonic transducer | | 58 | | kHz |

[1)] RPU must be chosen with respect to RPU_IO_ECU (e.g. 10kΩ // 10kΩ). The external elements should be chosen to set the rising edge and the falling edge of the communication via IO to the same slope.

# 9 Package Reference

The IC is available in a Pb free, RoHs compliant, QFN20L4 plastic package. Package outline and dimensions are according to JEDEC MO-220 K, variant VGGD-5.

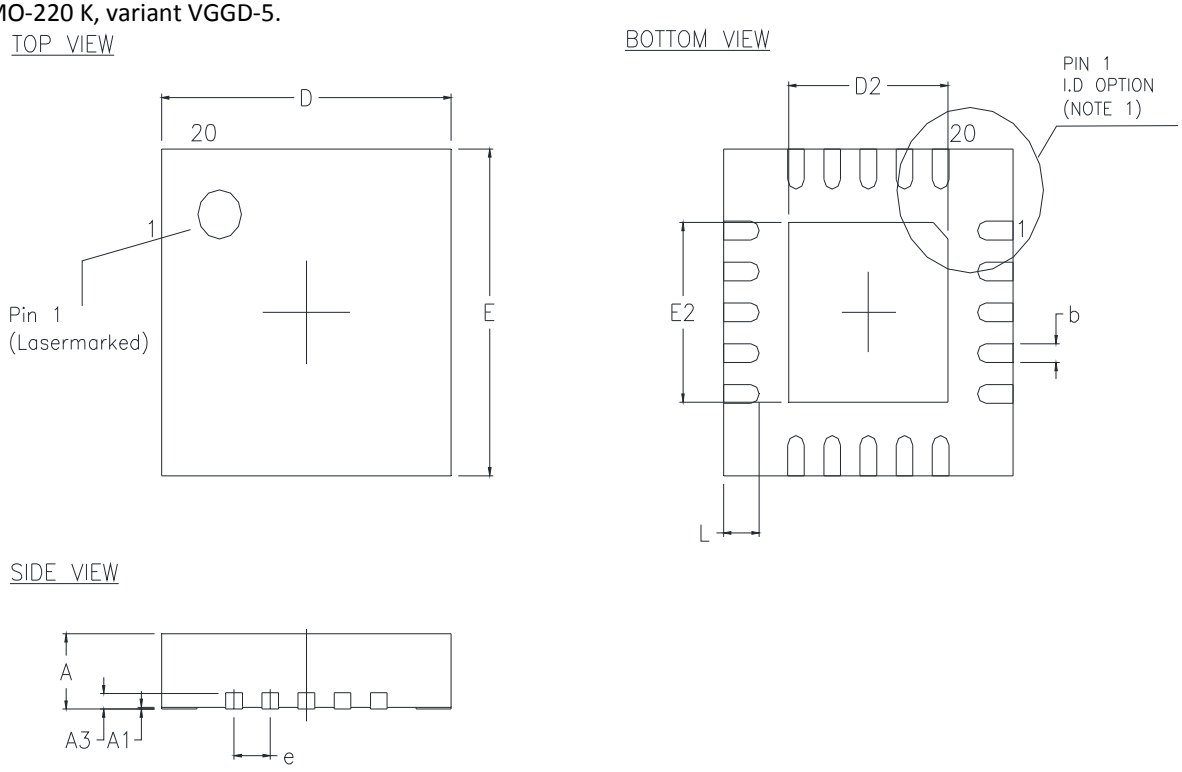



*Figure 9-1: Package Outline*

**Note 1:** Typical thermal resistance junction to ambient Rth,ja is 45 °C/W, based on JEDEC standard JESD-51-2 (still air), JESD-51-5 (exposed pad soldered to PCB with thermal via's) and JESD-51-7 (4-layer PCB).
**Note 2:** Contact factory for specific location and type of pin 1 identification.

Table 9-1: Package Dimensions

| ***Description*** | ***Symbol*** | | ***mm*** | | | ***inch*** | |
|---|---|---|---|---|---|---|---|
| | | **min** | **typ** | **max** | **min** | **typ** | **max** |
| Package height | A | 0.80 | 0.90 | 1.00 | 0.031 | 0.035 | 0.039 |
| Stand off | A1 | 0.00 | 0.02 | 0.05 | 0.000 | 0.00079 | 0.002 |
| Thickness of terminal leads, including lead finish | A3 | -- | 0.20 REF | -- | -- | 0.0079 REF | -- |
| Width of terminal leads | b | 0.18 | 0.25 | 0.30 | 0.0071 | 0.0098 | 0.012 |
| Package length / width | D / E | -- | 4.00 BSC | -- | -- | 0.157 BSC | -- |
| Length /width of exposed pad | D2 / E2 | 2.50 | 2.65 | 2.80 | 0.098 | 0.104 | 0.110 |
| Lead pitch | e | -- | 0.5 BSC | -- | -- | 0.020 BSC | -- |
| Length of terminal for soldering to sub-strate | L | 0.35 | 0.40 | 0.45 | 0.013 | 0.016 | 0.018 |
| Number of terminal positions | N | | 20 | | | 20 | |

**Note:** The mm values are valid, the inch values contain rounding errors.

# 10 Marking

## 10.1 Top Side

Table 10.1-1: Top Side

| |
|---|
| Elmos (optional) |
| 52405A or 52406A (optional) |
| XXXXU |
| YWW*# |

Table 10.1-2: Marking of the Devices

| ***Signature*** | ***Explanation*** |
|---|---|
| 52405 or 52406 | Elmos project number |
| A | Elmos project revision number |
| XXXX | Production lot number |
| U | Assembler Code |
| YWW | Year and week of assembly |
| * | Mask revision code |
| # | Elmos internal code |

## 10.2 Bottom Side

No marking

# 11 Reliability

## 11.1 Eeprom Data Retention

The data retention for the Eeprom within the given profile shown in Table 11.1-1 is statistically ensured according to AEC Q-100.

Table 11.1-1: Eeprom mission profile

| *Junction Temperature in [°C]* | *Operation Life Time in [h]* | *Storage Time in [a]* | *Comment* |
|---|---|---|---|
| -40 | 480 | | Operation mission profile |
| 23 | 1600 | | |
| 40 | 5200 | | |
| 80 | 640 | | |
| 95 | 80 | | |
| 105 | 50 | | |
| | | | |
| 23 | | 10 | In production standby |
| 85 | | 5 | |
| | | | |
| 23 | | 10 | After market storage |
| 95 | | 5 | |
| | 8000 | 30 | Sum |

# 12 Storage, Handling, Packing and Shipping

## 12.1 Storage

Storage conditions should not exceed those given in Chapter 2 Absolute Maximum Ratings.
The Moisture Sensitivity Level is specified according to MSL3 (JEDEC J-STD-020X in its valid revision).

## 12.2 Handling

Devices are sensitive to damage by Electrostatic Discharge (ESD) and should only be handled at an ESD protected workstation.

Handling conditions should not exceed those given in Chapter 2 Absolute Maximum Ratings.

## 12.3 Packing

Material shall be packed for shipment as follows:

- Tape-on-Reel
- Drybag for MPC samples
- Every reel respectively drybag will be packed in a packing carton. Each packing carton will be marked and sealed by using the standard label for packings.

## 12.4 Shipping

Each delivery shall be accompanied by the following:

- Certificate of conformance to the specification
- Delivery note

# 13 Contents

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## Illustration Index

# 14 General

## 14.1 WARNING - Life Support Applications Policy

Elmos Semiconductor AG is continually working to improve the quality and reliability of its products. Nevertheless, semiconductor devices in general can malfunction or fail due to their inherent electrical sensitivity and vulnerability to physical stress. It is the responsibility of the buyer, when utilizing Elmos Semiconductor AG products, to observe standards of safety, and to avoid situations in which malfunction or failure of an Elmos Semiconductor AG Product could cause loss of human life, body injury or damage to property. In development your designs, please ensure that Elmos Semiconductor AG products are used within specified operating ranges as set forth in the most recent product specifications.

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## 14.3 Application Disclaimer

Circuit diagrams may contain components not manufactured by Elmos Semiconductor AG, which are included as means of illustrating typical applications. Consequently, complete information sufficient for construction purposes is not necessarily given. The information in the application examples has been carefully checked and is believed to be entirely reliable. However, no responsibility is assumed for inaccuracies. Furthermore, such information does not convey to the purchaser of the semiconductor devices described any license under the patent rights of Elmos Semiconductor AG or others.

## 14.4 Contact Info

Table 14.4-1: Contact Information

| | |
|---|---|
| **Headquarters**<br>Elmos Semiconductor AG<br>Heinrich-Hertz-Str. 1,<br>D-44227 Dortmund (Germany)<br>www.elmos.com | Phone: +49 (0) 231 / 75 49-100<br>Fax: +49 (0) 231 / 75 49-149<br>sales-germany@elmos.com |
| **Sales and Application Support Office North America**<br>Elmos NA. Inc.<br>32255 Northwestern Highway, Suite 220<br>Farmington Hills, MI 48334 (USA) | Phone: +1 (0) 248 / 8 65 32 00<br>Fax: +1 (0) 248 / 8 65 32 03<br>sales-usa@elmos.com |
| **Sales and Application Support Office Korea**<br>Elmos Korea<br>B-1007, U-Space 2, #670 Daewangpangyo-ro,<br>Sampyoung-dong, Bunddang-gu, Sungnam-si<br>Kyounggi-do 463-400 Korea | Phone: +82 (0) 31 / 7 14 11 31<br>sales-korea@elmos.com |
| **Sales and Application Support Office Japan**<br>Elmos Japan K.K.<br>BR Shibaura N Bldg. 7F<br>3-20-9 Shibaura, Minato-ku, Tokyo 108-0023 Japan | Phone: +81 3 / 3451-7101<br>Fax: +81 3 / 3451-7104<br>sales-japan@elmos.com |
| **Sales and Application Support Office China**<br>Elmos Semiconductor Technology (Shanghai) Co., Ltd.<br>Unit 16B, 16F Zhao Feng World Trade Building,<br>No. 369 Jiang Su Road,<br>Chang Ning District, Shanghai, PR China, 200050 | Phone: +86 (0) 21 / 6210 0908<br>Fax: +86 (0) 21 / 6219 7502<br>sales-china@elmos.com |
| **Sales and Application Support Office Singapore**<br>Elmos Semiconductor Singapore Pte Ltd.<br>3A International Business Park,<br>#09-13 ICON@IBP, Singapore 609935 | Phone: +65 (0) 690 / 8 12 61<br>Fax: +65 (0) 6570 / 5906<br>sales-singapore@elmos.com |