

A decorative graphic on the left side of the slide consists of two overlapping parallelograms. The front one is blue and the back one is light green. They are positioned diagonally, with the blue one partially covering the green one.

Graphical Processing Unit

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Motivation

- Computer Architecture Design Pattern
- GPU and CPU
- Outperform Microblaze



Our Solution

- General but Dedicated Soft GPU
- Advanced Shading Algorithms
- Networking



Implementation

- General but Dedicated Soft GPU
 - Scalable
 - 16 Threads, 32 Warps, 1 Thread Block
 - ISA
 - 60 Instructions
 - 64 Integer, 64 Floating Point Reg



Implementation

- General but Dedicated Soft GPU
 - Score-board RF Dependency Tracker
 - Single Dispatch
 - Resolve Branch Divergence within one Warp using Execution Masks



Implementation

- Advanced Shading Algorithm
 - Partial Compiler Toolchain
 - Glsl to Custom ISA Assembly
 - Scalable for Advanced Shading Algorithms
 - Vertex Shader
 - Pixel Shader



Implementation

- Networking
 - Server Receives Instructions
 - Computation
 - Sends Rendered Frames to Client
 - Client Displays



Progress

- Implementation
 - ~5k Lines of Handwritten System Verilog
 - Fully Tested in Simulation
 - Syntax Migration to Vivado in progress
 - Fully Tested Networking Layer

Progress (Partial)

```
Feiyus-MacBook-Pro:meowGPU feiyuren$ wc -l assembler/*.py
 53 assembler/assembler.py
 16 assembler/assembler_util.py
195 assembler/assembly_fncode_parser.py
134 assembler/assembly_operand_parser.py
 88 assembler/codegen.py
107 assembler/isa.py
164 assembler/meow_driver.py
757 total
```

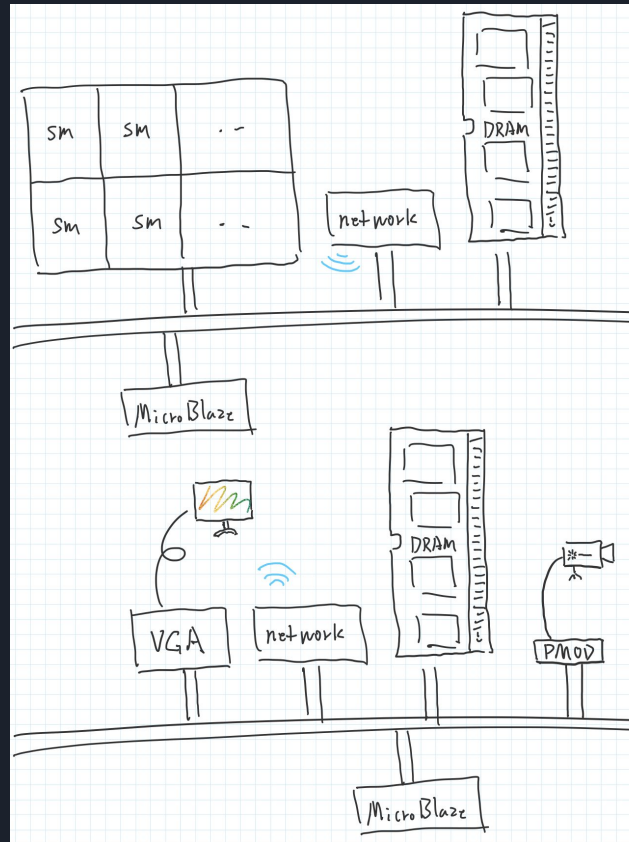
```
Feiyus-MacBook-Pro:meowGPU feiyuren$ wc -l verilator/*.*
137 verilator/SigDriver.hpp
 32 verilator/TestBenchBase.hpp
 97 verilator/TrrArbiter.cpp
 97 verilator/TrrArbiterHybrid.cpp
 10 verilator/tIntResvStation.cpp
 78 verilator/tRam.cpp
 48 verilator/tb_fma.cpp
 37 verilator/template.cpp
151 verilator/top.cpp
 33 verilator/tregFile.cpp
720 total
```

```
Feiyus-MacBook-Pro:meowGPU feiyuren$ wc -l hardware/*
 51 hardware/BranchUnit.sv
135 hardware/ContextManager.sv
521 hardware/Core.sv
231 hardware/DRAM_sim.sv
276 hardware/Decoder.sv
105 hardware/DispatchUnit.sv
137 hardware/DispatchUnitSimple.sv
140 hardware/FMA_sim.sv
 89 hardware/FPExecPipeline.sv
212 hardware/ISA.svh
 18 hardware/InstrIOQueue.sv
 53 hardware/InstrMemSim.sv
 74 hardware/InstrRingCache.sv
162 hardware/IntExecPipeline.sv
 51 hardware/MapTable.sv
121 hardware/OperandCollector.sv
 22 hardware/OperandCollectorSimple.sv
112 hardware/Pipe.sv
 53 hardware/RamP2.sv
 54 hardware/RamP3.sv
273 hardware/ResvStation.sv
259 hardware/ScoreBoard.sv
 26 hardware/WBBroadcast.svh
 23 hardware/WBQueue.sv
 77 hardware/Writeback.sv
 80 hardware/WritebackSimple.sv
 19 hardware/asm.mem
 14 hardware/asm2.mem
 32 hardware/clz.sv
 32 hardware/ctz.sv
 78 hardware/gDefine.svh
 63 hardware/hex_memory_file.mem
 54 hardware/instr.txt
 35 hardware/instr2.txt
 19 hardware/instr_memory_file.mem
18 hardware/interfaces.svh
 17 hardware/ioQueue.sv
 8 hardware/lsQueue.sv
 28 hardware/priArbiter.sv
 41 hardware/rrArbiter.sv
 44 hardware/rrArbiterDec.sv
 46 hardware/rrArbiterHybrid.sv
3903 total
```



GPU

Feiyu Ren



Functional Block Diagram



Implementation

- Thread, Warp, Thread Block
- Instruction Dispatch and Latency

Hiding



Implementation

- Execution Mask
- Score-board RF Dependency Tracking



Client Side, Networking, ISA Compiler Support

Lichen Liu



Client Side

- VGA display
 - Resolution 640 x 480
 - May need to downscale for ethernet bandwidth concern



Networking

- Server and Client Communication
 - Still/animated images
- Using TCP for now
- but it seems...



TCP Connection Issue





TCP Connection Issue

- Very Slow...
- Takes 2.91 second to send an image
 - $640 * 480 * 4$ bytes
 - 422,268 bytes/second
 - 3.22 Mbps



TCP Connection Issue Solutions

- Switch to UDP
- Lower image resolution
- Or display still image rather than animation



Compiler Support for custom ISA

- Compiler:
 - Gsl to Custom ISA Assembly Language
 - WIP
 - Ported from project in another course...
- Assembler
 - Custom ISA Assembly to machine code

Questions?

