

# HD74LS273

## Octal D-type Positive-edge-triggered Flip-Flops (with Clear)

REJ03D0473-0300  
Rev.3.00  
Jul.15.2005

The HD74LS273, positive-edge-triggered flip-flops utilize LS TTL circuitry to implement D-type flip-flop logic with a direct clear input.

Information at the D inputs meeting the setup time requirements is transferred to the Q outputs on the positive-going edge of the clock pulse.

When the clock input is at either the high or low level, the D input signal has no effect at the output.

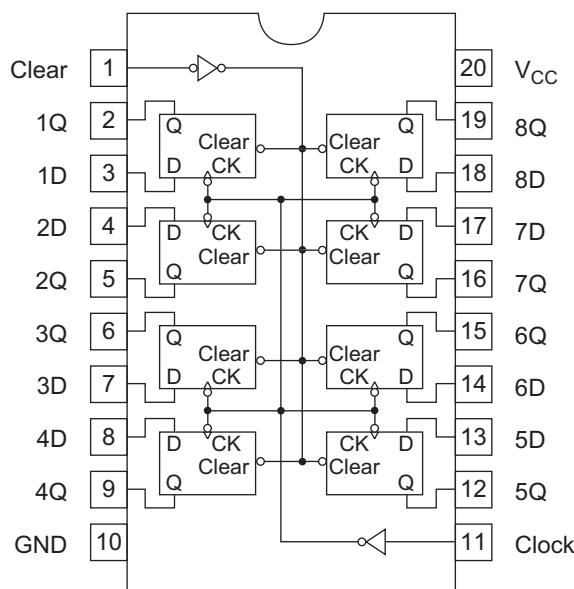
### Features

- Ordering Information

Part Name	Package Type	Package Code (Previous Code)	Package Abbreviation	Taping Abbreviation (Quantity)
HD74LS273P	DILP-20 pin	PRDP0020AC-B (DP-20NEV)	P	—
HD74LS273FPEL	SOP-20 pin (JEITA)	PRSP0020DD-B (FP-20DAV)	FP	EL (2,000 pcs/reel)
HD74LS273RPEL	SOP-20 pin (JEDEC)	PRSP0020DC-A (FP-20DBV)	RP	EL (1,000 pcs/reel)

Note: Please consult the sales office for the above package availability.

### Pin Arrangement



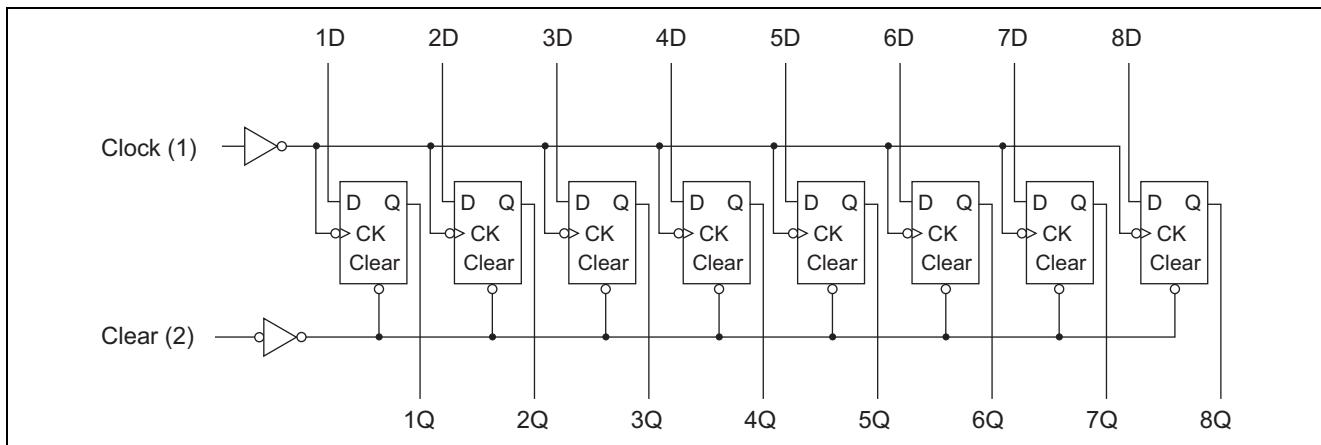
(Top view)

**Function Table**

Inputs			Output
Clear	Clock	D	Q
L	X	X	L
H	↑	H	H
H	↑	L	L
H	L	X	Q <sub>0</sub>

Notes: H; high level, L; low level, X; irrelevant

↑; transition from low to high level

Q<sub>0</sub>; level of Q before the indicated steady-state input conditions were established.**Block Diagram****Absolute Maximum Ratings**

Item	Symbol	Ratings	Unit
Supply voltage	V <sub>CC</sub>	7	V
Input voltage	V <sub>IN</sub>	7	V
Power dissipation	P <sub>T</sub>	400	mW
Storage temperature	T <sub>STG</sub>	-65 to +150	°C

Note: Voltage value, unless otherwise noted, are with respect to network ground terminal.

**Recommended Operating Conditions**

Item	Symbol	Min	Typ	Max	Unit
Supply voltage	V <sub>CC</sub>	4.75	5.00	5.25	V
Output current	I <sub>OH</sub>	—	—	-400	μA
	I <sub>OL</sub>	—	—	8	mA
Operating temperature	T <sub>OPR</sub>	-20	25	75	°C
Clock frequency	f <sub>CLOCK</sub>	0	—	30	MHz
Clock pulse width	t <sub>w</sub> (clock)	20	—	—	ns
Clear pulse width	t <sub>w</sub> (clear)	20	—	—	ns
Data setup time	t <sub>su</sub> (data)	20↑	—	—	ns
Clear (inactive-state) setup time	t <sub>su</sub> (clear)	25↑	—	—	ns
Data hold time	t <sub>h</sub> (data)	5↑	—	—	ns

## Electrical Characteristics

(Ta = -20 to +75 °C)

Item	Symbol	min.	typ.*	max.	Unit	Condition	
Input voltage	V <sub>IH</sub>	2.0	—	—	V		
	V <sub>IL</sub>	—	—	0.8	V		
Output voltage	V <sub>OH</sub>	2.7	—	—	V	V <sub>CC</sub> = 4.75 V, V <sub>IH</sub> = 2 V, V <sub>IL</sub> = 0.8 V, I <sub>OH</sub> = -400 μA	
	V <sub>OL</sub>	—	—	0.5	V	I <sub>OL</sub> = 8 mA	V <sub>CC</sub> = 4.75 V, V <sub>IH</sub> = 2 V,
		—	—	0.4		I <sub>OL</sub> = 4 mA	V <sub>IL</sub> = 0.8 V
Input current	I <sub>IH</sub>	—	—	20	μA	V <sub>CC</sub> = 5.25 V, V <sub>I</sub> = 2.7 V	
	I <sub>IL</sub>	—	—	-0.4	mA	V <sub>CC</sub> = 5.25 V, V <sub>I</sub> = 0.4 V	
	I <sub>I</sub>	—	—	0.1	mA	V <sub>CC</sub> = 5.25 V, V <sub>I</sub> = 7 V	
Short-circuit output current	I <sub>OS</sub>	-20	—	-100	mA	V <sub>CC</sub> = 5.25 V	
Supply current	I <sub>CC</sub> **	—	17	27	mA	V <sub>CC</sub> = 5.25 V	
Input clamp voltage	V <sub>IK</sub>	—	—	-1.5	V	V <sub>CC</sub> = 4.75 V, I <sub>IN</sub> = -18 mA	

Notes: \* V<sub>CC</sub> = 5 V, Ta = 25°C\*\* With all outputs open and 4.5 V applied to all data and clear inputs, I<sub>CC</sub> is measured after a momentary ground, then 4.5 V is applied to clock.

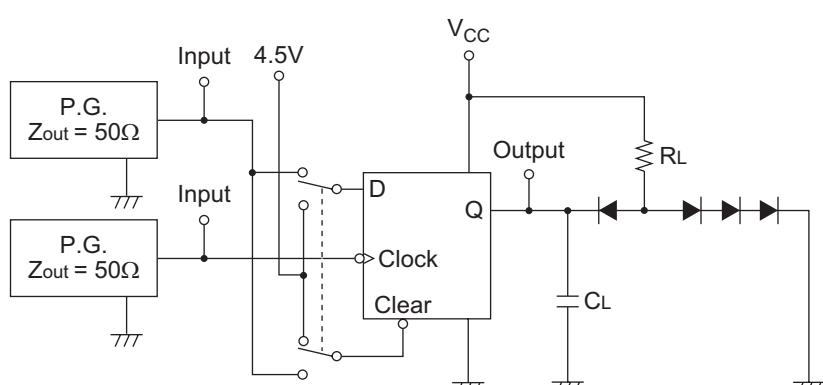
## Switching Characteristics

(V<sub>CC</sub> = 5 V, Ta = 25°C)

Item	Symbol	Inputs	min.	typ.	max.	Unit	Condition
Maximum clock frequency	f <sub>max</sub>	Clock	30	40	—	MHz	C <sub>L</sub> = 15 pF, R <sub>L</sub> = 2 kΩ
Propagation delay time	t <sub>PHL</sub>	Clear	—	18	27	ns	
	t <sub>PLH</sub>	Clock	—	17	27		
	t <sub>PHL</sub>		—	18	27		

## Testing Method

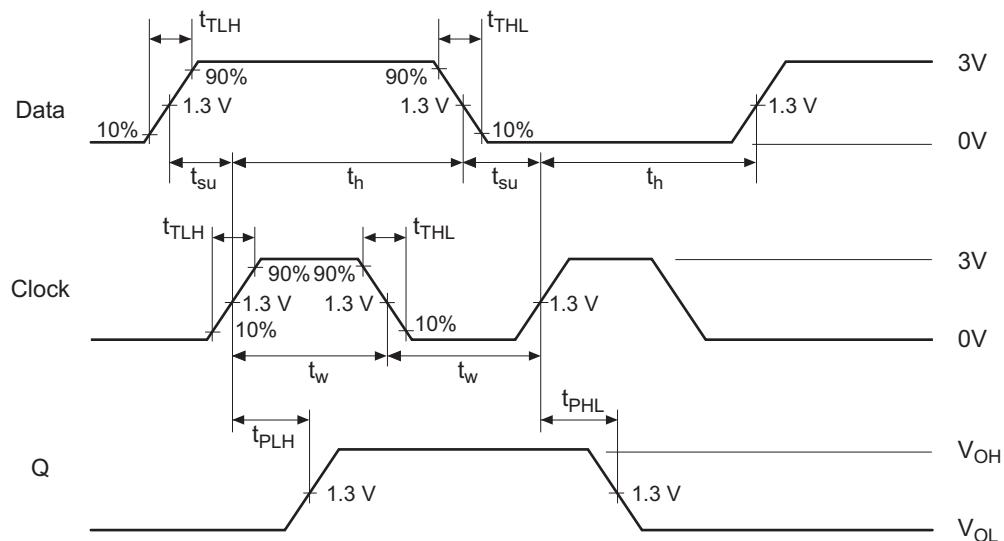
### Test Circuit



Notes:

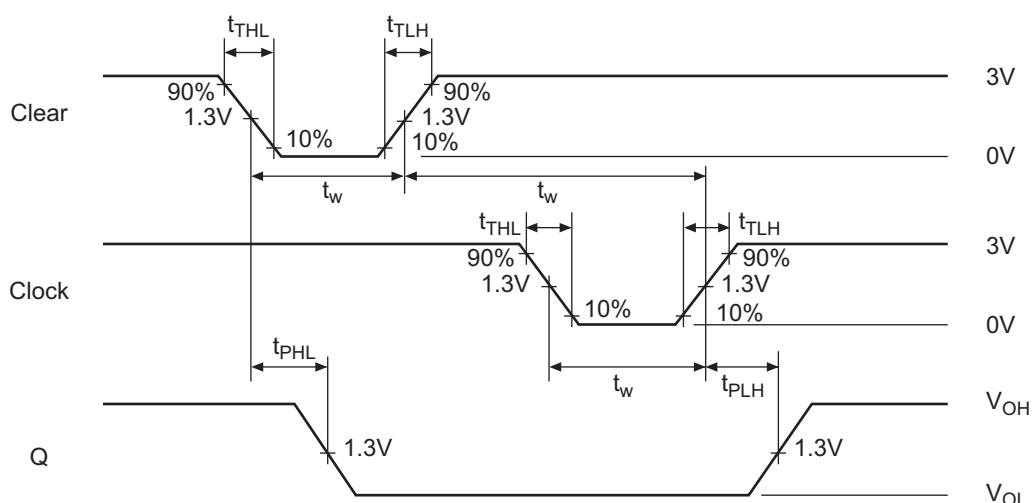
1. C<sub>L</sub> includes probe and jig capacitance.
2. All diodes are 1S2074(H).

## Waveforms 1



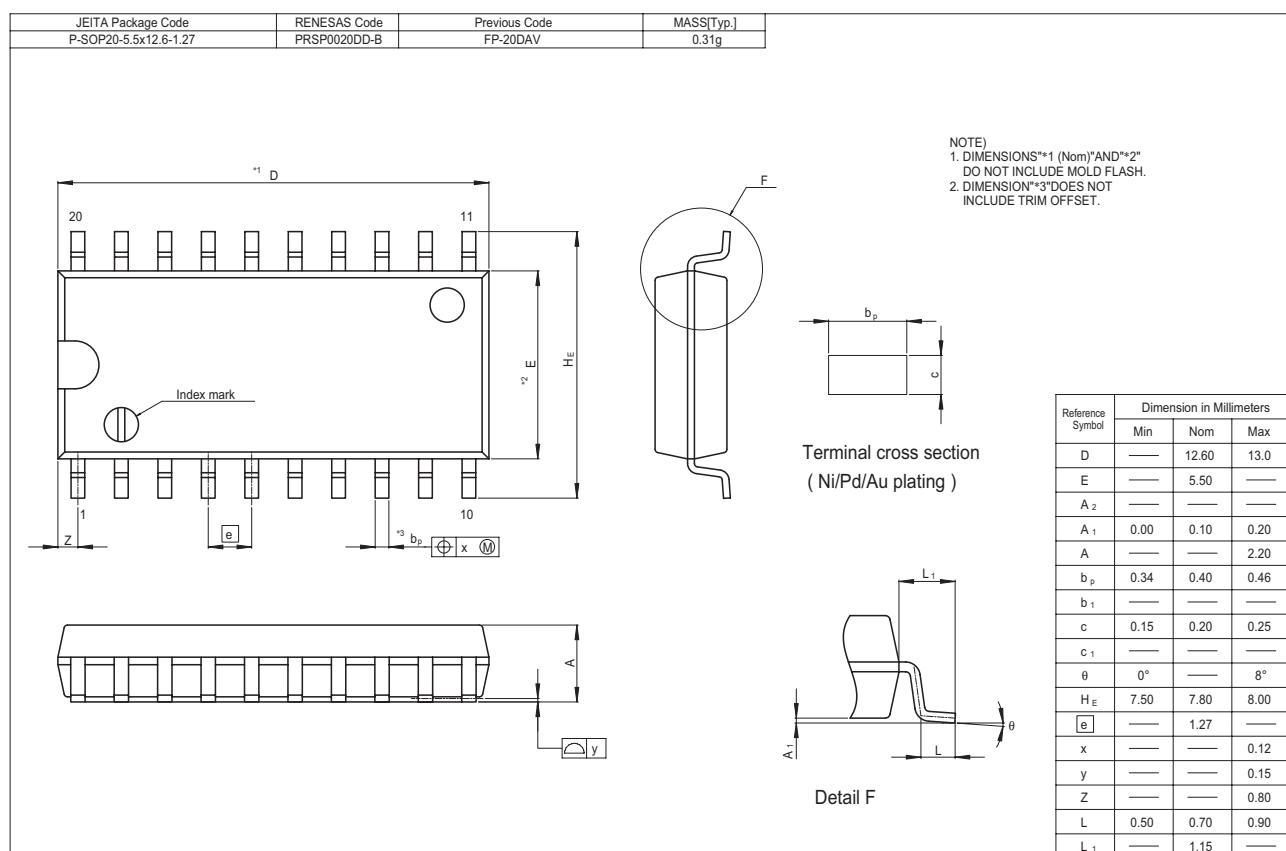
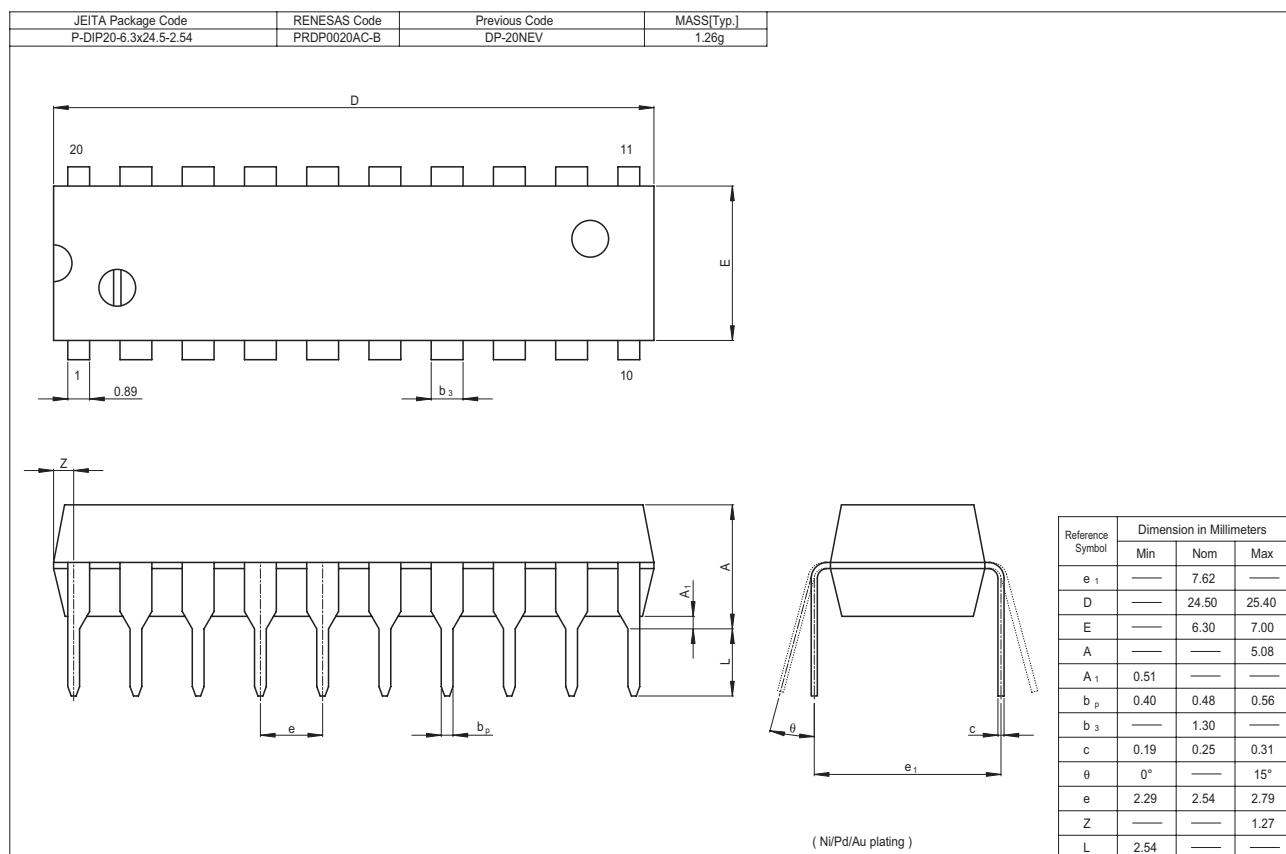
Notes: Input pulse;  $t_{TLH} \leq 15$  ns,  $t_{THL} \leq 6$  ns,  
Clock input; PRR = 1 MHz, duty cycle 50%  
Data input; PRR = 500 kHz, duty cycle 50%

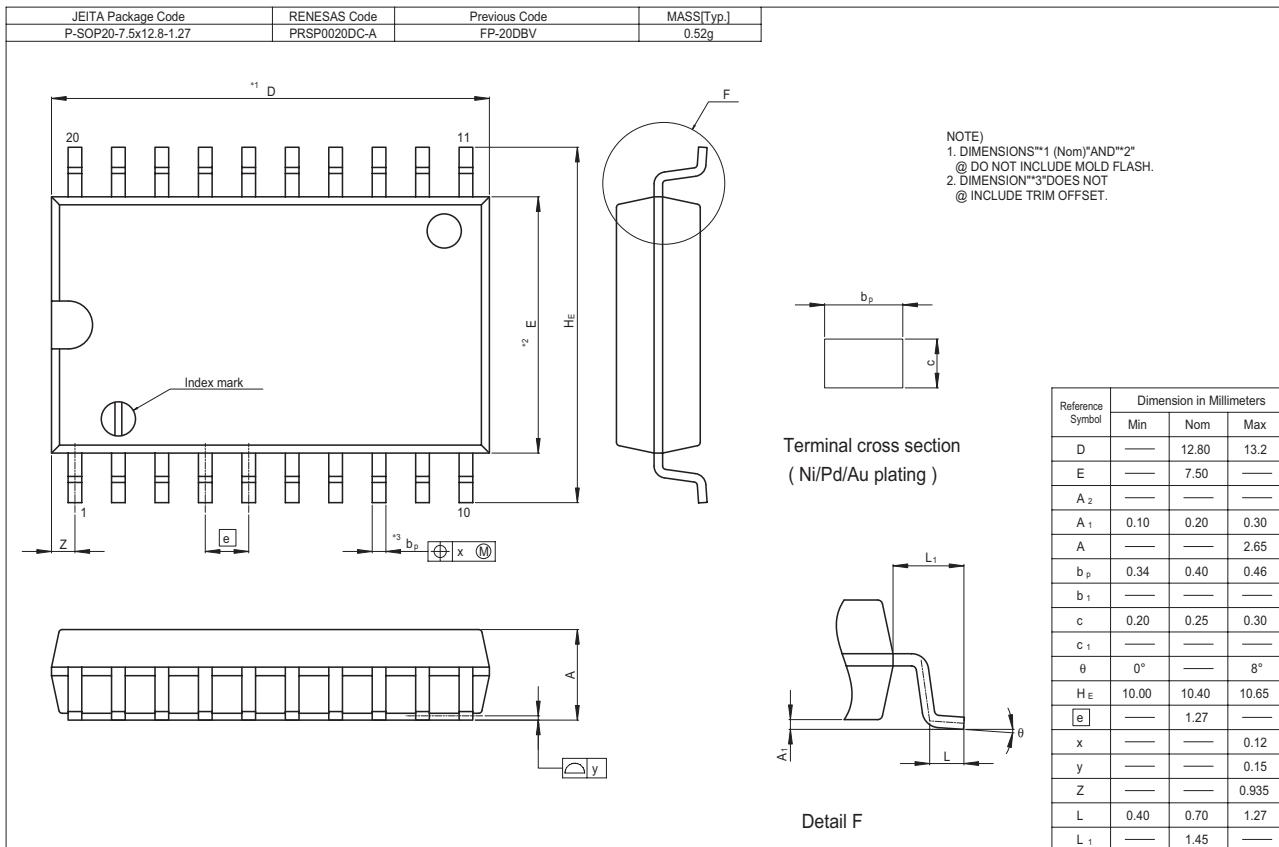
## Waveforms 2



Note: Input pulse:  $t_{TLH} \leq 15$  ns,  $t_{THL} \leq 6$  ns, PRR = 1 MHz.

## Package Dimensions





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