Application Notes

Intelligent Alphanumeric Displays

Interface Specifications

Specifications for AND Intelligent Alphanumeric displays are given in this section. The LCD controller used is the HD44780 or equivalent.

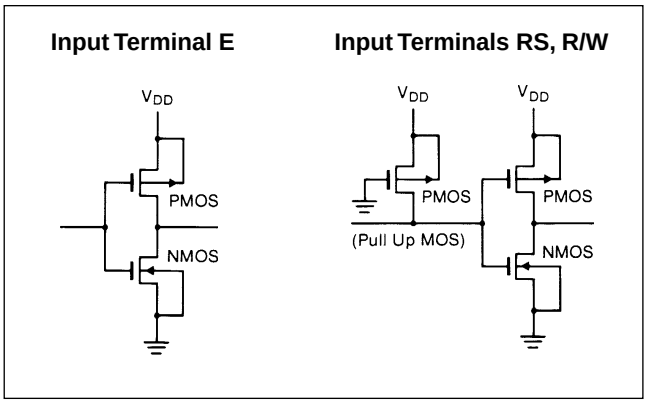
- AND671GST/GST-LED 16 characters x 1 line
- AND471GST/GST-LED 16 characters x 2 lines
- AND481GST/GST-LED 16 characters x 2 lines
- AND491GST/GST-LED 16 characters x 2 lines
- AND501GST/GST-LED 20 characters x 2 lines
- AND731GST/GST-LED 16 characters x 4 lines
- AND771GST/GST-LED 24 characters x 2 lines
- AND721GST/GST-LED 20 characters x 4 lines
- AND591GST/GST-LED 40 characters x 2 lines
- AND791GST/GST-LED 40 characters x 4 lines

Connector Pin Assignments (except for AND791GST)

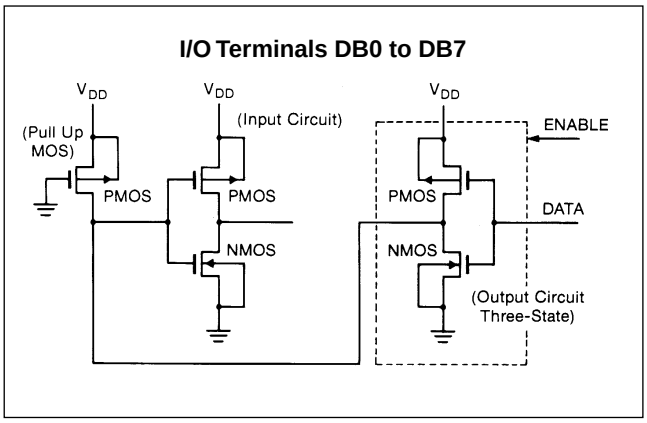
Pin No.	Signal	Function
1	GND	Ground
2	V_{DD}	+5 Power Supply
3	V_O	LCD Drive Voltage
4	RS	"H" Data Input "L" Command Input
5	R/$\overline{W}$	Read/Write
6	E	Enable
7	DBO	Data Bus DB0-DB7 is for 8 bit operation
8	DB1	
9	DB2	
10	DB3	
11	DB4	
12	DB5	
13	DB6	
14	DB7	
15*	LED	LED Anode (For LED option)
16*	LED	LED Cathode (For LED option)

* See specific mechanical drawing for details.

Terminal Characteristics



Terminal Characteristics



When input is at the intermediate level with CMOS, excessive current flows through the input circuit to the power supply. To avoid this, input level must be fixed at high or low.

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Character Position and Character Address

For each device, the relationship between character position and character address is straightforward. A hexadecimal code for each character position in each device is given in the following charts. Character positions are numbered from left to right beginning in the top left corner as you view the device from the front.

AND671

Character Position	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16
DD RAM (Hex) Add.	00	01	02	03	04	05	06	07	40	41	42	43	44	45	46	47

AND491, 481, 471

Character Position	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16
DD RAM (Hex) Add.	00	01	02	03	04	05	06	07	08	09	0A	0B	0C	0D	0E	0F

Character Position	17	18	19	20	21	22	23	24	25	26	27	28	29	30	31	32
DD RAM (Hex) Add.	40	41	42	43	44	45	46	47	48	49	4A	4B	4C	4D	4E	4F

AND501

Character Position	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19	20
DD RAM (Hex) Add.	00	01	02	03	04	05	06	07	08	09	0A	0B	0C	0D	0E	0F	10	11	12	13
Character Position	21	22	23	24	25	26	27	28	29	30	31	32	33	34	35	36	37	38	39	40
DD RAM (Hex) Add.	40	41	42	43	44	45	46	47	48	49	4A	4B	4C	4D	4E	4F	50	51	52	53

AND731

Character Position	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16
DD RAM (Hex) Add.	00	01	02	03	04	05	06	07	08	09	0A	0B	0C	0D	0E	0F
Character Position	17	18	19	20	21	22	23	24	25	26	27	28	29	30	31	32
DD RAM (Hex) Add.	40	41	42	43	44	45	46	47	48	49	4A	4B	4C	4D	4E	4F

Character Position	33	34	35	36	37	38	39	40	41	42	43	44	45	46	47	48
DD RAM (Hex) Add.	10	11	12	13	14	15	16	17	18	19	1A	1B	1C	1D	1E	1F
Character Position	49	50	51	52	53	54	55	56	57	58	59	60	61	62	63	64
DD RAM (Hex) Add.	50	51	52	53	54	55	56	57	58	59	5A	5B	5C	5D	5E	5F

AND771

Character Position	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19	20	21	22	23	24
DD RAM (Hex) Add.	00	01	02	03	04	05	06	07	08	09	0A	0B	0C	0D	0E	0F	10	11	12	13	14	15	16	17
Character Position	25	26	27	28	29	30	31	32	33	34	35	36	37	38	39	40	41	42	43	44	45	46	47	48
DD RAM (Hex) Add.	40	41	42	43	44	45	46	47	48	49	4A	4B	4C	4D	4E	4F	50	51	52	53	54	55	56	57

AND591

Character Position	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19	20	21	22	23	24	25	26	27	28	29	30	31	32	33	34	35	36	37	38	39	40
DD RAM (Hex) Add.	00	01	02	03	04	05	06	07	08	09	0A	0B	0C	0D	0E	0E	10	11	12	13	14	15	16	17	18	19	1A	1B	1C	1D	1E	1F	20	21	22	23	24	25	26	27
Character Position	41	42	43	44	45	46	47	48	49	50	51	52	53	54	55	56	57	58	59	60	61	62	63	64	65	66	67	68	69	70	71	72	73	74	75	76	77	78	79	80
DD RAM (Hex) Add.	40	41	42	43	44	45	46	47	48	49	4A	4B	4C	4D	4E	4F	50	51	52	53	54	55	56	57	58	59	5A	5B	5C	5D	5E	5F	60	61	62	63	64	65	66	67

AND721

Character Position	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19	20
DD RAM (Hex) Add.	00	01	02	03	04	05	06	07	08	09	0A	0B	0C	0D	0E	0F	10	11	12	13
Character Position	21	22	23	24	25	26	27	28	29	30	31	32	33	34	35	36	37	38	39	40
DD RAM (Hex) Add.	40	41	42	43	44	45	46	47	48	49	4A	4B	4C	4D	4E	4F	50	51	52	53
Character Position	41	42	43	44	45	46	47	48	49	50	51	52	53	54	55	56	57	58	59	60
DD RAM (Hex) Add.	14	15	16	17	18	19	1A	1B	1C	1D	1E	1F	20	21	22	23	24	25	26	27
Character Position	61	62	63	64	65	66	67	68	69	70	71	72	73	74	75	76	77	78	79	80
DD RAM (Hex) Add.	54	55	56	57	58	59	5A	5B	5C	5D	5E	5F	60	6	62	63	64	65	66	67

AND791

Character Position	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19	20	21	22	23	24	25	26	27	28	29	30	31	32	33	34	35	36	37	38	39	40
DD RAM (Hex) Add.	00	01	02	03	04	05	06	07	08	09	0A	0B	0C	0D	0E	0E	10	11	12	13	14	15	16	17	18	19	1A	1B	1C	1D	1E	1F	20	21	22	23	24	25	26	27
Character Position	41	42	43	44	45	46	47	48	49	50	51	52	53	54	55	56	57	58	59	60	61	62	63	64	65	66	67	68	69	70	71	72	73	74	75	76	77	78	79	80
DD RAM (Hex) Add.	40	41	42	43	44	45	46	47	48	49	4A	4B	4C	4D	4E	4F	50	51	52	53	54	55	56	57	58	59	5A	5B	5C	5D	5E	5F	60	61	62	63	64	65	66	67
Character Position	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19	20	21	22	23	24	25	26	27	28	29	30	31	32	33	34	35	36	37	38	39	40
DD RAM (Hex) Add.	00	01	02	03	04	05	06	07	08	09	0A	0B	0C	0D	0E	0E	10	11	12	13	14	15	16	17	18	19	1A	1B	1C	1D	1E	1F	20	21	22	23	24	25	26	27
Character Position	41	42	43	44	45	46	47	48	49	50	51	52	53	54	55	56	57	58	59	60	61	62	63	64	65	66	67	68	69	70	71	72	73	74	75	76	77	78	79	80
DD RAM (Hex) Add.	40	41	42	43	44	45	46	47	48	49	4A	4B	4C	4D	4E	4F	50	51	52	53	54	55	56	57	58	59	5A	5B	5C	5D	5E	5F	60	61	62	63	64	65	66	67

Note: Address locations for Lines 1 & 2 are controlled by E1, and lines 3 & 4 are controlled by E2.

Timing

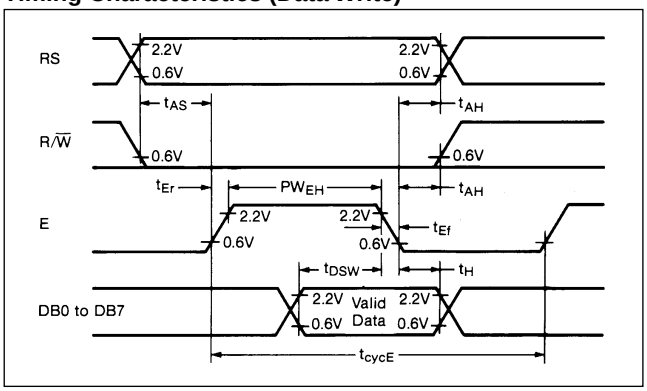
Timing Characteristics (TA = 25°C) Data Write

Item	Symbol	Value		Unit
		Min.	Max	
Enable Cycle Time	t_{CYCE}	1000	-	
Enable Pulse Width	PW_{EH}	450		
Enable Rise/Fall Time	t_{Er}, t_{Ef}		25	
Set Up Time	t_{AS}	140		ns
Address Hold Time	t_{AH}	10		
Data Set Up Time	t_{DSW}	195		
Data Hold Time	t_H	10		

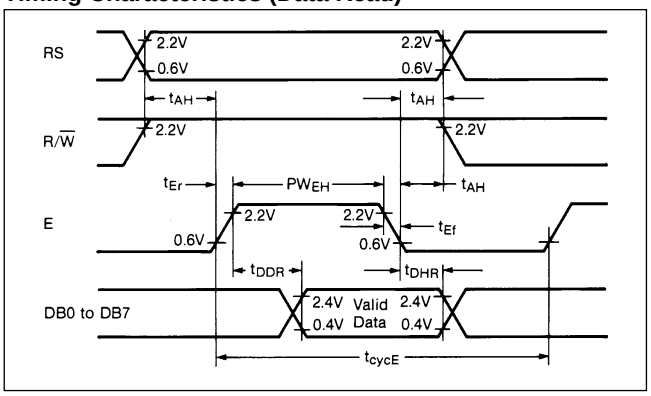
Data Read

Item	Symbol	Value		Unit
		Min.	Max.	
Enable Cycle Time	t_{CYCE}	1000		ns
Enable Pulse Width	PW_{EH}	450		
Enable Rise/Fall Time	t_{Er}, t_{Ef}		25	
Set Up Time	t_{AS}	140		
Address Hold Time	t_{AH}	10		
Data Delay Time	t_{DDR}		320	
Data Hold Time	t_{DHR}	20		

Timing Characteristics (Data Write)



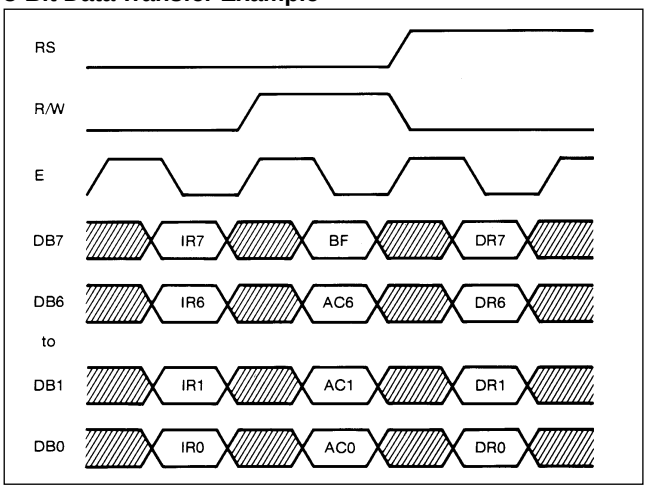
Timing Characteristics (Data Read)



Data Transfer Example

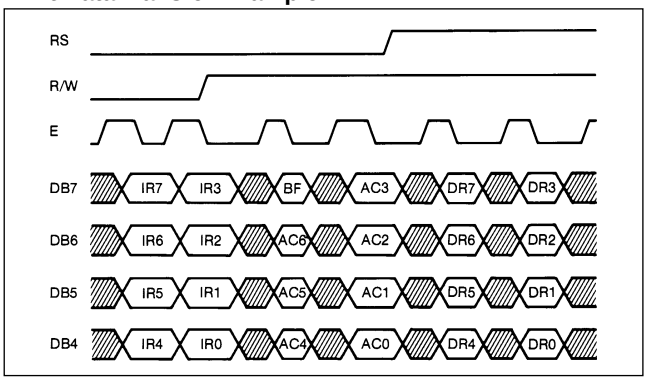
Data can be sent in the either two cycles of 4-bit data or one cycle of 8-bit data, a scheme that suits 4-bit or 8-bit CPUs. Data that is 8-bits long is transferred using 8 data lines of DB0 to DB7.

8-Bit Data Transfer Example



Data that is 4 bits long is transferred by using only 4 lines of DB7 to DB4—DB3 to DB0 are not used. Data transfer between the module and a 4-bit CPU is completed when the high order 4 bits are transferred first, followed by the low order 4 bits.

4-Bit Data Transfer Example



Command List

Command	Command Code										Description	Execution Time (Max.)[1]	Execution Time (Max.)[2]
	RS	R/W	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0			
Clear display[3]	0	0	0	0	0	0	0	0	0	1	Clear display and return cursor to home position (Address 0).	1.64ms	4.9ms
Return Home	0	0	0	0	0	0	0	0	1	X	Return cursor to home position (Address 0). Also return display being shifted to original position. DD RAM contents remain the same.	1.64ms	4.8ms
Entry Mode Set	0	0	0	0	0	0	0	1	I/$\overline{D}$	S	Set cursor move direction and specify whether to shift display. These operations are performed during data write.	40µs	120µs
Display ON/$\overline{OFF}$ Control	0	0	0	0	0	0	1	D	C	B	Set ON/$\overline{OFF}$ of entire display (D), dresser ON/$\overline{OFF}$ (C), and blinking of cursor position B	40µs	120µs
Cursor and Display Shift[4]	0	0	0	0	0	1	S/C	R/L	X	X	Move cursor and shift display without changing DD RAM contents.	40µs	120µs
Function Set	0	0	0	0	1	DL	N	F	X	X	Set interface data length (DL) number of display lines (L) and character font (F).	40µs	120µs
Set RAM Address	0	0	0	1	ACG						Set CG RAM address, CG RAM data is sent and received after this setting.	40µs	120µs
Set DD RAM Address	0	0	1	ADD							Set DD RAM address. DD RAM data is sent and received after this setting.	40µs	120µs
Read Busy Flag & Address	0	1	BF	AC							Read Busy flag (BF) indicating internal operation is being performed and reads address counter contents.	40µs	120µs
Write Data to CG or DD RAM	1	0	Write Data								Write Data from DD RAM or CG RAM.	40µs	120µs
Read Data to CG or DD RAM	1	1	Read Data								Read Data from DD RAM or CG RAM.	40µs	120µs
	I/$\overline{D}$ = 1 : Increment I/D = 0 Decrement S = 1 : Accompanies display shift S/C = 1 : Display shift S/C = 0 Cursor move R/L = 1 : Shift to the right R/L = 0 : Shift to the left DL = 1 : 8 bits DL = 0: 4 bits N =1 : 2 lines N = 0: 1 line F = 1 : 5 x 10 dots F = 0: 5 x 7 dots BF = 1 : Internally operating BF = 0 : Can accept instruction										DD RAM : Display Data RAM CG RAM : Character Gen RAM ACG : CG RAM Address ADD : DD RAM Address corresponds to Cursor Address AC : Address Counter used for DD and CG RAM Address.		

X = Don't Care

Notes:

1. Applies to AND491, AND481, AND491, and AND501.
2. Applies to AND591, AND731, AND721, AND771.
3. The repeat time interval of command Clear Display must be 13ms minimum (5 x 7 dot font) and 18ms minimum (5 x 10 dot font).
4. Commands “Cursor and Display Shift “are invalid for the AND671.

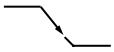
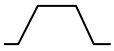
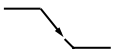
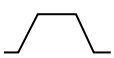
Function of Registers

The following paragraphs describe the function of the registers.

Instruction Register and Data Register
The built-in controller has two 8-bit registers, an Instruction Register (IR) and a Data Register (DR). The IR stores commands such as display clear and cursor shift, or address information of display data RAM (DD RAM), and character generator RAM (CG RAM). The IR can be written to by a CPU, but a CPU cannot read this register.

The DR temporarily stores data to be written into the DD RAM or the CG RAM. Data written into the DR is automatically sent to the DD RAM or the CG RAM as an internal operation. The DR is also used for data storage when reading data from the DD RAM or the CG RAM. When address information is written into the IR, data is transferred to the DR from the DD RAM or the CG RAM as an internal operation. Then, the CPU reads the DR and data transfer is completed. After the CPU reads the DR, data of the DD RAM or the CG RAM at the next address is sent to DR for the next reading. Register Selector (RS) signals select these two registers.

Register Selection

RS	R/W	Operation	Enable (E)
0	0	Write commands to IR.	
0	1	Read of a Busy Flag (DB7) and Address Counter (DBO to DB6)	
1	0	DR Write as internal operations (DR → DD or CG RAM)	
1	1	DR Read as internal operations (DD or CG RAM → DR)	

Busy Flag (BF)
When the Busy Flag is “1”, the LCD module is in the internal operation mode, and the next instruction is not accepted at this time. As shown in the “Command List” on page 5 of this section, the Busy Flag is shown in DB7 when RS = 0 and R/W = 1. The next instruction must be written after checking that the Busy Flag is “0”.

Address Counter (AC)
The address counter (AC) assigns DD and CG RAM address. When an instruction for address setting is written in IR, the address information is sent from IR to AC.

Selection of either the DD or CG RAM is also determined by an instruction. After writing into (or reading from) DD or CG RAM display data, AC is automatically incremented by 1 (or decremented by 1). Data in address counters (AC) are in DB6 to DBO when RS = 0 and R/W = 1, as shown in the table entitled “Command List” on page 5 of this section.

Display Data RAM (DD RAM)
The display data RAM (DD RAM) stores display data represented in 8-bit character codes. The relationship between the DD RAM address and display position on the LCD Display is described by a series of tables under the paragraph “Character Position and Character Address” on page 3 of this section.

Commands

The command code is the signal through which the LCD module is accessed through the CPU. The LCD module begins operation upon receipt of the code input. Because the internal processing operation of the LCD module is started with a timing that does not affect the LCD display, the busy status continues longer than the CPU cycle time.

Under the busy status (when the busy flag is set to “1”), the LCD module does not execute any commands other than the busy flag read. Accordingly, the CPU has to verify that the busy flag is set to “0” prior to the input of the command code.

Clear Display

	RS	R/W	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
Code	0	0	0	0	0	0	0	0	0	1

Write space code “20” (hexadecimal) into all the DD RAM addresses. The cursor returns to address “0” (DD RAM Address = “00H”) and the display, if it has been shifted, returns to the original position. In other words, the display disappears and the cursor goes to the left edge of the first line.

Return Home

	RS	R/W	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
Code	0	0	0	0	0	0	0	0	1	X

Return the cursor to character position 1 (DD RAM Address = “00H”) and returns the display to the original position if it has been shifted (S in the instruction register is 1). The DD RAM contents remain unchanged.

X = Don’t care

Entry Mode Set

	RS	R/W	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
Code	0	0	0	0	0	0	0	1	I/D	S

I/D: Increment (I/D = 1) or decrement (I/D = 0) the DD RAM address by one upon writing a character code into the DD RAM or reading a character code from the DD RAM. The cursor moves to the right when I/D = 1, and to the left when I/D = 0.

S: When writing to the DD RAM, shift the entire display to the right (when I/D = 0, S = 1) or to the left (when ID = 1, S = 1). Therefore, the cursor looks as if it stood still and only the display moves. Display is not shifted when reading from the DD RAM. Display is not shifted when S = 0.

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Display ON/OFF Control

	RS	R/W	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
Code	0	0	0	0	0	0	1	D	C	B

D: Display is turned ON when D = 1 and OFF when D = 0. When display is turned off due to D = 0, the display data remains in the DD RAM and they can be displayed immediately by setting D = 1.

C: The cursor is displayed when C = 1 and not displayed when C = 0. Even if the cursor disappears, the function of I/D does not change during "display data write." The cursor is displayed at the 8th line when the 5 x 7 dots character font is selected.

B: The character at the cursor position blinks when B = 1. The blink is done by switching between all black dots and display characters at 0.4 second interval. The cursor and the blink can be set concurrently.

Cursor or Display Shift

	RS	R/W	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
Code	0	0	0	0	0	1	S/C	R/L	X	X

Shift the cursor position or display position to the right or the left without writing or reading the display data. This function can be used for correction or search of display.

S/C	R/L	Function
0	0	Shift the cursor position to the left. (AC is decremented by one.)
0	1	Shift the cursor position to the right. (AC is incremented by one.)
1	0	Shift the entire display to the left. The cursor follows the display shift.
1	1	Shift the entire display to the right. The Cursor follows the display shift.

Function Set

	RS	R/W	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
Code	0	0	0	0	1	DL	N	F	X	X

DL: Sets the interface data length. Data is sent or received in 8-bit length (DB7 to DB0) when DL = 1 and 4-bit length (DB7 to DB4) when DL = 0. When 4-bit length is selected, data must be sent or received in two cycles.

N: Set number of display lines.

F: Set character font. The 5 x 7 dots character font is selected when F = 0. While 5 x 10 dots character font is selected when F = 1 and N = 0.

Module Type Number

N	F	No. of Display Lines	Character Font	Duty Ratio	AND Model No.
1	0	2	5 x 7 Dots	1/16	AND471, AND481, AND491, AND501, AND591, AND671, AND771
1	0	4	5 x 7 Dots	1/16	AND721, AND731, AND791

Set CG RAM Address

	RS	R/W	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
Code	0	0	0	1	A	A	A	A	A	A

Set the CG RAM address to a binary number of AAAAAA in the address counter. After execution of this instruction, all the data from MPU is written into the CG RAM and all the data is read from CG RAM.

Set DD RAM Address

	RS	R/W	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
Code	0	0	1	An	A	A	A	A	A	A

Set the DD RAM address to a binary number of AnAAAAAA in the address counter (An = 0 for the first line, An = 1 for the second line). After execution of this instruction, all the data from MPU is written into the DD RAM and all the data is read from DD RAM.

Read Busy Flag and Address

	RS	R/W	DB7	DB6	DB5	DB4	DB3	DB2	091	DB0
Code	0	1	BF	A	A	A	A	A	A	A

Read Busy Flag (BF) and the value of the address counter (AAAAAAA). The condition BF = 1 indicates that an internal operation is going on and the next command is not accepted until BF becomes "0." You must check the BF status before the next write operation. The address counter generates the CG or DD RAM address.

Write Data to CG RAM or DD RAM

	RS	R/W	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
Code	1	D	D	D	D	D	D	D	D	D

Write binary 8-bit data DDDDDDDD to the CG RAM or the DD RAM. Whether the CG RAM or the DD RAM is to be written is determined by the previous designation (CG RAM address setting or DD RAM address setting). After writing, the address is automatically incremented or decremented by one according to entry mode. Display shift also follows the entry mode.

Read Data from CG RAM or DD RAM

	RS	R/W	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
Code	1	1	D	D	D	D	D	D	D	D

Read binary 8-bit data DDDDDDDD from the CG RAM or the DD RAM. Whether the CG RAM or the DD RAM is to be read is determined by the previous designation. Prior to inputting this read command, either the CG RAM address set command or the DD RAM address set command must be executed. If it is not done, the first data read is invalid, and the second data read of the next address can be read normally. After reading, the address is automatically incremented or decremented by one according to the entry mode. However, display shift is not performed regardless of entry mode.

Character Patterns and Character Codes

The relationship between character patterns and character codes is explained in the following paragraphs.

Character Generator ROM (CG ROM)

The character generator ROM generates 5 x 7 dot (160 kinds) character patterns or 5 x 10 dot (32 kinds) character patterns from an 8-bit DD RAM character code signal.

When the 8-bit character code of the CG ROM is written into the DD RAM, the character pattern of the CG ROM corresponding to the code is displayed on the LCD display position corresponding to the DD RAM address. The table entitled “Character Pattern and Character Code” on page 9 of this section shows the relation between character patterns and character codes.

Note: AND671, AND471, AND481, AND491, AND501, AND591, AND771, AND731, AND721 and AND791 can only use 5 x 7 dot character patterns.

Character Generator RAM (CG RAM)

The character generator RAM is used for original character patterns other than for the CG ROM. The CG RAM has the capacity (64 bytes = 512 bits) to write 8 types of character patterns with 5x7 font, and 4 types with S x 10 font. When displaying character patterns stored in the CG RAM, write 8-bit character codes (00 to 07 or 02 to OF; hex.) on the left side as shown in the table entitled “Character Pattern and Character Code” on page 9 of this section.

The table entitled “5 x 7 Dots Character Pattern” on page 8 of this section shows the relation between CG RAM addresses and data and display patterns for 5 x 7 dots.

Address, Character Code, and Character Pattern

The following tables list the relationships between CG RAM address, character code (DD RAM), and character pattern (CG RAM) for two character patterns.

5 x 7 Dots Character Pattern

Character Code (DD RAM Data)	CG RAM Address	Character Pattern (CG RAM Data)
7 6 5 4 3 2 1 0	5 4 3 2 1 0	7 6 5 4 3 2 1 0
0 0 0 0 X 0 0 0	0 0 0	X X X 0 0 0 0 0
	0 0 1	X X X 0 0 0 0 0
	0 1 0	X X X 0 1 0 0 1
	0 0 0 0 1 1	X X X 1 0 1 0 1
	1 0 0	X X X 1 0 0 1 0
	1 0 1	X X X 1 0 0 1 0
	1 1 0	X X X 0 1 1 0 1
	1 1 1	X X X 0 0 0 0 0
0 0 0 0 X 0 0 1	0 0 0	X X X 0 0 0 0 0
	0 0 1	X X X 0 0 0 0 0
	0 1 0	X X X 0 1 1 1 0
	0 0 1 0 1 1	X X X 1 0 0 0 1
	1 0 0	X X X 1 0 0 0 1
	1 0 1	X X X 0 1 0 1 0
	1 1 0	X X X 1 1 0 1 1
	1 1 1	X X X 0 0 0 0 0

X = Don't care

Notes:

1. Character code bits 0 to 2 correspond to CG RAM address bits 3 to 5 (3 bits: 8 types).
2. CG RAM address bits 0 to 2 designate character pattern line position. The 8th line is the cursor position and the display is presented in logical OR with cursor.
3. Character pattern row positions correspond to CG RAM data bits 0 to 4, as shown in the figure (bit 4 is at the left end). Since the CG RAM data bits 5 to 7 are not used for the display, they can be used as general data RAM.
4. As shown in the above table CG RAM character patterns are selected when character code bits 4 to 7 are all “0.” However, since character code bit 3 is the “Don't care” bit, the “α” display in the character pattern, for example, is selected by character code “00” or “08”.
5. A “1” for CG RAM data corresponds to selection for display and a “0” for non-selection.

Character Pattern and Character Code

Upper 4 bit / Lower 4 bit	0000	0010	0011	0100	0101	0110	0111	1010	1011	1100	1101	1110	1111
XXXX0000	CG RAM (1)												
XXXX0001	(2)												
XXXX0010	(3)												
XXXX0011	(4)												
XXXX0100	(5)												
XXXX0101	(6)												
XXXX0110	(7)												
XXXX0111	(8)												
XXXX1000	(1)												
XXXX1001	(2)												
XXXX1010	(3)												
XXXX1011	(4)												
XXXX1100	(5)												
XXXX1101	(6)												
XXXX1110	(7)												
XXXX1111	(8)												

Initialization (Reset)

The following paragraphs describe initialization stepts.

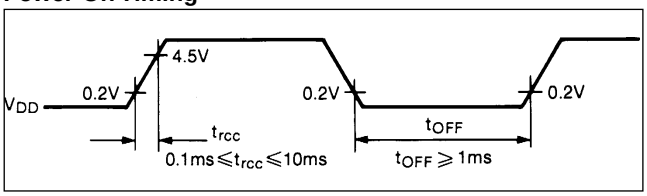
Automatic Initialization

The LCD module is automatically initialized when power is turned on (using internal reset circuit). The following commands are executed during initialization. The busy flag is kept in the busy state (BF does not equal 1) until initialization ends. The busy state is kept about 10ms after V_{DD} level reaches 4.5V.

1. Clear display
2. Function set:
   Data length of interface with MPU: 8-bit (DL-1)
   LCD: 1-line display (N = 0)
   Character font: 5 x 7 dots (F = 0)
3. Display ON/OFF control:
   Display: Display OFF (0 = 0)
   Cursor: Cursor OFF (C = 0)
   Blink: Blink OFF (B = 0)
4. Entry mode set:
   Address counter: Increment + 1 (I/D = 1)
   Display shift: No shift (S = 0)
5. DD RAM is selected:
   The function set command in automatic initialization does not always meet the configuration of each module, in this case your program must reset the "Function Set" command. (Refer to "Function Set" on page 7 of this section.)

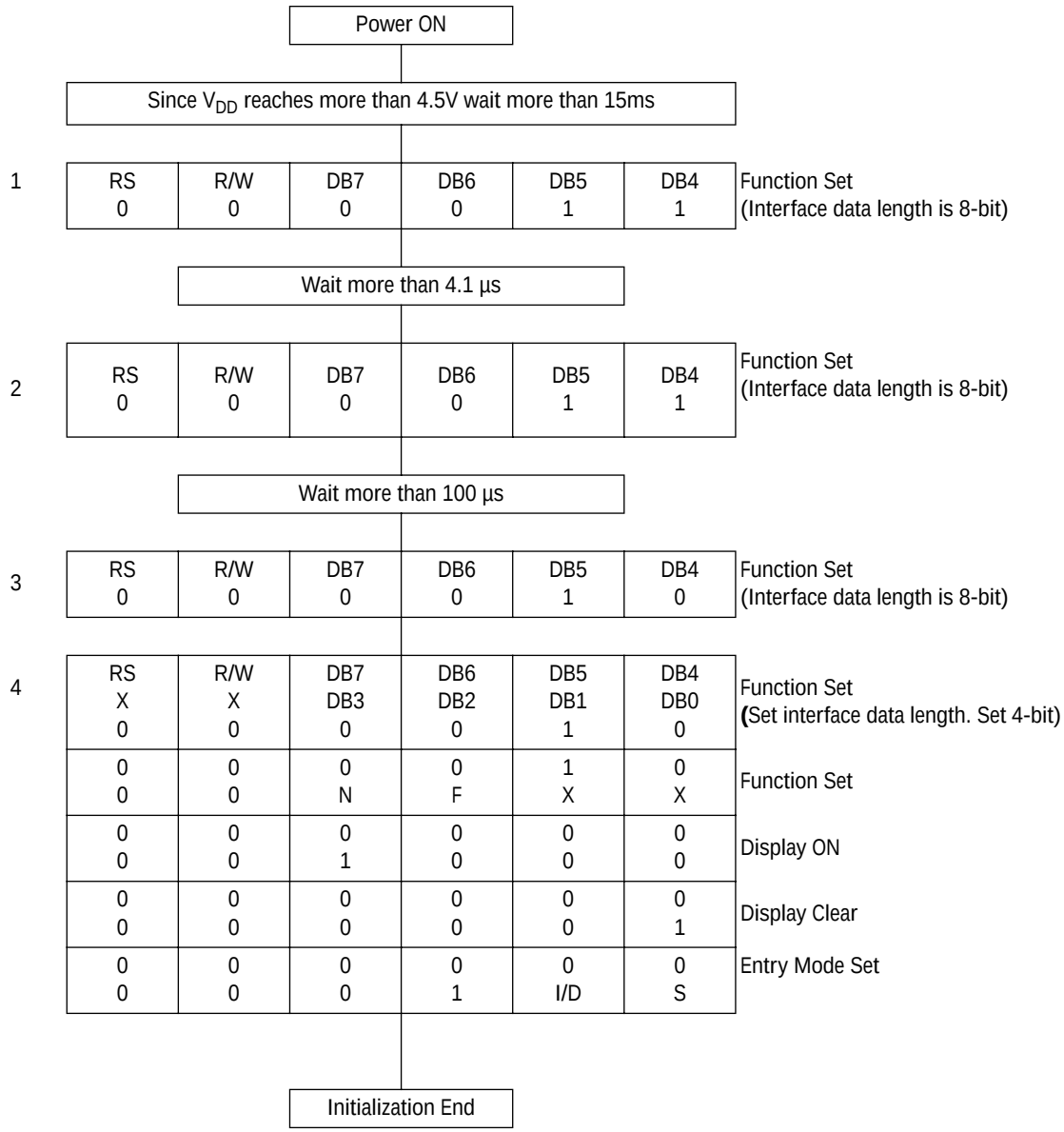
Note: Power-on timing is necessary to perform automatic initialization. When the above power supply condition is not satisfied, the internal reset circuit will not operate normally. In this case, perform the initialization by sending commands from the CPU after turning power to ON.

Power-On Timing



Manual Initialization Procedure

The following diagram applies when the interface data length is 4-bits.



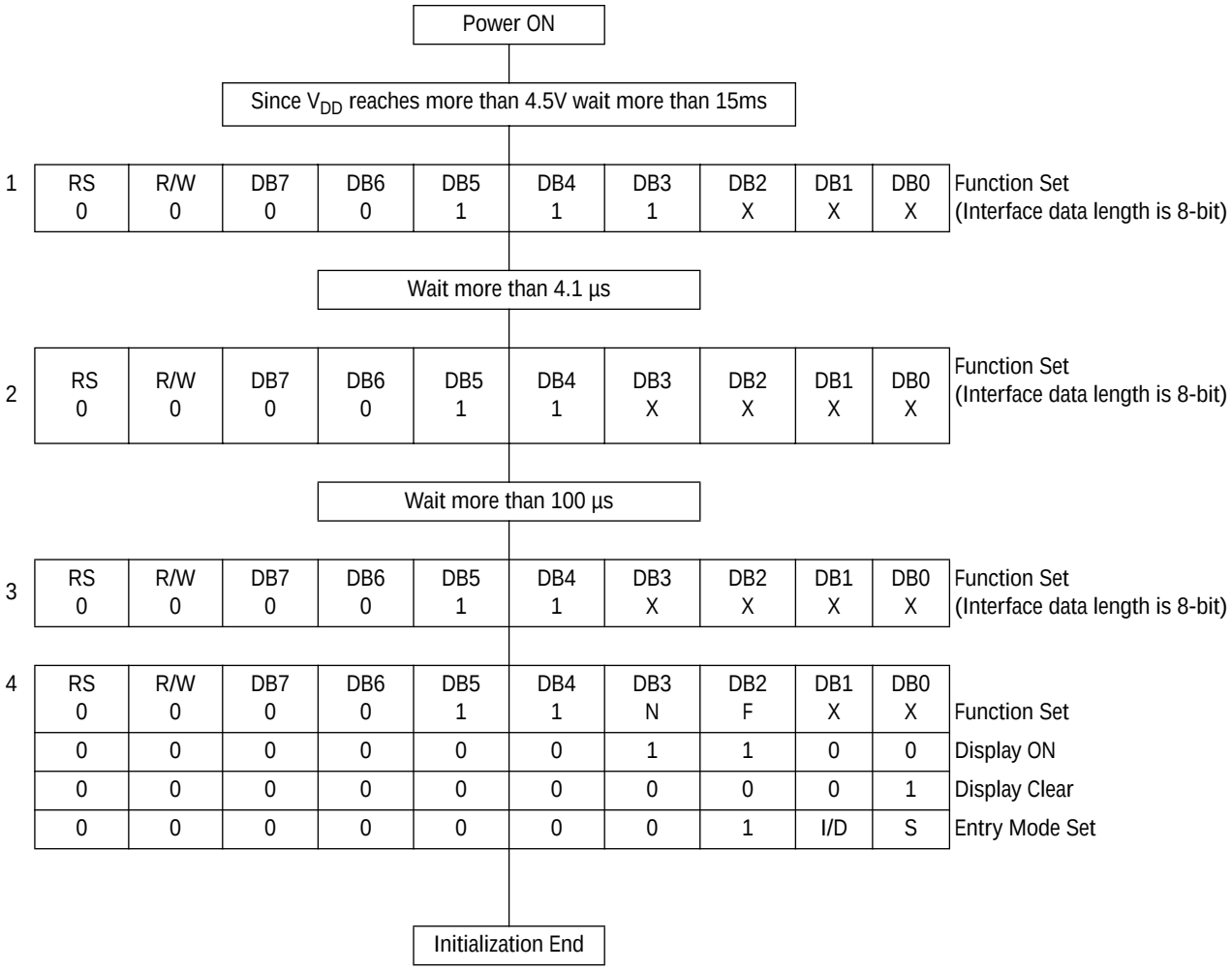
X = Don't care

Notes:

1. Before initialize step 1, 2, and 3, cannot check busy flag.
2. After initialize step 4, cannot change function set mode, number of display lines and character font.

Manual Initialization Procedure (Continued)

The following diagram applies when the interface data length is 8-bit.



X = Don't care

Notes:

(1) Before initialize step 1, 2 and 3, cannot check busy flag.

(2) After initialize step 4, cannot change function set, number of display lines and character font.

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Example of Operation (AND501)

4-Bit Operation

Command										Display	Operation
Power Supply ON (Internal Reset Circuit)											Initialized. No display appears.
Initialization											Initialized. No display appears.
Display ON/OFF Control											Turn on display and cursor. All display is in space mode because of initialization.
RS	R/W	DB7	DB6	DB5	DB4						
0 0	0 0	0 0	0 1	0 1	0 0						
Set DD RAM Address											Set RAM address so that the cursor is positioned at the head of first line.
0 0	0 0	1 0	0 0	0 0	0 0					__	
Write Data to CG/DD RAM										A__	Write “A”. The DD RAM was selected by the initialization performed when power was turned on. The cursor increments by one and shifts to the right.
1 1	0 0	0 0	1 0	0 0	0 1						

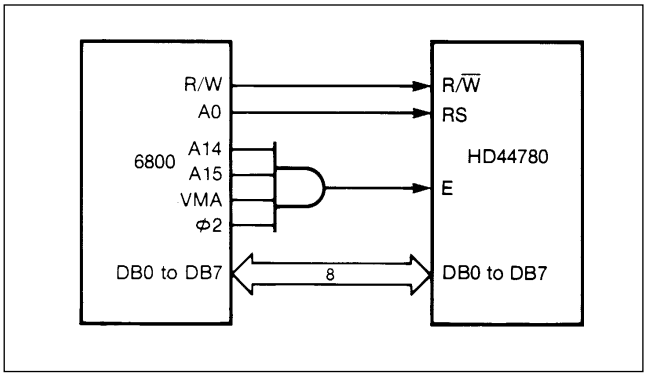
8-Bit Operation

Command										Display	Operation
Power Supply ON (Internal Reset Circuit)											Initialized. No display appears.
Initialization											Initialized. No display appears.
Display ON/OFF Control											Turn on display and cursor. All display is in space mode because of initialization.
RS	R/W	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0		
0	0	0	0	0	0	1	1	1	0		
Set DD RAM Address											Set RAM address so that the cursor is positioned at the head of first line.
0	0	1	0	0	0	0	0	0	0	__	
Write Data to CG/DD RAM										A__	Write “A”. The DD RAM was selected by the initialization performed when power was turned on. The cursor increments by one and shifts to the right.
1	0	0	1	0	0	0	0	0	1		
					|					Write “N”
					|					
Write Data to CG/DD RAM										AND__	Write “D”
1	0	0	1	0	0	0	1	0	0		
Set DD RAM Address										AND	Set RAM address so cursor is positioned at the head of second line.
0	0	1	1	0	0	0	0	0	0	__	
Write Data to CG/DD RAM										AND	Write “A”
1	0	0	1	0	0	0	0	0	1	A__	
					|					Write
					|					AND 501 20 x
Write Data to CG/DD RAM										AND	Write “2”
1	0	0	0	1	1	0	0	1	0	AND501 20 x 2	
Entry Mode Set										AND	Set mode for display shift at the time of write.
0	0	0	0	0	0	0	1	1	1	AND501 20 x 2	
					|					Written data moves to the right, cursor on position 2_
					|					
Return Home										AND501 20x2	Return both the display and cursor to the original position.
0	0	0	0	0	0	0	0	1	X		

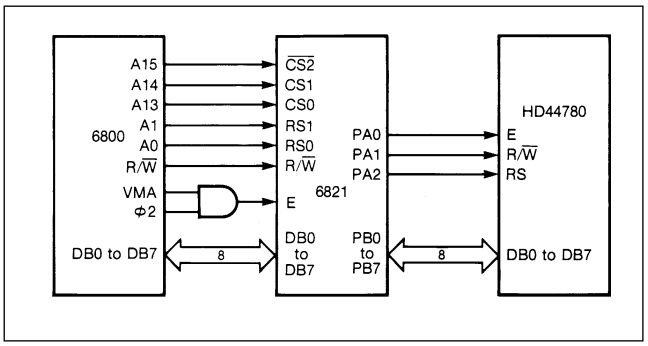
X = Don't care

HD44780 Electrical Interfaces

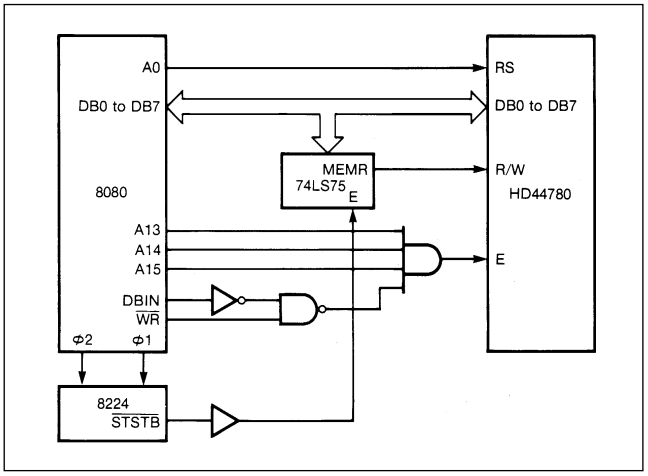
6800



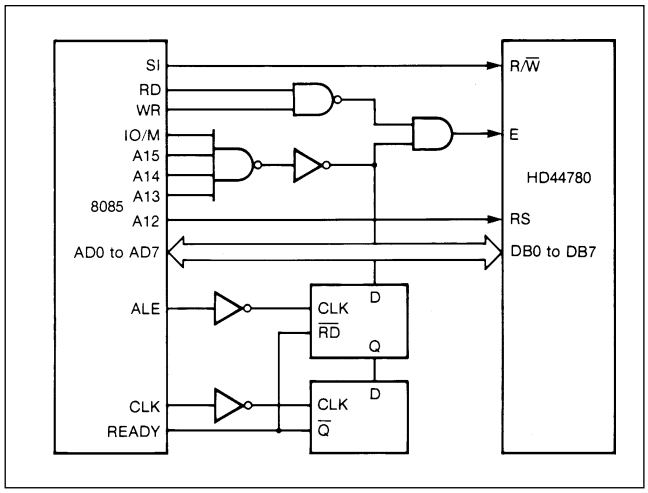
688 with 6821 PIA



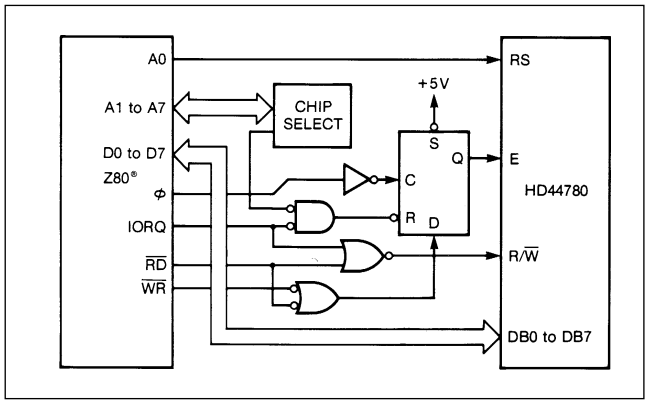
8080



8085



Z80



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DMM Connected to an 8085A Based System