

## Equações lógicas para a unidade de controle

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$$\begin{aligned} \text{RegDst0} &= \text{state7} = S0.S1.S2.\overline{S3}.\overline{S4} \\ \text{RegDst1} &= \text{state11} + \text{state17} = S0.S1.\overline{S2}.S3.\overline{S4} + S0.\overline{S1}.\overline{S2}.\overline{S3}.S4 \\ \text{RegWrite} &= \text{state4} + \text{state7} + \text{state11} + \text{state13} + \text{state16} + \text{state17} = \overline{S0}.\overline{S1}.S2.\overline{S3}.\overline{S4} + \\ &S0.S1.S2.\overline{S3}.\overline{S4} + S0.S1.S2.S3.\overline{S4} + S0.\overline{S1}.S2.S3.\overline{S4} + S0.\overline{S1}.\overline{S2}.\overline{S3}.S4 + S0.S1.\overline{S2}.\overline{S3}.S4 \\ \text{ALUSrcA} &= \text{state2} + \text{state6} + \text{state8} + \text{state12} + \text{state14} + \text{state15} = \overline{S0}.S1.\overline{S2}.\overline{S3}.\overline{S4} + \\ &\overline{S0}.S1.S2.\overline{S3}.\overline{S4} + \overline{S0}.\overline{S1}.S2.S3.\overline{S4} + S0.\overline{S1}.S2.S3.\overline{S4} + S0.S1.S2.S3.\overline{S4} + S0.S1.S2.S3.S4 \\ \text{ALUSrcB0} &= \text{state0} + \text{state1} = \overline{S0}.\overline{S1}.S2.\overline{S3}.S4 + S0.S1.\overline{S2}.\overline{S3}.S4 \\ \text{ALUSrcB1} &= \text{state1} + \text{state2} + \text{state12} + \text{state15} = S0.\overline{S1}.S2.\overline{S3}.\overline{S4} + \overline{S0}.S1.\overline{S2}.\overline{S3}.\overline{S4} + \\ &\overline{S0}.\overline{S1}.S2.S3.\overline{S4} + S0.S1.S2.S3.S4 \\ \text{ALUOp0} &= \text{state8} + \text{state14} = \overline{S0}.\overline{S1}.\overline{S2}.S3.\overline{S4} + \overline{S0}.S1.S2.S3.\overline{S4} \\ \text{ALUOp1} &= \text{state6} + \text{state15} = \overline{S0}.S1.S2.\overline{S3}.\overline{S4} + S0.S1.S2.S3.\overline{S4} \\ \text{PCSource0} &= \text{state8} + \text{state10} + \text{state11} + \text{state14} = \overline{S0}.\overline{S1}.S2.S3.\overline{S4} + \overline{S0}.S1.\overline{S2}.S3.\overline{S4} + \\ &S0.S1.\overline{S2}.S3.\overline{S4} + \overline{S0}.S1.S2.S3.S4 \\ \text{PCSource1} &= \text{state9} + \text{state10} + \text{state11} + \text{state17} = S0.\overline{S1}.\overline{S2}.S3.\overline{S4} + \overline{S0}.S1.\overline{S2}.S3.\overline{S4} + \\ &S0.S1.\overline{S2}.S3.\overline{S4} + S0.\overline{S1}.\overline{S2}.\overline{S3}.S4 \\ \text{PCWriteCond} &= \text{state8} + \text{state14} = \overline{S0}.\overline{S1}.\overline{S2}.S3.\overline{S4} + \overline{S0}.S1.S2.S3.\overline{S4} \\ \text{PCWrite} &= \text{state0} + \text{state9} + \text{state10} + \text{state11} + \text{state17} = \overline{S0}.\overline{S1}.\overline{S2}.\overline{S3}.\overline{S4} + \\ &S0.\overline{S1}.\overline{S2}.S3.\overline{S4} + \overline{S0}.S1.\overline{S2}.S3.\overline{S4} + S0.S1.\overline{S2}.S3.\overline{S4} + S0.\overline{S1}.\overline{S2}.\overline{S3}.S4 \\ \text{IorD} &= \text{state3} + \text{state5} = S0.S1.\overline{S2}.\overline{S3}.\overline{S4} + S0.\overline{S1}.S2.\overline{S3}.\overline{S4} \\ \text{MemRead} &= \text{state0} + \text{state3} + \overline{S0}.\overline{S1}.\overline{S2}.\overline{S3}.\overline{S4} + S0.S1.\overline{S2}.\overline{S3}.\overline{S4} \\ \text{MemWrite} &= \text{state5} = S0.\overline{S1}.S2.\overline{S3}.\overline{S4} \\ \text{BNE} &= \text{state14} = \overline{S0}.S1.S2.S3.\overline{S4} \\ \text{IRWrite} &= \text{state0} = \overline{S0}.\overline{S1}.\overline{S2}.\overline{S3}.\overline{S4} \\ \text{MemtoReg0} &= \text{state4} = \overline{S0}.\overline{S1}.S2.\overline{S3}.\overline{S4} \\ \text{MemtoReg1} &= \text{state11} + \text{state17} = S0.S1.\overline{S2}.S3.\overline{S4} + S0.\overline{S1}.\overline{S2}.\overline{S3}.S4 \end{aligned}$$

OPCodes:

- add = 000000 funct = 100000
- sub = 000000 funct = 100010
- slt = 000000 funct = 101010
- and = 000000 funct = 100100
- or = 000000 funct = 100101
- lw = 100011
- sw = 101011
- beq = 000100
- j = 000010
- jal = 000011
- jr = 010100
- jalr = 010101
- addi = 001000
- andi = 001100
- bne = 000101

NS0 =  $\overline{S0.S1.S2.S3.S4} + S0.\overline{S1.S2.S3.S4}.\overline{OP0.OP1.OP2.OP3.OP4.OP5}(\text{jump}) +$

...

NS1 =

NS2 =

NS3 =

NS4 =