Signal Integrity Analysis in Ansys Minerva using PyAEDT

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Ansys

Solution: pyAEDT

pyAEDT is intended to **consolidate** and **extend** all existing functionalities around AEDT-based scripting to allow **re-use of existing code**, **sharing of best-practice** and increase **collaboration:**

- Provides **connection** between development environments and Ansys Electronics Desktop
- Enables **access to CPython** functionality that is not natively available within Ansys Electronics Desktop
- **Simplified Syntax** and extended functionality

What is Siwave/AEDT?

What is SIwave?

- Hybrid Full Wave EM Field Solver
- Models Printed Circuit Boards and Packages
- Analyses Performed:
  - DC Analysis (with Thermal coupling)
  - Signal Integrity
  - Power Integrity

  Frequency and time domains
  - Electromagnetic Compatibility/Interference

What is AEDT?

The ANSYS Electronic Desktop is a graphical user interface (GUI) common to many electronic simulation tools.

Simulation Types Available within AEDT:

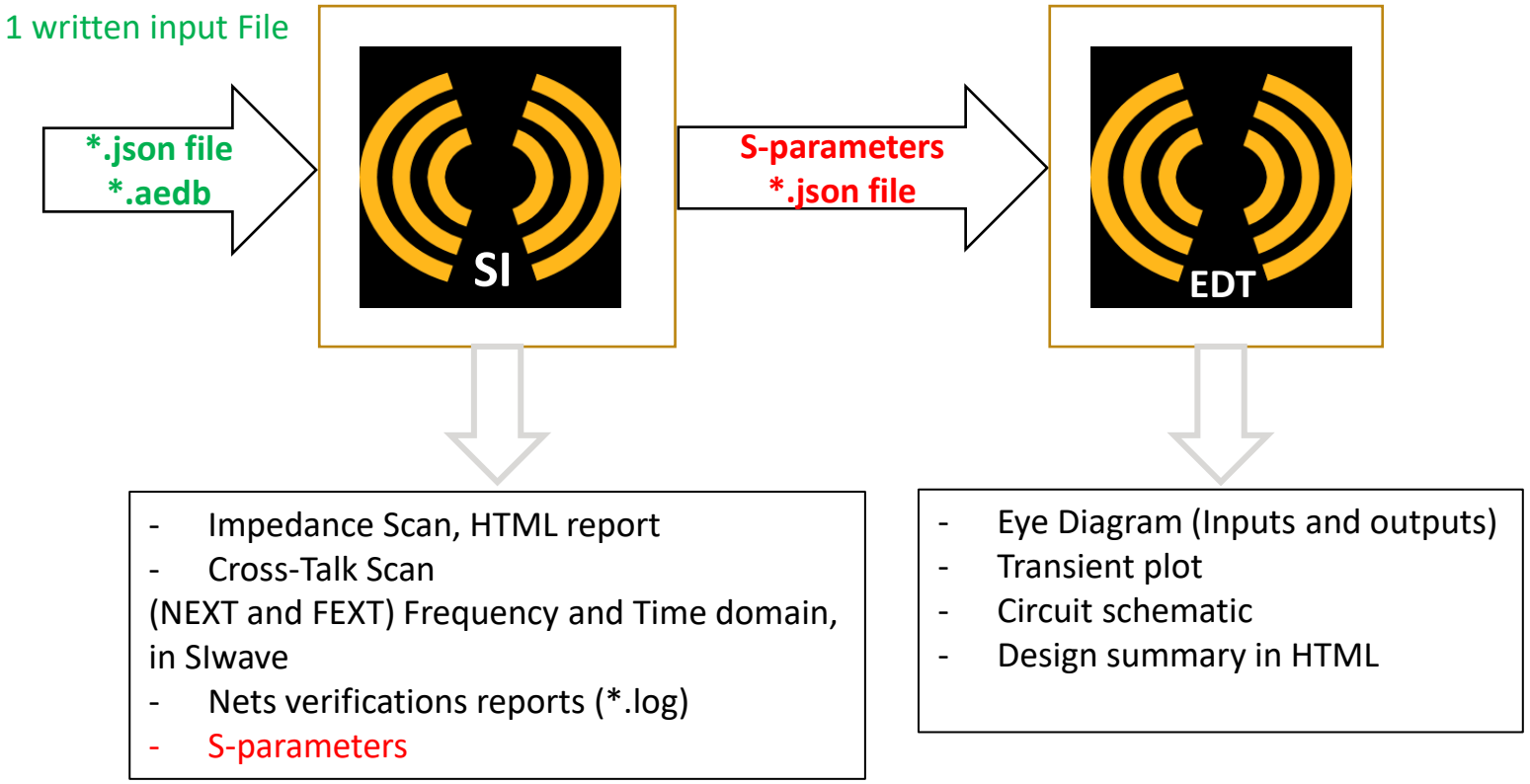
- HFSS fully arbitrary 3D FEM
- HFSS 3D Layout
- Maxwell 3D/2D
- Q3D/Q2D Extractor
- **Circuit Simulation**

What is Ansys Minerva?

- Enterprise level Simulation Process and Data Management solution
- User friendly and web based
- Addresses critical issues associated with simulation data such as:
  - Archiving
  - Traceability
  - Process Automation
  - Collaboration
  - Knowledge Capture
  - IP protection
  - Configuration Management
- Open architecture designed to integrate with other solutions and services
- Ability to leverage High Performance Computing resources (HPC)

Our proposed flow

For a full SI analysis, the workflow for the user interface is :



It is not necessary to use this interface to do a complete SI analysis. We can do targeted and individual simulations of the following types:

- Impedance scan
- Time domain crosstalk scan
- Frequency domain crosstalk scan
- SYZ-parameters computation
- S-parameters extraction **and full AEDT analysis**

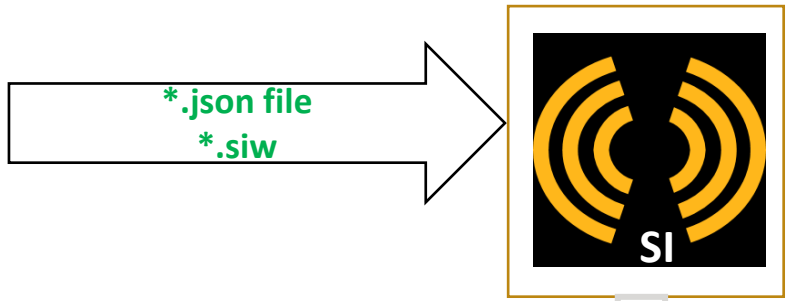
By specifying well in the JSON file the desired simulations combination.

Our proposed flow

It can happen that you only want to do a specific type of simulation, you can either use the full SI analysis interface or choose another type of interface.

SI analysis only on SIwave

1 written input File



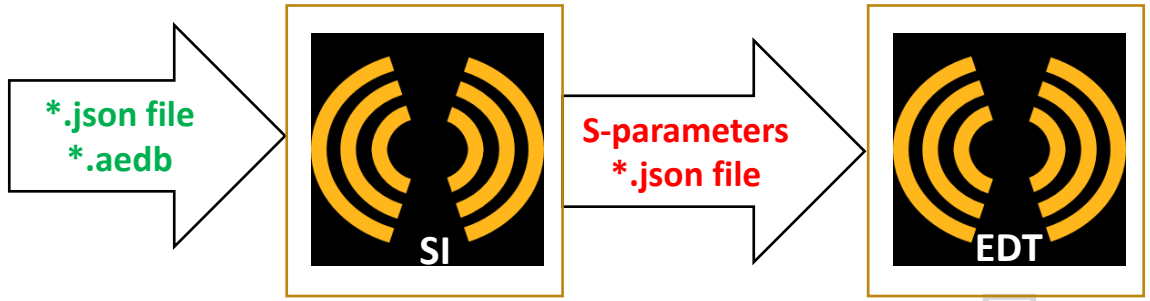
- Impedance Scan, HTML report
- Cross-Talk Scan

(NEXT and FEXT) Frequency and Time domain, in SIwave

- Nets verifications reports (*.log)

SI analysis only on AEDT using SIwave

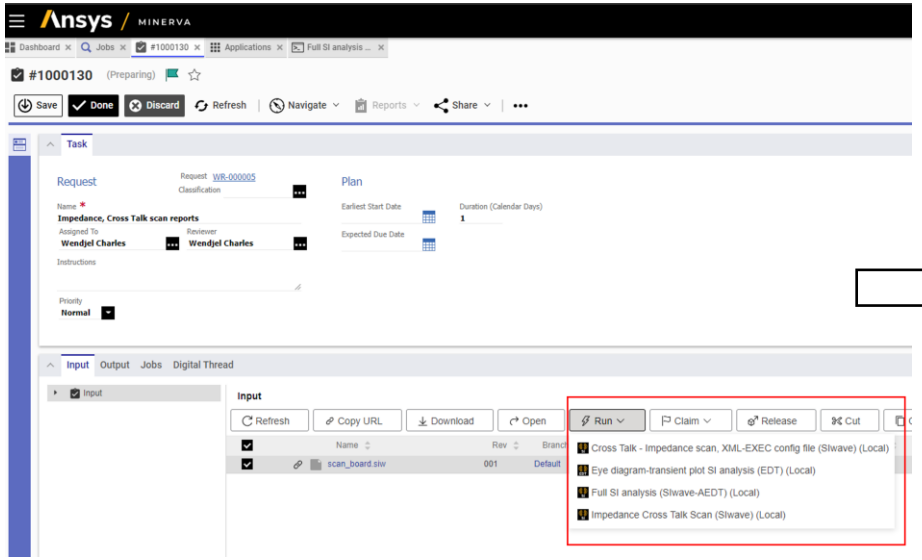
1 written input File

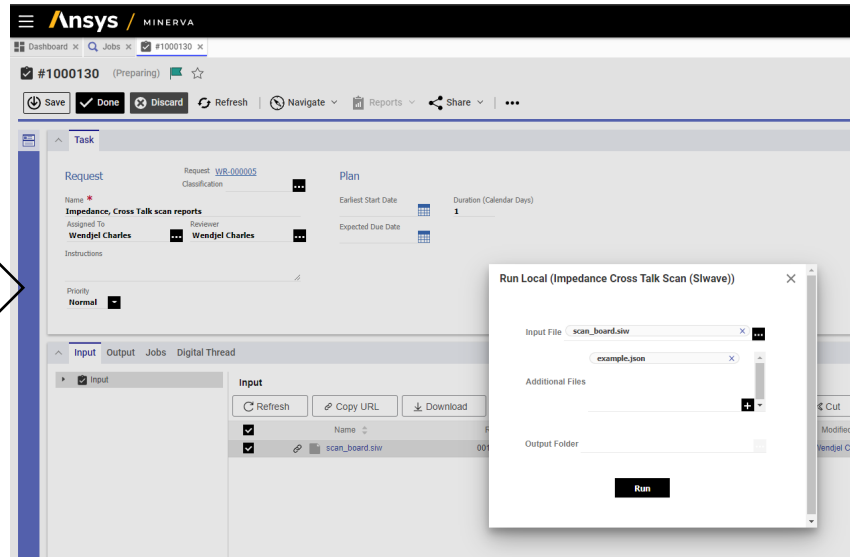


- Eye Diagram (Inputs and outputs)
- Transient plot
- Circuit schematic
- Design summary in HTML

Ansys solution

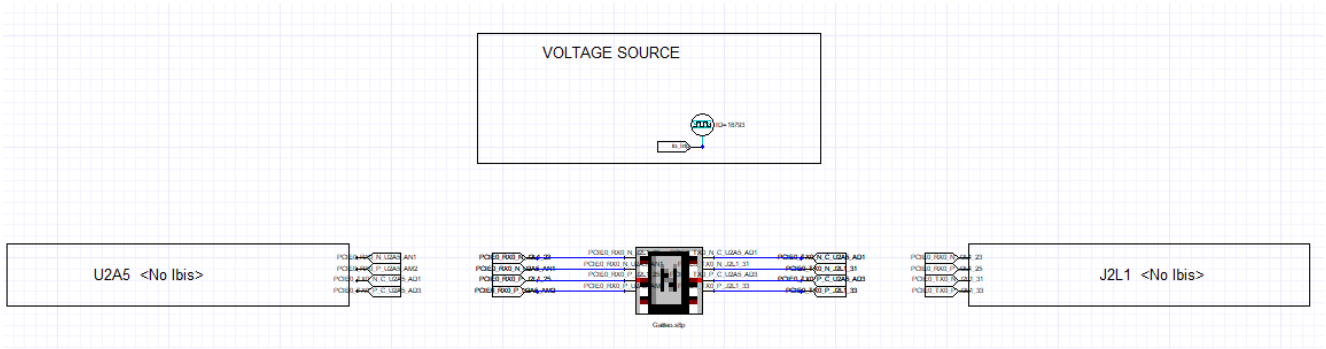
- It can be used internally to accelerate and facilitate SI analysis
- Or externally, on the customer side, to facilitate SI analysis for those who do not master SIwave or AEDT



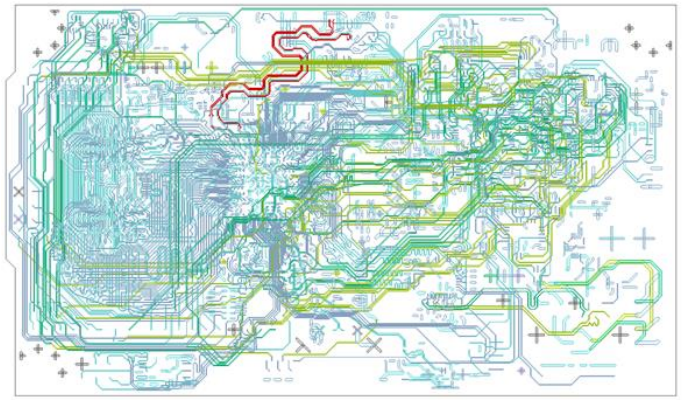


Study case: PCIe 1x

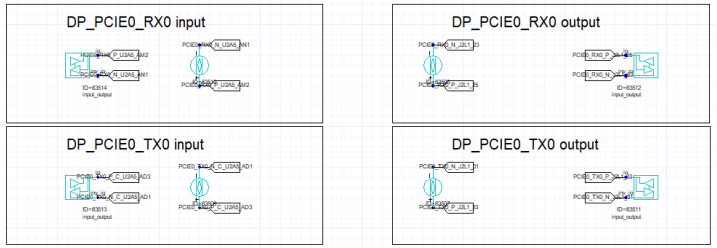
Equivalent model



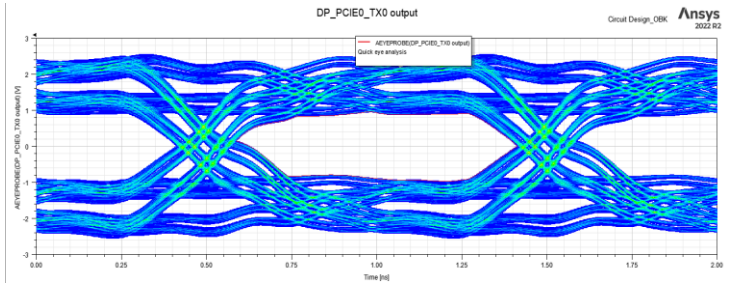
Galileo circuit board



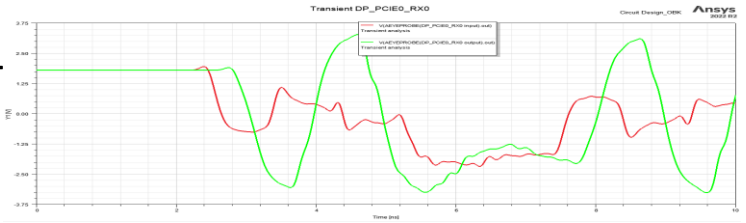
Non ideal inputs outputs



Eye diagram



Transient plot



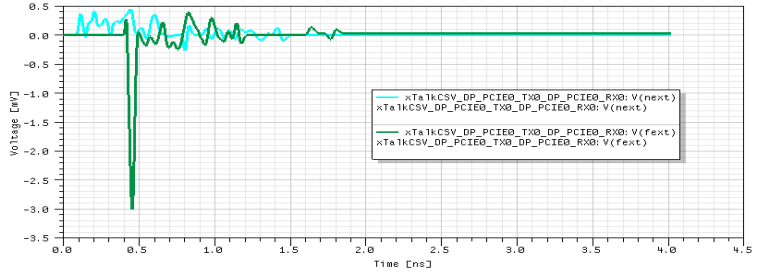
Impedance scan

Ansys SIwave 2022 R2 (solver build: Mar 16 2022 Win64) Host Name: LYOTRAINEE5

Single Ended and Differential Net Impedance Violation

Net Name	Impedance Warning Tolerance	Impedance Violation Tolerance	SE or Diff	Cross Section Type	Target Z0 (Ohms)	Violation	Layer of Violation	Max |Z-Z0|/Z0	Z of Max (Ohms)	Length of Max (mm)	Z of Longest Violation/Warning (Ohms)	Length of Longest Violation/Warning (mm)	Pairing Ratio length paired/length total
DP_PCIE0_RX0	10.0%	20.0%	Diff	MSL	100.0	Yes	"BOTTOM"	-71.3%	28.7	2.007	79.7	5.080	89.9%
							"TOP"	-20.3%	79.7	1.501	79.7	1.501	89.9%
DP_PCIE0_TX0	10.0%	20.0%	Diff	MSL	100.0	Yes	"BOTTOM"	-71.3%	28.7	2.007	79.7	3.291	84.8%
							"TOP"	-20.3%	79.7	1.160	79.7	1.160	84.8%

Time domain



Frequency domain

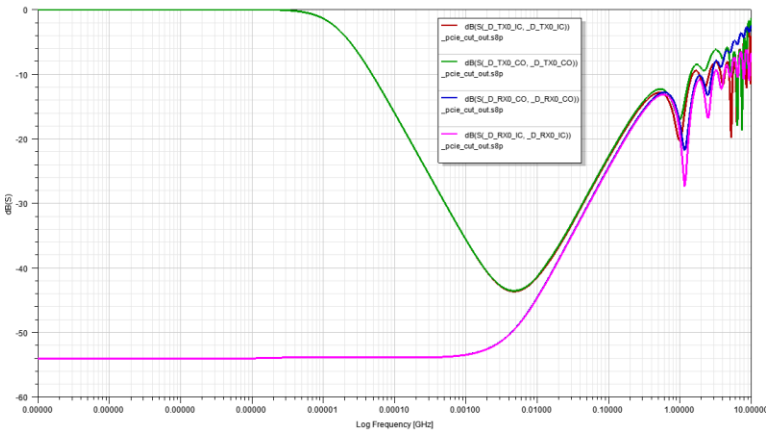
NEXT coefficient

Net Name	NEXT Warning Tolerance	NEXT Violation Tolerance	SE or Diff	Cross Section Type	Violation	Layer of Violation	Max NEXT	Length of Max NEXT (mm)	NEXT of Longest Line Section	Length of Longest Line Section (mm)
DP_PCIE0_RX0	0.100	0.200	Diff	MSL	No		0.002	2.682	0.002	4.550
DP_PCIE0_TX0	0.100	0.200	Diff	MSL	No		0.002	2.065	0.002	4.576

FEXT coefficient

Net Name	FEXT Warning Tolerance (ns/m)	FEXT Violation Tolerance (ns/m)	SE or Diff	Cross Section Type	Violation	Layer of Violation	Max FEXT (ns/m)	Length of Max FEXT (mm)	FEXT of Longest Line Section (ns/m)	Length of Longest Line Section (mm)
DP_PCIE0_RX0	0.100	0.200	Diff	MSL	No		0.011	2.682	0.011	4.550
DP_PCIE0_TX0	0.100	0.200	Diff	MSL	No		0.012	2.065	0.011	4.576

S-parameters



Benefits

- Impedance scan
- Time domain Crosstalk scan
- Frequency Domain Crosstalk scan
- S-parameters computation
- S-parameters exportation

SIwave

- Schematic Design
  - Input /outputs
  - Mode (ideal or not)
- Simulation configuration
- Eye diagrams
- Transient Plots

AEDT

- Write a **JSON** file with a predefined syntax, with the desired **simulation settings**.
- 3 clicks to run on Minerva

Only need to check that all the information recorded in the JSON is the wanted one.
In any case, there will be verifications for the nets name.

After each simulation step, there is a need for verifications before performing others.

Signal Integrity Analysis in Ansys Minerva using PyAEDT

Engineering Goals

- **Reduce** signal integrity (SI) analysis time
- **Prevent** unwanted errors while doing SI analysis
- **Reduce** SI analysis steps
- **Facilitate interaction** between teams on working files

Ansys Solution

- **Only one written Input** for the full SI analysis
- **One to many simulations type** with the same interface
- **Nets verification** in SIwave
- **Ports manager for AEDT**
- **Automatically generated organized reports**

Benefits

- **20-60%** reduction in SI analysis time
- **Optimized** analysis time
- **10 steps in 1 step** to get all SI factors**, 3 clicks** on Minerva
- **No need to be an expert** in SIwave or AEDT circuit