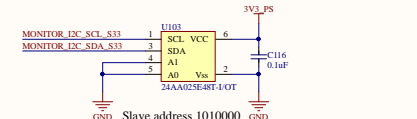
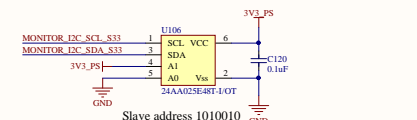


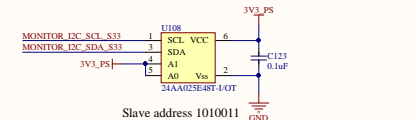
MAC-ID Ethernet SVC



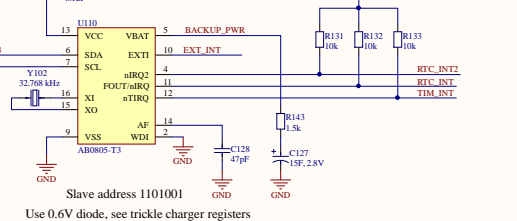
MAC-ID Ethernet Zynq



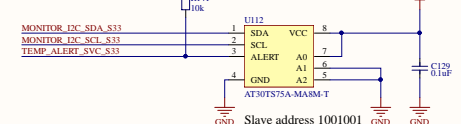
MAC-ID SFP Zynq

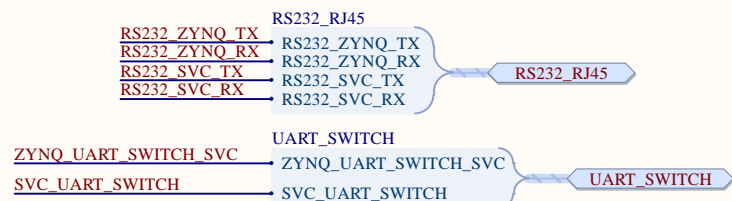
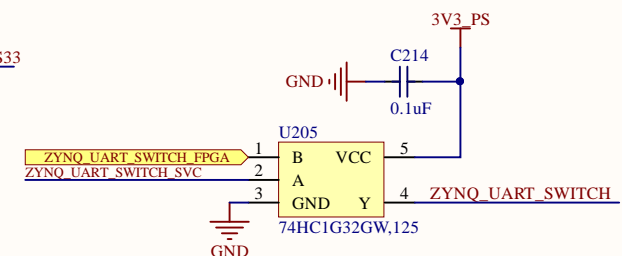
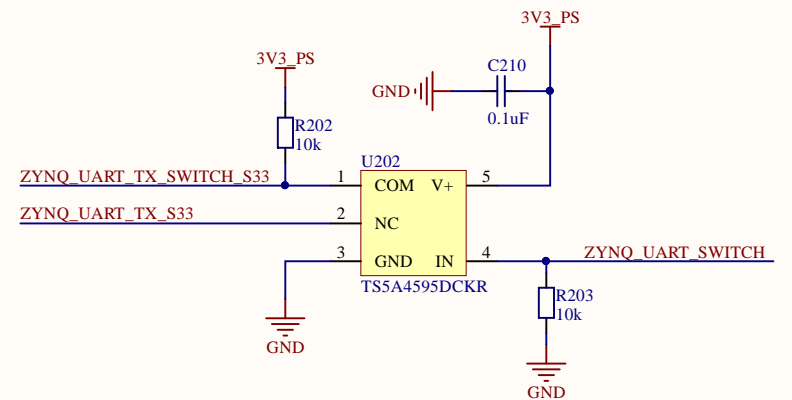
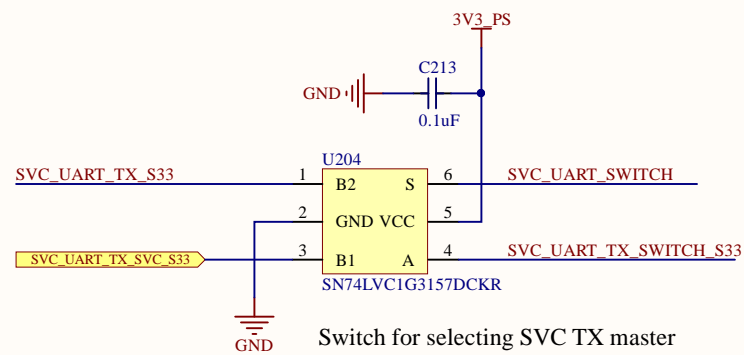
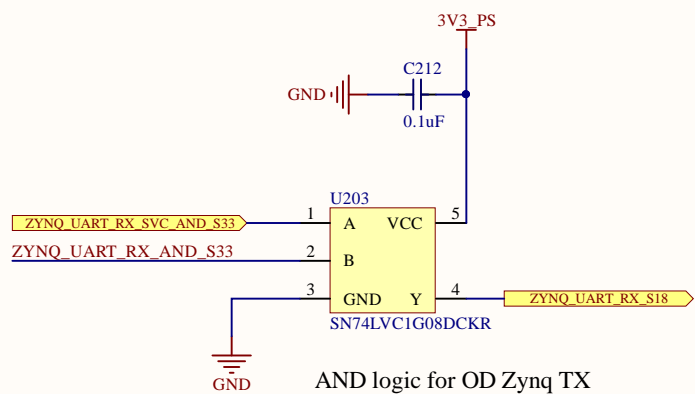
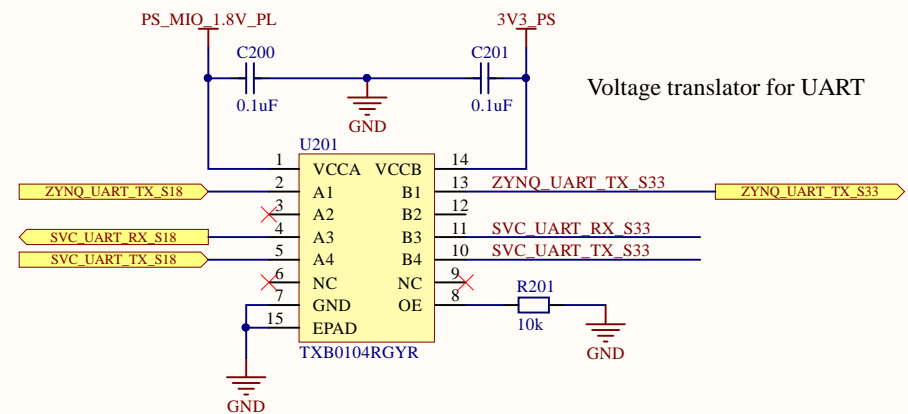
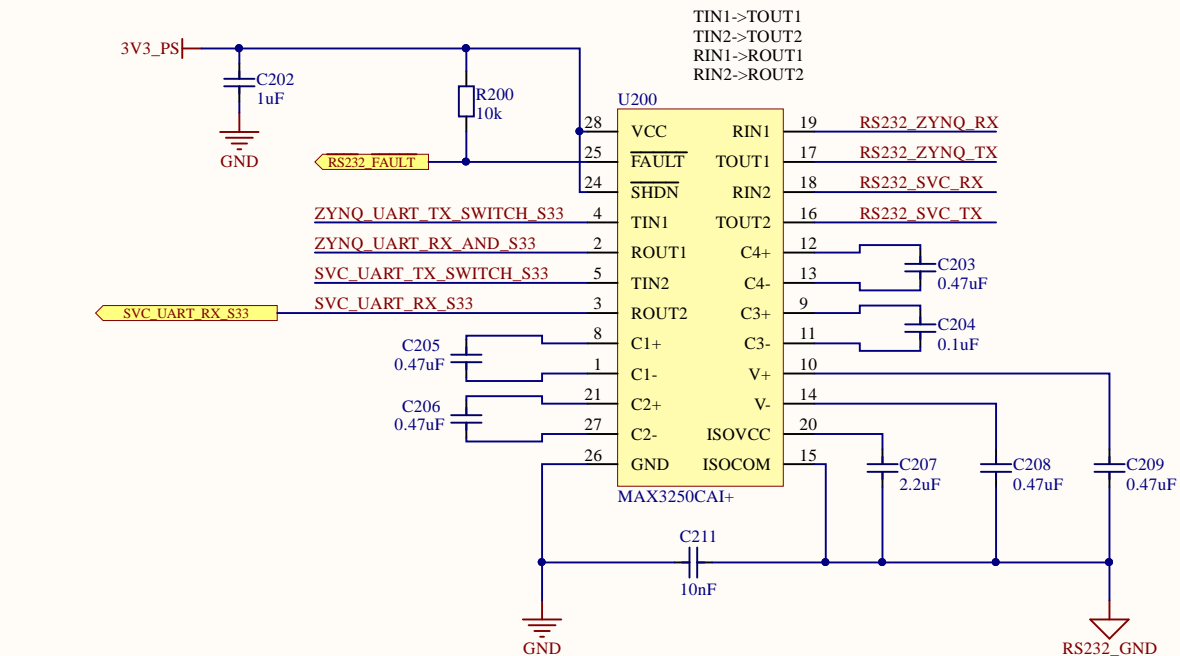



RTC

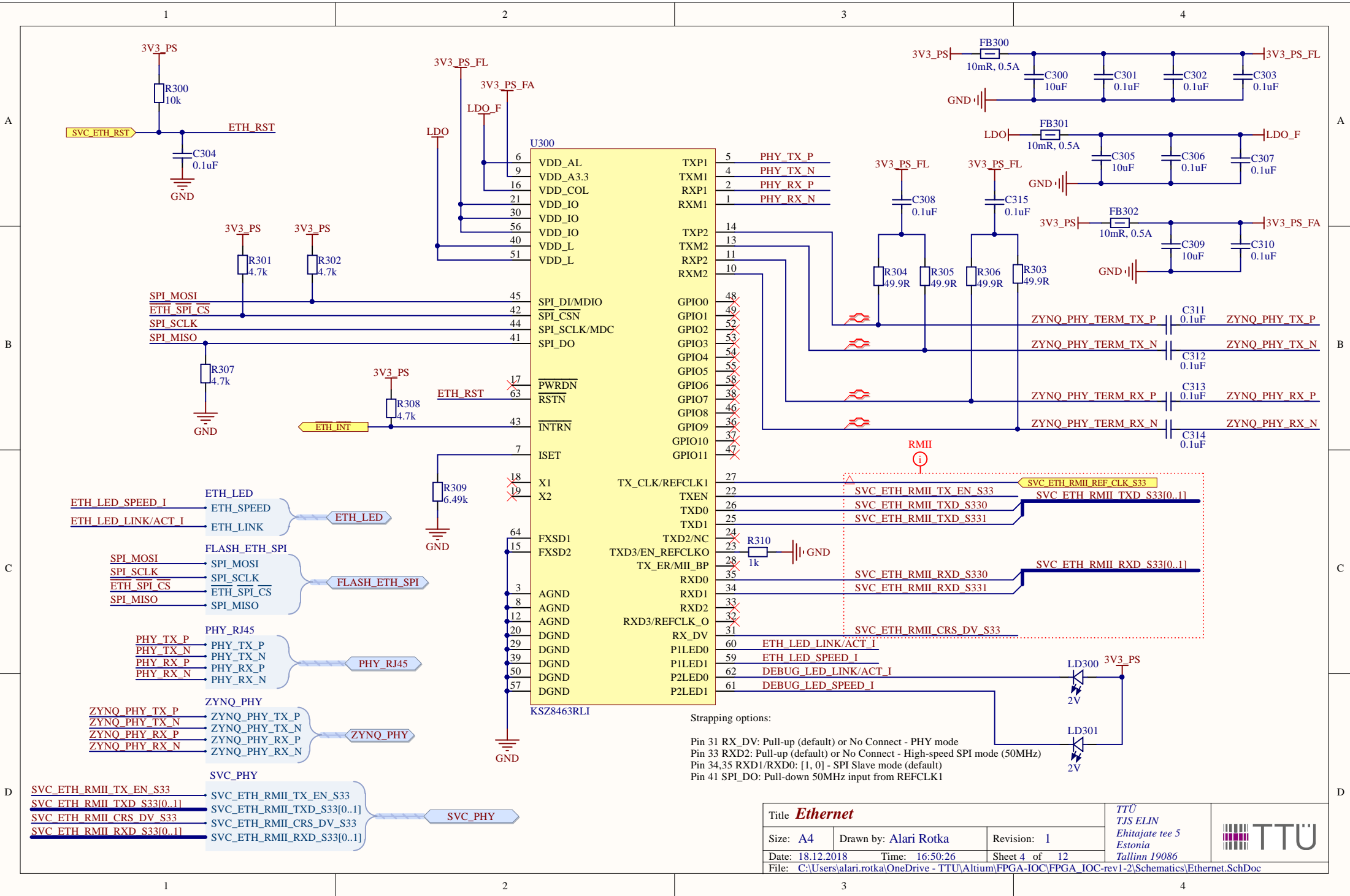


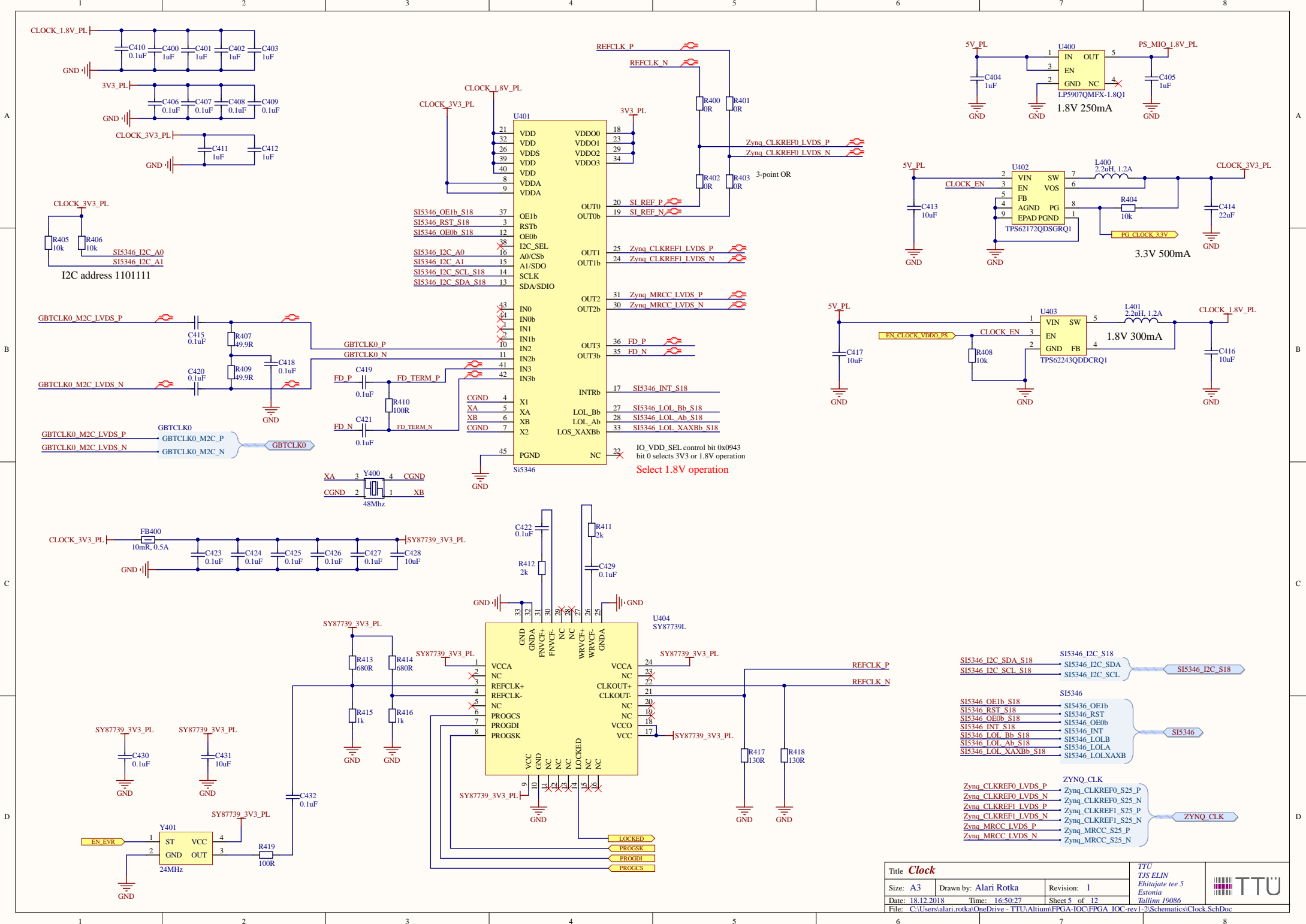
Temp sensor

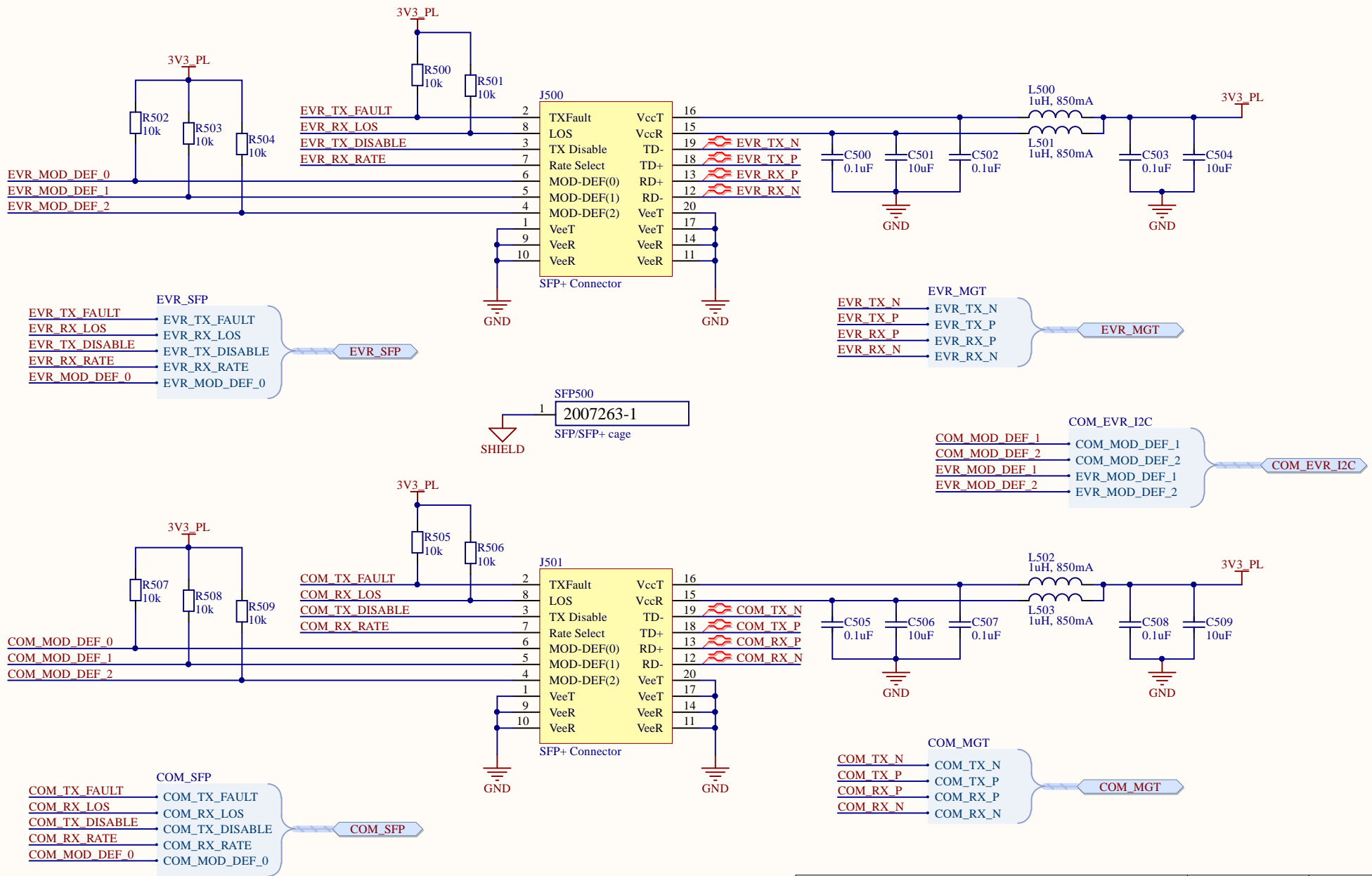




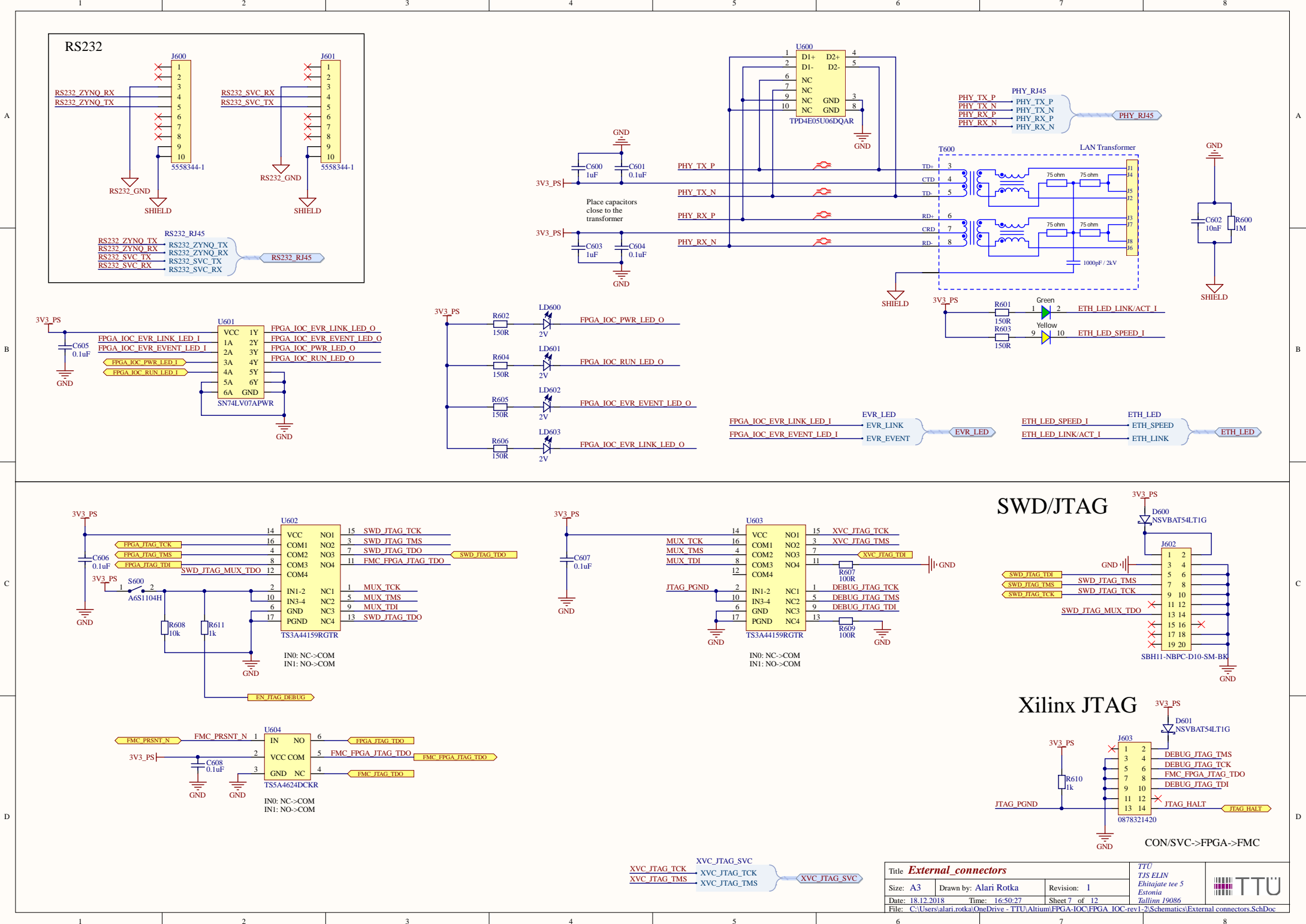
Title RS-232			<i>TTÜ</i> <i>TJS ELIN</i> <i>Ehitajate tee 5</i> <i>Estonia</i> <i>Tallinn 19086</i>		 T
Size: A4	Drawn by: Alari Rotka	Revision: 1			
Date: 18.12.2018	Time: 16:50:26	Sheet 3 of 12			
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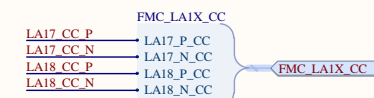
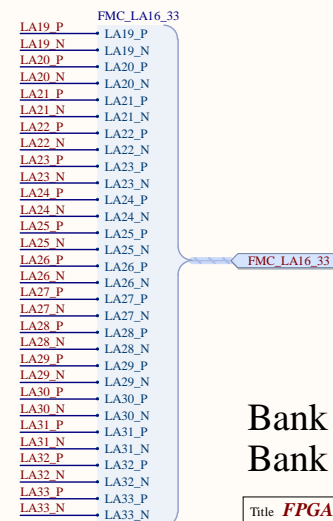
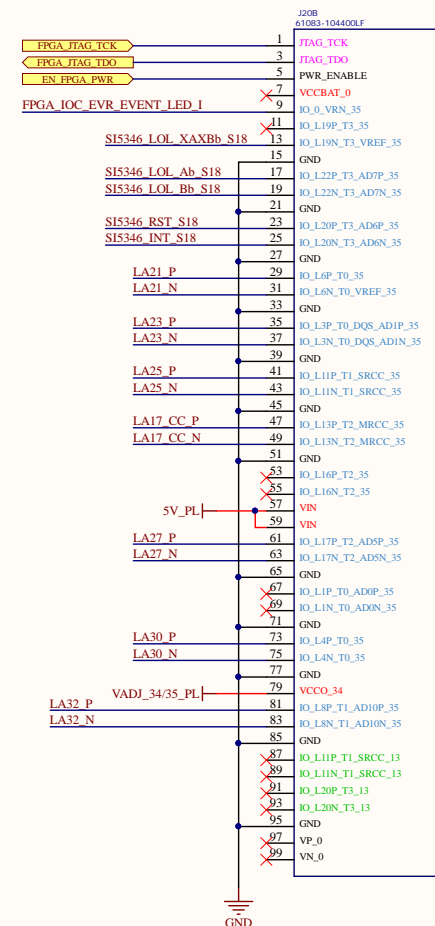
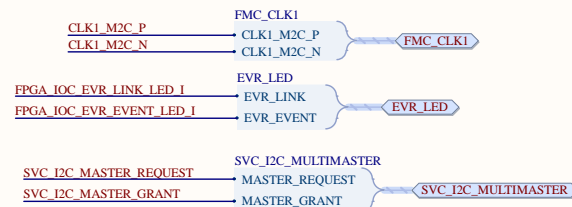
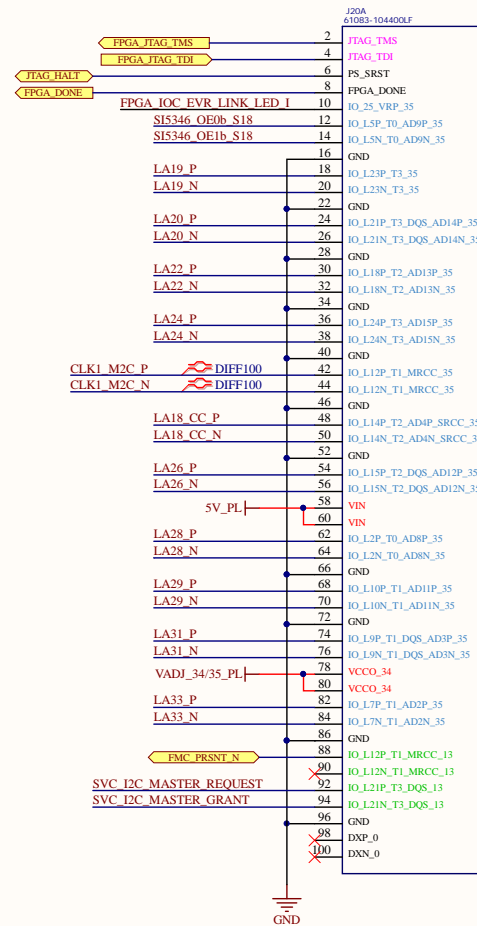
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Size: A4	Drawn by: Alari Rotka	Revision: 1		
Date: 18.12.2018	Time: 16:50:27	Sheet 6 of 12		
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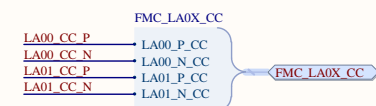
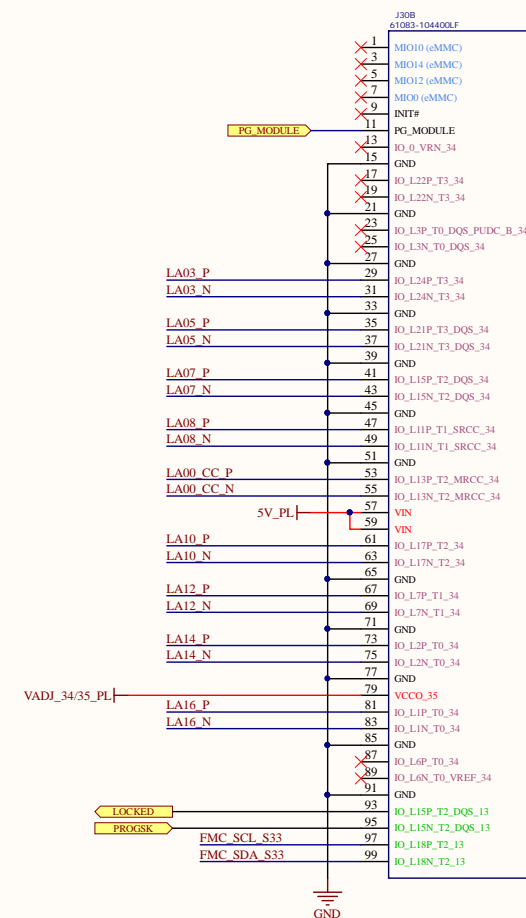
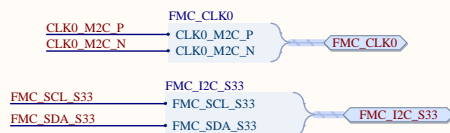
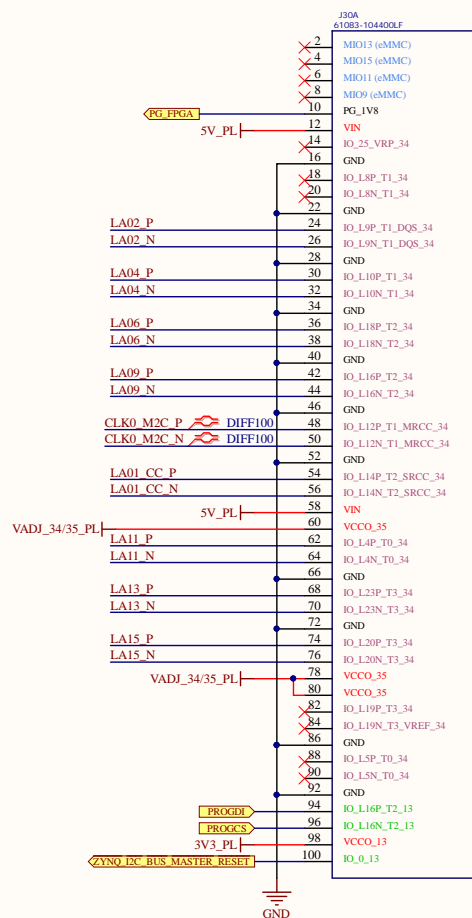
External connectors

Title	A3	Drawn by: Alari Rotka	Revision: 1
Date: 18.12.2018	Time: 16:50:27	Sheet 7 of 12	
File: C:\Users\alari.rotka\OneDrive - TTU\Altium\FPGA-IOC\FPGA_IOC-rev1-2\Schematics\External connectors.SchDoc			




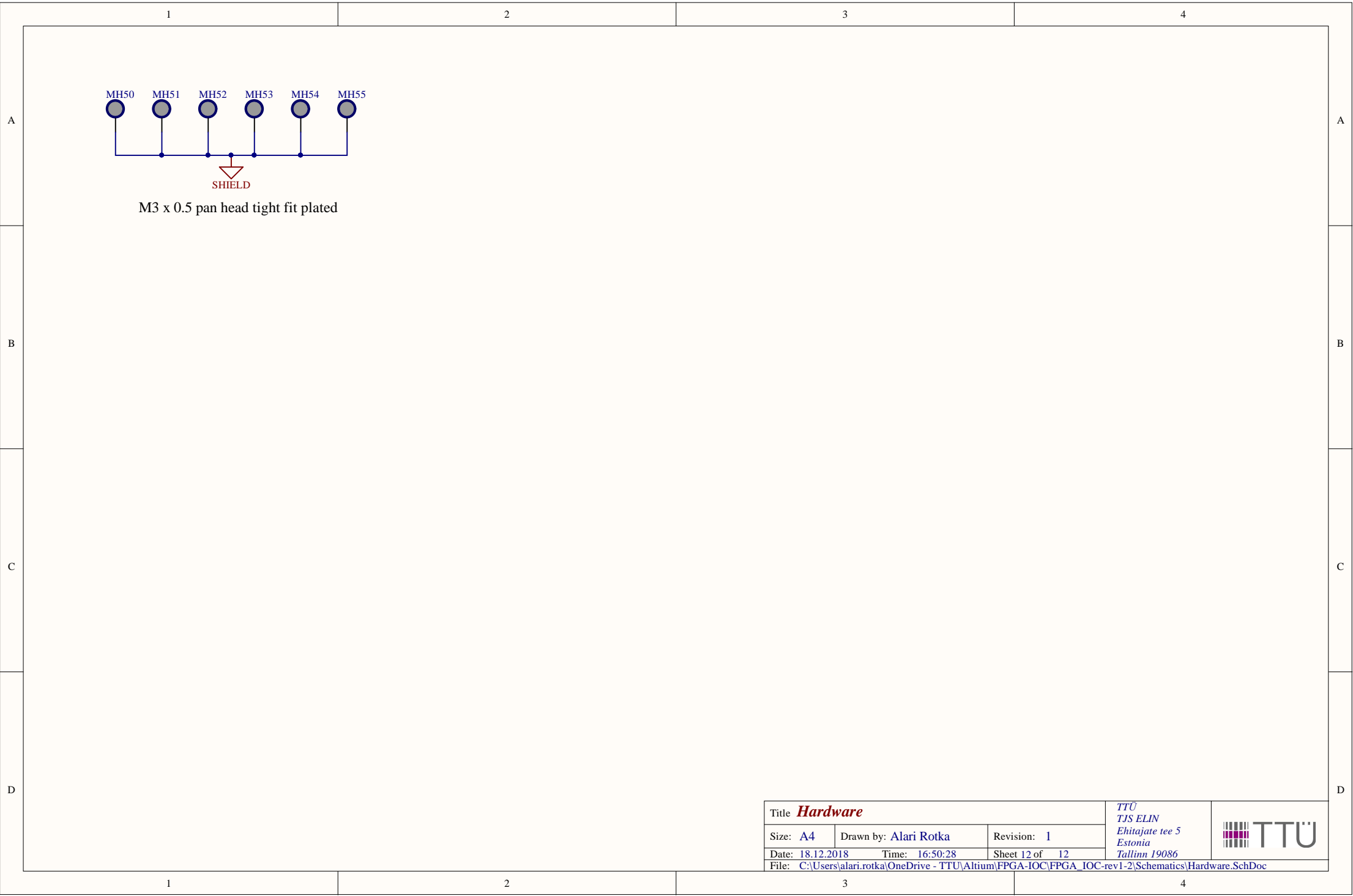



Bank 13 voltage 3.3V
Bank 35 voltage VADJ (1.2V, 1.5V, 1.8V)



Bank 0/500 voltage 3.3V
Bank 13 voltage 3.3V
Bank 34 voltage VADJ (1.2V, 1.5V, 1.8V)

Title FPGA_connector_B			<i>TTÜ</i> <i>TJŠ ELIN</i> <i>Ehitajate tee 5</i> <i>Estonia</i> 	
Size: A3	Drawn by: Alari Rotka	Revision: 1		
Date: 18.12.2018	Time: 16:50:28	Sheet 10 of 12	<i>Tallinn 19086</i> <i>C:\Users\alari.rotka\OneDrive - TTÜ\Altium\FPGA-IOC\FPGA_IOC-rev1.2\Schematics\FPGA_connector_B.SchDoc</i>	



Title <i>Hardware</i>			
Size: A4	Drawn by: Alari Rotka	Revision: 1	
Date: 18.12.2018	Time: 16:50:28	Sheet 12 of 12	
File: C:\Users\alari.rotka\OneDrive - TTÜ\Altium\FPGA-IOC\FPGA_IOC-rev1-2\Schematics\Hardware.SchDoc			