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TO: JECO Director of Engineering

SUBJECT: Project 1:

1. Statement of Purpose

The goal of the present project was to design an optical transmitter-receiver system to communicate audio signals under 3 kHz, encoding them around 80 kHz, utilizing a BJT and LED driver, to be received and decoded by a comparator and PLL system.

2. Theory and Design

2.1 Theory

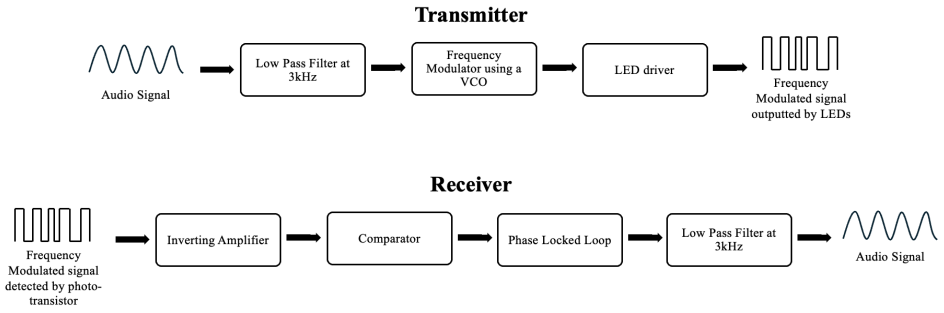

Figure 1 - System's block diagram

As described above, one of the main purposes of the system developed was to perform an FM modulation and demodulation of the input audio signal to achieve its optical transmission from one circuit to the other. The two sections below briefly explain how this modulation and demodulation was achieved using a VCO and PLL respectively.

2.1.1 Frequency Modulation using a Voltage Controlled Oscillator

Frequency Modulation consists of varying the frequency of the modulated signal in accordance to the amplitude of the modulating signal. This is achieved by choosing a carrier frequency f_c at which the modulated signal will oscillate when the modulating signal's amplitude is zero. Then, as the modulating signal's amplitude increases, the modulated frequency decreases and vice versa. Then, the modulated signal obtained will have a frequency that varies in an interval of $\left[f_c - \Delta f,\ f_c + \Delta f\right]$ and encodes the amplitude of the initial modulating wave (Iberite, 2021). This process is illustrated below in *Figure 2*. Further, it is important to note that the present project was designed with a carrier frequency of $f_c = 80kHz$ and the modulation was done with a bandwidth of $\pm\ 20\%$.

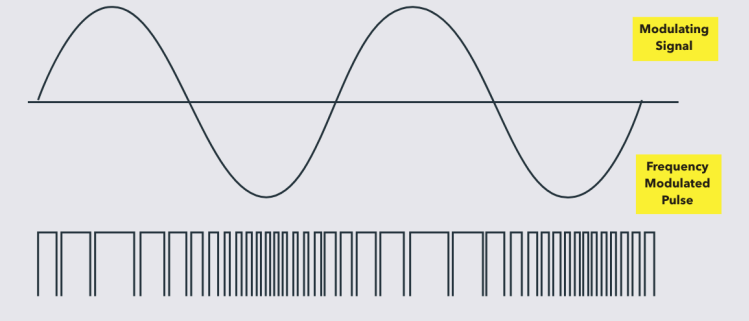

Figure 2 - Frequency Modulation of a Sinusoidal Signal

The Frequency Modulation of the input audio wave was done using a VCO circuit. A VCO is a device that outputs a square wave whose frequency varies depending on an inputted control voltage. Therefore, if the input is a sinusoidal wave, the output's frequency will vary in accordance with the input's amplitude, thus frequency modulating the input wave (Stiles, 2008).

2.1.2 Signal Demodulation using a Phase Locked Loop

Once the modulated signal was transmitted to the receiver circuit, it was demodulated using a Phase Locked Loop. PLLs are made of a feedback loop containing a phase detector, a low pass filter, and a VCO, as seen below in *Figure 3*. The phase detector takes in the input signal and the VCO's output, which is set to oscillate at the modulated signal's carrier frequency f_c. The phase detector outputs the phase difference of the two signals inputted. If the two signals oscillate at the same frequency, then the phase difference will be constant; however, if they oscillate at the different frequencies their phase differences will vary (Stiles, 2008). Therefore, the phase difference outputted by the phase detector encodes the modulated signal's deviation from the carrier frequency, and thus the amplitude of the original audio signal. This way, demodulation is achieved using the PLL's feedback loop.

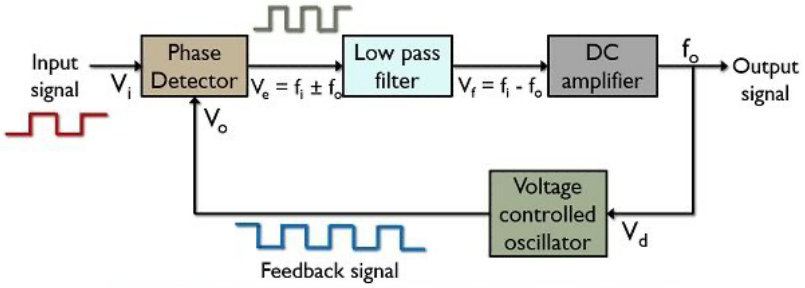

Figure 3 - PLL Block Diagram

2.2 Design

2.2.1 Transmitter

The design of the transmitter was created from the block diagram in *Figure 1*. The transmitter was broken into (3) components, each of which were designed separately, then integrated into the final transmitter board:

1. Input & Low Pass Filter
    a. Goal: Filter out input high-frequencies to only modulate audio frequencies < 3 kHz
2. Frequency Modulator (Voltage-Controlled Oscillator)
    a. Goal: Modulate the input audio message signal using Pulse-Position Modulation centered around 80 kHz.
3. LED Driver and LEDs
    a. Goal: Transmit the modulated message signal using infrared (IR) LEDs.

Beginning with the Input & Low Pass Filter component, an active low pass filter design was identified - Sallen Key Active Low Pass Filter. *Figure 4* below details the design of the active filter. For the OP AMP component, a LM318 was utilized with supply voltages of +9 V and -9 V. V_{IN} is the audio signal input, which is the input to our transmitter. For the purposes of testing the low-pass filter, V_{IN} was connected to the function generator.

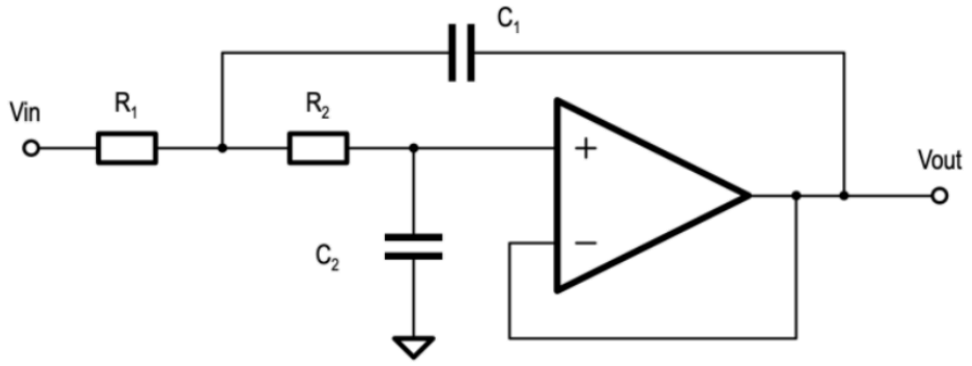

Figure 4 - Sallen Key Active Low Pass Filter Design

To achieve a f_C of approximately 3kHz, the following values were utilized. These values were determined based on testing using the function generator and oscilloscope, with varying frequencies. The graph in *Figure 5* below highlights the results of the testing - notably, the -3 dB point (also known as the break frequency) is approximately 2.9kHz.

- R_1 = 200 Ohm
- R_2 = 510 Ohm
- C_1 = C2 = 0.1 uF

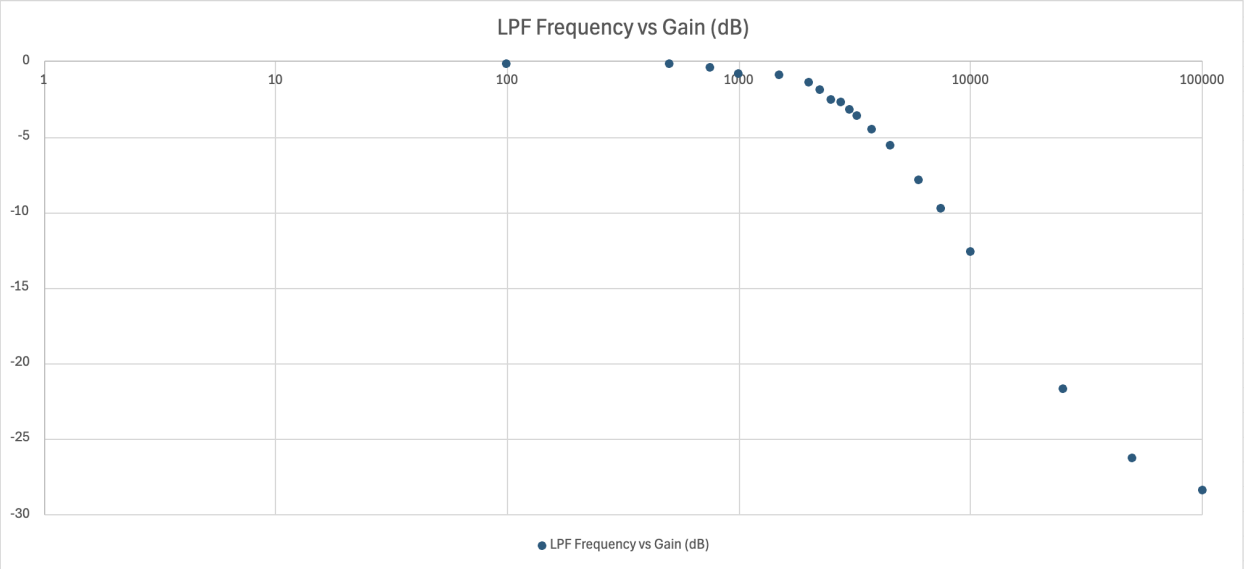

Figure 5 - Graph of Measured Data from Active Low Pass Filter

The frequency modulator of the transmitter was constructed with a 555 Timer. The 555 Timer was utilized in the 'Astable Mode' of operation to function as a Voltage-Controlled-Oscillator (VCO). The team chose the 555 timer to modulate frequencies due to the simplicity of the FM modulator circuit in comparison to the 4046 phase-lock-loop VCO. In order to modulate the message signal, the team analyzed the datasheet of the 555 timer (in this case, Texas Instrument's NE555P). From the datasheet, a frequency modulator circuit was identified, shown in *Figure 6* below.

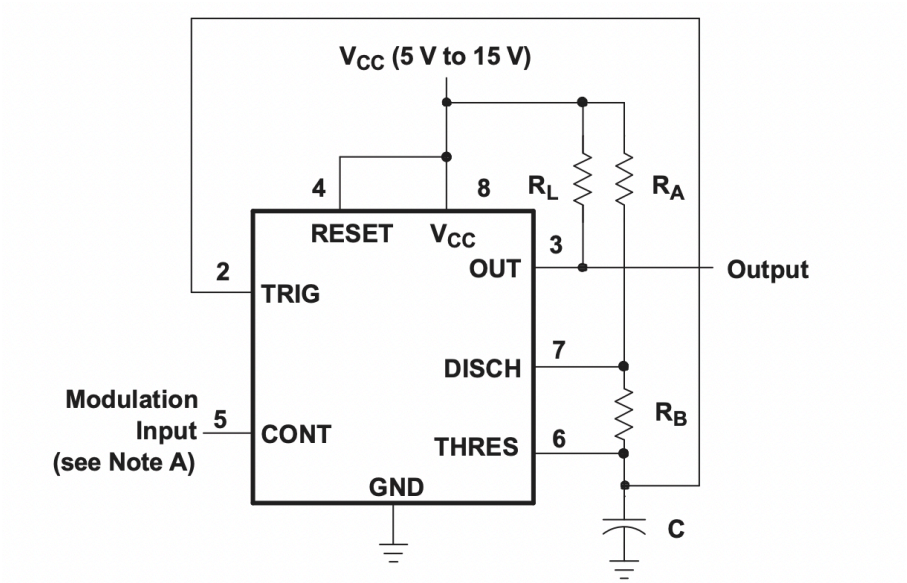

Figure 6 - Pulse-Position Modulation Application Circuit from XX555 Datasheet

In order for the frequency modulation to be centered at the given 80kHz, the team identified a relationship between the components in the above diagram and the astable frequency. The VCO should oscillate at 80kHz when the input (Pin 5 above) is 0 VDC. The relationship between the above components and the modulation center frequency is described by Equation 1 below:

$$frequency \approx \frac{1.44}{(R_A+2R_B)C} \quad (1)$$

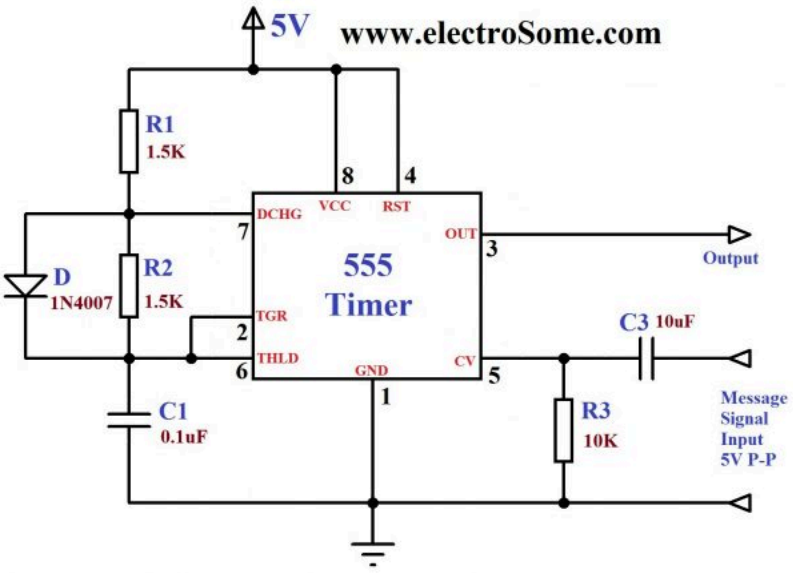

Figure 7 - electroSome Modified Pulse-Position Modulation Application Circuit

To ensure that the message signal was properly modulated, a few additional components were added to the application circuit from the datasheet. The above *Figure 7* from electroSome details changes: A diode *D*, Resistor R_3, and DC-blocking capacitor C_3 were added to improve modulation. Additionally, the VCC was set to +9 VDC, not +5 VDC.

In the case of our VCO, after testing the circuit with calculated values, final values for R_A, R_B, and C=C_1 were identified to ensure the VCO oscillated at a center-frequency of 80kHz:

- $R_A = R_1 = 91\ k\Omega$
- $R_B = R_2 = 129\ k\Omega$ (tuned using a potentiometer)
- $C = C_1 = 100\ pF$

After verifying the oscillation of the VCO at 80kHz without a message signal, the team inputted a message signal (at 2kHz) into Pin 5 of the NE555P component prior to the DC blocking capacitor C_3. The team varied the amplitude of the message signal and determined that an input of 0.450 V_{PP} at 2kHz successfully modulated at frequencies between 70 and 90 kHz. Furthermore, it was noted that as V_{PP} increased, the frequency deviation (Δf) from f_0 = 80 kHz increased. Concluding the VCO design, the team decided to delete the Low-Pass Filter before the VCO, and instead input the message signal directly from the function generator to the input of the VCO during demonstration testing.

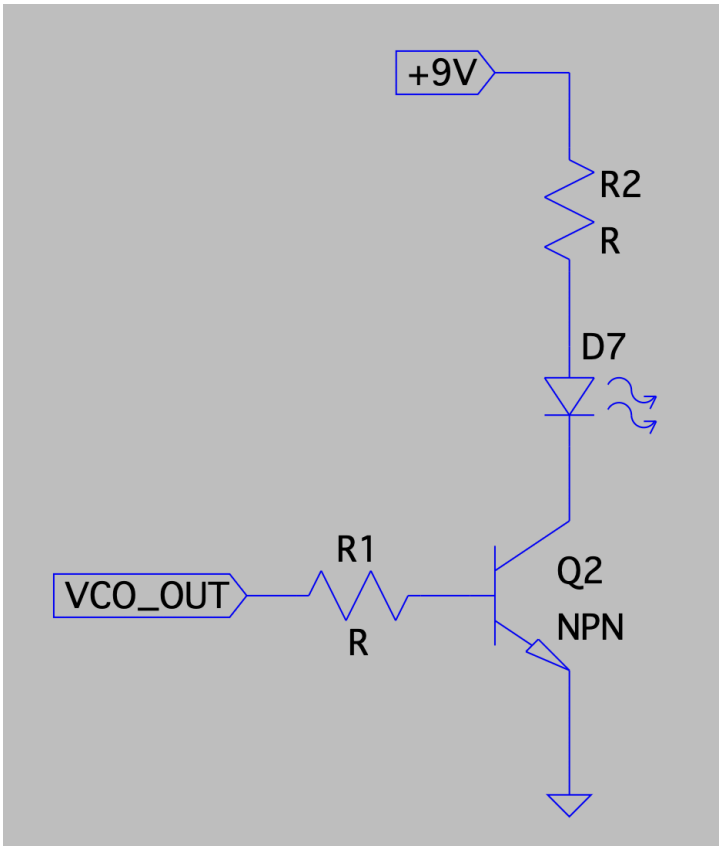

Figure 8 - Basic LED Driver

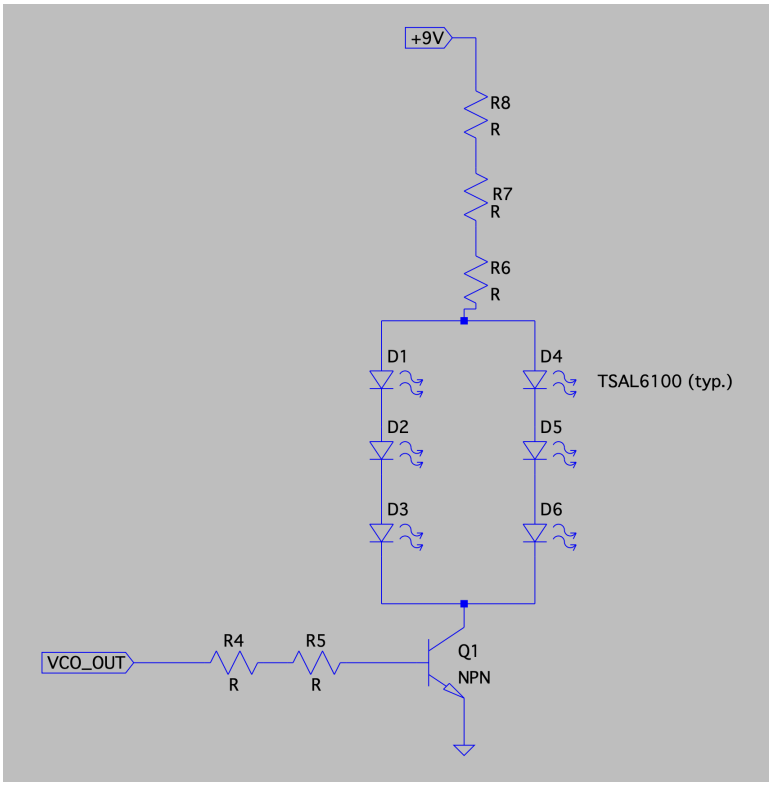

Figure 9 - Modified LED Driver

The LED Driver, shown in *Figure 8*, was designed around an NPN transistor in active mode. Since the amplitude of the VCO Output was +9 V (V_{DD}), the team utilized the LED Driver above to ensure the Infrared LEDs (6x TSAL6100) switched ON when the signal was high, and switched OFF when the signal was low. The switching rate is determined by the frequency of the VCO Output, which was the modulated version of the message signal.

A key decision that the team made that resulted in the success of the IR transmission was using (6) LEDs. The (6) LEDs were built out in parallel to ensure that the voltage drop of the diodes kept the NPN transistor in Active mode. Additionally, with parallel LED configuration, the nominal current through each of the (6) LEDs was 100 mA. This nominal current was determined by resistors R_6, R_7, and R_8 in the above *Figure 9*. The Electronics Circuit Diagram is shown below in *Figure 10*. This concludes the design of the Transmitter.

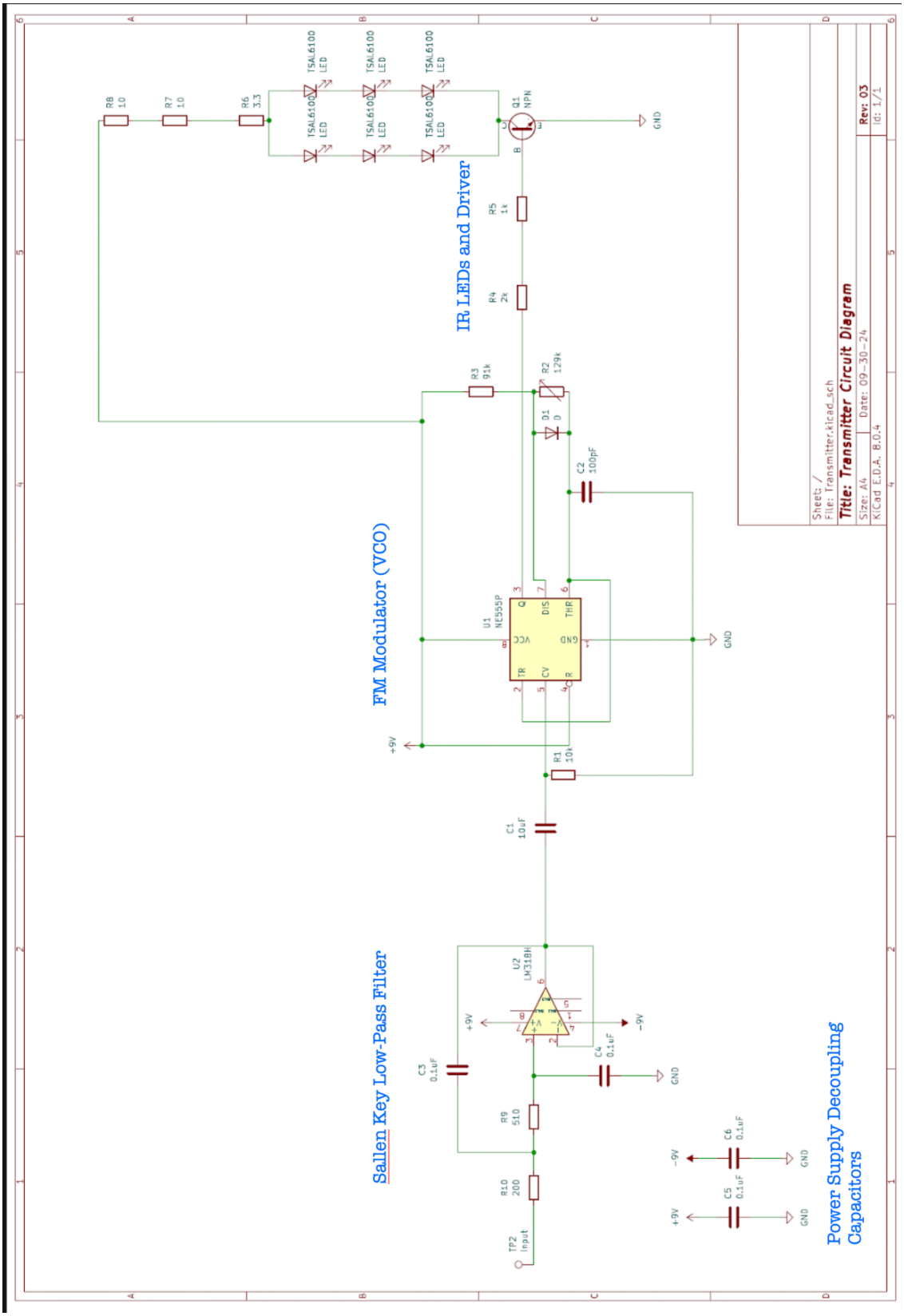

Figure 10 - Completed Transmitter Schematic

2.2.2 Receiver Design

The design of the receiver was based off of *Figure 1*, and a completed Electronic Circuit Diagram is shown below in *Figure 11*; this will be referenced throughout the section.

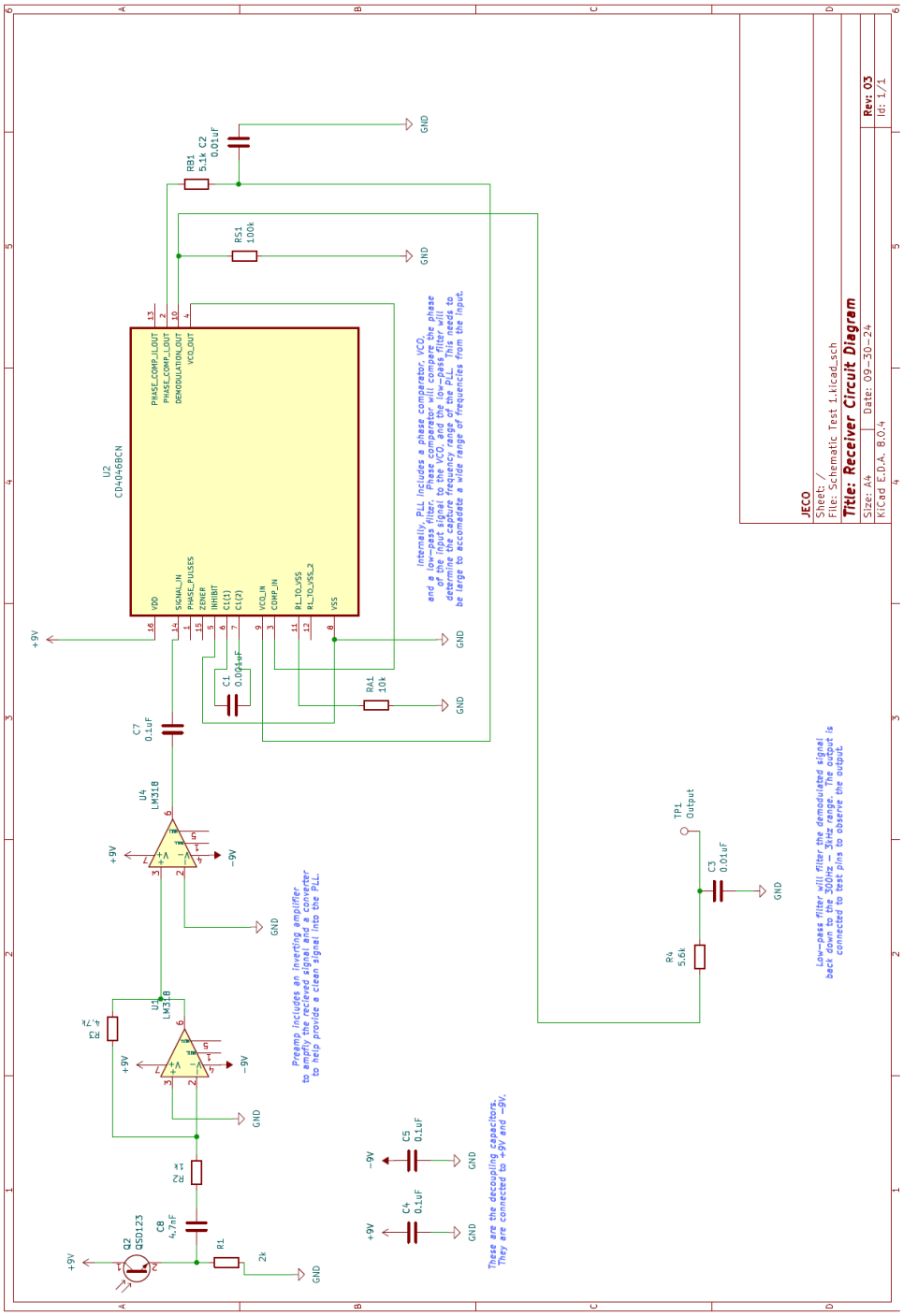

Figure 11 - Completed Receiver Schematic

The design begins with a detector. The detector circuit, provided by Fairchild Semiconductor, includes a phototransistor used as a Common-Collector Amplifier. This allows for the output to transition from a low to a high state, and the transistor operates in the active mode. Forcing the transistor to operate in the active mode allows it to create a proportional output to the amount of IR light it detects. The resistor "R_1" shown in *Figure 11* controls the sensitivity of the phototransistor, and a larger resistor makes it more sensitive to light. A 2kΩ resistor was chosen, for it was believed that it would be sufficiently large enough to help the phototransistor detect the IR light from the LED Driver. Once the output is obtained from the phototransistor, it goes through a 4.7nF decoupling capacitor, which removes the DC bias, giving the signal a DC average of 0; i.e., centers the signal at ground.

The next portion of the receiver is the Pre-Amp. The Pre-Amp is included to both amplify and clean the signal coming from the detector. The Pre-Amp includes an inverting amplifier and a comparator, which are both op-amp circuits. The inverting amplifier provides a gain of -4.7 to the signal. The calculation for the overall gain of the amplifier with the chosen resistor values is attached below in Equation 2 below.

$$A_v = \frac{-R_f}{R_i} \tag{2}$$

$$A_v = \frac{-4.7k\Omega}{1k\Omega} = -\ 4.7$$

This gain provides sufficient amplification. The signal then passes through the comparator; the design for the comparator was inspired by Josh Bishop's article on comparators. The signal enters the non-inverting pin of the op-amp and is compared to a reference voltage set by the connections at the inverting pin (Bishop, 2022). The reference voltage can be set by creating a voltage divider with resistors, but because the signal was centered at ground after going through the decoupling capacitor, it was beneficial to set the reference voltage to 0 in this case. Therefore, for the present design, the circuit will simply include an op-amp with the inverting pin connected to ground.

The next portion of the receiver is the PLL. Part of the constraints for the design is that the CD4046 must be used as the PLL. The data sheet for this device outlines how to use the CD4046 as a demodulator (Morgan, 2003), and the design is used in *Figure 11*. To find the values of R_{A1} and C_1, a chart was provided in the data sheet. These values determine what frequency the VCO is going to oscillate at and what voltage to apply to the CD4046. Because the design constraints require the VCO in the transmitter to oscillate at 80kHz, it was logical to have the PLL's VCO oscillate at the same frequency. The chart from the data sheet is shown below in *Figure 12*.

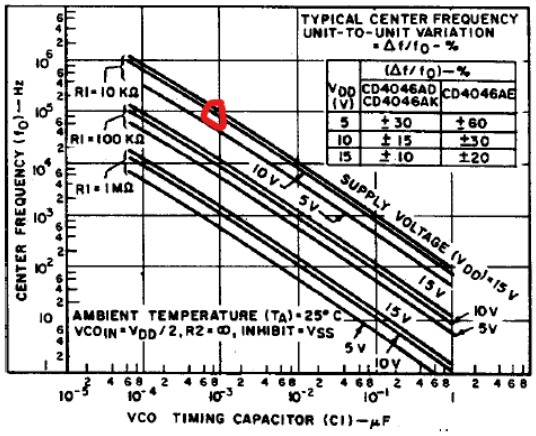

Figure 12 - Chart for R_1 and C_1

The red mark on the chart indicates all values chosen for the VCO portion of the PLL. At this mark, the center frequency is 80kHz, R_{A1} is 10kΩ, and C_1 is 0.001uF. Based on these values, the appropriate voltage to apply to the PLL is 9V. To find the values for the low-pass filter (R_{B1} and C_2 from Fig. 11), a simple equation can be used. This equation was also found in the data sheet and is shown below.

$$f_c = \frac{1}{2\pi}\sqrt{\frac{2\pi f_L}{R_{B1}C_2}} \tag{3}$$

f_c is the capture frequency, and f_L is the lock frequency of the PLL. According to the data sheet, the lock frequency can be set equal to the center frequency to allow the PLL to lock onto an input signal close to the VCO signal (Morgan, 2003). The capture frequency was set to be ±20% of the center frequency. If the center frequency is 80kHz, the capture frequency is 16kHz. This should be a broad enough range for the PLL to lock onto any signal from the transmitter. With the capacitor set to 0.01uF, R_{B1} can be solved for. The capacitor value was chosen so that the resistor value would be in the kΩs. The calculation is shown below.

$$16kHz = \frac{1}{2\pi}\sqrt{\frac{2\pi(80kHz)}{R_{B1}(0.01uF)}},\ R_{B1} = 5.1k\Omega$$

The final component needed for the demodulator is R_{S1}, and this resistor is connected from the output pin to ground. The data sheet suggested adding this resistor at the output in order to not load the LPF. This value needed to be less than 1MΩ, so 100kΩ was deemed to be sufficient enough.

The final part of the receiver design is the low-pass filter. As per the design constraints, the cutoff frequency was set to about 3kHz. Filtering the demodulated output provides a clean output signal that is nearly identical to the input. A 0.01uF capacitor was selected so the resistor

value would be sufficiently large. With this value and the cutoff frequency chosen, the remaining unknown can be found. The calculation is shown below.

$$f_{cutoff} = \frac{1}{2\pi CR} \tag{4}$$

$$3000 = \frac{1}{2\pi(1\times10^{-8})R}, R = 5.6k\Omega$$

Also seen in *Figure 11* are decoupling capacitors in the form of two 0.1uF capacitors connected from +9V to ground and -9V to ground. These capacitors filter out high-frequency noise from the power supplies, ensuring that the DC power supplies provide stable DC values.

3. Implementation

Figures 13 and *14* below are the implemented transmitter and receiver designs.

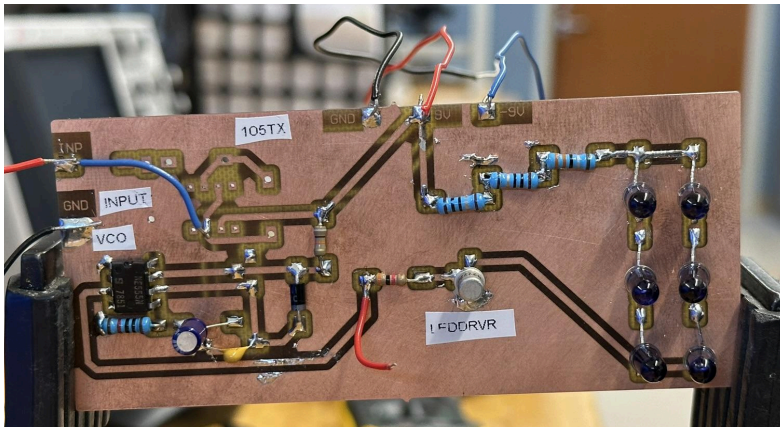

Figure 13 - Implemented Transmitter PCB

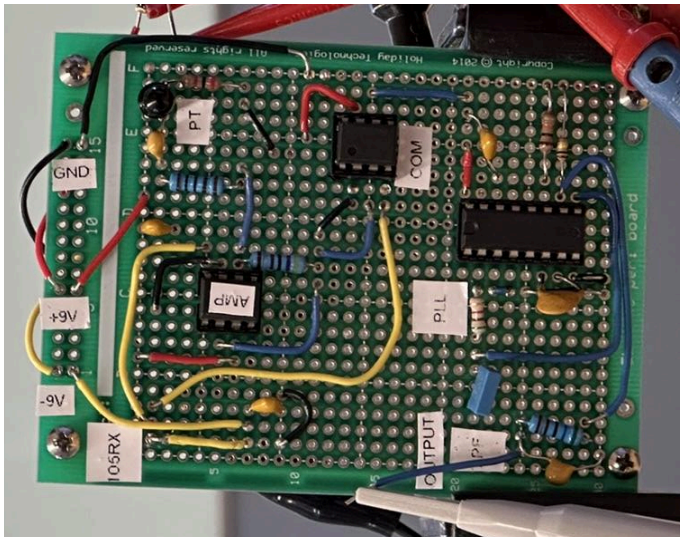

Figure 14 - Implemented Receiver on Vector (perforated) board

3.1 Transmitter

An issue the team had with the LED driver was the wattage of the resistors on the Collector of the transistor driving the LED. Since the nominal current through the LEDs was 100mA, and the LEDs were in a parallel configuration, the resistors R_6, R_7, and R_8 in the transmitter circuit (shown in *Figure 10*) had to be able to handle 200 mA. Originally, these resistors were going to be just (1), but were split up into (3) to accommodate for power ratings. During component procurement, it was noted that resistor power ratings were either ¼ Watts or ½ Watts. If using (1) resistor of ~25Ω, the power through the resistor can be calculated using $P = I^2R$. Plugging in I = 0.2A and R = 25Ω, the power dissipated by the single resistor is 1 Watt, which is far higher than the ½ Watt rating. To accommodate for this, the team decided to split the (1) 25Ω resistor into (3) Resistors of values $R_6 = 10\Omega$, $R_7 = 10\Omega$, $R_8 = 3.3\Omega$. In this scenario, the maximum power dissipated by any single resistor was $P = (0.2)^2(10) = 0.4$ Watts, which is in the acceptable range for a ½ Watt rated resistor.

3.2 Receiver

The PLL was built first using most of the components from the final design. Initially, the components for the low-pass filter portion of the PLL were different; C_2 was 0.1uF and R_{B1} was 510Ω. While testing the PLL, it was determined that R_{B1} was too small. To remedy this, R_{B1} was increased and C_2 was decreased. This allowed the PLL to lock onto a signal much better than before. Also, the size of the capacitor before the input to the PLL was changed several times, but the 0.1uF capacitor proved to be the superior choice.

Once the PLL was built, the detector and pre-amp were built. These two circuits were built as shown in the design. However, some components needed to be exchanged. Originally, two LM741 op-amps were used in the amplifier and comparator. However, the slew rate for this op-amp was not fast enough to keep up with high frequency inputs. Ultimately, the LM741 op-amps were replaced by the faster LM318s. For the phototransistor, the QSD123 was chosen. This worked well with the design since its peak sensitivity wavelength aligned with that of the chosen LEDs. However, the rise and fall time of the transistor are $7\mu s$ each, which implies a total of a minimum of $14\mu s$ for a full rise and fall of the output (excluding the time at which the output remains high to form the desired square wave). In comparison, since the modulated signal has a carrier frequency of 80kHz, it has a period of approximately $12\mu s$, which is less than the required $14\mu s$. As a result, the transistor's output looked like a triangle wave as opposed to a square wave, which led to the need of a comparator to recover the frequency modulated square wave generated by the transmitter.

Once the PLL, pre-amp, and detector were built, they were connected and tested together. During testing, the low-pass filter was added after the PLL. Originally, the LPF was an active LPF. However, the noise from the op-amp was causing the signal to distort. Therefore, instead of an active filter, a simple RC filter was used. This correctly filtered the demodulated signal

without additional distortion. After various tests, the receiver was finalized and soldered to a vector board. The implemented design is shown in *Figure 14*.

3.3 Board design

To increase the signal transmission distance, the team utilized PCBs and vector boards, as it was noted that using breadboards limited the transmission distance. Once prototyping of the transmitter was complete, Arul utilized Altium to design a PCB for fabrication. This PCB was milled by the EECS shop and assembled by Felipe and Arul. The *Figure 15* below shows the PCB:

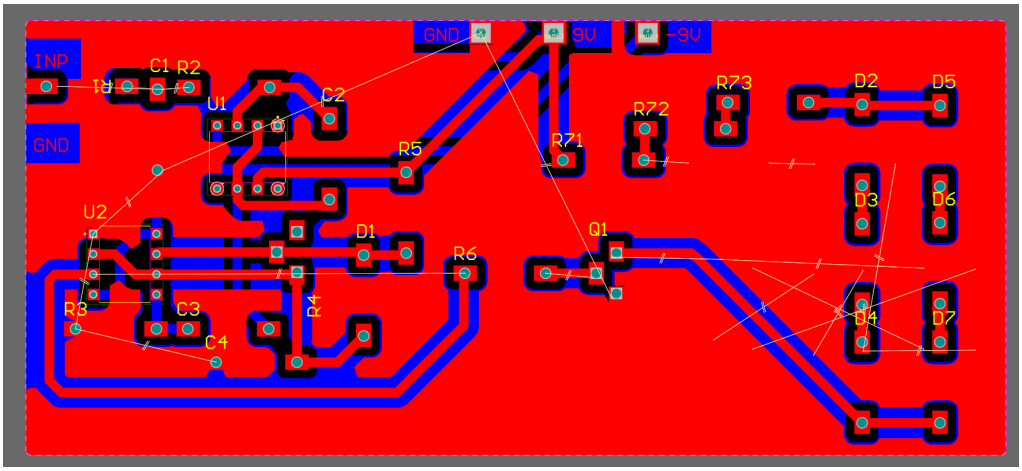

Figure 15 - Transmitter PCB Design (created in Altium, milled from EECS shop)

Upon completion of prototyping the receiver design, the EECS shop's PCB mill was broken, so the team had to compromise and use a Vector (perforated) board instead of a designed PCB for final implementation. The completed board implementations can be referenced in *Figure 13* and *Figure 14* at the beginning of Section 3.0.

4. Laboratory Circuit Evaluation

4.1 Configuration

The equipment used during the testing phase of the system is listed below:

i. Breadboards to assemble circuits.

ii. Agilent 33220A Function Generator (unit number MY44062508).

iii. Agilent E3630A OEM Triple Output DC Power Supply (unit MY40006658).

iv. Keysight InfiniiVision DSOX3024 Digital Storage Oscilloscope (unit MY63080075).

The first step in testing the system was to assemble the transmitter and receiver circuits on breadboards. Then, various tests were run on different components of the system by connecting them to the DC power supply while inputting a wave using the function generator and reading the output with the oscilloscope. The specifics of each of the tests run on the various parts of the system are further explained in section 4.2; however, the equipment setup used for all these tests is presented below in *Figure 16.*

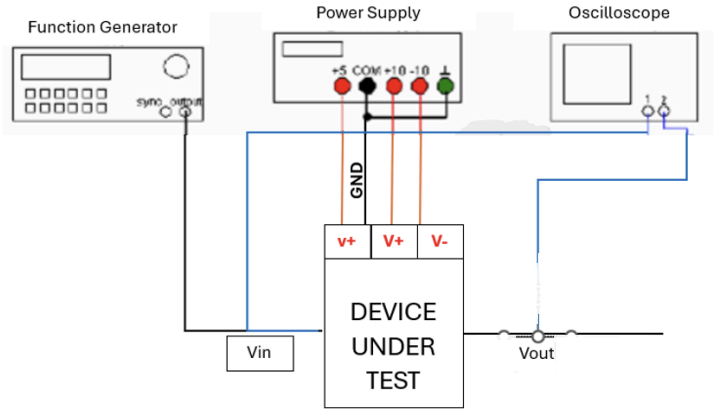

Figure 16 - Circuit testing general setup.

4.2 Procedure

4.2.1 VCO testing

The first step to test the VCO was to ensure that its carrier frequency was 80kHz. This was done by testing the circuit without any input voltage wave. Instead, the NE555P timer was powered by connecting the timer's pins 4 and 8 to the DC power supply set to supply 9V. Then, the output of the VCO was probed using the oscilloscope by connecting it pin 3 of the NE555P timer. Then, the frequency of oscillation of this output was measured.

After confirming that the center frequency of the VCO to 80 kHz, the function generator was connected to pin 5 and set to input a sinusoidal waveform of 500mV peak to peak voltage and 2kHz frequency. Once again, the output was probed at pin 3 and its frequency was measured

at the peaks and troughs of the input wave to ensure that it was varying with the input's amplitude as expected.

4.2.2 PLL testing

To test that the PLL was efficiently demodulating the signal, the output of the VCO was directly connected to the PLL circuit by connecting pin 3 of the NE555P timer to pin 14 of the PLL. Then, the function generator was once again connected to pin 5 of the NE555P timer and set to input a sinusoidal waveform of 500mV peak to peak voltage and 2kHz frequency. This input was also probed using the oscilloscope. Furthermore, the oscilloscope was used to probe the output of the PLL at its pin 10. Then, these two readings were compared to ensure the original input was fully recovered by the PLL after its demodulation.

4.2.3 Optical Testing

To test the optical portion of the circuit, the output of the VCO was connected to the LED driver as shown in *Figure 10* and the voltage across the LEDs were probed by connecting the oscilloscope probe to the leg of one of them. Then, this output was compared with the VCO's output to ensure the LEDs were transmitting the same wave. Afterwards, the LEDs were placed in front of the receiver and the output of the phototransistor was probed using the oscilloscope. Finally, another oscilloscope probe was connected to the output of the comparator. The comparator's output was compared to that of the VCO to ensure that the signal read by the receiver was the same as the signal transmitted by the LEDs.

4.2.4 Full System Test

To test the complete system, the transmitter and receiver boards were placed in front of each other at a distance of 1m. Then, the transmitter's input (TP2 in *Figure 10*) was connected to the function generator with a 2kHx, 500mVpp sinusoidal input and it was probed using the oscilloscope. Similarly, the oscilloscope probe was connected to TP1 in *Figure 11*; i.e., the output of the receiver. These two waveforms were compared to ensure the transmission occurred as expected. Then, the two circuits were moved further apart from each other to find the maximum transmission range at which the signal in the receiver had little to no distortion. When doing this, the maximum transmission distance was found to be 3.4m.

5. Evaluation of Test Data

5.1 Data

The results obtained for the tests ran are presented below. *Figure 17* presentes the output of the VCO where there is no input signal imputed; i.e., when the control voltage is zero. As seen in the image the frequency of oscillation is approximately $80kHz$.

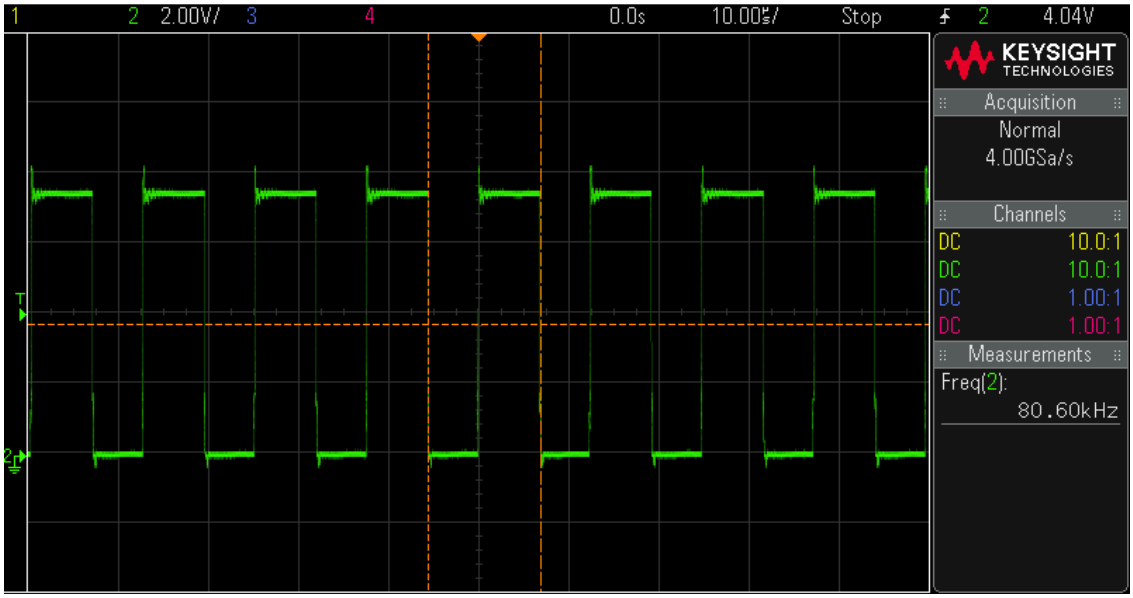

Figure 17 - VCO output when controlled voltage is equal to zero

Furthermore, the results for the tests run on the optical portion of the system are presented in *Figure 18* below. The yellow waveform corresponds to the output of the LED driver, the output of the phototransistor receiver circuit is presented in green, and the output of the receiver's comparator is presented in blue.

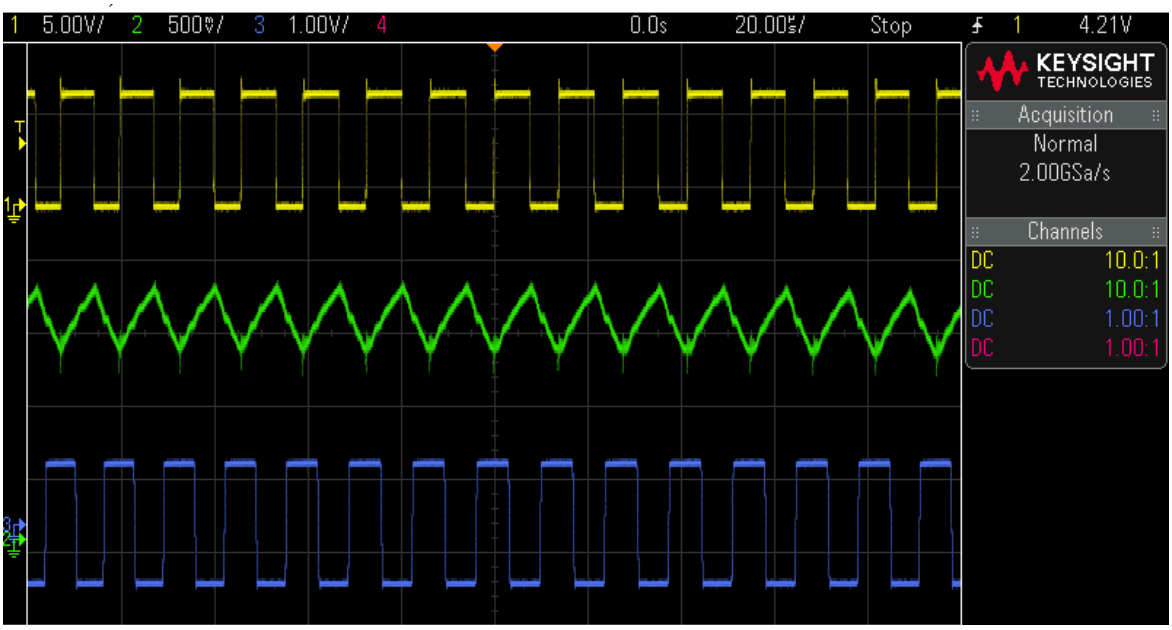

Figure 18 - Behavior of system's optical components

Finally, attached in *Figure 19* below is the result of the test run on the complete system (with the transmitter and receiver placed at a distance of approximately $1.5m$ away from each other). The yellow waveform in the image corresponds to the system's input, which was produced using the function generator. Additionally, the green waveform corresponds to the output of the LED driver, which corresponds to the modulated input signal. Finally, the blue waveform is the output of the last low-pass filter in the receiver. This corresponds to the signal obtained after the demodulation was performed by the PLL.

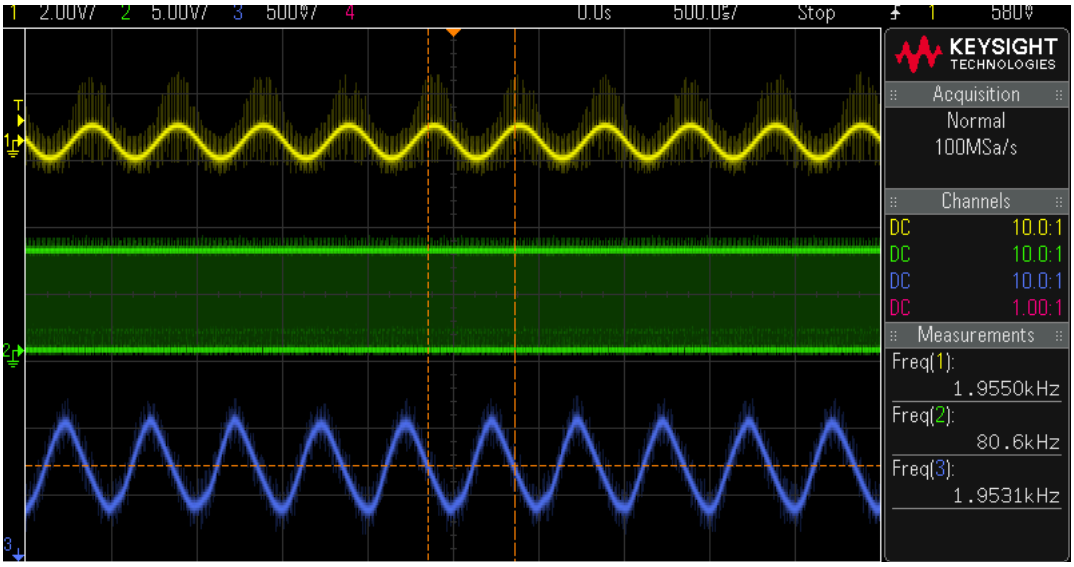

Figure 19 - Results obtained for test on complete system

5.2 Interpretation

Overall, the system behaved as expected. As seen in *Figure 17*, wherever the control voltage of the VCO is zero, the system oscillates at approximately $80kHZ$, which is the desired carrier frequency. This implies that once a sinusoidal wave is inputted into the system and the control voltage rises or falls above or below zero, the frequency of the VCO's output will increase and decrease while maintaining an average frequency of $80kHZ$; the desired carrier frequency.

This behavior can also be observed in *Figure 19*. Once a sinusoidal wave was inputted into the system, the VCO modulated this signal at with a carrier frequency of approximately $80kHZ$. Therefore, although the frequency of the VCO's output in *Figure 19* (green wave) varied with respect to the input's amplitude, whenever the oscilloscope was zoomed out, it read the average frequency of the wave; i.e., the carrier frequency. If the image on the oscilloscope was zoomed in into a peak of the input's waveform, the frequency of the VCO's output read approximately $65kHZ$. On the other hand, whenever the image was zoomed in into peak of the input's waveform, the frequency of the VCO's output was about $96kHZ$. Therefore, the VCO modulated the signal at a carrier frequency of $80kHZ$ and a bandwidth of $\pm$ 20%, as desired.

Finally, *Figure 18* shows the behavior of the optical portion of the system. As seen, in the yellow waveform, the output of the LED driver was the same as that of the VCO, thus, the LEDs were transmitting the desired signal. Furthermore, as seen in the green waveform, the output of the phototransistor receiver circuit was a triangle wave as opposed to the square wave transmitted by the LEDs. This is due to the issues related to the rise and fall time of the phototransistor in comparison to the period of the modulated wave (as discussed in section 3.2). Therefore, the phototransistor's output was inputted into a comparator circuit that converted it back into the original square wave. When comparing the transmitted modulated signal (yellow) to the output of the comparator (blue), it can be concluded that the comparator fully recovered the modulated signal since the waveforms have the same frequency and the only difference is a slight delay (phase shift) that will not impact the demodulation process.

5.3 Conclusions

In conclusion, the system behaved as desired. It was able to transmit a signal to a distance up to $3.4m$. Furthermore, the Frequency Modulation of the input was achieved with the desired carrier frequency and bandwidth since the frequency of the modulated signal varied in an interval of approximately $80kHz \pm 20\%$. This ensured that the PLL locked properly since it was also designed to demodulate signals with a carrier frequency of $80kHz$. However, it is important to note that this behavior of the VCO was observed only for inputs with a peak to peak voltage of $500mVpp$. If this voltage is exceeded, the bandwidth of the frequency modulated signal will increase, which can prevent the PLL from locking and properly demodulating the signal. Therefore, a possible improvement would be to add a resistor network prior to the VCO in order to bias the input and increase the system's operating range.

Another limitation observed was the maximum distance achieved for a clean transmission. As mentioned previously, the maximum distance between the transmitter and receiver that yielded an output without significant distortion or noise was $3.4m$. In order to increase this distance, the resistors in the LED driver could be swapped with resistors of higher wattage. This would allow higher current to flow through them and thus result in brighter LEDs that can transmit further. Another possible improvement would be to incorporate a system that helps the user align the receiver and transmitter properly. As th, which can result in higher noise and distortion in the transmitted signal due to misalignment of the system and not limitation in its transmission range.

6. References

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