

**PODER EXECUTIVO**

**MINISTÉRIO DA EDUCAÇÃO**

**UNIVERSIDADE FEDERAL DE RORAIMA**

**DEPARTAMENTO DE CIÊNCIA DA COMPUTAÇÃO**

**ARQUITETURA E ORGANIZAÇÃO DE COMPUTADORES**

RELATORIO: LABORÁTORIO DE VHDL – CODIFICAÇÃO E SIMULAÇÕES

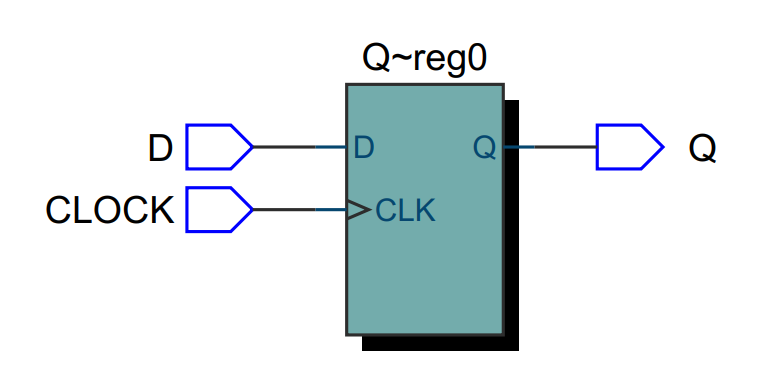
PROFESSOR: **HERBERT OLIVEIRA ROCHA**

ALUNO: PHILIP MAHAMA AKPANYI

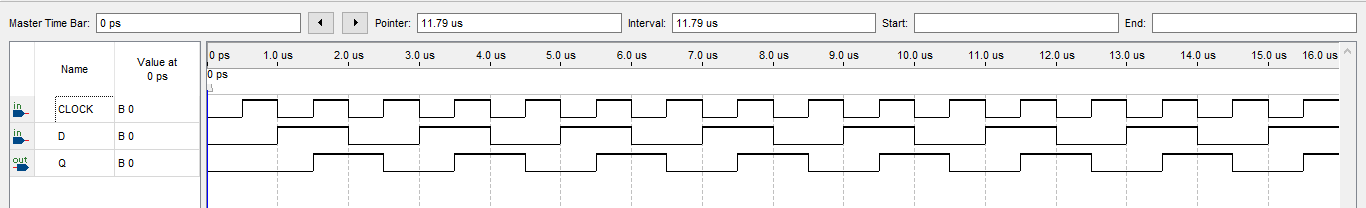
IDE: QUARTUS PRIME VERSION 17.0.0 BUILD 595 04/25/2017 SJ LITE EDITION

COMPONENTES

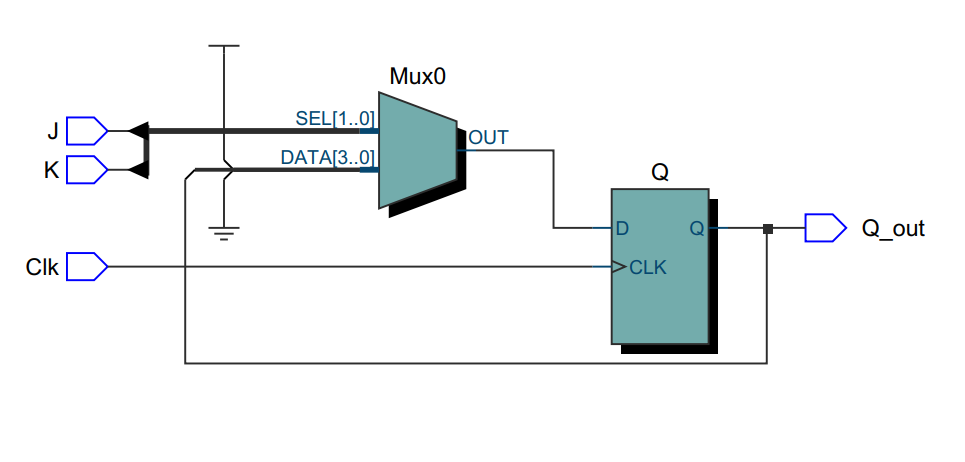
**[COMPONENTE 01].** Registrador Flip-Flop do tipo D e do tipo JK.



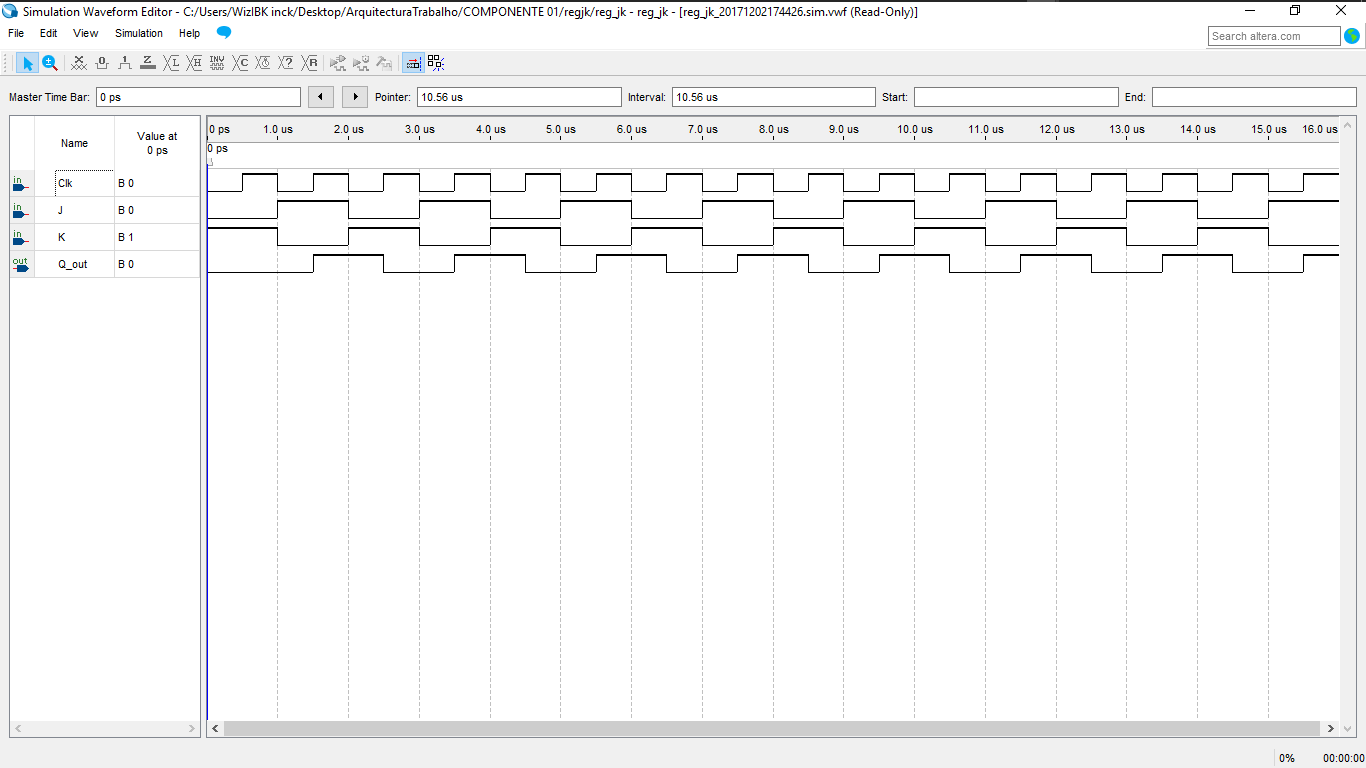
**[Figura 1.0] Imagem do RTL viewer do registrador Flip-Flop do tipo D**



**[Figura 1.1] Imagem do waveform do registrador Flip-Flop do tipo D**

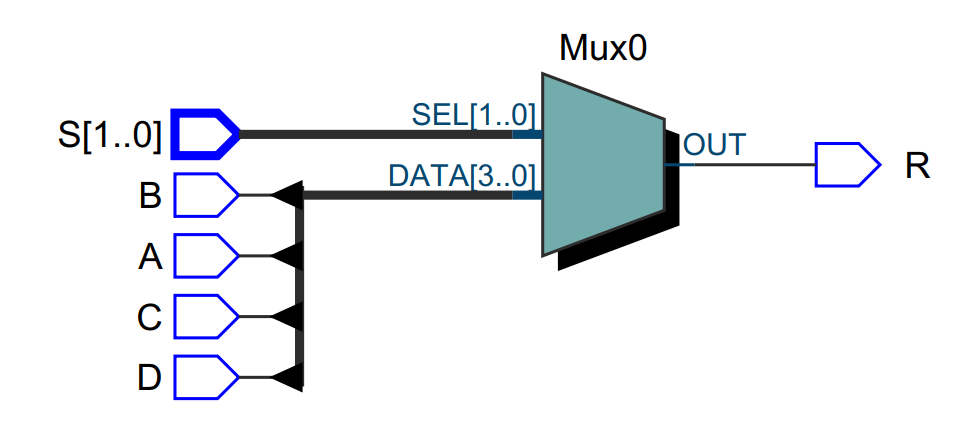


**[Figura 2.0] Imagem do RTL viewer do registrador Flip-Flop do tipo JK**

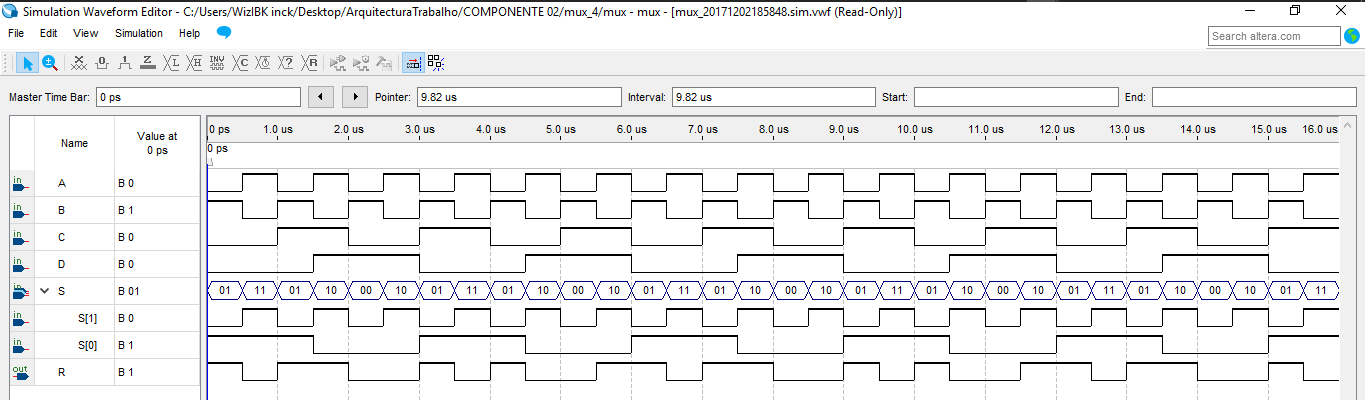


**[Figura 2.1] Imagem do waveform do registrador Flip-Flop do tipo JK**

**[COMPONENTE 02].** Multiplexador de quatro opções de entrada.

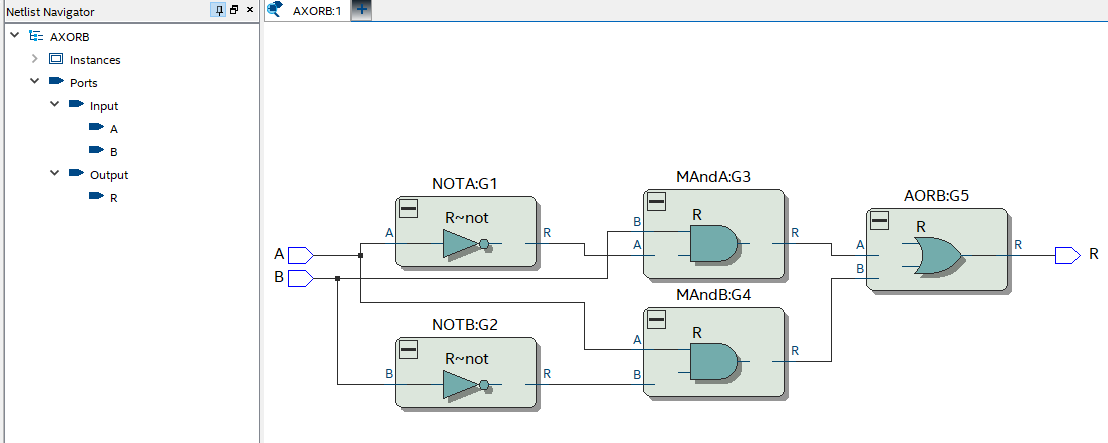


**[Figura 3.0] Imagem do RTL viewer do Multiplexador de 4 opções de entrada**

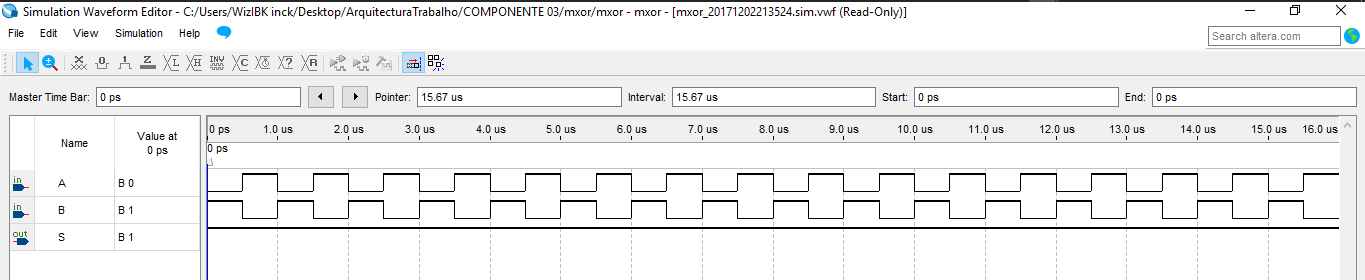


**[Figura 3.1] Imagem do waveform do Multiplexador de 4 opções de entrada**

**[COMPONENTE 03].** Porta lógica XOR usando port map com os componentes: AND, NOT, e OR.

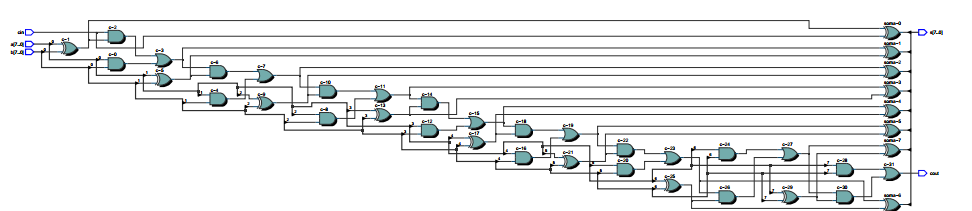


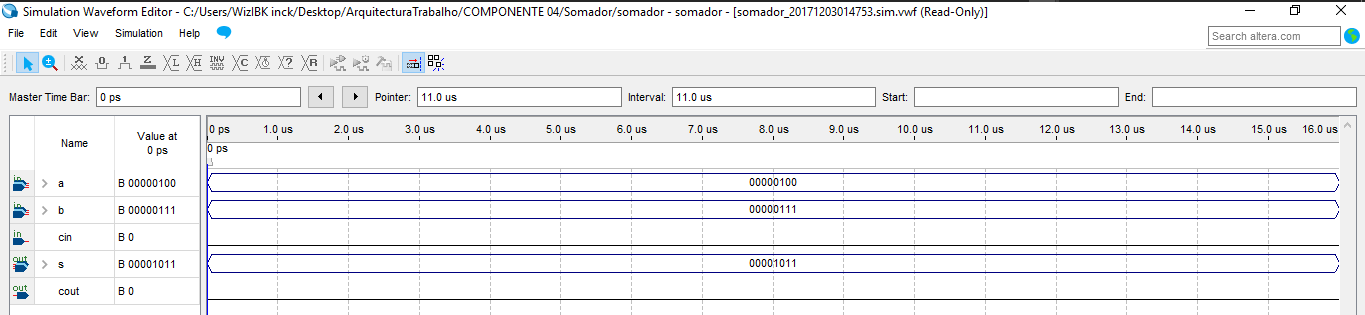
**[Figura 4.0] Imagem do RTL viewer da porta lógica XOR**



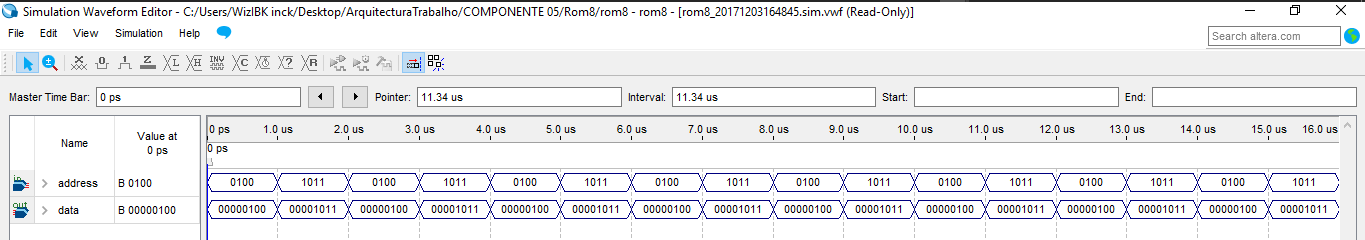
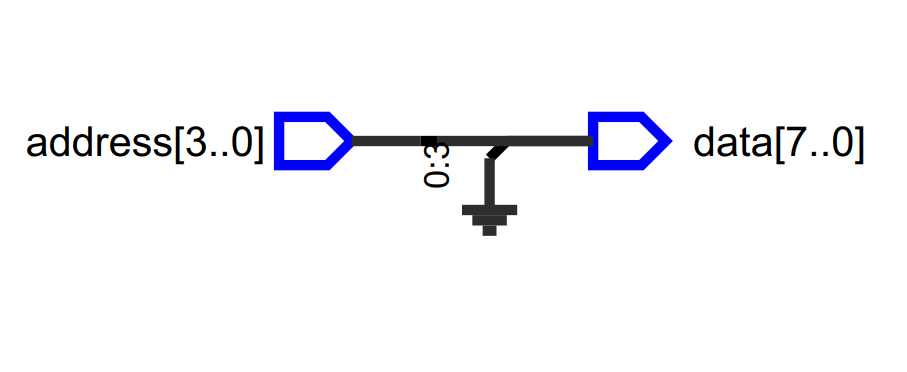
**[Figura 4.1] Imagem do waveform da porta lógica XOR**

**[COMPONENTE 04].** Somador que recebe um valor inteiro e soma com o valor 4.

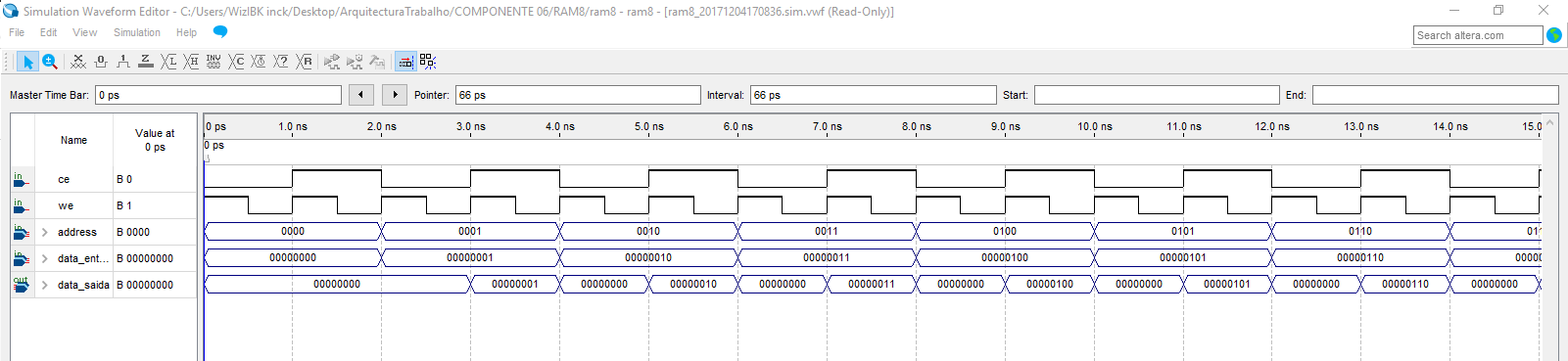
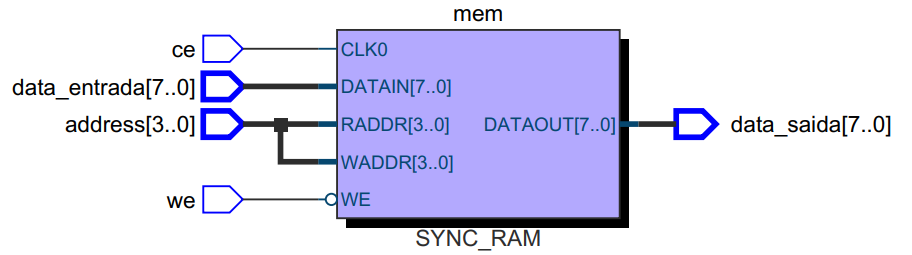




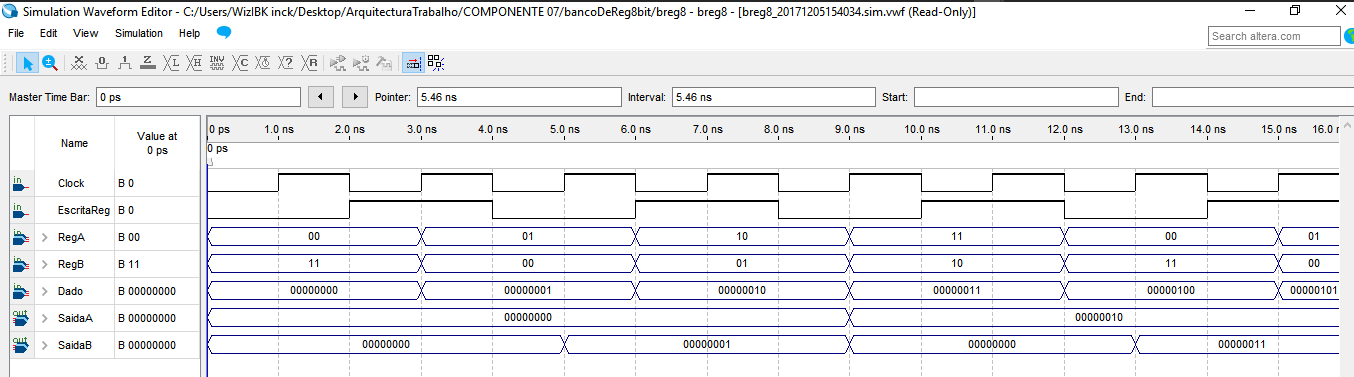
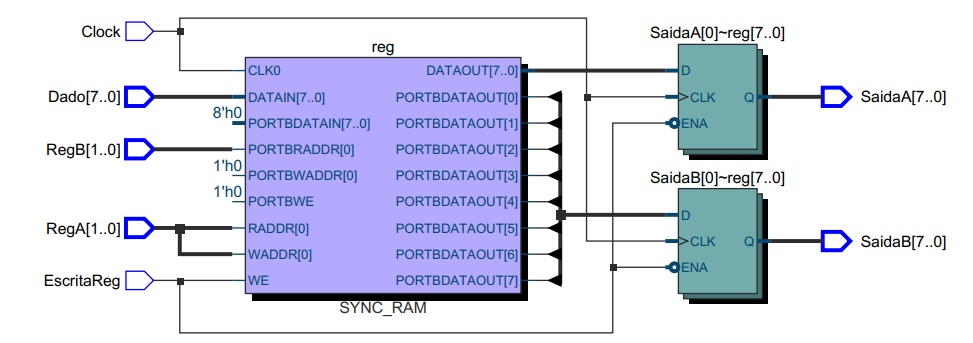
**[COMPONENTE 05].** Memória ROM de 8 bits.



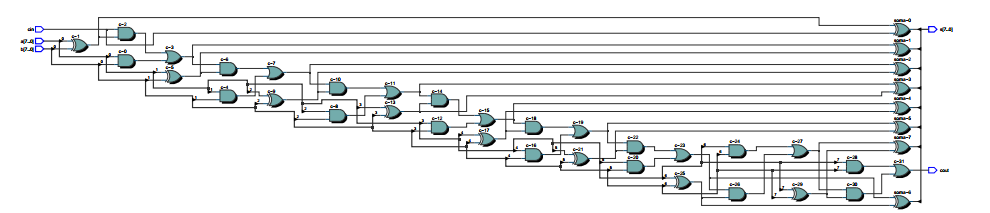
**[COMPONENTE 06].** Memória RAM de 8 bits.

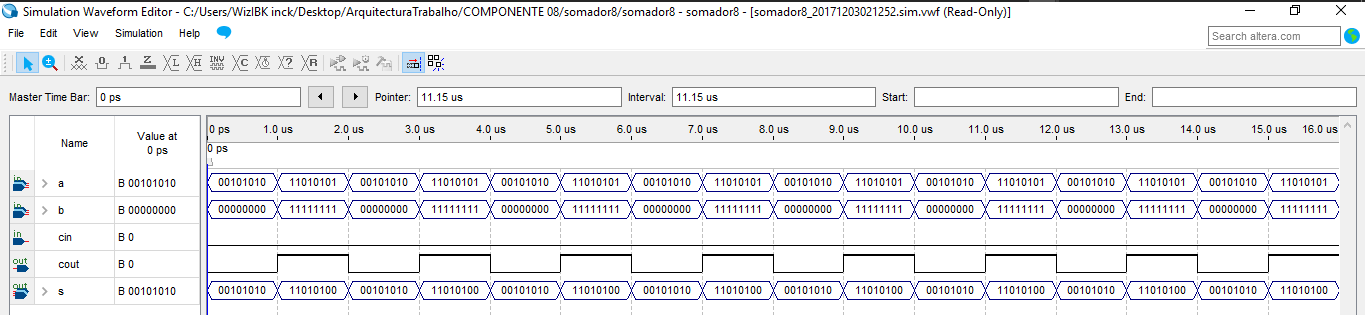


**[COMPONENTE 07].** Banco de Registradores de 8 bits.

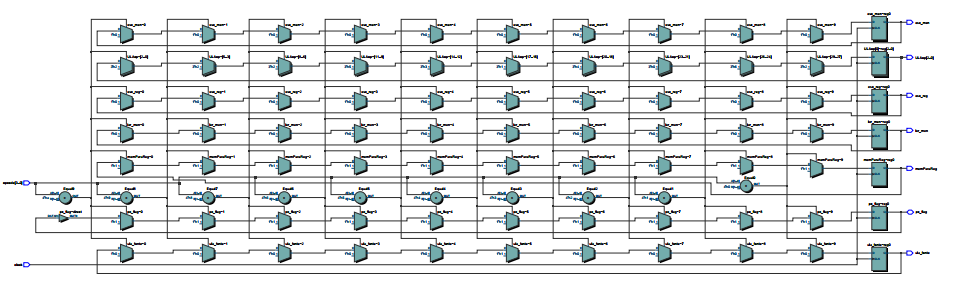


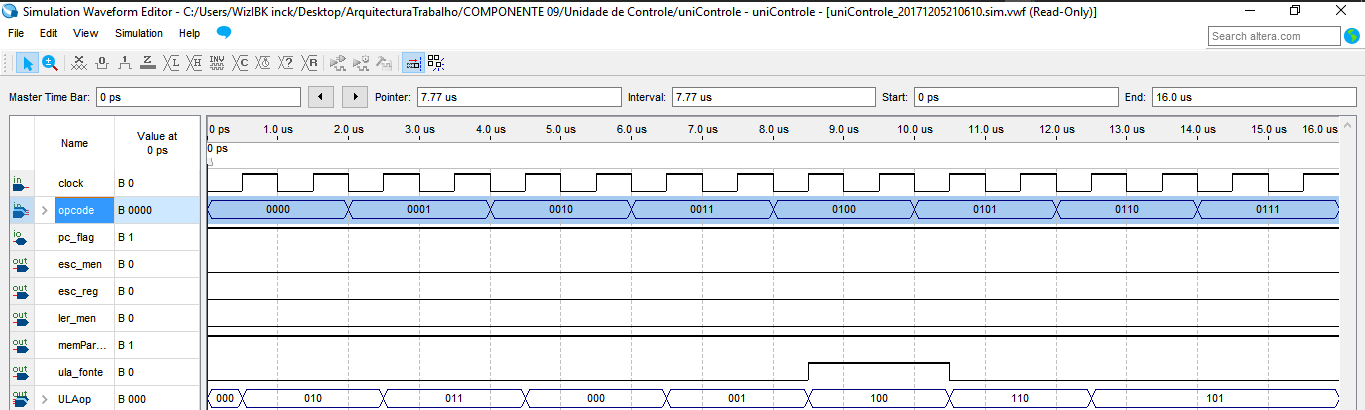
**[COMPONENTE 08].** Somador de 8 bits.

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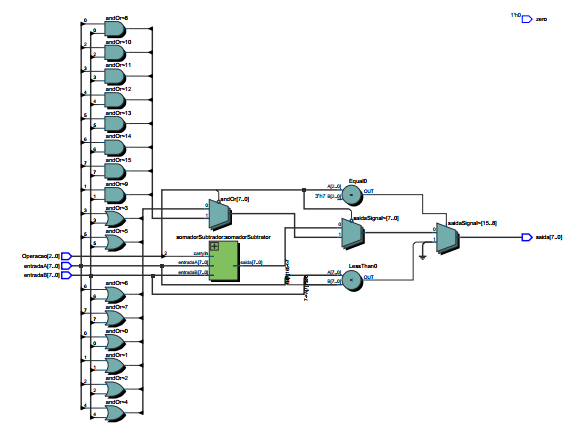


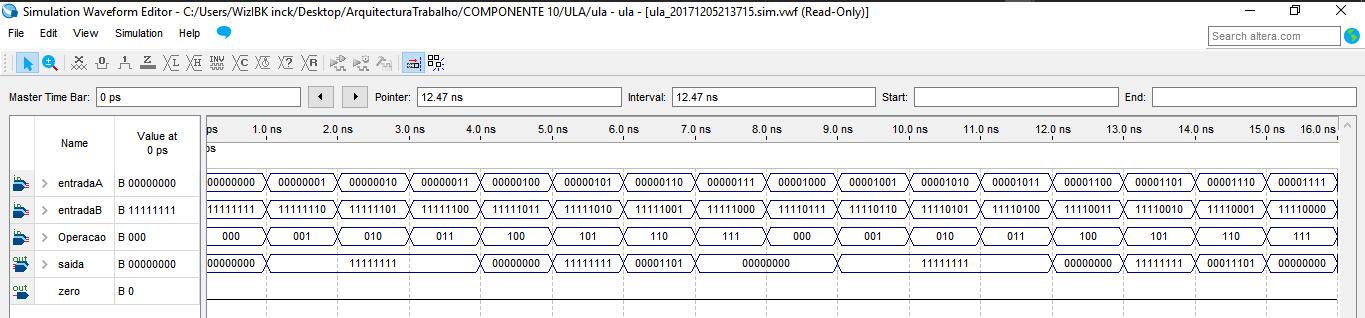
**[COMPONENTE 09].** Unidade de controle uniciclo do MIPS de 8 bits.



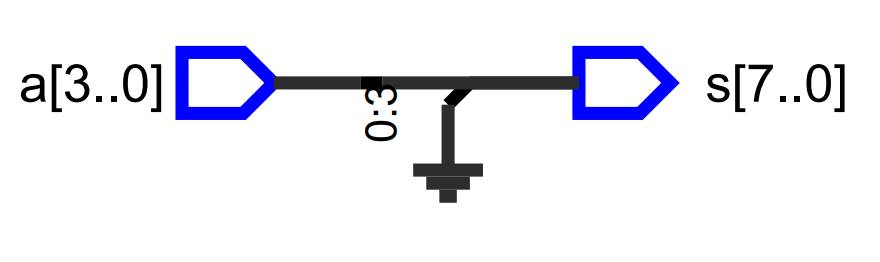


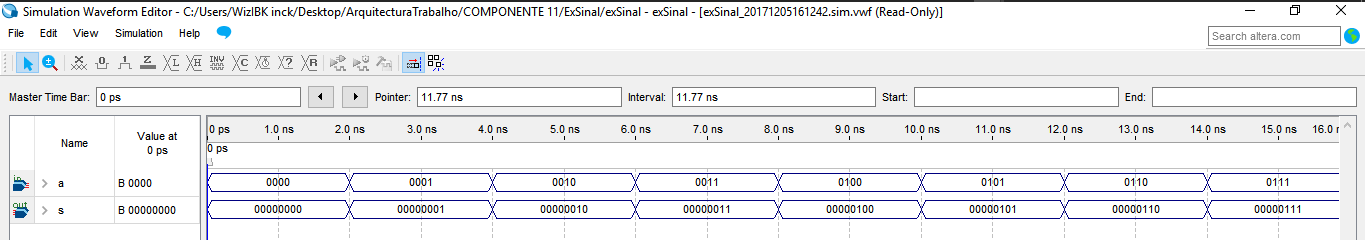
**[COMPONENTE 10].** ULA de 8 bits, utilizando port map, com as seguintes operações: AND, OR,  
NOT, NOR, NAND, XOR, SHIFT de 2 bits à esquerda, SHIFT de bits à direita,  
soma e subtração.



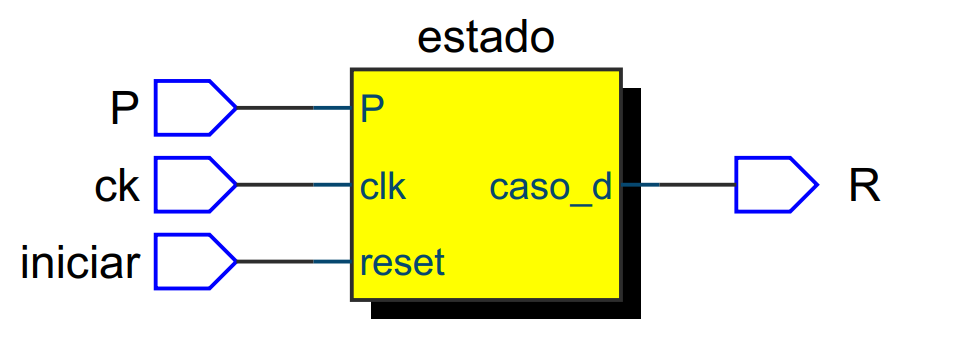


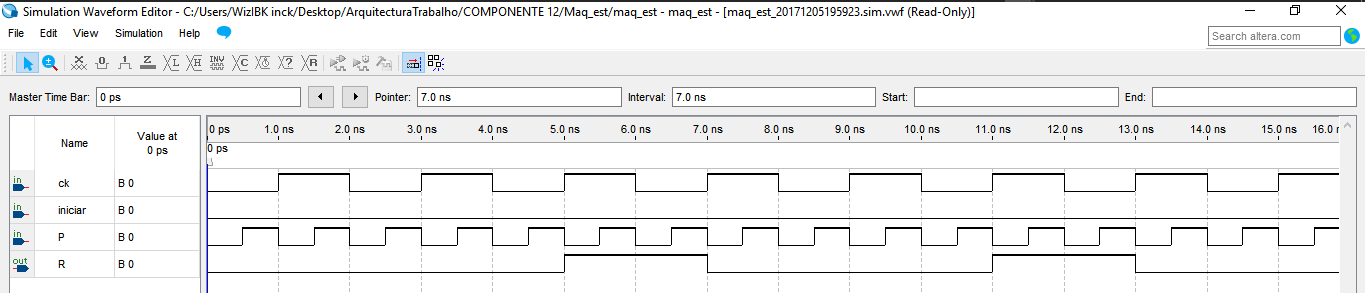
**[COMPONENTE 11].** Extensor de sinal de 4 bits para 8 bits.





**[COMPONENTE 12].** Implemente a maquina de estados ao lado.





**[COMPONENTE 13].** Contador Síncrono.

