JEDEC STANDARD

Serial Flash Discoverable Parameters (SFDP)

JESD216H

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JEDEC SOLID STATE TECHNOLOGY ASSOCIATION

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Foreword

This standard was prepared by the JEDEC SFDP Task Group authorized by the JC-42.4 Committee Chairman.

The intended audience is serial flash vendors and engineers writing device drivers for SFDP compliant serial flash devices.

The participating SFDP TG members included volunteers from Adesto, Infineon, Giga Device, Intel, ISSI, Macronix, Micron, Microchip, NXP, Sanyo, and Winbond.

Introduction

The Serial Flash Discoverable Parameter (SFDP) standard provides a consistent method of describing the functional and feature capabilities of serial flash devices in a standard set of internal parameter tables. These parameter tables can be interrogated by host system software to enable adjustments needed to accommodate divergent features from multiple vendors.

The SFDP standard defines a common parameter table describing important device characteristics and serial access methods used to read the parameter table data. Optional Special Function parameter tables for erase sector address map and 4-byte address instructions are included. In the JESD216D revision are optional Special Function parameter tables for the JEDEC x4 (Quad) eXtended Serial Peripheral Interface (x4 xSPI). New in the JESD216E revision is a description of the Replay Protected Monotonic Counter (RPMC) functionality and also descriptions of the Secure Read and Secure Write packet transfer transactions. Additional parameter headers and tables can be specified by future revisions of this standard or by flash vendors and are optional.

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SERIAL FLASH DISCOVERABLE PARAMETERS (SFDP) STANDARD

(From JEDEC Board Ballot JCB-25-48, formulated under the cognizance of the JC-42.4 subcommittee on Non-volatile Memory, item 1775.81B).

1 Scope

The SFDP standard defines the structure of the SFDP database within the memory device and methods used to read its data.

The JEDEC-defined header with Parameter ID FF00h and the related Basic Parameter Table is mandatory. This header and table provide basic information for a Serial Peripheral Interface (SPI) protocol memory. Additional headers and tables are optional.

The read command protocol using various I/O modes and standard clock rate are specified. The device electrical parameters are not specified.

NOTE: The SFDP is aligned with the factory default settings and does not change in case user overrides the reset default values or modifies non-volatile configuration registers (NVR).

2 Normative Reference

The following normative documents contain provisions that, through reference in this text, constitute provisions of this standard. For dated references, subsequent amendments to, or revisions of, any of these publications do not apply. However, parties to agreements based on this standard are encouraged to investigate the possibility of applying the most recent editions of the normative documents listed. For undated references, the latest edition of the normative document referred to applies.

1. JEP106, *Standard Manufacturers Identification Code* (see www.jedec.org for latest revision)

2. NIST SP800-147, *BIOS Protection Guidelines* (http://nvlpubs.nist.gov/nistpubs/Legacy/SP/nistspecialpublication800-147.pdf)

3. JEDEC Standard JESD251, *eXpanded Serial Peripheral Interface (xSPI) for Non-volatile Memory Devices* as approved by JC42.4 committee in the June 2017 meeting.

   JEDEC Standard JESDxxx, *SPI Protocol Reset (Serial Peripheral Interface - Flash Hardware Reset Method, Not Requiring a Dedicated Reset Signal Input,* **This document is in development.**

4. JEDEC Standard JESD230C, *NAND Flash Interface Interoperability*

3 Terms and Definitions

For the purposes of this standard, the following terms and definitions apply.

00b: The ‘b’ suffix indicates the ‘00’ digits are a binary representation of the number.

00h: The ‘h’ suffix indicates the ‘00’ digits are a hexadecimal representation of the number.

address: The three or four byte value following some instructions that is used to select a location within an address space of the flash memory.

basic parameter table: The table pointed to by Parameter ID FF00h. Contains general information about the flash device's capabilities.

block: A group of contiguous sectors.

command: The combination of the instruction, address, optional mode bits, wait states, and data cycles used to initiate functions or transfer information between the controller and the serial flash.

controller: The serial bus initiator

Double Transfer Rate (DTR): Instruction, address, and/or data may be input or output on both the rising and falling edges of the clock. NOTE: The term “Double Data Rate” (DDR) may also be encountered in some documentation.

Data Strobe (DS): Target to initiator strobe signal used to capture data sent by the target.

dummy cycles: Clock cycles during which no data is transferred to or from a memory.

DWORD: Four consecutive 8-bit bytes used as the basic 32-bit building block for headers and parameter tables.

instruction: The one byte code used to initiate a function in the serial flash or identify the type of information transfer between the controller and the serial flash.

mode bits: Optional control bits that follow the address bits. These bits are driven by the controller if they are specified.

wait states: Required clock cycles between the address bits or optional mode bits and the start of data when reading from the flash device. Some device data sheets describe these as dummy cycles because no information is transferred between the controller and memory during these cycles. Neither controller nor memory are required to drive the data lines during these cycles.

read latency: On flash read instructions, the total number of clocks between end of address and the start of data. The sum of clocks for mode bits and clocks for wait states equals the Read Latency.

sector: The minimum granularity - size and alignment - of an area that can be erased in the data array of a flash memory device. Different areas within the address range of the data array may have a different minimum erase granularity (sector size).

3 Terms and Definitions (cont'd)

(x-y-z): Command mode nomenclature used in JESD216A and JESD216B to indicate the number of active pins used for the instruction (x), address (y), and data (z). For new entries in the current standard, this is replaced by the (An-Bn-Cn) nomenclature described below. The (x-y-z) nomenclature is equivalent to (AS-BS-CS) unless otherwise noted. (4-4-4) is therefore equivalent to (4S-4S-4S).

(An-Bn-Cn): Command mode nomenclature used to indicate the number of active pins used for the instruction (A), address (B), and data (C), and the data rate used for each. Data rates(n) can be single (S) and dual (D). At the present time, the only valid Read SFDP command modes are: (1S-1S-1S), (2S-2S-2S), (4S-4S-4S), (4S-4D-4D), and (8D-8D-8D). (4S-4D-4D), and (8D-8D-8D) modes also use a Data Strobe (DS) as part of the communication protocol.

4 Read SFDP Command Protocol

4.1 Instruction

The Read SFDP instruction code is 5Ah.

- The very first SFDP instruction a Device receives from a Host is the READ SFDP (5Ah) instruction during POR discovery phase.

The Fetch SFDP instruction code is 5Bh.

- This instruction is added to support Long Latency NVM Devices. This instruction tells a Device to load all parameter tables, defined in SFDP Header Structure, from device Memory Cell Array to Device Cache Buffer. NAND Flash device is the first Long Latency NVM device supported by SFDP. Host shall wait for 120 µs tR (Read Latency) then Host can re-issue Read SFDP (5Ah) instruction to access SFDP parameter table and Long Latency NVM device MSPT (Media Specific Parameter Table) table.
- Fetch SFDP (5Bh) instruction shall follow the same mode established between a Host and a Device during POR Read SFDP (5Ah) instruction phase.

  NOTE Fetch SFDP instruction is only applicable for POR device discovery process for now. If needed, additional details of normal connected operation description would be available after JEDEC SPI NAND document is available.

4.2 Address

Indicates the starting byte address in the SFDP area and is always expressed as a three byte field for (1S-1S-1S), (2S-2S-2S), (4S-4S-4S), and (4S-4D-4D) modes. For the (8D-8D-8D) mode, 3 or 4 byte addressing may be used.

- Fetch SFDP (5Bh) instruction does not have or require an address field.

4.3 Wait States

Following the address, eight clocks are required before valid data is clocked out for (1S-1S-1S), (2S-2S-2S), (4S-4S-4S), and (4S-4D-4D) modes. For the (8D-8D-8D) mode, a variable number of wait states (dummy cycles) may be used.

- Not applicable for Fetch SFDP (5Bh) instruction since it does not have an address field and does not output data.

4.4 Clock Rate

SFDP compliant devices must support 50 MHz operation for the Read SFDP command (instruction 5Ah). Devices may support a wider frequency range, but a controller can always run SFDP cycles at 50 MHz or less and get valid results.

- Fetch SFDP (5Bh) instruction shall follow the same mode established between a Host and a Device during Read SFDP (5Ah) instruction phase.

4.5 Command Modes

The Read SFDP command can be used with device supported modes of (1S-1S-1S), (2S-2S-2S), (4S-4S-4S), or (4S-4D-4D), but the instruction (5Ah), address (24 bits), eight wait states, and 50 MHz requirements remain the same. For the (8D-8D-8D) mode, the instruction (5Ah) and 50 MHz requirements remain the same, while 24 or 32 address bits, and a variable number of wait states (dummy cycles) may be used. Support for SFDP does not imply or require that the target device supports 2S-2S-2S, 4S-4S-4S, 8S-8S-8S or 8D-8D-8D mode. If the controller knows a priori the mode in which the flash device is configured, then it can issue the Read SFDP command in that mode. If the controller does not know, then a suggested algorithm is to try to read the SFDP signature (see 6.1) in 4S-4S-4S mode, if that fails try 2S-2S-2 Smode, and if that fails try 1S-1S-1S mode. For Octal devices, these typically support SFDP read operation in both 1S-1S-1S mode and 8D-8D-8D mode. If the host controller does not know exactly which protocol mode is used for SFDP in 8D-8D-8D mode, this information can be found by reading SFDP in 1S-1S-1S mode first. (To read an unknown device directly in 8D-8D-8D mode, the host controller may read from address 0, and count the number of dummy clocks required before the SFDP signature is received.)

- Fetch SFDP (5Bh) instruction shall follow the same mode established between a Host and a Device during Read SFDP (5Ah) instruction phase.

4.5 Command Modes (cont'd)

Timing Diagram Signal Definitions:

- CS# = Select, low active. Memory device selection signal also often referred to as Chip Select or Chip Enable
- CK = Clock. Serial clock to the memory also often referred to as SCLK.
- IO0 = Data input or output zero. The least significant memory data input or output also often referred to as DQ0 or Serial Input (SI) when not used for two, four or eight bit data I/O.
- IO1 = Data input or output one. The next most significant memory data input or output above IO0, also often referred to as DQ1 or Serial Output (SO) when not used for two, four or eight bit data I/O.
- IO2 = Data input or output two. The next most significant memory data input or output above IO1, also often referred to as DQ2 or Write Protect, low active (WP#) when not used for four or eight bit data I/O.
- IO3 = Data input or output three. The most significant memory data input or output, also often referred to as DQ3 or Hold, low active (HOLD#) when not used for four or eight bit data I/O.
- IO4-7 = Data input or output four to seven. Used for eight bit data I/O (8D-8D-8D). Also often referred to as DQ4-7.
- DS = Data Strobe. Used for (4S-4D-4D) and (8D-8D-8D). The Data Strobe (DS) signal provides a timing reference for information transfer on the IO signals from the target to the initiator. DS is an output signal from the xSPI target device that is aligned with the edges of output data and is used by the host interface to optimize high frequency read data capture. DS may optionally be used as a signal from the target to the initiator, to indicate the duration of initial access latency or, as a signal from the initiator to the target, to indicate write data masking.

4.5.1 Read SFDP (1S-1S-1S) Mode

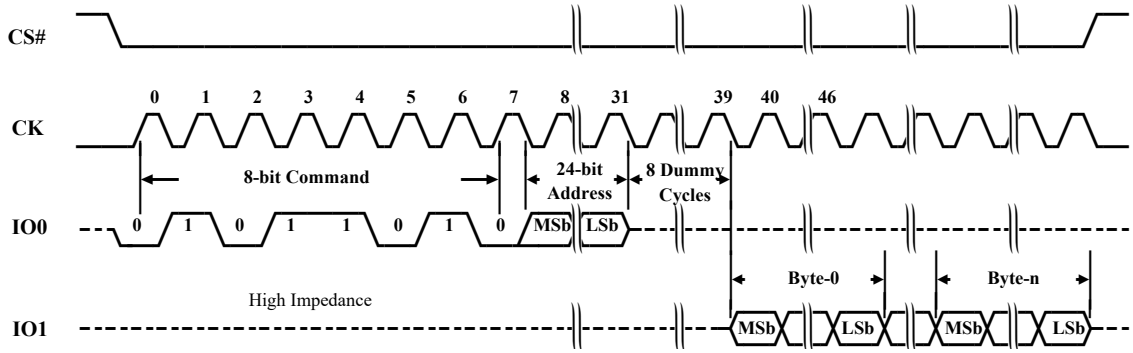


Figure 1 — Read SFDP (1S-1S-1S) Mode Timing Diagram

4.5.2 Read SFDP (2S-2S-2S) Mode

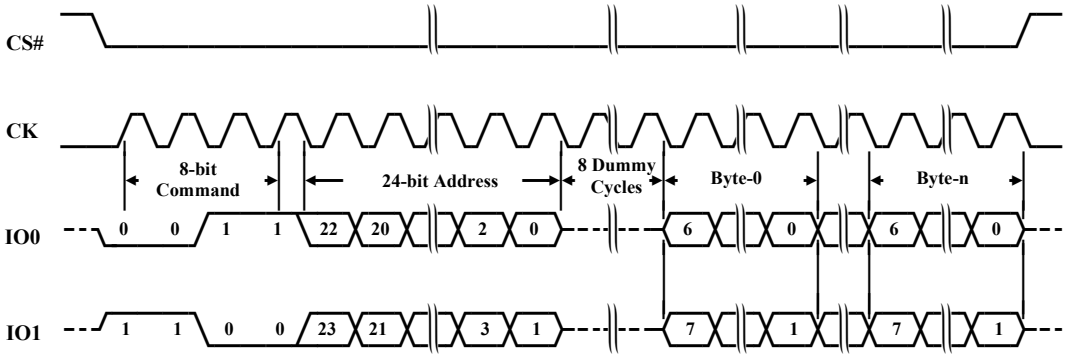


Figure 2 — Read SFDP (2S-2S-2S) Mode Timing Diagram

4.5.3 Read SFDP (4S-4S-4S) Mode

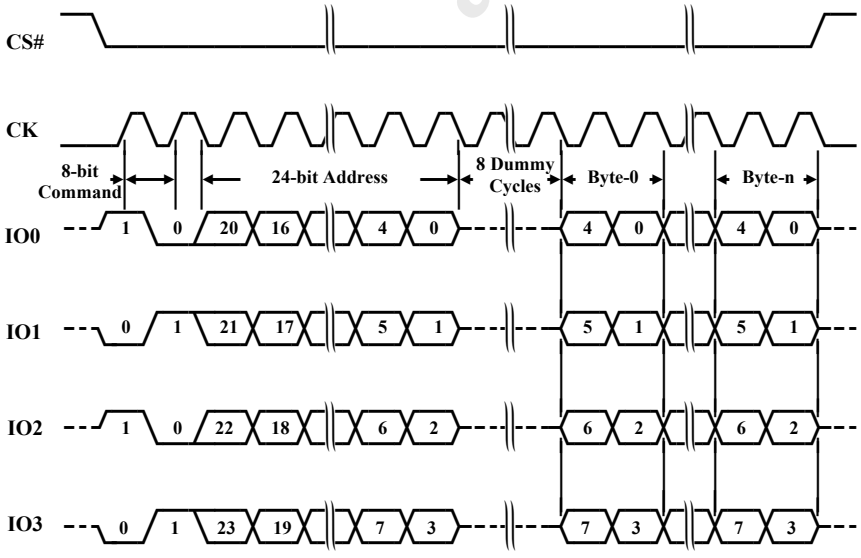
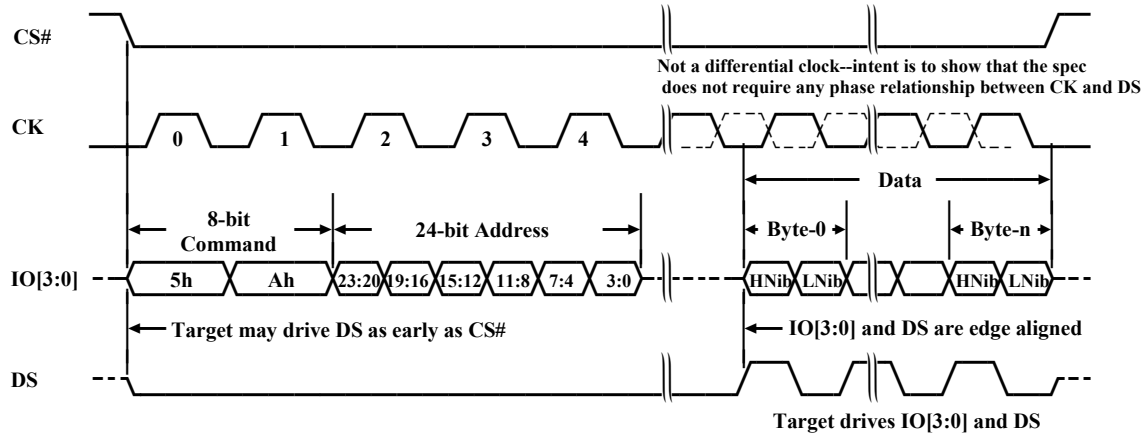


Figure 3 — Read SFDP (4S-4S-4S) Mode Timing Diagram

4.5.4 Read SFDP (4S-4D-4D) Mode



NOTE DS is optional in this mode.

Figure 4 — Read SFDP (4S-4D-4D) Mode Timing Diagram

4.5.5 Read SFDP (8D-8D-8D) Mode

See 6.4.21 for details about the addressing options in this mode.

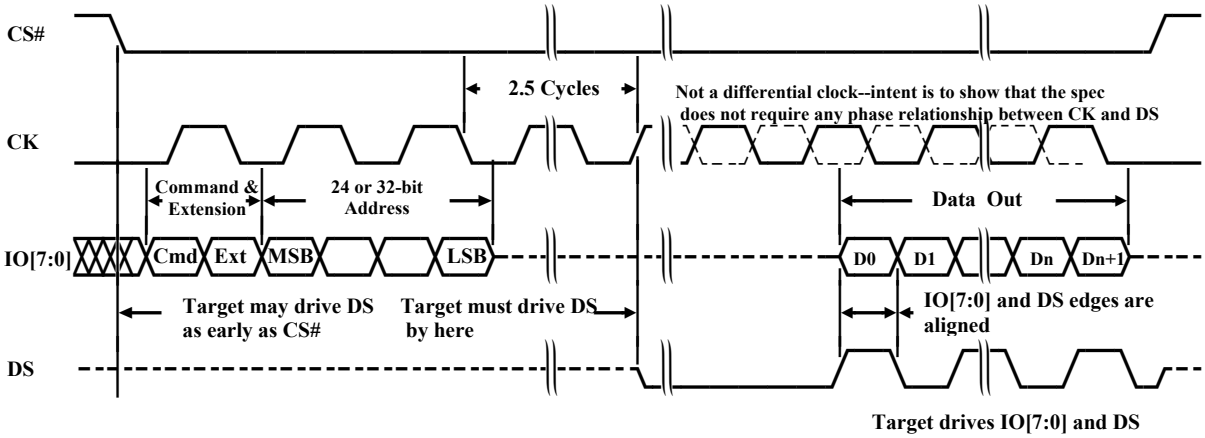


Figure 5 — Read SFDP (8D-8D-8D) Mode Timing Diagram

4.5.6 Fetch SFDP (1S-1S-1S) Mode

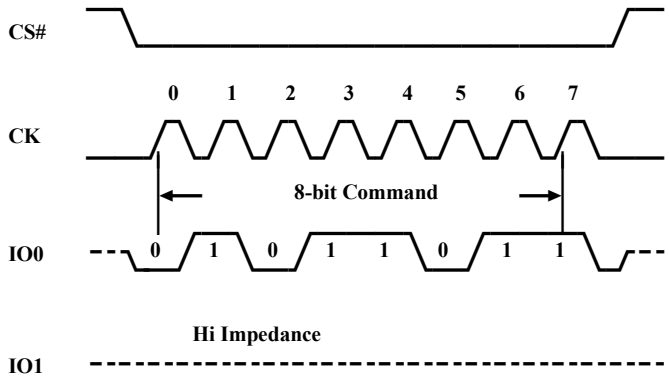


Figure 6 — Fetch SFDP (1S-1S-1S) Mode Timing Diagram

4.5.7 Fetch SFDP (2S-2S-2S) Mode

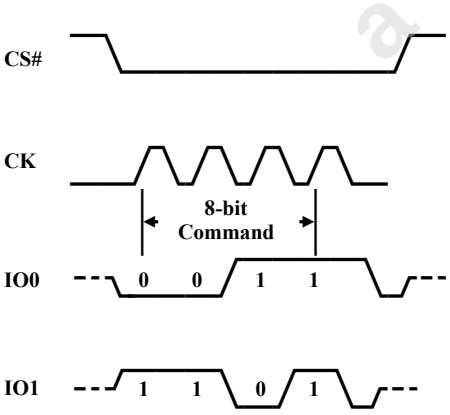


Figure 7 — Fetch SFDP (2S-2S-2S) Mode Timing Diagram

4.5.8 Fetch SFDP (4S-4S-4S and 4S-4D-4D) Mode

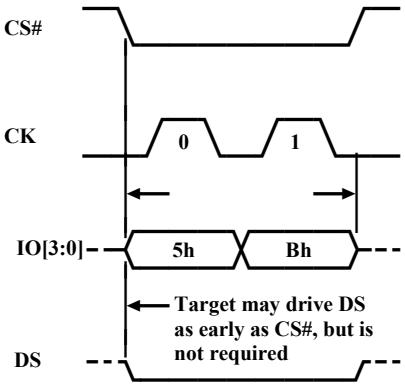


Figure 8 — Fetch SFDP (4S-4S-4S and 4S-4D-4D) Mode Timing Diagram

4.5.9 Fetch SFDP (8D-8D-8D) Mode

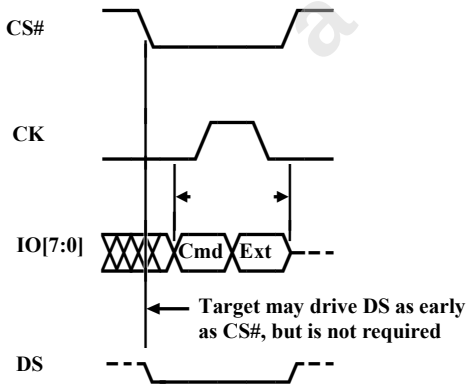


Figure 9 — Fetch SFDP (8D-8D-8D) Mode Timing Diagram

5 Read SFDP Behavior

5.1 Security

The SFDP and flash memory address ranges must never overlap. This ensures that address range checking the controller may perform to prevent access to security keys or other sensitive information stored in flash cannot be bypassed. Also, for PC BIOS applications non-overlap is required to comply with NIST SP800-147.

Addresses beyond the end of the SFDP tables must not alias into the flash memory. Regardless of the implementation, writes to SFDP tables must be permanently disabled before the memory device is released to a customer by the memory vendor factory.

5.2 Reset and Hold Functions

Reset and Hold functionality will be available during the Read SFDP command if the memory device command mode supports these features. Note that these functions may not be available in all modes, as the pins used for Reset or Hold may be reused for I/O pins in Quad and Octal modes.
The JEDEC SPI Protocol Reset is an alternative Reset function that may be used in any mode for devices which support it. See the JEDEC SPI Protocol Reset spec for details.

5.3 Read Wrap

Not supported with the Read SFDP command--even when a memory device defaults to Read Wrap-around mode for other read commands. Only continuous (sequential) read is supported with the Read SFDP command.

5.4 SFDP Address Boundary Wrap

Device behavior when the Read SFDP command crosses the SFDP structure boundary is not defined except for the security restriction specified in 5.1. There is no requirement for the address counter to wrap back to the beginning of the structure and the data read after that point is not specified.

5.5 Reserved SFDP Locations

The content of reserved SFDP locations (memory within the SFDP address space that has not yet been defined or used) is not specified, but recommended to be all FFh.

6 SFDP Database

6.1 SFDP Header Structure

The format of the SFDP header is shown in Figure 10 — Overall Header Structure

	[31:24]	[23:16]	[15:8]	[7:0]	Hex byte location
SFDP Header	Serial Flash Discoverable Parameters (SFDP) Signature = 50444653h				[3h:0h]
	Byte 3 = "P"	Byte 2 = "D"	Byte 1 = "F"	Byte 0 = "S"	
	SFDP Access Protocol	Number of Parameter Headers (NPH)	SFDP Major Revision	SFDP Minor Revision	[7h:4h]
1st Parameter Header	Parameter Length (in double words)	Parameter Major Revision	Parameter Minor Revision	Parameter ID LSB JEDEC ID (00h)	[Bh:8h]
	Parameter ID MSB JEDEC ID (FFh)	Parameter Table Pointer (byte address)			[Fh:Ch]
2nd Parameter Header (optional)	Parameter Length (in double words)	Parameter Major Revision	Parameter Minor Revision	Parameter ID LSB	[13h:10h]
	Parameter ID MSB	Parameter Table Pointer (byte address)			[17h:14h]
		...			
Nth Parameter Header (optional)	Parameter Length (in double words)	Parameter Major Revision	Parameter Minor Revision	Parameter ID LSB	
	Parameter ID MSB	Parameter Table Pointer (byte address)			

Figure 10 — Overall Header Structure

6.2 SFDP Header

The SFDP Header is located at address 000000h of the SFDP data structure. It identifies the SFDP Signature, the number of parameter headers, and the SFDP revision numbers.

Both the SFDP header and the individual parameter table headers include Major and Minor revision numbers.

Major revisions require code (BIOS/firmware) or hardware change to get previously defined discoverable parameters. For example, changes that reorganize previously defined fields.

Minor revisions are changes that define previously reserved fields, add fields to the end, or that clarify definitions of existing fields.

JESD216B maintains backwards compatibility with JESD216A, defines previously reserved bits in the15th DWORD of the Basic Flash Parameter Table and adds optional Function Specific table definitions.

JESD216C maintains backwards compatibility with JESD216B, defines previously reserved bits in the 2nd DWORD of the SFDP Header and adds optional Function Specific table definitions.

JESD216D maintains backwards compatibility with JESD216C.

JESD216E maintains backwards compatibility with JESD216D, defines Secure Read and Secure Write transaction details as well as Replay Protected Monotonic Counter (RPMC) functionality.

JESD216F maintains backwards compatibility with JESD216E.

JESD216G maintains backwards compatibility with JESD216F, defines Generic Register Access Method (GRAM) and SPI Safety Extension (SSE) functionality.

JESD216H maintains backwards compatibility with JESD216G, defines CRC over SFDP and ECC functionality.

The revision numbers of vendor-defined and Function Specific tables follow the same guidelines as the Basic Parameter Table.

Major vs. Minor Revisions

Major revisions indicate that the table structure has changed and may not be backwards compatible with software written for an earlier revision of SFDP.

Increments of minor revisions indicate that fields or DWORDS have been added but the definition of existing fields is unchanged. Software should accept any minor revision number and read only the number of parameter table fields that the software requires. Users should accept any minor revision greater than or equal to the current revision. All fields defined in the current tables will be unchanged in subsequent minor revisions. Undefined or reserved fields may be updated.

6.2.1 SFDP Header: 1st DWORD

Bits	Description
31:0	**SFDP Signature** Allows a user to know that the information is valid. Signature[31:0]: 50444653h

6.2.2 SFDP Header: 2nd DWORD

Bits	Description
31:24	**SFDP Access Protocol** See 6.2.3
23:16	**Number of Parameter Headers (NPH)** Specifies the number of parameter headers in the SFDP data structure. This number is 0-based. Therefore, 0 indicates 1 parameter header. The value of this field is not defined by this standard. It is dependent on the number of tables a vendor implements. The value FFh is reserved for future extensions of this standard.
15:8	**SFDP Major Revision Number** This 8-bit field indicates the major revision number of this standard. The value in this field is 01h for devices which implement the JESD216H revision (unchanged from JESD216D revision). NOTE The value of this field may only be changed by an update to the JESD216 standard.
7:0	**SFDP Minor Revision Number** This 8-bit field indicates the minor revision number of this standard. The value in this field is 0Ch for devices which implement the JESD216H revision. NOTE The value of this field may only be changed by an update to the JESD216 standard.

6.2.3 Definition of SFDP Access Protocol Field

The purpose of the Access Protocol Field is to provide the host controller necessary information about how to read the SFDP command. In early versions of this spec (up to and including JESD216B), this field was FFh. The value FFh still indicates that the SFDP command structure is backwards compatible with the description given in JESD216B. The device will in this case respond to one or more of the SFDP command options as described in JESD216B. Any other value indicates that the SFDP command will behave differently in one or more aspects.

(8D-8D-8D) devices still use FFh as the parameter value if they boot up in one of the modes that are compatible with the JESD216B revision. (Typically this would be (1S-1S-1S) mode.)

For devices where the boot mode may be changed by the user by setting fuses or similar, the device has to update the value returned in the SFDP Access Protocol Field according to the fuse settings.

SFDP Command Parameter Value		
Decimal	**Hex**	
0-239	00h-EFh	Reserved for future use
240	F0h	xSPI NAND class-1 device – parameter data is available in device cache buffer. xSPI Octal, (8D, 8D, 8D) operation, 4-byte addressing for SFDP command, 8 wait states. NAND Flash devices use JESD230C Parameter Page as MSPT. Follow Long latency NVM Class-1 device SFDP access behavior for reading SFDP and MSPT data (see Figure 11) SFDP Parameter Table and NVM Media Specific Parameter Table are available in Device's Cache Buffer before Device is ready to process Host commands during POR process, 1. After POR, Host always first issue READ SFDP (5Ah) with start address ‘00h’ for device discovery • Device returns the SFDP Header with the appropriate parameter value code representing NVM Class-1 Device after received READ SFDP (5Ah) command with start address ‘00h’ 2. Host issues 2nd (and more if needed) READ SFDP (5Ah) command(s) with a non-zero start address to access SFDP and MSPT table contents Device returns the SFDP/MSPT table data beginning from the start address specified in READ SFDP (5Ah) command.

6.2.3 Definition of SFDP Access Protocol Field Table (cont'd)

SFDP Command Parameter Value		
Decimal	**Hex**	
241	F1h	xSPI NAND class-2 device – parameter data is not available in device cache buffer. xSPI Octal, (8D, 8D, 8D) operation, 4-byte addressing for SFDP command, 8 wait states. NAND Flash devices use JESD230C Parameter Page as MSPT. Follow Long latency NVM Class-2 device SFDP access behavior for reading SFDP and MSPT data (see Figure 12) Parameter Tables are not available in the device's Cache Buffer before Device is ready to process Host commands during POR process, 1. After POR, Host always first issue READ SFDP (5Ah) with start address '00h' for device discovery • Device returns SFDP Header with the appropriate parameter value code representing NVM Class-2 Device after received READ SFDP (5Ah) command with '00h' start address 2. Host issue FETCH SFDP (5Bh) command to Device 3. Host: wait 120µs; Device: fetches SFDP and MSPT tables from memory cell array to Device's Cache Buffer 4. Host issues 2nd (and more if needed) READ SFDP (5Ah) command(s) with a non-zero start address to access SFDP and MSPT table contents • Device returns the SFDP/MSPT Table data beginning from the start address specified in READ SFDP (5Ah) command
242	F2h	Reserved for xSPI NAND class-3 device, Combo device includes both NOR Flash and Class-1 Long Latency NVM. -for octal interface to low Latency combo with SFDP table in the cache and can use a 5Ah command
243	F3h	Reserved for xSPI NAND class-3 device – combo device with both NOR Flash device and Class-2 Long Latency NVM device -for octal interface to low Latency combo with SFDP table is not in the cache and requires a 5Bh command before the 5Ah command
244	F4h	SPI NAND class-1 device – parameter data is available in device cache buffer Legacy option: Behavior consistent with JESD216B revision. (1S-1S-1S), (2S-2S-2S) or (4S-4S-4S) operation, 3-byte addressing for SFDP command, 8 wait states. NAND Flash devices use JESD230C Parameter Page as MSPT Follow Long latency NVM Class-1 device SFDP access behavior for reading SFDP and MSPT data (see Figure 11)

6.2.3 Definition of SFDP Access Protocol Field Table (cont'd)

SFDP Command Parameter Value		
Decimal	**Hex**	
245	F5h	SPI NAND class-2 device – parameter data is not available in device cache buffer Legacy option: Behavior consistent with JESD216B revision. (1S-1S-1S), (2S-2S-2S) or (4S-4S-4S) operation, 3-byte addressing for SFDP command, 8 wait states. NAND Flash devices use JESD230C Parameter Page as MSPT Follow Long latency NVM Class-2 device SFDP access behavior for reading SFDP and MSPT data
246	F6h	Reserved for SPI NAND class-3 device, Combo device includes both NOR Flash and Class-1 Long Latency NVM.
247	F7h	Reserved for SPI NAND class-3 device, Combo device includes both NOR Flash and SPI Class-2 Long Latency NVM.
248:249	F8h:F9h	Reserved for future use
250	FAh	xSPI NOR Profile 2 (8D, 8D, 8D) operation, 5-byte addressing, SFDP command (WREN1 and WREN2), Configurable wait states.
251	FBh	Reserved for future use
252	FCh	xSPI NOR Profile 1 Octal, (8D, 8D, 8D) operation, 3-byte addressing + 1/2 Cycle for Octal DTR Alignment for SFDP command, 8 wait states.
253	FDh	xSPI NOR Profile 1 Octal, (8D, 8D, 8D) operation, 4-byte addressing for SFDP command, 20 wait states.
254	FEh	xSPI NOR Profile 1 Octal, (8D, 8D, 8D) operation, 4-byte addressing for SFDP command, 8 wait states.
255	FFh	Legacy option: Behavior consistent with JESD216B revision. (1S-1S-1S), (2S-2S-2S) or (4S-4S-4S) operation, 3-byte addressing for SFDP command, 8 wait states.

6.2.3 Definition of SFDP Access Protocol Field (cont'd)

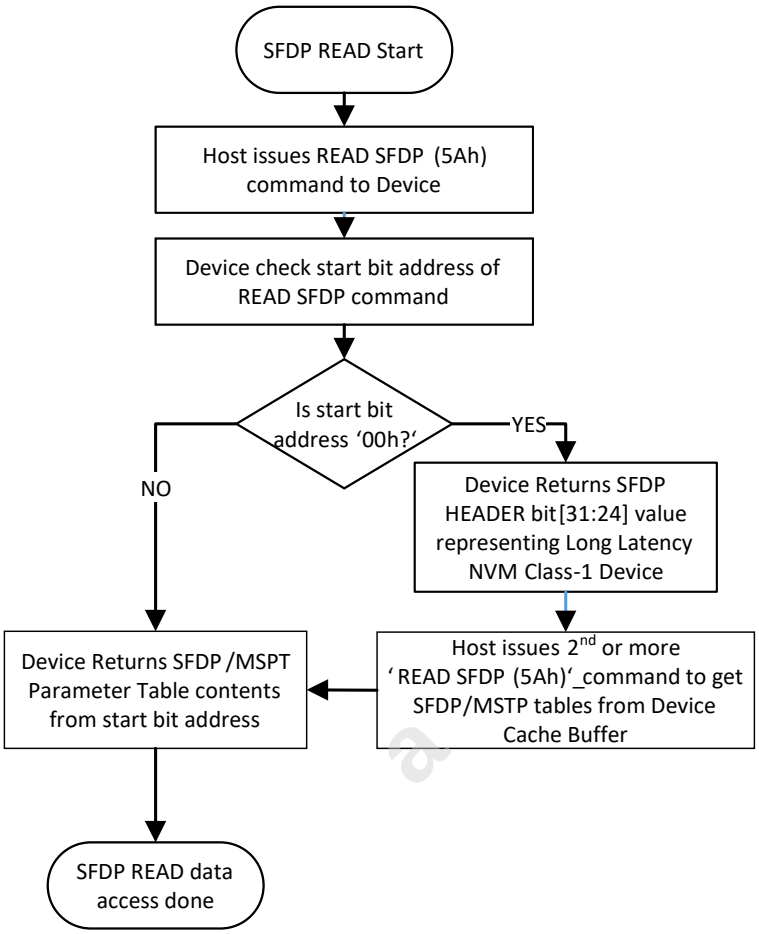


Figure 11 — xSPI NAND Class-1 Device Read SFDP Flow

6.2.3 Definition of SFDP Access Protocol Field (cont'd)

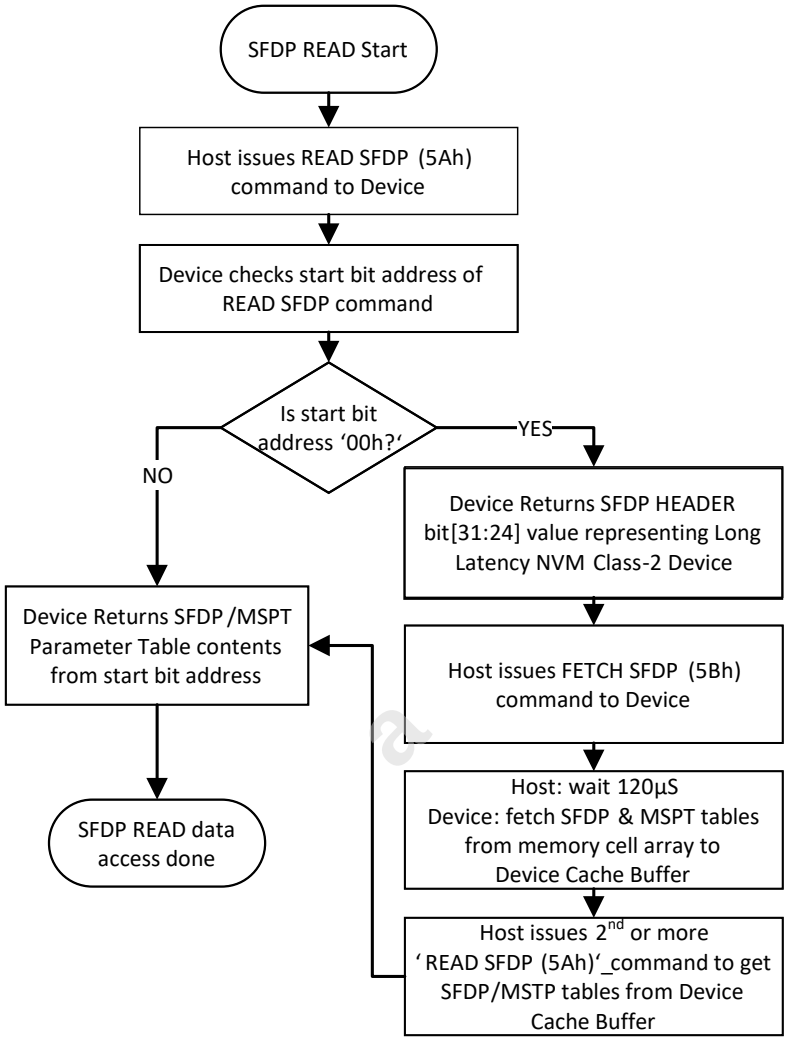


Figure 12 — xSPI NAND Class-2 Device Read SFDP Flow

6.3 Parameter Headers

Each Parameter Header identifies the size, location, revision, ownership, and function of their associated parameter tables. Parameter table ownership will be either JEDEC (via this standard) or an individual vendor (via vendor specific documentation).

Multiple parameter headers can be specified with each parameter header being 2 DWORDs (64-bits). The first parameter header is mandatory, is defined by this standard, and starts at byte offset 08h. If a vendor chooses to include multiple revisions of the Basic Parameter Table, they may do so provided the table headers are in order starting with the oldest version. The total number of parameter headers is specified in the NPH field of the SFDP header, see 6.2.2. All subsequent parameter headers need to be contiguous and may be specified by JEDEC or by vendors using the same structure (shown in Figure 10). Minor revisions may overlap earlier revisions by starting at the same address as an earlier revision but have additional length for parameters added in the later revision. This allows the use of legacy parameters without the need to repeat them in each new minor revision.

6.3.1 Parameter Header: 1st DWORD

Bits	Description
31:24	**Parameter Table Length** This field specifies how many DWORDs are in the Parameter table. NOTE This field is 1's based. Therefore, 1 indicates 1 DWORD.
23:16	**Parameter Table Major Revision Number[1]** This 8-bit field indicates the major revision number of the associated parameter table. NOTE Major Revision starts at 01h. The Major Revision of JEDEC defined parameter tables can only be modified by updates to this standard. The Major Revision of a vendor-specified table is controlled by that vendor.
15:8	**Parameter Table Minor Revision Number[1]** This 8-bit field indicates the minor revision number of the associated parameter table. NOTE Minor Revision starts at 00h. The Minor Revision of the JEDEC owned parameter tables can only be modified by updates to this standard. The Minor Revision of a vendor-specified table is controlled by that vendor.
7:0	**Parameter ID LSB:** Refer to Definition of Parameter ID Field in 6.3.3.
NOTE	See "Major vs. Minor Revisions" in 6.2

6.3.2 Parameter Header: 2nd DWORD

Bits	Description
31:24	**Parameter ID MSB** Refer to Definition of Parameter ID Field in 6.3.3.
23:0	**Parameter Table Pointer (PTP)** This address specifies the start of this header's Parameter Table in the SFDP structure. This is a byte address and must be DWORD-aligned.

6.3.3 Definition of Parameter ID Field

The Parameter ID indicates the parameter table ownership and type.

Parameter ID MSB	Parameter ID LSB	Type	Owner
01h – 7Fh	odd parity	Vendor specific	Vendor
01h – 7Fh	even parity	Function specific	Vendor
80h – FFh	even parity	Function specific	JEDEC JC-42.4
FFh	00h	Basic Parameter Table	JEDEC JC-42.4

Function Specific tables may be defined by the JC-42.4 Committee or a manufacturer (vendor). The purpose of the Function Specific tables is to allow development of features and associated parameter tables common to multiple manufacturers, prior to the parameter tables being incorporated into the next revision of JESD216. Allocation of IDs for Function Specific tables is requested through the JEDEC office, see Annex A.

Vendor Specific table structure is defined by the identified device vendor. The parameter table ID field identifies the vendor that owns the table definition.

The original JESD216 standard used only a one byte ID field to identify the parameter table owner. JESD216 revision A expanded the ID field to two bytes, MSB and LSB, because a single byte is insufficient to uniquely identify all manufacturers (vendors). The original single byte parameter ID is now referred to as the parameter ID LSB.

The Parameter ID LSB value of 00h is reserved for the Basic Parameter Table defined by this standard. For backwards compatibility the MSB is FFh when the LSB is 00h and LSB 00h shall not be used when the MSB is any value other than FFh. This is because some legacy systems using the original JESD216 standard may ignore the MSB and assume any parameter ID with LSB of 00h is the Basic Parameter Table.

Parameter IDs with:

- An MSB of 01h though 7Fh indicates a Vendor Owned table and provides the bank number of a JEDEC JEP106 assigned Manufacturer ID.
  - 00h is reserved because JEP106 bank numbering begins at 01h
  - The JEP106 Manufacturer's Identification Code LSB is an eight (8) bit field, consisting of seven (7) data bits plus one (1) odd parity bit in the most significant bit position. A Parameter ID LSB with odd parity signifies a Manufacturer's Identification Code and a Parameter ID LSB with even parity signifies a Function Specific table.

6.3.3 Definition of Parameter ID Field (cont'd)

- An MSB of 80h through FFh indicates a Function Specific or Basic Parameter Table defined by the JEDEC 42.4 committee. The LSB is used to identify the Function Specific table type.
  - Any parameter ID with LSB 00h identifies the SPI protocol Basic Parameter Table.
  - LSB values with even parity are Function Specific tables that are defined by the JC-42.4 committee.
  - LSB values with odd parity are illegal to prevent any confusion with JEP106 manufacturer ID values.

6.3.3.1 Function Specific parameter table ID assignments

Description	ID (Hex)
Basic SPI protocol	FF00
Sector map	FF81
Replay Protected Monotonic Counters (RPMC)	FF03
4-byte Address Instruction Table	FF84
eXtended Serial Peripheral Interface (xSPI) Profile 1.0	FF05
eXtended Serial Peripheral Interface (xSPI) Profile 2.0	FF06
Status, Control and Configuration Register Map	FF87
Status, Control and Configuration Register Map Offsets for Multi-Chip SPI Memory Devices	FF88
Status, Control and Configuration Register Map for xSPI Profile 2.0	FF09
Command Sequences to change to Octal DDR (8D-8D-8D) mode	FF0A
Long Latency NVM Media Specific Parameter Table (MSPT)	FF8B
x4 Quad IO with DS	FF0C
Command Sequences to change to Quad DDR (4S-4D-4D) mode	FF8D
Secure Packet Read / Secure Packet Write	FF8E
Generic Register Access Method (GRAM) Parameter Table	FF0F
SPI Safety Extensions (CRC) Parameter Table	FF90
SFDP CRC	FF11
Error Correction Code (ECC) Parameter Table	FF12
Reserved for next Function Specific Table assignment	FF93

6.3.4 Example SFDP Headers

Note the definition and discussion of Parameter Headers in paragraph 6.3.

Figure 13 shows an example of a basic SFDP Header (major revision 1, minor revision 7): one Parameter Header, Parameter Table length of 16 DWORDs, 1st Parameter Header Revision 1.7, JEDEC ID of FF00h, and the Parameter Table Pointer pointing to location 000010h. This header is backwards compatible with previous generations of this standard, therefore devices are not required to contain headers with prior revision numbers.

Figure 14 shows the same example as in Figure 13 but with Word based addressing (instead of byte) as needed for xSPI Profile 2.0.

6.3.4 Example SFDP Headers (cont'd)

In Figure 15, the first parameter header points to a version 1.0 format Basic Parameter Table of 9 DWORDs starting at location 100h and the second parameter headers both points to a separate version 1.6 format Basic Parameter Table of 16 DWORDs starting at location 200h.

Figure 16 adds one of the Optional Function Specific headers introduced in JESD216B. This third header indicates that this device supports 4-byte address instructions functionality.

In Figure 15 and Figure 16, devices that do not have the functionality of these features may not contain these additional parameters.

Example calculation using the Parameter Table Pointer (PTP):
The PTP is a byte address. The fields within this document are defined in terms of DWORDS.

To calculate the byte address of a particular field, given a PTP of 100h:
The SFDP byte address of the 3rd DWORD = 100h + ((3-1) * 4) = 100h + 2 *4 = 100h + 8 = 108h

For xSPI Profile 2.0, the PTP is a word address. The fields within this document are defined in terms of DWORDS.

To calculate the word address of a particular field, given a PTP of 100h:
The SFDP word address of the 3rd DWORD = 100h + ((3-1) * 2) = 100h + 1 *4 = 100h + 4 = 104h

	[31:24]	[23:16]	[15:8]	[7:0]	Hex Byte Location
SFDP Header	50h	44h	46h	53h	< [3h:0h]
	FFh	00h	01h	06h	< [7h:4h]
1st Parameter Header	10h	01h	06h	00h	< [Bh:8h]
	FFh	00h	00h	10h	< [Fh:Ch]

Figure 13 — Example SFDP Header with single Basic Parameter Table

	[31:24]	[23:16]	[15:8]	[7:0]	Hex Word Location
SFDP Header	50h	44h	46h	53h	< [1h:0h]
	FFh	00h	01h	06h	< [3h:2h]
1st Parameter Header	10h	01h	06h	00h	< [5h:4h]
	FFh	00h	00h	10h	< [7h:6h]

Figure 14 — Example SFDP Header with single Basic Parameter Table Word based (xSPI Profile 2.0)

6.3.4 Example SFDP Headers (cont'd)

	[31:24]	[23:16]	[15:8]	[7:0]	Hex Byte Location
SFDP Header	50h	44h	46h	53h	< [3h:0h]
	FFh	01h	01h	06h	< [7h:4h]
1st Parameter Header	09h	01h	00h	00h	< [Bh:8h]
	FFh	00h	01h	00h	< [Fh:Ch]
2nd Parameter Header	10h	01h	06h	00h	< [13h:10h]
	FFh	00h	02h	00h	< [17h:14h]

Figure 15 — Example SFDP Header with two Basic parameter Tables

	[31:24]	[23:16]	[15:8]	[7:0]	Hex Byte Location
SFDP Header	50h	44h	46h	53h	< [3h:0h]
	FFh	02h	01h	06h	< [7h:4h]
1st Parameter Header	09h	01h	00h	00h	< [Bh:8h]
	FFh	00h	01h	00h	< [Fh:Ch]
2nd Parameter Header	10h	01h	06h	00h	< [13h:10h]
	FFh	00h	02h	00h	< [17h:14h]
3rd Parameter Header	02h	01h	00h	84h	< [1Bh:18h]
	FFh	00h	02h	80h	< [1Fh:1Ch]

Figure 16 — Example SFDP Header with two basic Parameter Tables and one optional (4-Byte Address) Function Specific Tables

6.3.4 Example SFDP Headers (cont'd)

	[31:24]	[23:16]	[15:8]	[7:0]	Hex Byte Location
SFDP Header	50h	44h	46h	53h	< [3h:0h]
	FFh	03h	01h	06h	< [7h:4h]
1st Parameter Header	09h	01h	00h	00h	< [Bh:8h]
	FFh	00h	01h	00h	< [Fh:Ch]
2nd Parameter Header	10h	01h	06h	00h	< [13h:10h]
	FFh	00h	02h	00h	< [17h:14h]
3rd Parameter Header	02h	01h	01h	84h	< [1Bh:18h]
	FFh	00h	02h	80h	< [1Fh:1Ch]
4th Parameter Header	07	01h	00h	06h	< [23h:20h]
	FFh	00h	03h	00h	< [27h:24h]

Figure 17 — Example SFDP Header with two basic Parameter Tables and two optional (4-Byte Address and Status, Control and Configuration Register Map) Function Specific Tables

6.4 JEDEC Basic Flash Parameter Header and Table

Parameter tables contain coded information describing the features and capabilities of the serial flash. The first parameter table as defined by JEDEC is mandatory and its starting address is specified by the PTP field of the 1st Parameter Header. This table identifies some of the basic features of SPI protocol flash memory devices.

6.4.1 JEDEC Basic Flash Parameter Header: 1st DWORD

Bits	Description
31:24	**Parameter Table Length** This field specifies how many DWORDs are in the Parameter table. NOTE This field is 1's based. Therefore, 1 indicates 1 DWORD. For the JESD216G revision, this parameter table length is 23 (unchanged from JESD216F)
23:16	**Parameter Table Major Revision Number** This 8-bit field indicates the major revision number of the parameter table. The value in this field is 01h for this table defined by JESD216H revision (unchanged from JESD216G revision). NOTE The Major Revision of JEDEC defined parameter tables can only be modified by updates to this standard.

6.4.1 JEDEC Basic Flash Parameter Header Table: 1st DWORD (cont'd)

Bits	Description
15:8	**Parameter Table Minor Revision Number** This 8-bit field indicates the minor revision number of the JEDEC Basic Flash Parameter table. The value in this field is 09h for this table defined by JESD216H revision (incremented due to updates to DWORDs 15 and 19). NOTE The Minor Revision of the JEDEC owned parameter tables can only be modified by updates to this standard.
7:0	**Parameter ID LSB** The JEDEC Basic Flash Parameter Table is assigned the ID LSB of 00h.

6.4.2 JEDEC Basic Flash Parameter Header: 2nd DWORD

Bits	Description
31:24	**Parameter ID MSB** The JEDEC Basic Flash Parameter Table is assigned the ID MSB of FFh.
23:0	**Parameter Table Pointer (PTP)** This address specifies the start of this header's Parameter Table in the SFDP structure. The address is in terms of bytes and must be DWORD-aligned.

6.4.3 JEDEC Basic Flash Parameter Table Overview

DWORD	Description
1	Uniform 4KB Sectors, Write Buffer Size, Volatile Status Register, Fast Read Support (1S-1S-2S) (1S-2S-2S) (1S-4S-4S)(1S-1S-4S), Number of Address Bytes, DTR Support
2	Memory Density
3	Fast Read (1S-4S-4S) (1S-1S-4S): Wait States, Mode Bit Clocks, Instruction
4	Fast Read (1S-1S-2S) (1S-2S-2S): Wait States, Mode Bit Clocks, Instruction
5	Fast Read (2S-2S-2S) (4S-4S-4S) Support
6	Fast Read (2S-2S-2S): Wait States, Mode Bit Clocks, Instruction
7	Fast Read (4S-4S-4S): Wait States, Mode Bit Clocks, Instruction
8	Erase Type 1 and 2 Size and Instruction
9	Erase Type 3 and 4 Size and Instruction
10	Erase Type (1:4) Typical Erase Times and Multiplier Used To Derive Max Erase Times
11	Chip Erase Typical Time, Byte Program and Page Program Typical Times, Page Size
12	Erase/Program Suspend/Resume Support, Intervals, Latency, Keep Out Area Size
13	Program/Erase Suspend/Resume Instructions
14	Deep Powerdown and Status Register Polling Device Busy
15	Hold and WP Disable Function, Quad Enable Requirements, 4S-4S-4S Mode Enable/Disable Sequences, 0-4-4 Entry/Exit Methods and Support
16	32-bit Address Entry/Exit Methods and Support, Soft Reset and Rescue Sequences, Volatile and Non-volatile Status Register Support
17	Fast Read (1S-8S-8S) (1S-1S-8S): Wait States, Mode Bit Clocks, Instruction
18	Octal commands, Byte order, Data strobe, JEDEC SPI Protocol Reset
19	Octal Enable Requirements, 8D-8D-8D Mode Enable/Disable Sequences, 0-8-8 Entry/Exit Methods and Support
20	Maximum operating speeds
21	Fast Read (1S-1D-1D), (1S-2D-2D), (1S-4D-4D), and (4S-4D-4D) Support
22	Fast Read (1S-1D-1D) and (1S-2D-2D) Wait States, Mode Bit Clocks, and Instruction
23	Fast Read (1S-4D-4D) and (4S-4D-4D) Wait States, Mode Bit Clocks, and Instruction

6.4.4 JEDEC Basic Flash Parameter Table: 1st DWORD

Bits	Description
31:23	**Unused** Contains FFh and can never be changed.
22	**Supports (1S-1S-4S) Fast Read** Device supports single input instruction and address and quad output data Fast Read. 0: (1S-1S-4S) Fast Read NOT supported. 1: (1S-1S-4S) Fast Read supported.
21	**Supports (1S-4S-4S) Fast Read** Device supports single input instruction, quad input address, and quad output data Fast Read. 0: (1S-4S-4S) Fast Read NOT supported. 1: (1S-4S-4S) Fast Read supported.
20	**Supports (1S-2S-2S) Fast Read** Device supports single input instruction, dual input address, and dual output data Fast Read. 0: (1S-2S-2S) Fast Read NOT supported. 1: (1S-2S-2S) Fast Read supported.
19	**Supports Double Transfer Rate (DTR) Clocking** Indicates the device supports some type of double transfer rate clocking. 0: DTR NOT supported 1: DTR Clocking supported
18:17	**Address Bytes** Number of bytes used in addressing flash array read, write and erase: 00b: 3-Byte only addressing 01b: 3- or 4-Byte addressing (e.g., defaults to 3-Byte mode; enters 4-Byte mode on command) 10b: 4-Byte only addressing 11b: Reserved NOTE This field refers to the number of address bits/bytes that are clocked in for any command requiring an address except for SFDP Header or Table accesses. All SFDP accesses use 3-byte addressing. A device using 4-byte only addressing may still support 03h read using 3-byte addressing. Examples: Read, Fast Read, Write, 4 kilobyte Erase.
16	**Supports (1S-1S-2S) Fast Read** Device supports single input instruction and address and dual output data Fast Read with 8 wait states. 0: (1S-1S-2S) Fast Read NOT supported. 1: (1S-1S-2S) Fast Read supported.
15:8	**4 Kilobyte Erase Instruction** NOTE If 4 kilobyte erase is not supported, then enter FFh. This instruction must also be included in one of the Erase Types in 6.4.8 or 6.4.12

6.4.4 JEDEC Basic Flash Parameter Table: 1st DWORD (cont'd)

Bits	Description
7:5	**Unused** Contains 111b and can never be changed.
4	**Write Enable Instruction Select for Writing to Volatile Status Register** This bit only applies if bit 3 is 1. 0: flash device requires instruction 50h as the write enable prior to performing a volatile write to the status register 1: flash device requires instruction 06h as the write enable prior to performing a volatile write to the status register. NOTE If target flash status register is nonvolatile, then bits 3 and 4 must be set to 00b. This bit definition is maintained for legacy compatibility only. New system implementations should refer to 0 for a full definition of volatile and non-volatile behavior.
3	**Volatile Status Register Block Protect bits** 0: Block Protect bits in device's status register are solely non-volatile or may be programmed either as volatile using the 50h instruction for write enable or non-volatile using the 06h instruction for write enable. 1: Block Protect bits in device's status register are solely volatile. NOTE If target flash register is non-volatile, then bits 3 and 4 must be set to 00b. This bit definition is maintained for legacy compatibility only. New devices should refer to 0 for a full definition of volatile and non-volatile behavior.
2	**Write Granularity** 0: 1 Byte – Use this setting for single byte programmable devices or buffer programmable devices when the buffer is less than 64 bytes (32 Words). 1: Use this setting for buffer programmable devices when the buffer size is 64 bytes (32 Words) or larger. This bit definition is maintained for legacy compatibility only. New system implementations should refer to 6.4.14 for the buffer (page) size. The legacy minimum write granularity is a single byte within any size programming buffer.
1:0	**Block/Sector Erase Sizes** Identifies if the device supports uniform 4k erase blocks. This erase size information must also be included one of the Erase Types in 6.4.11or 6.4.12. 00b: Reserved 01b: 4 kilobyte Erase is supported throughout the device 10b: Reserved 11b: Use this setting only if uniform 4 kilobyte erase is unavailable. NOTE This is a legacy field. Refer to clauses 6.4.8 and 6.4.12 for information on what erase sizes are supported.

6.4.5 JEDEC Basic Flash Parameter Table: 2nd DWORD

Bits	Description
31:0	**Flash Memory Density** For densities 2 gigabits or less, bit-31 is set to 0b. The field 30:0 defines the size in bits. Example: 00FFFFFFh = 16 megabits For densities 4 gigabits and above, bit-31 is set to 1b. The field 30:0 defines 'N' where the density is computed as 2^N bits (N must be >= 32)**.** Example: 80000021h = 2^33 = 8 gigabits

6.4.6 JEDEC Basic Flash Parameter Table: 3rd DWORD

Bits	Description
31:24	**(1S-1S-4S) Fast Read Instruction** Instruction for single input instruction and address and quad output data Fast Read.
23:21	**(1S-1S-4S) Fast Read Number of Mode Clocks** This field will be 000b if Mode Bits are not supported, NOTE This field should be counted in clocks not number of bits received by the serial flash. The initiator drives the bus during "mode bits" cycles; the initiator tri-states the bus during "dummy" cycles. **Example:** If 4 mode bits are needed with a single input address phase command, this field would be 100b.
20:16	**(1S-1S-4S) Fast Read Number of Wait states (dummy clocks) needed before valid output** This field will be 00000b if wait states/dummy clocks are not supported. (The number of dummy clocks should be > 0 to avoid contention on bi-directional pins.)
15:8	**(1S-4S-4S) Fast Read Instruction** Instruction for single input instruction, quad input address, and quad output data Fast Read.
7:5	**Quad Input Address Quad Output (1S-4S-4S) Fast Read Number of Mode Clocks** This field will be 000b if Mode bits are not supported, NOTE This field should be counted in clocks not number of bits received by the serial flash. The initiator drives the bus during "mode bits" cycles; the initiator tri-states the bus during "dummy" cycles. **Example:** If 8 mode bits are needed with a quad input address phase command, this field would be 010b.
4:0	**(1S-4S-4S) Fast Read Number of Wait states (dummy clocks) needed before valid output** This field will be 00000b if wait states/dummy clocks are not supported. (The number of dummy clocks should be > 0 to avoid contention on bi-directional pins.)

6.4.7 JEDEC Basic Flash Parameter Table: 4th DWORD

Bits	Description
31:24	**(1S-2S-2S) Fast Read Instruction** Instruction for single input instruction, dual input address, and dual output data Fast Read.
23:21	**(1S-2S-2S) Fast Read Number of Mode Clocks** This field will be 000b if Mode bits are not supported, NOTE This field should be counted in clocks not number of bits received by the serial flash. The initiator drives the bus during "mode bits" cycles; the initiator tri-states the bus during "dummy" cycles. **Example:** If 8 mode bits are needed with a dual input address phase command, this field would be 100b.
20:16	**(1S-2S-2S) Fast Read Number of Wait states (dummy clocks) needed before valid output** This field will be 00000b if wait states/dummy clocks are not supported. (The number of dummy clocks should be > 0 to avoid contention on bi-directional pins.)
15:8	**(1S-1S-2S) Fast Read Instruction** Instruction for single input instruction and address and dual output data Fast Read. NOTE The industry standard is 3Bh
7:5	**(1S-1S-2S) Fast Read Number of Mode Clocks** This field will be 000b if Mode bits are not supported, NOTE This field should be counted in clocks not number of bits received by the serial flash. **Example:** If 4 mode bits are needed with a single input address phase command, this field would be 100b.
4:0	**(1S-1S-2S) Fast Read Number of Wait states (dummy clocks) needed before valid output** This field should be programmed with 01000b for 8 clocks of dummy cycle. (The number of dummy clocks should be > 0 to avoid contention on bi-directional pins.) NOTE For legacy reasons, if dummy clocks for this instruction is not 01000b, then bit 16 in 6.4.1 (Supports (1S-1S-2S) Fast Read with 8 wait states) must NOT be set to '1'.

6.4.8 JEDEC Basic Flash Parameter Table: 5th DWORD

Bits	Description
31:5	Reserved. These bits default to all 1's
4	**Supports (4S-4S-4S) Fast Read** Device supports Quad input instruction and address and quad output data Fast Read. 0: (4S-4S-4S) Fast Read NOT supported. 1: (4S-4S-4S) Fast Read supported.
3:1	Reserved. These bits default to all 1's
0	**Supports (2S-2S-2S) Fast Read** Device supports dual input instruction and address and dual output data Fast Read. 0: (2S-2S-2S) Fast Read NOT supported. 1: (2S-2S-2S) Fast Read supported.

6.4.9 JEDEC Basic Flash Parameter Table: 6th DWORD

Bits	Description
31:24	**(2S-2S-2S) Fast Read Instruction** Instruction for dual input instruction and address and dual output data Fast Read.
23:21	**(2S-2S-2S) Fast Read Number of Mode Clocks** This field will be 000b if Mode bits are not supported, NOTE This field should be counted in clocks not number of bits received by the serial flash. The initiator drives the bus during "mode bits" cycles; the initiator tri-states the bus during "dummy" cycles. **Example:** If 4 mode bits are needed with a (2S-2S-2S) Fast Read command, this field would be 010b.
20:16	**(2S-2S-2S) Fast Read Number of Wait states (dummy clocks) needed before valid output** This field will be 00000b if wait states/dummy clocks are not supported. (The number of dummy clocks should be > 0 to avoid contention on bi-directional pins.)
15:0	Reserved. These bits default to all 1's

6.4.10 JEDEC Basic Flash Parameter Table: 7th DWORD

Bits	Description
31:24	**(4S-4S-4S) Fast Read Instruction** Instruction for quad input instruction/address, quad output data Fast Read.
23:21	**(4S-4S-4S) Fast Read Number of Mode Clocks** This field will be 000b if Mode bits are not supported, NOTE This field should be counted in clocks not number of bits received by the serial flash. The initiator drives the bus during "mode bits" cycles; the initiator tri-states the bus during "dummy" cycles. **Example:** If 8 mode bits are needed with a (4S-4S-4S) Fast Read phase command, this field would be 010b.
20:16	**(4S-4S-4S) Fast Read Number of Wait states (dummy clocks) needed before valid output** This field will be 00000b if wait states/dummy clocks are not supported. (The number of dummy clocks should be > 0 to avoid contention on bi-directional pins.)
15:0	Reserved. These bits default to all 1's

6.4.11 JEDEC Basic Flash Parameter Table: 8th DWORD

NOTE If the device uses a 4k subsector size, that size and instruction must be included somewhere in the 8th or 9th DWORD. This allows the user to discover the typical and maximum erase times for the 4k subsector by referencing the 10th DWORD.

Bits	Description
31:24	**Erase Type 2 Instruction** Instruction used to erase the number of bytes specified by Erase Type 2 Size (bits 23-16).
23:16	**Erase Type 2 Size:** This field will be 00h if this erase type does not exist. NOTE This field specifies 'N' and is used to calculate erase type size = 2^N bytes **Example:** If the erase type size is 32 kilobytes, this field would 0Fh.
15:8	**Erase Type 1 Instruction** Instruction used to erase the number of bytes specified by Erase Type 1 Size (bits 7-0).
7:0	**Erase Type 1 Size** NOTE This field specifies 'N' and is used to calculate erase type size = 2^N bytes **Example:** If the erase type size is 4 kilobytes, this field would 0Ch.

6.4.12 JEDEC Basic Flash Parameter Table: 9th DWORD

Bits	Description
31:24	**Erase Type 4 Instruction** Instruction used to erase the number of bytes specified by Erase Type 4 Size (bits 23-16).
23:16	**Erase Type 4 Size** This field will be 00h if this erase type does not exist. NOTE This field specifies 'N' and is used to calculate erase type size = 2^N bytes **Example:** If the erase type size is 256 kilobytes, this field would 12h.
15:8	**Erase Type 3 Instruction** Instruction used to erase the number of bytes specified by Erase Type 3 Size (bits 7-0).
7:0	**Erase Type 3 Size** This field will be 00h if this erase type does not exist. NOTE This field specifies 'N' and is used to calculate erase type size = 2^N bytes **Example:** If the erase type size is 64 kilobytes, this field would 10h.

6.4.13 JEDEC Basic Flash Parameter Table: 10th DWORD

Bits	Description
31:25	**Erase Type 4 Erase, Typical time** Time the device *typically* takes to erase an Erase Type 4 size, see 6.4.12. User must poll device busy to determine if the operation has completed. This field has no meaning if the Erase Type 4 size is 00h. 31:30 units (00b: 1 ms, 01b: 16 ms, 10b: 128 ms, 11b: 1 s) 29:25 count Formula: typical time = (count + 1)*units Example: If count=2 and units=10b, then typical time is (2+1)*128ms = 384 ms The range is 1ms to 32 seconds in four groups: 1 ms to 32 ms, 16 ms to 512 ms, 128 ms to 4096 ms, 1 s to 32 s
24:18	**Erase Type 3 Erase, Typical time** Time the device *typically* takes to erase an Erase Type 3 size, see 6.4.12. User must poll device busy to determine if the operation has completed. This field has no meaning if the Erase Type 3 size is 00h. 24:23 units (00b: 1 ms, 01b: 16 ms, 10b: 128 ms, 11b: 1 s) 22:18 count Formula: typical time = (count + 1)*units Example: If count=1 and units=10b, then typical time is (1+1)*128ms = 256 ms The range is 1ms to 32 seconds in four groups: 1 ms to 32 ms, 16 ms to 512 ms, 128 ms to 4096 ms, 1 s to 32 s

6.4.13 JEDEC Basic Flash Parameter Table: 10th DWORD (cont'd)

Bits	Description
17:11	**Erase Type 2 Erase, Typical time** Time the device *typically* takes to erase an Erase Type 2 size, see 6.4.8. User must poll device busy to determine if the operation has completed. This field has no meaning if the corresponding Erase Type size is 00h. 17:16 units (00b: 1 ms, 01b: 16 ms, 10b: 128 ms, 11b: 1 s) 15:11 count Formula: typical time = (count + 1)*units Example: If count=0 and units=10b, then typical time is (0+1)*128ms = 128 ms The range is 1ms to 32 seconds in four groups: 1 ms to 32 ms, 16 ms to 512 ms, 128 ms to 4096 ms, 1 s to 32 s
10:4	**Erase Type 1 Erase, Typical time** Time the device *typically* takes to erase an Erase Type 1 size, see 6.4.8. User must poll device busy to determine if the operation has completed. This field has no meaning if the corresponding Erase Type size is 00h. 10:9 units (00b: 1 ms, 01b: 16 ms, 10b: 128 ms, 11b: 1 s) 8:4 count Formula: typical time = (count + 1)*units Example: If count=1 and units=10b, then typical time is 1*128ms = 128 ms The range is 1ms to 32 seconds in four groups: 1 ms to 32 ms, 16 ms to 512 ms, 128 ms to 4096 ms, 1 s to 32 s
3:0	**Multiplier from typical erase time to maximum erase time** 3:0 count Formula: Erase Type n (or Chip) erase maximum time = 2 * (count + 1) * Erase Type n (or Chip) erase typical time Example: If count = 9, then Erase Type n (or Chip) erase maximum time is 20 * Sector Type n (or Chip) erase typical time NOTE 1 'n' = 1, 2, 3, or 4 NOTE 2 This multiplier applies to all erase types and the chip erase. The maximum time is intended to be used as a watchdog timeout for an error or failure condition. Since a common scale factor is used across all erase sizes, any particular maximum time may only approximate the datasheet maximum time.

6.4.14 JEDEC Basic Flash Parameter Table: 11th DWORD

Bits	Description
31	**Reserved**
30:24	**Chip Erase, Typical time** Typical time to erase one chip (die). User must poll device busy to determine if the operation has completed. For a device consisting of multiple dies, that are individually accessed, the time is for each die to which a chip erase command is applied. 30:29 units (00b: 16 ms, 01b: 256 ms, 10b: 4 s, 11b: 64 s) 28:24 count Formula: typical time = (count + 1)*units Example: If count=5 and units=10b, then typical time is: 5*4 s = 20 s The range of this field is 16ms to 2048 seconds in four groups: 16 ms to 512 ms, 256 ms to 8192 ms, 4 s to 128 s, 64 s to 2048 s
23:19	**Byte Program Typical time, additional byte** Time the device *typically* takes to write each additional byte after the first. User must poll device busy to determine if the operation has completed. 23 units (0: 1 µs, 1: 8 µs) 22:19 count Formula: additional byte time = (count + 1)*units/byte Example: If units = 1 and count =4, then each additional byte typically adds (4+1)*8 µs = 40 µs to the programming time. For 16 bytes, the additional time would be 16 * 40 µs = 640 µs The range is 1 µs to 128 µs in two groups: 1 µs to 16 µs and 8 µs to 128 µs. NOTE The programming time for small numbers of bytes does not scale linearly up to a full page programming time. When the number of bytes being programmed exceeds ½ of a page size, users should base estimates on the Page Program typical time in this DWORD.
18:14	**Byte Program Typical time, first byte** Time the device *typically* takes to write the first byte in a sequence. User must poll device busy to determine if the operation has completed. 18 units (0: 1 µs, 1: 8 µs) 17:14 count Formula: first byte typical time = (count + 1)*units Example: If units = 0 and count = 7, then typical time is (7+1)*1 µs = 8 µs The range is 1 µs to 128 µs in two groups: 1 µs to 16 µs and 8 µs to 128 µs

6.4.14 JEDEC Basic Flash Parameter Table: 11th DWORD (cont'd)

Bits	Description
13:8	**Page Program Typical time** Time the device *typically* takes to write a full page. User must poll device busy to determine if the operation has completed. The user may scale this by ½ or ¼ to determine approximate times for ½ and ¼ page program operations 13 units (0: 8 µs, 1: 64 µs) 12:8 count Formula: typical page program time = (count + 1)*units The range is 8 µs to 2048 µs in two groups: 8 µs to 256 µs and 64 µs to 2048 µs
7:4	**Page Size** This field specifies 'N' and is used to calculate page size = 2^N bytes.
3:0	**Multiplier from typical time to max time for Page or byte program** 3:0 count Formula: maximum time = 2 * (count + 1)*typical time NOTE This multiplier applies to all page or byte typical program times. The maximum time is intended to be used as a watchdog timeout for an error or failure condition. Since a common scale factor is used across all program sizes, any particular maximum time may only approximate the datasheet maximum time.

6.4.15 JEDEC Basic Flash Parameter Table: 12th DWORD

Bits	Description
31	**Suspend / Resume supported** The device supports suspend and resume of both program and erase operations. 0: supported 1: not supported
30:24	**Suspend in-progress erase max latency** Maximum time required by the flash device to suspend an in-progress erase and be ready to accept another command which accesses the flash array. This time does not apply to the read status command. See also *Suspend in-progress program in this DWORD.* 30:29 units (00b: 128ns, 01b: 1µs, 10b: 8µs, 11b: 64µs) 28:24 count Formula: erase max latency = (count + 1)*units Example: if units =01b and count =19, then erase max latency = (19+1)*1 µs = 20 µs The range is 128 ns to 2048 µs in four groups: 128 ns to 4**.** 096 µs, 1 µs to 32 µs, 8 µs to 256 µs, 64 µs to 2048 µs
23:20	**Erase Resume to Suspend Interval** The device requires this typical amount of time to make progress on the erase before allowing another suspend. It is possible to immediately suspend again after a resume -- there is no required minimum time between resuming an operation and suspending the operation again. However, the device requires some average amount of active operation time, after a resume, to make progress on the operation, before another suspend. This parameter recommends an average interval of time that should be allowed between a resume and the next suspend in order for the operation to eventually complete. If there are some intervals less than the recommended value there should be a similar number of intervals that are longer than the recommended value. If the interval is consistently less than the recommended value the operation may never finish. 23:20 count of fixed units of 64µs Formula: erase resume to suspend interval = (count + 1)*64 µs Example: if count = 7, the erase resume to suspend interval = (7+1)*64 µs = 512 µs The range is 64 µs to 1024 µs
19:13	**Suspend in-progress program max latency** Maximum time required by the flash device to suspend an in-progress program and be ready to accept another command which accesses the flash array. This time does not apply to the read status command. See also *Suspend in-progress erase in this DWORD.* 19:18 units (00b: 128ns, 01b: 1µs, 10b: 8µs, 11b: 64µs) 17:13 count Formula: suspend in-progress program max latency = (count+1)*units Example: if units = 01b and count = 4, then suspend in-progress program max latency = (4+1)*1 µs = 5 µs The range is 128 ns to 2048 µs in four groups: 128 ns to 4.096 µs, 1 µs to 32 µs, 8 µs to 256 µs, and 64 µs to 2048 µs.

6.4.15 JEDEC Basic Flash Parameter Table: 12th DWORD (cont'd)

Bits	Description
12:9	**Program Resume to Suspend Interval** The device requires this typical amount of time to make progress on the program operation before allowing another suspend. It is possible to immediately suspend again after a resume -- there is no required minimum time between resuming an operation and suspending the operation again. However, the device requires some average amount of active operation time, after a resume, to make progress on the operation, before another suspend. This parameter recommends an average interval of time that should be allowed between a resume and the next suspend in order for the operation to eventually complete. If there are some intervals less than the recommended value there should be a similar number of intervals that are longer than the recommended value. If the interval is consistently less than the recommended value the operation may never finish. 12:9 count of fixed units of 64 µs Formula: program resume to suspend interval = (count + 1)*64 µs Example: if count = 15, the erase resume to suspend interval = (15+1)*64 µs = 1024 µs The range is 64 µs to 1024 µs
8	**Reserved**
7:4	**Prohibited Operations During Erase Suspend** xxx0b: May not initiate a new erase anywhere (erase nesting not permitted) xxx1b: May not initiate a new erase in the erase suspended erase type size xx0xb: May not initiate a page program anywhere xx1xb: May not initiate a page program in the erase suspended erase type size x0xxb: Refer to vendor datasheet for read restrictions x1xxb: May not initiate a read in the erase suspended erase type size 0xxxb: Additional erase or program restrictions apply 1xxxb: The erase and program restrictions in bits 5:4 are sufficient NOTE This list is not comprehensive. Consult the device datasheet for a full list of allowed and prohibited operations.
3:0	**Prohibited Operations During Program Suspend** xxx0b: May not initiate a new erase anywhere (erase nesting not permitted) xxx1b: May not initiate a new erase in the program suspended page size xx0xb: May not initiate a new page program anywhere (program nesting not permitted) xx1xb: May not initiate a new page program in the program suspended page size x0xxb: Refer to vendor datasheet for read restrictions x1xxb: May not initiate a read in the program suspended page size 0xxxb: Additional erase or program restrictions apply 1xxxb: The erase and program restrictions in bits 1:0 are sufficient NOTE This list is not comprehensive. Consult the device datasheet for a full list of allowed and prohibited operations.

6.4.16 JEDEC Basic Flash Parameter Table: 13th DWORD

Bits	Description
31:24	**Suspend Instruction** Instruction used to suspend a write or erase type operation.
23:16	**Resume Instruction** Instruction used to resume a write or erase type operation.
15:8	**Program Suspend Instruction** Instruction used to suspend a program operation. (If the device requires a unique instruction to suspend a "program" command then that instruction is listed here. Otherwise this field contains the same value as the "Suspend Instruction" field above.)
7:0	**Program Resume Instruction** Instruction used to resume a program operation. (If the device requires a unique instruction to resume a "program" command then that instruction is listed here. Otherwise this field contains the same value as the "Resume Instruction" field above.)

6.4.17 JEDEC Basic Flash Parameter Table: 14th DWORD

Bits	Description
31	**Deep Powerdown Supported** 0: supported 1: not supported
30:23	**Enter Deep Powerdown Instruction** Instruction used to enter deep powerdown
22:15	**Exit Deep Powerdown Instruction** Instruction used to exit deep powerdown
14:8	**Exit Deep Powerdown to next operation delay** Maximum time required by the flash device to exit Deep Powerdown and be ready to accept any command. (NOTE: Read status is not valid when exiting deep powerdown.) 14:13 units (00b: 128ns, 01b: 1µs, 10b: 8µs, 11b: 64µs) 12:8 count Formula: exit Deep Powerdown to next operation delay = (count+1)*units Example: if units = 10b and count = 4, then delay = (4+1)*8 µs = 40 µs The range is 128 ns to 2048 µs in four groups: 128 ns to 4.096 µs, 1 µs to 32 µs, 8 µs to 256 µs, and 64 µs to 2048 µs
7:2	**Status Register Polling Device Busy** This bit field defines various ways the flash device's busy status may be polled. A zero in a bit position indicates that the device does not support the particular polling method. 1x_xxxxb: Reserved x1_xxxxb: Reserved xx_1xxxb: Reserved xx_x1xxb: Reserved xx_xx1xb: Bit 7 of the Flag Status Register may be polled any time a Program, Erase, Suspend/Resume command is issued, or after a Reset command while the device is busy. The read instruction is 70h. Flag Status Register bit definitions: bit[7]: Program or erase controller status (0=busy; 1=ready) xx_xxx1b: Use of legacy polling is supported by reading the Status Register with 05h instruction and checking WIP bit[0] (0=ready; 1=busy).
1:0	**Reserved**

6.4.18 JEDEC Basic Flash Parameter Table: 15th DWORD

Bits	Description
31:24	**Reserved**
23	**HOLD or RESET Disable** Defines whether HOLD or RESET may be disabled via a configuration register If driving IO3 high during command phase HOLD or RESET do not need to be disabled. Device decodes instruction to determine functionality of HOLD/RESET vs. data 1: set bit 4 of the Non-volatile Extended Configuration Register = 0 to disable HOLD or RESET 0: above feature is not supported
22:20	**Quad Enable Requirements (QER)** This field describes whether the device contains a Quad Enable (QE) bit used to enable 1S-1S-4S and 1S-4S-4S quad read or quad program operations. If QE exists, this field also identifies the bit location and method to set/clear the bit. In this standard, status register 1 refers to the first data byte transferred on a Read Status (05h) or Write Status (01h) command. Status register 2 refers to the byte read using instruction 35h. Status register 2 is the second byte transferred in a Write Status (01h) command. Bits are numbered from 7 to 0, where bit 7 is transferred first on the wire. NOTE Industry naming and definitions of these status registers may differ. The user will typically perform a read-modify-write sequence of operations to maintain the state of all other writable status register bits. For example read both status registers, set/clear QE, Write Status with both data bytes. 000b: Device does not have a QE bit. Device may detect 1-1-4 and 1-4-4 commands based on their instruction. An IO3/HOLD# pin, if present, functions as hold during instruction input phase and an IO2/WP# pin, if present, functions as WP# during instruction input phase. 001b: QE is bit 1 of status register 2. It is set via Write Status with two data bytes where bit 1 of the second byte is one. It is cleared via Write Status with two data bytes where bit 1 of the second byte is zero. Writing only one byte to the status register has the side-effect of clearing status register 2, including the QE bit. The 100b code is used if writing one byte to the status register does not modify status register 2. 010b: QE is bit 6 of status register 1. It is set via Write Status with one data byte where bit 6 is one. It is cleared via Write Status with one data byte where bit 6 is zero. 011b: QE is bit 7 of status register 2. It is set via Write status register 2 instruction 3Eh with one data byte where bit 7 is one. It is cleared via Write status register 2 instruction 3Eh with one data byte where bit 7 is zero. The status register 2 is read using instruction 3Fh. 100b: QE is bit 1 of status register 2. It is set via Write Status with two data bytes where bit 1 of the second byte is one. It is cleared via Write Status with two data bytes where bit 1 of the second byte is zero. In contrast to the 001b code, writing one byte to the status register does not modify status register 2. 101b: QE is bit 1 of the status register 2. Status register 1 is read using Read Status instruction 05h. Status register 2 is read using instruction 35h. QE is set via Write Status instruction 01h with two data bytes where bit 1 of the second byte is one. It is cleared via Write Status with two data bytes where bit 1 of the second byte is zero. 110b: QE is bit 1 of the status register 2. Status register 1 is read using Read Status instruction 05h. Status register 2 is read using instruction 35h, and status register 3 is read using instruction 15h. QE is set via Write Status Register instruction 31h with one data byte where bit 1 is one. It is cleared via Write Status Register instruction 31h with one data byte where bit 1 is zero. 111b: Reserved
19:16	**0-4-4 Mode Entry Method** xxx1b: Mode Bits[7:0] = A5h NOTE: QE must be set prior to using this mode xx1xb: Read the 8-bit volatile configuration register with instruction 85h, set XIP bit[3] in the data read, and write the modified data using the instruction 81h, then Mode Bits [7:0] = 01h x1xxb: Mode Bit[7:0]=AXh 1xxxb: Reserved

6.4.18 JEDEC Basic Flash Parameter Table: 15th DWORD (cont'd)

Bits	Description
15:10	**0-4-4 Mode Exit Method** xx_xxx1b: Mode Bits[7:0] = 00h will terminate this mode at the end of the current read operation xx_xx1xb: If 3-Byte address active, input Fh on IO0-IO3 for 8 clocks. If 4-Byte address active, input Fh on IO0-IO3 for 10 clocks. This will terminate the mode prior to the next read operation. xx_x1xxb: Reserved xx_1xxxb: Input Fh (mode bit reset) on IO0-IO3 for 8 clocks. This will terminate the mode prior to the next read operation. x1_xxxxb: Mode Bit[7:0] ≠ AXh 1x_xxxxb: Reserved
9	**0-4-4 mode supported** This mode is variously referred to as implied instruction, continuous read, execute in place, etc. 0: not supported 1: supported
8:4	**4S-4S-4S mode enable sequences** This field describes the supported methods to enter 4S-4S-4S mode from 1S-1S-1S mode. x_xxx1b: set QE per QER description above, then issue instruction 38h x_xx1xb: issue instruction 38h x_x1xxb: issue instruction 35h x_1xxxb: device uses a read-modify-write sequence of operations: read configuration using instruction 65h followed by address 800003h, set bit 6, write configuration using instruction 71h followed by address 800003h. This configuration is volatile. 1_xxxxb: **4S-4S-4S mode enable sequences** Device uses a read-modify-write sequence of operations: Read Volatile Enhanced Configuration Register using instruction 65h, no address is required, reset bit 7 to 0. Write Volatile Enhanced Configuration Register using instruction 61h, no address is required. This configuration is volatile. **4S-4S-4S mode disable sequences** device uses a read-modify-write sequence of operations: Read Volatile Enhanced Configuration Register using instruction 65h, no address is required, set bit 7 to 1. Write Volatile Enhanced Configuration Register using instruction 61h, no address is required. This configuration is volatile. NOTE If device is in 0-4-4 mode, then this mode must be exited before the 4S-4S-4S enable sequence is issued.
3:0	**4S-4S-4S mode disable sequences** This field describes the supported methods to exit 4S-4S-4S mode. xxx1b: issue FFh instruction xx1xb: issue F5h instruction x1xxb: device uses a read-modify-write sequence of operations: read configuration using instruction 65h followed by address 800003h, clear bit 6, write configuration using instruction 71h followed by address 800003h. This configuration is volatile. 1xxxb: issue the Soft Reset 66/99 sequence, see 6.4.19, 16th DWORD bits[13:8] NOTE If device is in 0-4-4 mode, then this mode must be exited before the 4S-4S-4S disable sequence is issued.

6.4.19 JEDEC Basic Flash Parameter Table: 16th DWORD

Bits	Description
31:24	**Enter 4-Byte Addressing** This field defines the supported methods to enter 4-byte addressing mode or to use an extended address register with 3-byte addressing to access memory above 16 MBytes. xxxx_xxx1b: issue instruction B7h (preceding write enable not required) xxxx_xx1xb: issue write enable instruction 06h, then issue instruction B7h xxxx_x1xxb: 8-bit volatile extended address register used to define A[31:24] bits. Read with instruction C8h. Write instruction is C5h with 1 byte of data. Select the active 128 Mbit memory segment by setting the appropriate A[31:24] bits and use 3-Byte addressing. xxxx_1xxxb: 8-bit volatile bank register used to define A[30:A24] bits. MSB (bit[7]) is used to enable/disable 4-byte address mode. When MSB is set to '1', 4-byte address mode is active and A[30:24] bits are do not care. Read with instruction 16h. Write instruction is 17h with 1 byte of data. When MSB is cleared to '0', select the active 128 Mbit segment by setting the appropriate A[30:24] bits and use 3-Byte addressing. xxx1_xxxxb: A 16-bit nonvolatile configuration register controls 3-Byte/4-Byte address mode. Read instruction is B5h. Bit[0] controls address mode [0=3-Byte; 1=4-Byte]. Write configuration register instruction is B1h, data length is 2 bytes. xx1x_xxxxb: Supports dedicated 4-Byte address instruction set. Consult vendor data sheet for the instruction set definition. x1xx_xxxxb: Always operates in 4-Byte address mode 1xxx_xxxxb: Reserved
23:14	**Exit 4-Byte Addressing** xx_xxxx_xxx1b: issue instruction E9h to exit 4-Byte address mode (write enable instruction 06h is not required) xx_xxxx_xx1xb: issue write enable instruction 06h, then issue instruction E9h to exit 4-Byte address mode xx_xxxx_x1xxb: 8-bit volatile extended address register used to define A[31:A24] bits. Read with instruction C8h. Write instruction is C5h, data length is 1 byte. Return to lowest memory segment by setting A[31:24] to 00h and use 3-Byte addressing. xx_xxxx_1xxxb: 8-bit volatile bank register used to define A[30:A24] bits. MSB (bit[7]) is used to enable/disable 4-byte address mode. When MSB is cleared to '0', 3-byte address mode is active and A30:A24 are used to select the active 128 Mbit memory segment. Read with instruction 16h. Write instruction is 17h, data length is 1 byte. xx_xxx1_xxxxb: A 16-bit non-volatile configuration register controls 3-Byte/4-Byte address mode. Read instruction is B5h. Bit[0] controls address mode [0=3-Byte; 1=4-Byte]. Write configuration register instruction is B1h, data length is 2 bytes. xx_xx1x_xxxxb: Hardware reset xx_x1xx_xxxxb: Software reset (see bits 13:8 in this DWORD) xx_1xxx_xxxxb: Power cycle x1_xxxx_xxxxb: Reserved 1x_xxxx_xxxxb: Reserved

6.4.19 JEDEC Basic Flash Parameter Table: 16th DWORD (cont'd)

Bits	Description
13:8	**Soft Reset and Rescue Sequence Support** This field specifies how to return the device to its default power-on state. 00_0000b: no software reset instruction is supported xx_xxx1b: drive Fh on all 4 data wires for 8 clocks xx_xx1xb: drive Fh on all 4 data wires for 10 clocks if device is operating in 4-byte address mode xx_x1xxb: drive Fh on all 4 data wires for 16 clocks xx_1xxxb: issue instruction F0h x1_xxxxb: issue reset enable instruction 66h, then issue reset instruction 99h. The reset enable, reset sequence may be issued on 1, 2, 4, or 8 wires depending on the device operating mode. 1x_xxxxb: exit 0-4-4 mode is required prior to other reset sequences above if the device may be operating in this mode. See 6.4.18, 0-4-4 Mode Exit
7	**Reserved**
6:0	**Volatile or Non-volatile Register and Write Enable Instruction for Status Register 1** The instruction 01h is typically used to write status register 1 which contains Block Protection (BP) and other bits. Status register 1 is written by the first data byte following the instruction 01h. The protection bits must be written to zero to enable writes/erases to the device. This field describes how to modify the writable bits in status register 1 in either a volatile or non-volatile manner. Bits 1:0 in status register 1 are de-facto standard write enable and busy status and are excluded from the definitions below. xxx_xxx1b: Non-volatile Status Register 1, powers-up to last written value, use instruction 06h to enable write xxx_xx1xb: Volatile Status Register 1, status register powers-up with bits set to "1"s, use instruction 06h to enable write xxx_x1xxb: Volatile Status Register 1, status register powers-up with bits set to "1"s, use instruction 50h to enable write xxx_1xxxb: Non-volatile/Volatile status register 1 powers-up to last written value in the non-volatile status register, use instruction 06h to enable write to non-volatile status register. Volatile status register may be activated after power-up to override the non-volatile status register, use instruction 50h to enable write and activate the volatile status register. xx1_xxxxb: Status Register 1 contains a mix of volatile and non-volatile bits. The 06h instruction is used to enable writing of the register. x1x_xxxxb: Reserved 1xx_xxxxb: Reserved NOTE If the status register is read-only then this field will contain all zeros in bits 4:0.

6.4.20 JEDEC Basic Flash Parameter Table: 17th DWORD

Bits	Description
31:24	**(1S-1S-8S) Fast Read Instruction** Instruction for single input instruction and address and octal output data Fast Read. If this field is 0x00, (1S-1S-8S) Fast Read is not supported
23:21	**(1S-1S-8S) Fast Read Number of Mode Clocks** This field will be 000b if Mode Bits are not supported. NOTE This field should be counted in clocks not number of bits received by the serial flash. The initiator drives the bus during "mode bits" cycles; the initiator tri-states the bus during "dummy" cycles. **Example:** If 4 mode bits are needed with a single input address phase command, this field would be 100b.
20:16	**(1S-1S-8S) Fast Read Number of Wait states (dummy clocks) needed before valid output** This field will be 00000b if wait states/dummy clocks are not supported. (The number of dummy clocks should be > 0 to avoid contention on bi-directional pins.)
15:8	**(1S-8S-8S) Fast Read Instruction** Instruction for single input instruction, octal input address, and octal output data Fast Read. If this field is 0x00, (1S-8S-8S) Fast Read is not supported
7:5	**(1S-8S-8S) Fast Read Number of Mode Clocks** This field will be 000b if Mode bits are not supported. NOTE This field should be counted in clocks not number of bits received by the serial flash. The initiator drives the bus during "mode bits" cycles; the initiator tri-states the bus during "dummy" cycles. **Example:** If 8 mode bits are needed with a octal input address phase command, this field would be 001b.
4:0	**(1S-8S-8S) Fast Read Number of Wait states (dummy clocks) needed before valid output** This field will be 00000b if wait states/dummy clocks are not supported. (The number of dummy clocks should be > 0 to avoid contention on bi-directional pins.)

6.4.21 JEDEC Basic Flash Parameter Table: 18th DWORD

Bits	Description
31	**Byte Order in 8D-8D-8D mode** 0b: Byte order of 16-bit words is the same when read in 1S-1S-1S mode and 8D-8D-8D mode. 1b: Byte order of 16-bit words is swapped when read in 8D-8D-8D mode compared to 1S-1S-1S mode.
30-29	**Octal DTR (8D-8D-8D) Command and Command Extension** 00b: The Command Extension is the same as the Command. (The Command / Command Extension has the same value for the whole clock period.) 01b: Command Extension is the inverse of the Command. The Command Extension acts as a confirmation of the Command 10b: Reserved 11b: Command and Command Extension forms a 16 bit command word.
28	**Reserved. Leave as "0".** (This allows new features to be added to these bits in the future.)
27	**Data Strobe support for QPI DTR mode (4S-4D-4D)** 0b: DS is not supported for QPI DTR mode 1b: DS is supported for QPI DTR mode
26	**Data Strobe support for QPI STR mode (4S-4S-4S)** 0b: DS is not supported for QPI STR mode 1b: DS is supported for QPI STR mode
25:24	**Data Strobe Waveforms in STR Mode** 11b: First rising edge of DS half a clock cycle before the start of the first data bit, start of first data bit aligned with the first falling edge of DS, first rising edge of DS follows a rising edge of CK, as shown in Figure 18 10b: First rising edge of DS in the middle of the first data bit, start of second data bit aligned with the first falling edge of DS, first rising edge of DS follows a Rising edge of CK, as shown in Figure 19. 01b: Start of first data bit aligned with the first rising edge of DS, first rising edge of DS follows a falling edge of CK, as shown in Figure 20 00b: Reserved
23	**JEDEC SPI Protocol Reset (In-Band Reset)** 0: JEDEC SPI Protocol Reset NOT implemented 1: JEDEC SPI Protocol Reset implemented as described in JESD252.
22:18	**Variable Output Driver Strength** Mainly used for devices supporting the xSPI spec, but may also be used for other devices. See the xSPI spec for definition of driver strengths. See Clause 6.10.28 for a description of the control bits used to select driver type. 00000b: Not supported xxxx1: Driver Type 0 Supported (This option is required for devices supporting the xSPI spec) xxx1x: Driver Type 1 Supported xx1xx: Driver Type 2 Supported x1xxx: Driver Type 3 Supported 1xxxx: Driver Type 4 Supported
17:0	**Reserved. Leave as "0".** (This allows new features to be added to these bits in the future.)

6.4.21 JEDEC Basic Flash Parameter Table: 18th DWORD (cont'd)

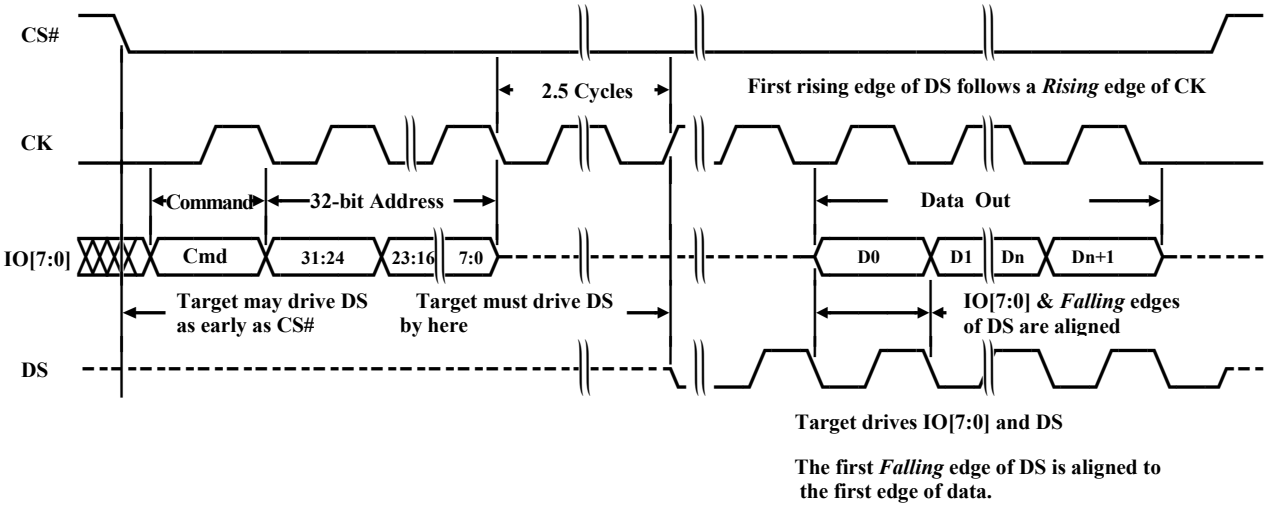


Figure 18 — Data Strobe Waveforms in STR Mode – Option 11b

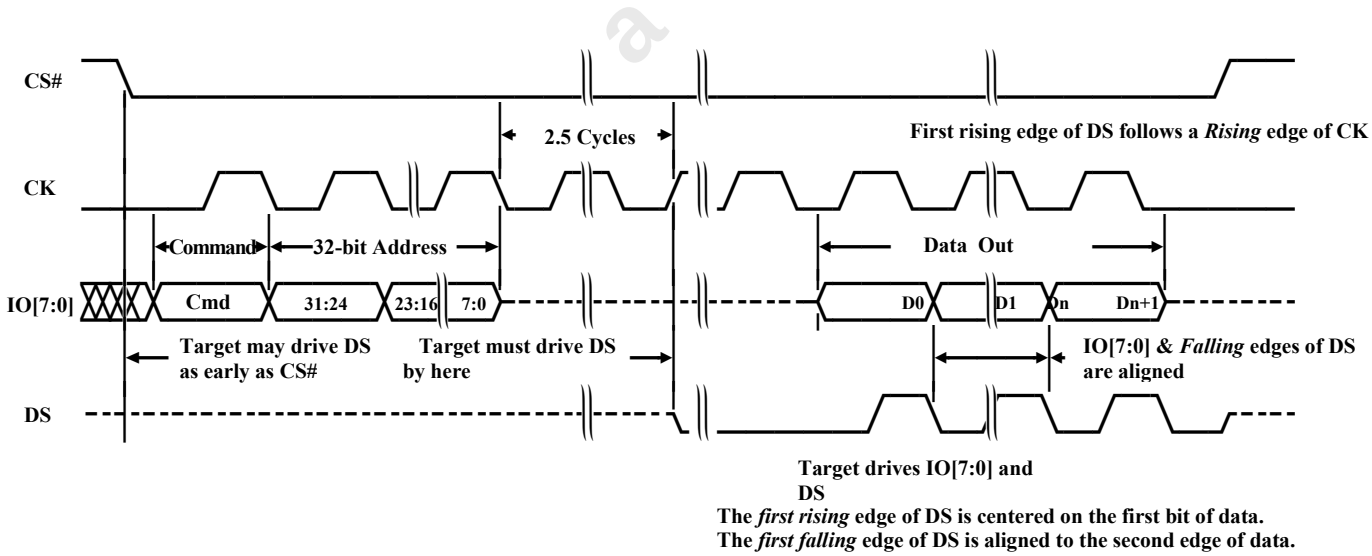


Figure 19 — Data Strobe Waveforms in STR Mode - Option 10b

6.4.21 JEDEC Basic Flash Parameter Table: 18th DWORD (cont'd)

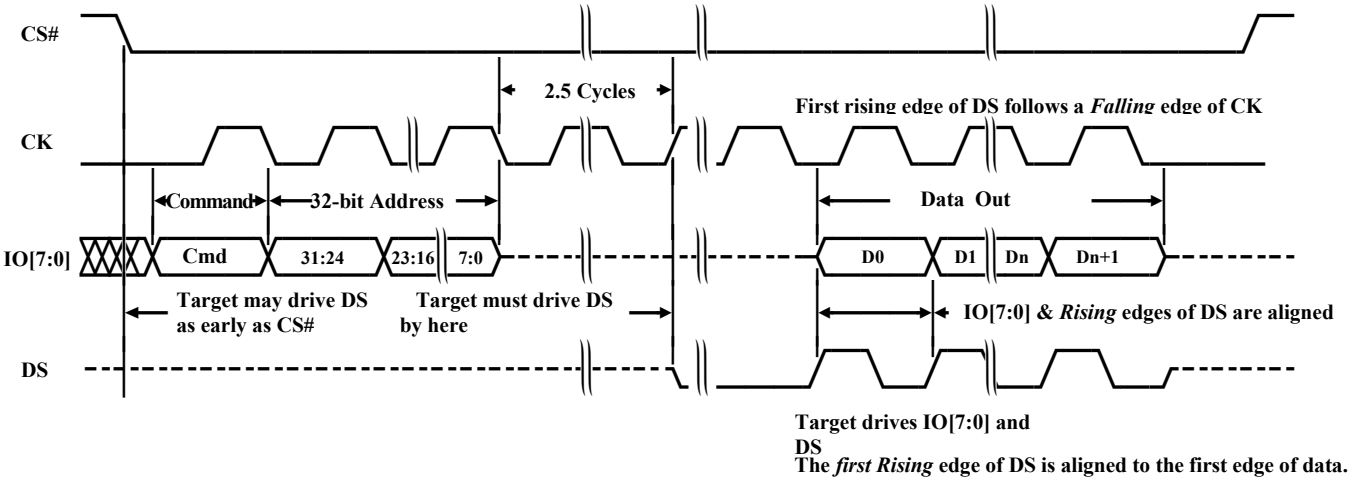


Figure 20 — Data Strobe Waveforms in STR Mode - Option 01b

6.4.22 JEDEC Basic Flash Parameter Table: 19th DWORD

Bits	Description
31:23	**Reserved. Leave as "0".** (This allows new features to be added to these bits in the future.)
22:20	**Octal Enable Requirements** This field describes whether the device contains an Octal Enable bit used to enable octal protocols; e.g., 1S-1S-8S and 1S-8S-8S. If Octal Enable exists, this field also identifies the bit location and method to set/clear the bit. The methods used for accessing Status/Configuration Registers differ between vendors, and are therefore described in detail. NOTE Industry naming and definitions of these status registers may differ. The user will typically perform a read-modify-write sequence of operations to maintain the state of all other writable status register bits. For example read both status registers, set/clear Octal Enable, Write Status with both data bytes. 000b: Device does not have an Octal Enable bit. If Octal protocols are supported, IO2-IO7 pins are available only for address or data transfer. 001b: Octal Enable is bit 3 of status register 2. It is set via Write status register 2 instruction 31h with one data byte where bit 3 is one. It is cleared via Write status register 2 instruction 3Eh with one data byte where bit 3 is zero. The status register 2 is read using instruction 65h with address byte 02h and one dummy byte. 010b: Octal enable bit is the same as Quad Enable bit, enabling use of IO2-IO7 pins for address or data transfer. Refer to Quad Enable Requirements (QER), at DWORD 15. Other: Reserved
19:16	**0-8-8 Mode Entry Method** 0000b: Device does not support 0-8-8 mode xxx1b: Read the 8-bit volatile configuration register with instruction 85h, set XIP bit[0] in the data read, and write the modified data using the instruction 81h, then Mode Bits [7:0] = 01h 001xb: XIP Mode Enable bit is located at addressable register (VR/NVR) at address 06h, bit [0]. If this bit is set to '0' (XiP Mode Enabled), the next Fast-Read instruction carries the XiP Mode bit (XMb) on IO0 of the first Dummy Cycle following the address. This is equivalent to bit [0] for Octal, [4] for Quad and [7] for Single, of the Mode-Byte, i.e. the first byte sent after the Address field. When XMb is set to '0', the device enters XiP mode and the next instruction will skip the OpCode (Command Phase). Refer to GRAM SFDP Table for methods to access the addressable registers. 010xb: XIP Mode Enable bit is located at addressable register (VR/NVR) at address 06h, bit [0]. If this bit is set to '0' (XiP Mode Enabled), the next Fast-Read instruction carries the XiP Mode bits (XMb) on IO1 and IO0 during the first Dummy Cycle following the address. This is equivalent to bit [1:0] for Octal, [5:4] for Quad and [7:6] for Single, of the Mode-Byte, i.e. the first byte sent after the Address field. When XMb is set to '10b', the device enters XiP mode and the next instruction will skip the OpCode (Command Phase). Refer to GRAM SFDP Table for methods to access the addressable registers. Other: Reserved (0).

6.4.22 JEDEC Basic Flash Parameter Table: 19th DWORD (cont'd)

Bits	Description
15:10	**0-8-8 Mode Exit Method** 00_0000b: Device does not support 0-8-8 mode xx_xxx1b: Mode Bits[7:0] = 00h will terminate this mode at the end of the current read operation xx_xx1xb: If 3-Byte address active, input FFh on DQ0-DQ7 for 4 clocks. If 4-Byte address active, input FFh on DQ0-DQ7 for 5 clocks. This will terminate the mode prior to the next read operation. x0_01xxb: When XMb is set to '1b' or '11b' the device exits XiP mode, the XIP Mode Enable register is reset to '1' (XiP Mode is disabled) and the next Fast-Read instruction will include an OpCode (Command Phase). x0_10xxb: When XMb is set to '1b' or '11b' the device exits XiP mode, the XIP Mode Enable register remains unchanged (XiP Mode remains **enabled**) and the next Fast-Read instruction will include an OpCode (Command Phase) and XMb on its Mode Bits (i.e. XiP mode can be reentered by setting the XMb to '0b' or '10b', as defined for 0-8-8 Mode Entry Method). Other: Reserved (0)
9	**0-8-8 Mode Supported** This mode is variously referred to as implied instruction, continuous read, execute in place, etc. 0: not supported 1: supported
8:4	**8s-8s-8s Mode Enable Sequences** This field describes the supported methods to enter 8-8-8 mode from 1S-1S-1S mode. x_xx1xb: Issue instruction 06h (WREN), then issue instruction E8h x_x1xxb: Issue instruction 06h (WREN), then issue instruction 72h (Write CFG Reg 2), Address = 00000000h, Data = 01h (8S-8S-8S) or 02h (8D-8D-8D) 0_1xx0b: 8s-8s-8s is entered by writing EFh to addressable register at address 00h. Refer to GRAM SFDP Table for methods to access the addressable registers. 1_0xx0b: 8s-8s-8s is entered by writing B7h to addressable register at address 00h. Refer to GRAM SFDP Table for methods to access the addressable registers. Other: Reserved (0)
3:0	**8s-8s-8s Mode Disable Sequences** This field describes the supported methods to exit 8-8-8 mode. xxx1b: Issue instruction 06h (WREN), then issue FFh instruction 1xxxb: Issue the Soft Reset 66/99 sequence, see 6.4.19, 16th DWORD bits[13:8]. This will revert the device to its default settings (as defined by its non-volatile configuration registers). x10xb: 1s-1s-1s is entered by writing FFh to addressable register at address 00h. Refer to GRAM SFDP Table for methods to access the addressable registers. Other: Reserved (0)

6.4.23 JEDEC Basic Flash Parameter Table: 20th DWORD

Bits	Description
31:28	**Maximum operation speed of device in 8D-8D-8D mode when utilizing Data Strobe** 1111b: 8D-8D-8D mode using Data Strobe is not supported 1110b: 8D-8D-8D mode using Data Strobe is not characterized 1010b: Reserved 1100b: 400 MHz* 1011b: 333 MHz* 1010b: 266 MHz* 1001b: 250 MHz* 1000b: 200 MHz 0111b: 166 MHz 0110b: 133 MHz 0101b: 100 MHz 0100b: 80 MHz 0011b: 66 MHz 0010b: 50 MHz 0001b: 33 MHz 0000b: Reserved * Operation faster than 200 MHz is not part of the current xSPI Spec. However, this does not prevent vendors from making devices that operate at higher speed.
27:24	**Maximum operation speed of device in 8D-8D-8D mode when not utilizing Data Strobe** 1111b: 8D-8D-8D mode without using Data Strobe is not supported 1110b: 8D-8D-8D mode without using Data Strobe is not characterized 1010b: Reserved 1100b: 400 MHz* 1011b: 333 MHz* 1010b: 266 MHz* 1001b: 250 MHz* 1000b: 200 MHz 0111b: 166 MHz 0110b: 133 MHz 0101b: 100 MHz 0100b: 80 MHz 0011b: 66 MHz 0010b: 50 MHz 0001b: 33 MHz 0000b: Reserved
23:20	**Maximum operation speed of device in 8S-8S-8S mode when utilizing Data Strobe** 1111b: 8S-8S-8S mode using Data Strobe is not supported 1110b: 8S-8S-8S mode using Data Strobe is not characterized 1010b: Reserved 1100b: 400 MHz 1011b: 333 MHz 1010b: 266 MHz 1001b: 250 MHz 1000b: 200 MHz 0111b: 166 MHz 0110b: 133 MHz 0101b: 100 MHz 0100b: 80 MHz 0011b: 66 MHz 0010b: 50 MHz 0001b: 33 MHz 0000b: Reserved

6.4.23 JEDEC Basic Flash Parameter Table: 20th DWORD (cont'd)

Bits	Description
19:16	**Maximum operation speed of device in 8S-8S-8S mode when not utilizing Data Strobe** 1111b: 8S-8S-8S mode without using Data Strobe is not supported 1110b: 8S-8S-8S mode without using Data Strobe is not characterized 1010b: Reserved 1100b: 400 MHz* 1011b: 333 MHz* 1010b: 266 MHz* 1001b: 250 MHz* 1000b: 200 MHz 0111b: 166 MHz 0110b: 133 MHz 0101b: 100 MHz 0100b: 80 MHz 0011b: 66 MHz 0010b: 50 MHz 0001b: 33 MHz 0000b: Reserved
15:12	**Maximum operation speed of device in 4S-4D-4D mode when utilizing Data Strobe** 1111b: 4S-4D-4D mode using Data Strobe is not supported 1110b: 4S-4D-4D mode using Data Strobe is not characterized 1010b: Reserved 1100b: 400 MHz 1011b: 333 MHz 1010b: 266 MHz 1001b: 250 MHz 1000b: 200 MHz 0111b: 166 MHz 0110b: 133 MHz 0101b: 100 MHz 0100b: 80 MHz 0011b: 66 MHz 0010b: 50 MHz 0001b: 33 MHz 0000b: Reserved
11:8	**Maximum operation speed of device in 4S-4D-4D mode when not utilizing Data Strobe** 1111b: 4S-4D-4D mode without using Data Strobe is not supported 1110b: 4S-4D-4D mode without using Data Strobe is not characterized 1010b: Reserved 1100b: 400 MHz* 1011b: 333 MHz* 1010b: 266 MHz* 1001b: 250 MHz* 1000b: 200 MHz 0111b: 166 MHz 0110b: 133 MHz 0101b: 100 MHz 0100b: 80 MHz 0011b: 66 MHz 0010b: 50 MHz 0001b: 33 MHz 0000b: Reserved

6.4.23 JEDEC Basic Flash Parameter Table: 20th DWORD (cont'd)

Bits	Description
7:4	**Maximum operation speed of device in 4S-4S-4S mode when utilizing Data Strobe** 1111b: 4S-4S-4S mode using Data Strobe is not supported 1110b: 4S-4S-4S mode using Data Strobe is not characterized 1010b - 1000b: Reserved 0111b: 166 MHz 0110b: 133 MHz 0101b: 100 MHz 0100b: 80 MHz 0011b: 66 MHz 0010b: 50 MHz 0001b: 33 MHz 0000b: Reserved
3:0	**Maximum operation speed of device in 4S-4S-4S mode when not utilizing Data Strobe** 1111b: 4S-4S-4S mode without using Data Strobe is not supported 1110b: 4S-4S-4S mode without using Data Strobe is not characterized 1010b: Reserved 1100b: 400 MHz* 1011b: 333 MHz* 1010b: 266 MHz* 1001b: 250 MHz* 1000b: 200 MHz 0111b: 166 MHz 0110b: 133 MHz 0101b: 100 MHz 0100b: 80 MHz 0011b: 66 MHz 0010b: 50 MHz 0001b: 33 MHz 0000b: Reserved

6.4.24 JEDEC Basic Flash Parameter Table: 21st DWORD

Bits	Description
31:4	**Reserved. These bits default to all 0's**
3	**Supports (4S-4D-4D) Fast Read** Device supports Quad input instruction and address and quad output data Fast Read. 0: (4S-4D-4D) Fast Read NOT supported. 1: (4S-4D-4D) Fast Read supported.
2	**Supports (1S-4D-4D) Fast Read** Device supports Quad input instruction and address and quad output data Fast Read. 0: (1S-4D-4D) Fast Read NOT supported. 1: (1S-4D-4D) Fast Read supported.
1	**Supports (1S-2D-2D) Fast Read** Device supports Quad input instruction and address and quad output data Fast Read. 0: (1S-2D-2D) Fast Read NOT supported. 1: (1S-2D-2D) Fast Read supported.
0	**Supports (1S-1D-1D) Fast Read** Device supports Quad input instruction and address and quad output data Fast Read. 0: (1S-1D-1D) Fast Read NOT supported. 1: (1S-1D-1D) Fast Read supported.

6.4.25 JEDEC Basic Flash Parameter Table: 22nd DWORD

Bits	Description
31:24	**(1S-2D-2D) Fast Read Instruction DTR** Instruction for quad input instruction and address, quad output data Fast Read DTR.
23:21	**(1S-2D-2D) Fast Read Number of Mode Clocks** This field will be 000b if Mode bits are not supported, NOTE This field should be counted in clocks not number of bits received by the serial flash. The initiator drives the bus during "mode bits" cycles; the initiator tri-states the bus during "dummy" cycles. **Example:** If 8 mode bits are needed with a (1S-2D-2D) Fast Read phase command, this field would be 010b.
20:16	**1S-2D-2D) Fast Read Number of Wait states (dummy clocks) needed before valid output** This field will be 00000b if wait states/dummy clocks are not supported. (The number of dummy clocks should be > 0 to avoid contention on bi-directional pins.)
15:8	**(1S-1D-1D) Fast Read Instruction** Instruction for quad input instruction/address, quad output data Fast Read.
7:5	**(1S-1D-1D) Fast Read Number of Mode Clocks** This field will be 000b if Mode bits are not supported, NOTE This field should be counted in clocks not number of bits received by the serial flash. The initiator drives the bus during "mode bits" cycles; the initiator tri-states the bus during "dummy" cycles. **Example:** If 8 mode bits are needed with a (1S-1D-1D) Fast Read phase command, this field would be 100b. (1-bit on rising edge and 1-bit on falling edge of clock)
4:0	**(1S-1D-1D) Fast Read Number of Wait states (dummy clocks) needed before valid output** This field will be 00000b if wait states/dummy clocks are not supported. (The number of dummy clocks should be > 0 to avoid contention on bi-directional pins.)

6.4.26 JEDEC Basic Flash Parameter Table: 23rd DWORD

Bits	Description
31:24	**(4S-4D-4D) Fast Read Instruction** Instruction for quad input instruction/address, quad output data Fast Read.
23:21	**(4S-4D-4D) Fast Read Number of Mode Clocks** This field will be 000b if Mode bits are not supported, NOTE This field should be counted in clocks not number of bits received by the serial flash. The initiator drives the bus during "mode bits" cycles; the initiator tri-states the bus during "dummy" cycles. **Example:** If 8 mode bits are needed with a (4S-4D-4D) Fast Read phase command, this field would be 001b. (4-bits on rising edge and 4-bits falling edge of clock)
20:16	**(4S-4D-4D) Fast Read Number of Wait states (dummy clocks) needed before valid output** This field will be 00000b if wait states/dummy clocks are not supported. (The number of dummy clocks should be > 0 to avoid contention on bi-directional pins.)
15:8	**(1S-4D-4D) Fast Read Instruction DTR** Instruction for quad input instruction and address, quad output data Fast Read DTR.
7:5	**(1S-4D-4D) Fast Read Number of Mode Clocks** This field will be 000b if Mode bits are not supported, NOTE This field should be counted in clocks not number of bits received by the serial flash. The initiator drives the bus during "mode bits" cycles; the initiator tri-states the bus during "dummy" cycles. **Example:** If 8 mode bits are needed with a (1S-4D-4D) Fast Read phase command, this field would be 001b. (4-bits rising edge and 4-bits falling edge of clock)
4:0	**1S-4D-4D) Fast Read Number of Wait states (dummy clocks) needed before valid output** This field will be 00000b if wait states/dummy clocks are not supported. (The number of dummy clocks should be > 0 to avoid contention on bi-directional pins.)

6.5 JEDEC Sector Map Parameter Header and Table

A sector is the minimum size and alignment (granularity) of an area that can be erased in the data array of a flash memory device. Different areas within the address range of the data array may have a different minimum erase granularity (sector size).

The Sector Map Parameter Table identifies the location and size of sectors within the main data array of the flash memory device and identifies which Erase Types are supported by each sector. This table is required when a memory device:

- Has sectors of more than one size, or
- does not allow all Erase Type commands to be applied to all sectors.

When there is more than one sector size in a device, each contiguous group of sectors, that are of the same size, and support the same erase types, is called a region. A region may be as small as a single sector. There are one or more regions for each sector size. There is more than one region of a particular sector size when that sector size appears in more than one area of the address space and these areas are separated by one or more regions of a different sector size. For example: a region of 4KB sectors, followed by a region of 64KB sectors, followed by a region of 4KB sectors.

There may also be more than one region of the same size sector when the regions support different sets of Erase Types. For example: one region of 4KB sectors may support use of Erase Types for 4KB erase and 64KB erase but not 8KB erase or 32KB erase and an adjacent region of 4KB sectors may support all these Erase Types. The Sector Map Parameter Table is used to identify which Erase Type commands may be used within each region.

There may be more than one possible map of sector size, location, or Erase Type support. For example: a memory device may be user configurable to have some small sectors at the top or at the bottom of the address space, with all remaining sectors being a larger size. Because the small sectors may appear at either the top or the bottom of the address space, two sector maps are needed to describe the top or bottom location and size of the smaller sectors.

If there is more than one user selected sector map (configuration), this table includes the definition of instructions needed to determine which sector map configuration is in use. The number of sector map configuration detection commands is variable, the number of configurations is variable, and the number of regions in each configuration is variable, thus the size of this table is variable.

6.5.1 Sector Map Parameter Header: 1st DWORD

Bits	Description
31:24	**Parameter Table Length** This field specifies how many DWORDs are in the Parameter table. NOTE This field is 1's based. Therefore, 1 indicates 1 DWORD.
23:16	**Parameter Table Major Revision Number** This 8-bit field indicates the major revision number of the Sector Map parameter table. The value in this field is 01h for this table defined by JESD216E revision (unchanged from JESD216D revision). NOTE The Major Revision of JEDEC defined parameter tables can only be modified by updates to this standard.
15:8	**Parameter Table Minor Revision Number** This 8-bit field indicates the minor revision number of the Sector Map parameter table. The value in this field is 00h for this table defined by JESD216E revision (unchanged from JESD216D revision). NOTE The Minor Revision of the JEDEC owned parameter tables can only be modified by updates to this standard.
7:0	**Parameter ID LSB** The Sector Map Function Specific Table is assigned the ID LSB of 81h.

6.5.2 Sector Map Parameter Header: 2nd DWORD

Bits	Description
31:24	**Parameter ID MSB** The Sector Map Function Specific Table is assigned the ID MSB of FFh.
23:0	**Parameter Table Pointer (PTP)** This address specifies the start of this header's Parameter Table in the SFDP structure. The address is in terms of bytes and must be DWORD-aligned.

The Sector Map table is built from a sequence of descriptors. There are two types of descriptors:

- A configuration detection command descriptor (command), and
- A configuration sector map descriptor (map).

The command descriptors are optional. If there is a single configuration then no command descriptors are needed. If there are more than two configurations, more than one command descriptor is needed. If command descriptors are provided, they always precede map descriptors in the table.

Each configuration detection command is described by two Dwords. These Dwords provide:

- A bit indicating that the descriptor is a configuration detection command,
- a bit indicating whether this descriptor is the last command descriptor,
- the instruction code for the command,
- the number of address bytes for the command,
- the number of read latency cycles between the last address byte and the read data byte,
- a mask to select the bit of interest in the returned data byte, and
- the address value for the command.

It is assumed that each command is reading a configuration register with a single byte of return data and that this type of command does not provide mode bits. Each command selects a single bit from the byte of returned data. There will be a separate command descriptor and command sent for each bit of configuration selecting information that is needed to select the current Sector Map Configuration that is in use.

6.5.3 Configuration Detection Command Descriptor, 1st DWORD

Bits	Description
31:24	**Read data mask** Eight bit field with a single bit = 1. The 8 bit field is logically ANDed with the one byte of data read by the configuration detection command specified in this Dword. This bit field is used as a mask to select one bit from the data byte that is read.
23:22	**Configuration detection command address length** Two bit field that defines the length of the address used in the configuration detection command. 00b: No address in the command. 01b: 3 byte address. 10b: 4 byte address 11b: Variable address length (the current setting of the address length mode defines the address length) When the length is defined as variable, the software or hardware controlling the memory is aware of the address length mode last set in the memory device and this same length of address is used in sending the configuration detection command.
21:20	**Reserved** These bits default to all 1's.
19:16	**Configuration detection command read latency, in clock cycles** Four bit field indicating the number of cycles between the end of address and the beginning of returning read data. Range from 0 to 14 cycles of read latency (wait states). A value of Fh indicates the read latency is variable. The software or hardware controlling the memory is aware of the latency last set in the memory device and this same value is used in the configuration detection command.
15:8	**Detection command instruction.** Eight bit instruction for the sector map configuration detection command.
7:2	**Reserved** These bits default to all 1's.
1	**Descriptor Type** 0b: Command descriptor 1b: Map descriptor
0	**Descriptor Sequence End Indicator** 0b: Another descriptor of the same type follows this descriptor 1b: This is the last descriptor of this type.

6.5.4 Configuration Detection Command Descriptor, 2nd DWORD

Bits	Description
31:0	**Sector map configuration detection command address** Thirty two bit field providing up to 4 bytes of address. The number of address bytes in this field that are used by the command is determined by the address length in bits 23:22 of the first Dword.

The first DWORD of a command descriptor contains a field that identifies it as a command type descriptor. A single bit field in each command descriptor indicates whether it is the last command descriptor in the sequence. Each command descriptor defines the format of a command used to detect the value of one configuration bit in the memory device and has an eight bit mask value used to select a single bit from one data byte read by the command. The second DWORD of each command descriptor provides a 4 byte address that may optionally be used as part of the configuration detection command.

Each configuration bit value detected is part of the selection for the current configuration of the sector map. For example: if there are five to eight possible sector map configurations, at least three configuration detection commands will be needed to extract three bits of configuration selection information from the device in order to identify which configuration is currently in use. The configuration selector is limited to a maximum of 8 bits, allowing for a maximum of 256 possible configurations. However, there may not be a separate configuration needed for every possible value of the selector value. Each detected configuration bit is shifted left into the configuration selector value such that the last detected bit is in the least significant bit of the selector value. If there are no command descriptors provided, because there is a single configuration, the default value of the configuration selector is zero.

Each configuration map descriptor is described by two or more Dwords. These Dwords provide:

- A map header DWORD
  - A bit indicating that the descriptor is a sector map descriptor,
  - a bit indicating whether this descriptor is the last map descriptor,
  - a configuration ID,
  - a count of the regions in the map.
- A DWORD for each region in the map
  - A value indicating the size of the region,
  - bits that indicate which Erase Types are supported in the region.

6.5.5 Configuration Map Descriptor Header DWORD

Bits	Description
31:24	**Reserved** These bits default to all 1's.
23:16	**Region count** The number of following region DWORDs minus 1
15:8	**Configuration ID** A value compared with the configuration selector value to determine if this map descriptor is for the currently selected sector map.
7:2	**Reserved** These bits default to all 1's.
1	**Descriptor Type** 0b: Command descriptor 1b: Map descriptor
0	**Descriptor Sequence End Indicator** 0b: Another descriptor of the same type follows this descriptor 1b: This is the last descriptor of this type.

6.5.6 Region DWORD

Bits	Description
31:8	**Region size** Region size as a multiple (count) of 256 Byte units. The Region size value is zero based, so a region of 256 Bytes has a size value = 0. Region size value = (count - 1) Region size = (value +1) * 256 bytes
7:4	**Reserved** These bits default to all 1's.
3	**Erase Type 4** 1b: Erase Type 4 erase command is supported in this region 0b: Erase Type 4 erase command is not supported in this region
2	**Erase Type 3** 1b: Erase Type 3 erase command is supported in this region 0b: Erase Type 3 erase command is not supported in this region
1	**Erase Type 2** 1b: Erase Type 2 erase command is supported in this region 0b: Erase Type 2 erase command is not supported in this region
0	**Erase Type 1** 1b: Erase Type 1 erase command is supported in this region 0b: Erase Type 1 erase command is not supported in this region

6.5.6 Region DWORD (cont'd)

At least one map descriptor is required. The first DWORD of a map descriptor is the header for the map and contains a field that identifies it as a map type descriptor. A single bit field in each map descriptor header indicates whether it is the last map descriptor in the sequence. The map descriptor header has a configuration ID field that is matched against the configuration selector value. If the configuration selector matches the configuration ID, the rest of the map descriptor defines the current sector map in use. If the configuration values do not match, the next map descriptor is examined. If there are no more map descriptors and no configuration ID matched the configuration identifier, the sector address map is unknown.

The map descriptor header contains a count of the number of regions in the map. Each region is described by a following DWORD. Each region DWORD indicates the size of sectors in the region and the supported Erase Types for that region. The region count indicates the number of DWORDs to skip when looking for the next map descriptor.

The first region starts at location zero of the data array in the flash device. Each additional region starts at the next higher location than the size of the previous region**.**

6.5.7 Sector Map Parameter Table – Example 1

The memory device in the following example is 256Mbit density and has three user settable sector map configurations. Two configuration detection commands are used to read the sector map related configuration control bits from registers. While there are four possible combinations of the two control bits, only three combinations are valid and only three configuration maps are provided. The three configurations are:

- Eight 4Kbyte sectors at the low address end (bottom) of the device address space, with all other sectors being 64Kbytes in size. Only Erase Type 1 for 4Kbyte sectors are supported in the region of 4Kbyte sectors and only Erase Type 2 for 64Kbyte erase is supported in the region containing 64Kbyte sectors.
- Eight 4Kbyte sectors at the high address end (top) of the device address space, with all other sectors being 64Kbytes in size. Only Erase Type 1 for 4Kbyte sectors are supported in the region of 4Kbyte sectors and only Erase Type 2 for 64Kbyte erase is supported in the region containing 64Kbyte sectors.
- Uniform 64Kbyte sectors with only Erase Type 2 for 64Kbyte sectors supported.

6.5.7 Sector Map Parameter Table – Example 1 (cont'd)

DWORD	Bits				NOTES	
	31:24	23:16	15:8	7:0		
0	Read Data Mask = 00001000b = 08h	Instruction Format (Address length variable = 11b [2 bits] Reserved = 11b [2 bits] Latency cycles variable = 1111b [4 bits]) = FFh	Instruction = 65h	Reserved = 111111b Descriptor type = command = 0b Not the last command = 0b FCh	Configuration Detect Command 1 (2 DWORDs) Instruction 65h, variable address length, variable latency, address 00800004h, select bit 3.	Configuration Detection
1	Address Value = 00800004h					
2	Read Data Mask = 00000100b = 04h	Instruction Format (Address length zero = 00b [2 bits] Reserved = 11b [2bits] Latency cycles = 00000b [6 bits] = 20h	Instruction = 35h	Reserved = 111111b Descriptor type = command = 0b Last command = 1b FDh	Configuration Detect Command 2 (2 DWORDs) Instruction 35h, no address, zero latency, select bit 2.	
3	Address Value = FFFFFFFFh					

6.5.7 Sector Map Parameter Table – Example 1 (cont'd)

DWORD	Bits				NOTES	
	31:24	23:16	15:8	7:0		
4	Reserved = FFh	Region Count = 3 Regions = 02h	Configuration ID = 00h	Reserved = 111111b Descriptor type = map = 1b Last map = 0b FEh	Configuration Map Header	1st Configuration Address Map Bottom: 8x 4KB sectors at bottom, 1x overlaid 64KB sector at bottom, 511 uniform 64KB sectors
5	Region size as count-1 of 256 Byte units [24 bits] 8x 4KB sectors = 32KB, count = 32KB/256 = 128 value = count - 1 = 128 -1 = 127 = 00007Fh			Reserved = 1111b Supported Sector Type commands bit-field = 0001b Assuming 4KB sector type is assigned to sector type 1 F1h	<- Sector Region 0 only 4KB erase commands supported in this region	
6	Region size as count-1 of 256 Byte units [24 bits] 32KB region, count = 32KB/256 = 128 value = count - 1 = 128 -1 = 127 = 00007Fh			Reserved = 1111b Supported Sector Type commands bit-field = 0010b Assuming 64KB sector type is assigned to sector type 2 F2h	<- Sector Region 1 only 64KB erase commands supported in this region	
7	Region size as count-1 of 256 Byte units [24 bits] 511 x 64KB sectors, count = 33488896 B/256 = 130816 value = count - 1 = 130816 -1 = 130815 = 01FEFFh			Reserved = 1111b Supported Sector Type commands bit-field = 0010b Assuming 64KB sector type is assigned to sector type 2 F2h	<- Sector Region 2 only 64KB erase commands supported in this region	

6.5.7 Sector Map Parameter Table – Example 1 (cont'd)

8	Reserved = FFh	Region Count = 3 Regions = 02h	Configuration ID = 01h	Reserved = 111111b Descriptor type = map = 1b Last map = 0b FEh	Configuration Map Header	2nd Configuration Address Map Top: 511x uniform 64KB sectors, 1x overlaid 64KB sector, 8x 4KB sectors at top
9	Region size as count-1 of 256 Byte units [24 bits] 511 x 64KB sectors, count = 33488896 B/256 = 130816 value = count - 1 = 130816 -1 = 130815 = 01FEFFh			Reserved = 1111b Supported Sector Type commands bit-field = 0010b Assuming 64KB sector type is assigned to sector type 2 F2h	<- Sector Region 0 only 64KB erase commands supported in this region	
10	Region size as count-1 of 256 Byte units [24 bits] 32KB region, count = 32KB/256 = 128 value = count - 1 = 128 -1 = 127 = 00007Fh			Reserved = 1111b Supported Sector Type commands bit-field = 0010b Assuming 64KB sector type is assigned to sector type 2 F2h	<- Sector Region 1 only 64KB erase commands supported in this region	
11	Region size as count-1 of 256 Byte units [24 bits] 8x 4KB sectors = 32KB, count = 32KB/256 = 128 value = count - 1 = 128 -1 = 127 = 00007Fh			Reserved = 1111b Supported Sector Type commands bit-field = 0001b Assuming 4KB sector type is assigned to sector type 1 F1h	<- Sector Region 2 only 4KB erase commands supported in this region	
12	Reserved = FFh	Region Count = 1 Regions = 00h	Configuration ID = 02h	Reserved = 111111b Descriptor type = map = 1b Last map = 1b FFh	Configuration Map Header	3rd Configuration Address Map Uniform 64KB sectors
13	Region size as count-1 of 256 Byte units [24 bits] 512 x 64KB sectors, count = 32MB/256 = 131072 value = count - 1 = 131072 -1 = 131071 = 01FFFFh			Reserved = 1111b Supported Sector Type commands bit-field = 0010b Assuming 64KB sector type is assigned to sector type 2 F2h	<- Sector Region 0 only 64KB erase commands supported in this region	

6.5.8 Sector Map Parameter Table – Example 2

The memory device in the following example is 128Mbit density and has one sector map configuration. No configuration detection commands are needed because there is a single fixed sector map. The sector format is:

- Sixteen 4Kbyte sectors at the low address end (bottom) of the device address space, sixteen 4Kbyte sectors at the high address end (top) of the device address space, with all other sectors being 32Kbytes in size.

The Erase Types are defined as:

- Erase Type 1 = 4KB
- Erase Type 2 = 32KB
- Erase Type 3 = 64KB

All three Erase Types are supported in 4KB sector regions at the bottom and top of the address space. Only Erase Types 2 and 3 are supported in the region containing 32Kbyte sectors.

<table>
<tr><th rowspan="2">DWORD</th><th colspan="4">Bits</th><th colspan="2" rowspan="2">NOTES</th></tr>
<tr><th>31:24</th><th>23:16</th><th>15:8</th><th>7:0</th></tr>
<tr><td>1</td><td>Reserved =

FFh</td><td>Region Count = 3 Regions =

02h</td><td>Configuration ID =

00h</td><td>Reserved = 111111b
Descriptor type = map = 1b
Last map = 1b

FFh</td><td>Configuration Map Header</td><td rowspan="5">Configuration Address Map

Top and bottom 16x 4KB sectors, remainder uniform 32KB sector map</td></tr>
<tr><td>2</td><td colspan="3">Region size as count-1 of 256 Byte units [24 bits]
16x 4KB sectors = 64KB, count = 64KB/256 = 256
value = count - 1 = 256 -1 = 255 =

0000FFh</td><td>Reserved = 1111b
Supported Sector Type commands bit-field = 0111b

F7h</td><td><- Sector Region 0
4KB, 32KB, and 64KB supported in this region</td></tr>
<tr><td>3</td><td colspan="3">Region size as count-1 of 256 Byte units [24 bits]
16MB -128KB region, count = 16646144 B/256 = 65024
value = count - 1 = 65024 -1 = 65023 =

00FDFFh</td><td>Reserved = 1111b
Supported Sector Type commands bit-field = 0110b

F6h</td><td><- Sector Region 1
32KB and 64KB erase commands supported in this region</td></tr>
<tr><td>5</td><td colspan="3">Region size as count-1 of 256 Byte units [24 bits]
16x 4KB sectors = 64KB, count = 64KB/256 = 256
value = count - 1 = 256 -1 = 255 =

0000FFh</td><td>Reserved = 1111b
Supported Sector Type commands bit-field = 0111b

F7h</td><td><- Sector Region 2
4KB, 32KB, and 64KB supported in this region</td></tr>
</table>

6.6 Replay Protected Monotonic Counters (RPMC) Parameter Header and Table

The widely supported RPMC functionality has been adopted by JEDEC to control multiple non-volatile monotonic counters integrated into a serial flash device. RPMC allows cryptographically secure host access to the (typically four) monotonic counters using packets that include a signature. The signature is generated using an HMAC-SHA256 process that guarantees the authenticity of the transferred packet. The details of RPMC functionality are described in a separate JEDEC standard.

This SFDP standard (starting with JESD216E) describes critical characteristics that allows a host to successfully communicate with an RPMC enabled device.

6.6.1 Replay Protected Monotonic Counters Parameter Header: 1st DWORD

Bits	Description
31:24	**Parameter Table Length = 02h** This field specifies how many DWORDs are in the Parameter table. NOTE This field is 1's based. Therefore, 1 indicates 1 DWORD.
23:16	**Parameter Table Major Revision Number = 01h** This 8-bit field indicates the major revision number of the parameter table. The value in this field is 01h for this table newly defined by this JESD216E revision. NOTE The Major Revision of JEDEC defined parameter tables can only be modified by updates to this standard.
15:8	**Parameter Table Minor Revision Number = 00h** This 8-bit field indicates the minor revision number of the Sector Map parameter table. The value in this field is 00h for this table newly defined by this JESD216E revision. NOTE The Minor Revision of the JEDEC owned parameter tables can only be modified by updates to this standard.
7:0	**Parameter ID LSB = 03h** The RPMC Parameter Table is assigned the ID (LSB) of 03h.

6.6.2 Replay Protected Monotonic Counters Parameter Header: 2nd DWORD

Bits	Description
31:24	**Parameter ID MSB = FFh** The RPMC Parameter Table is assigned the ID (MSB) of FFh.
23:0	**Parameter Table Pointer (PTP)** = *manufacturer specified* This address specifies the start of this header's Parameter Table in the SFDP structure. The address is in terms of bytes and must be DWORD-aligned.

6.6.3 Replay Protected Monotonic Counters Parameter Table, 1st DWORD

Bits	Description
31:28	**RESERVED = Fh** Value must be Fh.
27:24	**Update Rate** = *manufacturer specified* Rate of update = 5 * (2**Update Rate) seconds
23:16	**RPMC Packet READ Command Opcode (OP2) =** *manufacturer specified*
15:8	**RPMC Packet WRITE Command Opcode (OP1) =** *manufacturer specified*
7:4	**Num Counters – 1 =** *manufacturer specified* Number of supported counters minus one. Suggested value is 3 (4 counters supported).
3	**RESERVED = 1b** Value must be 1b.
2	**Busy_Polling_Method =** *manufacturer specified* 0b: Poll for OP1 BUSY using OP2 Extended Status[0]. No OP1 Suspend State support. 1b: Poll for OP1 BUSY using Read Status (05h). Suspend State is supported.
1	**Monotonic Counter Size = 0b** 0b: Monotonic Counter size is 32 bits 1b: Reserved
0	**Flash Hardening =** *manufacturer specified* 0b: Flash Hardening is supported 1b: Flash Hardening is not supported

6.6.4 Replay Protected Monotonic Counters Parameter Table, 2nd DWORD

Bits	Description
31:24	**RESERVED = FFh** Value must be FFh.
23:16	**Write Counter Polling Long Delay =** *manufacturer specified* Write + one HMAC Operation + Typical Subsector Erase Time Suggested usage: Allows controller to conserve power to delay polling if the short delay is not sufficient for completion of the write operation. Bit[23]: reserved Bits[22:21]: units (00b=1ms, 01b=16ms, 10b=128ms, 11b=1s) Bits[20:16]: polling_long_delay_write_counter
15:8	**Write Counter Polling Short Delay** = *manufacturer specified* Worst Case Write + one HMAC operation, No Erase Time Suggest usage: Allows controller to conserve power by delaying polling Bit [15]: reserved Bits[14:13]: units (00b=1us, 01b=16us, 10b=128us, 11b=1ms Bits [12:8]: polling short delay write counter
7:0	**Read Counter Polling Delay** = manufacturer specified Typical case to calculate HMAC two times Suggested usage: Allows controller to conserve power by delaying polling for read monotonic counter or update HMAC register commands. Bit[7]: reserved Bits[6:5]: units (00b=1us, 01b=16us, 10b=128us, 11b=1ms) Bits[4:0]: polling delay read counter

6.7 JEDEC 4-byte Address Instruction Parameter Header and Table

Legacy SPI memory devices were limited to 128-Mbits (16-Mbytes) of address space by commands that provided only three bytes (24-bits) of address. Recent SPI memories that exceed 128-Mbits density provide various options for providing 4-bytes (32-bits) of address. One option is the use of commands that always provide 4-bytes of address. These commands in some cases have the same function as legacy 3-byte address commands but use a different instruction to indicate that 4-bytes of address follow the instruction. The 4-byte address instruction special function table indicates which 4-byte address command instructions are supported by the SPI memory. The table also provides the 4-byte address instructions for the four Erase Types defined in 8th DWORD of the Basic Flash Parameter Table. If a 4-byte address instruction is not supported for an Erase Type, the instruction for that type is shown in the table as FFh.

6.7.1 4-byte Address Instruction Parameter Header: 1st DWORD

Bits	Description
31:24	**Parameter Table Length** This field specifies how many DWORDs are in the Parameter table. NOTE This field is 1's based. Therefore, 1 indicates 1 DWORD.
23:16	**Parameter Table Major Revision Number** This 8-bit field indicates the major revision number of the parameter table. The value in this field is 01h for this table defined by JESD216E revision (unchanged from JESD216D revision). NOTE The Major Revision of JEDEC defined parameter tables can only be modified by updates to this standard.
15:8	**Parameter Table Minor Revision Number** This 8-bit field indicates the minor revision number of the Sector Map parameter table. The value in this field is 01h for this table defined by JESD216E revision (unchanged from JESD216D revision). NOTE The Minor Revision of the JEDEC owned parameter tables can only be modified by updates to this standard.
7:0	**Parameter ID LSB** 4-byte Address Instruction Table is assigned the ID LSB of 84h.

6.7.2 4-byte Address Instruction Parameter Header: 2nd DWORD

Bits	Description
31:24	**Parameter ID MSB** 4-byte Address Instruction Table is assigned the ID MSB of FFh.
23:0	**Parameter Table Pointer (PTP)** This address specifies the start of this header's Parameter Table in the SFDP structure. The address is in terms of bytes and must be DWORD-aligned.

6.7.3 4-byte Address Instruction Table, 1st DWORD

Bit	Description
31:25	**Reserved** (Reserved bits did not have a defined value in previous versions of this spec, they are left unused)
24	**Support for (1S-8S-8S) Page Program Command, *Instruction=8Eh*** 0: Not supported 1: Supported
23	**Support for (1S-1S-8S) Page Program Command, *Instruction=84h*** 0: Not supported 1: Supported
22	**Support for (1S-8D-8D) DTR_READ Command, *Instruction=FDh*** 0: Not supported 1: Supported
21	**Support for (1S-8S-8S) FAST_READ Command, *Instruction=CCh*** 0: Not supported 1: Supported
20	**Support for (1S-1S-8S) FAST_READ Command, *Instruction=7Ch*** 0: Not supported 1: Supported
19	**Support for non-volatile individual sector lock write command, *Instruction=E3h*** 0: Not supported 1: Supported
18	**Support for non-volatile individual sector lock read command, *Instruction=E2h*** 0: Not supported 1: Supported
17	**Support for volatile individual sector lock Write command, *Instruction=E1h*** 0: Not supported 1: Supported
16	**Support for volatile individual sector lock Read command, *Instruction=E0h*** 0: Not supported 1: Supported
15	**Support for (1S-4D-4D) DTR_Read Command, *Instruction=EEh*** 0: Not supported 1: Supported
14	**Support for (1S-2D-2D) DTR_Read Command, *Instruction=BEh*** 0: Not supported 1: Supported
13	**Support for (1S-1D-1D) DTR_Read Command, *Instruction=0Eh*** 0: Not supported 1: Supported

6.7.3 4-byte Address Instruction Table, 1st DWORD (cont'd)

Bit	Description
12	**Support for Erase Command – *Type 4 size, Instruction lookup in next Dword*** 0: Not supported 1: Supported
11	**Support for Erase Command – *Type 3 size, Instruction lookup in next Dword*** 0: Not supported 1: Supported
10	**Support for Erase Command – *Type 2 size, Instruction lookup in next Dword*** 0: Not supported 1: Supported
9	**Support for Erase Command – *Type 1 size, Instruction lookup in next Dword*** 0: Not supported 1: Supported
8	**Support for (1S-4S-4S) Page Program Command, *Instruction=3Eh*** 0: Not supported 1: Supported
7	**Support for (1S-1S-4S) Page Program Command, *Instruction=34h*** 0: Not supported 1: Supported
6	**Support for (1S-1S-1S) Page Program Command, *Instruction=12h*** 0: Not supported 1: Supported
5	**Support for (1S-4S-4)S FAST_READ Command, *Instruction=ECh*** 0: Not supported 1: Supported
4	**Support for (1S-1S-4S) FAST_READ Command, *Instruction=6Ch*** 0: Not supported 1: Supported
3	**Support for (1S-2S-2S) FAST_READ Command, *Instruction=BCh*** 0: Not supported 1: Supported
2	**Support for (1S-1S-2)S FAST_READ Command, *Instruction=3Ch*** 0: Not supported 1: Supported
1	**Support for (1S-1S-1S) FAST_READ Command, *Instruction=0Ch*** 0: Not supported 1: Supported
0	**Support for (1S-1S-1S) READ Command, *Instruction=13h*** 0: Not supported 1: Supported

6.7.4 4-byte Address Instruction Table, 2nd DWORD

NOTE (informative) Industry common usage is:

21h 4 kbyte erase
5Ch 32 kbyte erase
DCh 64 kbyte erase
DCh 256 kbyte erase

Bit	Description
31:24	**Instruction for Erase Type 4** Erase Type is defined in 9th DWORD of the Basic Flash Parameter Table
23:16	**Instruction for Erase Type 3** Erase Type is defined in 9th DWORD of the Basic Flash Parameter Table
15:8	**Instruction for Erase Type 2** Erase Type is defined in 8th DWORD of the Basic Flash Parameter Table
7:0	**Instruction for Erase Type 1** Erase Type is defined in 8th DWORD of the Basic Flash Parameter Table

6.8 JEDEC eXtended Serial Peripheral Interface (xSPI) Profile 1.0 Parameter Header and Table

See JESD251, eXpanded Serial Peripheral Interface (xSPI) for Non-volatile Memory Devices, Version 1 for details about this interface. This interface supports 2 profiles. Profile 1.0 is covered in 6.8, Profile 2.0 is covered in 6.9. A host controller may support both profiles; target devices will typically support only one of the profiles.

6.8.1 JEDEC xSPI (Profile 1.0) Parameter Header: 1st DWORD

Bits	Description
31:24	**Parameter Table Length** This field specifies how many DWORDs are in the Parameter table. For the JESD216F revision, this parameter table length is 6. NOTE JESD216D and JESD216E did not specify a length, which was an error the TG missed before publication. NOTE This field is 1's based. Therefore, 1 indicates 1 DWORD.
23:16	**Parameter Table Major Revision Number** This 8-bit field indicates the major revision number of the parameter table. The value in this field is 01h for this table defined by JESD216F revision (unchanged from JESD216D revision). NOTE The Major Revision of JEDEC defined parameter tables can only be modified by updates to this standard.
15:8	**Parameter Table Minor Revision Number** This 8-bit field indicates the minor revision number of the Sector Map parameter table. The value in this field is 01h for this table defined by JESD216F revision (incremented by 1 from the JESD216E version). NOTE The Minor Revision of the JEDEC owned parameter tables can only be modified by updates to this standard.
7:0	**Parameter ID LSB** The eXtended Serial Peripheral Interface (Profile 1) is assigned the ID LSB of 05h.

6.8.2 JEDEC xSPI (Profile 1.0) Parameter Header: 2nd DWORD

Bits	Description
31:24	**Parameter ID MSB** The eXtended Serial Peripheral Interface is assigned the ID MSB of FFh.
23:0	**Parameter Table Pointer (PTP)** This address specifies the start of this header's Parameter Table in the SFDP structure. The address is in terms of bytes and must be DWORD-aligned.

6.8.3 JEDEC xSPI (Profile 1.0) Parameter Table: 1st DWORD - Command Codes Used in 8D-8D-8D Protocol Mode

The commands listed here are those that have more than one option for Command Code listed in "Table 6-2 Profile 1.0 commands used in 8D-8D-8D protocol mode (required commands)" or in "Table 6 3 Profile 1.0 commands used in 8D-8D-8D protocol mode (optional commands)" in the xSPI standard.

The opcodes for the Erase commands are provided in 6.4.11 to 6.4.13, and are therefore not repeated here. For the optional commands that are not supported as indicated in 3rd DWORD below, the parameter fields in this DWORD are not applicable.

Bits	Description
31	**SFDP Command in 8D-8D-8D mode – Address Bytes** See Figure 5 0b: 32-bit address (For most devices, SFDP is still limited to a 24-bit address space. This means MSB is 0, and the 24 bit address is in the last 3 bytes) 1b: 24-bit address, left adjusted (24 bit address is in the first 3 bytes, LSB is 0)
30	**SFDP Command in 8D-8D-8D mode – Dummy Cycles** See Figure 5 0b: 8 1b: 20
29	**Number of Additional Modifier Bytes Used for Read Status Register command** 1: 4 bytes 0: 0 bytes
28	**Initial Latency (CK cycles) for Read Status Register command** 1: 8 CK cycles 0: 4 CK cycles
27	**Number of Additional Modifier Bytes Used for Read Register command** 1: 4 bytes 0: 1 byte
26	**Initial Latency (CK cycles) for Read Volatile Register command** 1: 8 CK cycles 0: 4 CK cycles
25	**Initial Latency (CK cycles) for Read Non-volatile Register command** 1: 8 CK cycles 0: 4 CK cycles
24	**Number of Additional Modifier Bytes Used for Write Status-Cfg Register command** 1: 4 bytes 0: 0 bytes
23	**Number of Additional Modifier Bytes Used for Write Register command** 1: 4 bytes 0: 1 byte
22	**Number of Data Bytes Used for Write Register command** 1: 2 bytes 0: 1 byte
21:16	**Reserved. Leave as "0".** (This allows new features to be added to these bits in the future.)
15:8	**Read Fast command**
7:0	**Read Fast Wrapped command** 00h means not supported

6.8.4 JEDEC xSPI (Profile 1.0) Parameter Table: 2nd DWORD - Command Codes Used in 8D-8D-8D Protocol Mode

Bits	Description
31-24	**Read Volatile Register command**
23:16	**Read NV Register command**
15:8	**Write Volatile Register command**
7:0	**Write NV Register command**

6.8.5 JEDEC xSPI (Profile 1.0) Parameter Table: 3rd DWORD - Memory Commands Supported in 8D-8D-8D Protocol Mode

This is the list of *optional* commands in 8D-8D-8D protocol mode. The command code for each of these is found in and Table 6-3 in the xSPI standard. For the commands that have more than one option for Command Code listed in the xSPI standard, the command code for each of these is found in the JEDEC xSPI (Profile 1.0) Parameter Table: 1st to 2nd DWORD above. Table 6-2 in the xSPI standard lists the required commands for this profile. The required commands are not listed here.

Bits	Description
31	**Read SFDP 8D-8D-8D** 1: Command Supported 0: Command Not Supported
30	**Read Fast Wrapped** 1: Command Supported 0: Command Not Supported
29	**Setup Read Wrap** 1: Command Supported 0: Command Not Supported
28	**Erase 4Kbytes** 1: Command Supported 0: Command Not Supported
27	**Erase 32Kbytes** 1: Command Supported 0: Command Not Supported
26	**Erase Chip** 1: Command Supported 0: Command Not Supported
25	**Read Configuration Register** 1: Command Supported 0: Command Not Supported
24	**Read Flag Status Register** 1: Command Supported 0: Command Not Supported
23	**Read Register** 1: Command Supported 0: Command Not Supported
22	**Read Volatile Register** 1: Command Supported 0: Command Not Supported

6.8.5 JEDEC xSPI (Profile 1.0) Parameter Table: d DWORD - Memory Commands Supported in 8D-8D-8D Protocol Mode (cont'd)

Bits	Description
21	**Read NV Register** 1: Command Supported 0: Command Not Supported
20	**Write Status-Configuration Register** 1: Command Supported 0: Command Not Supported
19	**Clear Flag Status Reg** 1: Command Supported 0: Command Not Supported
18	**Write Register** 1: Command Supported 0: Command Not Supported
17	**Write Volatile Register** 1: Command Supported 0: Command Not Supported
16	**Write NV Register** 1: Command Supported 0: Command Not Supported
15	**Enter Deep Power Down** 1: Command Supported 0: Command Not Supported
14	**Exit Deep Power Down** 1: Command Supported 0: Command Not Supported
13	**Soft Reset** 1: Command Supported 0: Command Not Supported
12	**Reset Enable** 1: Command Supported 0: Command Not Supported
11	**Soft Reset and Enter default protocol mode.** 1: Command Supported 0: Command Not Supported
10	**Enter default protocol mode** 1: Command Supported 0: Command Not Supported
9-0	**Reserved. Leave as "0".** (This allows new features to be added to these bits in the future.)

6.8.6 JEDEC xSPI (Profile 1.0) Parameter Table: 4th DWORD - Dummy Cycles Used for Various Frequencies

Bits	Description
31-12	**Reserved. Leave as "0".** (This allows new features to be added to these bits in the future.)
11:7	**200 MHz operation: number of dummy cycles required** A value of 0 means this frequency is not supported
6:2	**200 MHz operation: configuration bit pattern to set this number of dummy cycles**
1:0	**Reserved. Leave as "0".** (This allows new features to be added to these bits in the future.)

6.8.7 JEDEC xSPI (Profile 1.0) Parameter Table: 5th DWORD - Dummy Cycles Used for Various Frequencies

Bits	Description
31-27	**166 MHz operation: number of dummy cycles required** A value of 0 means this frequency is not supported
26:22	**166 MHz operation: configuration bit pattern to set this number of dummy cycles**
21:17	**133 MHz operation: number of dummy cycles required** A value of 0 means this frequency is not supported
16:12	**133 MHz operation: configuration bit pattern to set this number of dummy cycles**
11:7	**100 MHz operation: number of dummy cycles required** A value of 0 means this frequency is not supported
6:2	**100 MHz operation: configuration bit pattern to set this number of dummy cycles**
1:0	**Reserved. Leave as "0".** (This allows new features to be added to these bits in the future.)

6.8.8 JEDEC xSPI (Profile 1.0) Parameter Table: 6th DWORD – Default Dummy Cycles After POR

Bits	Description
31-10	**Reserved. Leave as "0".** (This allows new features to be added to these bits in the future.)
9:5	**(8S-8S-8S) Default Dummy Cycles after POR** A value of 0 means this IO mode is not supported
4:0	**(8D-8D-8D) Default Dummy Cycles after POR** A value of 0 means this IO mode is not supported

6.9 JEDEC eXtended Serial Peripheral Interface (xSPI) - Profile 2.0 Parameter Header and Table

See JESD251, eXpanded Serial Peripheral Interface (xSPI) for Non-volatile Memory Devices, Version 1 for details about this interface. This interface supports 2 profiles. Profile 1.0 is covered in 6.8, Profile 2.0 is covered in 6.9. A host controller may support both profiles, target devices will typically support only one of the profiles.

6.9.1 JEDEC xSPI (Profile 2.0) Parameter Header: 1st DWORD

Bits	Description
31:24	**Parameter Table Length** This field specifies how many DWORDs are in the Parameter table. NOTE This field is 1's based. Therefore, 1 indicates 1 DWORD.
23:16	**Parameter Table Major Revision Number[1]** This 8-bit field indicates the major revision number of the associated parameter table. The value in this field is 01h for this table defined by JESD216E revision (unchanged from JESD216D revision). NOTE Major Revision starts at 01h. The Major Revision of JEDEC defined parameter tables can only be modified by updates to this standard.
15:8	**Parameter Table Minor Revision Number[1]** This 8-bit field indicates the minor revision number of the associated parameter table. The value in this field is 00h for this table defined by JESD216E revision (unchanged from JESD216D revision). NOTE Minor Revision starts at 00h. The Minor Revision of the JEDEC owned parameter tables can only be modified by updates to this standard.
7:0	**Parameter ID LSB (0x06)** The eXtended Serial Peripheral Interface (Profile 2) is assigned the ID LSB of 06h.
NOTE See "Major vs. Minor Revisions" in clause 6.2.	

6.9.2 JEDEC xSPI (Profile 2.0) Parameter Header: 2nd DWORD

Bits	Description
31:24	**Parameter ID MSB (0xFF)** Refer to Definition of Parameter ID Field below.
23:0	**Parameter Table Pointer (PTP)** This address specifies the start of this header's Parameter Table in the SFDP structure. This is a byte address and must be DWORD-aligned.

6.9.3 JEDEC xSPI (Profile 2.0) Parameter Table: 1st DWORD - Command Codes Used in 8D-8D-8D Profile 2.0 Protocol Mode

Bits	Description
31	**xSPI Support** 1: Device implements 8D-8D-8D Profile 2.0 protocol mode as defined in JEDEC xSPI spec 0: Not Supported
30	**Read Register Wrapped** 1: Command Supported 0: Command Not Supported
29	**Read Register Linear** 1: Command Supported 0: Command Not Supported
28	**Read Memory Wrapped** 1: Command Supported 0: Command Not Supported
27	**Read Memory Linear** 1: Command Supported 0: Command Not Supported
26	**Write Register Wrapped** 1: Command Supported 0: Command Not Supported
25	**Write Register Linear** 1: Command Supported 0: Command Not Supported
24	**Memory Wrapped** 1: Command Supported 0: Command Not Supported
23	**Write Memory Wrapped** 1: Command Supported 0: Command Not Supported
22	**WREN1 (Write Enable 1)** 1: Command Supported 0: Command Not Supported
21	**WREN2 (Write Enable 2)** 1: Command Supported 0: Command Not Supported
20	**SREN (Status Register Enable)** 1: Command Supported 0: Command Not Supported
19	**Status Register Read** 1: Command Supported 0: Command Not Supported
18	**Status Register Clear** 1: Command Supported 0: Command Not Supported
17	**Configuration Register Read** 1: Command Supported 0: Command Not Supported

6.9.3 JEDEC xSPI (Profile 2.0) Parameter Table: 1st DWORD - Command Codes Used in 8D- 8D-8D Profile 2.0 Protocol Mode (cont'd)

Bits	Description
16	**Configuration Register Load** 1: Command Supported 0: Command Not Supported
15	**Deep Power Down** 1: Command Supported 0: Command Not Supported
14	**Word Program** 1: Command Supported 0: Command Not Supported
13	**Sector Erase** 1: Command Supported 0: Command Not Supported
12	**Chip Erase** 1: Command Supported 0: Command Not Supported
11	**Erase Suspend** 1: Command Supported 0: Command Not Supported
10	**Erase Resume** 1: Command Supported 0: Command Not Supported
9	**Write to Buffer** 1: Command Supported 0: Command Not Supported
8	**Program Write to Buffer** 1: Command Supported 0: Command Not Supported
7	**Program Suspend** 1: Command Supported 0: Command Not Supported
6	**Program Resume** 1: Command Supported 0: Command Not Supported
5	**Enter SPI (1S-1S-1S)** 1: Command Supported 0: Command Not Supported
4:0	**Reserved. Leave as "0".** (This allows new features to be added to these bits in the future.)

6.9.4 JEDEC xSPI (Profile 2.0) Parameter Table: 2nd DWORD - Dummy Cycles Used for Various Frequencies

Bits	Description
31-12	**Reserved. Leave as "0".** (This allows new features to be added to these bits in the future.)
11:7	**200 MHz operation: number of dummy cycles required** A value of 0 means this frequency is not supported
6:2	**200 MHz operation: configuration bit pattern to set this number of dummy cycles**
1:0	**Reserved. Leave as "0".** (This allows new features to be added to these bits in the future.)

6.9.5 JEDEC xSPI (Profile 2.0) Parameter Table: 3rd DWORD - Dummy Cycles Used for Various Frequencies

Bits	Description
31-27	**166 MHz operation: number of dummy cycles required** A value of 0 means this frequency is not supported
26:22	**166 MHz operation: configuration bit pattern to set this number of dummy cycles**
21:17	**133 MHz operation: number of dummy cycles required** A value of 0 means this frequency is not supported
16:12	**133 MHz operation: configuration bit pattern to set this number of dummy cycles**
11:7	**100 MHz operation: number of dummy cycles required** A value of 0 means this frequency is not supported
6:2	**100 MHz operation: configuration bit pattern to set this number of dummy cycles**
1:0	**Reserved. Leave as "0".** (This allows new features to be added to these bits in the future.)

6.10 Status, Control and Configuration Register Map for SPI Memory Devices

SPI memory devices from different manufacturers have widely different configurations for Status, Control and Configuration registers. The Status, Control and Configuration Register Map (SCCR Map for short) defines a common nomenclature for the most common register bits and their functions, and describes how the individual bits may be accessed for a specific device.

This clause covers the SCCR Map for Single, Dual, Quad and xSPI Profile 1.0 Octal memory devices. xSPI Profile 2.0 Octal memory devices are covered in 6.11.

The purpose of the SCCR Map is to provide a host controller with a minimum amount of information to be able to boot a system and load necessary code for the system to run. It is to be expected that the code loaded from the memory device will contain the necessary information required to achieve optimum performance from the device.

6.10 Status, Control and Configuration Register Map for SPI Memory Devices (cont'd)

Register bits may be accessed by a command specifying an address and a register value, or by a direct command accessing a specific register or bit directly. (05h, "Read Status Register", is an example of a direct command.) For each bit, the SCCR Map defines which command (if any) is used to write the bit, which command is used to read the bit, which position the bit has in the register and at which address (if any) the register is located. (An address of FFh indicates that no address is used and the commands are direct commands.)

The register address is defined as a 32-bit address in the SCCR Map. For devices using less than 32 bits for Generic Addressable Read/Write Status/Control register commands, the uppermost bits should be ignored. (Sending a 32-bit address to a device expecting an 8-bit address will not produce the desired result.) The actual number of address bytes and the number of dummy bytes/dummy cycles used for Generic Addressable Read/Write Status/Control register commands by the device is provided in 6.10.5.

To avoid the need to provide a full 32-bit address for each bit, the addressing scheme in this table takes into account that every device uses a narrow range of addresses for the SCCRs. The address is therefore defined as a 32-bit offset address pointer, which indicates the start of the address block, and an 8-bit local address, which indicates the position of each register within the block.

The physical address of a register is found by adding the 32-bit offset address pointer and the 8-bit local address. Separate 32-bit offset address pointers are provided for volatile and non-volatile address blocks.

The 8-bit local address can either be added to the last byte of the 32-byte address, creating an address of the format xxxx-xxxx xxxx-xxxx AAAA-AAAA.

The 8- bit local address can be added to Byte 1 of the 32-bit address, creating an address of the format xxxx-xxxx xxxx-xxxx AAAA-AAAA xxxx-xxxx.

Which of the two options is used is described in the parameter table for each bit.

In the SCCR Map, each bit is defined separately. In an actual device, multiple of these bits will be combined into one physical register (e.g., the Status Register). The physical registers may also include additional bits that are not part of the current SCCR Map. **It is therefore important that the host controller reads the current value of the register and only changes the intended bits before writing the value back to the register to ensure that other functions are not affected.** ("Read-Modify-Write" operations may be used if available.)

Even though the Status, Control and Configuration Register Map was initially developed as part of the xSPI protocol spec, this information can also be added for other devices.

Registers may be status, control or configuration registers.

These register definitions describe the bit locations after the device is powered up. For devices where status control register bits change to other address locations after a mode change, the host controller software (loaded from the device at boot) will have to deal with that.

6.10.1 SCCR Map for SPI Memory Devices Parameter Header: 1st DWORD

Bits	Description
31:24	**Parameter Table Length** This field specifies how many DWORDs are in the Parameter table. NOTE This field is 1's based. Therefore, 1 indicates 1 DWORD.
23:16	**Parameter Table Major Revision Number** This 8-bit field indicates the major revision number of the parameter table. The value in this field is 01h for this table defined by JESD216E revision (unchanged from JESD216D revision). NOTE The Major Revision of JEDEC defined parameter tables can only be modified by updates to this standard.
15:8	**Parameter Table Minor Revision Number** This 8-bit field indicates the minor revision number of the Status, Control and Configuration Register Map Parameter Table. The value in this field is 01h for this table defined by JESD216D. NOTE The Minor Revision of the JEDEC owned parameter tables can only be modified by updates to this standard.
7:0	**Parameter ID LSB** The Status, Control and Configuration Register Map is assigned the ID LSB of 87h.

6.10.2 SCCR Map for SPI Memory Devices Parameter Header: 2nd DWORD

Bits	Description
31:24	**Parameter ID MSB** The Status, Control and Configuration Register Map is assigned the ID MSB of FFh.
23:0	**Parameter Table Pointer (PTP)** This address specifies the start of this header's Parameter Table in the SFDP structure. The address is in terms of bytes and must be DWORD-aligned.

6.10.3 SCCR Map for SPI Memory Devices Parameter Table: 1st DWORD – Volatile Registers Address Offset

Bits	Description
31:0	Address offset for volatile registers

6.10.4 SCCR Map for SPI Memory Devices Parameter Table: 2nd DWORD – Non-volatile Registers Address Offset

Bits	Description
31:0	Address offset for non-volatile registers

6.10.5 SCCR Map for SPI Memory Devices Parameter Table: 3rd DWORD – Generic Addressable Read/Write Status/Control Register Commands for Volatile Registers

Bits	Description
31	**Generic Addressable Read Status/Control register command for volatile registers supported for some (or all) registers** 0: Not supported for any register 1: Supported for some (or all) registers
30	**Generic Addressable Write Status/Control register command for volatile registers supported for some (or all) registers** 0: Not supported for any register 1: Supported for some (or all) registers
29:28	**Number of address bytes used for Generic Addressable Read/Write Status/Control register commands for volatile registers:** (The number of address bytes used for accessing registers may be different from the number of address bytes used for accessing the memory array.) 00: 1 byte (8-bit) 01: 2 bytes (16-bit) 10: 3 bytes (24-bit) 11: 4 bytes (32-bit)
27:26	**Number of dummy bytes used for Generic Addressable Read Status/Control register command for volatile registers in (1S-1S-1S) mode:** 00: 0 bytes (no dummy cycles required) 01: 1 byte (8-bit) 10: Use the number of bits as defined in bits 3:0 in this DWORD 11: Command not supported in this mode
25:22	**Number of dummy cycles used for Generic Addressable Read Status/Control register command for volatile registers in (2S-2S-2S) mode** 0000-1110:[0-14 cycles] 1111: Command not supported in this mode
21:18	**Number of dummy cycles used for Generic Addressable Read Status/Control register command for volatile registers in (4S-4S-4S) mode** 0000-1110:[0-14 cycles] 1111: Command not supported in this mode
17:14	**Number of dummy cycles used for Generic Addressable Read Status/Control register command for volatile registers in (4S-4D-4D) mode** 0000-1110:[0-14 cycles] 1111: Command not supported in this mode
13:10	**Number of dummy cycles used for Generic Addressable Read Status/Control register command for volatile registers in (8S-8S-8S) mode** 0000-1110:[0-14 cycles] 1111: Command not supported in this mode
9:6	**Number of dummy cycles used for Generic Addressable Read Status/Control register command for volatile registers in (8D-8D-8D) mode** 0000-1110:[0-14 cycles] 1111: Command not supported in this mode
5:4	**Reserved. Leave as "0".** (This allows new features to be added to these bits in the future.)
3:0	**Number of dummy cycles used for Generic Addressable Read Status/Control register command for volatile registers in (1S-1S-1S) mode – If bits 27:26 above equal 10:** 0000-1110: [0-14 cycles] 1111: Command not supported in this mode

6.10.6 SCCR Map for SPI Memory Devices Parameter Table: 4th DWORD – Generic Addressable Read/Write Status/Control Register Commands for Non-volatile Registers

Bits	Description
31	**Generic Addressable Read Status/Control register command for non-volatile registers supported for some (or all) registers** 0: Not supported for any register 1: Supported for some (or all) registers
30	**Generic Addressable Write Status/Control register command for non-volatile registers supported for some (or all) registers** 0: Not supported for any register 1: Supported for some (or all) registers
29:28	**Number of address bytes used for Generic Addressable Read/Write Status/Control register commands for non-volatile registers:** (The number of address bytes used for accessing registers may be different from the number of address bytes used for accessing the memory array.) 00: 1 byte (8-bit) 01: 2 bytes (16-bit) 10: 3 bytes (24-bit) 11: 4 bytes (32-bit)
27:26	**Number of dummy bytes used for Generic Addressable Read Status/Control register command for non-volatile registers in (1S-1S-1S) mode:** 00: 0 bytes (no dummy cycles required) 01: 1 byte (8-bit) 10: Use the number of bits as defined in bits 3:0 in this DWORD 11: Command not supported in this mode
25:22	**Number of dummy cycles used for Generic Addressable Read Status/Control register command in (2S-2S-2S) mode** 0000-1110:[0-14 cycles] 1111: Command not supported in this mode
21:18	**Number of dummy cycles used for Generic Addressable Read Status/Control register command for non-volatile registers in (4S-4S-4S) mode** 0000-1110:[0-14 cycles] 1111: Command not supported in this mode
17:14	**Number of dummy cycles used for Generic Addressable Read Status/Control register command for non-volatile registers in (4S-4D-4D) mode** 0000-1110:[0-14 cycles] 1111: Command not supported in this mode
13:10	**Number of dummy cycles used for Generic Addressable Read Status/Control register command for non-volatile registers in (8S-8S-8S) mode** 0000-1110:[0-14 cycles] 1111: Command not supported in this mode
9:6	**Number of dummy cycles used for Generic Addressable Read Status/Control register command for non-volatile registers in (8D-8D-8D) mode** 0000-1110:[0-14 cycles] 1111: Command not supported in this mode
5:4	**Reserved. Leave as "0".** (This allows new features to be added to these bits in the future.)
3:0	**Number of dummy cycles used for Generic Addressable Read Status/Control register command for non-volatile registers in (1S-1S-1S) mode – If bits 27:26 above equal 10:** 0000-1110: [0-14 cycles] 1111: Command not supported in this mode

6.10.7 SCCR Map for SPI Memory Devices Parameter Table: 5th DWORD – WIP (Required for xSPI)

Bits	Description
31	**Write In Progress (WIP) bit available:** 0: Not supported 1: Supported
30	**Write In Progress (WIP) polarity:** 0: Positive (WIP=1 means write is in progress) 1: Inverted (WIP=0 means write is in progress)
29	**Reserved. Leave as "0".** (This allows new features to be added to these bits in the future.)
28	**Bit is accessed by commands using address** 0: Bit is accessed by direct commands (Commands do not use address) 1: Bit is accessed by commands using address
27	**0: Local address for WIP bit is found in last byte of the address:** (Byte 0 of 32-bit address space): xxxx-xxxx xxxx-xxxx xxxx-xxxx AAAA-AAAA (Byte 0 of 24-bit address space): xxxx-xxxx xxxx-xxxx AAAA-AAAA (Byte 0 of 8-bit address space): AAAA-AAAA **1: Local address for WIP bit is found in Byte 1 of 32-bit address:** xxxx-xxxx xxxx-xxxx AAAA-AAAA xxxx-xxxx (This option may also be used for 24-bit addressing, but is not applicable for devices using 8-bit addressing)
26-24	**Bit location of WIP bit in register**
23-16	**If Bit 28 is 1: Address of register where bit is located** Local address AAAA-AAAA **If Bit 28 is 0: Modes supported and dummy cycles used for direct command** Bit 23: 1: 8D-8D-8D mode supported, using the # of dummy cycles shown in bits 19-16 0: 8D-8D-8D mode not supported, using the # of dummy cycles shown in bits 19-16 Bit 22: 1: 8S-8S-8S mode supported, using the # of dummy cycles shown in bits 19-16 0: 8S-8S-8S mode not supported, using the # of dummy cycles shown in bits 19-16 Bit 21: 1: 4S-4D-4D mode supported, using the # of dummy cycles shown in bits 19-16 0: 4S-4D-4D mode not supported, using the # of dummy cycles shown in bits 19-16 Bit 20: 1: 4S-4S-4S mode supported, using the # of dummy cycles shown in bits 19-16 0: 4S-4S-4S mode not supported, using the # of dummy cycles shown in bits 19-16 Bits 19-16: Number of dummy cycles (0-15) used NOTE 1S-1S-1S mode, if supported by the device, will be supporting this command without using dummy cycles. NOTE Modes indicated as not supported may still be supported by the device, but not using the same number of dummy cycles as listed here. NOTE Other modes may also be supported by the device.
15-8	**Command used for read access** 00h means not supported
7-0	**Command used for write access** 00h means not supported (bit is read only)

6.10.8 SCCR Map for SPI Memory Devices Parameter Table: 6th DWORD – WEL

Bits	Description
31	**Write Enable (WEL) bit available:** 0: Not supported 1: Supported
30	**Write Enable (WEL) polarity:** 0: Positive (WEL =1 means write is enabled) 1: Inverted (WEL =0 means write is enabled)
29	**Write access of WEL bit** 0: Write command uses a bit field to identify bit location of WEL bit in register 1: Write command is a direct operation to set WEL bit
28	**Bit is accessed by commands using address** 0: Bit is accessed by direct commands (Commands do not use address) 1: Bit is accessed by commands using address
27	**0: Local address for WEL bit is found in last byte of the address:** (Byte 0 of 32-bit address space): xxxx-xxxx xxxx-xxxx xxxx-xxxx AAAA-AAAA (Byte 0 of 24-bit address space): xxxx-xxxx xxxx-xxxx AAAA-AAAA (Byte 0 of 8-bit address space): AAAA-AAAA **1: Local address for WEL bit is found in Byte 1 of 32-bit address:** xxxx-xxxx xxxx-xxxx AAAA-AAAA xxxx-xxxx (This option may also be used for 24-bit addressing, but is not applicable for devices using 8-bit addressing)
26-24	**Bit location of WEL bit in register**
23-16	**If Bit 28 is 1: Address of register where bit is located** Local address AAAA-AAAA **If Bit 28 is 0: Modes supported and dummy cycles used for direct command** Bit 23: 1: 8D-8D-8D mode supported, using the # of dummy cycles shown in bits 19-16 0: 8D-8D-8D mode not supported, using the # of dummy cycles shown in bits 19-16 Bit 22: 1: 8S-8S-8S mode supported, using the # of dummy cycles shown in bits 19-16 0: 8S-8S-8S mode not supported, using the # of dummy cycles shown in bits 19-16 Bit 21: 1: 4S-4D-4D mode supported, using the # of dummy cycles shown in bits 19-16 0: 4S-4D-4D mode not supported, using the # of dummy cycles shown in bits 19-16 Bit 20: 1: 4S-4S-4S mode supported, using the # of dummy cycles shown in bits 19-16 0: 4S-4S-4S mode not supported, using the # of dummy cycles shown in bits 19-16 Bits 19-16: Number of dummy cycles (0-15) used NOTE 1S-1S-1S mode, if supported by the device, will be supporting this command without using dummy cycles. NOTE Modes indicated as not supported may still be supported by the device, but not using the same number of dummy cycles as listed here. NOTE Other modes may also be supported by the device.
15-8	**Command used for read access** 00h means not supported
7-0	**Command used for write access** 00h means not supported

6.10.9 SCCR Map for SPI Memory Devices Parameter Table: 7th DWORD – Program Error

Bits	Description
31	**Program Error bit available:** 0: Not supported 1: Supported
30	**Program Error bit polarity:** 0: Positive (Program Error = 0 means no error, Program Error = 1 means last Program operation created an error) 1: Inverted (Program Error = 1 means no error , Program Error = 0 means last Program operation created an error)
29	**Sharing** 0: Not shared: The device has separate bits for Program Error and Erase Error 1: Shared: The same bit is used for both Program Error and Erase Error
28	**Bit is accessed by commands using address** 0: Bit is accessed by direct commands (Commands do not use address) 1: Bit is accessed by commands using address
27	**0: Local address for Program Error bit is found in last byte of the address:** (Byte 0 of 32-bit address space): xxxx-xxxx xxxx-xxxx xxxx-xxxx AAAA-AAAA (Byte 0 of 24-bit address space): xxxx-xxxx xxxx-xxxx AAAA-AAAA (Byte 0 of 8-bit address space): AAAA-AAAA **1: Local address for Program Error bit is found in Byte 1 of 32-bit address:** xxxx-xxxx xxxx-xxxx AAAA-AAAA xxxx-xxxx (This option may also be used for 24-bit addressing, but is not applicable for devices using 8-bit addressing)
26-24	**Bit location of Program Error bit in register**
23-16	**If Bit 28 is 1: Address of register where bit is located** Local address AAAA-AAAA **If Bit 28 is 0: Modes supported and dummy cycles used for direct command** Bit 23: 1: 8D-8D-8D mode supported, using the # of dummy cycles shown in bits 19-16 0: 8D-8D-8D mode not supported, using the # of dummy cycles shown in bits 19-16 Bit 22: 1: 8S-8S-8S mode supported, using the # of dummy cycles shown in bits 19-16 0: 8S-8S-8S mode not supported, using the # of dummy cycles shown in bits 19-16 Bit 21: 1: 4S-4D-4D mode supported, using the # of dummy cycles shown in bits 19-16 0: 4S-4D-4D mode not supported, using the # of dummy cycles shown in bits 19-16 Bit 20: 1: 4S-4S-4S mode supported, using the # of dummy cycles shown in bits 19-16 0: 4S-4S-4S mode not supported, using the # of dummy cycles shown in bits 19-16 Bits 19-16: Number of dummy cycles (0-15) used NOTE 1S-1S-1S mode, if supported by the device, will be supporting this command without using dummy cycles. NOTE Modes indicated as not supported may still be supported by the device, but not using the same number of dummy cycles as listed here. NOTE Other modes may also be supported by the device.
15-8	**Command used for read access** 00h means not supported
7-0	**Command used for write access** 00h means not supported (bit is read only)

6.10.10 SCCR Map for SPI Memory Devices Parameter Table: 8th DWORD – Erase Error

Bits	Description
31	**Erase Error bit available:** 0: Not supported 1: Supported
30	**Erase Error bit polarity:** 0: Positive (Erase Error = 0 means no error, Erase Error = 1 means last Erase operation created an error) 1: Inverted (Erase Error = 1 means no error, Erase Error = 0 means last Erase operation created an error)
29	**Sharing** 0: Not shared: The device has separate bits for Program Error and Erase Error 1: Shared: The same bit is used for both Program Error and Erase Error
28	**Bit is accessed by commands using address** 0: Bit is accessed by direct commands (Commands do not use address) 1: Bit is accessed by commands using address
27	**0: Local address for Erase Error bit is found in last byte of the address:** (Byte 0 of 32-bit address space): xxxx-xxxx xxxx-xxxx xxxx-xxxx AAAA-AAAA (Byte 0 of 24-bit address space): xxxx-xxxx xxxx-xxxx AAAA-AAAA (Byte 0 of 8-bit address space): AAAA-AAAA **1: Local address for Erase Error bit is found in Byte 1 of 32-bit address:** xxxx-xxxx xxxx-xxxx AAAA-AAAA xxxx-xxxx (This option may also be used for 24-bit addressing, but is not applicable for devices using 8-bit addressing)
26-24	**Bit location of Erase Error bit in register**
23-16	**If Bit 28 is 1: Address of register where bit is located** Local address AAAA-AAAA **If Bit 28 is 0: Modes supported and dummy cycles used for direct command** Bit 23: 1: 8D-8D-8D mode supported, using the # of dummy cycles shown in bits 19-16 0: 8D-8D-8D mode not supported, using the # of dummy cycles shown in bits 19-16 Bit 22: 1: 8S-8S-8S mode supported, using the # of dummy cycles shown in bits 19-16 0: 8S-8S-8S mode not supported, using the # of dummy cycles shown in bits 19-16 Bit 21: 1: 4S-4D-4D mode supported, using the # of dummy cycles shown in bits 19-16 0: 4S-4D-4D mode not supported, using the # of dummy cycles shown in bits 19-16 Bit 20: 1: 4S-4S-4S mode supported, using the # of dummy cycles shown in bits 19-16 0: 4S-4S-4S mode not supported, using the # of dummy cycles shown in bits 19-16 Bits 19-16: Number of dummy cycles (0-15) used NOTE 1S-1S-1S mode, if supported by the device, will be supporting this command without using dummy cycles. NOTE Modes indicated as not supported may still be supported by the device, but not using the same number of dummy cycles as listed here. NOTE Other modes may also be supported by the device.
15-8	**Command used for read access** 00h means not supported
7-0	**Command used for write access** 00h means not supported (bit is read only)

6.10.11 SCCR Map for SPI Memory Devices Parameter Table: 9th DWORD – Variable Dummy Cycle Settings – Volatile Register

Bits	Description
31	**Variable number of dummy cycles supported** 0: Not supported, or supported in a way that cannot be described correctly by this parameter table 1: Supported
30-29	**Number of physical bits used to set wait states** 00: 2 bits 01: 3 bits 10: 4 bits 11: 5 bits
28	**Bits are accessed by commands using address** 0: Bits are accessed by direct commands (Commands do not use address) 1: Bits are accessed by commands using address
27	**0: Local address for Variable Dummy Cycle Settings bits is found in last byte of the address:** (Byte 0 of 32-bit address space): xxxx-xxxx xxxx-xxxx xxxx-xxxx AAAA-AAAA (Byte 0 of 24-bit address space): xxxx-xxxx xxxx-xxxx AAAA-AAAA (Byte 0 of 8-bit address space): AAAA-AAAA **1: Local address for Variable Dummy Cycle Settings bits is found in Byte 1 of 32-bit address:** xxxx-xxxx xxxx-xxxx AAAA-AAAA xxxx-xxxx (This option may also be used for 24-bit addressing, but is not applicable for devices using 8-bit addressing)
26-24	**Bit location of LSb of physical bits in register** (Requirements: The physical bits used in a device are in the same (one) register, the bits form a continuous field and the bits are in order. If these requirements are not met, bit 31 above has to be set to 0.)
23-16	**If Bit 28 is 1: Address of registers where bits are located** Local address AAAA-AAAA **If Bit 28 is 0: Modes supported and dummy cycles used for direct command** Bit 23: 1: 8D-8D-8D mode supported, using the # of dummy cycles shown in bits 19-16 0: 8D-8D-8D mode not supported, using the # of dummy cycles shown in bits 19-16 Bit 22: 1: 8S-8S-8S mode supported, using the # of dummy cycles shown in bits 19-16 0: 8S-8S-8S mode not supported, using the # of dummy cycles shown in bits 19-16 Bit 21: 1: 4S-4D-4D mode supported, using the # of dummy cycles shown in bits 19-16 0: 4S-4D-4D mode not supported, using the # of dummy cycles shown in bits 19-16 Bit 20: 1: 4S-4S-4S mode supported, using the # of dummy cycles shown in bits 19-16 0: 4S-4S-4S mode not supported, using the # of dummy cycles shown in bits 19-16 Bits 19-16: Number of dummy cycles (0-15) used NOTE 1S-1S-1S mode, if supported by the device, will be supporting this command without using dummy cycles. NOTE Modes indicated as not supported may still be supported by the device, but not using the same number of dummy cycles as listed here. NOTE Other modes may also be supported by the device.
15-8	**Command used for read access** 00h means not supported
7-0	**Command used for write access** 00h means not supported

6.10.12 SCCR Map for SPI Memory Devices Parameter Table: 10th DWORD – Variable Dummy Cycle Settings- Non-volatile Register

Bits	Description
31	**Variable number of dummy cycles supported** 0: Not supported, (or supported in a way that cannot be described correctly by this parameter table) 1: Supported
30-29	**Number of physical bits used to set dummy cycles** See the following DWORDs for bit patterns used to set dummy cycles (wait states) 00: 2 bit 01: 3 bits 10: 4 bit 11: 5 bits
28	**Bits are accessed by commands using address** 0: Bits are accessed by direct commands (Commands do not use address) 1: Bits are accessed by commands using address
27	**0: Local address for Variable Dummy Cycle Settings bits is found in last byte of the address:** (Byte 0 of 32-bit address space): xxxx-xxxx xxxx-xxxx xxxx-xxxx AAAA-AAAA (Byte 0 of 24-bit address space): xxxx-xxxx xxxx-xxxx AAAA-AAAA (Byte 0 of 8-bit address space): AAAA-AAAA **1: Local address for Variable Dummy Cycle Settings bits is found in Byte 1 of 32-bit address:** xxxx-xxxx xxxx-xxxx AAAA-AAAA xxxx-xxxx (This option may also be used for 24-bit addressing, but is not applicable for devices using 8-bit addressing)
26-24	**Bit location of LSb of physical bits in register** (Requirements: The physical bits used in a device are in the same (one) register, the bits form a continuous field and the bits are in order. If these requirements are not met, bit 31 above has to be set to 0.)
23-16	**If Bit 28 is 1: Address of registers where bits are located** Local address AAAA-AAAA **If Bit 28 is 0: Modes supported and dummy cycles used for direct command** Bit 23: 1: 8D-8D-8D mode supported, using the # of dummy cycles shown in bits 19-16 0: 8D-8D-8D mode not supported, using the # of dummy cycles shown in bits 19-16 Bit 22: 1: 8S-8S-8S mode supported, using the # of dummy cycles shown in bits 19-16 0: 8S-8S-8S mode not supported, using the # of dummy cycles shown in bits 19-16 Bit 21: 1: 4S-4D-4D mode supported, using the # of dummy cycles shown in bits 19-16 0: 4S-4D-4D mode not supported, using the # of dummy cycles shown in bits 19-16 Bit 20: 1: 4S-4S-4S mode supported, using the # of dummy cycles shown in bits 19-16 0: 4S-4S-4S mode not supported, using the # of dummy cycles shown in bits 19-16 Bits 19-16: Number of dummy cycles (0-15) used NOTE 1S-1S-1S mode, if supported by the device, will be supporting this command without using dummy cycles. NOTE Modes indicated as not supported may still be supported by the device, but not using the same number of dummy cycles as listed here. NOTE Other modes may also be supported by the device.
15-8	**Command used for read access** 00h means not supported
7-0	**Command used for write access** 00h means not supported

6.10.13 SCCR Map for SPI Memory Devices Parameter Table: 11th DWORD – Variable Dummy Cycle Settings – Bit Patterns

Bits	Description
31	**30 dummy cycles supported:** 0: Not supported 1: Supported
30-26	**Bit pattern used to set 30 dummy cycles:** If less than 5 physical bits are used to set dummy cycles, the least significant bits are used, and the most significant bit(s) are set to 0.
25	**28 dummy cycles supported:** 0: Not supported 1: Supported
24-20	**Bit pattern used to set 28 dummy cycles:** If less than 5 physical bits are used to set dummy cycles, the least significant bits are used, and the most significant bit(s) are set to 0.
19	**26 dummy cycles supported:** 0: Not supported 1: Supported
18-14	**Bit pattern used to set 26 dummy cycles:** If less than 5 physical bits are used to set dummy cycles, the least significant bits are used, and the most significant bit(s) are set to 0.
13	**24 dummy cycles supported:** 0: Not supported 1: Supported
12-8	**Bit pattern used to set 24 dummy cycles:** If less than 5 physical bits are used to set dummy cycles, the least significant bits are used, and the most significant bit(s) are set to 0.
7	**22 dummy cycles supported:** 0: Not supported 1: Supported
6-2	**Bit pattern used to set 22 dummy cycles:** If less than 5 physical bits are used to set dummy cycles, the least significant bits are used, and the most significant bit(s) are set to 0.
1-0	**Reserved. Leave as "0".** (This allows new features to be added to these bits in the future.)

6.10.14 SCCR Map for SPI Memory Devices Parameter Table: 12th DWORD – Variable Dummy Cycle Settings – Bit Patterns

Bits	Description
31	**20 dummy cycles supported:** 0: Not supported 1: Supported
30-26	**Bit pattern used to set 20 dummy cycles:** If less than 5 physical bits are used to set dummy cycles, the least significant bits are used, and the most significant bit(s) are set to 0.
25	**18 dummy cycles supported:** 0: Not supported 1: Supported
24-20	**Bit pattern used to set 18 dummy cycles:** If less than 5 physical bits are used to set dummy cycles, the least significant bits are used, and the most significant bit(s) are set to 0.
19	**16 dummy cycles supported:** 0: Not supported 1: Supported
18-14	**Bit pattern used to set 16 dummy cycles:** If less than 5 physical bits are used to set dummy cycles, the least significant bits are used, and the most significant bit(s) are set to 0.
13	**14 dummy cycles supported:** 0: Not supported 1: Supported
12-8	**Bit pattern used to set 14 dummy cycles:** If less than 5 physical bits are used to set dummy cycles, the least significant bits are used, and the most significant bit(s) are set to 0.
7	**12 dummy cycles supported:** 0: Not supported 1: Supported
6-2	**Bit pattern used to set 12 dummy cycles:** If less than 5 physical bits are used to set dummy cycles, the least significant bits are used, and the most significant bit(s) are set to 0.
1-0	**Reserved. Leave as "0".** (This allows new features to be added to these bits in the future.)

6.10.15 SCCR Map for SPI Memory Devices Parameter Table: 13th DWORD – Variable Dummy Cycle Settings – Bit Patterns

Bits	Description
31	**10 dummy cycles supported:** 0: Not supported 1: Supported
30-26	**Bit pattern used to set 10 dummy cycles:** If less than 5 physical bits are used to set dummy cycles, the least significant bits are used, and the most significant bit(s) are set to 0.
25	**8 dummy cycles supported:** 0: Not supported 1: Supported
24-20	**Bit pattern used to set 8 dummy cycles:** If less than 5 physical bits are used to set dummy cycles, the least significant bits are used, and the most significant bit(s) are set to 0.
19	**6 dummy cycles supported:** 0: Not supported 1: Supported
18-14	**Bit pattern used to set 6 dummy cycles:** If less than 5 physical bits are used to set dummy cycles, the least significant bits are used, and the most significant bit(s) are set to 0.
13	**4 dummy cycles supported:** 0: Not supported 1: Supported
12-8	**Bit pattern used to set 4 dummy cycles:** If less than 5 physical bits are used to set dummy cycles, the least significant bits are used, and the most significant bit(s) are set to 0.
7	**2 dummy cycles supported:** 0: Not supported 1: Supported
6-2	**Bit pattern used to set 2 dummy cycles:** If less than 5 physical bits are used to set dummy cycles, the least significant bits are used, and the most significant bit(s) are set to 0.
1-0	**Reserved. Leave as "0".** (This allows new features to be added to these bits in the future.)

6.10.16 SCCR Map for SPI Memory Devices Parameter Table: 14th DWORD – QPI Mode Enable Volatile

Bits	Description
31	**QPI Mode Enable bit available:** 0: Not supported 1: Supported
30	**QPI Mode Enable bit polarity:** 0: Positive (QPI Mode Enable bit = 1 means QPI mode is enabled) 1: Inverted (QPI Mode Enable bit = 0 means QPI mode is enabled)
29	**Reserved. Leave as "0".** (This allows new features to be added to these bits in the future.)
28	**Bit is accessed by commands using address** 0: Bit is accessed by direct commands (Commands do not use address) 1: Bit is accessed by commands using address
27	**0: Local address for QPI Mode Enable bit is found in last byte of the address:** (Byte 0 of 32-bit address space): xxxx-xxxx xxxx-xxxx xxxx-xxxx AAAA-AAAA (Byte 0 of 24-bit address space): xxxx-xxxx xxxx-xxxx AAAA-AAAA (Byte 0 of 8-bit address space): AAAA-AAAA **1: Local address for QPI Mode Enable bit is found in Byte 1 of 32-bit address:** xxxx-xxxx xxxx-xxxx AAAA-AAAA xxxx-xxxx (This option may also be used for 24-bit addressing, but is not applicable for devices using 8-bit addressing)
26-24	**Bit location of QPI Mode Enable bit in register**
23-16	**If Bit 28 is 1: Address of register where bit is located** Local address AAAA-AAAA **If Bit 28 is 0: Modes supported and dummy cycles used for direct command** Bit 23: 1: 8D-8D-8D mode supported, using the # of dummy cycles shown in bits 19-16 0: 8D-8D-8D mode not supported, using the # of dummy cycles shown in bits 19-16 Bit 22: 1: 8S-8S-8S mode supported, using the # of dummy cycles shown in bits 19-16 0: 8S-8S-8S mode not supported, using the # of dummy cycles shown in bits 19-16 Bit 21: 1: 4S-4D-4D mode supported, using the # of dummy cycles shown in bits 19-16 0: 4S-4D-4D mode not supported, using the # of dummy cycles shown in bits 19-16 Bit 20: 1: 4S-4S-4S mode supported, using the # of dummy cycles shown in bits 19-16 0: 4S-4S-4S mode not supported, using the # of dummy cycles shown in bits 19-16 Bits 19-16: Number of dummy cycles (0-15) used NOTE 1S-1S-1S mode, if supported by the device, will be supporting this command without using dummy cycles. NOTE Modes indicated as not supported may still be supported by the device, but not using the same number of dummy cycles as listed here. NOTE Other modes may also be supported by the device.
15-8	**Command used for read access** 00h means not supported
7-0	**Command used for write access** 00h means not supported

6.10.17 SCCR Map for SPI Memory Devices Parameter Table: 15th DWORD – QPI Mode Enable - Non -volatile

Bits	Description
31	**QPI Mode Enable bit available:** 0: Not supported 1: Supported
30	**QPI Mode Enable bit polarity:** 0: Positive (QPI Mode Enable bit = 1 means QPI mode is enabled) 1: Inverted (QPI Mode Enable bit = 0 means QPI mode is enabled)
29	**Reserved. Leave as "0".** (This allows new features to be added to these bits in the future.)
28	**Bit is accessed by commands using address** 0: Bit is accessed by direct commands (Commands do not use address) 1: Bit is accessed by commands using address
27	**0: Local address for QPI Mode Enable bit is found in last byte of the address** (Byte 0 of 32-bit address space): xxxx-xxxx xxxx-xxxx xxxx-xxxx AAAA-AAAA (Byte 0 of 24-bit address space): xxxx-xxxx xxxx-xxxx AAAA-AAAA (Byte 0 of 8-bit address space): AAAA-AAAA **1: Local address for QPI Mode Enable bit is found in Byte 1 of 32-bit address:** xxxx-xxxx xxxx-xxxx AAAA-AAAA xxxx-xxxx (This option may also be used for 24-bit addressing, but is not applicable for devices using 8-bit addressing)
26-24	**Bit location of QPI Mode Enable bit in register**
23-16	**If Bit 28 is 1: Address of register where bit is located** Local address AAAA-AAAA **If Bit 28 is 0: Modes supported and dummy cycles used for direct command** Bit 23: 1: 8D-8D-8D mode supported, using the # of dummy cycles shown in bits 19-16 0: 8D-8D-8D mode not supported, using the # of dummy cycles shown in bits 19-16 Bit 22: 1: 8S-8S-8S mode supported, using the # of dummy cycles shown in bits 19-16 0: 8S-8S-8S mode not supported, using the # of dummy cycles shown in bits 19-16 Bit 21: 1: 4S-4D-4D mode supported, using the # of dummy cycles shown in bits 19-16 0: 4S-4D-4D mode not supported, using the # of dummy cycles shown in bits 19-16 Bit 20: 1: 4S-4S-4S mode supported, using the # of dummy cycles shown in bits 19-16 0: 4S-4S-4S mode not supported, using the # of dummy cycles shown in bits 19-16 Bits 19-16: Number of dummy cycles (0-15) used NOTE 1S-1S-1S mode, if supported by the device, will be supporting this command without using dummy cycles. NOTE Modes indicated as not supported may still be supported by the device, but not using the same number of dummy cycles as listed here. NOTE Other modes may also be supported by the device.
15-8	**Command used for read access** 00h means not supported
7-0	**Command used for write access** 00h means not supported

6.10.18 SCCR Map for SPI Memory Devices Parameter Table: 16th DWORD – Octal Mode Enable – Volatile

Bits	Description
31	**Octal Mode Enable Volatile bit available:** 0: Not supported 1: Supported
30	**Octal Mode Enable Volatile bit polarity:** 0: Positive (Octal Mode Enable bit = 1 means Octal mode is enabled) 1: Inverted (Octal Mode Enable bit = 0 means Octal mode is enabled)
29	**Reserved. Leave as "0".** (This allows new features to be added to these bits in the future.)
28	**Bit is accessed by commands using address** 0: Bit is accessed by direct commands (Commands do not use address) 1: Bit is accessed by commands using address
27	**0: Local address for Octal Mode Enable Volatile bit is found in last byte of the address:** (Byte 0 of 32-bit address space): xxxx-xxxx xxxx-xxxx xxxx-xxxx AAAA-AAAA (Byte 0 of 24-bit address space): xxxx-xxxx xxxx-xxxx AAAA-AAAA (Byte 0 of 8-bit address space): AAAA-AAAA **1: Local address for Octal Mode Enable Volatile bit is found in Byte 1 of 32-bit address:** xxxx-xxxx xxxx-xxxx AAAA-AAAA xxxx-xxxx (This option may also be used for 24-bit addressing, but is not applicable for devices using 8-bit addressing)
26-24	**Bit location of Octal Mode Enable Volatile bit in register**
23-16	**If Bit 28 is 1: Address of register where bit is located** Local address AAAA-AAAA **If Bit 28 is 0: Modes supported and dummy cycles used for direct command** Bit 23: 1: 8D-8D-8D mode supported, using the # of dummy cycles shown in bits 19-16 0: 8D-8D-8D mode not supported, using the # of dummy cycles shown in bits 19-16 Bit 22: 1: 8S-8S-8S mode supported, using the # of dummy cycles shown in bits 19-16 0: 8S-8S-8S mode not supported, using the # of dummy cycles shown in bits 19-16 Bit 21: 1: 4S-4D-4D mode supported, using the # of dummy cycles shown in bits 19-16 0: 4S-4D-4D mode not supported, using the # of dummy cycles shown in bits 19-16 Bit 20: 1: 4S-4S-4S mode supported, using the # of dummy cycles shown in bits 19-16 0: 4S-4S-4S mode not supported, using the # of dummy cycles shown in bits 19-16 Bits 19-16: Number of dummy cycles (0-15) used NOTE 1S-1S-1S mode, if supported by the device, will be supporting this command without using dummy cycles. NOTE Modes indicated as not supported may still be supported by the device, but not using the same number of dummy cycles as listed here. NOTE Other modes may also be supported by the device.
15-8	**Command used for read access** 00h means not supported
7-0	**Command used for write access** 00h means not supported

6.10.19 SCCR Map for SPI Memory Devices Parameter Table: 17th DWORD – Octal Mode Enable-Non-volatile

Bits	Description
31	**Octal Mode Enable Non-volatile bit available:** 0: Not supported 1: Supported
30	**Octal Mode Enable Non-volatile bit polarity:** 0: Positive (Octal Mode Enable bit = 1 means Octal mode is enabled) 1: Inverted (Octal Mode Enable bit = 0 means Octal mode is enabled)
29	**OTP bit** 0: Bit can be changed multiple times 1: Bit is an OTP bit that can only be set once.
28	**Bit is accessed by commands using address** 0: Bit is accessed by direct commands (Commands do not use address) 1: Bit is accessed by commands using address
27	**0: Local address for Octal Mode Enable Non-volatile bit is found in last byte of the address:** (Byte 0 of 32-bit address space): xxxx-xxxx xxxx-xxxx xxxx-xxxx AAAA-AAAA (Byte 0 of 24-bit address space): xxxx-xxxx xxxx-xxxx AAAA-AAAA (Byte 0 of 8-bit address space): AAAA-AAAA **1: Local address for Octal Mode Enable Non-volatile bit is found in Byte 1 of 32-bit address:** xxxx-xxxx xxxx-xxxx AAAA-AAAA xxxx-xxxx (This option may also be used for 24-bit addressing, but is not applicable for devices using 8-bit addressing)
26-24	**Bit location of Octal Mode Enable Non-volatile bit in register**
23-16	**If Bit 28 is 1: Address of register where bit is located** Local address AAAA-AAAA **If Bit 28 is 0: Modes supported and dummy cycles used for direct command** Bit 23: 1: 8D-8D-8D mode supported, using the # of dummy cycles shown in bits 19-16 0: 8D-8D-8D mode not supported, using the # of dummy cycles shown in bits 19-16 Bit 22: 1: 8S-8S-8S mode supported, using the # of dummy cycles shown in bits 19-16 0: 8S-8S-8S mode not supported, using the # of dummy cycles shown in bits 19-16 Bit 21: 1: 4S-4D-4D mode supported, using the # of dummy cycles shown in bits 19-16 0: 4S-4D-4D mode not supported, using the # of dummy cycles shown in bits 19-16 Bit 20: 1: 4S-4S-4S mode supported, using the # of dummy cycles shown in bits 19-16 0: 4S-4S-4S mode not supported, using the # of dummy cycles shown in bits 19-16 Bits 19-16: Number of dummy cycles (0-15) used NOTE 1S-1S-1S mode, if supported by the device, will be supporting this command without using dummy cycles. NOTE Modes indicated as not supported may still be supported by the device, but not using the same number of dummy cycles as listed here. NOTE Other modes may also be supported by the device.
15-8	**Command used for read access** 00h means not supported
7-0	**Command used for write access** 00h means not supported

6.10.20 SCCR Map for SPI Memory Devices Parameter Table: 18th DWORD – STR or DTR Mode Select – Volatile

Bits	Description
31	**STR or DTR mode select Volatile bit available:** 0: Not supported 1: Supported
30	**STR or DTR mode select Volatile bit polarity:** 0: Positive (STR or DTR mode select bit = 0 means STR mode, 1 means DTR mode) 1: Inverted (STR or DTR mode select bit = 1 means STR mode, 0 means DTR mode)
29	**Reserved. Leave as "0".** (This allows new features to be added to these bits in the future.)
28	**Bit is accessed by commands using address** 0: Bit is accessed by direct commands (Commands do not use address) 1: Bit is accessed by commands using address
27	**0: Local address for STR or DTR mode select Volatile bit is found in last byte of the address:** (Byte 0 of 32-bit address space): xxxx-xxxx xxxx-xxxx xxxx-xxxx AAAA-AAAA (Byte 0 of 24-bit address space): xxxx-xxxx xxxx-xxxx AAAA-AAAA (Byte 0 of 8-bit address space): AAAA-AAAA **1: Local address for STR or DTR mode select Volatile bit is found in Byte 1 of 32-bit address:** xxxx-xxxx xxxx-xxxx AAAA-AAAA xxxx-xxxx (This option may also be used for 24-bit addressing, but is not applicable for devices using 8-bit addressing)
26-24	**Bit location of STR or DTR mode select Volatile bit in register**
23-16	**If Bit 28 is 1: Address of register where bit is located** Local address AAAA-AAAA **If Bit 28 is 0: Modes supported and dummy cycles used for direct command** Bit 23: 1: 8D-8D-8D mode supported, using the # of dummy cycles shown in bits 19-16 0: 8D-8D-8D mode not supported, using the # of dummy cycles shown in bits 19-16 Bit 22: 1: 8S-8S-8S mode supported, using the # of dummy cycles shown in bits 19-16 0: 8S-8S-8S mode not supported, using the # of dummy cycles shown in bits 19-16 Bit 21: 1: 4S-4D-4D mode supported, using the # of dummy cycles shown in bits 19-16 0: 4S-4D-4D mode not supported, using the # of dummy cycles shown in bits 19-16 Bit 20: 1: 4S-4S-4S mode supported, using the # of dummy cycles shown in bits 19-16 0: 4S-4S-4S mode not supported, using the # of dummy cycles shown in bits 19-16 Bits 19-16: Number of dummy cycles (0-15) used NOTE 1S-1S-1S mode, if supported by the device, will be supporting this command without using dummy cycles. NOTE Modes indicated as not supported may still be supported by the device, but not using the same number of dummy cycles as listed here. NOTE Other modes may also be supported by the device.
15-8	**Command used for read access** 00h means not supported
7-0	**Command used for write access** 00h means not supported

6.10.21 SCCR Map for SPI Memory Devices Parameter Table: 19th DWORD – STR or DTR Mode Select – Non-volatile

Bits	Description
31	**STR or DTR mode select Non-volatile bit available:** 0: Not supported 1: Supported
30	**STR or DTR mode select Non-volatile bit polarity:** 0: Positive (STR or DTR mode select bit = 0 means STR mode, 1 means DTR mode) 1: Inverted (STR or DTR mode select bit = 1 means STR mode, 0 means DTR mode)
29	**Reserved. Leave as "0".** (This allows new features to be added to these bits in the future.)
28	**Bit is accessed by commands using address** 0: Bit is accessed by direct commands (Commands do not use address) 1: Bit is accessed by commands using address
27	**0: Local address for STR or DTR mode select Non-volatile bit is found in last byte of the address:** (Byte 0 of 32-bit address space): xxxx-xxxx xxxx-xxxx xxxx-xxxx AAAA-AAAA (Byte 0 of 24-bit address space): xxxx-xxxx xxxx-xxxx AAAA-AAAA (Byte 0 of 8-bit address space): AAAA-AAAA **1: Local address for STR or DTR mode select Non-volatile bit is found in Byte 1 of 32-bit address:** xxxx-xxxx xxxx-xxxx AAAA-AAAA xxxx-xxxx (This option may also be used for 24-bit addressing, but is not applicable for devices using 8-bit addressing)
26-24	**Bit location of STR or DTR mode select Non-volatile bit in register**
23-16	**If Bit 28 is 1: Address of register where bit is located** Local address AAAA-AAAA **If Bit 28 is 0: Modes supported and dummy cycles used for direct command** Bit 23: 1: 8D-8D-8D mode supported, using the # of dummy cycles shown in bits 19-16 0: 8D-8D-8D mode not supported, using the # of dummy cycles shown in bits 19-16 Bit 22: 1: 8S-8S-8S mode supported, using the # of dummy cycles shown in bits 19-16 0: 8S-8S-8S mode not supported, using the # of dummy cycles shown in bits 19-16 Bit 21: 1: 4S-4D-4D mode supported, using the # of dummy cycles shown in bits 19-16 0: 4S-4D-4D mode not supported, using the # of dummy cycles shown in bits 19-16 Bit 20: 1: 4S-4S-4S mode supported, using the # of dummy cycles shown in bits 19-16 0: 4S-4S-4S mode not supported, using the # of dummy cycles shown in bits 19-16 Bits 19-16: Number of dummy cycles (0-15) used NOTE 1S-1S-1S mode, if supported by the device, will be supporting this command without using dummy cycles. NOTE Modes indicated as not supported may still be supported by the device, but not using the same number of dummy cycles as listed here. NOTE Other modes may also be supported by the device.
15-8	**Command used for read access** 00h means not supported
7-0	**Command used for write access** 00h means not supported

6.10.22 SCCR Map for SPI Memory Devices Parameter Table: 20th DWORD – STR Octal Mode Enable – Volatile

Bits	Description
31	**STR Octal Mode Enable Volatile bit available:** 0: Not supported 1: Supported
30	**STR Octal Mode Enable Volatile bit polarity:** 0: Positive (STR Octal Mode Enable = 1 means STR Octal Mode is enabled) 1: Inverted (STR Octal Mode Enable = 0 means STR Octal Mode is enabled)
29	**Reserved. Leave as "0".** (This allows new features to be added to these bits in the future.)
28	**Bit is accessed by commands using address** 0: Bit is accessed by direct commands (Commands do not use address) 1: Bit is accessed by commands using address
27	**0: Local address for STR Octal Mode Enable Volatile bit is found in last byte of the address** (Byte 0 of 32-bit address space): xxxx-xxxx xxxx-xxxx xxxx-xxxx AAAA-AAAA (Byte 0 of 24-bit address space): xxxx-xxxx xxxx-xxxx AAAA-AAAA (Byte 0 of 8-bit address space): AAAA-AAAA **1: Local address for STR Octal Mode Enable Volatile bit is found in Byte 1 of 32-bit address:** xxxx-xxxx xxxx-xxxx AAAA-AAAA xxxx-xxxx (This option may also be used for 24-bit addressing, but is not applicable for devices using 8-bit addressing)
26-24	**Bit location of STR Octal Mode Enable Volatile bit in register**
23-16	**If Bit 28 is 1: Address of register where bit is located** Local address AAAA-AAAA **If Bit 28 is 0: Modes supported and dummy cycles used for direct command** Bit 23: 1: 8D-8D-8D mode supported, using the # of dummy cycles shown in bits 19-16 0: 8D-8D-8D mode not supported, using the # of dummy cycles shown in bits 19-16 Bit 22: 1: 8S-8S-8S mode supported, using the # of dummy cycles shown in bits 19-16 0: 8S-8S-8S mode not supported, using the # of dummy cycles shown in bits 19-16 Bit 21: 1: 4S-4D-4D mode supported, using the # of dummy cycles shown in bits 19-16 0: 4S-4D-4D mode not supported, using the # of dummy cycles shown in bits 19-16 Bit 20: 1: 4S-4S-4S mode supported, using the # of dummy cycles shown in bits 19-16 0: 4S-4S-4S mode not supported, using the # of dummy cycles shown in bits 19-16 Bits 19-16: Number of dummy cycles (0-15) used NOTE 1S-1S-1S mode, if supported by the device, will be supporting this command without using dummy cycles. NOTE Modes indicated as not supported may still be supported by the device, but not using the same number of dummy cycles as listed here. NOTE Other modes may also be supported by the device.
15-8	**Command used for read access** 00h means not supported
7-0	**Command used for write access** 00h means not supported

6.10.23 SCCR Map for SPI Memory Devices Parameter Table: 21st DWORD – STR Octal Mode Enable - Non-volatile

Bits	Description
31	**STR Octal Mode Enable Non-volatile bit available:** 0: Not supported 1: Supported
30	**STR Octal Mode Enable Non-volatile bit polarity:** 0: Positive (STR Octal Mode Enable = 1 means STR Octal Mode is enabled) 1: Inverted (STR Octal Mode Enable = 0 means STR Octal Mode is enabled)
29	**OTP bit** 0: STR Octal Mode Enable Non-volatile Bit can be changed multiple times 1: STR Octal Mode Enable Non-volatile Bit is an OTP bit that can only be set once.
28	**Bit is accessed by commands using address** 0: Bit is accessed by direct commands (Commands do not use address) 1: Bit is accessed by commands using address
27	**0: Local address for STR Octal Mode Enable Non-volatile bit is found in last byte of the address** (Byte 0 of 32-bit address space): xxxx-xxxx xxxx-xxxx xxxx-xxxx AAAA-AAAA (Byte 0 of 24-bit address space): xxxx-xxxx xxxx-xxxx AAAA-AAAA (Byte 0 of 8-bit address space): AAAA-AAAA **1: Local address for STR Octal Mode Enable Non-volatile bit is found in Byte 1 of 32-bit address:** xxxx-xxxx xxxx-xxxx AAAA-AAAA xxxx-xxxx (This option may also be used for 24-bit addressing, but is not applicable for devices using 8-bit addressing)
26-24	**Bit location of STR Octal Mode Enable Non-volatile bit in register**
23-16	**If Bit 28 is 1: Address of register where bit is located** Local address AAAA-AAAA **If Bit 28 is 0: Modes supported and dummy cycles used for direct command** Bit 23: 1: 8D-8D-8D mode supported, using the # of dummy cycles shown in bits 19-16 0: 8D-8D-8D mode not supported, using the # of dummy cycles shown in bits 19-16 Bit 22: 1: 8S-8S-8S mode supported, using the # of dummy cycles shown in bits 19-16 0: 8S-8S-8S mode not supported, using the # of dummy cycles shown in bits 19-16 Bit 21: 1: 4S-4D-4D mode supported, using the # of dummy cycles shown in bits 19-16 0: 4S-4D-4D mode not supported, using the # of dummy cycles shown in bits 19-16 Bit 20: 1: 4S-4S-4S mode supported, using the # of dummy cycles shown in bits 19-16 0: 4S-4S-4S mode not supported, using the # of dummy cycles shown in bits 19-16 Bits 19-16: Number of dummy cycles (0-15) used NOTE 1S-1S-1S mode, if supported by the device, will be supporting this command without using dummy cycles. NOTE Modes indicated as not supported may still be supported by the device, but not using the same number of dummy cycles as listed here. NOTE Other modes may also be supported by the device.
15-8	**Command used for read access** 00h means not supported
7-0	**Command used for write access** 00h means not supported

6.10.24 SCCR Map for SPI Memory Devices Parameter Table: 22nd DWORD – DTR Octal Mode Enable – Volatile

Bits	Description
31	**DTR Octal Mode Enable Volatile bit available:** 0: Not supported 1: Supported
30	**DTR Octal Mode Enable Volatile bit polarity:** 0: Positive (DSTR Octal Mode Enable = 1 means DTR Octal Mode is enabled) 1: Inverted (DTR Octal Mode Enable = 0 means DTR Octal Mode is enabled)
29	**Reserved. Leave as "0".** (This allows new features to be added to these bits in the future.)
28	**Bit is accessed by commands using address** 0: Bit is accessed by direct commands (Commands do not use address) 1: Bit is accessed by commands using address
27	**0: Local address for DTR Octal Mode Enable - Volatile bit is found in last byte of the address:** (Byte 0 of 32-bit address space): xxxx-xxxx xxxx-xxxx xxxx-xxxx AAAA-AAAA (Byte 0 of 24-bit address space): xxxx-xxxx xxxx-xxxx AAAA-AAAA (Byte 0 of 8-bit address space): AAAA-AAAA **1: Local address for DTR Octal Mode Enable - Volatile bit is found in Byte 1 of 32-bit address:** xxxx-xxxx xxxx-xxxx AAAA-AAAA xxxx-xxxx (This option may also be used for 24-bit addressing, but is not applicable for devices using 8-bit addressing)
26-24	**Bit location of STR Octal Mode Enable Volatile bit in register**
23-16	**If Bit 28 is 1: Address of register where bit is located** Local address AAAA-AAAA **If Bit 28 is 0: Modes supported and dummy cycles used for direct command** Bit 23: 1: 8D-8D-8D mode supported, using the # of dummy cycles shown in bits 19-16 0: 8D-8D-8D mode not supported, using the # of dummy cycles shown in bits 19-16 Bit 22: 1: 8S-8S-8S mode supported, using the # of dummy cycles shown in bits 19-16 0: 8S-8S-8S mode not supported, using the # of dummy cycles shown in bits 19-16 Bit 21: 1: 4S-4D-4D mode supported, using the # of dummy cycles shown in bits 19-16 0: 4S-4D-4D mode not supported, using the # of dummy cycles shown in bits 19-16 Bit 20: 1: 4S-4S-4S mode supported, using the # of dummy cycles shown in bits 19-16 0: 4S-4S-4S mode not supported, using the # of dummy cycles shown in bits 19-16 Bits 19-16: Number of dummy cycles (0-15) used NOTE 1S-1S-1S mode, if supported by the device, will be supporting this command without using dummy cycles. NOTE Modes indicated as not supported may still be supported by the device, but not using the same number of dummy cycles as listed here. NOTE Other modes may also be supported by the device.
15-8	**Command used for read access** 00h means not supported
7-0	**Command used for write access** 00h means not supported

6.10.25 SCCR Map for SPI Memory Devices Parameter Table: 23rd DWORD – DTR Octal Mode Enable – Non-volatile

Bits	Description
31	**DTR Octal Mode Enable Non-volatile bit available:** 0: Not supported 1: Supported
30	**DTR Octal Mode Enable Non-volatile bit polarity:** 0: Positive (DSTR Octal Mode Enable = 1 means DTR Octal Mode is enabled) 1: Inverted (DTR Octal Mode Enable = 0 means DTR Octal Mode is enabled)
29	**OTP bit** 0: DTR Octal Mode Enable – Non-volatile Bit can be changed multiple times 1: DTR Octal Mode Enable – Non-volatile Bit is an OTP bit that can only be set once.
28	**Bit is accessed by commands using address** 0: Bit is accessed by direct commands (Commands do not use address) 1: Bit is accessed by commands using address
27	**0: Local address for DTR Octal Mode Enable – Non-volatile bit is found in last byte of the address** (Byte 0 of 32-bit address space): xxxx-xxxx xxxx-xxxx xxxx-xxxx AAAA-AAAA (Byte 0 of 24-bit address space): xxxx-xxxx xxxx-xxxx AAAA-AAAA (Byte 0 of 8-bit address space): AAAA-AAAA **1: Local address for DTR Octal Mode Enable – Non-volatile bit is found in Byte 1 of 32-bit address:** xxxx-xxxx xxxx-xxxx AAAA-AAAA xxxx-xxxx (This option may also be used for 24-bit addressing, but is not applicable for devices using 8-bit addressing)
26-24	**Bit location of STR Octal Mode Enable Non-volatile bit in register**
23-16	**If Bit 28 is 1: Address of register where bit is located** Local address AAAA-AAAA **If Bit 28 is 0: Modes supported and dummy cycles used for direct command** Bit 23: 1: 8D-8D-8D mode supported, using the # of dummy cycles shown in bits 19-16 0: 8D-8D-8D mode not supported, using the # of dummy cycles shown in bits 19-16 Bit 22: 1: 8S-8S-8S mode supported, using the # of dummy cycles shown in bits 19-16 0: 8S-8S-8S mode not supported, using the # of dummy cycles shown in bits 19-16 Bit 21: 1: 4S-4D-4D mode supported, using the # of dummy cycles shown in bits 19-16 0: 4S-4D-4D mode not supported, using the # of dummy cycles shown in bits 19-16 Bit 20: 1: 4S-4S-4S mode supported, using the # of dummy cycles shown in bits 19-16 0: 4S-4S-4S mode not supported, using the # of dummy cycles shown in bits 19-16 Bits 19-16: Number of dummy cycles (0-15) used NOTE 1S-1S-1S mode, if supported by the device, will be supporting this command without using dummy cycles. NOTE Modes indicated as not supported may still be supported by the device, but not using the same number of dummy cycles as listed here. NOTE Other modes may also be supported by the device.
15-8	**Command used for read access** 00h means not supported
7-0	**Command used for write access** 00h means not supported

6.10.26 SCCR Map for SPI Memory Devices Parameter Table: 24th DWORD – DPD Status

Bits	Description
31	**Deep Power-Down (DPD) Status bit available:** 0: Not supported 1: Supported
30	**Deep Power-Down (DPD) Status bit polarity:** 0: Positive (DPD Status = 0 means device is in Deep Power-Down) 1: Inverted (DPD Status = 1 means device is in Deep Power-Down)
29	**Reserved. Leave as "0".** (This allows new features to be added to these bits in the future.)
28	**Bit is accessed by commands using address** 0: Bit is accessed by direct commands (Commands do not use address) 1: Bit is accessed by commands using address
27	**0: Local address for DPD Status bit is found in last byte of the address:** (Byte 0 of 32-bit address space): xxxx-xxxx xxxx-xxxx xxxx-xxxx AAAA-AAAA (Byte 0 of 24-bit address space): xxxx-xxxx xxxx-xxxx AAAA-AAAA (Byte 0 of 8-bit address space): AAAA-AAAA **1: Local address for DPD Status bit is found in Byte 1 of 32-bit address:** xxxx-xxxx xxxx-xxxx AAAA-AAAA xxxx-xxxx (This option may also be used for 24-bit addressing, but is not applicable for devices using 8-bit addressing)
26-24	**Bit location of DPD Status bit in register**
23-16	**If Bit 28 is 1: Address of register where bit is located** Local address AAAA-AAAA **If Bit 28 is 0: Modes supported and dummy cycles used for direct command** Bit 23: 1: 8D-8D-8D mode supported, using the # of dummy cycles shown in bits 19-16 0: 8D-8D-8D mode not supported, using the # of dummy cycles shown in bits 19-16 Bit 22: 1: 8S-8S-8S mode supported, using the # of dummy cycles shown in bits 19-16 0: 8S-8S-8S mode not supported, using the # of dummy cycles shown in bits 19-16 Bit 21: 1: 4S-4D-4D mode supported, using the # of dummy cycles shown in bits 19-16 0: 4S-4D-4D mode not supported, using the # of dummy cycles shown in bits 19-16 Bit 20: 1: 4S-4S-4S mode supported, using the # of dummy cycles shown in bits 19-16 0: 4S-4S-4S mode not supported, using the # of dummy cycles shown in bits 19-16 Bits 19-16: Number of dummy cycles (0-15) used NOTE 1S-1S-1S mode, if supported by the device, will be supporting this command without using dummy cycles. NOTE Modes indicated as not supported may still be supported by the device, but not using the same number of dummy cycles as listed here. NOTE Other modes may also be supported by the device.
15-8	**Command used for read access** 00h means not supported
7-0	**Command used for write access** 00h means not supported

6.10.27 SCCR Map for SPI Memory Devices Parameter Table: 25th DWORD – UDPD Status

Bits	Description
31	**Ultra-Deep Power-Down (UDPD) Status bit available:** 0: Not supported 1: Supported
30	**Ultra-Deep Power-Down (UDPD) Status bit polarity:** 0: Positive (UDPD Status bit = 0 means device is in Ultra-Deep Power-Down) 1: Inverted (UDPD Status bit = 1 means device is in Ultra-Deep Power-Down)
29	**Reserved. Leave as "0".** (This allows new features to be added to these bits in the future.)
28	**Bit is accessed by commands using address** 0: Bit is accessed by direct commands (Commands do not use address) 1: Bit is accessed by commands using address
27	**0: Local address for each bit is found in last byte of the address:** (Byte 0 of 32-bit address space): xxxx-xxxx xxxx-xxxx xxxx-xxxx AAAA-AAAA (Byte 0 of 24-bit address space): xxxx-xxxx xxxx-xxxx AAAA-AAAA (Byte 0 of 8-bit address space): AAAA-AAAA **1: Local address for each bit is found in Byte 1 of 32-bit address:** xxxx-xxxx xxxx-xxxx AAAA-AAAA xxxx-xxxx (This option may also be used for 24-bit addressing, but is not applicable for devices using 8-bit addressing)
26-24	**Bit location of UDPD Status bit in register**
23-16	**If Bit 28 is 1: Address of register where bit is located** Local address AAAA-AAAA **If Bit 28 is 0: Modes supported and dummy cycles used for direct command** Bit 23: 1: 8D-8D-8D mode supported, using the # of dummy cycles shown in bits 19-16 0: 8D-8D-8D mode not supported, using the # of dummy cycles shown in bits 19-16 Bit 22: 1: 8S-8S-8S mode supported, using the # of dummy cycles shown in bits 19-16 0: 8S-8S-8S mode not supported, using the # of dummy cycles shown in bits 19-16 Bit 21: 1: 4S-4D-4D mode supported, using the # of dummy cycles shown in bits 19-16 0: 4S-4D-4D mode not supported, using the # of dummy cycles shown in bits 19-16 Bit 20: 1: 4S-4S-4S mode supported, using the # of dummy cycles shown in bits 19-16 0: 4S-4S-4S mode not supported, using the # of dummy cycles shown in bits 19-16 Bits 19-16: Number of dummy cycles (0-15) used NOTE 1S-1S-1S mode, if supported by the device, will be supporting this command without using dummy cycles. NOTE Modes indicated as not supported may still be supported by the device, but not using the same number of dummy cycles as listed here. NOTE Other modes may also be supported by the device.
15-8	**Command used for read access** 00h means not supported
7-0	**Command used for write access** 00h means not supported

6.10.28 SCCR Map for SPI Memory Devices Parameter Table: 26th DWORD – Output Driver Strength - Volatile

See JEDEC Standard JESD251, *eXpanded Serial Peripheral Interface (xSPI) for Non-volatile Memory Devices*, for details about Output Driver Strength values.

Bits	Description
31-30	**Number of physical bits used to set Output Driver Strength** 00: Control bits for Variable Output Driver Strength not available (or not available in a form that can be described in this format). 01: 1 bit 10: 2 bits 11: 3 bits
29	**Reserved. Leave as "0".** (This allows new features to be added to these bits in the future.)
28	**Bits are accessed by commands using address** 0: Bits are accessed by direct commands (Commands do not use address) 1: Bits are accessed by commands using address
27	**0: Local address for each bit is found in last byte of the address:** (Byte 0 of 32-bit address space): xxxx-xxxx xxxx-xxxx xxxx-xxxx AAAA-AAAA (Byte 0 of 24-bit address space): xxxx-xxxx xxxx-xxxx AAAA-AAAA (Byte 0 of 8-bit address space): AAAA-AAAA **1: Local address for each bit is found in Byte 1 of 32-bit address:** xxxx-xxxx xxxx-xxxx AAAA-AAAA xxxx-xxxx (This option may also be used for 24-bit addressing, but is not applicable for devices using 8-bit addressing)
26-24	**Bit location of Least Significant Output Driver Strength bit in register**
23-16	**If Bit 28 is 1: Address of registers where bits are located** Local address AAAA-AAAA **If Bit 28 is 0: Modes supported and dummy cycles used for direct command** Bit 23: 1: 8D-8D-8D mode supported, using the # of dummy cycles shown in bits 19-16 0: 8D-8D-8D mode not supported, using the # of dummy cycles shown in bits 19-16 Bit 22: 1: 8S-8S-8S mode supported, using the # of dummy cycles shown in bits 19-16 0: 8S-8S-8S mode not supported, using the # of dummy cycles shown in bits 19-16 Bit 21: 1: 4S-4D-4D mode supported, using the # of dummy cycles shown in bits 19-16 0: 4S-4D-4D mode not supported, using the # of dummy cycles shown in bits 19-16 Bit 20: 1: 4S-4S-4S mode supported, using the # of dummy cycles shown in bits 19-16 0: 4S-4S-4S mode not supported, using the # of dummy cycles shown in bits 19-16 Bits 19-16: Number of dummy cycles (0-15) used NOTE 1S-1S-1S mode, if supported by the device, will be supporting this command without using dummy cycles. NOTE Modes indicated as not supported may still be supported by the device, but not using the same number of dummy cycles as listed here. NOTE Other modes may also be supported by the device.
15-8	**Command used for read access** 00h means not supported
7-0	**Command used for write access** 00h means not supported

6.10.29 SCCR Map for SPI Memory Devices Parameter Table: 27th DWORD – Output Driver Strength – Non-volatile

See JEDEC Standard JESD251, *eXpanded Serial Peripheral Interface (xSPI) for Non-volatile Memory Devices*, for details about Output Driver Strength values.

Bits	Description
31-30	**Number of physical bits used to set Output Driver Strength** 00: Control bits for Variable Output Driver Strength not available (or not available in a form that can be described in this format). 01: 1 bit 10: 2 bits 11: 3 bits
29	**Reserved. Leave as "0".** (This allows new features to be added to these bits in the future.)
28	**Bits are accessed by commands using address** 0: Bits are accessed by direct commands (Commands do not use address) 1: Bits are accessed by commands using address
27	**0: Local address for each bit is found in last byte of the address:** (Byte 0 of 32-bit address space): xxxx-xxxx xxxx-xxxx xxxx-xxxx AAAA-AAAA (Byte 0 of 24-bit address space): xxxx-xxxx xxxx-xxxx AAAA-AAAA (Byte 0 of 8-bit address space): AAAA-AAAA **1: Local address for each bit is found in Byte 1 of 32-bit address:** xxxx-xxxx xxxx-xxxx AAAA-AAAA xxxx-xxxx (This option may also be used for 24-bit addressing, but is not applicable for devices using 8-bit addressing)
26-24	**Bit location of Least Significant Output Driver Strength bit in register**
23-16	**If Bit 28 is 1: Address of registers where bits are located** Local address AAAA-AAAA **If Bit 28 is 0: Modes supported and dummy cycles used for direct command** Bit 23: 1: 8D-8D-8D mode supported, using the # of dummy cycles shown in bits 19-16 0: 8D-8D-8D mode not supported, using the # of dummy cycles shown in bits 19-16 Bit 22: 1: 8S-8S-8S mode supported, using the # of dummy cycles shown in bits 19-16 0: 8S-8S-8S mode not supported, using the # of dummy cycles shown in bits 19-16 Bit 21: 1: 4S-4D-4D mode supported, using the # of dummy cycles shown in bits 19-16 0: 4S-4D-4D mode not supported, using the # of dummy cycles shown in bits 19-16 Bit 20: 1: 4S-4S-4S mode supported, using the # of dummy cycles shown in bits 19-16 0: 4S-4S-4S mode not supported, using the # of dummy cycles shown in bits 19-16 Bits 19-16: Number of dummy cycles (0-15) used NOTE 1S-1S-1S mode, if supported by the device, will be supporting this command without using dummy cycles. NOTE Modes indicated as not supported may still be supported by the device, but not using the same number of dummy cycles as listed here. NOTE Other modes may also be supported by the device.
15-8	**Command used for read access** 00h means not supported
7-0	**Command used for write access** 00h means not supported

6.10.30 SCCR Map for SPI Memory Devices Parameter Table: 28th DWORD – Output Driver Strength Control Bit Patterns

Bits	Description
31-29	**Bit pattern to support Driver type 0** If less than 3 control bits are used to control Variable Output Driver Strength, the most significant bit(s) are unused and should be set to 0.
28-26	**Bit pattern to support Driver type 1** If less than 3 control bits are used to control Variable Output Driver Strength, the most significant bit(s) are unused and should be set to 0.
25-23	**Bit pattern to support Driver type 2** If less than 3 control bits are used to control Variable Output Driver Strength, the most significant bit(s) are unused and should be set to 0.
22-20	**Bit pattern to support Driver type 3** If less than 3 control bits are used to control Variable Output Driver Strength, the most significant bit(s) are unused and should be set to 0.
19-17	**Bit pattern to support Driver type 4** If less than 3 control bits are used to control Variable Output Driver Strength, the most significant bit(s) are unused and should be set to 0.
16-0	**Reserved. Leave as "0".** (This allows new features to be added to these bits in the future.)

6.11 Status, Control and Configuration Register Map for xSPI Profile 2.0 Memory Devices

xSPI Profile 2.0 memory devices from different manufacturers can have widely different configurations for Status, Control and Configuration registers. The Status, Control and Configuration Register Map (SCCR Map for short) defines a common nomenclature for the most common register bits and their functions, and describes how the individual bits may be accessed for a specific device.

This clause covers the SCCR Map for xSPI Profile 2.0 Octal memory devices. Single, Dual, Quad and xSPI Profile 1.0 Octal memory devices. are covered in 6.10.

The purpose of the SCCR Map is to provide a host controller with a minimum amount of information to be able to boot a system and load necessary code for the system to run. It is to be expected that the code loaded from the memory device will contain the necessary information required to achieve optimum performance from the device.

The register address is defined as a 32-bit address in the SCCR Map. For devices using less than 32 bits for Generic Addressable Read/Write Status/Control register commands, the uppermost bits should be ignored. (Sending a 32-bit address to a device expecting an 8-bit address will not produce the desired result.) The actual number of address bytes and the number of dummy bytes/dummy cycles used for Generic Addressable Read/Write Status/Control register commands by the device is provided in 6.11.5.

To avoid the need to provide a full 32-bit address for each bit, the addressing scheme in this table takes into account that every device uses a narrow range of addresses for the SCCRs. The address is therefore defined as a 32-bit offset address pointer, which indicates the start of the address block, and an 8-bit local address, which indicates the position of each register within the block. The physical address of a register is found by adding the 32-bit offset address pointer and the 8-bit local address. Separate 32-bit offset address pointers are provided for volatile and non-volatile address blocks.

The 8-bit local address can either be added to the last byte of the 32-byte address, creating an address of the format xxxx-xxxx xxxx-xxxx xxxx-xxxx AAAA-AAAA.

The 8- bit local address can be added to Byte 1 of the 32-bit address, creating an address of the format xxxx-xxxx xxxx-xxxx AAAA-AAAA xxxx-xxxx.

Which of the two options is used is described in clause 6.11.5.

In the SCCR Map, each bit is defined separately. In an actual device, multiple of these bits will be combined into one physical register (e.g., the Status Register). The physical registers may also include additional bits that are not part of the current SCCR Map. **It is therefore important that the host controller reads the current value of the register and only changes the intended bits before writing the value back to the register to ensure that other functions are not affected.** (“Read-Modify-Write” operations may be used if available.)

Even though the Status, Control and Configuration Register Map was initially developed as part of the xSPI protocol spec, this information can also be added for other devices.

Registers may be status, control, or configuration registers.

6.11.1 SCCR Map for xSPI Profile 2.0 Memory Devices Parameter Header: 1st DWORD

Bits	Description
31:24	**Parameter Table Length** This field specifies how many DWORDs are in the Parameter table. NOTE This field is 1's based. Therefore, 1 indicates 1 DWORD.
23:16	**Parameter Table Major Revision Number** This 8-bit field indicates the major revision number of the parameter table. The value in this field is 01h for this table defined by JESD216E revision (unchanged from JESD216D revision). NOTE The Major Revision of JEDEC defined parameter tables can only be modified by updates to this standard.
15:8	**Parameter Table Minor Revision Number** This 8-bit field indicates the minor revision number of the Status, Control and Configuration Register Map Parameter Table. The value in this field is 00h for this table defined by JESD216E revision (unchanged from JESD216E revision). NOTE The Minor Revision of the JEDEC owned parameter tables can only be modified by updates to this standard.
7:0	**Parameter ID LSB** The Status, Control and Configuration Register Map is assigned the ID LSB of 09h.

6.11.2 SCCR Map for xSPI Profile 2.0 Memory Devices Parameter Header: 2nd DWORD

Bits	Description
31:24	**Parameter ID MSB** The Status, Control and Configuration Register Map for xSPI Profile 2.0 Memory Devices is assigned the ID MSB of FFh.
23:0	**Parameter Table Pointer (PTP)** This address specifies the start of this header's Parameter Table in the SFDP structure. The address is in terms of bytes and must be DWORD-aligned.

6.11.3 SCCR Map for xSPI Profile 2.0 Memory Devices Parameter Table: 1st DWORD – Volatile Registers Address Offset

Bits	Description
31:0	Address offset for volatile registers

6.11.4 SCCR Map for xSPI Profile 2.0 Memory Devices Parameter Table: 2nd DWORD – Non-volatile Registers Address Offset

Bits	Description
31:0	Address offset for non-volatile registers

6.11.5 SCCR Map for xSPI Profile 2.0 Memory Devices Parameter Table: 3rd DWORD – Generic Addressable Read/Write Status/Control Register Commands

Bits	Description
31	**Generic Addressable Read Status/Control register command supported for all registers** 0: Not supported for any register 1: Supported for all registers
30	**Generic Addressable Write Status/Control register command supported for all registers** 0: Not supported for any register 1: Supported for some all registers
29:28	**Number of command/address bytes used for Generic Addressable Read/Write Status/Control register commands:** 00: 6 bytes (48-bit) 01: Reserved 10: Reserved 11: Reserved
27:23	**Number of dummy cycles used for Generic Addressable Read Status/Control volatile register command** 00000-11111:[0-31 cycles]
22:18	**Number of dummy cycles used for Generic Addressable Read Status/Control non-volatile register command** 00000-11111:[0-31 cycles]
17	**Work In Progress – Device Busy (WIP) bit available:** 0: Not supported 1: Supported
16	**Work In Progress – Device Busy (WIP) polarity:** 0: Positive (WIP=1 means write is in progress) 1: Inverted (WIP=0 means write is in progress)
15	**0: Local address for WIP bit is found in last byte of the command-address:** (Byte 0 of 48-bit command-address space): xxxx-xxxx xxxx-xxxx-xxxx-xxxx-xxxx-xxxx xxxx-xxxx AAAA-AAAA **1: Local address for WIP bit is found in Byte 1 of 48-bit command-address:** (Byte 0 of 48-bit command-address space): xxxx-xxxx xxxx-xxxx-xxxx-xxxx-xxxx-xxxx AAAA-AAAA xxxx-xxxx
14:11	**Bit location of WIP bit in register**
10:3	**Address of register where WIP is located**
2:0	**Reserved. Leave as "0".** (This allows new features to be added to these bits in the future.)

6.11.6 SCCR Map for xSPI Profile 2.0 Memory Devices Parameter Table: 4th DWORD – Program Error

Bits	Description
31	**Program Error bit available:** 0: Not supported 1: Supported
30	**Program Error bit polarity:** 0: Positive (Program Error = 0 means no error, Program Error = 1 means last Program operation created an error) 1: Inverted (Program Error = 1 means no error , Program Error = 0 means last Program operation created an error)
29	**0: Local address for Program Error bit is found in last byte of the command-address:** (Byte 0 of 48-bit command-address space): xxxx-xxxx xxxx-xxxx-xxxx-xxxx-xxxx-xxxx xxxx-xxxx AAAA-AAAA **1: Local address for Program Error bit is found in Byte 1 of 48-bit command-address:** (Byte 0 of 48-bit command-address space): xxxx-xxxx xxxx-xxxx-xxxx-xxxx-xxxx-xxxx AAAA-AAAA xxxx-xxxx
28	**Sharing** 0: Not shared: The device has separate bits for Program Error and Erase Error 1: Shared: The same bit is used for both Program Error and Erase Error
27:24	**Bit location of Program Error bit in register**
23:16	**Address of register where Program Error is located**
15:0	**Reserved. Leave as "0".** (This allows new features to be added to these bits in the future.)

6.11.7 SCCR Map for xSPI Profile 2.0 Memory Devices Parameter Table: 5th DWORD – Erase Error

Bits	Description
31	**Erase Error bit available:** 0: Not supported 1: Supported
30	**Erase Error bit polarity:** 0: Positive (Erase Error = 0 means no error, Erase Error = 1 means last Erase operation created an error) 1: Inverted (Erase Error = 1 means no error, Erase Error = 0 means last Erase operation created an error)
29	**0: Local address for Erase Error bit is found in last byte of the command-address:** (Byte 0 of 48-bit command-address space): xxxx-xxxx xxxx-xxxx-xxxx-xxxx-xxxx-xxxx xxxx-xxxx AAAA-AAAA **1: Local address for WIP bit is found in Byte 1 of 48-bit command-address:** (Byte 0 of 48-bit command-address space): xxxx-xxxx xxxx-xxxx-xxxx-xxxx-xxxx-xxxx AAAA-AAAA xxxx-xxxx
28	**Sharing** 0: Not shared: The device has separate bits for Program Error and Erase Error 1: Shared: The same bit is used for both Program Error and Erase Error
27:24	**Bit location of Erase Error bit in register**
23:16	**Address of register where Erase Error is located**
15:0	**Reserved. Leave as "0".** (This allows new features to be added to these bits in the future.)

6.11.8 SCCR Map for xSPI Profile 2.0 Memory Devices Parameter Table: 6th DWORD – Variable Dummy Cycle Settings – Volatile Register

Bits	Description
31	**Variable number of dummy cycles supported:** 0: Not supported, or supported in a way that cannot be described correctly by this parameter table 1: Supported
30	**Reserved. Leave as "0".** (This allows new features to be added to these bits in the future.)
29	**0: Local address for Variable Dummy Cycle Setting bit is found in last byte of the command-address:** (Byte 0 of 48-bit command-address space): xxxx-xxxx xxxx-xxxx-xxxx-xxxx-xxxx-xxxx xxxx-xxxx AAAA-AAAA **1: Local address for Variable Dummy Cycle Setting bit is found in Byte 1 of 48-bit command-address:** (Byte 0 of 48-bit command-address space): xxxx-xxxx xxxx-xxxx-xxxx-xxxx-xxxx-xxxx AAAA-AAAA xxxx-xxxx
28:27	**Number of physical bits used to set wait states** 00: 2 bit 01: 3 bits 10: 4 bit 11: 5 bits
26:23	**Bit location of LSb of physical bits in register**
22:15	**Address of register where Erase Error is located**
14:0	**Reserved. Leave as "0".** (This allows new features to be added to these bits in the future.)

6.11.9 SCCR Map for xSPI Profile 2.0 Memory Devices Parameter Table: 7th DWORD – Variable Dummy Cycle Settings – Non-volatile Register

Bits	Description
31	**Variable number of dummy cycles supported:** 0: Not supported, or supported in a way that cannot be described correctly by this parameter table 1: Supported
30	**Reserved. Leave as "0".** (This allows new features to be added to these bits in the future.)
29	**0: Local address for Variable Dummy Cycle Setting bit is found in last byte of the command-address:** (Byte 0 of 48-bit command-address space): xxxx-xxxx xxxx-xxxx-xxxx-xxxx-xxxx-xxxx xxxx-xxxx AAAA-AAAA **1: Local address for Variable Dummy Cycle Setting bit is found in Byte 1 of 48-bit command-address:** (Byte 0 of 48-bit command-address space): xxxx-xxxx xxxx-xxxx-xxxx-xxxx-xxxx-xxxx AAAA-AAAA xxxx-xxxx
28:27	**Number of physical bits used to set wait states** 00: 2 bit 01: 3 bits 10: 4 bit 11: 5 bits
26:23	**Bit location of LSb of physical bits in register**
22:15	**Address of register where Erase Error is located**
14:0	**Reserved. Leave as "0".** (This allows new features to be added to these bits in the future.)

6.11.10 SCCR Map for xSPI Profile 2.0 Memory Devices Parameter Table: 8th DWORD – Variable Dummy Cycle Settings – Bit Patterns

Bits	Description
31	**30 dummy cycles supported:** 0: Not supported 1: Supported
30-26	**Bit pattern used to set 30 dummy cycles:** If less than 5 physical bits are used to set dummy cycles, the least significant bits are used, and the most significant bit(s) are set to 0.
25	**28 dummy cycles supported:** 0: Not supported 1: Supported
24-20	**Bit pattern used to set 28 dummy cycles:** If less than 5 physical bits are used to set dummy cycles, the least significant bits are used, and the most significant bit(s) are set to 0.
19	**26 dummy cycles supported:** 0: Not supported 1: Supported
18-14	**Bit pattern used to set 26 dummy cycles:** If less than 5 physical bits are used to set dummy cycles, the least significant bits are used, and the most significant bit(s) are set to 0.
13	**24 dummy cycles supported:** 0: Not supported 1: Supported
12-8	**Bit pattern used to set 24 dummy cycles:** If less than 5 physical bits are used to set dummy cycles, the least significant bits are used, and the most significant bit(s) are set to 0.
7	**22 dummy cycles supported:** 0: Not supported 1: Supported
6-2	**Bit pattern used to set 22 dummy cycles:** If less than 5 physical bits are used to set dummy cycles, the least significant bits are used, and the most significant bit(s) are set to 0.
1-0	**Reserved. Leave as "0".** (This allows new features to be added to these bits in the future.)

6.11.11 SCCR Map for xSPI Profile 2.0 Memory Devices Parameter Table: 9th DWORD – Variable Dummy Cycle Settings – Bit Patterns

Bits	Description
31	**20 dummy cycles supported:** 0: Not supported 1: Supported
30-26	**Bit pattern used to set 20 dummy cycles:** If less than 5 physical bits are used to set dummy cycles, the least significant bits are used, and the most significant bit(s) are set to 0.
25	**18 dummy cycles supported:** 0: Not supported 1: Supported
24-20	**Bit pattern used to set 18 dummy cycles:** If less than 5 physical bits are used to set dummy cycles, the least significant bits are used, and the most significant bit(s) are set to 0.
19	**16 dummy cycles supported:** 0: Not supported 1: Supported
18-14	**Bit pattern used to set 16 dummy cycles:** If less than 5 physical bits are used to set dummy cycles, the least significant bits are used, and the most significant bit(s) are set to 0.
13	**14 dummy cycles supported:** 0: Not supported 1: Supported
12-8	**Bit pattern used to set 14 dummy cycles:** If less than 5 physical bits are used to set dummy cycles, the least significant bits are used, and the most significant bit(s) are set to 0.
7	**12 dummy cycles supported:** 0: Not supported 1: Supported
6-2	**Bit pattern used to set 12 dummy cycles:** If less than 5 physical bits are used to set dummy cycles, the least significant bits are used, and the most significant bit(s) are set to 0.
1-0	**Reserved. Leave as "0".** (This allows new features to be added to these bits in the future.)

6.11.12 SCCR Map for xSPI Profile 2.0 Memory Devices Parameter Table: 10th DWORD – Variable Dummy Cycle Settings – Bit Patterns

Bits	Description
31	**10 dummy cycles supported:** 0: Not supported 1: Supported
30-26	**Bit pattern used to set 10 dummy cycles:** If less than 5 physical bits are used to set dummy cycles, the least significant bits are used, and the most significant bit(s) are set to 0.
25	**8 dummy cycles supported:** 0: Not supported 1: Supported
24-20	**Bit pattern used to set 8 dummy cycles:** If less than 5 physical bits are used to set dummy cycles, the least significant bits are used, and the most significant bit(s) are set to 0.
19	**6 dummy cycles supported:** 0: Not supported 1: Supported
18-14	**Bit pattern used to set 6 dummy cycles:** If less than 5 physical bits are used to set dummy cycles, the least significant bits are used, and the most significant bit(s) are set to 0.
13	**4 dummy cycles supported:** 0: Not supported 1: Supported
12-8	**Bit pattern used to set 4 dummy cycles:** If less than 5 physical bits are used to set dummy cycles, the least significant bits are used, and the most significant bit(s) are set to 0.
7	**2 dummy cycles supported:** 0: Not supported 1: Supported
6-2	**Bit pattern used to set 2 dummy cycles:** If less than 5 physical bits are used to set dummy cycles, the least significant bits are used, and the most significant bit(s) are set to 0.
1-0	**Reserved. Leave as "0".** (This allows new features to be added to these bits in the future.)

6.11.13 SCCR Map for xSPI Profile 2.0 Memory Devices Parameter Table: 11th DWORD – Output Driver Strength - Volatile

See JEDEC Standard JESD251, *eXpanded Serial Peripheral Interface (xSPI) for Non-volatile Memory Devices*, for details about Output Driver Strength values.

Bits	Description
31:30	**Number of physical bits used to set Output Driver Strength** 00: Control bits for Variable Output Driver Strength not available (or not available in a form that can be described in this format). 01: 1 bit 10: 2 bits 11: 3 bits
29	**0: Local address for Output Driver Strength Setting bit is found in last byte of the command-address:** (Byte 0 of 48-bit command-address space): xxxx-xxxx xxxx-xxxx-xxxx-xxxx-xxxx-xxxx xxxx-xxxx AAAA-AAAA **1: Local address for Variable Dummy Cycle Setting bit is found in Byte 1 of 48-bit command-address:** (Byte 0 of 48-bit command-address space): xxxx-xxxx xxxx-xxxx-xxxx-xxxx-xxxx-xxxx AAAA-AAAA xxxx-xxxx
28:25	**Bit location of MSb of physical bits in register**
24:17	**Address of register where Erase Error is located**
16:0	**Reserved. Leave as "0".** (This allows new features to be added to these bits in the future.)

6.11.14 SCCR Map for xSPI Profile 2.0 Memory Devices Parameter Table: 12th DWORD – Output Driver Strength – Non-volatile

See JEDEC Standard JESD251, *eXpanded Serial Peripheral Interface (xSPI) for Non-volatile Memory Devices*, for details about Output Driver Strength values.

Bits	Description
31:30	**Number of physical bits used to set Output Driver Strength** 00: Control bits for Variable Output Driver Strength not available (or not available in a form that can be described in this format). 01: 1 bit 10: 2 bits 11: 3 bits
29	**0: Local address for Output Driver Strength Setting bit is found in last byte of the command-address:** (Byte 0 of 48-bit command-address space): xxxx-xxxx xxxx-xxxx-xxxx-xxxx-xxxx-xxxx xxxx-xxxx AAAA-AAAA **1: Local address for Variable Dummy Cycle Setting bit is found in Byte 1 of 48-bit command-address:** (Byte 0 of 48-bit command-address space): xxxx-xxxx xxxx-xxxx-xxxx-xxxx-xxxx-xxxx AAAA-AAAA xxxx-xxxx
28:25	**Bit location of MSb of physical bits in register**
24:17	**Address of register where Erase Error is located**
16:0	**Reserved. Leave as "0".** (This allows new features to be added to these bits in the future.)

6.11.15 SCCR Map for xSPI Profile 2.0 Memory Devices Parameter Table: 13th DWORD – Output Driver Strength Control Bit Patterns

Bits	Description
31-29	**Bit pattern to support Driver type 0** If less than 3 control bits are used to control Variable Output Driver Strength, the most significant bit(s) are unused and should be set to 0.
28-26	**Bit pattern to support Driver type 1** If less than 3 control bits are used to control Variable Output Driver Strength, the most significant bit(s) are unused and should be set to 0.
25-23	**Bit pattern to support Driver type 2** If less than 3 control bits are used to control Variable Output Driver Strength, the most significant bit(s) are unused and should be set to 0.
22-20	**Bit pattern to support Driver type 3** If less than 3 control bits are used to control Variable Output Driver Strength, the most significant bit(s) are unused and should be set to 0.
19-17	**Bit pattern to support Driver type 4** If less than 3 control bits are used to control Variable Output Driver Strength, the most significant bit(s) are unused and should be set to 0.
16-0	**Reserved. Leave as "0".** (This allows new features to be added to these bits in the future.)

6.12 Status, Control and Configuration Register Map Offsets for Multi-Chip SPI Memory Devices

For multi-chip devices, each chip (die) will follow the same Status, Control and Configuration Register Map as described in 6.10. Direct commands are not an option in this case, register bits may only be accessed by a command specifying an address and a register value.

The local address for each bit remains the same for every die in the multi-chip device, but the address offset for each die will be different. The offset for die 0 is provided in 6.10, the offset for every additional die is provided in this clause.

The length of the table indicates the number of dice in the multi-chip device. The example below indicates 4 dice, but any number from 2 and up may be used.

6.12.1 Status, Control, and Configuration Register Map Parameter Header: 1st DWORD

Bits	Description
31:24	**Parameter Table Length** This field specifies how many DWORDs are in the Parameter table. NOTE This field is 1's based. Therefore, 1 indicates 1 DWORD.
23:16	**Parameter Table Major Revision Number** This 8-bit field indicates the major revision number of the parameter table. The value in this field is 01h for this table defined by JESD216E revision (unchanged from JESD216D revision). NOTE The Major Revision of JEDEC defined parameter tables can only be modified by updates to this standard.
15:8	**Parameter Table Minor Revision Number** This 8-bit field indicates the minor revision number of the Status, Control and Configuration Register Map Parameter Table. The value in this field is 01h for this table defined by JESD216D revision. NOTE The Minor Revision of the JEDEC owned parameter tables can only be modified by updates to this standard.
7:0	**Parameter ID LSB** The Status, Control and Configuration Register Map Offsets for Multi-Chip SPI Memory Devices is assigned the ID LSB of 88h.

6.12.2 Status, Control and Configuration Register Map Parameter Header: 2nd DWORD

Bits	Description
31:24	**Parameter ID MSB** The Status, Control and Configuration Register Map is assigned the ID MSB of FFh.
23:0	**Parameter Table Pointer (PTP)** This address specifies the start of this header's Parameter Table in the SFDP structure. The address is in terms of bytes and must be DWORD-aligned.

6.12.3 Status, Control and Configuration Register Map Parameter Table: 1st DWORD – Volatile Registers Address Offset for Die 1

Bits	Description
31:0	Address offset for volatile registers

6.12.4 Status, Control and Configuration Register Map Parameter Table: 2nd DWORD – Non-volatile Registers Address Offset for Die 1

Bits	Description
31:0	Address offset for non-volatile registers

6.12.5 Status, Control and Configuration Register Map Parameter Table: 3rd DWORD – Volatile Registers Address Offset for Die 2

Bits	Description
31:0	Address offset for volatile registers

6.12.6 Status, Control and Configuration Register Map Parameter Table: 4th DWORD – Non-volatile Registers Address Offset for Die 2

Bits	Description
31:0	Address offset for non-volatile registers

6.12.7 Status, Control and Configuration Register Map Parameter Table: 5th DWORD – Volatile Registers Address Offset for Die 3

Bits	Description
31:0	Address offset for volatile registers

6.12.8 Status, Control and Configuration Register Map Parameter Table: 6th DWORD – Non-volatile Registers Address Offset for Die 3

Bits	Description
31:0	Address offset for non-volatile registers

6.13 Command Sequences to Change to Octal DDR (8D-8D-8D) Mode

To simplify hardware based host controllers, a set of simple command sequences is provided which can be executed directly by the host controller to enable

- Octal DDR read mode
- 50 ohm I/O driver strength (Driver Type 0, mandatory for xSPI devices)
- 20 dummy cycles for Read Fast commands
- Operation at 100 MHz (or higher, if supported)

This will typically be used when the host controller and target memory device are communicating in single SPI mode after power up, and the host controller is reading SFDP in this mode.

NOTE Using this command sequence will also change the Read SFDP behavior of the device. It is therefore recommended that the host reads all SFDP data from the device before changing modes.

For xSPI devices that do not boot in single SPI mode, this command sequence may not be applicable or required. If the device boots in Octal DDR mode with the above parameters set as default, no change is required. If the device settings after boot are different than described above, these sequences may be implemented to give the host controller an option to change to this operation mode. The host controller will have to determine the boot mode in this case as described in clause 4.5.

The host will have to send several command sequences of varying length to the xSPI device.

Each command sequence starts with CS pulled low, followed by one or more bytes of data clocked in on the SI/IO0 line (or multiple IO lines for other modes than single SPI mode) and finally CS is pulled high at the end. Each command sequence consists of 2 DWORDs (8 bytes) in the JEDEC xSPI (Profile 1.0) Parameter Table. The first byte of each command sequence indicates the length of the sequence (0 to 7 bytes), the following 7 indicates the byte values to be output by the host controller. A length of 0 indicates that the sequence is not required. For a length less than 7, the remaining values in the tables can be ignored. (They will typically be set to 0 by the device manufacturer, but may contain any value.) Up to 4 command sequences are supported. Command Sequence 1 and 3 (if required) will typically contain the Write Enable commands required for Command sequence 2 and 4.

It is important that the host controller outputs exactly the correct number of clock cycles as indicated by the length of each command sequence (8 per byte for single SPI mode), as the target device may ignore a command sequence that does not contain the correct number of clock cycles.

6.13.1 Command Sequences to Change to Octal DDR (8D-8D-8D) Mode, Parameter Header: 1st DWORD

Bits	Description
31:24	**Parameter Table Length** This field specifies how many DWORDs are in the Parameter table. NOTE This field is 1's based. Therefore, 1 indicates 1 DWORD. The Parameter Table length indicates how much of the Parameter Table is included in a device. If the parameters at the end of the Parameter Table are not applicable for a device, these entries may be omitted to save space.
23:16	**Parameter Table Major Revision Number** This 8-bit field indicates the major revision number of the parameter table. The value in this field is 01h for this table defined by JESD216E revision (unchanged from JESD216D revision). NOTE The Major Revision of JEDEC defined parameter tables can only be modified by updates to this standard.
15:8	**Parameter Table Minor Revision Number** This 8-bit field indicates the minor revision number of the Sector Map parameter table. The value in this field is 00h for this table defined by JESD216E revision (unchanged from JESD216D revision). NOTE The Minor Revision of the JEDEC owned parameter tables can only be modified by updates to this standard.
7:0	**Parameter ID LSB** The Command Sequences to Change to Octal DDR (8D-8D-8D) mode is assigned the ID LSB of 0Ah.

6.13.2 Command Sequences to Change to Octal DDR (8D-8D-8D) Mode, Parameter Header: 2nd DWORD

Bits	Description
31:24	**Parameter ID MSB** The Command Sequences to Change to Octal DDR (8D-8D-8D) is assigned the ID MSB of FFh.
23:0	**Parameter Table Pointer (PTP)** This address specifies the start of this header's Parameter Table in the SFDP structure. The address is in terms of bytes and must be DWORD-aligned.

6.13.3 Command Sequences to Change to Octal DDR (8D-8D-8D) Mode, Parameter Table: 1st DWORD - First Command Sequence

Bits	Description
31-24	**Length of first command sequence (0 if not implemented)**
23:16	**Byte 1 of first command sequence**
15:8	**Byte 2 of first command sequence (if required)**
7:0	**Byte 3 of first command sequence (if required)**

6.13.4 Command Sequences to Change to Octal DDR (8D-8D-8D) Mode, Parameter Table: 2nd DWORD - First Command Sequence (continued)

Bits	Description
31-24	**Byte 4 of first command sequence (if required)**
23:16	**Byte 5 of first command sequence (if required)**
15:8	**Byte 6 of first command sequence (if required)**
7:0	**Byte 7 of first command sequence (if required)**

6.13.5 Command Sequences to Change to Octal DDR (8D-8D-8D) Mode, Parameter Table: 3rd DWORD - 2nd Command Sequence

Bits	Description
31-24	**Length of 2nd command sequence (0 if not implemented)**
23:16	**Byte 1 of 2nd command sequence**
15:8	**Byte 2 of 2nd command sequence (if required)**
7:0	**Byte 3 of 2nd command sequence (if required)**

6.13.6 Command Sequences to Change to Octal DDR (8D-8D-8D) Mode, Parameter Table: 4th DWORD - 2nd Command Sequence (continued)

Bits	Description
31-24	**Byte 4 of 2nd command sequence (if required)**
23:16	**Byte 5 of 2nd command sequence (if required)**
15:8	**Byte 6 of 2nd command sequence (if required)**
7:0	**Byte 7 of 2nd command sequence (if required)**

6.13.7 Command Sequences to Change to Octal DDR (8D-8D-8D) Mode, Parameter Table: 5th DWORD - 3rd Command Sequence

Bits	Description
31-24	**Length of 3rd command sequence (0 if not implemented)**
23:16	**Byte 1 of 3rd command sequence**
15:8	**Byte 2 of 3rd command sequence (if required)**
7:0	**Byte 3 of 3rd command sequence (if required)**

6.13.8 Command Sequences to Change to Octal DDR (8D-8D-8D) Mode, Parameter Table: 6th DWORD - 3rd Command Sequence (continued)

Bits	Description
31-24	**Byte 4 of 3rd command sequence (if required)**
23:16	**Byte 5 of 3rd command sequence (if required)**
15:8	**Byte 6 of 3rd command sequence (if required)**
7:0	**Byte 7 of 3rd command sequence (if required)**

6.13.9 Command Sequences to Change to Octal DDR (8D-8D-8D) mode, Parameter Table: 7th DWORD - 4th Command Sequence

Bits	Description
31-24	**Length of 4th command sequence (0 if not implemented)**
23:16	**Byte 1 of 4th command sequence**
15:8	**Byte 2 of 4th command sequence (if required)**
7:0	**Byte 3 of 4th command sequence (if required)**

6.13.10 Command Sequences to Change to Octal DDR (8D-8D-8D) mode, Parameter Table: 8th DWORD - 4th Command Sequence (continued)

Bits	Description
31-24	**Byte 4 of 4th command sequence (if required)**
23:16	**Byte 5 of 4th command sequence (if required)**
15:8	**Byte 6 of 4th command sequence (if required)**
7:0	**Byte 7 of 4th command sequence (if required)**

6.14 x4 Quad IO with DS Parameter Header and Table

See JESD251-1, Addendum No. 1 to JESD251 – Optional x4 Quad I/O with Data Strobe for details about this interface.

6.14.1 x4 Quad IO with DS Parameter Header: 1st DWORD

Bits	Description
31:24	**Parameter Table Length** This field specifies how many DWORDs are in the Parameter table. NOTE This field is 1's based. Therefore, 1 indicates 1 DWORD.
23:16	**Parameter Table Major Revision Number** This 8-bit field indicates the major revision number of the parameter table. The value in this field is 01h for this table defined by JESD216D revision. NOTE The Major Revision of JEDEC defined parameter tables can only be modified by updates to this standard.
15:8	**Parameter Table Minor Revision Number** This 8-bit field indicates the minor revision number of the Sector Map parameter table. The value in this field is 00h for this table defined by JESD216D revision. NOTE The Minor Revision of the JEDEC owned parameter tables can only be modified by updates to this standard.
7:0	**Parameter ID LSB** The eXtended Serial Peripheral Interface is assigned the ID LSB of 0Ch.

6.14.2 x4 Quad IO with DS Parameter Header: 2nd DWORD

Bits	Description
31:24	**Parameter ID MSB** The eXtended Serial Peripheral Interface is assigned the ID MSB of FFh.
23:0	**Parameter Table Pointer (PTP)** This address specifies the start of this header's Parameter Table in the SFDP structure. The address is in terms of bytes and must be DWORD-aligned.

6.14.3 x4 Quad IO with DS Parameter Table: 1st DWORD - Command Codes Used in 4S-4D-4D Protocol Mode

The commands listed here are those that have more than one option for Command Code listed in "Table 2 Profile 1.0 commands used in 4S-4D-4D protocol mode (required commands)" or in "Table 3: Profile 1.0 commands used in 4S-4D-4D protocol mode (optional commands)" in the x4 Addendum to the xSPI standard JESD251 (JESD251-1).

The opcodes for the Erase commands are provided in clauses 6.4.11 to 6.4.12, and are therefore not repeated here.

For the optional commands that are not supported as indicated in 3rd DWORD below, the parameter fields in this DWORD are not applicable.

Bits	Description
31	**SFDP Command in 4S-4D-4D mode – Address Bytes** See Figure 4 — Read SFDP (4S-4D-4D) Mode Timing Diagram 0b: 32-bit address (For most devices, SFDP is still limited to a 24-bit address space. This means MSB is 0, and the 24-bit address is in the last 3 bytes) 1b: 24-bit address, left adjusted (24-bit address is in the first 3 bytes, LSB is 0)
30	**SFDP Command in 4S-4D-4D mode – Dummy Cycles** See Figure 4 — Read SFDP (4S-4D-4D) Mode Timing Diagram 0b: 8 1b: 20
29	**Number of Additional Modifier Bytes Used for Read Status Register command** 1: 4 bytes 0: 0 bytes
28	**Initial Latency (CK cycles) for Read Status Register command** 1: 8 CK cycles 0: 4 CK cycles
27	**Number of Additional Modifier Bytes Used for Read Register command** 1: 4 bytes 0: 1 byte
26	**Initial Latency (CK cycles) for Read Volatile Register command** 1: 8 CK cycles 0: 4 CK cycles
25	**Initial Latency (CK cycles) for Read Non-volatile Register command** 1: 8 CK cycles 0: 4 CK cycles
24	**Number of Additional Modifier Bytes Used for Write Status-Cfg Register command** 1: 4 bytes 0: 0 bytes

6.14.3 x4 Quad IO with DS Parameter Table: 1st DWORD - Command Codes Used in 4S-4D-4D Protocol Mode (cont'd)

Bits	Description
23	**Number of Additional Modifier Bytes Used for Write Register command** 1: 4 bytes 0: 1 byte
22	**Number of Data Bytes Used for Write Register command** 1: 2 bytes 0: 1 byte
21:16	**Reserved. Leave as "0".** (This allows new features to be added to these bits in the future.)
15:8	**Read Fast command**
7:0	**Read Fast Wrapped command** 00h means not supported

6.14.4 x4 Quad IO with DS Parameter Table: 2nd DWORD - Command Codes Used in 4S-4D-4D Protocol Mode

Bits	Description
31-24	**Read Volatile Register command**
23:16	**Read NV Register command**
15:8	**Write Volatile Register command**
7:0	**Write NV Register command**

6.14.5 x4 Quad IO with DS Parameter Table: 3rd DWORD - Memory Commands Supported in 4S-4D-4D Protocol Mode

This is the list of *optional* commands in 4S-4D-4D protocol mode. The command code for each of these is found in Table 3 in the x4 xSPI Addendum to the xSPI standard JESD251 (JESD251-1). For the commands that have more than one option for Command Code listed in the xSPI standard, the command code for each of these is found in the JEDEC xSPI (Profile 1.0) Parameter Table: 1st to 2nd DWORD above. Table 6-2 in the xSPI standard lists the required commands for this profile. The required commands are not listed here.

6.14.6 x4 Quad IO with DS Parameter Table: 4th DWORD - Dummy Cycles Used for Various Frequencies

Bits	Description
31-12	**Reserved. Leave as "0".** (This allows new features to be added to these bits in the future.)
11:7	**200 MHz operation: number of dummy cycles required** A value of 0 means this frequency is not supported
6:2	**200 MHz operation: configuration bit pattern to set this number of dummy cycles**
1:0	**Reserved. Leave as "0".** (This allows new features to be added to these bits in the future.)

6.14.7 x4 Quad IO with DS Parameter Table: 5th DWORD - Dummy Cycles Used for Various Frequencies

Bits	Description
31-27	**166 MHz operation: number of dummy cycles required** A value of 0 means this frequency is not supported
26:22	**166 MHz operation: configuration bit pattern to set this number of dummy cycles**
21:17	**133 MHz operation: number of dummy cycles required** A value of 0 means this frequency is not supported
16:12	**133 MHz operation: configuration bit pattern to set this number of dummy cycles**
11:7	**100 MHz operation: number of dummy cycles required** A value of 0 means this frequency is not supported
6:2	**100 MHz operation: configuration bit pattern to set this number of dummy cycles**
1:0	**Reserved. Leave as "0".** (This allows new features to be added to these bits in the future.)

6.15 Command Sequences to Change to Quad DDR (4S-4D-4D) Mode

To simplify hardware based host controllers, a set of simple command sequences is provided which can be executed directly by the host controller to enable

- Quad DDR read mode
- 50 ohm I/O driver strength (Driver Type 0, mandatory for xSPI devices)
- 20 dummy cycles for Read Fast commands
- Operation at 100 MHz (or higher, if supported)

This will typically be used when the host controller and target memory device are communicating in single SPI mode after power up, and the host controller is reading SFDP in this mode.

NOTE: Using this command sequence will also change the Read SFDP behavior of the device. It is therefore recommended that the host reads all SFDP data from the device before changing modes.

For xSPI devices that do not boot in single SPI mode, this command sequence may not be applicable or required. If the device boots in Quad DDR mode with the above parameters set as default, no change is required. If the device settings after boot are different than described above, these sequences may be implemented to give the host controller an option to change to this operation mode. The host controller will have to determine the boot mode in this case as described in Clause 4.5.

The host will have to send several command sequences of varying length to the xSPI device.

Each command sequence starts with CS pulled low, followed by one or more bytes of data clocked in on the SI/IO0 line (or multiple IO lines for other modes than single SPI mode) and finally CS is pulled high at the end. Each command sequence consists of 2 DWORDs (8 bytes) in the JEDEC xSPI (Profile 1.0) Parameter Table. The first byte of each command sequence indicates the length of the sequence (0 to 7 bytes), the following 7 indicates the byte values to be output by the host controller. A length of 0 indicates that the sequence is not required. For a length less than 7, the remaining values in the tables can be ignored. (They will typically be set to 0 by the device manufacturer, but may contain any value.) Up to 4 command sequences are supported. Command Sequence 1 and 3 (if required) will typically contain the Write Enable commands required for Command sequence 2 and 4.

It is important that the host controller outputs exactly the correct number of clock cycles as indicated by the length of each command sequence (8 per byte for single SPI mode), as the target device may ignore a command sequence that does not contain the correct number of clock cycles.

6.15.1 Command Sequences to Change to Quad DDR (4S-4D-4D) mode, Parameter Header: 1st DWORD

Bits	Description
31:24	**Parameter Table Length** This field specifies how many DWORDs are in the Parameter table. NOTE This field is 1's based. Therefore, 1 indicates 1 DWORD. The Parameter Table length indicates how much of the Parameter Table is included in a device. If the parameters at the end of the Parameter Table are not applicable for a device, these entries may be omitted to save space.
23:16	**Parameter Table Major Revision Number** This 8-bit field indicates the major revision number of the parameter table. The value in this field is 01h for this table defined by JESD216D revision. NOTE The Major Revision of JEDEC defined parameter tables can only be modified by updates to this standard.
15:8	**Parameter Table Minor Revision Number** This 8-bit field indicates the minor revision number of the Sector Map parameter table. The value in this field is 00h for this table defined by JESD216D revision. NOTE The Minor Revision of the JEDEC owned parameter tables can only be modified by updates to this standard.
7:0	**Parameter ID LSB** The Command Sequences to Change to Quad DDR (4S-4D-4D) mode is assigned the ID LSB of 8Dh.

6.15.2 Command Sequences to Change to Quad DDR (4S-4D-4D) Mode, Parameter Header: 2nd DWORD

Bits	Description
31:24	**Parameter ID MSB** The Command Sequences to Change to Quad DDR (4S-4D-4D) is assigned the ID MSB of FFh.
23:0	**Parameter Table Pointer (PTP)** This address specifies the start of this header's Parameter Table in the SFDP structure. The address is in terms of bytes and must be DWORD-aligned.

6.15.3 Command Sequences to Change to Quad DDR (4S-4D-4D) Mode, Parameter Table: 1st DWORD - First Command Sequence

Bits	Description
31-24	**Length of first command sequence (0 if not implemented)**
23:16	**Byte 1 of first command sequence**
15:8	**Byte 2 of first command sequence (if required)**
7:0	**Byte 3 of first command sequence (if required)**

6.15.4 Command Sequences to Change to Quad DDR (4S-4D-4D) Mode, Parameter Table: 2nd DWORD - First Command Sequence (continued)

Bits	Description
31-24	**Byte 4 of first command sequence (if required)**
23:16	**Byte 5 of first command sequence (if required)**
15:8	**Byte 6 of first command sequence (if required)**
7:0	**Byte 7 of first command sequence (if required)**

6.15.5 Command Sequences to Change to Quad DDR (4S-4D-4D) Mode, Parameter Table: 3rd DWORD - 2nd Command Sequence

Bits	Description
31-24	**Length of 2nd command sequence (0 if not implemented)**
23:16	**Byte 1 of 2nd command sequence**
15:8	**Byte 2 of 2nd command sequence (if required)**
7:0	**Byte 3 of 2nd command sequence (if required)**

6.15.6 Command Sequences to Change to Quad DDR (4S-4D-4D) Mode, Parameter Table: 4th DWORD - 2nd Command Sequence (continued)

Bits	Description
31-24	**Byte 4 of 2nd command sequence (if required)**
23:16	**Byte 5 of 2nd command sequence (if required)**
15:8	**Byte 6 of 2nd command sequence (if required)**
7:0	**Byte 7 of 2nd command sequence (if required)**

6.15.7 Command Sequences to Change to Quad DDR (4S-4D-4D) Mode, Parameter Table: 5th DWORD - 3rd Command Sequence

Bits	Description
31-24	**Length of 3rd command sequence (0 if not implemented)**
23:16	**Byte 1 of 3rd command sequence**
15:8	**Byte 2 of 3rd command sequence (if required)**
7:0	**Byte 3 of 3rd command sequence (if required)**

6.15.8 Command Sequences to Change to Quad DDR (4S-4D-4D) Mode, Parameter Table: 6th DWORD - 3rd Command Sequence (continued)

Bits	Description
31-24	**Byte 4 of 3rd command sequence (if required)**
23:16	**Byte 5 of 3rd command sequence (if required)**
15:8	**Byte 6 of 3rd command sequence (if required)**
7:0	**Byte 7 of 3rd command sequence (if required)**

6.15.9 Command Sequences to Change to Quad DDR (4S-4D-4D) Mode, Parameter Table: 7th DWORD - 4th Command Sequence

Bits	Description
31-24	**Length of 4th command sequence (0 if not implemented)**
23:16	**Byte 1 of 4th command sequence**
15:8	**Byte 2 of 4th command sequence (if required)**
7:0	**Byte 3 of 4th command sequence (if required)**

6.15.10 Command Sequences to Change to Quad DDR (4S-4D-4D) Mode, Parameter Table: 8th DWORD - 4th Command Sequence (continued)

Bits	Description
31-24	**Byte 4 of 4th command sequence (if required)**
23:16	**Byte 5 of 4th command sequence (if required)**
15:8	**Byte 6 of 4th command sequence (if required)**
7:0	**Byte 7 of 4th command sequence (if required)**

6.16 Secure Packet READ/WRITE Parameter Header and Table

As serial flash manufacturers have adopted cryptographic security in their devices the need for a packet transfer transaction has emerged. This SFDP standard (starting with JESD216E) describes critical characteristics that allow a host to successfully utilize the Secure Packet READ and Secure Packet WRITE transactions supported on an enabled device.

6.16.1 Secure Packet READ/WRITE Parameter Header: 1st DWORD

Bits	Description
31:24	**Parameter Table Length = 04h** This field specifies how many DWORDs are in the Parameter table. NOTE This field is 1's based. Therefore, 1 indicates 1 DWORD.
23:16	**Parameter Table Major Revision Number = 01h** This 8-bit field indicates the major revision number of the parameter table. The value in this field is 01h for this table is newly defined by JESD216E revision. NOTE The Major Revision of JEDEC defined parameter tables can only be modified by updates to this standard.
15:8	**Parameter Table Minor Revision Number = 00h** This 8-bit field indicates the minor revision number of the Sector Map parameter table. The value in this field is 00h for this table is newly defined by JESD216E revision. NOTE The Minor Revision of the JEDEC owned parameter tables can only be modified by updates to this standard.
7:0	**Parameter ID LSB = 8Eh** The Secure Packet READ/WRITE Parameter Table is assigned the ID (LSB) of 8Eh.

6.16.2 Secure Packet READ/WRITE Parameter Header: 2nd DWORD

Bits	Description
31:24	**Parameter ID MSB = FFh** The Secure Packet READ/WRITE Parameter Table is assigned the ID (MSB) of FFh.
23:0	**Parameter Table Pointer (PTP)** = *manufacturer specified* This address specifies the start of this header's Parameter Table in the SFDP structure. The address is in terms of bytes and must be DWORD-aligned.

6.16.3 Secure Packet READ/WRITE Parameter Table, 1st DWORD

Bits	Description
31:30	**Number of Latency Clocks for Secure READ** (see JESD216 6.4-6.10) 00b: Same as Fast Read number of latency cycles 01b: Same as Linear/Wrapped Read number of latency clocks 10b: Reserved 11b: Reserved
29:28	**Size of Command Modifier field** 00b: 0 bytes 01b: 3 bytes 10b: 4 bytes 11b: 3 or 4 bytes (as described by Address Byte definition in JESD216 6.4.4)
27:24	**Packet Buffer Size** (largest packet size allowed) 0000b: 64 bytes 0001b: 128 bytes 0010b: 256 bytes 0011b: 512 bytes 0100b: 1024 bytes 0101b: 2048 bytes others: Reserved
23:8	**Reserved**
7:0	**Secure Packet Structure** = *manufacturer specified* xxxxxxx1b = Proprietary xxxxxx1xb = SPDM xxxxx1xxb = RPMC others = Reserved

6.16.4 Secure Packet READ/WRITE Parameter Table, 2nd DWORD

Bits	Description *(00h means that the command opcode is not supported)*
31:24	**x1 SDR Secure Packet READ Command Opcode** = *manufacturer specified*
23:16	**x1 SDR Secure Packet WRITE Command Opcode** = *manufacturer specified*
15:8	**x2 SDR Secure Packet READ Command Opcode** = *manufacturer specified*
7:0	**x2 SDR Secure Packet WRITE Command Opcode** = *manufacturer specified*

6.16.5 Secure Packet READ/WRITE Parameter Table, 3rd DWORD

Bits	Description *(00h means that the command opcode is not supported)*
31:24	**x4 SDR Secure Packet READ Command Opcode** = *manufacturer specified*
23:16	**x4 SDR Secure Packet WRITE Command Opcode** = *manufacturer specified*
15:8	**x8 SDR Secure Packet READ Command Opcode** = *manufacturer specified*
7:0	**x8 SDR Secure Packet WRITE Command Opcode** = *manufacturer specified*

6.16.6 Secure Packet READ/WRITE Parameter Table, 4th DWORD

Bits	Description *(00h means that the command opcode is not supported)*
31:24	**x4 DDR Secure Packet READ Command Opcode** = *manufacturer specified*
23:16	**x4 DDR Secure Packet WRITE Command Opcode** = *manufacturer specified*
15:8	**x8 DDR Secure Packet READ Command Opcode** = *manufacturer specified*
7:0	**x8 DDR Secure Packet WRITE Command Opcode** = *manufacturer specified*

6.17 Generic Register Access Method (GRAM) Parameter Header and Table

This SFDP parameter table defines a unified framework to access volatile and non-volatile registers (VR and NVR, respectively) **through a register address space** (using instructions with address). In some cases, dedicated instructions to access the registers are defined.

It also defines commonly used Status Register (SR), Flag Register (FR) and Interrupt Status Register (INTSR).

6.17.1 GRAM Parameter Header: 1st DWORD

Bits	Description
31:24	**Parameter Table Length = 0Ah** This field specifies how many DWORDs are in the Parameter table. NOTE This field is 1's based. Therefore, 1 indicates 1 DWORD.
23:16	**Parameter Table Major Revision Number = 01h** This 8-bit field indicates the major revision number of the parameter table. The value in this field is 01h for this table is unchanged from JESD216G revision. NOTE The Major Revision of JEDEC defined parameter tables can only be modified by updates to this standard.
15:8	**Parameter Table Minor Revision Number = 01h** This 8-bit field indicates the minor revision number of the parameter table. The value in this field is 01h for this table is incremented from JESD216G revision. NOTE: The Minor Revision of the JEDEC owned parameter tables can only be modified by updates to this standard.
7:0	**Parameter ID LSB = 0Fh** The GRAM Parameter Table is assigned the ID (LSB) of 0Fh.

6.17.2 GRAM Parameter Header: 2nd DWORD

Bits	Description
31:24	**Parameter ID MSB = FFh** The GRAM Parameter Table is assigned the ID (MSB) of FFh.
23:0	**Parameter Table Pointer (PTP)** = *manufacturer specified* This address specifies the start of this header's Parameter Table in the SFDP structure. The address is in terms of bytes and must be DWORD-aligned.

6.17.3 GRAM Parameter Table, 1st DWORD, General Information

Bits	Description
31:28	**Multi-Die Address offset for Addressable Register (VR/NVR) access:** Individual die addressable register (VR/NVR) access is supported by specifying an address offset for each die: **x001b**: Target die is identified by address bits [27:24] **x010b**: Target die is identified by address bits [31:24] **x011b**: Target die is identified by address bit [25] **x100b**: Target die is identified by address bit [27] **x111b**: Target die is identified by an address offset. Die-offsets are defined by "Status, Control and Configuration Register Map Offsets for Multi-Chip SPI Memory Devices" parameter table (refer to section 6.12). Offset for Die-0 is 00h. Other: Reserved (0)
27:24	**Active-Die Selection for Multi-Die Packages:** **0000b:** Device is a monolithic die. Die-0 is the only die and always active. **xx01b:** SW Die Select (C2h) instruction, with 1B payload containing the value used to explicitly select the active-die. **xx10b:** SW Die Select (C4h) instruction, with 1B payload containing the value used to explicitly select the active-die. **1xxxb**: Some instructions may implicitly affect the active die selection. Therefore, care should be taken to track or explicitly select the active/target die when accessing Registers. Other: Reserved (0) NOTE: Changing the Active Die affects all dies in the Stacked-Die device (i.e., all dies track the Active Die selection).
23:20	**Multi-Die Addressable-Register Read Access (RD_VR/NVR):** **0000b**: Multi-Die Register Read Access is not supported. **0001b**: Reading from the *Volatile/Non-volatile Registers (RD_VR/RD_NVR)* targets the Active Die. Refer to Active-Die Selection (bits [27:24]). **0010b**: Reading from the *Volatile/Non-volatile Registers (RD_VR/RD_NVR)* targets one of the dies, where target die is identified by an address offset. Refer to Multi-Die Address Offset (bits [31:28]). **0011b**: If address bit [28] is 0, reading from VR/NVR targets the Active Die (as in option 0001b above). Otherwise, reading from VR/NVR targets one of the dies (as in option 0010b above). Other: Reserved (0)

6.17.3 GRAM Parameter Table, 1st DWORD, General Information (cont'd)

Bits	Description
19:16	**Multi-Die Addressable-Register Write Access (WR_VR/NVR):** **0000b**: Multi-Die Register Write Access is not supported. **0001b**: Writing to the *Volatile/Non-volatile Registers (VR/NVR)* targets the active die. Refer to Active-Die Selection (bits [27:24]). **0010b**: Writing to the *Volatile/Non-volatile Registers (VR/NVR)* targets one of the dies, where target die is identified by an address offset. Refer to Multi-Die Address Offset (bits [31:28]). **0100b**: Writing to the *Volatile/Non-volatile Registers (VR/NVR)* targets all dies ("Broadcast"). **0110b**: If address bit [28] is 0, writing to VR/NVR targets all dies ("Broadcast" mode, as in option 0100b above). Otherwise, writing to VR/NVR targets one of the dies identified by an address offset (as in option 0010b above). Other: Reserved (0)
15:12	Reserved (0)
11:8	**Address Format for Addressable-Register (VR/NVR) Access Instruction:** **0000b**: No Address. Use dedicated instructions to access each register. **0001b**: 8b Address (zero padded to 16b for DOPI mode) **0010b**: 24b Address (zero padded to 32b for DOPI mode) **0100b**: 32b Address **0110b**: 24b/32b Address, depending on device addressing mode (32b for DOPI mode) Other - Reserved
7:6	Reserved (0)
5	**Address Shift:** **1b:** The specified 8b register address (AUX1, AUX2 fields) is shifted left by 8 (i.e., padded by 8'b0 LS bits). **0b:** The specified 8b register address (AUX1, AUX2 fields) is not shifted.
4	**GRAM SPI Modes:** **1b**: Device registers can be accessed using GRAM Methodology in any SPI Bus Mode that is supported by the device (e.g., SPI, QPI, SOPI, DOPI). **0b**: Device registers can be accessed using GRAM methodology only in single-SPI bus mode (1s-1s-1s). SW must revert to SPI bus mode before accessing device registers. Note: this does not relate to other Register-Access Methods supported by the device.
3:0	Reserved (0)

6.17.4 GRAM Parameter Table, 2nd DWORD, Volatile Register (VR) Access

Bits	Description
31:28	**Volatile Register (VR) Address Offset:** **x000b**: No Address Offset is needed for Volatile Register access. **x100b**: VR access is supported using a dedicated address offset (0080_0000h). This offset is added to the register *byte address* defined by AUX1 and AUX2 fields. Other: Reserved (0)
27:24	**Write Enable** for Volatile Register Write access (WR_VR): **0000b**: No preceding write enable is required. **0001b**: WR_EN (06h) is required before a WR_VR is issued. **0010b**: WR_EN (50h) is required before a WR_VR is issued. Other: Reserved
23:21	**Dummy Cycles Override:** Override number of Dummy Cycles for RD_VR instruction in Single-SPI (1S-1S-1S) bus mode: **000b**: In Single-SPI Bus Mode, use same value as all bus modes (bits [20:16]). **100b**: 0 Dummy cycles. **101b**: 4 Dummy cycles. **110b**: 8 Dummy cycles. **111b**: Reserved.
20:16	**Dummy Cycles (0-31) for Volatile Addressable-Register Read instruction (RD_VR)**
15:8	**OpCode for Volatile Addressable-Register Read instruction (RD_VR)**
7:0	**OpCode for Volatile Addressable-Register Write instruction (WR_VR)**

6.17.5 GRAM Parameter Table, 3rd DWORD: Non-volatile Addressable-Register (NVR) Access

Bits	Description
31:28	**Non-volatile Register (NVR) Address Offset:** **x000b**: No Address Offset is needed for Non-volatile Register access. **x100b**: NVR access is supported using a dedicated address offset (4000_0000h). This offset is added to the register *byte address* defined by AUX1 and AUX2 fields. Other: Reserved (0)
27:24	**Write Enable** for non-Volatile Addressable-Register Write access (WR_NVR): **0000b**: No preceding write enable is required. **0001b**: WR_EN (06h) is required before a WR_NVR is issued. **0010b**: WR_EN (50h) is required before a WR_NVR is issued. Other: Reserved
23:21	**Dummy Cycles Override:** Override number of Dummy Cycles for RD_NVR instruction in Single-SPI (1S-1S-1S) bus mode: **000b**: In Single-SPI Bus Mode, use same value as all bus modes (bits [20:16]). **100b**: 0 Dummy cycles. **101b**: 4 Dummy cycles. **110b**: 8 Dummy cycles. **111b**: Reserved.
20:16	**Dummy Cycles (0-31) for Non-volatile Addressable-Register Read instruction (RD_NVR)** Value of 1Fh represents that the number of Dummy Cycles is the same as the number of Dummy Cycles configured for the Fast-Read instruction.
15:8	**OpCode for Non-volatile Addressable-Register Read instruction (RD_NVR)** via register address space
7:0	**OpCode for Non-volatile Addressable-Register Write instruction (WR_NVR)** via register address space

6.17.6 GRAM Parameter Table, 4th DWORD, Status Register (SR)

Function Specific Register Info (FSRI) to describe the Status Register (SR):

Bits	Description
31:24	**AUX2:** This holds the instruction OpCode for direct read access of the SR.
23:16	**AUX1:** This holds the Status Register (SR) Byte Address.
15	Reserved (0)
14:12	**Dummy Cycles:** Number of Dummy Cycles for the dedicated SR read instruction (OpCode defined by AUX2): **x00b**: 0 Dummy cycles **x01b**: 4 Dummy cycles **x10b**: 8 Dummy cycles **x11b**: Per GRAM DWORD #2 (volatile) or #3 (non-volatile) bits [20:16] **1xxb**: In Single-SPI Bus Mode, use 0 Dummy Cycles. For other bus modes use the configured value (as set by bits [13:12]).
11:8	**Status Register (SR) Access:** **0000b:** *Status Register (SR)* is not covered by the GRAM. **Xxx1b**: *Status Register (SR)* is mapped to *Volatile Register (VR)* at byte address defined by AUX1 (bits [23:16]). **Xx1xb**: *Status Register (SR)* is read from the Active-Die (refer to GRAM DWORD#1 bits [27:24]), using the dedicated read instruction (RD_SR) with OpCode defined by AUX2 (bits [31:24]) Other – Reserved
7:4	Reserved (0)
3:0	**Status Register (SR):** **Xxx1b**: bit [0] of the SR is the **BUSY** bit (a.k.a. "Write In Progress (WIP) bit"). If set (1), indicates the device is busy and cannot accept new operations. **xx1xb**: bit [1] of the SR is the **Write Enable Latch (WEL)** bit. If set (1), indicates the device can accept program/erase/register-write operations. Other: Reserved

(*) If the SR is not supported, all bits of this DWORD are set to 0.

6.17.7 GRAM Parameter Table, 5th DWORD, Flag Register (FR)

Function Specific Register Info (FSRI) to describe the Flag Register (FR):
NOTE: The "Flag Register" is sometimes referred to as "Flag Status Register".

Bits	Description
31:24	**AUX2:** This holds the instruction OpCode for direct read access of the FR.
23:16	**AUX1:** This holds the Flag Register (FR) Byte Address, or the instruction OpCode for direct write access for clearing the FR (if supported, refer to bits [7:4]).
15	Reserved (0)
14:12	**Dummy Cycles:** Number of Dummy Cycles for the dedicated FR read instruction (OpCode defined by AUX2): **x00b**: 0 Dummy cycles **x01b**: 4 Dummy cycles **x10b**: 8 Dummy cycles **x11b**: Per GRAM DWORD #2 (volatile) or #3 (non-volatile) bits [20:16] **1xxb**: In Single-SPI Bus Mode, use 0 Dummy Cycles. For other bus modes use the configured value (as set by bits [13:12]).
11:8	**Flag Register Read Access:** **0000b**: *Flag Register* (*FR*) not supported. **xx01b**: *Flag Register (FR)* is mapped to *Volatile Register (VR)* at byte address defined by AUX1 (bits [23:16]). **xx10b**: *Flag Register (FR)* is mapped to *Volatile Register (VR)* at byte address defined by AUX1 (bits [23:16]) with additional offset of 8000.0000h. **x1xxb**: *Flag Register (FR)* is read from the Active-Die (refer to GRAM DWORD#1 bits [27:24]), using the dedicated RD_FR instruction with OpCode defined by AUX2 (bits [31:24]). Other: Reserved
7:4	**Flag Register Clear Method:** **xxx1b**: *Flag Register (FR)* is cleared by writing FFh to the *Volatile Register (VR)* at byte address defined by AUX1 (bits [23:16]). **xx1xb**: *Flag Register (FR)* is defined as "Write-1-to-Clear" such that individual bits are cleared by writing '1' to the corresponding bits of the *Volatile Register (VR)* at byte address defined by AUX1 (bits [23:16]). **x1xxb**: *Flag Register (FR)* is cleared by the dedicated CLR_FR (50h) instruction. 1xxxb: *Flag Register (FR)* is cleared by the dedicated instruction with OpCode defined by AUX1 (bits [23:16]).
3:0	**Flag Register (FR):** **xxx1b**: bit [7] of the FR is the **READY Flag (RF)**. If set (1), indicates the device is idle and can accept new operations. **xx1xb**: bits [0] of the FR is the **Address Mode Flag (AMF)**. If set (1), indicates the device is operating in 32b addressing mode.

(*) If the FR is not supported, all bits of this DWORD are set to 0.

6.17.8 GRAM Parameter Table, 6th DWORD, Interrupt Controller

Function Specific Register Info (FSRI) to describe the Interrupt Controller Status Registers:

Bits	Description
31:24	**AUX2:** This holds the 2nd Interrupt Status Register (INTSR2) Byte Address (FFh if unused)
23:16	**AUX1:** This holds the 1st Interrupt Status Register (INTSR) Byte Address (FFh if unused)
15:9	Reserved (0)
8	**Interrupt Status Active Polarity:** 0: Interrupt Status Bit(s) set to 0 (active when zero) in the INSTR*, indicate that the corresponding interrupt event has occurred. 1: Interrupt Status Bit(s) set to 1 (active when one) in the INSTR*, indicate that the corresponding interrupt event has occurred.
7:0	**Interrupt Controller support:** **0000_0000b**: Interrupt Controller is not supported. **xxxx_xx01b**: Interrupt Controller is supported, including *Interrupt Status Register (INTSR):* • *INTSR* is mapped to *Volatile Register (VR)* at byte address defined by AUX1 (bits [23:16]). • Each bit of the INTSR is associated with an interrupt source, active when the source is triggered and cleared by writing '1' to that bit ("Write-1-to-Clear"). **xxxx_01xxb**: Interrupt Controller is supported, including *Interrupt Status Register (INTSR2):* • *INTSR2* is mapped to *Volatile Register (VR)* at byte address defined by AUX2 (bits [31:24]). • Each bit of the INTSR2 is associated with an interrupt source, active when the source is triggered and cleared by writing '1' to that bit ("Write-1-to-Clear"). **1xxx_xxxxb**: Proprietary Interrupt Scheme is supported. Refer to datasheet. Other: Reserved (0)

(*) If the INTSR* is not supported, all bits of this DWORD are set to 0.

NOTE: The GRAM SFDP Table defines the Interrupt register and access method. The assignment of interrupt sources to specific bits in the interrupt status registers is defined by other Function Specific SFDP Tables.

6.17.9 GRAM Parameter Table, 7th DWORD, Interrupt Controller

Function Specific Register Info (FSRI) to describe the Interrupt Controller Mask Registers:

Bits	Description
31:24	**AUX2:** This holds the 2nd Interrupt Mask Register (IMSKR2) Byte Address (FFh if unused)
23:16	**AUX1:** This holds the 1st Interrupt Mask Register (IMSKR) Byte Address (FFh if unused)
15:9	Reserved (0)
8	**Interrupt Mask Polarity:** 0: If a bit of IMSKR* is set to '1', the corresponding interrupt source is masked. 1: If a bit of IMSKR* is set to '0', the corresponding interrupt source is masked.
7:0	**Interrupt Mask Register support:** **0000_0000b**: Interrupt Mask Register is not supported. **xxxx_xx01b**: Interrupt Controller is supported, including *Interrupt Mask Register (IMSKR):* • *IMSKR* is mapped to *Volatile Register (VR)* at byte address defined by AUX1 (bits [23:16]). • Each bit of the INTSR is Masked by the corresponding bit of IMSKR. • An unmasked interrupt source asserts the interrupt output pin. **xxxx_01xxb**: Interrupt Controller is supported, including *Interrupt Mask Register (IMSKR2):* • *IMSKR2* is mapped to *Volatile Register (VR)* at byte address defined by AUX2 (bits [31:24]). • Each bit of the INTSR2 is Masked by the corresponding bit of IMSKR2. • An unmasked interrupt source asserts the interrupt output pin. **x1xx_xxxxb**: If bit [7] of the IMSKR is set (1), Interrupt sources associated with INTSR bits [6:0] will not assert the INT# output pin. This bit must be set to 0 to use the INT# output pin functionality of IMSKR. **1xxx_xxxxb**: If bit [7] of the IMSKR2 is set (1), Interrupt sources associated with INTSR2 bits [6:0] will not assert the INT# output pin. This bit must be set to 0 to use the INT# output pin functionality of IMSKR2. Other: Reserved (0)

6.17.10 GRAM Parameter Table, 8th DWORD, Extended Address Register (EAR)

Function Specific Register Info (FSRI) to describe the Extended Address Register (EAR)

Bits	Description
31:24	**AUX2:** This holds the instruction OpCode for direct read access of the EAR.
23:16	**AUX1:** EAR Byte Address, or the instruction OpCode for direct write access of the EAR.
15	Reserved (0)
14:12	**Dummy Cycles:** Number of Dummy Cycles for the dedicated EAR read instruction (OpCode defined by AUX2): **x00b**: 0 Dummy cycles **x01b**: 4 Dummy cycles **x10b**: 8 Dummy cycles **x11b**: Per GRAM DWORD #2 (volatile) or #3 (non-volatile) bits [20:16] **1xxb**: In Single-SPI Bus Mode, use 0 Dummy Cycles. For other bus modes use the configured value (as set by bits [13:12]).
11:8	**Extended Address Register (EAR) Access:** **0000b:** *Extended Address Register (EAR)* is not supported or not covered by the GRAM. **xxx1b**: *Extended Address Register (EAR)* is mapped to *Volatile Register (VR)* at byte address defined by AUX1 (bits [23:16]). **xx1xb**: *Extended Address Register (EAR)* is accessed through dedicated write instruction defined by AUX1 (bits [23:16]), and dedicated read instruction defined by AUX2 (bits [31:24]). The dedicated write instruction must be preceded by a Write-Enable instruction (WREN) if the WR_VR requires it (as defined by the GRAM). Other – Reserved
7:5	Reserved (0)
4	If set, EAR contains additional Function-Specific configuration bits, thus user should use read-modify-write operations.
3:0	**Extended Address Register (EAR):** **x100b**: bit [0] of the EAR extends address of instructions with 24b address. **x101b**: bits [1:0] of the EAR extends address of instructions with 24b address. **x110b**: bits [2:0] of the EAR extends address of instructions with 24b address. **x111b**: bits [3:0] of the EAR extends address of instructions with 24b address. **10xxb:** EAR bits, starting from bit 0, are the Die-ID that select the Active-Die **1100b:** EAR bits, starting from bit 1, are the Die-ID that select the Active-Die **1101b:** EAR bits, starting from bit 2, are the Die-ID that select the Active-Die **1110b:** EAR bits, starting from bit 3, are the Die-ID that select the Active-Die **1111b:** EAR bits, starting from bit 4, are the Die-ID that select the Active-Die Other: Reserved (0)

(*) If the EAR is not supported, all bits of this DWORD are set to 0.

6.17.11 GRAM Parameter Table, 9th DWORD, Status Register 2 (SR2)

Function Specific Register Info (FSRI) to describe the Status Register 2 (SR2).
NOTE: This register may contain both status indications and configuration bits.

Bits	Description
31:24	**AUX2:** This holds the instruction OpCode for direct read access of the SR2.
23:16	**AUX1:** SR2 Byte Address, or the instruction OpCode for direct write access of the SR2.
15	Reserved (0)
14:12	**Dummy Cycles:** Number of Dummy Cycles for the dedicated SR2 read instruction (OpCode defined by AUX2): **x00b**: 0 Dummy cycles **x01b**: 4 Dummy cycles **x10b**: 8 Dummy cycles **x11b**: Per GRAM DWORD #2 (volatile) or #3 (non-volatile) bits [20:16] **1xxb**: In Single-SPI Bus Mode, use 0 Dummy Cycles. For other bus modes use the configured value (as set by bits [13:12]).
11:8	**Status Register 2 (SR2) Access:** **0000b:** *Status Register 2 (SR2)* is not supported or not covered by the GRAM. **xxx1b**: *Status Register 2 (SR2)* is mapped to *Volatile Register (VR)* at byte address defined by AUX1 (bits [23:16]). **xx1xb**: *Status Register 2 (SR2)* is accessed through dedicated write instruction defined by AUX1 (bits [23:16]), or dedicated read instruction defined by AUX2 (bits [31:24]). The dedicated write instruction must be preceded by a Write-Enable instruction (WREN) if the WR_VR requires it (as defined by the GRAM). **1xxxb**: *Status Register 2 (SR2)*, is mapped to *Non-volatile Register (NVR)* at byte address defined by AUX1 (bits [23:16]). Other – Reserved (0)
7:0	Reserved (0)

(*) If the SR2 is not supported, all bits of this DWORD are set to 0.

6.17.12 GRAM Parameter Table, 10th DWORD, Status Register 3 (SR3)

Function Specific Register Info (FSRI) to describe the Status Register 3 (SR3).
NOTE: This register may contain both status indications and configuration bits.

Bits	Description
31:24	**AUX2:** This holds the instruction OpCode for direct read access of the SR3.
23:16	**AUX1:** SR3 Byte Address, or the instruction OpCode for direct write access of the SR3.
15	Reserved (0)
14:12	**Dummy Cycles:** Number of Dummy Cycles for the dedicated SR3 read instruction (OpCode defined by AUX2): **x00b**: 0 Dummy cycles **x01b**: 4 Dummy cycles **x10b**: 8 Dummy cycles **x11b**: Per GRAM DWORD #2 (volatile) or #3 (non-volatile) bits [20:16] **1xxb**: In Single-SPI Bus Mode, use 0 Dummy Cycles. For other bus modes use the configured value (as set by bits [13:12]).
11:8	**Status Register 3 (SR3) Access:** **0000b:** *Status Register 3 (SR3)* is not supported or not covered by the GRAM. **xxx1b**: *Status Register 3 (SR3)* is mapped to *Volatile Register (VR)* at byte address defined by AUX1 (bits [23:16]). **xx1xb**: *Status Register 3 (SR3)* is accessed through dedicated write instruction defined by AUX1 (bits [23:16]), and dedicated read instruction defined by AUX2 (bits [31:24]). The dedicated write instruction must be preceded by a Write-Enable instruction (WREN) if the WR_VR requires it (as defined by the GRAM). **1xxxb**: *Status Register 3 (SR3)*, is mapped to *Non-volatile Register (NVR)* at byte address defined by AUX1 (bits [23:16]). Other – Reserved (0)
7:0	Reserved (0)

(*) If the SR3 is not supported, all bits of this DWORD are set to 0.

6.18 SPI Safety Extensions (Interface CRC) Parameter Header and Table

This SFDP parameter table contains Function Specific Register Info (FSRI) to describe the Management status and configuration registers used to operate the SPI Safety Extension (Interface CRC) Function, defined by the **JESD255** standard.

This definition utilizes the Generic Register Access Method (GRAM) defined by the GRAM SFDP Parameter Table.

6.18.1 SPI Safety Extensions (Interface CRC) Parameter Header: 1st DWORD

Bits	Description
31:24	**Parameter Table Length = 02h** This field specifies how many DWORDs are in the Parameter table. NOTE This field is 1's based. Therefore, 1 indicates 1 DWORD.
23:16	**Parameter Table Major Revision Number = 01h** This 8-bit field indicates the major revision number of the parameter table. The value in this field is 01h for this table is newly defined by JESD216G revision. NOTE The Major Revision of JEDEC defined parameter tables can only be modified by updates to this standard.
15:8	**Parameter Table Minor Revision Number = 01h** This 8-bit field indicates the minor revision number of the parameter table. The value in this field is 01h for this table is incremented from JESD216G. NOTE The Minor Revision of the JEDEC owned parameter tables can only be modified by updates to this standard.
7:0	**Parameter ID LSB = 90h** The Interface CRC Parameter Table is assigned the ID (LSB) of 90h.

6.18.2 SPI Safety Extensions (Interface CRC) Parameter Header: 2nd DWORD

Bits	Description
31:24	**Parameter ID MSB = FFh** The CRC Parameter Table is assigned the ID (MSB) of FFh.
23:0	**Parameter Table Pointer (PTP)** = *manufacturer specified* This address specifies the start of this header's Parameter Table in the SFDP structure. The address is in terms of bytes and must be DWORD-aligned.

6.18.3 SPI Safety Extensions (CRC) Parameter Table, 1st DWORD, CRC Configuration Register

Function Specific Register Info (FSRI) to describe the CRC Configuration Register (SSER):
Note: refer to GRAM SFDP table for definition of addressable register access methods.

Bits	Description
31:24	**AUX2:** Instruction OpCode for direct read access of the SSER (FFh if unused)
23:16	**AUX1:** SSER Byte Address, or the instruction OpCode for direct write access of the SSER
15	**Register specific multi-die access:** If set (1), writing to this register affects all dies (broadcast). Otherwise, this register accessed as defined by the GRAM (DWORD#1).
14:12	**Dummy Cycles:** Number of Dummy Cycles for the dedicated SSER read instruction (OpCode defined by AUX2): **x00b:** 0 Dummy cycles **x01b:** 4 Dummy cycles **x10b:** 8 Dummy cycles **x11b:** Per GRAM DWORD #2 (volatile) or #3 (non-volatile) bits [20:16] **1xxb:** In Single-SPI Bus Mode, use 0 Dummy Cycles. For other bus modes use the configured value (as set by bits [13:12]).
11:8	**CRC Configuration Register (SSER) Access:** **xxx1b**: The CRC function is controlled by the 1B *SSE Register (SSER)*, mapped to *Volatile Register (VR)* at byte address defined by AUX1 (bits [23:16]). **xx1xb**: The CRC function is controlled by the 1B *SSE Register (SSER)*, accessed through dedicated write instruction defined by AUX1 (bits [23:16]), and dedicated read instruction defined by AUX2 (bits [31:24]). The dedicated write instruction must be preceded by a Write-Enable instruction (WREN) if the WR_VR requires it (as defined by the GRAM). **1xxxb**: The CRC function is controlled by the 1B *SSE Register (SSER)*, mapped to *Non-volatile Register (NVR)* at byte address defined by AUX1 (bits [23:16]). Other = Reserved

6.18.3 SPI Safety Extensions (CRC) Parameter Table, 1st DWORD, CRC Configuration Register (cont'd)

Bits	Description
7:4	**CRC Configuration Register (SSER):** **0001b:** SSER bits [2:0] is the CRC_EN that controls the CRC Function. Possible values for the CRC_EN field are: <000b> - CRC Function is disabled <001b> - CRC Function is enabled with 16B lines <011b> - CRC Function is enabled with 32B lines <101b> - CRC Function is enabled with 64B lines <111b> - CRC Function is enabled with 128B lines <Other> - Reserved. **0010b:** SSER bits [6:4] is the CRC_EN that controls the CRC Function (with same enumeration as above) **0100b:** SSER bits [2:0] is the CRC_EN that controls the CRC Function. Possible values for the CRC_EN field are: <001b> - CRC Function is disabled <000b> - CRC Function is enabled with 16B lines <010b> - CRC Function is enabled with 32B lines <100b> - CRC Function is enabled with 64B lines <110b> - CRC Function is enabled with 128B lines <Other> - Reserved. **0101b:** SSER bits [7:5] is the CRC_EN that controls the CRC Function. Possible values for the CRC_EN field are: <111b> - CRC Function is disabled <110b> - CRC Function is enabled with 16B lines <101b> - CRC Function is enabled with 32B lines <100b> - CRC Function is enabled with 64B lines <011b> - CRC Function is enabled with 128B lines <Other> - Reserved. Other = reserved
3:1	Reserved (0)
0	**CRC Function support**: If set (1), the Interface CRC function is supported as per JESD255.

6.18.4 SPI Safety Extensions (CRC) Parameter Table, 2nd DWORD, CRC Status Register

Function Specific Register Info (FSRI) to describe the CRC Status Register:

Bits	Description
31:8	Reserved (0)
7:4	**CRC Interrupt Status Indications:** Interface CRC Errors are indicated by: **x001b**: *Interrupt Status Register (INTSR)* bit [3]. **x010b**: *Interrupt Status Register (INTSR2)* bit [0]. Other: Reserved (0)
3:0	**CRC Status Indications:** Interface CRC Errors are indicated by: **x001b**: *Flag Register (FR)* bit [3]. **x010b**: *Flag Register (FR)* bit [2]. Other: Reserved (0)

6.19 SFDP CRC-32 Parameter Header and Table

This SFDP parameter table adds a 32-bit Cyclic Redundancy Check (CRC-32) error detection method for the entire SFDP data structure.

The CRC used is the 32-bit Ethernet CRC Calculation defined by IEEE-802.3.

CRC result width	32bits
Polynomial:	04C11DB7h

The CRC-32 parameter table contains a single DWORD that must be placed as the last DWORD in the SFDP data structure. The SFDP data structure starts at byte address 0 and continues through the last byte of the CRC-32 parameter table. The CRC-32 Parameter Header Parameter Table Pointer (CRC-32 PTP) provides the address of the least significant byte of the CRC-32 parameter table.

The CRC-32 parameter table value is calculated based on all DWORDs of the SFDP data structure address space, from the DWORD starting at byte address zero (0) through the last DWORD before the CRC-32 parameter table DWORD (ending at byte CRC-32 PTP -1). All SFDP address space bytes from 0 to CRC-32 PTP -1 must have stable and valid bit values; none of these bytes can have a floating or indeterminate value. This is because the SFDP standard allows there to be unused space between the parameter table headers and following tables or between tables. These unused spaces are included in the CRC-32 calculation and therefore must have stable and valid values even though the spaces are not part of any header or table in the SFDP data structure.

The CRC-32 for the SFDP data structure is simply another SFDP parameter table, like any other. It has a parameter table header that identifies the table as the SFDP CRC-32 parameter table. The header points to the Parameter Table contents.

Because the CRC-32 parameter table contents must be placed as the last table in the SFDP data structure, the header pointing to the table defines the location of the last DWORD in the SFDP data structure. Thus, serving as an indication of the total length of the SFDP data structure.

Note that SFDP is defined such that the lowest address byte of each DWORD is transferred first, and each byte is transferred most significant bit first, on the SPI. The below table is an example SFDP transmission order on SPI, left to right column and bit order:

Example DWORD Byte and Bit Transmission Order on SPI

First	Second	Third	Fourth
DWORD-Byte0[7:0]	DWORD-Byte1[15:8]	DWORD-Byte2[23:16]	DWORD-Byte3[31:24]
ASCII “S”	ASCII “F”	ASCII “D”	ASCII “P”
53h	46h	44h	50h
01010011	01000110	01000100	01010000

The same order is used for the CRC-32 parameter table DWORD.

6.19.1 SFDP CRC-32 Parameter Header: 1st DWORD

Bits	Description
31:24	**Parameter Table Length = 01h** This field specifies how many DWORDs are in the Parameter table. NOTE This field is 1's based. Therefore, 1 indicates 1 DWORD.
23:16	**Parameter Table Major Revision Number = 01h** This 8-bit field indicates the major revision number of the parameter table. The value in this field is 01h for this table is newly defined by JESD216G revision. NOTE The Major Revision of JEDEC defined parameter tables can only be modified by updates to this standard.
15:8	**Parameter Table Minor Revision Number = 00h** This 8-bit field indicates the minor revision number of the parameter table. The value in this field is 00h for this table is newly defined by JESD216G revision. NOTE The Minor Revision of the JEDEC owned parameter tables can only be modified by updates to this standard.
7:0	**Parameter ID LSB = 11h** The SFDP CRC-32 Parameter Table is assigned the ID (LSB) of 11h.

6.19.2 SFDP CRC-32 Parameter Header: 2nd DWORD

Bits	Description
31:24	**Parameter ID MSB = FFh** The SFDP CRC-32 Parameter Table is assigned the ID (MSB) of FFh.
23:0	**Parameter Table Pointer (PTP)** = *manufacturer specified* This address specifies the start of this header's Parameter Table in the SFDP structure. The address is in terms of bytes and must be DWORD-aligned. And must be the last DWORD in the entire SFDP data structure.

6.19.3 SFDP CRC-32 Parameter Table, 1st DWORD, CRC-32 Value

Bits	Description
31:24	CRC-32 value, bits 31:24 (most significant byte)
23:16	CRC-32 value, bits 23:16
15:8	CRC-32 value, bits 15:8
7:0	CRC-32 value, bits 7:0 (least significant byte)

6.19.4 SFDP CRC-32 Parameter Table, 1st DWORD, Byte and Bit Transmission Order on SPI

First	Second	Third	Fourth
DWORD-Byte0[7:0]	DWORD-Byte1[15:8]	DWORD-Byte2[23:16]	DWORD-Byte3[31:24]
CRC-32 value bits 7:0	CRC-32 value bits 15:8	CRC-32 value bits 23:16	CRC-32 value bits 31:24
Bit order 7,6,5,4,3,2,1,0	Bit order 15,14,13,12,11,10,9,8	Bit order 23,22,21,20,19,18,17,16	Bit order 31,30,29,28,27,26,25,24

6.20 Error Correction Code (ECC) Parameter Header and Table

This SFDP parameter table contains Function Specific Register Info (FSRI) to describe the Management status and configuration registers used to operate the internal **E**rror **C**orrection **C**ode (**ECC**) Function. The description refers to the following events:

- **REC** – Single-bit or multiple-bit **R**ecoverable **E**rror **C**orrection. Returned data is valid.
- **NRED** –Dual-bit or multiple-bit **N**on-**R**ecoverable **E**rror **D**etection. Returned data is invalid.
- **MULTP** – **Mult**iple **P**rogramming of a single ECC protected memory line, i.e. programming of a non-erased line.

This definition utilizes the Generic Register Access Method (GRAM) defined by the GRAM SFDP Parameter Table.

6.20.1 Error Correction Code (ECC) Parameter Header: 1st DWORD

Bits	Description
31:24	**Parameter Table Length = 03h** This field specifies how many DWORDs are in the Parameter table. NOTE This field is 1's based. Therefore, 1 indicates 1 DWORD.
23:16	**Parameter Table Major Revision Number = 01h** This 8-bit field indicates the major revision number of the parameter table. The value in this field is 01h for this table is newly defined by JESD216H revision. NOTE The Major Revision of JEDEC defined parameter tables can only be modified by updates to this standard.
15:8	**Parameter Table Minor Revision Number = 00h** This 8-bit field indicates the minor revision number of the parameter table. The value in this field is 00h for this table is newly defined by JESD216H revision. NOTE The Minor Revision of the JEDEC owned parameter tables can only be modified by updates to this standard.
7:0	**Parameter ID LSB = 12h** The ECC Parameter Table is assigned the ID (LSB) of 12h.

6.20.2 Error Correction Code (ECC) Parameter Header: 2nd DWORD

Bits	Description
31:24	**Parameter ID MSB = FFh** The CRC Parameter Table is assigned the ID (MSB) of FFh.
23:0	**Parameter Table Pointer (PTP)** = *manufacturer specified* This address specifies the start of this header's Parameter Table in the SFDP structure. The address is in terms of bytes and must be DWORD-aligned.

6.20.3 Error Correction Code (ECC) Parameter Table, 1st DWORD, General Information

Bits	Description
31:24	**AUX:** Instruction OpCode for direct read access of the ECCSR (FFh if unused).
31:22	Reserved (0)
21	If set (1), bits [3,1,0] of *ECC Line Status Register (ECCSR)* are used to indicate NRED, REC events and ECC On/Off status (respectively) in a Protected Memory Line. This register is read by issuing the dedicated instruction with OpCode defined by AUX (bits [31:24]), followed by 3B/4B address, 0/2/4 dummy cycles, and a 1B response containing the ECCLSR. Refer to Datasheet for further information.
20	**ECC Interrupt Synchronicity:** If set (1), the INT# output pin is synchronous to the output data, i.e., it is asserted when the ECC protected memory line of data is output on the SPI bus, if that line is associated with an ECC event. In this case, the INT# pin is sometimes referred to as ECS# pin. Otherwise (0), the INT# pin is asynchronous to the output data.
19:16	**ECC Interrupts:** **0000b**: ECC Interrupts are not supported. **0001b**: Bits [4,5,6] of the *Interrupt Status Register (INTSR)* are used to indicate ECC REC, NRED and MULTP events, respectively. **0010b**: Bits [0,1] of the *Interrupt Status Register (INTSR)* are used to indicate ECC REC and ECC NRED events, respectively. **0100b**: Bits [0,1] of the *Volatile Register (VR)* and *Non-volatile Register (NVR)* at Byte address 04h are used to mask ECC REC and NRED events, respectively ('1'=Masked). **0101b:** Bits [1:0] of the *Volatile Register (VR)* and *Non-volatile Register (NVR)* at Byte address 04h are used to mask ECC interrupts: <11> interrupts disabled, <10> interrupts on REC events, <01> interrupts on NRED events, <00> interrupts on REC and NRED events. (bits [7:2] must be set to 1). **0110b:** Bits [2:1] of the *Volatile Register (VR)* at Byte address 05h are used to mask ECC interrupts: <00> interrupts on NRED and MULTP events, <01> interrupts on REC, NRED, and MULTP events <10> interrupts on NRED events, <11> interrupts on REC, NRED events. **1000b**: Bits [1:0] of the *Interrupt Mask Register (IMSKR)* (*Volatile Register (VR)* and *Non-volatile Register (NVR)*) are used to enable/mask ECC interrupts: <00> Interrupts disabled, <01> interrupts on REC and NRED events, <10> interrupts on NRED events, <11> interrupts on NRED and MULTP events. **1001b**: Bit [2] of the *Extended Address Register (EAR)* is used to select which ECC events to indicate: <0> interrupts on REC events <1> interrupts on NRED events. Writing to these bits is done using Write-Enable instruction (WREN) followed by 56h instruction with a 1B EAR. **1111b:** ECC Interrupts are enabled whenever the ECC function is enabled. Other: Reserved.

6.20.3 Error Correction Code (ECC) Parameter Table, 1st DWORD, General Information (cont'd)

Bits	Description
15:12	**ECC Function Properties:** **xxx1b**: ECC Function is enabled by default after reset or power-up. **xx1xb**: Disabling the ECC function affects only read operations. Program operations always use the ECC function to add ECC bits to each ECC line of programmed data if possible. **01xxb**: Disabling the ECC function is done using the 4B instruction: 9Bh, 1Ah, 01h, FEh. Enabling the ECC function is done using the 4B instruction: 9Bh, 1Ah, 00h, FFh
11	Reserved (0)
10:8	**ECC Protected Memory Line Length:** <001b> = 8B <010b> = 16B <011b> = 32B Other = Reserved
7	Reserved (0).
6:0	**ECC Function Support:** **000_0000b**: Internal ECC function is not supported **xxx_xxx1b**: Internal Recoverable Error Correction (REC) is supported. **xxx_xx1xb**: Internal Non-Recoverable Error Detection (NRED) is supported. **x00_xxxxb:** Multiple Programming (MULTP) of memory lines is not supported and may be rejected by the device or may cause non-deterministic results. **x01_xxxxb**: Multiple Programming (MULTP) of memory lines is supported, automatically disabling the ECC for each specific line. **x10_xxxxb**: Multiple Programming (MULTP) of memory lines is fully supported, automatically updating the ECC according to the new data. **1xx_xxxxb:** Partial programming of an ECC protected memory line is supported, i.e. user can program a few bytes that are less than a complete ECC protected memory line length. In this case, the device forms a complete ECC protected memory line and protects it with ECC (subject to MULTP restrictions). **0xx_xxxxb:** Partial programming of an ECC protected memory line is **not** supported, i.e., if a partial memory line is programmed, the ECC is turned off for that memory line. In this case, user can pad the data with FFh to form a complete ECC protected memory line.

6.20.4 Error Correction Code (ECC) Parameter Table, 2nd DWORD, ECC Register

Function Specific Register Info (FSRI) to describe the *ECC Register (ECCR)*. This register holds configuration and status indications of the ECC function:
NOTE: This register may contain both status indications and configuration bits.

Bits	Description
31:24	**AUX2:** Instruction OpCode for direct read access of the ECCR, or Byte Address for ECC Status Register (FFh if unused).
23:16	**AUX1:** ECCR Byte Address, or the instruction OpCode for direct write access of the ECCR (FFh if unused)
15	Reserved (0)
14:12	**Dummy Cycles:** Number of Dummy Cycles for the dedicated ECCR read instruction (OpCode defined by AUX2): **x00b**: 0 Dummy cycles **x01b**: 4 Dummy cycles **x10b**: 8 Dummy cycles **x11b**: Per GRAM WORD #2 (volatile) or #3 (non-volatile) bits [20:16] **1xxb**: In Single-SPI Bus Mode, use 0 Dummy Cycles. For other bus modes use the configured value (as set by bits [13:12]).
11:8	**ECC Register (ECCR) Access:** **0000b**: The *ECC Register (ECCR)* is not supported. **xxx1b**: The ECC function is controlled by the 1B *ECC Register (ECCR)*, mapped to *Volatile Register (VR)* at byte address defined by AUX1 (bits [23:16]). **xx1xb**: The ECC function is controlled by the 1B *ECC Register (ECCR)*, accessed through dedicated write instruction defined by AUX1 (bits [23:16]), and dedicated read instruction defined by AUX2 (bits [31:24]). The dedicated write instruction must be preceded by a Write-Enable instruction (WREN) if required by WR_VR (as defined by the GRAM). **1xxxb**: The ECC function is controlled by the 1B *ECC Register (ECCR)*, mapped to *Non-volatile Register (NVR)* at byte address defined by AUX1 (bits [23:16]). Other = Reserved
7:4	**ECC Status Indications:** **0001b**: ECCR status bits [7,6,5] indicate REC, NRED and MULTP events (respectively) in the most recent Read/Program operation. **0010b:** ECCR status bits [4,5,6] indicate REC, NRED and MULTP events (respectively) in the most recent Read/Program operation. **0011b:** ECCR status bits [6,5,4] indicate REC, NRED and MULTP events (respectively) in the most recent Read/Program operation. **0100b:** ECCR status bits [0,1,2] indicate REC, NRED and MULTP events (respectively) in the most recent Read/Program operation. **0101b**: ECCR status bit [0] indicates that ECC is disabled for at least 1 memory line in the most recent read operation. **0110b**: ECCR status bits [4,3] indicate REC and NRED events (respectively) in the most recent read operation. **0111b**: Bits [3,4] of the *Volatile Register (VR)* at Byte address defined by AUX2 (bits [31:24]) are used to indicate REC and NRED events (respectively, during normal reads since the last ECC clear or reset). **1000b:** EAR status bits [7,6] indicate REC and NRED events (respectively) in the most recent Read/Program operation. Other = Reserved

6.20.4 Error Correction Code (ECC) Parameter Table, 2nd DWORD, ECC Register (cont'd)

Bits	Description
3:0	**ECC Function Enable:** **x001b**: ECCR configuration bit [2] is used to enable the ECC function. **x010b**: ECCR configuration bit [3] is used to disable the NRED function (REC is always enabled). **x100b**: SR3 configuration bit [2] is used to enable the ECC function. **x101b**: The ECC function is enabled if any of the ECC interrupts is unmasked (refer to bits [19:16] of Dword #1). Other = Reserved

6.20.5 Error Correction Code (ECC) Parameter Table, 3rd DWORD, Advanced ECC Status Register (AECCSR)

Function Specific Register Info (FSRI) to describe the *Advanced ECC Status Register (AECCSR)*:

Bits	Description
31:24	**AUX2:** Byte Address for reading the first (LS) Byte of AECCSR, or the instruction OpCode for direct read access of the AECCSR (FFh if unused)
23:16	**AUX1:** Byte Address for clearing of AECCSR, or the instruction OpCode for direct write access for clearing of the AECCSR (FFh if unused)
15	Reserved (0)
14:12	**Dummy Cycles:** Number of Dummy Cycles for the dedicated AECCSR read instruction (OpCode defined by AUX2): **x00b**: 0 Dummy cycles **x01b**: 4 Dummy cycles **x10b**: 8 Dummy cycles **x11b**: Per GRAM WORD #2 (volatile) or #3 (non-volatile) bits [20:16] **1xxb**: In Single-SPI Bus Mode, use 0 Dummy Cycles. For other bus modes use the configured value (as set by bits [13:12]).
11:8	**Advanced ECC Status Register (AECCSR) Access Method:** **xxx1b:** AECCSR is mapped to N consecutive bytes of the *Volatile Register (VR)* beginning with the LS-byte at byte address defined by AUX2 (bits [31:24]). **xx1xb:** AECCSR is accessed using a dedicated read instruction (RD_AECCSR) with OpCode defined by AUX2 (bits [31:24]). This returns an N-Byte response containing the AECCSR (LS-byte first). **01xxb**: AECCSR content must be internally generated before it can be read. This is done using a dedicated instruction: 9Bh, 92h, ADDR-Start (4B), ADDR-End (4B). **11xxb**: Refer to vendor documentation for description of the AECCSR generation method. Other = Reserved
7:4	**Advanced ECC Status Register (AECCSR) Clear Method:** AECCSR is cleared on power up, device reset **and** on the following conditions: **xxx1b**: AECCSR is cleared by writing FFh to *Volatile Register (VR)* at byte address defined by AUX1 (bits [23:16]). **xx1xb**: AECCSR is cleared by the dedicated CLR_AECCSR instruction with OpCode defined by AUX1 (bits [23:16]). **1xxxb**: AECCSR is cleared whenever the AECCSR content is regenerated. Other = Reserved
3:0	**Advanced ECC Status Register (AECCSR):** **0000b**: AECCSR is not supported. **0001b**: AECCSR is a 64b (N=8) register with bits as described by Option 1 table below. **0010b**: AECCSR is a 40b (N=5) register with bits as described by Option 2 table below. **0011b**: AECCSR is a 48b (N=6) register with bits as described by Option 3 table below. **0100b**: AECCSR is a 32b (N=4) register with bits as described by Option 4 table below. **1000b**: Consult with memory vendor documentation for description of the AECCSR. Other = Reserved

6.20.5 Error Correction Code (ECC) Parameter Table, 3rd DWORD, Advanced ECC Status Register (AECCSR) (cont'd)

AECCSR Option 1:

Advanced ECC Status Register (AECCSR) is a 64b (N=8) read-only register with following bit definition:

Byte	Bits	Field name	Description
0	7	REC	If set, indicates REC events (one or more) were detected.
	6:4	Reserved	Reserved (0)
	3:0	REC-ADDR3	Bits [27:24] of the Captured Address of the first REC event.
1	7:0	REC-ADDR2	Bits [23:16] of the Captured Address of the first REC event.
2	7:0	REC-ADDR1	Bits [15:8] of the Captured Address of the first REC event.
3	7:4	REC-ADDR0	Bits [7:4] of the Captured Address of the first REC event.
	3:0	REC_CNT	REC Counter: 4 bits counter of the number of REC events.
4	7	NRED	If set, indicates NRED events (one or more) were detected.
	6:4	Reserved	Reserved (0)
	3:0	NRD-ADDR3	Bits [27:24] of the Captured Address of the first NRED event.
5	7:0	NRD-ADDR2	Bits [23:16] of the Captured Address of the first NRED event.
6	7:0	NRD-ADDR1	Bits [15:8] of the Captured Address of the first NRED event.
7	7:4	NRD-ADDR0	Bits [7:4] of the Captured Address of the first NRED event.
	3:0	NRED_CNT	NRED Counter: 4 bits counter of the number of NRED events.

AECCSR Option 2:

Advanced ECC Status Register (AECCSR) is a 40b (N=5) read-only register with following bit definition:

Byte	Bits	Field name	Description
0	7	ADDR-VALID	If set, indicates ECC-ADDR is valid.
	6	MULTP	If set, indicates MULTP event was detected.
	5	NRED	If set, indicates NRED event was detected.
	4	REC	If set, indicates REC event was detected.
	3:0	CNT	ECC event counter: 4 bits counter of the number of ECC events.
1	7:0	ADDR0 (*)	Bits [7:0] of the Captured Address of the first ECC event.
2	7:0	ADDR1	Bits [15:8] of the Captured Address of the first ECC event.
3	7:0	ADDR2	Bits [23:16] of the Captured Address of the first ECC event.
4	7:0	ADDR3 (*)	Bits [31:24] of the Captured Address of the first ECC event.

(*) ADDR0 LS bits and ADDR3 MS bits may be ignored, depending on ECC-line length and Device capacity. These are forced to 0 by the Flash device.

6.20.5 Error Correction Code (ECC) Parameter Table, 3rd DWORD, Advanced ECC Status Register (AECCSR) (cont'd)

AECCSR Option 3:

Advanced ECC Status Register (AECCSR) is a 48b (N=6) read-only register with following bit definition (Byte-Addresses are not consecutive. Byte-Address is specified by the Address column in the table below which overrides AUX2 byte address):

Byte	Byte Address	Bits	Field name	Description
0	8Eh	7:0	ADDR0	Bits [7:0] of the Captured Address of the first ECC event.
1	8Fh	7:0	ADDR1	Bits [15:8] of the Captured Address of the first ECC event.
2	40h	7:0	ADDR2	Bits [23:16] of the Captured Address of the first ECC event.
3	41h	7:0	ADDR3	Bits [31:24] of the Captured Address of the first ECC event.
4	8Ah	7:0	ECC_CNT0	Bits [7:0] of the ECC event counter
5	8Bh	7:0	ECC_CNT1	Bits [15:8] of the ECC event counter

AECCSR Option 4:

Advanced ECC Status Register (AECCSR) is a 32b (N=4) read-only register with following bit definition:

Byte	Bits	Field name	Description
0	7:4	ADDR0	Bits [7:4] of the Captured Address of the first ECC event.
	3:0	Reserved	Reserved (0)
1	7:0	ADDR1	Bits [15:8] of the Captured Address of the first ECC event.
2	7:0	ADDR2	Bits [23:16] of the Captured Address of the first ECC event.
3	7:4	Reserved	Reserved (0)
	3:0	ADDR3	Bits [27:24] of the Captured Address of the first ECC event.

For Option 4, bit [7] of the Volatile Register (VR) at Byte address 08h is used to indicate the captured address in AECCSR (ADDR0-ADDR3) is valid and bits [3:0] are the ECC event counter, indicating the number of REC events..

7 Rules for Header and Table Additions and Modifications

- Additional headers and parameter tables can be added by vendors without JEDEC approval.
- The first four DWORDs of clause 6.4 JEDEC Flash Parameters Table can never be modified.
- New headers must be built using exactly two DWORDs and they must immediately follow the existing header(s).
- Minimum parameter table size is one DWORD. The maximum parameter table size is not specified.
- Parameter tables may be located anywhere in the SFDP space. They do not need to immediately follow the parameter headers.
- Overlapping parameter tables are permitted.

8 Legacy Compatibility

Prior to the release of this standard, Intel published SFDP guidelines with a four DWORD parameter table. The first four DWORDs of the JEDEC Basic Parameter Table are identical to the table in Intel's guidelines. Devices in production prior to the release of the initial JESD216 standard might only contain these four DWORDs.

Revision A increased the number of DWORDs from nine to sixteen. The first nine DWORDs in Revision A maintain backwards compatibility. Devices in production prior to the release of this revision may not contain all of the currently defined DWORDs.

Revision B continues to maintain backwards compatibility of the Basic Parameter Table. Optional Function Specific tables for Sector Map Parameters and 4-Byte address commands are added. See Annex B revision history for details.

Revision C continues to maintain backwards compatibility of the Basic Parameter Table, Optional Function Specific tables for Sector Map Parameters and 4-Byte address commands. Definitions for Octal interface devices are added. See Annex B revision history for details.

Revision D continues to maintain backwards compatibility of the Basic Parameter Table, Optional Function Specific tables for Sector Map Parameters, 4-Byte address commands, and Octal interface devices. Definitions for x4 (Quad) interface devices are added and dummy cycle definitions for some registers are changed. See Annex B revision history for details.

Revision E continues to maintain backwards compatibility of the Basic Parameter Table, Optional Function Specific tables for Sector Map Parameters, 4-Byte address commands, Octal interface devices, definitions for x4 (Quad) interface devices and dummy cycle definitions for some registers are changed. Definitions for RPMC and Secure Read/Write transactions have been added to Revision E. See Annex B revision history for details.

Revision F continues to maintain backwards compatibility of the Basic Parameter Table, Optional Function Specific tables, for Sector Map Parameters, 4-Byte address commands, and Octal interface devices. Three DWORDs were added to the Basic Parameter Table and one DWORD was added to the xSPI (Profile 1.0) Parameter Table. Minor revision numbers were incremented by 1 in the Basic Flash Parameter Header and the xSPI (Profile 1.0) Parameter Header. See Annex B revision history for details.

Annex A — (Informative) Procedure for Requesting Function Specific ID

The Function Specific ID list is not a fixed listing. Any company may request a Function Specific ID by making a request to the JEDEC office at angies@jedec.org. Please include “Function Specific ID Request, JESD216” in the email subject line. Upon receipt of the email, the request will be forwarded to the JC-42.4 Chair and the JC-42.4 TG Chair for committee consideration. The chair will then respond to the request. Updates to the list will be made periodically.

The SFDP Standard will allow Serial Flash vendors to describe the functions and features of their devices in a standard set of internal parameter tables. These internal parameter tables can be read by users to determine the characteristics of the device.

Annex B — (Informative) Differences between Revisions

This annex briefly describes most of the changes made to entries that appear in this standard, JESD216H (August 2025), compared to its predecessors, JESD216G (November 2024), JESD216F.02 (June 2022), JESD216F.01 (February 2022), JESD216F (December 2021), JESD216E (August 2021), JESD216D (August 2019), JESD216C (August 2018), JESD216B (May 2014), JESD216A (July 2013), and JESD216 (April 2011).

B.1 Differences between JESD216H and JESD216G

Edits made in May 2025:

Clause	Description of change
6.2	Added revision descriptions for JESD216F, G, and H
6.2.2	Modified descriptions for Bits 15:8 and 7:0
6.3.3.1	Update SFDP Table Codes
6.4.1	Updated description for Bit 23:16 and 15:8
6.4.18	Basic Flash Parameter Table, DWORD #15, bits [22:20] – Quad Enable requirements
6.4.22	Basic Flash Parameter Table, DWORD #19, Octal Enable, 8-8-8 and 0-8-8 Entry/Exit.
6.13, 6.15	Note that a Write Enable should precede every command sequence
6.17.1	Updated table for GRAM Parameter Header 1st DWORD
6.17.3	Modified NOTE for Bit 27:24 in GRAM Parameter Table, 1st DWORD, General Information
6.17.6	Updated descriptions for Bits 11:8 and 3:0 in GRAM Parameter Table, 4th DWORD, Status Register (SR)
6.17.7	GRAM DWORD#5, bits [7:4] – add FR Clear method
6.17.9	GRAM DWORD#7, bit [8],[7:0] – add Interrupt Mask Polarity
6.17.10-12	Add GRAM DWORD#8-10, for EAR, SR2, and SR3 registers
6.18.3	SSE DWORD#1, bits [7:4] – add option x101b for CRC Enable configuration
6.18.4	SSE DWORD#2, bits [3:0] – add option x010b for FR Indication
6.19	SFDP CRC-32 Parameter Header and Table (with revised references)
6.20	ECC Parameter Header and Table

Editorial changes:

Clause	Description of change
6.17.3	GRAM DWORD#1, bits [27:24] – expand the term “affects all dies”
6.17.6	GRAM DWORD#4, bits [11:0], [3:0] – phrasing and terminology
6.17.7	GRAM DWORD#5, description - terminology
6.18.1	SSE Header DWORD#1, bits [7:0] - typo

B.2 Differences between JESD216G and JESD216F.02

Edits made in July 2024:

Clause	Description of change
1	Added note in “Scope”: SFPD represents factory defaults
6.17	Added “Generic Register Access Method (GRAM) Parameter Table”
6.18	Added “SPI Safety Extensions (CRC) Parameter Table”

B.3 Differences between JESD216F.02 and JESD216F.01

Editorial changes made by the Serial Flash Task Group on May 11, 2022, item number 1775.75 (approved by the JC-42.4 subcommittee on June 8, 2022)

1) Page 25: Clause 6.4.1, Bits[15:8], Minor Revision Number incremented from 07h to 08h due to 3 DWORDs added to Basic Flash Parameter Table
2) Page 28: Clause 6.4.6, Bits[20:16] and Bits[4:0], deleted examples showing conversion of bits to clocks
3) Page 29: Clause 6.4.7, Bits[20:16], deleted example showing conversion of bits to clocks
4) Page 30: Clause 6.4.9, Bits[20:16], deleted example showing conversion of bits to clocks
5) Page 31, Clause 6.4.10, Bits[20:16], delete example showing conversion of bits to clocks
6) Page 44: Clause 6.4.20, Bits[20:16] and bits[4:0], deleted examples showing conversion of bits to clocks
7) Page 53: Clause 6.4.25, Bits[20:16] and Bits[4:0] deleted example showing conversion of bits to clocks
8) Page 53: Clause 6.4.25, Bits[7:5], corrected example from 010b to 001b
9) Page 54: Clause 6.4.26, Bits[23:21] and Bits[7:5], corrected examples from 010b to 001b
10) Page 54: Clause 6.4.26, Bits[20:16] and Bits[4:0], deleted examples showing conversion of bits to clocks
11) Page 72: Clause 6.8.1, Bits[15:8], Minor Revision Number incremented from 00h to 01h due to 1 DWORD added to xSPI (Profile 1.0) Parameter Table
12) Page 138: Section 8 Legacy Compatibility, added a legacy compatibility statement for JESD216F

B.4 Differences between JESD216F.01 and JESD216F

Editorial changes made by the Serial Flash Task Group on December 13, 2021, item number 1775.73 (Reference: JC-42 Meeting Minutes December 7-14, 2021, Waikoloa, HI, clause 6.5.1.0).

1) Page 13: Clause 6.2.2, Bits[15:8}, "JESD216E" corrected to "JESD216F"
2) Pages 24 and 25: Clause 6.4.1,
    a. Bits[31:24], "JESD216E" corrected to "JESD216F"
    b. Bits[31:24), "parameter table length is 20" corrected to "parameter table length is 23"
    c. Bits[31:24], "(unchanged from JESD216D revision) corrected to (3 new DWORDs added to JESD216E)"
    d. Bits[15:8], "JESD216E" corrected to "JESD216F"
3) Page 72: Clause 6.8.1,
    a. Bits[31:24], added "For the JESD216F revision, this parameter table length is 6"
    b. Bits[23:16], "JESD216E" corrected to "JESD216F"
    c. Bits[15:8], "JESD216E" corrected to "JESD216F"

B.5 Differences between JESD216F and JESD216E

Globally added missing ‘S’ and ‘D’ designations to IO modes (e.g., 1-1-1 -> 1S-1S-1S)

Clause Description of change

6.2.2 Incremented spec revision from JESD216E to JEDS216F and SFDP Minor Revision Number from ‘09h’ to ‘0Ah’

6.4.3 JEDEC Basic Flash Parameter Table Overview: added DWORDs 21, 22, and 23

DWORD 21	Fast Read (1S-1D-1D), (1S-2D-2D), (1S-4D-4D), and (4S-4D-4D) Support
DWORD 22	Fast Read (1S-1D-1D) and (1S-2D-2D) Wait States, Mode Bit Clocks, and Instruction
DWORD 23	Fast Read (1S-4D-4D) and (4S-4D-4D) Wait States, Mode Bit Clocks, and Instruction

6.4.24 JEDEC Basic Flash Parameter Table: added 21ST DWORD

6.4.25 JEDEC Basic Flash Parameter Table: added 22ND DWORD

6.4.26 JEDEC Basic Flash Parameter Table: added 23RD DWORD

6.8.8 JEDEC xSPI (Profile 1.0) Parameter Table: added 6th DWORD – Default Dummy cycles after POR.

B.6 Differences between JESD216E and JESD216D.01

Clause	Description of change
6.6	Added "Replay Protected Monotonic Counters (RPMC) Parameter Header and Table"
6.16	Added "Secure Packet READ/WRITE Parameter Header and Table"

Editorial changes made by Serial Flash TG on March 1, 2021

NOTE: The page numbers shown below are from the original JESD216E document and do not necessarily match the page numbers in this revised document. Additionally, the page numbers are the spec page numbers shown at the top of each page and not the physical page numbers.

Globally changed:

a. replaced sensitive/offensive terminology to "initiator" (19 instances)
b. replace sensitive/offensive terminology to "target" (30 instances)
c. Made appropriate "JESD216D" to "JESD216E" changes

B.7 Differences between JESD216D.01 and JESD216D

Editorial changes made by Serial Flash TG on August 1, 2019

NOTE: The page numbers shown below are from the original JESD216D document and do not necessarily match the page numbers in this revised document. Additionally, the page numbers are the spec page numbers shown at the top of each page and not the physical page numbers.

1) Globally changed:
   a. "supported" to "supported" (160 instances)
2) Page 3: Clause 3, "definitions" corrected to "definitions"
3) Page 8: Clause 4.5.6, inserted missing timing diagram for Figure 6
4) Page 13: Clause 6.2.2,
   a. bits[31:24], "See 0" corrected to "See 6.2.3"
   b. bits[15:8], "1" corrected to "01h"
   c. bits[7:0]. "8" corrected to "08h"
5) Page 15: Clause 6.2.3, F1h, "See Error! Reference source not found." changed to "See Figure 12"
6) Page 17: Clause 6.2.3, add caption "Figure 21 — xSPI NAND Class-1 Device Read SFDP Flow"
7) Page 18: Clause 6.2.3, add caption "Figure 22 — xSPI NAND Class-2 Device Read SFDP Flow"
8) Page 19: Clause 6.3,
   a. Added a comma after "If a vendor chooses to include multiple revisions of the Basic Parameter Table"
   b. Corrected "see 0' to "see 6.2.2"
9) Page 21: Clause 6.3.3.1,
   a. Changed "Reserved for next Function Specific Table assignment ID from FF0C to FF8E"
   b. Added "x4 Quad IO with DS" and assigned ID = "FF0C"
   c. Added "Command Sequences to change to Quad DDR (4S-4D-4D) mode" with ID = "FF8D"
10) Page 24: Clause 6.4.1,
   a. bits[23:16], "1" corrected to "01h"
   b. bits[15:8], "7" corrected to "07h"

B.8 Differences between JESD216D.01 and JESD216D (cont'd)

11) Page 25: Clause 6.4.3, DWORD 18, "Jedec" corrected to "JEDEC"
12) Page 40: Clause 6.4.18, bits[22:20], 010b, removed double ".." after the word "zero"
13) Page 41: Clause 6.4.18, bits[3:0], x1xxb, removed double ".." after "800003h"
14) Page 43: Clause 6.4.19, bits[13:8], change "issued on 1, 2, or 4 wires" to "issued on 1, 2, 4, or 8 wires"
15) Page 45: Clause 6.4.21, bits[25:24], 01b,
    a. Inserted space between "01b:" and "Start"
    b. Changed "in in" to "in"
    c. Changed "1: JEDEC SPI Protocol Reset implemented as described in JEDEC SPI Protocol Reset spec" to "1: JEDEC SPI Protocol Reset implemented as described in JESD252"
16) Page 46: Clause 6.4.21, changed "198th DWORD" to "18th DWORD"
17) Page 47: Clause 6.4.21, changed "208th DWORD" to "18th DWORD"
18) Page 52: Clause 6.4.23, changed "210th DWORD" to "20th DWORD"
19) Page 54: Clause 6.5.1,
    a. bits[23:16], "1" corrected to "01h"
    b. bits[15:8], "0" corrected to "00h"
20) Page 57: Clause 6.5.4, removed double "for for" in "A DWORD for for each…"
21) Page 64: Clause 6.6.1,
    a. bits[23:16], "1" corrected to "01h"
    b. bits[15:8], "1" corrected to "01h"
22) Page 75: Clause 6.8.3, bit[21], "Enbale" corrected to "Enable"
23) Page 78: Clause 6.9.1,
    a. bits[23:16], "1" corrected to "01h"
    b. bits[15:8], "1" corrected to "01h"
24) Page 103: Clause 6.9.27, bit[30], replaced 2 instances of "means means" with "means"
25) Page 108: Clause 6.10.1,
    a. bits[23:16], "1" corrected to "01h"
    b. bits[15:8], "0" corrected to "00h"
26) Page 118: Clause 6.11.1,
    a. bits[23:16], "1" corrected to "01h"
    b. bits[15:8], "1" corrected to "01h"
27) Page 121: Clause 6.12.1,
    a. bits[23:16], "1" corrected to "01h"
    b. bits[15:8], "0" corrected to "00h"
28) Page 124:
    a. Clause 6.13, reworded "See JESD251, eXpanded Serial Peripheral Interface (xSPI) for Non-volatile Memory Devices x4 xSPI Addendum (still at committee level for discussion)" to "See JESD251-1, Addendum No. 1 to JESD251 – OPTIONAL x4 QUAD I/O WITH DATA STROBE"
    b. Clause 6.13.3, removed "(still at committee level for discussion)"
29) Page 125: Clause 6.13.3, bit[31], changed "24 bit" to "24-bit" for 2 instances
30) Page 126: Clause 6.13.5, replace "(still at committee level for discussion)" with "(JESD251-1)"
31) Page 129: Clause 6.14.1,
    a. Bits[23-16], "1" corrected to "01h"
    b. Bits[15-8], "0" corrected to "00h"
    c. Bits[7:0], "09h" corrected to "8Dh"

B.9 Differences between JESD216D and JESD216C

Clause	Description of change
6.3.3.1	Added ID FF0C for "x4 Quad IO with DS"; changed "Reserved for next Function Specific Table assignment" from FF0C to FF8D.
6.9.5	SCCR Map for SPI Memory Devices Parameter Table: 3rd DWORD, *Bits 27:26 Number of dummy bytes used for Generic Addressable Read Status/Control register command for volatile registers in (1S-1S-1S) mode* and *5:0 Reserved* are redefined
6.9.6	SCCR Map for SPI Memory Devices Parameter Table: 4th DWORD, *Bits 27:26 Number of dummy bytes used for Generic Addressable Read Status/Control register command for volatile registers in (1S-1S-1S) mode* and *5:0 Reserved* are redefined
Added the following new optional clauses:	
6.13	x4 Quad IO with DS Parameter Header and Table
6.14	Command Sequences to Change to Quad DDR (4S-4D-4D) mode

B.10 Differences between JESD216C and JESD216B

Clause	Description of change
3	Terms and definitions: Updated description of command mode nomenclature
6.2.2	SFDP Header: 2nd DWORD: Bits 31:24 redefined as SFDP Access Protocol. Updated definition of bits 23:16, Number of Parameter Headers (NPH).
Added 6.2.3	Definition of SFDP Access Protocol Field
6.4.20 – 6.2.23	Added DWORDs 17 to 20 to the JEDEC Basic Flash Parameter Header and Table.
Added the following new optional clauses:	
6.7	JEDEC eXtended Serial Peripheral Interface (xSPI) Profile 1.0 Parameter Header and Table
6.8	JEDEC eXtended Serial Peripheral Interface (xSPI) Profile 2.0 Parameter Header and Table
6.9	Status, Control and Configuration Register Map for SPI Memory Devices
6.10	Status, Control and Configuration Register Map Offsets for Multi-Chip SPI Memory Devices
6.11	Command Sequences to Change to Octal DDR (8D-8D-8D) mode

Removed the example code in the previous Annex A and Annex B, and renamed Annex C and Annex D accordingly

B.10.1 Editorial changes made by Serial Flash TG on August 17, 2018

1) Globally changed:
   a. "Bit is set /cleared by" to "Bit is accessed by" (16 instances)
   b. "Bit is set/cleared by" to "Bit is accessed by" (32 instances)
   c. "Bits are set /cleared by" to "Bits are accessed by" (4 instances)
   d. "Bits are set/cleared by" to "Bits are accessed by" (8 instances)
2) Page 7: "See 0…" – Changed to a link to clause 6.4.21 "See 6.4.21…"
3) Page 12: To use a format consistent with the rest of the document, "DWORD 2" changed to "the 2nd DWORD" and "DWORD 15" changed to "the 15th DWORD".
4) Page 14: Clause 6.2.3,
   a. Removed flow diagram from SFDP Command Parameter Value 240/F0h (Decimal/Hex) and created new "Figure 11 — xSPI NAND Class-1 Device Read SFDP Flow"
   b. Added "(see Figure 11)" reference: "Follow Long latency NVM Class-1 device SFDP access behavior for reading SFDP and MSPT data (see Figure 11)" to SFDP Command Parameter Value 240/F0h (Decimal/Hex) and 244/F4h (Decimal/Hex)
5) Page 15: Clause 6.2.3,
   a. Removed flow diagram from SFDP Command Parameter Value 241/F1h (Decimal/Hex) and created new "Figure 12 — xSPI NAND Class-2 Device Read SFDP Flow"
   b. Added "(see Figure 12)" reference: "Follow Long latency NVM Class-2 device SFDP access behavior for reading SFDP and MSPT (see Figure 12)"
6) Page 17: Clause 6.3.3, Changed the reference "see Annex C' to "see Annex A"

B.10.1 Editorial changes made by Serial Flash TG on August 17, 2018 (cont'd)

7) Page 19: To use a format consistent with the rest of the document, "DWORD 3" changed to "the 3rd DWORD" (two instances on the page).
8) Page 23: Clause 6.4.4, bits 18:17: After "All SFDP accesses use 3-byte addressing." we should add "A device using 4-byte only addressing may still support 03h read using 3-byte addressing."
9) Page 28: Clause 6.4.11. To use a format consistent with the rest of the document,
   a. "DWORDs 8 or 9" changed to "the 8th or 9th DWORD"
   b. "DWORD 10" changed to "the 10th DWORD"
10) Page 45: Clause 6.4.22
   a. bits 8:4 "x_xx1xb: Issue instruction E8h" should read "x_xx1xb: Issue instruction 06h (WREN), then issue instruction E8h"
   b. bits 3:0 add a line between the two already there: "xx1xb: Issue instruction 06h (WREN), then issue FFh instruction"
11) Page 63: Clause 6.7.1, bits 7:0 "The eXtended Serial Peripheral Interface is assigned the ID LSB of 05h." changed to "The eXtended Serial Peripheral Interface (Profile 1) is assigned the ID LSB of 05h."
12) Page 68: Clause 6.9.1, bits 7:0
   a. "Parameter ID LSB (0x86)" changed to "Parameter ID LSB (0x06)"
   b. "Refer to Definition of Parameter ID Field in below." Changed to "The eXtended Serial Peripheral Interface (Profile 2) is assigned the ID LSB of 06h."
13) Page 71: "xSPI Profile 2.0 Octal memory devices are covered in 6.9.10." This link should be "6.11"
14) Page 72: "Which of the two options is used is described in 6.9.5." Actually, this is not only found in 6.10.5, it is described for every bit. So we should write "Which of the two options is used is described in the parameter table for each bit."
15) Page 72: Clause 6.10.1, bits 7:0 "The Status, Control and Configuration Register Map is assigned the ID LSB of 06h." changed to "… ID LSB of 87h"
16) Page 80: Clause 6.10.11
   a. Bit 30-29: "2 bit" and "4 bit" changed to "2 bits" and "4 bits"
   b. Bit 26-24: Added comment: "(Requirements: The physical bits used in a device are in the same (one) register, the bits form a continuous field and the bits are in order. If these requirements are not met, bit 31 above has to be set to 0.)"
17) Page 91: Clause 6.10.22, This is a volatile bit, all references to non-volatile bits are typos (copied from previous table by mistake). This typo is found in bits 31, 30, 27 (twice) and 26-24. "Non-volatile" changed to "Volatile"
18) Page 101: Clause 6.11.1, bits 7:0 "The Status, Control and Configuration Register Map is assigned the ID LSB of 06h." changed to "The Status, Control and Configuration Register Map for xSPI Profile 2.0 is assigned the ID LSB of 09h"
19) Page 109: Clause 6.11.14 "See the JEDEC xSPI Standard for details about Output Driver Strength values." should be updated to "See the JEDEC Standard JESD251, *eXpanded Serial Peripheral Interface (xSPI) for Non-volatile Memory Devices*, for details about Output Driver Strength values."
20) Page 111: Clause 6.12.1, bits 7:0 "The Status, Control and Configuration Register Map is assigned the ID LSB of 88h." changed to "The Status, Control and Configuration Register Map Offsets for Multi-Chip SPI Memory Devices is assigned the ID LSB of 88h."
21) Page 114: Clause 6.13.1 bits 7:0 "The Command Sequences to Change to Octal DDR (8D-8D-8D) mode is assigned the ID LSB of 09h." should be "… ID LSB of 0Ah."
22) Page 117: Clause 8, Changed references in the text containing "See Annex D' to "See Annex B"
23) Updated Contents page numbers
24) Inserted Figures 11 and 12 in the figures listed in the Contents and updated the figure and page numbers
25) Updated the figure references in the text to match the new figure numbers:
   a. Figure 11 -> Figure 13 (2 instances on old page 19; new page 22)
   b. Figure 12 -> Figure 14 (1 instance on old page 19; new page 22)
   c. Figure 13 -> Figure 15 (2 instances on old page 19; new page 22)
   d. Figure 14 -> Figure 16 (2 instances on old page 19; new page 22)
   e. Figure 16 -> Figure 18 (1 instance on old page 42; new page 45)
   f. Figure 17 -> Figure 19 (1 instance on old page 42; new page 45)
   g. Figure 18 -> Figure 20 (1 instance on old page 42; new page 45)

B.11 Differences between JESD216B and JESD216A

- Added a definition for Sector and Block to clarify terminology
- Changed Sector Type nomenclature to Erase Type, to clarify that the erase operation type is independent of the minimum erase granularity of the sectors affected by the erase operation e.g., several erase types (sizes of erase operations e.g., 8KB, 32KB, 64KB) may be applied to sectors of a smaller granularity than the erase operation (e.g., 4KB sectors).
- Clarified parameter ID LSB parity being located in the most significant Bit of the Byte
- Added the Function Specific Parameter Table ID assignments
- Added the Header for the JEDEC Basic Flash Parameter Table, separate from the general description for Parameter Table Headers. Removed references to the Basic Flash Parameter Table in the general Parameter Table Header description. Incremented the JEDEC Basic Flash Parameter Table Minor Revision to 6 as an indication that there has been an additional definition for a previously reserved bits: DWORD 15[18, 14, and 8].
- Removed use of the terms “sector” or “block” in relationship to erase operations, instead using the term Erase Type
- DW11, [31:24] Clarified the Chip Erase time applies separately to each die for multi-die devices in which the dice are individually accessed.
- DW12, [23:20], [12:9], Added comments that suspend can be issued at any time, there is no required minimum timing. However, … this parameter recommends an average resume to suspend interval so the operation can make progress
- DW15, [23], Updated description and replaced WP by RESET
- DW15, [8:4], added 4-4-4 enable option
- Added a clause with the optional Function Specific Sector Map Parameter Tables
- Added a clause with the optional Function Specific 4-Byte Address Instruction Tables
- Added Annex B code example for Sector Map Parameter Table reading and moved previous Annex B and Annex C to be Annex C and Annex D

B.12 Differences between JESD216A and JESD216

- Extensive rewrite to clarify requirements, but functionality of JESD216 has been maintained.
- The JESD216A parameter table is marked with Major Revision 1 and Minor Revision 5. Using Minor Revision 5 instead of 1 is required to avoid version conflicts with legacy devices which implemented SFDP tables prior to JEDEC standardization.
- Increased the number of DWORDs in the Basic Parameters Table from nine to sixteen.
- Provided hooks for future expansion using Function Specific Tables.
- Added Annex A Example code for SFDP discovery
- Added Annex B Procedure for requesting a Function Specific ID

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Standard Improvement Form **JEDEC Standard** **JESD216H**

The purpose of this form is to provide the Technical Committees of JEDEC with input from the industry regarding usage of the subject standard. Individuals or companies are invited to submit comments to JEDEC. All comments will be collected and dispersed to the appropriate committee(s).

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1. I recommend changes to the following:

☐ Requirement, clause number _____

☐ Test method number _____ Clause number _____

The referenced clause number has proven to be:

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