JEDEC STANDARD

Serial Flash Discoverable Parameters (SFDP)

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SERIAL FLASH DISCOVERABLE PARAMETERS (SFDP) STANDARD

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Foreword

This standard was prepared by the JEDEC SFDP Task Group authorized by the JC-42.4 Committee Chairman. It was derived from prior work done by Intel on their 'Serial Flash Discoverable Parameters Guidelines' document.

The intended audience is serial flash vendors and engineers writing device drivers for SFDP compliant serial flash devices.

The participating SFDP TG members were volunteers from AMD, ASPEED, Emulex, Intel, Macronix, Micron, Microchip, Sanyo, Spansion, and Winbond.

Introduction

The Serial Flash Discoverable Parameter (SFDP) standard provides a consistent method of describing the functional and feature capabilities of serial flash devices in a standard set of internal parameter tables. These parameter tables can be interrogated by host system software to enable adjustments needed to accommodate divergent features from multiple vendors.

The SFDP standard defines a common parameter table describing important device characteristics and serial access methods used to read the parameter table data. Additional parameter headers and tables can be specified by future revisions of this standard or by flash vendors and are optional.

SERIAL FLASH DISCOVERABLE PARAMETERS (SFDP) STANDARD

(From JEDEC Board Ballot JCB-13-01, formulated under the cognizance of the JC-42.4 Committee on Nonvolatile Memory.)

1 Scope

The SFDP standard defines the structure of the SFDP database within the memory device and methods used to read its data.

The JEDEC-defined header with Parameter ID FF00h and the related Basic Parameter Table is mandatory. This header and table provide basic information for a Serial Peripheral Interface (SPI) protocol memory. Additional headers and tables are optional.

The read command protocol using various I/O modes and standard clock rate are specified. The device electrical parameters are not specified.

2 Normative reference

The following normative documents contain provisions that, through reference in this text, constitute provisions of this standard. For dated references, subsequent amendments to, or revisions of, any of these publications do not apply. However, parties to agreements based on this standard are encouraged to investigate the possibility of applying the most recent editions of the normative documents indicated below. For undated references, the latest edition of the normative document referred to applies.

1. JEP106, Standard Manufacturers Identification Code (contact jedec.org for the latest revision of this document)

2. NIST SP800-147, BIOS Protection Guidelines (http://csrc.nist.gov/publications/nistpubs/)

3 Terms and definitions

For the purposes of this standard, the following terms and definitions apply:

00b: The ‘b’ suffix indicates the ‘00’ digits are a binary representation of the number.

00h: The ‘h’ suffix indicates the ‘00’ digits are a hexadecimal representation of the number.

0x00: The ‘0x’ prefix indicates the ‘00’ digits are a hexadecimal representation of the number. This form is used in the ‘C’ sample code in the Appendix.

Address: The three or four byte value following some instructions that is used to select a location within an address space of the flash memory.

3 Terms and definitions (cont'd)

Basic Parameter Table: The table pointed to by Parameter ID FF00h. Contains general information about the flash device's capabilities.

Command: The combination of the instruction, address, optional mode bits, wait states, and data cycles used to initiate functions or transfer information between the controller and the serial flash.

Controller: The serial bus master

Double Transfer Rate (DTR). Instruction, address, and/or data may be input or output on both the rising and falling edges of the clock.

Dummy Cycles: Clock cycles during which no data is transferred to or from a memory.

DWORD: Four consecutive 8-bit bytes used as the basic 32-bit building block for headers and parameter tables.

Instruction: The one byte code used to initiate a function in the serial flash or identify the type of information transfer between the controller and the serial flash.

Mode Bits: Optional control bits that follow the address bits. These bits are driven by the controller if they are specified.

Wait States: Required clock cycles between the address bits or optional mode bits and the start of data when reading from the flash device. Some device data sheets describe these as dummy cycles because no information is transferred between the controller and memory during these cycles. Neither controller nor memory are required to drive the data lines during these cycles.

Read Latency: On flash read instructions, the total number of clocks between end of address and the start of data. The sum of clocks for mode bits and clocks for wait states equals the Read Latency.

(x-y-z): Command mode nomenclature used to indicate the number of active pins used for the instruction (x), address (y), and data (z). At the present time, the only valid Read SFDP command modes are: (1-1-1), (2-2-2), and (4-4-4)

4 Read SFDP Command Protocol

4.1 Instruction

The Read SFDP instruction code is 5Ah.

4.2 Address

Indicates the starting read location in the SFDP area and is always expressed as a three byte (24-bit) address.

4.3 Wait States

Following the address, eight clocks are required before valid data is clocked out.

4.4 Clock Rate

SFDP compliant devices must support 50 MHz operation for the Read SFDP command (instruction 5Ah). Devices may support a wider frequency range, but a controller can always run SFDP cycles at 50 MHz or less and get valid results.

4.5 Command Modes

The Read SFDP command can be used with device supported modes of (1-1-1), (2-2-2), or (4-4-4), but the instruction (5Ah), address (24 bits), eight wait states, and 50 MHz requirements remain the same. Support for SFDP does not imply or require that the flash device support 2-2-2 or 4-4-4 mode. If the controller knows a priori the mode in which the flash device is configured, then it can issue the Read SFDP command in that mode. If the controller does not know, then a suggested algorithm is to try to read the SFDP signature (see 6.1) in 4-4-4 mode, if that fails try 2-2-2 mode, and if that fails try 1-1-1 mode.

Timing Diagram Signal Definitions:

- S# = Select, low active. Memory device selection signal also often referred to as Chip Select or Chip Enable
- C = Clock. Serial clock to the memory also often referred to as SCLK.
- DQ0 = Data input or output zero. The least significant memory data input or output also often referred to as IO0 or Serial Input (SI) when not used for two or four bit data I/O.
- DQ1 = Data input or output one. The next most significant memory data input or output above DQ0, also often referred to as IO1 or Serial Output (SO) when not used for two or four bit data I/O.
- DQ2 = Data input or output two. The next most significant memory data input or output above DQ1, also often referred to as IO2 or Write Protect, low active (WP#) when not used for four bit data I/O.
- DQ3 = Data input or output three. The most significant memory data input or output, also often referred to as IO3 or Hold, low active (HOLD#) when not used for four bit data I/O.

4.5.1 Read SFDP (1-1-1) Mode

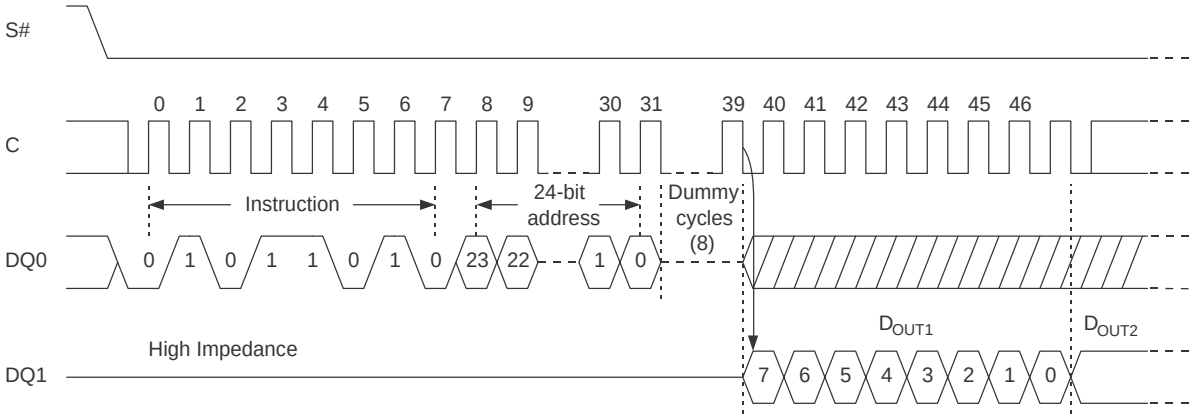

Figure 1 — Read SFDP (1-1-1) Mode Timing Diagram

4.5.2 Read SFDP (2-2-2) Mode

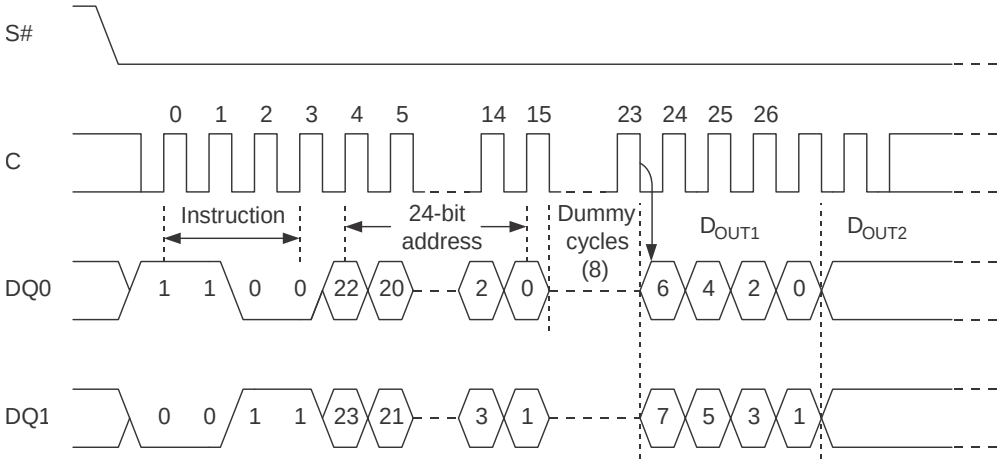

Figure 2 — Read SFDP (2-2-2) Mode Timing Diagram

4.5.3 Read SFDP (4-4-4) Mode

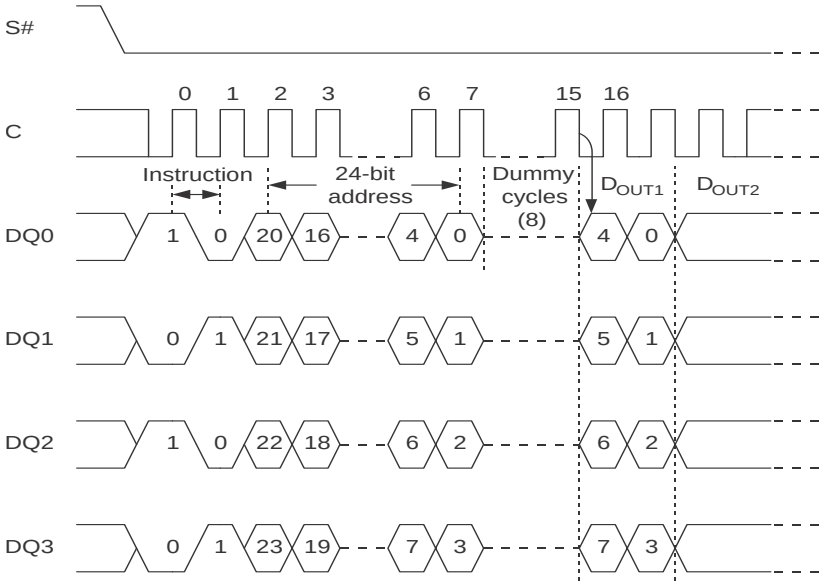

Figure 3 — Read SFDP (4-4-4) Mode Timing Diagram

5 Read SFDP Behavior

5.1 Security

The SFDP and flash memory address ranges must never overlap. This ensures that address range checking the controller may perform to prevent access to security keys or other sensitive information stored in flash cannot be bypassed. Also, for PC BIOS applications non-overlap is required to comply with NIST SP800-147.

Addresses beyond the end of the SFDP tables must not alias into the flash memory. Regardless of the implementation, writes to SFDP tables must be permanently disabled before the memory device is released to a customer by the memory vendor factory.

5.2 Reset and Hold Functions

Reset and Hold functionality will be available during the Read SFDP command if the memory device command mode supports these features.

5.3 Read Wrap

Not supported with the Read SFDP command--even when a memory device defaults to Read Wrap-around mode for other read commands. Only continuous (sequential) read is supported with the Read SFDP command.

5.4 SFDP Address Boundary Wrap

Device behavior when the Read SFDP command crosses the SFDP structure boundary is not defined except for the security restriction specified in 5.1. There is no requirement for the address counter to wrap back to the beginning of the structure and the data read after that point is not specified.

5.5 Reserved SFDP Locations

The content of reserved SFDP locations (memory within the SFDP address space that has not yet been defined or used) is not specified, but recommended to be all FFh.

6 SFDP Database

6.1 SFDP Header Structure

The format of the SFDP header is shown in Figure 4.

	[31:24]	[23:16]	[15:8]	[7:0]	Hex byte location
SFDP Header	Serial Flash Discoverable Parameters (SFDP) Signature = 50444653h				[3h:0h]
	Byte 3 = "P"	Byte 2 = "D"	Byte 1 = "F"	Byte 0 = "S"	
	Unused (set to FFh)	Number of Parameter Headers (NPH)	SFDP Major Revision	SFDP Minor Revision	[7h:4h]
1st Parameter Header	Parameter Length (in double words)	Parameter Major Revision	Parameter Minor Revision	Parameter ID LSB JEDEC ID (00h)	[Bh:8h]
	Parameter ID MSB JEDEC ID (FFh)	Parameter Table Pointer			[Fh:Ch]
2nd Parameter Header (optional)	Parameter Length (in double words)	Parameter Major Revision	Parameter Minor Revision	Parameter ID LSB	[13h:10h]
	Parameter ID MSB	Parameter Table Pointer			[17h:14h]
...					
Nth Parameter Header (optional)	Parameter Length (in double words)	Parameter Major Revision	Parameter Minor Revision	Parameter ID LSB	
	Parameter ID MSB	Parameter Table Pointer			

Figure 4 — Overall Header Structure

6.2 SFDP Header

The SFDP Header is located at address 000000h of the SFDP data structure. It identifies the SFDP Signature, the number of parameter headers, and the SFDP revision numbers.

Both the SFDP header and the individual parameter table headers include Major and Minor revision numbers.

Major revisions require code (BIOS/firmware) or hardware change to get previously defined discoverable parameters. For example, changes that reorganize previously defined fields.

Minor revisions are changes that define previously reserved fields, add fields to the end, or that clarify definitions of existing fields.

Revision A of JESD216 maintains backwards compatibility by appending new fields to the end of the previous Basic Parameter Table.

The revision numbers of vendor-defined and Function Specific tables follow the same guidelines as the Basic Parameter Table.

6.2.1 SFDP Header: 1st DWORD

Bits	Description
31:0	**SFDP Signature** Allows a user to know that the information is valid. Signature[31:0]: 50444653h

6.2.2 SFDP Header: 2nd DWORD

Bits	Description
31:24	**Unused** Contains FFh and can never be changed.
23:16	**Number of Parameter Headers (NPH)** Specifies the number of parameter headers in the SFDP data structure. This number is 0-based. Therefore, 0 indicates 1 parameter header. The value of this field is not defined by this standard. It is dependent on the number of tables a vendor implements.
15:8	**SFDP Major Revision Number** This 8-bit field indicates the major revision number of this standard. The value in this field is 1 for devices which implement the JESD216A revision. NOTE The value of this field may only be changed by an update to the JESD216 standard.
7:0	**SFDP Minor Revision Number** This 8-bit field indicates the minor revision number of this standard. The value in this field is 5 for devices which implement the JESD216A revision. NOTE The value of this field may only be changed by an update to the JESD216 standard.

6.3 Parameter Headers

Each Parameter Header identifies the size, location, revision, ownership and function of their associated parameter tables. Parameter table ownership will be either JEDEC (via this standard) or an individual vendor (via vendor specific documentation).

Multiple parameter headers can be specified with each parameter header being 2 DWORDs (64-bits). The first parameter header is mandatory, is defined by this standard, and starts at byte offset 08h. If a vendor chooses to include multiple revisions of the Basic Parameter Table they may do so provided the table headers are in order starting with the oldest version. The total number of parameter headers is specified in the NPH field of the SFDP header , see 6.2. All subsequent parameter headers need to be contiguous and may be specified by JEDEC or by vendors using the same structure (shown in Figure 4). Minor revisions may overlap earlier revisions by starting at the same address as an earlier revision but have additional length for parameters added in the later revision. This allows the use of legacy parameters without the need to repeat them in each new minor revision.

6.3.1 Parameter Header: 1st DWORD

Bits	Description
31:24	**Parameter Table Length** This field specifies how many DWORDs are in the Parameter table. NOTE This field is 1's based. Therefore, 1 indicates 1 DWORD.
23:16	**Parameter Table Major Revision Number** This 8-bit field indicates the major revision number of the associated parameter table. The value in this field is 1 for tables defined by the JESD216A revision. NOTE Major Revision starts at 01h. The Major Revision of JEDEC defined parameter tables can only be modified by updates to this standard. The Major Revision of a vendor-specified table is controlled by that vendor.
15:8	**Parameter Table Minor Revision Number** This 8-bit field indicates the minor revision number of the associated parameter table. The value in this field is 5 for tables defined by the JESD216A revision. The value in this field is 0 for tables defined by the JESD216 initial release. NOTE Minor Revision starts at 00h. The Minor Revision of the JEDEC owned parameter tables can only be modified by updates to this standard. The Minor Revision of a vendor-specified table is controlled by that vendor.
7:0	**Parameter ID LSB:** Refer to the paragraph below for the definition of this field.

6.3.2 Parameter Header: 2nd DWORD

Bits	Description
31:24	**Parameter ID MSB** Refer to 6.3.2.1 for the definition of this field.
23:0	**Parameter Table Pointer (PTP)** This 24-bit address specifies the start of this header's Parameter Table in the SFDP structure. The address must be DWORD-aligned.

6.3.2 Parameter Header: 2nd DWORD (cont'd)

6.3.2.1 Definition of Parameter ID Field

The Parameter ID indicates the parameter table ownership and type.

The ID field is expanded to two bytes because a single byte is insufficient to uniquely identify all manufacturers (potential owners). For example, in JEP106 the Manufacturer's Identification Code of 2Ch is shared by Micron, Celestica, Tachyon Semiconductor, etc. The Bank Number uniquely associates the 2Ch code with a single manufacturer. Micron is on Bank one, Celestica is on Bank two, and Tachyon Semiconductor is on Bank three. In the SFDP headers, when a Manufacturer's Identification Code is stored in the Parameter ID Least Significant Byte (LSB) the Bank number is stored in the Parameter ID Most Significant Byte (MSB).

JEP106 Manufacturer's Identification Code is an eight (8) bit field, consisting of seven (7) data bits plus one (1) odd parity bit. In SFDP headers, a Parameter ID LSB with odd parity signifies a Manufacturer's Identification Code and a Parameter ID LSB with even parity signifies a Function Specific table.

Parameter IDs with an MSB of:
- FFh through 80h are defined by the JEDEC 42.4 committee
- 7Fh though 01h identify the bank number of a JEDEC JEP106 assigned Manufacturer ID.
- 00h is reserved because JEP106 bank numbering begins at 01h

Parameter IDs with an MSB of FFh through 80h use the LSB to identify the Function Specific table type:
- Any parameter ID with LSB 00h identifies the SPI protocol Basic Parameter Table.
- LSB values with even parity are Function Specific tables that are defined by the JC-42.4 committee.
- LSB values with odd parity are illegal to prevent any confusion with JEP106 manufacturer ID values.

The Parameter ID LSB value of 00h is reserved for the Basic Parameter Table defined by this standard. For backwards compatibility the MSB is FFh when the LSB is 00h and LSB 00h shall not be used when the MSB is any value other than FFh. This is because some legacy systems using the original JESD216 may ignore the MSB and assume any parameter ID with LSB of 00h is the Basic Parameter Table.

Function Specific tables may be defined by the JC-42.4 Committee, a manufacturer, or third-party. The purpose of the Function Specific tables is to allow development of features and associated parameter tables common to multiple manufacturers, prior to the parameter tables being incorporated into the next revision of JESD216. Allocation of IDs for Function Specific tables is requested through the JEDEC office, see Annex B.

Parameter IDs with an MSB of 7Fh though 01h use the LSB to identify the JEDEC JEP106 assigned Manufacturer ID within the designated bank. The identified manufacturer owns the definition of the parameter table. The parameter table structure is vendor specific.

6.3.3 Example of an SFDP Header

Figure 5 shows an example of an SFDP Header with SFDP Revision 1.0, one Parameter Header, Parameter Table length of 9 DWORDs, 1st Parameter Header Revision 1.0, JEDEC ID of 00h, and the Parameter Table Pointer pointing to location 000010h.

	[31:24]	[23:16]	[15:8]	[7:0]	Hex Byte Location
SFDP Header	50h	44h	46h	53h	< [3h:0h]
	FFh	00h	01h	00h	< [7h:4h]
1st Parameter Header	09h	01h	00h	00h	< [Bh:8h]
	FFh	00h	00h	10h	< [Fh:Ch]

Figure 5 — Example of an SFDP Header

6.4 JEDEC Basic Flash Parameter Table

Parameter tables contain coded information describing the features and capabilities of the serial flash. The first parameter table as defined by JEDEC is mandatory and its starting address is specified by the PTP field of the 1st Parameter Header. This table identifies some of the basic features of SPI protocol flash memory devices.

DWORD	Description
1	Uniform 4KB Sectors, Write Buffer Size, Volatile Status Register, Fast Read Support (1-1-2) (1-2-2) (1-4-4)(1-1-4), Number of Address Bytes, DTR Support
2	Memory Density
3	Fast Read (1-4-4) (1-1-4): Wait States, Mode Bit Clocks, Instruction
4	Fast Read (1-1-2) (1-2-2): Wait States, Mode Bit Clocks, Instruction
5	Fast Read (2-2-2) (4-4-4) Support
6	Fast Read (2-2-2): Wait States, Mode Bit Clocks, Instruction
7	Fast Read (4-4-4): Wait States, Mode Bit Clocks, Instruction
8	Sector Type 1 & 2 Size and Instruction
9	Sector Type 3 & 4 Size and Instruction
10	Sector Type (1:4) Typical Erase Times and Multiplier Used To Derive Max Erase Times
11	Chip Erase Typical Time, Byte Program and Page Program Typical Times, Page Size
12	Erase/Program Suspend/Resume Support, Intervals, Latency, Keep Out Area Size
13	Program/Erase Suspend/Resume Instructions
14	Deep Powerdown and Status Register Polling Device Busy
15	Hold and WP Disable Function, Quad Enable Requirements, 4-4-4 Mode Enable/Disable Sequences, 0-4-4 Entry/Exit Methods and Support
16	32-bit Address Entry/Exit Methods and Support, Soft Reset and Rescue Sequences, Volatile and Nonvolatile Status Register Support

6.4.1 JEDEC Basic Flash Parameter Table: 1st DWORD

Bits	Description
31:23	**Unused** Contains FFh and can never be changed.
22	**Supports (1-1-4) Fast Read** Device supports single input instruction & address and quad output data Fast Read. 0: (1-1-4) Fast Read NOT supported. 1: (1-1-4) Fast Read supported.
21	**Supports (1-4-4) Fast Read** Device supports single input instruction, quad input address, and quad output data Fast Read. 0: (1-4-4) Fast Read NOT supported. 1: (1-4-4) Fast Read supported.
20	**Supports (1-2-2) Fast Read** Device supports single input instruction, dual input address, and dual output data Fast Read. 0: (1-2-2) Fast Read NOT supported. 1: (1-2-2) Fast Read supported.
19	**Supports Double Transfer Rate (DTR) Clocking** Indicates the device supports some type of double transfer rate clocking. 0: DTR NOT supported 1: DTR Clocking supported
18:17	**Address Bytes** Number of bytes used in addressing flash array read, write and erase: 00b: 3-Byte only addressing 01b: 3- or 4-Byte addressing (e.g., defaults to 3-Byte mode; enters 4-Byte mode on command) 10b: 4-Byte only addressing 11b: Reserved NOTE This field refers to the number of address bits/bytes that are clocked in for any command requiring an address except for SFDP Header or Table accesses. All SFDP accesses use 3-byte addressing. Examples: Read, Fast Read, Write, 4 kilobyte Erase.
16	**Supports (1-1-2) Fast Read** Device supports single input instruction & address and dual output data Fast Read with 8 wait states. 0: (1-1-2) Fast Read NOT supported. 1: (1-1-2) Fast Read supported.
15:8	**4 Kilobyte Erase Instruction** NOTE If 4 kilobyte erase is not supported, then enter FFh. This instruction must also be included in one of the Sector Types in 6.4.8 or 6.4.9.

Bits	Description
7:5	**Unused** Contains 111b and can never be changed.
4	**Write Enable Instruction Select for Writing to Volatile Status Register** This bit only applies if bit 3 is 1. 0: flash device requires instruction 50h as the write enable prior to performing a volatile write to the status register 1: flash device requires instruction 06h as the write enable prior to performing a volatile write to the status register. NOTE If target flash status register is nonvolatile, then bits 3 and 4 must be set to 00b. This bit definition is maintained for legacy compatibility only. New system implementations should refer to 6.4.16 for a full definition of volatile and non-volatile behavior.
3	**Volatile Status Register Block Protect bits** 0: Block Protect bits in device's status register are solely non-volatile or may be programmed either as volatile using the 50h instruction for write enable or non-volatile using the 06h instruction for write enable. 1: Block Protect bits in device's status register are solely volatile. NOTE If target flash register is nonvolatile, then bits 3 and 4 must be set to 00b. This bit definition is maintained for legacy compatibility only. New devices should refer to 6.4.16 for a full definition of volatile and non-volatile behavior.
2	**Write Granularity** 0: 1 Byte – Use this setting for single byte programmable devices or buffer programmable devices when the buffer is less than 64 bytes (32 Words). 1: Use this setting for buffer programmable devices when the buffer size is 64 bytes (32 Words) or larger. This bit definition is maintained for legacy compatibility only. New system implementations should refer to 6.4.11for the buffer (page) size. The legacy minimum write granularity is a single byte within any size programming buffer.
1:0	**Block/Sector Erase Sizes** Identifies if the device supports uniform 4k erase blocks. This erase size information must also be included one of the Sector Types in 6.4.8 or 6.4.9. 00b: Reserved 01b: 4 kilobyte Erase is supported throughout the device 10b: Reserved 11b: Use this setting only if uniform 4 kilobyte erase is unavailable. NOTE This is a legacy field. Refer to sections 6.4.8 and 6.4.9 for information on what sector sizes are supported.

6.4.2 JEDEC Basic Flash Parameter Table: 2nd DWORD

Bits	Description
31:0	**Flash Memory Density** For densities 2 gigabits or less, bit-31 is set to 0b. The field 30:0 defines the size in bits. Example: 00FFFFFFh = 16 megabits For densities 4 gigabits and above, bit-31 is set to 1b. The field 30:0 defines 'N' where the density is computed as 2^N bits (N must be >= 32)**.** Example: 80000021h = 2^33 = 8 gigabits

6.4.3 JEDEC Basic Flash Parameter Table: 3rd DWORD

Bits	Description
31:24	**(1-1-4) Fast Read Instruction** Instruction for single input instruction & address and quad output data Fast Read.
23:21	**(1-1-4) Fast Read Number of Mode Clocks** This field will be 000b if Mode Bits are not supported, NOTE This field should be counted in clocks not number of bits received by the serial flash. The master drives the bus during "mode bits" cycles; the master tri-states the bus during "dummy" cycles. **Example:** If 4 mode bits are needed with a single input address phase command, this field would be 100b.
20:16	**(1-1-4) Fast Read Number of Wait states (dummy clocks) needed before valid output** This field will be 00000b if wait states/dummy clocks are not supported. (The number of dummy clocks should be > 0 to avoid contention on bi-directional pins.) **Example:** If 8 bits are needed with a single input address phase command, this field would be 01000b.
15:8	**(1-4-4) Fast Read Instruction** Instruction for single input instruction, quad input address, and quad output data Fast Read.
7:5	**Quad Input Address Quad Output (1-4-4) Fast Read Number of Mode Clocks** This field will be 000b if Mode bits are not supported, NOTE This field should be counted in clocks not number of bits received by the serial flash. The master drives the bus during "mode bits" cycles; the master tri-states the bus during "dummy" cycles. **Example:** If 8 mode bits are needed with a quad input address phase command, this field would be 010b.
4:0	**(1-4-4) Fast Read Number of Wait states (dummy clocks) needed before valid output** This field will be 00000b if wait states/dummy clocks are not supported. (The number of dummy clocks should be > 0 to avoid contention on bi-directional pins.) **Example:** If 16 bits are needed with a quad input address phase command, this field would be 00100b.

6.4.4 JEDEC Basic Flash Parameter Table: 4th DWORD

Bits	Description
31:24	**(1-2-2) Fast Read Instruction** Instruction for single input instruction, dual input address, and dual output data Fast Read.
23:21	**(1-2-2) Fast Read Number of Mode Clocks** This field will be 000b if Mode bits are not supported, NOTE This field should be counted in clocks not number of bits received by the serial flash. The master drives the bus during "mode bits" cycles; the master tri-states the bus during "dummy" cycles. **Example:** If 8 mode bits are needed with a dual input address phase command, this field would be 100b.
20:16	**(1-2-2) Fast Read Number of Wait states (dummy clocks) needed before valid output** This field will be 00000b if wait states/dummy clocks are not supported. (The number of dummy clocks should be > 0 to avoid contention on bi-directional pins.) **Example:** If 8 bits are needed with a dual input address phase command, this field would be 00100b.
15:8	**(1-1-2) Fast Read Instruction** Instruction for single input instruction& address and dual output data Fast Read. Note: The industry standard is 3Bh
7:5	**(1-1-2) Fast Read Number of Mode Clocks** This field will be 000b if Mode bits are not supported, NOTE This field should be counted in clocks not number of bits received by the serial flash. **Example:** If 4 mode bits are needed with a single input address phase command, this field would be 100b.
4:0	**(1-1-2) Fast Read Number of Wait states (dummy clocks) needed before valid output** This field should be programmed with 01000b for 8 clocks of dummy cycle. (The number of dummy clocks should be > 0 to avoid contention on bi-directional pins.) NOTE For legacy reasons, if dummy clocks for this instruction is not 01000b, then bit 16 in 6.4.1 (Supports (1-1-2) Fast Read with 8 wait states) must NOT be set to '1'.

6.4.5 JEDEC Basic Flash Parameter Table: 5th DWORD

Bits	Description
31:5	Reserved. These bits default to all 1's
4	**Supports (4-4-4) Fast Read** Device supports Quad input instruction & address and quad output data Fast Read. 0: (4-4-4) Fast Read NOT supported. 1: (4-4-4) Fast Read supported.
3:1	Reserved. These bits default to all 1's
0	**Supports (2-2-2) Fast Read** Device supports dual input instruction& address and dual output data Fast Read. 0: (2-2-2) Fast Read NOT supported. 1: (2-2-2) Fast Read supported.

6.4.6 JEDEC Basic Flash Parameter Table: 6th DWORD

Bits	Description
31:24	**(2-2-2) Fast Read Instruction** Instruction for dual input instruction& address and dual output data Fast Read.
23:21	**(2-2-2) Fast Read Number of Mode Clocks** This field will be 000b if Mode bits are not supported, NOTE This field should be counted in clocks not number of bits received by the serial flash. The master drives the bus during "mode bits" cycles; the master tri-states the bus during "dummy" cycles. **Example:** If 4 mode bits are needed with a (2-2-2) Fast Read command, this field would be 010b.
20:16	**(2-2-2) Fast Read Number of Wait states (dummy clocks) needed before valid output** This field will be 00000b if wait states/dummy clocks are not supported. (The number of dummy clocks should be > 0 to avoid contention on bi-directional pins.) **Example:** If 8 bits are needed with a (2-2-2) Fast Read command, this field would be 00100b.
15:0	Reserved. These bits default to all 1's

6.4.7 JEDEC Basic Flash Parameter Table: 7th DWORD

Bits	Description
31:24	**(4-4-4) Fast Read Instruction** Instruction for quad input instruction/address, quad output data Fast Read.
23:21	**(4-4-4) Fast Read Number of Mode Clocks** This field will be 000b if Mode bits are not supported, NOTE This field should be counted in clocks not number of bits received by the serial flash. The master drives the bus during "mode bits" cycles; the master tri-states the bus during "dummy" cycles. **Example:** If 8 mode bits are needed with a (4-4-4) Fast Read phase command, this field would be 010b.
20:16	**(4-4-4) Fast Read Number of Wait states (dummy clocks) needed before valid output** This field will be 00000b if wait states/dummy clocks are not supported. (The number of dummy clocks should be > 0 to avoid contention on bi-directional pins.) **Example:** If 16 bits are needed with a (4-4-4) Fast Read phase command, this field would be 00100b.
15:0	Reserved. These bits default to all 1's

6.4.8 JEDEC Basic Flash Parameter Table: 8th DWORD

NOTE If the device uses a 4k subsector size, that size and instruction must be included somewhere in DWORDs 8 or 9. This allows the user to discover the typical and maximum erase times for the 4k subsector by referencing DWORD 10.

Bits	Description
31:24	**Sector Type 2 Instruction** Instruction used to erase the number of bytes specified by Sector Type 2 Size (bits 23-16).
23:16	**Sector Type 2 Size:** This field will be 00h if this sector type does not exist. NOTE This field specifies 'N' and is used to calculate sector/block size = 2^N bytes **Example:** If the sector size is 32 kilobytes, this field would 0Fh.
15:8	**Sector Type 1 Instruction** Instruction used to erase the number of bytes specified by Sector Type 1 Size (bits 7-0).
7:0	**Sector Type 1 Size** NOTE This field specifies 'N' and is used to calculate sector/block size = 2^N bytes **Example:** If the sector size is 4 kilobytes, this field would 0Ch.

6.4.9 JEDEC Basic Flash Parameter Table: 9th DWORD

Bits	Description
31:24	**Sector Type 4 Instruction** Instruction used to erase the number of bytes specified by Sector Type 4 Size (bits 23-16).
23:16	**Sector Type 4 Size** This field will be 00h if this sector type does not exist. NOTE This field specifies 'N' and is used to calculate sector/block size = 2^N bytes **Example:** If the sector size is 256 kilobytes, this field would 12h.
15:8	**Sector Type 3 Instruction** Instruction used to erase the number of bytes specified by Sector Type 3 Size (bits 7-0).
7:0	**Sector Type 3 Size** This field will be 00h if this sector type does not exist. NOTE This field specifies 'N' and is used to calculate sector/block size = 2^N bytes **Example:** If the sector size is 64 kilobytes, this field would 10h.

6.4.10 JEDEC Basic Flash Parameter Table: 10th DWORD

Bits	Description
31:25	**Sector Type 4 Erase, Typical time** Time the device *typically* takes to erase a sector of Type 4 size, see 6.4.9. User must poll device busy to determine if the operation has completed. This field has no meaning if the Sector Type 4 size is 00h. 31:30 units (00b: 1 ms, 01b: 16 ms, 10b: 128 ms, 11b: 1 s) 29:25 count Formula: typical time = (count + 1)*units Example: If count=2 and units=10b, then typical time is (2+1)*128ms = 384 ms The range is 1ms to 32 seconds in four groups: 1 ms to 32 ms, 16 ms to 512 ms, 128 ms to 4096 ms, 1 s to 32 s
24:18	**Sector Type 3 Erase, Typical time** Time the device *typically* takes to erase a sector of Type 3 size, see 6.4.9. User must poll device busy to determine if the operation has completed. This field has no meaning if the Sector Type 3 size is 00h. 24:23 units (00b: 1 ms, 01b: 16 ms, 10b: 128 ms, 11b: 1 s) 22:18 count Formula: typical time = (count + 1)*units Example: If count=1 and units=10b, then typical time is (1+1)*128ms = 256 ms The range is 1ms to 32 seconds in four groups: 1 ms to 32 ms, 16 ms to 512 ms, 128 ms to 4096 ms, 1 s to 32 s
17:11	**Sector Type 2 Erase, Typical time** Time the device *typically* takes to erase a sector of Type 2 size, see 6.4.8. User must poll device busy to determine if the operation has completed. This field has no meaning if the corresponding Sector Type size is 00h. 17:16 units (00b: 1 ms, 01b: 16 ms, 10b: 128 ms, 11b: 1 s) 15:11 count Formula: typical time = (count + 1)*units Example: If count=0 and units=10b, then typical time is (0+1)*128ms = 128 ms The range is 1ms to 32 seconds in four groups: 1 ms to 32 ms, 16 ms to 512 ms, 128 ms to 4096 ms, 1 s to 32 s

10:4	**Sector Type 1 Erase, Typical time** Time the device *typically* takes to erase a sector of Type 1 size, see 6.4.8. User must poll device busy to determine if the operation has completed. This field has no meaning if the corresponding Sector Type size is 00h. 10:9 units (00b: 1 ms, 01b: 16 ms, 10b: 128 ms, 11b: 1 s) 8:4 count Formula: typical time = (count + 1)*units Example: If count=1 and units=10b, then typical time is 1*128ms = 128 ms The range is 1ms to 32 seconds in four groups: 1 ms to 32 ms, 16 ms to 512 ms, 128 ms to 4096 ms, 1 s to 32 s
3:0	**Multiplier from typical erase time to maximum erase time** 3:0 count Formula: Sector Type n (or Chip) erase maximum time = 2 * (count + 1) * Sector Type n (or Chip) erase typical time Example: If count = 9, then Sector Type n (or Chip) erase maximum time is 20 * Sector Type n (or Chip) erase typical time NOTE 1 'n' = 1, 2, 3, or 4 NOTE 2 This multiplier applies to all sector erases and the chip erase. The maximum time is intended to be used as a watchdog timeout for an error or failure condition. Since a common scale factor is used across all erase sizes, any particular maximum time may only approximate the datasheet maximum time.

6.4.11 JEDEC Basic Flash Parameter Table: 11th DWORD

Bits	Description
31	**Reserved**
30:24	**Chip Erase, Typical time** Typical time to erase the entire device. User must poll device busy to determine if the operation has completed. 30:29 units (00b: 16 ms, 01b: 256 ms, 10b: 4 s, 11b: 64 s) 28:24 count Formula: typical time = (count + 1)*units Example: If count=5 and units=10b, then typical time is: 5*4 s = 20 s The range of this field is 16ms to 2048 seconds in four groups: 16 ms to 512 ms, 256 ms to 8192 ms, 4 s to 128 s, 64 s to 2048 s
23:19	**Byte Program Typical time, additional byte** Time the device *typically* takes to write each additional byte after the first. User must poll device busy to determine if the operation has completed. 23 units (0: 1 us, 1: 8 us) 22:19 count Formula: additional byte time = (count + 1)*units/byte Example: If units = 1 and count =4, then each additional byte typically adds (4+1)*8 us = 40 us to the programming time. For 16 bytes, the additional time would be 16 * 40 us = 640 us The range is 1 us to 128 us in two groups: 1 us to 16 us and 8 us to 128 us. NOTE The programming time for small numbers of bytes does not scale linearly up to a full page programming time. When the number of bytes being programmed exceeds ½ of a page size, users should base estimates on the Page Program typical time in this DWORD.
18:14	**Byte Program Typical time, first byte** Time the device *typically* takes to write the first byte in a sequence. User must poll device busy to determine if the operation has completed. 18 units (0: 1 us, 1: 8 us) 17:14 count Formula: first byte typical time = (count + 1)*units Example: If units = 0 and count = 7, then typical time is (7+1)*1 us = 8 us The range is 1 us to 128 us in two groups: 1 us to 16 us and 8 us to 128 us

13:8	**Page Program Typical time** Time the device *typically* takes to write a full page. User must poll device busy to determine if the operation has completed. The user may scale this by ½ or ¼ to determine approximate times for ½ and ¼ page program operations 13 units (0: 8 us, 1: 64 us) 12:8 count Formula: typical page program time = (count + 1)*units The range is 8 us to 2048 us in two groups: 8 us to 256 us and 64 us to 2048 us
7:4	**Page Size** This field specifies 'N' and is used to calculate page size = 2^N bytes.
3:0	**Multiplier from typical time to max time for Page or byte program** 3:0 count Formula: maximum time = 2 * (count + 1)*typical time NOTE This multiplier applies to all page or byte typical program times. The maximum time is intended to be used as a watchdog timeout for an error or failure condition. Since a common scale factor is used across all program sizes, any particular maximum time may only approximate the datasheet maximum time.

6.4.12 JEDEC Basic Flash Parameter Table: 12th DWORD

Bits	Description
31	**Suspend / Resume supported** The device supports suspend and resume of both program and erase operations. 0: supported 1: not supported
30:24	**Suspend in-progress erase max latency** Maximum time required by the flash device to suspend an in-progress erase and be ready to accept another command which accesses the flash array. This time does not apply to the read status command. See also *Suspend in-progress program in this DWORD.* 30:29 units (00b: 128ns, 01b: 1us, 10b: 8us, 11b: 64us) 28:24 count Formula: erase max latency = (count + 1)*units Example: if units =01b and count =19, then erase max latency = (19+1)*1 us = 20 us The range is 128 ns to 2048 us in four groups: 128 ns to 4**.** 096 us, 1 us to 32 us, 8 us to 256 us, 64 us to 2048 us
23:20	**Erase Resume to Suspend Interval** The device requires this typical amount of time to make progress on the erase before allowing another suspend. 23:20 count of fixed units of 64us Formula: erase resume to suspend interval = (count + 1)*64 us Example: if count = 7, the erase resume to suspend interval = (7+1)*64 us = 512 us The range is 64 us to 1024 us
19:13	**Suspend in-progress program max latency** Maximum time required by the flash device to suspend an in-progress program and be ready to accept another command which accesses the flash array. This time does not apply to the read status command. See also *Suspend in-progress erase in this DWORD.* 19:18 units (00b: 128ns, 01b: 1us, 10b: 8us, 11b: 64us) 17:13 count Formula: suspend in-progress program max latency = (count+1)*units Example: if units = 01b and count = 4, then suspend in-progress program max latency = (4+1)*1 us = 5 us The range is 128 ns to 2048 us in four groups: 128 ns to 4.096 us, 1 us to 32 us, 8 us to 256 us, and 64 us to 2048 us.

12:9	**Program Resume to Suspend Interval** The device requires this typical amount of time to make progress on the program operation before allowing another suspend. 12:9 count of fixed units of 64us Formula: program resume to suspend interval = (count + 1)*64 us Example: if count = 15, the erase resume to suspend interval = (15+1)*64 us = 1024 us The range is 64 us to 1024 us
8	**Reserved**
7:4	**Prohibited Operations During Erase Suspend** xxx0b: May not initiate a new erase anywhere (erase nesting not permitted) xxx1b: May not initiate a new erase in the erase suspended sector size xx0xb: May not initiate a page program anywhere xx1xb: May not initiate a page program in the erase suspended sector size x0xxb: Refer to vendor datasheet for read restrictions x1xxb: May not initiate a read in the erase suspended sector size 0xxxb: Additional erase or program restrictions apply 1xxxb: The erase and program restrictions in bits 5:4 are sufficient NOTE This list is not comprehensive. Consult the device datasheet for a full list of allowed and prohibited operations.
3:0	**Prohibited Operations During Program Suspend** xxx0b: May not initiate a new erase anywhere (erase nesting not permitted) xxx1b: May not initiate a new erase in the program suspended page size xx0xb: May not initiate a new page program anywhere (program nesting not permitted) xx1xb: May not initiate a new page program in the program suspended page size x0xxb: Refer to vendor datasheet for read restrictions x1xxb: May not initiate a read in the program suspended page size 0xxxb: Additional erase or program restrictions apply 1xxxb: The erase and program restrictions in bits 1:0 are sufficient NOTE This list is not comprehensive. Consult the device datasheet for a full list of allowed and prohibited operations.

6.4.13 JEDEC Basic Flash Parameter Table: 13th DWORD

Bits	Description
31:24	**Suspend Instruction** Instruction used to suspend a write or erase type operation.
23:16	**Resume Instruction** Instruction used to resume a write or erase type operation.
15:8	**Program Suspend Instruction** Instruction used to suspend a program operation. (If the device requires a unique instruction to suspend a "program" command then that instruction is listed here. Otherwise this field contains the same value as the "Suspend Instruction" field above.)
7:0	**Program Resume Instruction** Instruction used to resume a program operation. (If the device requires a unique instruction to resume a "program" command then that instruction is listed here. Otherwise this field contains the same value as the "Resume Instruction" field above.)

6.4.14 JEDEC Basic Flash Parameter Table: 14th DWORD

Bits	Description
31	**Deep Powerdown Supported** 0: supported 1: not supported
30:23	**Enter Deep Powerdown Instruction** Instruction used to enter deep powerdown
22:15	**Exit Deep Powerdown Instruction** Instruction used to exit deep powerdown
14:8	**Exit Deep Powerdown to next operation delay** Maximum time required by the flash device to exit Deep Powerdown and be ready to accept any command. (Note: Read status is not valid when exiting deep powerdown.) 14:13 units (00b: 128ns, 01b: 1us, 10b: 8us, 11b: 64us) 12:8 count Formula: exit Deep Powerdown to next operation delay = (count+1)*units Example: if units = 10b and count = 4, then delay = (4+1)*8 us = 40 us The range is 128 ns to 2048 us in four groups: 128 ns to 4.096 us, 1 us to 32 us, 8 us to 256 us, and 64 us to 2048 us

7:2	**Status Register Polling Device Busy** This bit field defines various ways the flash device's busy status may be polled. A zero in a bit position indicates that the device does not support the particular polling method. 1x_xxxxb: Reserved x1_xxxxb: Reserved xx_1xxxb: Reserved xx_x1xxb: Reserved xx_xx1xb: Bit 7 of the Flag Status Register may be polled any time a Program, Erase, Suspend/Resume command is issued, or after a Reset command while the device is busy. The read instruction is 70h. Flag Status Register bit definitions: bit[7]: Program or erase controller status (0=busy; 1=ready) xx_xxx1b: Use of legacy polling is supported by reading the Status Register with 05h instruction and checking WIP bit[0] (0=ready; 1=busy).
1:0	**Reserved**

6.4.15 JEDEC Basic Flash Parameter Table: 15th DWORD

Bits	Description
31:24	**Reserved**
23	**HOLD and WP Disable** Defines whether HOLD and WP may be disabled via a configuration register If driving DQ2 and DQ3 high during command phase WP and HOLD do not need to be disabled. Device decodes instruction to determine functionality of HOLD/WP vs. data 1: set bit 4 of the Non-Volatile Extended Configuration Register = 0 to disable HOLD and WP 0: above feature is not supported
22:20	**Quad Enable Requirements (QER):** This field describes whether the device contains a Quad Enable (QE) bit used to enable 1-1-4 and 1-4-4 quad read or quad program operations. If QE exists, this field also identifies the bit location and method to set/clear the bit. In this standard, status register 1 refers to the first data byte transferred on a Read Status (05h) or Write Status (01h) command. Status register 2 refers to the byte read using instruction 35h. Status register 2 is the second byte transferred in a Write Status (01h) command. Bits are numbered from 7 to 0, where bit 7 is transferred first on the wire. NOTE Industry naming and definitions of these status registers may differ. The user will typically perform a read-modify-write sequence of operations to maintain the state of all other writable status register bits. For example read both status registers, set/clear QE, Write Status with both data bytes. 000b: Device does not have a QE bit. Device detects 1-1-4 and 1-4-4 reads based on instruction. DQ3/HOLD# functions as hold during instruction phase. 001b: QE is bit 1 of status register 2. It is set via Write Status with two data bytes where bit 1 of the second byte is one. It is cleared via Write Status with two data bytes where bit 1 of the second byte is zero. Writing only one byte to the status register has the side-effect of clearing status register 2, including the QE bit. The 100b code is used if writing one byte to the status register does not modify status register 2. 010b: QE is bit 6 of status register 1. It is set via Write Status with one data byte where bit 6 is one. It is cleared via Write Status with one data byte where bit 6 is zero.. 011b: QE is bit 7 of status register 2. It is set via Write status register 2 instruction 3Eh with one data byte where bit 7 is one. It is cleared via Write status register 2 instruction 3Eh with one data byte where bit 7 is zero. The status register 2 is read using instruction 3Fh. 100b: QE is bit 1 of status register 2. It is set via Write Status with two data bytes where bit 1 of the second byte is one. It is cleared via Write Status with two data bytes where bit 1 of the second byte is zero. In contrast to the 001b code, writing one byte to the status register does not modify status register 2. 101b: QE is bit 1 of the status register 2. Status register 1 is read using Read Status instruction 05h. Status register 2 is read using instruction 35h. QE is set via Write Status instruction 01h with two data bytes where bit 1 of the second byte is one. It is cleared via Write Status with two data bytes where bit 1 of the second byte is zero. other: reserved

19:16	**0-4-4 Mode Entry Method:** xxx1b: Mode Bits[7:0] = A5h Note: QE must be set prior to using this mode xx1xb: Read the 8-bit volatile configuration register with instruction 85h, set XIP bit[3] in the data read, and write the modified data using the instruction 81h, then Mode Bits [7:0] = 01h x1xxb: Reserved 1xxxb: Reserved
15:10	**0-4-4 Mode Exit Method** xx_xxx1b: Mode Bits[7:0] = 00h will terminate this mode at the end of the current read operation xx_xx1xb: If 3-Byte address active, input Fh on DQ0-DQ3 for 8 clocks. If 4-Byte address active, input Fh on DQ0-DQ3 for 10 clocks. This will terminate the mode prior to the next read operation. xx_x1xxb: Reserved xx_1xxxb: Input Fh (mode bit reset) on DQ0-DQ3 for 8 clocks. This will terminate the mode prior to the next read operation. x1_xxxxb: Reserved. 1x_xxxxb: Reserved
9	**0-4-4 mode supported** This mode is variously referred to as implied instruction, continuous read, execute in place, etc. 0: not supported 1: supported
8:4	**4-4-4 mode enable sequences** This field describes the supported methods to enter 4-4-4 mode from 1-1-1 mode. x_xxx1b: set QE per QER description above, then issue instruction 38h x_xx1xb: issue instruction 38h x_x1xxb: issue instruction 35h x_1xxxb: device uses a read-modify-write sequence of operations: read configuration using instruction 65h followed by address 800003h, set bit 6, write configuration using instruction 71h followed by address 800003h. This configuration is volatile. 1_xxxxb: Reserved NOTE If device is in 0-4-4 mode, then this mode must be exited before the 4-4-4 enable sequence is issued.
3:0	**4-4-4 mode disable sequences** This field describes the supported methods to exit 4-4-4 mode. xxx1b: issue FFh instruction xx1xb: issue F5h instruction x1xxb: device uses a read-modify-write sequence of operations: read configuration using instruction 65h followed by address 800003h, clear bit 6, write configuration using instruction 71h followed by address 800003h.. This configuration is volatile. 1xxxb: issue the Soft Reset 66/99 sequence, see 6.4.16 NOTE If device is in 0-4-4 mode, then this mode must be exited before the 4-4-4 disable sequence is issued.

6.4.16 JEDEC Basic Flash Parameter Table: 16th DWORD

Bits	Description
31:24	**Enter 4-Byte Addressing** This field defines the supported methods to enter 4-byte addressing mode or to use an extended address register with 3-byte addressing to access memory above 16 MBytes. xxxx_xxx1b: issue instruction B7h (preceding write enable not required) xxxx_xx1xb: issue write enable instruction 06h, then issue instruction B7h xxxx_x1xxb: 8-bit volatile extended address register used to define A[31:24] bits. Read with instruction C8h. Write instruction is C5h with 1 byte of data. Select the active 128 Mbit memory segment by setting the appropriate A[31:24] bits and use 3-Byte addressing. xxxx_1xxxb: 8-bit volatile bank register used to define A[30:A24] bits. MSB (bit[7]) is used to enable/disable 4-byte address mode. When MSB is set to '1', 4-byte address mode is active and A[30:24] bits are don't care. Read with instruction 16h. Write instruction is 17h with 1 byte of data. When MSB is cleared to '0', select the active 128 Mbit segment by setting the appropriate A[30:24] bits and use 3-Byte addressing. xxx1_xxxxb: A 16-bit nonvolatile configuration register controls 3-Byte/4-Byte address mode. Read instruction is B5h. Bit[0] controls address mode [0=3-Byte; 1=4-Byte]. Write configuration register instruction is B1h, data length is 2 bytes. xx1x_xxxxb: Supports dedicated 4-Byte address instruction set. Consult vendor data sheet for the instruction set definition. x1xx_xxxxb: Always operates in 4-Byte address mode 1xxx_xxxxb: Reserved
23:14	**Exit 4-Byte Addressing** xx_xxxx_xxx1b: issue instruction E9h to exit 4-Byte address mode (write enable instruction 06h is not required) xx_xxxx_xx1xb: issue write enable instruction 06h, then issue instruction E9h to exit 4-Byte address mode xx_xxxx_x1xxb: 8-bit volatile extended address register used to define A[31:A24] bits. Read with instruction C8h. Write instruction is C5h, data length is 1 byte. Return to lowest memory segment by setting A[31:24] to 00h and use 3-Byte addressing. xx_xxxx_1xxxb: 8-bit volatile bank register used to define A[30:A24] bits. MSB (bit[7]) is used to enable/disable 4-byte address mode. When MSB is cleared to '0', 3-byte address mode is active and A30:A24 are used to select the active 128 Mbit memory segment. Read with instruction 16h. Write instruction is 17h, data length is 1 byte. xx_xxx1_xxxxb: A 16-bit nonvolatile configuration register controls 3-Byte/4-Byte address mode. Read instruction is B5h. Bit[0] controls address mode [0=3-Byte; 1=4-Byte]. Write configuration register instruction is B1h, data length is 2 bytes. xx_xx1x_xxxxb: Hardware reset xx_x1xx_xxxxb: Software reset (see bits 13:8 in this DWORD) xx_1xxx_xxxxb: Power cycle x1_xxxx_xxxxb: Reserved 1x_xxxx_xxxxb: Reserved

13:8	**Soft Reset and Rescue Sequence Support** This field specifies how to return the device to its default power-on state. 00_0000b: no software reset instruction is supported xx_xxx1b: drive Fh on all 4 data wires for 8 clocks xx_xx1xb: drive Fh on all 4 data wires for 10 clocks if device is operating in 4-byte address mode xx_x1xxb: drive Fh on all 4 data wires for 16 clocks xx_1xxxb: issue instruction F0h x1_xxxxb: issue reset enable instruction 66h, then issue reset instruction 99h. The reset enable, reset sequence may be issued on 1, 2, or 4 wires depending on the device operating mode. 1x_xxxxb: exit 0-4-4 mode is required prior to other reset sequences above if the device may be operating in this mode. See 6.4.15, 0-4-4 Mode Exit
7	**Reserved**
6:0	**Volatile or Non-Volatile Register and Write Enable Instruction for Status Register 1** The instruction 01h is typically used to write status register 1 which contains Block Protection (BP) and other bits. Status register 1 is written by the first data byte following the instruction 01h. The protection bits must be written to zero to enable writes/erases to the device. This field describes how to modify the writable bits in status register 1 in either a volatile or non-volatile manner. Bits 1:0 in status register 1 are de-facto standard write enable and busy status and are excluded from the definitions below. xxx_xxx1b: Non-Volatile Status Register 1, powers-up to last written value, use instruction 06h to enable write xxx_xx1xb: Volatile Status Register 1, status register powers-up with bits set to "1"s, use instruction 06h to enable write xxx_x1xxb: Volatile Status Register 1, status register powers-up with bits set to "1"s, use instruction 50h to enable write xxx_1xxxb: Non-Volatile/Volatile status register 1 powers-up to last written value in the non-volatile status register, use instruction 06h to enable write to non-volatile status register. Volatile status register may be activated after power-up to override the non-volatile status register, use instruction 50h to enable write and activate the volatile status register. xx1_xxxxb: Status Register 1 contains a mix of volatile and non-volatile bits. The 06h instruction is used to enable writing of the register. x1x_xxxxb: Reserved 1xx_xxxxb: Reserved NOTE If the status register is read-only then this field will contain all zeros in bits 4:0.

7 Rules for Header and Table Additions and Modifications

- Additional headers and parameter tables can be added by vendors without JEDEC approval.
- The first four DWORDs of the 6.4 JEDEC Flash Parameters Table can never be modified.
- New headers must be built using exactly two DWORDs and they must immediately follow the existing header(s).
- Minimum parameter table size is one DWORD. The maximum parameter table size is not specified.
- Parameter tables may be located anywhere in the SFDP space. They do not need to immediately follow the parameter headers.
- Overlapping parameter tables are permitted.

8 Legacy Compatibility

Prior to the release of this standard, Intel published SFDP guidelines with a four DWORD parameter table. The first four DWORDs of the JEDEC Basic Parameter Table are identical to the table in Intel's guidelines. Devices in production prior to the release of the initial JESD216 standard might only contain these four DWORDs. Revision A increased the number of DWORDs from nine to sixteen. The first nine DWORDs in Revision A maintain backwards compatibility. Devices in production prior to the release of this revision may not contain all of the currently defined DWORDs.

Annex A (informative)-Example SFDP Discovery Code

```
// C-syntax pseudo code for discovering SFDP table
// This code is provided as an example. It is not optimized.
// Code searches flash for the highest revision table that the driver
supports.
// Code assumes that driver can support all revisions up to and including
// some maximum supported revision.
// Use three functions:
// spi()            performs a SPI flash operation
// update_current() updates global Parameter Header variables from the
//                  data buffer of bytes read from flash
// find_table()     checks for a valid SFDP header in flash and sets
//                  global Parameter Header variables to the
//                  highest revision supported by the driver

#include <stdbool.h>
#define JEDEC_TABLE_ID 0
#define READ_SFDP      0x5A

int ms_major_rev = 1;       // maximum major revision supported by driver
int ms_minor_rev = 0;       // maximum minor revision supported by driver

int NPH = 0;                // Number of Parameter Headers
int sfdp_major_revision = 0;
int sfdp_minor_revision = 0;

int curr_major_rev = 0; // current Parameter Table revision
int curr_minor_rev = 0; // current Parameter Table revision
int curr_PTP = 0;       // current Parameter Table Pointer
int curr_length = 0;    // current parameter table length in dwords
int curr_address = 0;   // current address

bool table_found = false;

#define MAX_BYTES 128
unsigned char data[MAX_BYTES];

extern void
spi(int opcode, int address, int byte_count, unsigned char *buffer);
// the implementation of spi() is flash-controller dependent

void
update_current()
{
  curr_minor_rev = data[1];
  curr_major_rev = data[2];
  curr_length    = data[3];
  curr_PTP       = (data[6] << 16) | (data[5] << 8) | (data[4]);
}

bool
find_table()
{
```

```
  // Read the first 8 bytes of the SFDP header. If the device does not
  // support SFDP it will not drive any return data to the controller.
  // This example code does not make use of the SFDP major/minor revision.
  spi(READ_SFDP, curr_address, 8, data);

  // check signature
  if (!(data[0] == "S" &&
        data[1] == "F" &&
        data[2] == "D" &&
        data[3] == "P"))
  {
    return false;
  }

  NPH = data[6];
  sfdp_major_revision = data[5];
  sfdp_minor_revision = data[4];

  // search for highest revision JEDEC-standard table in flash device
  // loop over all parameter headers
  while (NPH >= 0)
  {
    curr_address = curr_address + 8;

    spi(READ_SFDP, curr_address, 8, data);

    if (data[0] == JEDEC_TABLE_ID)
    {
      // if the major revision is newer then minor revision is don't care
      if (data[2] >  curr_major_rev &&
          data[2] <= ms_major_rev     )
      {
        update_current();
        table_found = true;
      }
      // if the major revision is the same then use newer minor revision
      else if (data[2] == curr_major_rev &&
               data[2] <= ms_major_rev   &&
               data[1] >  curr_minor_rev &&
               data[1] <= ms_minor_rev     )
      {
        update_current();
        table_found = true;
      }
    } // end if JEDEC TABLE ID

    NPH = NPH - 1;
  } // end while NPH

  // read the parameter table into the data buffer, converting
  // dword count in curr_length to byte count
  if (table_found)
  {
    spi(READ_SFDP, curr_PTP, curr_length * 4, data);
  }
 return table_found;
}
```

Annex B (Informative) Procedure For Requesting Function Specific ID

The Function Specific ID list is not a fixed listing. Any company may request a Function Specific ID by making a request to the JEDEC office at (703) 907-7540. Updates to the list will be made periodically.

The SFDP Standard will allow Serial Flash vendors to describe the functions and features of their devices in a standard set of internal parameter tables. These internal parameter tables can be read by users to determine the characteristics of the device.

Annex C (informative) Revision History

This annex briefly describes most of the changes made to entries that appear in this standards, JESD216A, comparded to its predecessor, JESD216 (April 2011).

Extensive rewrite to clarify requirements, but functionality of JESD216 has been maintained.

The JESD216A parameter table is marked with Major Revision 1 and Minor Revision 5. Using Minor Revision 5 instead of 1 is required to avoid version conflicts with legacy devices which implemented SFDP tables prior to JEDEC standardization.

Increased the number of DWORDs in the Basic Parameters Table from nine to sixteen.

Provided hooks for future expansion using Function Specific Tables.

Added Annex A Example code for SFDP discovery

Added Annex B Procedure for requesting a Function Specific ID

Standard Improvement Form JEDEC JESD216A

The purpose of this form is to provide the Technical Committees of JEDEC with input from the industry regarding usage of the subject standard. Individuals or companies are invited to submit comments to JEDEC. All comments will be collected and dispersed to the appropriate committee(s).

If you can provide input, please complete this form and return to:

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Fax: 703.907.7583

1. I recommend changes to the following:

☐ Requirement, clause number _____

☐ Test method number _____ Clause number _____

The referenced clause number has proven to be:

☐ Unclear ☐ Too Rigid ☐ In Error

☐ Other _____

2. Recommendations for correction:

_____

_____

_____

_____

3. Other suggestions for document improvement:

_____

_____

_____

_____

Submitted by

Name: _____ Phone: _____

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