

HLSM (FINAL VERSION)

- condition/assignment
(like a mealy machine)
- If... then $P \Rightarrow Q \rightarrow P + Q$
- $\star = (\text{level} \text{ II } !\text{level}) \& (\text{pattern} == 4'b'0001 \text{ II } \text{pattern} == 4'b'0010 \text{ II } \text{pattern} == 4'b'0100 \text{ II } \text{pattern} == 4'b1000)]$

Inputs:

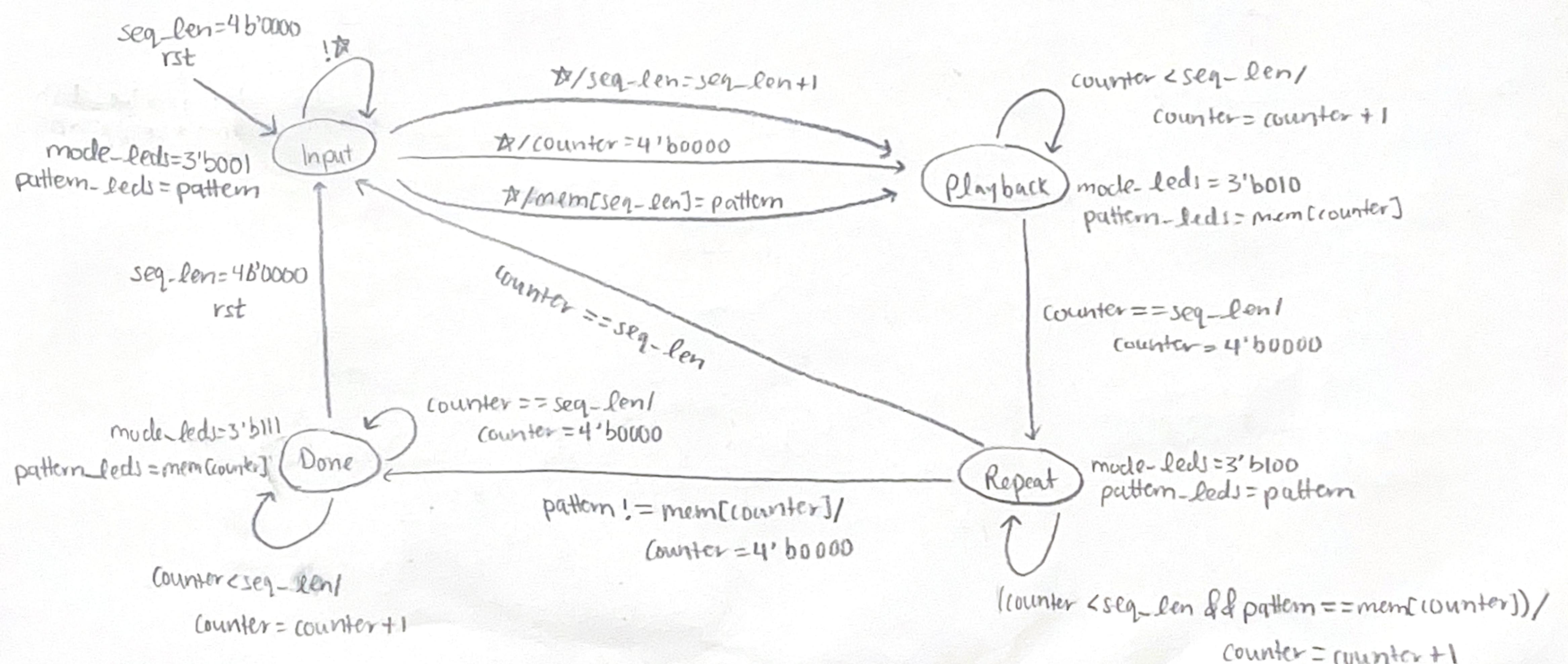
pattern[3:0] (4 bits)
level -> 1(hard)
 0(easy)
rst (1 bit)
pclK (1 bit)

Outputs:

pattern_leds[3:0] (4 bits)
mode_leds[2:0] (3 bits)

Local Registers:

seq_len[5:0] (6 bits)
counter[5:0] (6 bits)
mem[seq_len] (pattern)
(4-bit patterns in seq-len index)
(64-entry 4-bit memory)



Datapath

Datapath Components:

comparators

Counters (also a register)

64-entry 4-bit memory

- Count1 = $\$ & \& (\text{mode_leds} == 3'b001)$
- Count2 = $(\text{mode_leds} != 3'b0001)$
- w_en = $\$$

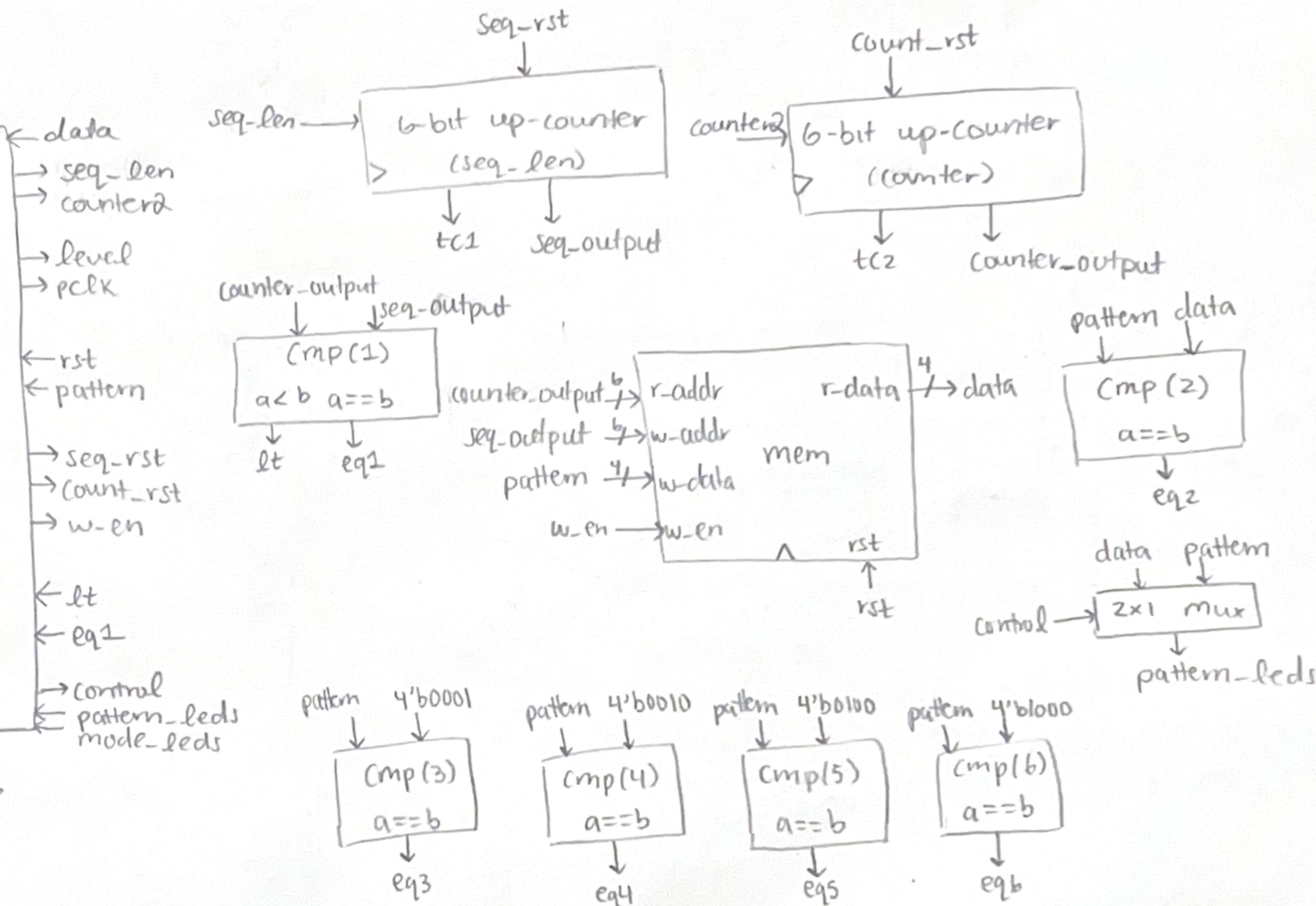
User input signals
→ pattern, rst

Controller

Combinational logic

State Register

\uparrow
eq2 eq3 eq4 eq5 eq6
 \uparrow
pattern mode-leds



FSM

$$\star = (\text{level} + [\text{level}] \cdot (\text{eq3} + \text{eq4} + \text{eq5} + \text{eq6}))$$

