Josephson junction in QUCS

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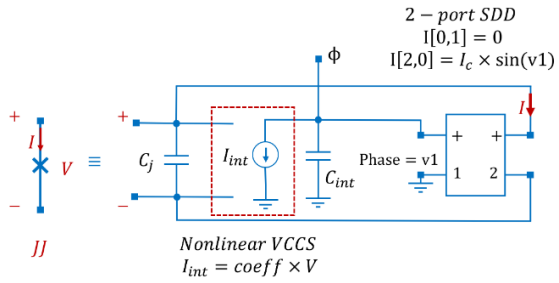
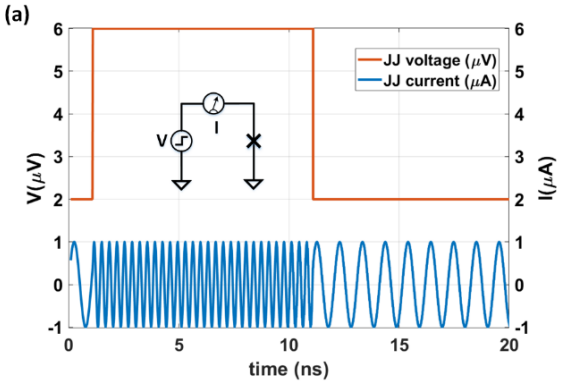
1 Introduction

The aim of this project was to recreate the classical circuit model of a Josephson Junction (JJ) first modeled in Keysight ADS in [1], see Fig. 1a, in the open source software Quite Universal Circuit Simulator (QUCS). As a comparative simulation, a transient simulation over 25 ns was used to test the performance of the model, see Fig. 1b.



(a) The circuit model of the JJ simulated in Keysight ADS, with the following values: *coeff* = 3038.5349, $C_{int} = 1\,\text{pF}$, $I_c = 1\,\mu\text{A}$ and $C_j = 6\,\text{fF}$ to 8 fF.



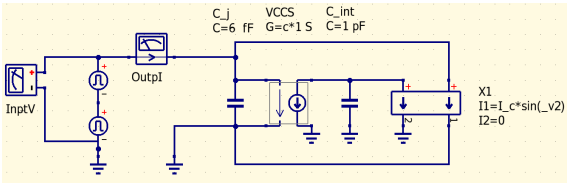
(b) Circuit response to a step function as a function of time, where the two frequencies of the output current is 0.966 GHz and 2.898 GHz for $2\,\mu\text{V}$ and $6\,\mu\text{V}$ respectively.

Fig. 1: Simulated circuit in Keysight ADS and transient response to stepfunction simulation used to validate the circuit. [1].

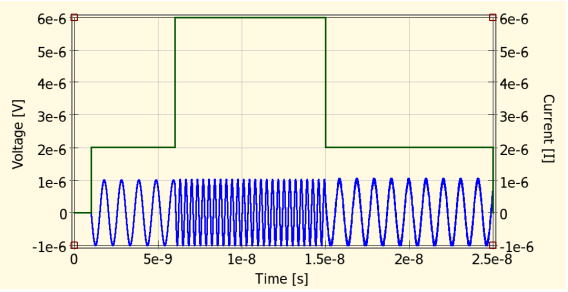
2 Simulation in QUCS

The port of the JJ circuit from ADS to QUCS can be seen in Fig. 2a where the circuit is mostly identical except for the equation defined device (EDD), SDD in ADS. The EDD does not have as high degree of customizability compared to the SDD but is sufficient for this application. All other components in ADS had an equivalent counterpart in QUCS.

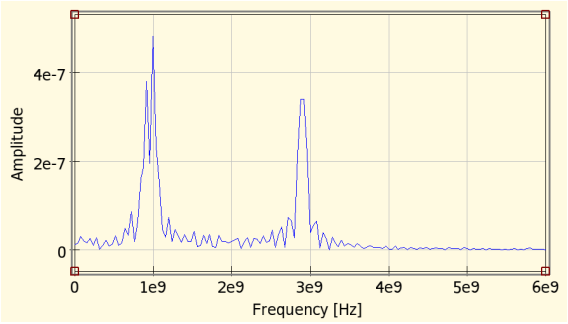
For all the simulations done in QUCS for this report the Gear 6 integration method for transient simulations was used. When comparing the setup for the transient simulation there is a key difference. Due to convergence issues in the initial DC simulation it is necessary to combine two step functions where one is a step from 0 V to the baseline voltage V_1, $2\,\mu\text{V}$ in this simulation, see Fig. 2b. Without this initial step the DC simulation cannot converge. There is also the rise time for this step function which can be set to a small value but at approximately $\leq 1 \times 10^{-3}\,\text{nS}$ the transient simulation will struggle and there is a considerable slow down. For the second step function there is no issue setting the rise time to zero even if there is a slight reduction in simulation speed for larger voltage differences, which is to be expected due to higher difficulty to converge. All values used for simulating the circuit can be seen in Table 1.



(a) The circuit model of the JJ simulated in Keysight ADS, with the following values: *coeff* $c = 3038.5349$, $C_{int} = 1\,\text{pF}$, $I_c = 1\,\mu\text{A}$ and $C_j = 6\,\text{fF}$.



(b) Circuit response to a step function as a function of time.



(c) Fourier transform of the step response in 2b.

Fig. 2: Simulated circuit in Keysight ADS and transient response to stepfunction simulation used to validate the circuit.

Table 1: Values used for the transient simulations, t_i is the time for each voltage change to V_i.

Variable:	t_{total}	t_{step}	V_0	t_1	V_1	t_2	V_2	t_3	V_3
Value:	25 ns	1×10^{-3} ns	0 V	1 ns	2 μV	6 ns	6 μV	15 ns	2 μV

For the validate the JJ simulated in QUCS the output current response for the two voltage levels should be at frequencies 0.966 GHz and 2.898 GHz for 2 μV and 6 μV respectively. For the higher frequency response is near expected, at 2.8799 GHz. The lower frequency is not as expected, there is a clear double peak where the lower is 0.9200 GHz and higher is 1.0000 GHz. The lower peak would correspond to the current before the higher step and the higher peak to the current after, see Fig. 2b, as the longer time after the step will result in a higher peak. Neither of these frequencies are at the expected 0.966 GHz. This frequency error appears first in the voltage over C_{int} which for the same two current values get a steeper voltage change. Hence, the error is probably introduced in either C_{int} or in the EDD.

Considering the three lines in Fig. 3, from this it seems that it is not the EDD which causes the frequency error. This is as the current flowing into the EDD is zero at all times and as such V should rise linearly over the capacitance as a function of I ($I = \frac{\mathrm{d}V}{\mathrm{d}t}$). However, the voltage plot has different incline for the same voltage.

This effect is dependent on the relative length the higher voltage step. Where the correct output current is observed for simulations where the time at higher voltage is less than approximately 24% of the total simulation time or more. Which was determined by testing different length for the high voltage step for two different simulation times 25 ns and 250 ns. For the these simulations the higher voltage step is centred so that the time is equal for the two voltage steps and the number of points were 40 000 steps and 400 000 steps. Changing to a non-zero rise and fall time (0.5 ns) the results did not change.

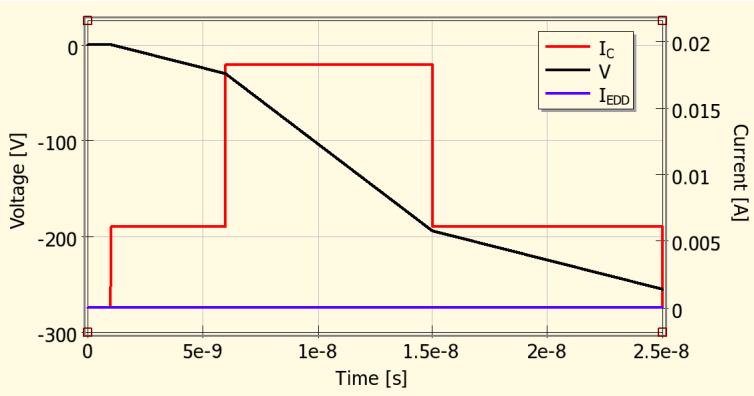


Fig. 3: Here the current to the EDD and through C_{int} is show together with the voltage.

3 Conclusion

From the simulations that have been done for this report it seems that the error induced by the voltage step is caused by an error in the solver. This conclusion is based on that without the higher voltage step the expected frequency is reached and there relation between voltage and current for a ideal capacitor is not followed as expected. Further more, the splitting of the peak is heavily dependent on how large time is spent at the higher voltage level for which there is no physical reason.

To explore this further one could test different height of the voltage step, different rise/fall times as well as different solver than used in these simulations.

References

[1] D. Shiri, H. R. Nilsson, P. Telluri, *et al.*, *Modeling and harmonic balance analysis of parametric amplifiers for qubit read-out*, 2024. arXiv: `2306.05177 [quant-ph]`. [Online]. Available: `https://arxiv.org/abs/2306.05177`.