King's College London

This paper is part of an examination of the College counting toward the award of a degree. Examinations are governed by the College Regulations under the authority of the Academic Board.

Degree Programmes BSc, MSci

Module Code **4CCS1CS1**
Module Title **Computer Systems 1**

Examination Period

Time Allowed ONE HOURS
Rubric *ANSWER **ALL** QUESTIONS*

Calculators Calculators are permitted. The following models are permitted: Casio fx83 / Casio fx85

PLEASE COMPLETE YOUR ANSWERS IN THIS BOOKLET AND PROVIDE YOUR CANDIDATE NUMBER BELOW	
CANDIDATE NUMBER	

HAND THIS PAPER IN TO THE INVIGILATOR AT THE END OF THE EXAMINATION

PLEASE DO NOT REMOVE THIS PAPER FROM THE EXAMINATION ROOM

Question 1

Express 74 (decimal) in

a. 8-bit Unsigned binary

b.8-bit sign-and-magnitude form

c.8-bit one's-complement form

d. 8-bit two's-complement form

e. unsigned hexadecimal

Question 2

Perform the following base conversion using subtraction or division-remainder: 586_{10} = _____ $_5$

Question 3

Convert the fixed-point binary form 1100.0110 to decimal

Question 4

a. Evaluate the binary sum 00101010 + 00111111

b. Evaluate in 8-bit two's complement form 31 – 64 (decimal)

c. Multiply 01010101 (binary) by 11 (binary)

Question 5

a. How many bytes of RAM can be addressed using 10 bits?

b. How many bytes are needed to address 1024 GB of RAM?

Question 6

a. Display the binary representation of 15.0625 (decimal) according to the IEEE-754 single precision standard (1 sign bit, 8 exponent bits biased by 127, 23 significand bits with an implied normalising bit)

b. Find the maximum relative error of IEEE-754 single precision representation.

c.What happens if a single-precision number is larger than this value?

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Question 7

Consider a byte-addressable computer with 16-bit addresses, a cache capable of storing a total of 1K bytes of data, and blocks of 16 bytes. Show the format (include field names and sizes) of a 16-bit memory address for:

a. direct mapped

b. fully associative

c. Where (which block or set) in cache would the memory address $BEEF_{16}$ be mapped for each of two mapping techniques above? You can specify the answer in decimal if you wish.

Question **8**

Trace the execution of the MARIE program below, showing the contents of AC, X and S at each step, and the final output, when it is provided with the following (decimal) inputs: 17 42 -28 0

100 Clear
101 Store S
102 Input
103 Store X
104 Add S
105 Store S
106 Load X
107 Skipcond 400
108 Jump 102
109 Load S
110 Output
111 Halt

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Question **9**

Consider the execution of the Java statement:

Result = (A + B) - (C + D)

a. write down the MARIE code for using a processor that has just one register for holding memory data values.

b. determine the number of memory accesses necessary of case (a)

c. write down the MARIE code for perform the same arithmetic computation for a processor that has at least 4 registers for holding memory data values.

d. determine the number of memory accesses necessary of case (c)

Question **10**

Show how the following value "ABC123E1$_{16}$" would be stored by byte-addressable machines with 32-bit words, using little endian and then big endian format. Assume each value starts at address 10_{16}. Draw a diagram of memory, placing the appropriate values in the correct (and labeled) memory locations.

Address	10_{16}	11_{16}	12_{16}	13_{16}
Big Endian				
Little Endian				

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Question **11**

MARIE's Instruction Set contains 13 instructions. Each instruction is 16 bits in length and may use either direct or indirect mode addressing.

a. Consider the MARIE instruction {AddI ADD}. Write down the binary machine code for this instruction and label the bits containing the opcode and address field.

b. Write down the operations involved in executing {AddI ADD} using register transfer language.

c. Does {AddI ADD} use direct or indirect mode addressing? Name two other instructions from the MARIE Instruction Set that use direct mode addressing.

Question 12

A nonpipelined system takes 200ns to process a task. The same task can be processed in a 20-segment pipeline with a clock cycle of 10ns.

a. Determine the speedup ratio of the pipeline for 60 tasks

b. What is the theoretical speedup that could be achieved with the pipeline system over a nonpipelined system?

Question 13

A certain microprocessor requires 2, 6, 9, or 12 machine cycles to perform various operations. 30% percent of its instructions require 2 machine cycles, 20% require 6 machine cycles, 10% require 9 machine cycles, and 40% require 12 machine cycles.

a. What is the average number of machine cycles per instruction for this microprocessor?

b. Suppose this system requires on average an extra 10 machine cycles to retrieve an operand from memory. It has to go to memory 30% of the time. What is the average number of machine cycles per instruction for this microprocessor including its memory fetch instructions?

Question **14**

A computer with a single cache (access time 20ns) and main memory (access time 300ns) also uses the hard disk (average access time 0.02 ms) for virtual memory pages. Assume the page table is **only** accessed when cache miss occurs and the cache and memory are accessed in sequential, if it is found that the cache hit rate is 90% and the page fault rate is 1%.

a. calculate the effective (average) access time (EAT) of this system.

b. What is the speed-up due to the use of cache?