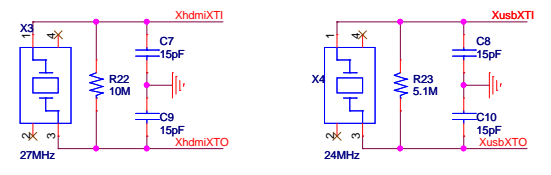
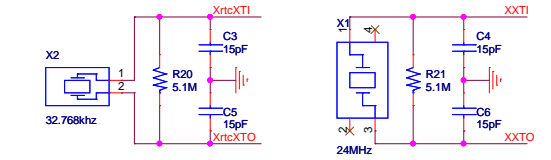
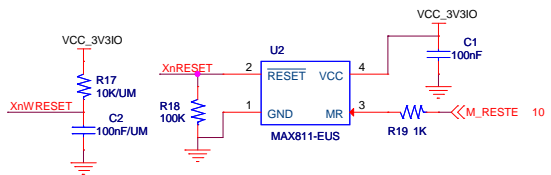
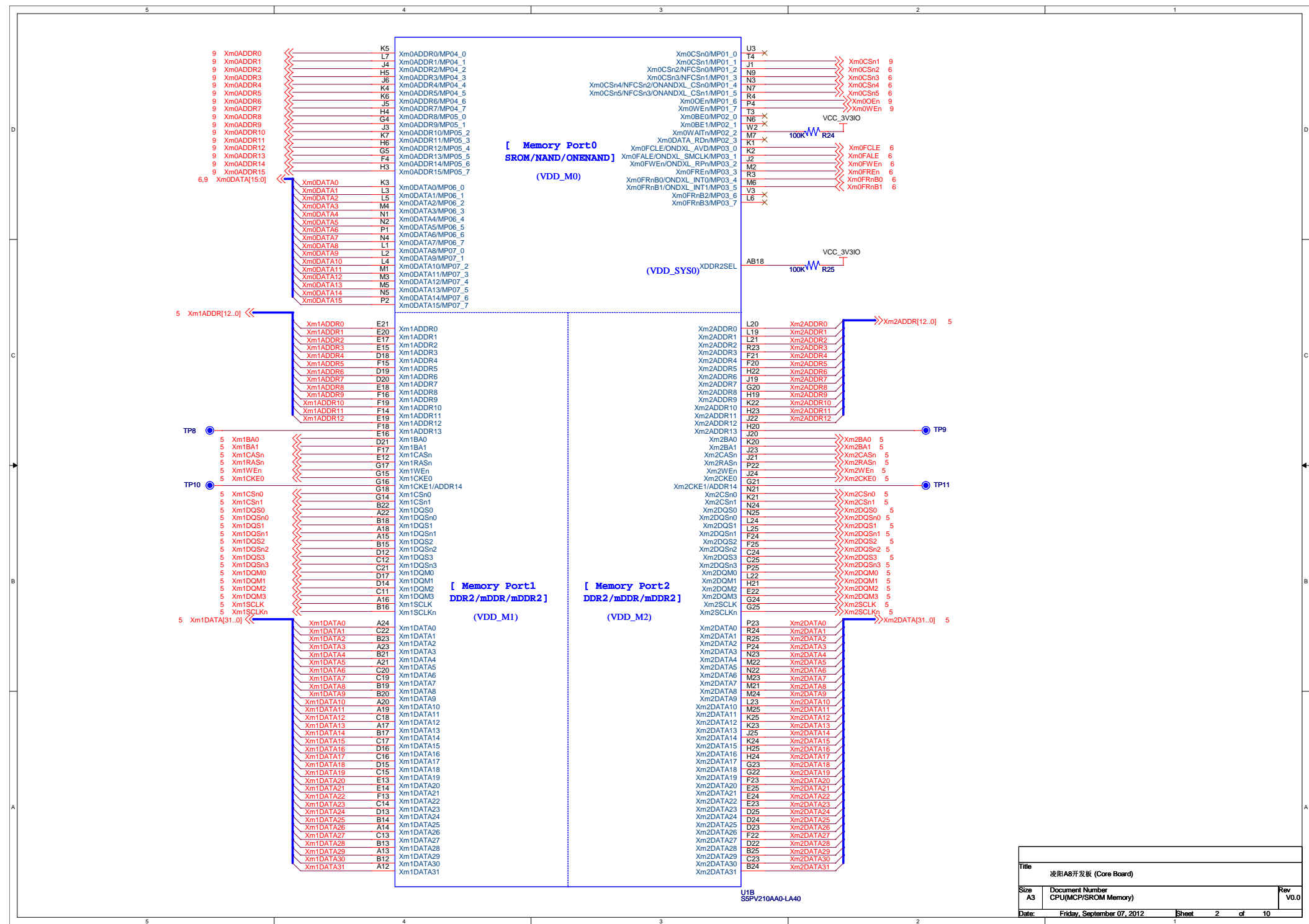


OM[5]	OM[4: 1]	OM[0]	Storage
Boot Seq.	0 0 0 0	PLL	NAND 512B-4cycle
1: USB->	0 0 0 1	Clock	NAND 2KB-5cycle
UART->	0 1 0 0	Source	NAND 4KB-5cycle 8-ECC
Storage	0 1 0 1	0: X-TAL	OneNAND Mux(Audi)
	0 1 1 0		SD/MMC
	0 1 1 1		eMMC(4bit)
Boot Seq.	1 0 0 0	1: X-TAL (USB)	Reserved
0: Storage	1 0 0 1		NAND 2KByte Page, 4cycle
	1 0 1 0		iROM NOR boot
	1 0 1 1		eMMC(8bit)





Title			
凌阳A8开发板 (Core Board)			
Size	Document Number	Rev	
A3	CPU(MCP/SROM Memory)	V0.0	
Date:	Friday, September 07, 2012	Sheet	2 of 10

10 XvHSYNC  
10 XvVSYNC  
10 XvDEN  
10 XvCLK  
10 XvD0  
10 XvD1  
10 XvD2  
10 XvD3  
10 XvD4  
10 XvD5  
10 XvD6  
10 XvD7  
10 XvD8  
10 XvD9  
10 XvD10  
10 XvD11  
10 XvD12  
10 XvD13  
10 XvD14  
10 XvD15  
10 XvD16  
10 XvD17  
10 XvD18  
10 XvD19  
10 XvD20  
10 XvD21  
10 XvD22  
10 XvD23  
10 XadcAIN2/YM0  
10 XadcAIN3/YP0  
10 XadcAIN4/XM0  
10 XadcAIN5/XP0  
10 XadcAIN6/YM1  
10 XadcAIN7/YP1  
10 XadcAIN8/XM1  
10 XadcAIN9/XP1

AA13 XvHSYNC/SYSCS0/VENHSYNC/GPF0\_0  
Y10 XvVSYNC/SYSCS1/VENVSYNC/GPF0\_1  
AB10 XvDEN/SYSRS/VENHREF/GPF0\_2  
AA10 XvCLK/SYSWE/V601CLK/GPF0\_3  
AA9 XvD0/SYSD0/VEND0/GPF0\_4  
AB9 XvD1/SYSD1/VEND1/GPF0\_5  
AB8 XvD2/SYSD2/VEND2/GPF0\_6  
AB7 XvD3/SYSD3/VEND3/GPF0\_7  
Y9 XvD4/SYSD4/VEND4/GPF1\_0  
AB6 XvD5/SYSD5/VEND5/GPF1\_1  
AE7 XvD6/SYSD6/VEND6/GPF1\_2  
AC9 XvD7/SYSD7/VEND7/GPF1\_3  
AA8 XvD8/SYSD8/656D0/GPF1\_4  
W9 XvD9/SYSD9/656D1/GPF1\_5  
AC8 XvD10/SYSD10/656D2/GPF1\_6  
XvD11/SYSD11/656D3/GPF1\_7  
Y8 XvD12/SYSD12/656D4/GPF2\_0  
AC7 XvD13/SYSD13/656D5/GPF2\_1  
AE5 XvD14/SYSD14/656D6/GPF2\_2  
AD7 XvD15/SYSD15/656D7/GPF2\_3  
XvD16/SYSD16/GPF2\_4  
AA7 XvD17/SYSD17/GPF2\_5  
AB6 XvD18/SYSD18/GPF2\_6  
AB5 XvD19/SYSD19/GPF2\_7  
AC5 XvD20/SYSD20/GPF3\_0  
AC6 XvD21/SYSD21/GPF3\_1  
Y7 XvD22/SYSD22/GPF3\_2  
XvD23/SYSD23/V656\_CLK/GPF3\_3  
VSYNC\_LDI/GPF3\_4  
SYS\_OE/VEN\_FIELD/GPF3\_5

[LCDC]  
(VDD\_LCD)

[TouchScreen  
ADC]  
(VDD\_ADC)

[TVOUT  
DAC]  
(VDD\_DAC\_A)

[CAM I/F]  
(VDD\_CAM)

[MIPI-DSI/CSI]  
(VDD\_MIPI\_A)

[DSI]

[CSI]

[HDMI]  
(VDD\_HDMI)

Modem  
Camera B  
CF  
MHL  
Key  
SROM addr[16:22]  
(VDD\_MODEM)

XmsmADDR0/CAM\_B\_D0/CF\_ADDR0/MIPI\_BYTE\_CLK/GPJ0\_0  
XmsmADDR1/CAM\_B\_D1/CF\_ADDR1/MIPI\_ESC\_CLK/GPJ0\_1  
XmsmADDR2/CAM\_B\_D2/CF\_ADDR2/TS\_CLK/GPJ0\_2  
XmsmADDR3/CAM\_B\_D3/CF\_IORDY/TS\_SYNC/GPJ0\_3  
XmsmADDR4/CAM\_B\_D4/CF\_INTRO/TS\_VAL/GPJ0\_4  
XmsmADDR5/CAM\_B\_D5/CF\_DMARQ/TS\_DATA/GPJ0\_5  
XmsmADDR6/CAM\_B\_D6/CF\_DRESETN/TS\_ERROR/GPJ0\_6  
XmsmADDR7/CAM\_B\_D7/CF\_DMACKN/MHL\_D0/GPJ0\_7  
XmsmADDR8/CAM\_B\_PCLK/SROM\_ADDR16/MHL\_D1/GPJ1\_0  
XmsmADDR9/CAM\_B\_VSYNC/SROM\_ADDR17/MHL\_D2/GPJ1\_1  
XmsmADDR10/CAM\_B\_HREF/SROM\_ADDR18/MHL\_D3/GPJ1\_2  
XmsmADDR11/CAM\_B\_FIELD/SROM\_ADDR19/MHL\_D4/GPJ1\_3  
XmsmADDR12/CAM\_B\_CLKOUT/SROM\_ADDR20/MHL\_D5/GPJ1\_4  
XmsmADDR13/KP\_COL\_0/SROM\_ADDR21/MHL\_D6/GPJ1\_5  
XmsmDATA0/KP\_COL\_1/CF\_DATA0/MHL\_D7/GPJ2\_0  
XmsmDATA1/KP\_COL\_2/CF\_DATA1/MHL\_D8/GPJ2\_1  
XmsmDATA2/KP\_COL\_3/CF\_DATA2/MHL\_D9/GPJ2\_2  
XmsmDATA3/KP\_COL\_4/CF\_DATA3/MHL\_D10/GPJ2\_3  
XmsmDATA4/KP\_COL\_5/CF\_DATA4/MHL\_D11/GPJ2\_4  
XmsmDATA5/KP\_COL\_6/CF\_DATA5/MHL\_D12/GPJ2\_5  
XmsmDATA6/KP\_COL\_7/CF\_DATA6/MHL\_D13/GPJ2\_6  
XmsmDATA7/KP\_ROW\_0/CF\_DATA7/MHL\_D14/GPJ2\_7  
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XmsmDATA15/KP\_ROW\_8/CF\_DATA15/MHL\_D22/GPJ3\_7  
XmsmCSnKP\_ROW\_9/CF\_CSn0/MHL\_D23/GPJ4\_0  
XmsmWEnKP\_ROW\_10/CF\_CSn1/MHL\_HSVCN/GPJ4\_1  
XmsmRnKP\_ROW\_11/CF\_IORNI/MHL\_DCK/GPJ4\_2  
XmsmIRQnKP\_ROW\_12/CF\_IOWN/MHL\_VSYNC/GPJ4\_3  
XmsmADVnKP\_ROW\_13/SROM\_ADDR22/MHL\_DE/GPJ4\_4

XmpIMDPCLK  
XmpIMDNCLK  
XmpIMDP0  
XmpIMDN0  
XmpIMDP1  
XmpIMDN1  
XmpIMDP2  
XmpIMDN2  
XmpIMDP3  
XmpIMDN3

XmpISDPCLK  
XmpISDNCLK  
XmpISDP0  
XmpISDN0  
XmpISDP1  
XmpISDN1  
XmpISDP2  
XmpISDN2  
XmpISDN3

XmpiVREG\_OP4V

XhdmITX0P  
XhdmITX0N  
XhdmITX1P  
XhdmITX1N  
XhdmITX2P  
XhdmITX2N  
XhdmITXCP  
XhdmITXCN  
XhdmIREXT

AE15  
AD15  
AE17  
AD17  
AE16  
AD16  
AE14  
AD14  
AE13  
AD13

AD10  
AE10  
AD12  
AE12  
AD11  
AE11  
AD9  
AE9  
AD8  
AE8

AC15

T2  
T1  
U2  
U1  
V2  
V1  
R2  
R1  
W1

H1  
G6  
E4  
H7  
G1  
H2  
D5  
F6  
G2  
F1  
G3  
E5  
F2

F3  
E2  
E1  
D3  
D1  
E3  
D2  
C1  
C2  
D4  
B1  
C3  
C4  
B2  
B3  
A2  
G8  
B4  
G9  
A3  
A4

C12  
1.8nF

R26  
4.7K

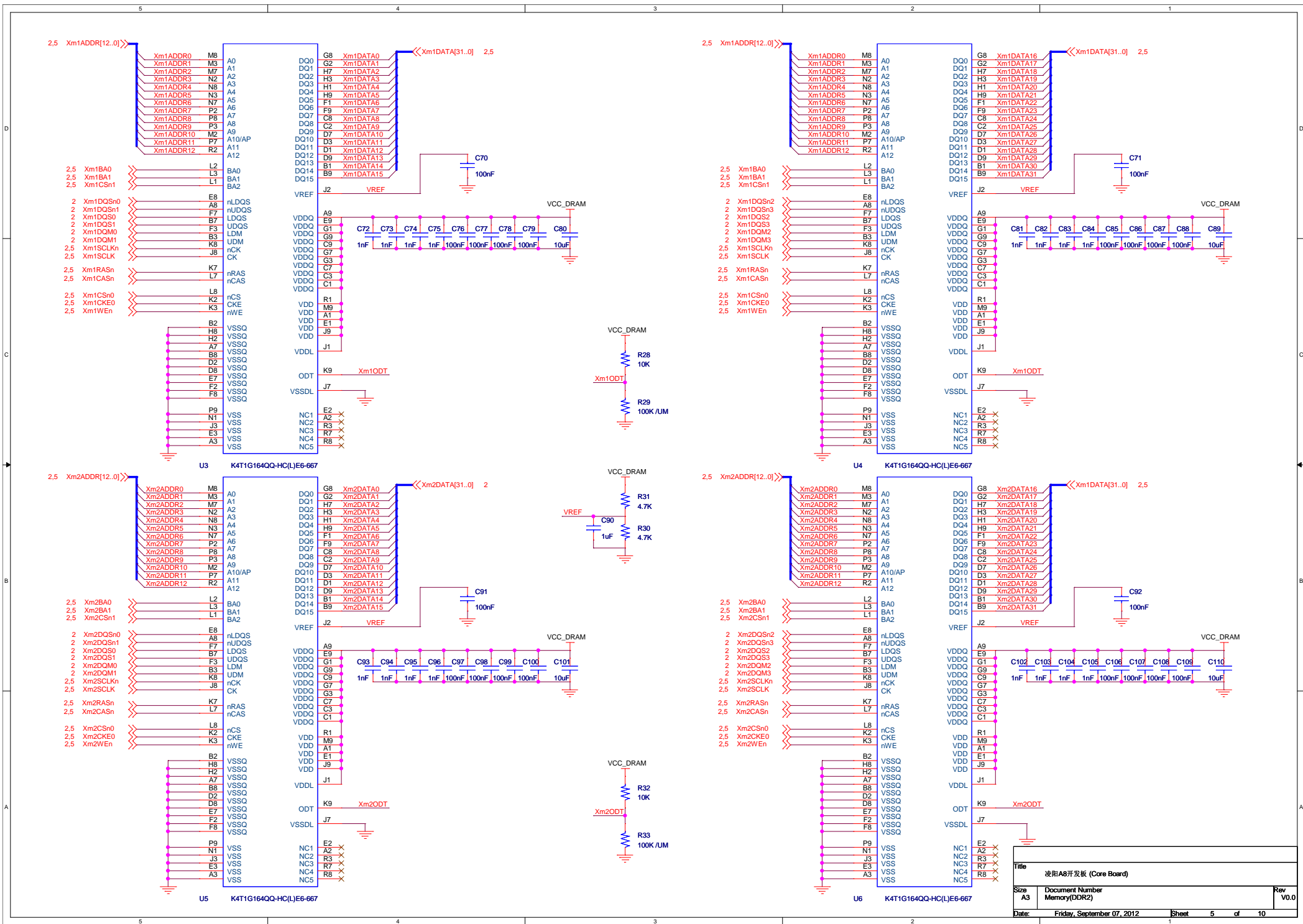
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XmsmADDR4/CAM\_B\_D4/CF\_INTRO/TS\_VAL [20:21]  
XmsmADDR5/CAM\_B\_D5/CF\_DMARQ/TS\_DATA [20:21]  
XmsmADDR6/CAM\_B\_D6/CF\_DRESETN/TS\_ERROR [20:21]  
XmsmADDR7/CAM\_B\_D7/CF\_DMACKN/MHL\_D0 [21]  
XmsmADDR8/CAM\_B\_PCLK/SROM\_ADDR16/MHL\_D1 [21]  
XmsmADDR9/CAM\_B\_VSYNC/SROM\_ADDR17/MHL\_D2 [21]  
XmsmADDR10/CAM\_B\_HREF/SROM\_ADDR18/MHL\_D3 [21]  
XmsmADDR11/CAM\_B\_FIELD/SROM\_ADDR19/MHL\_D4 [21]  
XmsmADDR12/CAM\_B\_CLKOUT/SROM\_ADDR20/MHL\_D5 [21]  
XmsmADDR13/KP\_COL0/SROM\_ADDR21/MHL\_D6 [21]

UTC S5PV210AA0-LA40

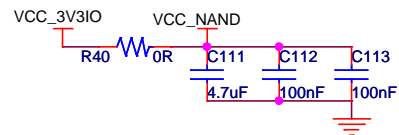
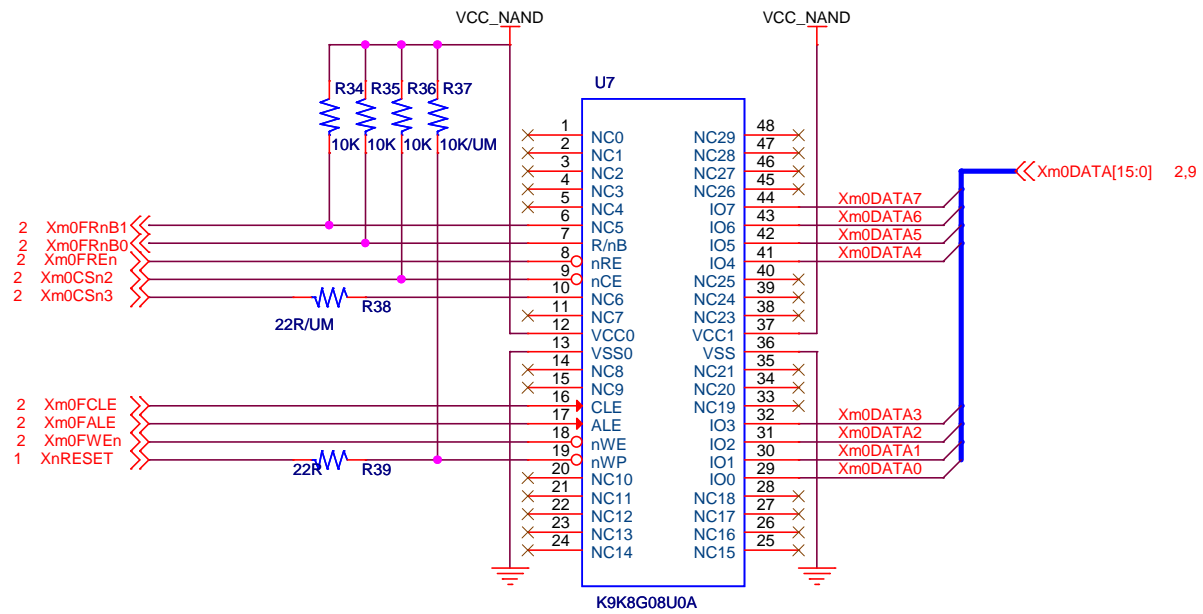
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凌阳A8开发板 (Core Board)		
Size	Document Number	Rev
A3	CPU(Media)	V0.0
Date:	Friday, September 07, 2012	Sheet 3 of 10



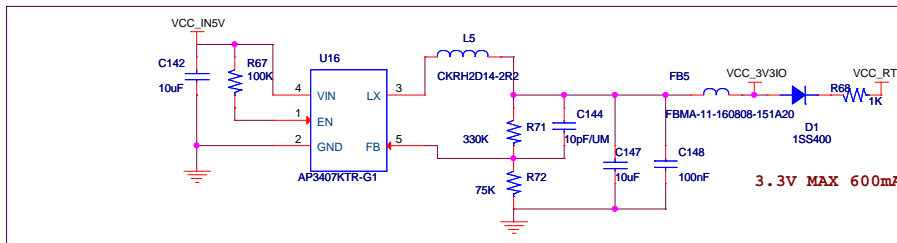
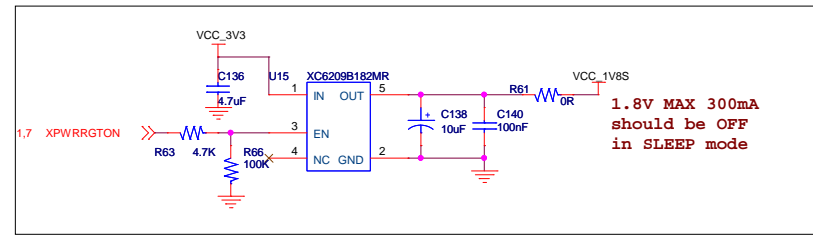
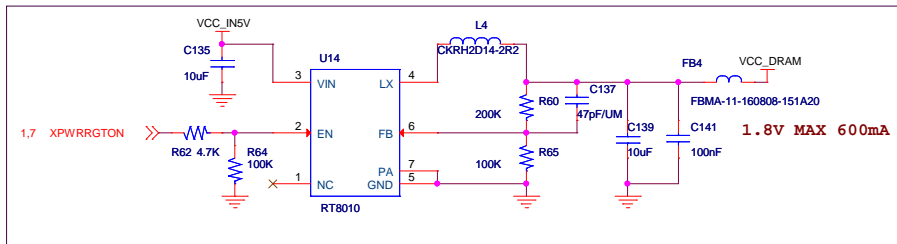
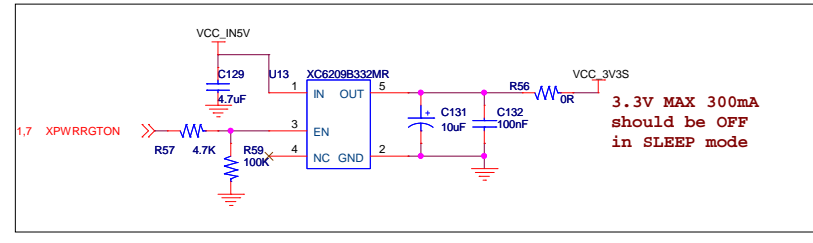
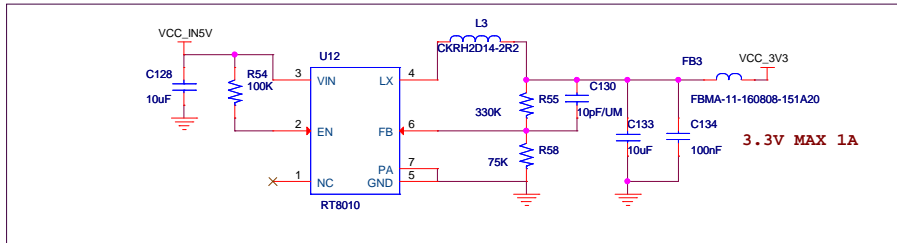
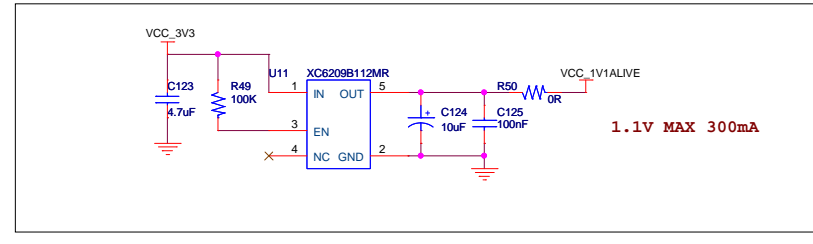
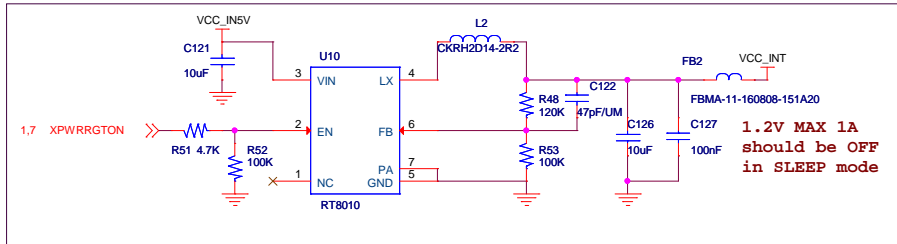
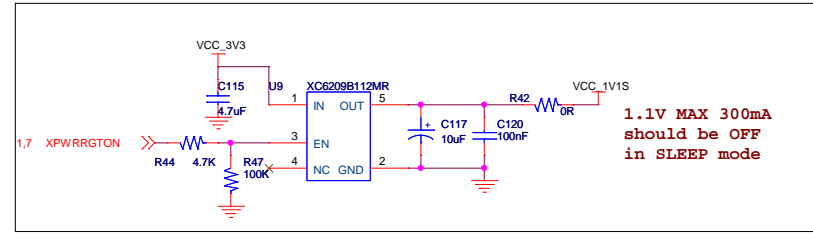
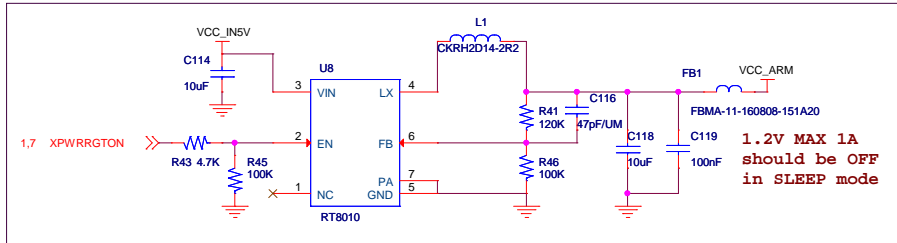
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凌阳A8开发板 (Core Board)				
Size A3	Document Number CPU(Power)			Rev V0.0
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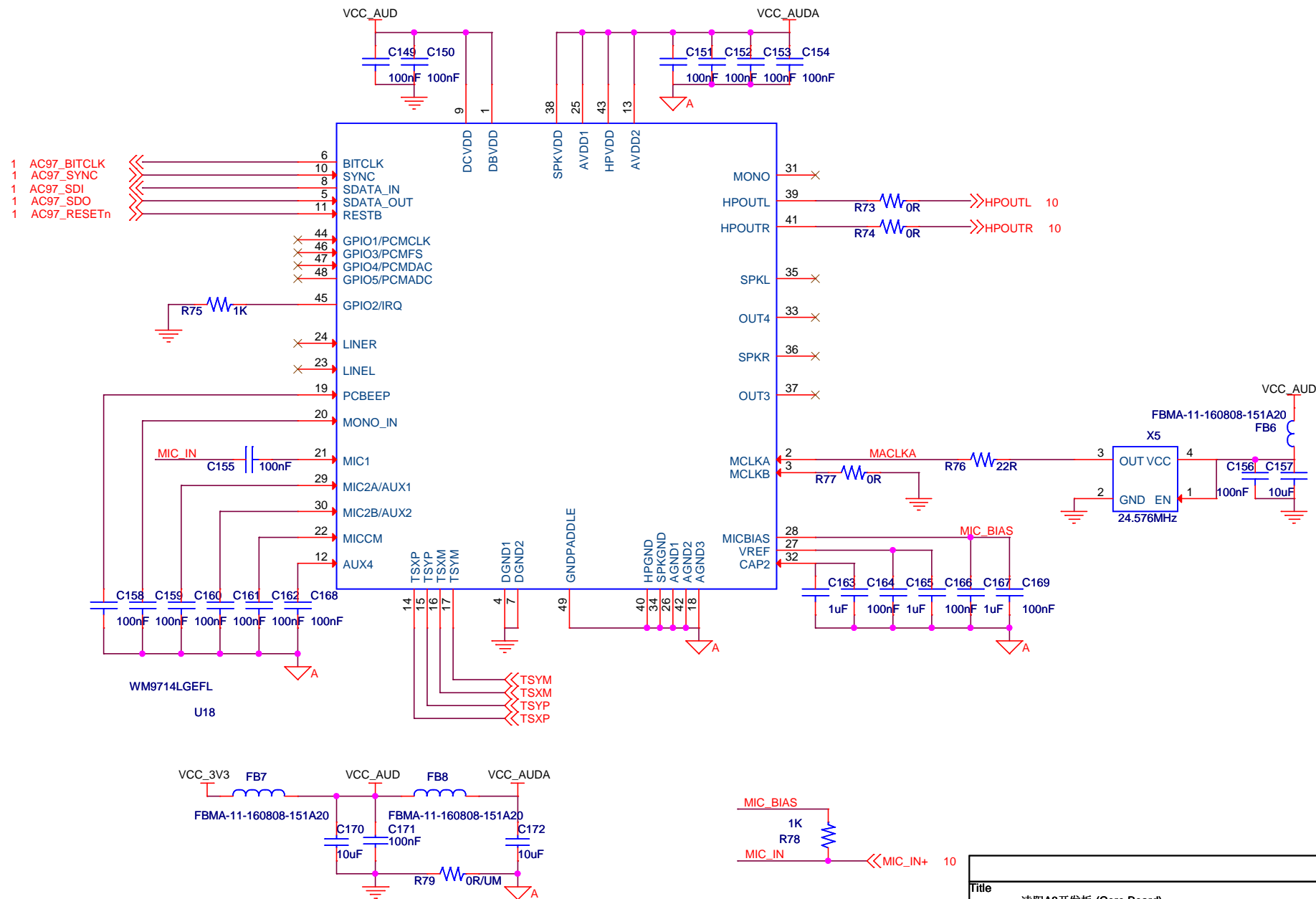
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凌阳A8开发板 (Core Board)			
Size A3	Document Number		Rev V0.0
	Memory(DDR2)		
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Size	Document Number	Rev
A4	NAND(iNAND)	V0.0
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A3	Power	V0.0
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Title		
凌阳A8开发板 (Core Board)		
Size	Document Number	Rev
A4	Audio	V0.0
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