Power Delivery Network Design Training

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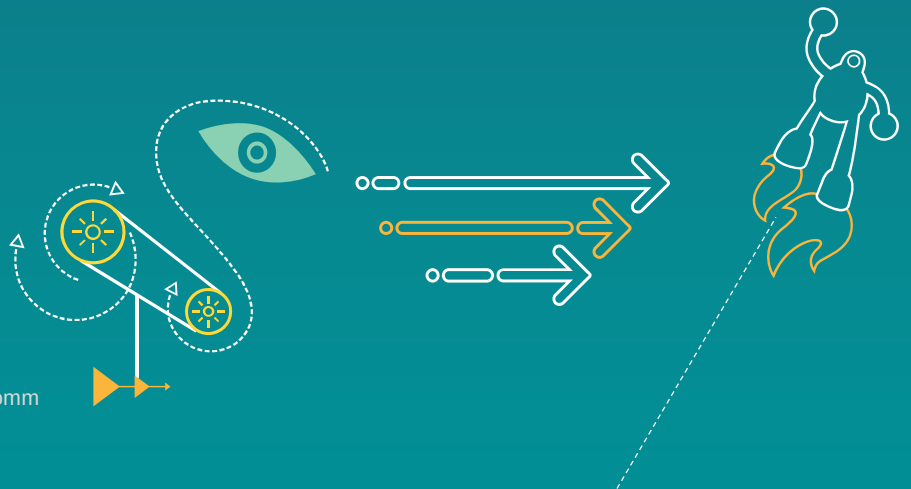

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Revision History (1 of 4)

Revision	Date	Description
A	June 2010	Initial release
B	July 2010	Introduction: Enhanced definition of V_{min} and V_{max}. Explained that, beyond 25 MHz, the PDN is dominated by device package internal RLC circuits. PDN Theory: Added this section. PCB Design Requirements: For frequency range 300 kHz–10 MHz, added the comment that each decoupling cap must have its own via directly to the ground plane. PDN Design Example: Clarified the reference design example as using the QSD8650A™ device. Added an important note about the need for PMIC bulk caps. Clarified the case 5 plots and added an explanation related to the increase/decrease of C/L. FAQ: Rewritten, adding new FAQs. Added more information on simulation.
C	August 2010	Clarified the following FAQs: FAQ – PDN Guidelines; added figures and replaced the “fr” acronym with “ac” FAQ – PDN Measurement Recommendations; added a figure FAQ – Stress Test for Other Power Rails; reworded sentences Added the following new FAQs: FAQ – Mentor Graphics PADS Files FAQ – Precautions for Layout Files FAQ – PCB Stack-up FAQ – Measuring PMIC DC Error

D	September 2010	• Slide 6 – Added new slide, Scope and Intended Audience
		• Slide 8 – Corrected typo in V(t) formula for F^{-1} in the Introduction
		• Slide 14 – PDN Theory – updated figure for clarification
		• Slide 18 – PCB Z(w) Design Guidelines – Removed the recommendation for 2x voltage rating on capacitor selection
		• Slide 22:
		  • Added for PCB to PDN Maximum Impedance Guideline title
		  • Added new device MSM7x27T to PDN Maximum Impedance Guidelines
		• Slide 25 – PDN Design Example – Added a note that all plots are simulations and correlate with actual measured data

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Revision History (2 of 4)

Revision	Date	Description
D (cont.)	September 2010	•Slide 26 – PDN Design Example – Added a note about 10 mohm target PDN impedance guideline for DC •Slide 39 – PDN Design Example, Modification 5, Step 3 – Labeled GND and power layers •FAQ section: •Slide 45 – FAQ – PDN Design Guidelines – Changed terminology Vpm to Vpmdcerror for consistency with other slide and added scale in figure. •Slide 50 – Files Needed for Simulation – Added a note about providing PCB stack-up information •Slides 53 and 54 – Preparation for Layout File – Added examples •Slide 63 – Distance and Heat Concentration – Added note about thermal conductivity •Slides 67 and 68 – Via Routing – Updated figure for clarification •Slide 75 – Measuring PMIC DC Error – Corrected formula in $V_{margin\_h,}$ and removed rework for new configuration requirement •Added the following new FAQ: •Slide 55 – Turn Around Time for Simulations •Slides 56 and 57 – Flow Chart of the Simulation Environment •Slide 78 – Overshoot Impact •Slide 79 – Zero Ohm Resistor
E	April 2012	•Slide 6 – Added AC1 and FAQ sub-sections to Agenda •Slide 7 – Added Terms and Definitions •Slide 17 – PDN Theory – Modified PDN circuit diagram •Slide 25 – PDN Theory– Added Static IR Drop •Slide 26 – PDN Theory – Added PCB Stack-up Considerations •Slide 27 – PDN Theory – Added Capacitor Placements •Slide 28 – PDN Theory – Added Decoupling Capacitor Routing Scenarios •Slide 50 – AC1 Stress Test – Added title slide •Slide 51 – AC1 Stress Test – Added Introduction and Recommended lab setup information •Slide 52 – AC1 Stress Test – Added Probe Setup •Slide 53 – AC1 Stress Test – Added Typical AC1 Waveform •Slide 54 – AC1 Stress Test – Added Terms and Definitions •Slide 55 – AC1 Stress Test – Added Terms and Definitions (cont.) •Slide 56 – AC1 Stress Test – Added Margin Calculations •Slide 57 – FAQ General – Added title slide •Slide 58 – FAQ General – Added PDN Targets

Revision History (3 of 4)

Revision	Date	Description
E (cont.)	April 2012	•Slide 60 – FAQ General – Modified PDN Guidelines (cont.) •Slide 62 – FAQ General – Modified VRM Models, Transient Simulations •Slide 73 – FAQ Simulation – Added new title •Slide 77 – FAQ Simulation – Added additional files to be provided from Rev B. •Slide 86 – FAQ Simulation – Added PMIC Models •Slide 87 – FAQ Simulation – Added Package/Die Models •Slide 88 – FAQ Simulation – Added Port Definition •Slide 89 – FAQ Simulation – Added Resistance Measurement •Slide 90 – FAQ Simulation – Added Current Measuring Resistor •Slide 91 – FAQ Simulation – Added Time Domain Simulation •Slide 92 – FAQ Simulation – Added Chip Power Model •Slide 93 – FAQ Simulation – Added Transient Simulation •Slide 94 – FAQ AC1 Stress Test – Added new title •Slide 95 – FAQ AC1 Stress Test – Added Stress Tests for Other Power Rails •Slide 96 – FAQ Impedance Measurement – Added new title •Slide 97 – FAQ Impedance Measurement – Added Simulation vs. Lab Measurement Correlation
F	October 2014	• Clarified throughout the document that PDN simulations must be done as soon as parts placement and PDN routing is finished. Also changed “targets” to “specifications” throughout the document • Clarified throughout the document that the regulator in the PDN system can be SMPS or LDO • Removed obsolete references to QSD from the document • Slide 8 – Terms and Definitions: Modified the definition of bulk capacitors and local decoupling capacitors • Slide 11 – Introduction: Clarified the introduction • Slide 19 – Key Concept – Loop Inductance: Added a slide to explain loop inductance and identify the key items for reducing it • Slide 23-26 – PCB Z(ω) Design Guidelines: Modified the explanations on the graphs • Slide 53 – Stress Test: Clarified the use of AC1 and added that customers should also run their own high concurrency tests at temperature extremes • Slide 55 – Stress Test Probe Setup: Added arrows indicating where to solder the shield and center conductor of the semi-rigid coaxial shield • Slides 66 – General – PDN Specifications: Modified answers for frequently answered questions • Slides 67-68 – General – Failure to Meet PDN Specifications: Added slides to frequently answered questions

Revision History (3 of 4)

Revision	Date	Description
F (cont.)	October 2014	•Slide 73 – General – Via Routing: Modified the figure to show both power and ground routing. •Slide 74 – General – PCB Area and BOM Count: Modified the answers •Slide 75 – General – Placement Distance between PMIC and the Processor: Clarified that thermal considerations take priority when determining the distance from the PMIC to the MSM •Slide 81 – General – Simulation Tools: Modified the answers •Slide 89 – General – Flowchart of Simulation Procedures: Modified the flowchart and deleted the second page •Slide 90 – General – PMIC Models: Modified the answer about the PMIC VRM model •Slide 92 – General – Port Definition: Modified the answer to include distributed ports

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Contents

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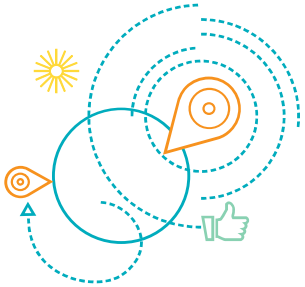

Terms and Definitions

Term	Definition
Processor	Qualcomm Technologies, Inc. (QTI) ICs – MSM™, APQ, MPQ, and MDM
Bulk capacitors	Capacitors to smooth PMIC output response, normally by ≥ 4.7 µF
Local decoupling capacitors	Capacitors closest to the processor. These capacitors improve processor response to transient current demand, normally by ≤ 1 µF

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Section 1

Introduction

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Scope and Intended Audience

This document is intended for engineers who are designing with QTI devices that operate with clock frequencies of approximately 800 MHz and higher. This document contains important information about how to design the power delivery network (PDN) to minimize impedance over the frequency range of interest. Proper PDN design prevents violations of V_{min} or V_{max} during voltage transients that occur under normal operating conditions.

What is included in the PDN?

- Voltage regulators residing in the power management IC (PMIC)
  - Switched mode power supply (SMPS)
  - Low-dropout regulator (LDO)
- Regulator output inductor (SMPS only) + bulk capacitor(s)
- All passive components and their connections to the processor power grid
- Copper traces connecting the regulator output to the processor power pins
- Copper plane connecting processor ground pins to regulator ground pins

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Introduction (1 of 2)

A properly designed PDN helps ensure supply voltage compliance to the required operating conditions of processors and other integrated circuitry.

Proper PDN design ensures that $V_{min} \leq V(t) \leq V_{max}$ during all di/dt events.

- V(t) is the voltage measured at the processor power pins as a function of time.
- V_{min} is the minimum voltage allowed (DC + transient) at the processor power supply pins to guarantee proper operation over all variations of process and temperature as listed in the device specification.
- V_{max} is the maximum voltage allowed (DC + transient) at the processor power supply pins to guarantee proper operation over all variations of process and temperature as listed in the device specification.

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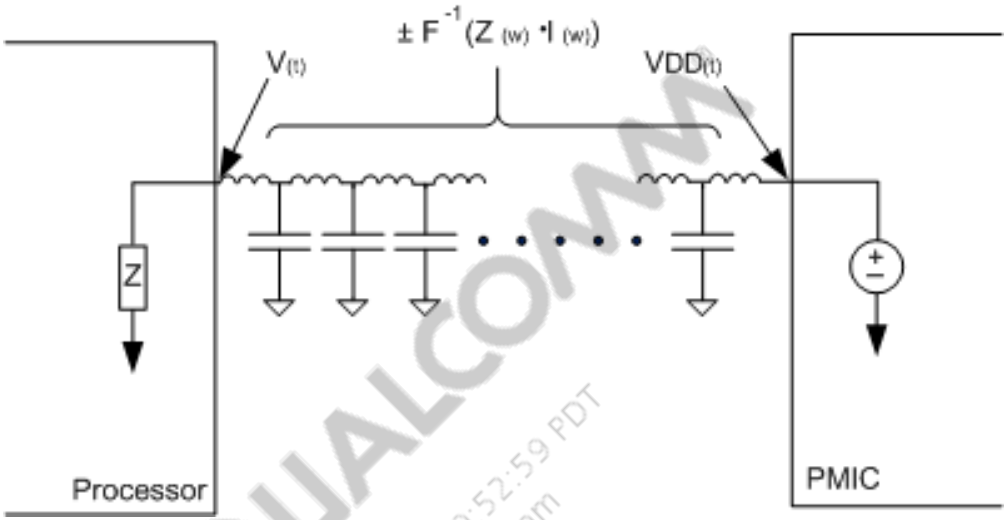
Introduction (2 of 2)



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- Key formula: $V(t) = VDD(t) \pm F^{-1}\{Z(\omega)I(\omega)\}$
  - VDD (t) is the instantaneous voltage at the PMIC output.
  - I(w) is the load current as a function of frequency.
  - Z(w) is the impedance of the PDN determined from the load (processor power supply pins), back toward the PMIC and is dominated by:
    - PCB metal power planes (DC to ~3 kHz)
    - PMIC regulator response and external bulk capacitors (~3 kHz to ~300 kHz)
    - PCB metal planes and local decoupling capacitor values (~300 kHz to ~10 MHz)
    - Local decoupling capacitor connections to processor power supply pins and distance between power and ground planes (~10 MHz onwards)

Section 2

PDN Theory

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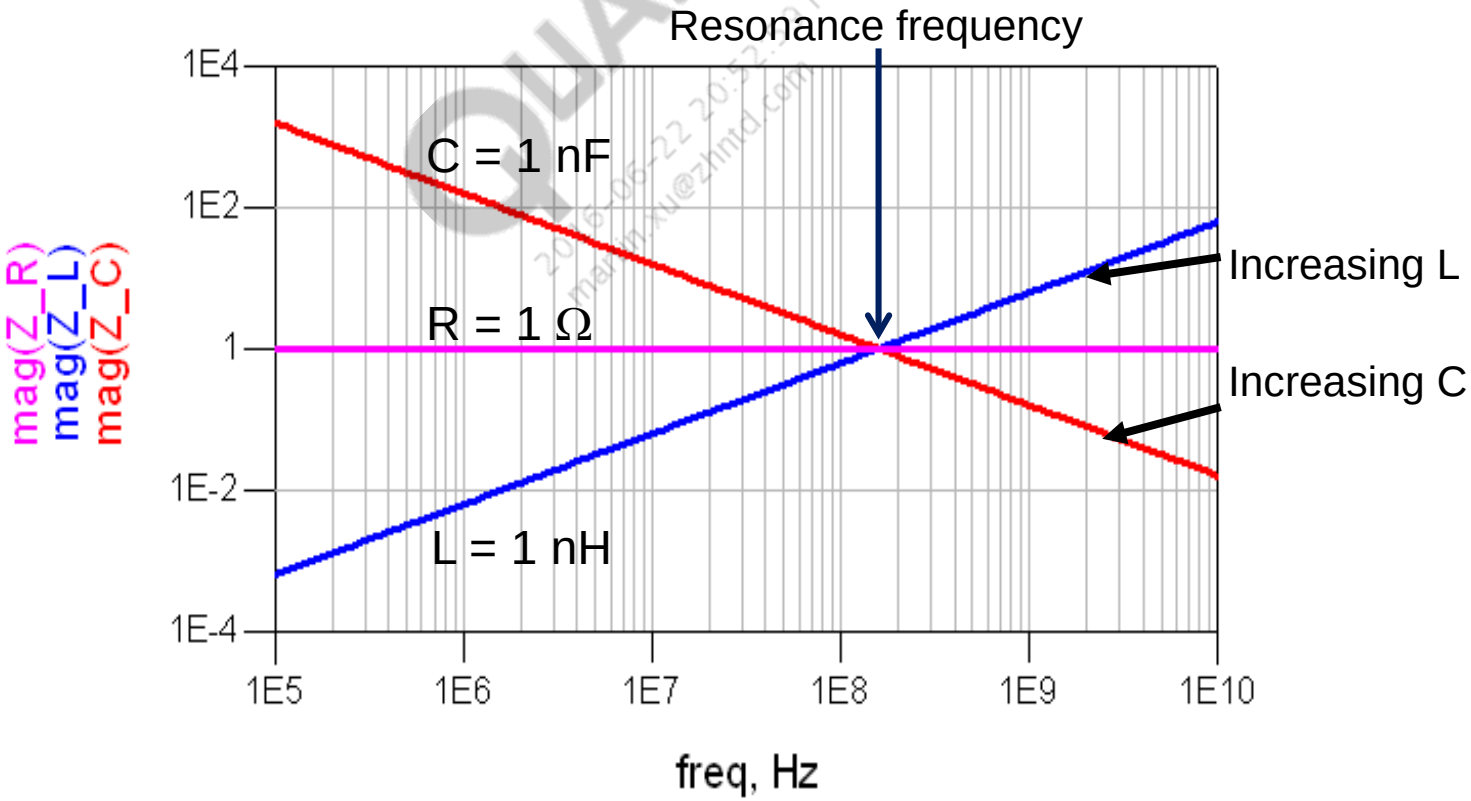
Z(f): R, L, C

Impedance: Resistor Z = R

Inductor Z = jωL

Capacitor Z = 1/(jωC)

On a log/log scale, these impedances graph as lines of constant slope vs ω.



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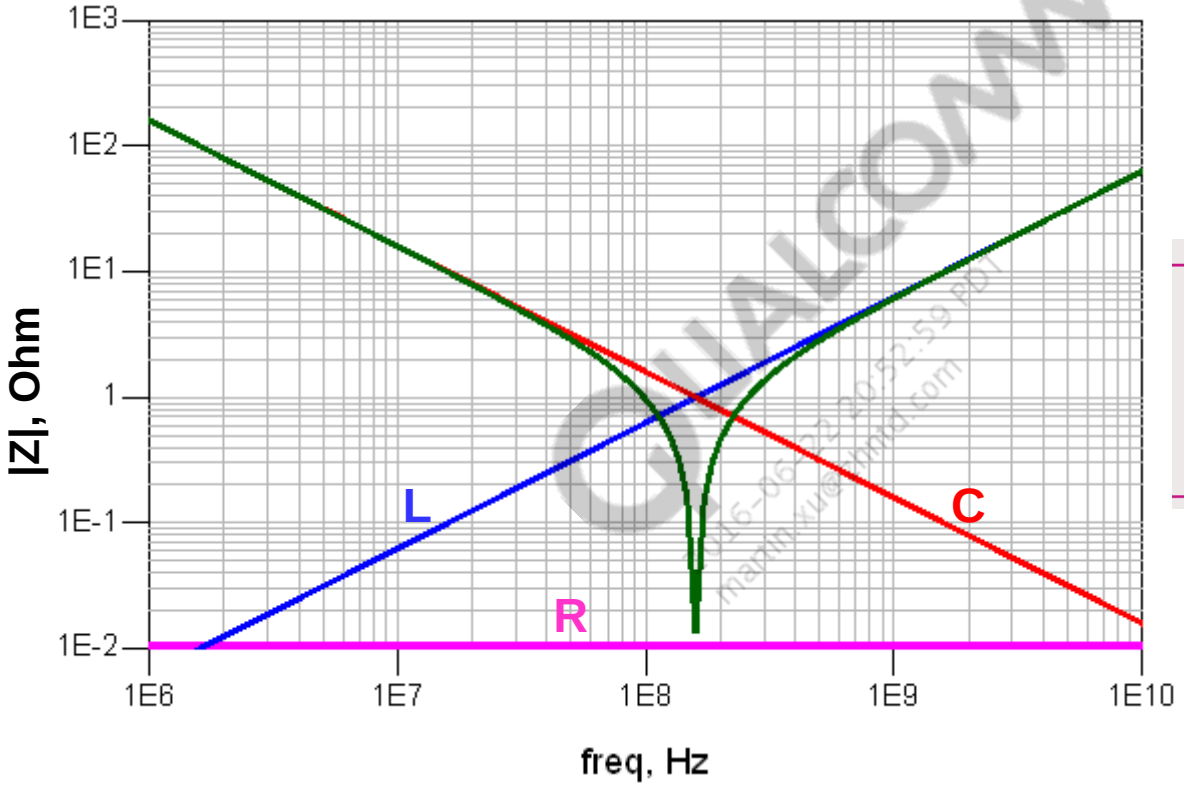
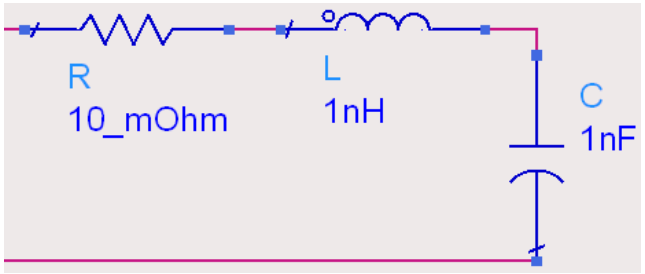
Series RLC Resonance





$$f_0 = \frac{1}{2\pi\sqrt{LC}}$$

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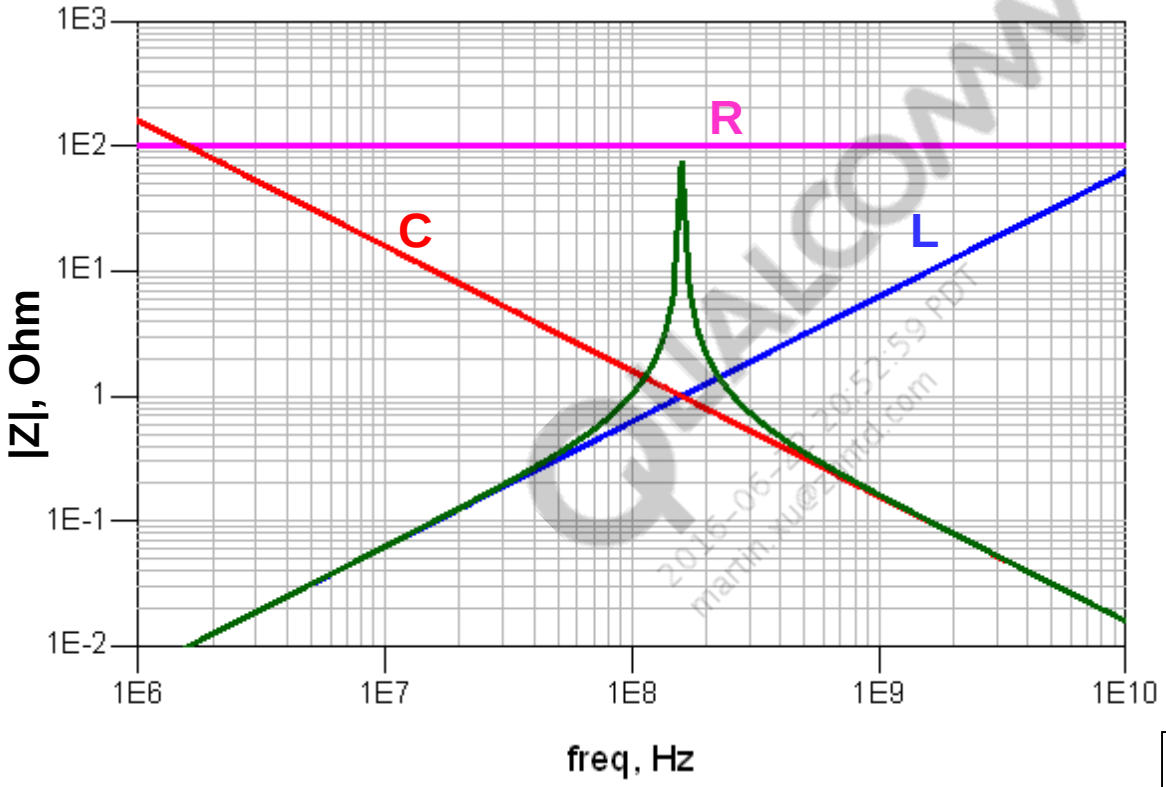
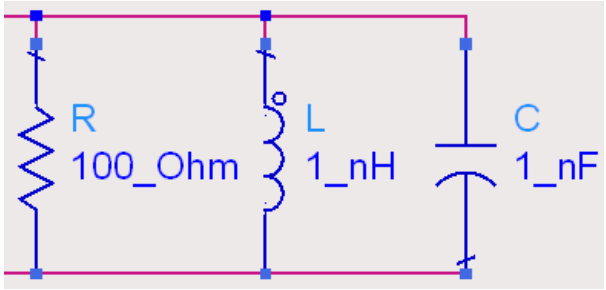
Parallel RLC Resonance





$$f_0 = \frac{1}{2\pi\sqrt{LC}}$$

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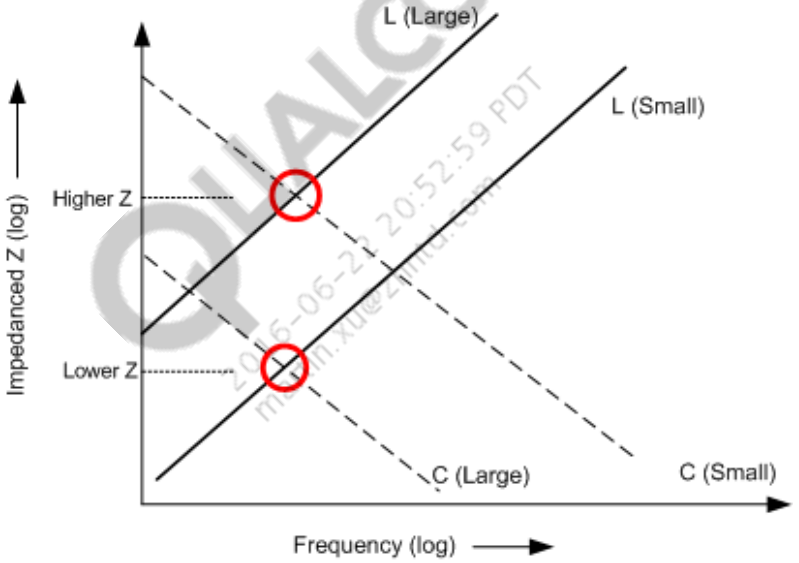
PDN Theory (1 of 5)

The PDN impedance (Z) is modeled by combinations of capacitance, inductance, and resistance.

- Inductor: Z = jωL
- Capacitor: Z = 1/(jωC)
- Resistor: Z = R



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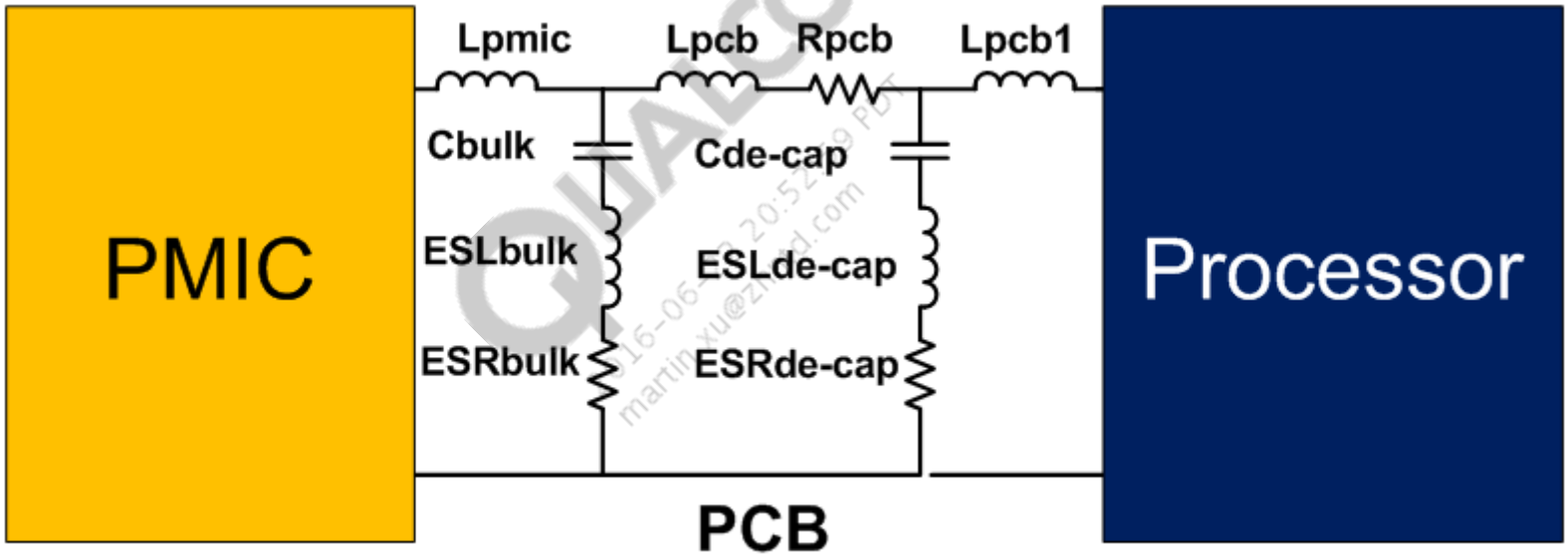
- Combinations of larger inductance and smaller capacitance result in a higher impedance.
- Combinations of smaller inductance and larger capacitance result in a lower impedance.

PDN Theory (2 of 5)



Note: This is a simplified PDN model.

PDN Theory (3 of 5)

Key Concept – Loop Inductance

The amount of *loop inductance* associated with the PDN routing on a PCB is primarily determined by:

- The physical dimensions of the current carrying conductors (power net) and the closeness of the return path (ground net).
- The physical dimensions and placement of the passive components connected to the PDN (primarily decoupling capacitors and possibly resistors).

Loop inductance is directly proportional to the area encompassed by a power net and its return path. *A large area implies a large loop inductance*.

Therefore, key steps to reducing loop inductance are:

- **Reducing the lengths (x) of both power and ground nets.**
- **Reducing the vertical distance (y) between power and ground (return) nets.**
  - See the *Stack-up Considerations* slide.
- **Routing multiple current loops in parallel. Ltotal = L1 × L2/(L1 + L2). This is because the parallel loops can support more current for the same voltage drop.**
  - **Wider power and ground (return) traces with broadside (over-under) coupling effectively provide more loops in parallel to reduce inductance.**
- **Optimally placing and connecting decoupling capacitors. This reduces *effective* loop area because the capacitors electrically close the parallel inductive branch loops; good placement + connection = smaller loops in parallel.**
  - See the *Capacitor Placements* slide.

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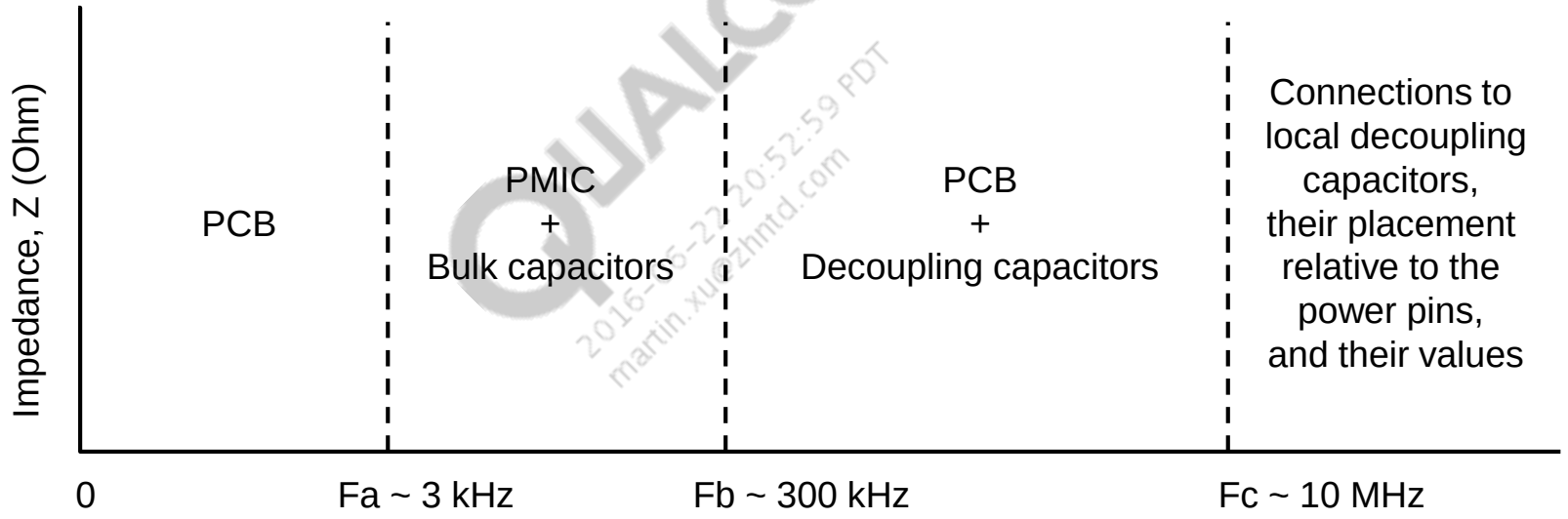
PDN Theory (4 of 5)

At higher frequencies (not shown in figure), the PDN impedance is a function of package RLC and board loop inductance.



Note: The exact frequencies Fa, Fb, and Fc depend on the PMIC regulator used, bulk capacitors, inductor (SMPS only), board impedance, decoupling capacitors, etc.

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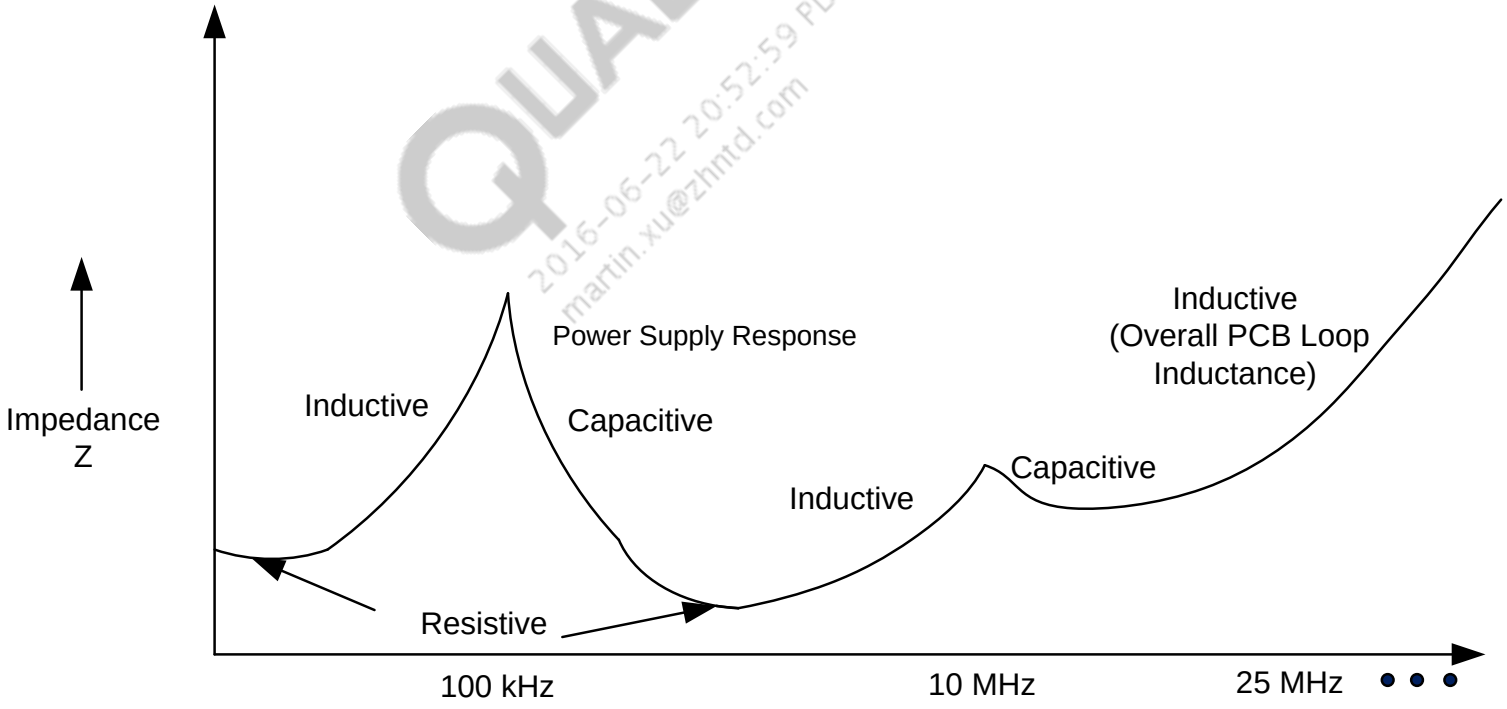
PDN Theory (5 of 5)

The PDN response in a given frequency range can be resistive, capacitive, or inductive. It is composed of both series and parallel resonances as shown below.



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Section 2.1

PCB Z(ω) Design Guidelines

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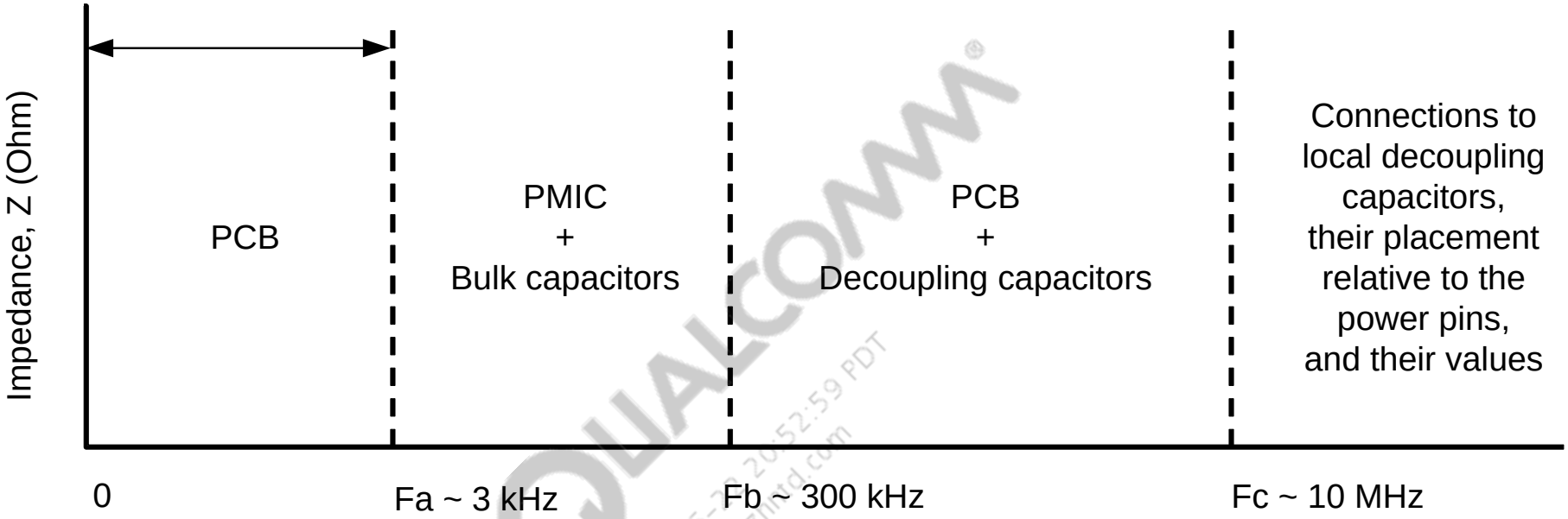
PCB Z(ω) Design Guidelines (1 of 4)



- DC–3 kHz → PCB metal routing to meet the DC resistance specification
  - First, address thermal design requirements relative to the placement of the PMIC and processor
  - Maximize metal thickness (½ vs. ⅓ oz. Cu)
  - Use sufficiently wide power traces
  - Use multiple parallel power and ground vias

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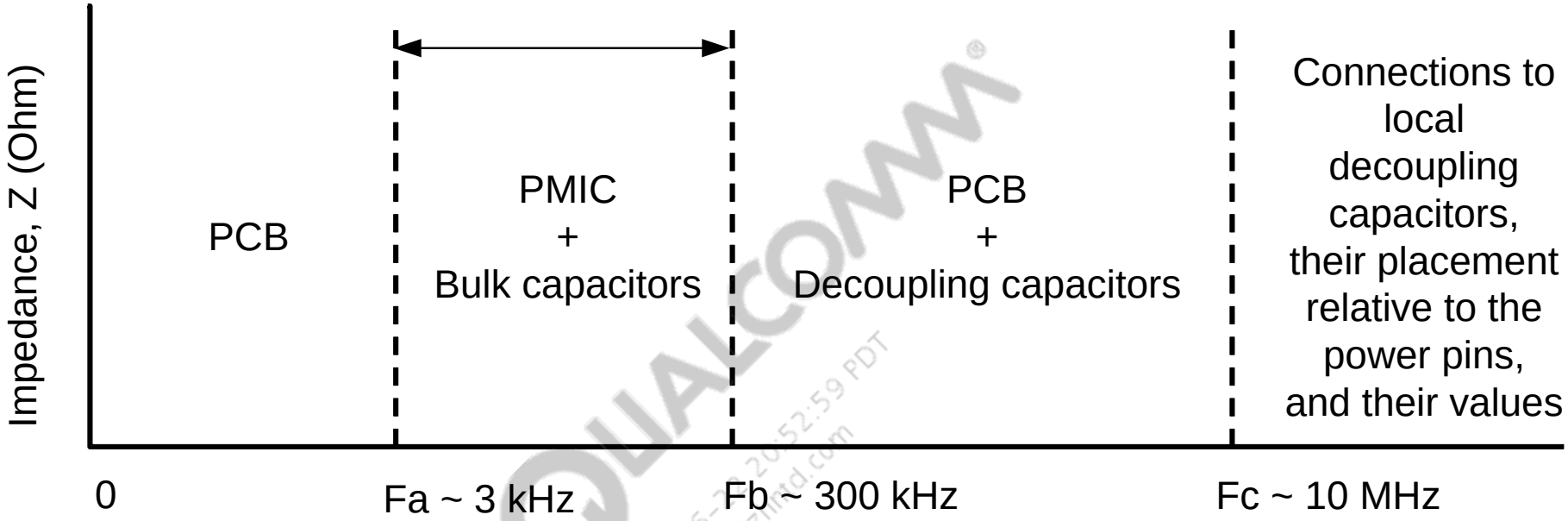
PCB Z(ω) Design Guidelines (2 of 4)



- 3 kHz–300 kHz → PMIC regulator response and bulk capacitors
  - Use QTI-supplied PMIC settings and reference schematic values
  - Follow QTI design guidelines for optimal placement of the bulk capacitors
  - Maximize metal thickness (½ vs. ⅓ oz. Cu); use wider power traces
  - Use multiple parallel power and ground vias

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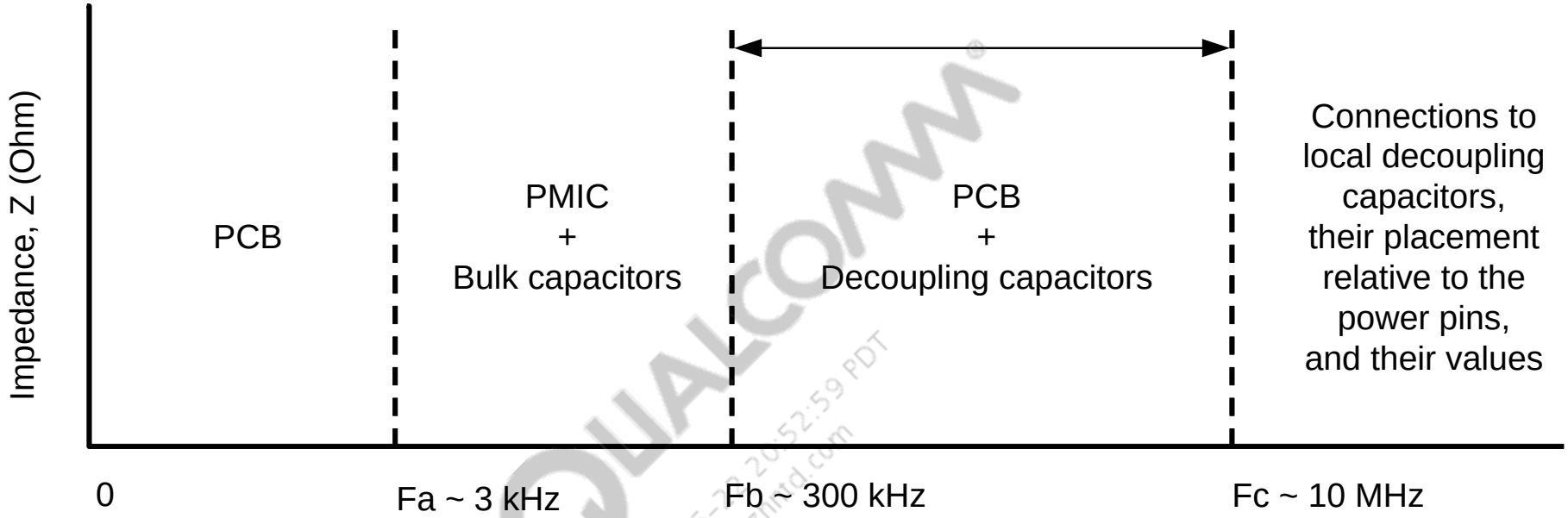
PCB Z(ω) Design Guidelines (3 of 4)



- 300 kHz–10 MHz → PCB layout and decoupling capacitors
  - Engineer capacitor values, body sizes, and placement to meet impedance specification

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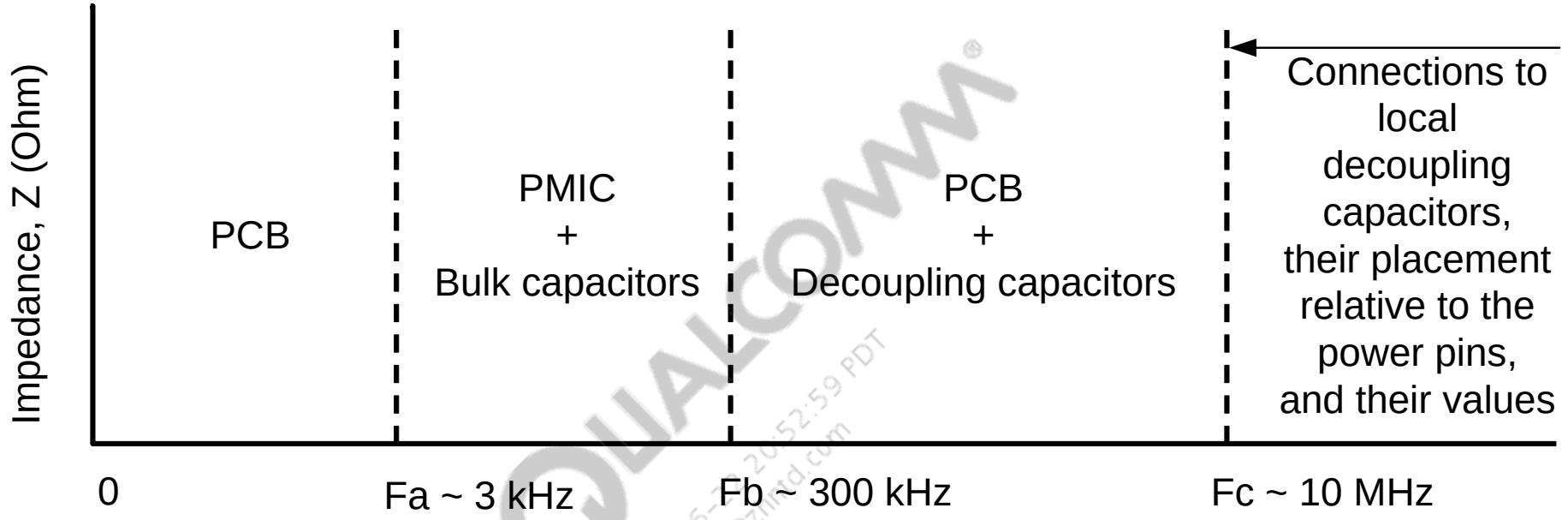
PCB Z(ω) Design Guidelines (4 of 4)



- 10 MHz onwards → Capacitors and PCB connection
  - Current always takes the path of least impedance. At these high frequencies, PDN loop inductance, value, and placement of capacitors attached to power pins dominates impedance.
  - Local decoupling capacitors should be placed as close as possible to the processor power and ground pins. Use back-side capacitors if possible. Each capacitor should have its own via directly to the ground plane and power plane layer.
  - Power and ground vias and planes should be as close together as possible.
- See the Stack-up Considerations and Capacitor Placements slides.

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PCB Z(ω) Design Guidelines – Static DC IR Drop

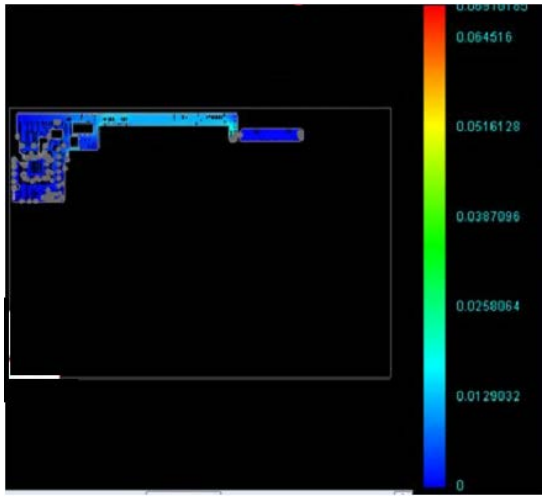
Calculate the resistance of power trace between PMIC and MSM using:

- R = ρ (L/A) where
- ρ = Resistivity of copper
- L = Length of trace
- A = Cross-section area = Width of trace × thickness of trace

Calculate the minimum number of vias required to carry the current. Always use more vias than the minimum required.

- Minimum vias ≥ Total current/Current carrying capacity of each via
- Copper paste filled vias are used in certain PCBs. Copper paste is electrically and thermally less conductive than copper. More vias are required when using copper paste vias.

Static IR drop analysis shows current densities at different locations in the layout.



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PCB Z(ω) Design Guidelines – Stack-up Considerations

Power and ground should be located on adjacent layers separated by as thin a dielectric as possible to reduce loop inductance.

No	Layer	Thickness (µm)	Scenario I	Scenario II
1	Cu	25		
	Dielectric	50		
2	Cu	20		
	Dielectric	50		
3	Cu	20	Gnd	Signal
	Dielectric	65		
4	Cu	20	Signal	Gnd
	Dielectric	65		
5	Cu	17	Pwr	Pwr
	CORE	100		
6	Cu	17	Gnd	Signal
	Dielectric	65		
7	Cu	20	Signal	Gnd
	Dielectric	65		
8	Cu	20		
	Dielectric	50		
9	Cu	20		
	Dielectric	50		
10	Cu	25		

Better (Dielectric is thinner)

Worse (Dielectric is thicker)

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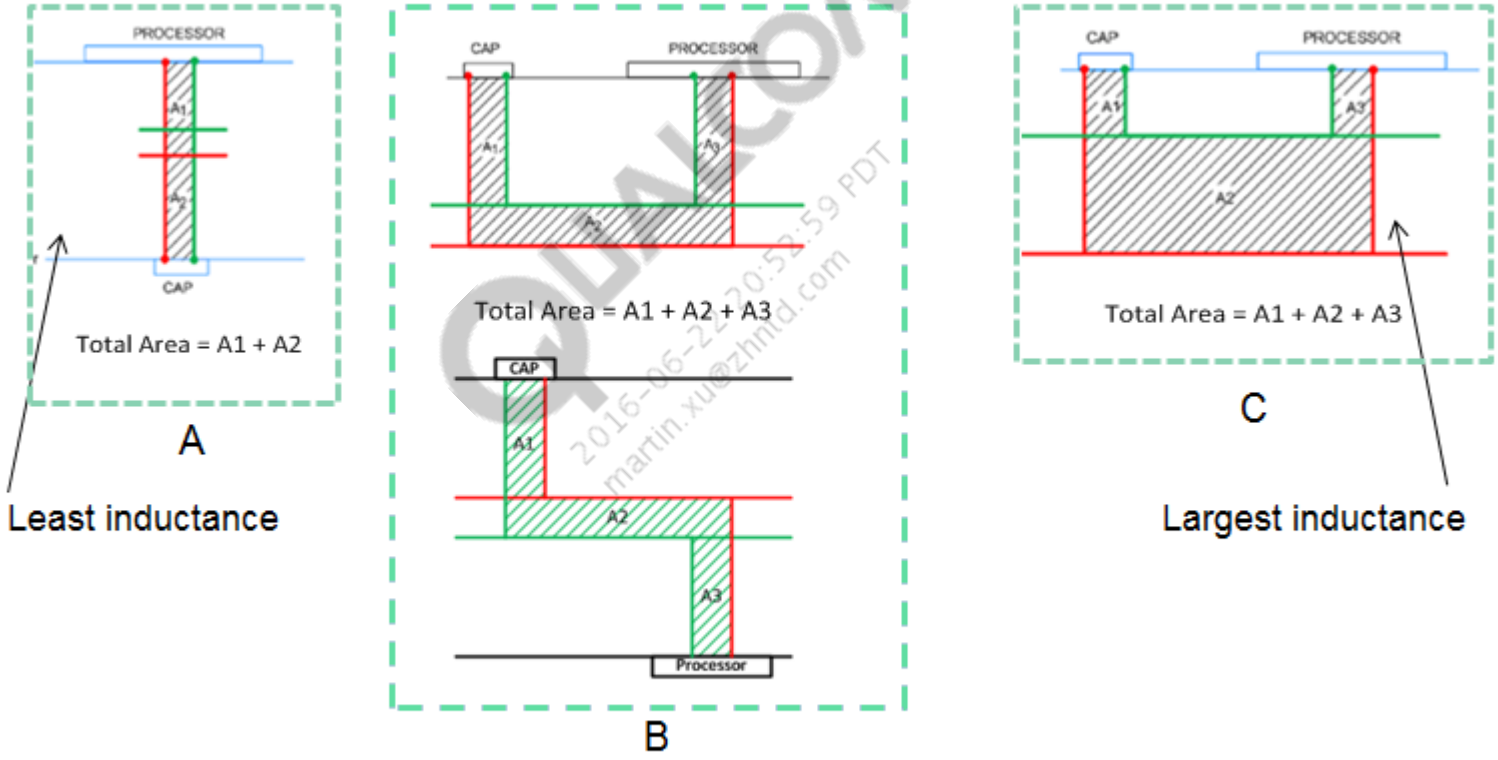
PCB Z(ω) Design Guidelines – Capacitor Placements

Lower power-ground loop area reduces loop inductance thereby improving the effectiveness of a capacitor at high frequencies.

Local decoupling capacitors must be placed as close to the MSM pins as possible.



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Note: Geometries are not to scale.

PCB Z(ω) Design Guidelines – Decoupling Capacitor Routing

Capacitor effective loop inductance is geometry based.

- Body size influences self-inductance; capacitors with smaller body sizes have lower ESL.
- Locate power-ground vias as close to each other as possible; small loops have lower inductance.
- Locate vias close to the capacitor terminals; small loops have lower inductance.
- Multiple parallel power-ground via pair connections reduce mounting inductance; parallel loops have lower inductance.
- Avoid sharing vias with adjacent capacitors; parallel loops have lower inductance, series loops have higher inductance.
- Three-terminal capacitors such as X2Y devices can offer lower inductance than two-terminal devices.
  - With good layout the three-terminal devices are connected with small loops and parallel loops.
  - The multiple terminal design also provides small loops and parallel loops inside the device for lower ESL.

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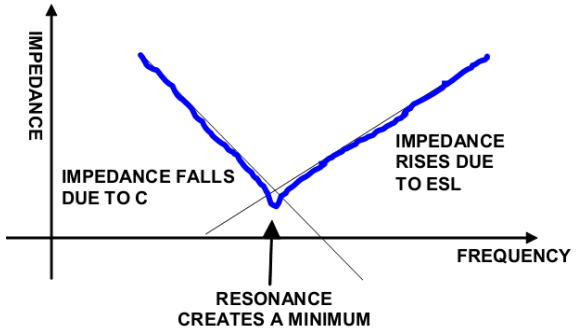
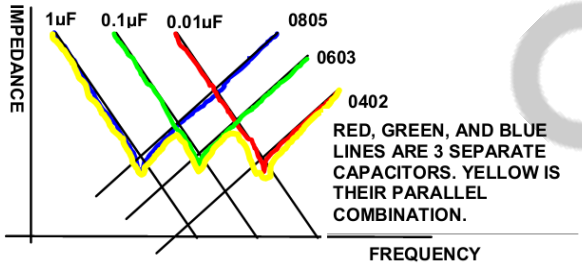
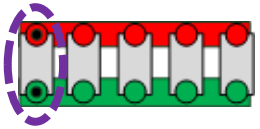
PCB Z(ω) Design Guidelines – Decoupling Capacitors Response and Routing

Typical Capacitor Response





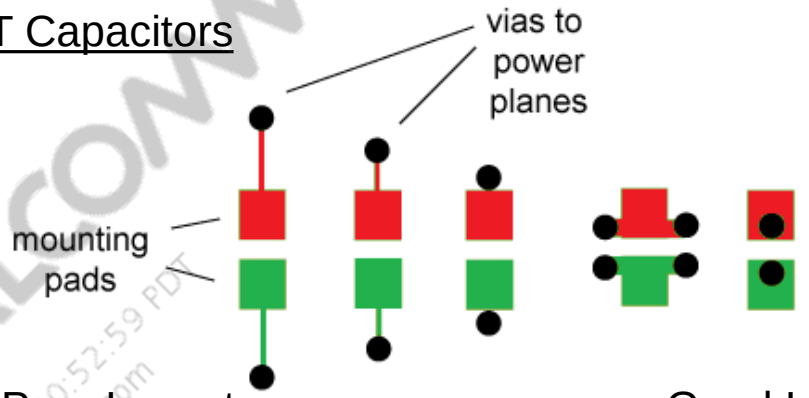
Avoid sharing vias



Bad

Good

2-T Capacitors

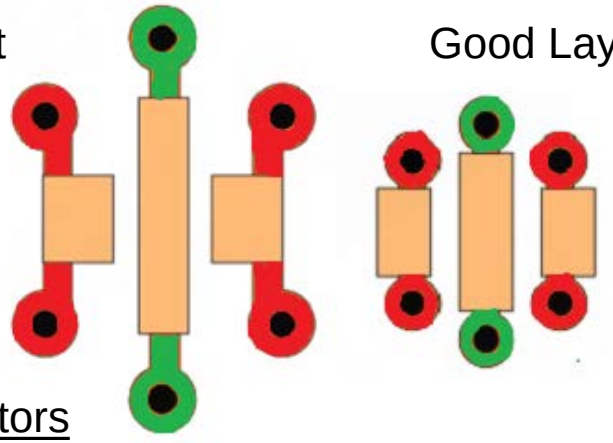


Poor Layout — Good Layout

Decreasing inductance

3-T X2Y Capacitors

Poor Layout — Good Layout



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Section 3

PDN Design Example – Simulation

Steps to Reduce the PDN Impedance of the PCB

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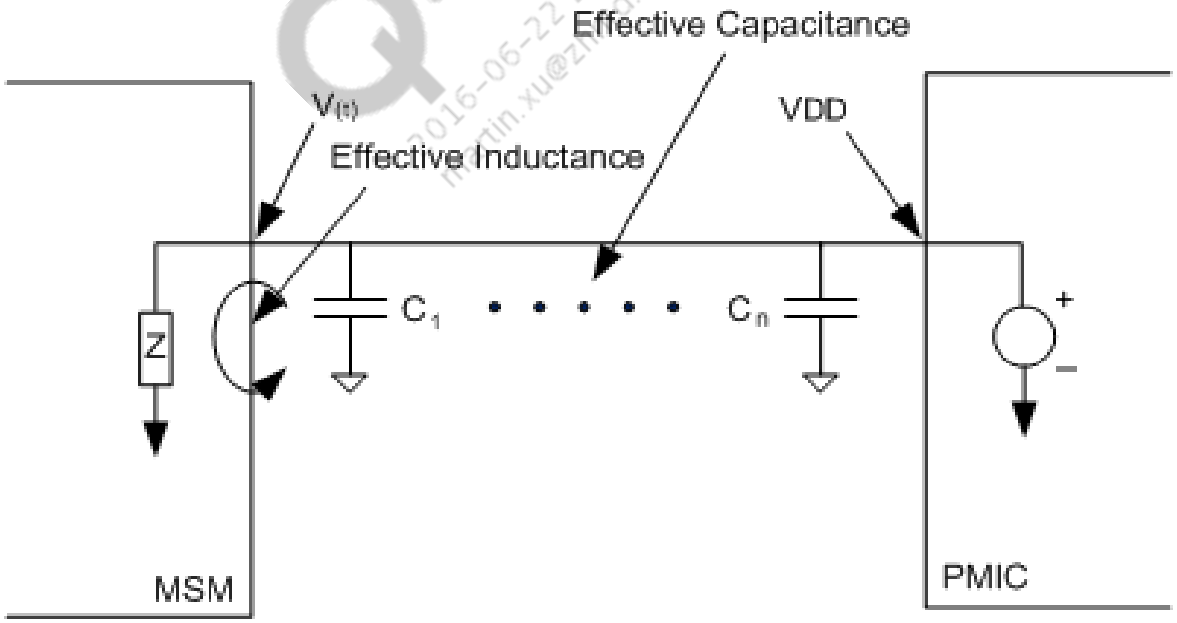
PDN Design Example (1 of 2)

The following definitions are used throughout this design example:

- Effective capacitance: The total shunt capacitance over the PDN between the source and the load
- Effective inductance: The loop inductance from the processor power pins to the closest “local” bypass capacitors



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PDN Design Example (2 of 2)

This PDN impedance reduction example uses the QSD8650A device.

Note: All impedance graphs shown in the following slides are simulated results that correlate accurately to measured results.

- Bulk capacitor (at the PMIC output) (modification case 1)
- Wide traces/copper fill (modification case 2 and case 3)
- Local decoupling capacitors (at the MSM input)
  - Placement (minimize the distance to the processor power supply pins) (modification case 4, step 1 and case 5, step 1)
  - Value (modification case 5, step 2)
- Layer thickness (modification case 5, step 3)
- Distance between PMIC and the processor power supply pins (General – Via Routing)
- Distance between power and ground planes (General – PCB Area and BOM Count)
- Via (General – Trace Width)

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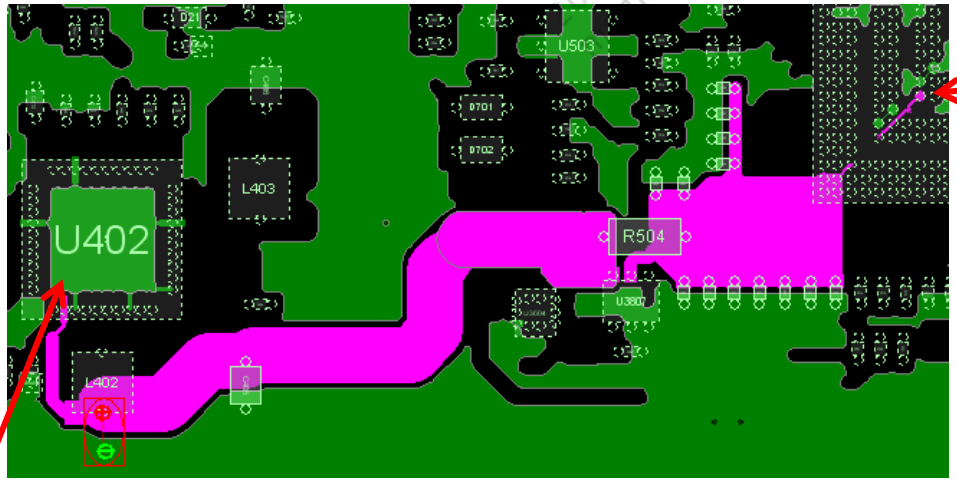
Original Layout/Conditions

- DC resistance (by PowerDC):
- Power path:
  - From MSM/QSD to R504: 1 mΩ
  - R504: 4 mΩ
  - From R504 to L402: 6.5 mΩ (11.5 mΩ total)
- Ground path:
  - From U201 to GND node near L402: 1.7 mΩ
- Total is 11.5 mΩ + 1.7 mΩ = 13.2 mΩ – This does not meet the 10 mΩ specification at DC.



Port 1 – Processor

Port 2 – PMIC (L402)

Capacitance	2.2 µF	1 µF	22 µF
Quantity	9	4	1

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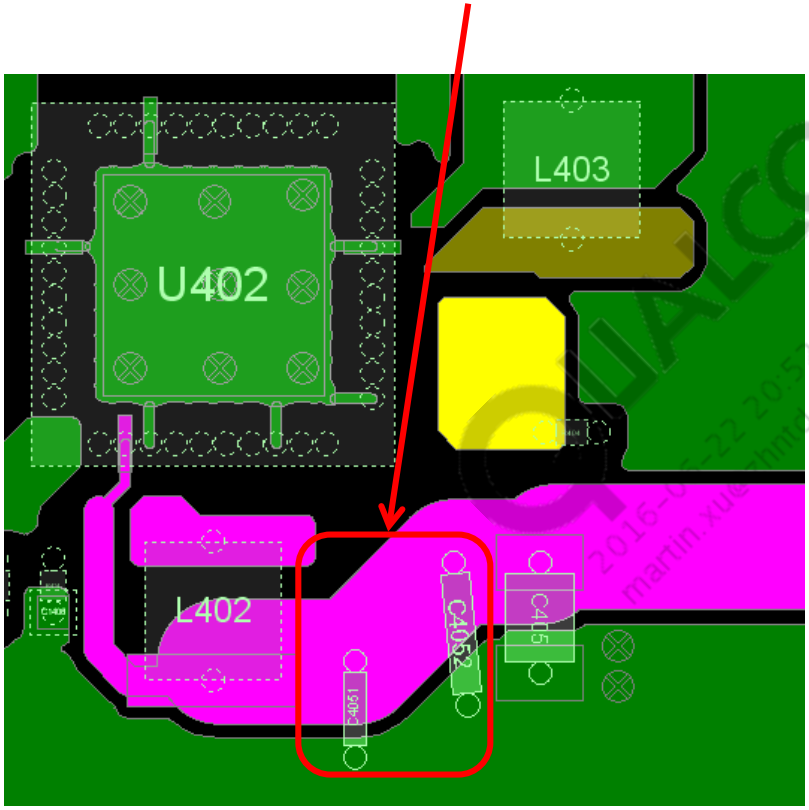
Modification – Case 1

Add more bulk capacitors at the PMIC side to improve the low-frequency response.



Capacitance	Original	Case 1
2.2 µF	9	9
1 µF	4	4
22 µF	1	1
47 µF	–	2
Total	14	16

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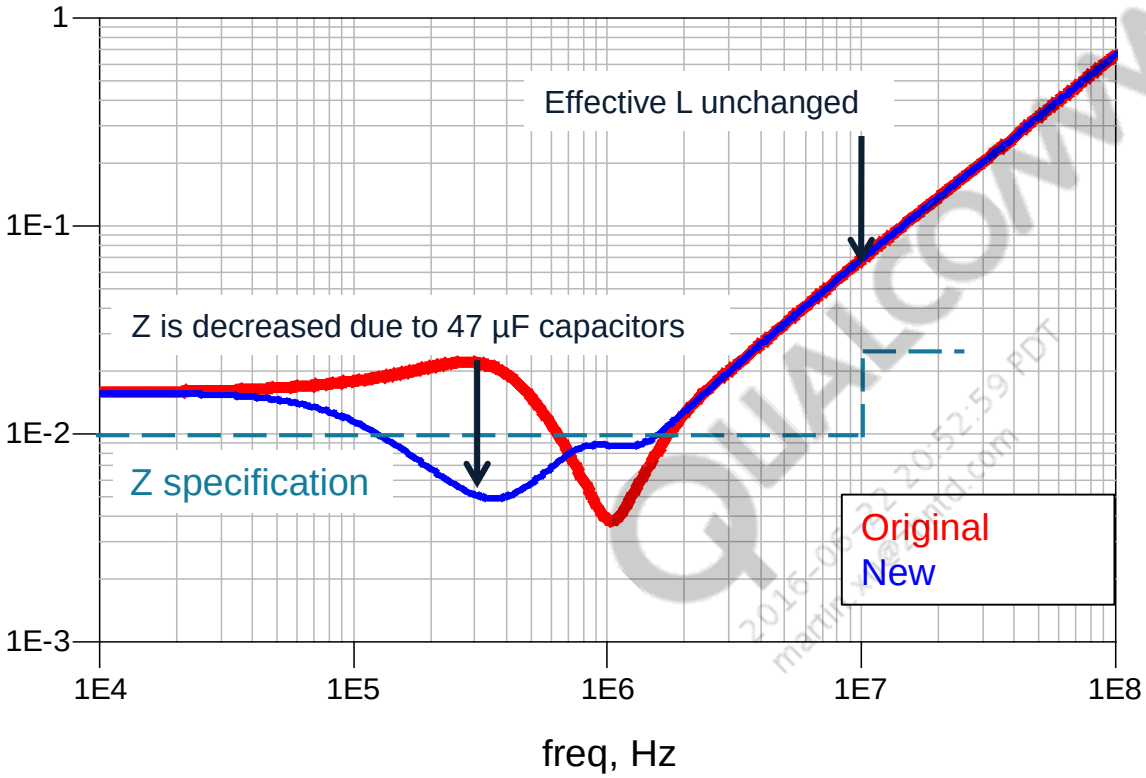
Change in PDN Impedance – Case 1



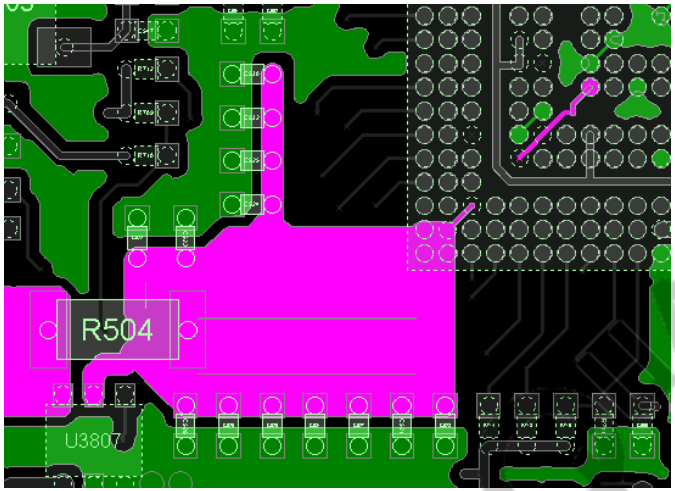
PMIC = ideal voltage source

	Effective C	Effective L
Original	45.3 µF	1.05 nH
New	137.2 µF	1.05 nH

Observation: Large bulk capacitors improve PDN impedance as shown, but even more important is their role in reducing PMIC effective impedance below 100 kHz (not shown in these simulations). Follow the PMIC data sheet and reference schematic for proper values (i.e., the QSD8250A PMIC only recommends a 22 µF maximum bulk capacitor).

Modification – Case 2

- Replace the 2.2 µF capacitors with 4.7 µF with no change to routing.



Capacitance	Original	New
2.2 µF	9	–
1 µF	4	–
4.7 µF	–	9
0.47 µF	–	4
22 µF	1	1
47 µF	–	–
Total	14	14

- No layout/capacitor placement changes
- Replaced only the 2.2 µF capacitor with 4.7 µF capacitors and replaced the 1 µF capacitors with 0.47 µF capacitors

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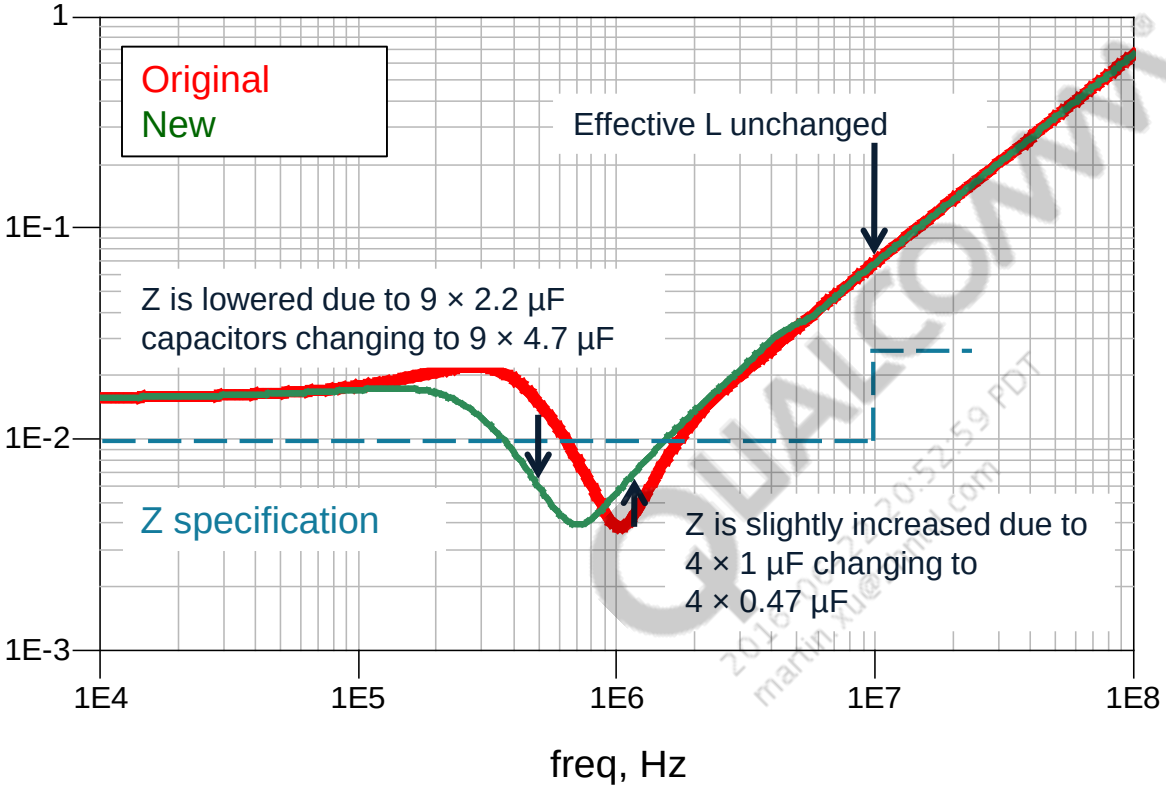
Change in PDN Impedance – Case 2



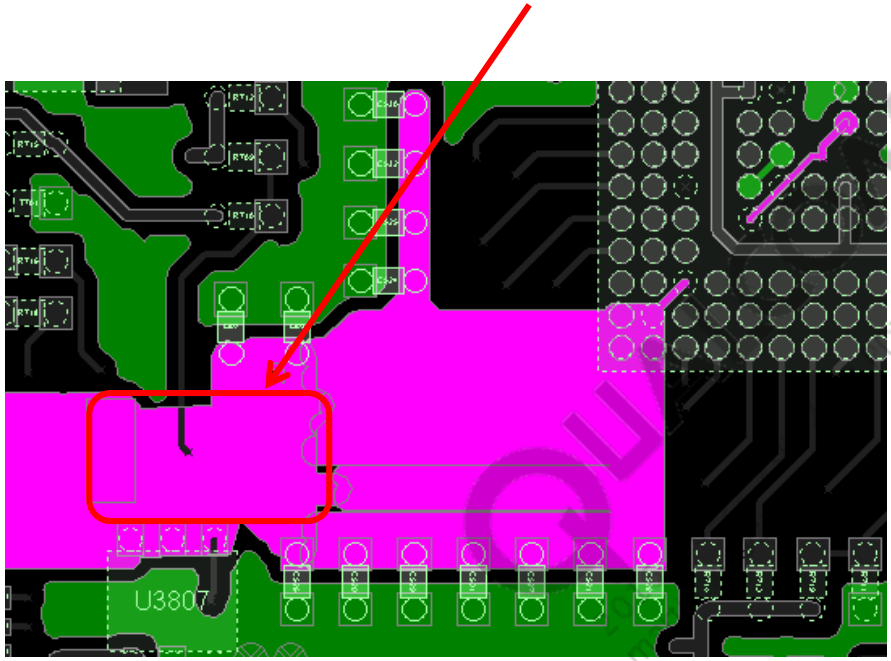
PMIC = ideal voltage source

	Effective C	Effective L
Original	45.3 µF	1.05 nH
New	66.3 µF	1.05 nH

Observation: Increasing the value of local capacitors without changing the PDN routing did not help reduce the effective inductance. Effective inductance is dominated by the current path from the chip pins to the local decoupling capacitors, not the capacitor values themselves.

Modification – Case 3

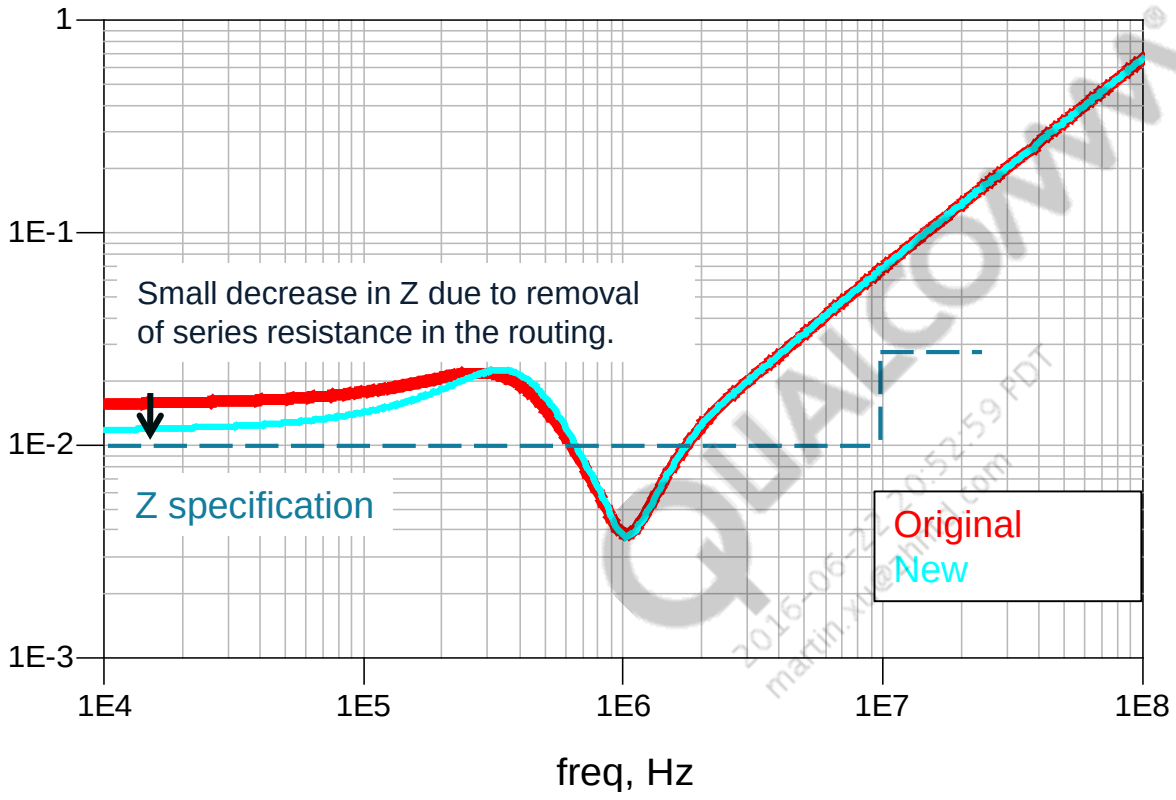
Take out the current measurement resistor and fill in the shape.



Capacitance	Original	New
2.2 µF	9	9
1 µF	4	4
22 µF	1	1
Total	14	14

- No changes in the bypass capacitor arrangements

Change in PDN Impedance – Case 3



PMIC = ideal voltage source

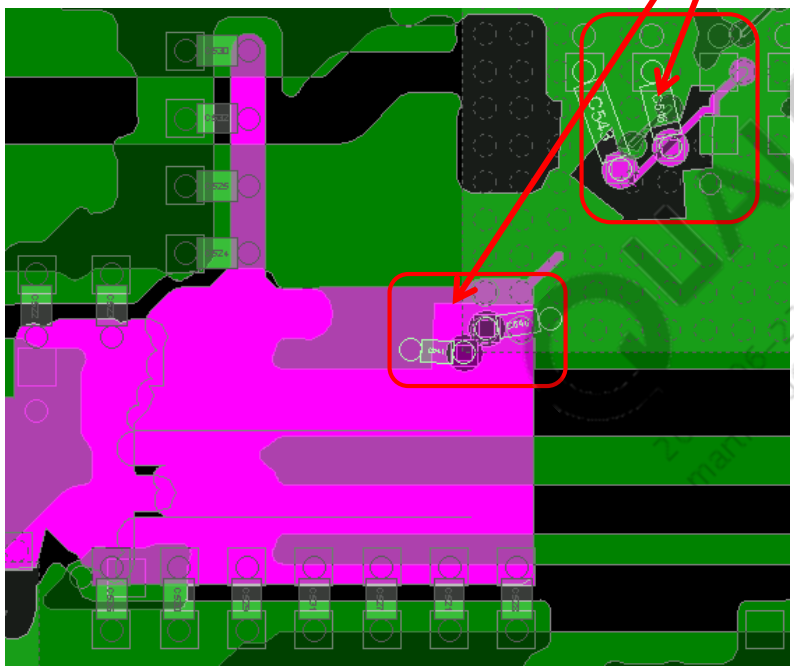
	Effective C	Effective L
Original	45.3 µF	1.05 nH
New	45.3 µF	1.05 nH

Observation: Removing the series R showed a 4 mΩ improvement in low-frequency impedance from the MSM chip to the PMIC (see Original Layout/Conditions).

Modification – Case 4

Add four back-side bypass capacitors.

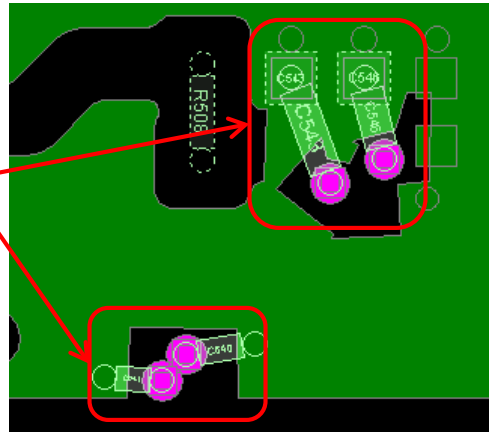
Top and bottom layer



Capacitance	Original	New
2.2 µF	9	13
1 µF	4	4
22 µF	1	1
Total	**14**	**18**

Bottom layer only

Four extra 2.2 µF capacitors were added on the opposite side from the chip.



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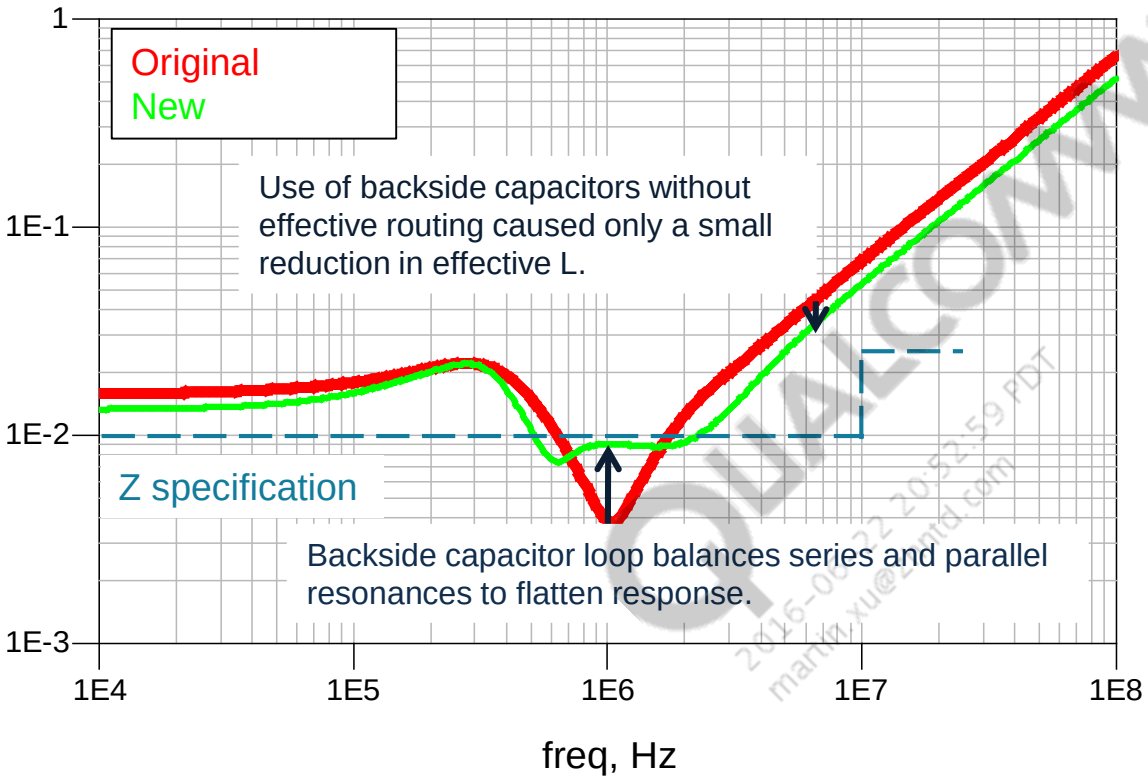
Change in PDN Impedance – Case 4



PMIC = ideal voltage source

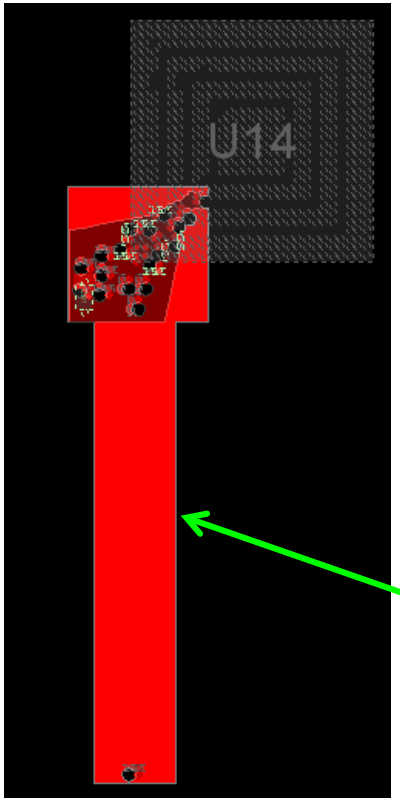
	Effective C	Effective L
Original	45.3 µF	1.05 nH
New	54.7 µF	0.83 nH

Observation: Adding back-side capacitors without optimizing the capacitor routing only marginally reduced the PDN inductance. The next case shows that re-engineering the routing of those capacitors was key.

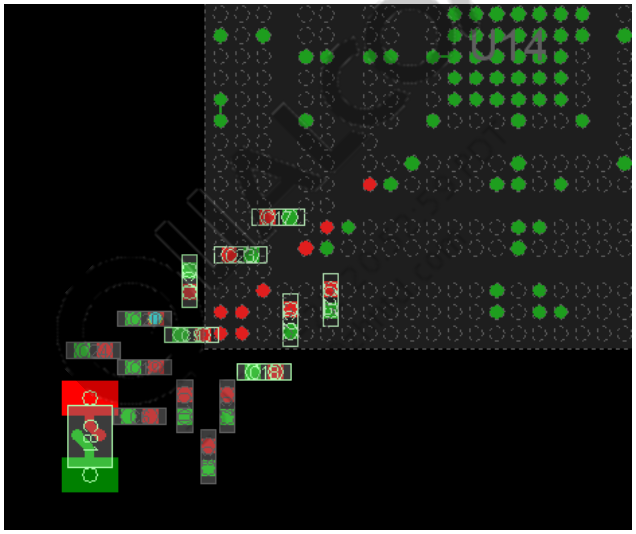
Modification – Case 5 Step 1

Use back-side capacitors and reduce the size of other capacitors to place them as close to the processor power pins as possible.

Power routing (all layer view)



Local decoupling capacitor placement (top/bottom layers)



Capacitance	Original	New
0.47 µF (same side)	–	7
0.47 µF (back side)	–	7
2.2 µF	9	–
1 µF	4	–
22 µF	1	1
Total	14	15

Reduced overall DC resistance from U14 (MSM) to PMIC by decreasing length and widening the PDN trace

Power: 6.3 mΩ; GND: 3.5 mΩ
Total loop: **9.8 mΩ vs. 13.2 mΩ original (26% reduction)**

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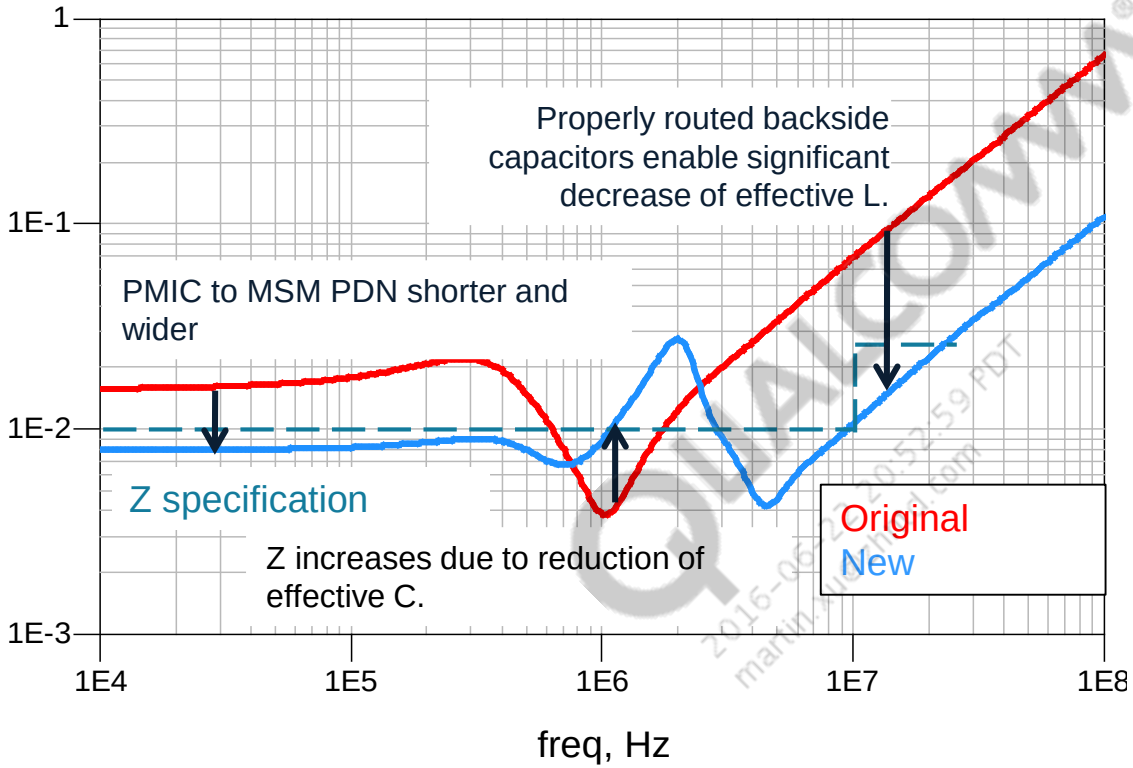
Change in PDN Impedance – Case 5 Step 1



PMIC = ideal voltage source

	Effective C	Effective L
Original	45.3 µF	1.05 nH
Step 1	29.0 µF	0.17 nH

Observation: With an improved breakout strategy and re-engineering of the via patterns, the PDN impedance is significantly reduced at both low and high frequency.
Back-side capacitors with close **placement** and short **routing** of the traces to the processor power pins and ground plane reduce effective L. However, reduction of effective C has caused an increase in impedance at mid frequency.

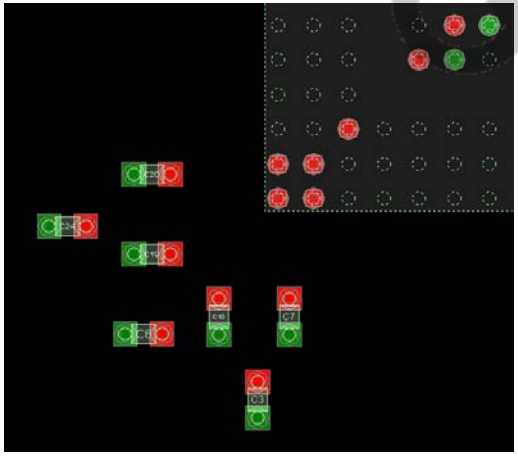
Modification – Case 5 Step 2

- To reduce the LC resonance peak ~1.5 MHz, all of the same-side decoupling capacitors were changed from 0.47 µF 0201 to 2.2 µF 0402. The pad size and PDN routing stayed the same; only the capacitance and ESL value in the circuit definition were changed.
- The impedance beyond 10 MHz is dominated by the effective inductance of the back-side capacitors and their routing to the processor power supply pins.

Note: There was not enough room for the required power/ground vias if all back-side 0201 capacitors were replaced by 0402.

Improve the LC resonance region.

Local decoupling capacitors (top side)



Capacitance	Quantities
2.2 µF (top side)	7
0.47 µF (back side)	7
22 µF	1
Total	15

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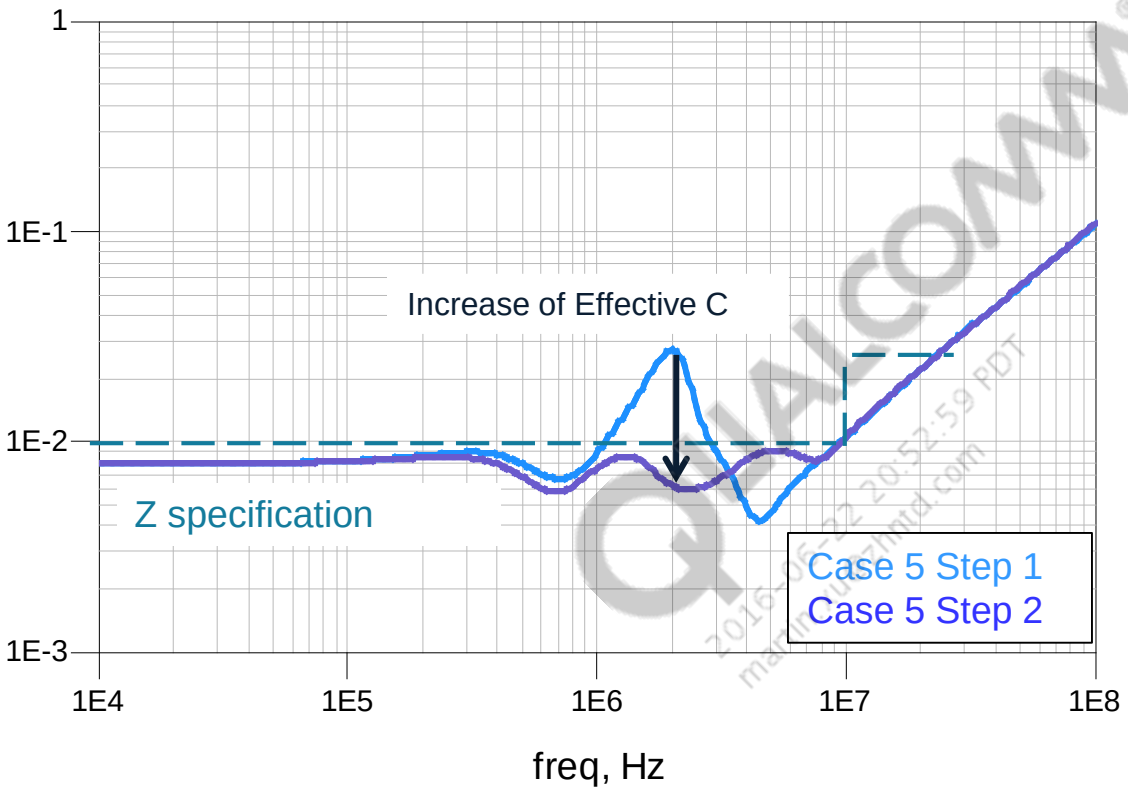
Change in PDN Impedance – Case 5 Step 2



PMIC = ideal voltage source

	Effective C	Effective L
Case 5 Step1	29.0 µF	0.17 nH
Case 5 Step 2	41.2 µF	0.17 nH

Observation: Replacing all of the same-side 0.47 µF capacitors with the 2.2 µF capacitors helped reduce the mid-frequency LC resonance peak. The high-frequency response (> 10 MHz) stays the same as Case 5 Step 1 because there were no routing changes. (This effective inductance is due to the back-side capacitors and their routing to the processor power supply pins.)

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Change in board stack-up

Original

Stackup

Layer Icon	Layer Name	Thickness(mil)
	Medium01	1.2000e+000
	Signal$LYR_1	1.2000e+000
	Medium$1	2.9500e+000
	Signal$LYR_2	1.2000e+000
	Medium$2	2.9500e+000
	Signal$LYR_3	1.2000e+000
	Medium$3	8.0000e+000
	Signal$LYR_4	1.2000e+000
	Medium$4	8.0000e+000
	Signal$LYR_5	1.2000e+000
	Medium$5	8.0000e+000
	Signal$LYR_6	1.2000e+000
	Medium$6	2.9500e+000
	Signal$LYR_7	1.2000e+000
	Medium$7	2.9500e+000
	Signal$LYR_8	1.2000e+000
	Medium02	1.2000e+000

Layer 3 = Power
Layer 4 = GND
Layer 5 = Power

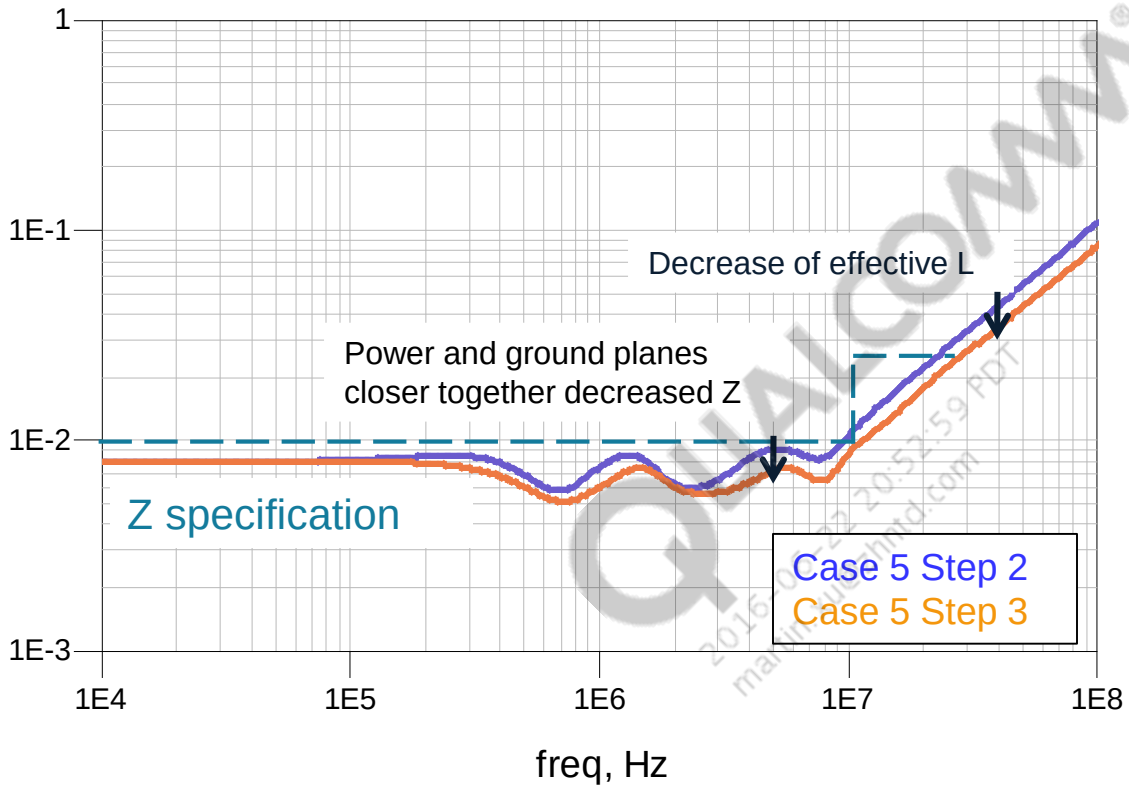
Thinner board

Stackup

Layer Icon	Layer Name	Thickness(mil)
	Medium01	1.2000e+000
	Signal$LYR_1	1.2000e+000
	Medium$1	2.9500e+000
	Signal$LYR_2	1.2000e+000
	Medium$2	2.9500e+000
	Signal$LYR_3	1.2000e+000
	Medium$3	6.0000e+000
	Signal$LYR_4	1.2000e+000
	Medium$4	4.0000e+000
	Signal$LYR_5	1.2000e+000
	Medium$5	6.0000e+000
	Signal$LYR_6	1.2000e+000
	Medium$6	2.9500e+000
	Signal$LYR_7	1.2000e+000
	Medium$7	2.9500e+000
	Signal$LYR_8	1.2000e+000
	Medium02	1.2000e+000

- The dielectric thickness between core layers was reduced as shown above.
- The total board thickness was reduced by 200 µm.

Change in PDN Impedance – Case 5 Step 3



PMIC = ideal voltage source

	Effective C	Effective L
Case 5 Step 2	41.2 µF	0.17 nH
Case 5 Step 3	41.2 µF	0.135 nH

Observation: When the board thickness (distance between power and ground planes) was reduced, the vias and current loop associated with the back-side capacitors became smaller, reducing the effective inductance.

Final Capacitors Selections

Capacitance	Original	Case 5 Step 1	Case 5 Step 2
2.2 µF (same side)	9	–	7
1 µF (same side)	4	–	–
0.47 µF (same side)	–	7	–
0.47 µF (back side)	–	7	7
22 µF (PMIC load capacitor)	1	1	1
Total	14	15	15

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Summary

Design changes	Modifications	Z_{PDN} DC–100 kHz	Z_{PDN} 100 kHz–10 MHz	Z_{PDN} (> 10 MHz)
Original		13.2 mΩ	–	164.85 mΩ
Modification Case 5 Step 1	• Layout changes • Decaps selections/placements	9.8 mΩ	22 mΩ	26.69 mΩ
Modification Case 5 Step 2	• Larger capacitance/dimension change (0201 → 0402)	9.8 mΩ	8 mΩ	26.69 mΩ
Modification Case 5 Step 3	• Board thickness reduced by 200 µm	9.8 mΩ	8 mΩ	21.19 mΩ

PDN impedance specification achieved.

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Section 4

Stress Test (AC1)

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Stress Test

- QTI provides a stress test vector named AC1 to create large processor PDN voltage transients in order to help verify the PDN design. (Customers should also run their own high concurrency tests at temperature extremes to supplement AC1).
- This test vector can be used only on a physical board.
- Designs must meet the PDN specifications (listed in the device specifications) first by simulation before tapeout. AC1 stress test is a supplement to, not a replacement for, meeting the PDN specifications.

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Recommended Lab Setup

- See the next slide for probe setup.
- Use an oscilloscope with BW ≥ 500 MHz, DC-couple, no low-pass filter, 50 Ω input, and infinite persistence mode to capture peaks. Use 50 Ω input because it is high-impedance to the PDN and has the advantage of allowing a very stable mechanical connection to the PDN. This allows repeatable measurements without picking up RF noise.
- Connect a 50 Ω coaxial cable to the scope (not a high impedance scope probe).
- PCB: Solder the center conductor of a semi-rigid coaxial shield to the capacitor closest to the MSM. Connect the shield of the coaxial cable to the ground closest to the above mentioned capacitor. The semi-rigid coaxial shield should have an SMA-type connector to connect to the 50 Ω coaxial cable from the scope.

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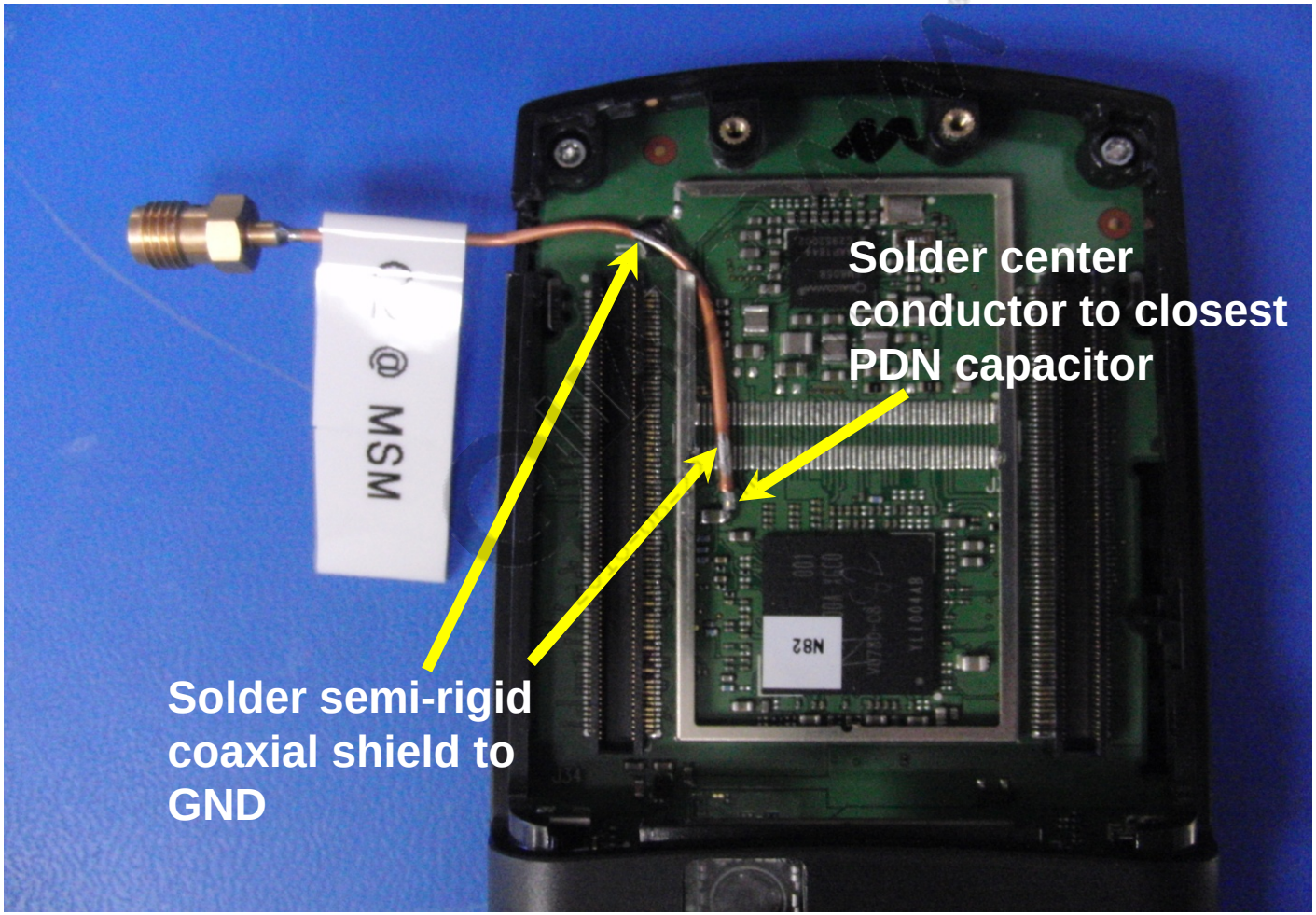
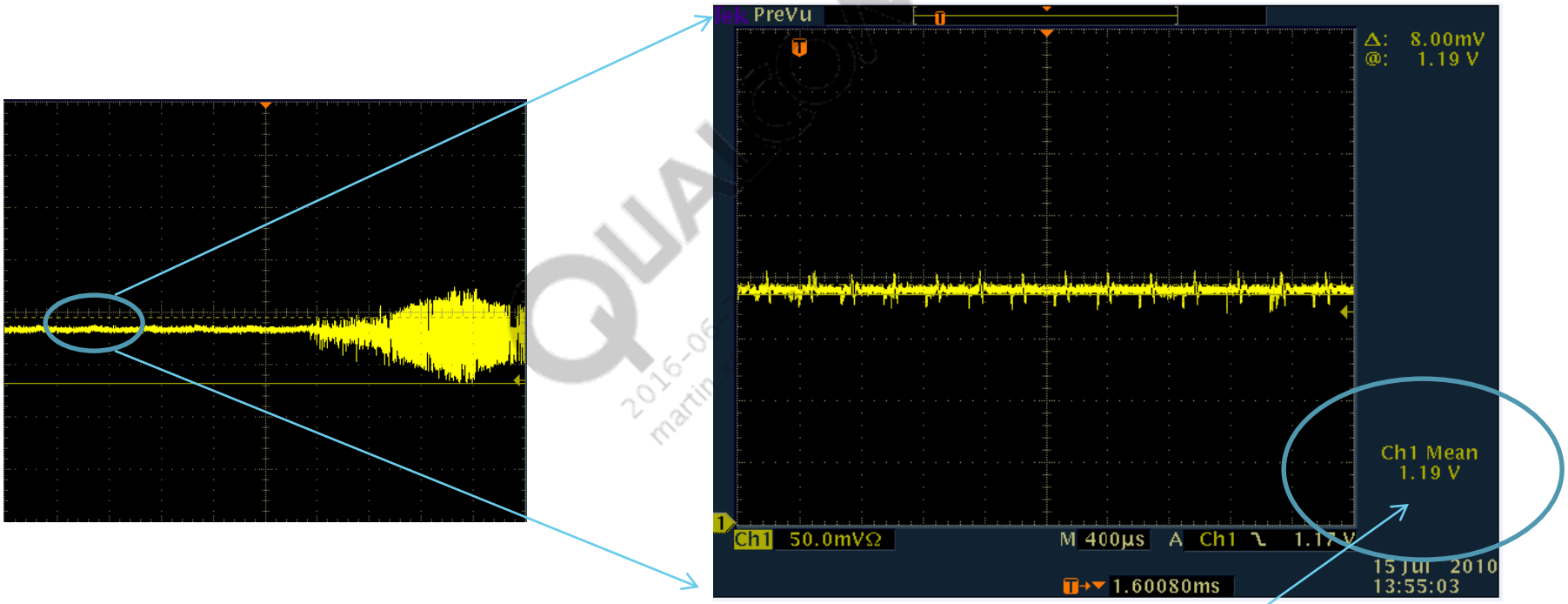
Stress Test Probe Setup



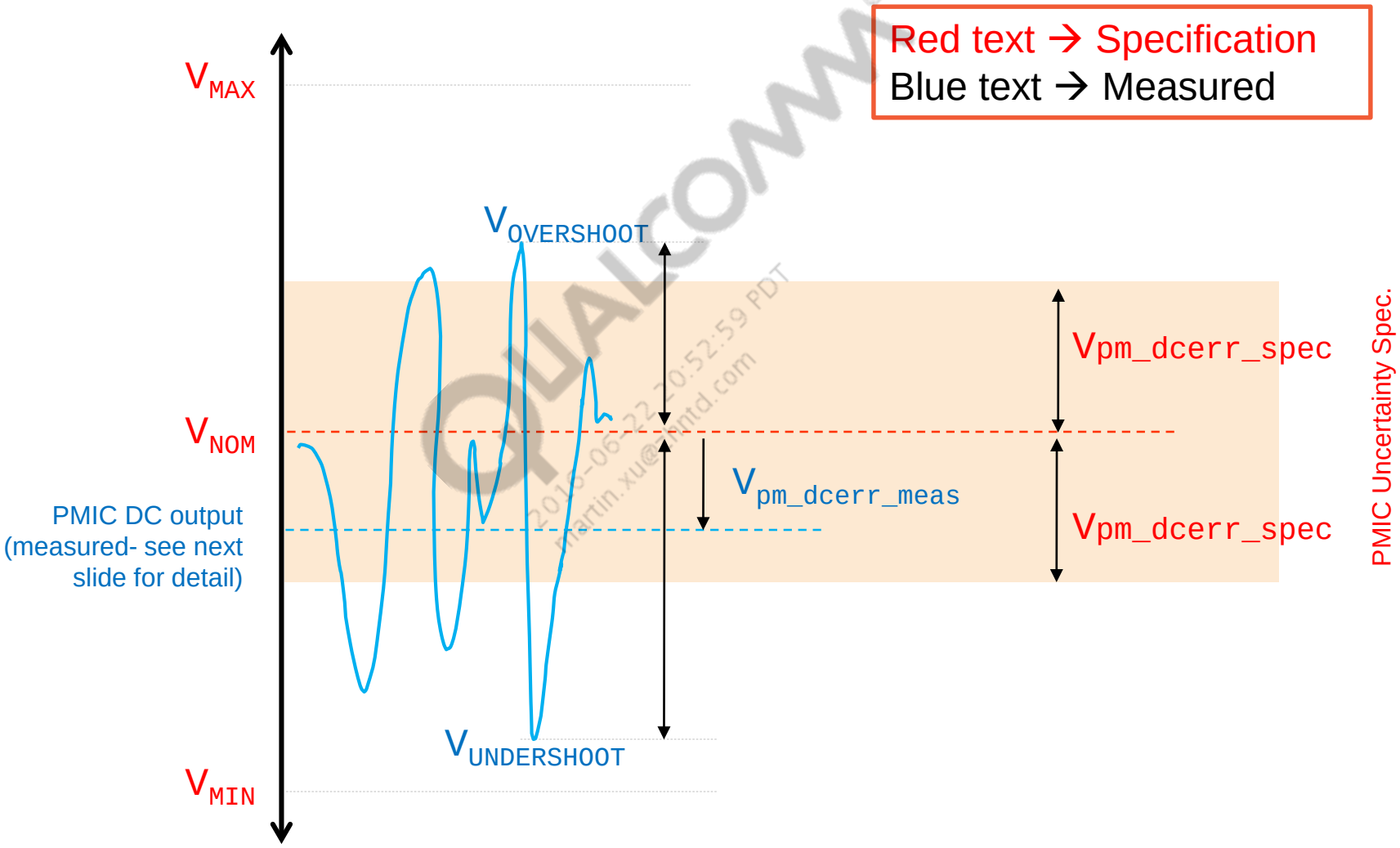
Typical AC1 Waveform

Scope capture of the AC1 script running on a MSM7x30 FFA



PMIC DC error at 25°C

Stress Test – Terms and Definitions (1 of 2)



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Stress Test – Terms and Definitions (2 of 2)

- **V_{nom}** = The PMIC set point (example: 1.2 V for the MSM8x55 device).
- **V_{min}** and **V_{max}** = Refer to the specification document.
- **$V_{undershoot}$** = The absolute value of measured undershoot relative to V_{nom} (when running the AC1 stress test).
- **$V_{overshoot}$** = The absolute value of measured overshoot relative to V_{nom} (when running the AC1 stress test).
- **$V_{pm\_dcerr\_meas}$** = The measured DC error of the PMIC relative to V_{nom}. This will be negative if the actual DC voltage is below V_{nom} and positive if it is above V_{nom}.
- **$V_{pm\_dcerr\_spec}$** = The error specified in the PMIC datasheet for PMIC output voltage relative to V_{nom}. Typically, it is expressed as a percentage of output voltage; it is converted to mV.

  Example: For PM8058 with MSM8x55, it was ±1% of V_{nom}. Hence, $V_{pm\_dcerr\_spec}$ = 0.01 * 1.2 V = 12 mV.

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Stress Test – Margin Calculations – High (V_{margin_h}) and Low (V_{margin_l})

- $V_{margin\_l} = V_{nom} - V_{min} - V_{undershoot} - (V_{pm\_dcerr\_meas} + V_{pm\_dcerr\_spec})$
- $V_{margin\_h} = V_{max} - V_{nom} - V_{overshoot} - (- V_{pm\_dcerr\_meas} + V_{pm\_dcerr\_spec})$

- Positive V_{margin_l} and V_{margin_h} ensures that the device V_{min} and V_{max} specifications are not violated.

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$V_{pm\_dcerr\_meas}$ Measurement

- Repeat the test setup and PCB solder connection as mentioned in Probe Setup.
- Run the AC1 stress test vector and measure the plot before the loop count begins. Use the Mean function in the scope for measurement. (See Typical AC1 waveform slide for an example.)
- Repeat the preceding steps over temperature (-30°C, 25°C, and 60°C).

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Stress Test for Other Power Rails

Question: Are stress tests being developed for other power rails besides the applications processor?

Answer:

- Not at this time.
- However, OEMs can do the following to verify other power rails:
  - Run the applications that switches maximum load current.
  - Measure the worst-case $V_{undershoot}$ and $V_{overshoot}$ as described in the previous Stress Test (AC1) section.
  - Measure the $V_{pmdcerr}$ as described in the Stress Test (AC1) section.
  - Calculate V_{margin_l} and V_{margin_h} as described in the Stress Test (AC1) section.

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Section 5

Frequently Asked Questions

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Section 5.1

General

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General – PDN Guidelines (1 of 2)

Question: Can you explain how the PDN impedance specifications were derived?

Answer: An approximation of the PCB PDN maximum impedance guideline (Zpcb) for frequencies where the PMIC impedance behavior dominates is calculated:

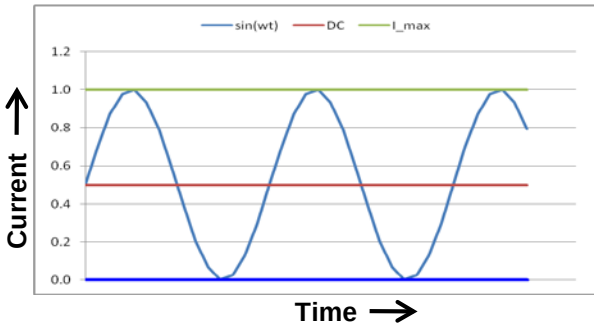
A. Define Z_{pm} as the maximum PMIC impedance (occurs at some frequency)
B. Define Z_{pcb} as the PCB impedance which is in series with the PMIC
C. Define V_{tr} as the maximum allowed voltage transient on the PCB
D. Assume the device draws a current consisting of a sinusoid (I_{ac}) with a DC offset (I_{dc}); see the graph below. The frequency of the sinusoid can be at the peak PMIC impedance.
E. The total worst case current (I_{max}) = I_{dc} + I_{ac}
F. The nominal voltage provided by the PMIC has some error represented as $V_{pmdcerror}$
G. The PMIC impedance at DC is ~0 Ω.

Apply Ohm's law:

- $(V_{tr} - V_{pmdcerror}) \geq Z_{pcb} * (I_{dc} + I_{ac}) + (Z_{pm} * I_{ac})$

Solve for Z_{pcb}:

- $Z_{pcb} \leq \{(V_{tr} - V_{pmdcerror}) - (Z_{pm} * I_{ac})\} / (I_{dc} + I_{ac})$



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General – PDN Guidelines (2 of 2)

MSM8x55 1.2 GHz calculation: Zpm = 140 mΩ (2 × 47 µF capacitors)

- I_{dc} = 0.517 A, I_{ac} = 0.413 A, V_{tr} = (1.2 V - 1.1 V) = 100 mV, $V_{pmdecerror}$ = 12 mV

- $Z_{pcb} \leq (V_{tr} - (Z_{pm} * I_{ac}) - V_{pmdecerror})/(I_{dc} + I_{ac})$
  $\leq$ (100 mV - (140 mΩ * 0.413 A) - 12 mV)/(0.517 A + 0.413 A)
  $\leq$ 32.5 mΩ for PCB PDN at the PMIC resonance frequency

MSM8x55 calculation: Zpm = 185 mΩ (2 × 22 µF capacitors)

- I_{dc} = 0.517 A, I_{ac} = 0.413 A, V_{tr} = (1.2 V - 1.1 V) = 100 mV, $V_{pmdecerror}$ = 12 mV

- $Z_{pcb} \leq (V_{tr} - (Z_{pm} * I_{ac}) - V_{pmdecerror})/(I_{dc} + I_{ac})$
  $\leq$ (100 mV - (185 mΩ * 0.413 A) - 12 mV)/(0.517 A + 0.413 A)
  $\leq$ 12.5 mΩ for PCB PDN at the PMIC resonance frequency

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General – PDN Specifications

Question: Where can I find the PDN specifications for each chipset?

Answer:

- Starting with the MSM8x30, PDN specifications are listed in Section 3.3 of the device specification (80-xxxxx-1, where xxxxx is the family number for a chipset). For older MSM devices, Section 3.3 was used for other topics, and PDN targets are listed in Section 3.2.

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General – Failure to Meet PDN Specification (1 of 2)

Question: Why are these impedances referred to as “Specifications” instead of just “Targets”?

Answer: Maximum PCB impedances defined in Section 3.3 of the device specification are “guaranteed to pass specifications”. This is similar to V_{min} and other specifications for ICs. It means that if the PCB meets the impedance specification, CS devices should not fail while being operated according to the operating conditions (defined in the device specification). However, failure to meet the PCB Z specification does not mean that every device will experience a failure. It means that for mass production quantities operated over the valid range of voltages and temperatures allowed by the device specification, the probability of failure for some percentage of the devices is not zero.

Question: What if I come close to meeting the impedance specification from DC to 25 MHz, but have trouble meeting it completely at some frequencies?

Answer: Failing to meet the impedance specification introduces the probability of failure under the allowed range of valid operating conditions. These conditions include normal silicon aging, temperature ranges, PMIC output voltages, maximum processor operating frequencies and certain processor instruction sequences. Meeting PDN impedance specifications ensures a zero chance of failure due to PDN issues for all devices under all operating conditions.

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General – Failure to Meet PDN Specifications (2 of 2)

Question: Do I need to raise the PMIC set point voltage if I cannot meet the PDN specifications? If so, by how much?

Answer: Raising the PMIC voltage by a PMIC step may reduce stability issues. However, if the PCB PDN design is not meeting the specification, the extra power consumption and related thermal issues may impact days of use and/or processor performance. Therefore, it is strongly recommended to submit your PDN design to the QTI Customer Engineering review team as soon as possible to ensure there is enough time to achieve the PDN specifications.

Question: If we do not see a launch gating issue when running AC1 or our maximum concurrency use cases and we still do not meet the PDN specification, then why should we be concerned about meeting the specification?

Answer: During a product launch, typically only a subset of the full production distribution of the silicon has been tested.

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General – VRM Models, Transient Simulations

Question: We do not want to provide our board layout to QTI, so can QTI provide validated transient step models and PMIC models for us to do our own time domain simulations?

Answer: Refer to the *Simulation* section for answers regarding PMIC, package/die models, etc.

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General – Trace Width (1 of 2)

Question: How wide must the PDN traces be to meet the required impedance?

Answer:

- Wide traces reduce overall PDN impedance.
- Resistance (R) = (resistivity of copper) * length/(width * thickness).
- There is no specific rule for PDN trace width. To meet PDN impedance specifications, QTI recommends performing **simulations as soon as parts placement and PDN routing are done** to verify that traces are wide enough.
- The length and width of the trace can be measured in the layout. The thickness is decided by the weight of copper. Resistivity of copper is a constant. Hence, a first-order approximation of the trace resistance can be calculated.

- Refer to the next slide for simulation examples/recommendations.

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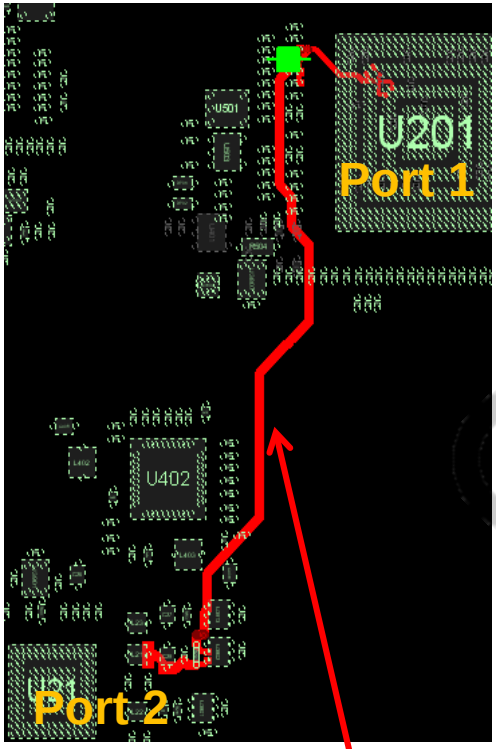
General – Trace Width (2 of 2)

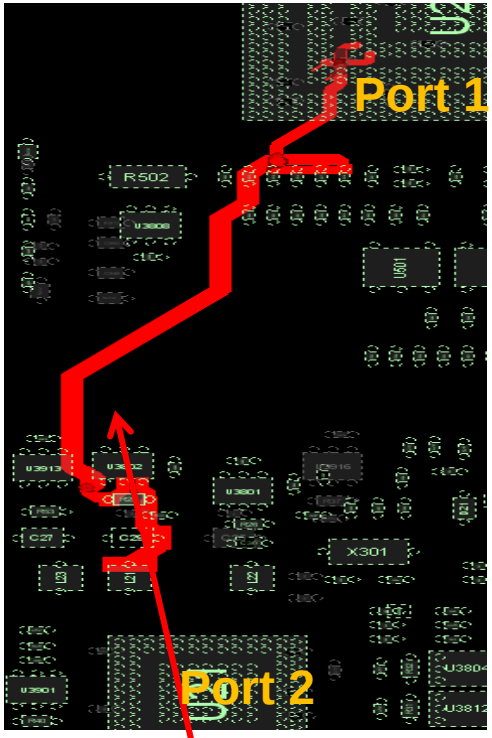
All layer view (from PMIC (port 2) output L to MSM (port 1))



Not recommended; need a wider trace for PDN

DC resistance (in PowerDC):

- From port 1 (MSM) to R29: 45.3 mΩ
- From R29 to L21: 3.4 mΩ



Wider trace reduces PDN impedance

DC resistance (in PowerDC):

- From port 1 (MSM) to R29: 25 mΩ
- From R29 to L21: 2.3 mΩ

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General – Back-side Capacitors

Question: We are doing a single-sided PCB. Are back-side capacitors (under the processor) required?

Answer:

- Properly placed and routed back-side capacitors are an effective design option because they can greatly reduce the PDN impedance at high frequencies (> ~10 MHz) when placed as close as possible to the processor power pins. This minimizes the effective inductance associated with those capacitors. It is usually more difficult to place top-side capacitors (on the same side as the processor) with as low an effective loop inductance.
- However, there is no hard requirement to use back-side capacitors. To meet the PDN impedance specifications, QTI recommends performing simulations as soon as parts placement and PDN routing are done.
- Refer to Modification Case 4 and Case 5 Step 1 in the PDN Design Example section for more information.

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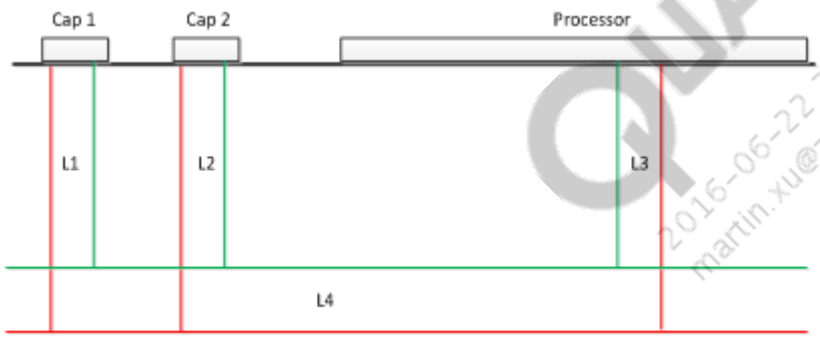
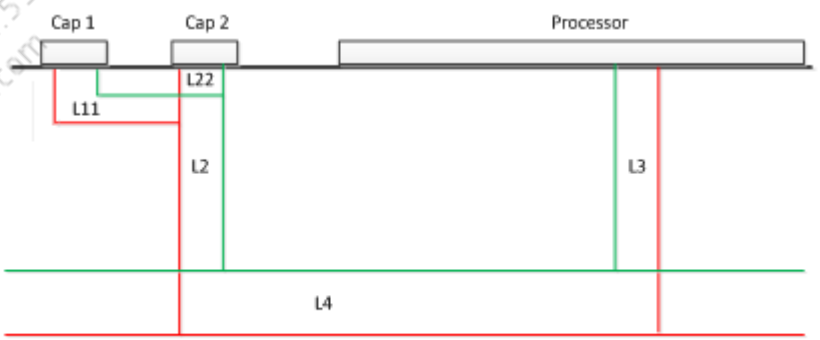
General – Via Routing

Question: How does via routing affect the PDN impedance?

Answer: Via routes to the power and ground should not be shared, but should be done individually to minimize the inductance due to the metal traces. Power and ground vias should be placed as close to each other as is practical to minimize the inductance due to loop area.





LEQ1 = L1//L2 + L4 + L3

LEQ2 = L11//L22 + L2 + L4 + L3

LEQ2 > LEQ1

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General – PCB Area and BOM Count

Question: We are concerned about PCB area and BOM count in our design. Do we need to keep all the PDN bulk capacitors and local decoupling capacitors in our design as shown in the reference schematic?

Answer:

- For bulk capacitors, following the reference schematic is highly recommended. Its values have been characterized and validated on MTPs (unless otherwise noted).
- Some of the decoupling capacitors may be DNIed provided meeting PDN specifications. Refer to design guidelines for each chipsets on decoupling capacitor reduction and optimization.
- For any questions on this subject, contact QTI (open a case) to get specific answers for your particular chipset at support.cdmatech.com.

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General – Placement Distance between PMIC and the Processor

Question: What is the recommended distance between the PMIC and the processor power supply pins?

Answer:

- The PCB placement distance between the PMIC and the processor must be determined from the results of phone level thermal simulations using commercially available thermal simulation software (e.g., Icepak or FloTHERM).
- Placing the PMIC and the processor too close together on the PCB can greatly compromise the design from a thermal perspective.
- Once the placement of the PMIC and the processor has been defined by thermal simulation, PDN traces should be routed and verified by simulation in order to meet the device specification requirements.

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General – Power and Ground Planes

Question: What is the recommended distance between the power plane and the ground plane?

Answer: Power and ground planes should be placed as close to each other as possible to minimize the PDN impedance/loop inductance. Use adjacent layers and minimize the distance between those layers. To meet PDN impedance specifications, QTI recommends performing **simulations as soon as parts placement and PDN routing are done**.

Refer to the PDN design example.

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General – Overshoot Impact

Question: Does voltage overshoot on the power rail impact the MSM device?

Answer: Yes. Voltage overshoot on the power rail does impact the MSM device. For example:

- A 1 GHz processor clock implies a 1 ns clock period.
- 1 µs of voltage overshoot transient on a corresponding PDN power rail will impact 1000 clock cycles.
- This could cause a violation of the hold time requirements of the corresponding circuitry.

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General – Zero-Ohm Resistor

Question: Can we place a small resistor in series with the PDN for current measurement/debugging on the PDN?

Answer:

- Even 0 Ω resistors can raise the PDN impedance by 10 to 25 mΩ. This is usually unacceptable. Therefore, it is suggested that a special shorted resistor component be created in the CAD library and placed in series with the PDN. This is the exact same size as a resistor however with a thick copper trace shorting the two pads.
- In mass production, this is simply a short circuit. When current consumption breakdown measurements are needed (usually on only a few phones), the copper trace on the shorted resistor component can be carefully cut and a small ohm resistor can be soldered across the two pads.

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Section 5.2

Simulation

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Simulation – QTI Help with Simulations

Question: Will QTI simulate my design?

Answer: QTI can:

- Simulate the customer's PDN in the frequency domain.
- Provide the feedback on improving the PDN design where needed to meet PDN specifications.
- Send a response within five business days.
  - QTI recommends that customers open a case to do simulations for each project at https://support.cdmatech.com.

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Simulation – Simulation Tools

Question: What simulation tools does QTI use?

Answer:

- Sigrity PowerDC: http://www.sigrity.com/products/powerdc/powerdc.htm
- Sigrity PowerSI: http://www.sigrity.com/products/powersi/powersi.htm

- **IMPORTANT NOTE:** When the PMIC is modeled as an ideal voltage source, the importance of the large bulk capacitors at the PMIC output will not be seen in the simulation. However, these large capacitors are critical for reducing the effective impedance of the PMIC and must be retained in the design according to the reference schematics.

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Simulation – Files Needed for Simulations

Question: Which files should we provide to QTI to do simulations?

Answer: One of the following layout files should be provided:

- Cadence Allegro → .brd
- OrCAD → .dsn
- Mentor Graphics – PADS → .pcb and .asc
- Mentor Graphics → Board Station → pcb folder
- ODB++ file – Make sure that the signal names are preserved when exported from CAD tools.

- The customer MUST provide:
  A. Accurate PCB stack-up information file in either the layout or a separate spreadsheet file. See *Simulation – PCB Stack-up*.
  B. The PCB schematic.
  C. A document highlighting all the changes to the PDN from any previous revision. Include snapshots of the PCB layout. This step is very important to improve response time from QTI.

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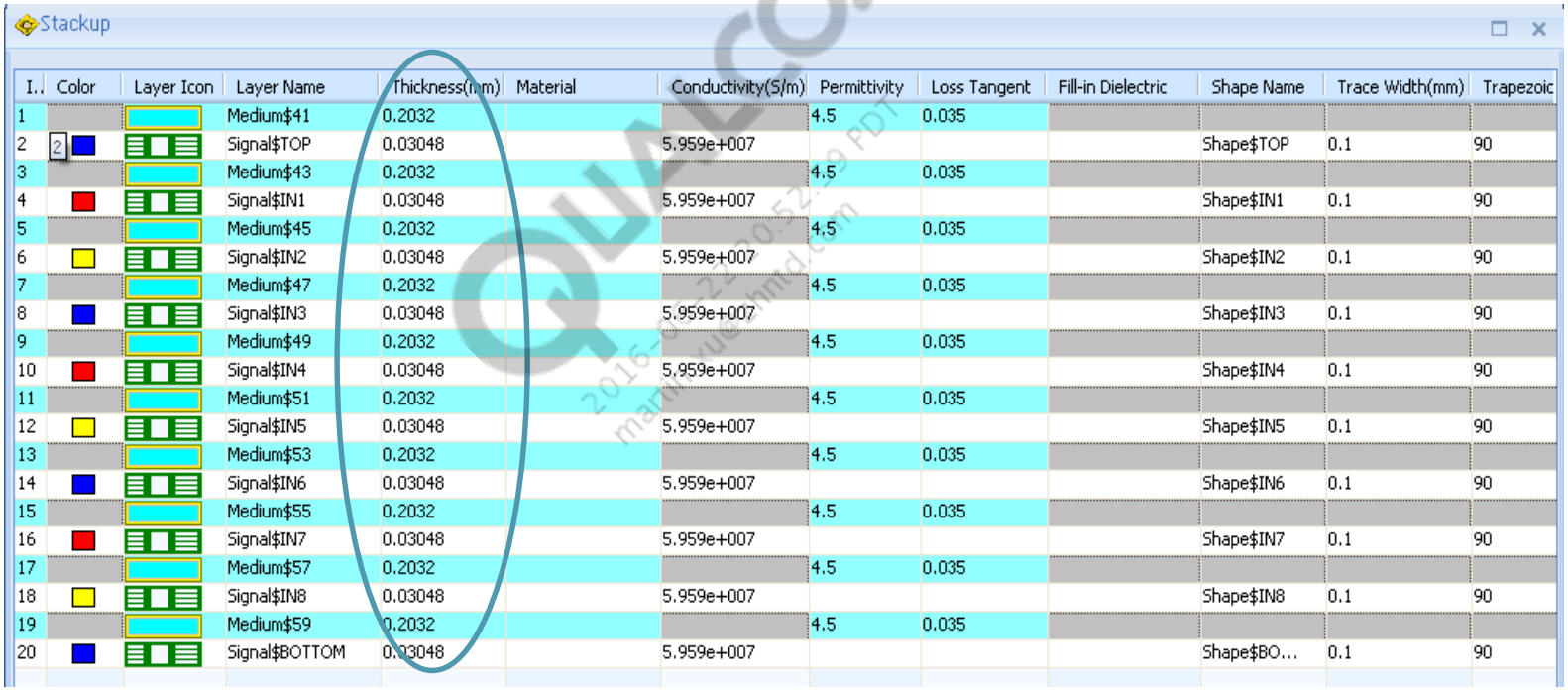
Simulation – PCB Stack-up

General: A PCB stack-up is extracted from the layout file during translation. It is very important for OEMs to verify this PCB stack-up and the thickness of each layer with the PCB manufacturer to ensure the correct information is used in the PDN simulation.



I..	Color	Layer Icon	Layer Name	Thickness(mm)	Material	Conductivity(S/m)	Permittivity	Loss Tangent	Fill-in Dielectric	Shape Name	Trace Width(mm)	Trapezoic
1			Medium$41	0.2032			4.5	0.035				
2			Signal$TOP	0.03048		5.959e+007				Shape$TOP	0.1	90
3			Medium$43	0.2032			4.5	0.035				
4			Signal$IN1	0.03048		5.959e+007				Shape$IN1	0.1	90
5			Medium$45	0.2032			4.5	0.035				
6			Signal$IN2	0.03048		5.959e+007				Shape$IN2	0.1	90
7			Medium$47	0.2032			4.5	0.035				
8			Signal$IN3	0.03048		5.959e+007				Shape$IN3	0.1	90
9			Medium$49	0.2032			4.5	0.035				
10			Signal$IN4	0.03048		5.959e+007				Shape$IN4	0.1	90
11			Medium$51	0.2032			4.5	0.035				
12			Signal$IN5	0.03048		5.959e+007				Shape$IN5	0.1	90
13			Medium$53	0.2032			4.5	0.035				
14			Signal$IN6	0.03048		5.959e+007				Shape$IN6	0.1	90
15			Medium$55	0.2032			4.5	0.035				
16			Signal$IN7	0.03048		5.959e+007				Shape$IN7	0.1	90
17			Medium$57	0.2032			4.5	0.035				
18			Signal$IN8	0.03048		5.959e+007				Shape$IN8	0.1	90
19			Medium$59	0.2032			4.5	0.035				
20			Signal$BOTTOM	0.03048		5.959e+007				Shape$BO...	0.1	90

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Simulation – Mentor Graphics (PADS) Files

Question: We are working on Mentor Graphics PADS. Do we need to provide both .pcb and .asc layout files for simulation?

Answer: Yes. You need to provide both .pcb and .asc layout files for simulation. The simulation environment cannot convert a .pcb file alone to an .spd (Sigrity PowerSI) file for simulation. An .asc file is also required.

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Simulation – Preparation of Layout Files

Question: What preparations must be done in the layout files before they are provided to Qualcomm for simulations?

Answer: Ensure that the following steps are implemented properly in the layout before providing the layout files to QTI.

A. Flood the Ground fill throughout the layout.
B. Ensure that all capacitors' values (or at least the values of the capacitors for the processor and modem power rails) are assigned to the components in the file. (Refer to the examples on the next two slides.)
C. Ensure that all capacitors' sizes/dimensions (or at least the sizes of the capacitors for the processor and modem power rails) are assigned to the components in the file. (Refer to the examples on the next two slides.)
D. Make sure all DNI/DNP (do not install/place) capacitors are accurately documented in the schematic.

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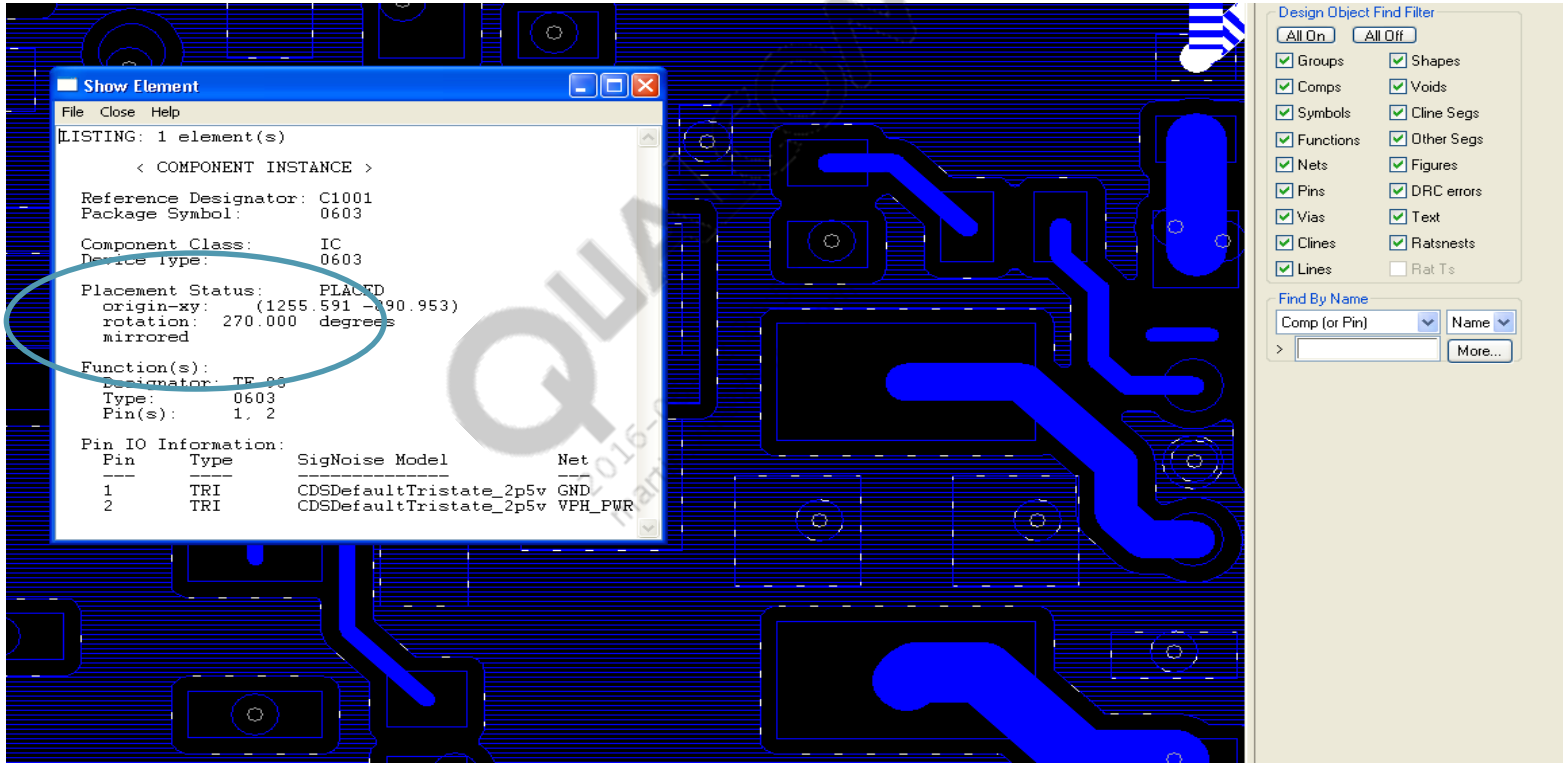
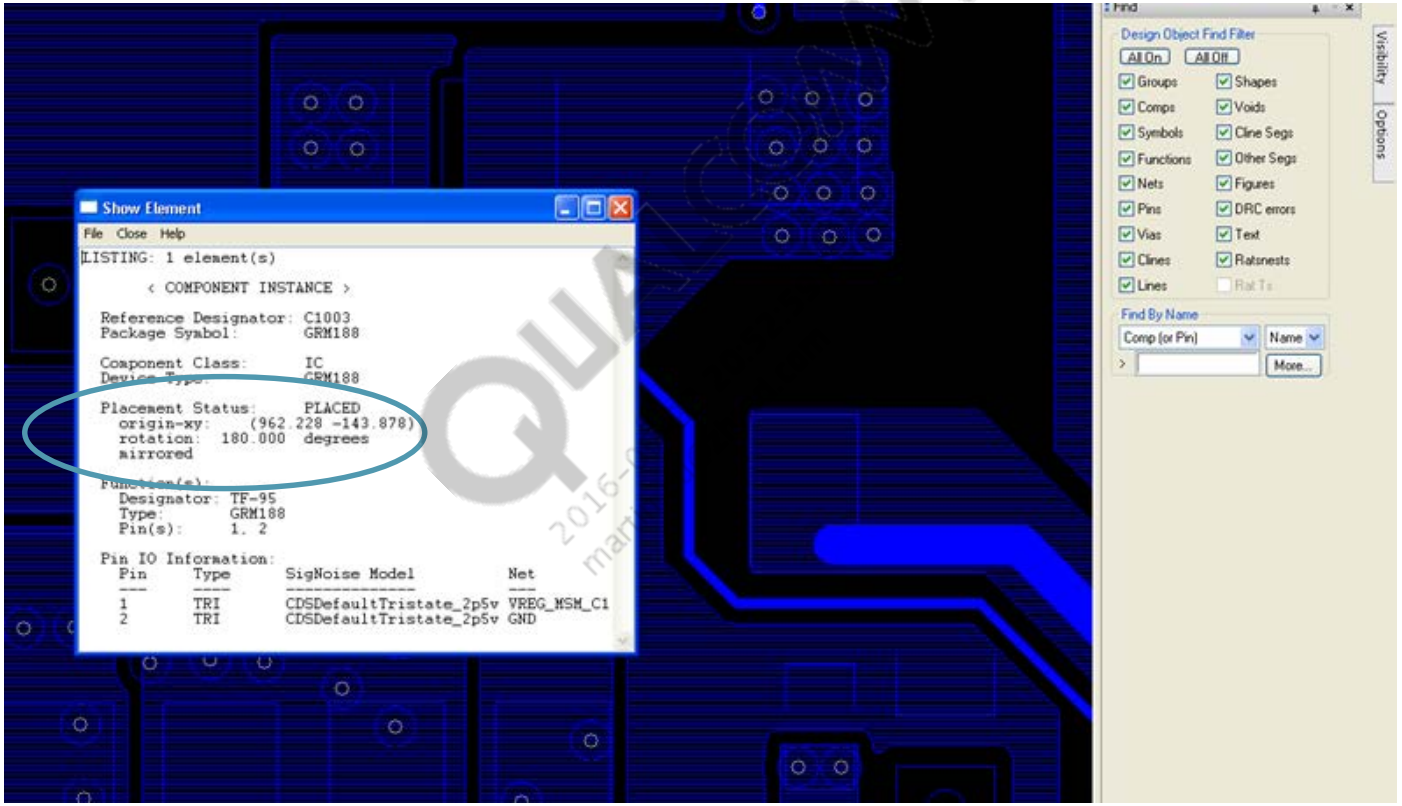
Preparation for Layout Files – Example of Missing Capacitor Value in Cadence Allegro

- All capacitor values (Farad) should be assigned in standard SPICE format such as 47µ, 2200n, 470n, etc.
  - Do not assign values as 0_47uF.



Preparation for Layout Files – Example of Missing Capacitor Size/Dimension in Cadence Allegro

- All capacitor dimensions should be assigned in standard package format such as 0805, 0603, 0402, or 0201.



Simulation – Turnaround Time for Simulation Report

Question: What is the turnaround time to get the simulation report from QTI on my design?

Answer:

- QTI will make the maximum effort to provide a simulation report as soon as possible. However, given time and resource constraints, the **OEM should expect five business days of turnaround time to get the simulation report.** To improve this turnaround time, it is very important that the OEM provides the right files in the beginning of project. This will help facilitate the entire process. Refer to the following for more details:
  - Files Needed for Simulation
  - Preparation for Layout Files
  - Additional files from Rev B of the customer design onwards
- It is also very important, from Revision B of the customer design and onwards, to provide a document highlighting all the changes to PDN from the previous revision.

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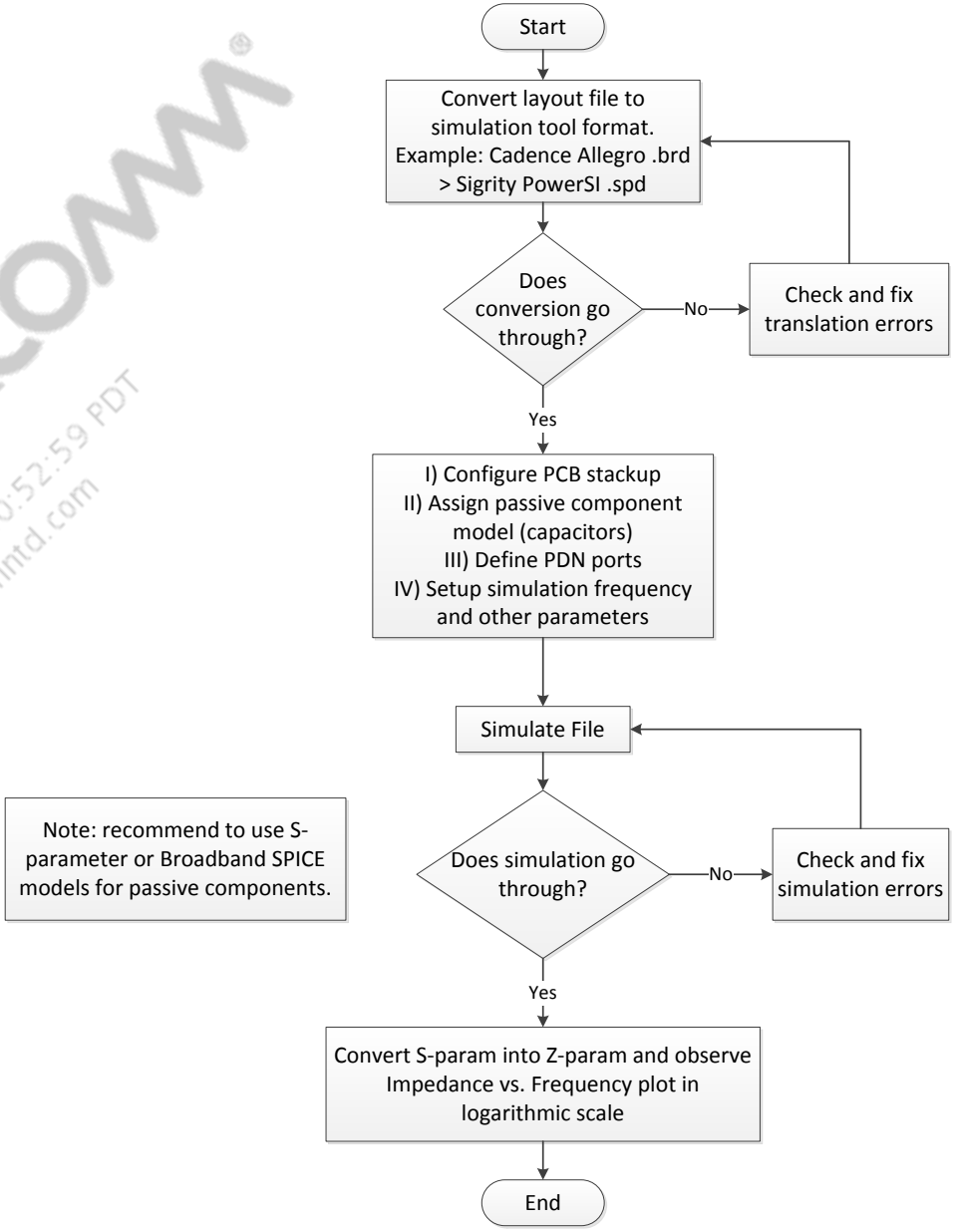
Simulation – Flowchart of Simulation Procedures

Question: We have the necessary software to do the simulations. What are the simulation steps?

Answer: See the flowchart on the right.



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Simulation – PMIC Models

Question: What PMIC models are used by QTI in PDN simulations?

Answer:

- QTI does not include the PMIC in the simulation. Refer to *Simulation – Port Definition* for more information.
- The VRM (PMIC) is taken into account by QTI when the specification impedance is defined in the device specification and when the VRM (PMIC) load capacitors are defined on the reference schematic. Note that frequency-domain PMIC models are small signal models that are not accurate under large loads, so QTI does lab measurements of PMIC impedance vs. load capacitor values. QTI then specifies the low frequency PDN specifications in the device specification so the PMIC impedance at resonance, added in series with the loop inductance of the PCB PDN at that frequency, will be low enough to avoid voltage excursions below V_{min} or above V_{max} as defined in the device specification.

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Simulation – Package/Die Models

Question: Does QTI include package and die models in the simulation?

Answer: The die + package parasitic is taken account by QTI when the specification impedance is defined in the device specification. QTI specifies the PDN specifications at 25 MHz so that the loop inductance of the PCB, added in series with the loop inductance of the package + die, creates a low enough impedance to avoid voltage excursions below V_{min} or above V_{max} as defined in the device specification. This makes it easier for customers because they only have to focus on meeting device specification impedances for their PCB PDN. This is done by optimizing parts placement, capacitor selection, power trace/via size, routing, and following the reference schematic.

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Simulation – Port Definition

Question: We have the tools to perform PDN simulation. How do we select the ports for simulation to generate S-parameters?

Answer: Refer to the PDN section of device specifications where QTI defines the ports for each power rail. Some power rails have lumped ports (all power pins as positive and all GND pins as negative on a port), while some other rails have distributed ports with clear port definition.

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Simulation – Resistance Measurement

Question: Does QTI calculate power trace resistance or the power-ground loop resistance?

Answer: QTI specifications refer to the power-ground loop resistance. PowerDC provides the option to calculate both. Calculating the power trace resistance and the power-ground loop resistance is recommended so that the relative contributions can be understood. QTI provides the power-ground loop resistance.

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Simulation – Current Measuring Resistor

Question: We have current measurement resistors on some of the power rails. How are these resistors modeled in the simulation?

Answer: Current measurement resistors are ignored in the PDN simulation, i.e., they are treated as 0 Ω resistors.

Refer to the *General – Zero-Ohm Resistor* section for recommendations regarding current measurement resistors.

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Simulation – Time Domain Analysis

Question: The PDN simulation is done in the frequency domain. What does QTI provide for time domain verification?

Answer: QTI supplies the AC1 test (described in the section *Stress Test (AC1)* to help customers evaluate the margin in their designs. The PCB specification impedances are defined so that worst-case changes in load current will not cause CS quality devices to have excessive voltage excursions (below V_{min} or above V_{max}) when they are tested over the frequency and temperature ranges listed in the operating conditions of the device specification.

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Simulation – Chip Power Models

Question: Does QTI use the chip power model (CPM) for PDN analysis?

Answer: Although QTI has evaluated CPM modeling, there are problems with the accuracy of these models; hence, QTI does not use these models to develop PCB PDN specifications.

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Simulation – Transient Simulation

Question: Does QTI do transient simulation? In transient simulation, what kind of current sink models do you use? Does QTI simulate transient voltage drop?

Answer: QTI PDN specifications are created as described in *General – PDN Guidelines*. The assumed current source is described in *General – PDN Guidelines* as a simple sinusoid + DC that is swept over frequency. This slide also calculates transient voltage drop.

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Questions?

You may also submit questions to:
https://support.cdmatech.com

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