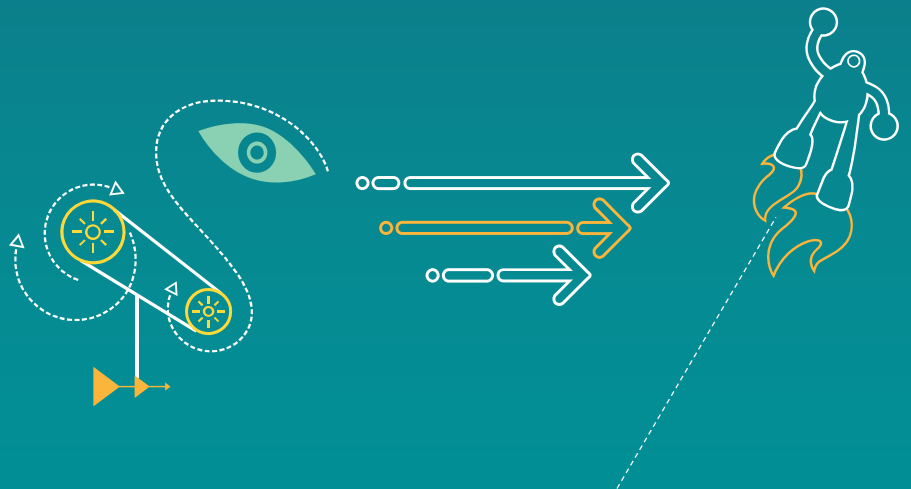
Design Guidelines/Training Slides

PM8937/PM8940 + PMI8937/PMI8940 Power Management IC

Qualcomm Technologies, Inc.

80-P2564-5B Rev. D



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Revision History (1 of 2)

Revision	Date	Description
A	October 2015	Initial release
B	December 2015	Slide 7: Updated comparison table with parallel charging and dual charging path support Slide 14: Updated description about MPP Slide 97: Updated SMPS S1 default state Slide 99 and 100: Added power grid information Slide 155: Removed series resistor for MPP
C	June 2016	• Updated PM8937 to PM8937/PM8940 throughout the document • Updated PMI8937 to PMI8937/PMI8940 throughout the document • Slide 7, *Power Management System*: Updated the PM8940 pairing details • Slide 8, *Power Management System Comments (1 of 2)*: ▪ Updated the PM8937 and PM8940 pairing details ▪ Modified SMB1358 to SMB135x • Slide 9, *Power Management System Comments (2 of 2)*: Updated the table details for the different PMIC variants • Slide 10, *PMI8937/PMI8940 High-level Block Diagram*: Updated the block diagram and added a note • Slide 12, *PMI8937/PMI8940 Features (1 of 5):* Updated the details of high charging current on PMI8937 and PMI8940 • Slide 14, *PMI8937/PMI8940 Features (3 of 5)*: Added the display bias supplies feature • Slide 17, *PM8937/PM8940 Features (1 of 4):* Added a note for the S1 SMPS rated current • Slide 22, *PMI8940 Keypad Groupings*: Added the PMI8940 pin map

Revision History (2 of 2)

Revision	Date	Description
C (cont.)	June 2016	• Slide 26, *SCHG Feature Summary*: Updated the charging current details • Slide 31, *USB Power Source and OVP – Architecture and Schematic*: Updated the charging current details • Slide 59, *CHG_LED Output for Charging Indication*: Updated the CHG_LED active status • Slide 93, *Battery Missing Detection*: Updated the MSM8940 schematic review checklist document details • Slide 100, *Output Power Management - Summary (1 of 2)*: ▪ Added a note for the S1 SMPS rated current ▪ Updated the rated current value for the L5 function • Slide 101, *Output Power Management - Summary (2 of 2)*: ▪ Updated the default ON value for the L10 function ▪ Updated the default voltage value for L23 function • Slide 143, *User Interfaces*: Added the display bias details • Slide 145 to Slide 155: Updated Haptics section • Slide 157 to Slide 159: Added Display ± Bias section • Slide 183, *PM8937/PM8940 OPT Pins*: ▪ Modified the details and updated the OPT_1 value ▪ Updated the OPT_1 and configuration values • Slide 191, *Reset Timers*: Updated notes • Slide 192 to Slide 195: Added the Reset Scheme and PON recommendations • Slide 205: *Unused Pin Terminations*: Updated the schematic review checklist for PM8937 and PM8940
D	16 June 2016	• Slide 7, *Power Management System*: Updated the PM8937 and PM8940 pairing details • Slide 8, *Power Management System Comments (1 of 2)*: ▪ Updated the PM8937 and PM8940 pairing details

Contents

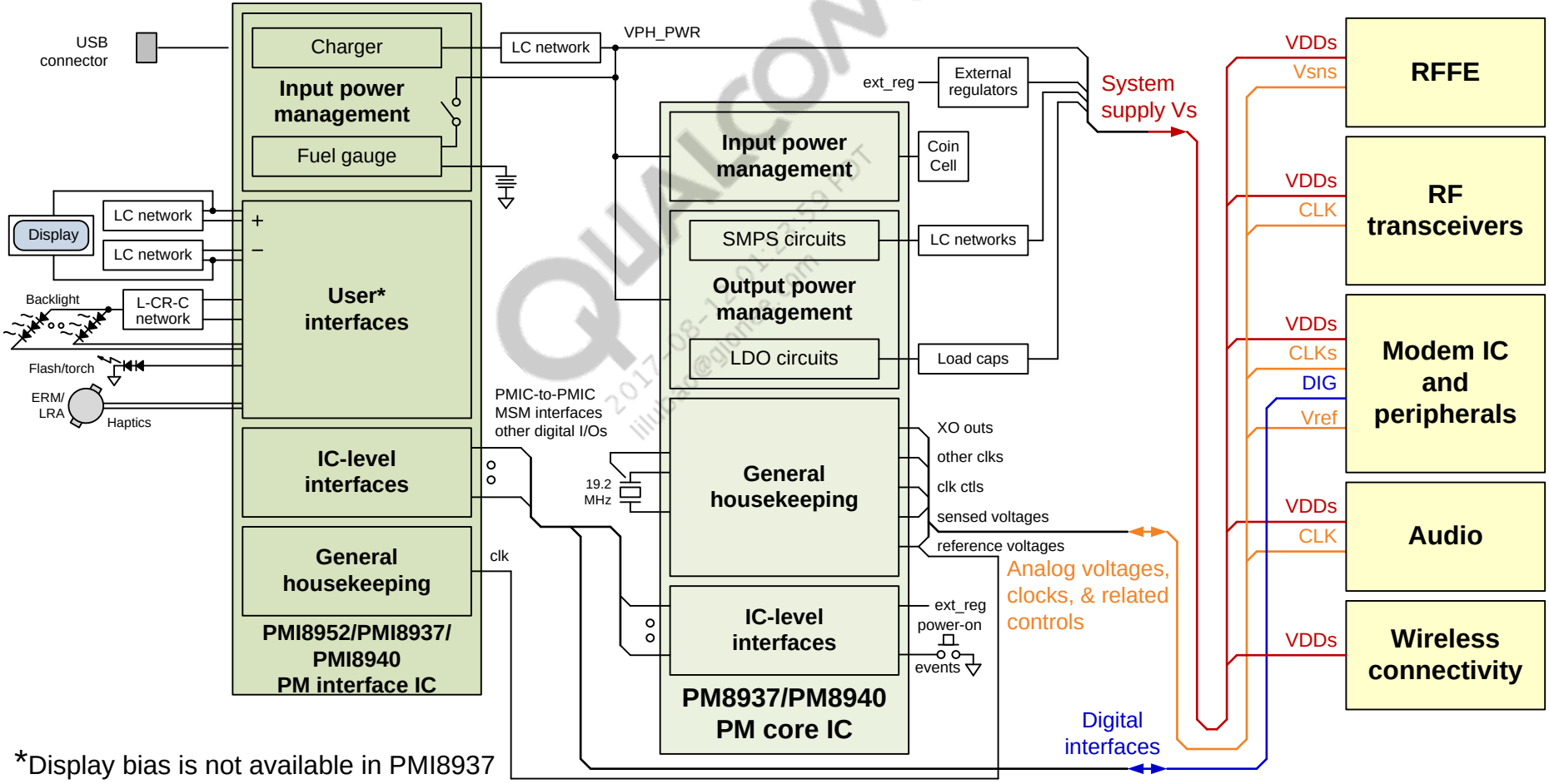
Section 1

Power Management System and IC Overviews

Refer to the MSM8937 Design Guidelines (80-P2468-5B) for available documents, reference designs, and evaluation platforms.

Power Management System

- Functions divided between a PM core and the PM interface devices
- PM8937/PM8940 can pair with either PMI8952 or PMI8940 or PMI8937
- DC power sources for all wireless product circuits
- System and sleep clock sources for the entire chipset
- Digital interfaces between PMIC, PMI, and modem IC



*Display bias is not available in PMI8937

Power Management System Comments (1 of 2)

PM8937/PM8940 – the PM core IC

- Most of the housekeeping (including system clocks) and output power management functions.

PM interface IC

- PM interface IC can be either PMI8952 or PMI8937 or PMI8940.

  Refer to the *PM8937/PM8940 + PMI8952 Power Management IC Design Guidelines/Training Slides* (80-P2564-5A)

  - PM8937/PM8940 can pair with either PMI8952 or PMI8940 or PMI8937
- Most of the input power management functions (including charger) and user interfaces

The PM pair

- Both the PM core and the PMI have IC-level interfaces to communicate with the modem IC and each other
- The PM core is the master while the PMI device is the slave

External regulators

- Supported for supplying specific circuits

SMB135x is optional and is used for parallel charging with PMI8952 to increase charging efficiency and thermal performance at high charge currents

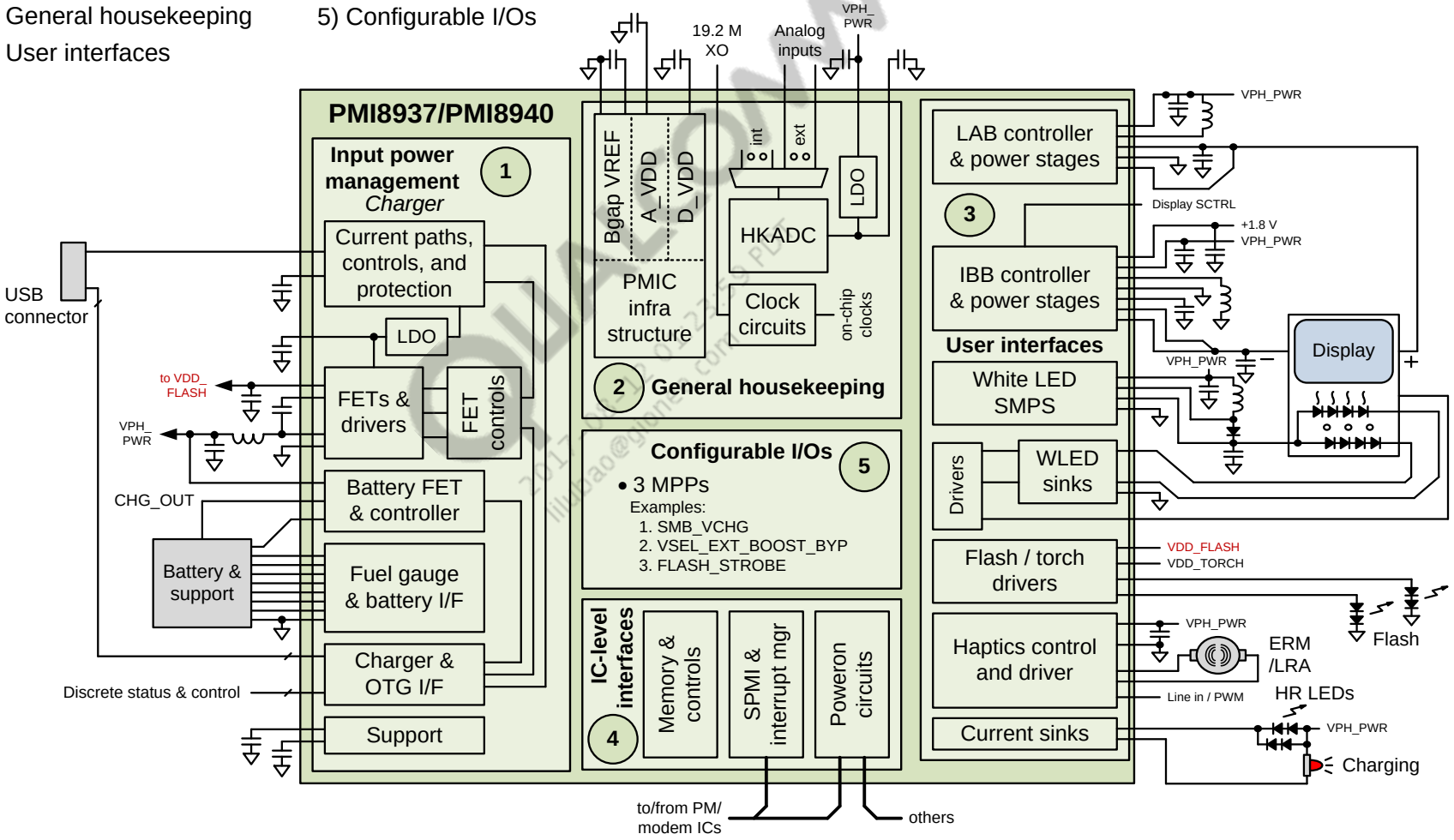
Power Management System Comments (2 of 2)

	PMI8952	PMI8937	PMI8940	PM8937/PM8940
Input power management	• Battery charger with HVDCP support integrated battery FET battery fuel gauge • Parallel charging support with SMB1358 • Dual charging path support with external PMUX • Maximum of 3 A charging current	• Battery charger-integrated battery FET battery fuel gauge • No parallel charging support • No dual charging path support • Maximum of 1.5 A charging current	• Battery charger-integrated battery FET battery fuel gauge • No parallel charging support • No dual charging path support • Maximum of 2 A charging current	Coin cell backup support
Output power management				3-SMPS (3.0 A each) 1-SMPS (2.7 A) 1-SMPS (2.5 A) 1-SMPS (2.0 A) 4 x 1200 mA NMOS LDOs 1 x 300 mA NMOS LDO 4 x 600 mA PMOS LDOs 1 x 450 mA PMOS LDO 3 x 300 mA PMOS LDOs 4 x 150 mA PMOS LDOs 4 x 50 mA PMOS LDOs 2 x clock LDOs
User interfaces	• LCD/AMOLED driver bias supplies • WLED backlight SMPS and drivers (8s4p) • Camera flash/video torch driver • ERM/LRA Haptics • Charging indicator	• WLED backlight SMPS & drivers (8s2p) • Camera flash/video torch driver • ERM/LRA Haptics • Charging indicator	• WLED backlight SMPS & drivers (8s2p) • Camera flash/video torch driver • ERM/LRA Haptics • Charging indicator • LCD driver bias supplies	
Audio codec				1 differential, 2 single-ended inputs Earpiece, HPH L&R, class-D driver Up to 5 button MBHC support Multiple audio I/O sample rates Audio-specific power supplies
General housekeeping & IC-level interfaces	Analog multiplexing & HK ADC SPMI for modem communications Battery UICC alarm (BUA) support MIPI battery interface (BIF) support 4 MPPs, 2 GPIOs	Analog multiplexing & HK ADC SPMI for modem communications BUA support BIF support 3 MPPs	Analog multiplexing & HK ADC SPMI for modem communications BUA support BIF support 3 MPPs	System clock generation System clock distribution Real-time clock Analog multiplexing & HK/XO ADC SPMI for modem communications System control (on/off/reset) 4 MPPs, 8 GPIOs

PMI8937/PMI8940 High-level Block Diagram

Five major functional blocks:

1) Input power management
2) General housekeeping
3) User interfaces
4) IC-level interfaces
5) Configurable I/Os

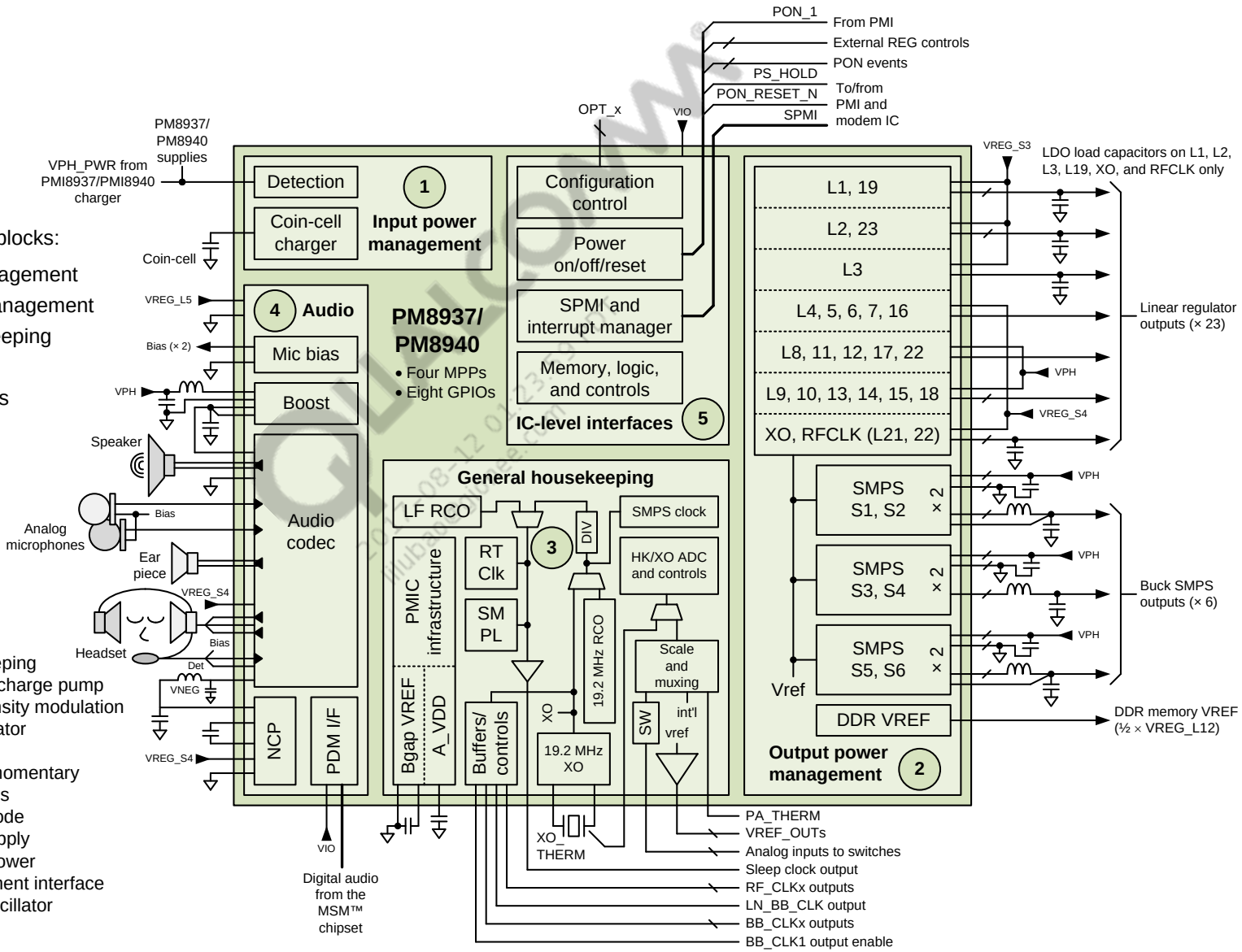


Note: LAB/IBB is present only in PMI8940

PM8937/PM8940 High-level Block Diagram

Five major functional blocks:

1) Input power management
2) Output power management
3) General housekeeping
4) Audio
5) IC-level interfaces



HK = housekeeping
NCP = negative charge pump
PDM = pulse density modulation
RCO = RC oscillator
RT = real-time
SMPL = sudden momentary power loss
SMPS = switch mode power supply
SPMI = system power management interface
XO = crystal oscillator

PMI8937/PMI8940 Features (1 of 5)

Feature	PMI8937/PMI8940 capability
Input power management	
Input source selection	▪ Supports USB power source ▪ Automatic and programmable input current limit for USB compatibility
Battery charger	Switched-mode battery charger/boost (SCHG) – battery charger with reverse-boost mode ▪ Highly efficient (~91% peak efficiency) power conversion ▪ 4 V–7.2 V operating input voltage range ▪ 28 V overvoltage protection (OVP), nonoperating ▪ Automatic power source detection (APSD), prioritization, and programmable input current limiting per the *USB Charging Specification 1.2* (USB 2.0/3.0 compliant) ▪ High charging current, up to 1.5 A on PMI8937 and 2 A on PMI8940 (subject to thermal and efficiency requirements) ▪ Current path control allows system operation with deeply discharged or missing battery ▪ Trickle, precharge, and constant current/voltage charging ▪ Integrated BATFET; also functions as current sense element for charging control ▪ TurboCharge–750 mA charge from 500 mA USB port ▪ JEITA and JISC 8714 support ▪ 1.0 MHz, 1.5 MHz, 2.0 MHz, or 3.0 MHz switching frequency – tiny external parts ▪ Real-time charge and discharge current measurement ▪ USB On-The-Go (OTG) supports up to 1 A (USB OTG standard compliant and USB-IF ACA specification compliant) ▪ Reverse-boost support for flash LED current, up to 2 A (supports concurrency cases for USB OTG and flash LED) ▪ Comprehensive protection features

PMI8937/PMI8940 Features (2 of 5)

Feature	PMI8937/PMI8940 capability
Input power management (cont.)	

Fuel gauge	▪ Optimized mixed algorithm with current and voltage monitoring
	▪ Highly accurate battery state-of-charge estimation
	▪ 16-bit dedicated current ADC (15 bits plus sign bit)
	▪ 15-bit dedicated voltage ADC for measuring the VBAT, BATT_THERM, and BATT_ID
	▪ Operates independently of software and reports state of charge without algorithms running on the modem IC:
	  ▪ No external nonvolatile memory required
	  ▪ No external configuration required
	▪ Precise voltage, current temperature, and aging compensation
	▪ Complete battery cycling is not required to maintain accuracy
	▪ Missing battery detection
	▪ One-time programmable (OTP) for default, nonvolatile settings
	▪ Supports multiple battery profiles

BIF (BSI) support	BIF support for MIPI-BIF enabled battery packs via the BATT_ID pin
General housekeeping	
On-chip ADC	Housekeeping (HK) ADC supports internal and external (via MPPs) monitoring
Internal clocks	Internal 19.2 MHz clock on PMI8937
Overtemperature protection	Multistage smart thermal control
Programmable boot sequence	Programmable boot sequence (PBS) with OTP memory and user programmable RAM

PMI8937/PMI8940 Features (3 of 5)

Feature	PMI8937/PMI8940 capability
User interfaces	
Display bias supplies (applicable only for PMI8940)	Dual synchronous SMPS topology: Boost and inverting buck-boost ▪ Supports thin film transistor LCD (TFT-LCD) ▪ 86% efficiency converters for both rails with a compact BOM ▪ 2.5 V to 4.75 V input voltage range ▪ Independently programmable positive and negative output voltages ▪ Programmable output voltage range of ±4.6 V to ±6.0 V (default = ±5.5 V) ▪ 100 mV resolution on both bias rails ▪ 150 mA output current capability on both supplies ▪ Auto output disconnect and active discharge on module shutdown ▪ Short circuit protection and auto power sequencing on module enable/disable ▪ Antiringing compensation on both rails
White LED (WLED) backlighting	Switched-mode boost supply to adaptively boost voltage for series WLEDs plus four regulated current sinks ▪ Two LED strings of up to 30 mA each, configurable in 2.5 mA steps ▪ 28 V maximum boost voltage ▪ Hybrid dimming mode (analog dimming at high LED currents, digital dimming for low currents) ▪ 12-bit analog dimming; 9bit digital dimming ▪ Each current sink can be independently controlled via a combination of the brightness control register, full scale current setting register, and an external content adaptive backlight control (CABC) pulse width modulation (PWM) input ▪ 85% efficiency under typical conditions and 15 mA per string ▪ High efficiency always-on mode ▪ Light load efficiency mode

PMI8937/PMI8940 Features (4 of 5)

Feature	PMI8937/PMI8940 capability
User interfaces (cont.)	
Flash/torch drivers	Two independent high-side current sources for driving LEDs ▪ Up to 1.0 A per channel for flash (up to 200 mA for torch) ▪ Flexible to support one LED or two LEDs with 2.0 A maximum current ▪ Fully programmable LED currents (0 A~1.0 A per LED, with 12.5 mA/step) ▪ PWM dimming at current set at ≤ 100 mA ▪ Current ramp up/down control (programmable ramp rate) ▪ Current mask upon Tx_GTR_THRESH input (over SPMI) ▪ Thermal current derating ▪ Short/open circuit detection ▪ Max-on safety timer, watchdog timer, and thermal shutdown safety
Haptics driver	One full H-bridge power stage for driving haptics ▪ Bidirectional drive capability with support for active braking ▪ Support for eccentric rotating machines (ERM) and linear resonant actuators (LRA) ▪ Programmable internal PWM frequency from 250–1000 kHz in ~250 kHz steps ▪ Programmable LRA frequency from 50 Hz to 300 Hz, with a 0.5 Hz tuning resolution ▪ 5-bit output control from 0 V to Vmax; Vmax configurable from 1.2 V–3.6 V in 116 mV steps ▪ Support for internal 8bit LUT to store haptics pattern, repeat, and loop ▪ Dual PWM for double the effective switching frequency ▪ Automatic resonance tracking ▪ External input for audio/PWM mode support ▪ Short circuit detection and current limit protection ▪ Supports fixed DC output for simple vibration patterns
Other current sinks	▪ Charging indicator ▪ Two MPP can function as current sink ▪ Support for up to 40 mA current in 5 mA steps; ±20% accuracy

PMI8937/PMI8940 Features (5 of 5)

Feature	PMI8937/PMI8940 capability
IC-level interfaces	
Primary status and control	Two-line serial power management interface (MIPI SPMI)
Interrupt managers	Supported by SPMI
BUA	Battery UICC alarm for graceful shutdown to prevent corruption of UICC on a battery disconnection event
BIF	BIF support for MIPI-BIF enabled battery packs via the BAT_ID pin
Configurable I/Os	
MPPs	Three MPPS, all configurable as digital inputs, digital outputs, one as analog multiplexer inputs; two configurable as current sinks; one configurable as analog output
Fabrication technology and package	
Fabrication technology	Mixed-signal BiCMOS
Size	5.11 × 4.77 × 0.55 mm
Type and pin count	144-pin wafer-level nanoscale package (144 WLNSP)

PM8937/PM8940 Features (1 of 4)

Feature	PM8937/PM8940 capability
Input power management	
Coin cell or capacitor backup	Keep-alive power source; orchestrated charging
VPH_PWR detector	Validates primary VPH_PWR input voltage
Output power management	
Switched mode power supplies S1 S2, S5, S6 S3 S4	 ▪ Rated for 2.0 A **Note:** S1 SMPS rated current increased to 3000 mA on PM8940 to support CAT6 modem. ▪ Rated for 3.0 A each ▪ Rated for 2.7 A ▪ Rated for 2.5 A
Low-dropout linear regulators	23 total – eight different design types ▪ Four 1200 mA NMOS ▪ One 300 mA NMOS ▪ Four 600 mA PMOS ▪ One 450 mA PMOS ▪ Three 300 mA PMOS ▪ Four 150 mA PMOS ▪ Four 50 mA PMOS ▪ Two for clocks
Pseudocapless low dropout (LDO) designs	13 of 23 LDOs
LP DDR memory support	Voltage reference source

PM8937/PM8940 Features (2 of 4)

Feature	PM8937/PM8940 capability
General housekeeping	
On-chip ADC	Shared housekeeping (HK) and XO support
Analog multiplexing for ADC	▪ HK inputs – many internal nodes and external inputs, including configurable MPPs ▪ XO input – dedicated pins for XO_THERM and PA_THERM
Overtemperature protection	Multistage smart thermal control
19.2 MHz oscillator support	XO (with on-chip ADC)
XO controller and XO output	Five sets: two low-noises (RF), two low-power basebands (BB), and one low-noise BB output
Special purpose clock outputs	▪ Sleep clock; 19.2, 9.6, 4.8, 2.4, and 1.2 MHz, including low-power mode ▪ 2.4 MHz for MP3; four high-speed GPIOs for fast clocks
Real-time clock	RTC clock circuits and alarms
IC infrastructure circuits	Bandgap voltage reference and LDO for analog circuits
IC-level interfaces	
Primary status and control	Two-line SPMI
Interrupt managers	Supported by SPMI
Optional hardware configurations	OPT bits select hardware configuration
Power sequencing	Power on, power off, and soft resets

PM8937/PM8940 Features (3 of 4)

Feature	PM8937/PM8940 capability
Audio codec	
Audio inputs	▪ Two single-ended and one differential capless input with programmable input gain (0 dB to 24 dB gain in 6 dB increments and additional 21 dB gain) ▪ 5.5 µVrms input referred noise, 97 dB SNR, and -87 THD at 12 dB gain ▪ Integrated IEC ESD protection on microphone 2 input ▪ Two ADCs
Multibutton headset control	▪ Mechanical plug insertion and removal detection with either tip or both tip and ground detection pins while minimizing PoP noise ▪ Accessory plug type (3-pole or 4-pole: CTIA or OMTP) detection ▪ Detection for up to five buttons (send/end, volume, and play control) ▪ Headphone impedance detection
Audio outputs	▪ Four outputs: • Class-AB earpiece amplifier; o 125 mW into 32 Ω; 150 mW (minimum) into 16 Ω or 10.67 Ω • Stereo Class-AB headphone amplifier; capless; 16 Ω or 32 Ω o 1 Vrms; 106 dB dynamic range, -90 dB THD+N, and 140 µVpp click and PoP into 16 Ω • Mono Class-D mono speaker driver; 4 Ω or 8 Ω o 1.43 W into 8Ω with VDD_SPKR = 5 V and 1% THD+N ▪ Three DACs ▪ Overcurrent protection and click-and-pop suppression on HPH, EAR, and speaker outputs ▪ Shared transducer for earpiece and loudspeaker
Multiple audio I/O sample rates	Supports 8, 16, 32, and 48 kHz sample rates
Audio-specific power supplies	▪ +5 V boost SMPS to supply speaker driver for higher output power ▪ Negative charge pump for HPH negative supply
Microphone biasing	▪ Two outputs sharing one voltage source for powering analog or digital microphones ▪ Internal bias resistor for analog ECM type microphone ▪ Programmable from 1.6 V to 2.85 V, in 50 mV steps

PM8937/PM8940 Features (4 of 4)

Feature	PM8937/PM8940 capability
Configurable I/Os	
MPPs	Four; configurable as digital in/out; level-translating bidirectional I/Os; analog multiplexer inputs; current sinks; VREF buffer outputs; MPP_01 and MPP_03 are fixed for VDD_PX_BIAS and VREF_DAC, respectively
GPIO pins	Eight; configurable as digital inputs or outputs or level-translating I/Os; all are faster than MPPs
Audio interface	PDM interface to MSM8937 digital audio circuits (decimator and interpolator)
Fabrication technology and package	
Fab	0.18 µm HV CMOS
Size	5.78 × 5.78 × 0.65 mm
Pin count and package type	183-pin fan-out wafer nanoscale package (183 FOWNSP)

PMI8937 Keypad Groupings

1 NC	2 NC	3 VPH_ PWR	4 GNDC	5 NC	6 VREG_ WLED	7 VDD_ WLED	8 GND_ WLED	9 VSW_ WLED	10 NC	11 HAP_ PWM_IN	12 HAP_ PWM_IN
13 NC	14 NC	15 NC	16 NC	17 NC	18 NC	19 NC	20 WLED_ SINK2	21 WLED_ SINK1	22 MPP_1	23 GNDC	24 HAP_ OUT_N
25 VBIAS_1P8	26 GNDC	27 NC	28 VPH_ PWR	29 NC	30 WLED_ CABC	31 GND_ WLED_I	32 NC	33 NC	34 MPP_2	35 HAP_ OUT_P	36 GND_ HAP
37 GNDC	38 SPMI_ CLK	39 SPMI_ DATA	40 NC	41 NC	42 VDD_ MSM_IO	43 BUA	44 NC	45 GNDC	46 VREG_ ADC_LDO	47 MPP_4	48 VDD_ HAP
49 GNDC	50 CLK_IN	51 NC	52 GNDC	53 AVDD _BYP	54 DVDD _BYP	55 SHDN_N	56 GNDC	57 VDD_ ADC_LDO	58 REF_ BYP	59 GND_ REF	60 VDD_ TORCH
61 CS_ PLUS	62 BATT_ PLUS	63 NC	64 GNDC	65 GNDC	66 GNDC	67 GNDC	68 RESIN_N	69 PS_HOLD	70 GNDC	71 FLASH _LED1	72 VDD_ FLASH
73 CS_ MINUS	74 BATT_ MINUS	75 NC	76 GNDC	77 GNDC	78 GNDC	79 GNDC	80 USB_ID	81 GNDC	82 GNDC	83 FLASH _LED2	84 VDD_ FLASH
85 R_BIAS	86 BATT_ID	87 GNDC	88 NC	89 NC	90 USB_ID _RVAL1	91 CHG_LED	92 USB_SNS	93 SYSON	94 FLASH _OUT	95 FLASH _OUT	96 FLASH _OUT
97 BATT_ THERM	98 VAA_ CAP	99 GNDC	100 NC	101 USB_CS	102 CHG_EN	103 PGOOD _SYSOK	104 NC	105 BOOT_ CAP	106 VSW_ CHG	107 VSW_ CHG	108 VSW_ CHG
109 GNDC	110 GND_FG	111 USB_DP	112 USB_ID _RVAL2	113 CHG_OUT	114 VPH_ PWR	115 GNDC	116 VSW_ CHG	117 VSW_ CHG	118 VSW_ CHG	119 VSW_ CHG	120 VSW_ CHG
121 GNDC	122 GND_ REF_CHG	123 USB_DM	124 CHG_ VBAT _SNS	125 CHG_OUT	126 CHG_OUT	127 VPH_ PWR	128 GND_ CHG	129 GND_ CHG	130 USB_ MID	131 USB_ MID	132 USB_ MID
133 GNDC	134 KYPD_ PWR_N	135 V_ARB	136 GNDC	137 CHG_OUT	138 VPH_ PWR	139 VPH_ PWR	140 NC	141 GND_ CHG	142 USB_IN	143 USB_IN	144 USB_IN

Configurable IOs	General housekeeping	Ground	IC-level interfaces	Input power management	No connect	Power	User interfaces

PMI8940 Keypad Groupings

1 VDIS_N_OUT	2 VSW_DIS_N	3 VDD_DIS_N	4 GND_DIS_P	5 VDIS_P_OUT	6 VREG_WLED	7 VDD_WLED	8 GND_WLED	9 VSW_WLED	10 NC	11 HAP_PWM_IN	12 HAP_PWM_IN
13 VDIS_N_OUT	14 VSW_DIS_N	15 DIS_N_CAP_REF	16 VSW_DIS_P	17 VSW_DIS_P	18 NC	19 NC	20 WLED_SINK2	21 WLED_SINK1	22 MPP_1	23 GNDC	24 HAP_OUT_N
25 VDD_1P8_DIS_N	26 GND_DIS_N_REF	27 VDIS_N_FB	28 VDD_DIS_P	29 VDIS_P_FB	30 WLED_CABC	31 GND_WLED_I	32 NC	33 NC	34 MPP_2	35 HAP_OUT_P	36 GND_HAP
37 GNDC	38 SPMI_CLK	39 SPMI_DATA	40 NC	41 NC	42 VDD_MSM_IO	43 BUA	44 NC	45 GNDC	46 VREG_ADC_LDO	47 MPP_4	48 VDD_HAP
49 GNDC	50 CLK_IN	51 DIS_SCTRL	52 GNDC	53 AVDD_BYP	54 DVDD_BYP	55 SHDN_N	56 GNDC	57 VDD_ADC_LDO	58 REF_BYP	59 GND_REF	60 VDD_TORCH
61 CS_PLUS	62 BATT_PLUS	63 NC	64 GNDC	65 GNDC	66 GNDC	67 GNDC	68 RESIN_N	69 PS_HOLD	70 GNDC	71 FLASH_LED1	72 VDD_FLASH
73 CS_MINUS	74 BATT_MINUS	75 NC	76 GNDC	77 GNDC	78 GNDC	79 GNDC	80 USB_ID	81 GNDC	82 GNDC	83 FLASH_LED2	84 VDD_FLASH
85 R_BIAS	86 BATT_ID	87 GNDC	88 NC	89 NC	90 USB_ID_RVAL1	91 CHG_LED	92 USB_SNS	93 SYSON	94 FLASH_OUT	95 FLASH_OUT	96 FLASH_OUT
97 BATT_THERM	98 VAA_CAP	99 GNDC	100 NC	101 USB_CS	102 CHG_EN	103 PGOOD_SYSOK	104 NC	105 BOOT_CAP	106 VSW_CHG	107 VSW_CHG	108 VSW_CHG
109 GNDC	110 GND_FG	111 USB_DP	112 USB_ID_RVAL2	113 CHG_OUT	114 VPH_PWR	115 GNDC	116 VSW_CHG	117 VSW_CHG	118 VSW_CHG	119 VSW_CHG	120 VSW_CHG
121 GNDC	122 GND_REF_CHG	123 USB_DM	124 CHG_VBAT_SNS	125 CHG_OUT	126 CHG_OUT	127 VPH_PWR	128 GND_CHG	129 GND_CHG	130 USB_MID	131 USB_MID	132 USB_MID
133 GNDC	134 KYPD_PWR_N	135 V_ARB	136 GNDC	137 CHG_OUT	138 VPH_PWR	139 VPH_PWR	140 NC	141 GND_CHG	142 USB_IN	143 USB_IN	144 USB_IN

Configurable IOs	General Housekeeping	Ground	IC-level Interfaces	Input Power Management	No Connect	Power	User Interfaces

PM8937/PM8940 Keypad Groupings

1 GND_ XO_ISO	2 XTAL_19M_O UT	3 XTAL_19M_I N		4 VREG_XO	5 VREG_RFCL K		6 BB_CLK1	7 VREG_L22		8 VREG_L16	9 VDD_S4	10 VSW_S4	11 GND_S4
12 VREG_L18	13 GND_ XO_ISO	14 GND_XO	15 GND_RFCLK	16 VDD_XO_RF CLK	17 VDD_L9_10_1 3_14_15_18	18 VREG_L11	19 VDD_L8_11_1 _17_22	20 VREG_L4	21 VREG_L5	22 GPIO_01	23 VSW_S4	24 GND_S4	25 GPIO_06
26 BB_CLK1_EN	27 VREG_L14	28 VDD_L9_10_1 3_14_15_18	29 VREG_L13	30 VREG_L9	31 VDD_L9_10_1 3_14_15_18	32 VREG_L10	33 VDD_L8_11_1 _17_22	34 VDD_L4_5_6 _7_16_VREG_ S4	35 VDD_L4_5_6 _7_16_VREG_ S4	36 GPIO_04	37 VSW_S4	38 GPIO_02	39 VDD_S1
	40 RF_CLK2	41 VREG_L15	42 RF_CLK1	43 LN_BB_CLK	44 BB_CLK2	45 VREG_L17	46 VDD_L8_11_1 _17_22	47 VREG_L8	48 VREG_L7	49 GPIO_05	50 GPIO_3	51 VSW_S1	52 VSW_S1
53 HPH_REF	54 HPH_L	55 HPH_R	56 MIC1_IN_P	57 GND	58 GND_REF	59 REF_BYP	60 VREG_L12	61 VREG_L6	62 SPMI_DATA	63 VPH_PWR	64 VREG_S1	65 GND_S1	66 GND_S1
67 VDD_HPH		68 VNEG_HPH	69 MIC1_IN_M	70 GND_CFILT	71 GND	72 GND	73 GND	74 SLEEP_CLK1	75 SPMI_CLK	76 DNC	77 VDD_S2	78 VDD_S2	79 VDD_S2
		80 HS_DET	81 GND	82 MIC_BIAS1	83 GND	84 GND	85 NC_WLP_TS T1	86 GND	87 OPT_1	88 VREG_S2	89 MPP_04	90 VSW_S2	91 VSW_S2
92 EARO_P	93 EARO_M	94 VDD_SPKR_ PA	95 MIC3_IN	96 MIC_BIAS2	97 GND	98 GND	99 GND	100 GND	101 VREG_S6	102 KYPD_PWR_ N	103 GND_S2	104 GND_S2	105 GND_S2
	106 SPKR_DRV_ P	107 SPKR_DRV_ M	108 MIC2_IN	109 GND_XOAD C	110 GND	111 VDD_L1_19	112 VREG_L23	113 VREF_NEG_ S6	114 GND	115 CBL_PWR_N	116 VREG_S5	117 VDD_L3	118 VREG_L3
119 XO_THERM	120 GND_SPKR_ PA	121 SPKR_DRV_ M	122 PA_THERM	123 VREF_LPDD R	124 VREG_L1	125 VDD_L1_19	126 VREG_L19	127 AVDD_BYP	128 RESIN_N	129 PS_HOLD	130 VREF_NEG_ S5	131 MPP_03	
132 VCOIN	133 CP_C1_M	134 CP_VNEG	135 BOOST_SNS	136 NC_3	137 MPP_01	138 NC_2	139 VDD_L2_23_ VREG_S3	140 VREG_L2	141 GPIO_07	142 NC_1	143 PON_1	144 GND_S5	145 GND_S5
146 GND_CP	147 CP_C1_P	148 VDD_CP	149 PDM_TX	150 PDM_RX0	151 MPP_02	152 GPIO_08	153 VSW_S3	154 GND_S3		155 VSW_S6	156 VDD_S5	157 VSW_S5	158 VSW_S5
159 PDM_RX2	160 GND_BOOST	161 VSW_BOOST	162 VREG_BOOS T	163 VDD_AUDIO_ IO		164 VDD_S3	165 VSW_S3	166 GND_S3	167 VDD_S6	168 VSW_S6	169 GND_S6	170 VDD_S5	171 GND_S5
172 GND_BOOST	173 PDM_RX1	174 PDM_CLK		175 PDM_SYNC		176 VDD_S3	177 VSW_S3	178 GND_S3	179 VDD_S6	180 VSW_S6	181 GND_S6	182 PON_RESET _N	183 VDD_S5

Audio	Configurable IOs	Do not connect	General housekeeping	Ground	IC-level interfaces	Input power management	Output power management	Power

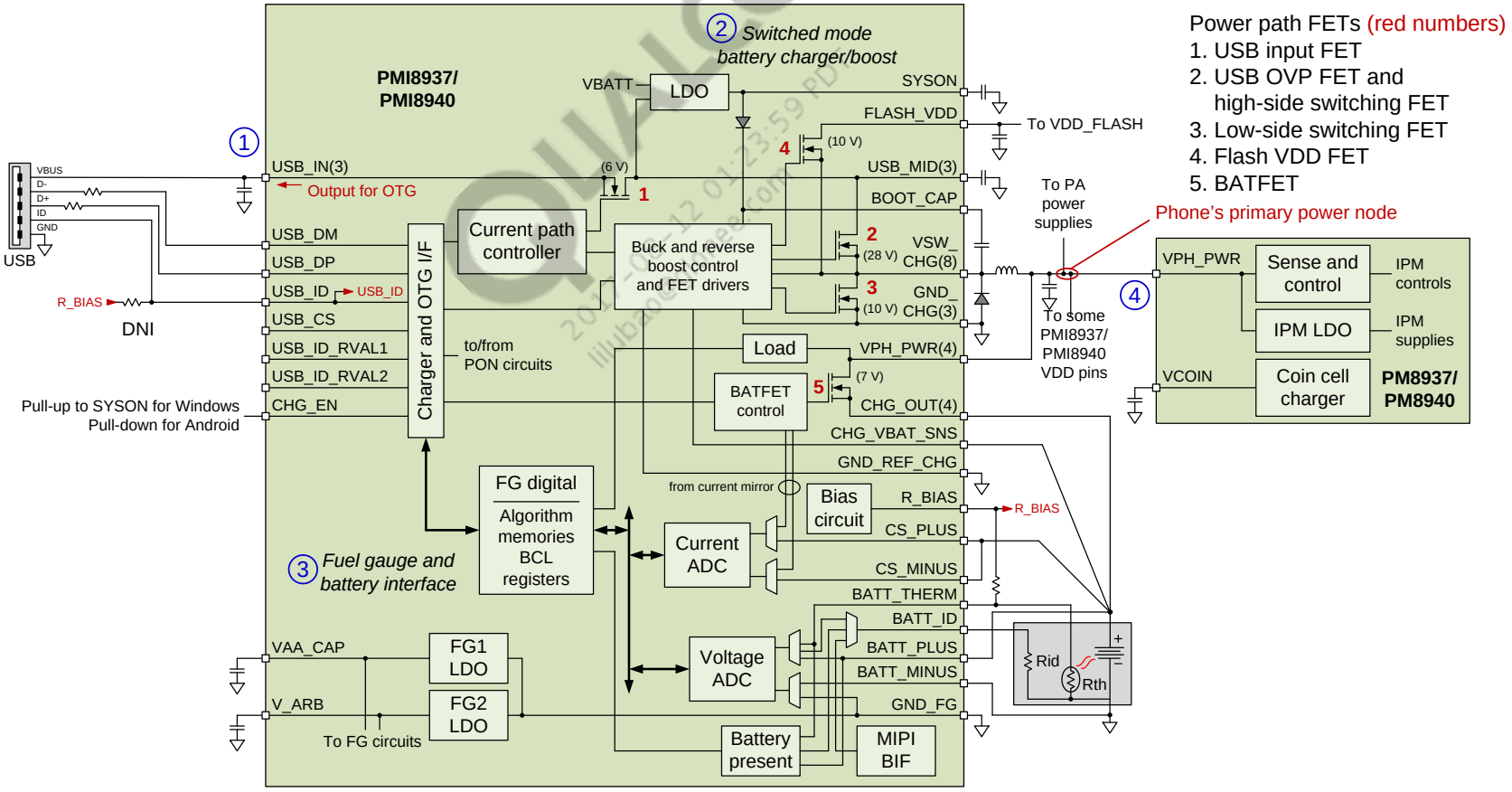
Section 2

Input Power Management

Input Power Management

Input power management topics are highlighted in blue:

1. PMI input power sources, selection, and protection
2. PMI8937/PMI8940 SCHG and battery charging
3. PMI8937/PMI8940 fuel gauge and battery interface
4. PM8937/PM8940 VPH_PWR input and coin cell

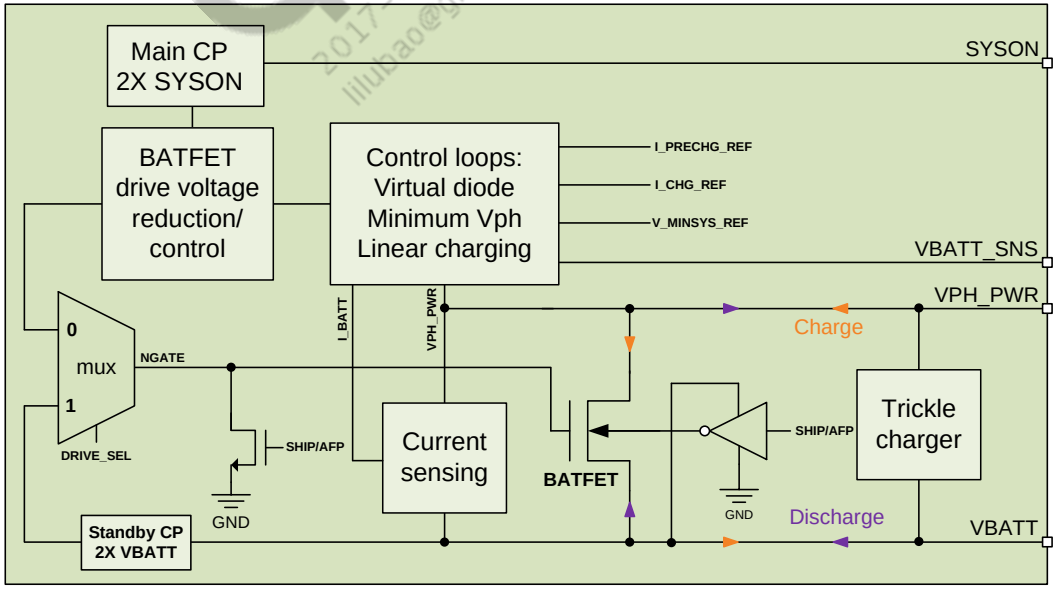


SCHG Feature Summary

- Autonomous charging – requires no software involvement for trickle charge, precharge, fast charge, taper-charge, or charge termination
- Efficient battery charging removes heat issues
- Charging current – up to 1.5 A for PMI8937 and 2 A for PMI8940
- Automatic input current limit for universal USB/AC/DC adapter compatibility
- Optional automatic power source detection per USB charging specification 1.2
- Programmable input current limiting (USB 2.0/3.0 compliant)
- Up to 750 mA charging output from 500 mA USB port using the TurboCharge™ mode
- Input/output current path control allows system operation with deeply discharged/missing battery
- USB OTG power support (1 A at +5.0 V)
- JEITA and JISC 8714 support
- 1 MHz switching allows tiny external components
- Real-time input current measurement with VDIR_CHG
- 4 V–7.2 V operating input voltage range
- +28 V input voltage tolerance (nonoperating) with overvoltage protection
- Digital programming of all major parameters via SPMI
- Comprehensive protection features

Battery FET Architecture

- If the battery voltage is above the minimum system voltage, the BATFET fully turns on, and only charging or discharging current is sensed by the BATFET control logic.
- If the battery voltage is between 0 V – 2.1 V, the battery is disconnected from the system. A 45 mA current source is turned on, which charges the battery up to 2.1 V.
  - When the SHIP/AFP signal is high in the figure below, BATFET gate and back gate both are connected to GND. This reverses the direction of the body diode and prevents conduction from VBATT to VPH_PWR. This is used only in ship mode and AFP mode to prevent any power from being provided to the system through the BATFET. In normal power off mode, VPH_PWR is still connected to VBATT through body diode of BATFET.
- During precharge and constant-current mode (fast-charge) charging, both the VSYS_MIN and ICHG loops are active at the same time. The VSYS_MIN loop maintains VPH_PWR to VSYS_MIN voltage until VBATT reaches VSYS_MIN and the ICHG loop controls the charge current to the battery.
- If the system load is high enough and requires the battery to supplement the load, the virtual diode kicks in and regulates the system voltage ~50 mV below the battery voltage. This is called supplemental mode. Refer to the CurrentPath control section for more information on supplemental mode.
- The main charge pump is powered from the SYSON supply and has a gain of 2X. A protection mechanism exists and clamps the charge-pump voltage to a maximum of VBATT + 5 V.
- When running on battery only, the standby charge pump is used to save power. One exception to this is OTG mode, which uses the main charge pump.



Section 2.1

USB Input

Section 2.1.1

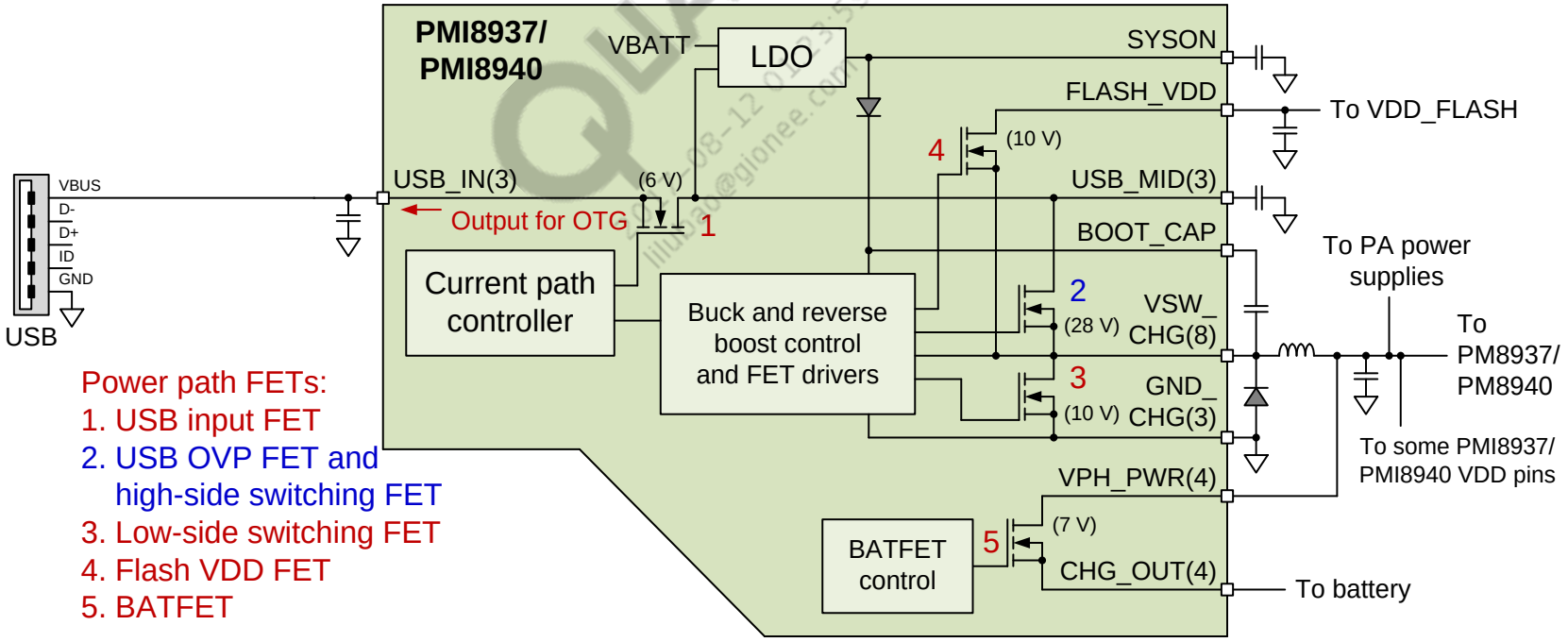
Input Power Sources and Protection

Input Power Comments

- Power source detection uses D+ and D- signaling to determine how much current is allowed to be drawn from an upstream USB port and adjust the input current limit levels accordingly as discussed on the *USB Automatic Power Source Detection* slide.
- Input voltage bias
  - A 50 mA (minimum) automatic prebias current allows loosely regulated power sources to be used for battery charging
  - Such power sources (wall adapters, wireless pads, etc.) cannot be preloaded to reduce quiescent current when an external load is not present
  - Prebias is enabled when: 1) input power is present at USB_IN, and 2) the feature is enabled by its configuration register
- Soft start
  - Soft start control provides a smooth input voltage ramp-up and reduces input current and voltage transients
  - It is active anytime the input power transitions to a new state: 1) initial input power, 2) input current limit changes (like USB1 to USB5) and others
- Bad adapter insertion
  - To prevent the acceptance of a bad adapter being inserted, an input is only considered present and valid if it has remained above the UVLO and below the OVLO level for a minimum of 30 ms
  - A register and/or an output pin can indicate this status

USB Power Source and OVP – Architecture and Schematic

- The PMI8937/PMI8940 device supports USB source only without parallel charging – connect VBUS directly to USB_IN and USB_SNS; 4.7 µF USB_IN capacitor.
- The USB_MID node may be exposed to the same voltage level as the USB_IN input (up to 1.5 A for PMI8937 and 2A for PMI8940, 4.5 V–7.2 V input range, 28 V OVP).
- Illegal chargers are detected and rejected (for example, 50 Hz–60 Hz unfiltered, unregulated wall wart chargers).



SYSOK Operation

- SYSOK is the charger insertion PON trigger to PM (connected to PON1)

Notes:

- PGOOD_SYSOK signal is low if the charger module is in its shutdown state.
- Battery Missing is reported as true based on the logical OR of the battery missing detection (pin method) status and the V_lowbatt status.

Input source	SHDN_N	Battery voltage	Battery missing (pin method)	SYSOK output
Missing	Low	Don't care	Don't care	Low
Missing	High	< V_lowbatt	FALSE	Low
Missing	High	> V_lowbatt	FALSE	High
Missing	High	Don’t care	TRUE	Low
SDP500 or DCP/CDP/DC_IN; AICL ≥ 500 mA	Don't care	Don’t care	Don’t care	High
SDP100 or DCP/CDP; AICL < 500 mA	Don't care	< V_lowbatt	FALSE	Low
SDP100 or DCP/CDP; AICL < 500 mA	Don't care	> V_lowbatt	FALSE	High
SDP100 or DCP/CDP; AICL < 500 mA	Don't care	Don’t care	TRUE	Low

Section 2.1.2

USB Automatic Power Source Detection (APSD)

APSD

The SCHG is compatible with the *Battery Charging Specification Revisions 1.2* developed by the USB Implementers Forum (USB-IF). Its APSD algorithm determines how much current is allowed to be drawn from an upstream USB port and adjusts input current limit levels accordingly.

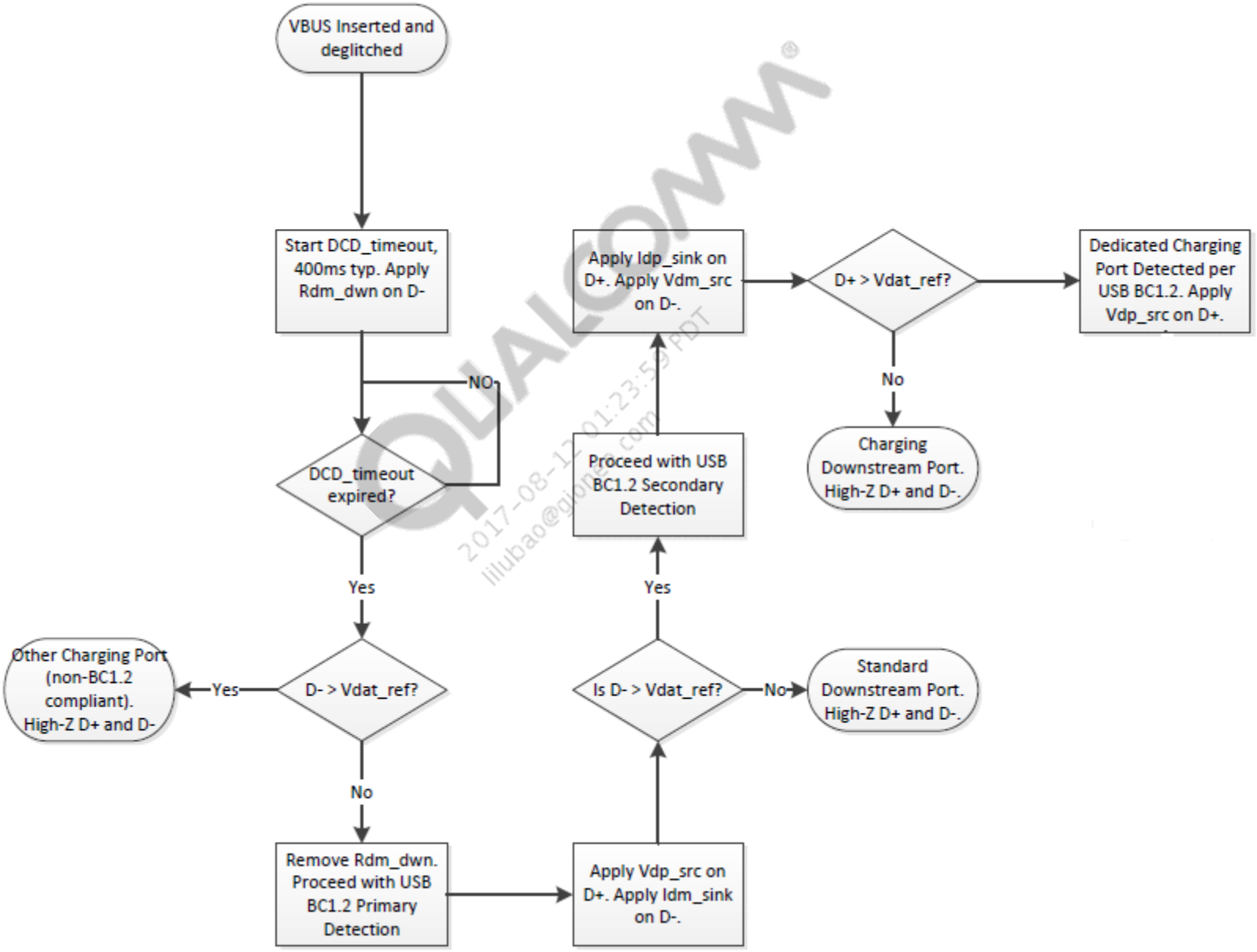
- The PMI8937/PMI8940 device automatically detects the type of adapter that is inserted in USBIN by performing D+ and D- lines to set an appropriate input current limit.
- The four power source types that are detected are:
  - Standard downstream port (SDP)
    - This is a computer USB port capable of USB 1.1 (100 mA), USB 2.0 (100/500 mA), or USB 3.0 (150/900 mA). D+ and D- are independently pulled down in the host with a 14.25 kΩ–24.8 kΩ resistance.
  - Charging downstream port (CDP)
    - This is typically a powered USB hub capable of 1.5 A.
  - Dedicated charging port (DCP)
    - This is a standard wall charger capable of at least 500 mA. D+ and D- are shorted in the wall adapter with a maximum resistance of 200 Ω. SCHG defaults to high current mode and runs automatic input current limiting (AICL).
  - Other charging port (not covered by USB charging specification 1.2)
    - This is a nonstandard charger with a proprietary D+/D- configuration. Typically, these chargers have similar current capability to normal DCPs. D+ and D- are connected to Vbus via a resistor divider, which causes them to be at specific fixed voltage levels.

USB APSD (1 of 3)

Operational details

- The algorithm begins as soon as VBUS voltage is detected and is independent of the charge enable status.
- A status register indicates the APSD algorithm results (power source type).
- Writing to the command register after power source detection has been completed does not reset the corresponding APSD status bit, but the current levels change.
- Input current limits change once the command register is written; before this, the input current limit is determined only by APSD results.
- When the APSD algorithm is completed, the D+ and D- signal lines of the PMI8937/PMI8940 device enters a Hi-Z state with ~ 4 pF of capacitive load.
- A write to the command register overrides the output of the source detection.
  - If source detection is enabled, the status of the source detection should be read each time before the command register is written to incorporate the source detection output into the command.
  - For example, if the source detection has determined that a dedicated charger is connected, the write to the command register should include setting the USB_IN current limit.
  - If the source detection status shows that the detection function is in progress, the system should poll the status until it is complete before issuing a command.
- When an SDP is detected with APSD, the default current limit is 500 mA, configured by register control. The USB_CS pin can be used to select the current limit if pin control is desired.

USB APSD (2 of 3)



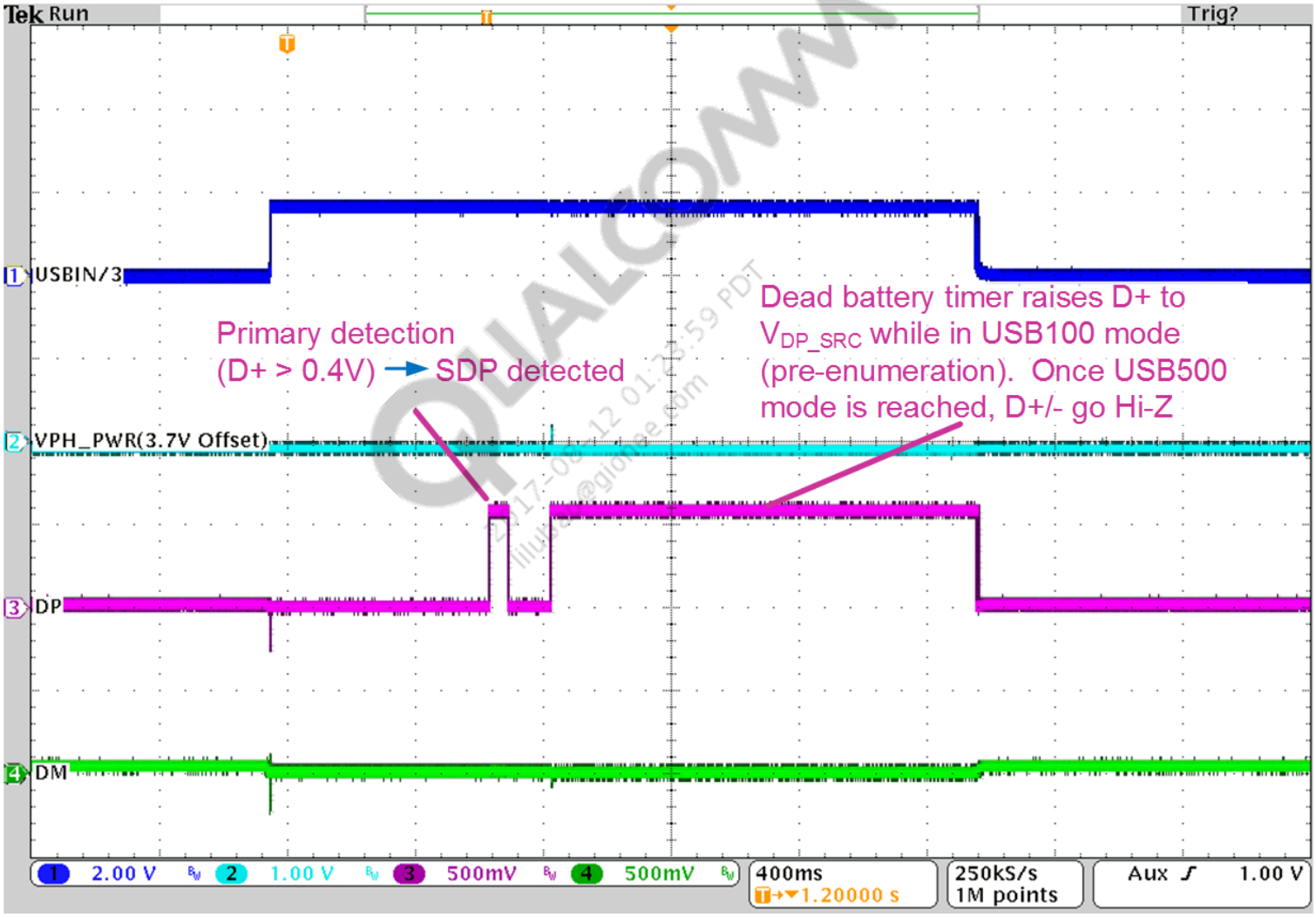
USB APSD (3 of 3)

Dead battery provision:

- An integrated 30-minute timer ensures that the portable device with a dead battery does not draw 100 mA indefinitely.
- The timer is active when USB_IN is present and a USB host is detected.
- The timer ends under the following conditions:
  - Suspend mode is entered
  - SPMI write command to register 33h
  - USB5/9 mode is selected
  - Power source is not an SDP
- During dead-battery charging, the SMBB also brings D+ high to +0.6 V to notify the host of its condition.

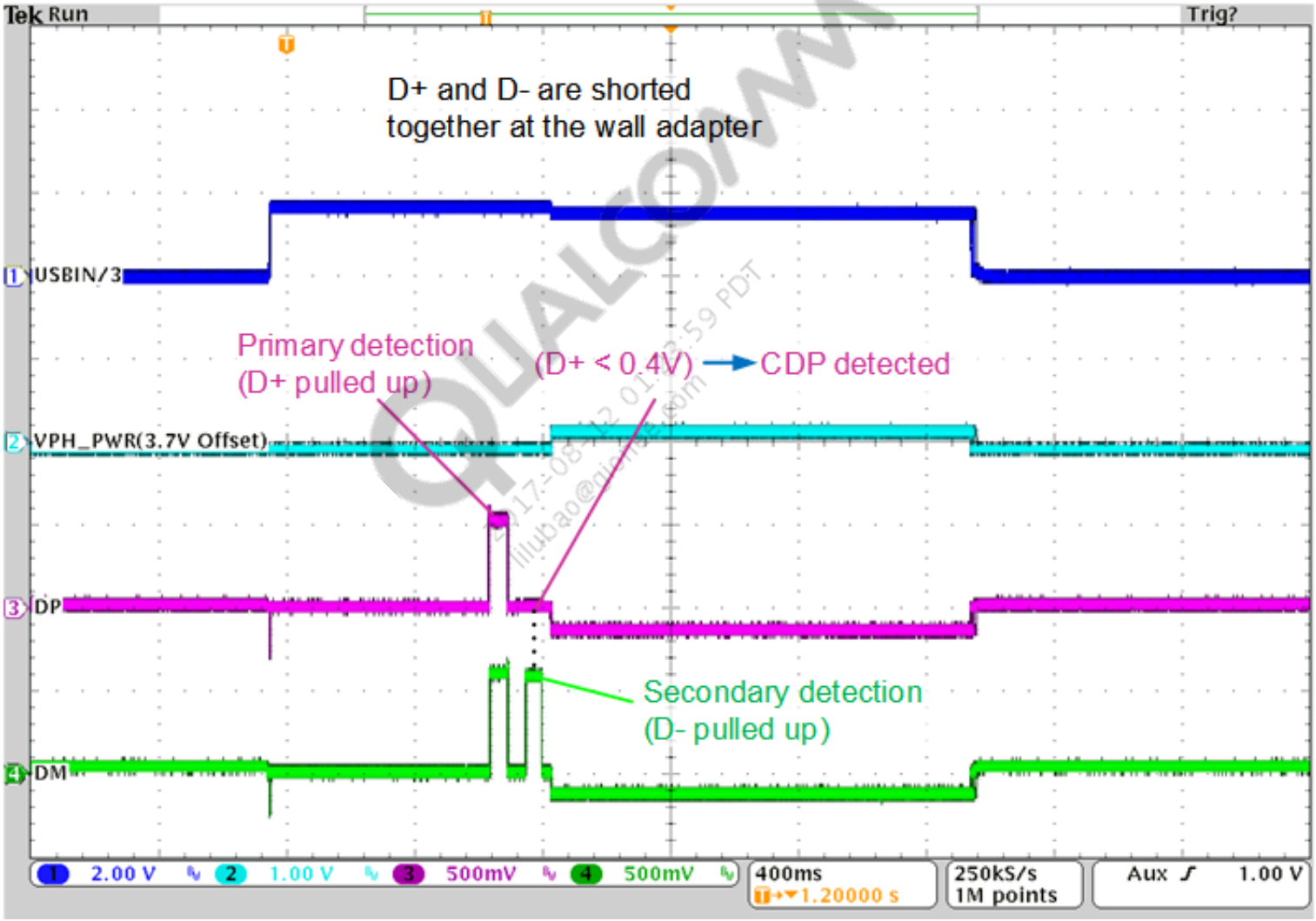
APSD Plots (1 of 4)

SDP – PMIC on, running from battery (VBAT = 3.7 V)



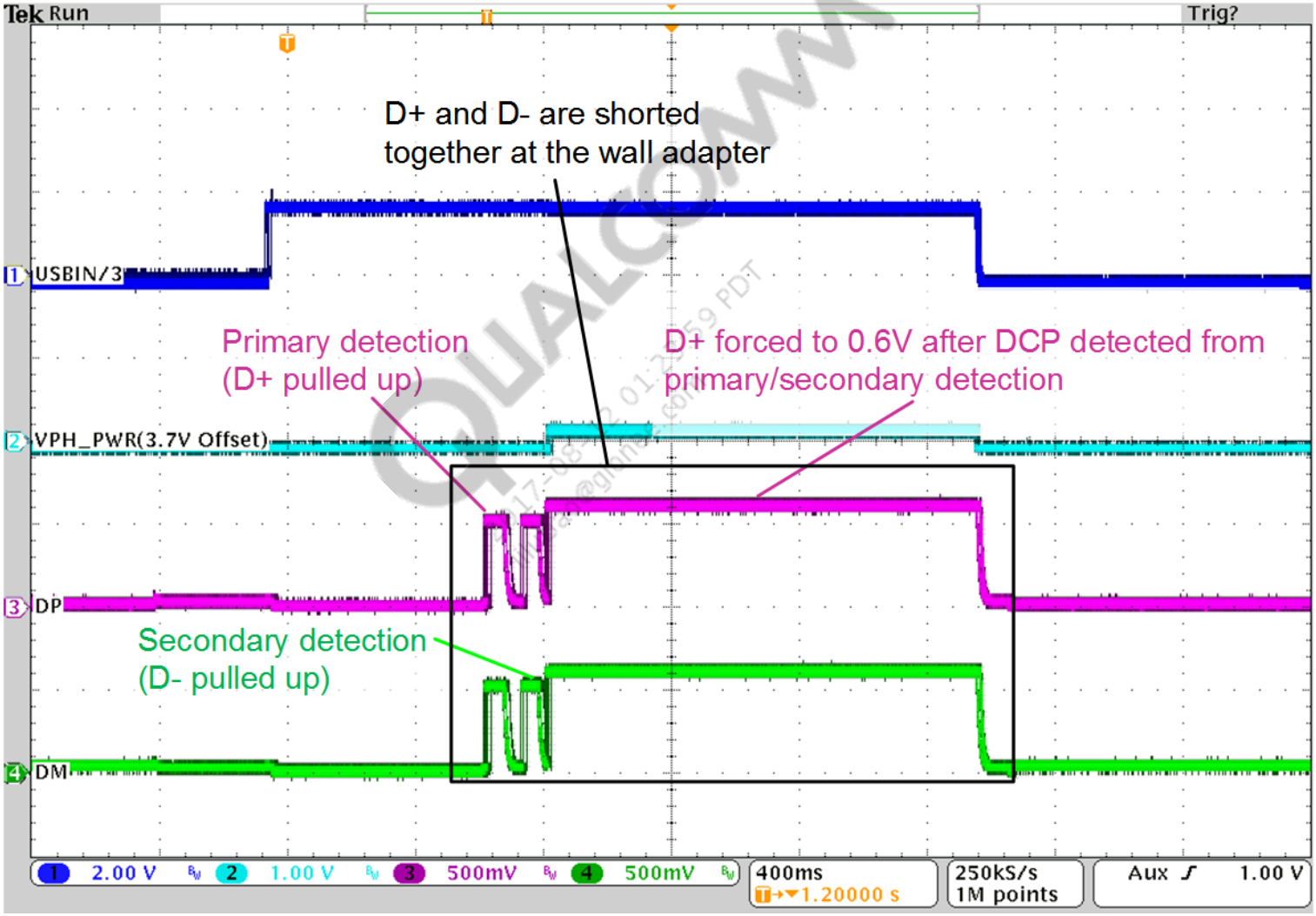
APSD Plots (2 of 4)

CDP – PMIC on, running from battery (VBAT = 3.7 V)



APSD Plots (3 of 4)

DCP – PMIC on, running from battery (VBAT = 3.7 V)



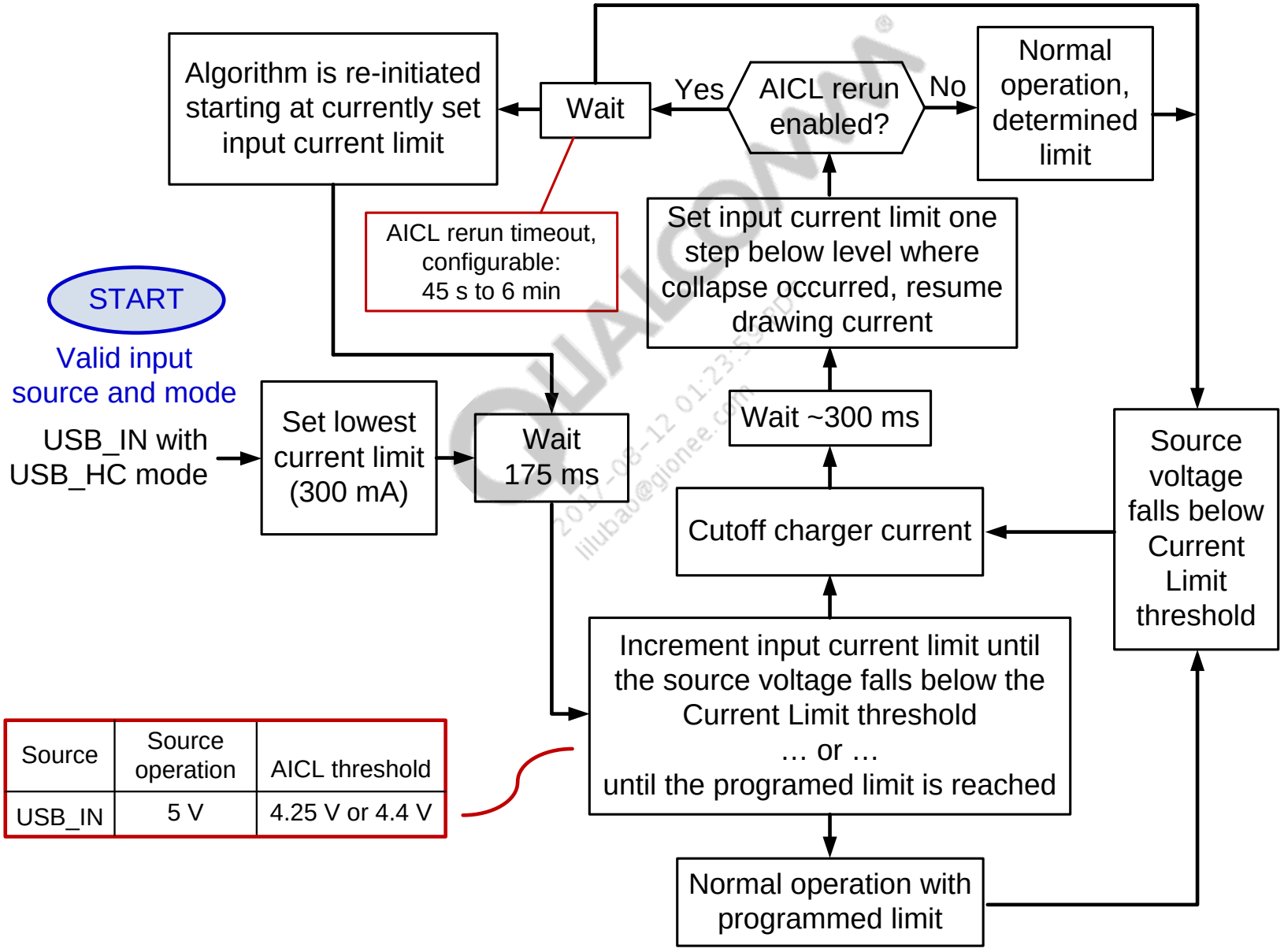
Section 2.1.3

AICL

AICL (1 of 2)

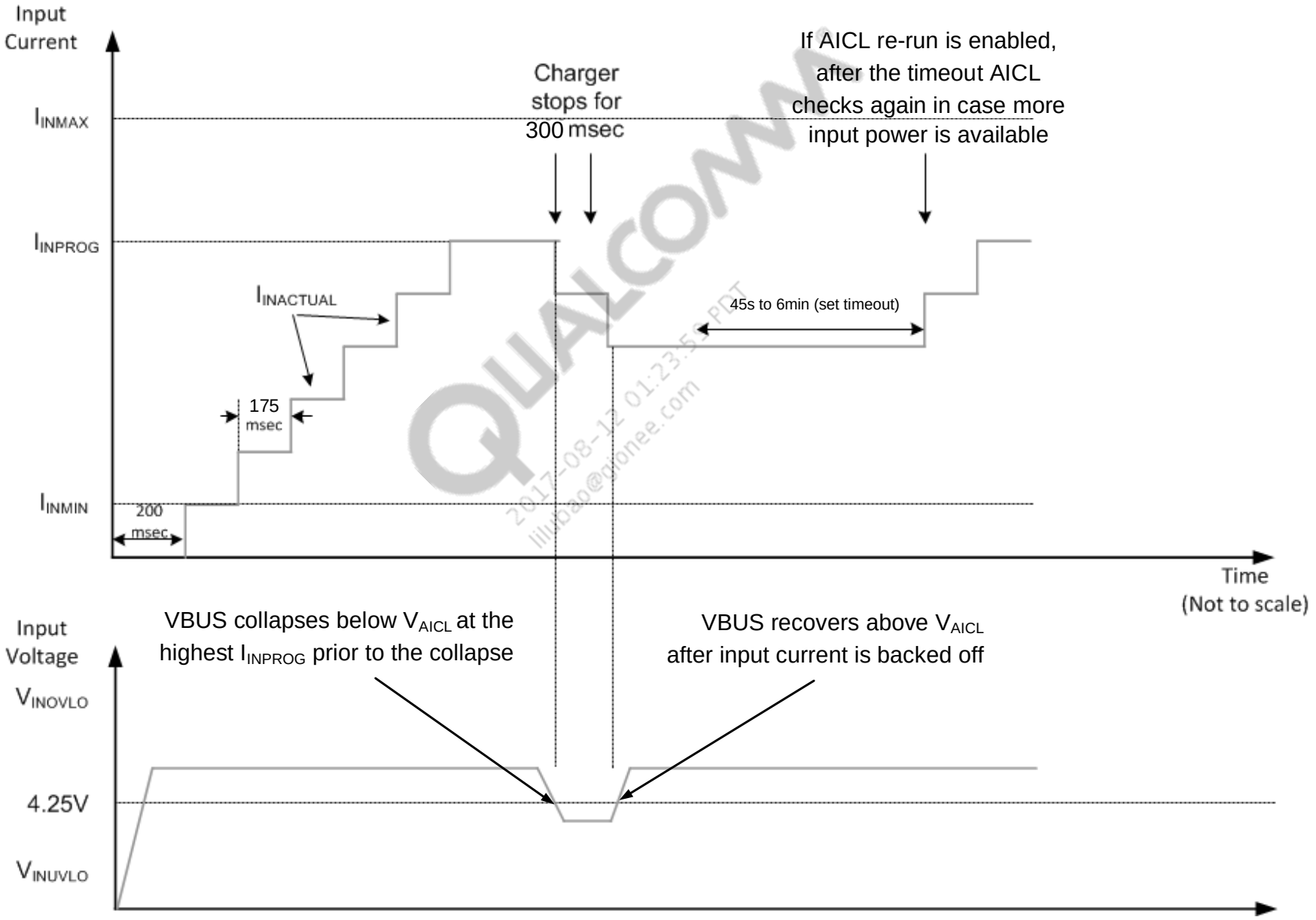
- AICL is an automatic and safe maximization of current from the USB input (only during the USBHC mode).
- The algorithm is only initiated for USBHC mode (default), but the feature can be disabled via register (0x13F3[2]).
- If AICL is enabled, four events can trigger the algorithm:
  - The AICL operation is running but not yet completed.
  - The AICL operation is completed, but the source voltage has collapsed (AICL did not find the true limit and the system load caused a collapse).
  - The current setting in a volatile register was updated with a value lower than the AICL setting.
  - The battery voltage rises above the automatic charger shutdown threshold; the AICL threshold is updated to the VBATT plus the automatic charger shut down threshold.
- If the algorithm must reduce the input current limit due to one of the above triggers, it decrements the input current limit setting until the source voltage is above the AICL threshold.
  - If the input voltage collapses at the lowest current limit setting (300 mA), the charger enters suspend.
  - The PMI8937/PMI8940 device has two AICL methods (selectable): discrete and continuous.
    - The continuous method (faster – default) uses a fast ramp and then uses an ADC reading to detect the input current limit.
    - The discrete method (slower) uses discrete incremental steps and checks the voltage at every step.
  - Both AICL methods are performed in hardware – minimal software is required.

AICL (2 of 2)

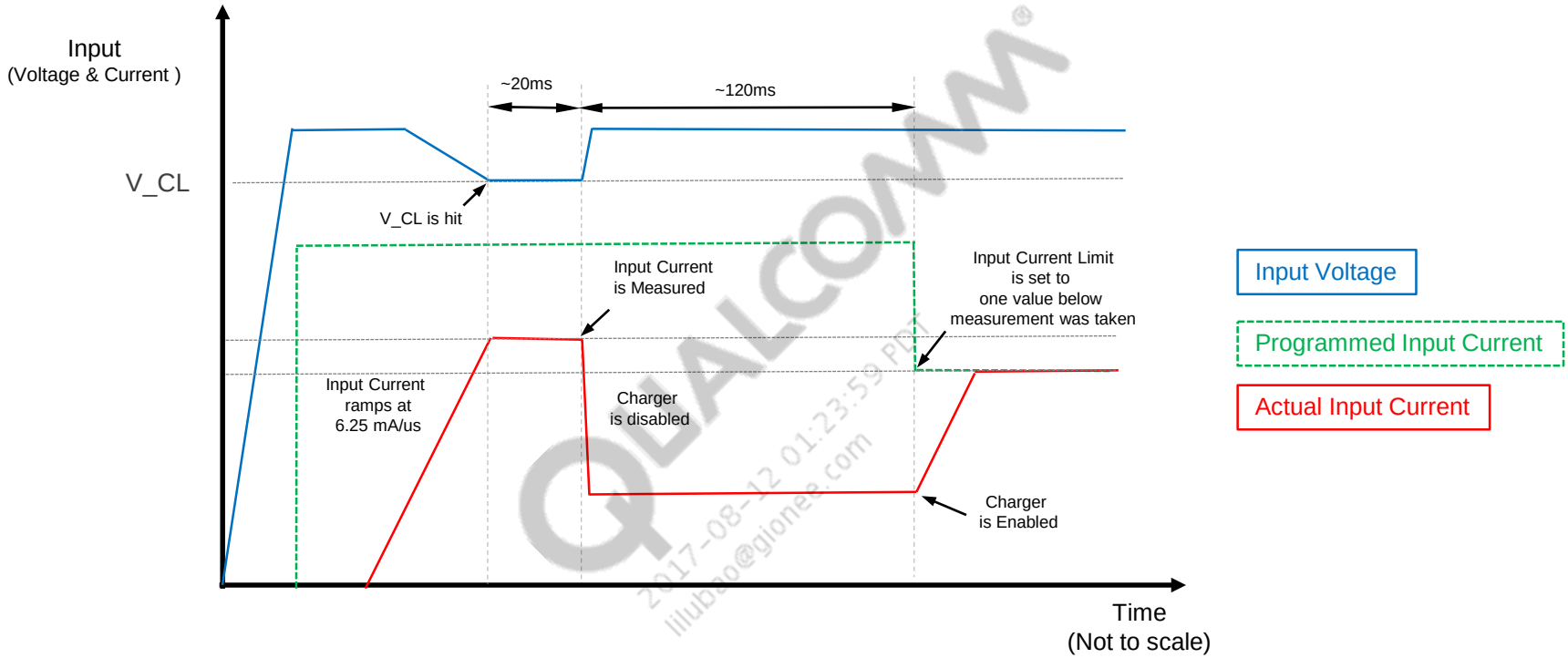


Source	Source operation	AICL threshold
USB_IN	5 V	4.25 V or 4.4 V

AICL Discrete Method



AICL Continuous Method



1. Input current ramps up in a continuous fashion at the rate of 6.25 mA/µs.
2. Once the input voltage at negative slope hits the V_CL threshold, after a deglitch time of about 20 ms, the input current is measured and the charger is disabled.*
3. Charger is kept disabled for about 120 ms before re-enabling.
4. The input current limit is set to one value below where the measurement was taken and charging is enabled.

* System current is not interrupted during the collapse event, since the charger buck stays enabled.

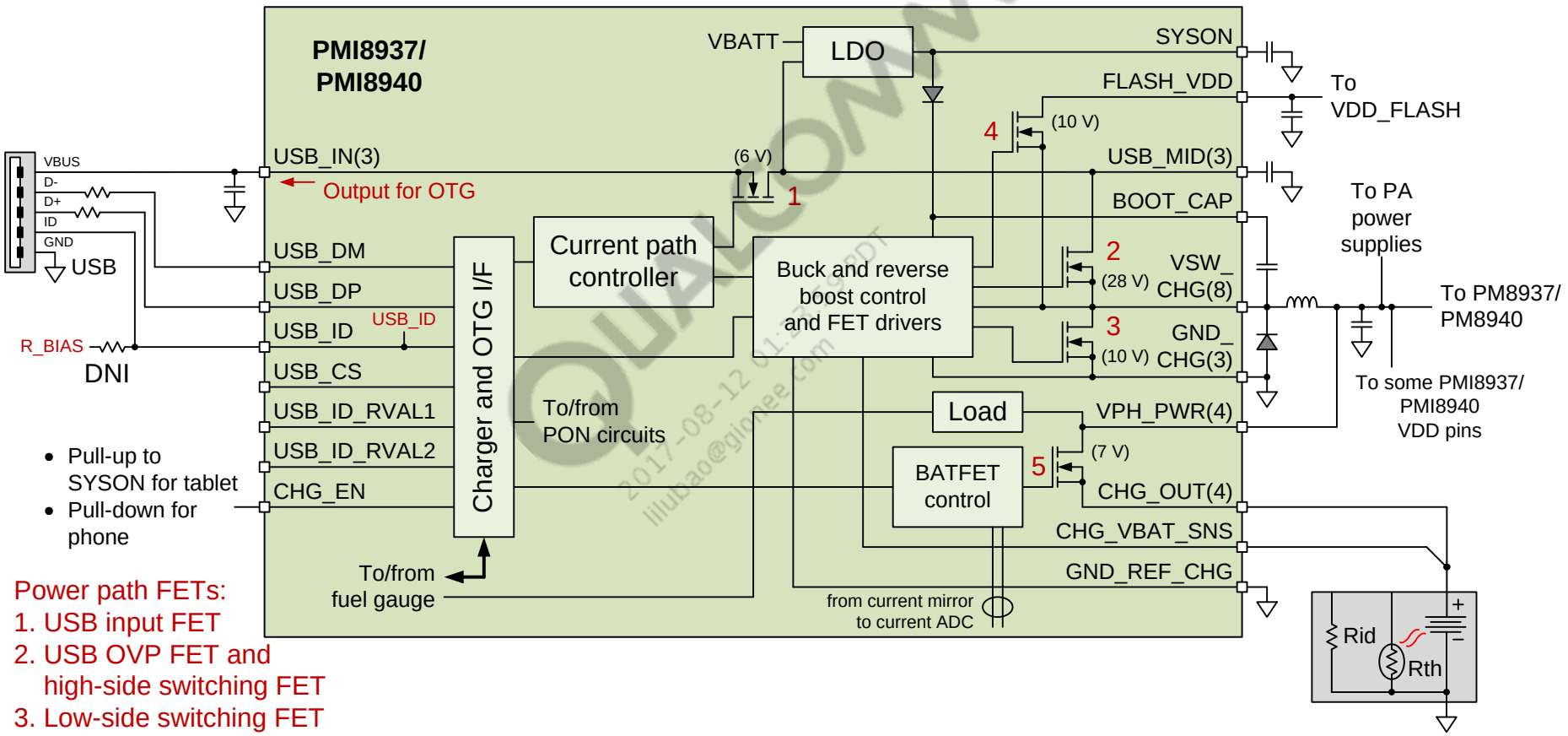
Section 2.2

SCHG and Battery Charging

Section 2.2.1

SCHG

SCHG Architecture



- Pull-up to SYSON for tablet
- Pull-down for phone

Power path FETs:
1. USB input FET
2. USB OVP FET and high-side switching FET
3. Low-side switching FET
4. Flash VDD FET
5. BATFET

Basic Charging Operation Sequence (1 of 2)

Prequalification: A series of tests after an external source is connected, before initiating the first charge cycle.

- Input voltage level > UVLO threshold, < OVLO threshold, and > battery voltage + 0.1 V.
- The appropriate ENABLE register SPMI command or EN input must be asserted.
- Prequalification parameters are continuously monitored and the charging cycle is suspended when any fall outside their limits.

Trickle-charge mode: The PMIC checks the battery voltage to decide if trickle-charging is required.

- If the battery voltage is below ~ 2.1 V, a charging current of 45 mA (typical) is applied.
- This charging current resets the battery pack protection circuit and safely raises the battery voltage.

Precharge mode: A new charging category added for this generation PMIC; once the battery voltage exceeds 2.1 V. The PMIC safely performs precharge on deeply discharged cells.

- The precharge (preconditioning) current is programmable from 100 mA–250 mA, in 50 mA steps, with an optional 550 mA setting.
- The PMIC remains in this mode until the battery voltage reaches the precharge to fast-charge voltage threshold (programmable from 2.4 V–3.0 V, in 200 mV steps).
- If this threshold is not exceeded before the precharge timer expires, the charge cycle is terminated and a corresponding timeout fault signal is asserted.

Constant current mode: When the precharge to fast-charge threshold is crossed, the PMIC enters its constant current (fast charge) mode.

- The fast charge current level is set by a corresponding register, programmable from 300 mA–3000 mA, in eight steps.
- The fast charge current level (output) is always limited by the input current limit setting.

Basic Charging Operation Sequence (2 of 2)

Constant voltage mode: When the predefined *float voltage* is reached, the fast-charge current begins to drop, and the mode transitions into constant voltage mode.

- Float voltage is programmable from 3.60 V–4.50 V, in 20 mV steps.
- High float voltage settings support modern battery packs that have float voltages of 3.6 V and 4.35 V.
- Dynamic float voltage adjustment allows sophisticated battery charging techniques and control algorithms.

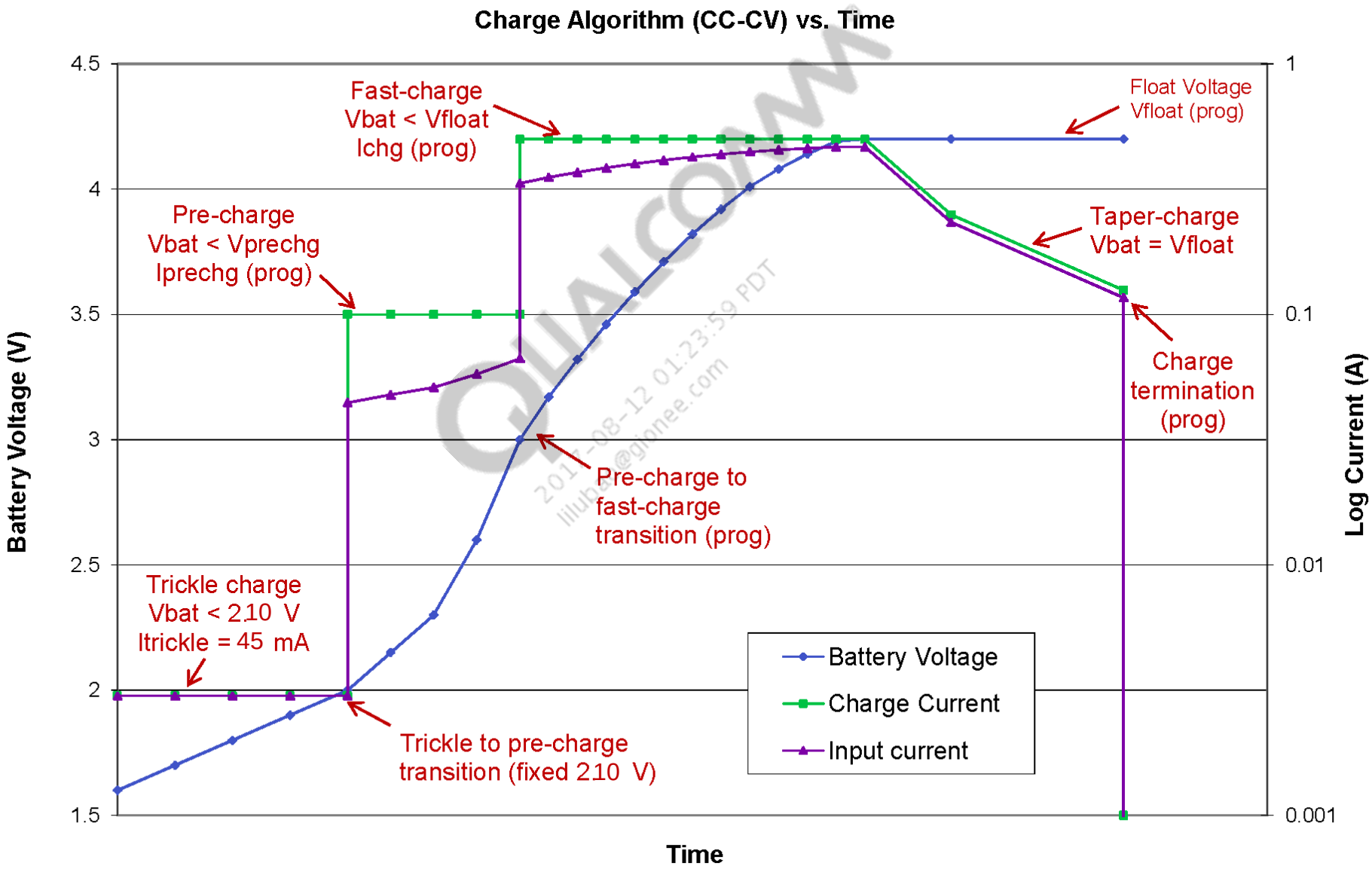
Charge completion: The charge cycle is considered complete when the charge current reaches the programmed termination current threshold, assuming current termination is enabled.

- Termination current is programmable in eight steps: 50, 100, 150, 200, 250, 300, 500, and 600 mA.
- If the termination current threshold is not met before the charge timer expires, the charge cycle is terminated and a corresponding timeout fault signal is asserted.

Automatic battery recharge: The PMIC automatically recharges the battery when its voltage falls by a value of V_RECH below the programmed float voltage; this part of the sequence is also called top off.

- If 1) the input power supply is still present, 2) charging remains enabled (SPMI command), and 3) all the prequalification parameters are still met, then a new charging cycle is initiated
- This charging cycle ensures that the battery capacity remains high, without needing to manually restarting a charging cycle.
- When the charge inhibit function is enabled, the automatic recharge threshold is overridden to the (higher) charge inhibit voltage threshold.
- The PMIC provides the following option: if charging terminates when the PMIC is in a soft temperature limit with reduced float voltage and then the temperature returns to normal (acceptable) levels, the PMIC starts charging again even if automatic recharge is disabled.

Voltage and Current Waveforms – Constant Current/Constant Voltage Operation



CurrentPath Control (1 of 2)

- CurrentPath technology allows separate control of the system and the battery outputs, with the system output (VPH_PWR) given priority of input power to allow the system to power up even with a defective, deeply discharged, or missing battery.
- When charging, if the system current requirements increase, the input current is steered towards the system by appropriately reducing charging current to the battery (see the plot on the Basic Charging and Float Voltage slide), thereby maintaining a constant input current level.
- When the input current is not adequate to satisfy the system requirements and the system voltage falls below the VREVFET threshold, the charger regulates the system voltage to 50 mV below the battery voltage and turns on the BATFET. This is called virtual diode mode. The battery and charger buck both supply current to the system. This is also called supplemental mode.
- In all of these cases, the input current remains limited per the device configuration for meeting the USB and other similar electrical specifications.

Condition	Batt (V)	Vsys (V)	Action
Isys + Ichg < (η × Iin)/D	< Vsys_min	Vsys_min	Battery is supplied with full charge current
Isys + Ichg ≥ (η × Iin)/D	< Vsys_min	Vsys_min	Battery charge current is reduced to supply full system load current
Isys > (η × Iin)/D	< Vsys_min	Vbatt – 50 mV	Battery discharges to supplement the system load current
Isys + Ichg < (η × Iin)/D	> Vsys_min	Vbatt + Ichg × Rsdon	Battery is supplied with full charge current
Isys + Ichg ≥ (η × Iin)/D	> Vsys_min	Vbatt + Ichg × Rsdon	Battery charge current is reduced to supply full system load current
Isys > (η × Iin)/D	> Vsys_min	Vbatt – 50 mV	Battery discharges to supplement the system load current

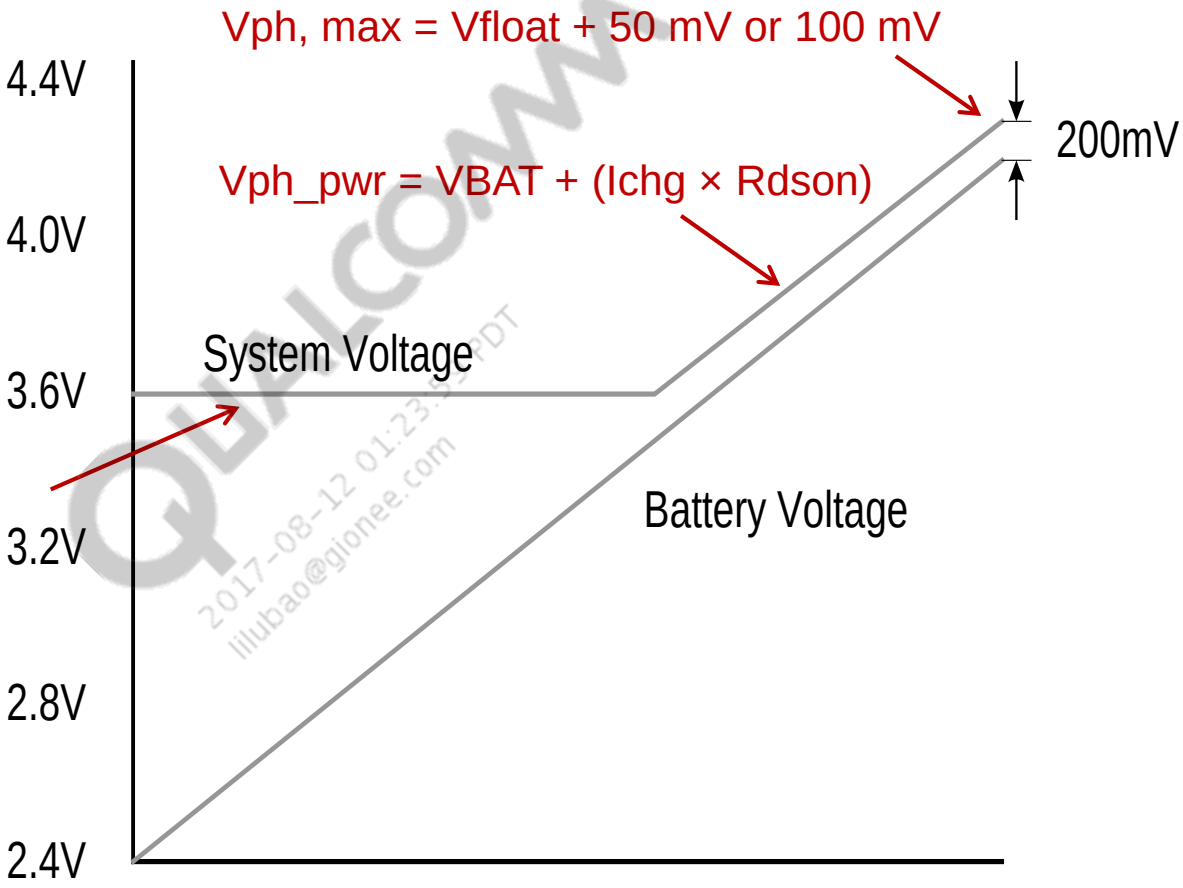
Notes:

1. In previous generations, the supplemental mode was called voltage collapse protection.
2. D = duty cycle = Vout/Vin; η = efficiency.

CurrentPath Control (2 of 2)

- CurrentPath also yields accurate charge termination.
  - It allows the system to know precisely when the charging current has hit the current termination threshold vs. implementations in which battery and system are connected to the same node.
- Four conditions must be met for the SCHG to terminate charge:
  - The device has entered the constant voltage charging phase.
  - The input current has not reached its input current limit.
  - The battery is not supplementing input power for the system.
  - The device has not entered thermal regulation mode.
- When the battery voltage is below a programmable value (see below), the system and battery are not connected together and the system voltage is regulated to these voltage levels.
- When the battery voltage is above the programmed value, the system voltage tracks the battery voltage with an approximate voltage differential of I_CHG × RDS_ON (the charge current times the on resistance of the BATFET).
  - This ensures that charging FET power dissipation is kept to a minimum.
  - See the plot on the Basic Charging and Float Voltage slide.
- When battery charging is completed, the system output (VPH_PWR) is regulated to Vfloat + 100 mV or Vfloat + 200 mV (programmable).

Basic Charging and Float Voltage



Programmable minimum system voltage (3.15 V, 3.45 V, and 3.6 V)

Vph_pwr, charger disabled = Vph, max, or VBAT + 100 mV

The above plot is for Vfloat = 4.2 V.

Other Battery and Charging Related Topics (1 of 2)

Safety timers – integrated safety timers protect against a defective battery pack.

- Both the precharge (24 min–191 min) and the complete charge timer (192 min–1527 min) start after the prequalification check is completed (and trickle-charging has started).
  - The precharge timer resets at the constant current mode transition.
  - The charge timer expires and charging mode is terminated if the termination current level is not reached within the predetermined duration.
- Both timers can be disabled by appropriate bit selection.
- Safety timers do not operate during the USB-OTG mode. They are paused during supplemental mode and during a thermal shutdown event.

USB dead battery recovery (automatic battery charging)

- The PMIC allows the portable device to automatically start the charging process when the battery voltage is below a low (dead) battery threshold and hence the system is off.
- This is accomplished by setting the charge enable in the active low mode.
- When the system wakes up, charging can be reinitiated.

Programmable battery charging – the PMIC is able to modify all the important charger parameters via software.

Safe charging protects against malware.

- The float voltage, charge currents, and battery temperature monitoring settings can be locked to prevent tampering.
- When an input is first inserted, the corresponding command register can be written to a 1 to lock the appropriate registers.
- This bit only returns to a 0 when the device exits a power-on reset condition.

Other Battery and Charging Related Topics (2 of 2)

Charger inhibit function – Prevents charging initiation under certain conditions

- The charger module provides the option of preventing charging initiation on power cycling or charge enabling/disabling unless the battery voltage is 50, 100, 200, or 300 mV below the float voltage.
- This prevents extreme stressing of the battery via continuous charging cycles in systems with short run times and frequent power cycling (input power connects and disconnects).
- Since this function is only active during power cycling and manual charge enabling, if the device enters and then exists suspend mode, charging continues even if the battery is above the charge inhibit voltage threshold.
- When this function is enabled, the automatic recharge threshold is overridden to the same threshold. As such, the automatic recharge thresholds can also be used for the charger inhibit function.

Current sinks – Easily recognize a charger removal event

- The USB_IN and MID_USB_IN pins each have a 10 mA current sink that is enabled to discharge the capacitance associated with the pins. This is useful to help protect the device in the case of an overvoltage condition and to more quickly recognize an input removal event.
- The MID_x 10 mA current sinks are enabled if their respective input pin voltage is above ~1 V, below the UVLO threshold, and/or below the V_ASHDN threshold. This current sink also turns on if the input pin is above its OVLO threshold, and remains on for ~100 ms after the input source drops below its OVLO threshold. During this ~100 ms, the input is not recognized as valid.
- The USB_IN 10 mA current sink works identical to the MID_x current sink described in the previous bullet, with the exception that it is disabled whenever USB_IN is above the OVLO threshold.

TurboCharge Mode

When charging, the PMIC exploits the intrinsic ability of the buck architecture to multiply the input current while stepping down the output voltage.

- This property is expressed mathematically in the comparison below and maximizes battery charging from current limited devices, and greatly decreases power dissipation and any heat-related dissipation.
- Using TurboCharge, devices can charge the battery with a charging current as high as 750 mA when charging from a port limited to 500 mA.

Linear charging

Equation 1 (linear charge current relationship, not accounting for thermal foldback): $I_{OUT} \approx I_{IN}$

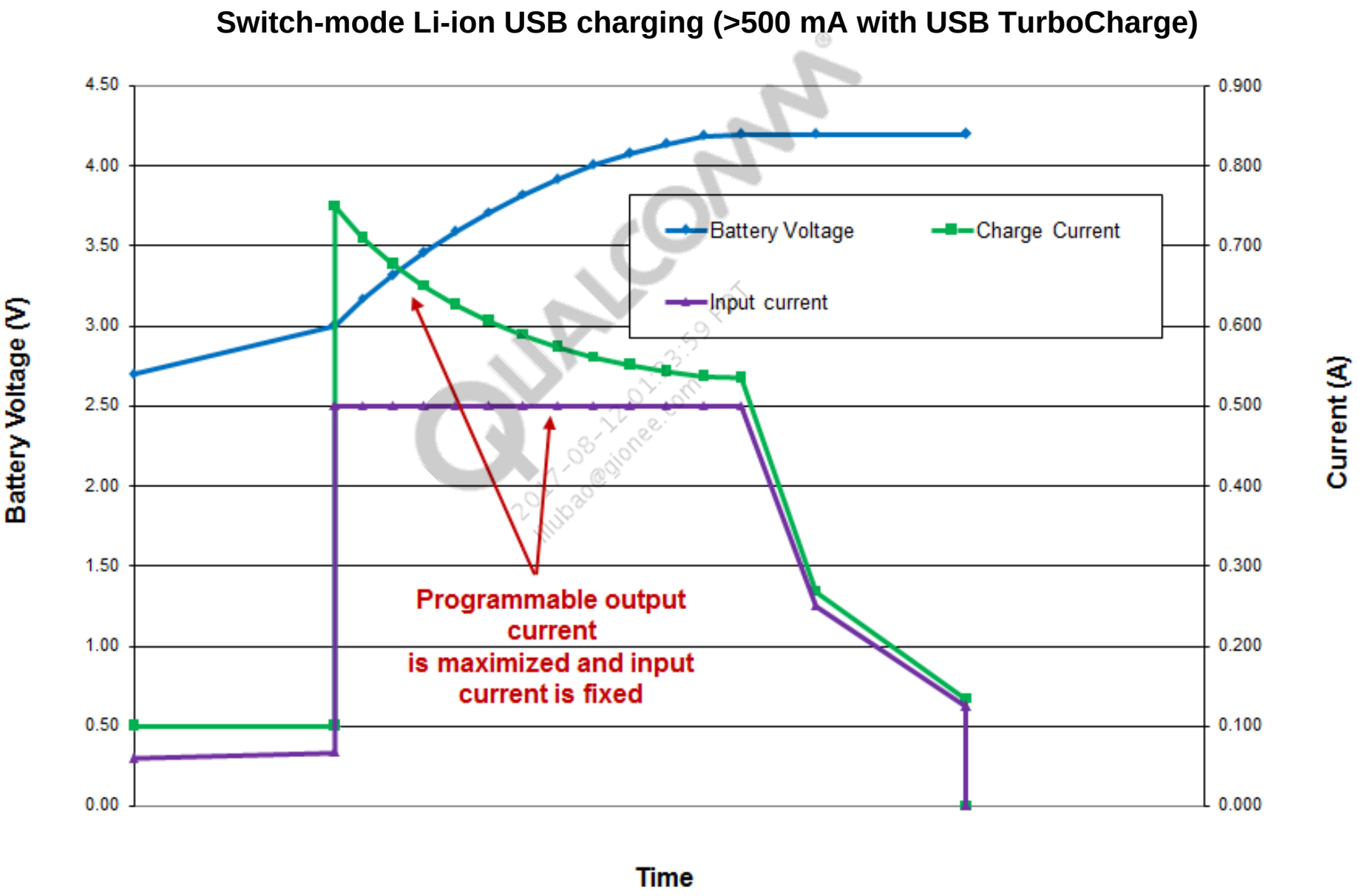
Equation 2 (efficiency of linear charger): $\eta = \frac{V_{BATTERY}}{V_{INPUT}}$

TurboCharge mode – optimized buck efficiency allows 500 mA at the charging port to deliver 750 mA output

Equation 3 (TurboCharge current relationship): $I_{BAT} = \frac{\eta \, VINIIN}{V_{BATT}}$

$\eta = 90\%$

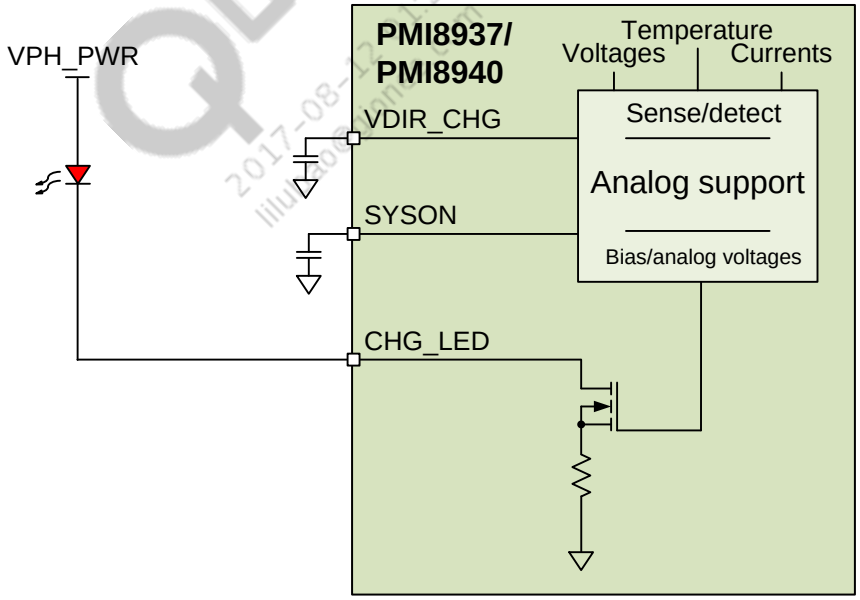
Voltage and Current Waveforms – TurboCharge Operation



CHG_LED Output for Charging Indication

CHG_LED can be used for a charging indication LED if automatic charging indication is desired.

- Charging indication is typically configured in the secondary boot loader (SBL) by using SPMI to write to the module.
- CHG_LED can be used if a charging indication is desired when the MSM™ device is not available to use SPMI to configure the module.
- When software is available to write over SPMI, the CHG_LED output can be configured to any desired state.
- Dead battery charging is indicated with default blinking pattern. Blinking pattern can be changed in the register 0x00001243 [2:1] once SBL comes up.
- Software control is not available for CHG_LED.
- CHG_LED is always active only if charger is present.

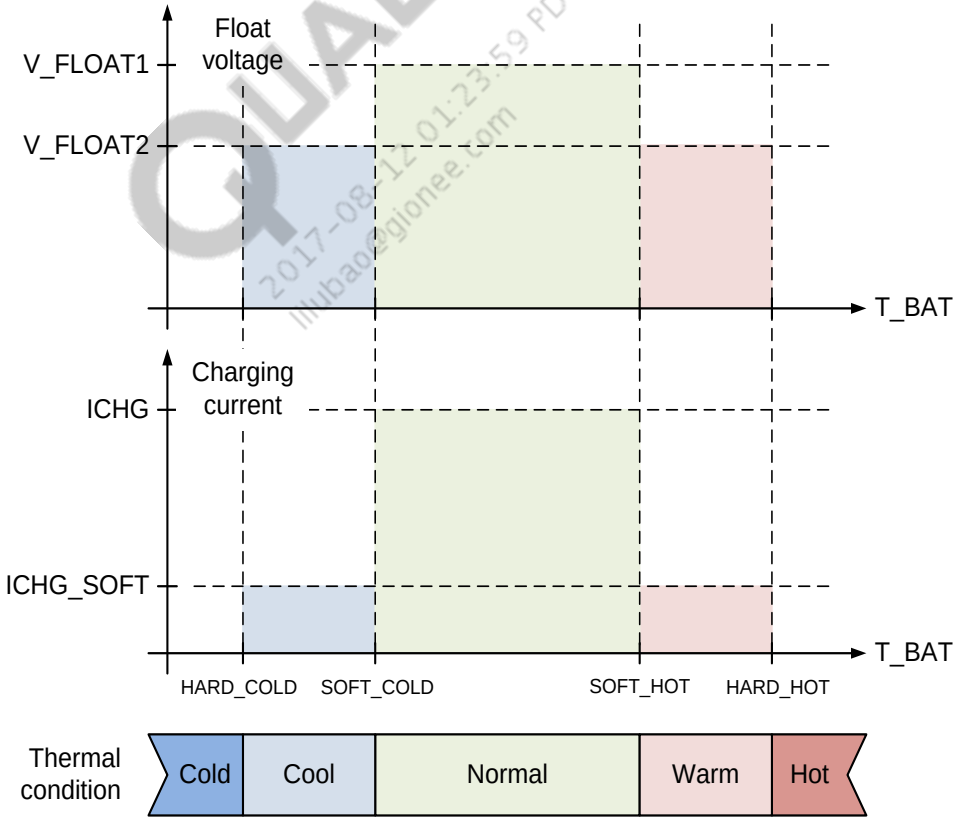


Section 2.2.2

JEITA Compliance

JEITA Compliance (1 of 3)

- The JEITA standard allows battery charging with reduced charging voltage and/or current outside the conventional battery temperature range (illustrated below).
  - Temperature threshold points (HARD_COLD, SOFT_COLD, HARD_HOT, and SOFT_HOT) are determined by battery chemistry and vary with different battery vendors; the thermistor temperature coefficient also varies.
  - As a result, the BATT_THERM voltages corresponding to the temperature points vary.
- JEITA compliance is mandatory in Japan after November 2011.
- Refer to *A Guide to the Safe Use of Secondary Lithium Ion Batteries in Notebook-type Personal Computers*.



JEITA Compliance (2 of 3)

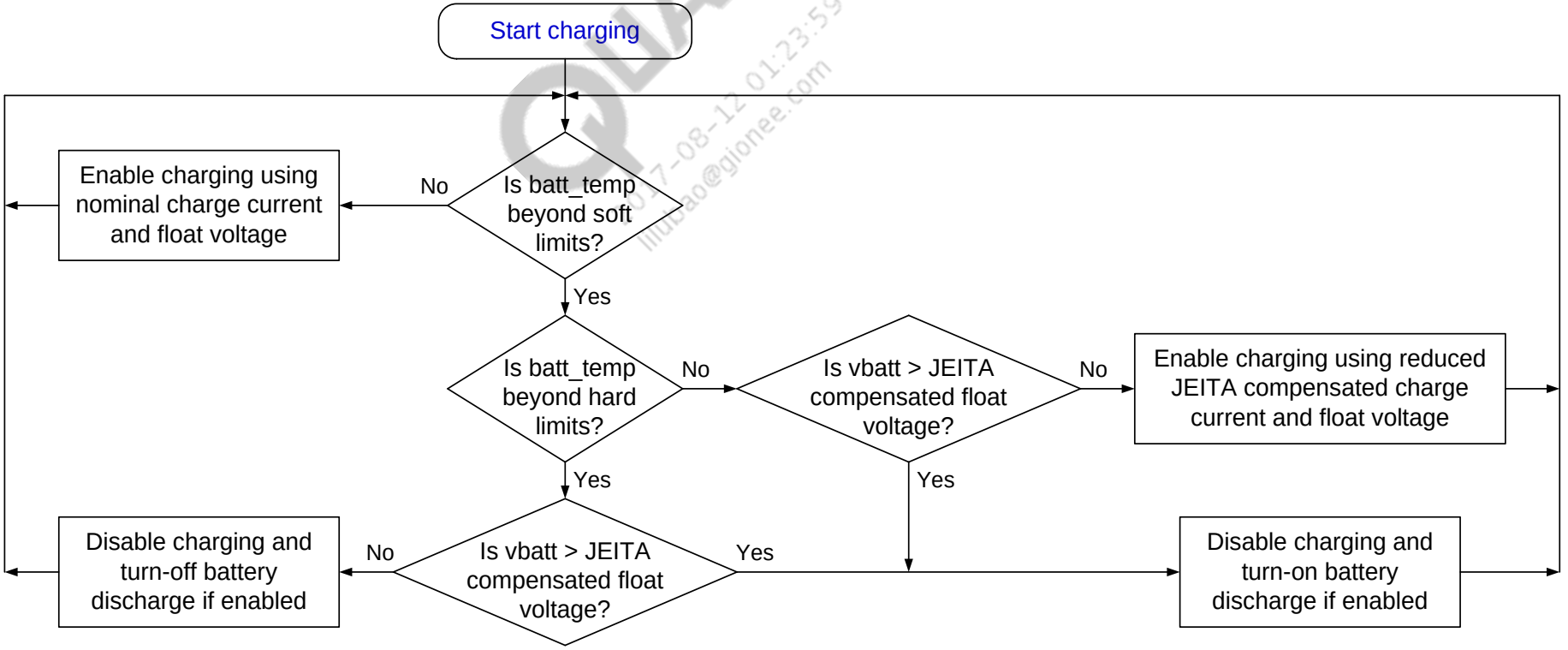
- The SCHG battery temperature monitor (BTM) has threshold configurability that helps cover both the traditional battery charging temperature range and the extended JEITA temperature range.
- The HARD_COLD, SOFT_COLD, HARD_HOT, and SOFT_HOT thresholds are fully software-programmable over a wide temperature range.
  - JEITA thresholds are programmed into an 8-bit unsigned register, LSB = 1 kΩ, 0x00 = 243 kΩ, 0x7F = 371 kΩ
- The bias resistor for the BAT_THERM must be chosen to match the resistance of the BAT_THERM at room temperature.
  - The battery's NTC thermistor beta coefficients are programmed into the fuel gauge's registers to convert the temperature of the battery. There are three coefficients based on the NTC's beta value. These coefficients are stored using half-floating encoding: 5 bits for exponent, 1 bit for sign, and 10 bits for mantissa.
- The fuel gauge uses an automated digital BTM routine to monitor the battery HARD_COLD, SOFT_COLD, HARD_HOT, and SOFT_HOT conditions.
- If enabled, the battery temperature is automatically measured by the ADC arbiter in programmable intervals from 1.47 s–392 s.
- The battery temperature measurement result is compared with programmable HARD_COLD, SOFT_COLD, HARD_HOT, and SOFT_HOT thresholds; interrupts are generated if any of the thresholds are exceeded.
  - The charger module automatically adjusts the charge current to the JEITA-compensated charge current and adjusts the float voltage to the JEITA-compensated float voltage.
  - Battery discharge commences if configured.
  - A JEITA compliance flowchart is shown on the next slide.

JEITA Compliance (3 of 3)

When the battery temperature is outside the soft temperature limits and the battery voltage is above the JEITA-compensated float voltage, a 10 mA current source can be used to discharge the battery voltage to the new JEITA-compensated float voltage. In this mode:

- Charging is disabled.
- The system voltage remains 100 mV above the battery voltage and is supplied by the input source.
- A supplemental battery current is provided if system loads increase beyond the capability of the input source.

This function is optional and can be disabled if required.



Section 2.3

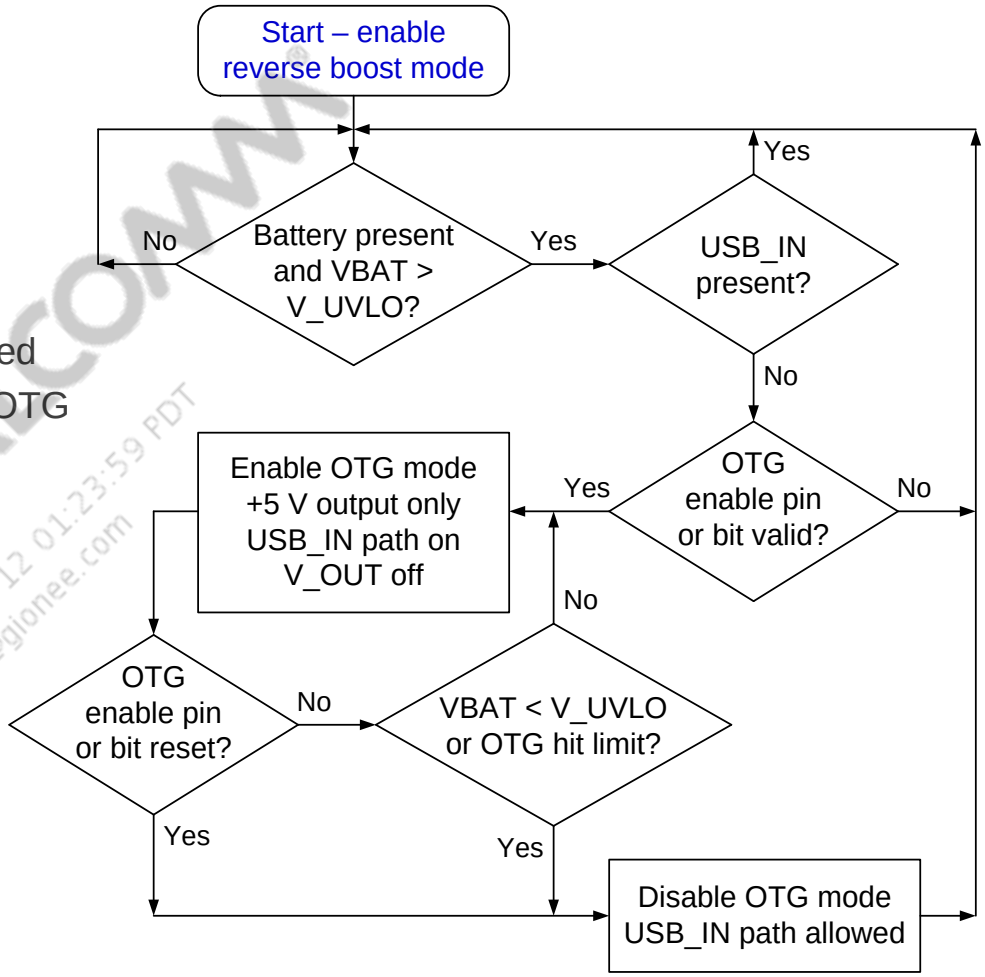
Special SCHG Topics

Section 2.3.1

Reverse Boost

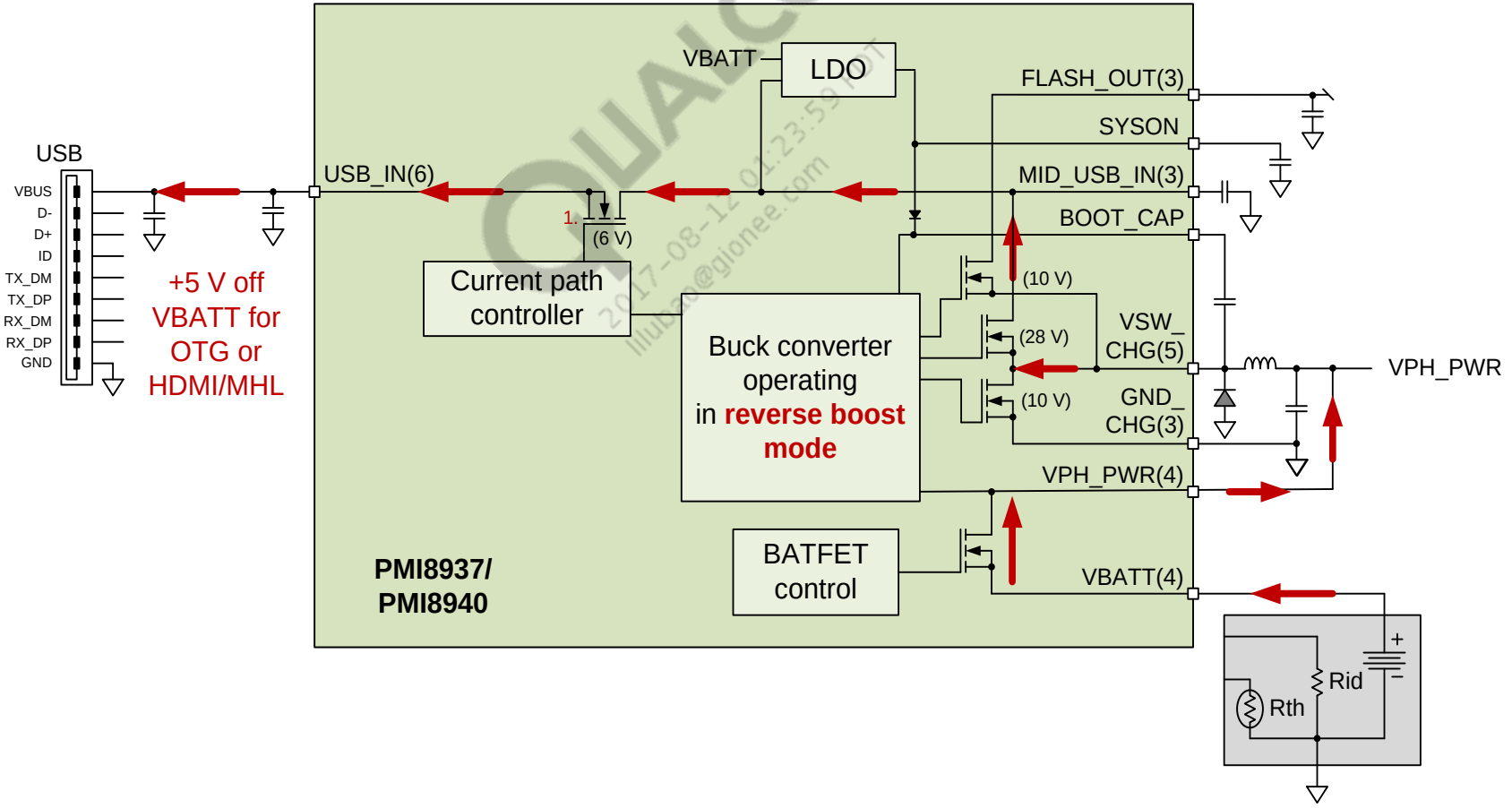
SCHG Reverse Boost Mode

- The SCHG operates in reverse boost mode to provide a 4 V–5 V supply for:
  - Flash LED drivers
  - USB-OTG
- A flash adaptive mode regulates the minimum headroom required, to minimize the voltage drop across LED drivers, and to minimize the associated heat generation. This mode is disabled when an OTG device is connected so that USB_IN and FLASH_OUT are both regulated to 5 V.
- The SCHG reverse boost mode runs the buck regulator in reverse by using existing components and on-chip switches.
- This mode supports up to 1000 mA.
- The programmable battery UVLO prevents over discharge.



USB On-The-Go Mode (1 of 2)

- The SCHG supplies a regulated 5.0 V output (sourced by the battery) at the USB_IN pin for powering peripherals compliant with the USB On-The-Go specifications.
- The boost converter is synchronous and uses the same power train and external components as the buck converter when in its charging mode.
- This mode, and corresponding power path, is enabled by either pin control (USBID = GND) or an SPMI command (bit active high).



USB On-The-Go Mode (2 of 2)

- The OTG mode is not entered if the battery is below the UVLO threshold to ensure that the battery is not drained.
  - Re-initiating OTG power delivery requires toggling the OTG pin or register.
  - To enable OTG mode, the USB_IN pin must be below ~ 1.0 V, otherwise reverse boost mode does not begin.
- The integrated boost converter has four output current limit levels.
- Once OTG is enabled, if the USB_IN pin does not go above the USB_FAIL level (4.15 V) within ~ 30 ms, the OTG OC IRQ is set and OTG is disabled until the OTG pin or register is toggled.
- During the OTG mode, the body diode remains off only during the soft-start duration and when the system voltage equals the battery voltage.
- When USB_IN is below ~ 1.0 V (no valid USB_IN source) and the battery is above the OTG UVLO level, priority is transferred from charging to OTG power.
- When both charging and OTG mode is enabled, the reverse boost power delivery takes priority.
- When the battery voltage is initially above the OTG UVLO threshold, but then falls below it because of OTG power consumption, OTG is suspended and charging is initiated.
  - In this case, re-initiating OTG power delivery requires toggling the OTG pin or register.
  - An interrupt signal indicates when OTG is enabled but does not start (overcurrent limit or battery undervoltage event).
- When the battery voltage falls below ~ 2.6 V during OTG mode, the SCHG shuts down.

USB_ID

An accessory charger adapter (ACA) is not supported on the PMI8937/PMI8940 device.

- USB_ID detection uses a two-phase process to detect R_{ID}.
  - Phase 1:
    - A coarse detector determines if a pull-down has been connected to the pin using a pull-up. USB_ID is internally pulled high to either 3.5 V (if charger is attached) or VPH_PWR (if charger is not attached) via 315 KΩ resistor.
    - If a pull-down is detected, proceed to phase 2.
  - Phase 2:
    - The 3.5 V pull-up is disabled and a series of current sources and a 1 V comparator are enabled.
    - As it rotates through the current sources, the output of the comparator is used to determine the R_{ID} value.
- Once RID_GND is detected, OTG is initiated.

Section 2.3.2

Charger Watchdog Timer

Charger Watchdog Timer

- The watchdog timer is started when enabled by an SPMI command.
- The watchdog timer is *pet*, that is, the timer is reset with every SPMI write to the PMI.
- The timer duration is 72, 36, or 18 s (programmable) when enabled.
- If the watchdog timer expires, there are three possible actions that the PMI can take:
  - If charging is enabled, charging is disabled.
  - If the watchdog IRQ is enabled, an IRQ is issued over the SPMI bus.
  - If automatic fault protection (AFP) is enabled, the PMI8937/PMI8940 device enters AFP mode and shuts down the system by reversing the direction of the BATFET body diode to fully isolate VPH_PWR from VBATT.
- When the PMI8937/PMI8940 device powers down, the state of the watchdog timer is reset to its default state (disabled). Therefore, the watchdog timer must be enabled after power on every time in the software.

Section 2.4

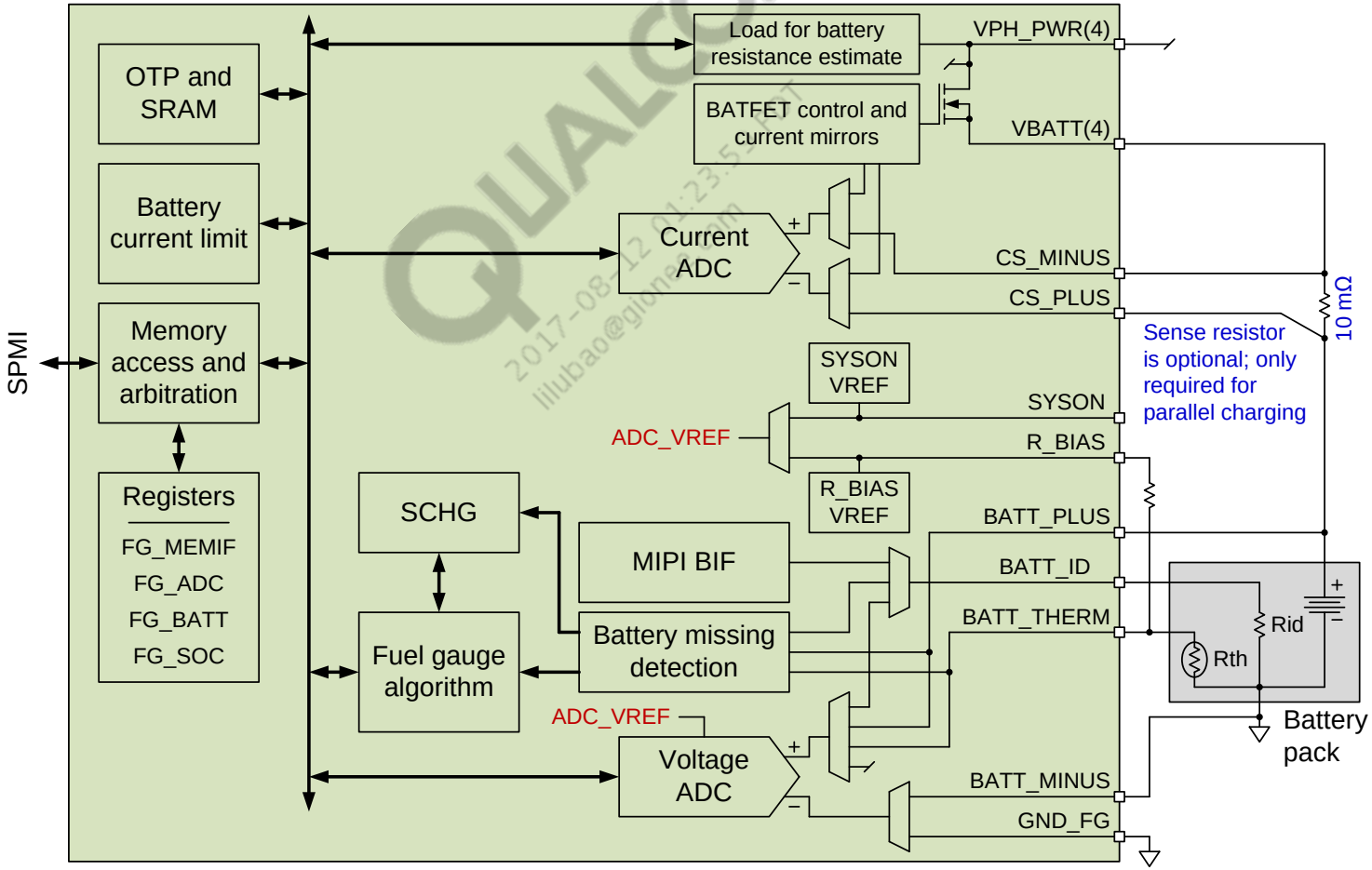
Fuel Gauge

Section 2.4.1

Fuel Gauge Architecture and Features

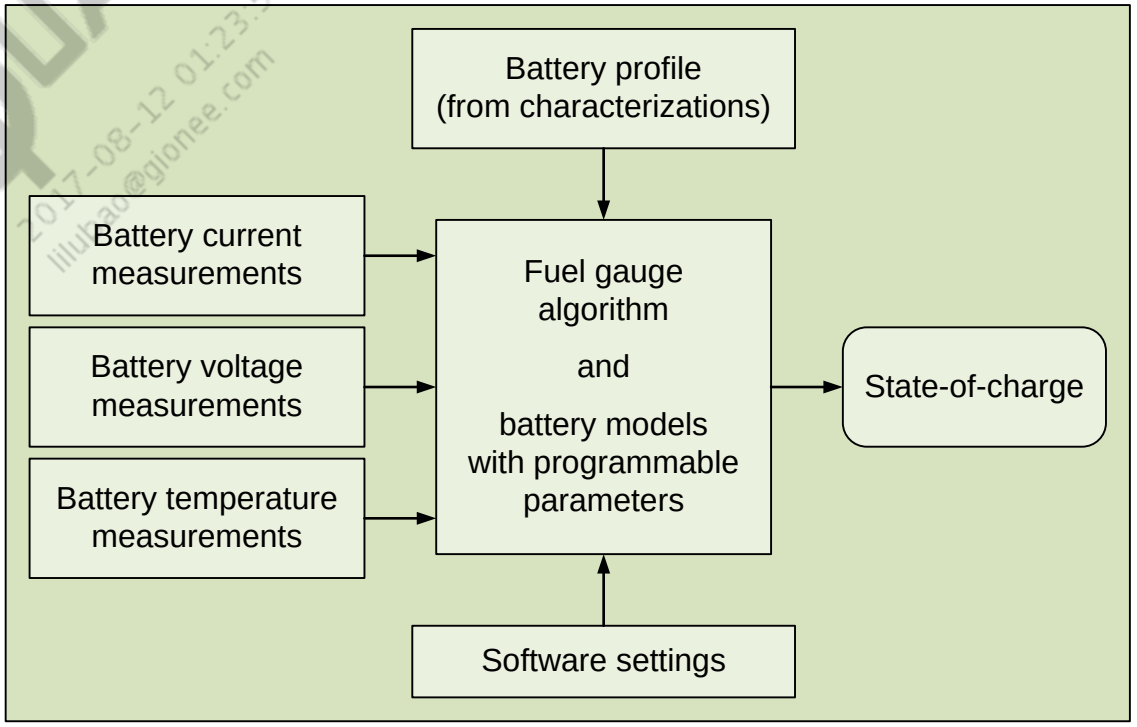
Fuel Gauge Architecture

- New current and voltage ADCs
- New BATFET-sensing circuits
- ADC voltage reference includes integrated temperature correction
- Accurate and stable voltage ADC over operating conditions
- Synchronous conversions are always used for battery voltage estimates
- MIPI BIF support for smart batteries via BATT_ID (see the IC-level Interfaces slide)



Fuel Gauge Features

- Estimate of state of charge is not performed by the application processor, but entirely executed inside of the PMIC
- Software only must read the state of charge from a register
- Interaction with the charger is primarily at the hardware level, not software
- Digital detection of the termination current improves accuracy
- Digital detection of JEITA
- Automatic recharge using state of charge threshold
- Detection of supplemental mode – when the battery is supplementing charger to power the system
- Effective in tracking state of charge during very dynamic changes in battery current
- Avoids monotonicity problem
- Reduced first-connection inaccuracy
- Good accuracy is provided without full cycling
- Online estimate of battery resistance
- Improved robustness towards aging and production spread



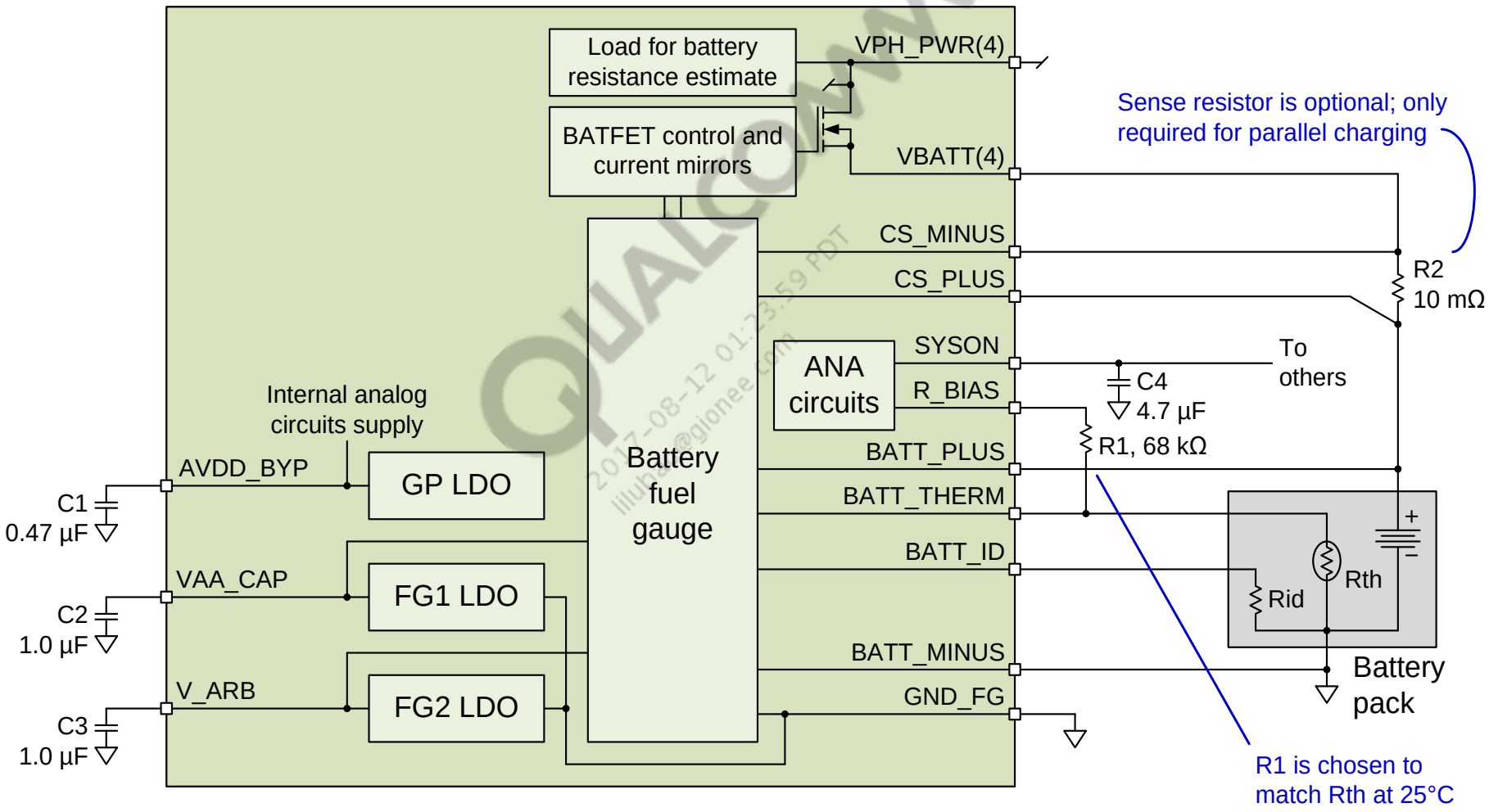
Comparison to Previous Generation (PM8941)

PM8941 battery monitor system (BMS)	PMI8937/PMI8940 fuel gauge hardware
Heavily software-dependent	Accomplished in hardware alone
State of charge estimate is computed in software based on ADC readings	Fuel gauge state of charge estimate is computed entirely in hardware
State of charge is estimated using BMS algorithm	All new proprietary fuel gauge algorithm
ADCs are mainly software-controlled	ADCs are directly controlled by the PMI fuel gauge
Software is needed to interact with charger	Interactions with charger are mainly handled by hardware
BMS ADCs require periodical software calibration	ADCs do not require periodical software calibrations
Bidimensional table for resistance	Online effective series resistance (ESR) estimate
Table approach requires additional table for internal resistance aging that is difficult to obtain	Estimate does not need known correlation between aging and internal battery resistance; online ESR is sufficient
State of charge information may be maintained or not depending on BMS generation	Fuel gauge memory is preserved as long as there is a valid power source connected to the phone

Section 2.4.2

Fuel Gauge Schematic, Layout, and Components

Fuel Gauge Schematic



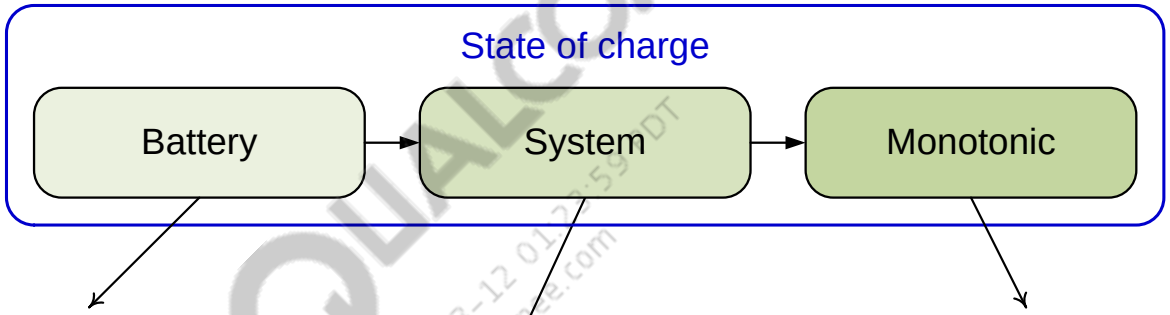
Section 2.4.3

Fuel Gauge Algorithm

Fuel Gauge Algorithm Overview

The fuel gauge module features three different layers of state of charge.

- Battery state of charge
- System available state of charge
- Monotonic state of charge



- State of charge referred to the battery
- Estimated using actual ESR, voltage, current, temperature, status, and values

- Cut-off state of charge – a correction based upon the system cut-off voltage; it is applied to the battery state of charge in order to estimate the system state of charge
- Full state of charge – a correction based upon charge float voltage and termination current; also applied to the battery state of charge in order to estimate the system state of charge

- Guarantees that the system state of charge is monotonic
  - Decreases only during discharging or supplemental mode
  - Increases only during charging
- Implements the maximum allowed slope to guarantee a smooth user experience

Battery State of Charge

- The battery state of charge is a result of coulomb counted state of charge corrected by a voltage mode feedback loop.
- The voltage mode correction loop uses the battery profile and battery model to predict the battery voltage and corrects the coulomb counted state of charge based on the calculated error.
- Regarding the model used to estimate the battery state of charge:
  - The value of R1 used is ESR – the latest detected battery resistance value stored in the ESR_actual register.
  - The open circuit voltage (OCV)/state of charge relationship uses the battery profile.
  - The value of R2 used is the Rslow resistance mapping.
  - The value of the time constant used is fixed, selected within the tau_rslow register.
- These parameters are discussed on the following slides.

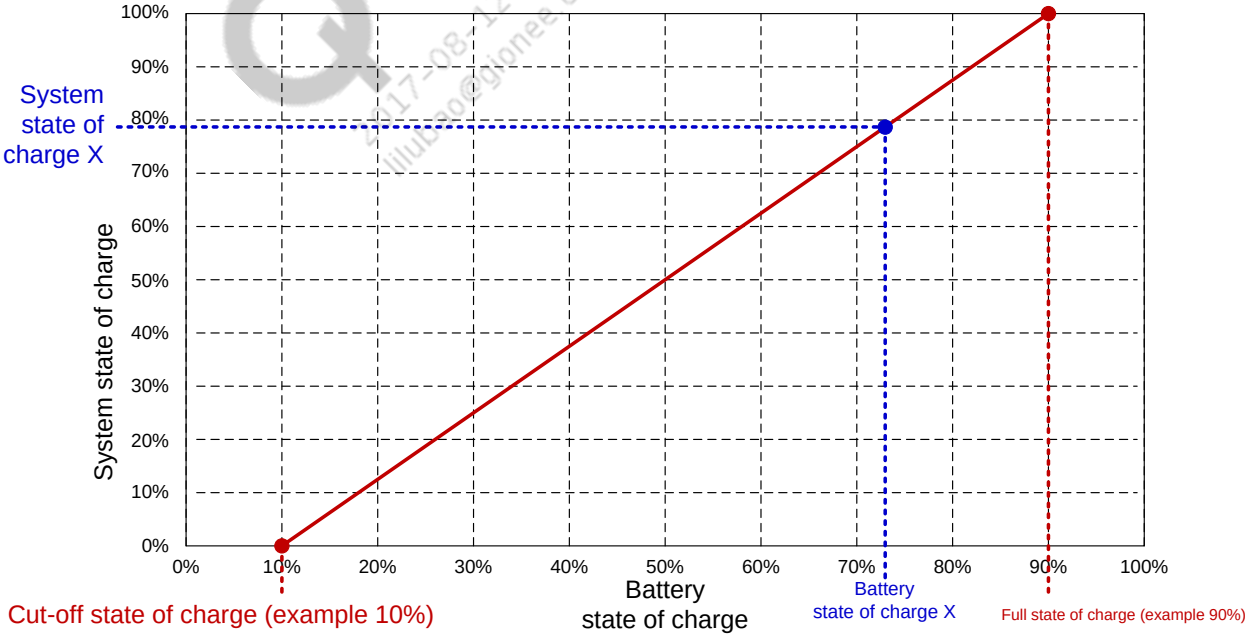
System Available State of Charge

The reported 0% state of charge point is adaptively estimated based on:

- Cutoff voltage
  - The cutoff voltage setting is used to adjust the 0% state of charge point to any battery voltage desired. The fuel gauge does this matching autonomously without software intervention.

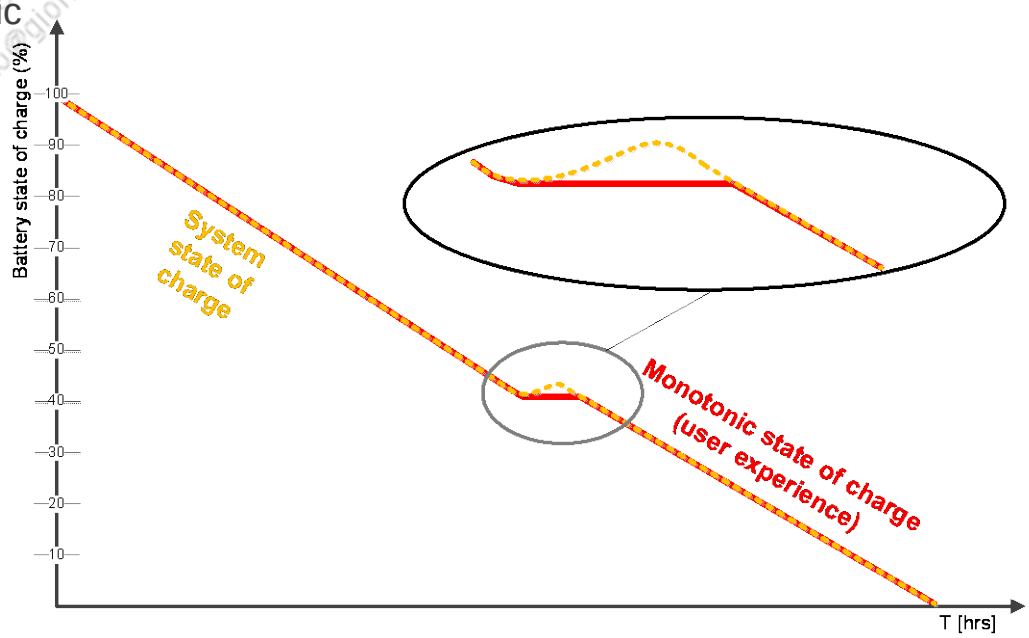
The 100% state of charge point is adaptively based on:

- The programmable system termination current
  - This calculation predicts when 100% state of charge is displayed by using a programmable termination current threshold (system termination current). The system termination current must be set higher than the charger's end of charge termination current, or 100% state of charge will never be reached.

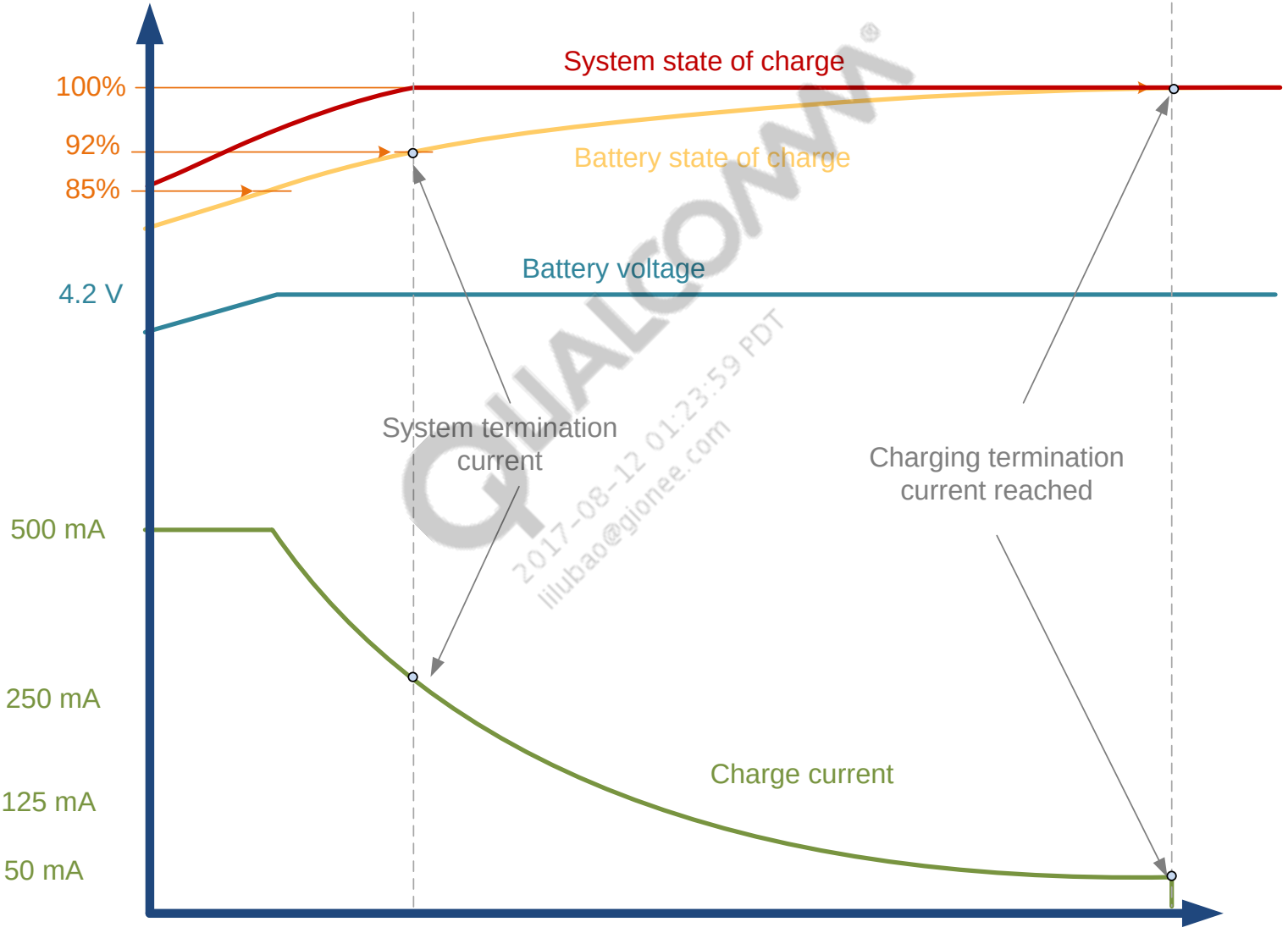


Monotonic State of Charge

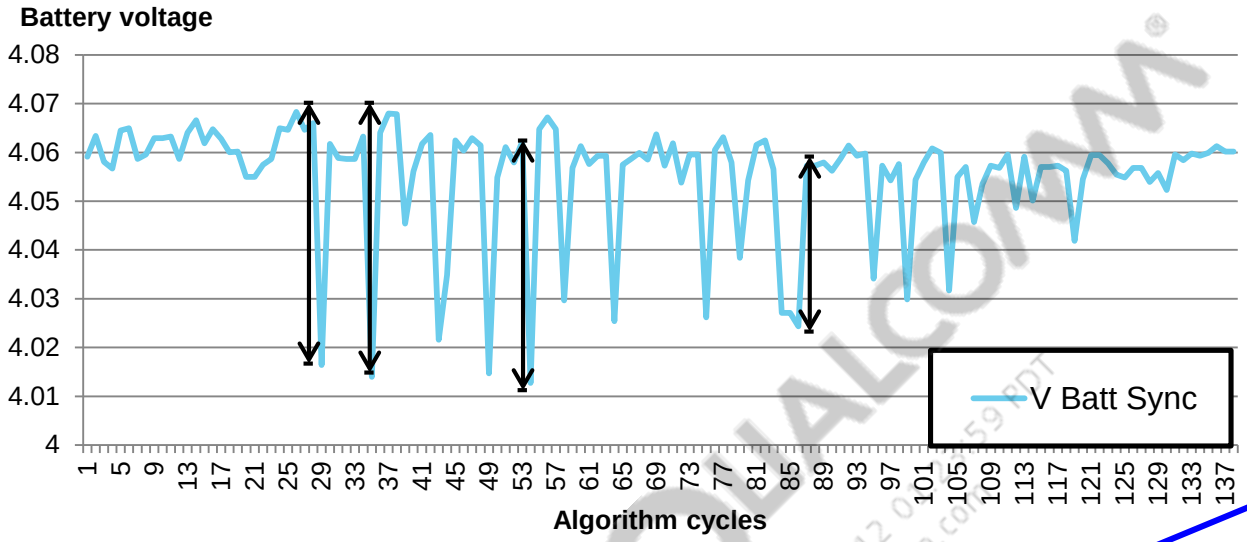
- Since change in the operating conditions of the battery could result in an increase or decrease of the system available state of charge, value filtering is applied to obtain a desirable monotonic behavior.
- Monotonic filtering handles situations where the cutoff state of charge is increased and then decreased, which can happen due to:
  - Increases and decreases of the battery internal resistance value
  - Increases and decreases of the battery load current
- The default configuration also enforces a slope limiter on the direction allowed given the current sign.
- The slope limiter is needed when:
  - Certain event sequences where the monotonic filter is applied and then a change in the operating conditions occurs that would otherwise cause the clamped system state of charge value to propagate directly to the monotonic state of charge read by the user thus creating an undesired step.
- The slope limiter prevents steps in the monotonic state of charge.
- Guarantees that the system state of charge is monotonic:
  - Decreases only during battery discharge or supplemental mode
  - Increases only during battery charge
- This implements the maximum-allowed slope to guarantee a smooth user experience.

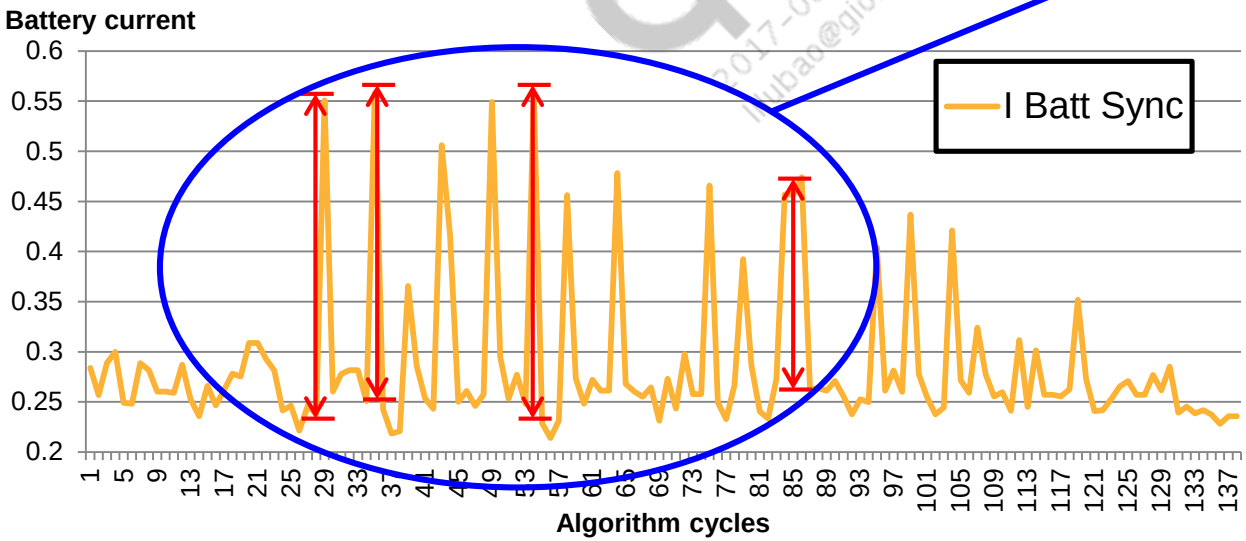


System Available State of Charge



ESR (1 of 2)



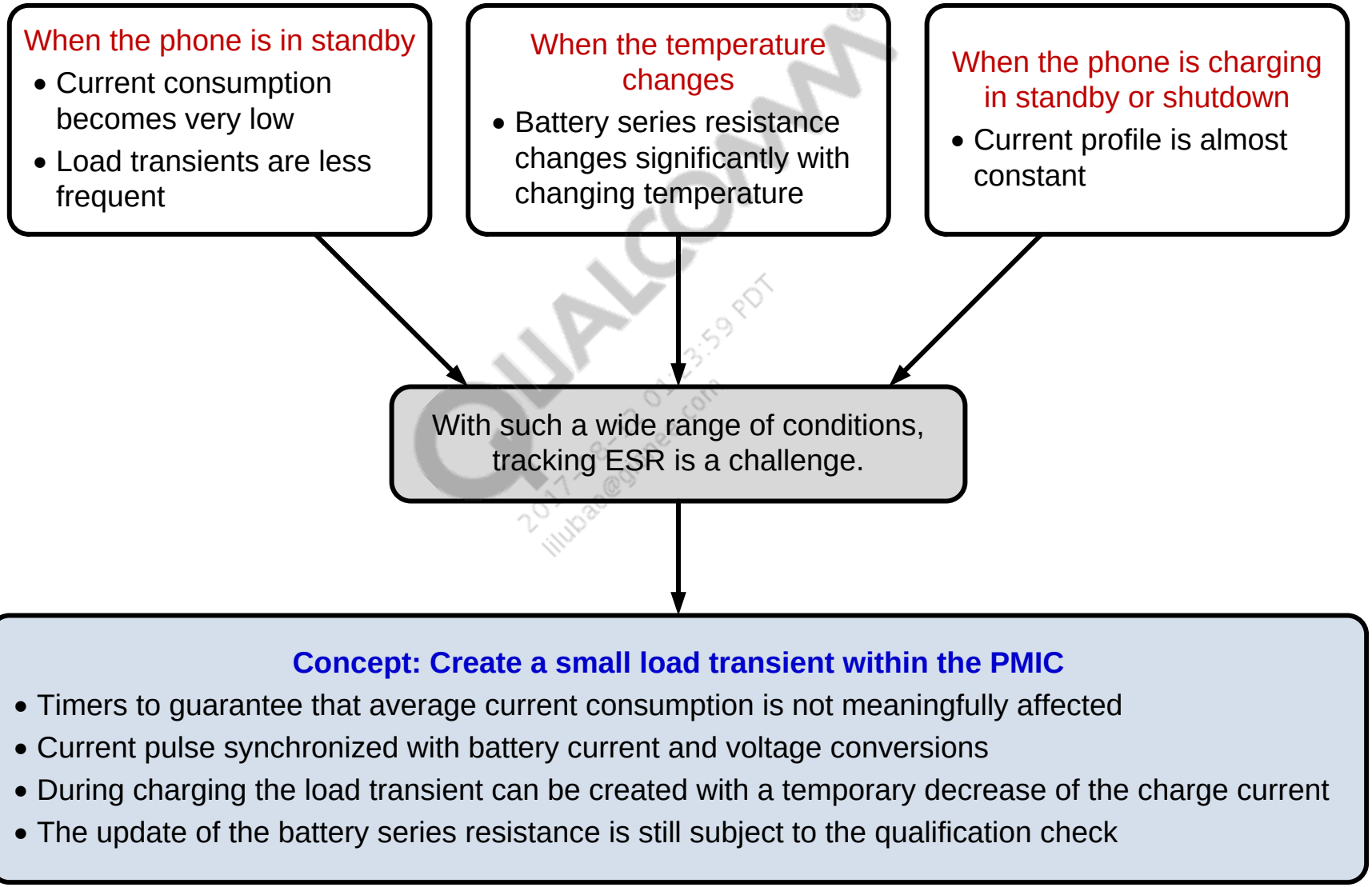


During device operation, there are various current transients that the fuel gauge can use to estimate the online ESR.

First step: qualify the battery current transient amplitude

Estimated battery resistance value is then filtered

ESR (2 of 2)

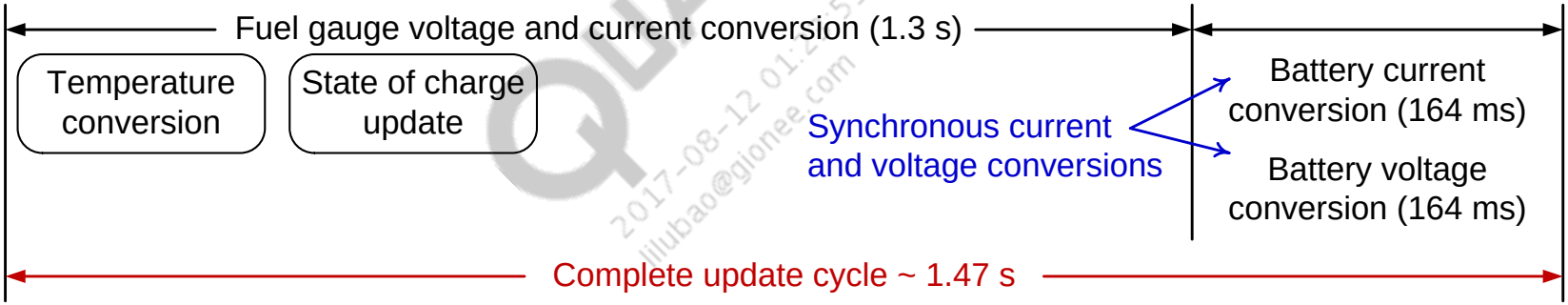


Section 2.4.4

Fuel Gauge Operational Details

Standard Fuel Gauge Update Cycle

- If the fuel gauge is not in reset, all activities are coordinated by the fuel gauge algorithm.
- The fuel gauge algorithm activity is scheduled in cycles; during a cycle:
  - The battery voltage and current are synchronously acquired
  - The model of the battery is evaluated, and the different levels of state of charge are updated
  - The temperature of the battery may be updated
  - Other activities are performed



Interrupts

The hardware fuel gauge provides the system with information about the status.

- Configurable interrupts related to state of charge
  - State of charge > high state of charge threshold
  - State of charge < low state of charge threshold
  - Delta state of charge > state of charge threshold
  - Battery full: monotonic state of charge = 100%
  - Battery voltage < configurable empty voltage
- Interrupt related to battery voltage
  - Battery voltage < voltage threshold
- Additional interrupts
  - Monotonic state of charge = 0% (experienced by the user) or battery voltage < configurable empty voltage
- Thresholds for high, low, and delta states of charge and battery voltage low interrupts are programmable via SPMI.

Battery Identification

Battery identification is accomplished autonomously in hardware by the fuel gauge module using the following algorithm on the BATT_ID pin. The steps of the algorithm are:

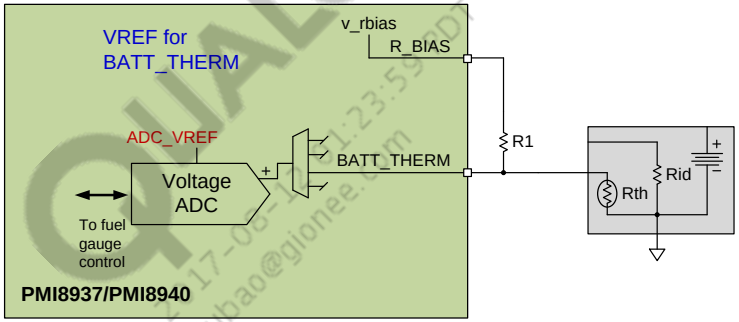
1. BSI is disabled, and the detection sequence is started.
2. The pull-up is enabled with the weakest current level (5 µA).
3. The first conversion is performed.
   a. If the converted value exceeds the allowed range conversion, conversion is repeated, increasing the bias current (15 µA or 150 µA).
4. After the resistance is detected, a second conversion is performed to verify stability.
5. The tolerances are stored in the battery_id_recheck_range register.
6. Conversion values are checked.
7. The value of the battery ID is detected and the corresponding profile can be selected using software.

Battery ID bias currents and resistor detectable range

Battery ID resistor bias current value		Resistor
5 µA	Start of range	175 kΩ
	End of range	450 kΩ
15 µA	Start of range	15 kΩ
	End of range	140 kΩ
150 µA	Start of range	960 Ω
	End of range	15 kΩ

Battery Pack Thermal Monitor (1 of 2)

- Cold and hot battery pack temperature events are detected in the fuel gauge module and reported to the charger module internally within the PMIC.
- Thermal monitor trip points correspond with the JEITA soft and hard limits set in the fuel gauge SRAM.
- Since the thermal limits are compared to digital values, a very high accuracy comparison can be made compared to the analog method of previous PMICs.
- The fuel gauge module periodically enables R_BIAS and takes a reading at BATT_THERM to convert the temperature. The temperature is converted at every eight fuel gauge update cycles (8 × 1.47 s = ~11.76 s) during discharge.
- The external bias resistor R1 must be chosen to match the resistance of the thermistor Rth at 25°C.



- The PMI8937/PMI8940 fuel gauge also supports the inclusion of capacitance on BAT_THERM as an improvement over previous generations by including the ability to delay measurements on BATT_THERM by up to 160 ms, giving RBIAS time to settle when enabled. The supported range of capacitance can be found in this table.

Nominal thermistor resistance (at 25°C)	Absolute maximum thermistor capacitance with 160 ms delay
10 kΩ	4.7 µF
33 kΩ	1.5 µF
47 kΩ	1.0 µF
68.1 kΩ	0.68 µF
100 kΩ	0.47 µF

Note: The BATT_THERM measurement delay has to be adjusted to support this capacitance on BATT_THERM. A longer delay due to the addition of capacitance increases the rock bottom sleep current.

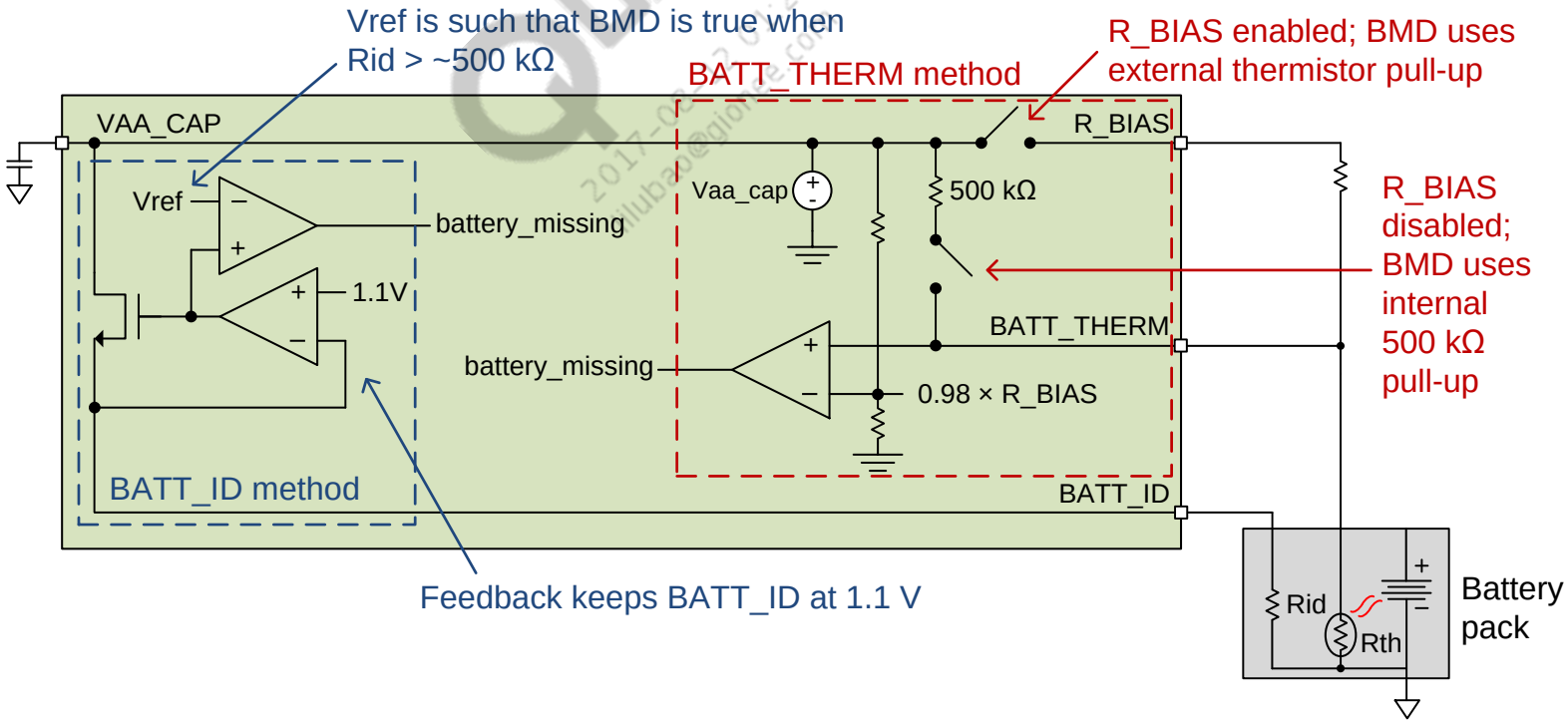
Battery Pack Thermal Monitor (2 of 2)

- Fuel gauge temperature sensing prevents excessive battery temperatures during charging.
- If the temperature limits are exceeded, battery charging is suspended and safety timers maintain their values but are paused.
  - During this mode, the system is powered by the battery.
- If the temperature returns to a safe level, charging is automatically re-enabled, the corresponding fault bit is reset, and safety timers continue counting when temperature level has returned to within the safe operating range.
- The corresponding status bit is not latched; instead, it is updated when a temperature conversion is completed.
- When the battery temperature is outside the specified temperature limits, as soon as charging is enabled (before the hold-off timer has expired), charging does not start.
- The SCHG can notify the system of a battery thermal condition without suspending battery charging (optional).
- See the JEITA Compliance section for more details.

Battery Missing Detection

The PMIC can be programmed to check for a missing battery; it uses the battery pack thermal monitor (BATT_THERM) **and/or** battery ID (BATT_ID). By default, both are used.

- The PMIC checks for a resistor to ground on BATT_ID and/or BATT_THERM.
  - If not found, a corresponding bit is asserted and charging is suspended.
- Once the battery is reconnected, charging is automatically initiated, assuming that input power is present, all qualification parameters are met, and charging is enabled.
- Refer to the *MSM8937 + PM8937 + PMI8952/PMI8937 Schematic Review Checklist* (80-P2468-111) and *MSM8940 + PM8940 + PMI8952/PMI8940 Schematic Review Checklist* (80-P4978-111) for information on how to terminate BATT_ID and BATT_THERM if unused.

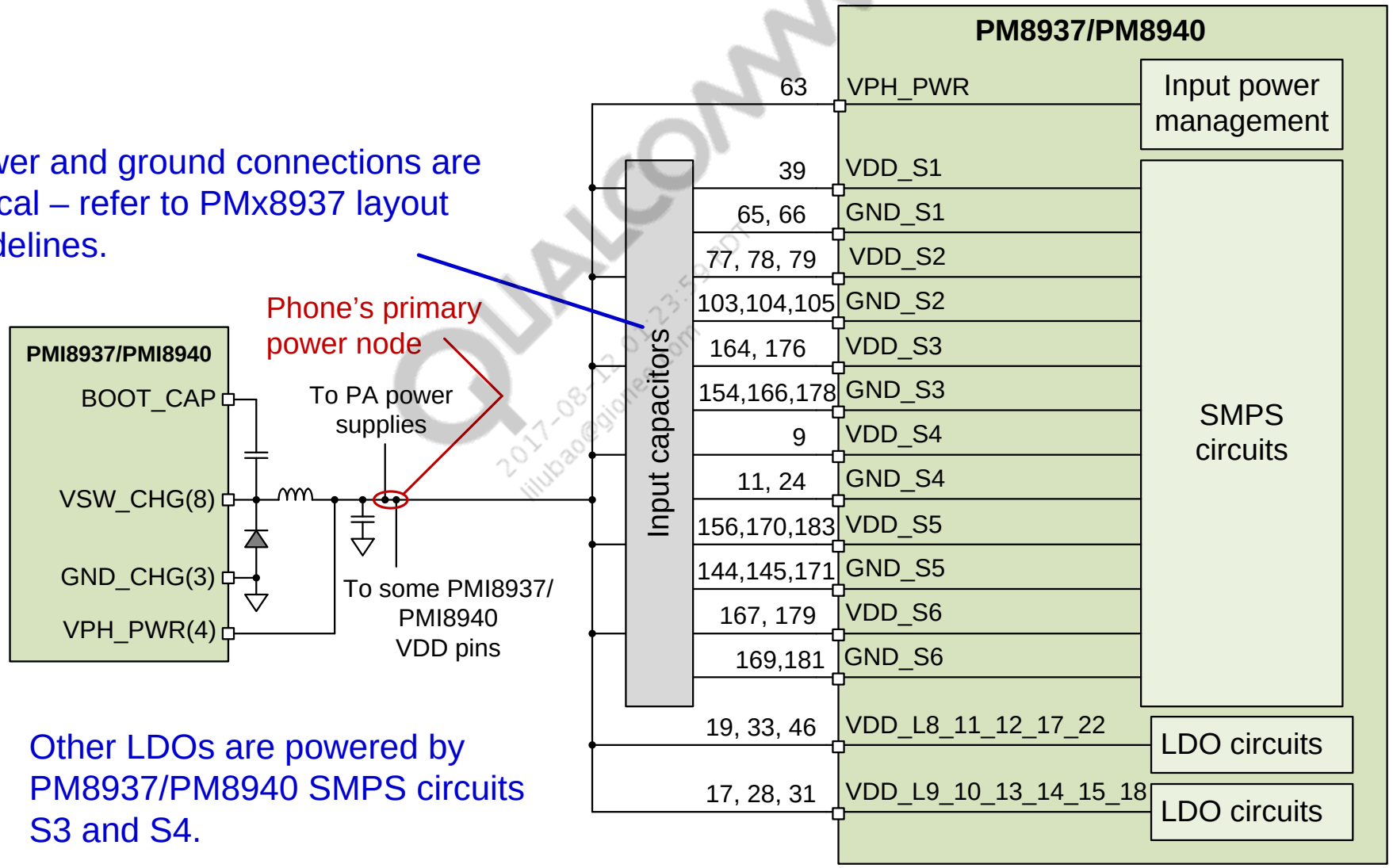


Section 2.5

PM8937/PM8940 VPH_PWR and Coin Cell

PM8937/PM8940 VPH_PWR Input Schematic

See the PM8937/PM8940 Output Power Management section for all SMPS and LDO input power connections.



Coin Cell or Keep-alive Capacitor (1 of 2)

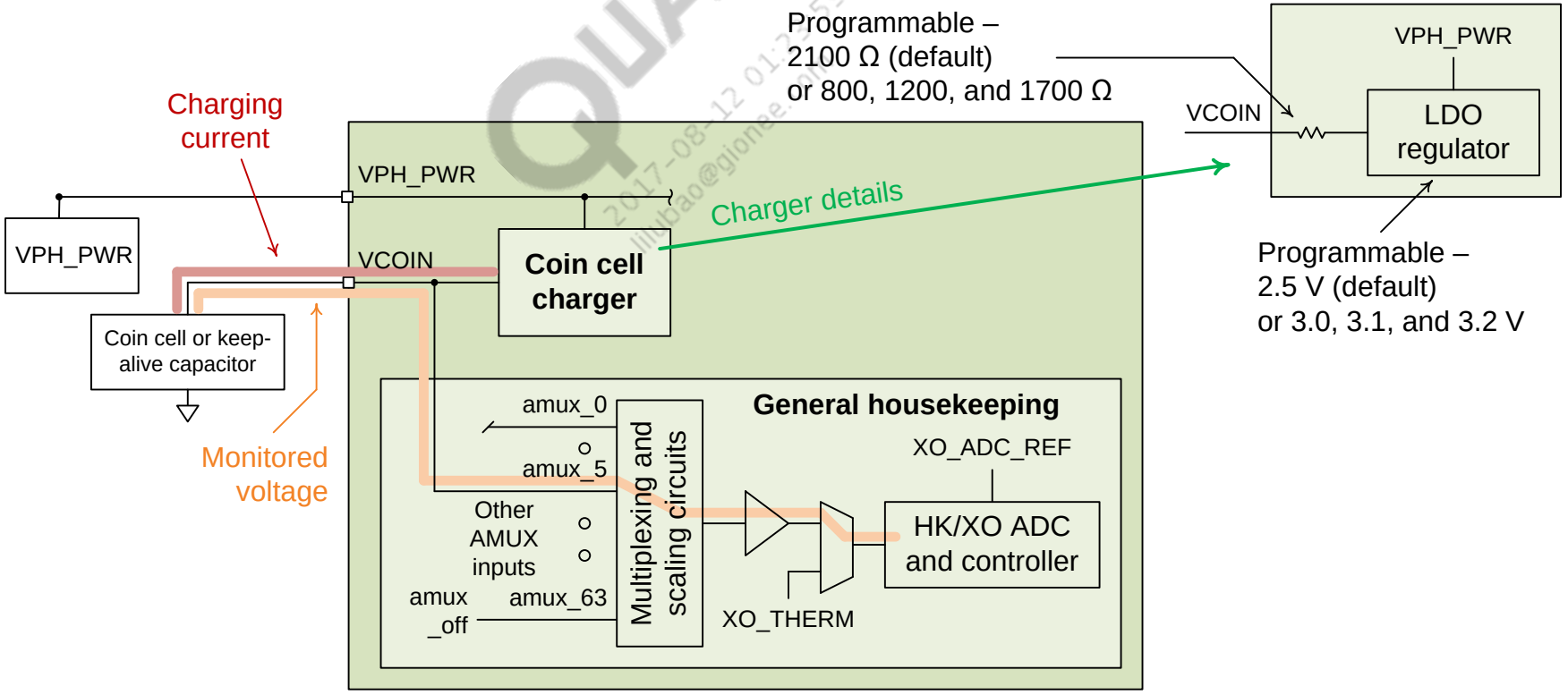
- The PM8937/PM8940 device's VCOIN requires either a lithium manganese dioxide rechargeable coin cell or a keep-alive capacitor.
  - Only the PM8937/PM8940 device requires a coin cell; the PMI8937/PMI8940 device does not have real-time clock (RTC) or sudden momentary power loss (SMPL) features.
- The Panasonic ML-series (or an equivalent) is an example coin cell that complements the PMIC well.
- In addition to numerical specifications, consider the discharge characteristics – the coin cell voltage should stay above 1.5 V for as long as possible, then drop off quickly from there.
  - This keeps the real-time clock, SMPS, and crystal oscillator circuits running during the PMIC's off modes and ensures an abrupt turn-off as the backup voltage drops.
- When a coin cell is used
  - When the phone is powered off, the appropriate oscillator and real-time clock circuits continue to run.
    - These circuits are powered by the main battery, if present and valid.
    - If not, these circuits are powered by the coin cell.
  - A valid voltage on VCOIN is required to run the SMPL timer, but the coin cell may be replaced with an appropriate capacitor to maintain the SMPL feature only (as explained below).
- When a keep-alive capacitor is used
  - When the phone is powered off, the appropriate oscillator and real-time clock circuits continue to run.
    - These circuits are powered by the main battery, if present and valid.
    - If not, these circuits are powered down; the keep-alive capacitor does not store enough energy to power these circuits.
    - The keep-alive capacitor is sufficient to power the SMPL timer and supporting circuits only.

Note: The coin cell/keep-alive capacitor is not available on the PMI, and thus the PMI cannot maintain its volatile memory without a valid power source. RTC and SMPL are exclusively handled by the PM.

Coin Cell or Keep-alive Capacitor (2 of 2)

Charging

- The coin cell charger's programmed settings remain valid even if the main battery is removed.
- Charging resumes even if the phone is in an off state.
- Settings are reset to their default values only if the coin cell itself is removed.
- Coin cell charger settings are not reset if an SMPL event occurs.



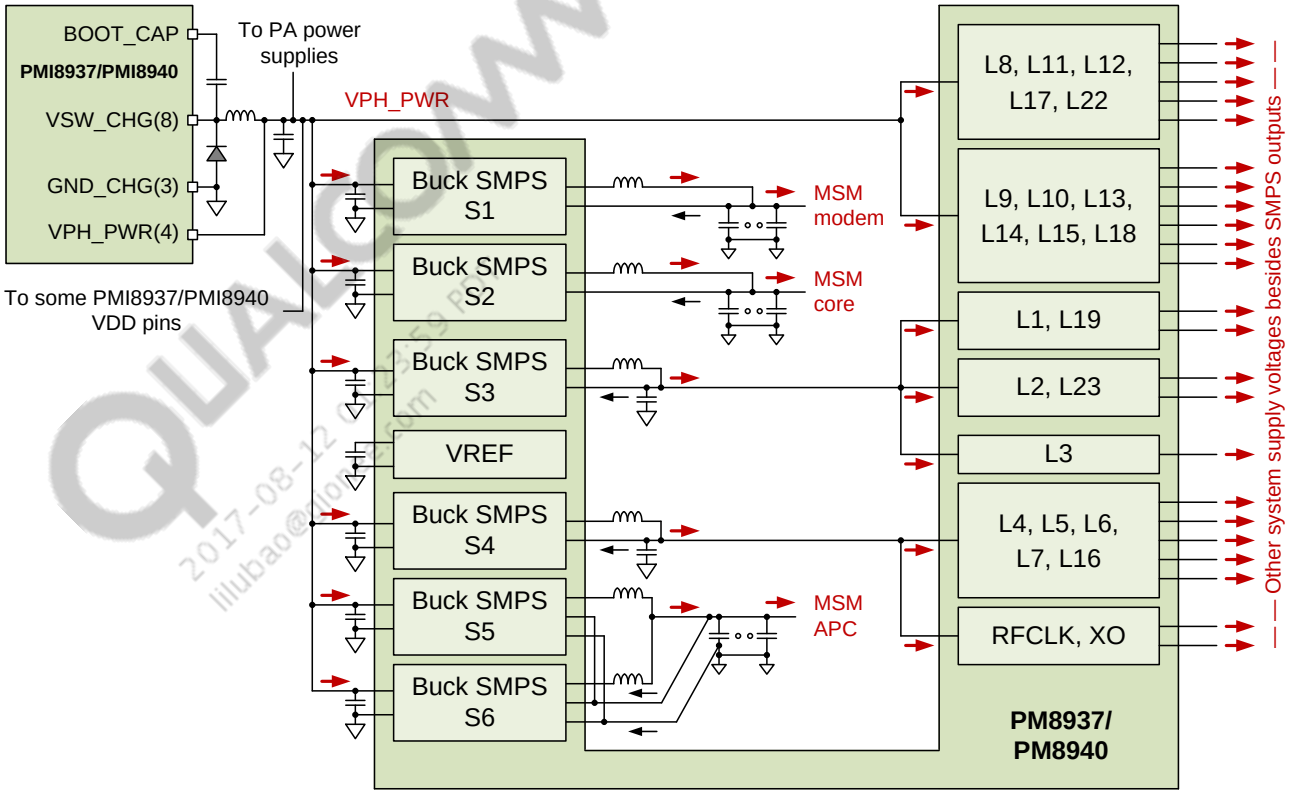
Section 3

PM8937/PM8940 Output Power Management

Output Power Management – MSM8937 Chipset Example

Output power management topics

- Summary of OPM outputs and expected uses
- SMPS S5 and S6
- SMPS S1, S2, S3, and S4
- Topics common to all SMPS circuit types
- Linear LDOs
- Bandgap references
- Internal connections, external options



Output Power Management – Summary (1 of 2)

Function	Circuit type	Default voltage (V)	Specified range (V)	Programmable range (V)	Rated current (mA)	Default ON	Expected use
S1	SMPS	1.225	0.900–1.350	0.375–1.5625	2000	N	MSM modem
S2	SMPS	1.225	0.550–1.350	0.375–1.5625	3000	Y	MSM core and graphics
S3	SMPS	1.288	1.200–1.4125	0.375–1.5625	2700	Y	Low-voltage LDOs (1, 2, 3, 19, and 23)
S4	SMPS	2.050	1.800–2.050	1.550–3.126	2500	Y	High-voltage LDOs (4, 5, 6, 7, 16, RFCLK, and XO)
S5	SMPS	1.225	1.050–1.350	0.350–1.355	3000	Y	MSM applications processor
S6	SMPS	1.225	1.050–1.350	0.350–1.355	3000	Y	MSM applications processor
L1	NMOS LDO	1.000	1.000	0.375–1.5375	1200	N	RFICs
L2	NMOS LDO	1.200	1.200	0.375–1.5375	1200	Y	LPDDR2/LPDDR3, MIPI CSI, and DSI
L3	NMOS LDO	1.225	0.750–1.350	0.375–1.5375	1200	Y	VDDMX
L4	PMOS LDO	1.800	1.800	1.750–3.3375	450	N	RFICs and GPS eLNA
L5	PMOS LDO	1.800	1.800	1.750–3.3375	500	Y	Most digital I/Os, MSM pad groups 3 and 7, LPDDR, and eMMC
L6	PMOS LDO	1.800	1.800	1.750–3.3375	300	N	MSM DSI PLL and OTP, camera, touchscreen, display, and sensors
L7	PMOS LDO	1.800	1.800	1.750–3.3375	150	Y	MSM analog and PLLs, WCN XO, and PM baseband clock driver
L8	PMOS LDO	2.900	2.900	1.750–3.3375	600	Y	eMMC
L9	PMOS LDO	Vout = 3.3 V for VBAT > 3.575 V; Vout = 3 V for VBAT < 3.575 V	3.000–3.300	1.750–3.3375	600	N	WCN

Note: S1 SMPS rated current increased to 3000 mA on PM8940 to support the Cat6 modem.

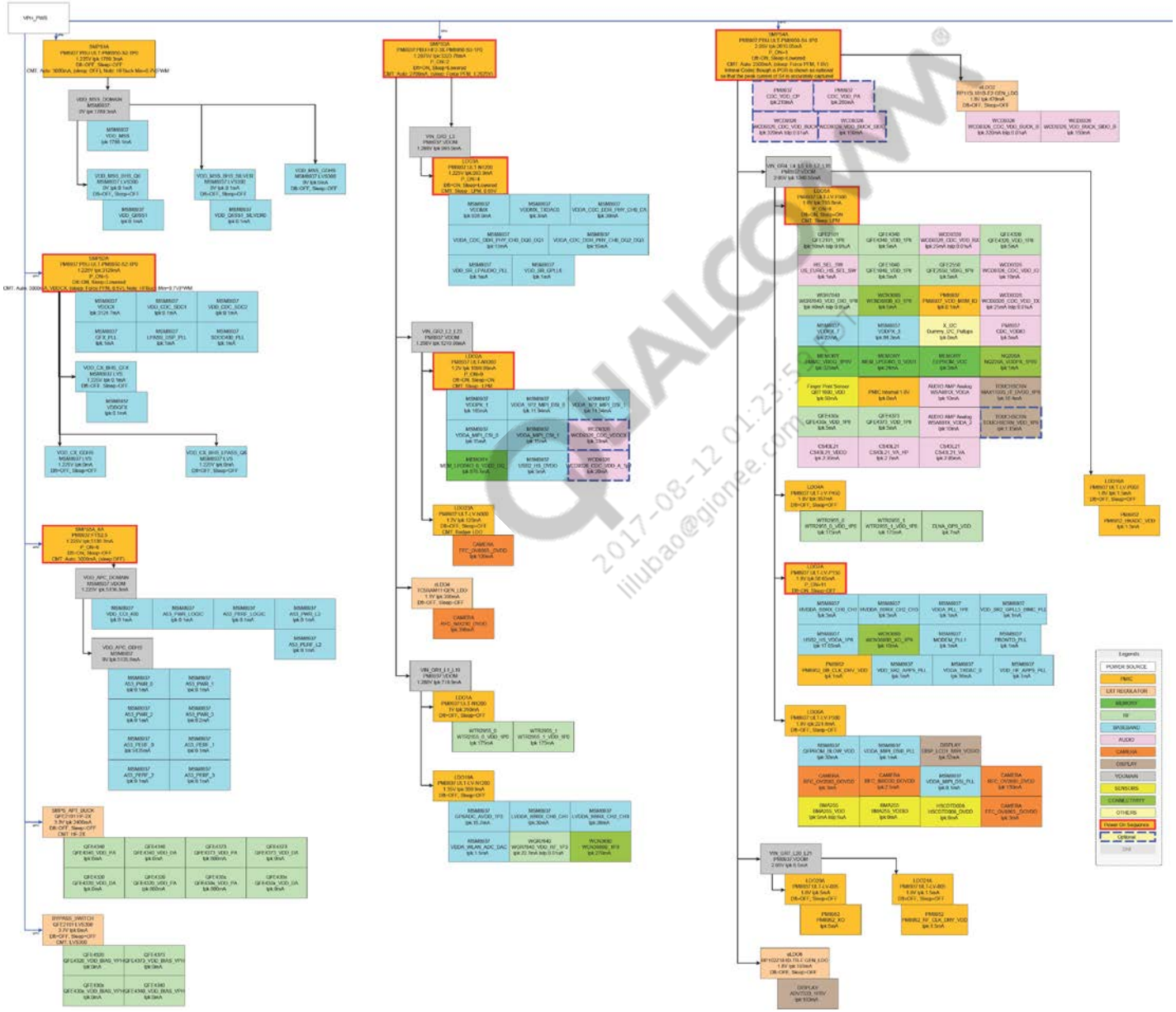
Output Power Management – Summary (2 of 2)

Function	Circuit type	Default voltage (V)	Specified range (V)	Programmable range (V)	Rated current (mA)	Default ON	Expected use
L10	PMOS LDO	2.850	2.800	1.750–3.3375	150	N	Sensors
L11	PMOS LDO	2.950	2.950	1.750–3.3375	800	Y	Micro SD
L12	PMOS LDO	2.950	1.800/2.950	1.750–3.3375	150	Y	MSM pad group 2 and SDC2
L13	PMOS LDO	3.075	3.075	1.750–3.3375	50	Y	MSM USB and audio
L14	PMOS LDO	1.800	1.800/3.300	1.750–3.3375	50	N	MSM pad group 5, dual-voltage UIM1, and NFC
L15	PMOS LDO	1.800	1.800/3.300	1.750–3.3375	50	N	MSM pad group 6 and dual-voltage UIM2
L16	PMOS LDO	1.800	1.800	1.750–3.3375	5	N	PMIC HKADC
L17	PMOS LDO	2.850	2.850	1.750–3.3375	600	N	Camera, display, and touchscreen
L18	PMOS LDO	2.700	2.700	1.750–3.3375	150	N	Qualcomm® Technologies, Inc. (QTI) RF front end
L19	NMOS LDO	1.350	1.350	0.375–1.5375	1200	N	MSM analog, WCN, and WGR
L20	Low-noise LDO	1.800	1.800	1.750–3.3375	5	Y	PMIC XO circuits
L21	Low-noise LDO	1.800	1.800	1.750–3.3375	5	Y	PMIC RF clock buffers
L22	PMOS LDO	2.800	2.800	1.750–3.3375	300	N	Camera – analog
L23	NMOS LDO	1.300	1.200	0.375–1.5375	300	N	Camera – digital

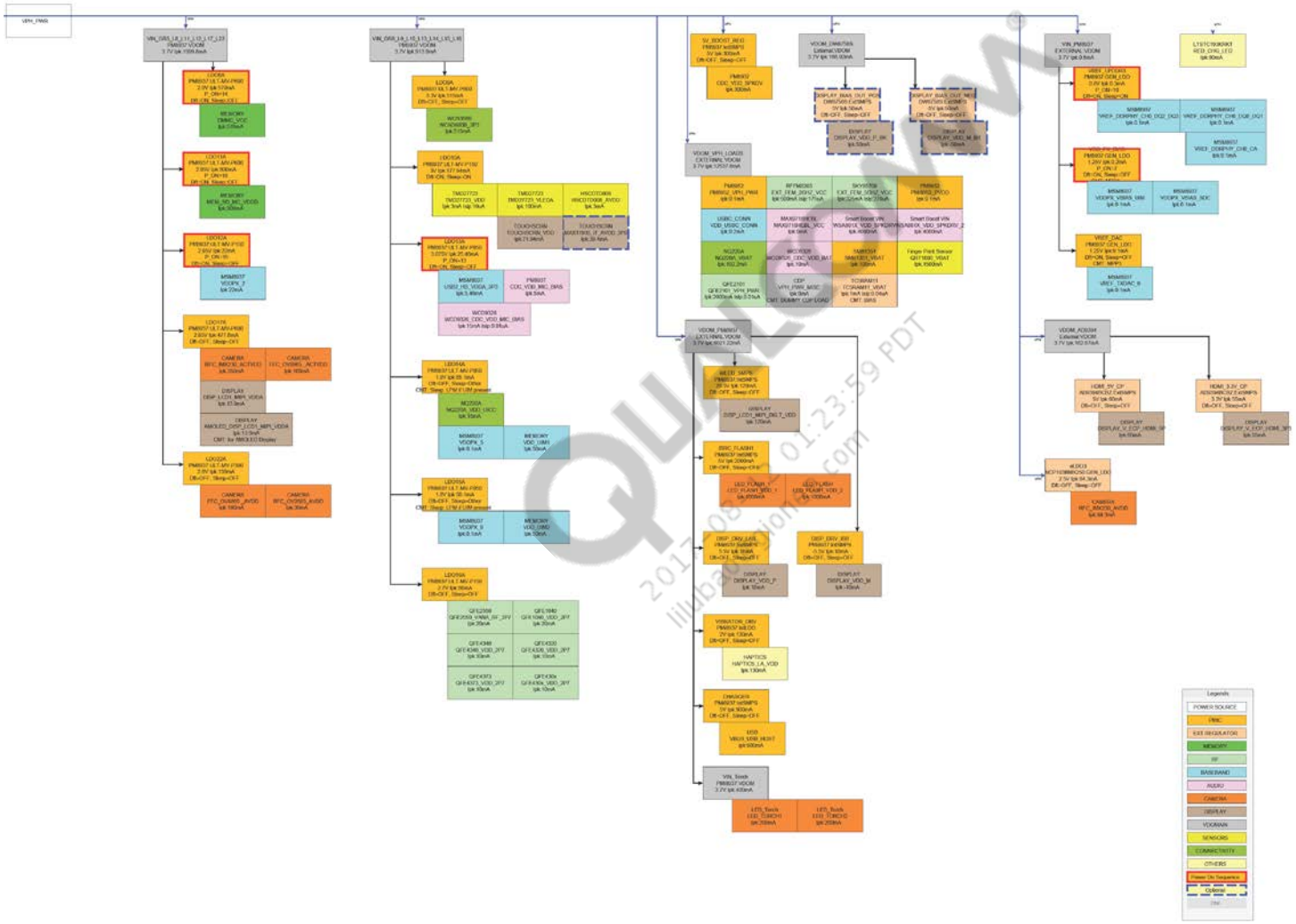
Notes:

- L5 powers internal circuits that are limited to 1.8 V operation; its programmed voltage should not be changed, and it should not be turned off.
- L11, L14, and L15, as well as all PMOS LDOs, have overcurrent protection (OCP).
- All regulators have default voltage settings, whether they default on or not; the voltage and state depends upon the PBS configuration.

Power Grid Information (1 of 2)



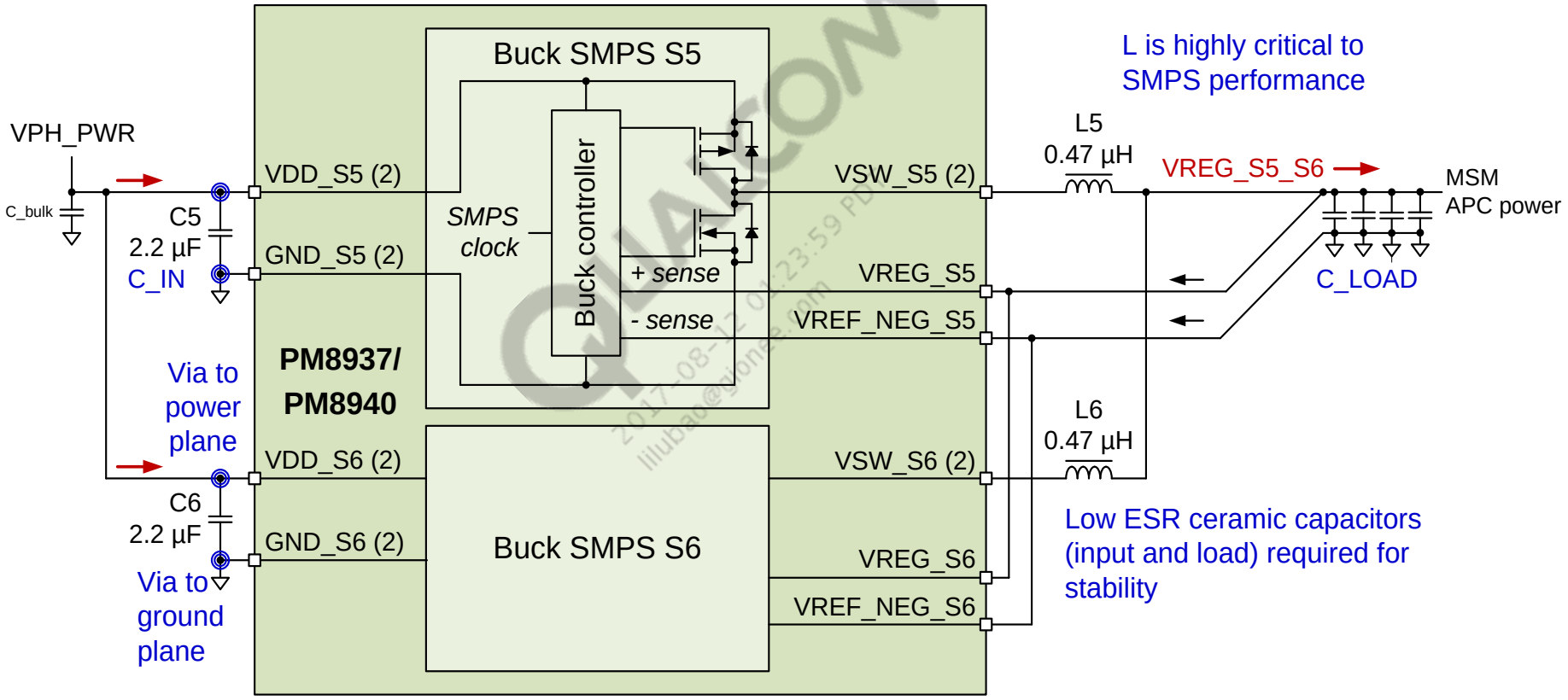
Power Grid Information (2 of 2)



Section 3.1

SMPS S5 and S6

SMPS S5 and S6 Schematic



Note: The PM8937/PM8940 device's S5 and S6 are not multiphase and are not tied together.

SMPS S5 and S6 – Operational Details and Features (1 of 2)

- Tight regulation/extremely fast transient response.
- Transients that are too fast for linear duty cycle control trigger an immediate nonlinear (100% or 0%) response for fast and smooth transitions back into linear control.
- A major benefit of the new SMPS S5 and S6 design is the ability to support multiphase operation with an arbitrary and configurable number of phases; multiphase operation increases the maximum current and transient capability.
  - See the Multiphase SMPS section for details
- New features
  - Autonomous phase control (APC) – while in multiphase operation, the phase count is autonomously managed in the hardware to select the appropriate number of phases for optimal efficiency based on the operative load current
  - Autonomous mode control (AMC) – managed in hardware to select PWM or pulse frequency modulation (PFM) mode based on the operative load current
- Terminology
  - LPM: low-power mode
  - PFM: pulse frequency modulation (control during LPM)
  - NPM: normal power mode
  - PWM: pulse width modulation (control during NPM)
  - AMC: autonomous mode control qualifies transitions into LPM mode; LPM exit qualification is still based on PFM IPLIM events
  - H-PFM: hyper-PFM mode, the transitory state between LPM and NPM
  - APC: autonomous phase control adjusts the phase relationships in multiphase applications
  - See the Other Common SMPS Topics section for descriptions of the SMPS S5, S6 block LPM, and NPM operations

SMPS S5, S6 – Operational Details and Features (2 of 2)

- Remote feedback with differential sensing helps compensate for power delivery network (PDN) impedance on both plus (power) and minus (ground) paths
- Current capability, single phase operation
  - NPM or AMC: 3.0 A continuous (**Note**: SMPS S5 and S6 are expected to be rated for 4 A on validation of physical silicon)
  - LPM: 500 mA continuous
- Current capability, multiphase domain
  - NPM or AMC: 6 A continuous
  - LPM: 500 mA continuous (LPM only supported in single-phase mode)
- Fast transient response
- Phase options: Arbitrary phase count with the software is definable by ganging; phase currents are automatically balanced
- Low voltage (LV, 0.350 V–1.355 V) and mid voltage (MV, 0.700 V–2.200 V) ranges
- Reference voltage DAC with 5 mV LSB (LV range) and 10 mV LSB (MV range)
- Voltage stepper with programmable voltage and time steps
- Switching frequency coverage: 1.6, 3.2 (default), 4.8, and 6.4 MHz
- Voltage limit stops
- VREG_FAULT (OCP event) and LIMIT_ERR (voltage limit/threshold flags)
- OCP based on short-circuit qualification

Improvements Over Previous Generation

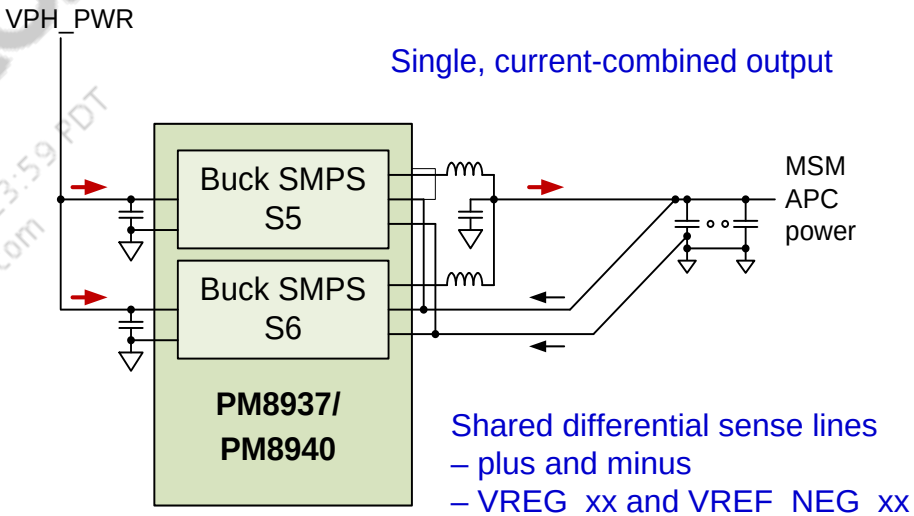
- Current balance is improved on multiphase domains
- Improved auto mode transitions
- Improved duty cycle seeding when phases are added
- APC while in multiphase configuration – phase count is autonomously managed in hardware to select the appropriate number of phases for optimal efficiency based on the operating load current
- AMC is managed in hardware to select PWM or PFM mode based on the operating load current; during multiphase operation, AMC can be enabled to apply when APC takes down the phase count to a single phase
- Reduced PFM consumption – a maximum of 60 µA unloaded current for PFM
- OCP feature – retry, latch off, and PMIC shutdown options
  - Coordinates shutdown with PON
  - Immediate shut down as triggered by OTS3 to minimize system exposure to orphaned power grid, which could result in damage or data corruption

Section 3.2

Multiphase SMPS

Multiphase SMPS – Operational Details and Features (1 of 2)

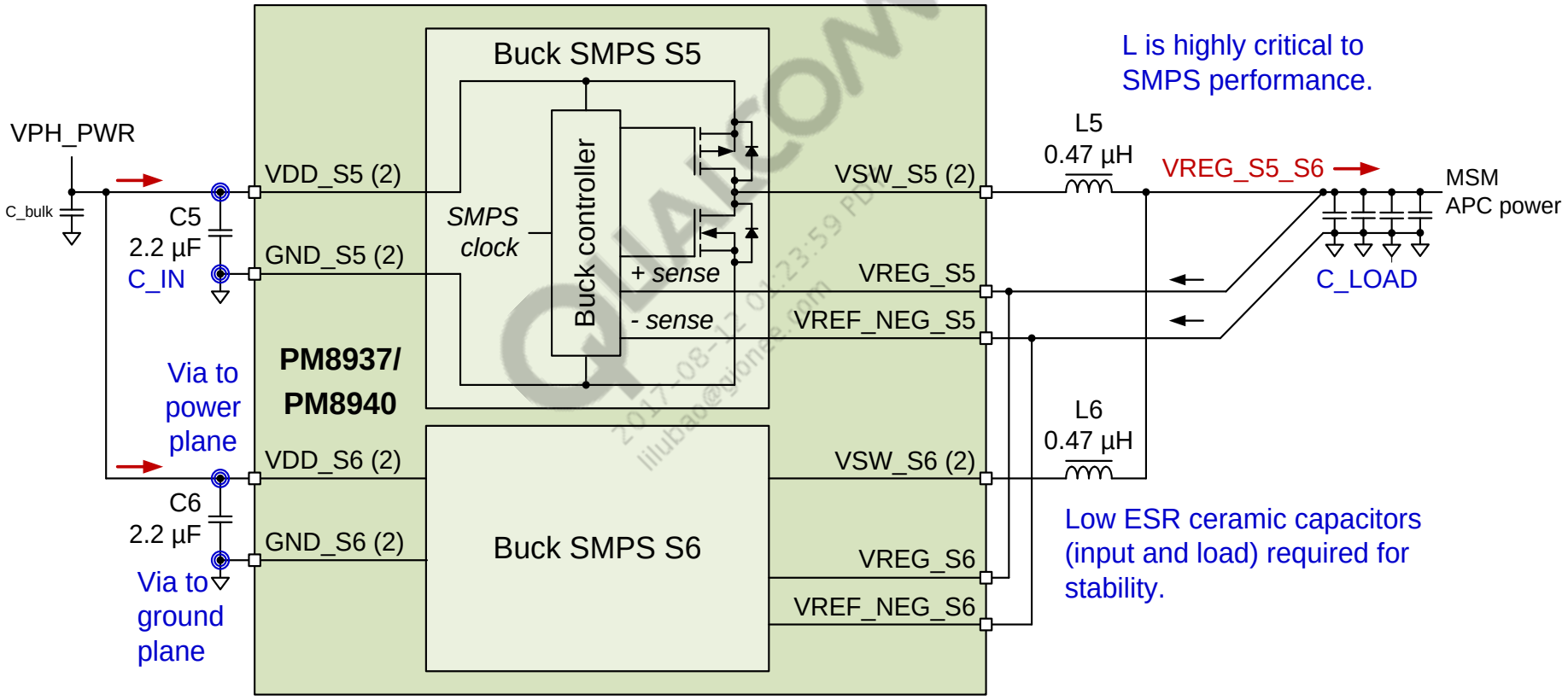
- Phase count blocks can be adjusted dynamically to optimize efficiency based on operating conditions such as load level, maximum load capability, or transient performance.
- Phase count can be changed manually via explicit register control or autonomously using APC.
- As slave phases are enabled, the starting point of each switching cycle is phase-staggered relatively to minimize ripple voltage and spread out current surges drawn from the battery.
- Peak inductor currents in each active phase are digitized and driven for balance across the active phases.



Multiphase SMPS – Operational Details and Features (2 of 2)

- APC
  - Digitizes the phase current to add and shed phases to optimize efficiency vs. load current
  - This scheme maintains high performance while optimizing for steady state efficiency
- AMC
  - Allowed even when multiphase SMPS blocks are used (previous generation only allowed single phase)
- AMC threshold control
  - LPM entry qualification is based on a programmable current threshold, thereby providing flexibility and better control than the previous generation DCM qualification
  - LPM exit qualification is based on PFM IPLIM events (no change)
- High-current PFM mode (HC-PFM)
  - Transitory state between LPM and NPM; maintains regulation with good transient response
  - Does not require the rated load capability to be scaled back when AMC is enabled

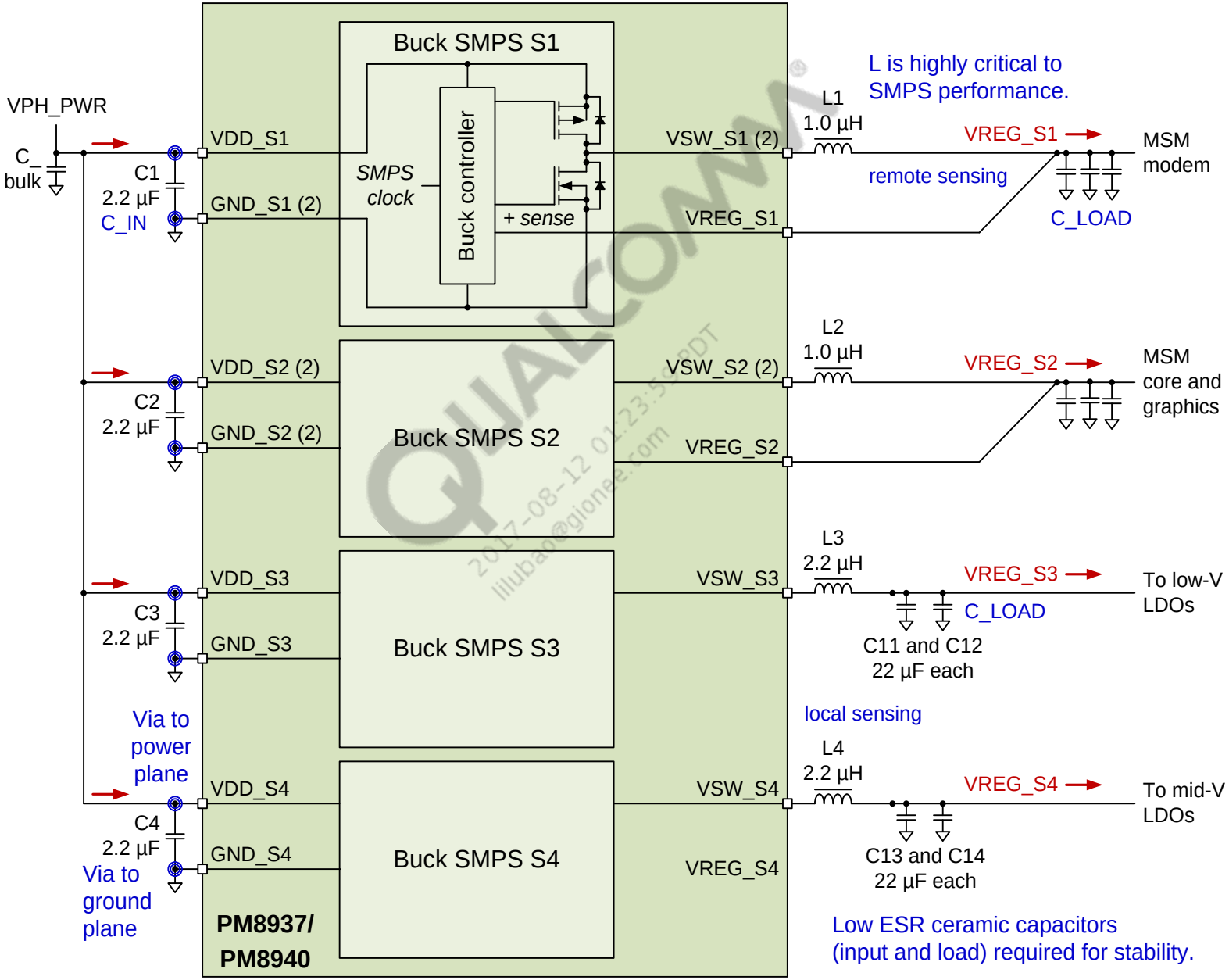
Multiphase SMPS – Schematic



Section 3.3

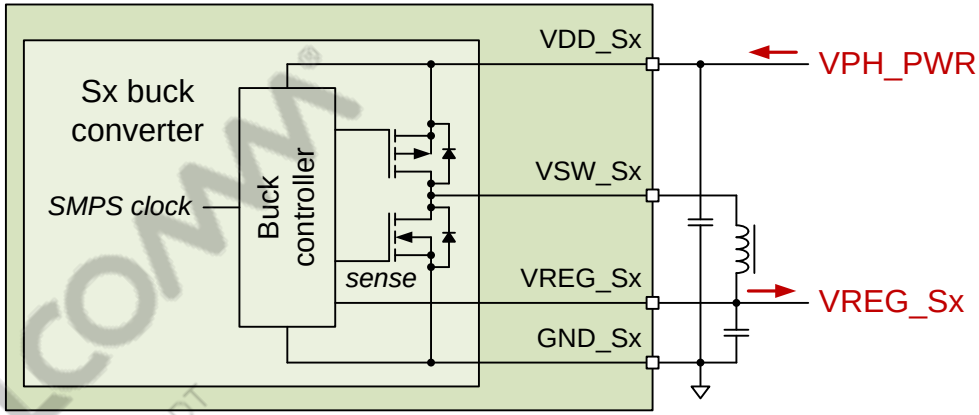
SMPS S1, S2, S3, and S4

PM8937/PM8940 SMPS S1, S2, S3, and S4 Schematic



SMPS S1, S2, S3, and S4 Features and Operation

- Good transient response
- Slow start feature
- Current limiting
- Operating modes
  - PWM
    - Current-mode constant-frequency PWM control
    - Delivers the specified rated current to the load
    - Pulse skipping
  - PFM
    - The power switch is only turned on when the output voltage dips below a threshold
    - Maintains high efficiency even at light loads
  - Auto mode
    - Automatic switching between PFM and PWM modes, based on load current
    - Programmable threshold



SMPS S1, S2, S3, and S4 SMPS OCP

The OCP feature has been implemented to avoid inductor current runaway in Lo-Z faults.

- An overcurrent event is detected when either of the following conditions are met:
  - VREG_Sx drops below the fault voltage threshold (~300 mV) combined with four to eight (programmable) consecutive current limit hits
  - VREG_SNS remains below the fault voltage threshold until a 4 µs backup timer expires
- The OCP turns off SMPS S1, S2, S3, and S4 to protect it against damage.
- To recover, SMPS S1, S2, S3, and S4 must be reset (disable and then enable it).

Section 3.4

Other Common SMPS Topics

SMPS Switching Frequencies and Inductor Recommendations

- SMPS inductors are especially critical to performance and should be selected according to the guidelines found in the *Application Note: Switched-Mode Power Supply (SMPS) Inductor Selection* (80-VC603-9).
- SMPS components and control parameters have been optimized for the switching frequencies given in this table. QTI has characterized and validated the SMPS performance at these switching frequencies, and customers are not permitted to change them.

SMPS	Frequency (MHz)	L (µH)
S1	3.2	1.0
S2	3.2	1.0
S3	1.6	2.2
S4	1.6	2.2
S5	3.2	0.47
S6	3.2	0.47

Other External Component Recommendations

- See the SMPS Switching Frequencies and Inductor Recommendations slide for inductor guidelines.
- See the schematics in each SMPS section for capacitor values.
- Other capacitor selection guidelines
  - C_LOAD ESL values are an important factor in susceptibility to multipulsing, so low-ESL capacitors should be used to achieve the highest efficiency at the lowest usable switching frequency and for the best transient performance at a given frequency.
  - In addition to the input and load capacitors shown in the schematics, 22 µF bulk capacitors should be included on VPH_PWR nodes.
    - PMICs assume that there are 6.3 V, 0603, 22 µF capacitors on each side of the PMIC wherever high current power supplies are routed (typically two or three capacitors that provide an additional charge reservoir for input current pulses).

Notes:

1. The inductors and capacitors used on QTI reference designs should be used; refer to the parts list at the end of the reference schematic for vendors and part numbers. If other parts are used, compare the performance specifications; alternate parts must meet or exceed recommended parts. Thoroughly test and evaluate alternate parts before completing selections.
2. Refer to the *Application Note: Switched-Mode Power Supply (SMPS) Inductor Selection* (80-VC603-9) for SMPS inductor selection guidelines.

Section 3.5

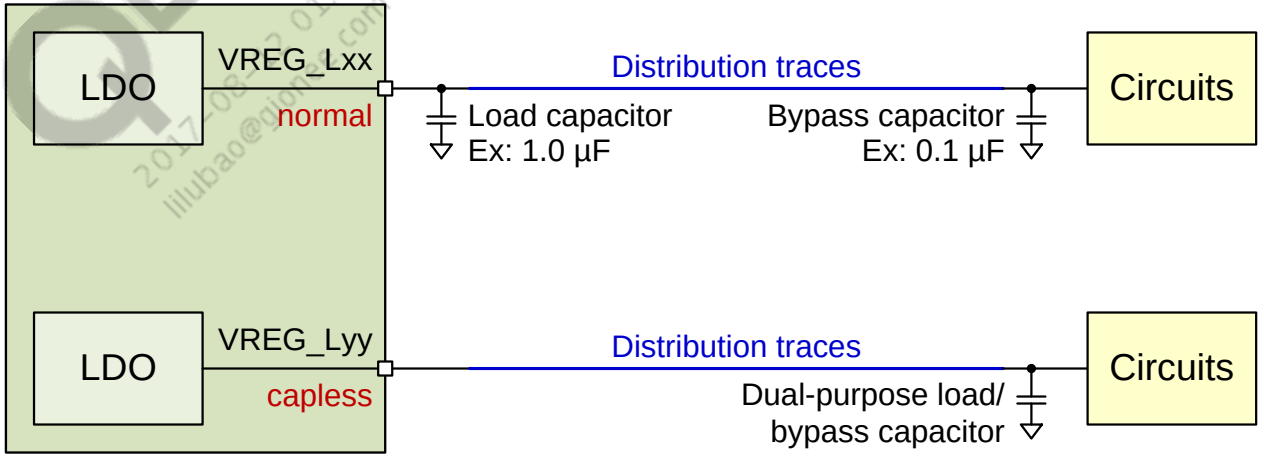
Linear LDO Regulators

LDO Types (Nearby Load Capacitors or Pseudo-capless) and the LDO LPM

- LDOs that do not require load capacitors near the PMIC are called pseudocapless LDOs.
  - The capacitors at the circuits powered by pseudocapless LDOs are sufficient; additional local capacitors are not required.
  - Pseudocapless LDOs have PCB routing requirements that must be met to remove the local capacitor.
- L20 (XO circuits) and L21 (RF clock buffers) are p-type LDOs used to power internal PMIC circuits only – they do not support external circuits so their load capacitors must be located near the PMIC.
- L16 (HK/XO ADC) is a p-type LDO that powers internal PMIC circuits and provides the pull-up voltage for external thermistor networks only – its load capacitor is local.
- L5, L7, and L13 are p-type LDOs that support internal and external circuits – they require 0.1 µF local capacitors plus at least 1.0 µF near the external circuits they power.

Normal load capacitor situation
- Load capacitor at LDO output
- Decoupling capacitor at load

Pseudo-capless situation
- Reduce BOM cost
- Reduce board area

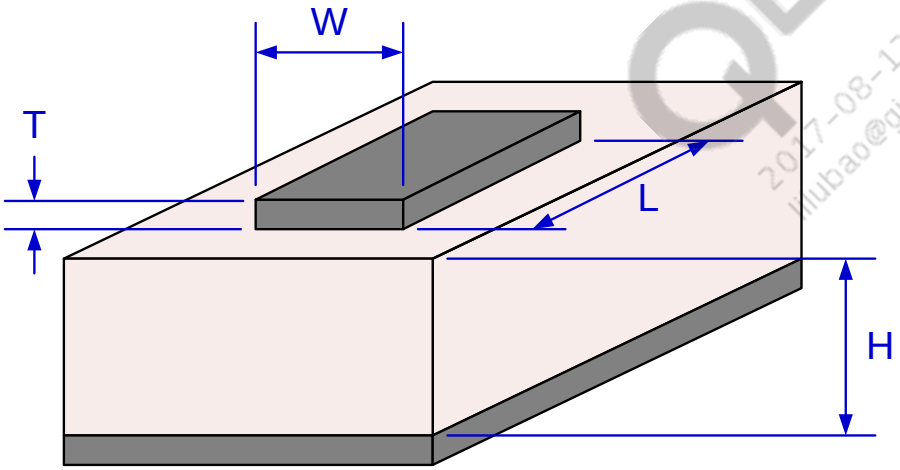


- An LDO implements its LPM by reducing the current of its feedback loop. During low-power operation, the regulator performance is degraded – lower PSRR, less output current capability, and so forth. If the load is greater than 10 mA, the output voltage is likely to be out of specification during LPM.

Pseudocapless Restrictions

Rough guidelines – use worst-case CAD extraction	W (µm)	H (µm)	T (µm)	L (cm)	Trace inductance (nH)	Trace resistance (mΩ)
Long trace carrying 600 mA	1600	90	17	5	4.6	< 30
Long trace carrying 300 mA	1000	90	17	5	5.7	40
Long trace carrying 200 mA	800	90	17	5	7.05	60
Long trace carrying 100 mA	400	90	17	5	14.1	120
Long trace carrying 25 mA	100	90	17	5	56.5	480

Recommendation: When a pseudocapless LDO powers a circuit that is located within 5 cm of the LDO output pin, combine the PMIC load capacitor value and the circuits bypass capacitor value and place a single equivalent capacitor near the circuit.



W = trace width
L = trace length
T = trace thickness
H = dielectric heighth

Internal Regulator Connections

Some regulated outputs are used to power internal PMIC circuits. These regulators must be enabled and set to their default values for proper PMIC operation.

Pin	Default	Usage	Comments
VREG_L2	1.200 V	MPPs and GPIOs	Also loaded externally
VREG_L5	1.800 V	Digital I/Os, MPPs, and GPIOs	Also loaded externally
VREG_L7	1.800 V	Baseband clock drivers	Also loaded externally
VREG_L13	3.075 V	Microphone bias	Also loaded externally
VREG_L16	1.800 V	AMUX and HK/XO ADC circuits	Plus thermistor networks only
VREG_XO	1.800 V	XO circuits	Do not load externally
VREG_RFCLK	1.800 V	RF clock output buffers	Do not load externally

Section 4

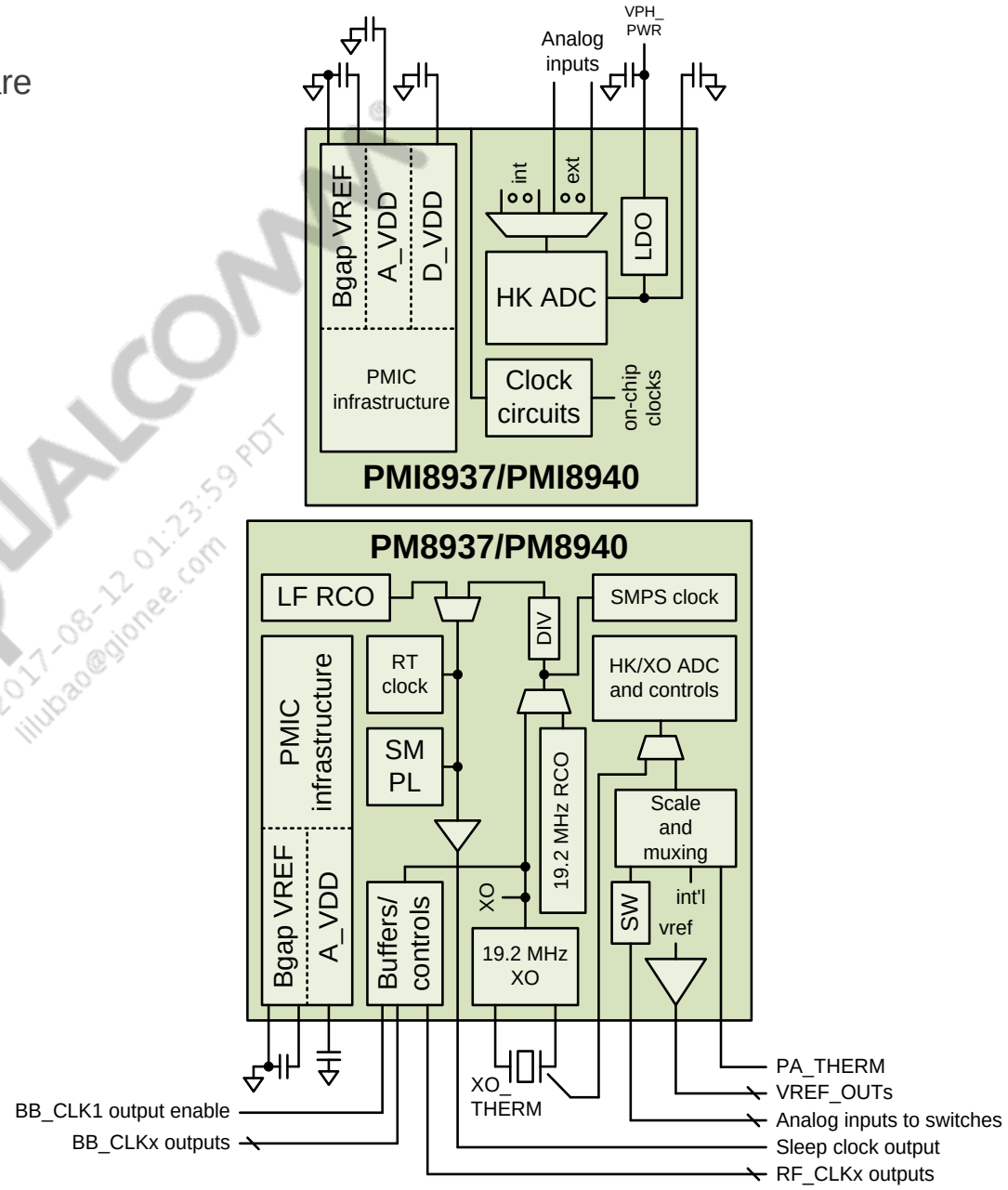
General Housekeeping

General Housekeeping

Almost all general housekeeping functions are provided by the PM8937/PM8940 device.

General housekeeping includes:

- Analog multiplexer (AMUX) and ADC
- Clocks
  - 19.2 MHz XO
  - Sleep clock
  - Other on-chip clock functions
- System-wide clock distribution
- Overtemperature protection
- Automatic fault protection (AFP)
- IC infrastructure



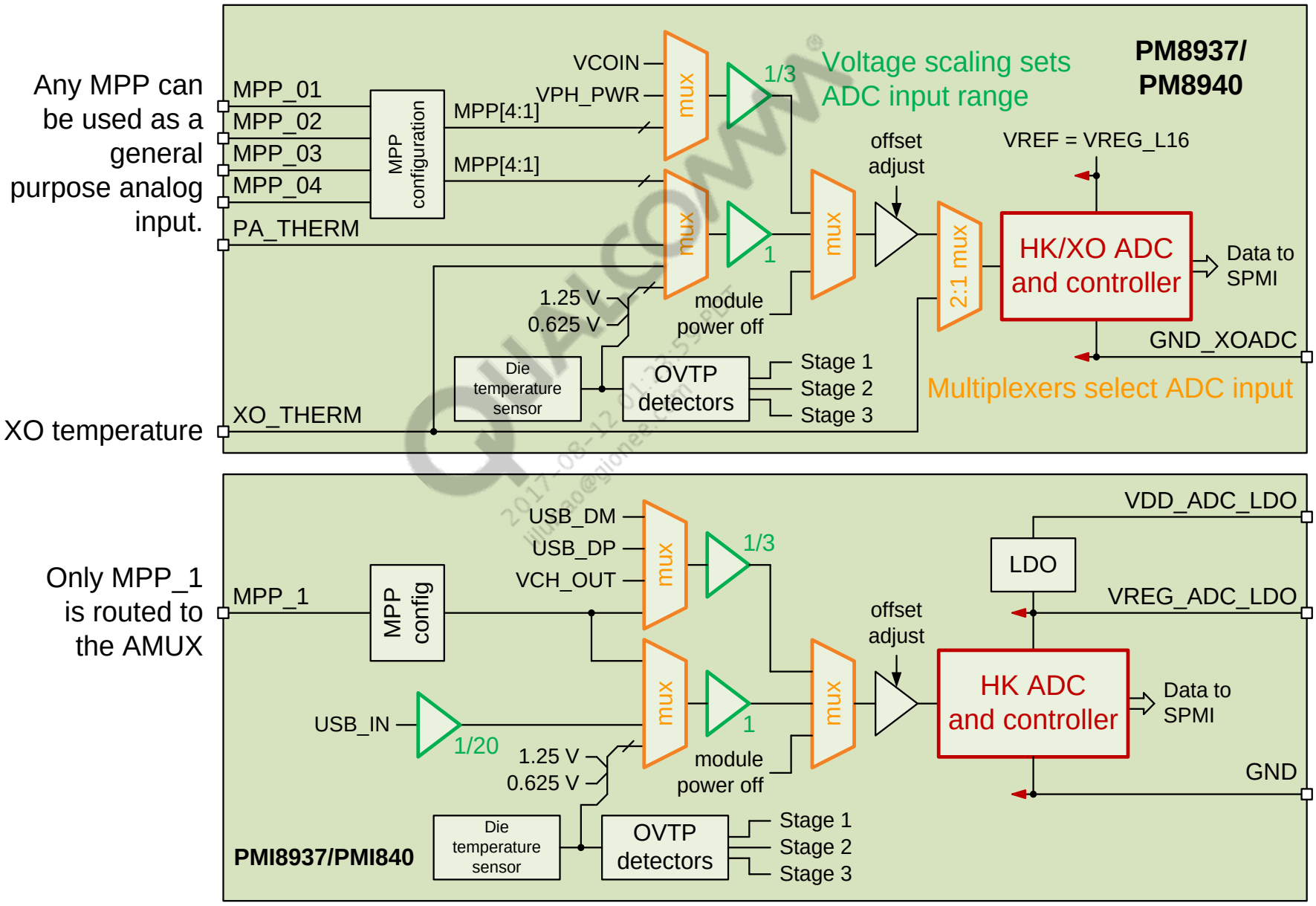
Section 4.1

AMUX and HK/XO ADC

AMUX and Scaling Circuits (1 of 3)

- Several analog switches and multiplexers select one signal for ADC conversion.
- Nestled within the multiplexers are voltage scaling circuits that condition the signals to best use the ADC's dynamic range.
- The selected signal allows handset software to monitor various voltage nodes, auxiliary inputs, and the die temperature using a single ADC.
- Gain and offset errors vary between multiplexer channels; calibration values apply to the specific channel being calibrated only. Calibrate each channel separately.
- Refer to the *PM8937/PM8940 Power Management IC Device Specification* (80-P2564-1) for the ADC and scaling circuits specifications.

AMUX and Scaling Circuits (2 of 3)



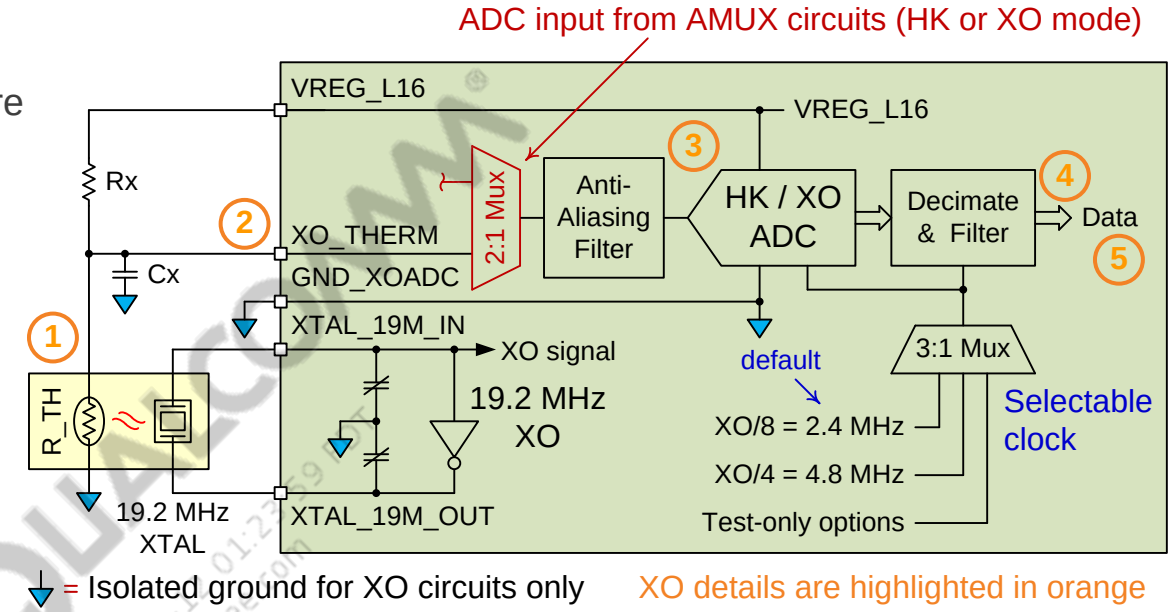
AMUX and Scaling Circuits (3 of 3)

Channel	Description	Typical input range (V)	Scaling	Typical output range (V)
0–3	–	–	–	–
4	–	–	–	–
5	VCOIN pin	2.0–3.25	1/3	0.67–1.08
6	–	–	–	–
7	VPH_PWR pin	2.5–4.5	1/3	0.83–1.50
8	Die-temperature monitor	0.4–0.9	1	0.4–0.9
9	0.625 V reference voltage	0.625	1	0.625
10	1.25 V reference voltage	1.25	1	1.25
11	–	–		–
12	Buffered 0.625 V reference voltage	0.625	1	0.625
13	–	–	–	–
14–15	GND_REF and VDD_ADC	Direct connections to ADC for calibration		
16–19	Pins MPP_01–MPP_04	0–1.7	1	0–1.7
20–31	–	–	–	–
32–35	Pins MPP_01–MPP_04	0.3–4.5	1/3	0–1.7
36–49	–	–	–	–
50	XO_THERM pin direct	0.1– (VL8-0.05)	1	0.1– (VL8-0.05)
51–59	–	–	–	–
60	XO_THERM through AMUX	0.1– (VL8-0.05)	1	0.1– (VL8-0.05)
61–62	–	–	–	–
63	Module power off	–	–	–

HK and XO ADC Circuits

XO operation details

1. Thermistor detects crystal temperature
2. Analog voltage into PMIC is proportional to crystal temperature
3. The analog voltage is filtered and converted to the digital domain
4. Digital data is transferred to the modem IC via SPMI
5. Modem IC algorithms compensate for errors/drift vs. cellular network
   - Data format: 2 s complement; 16 bits (sign + 15-bit data)



• **Sigma-delta (ΣΔ) type ADC** • **High accuracy** • **Slow conversion and filtering**

Clock rate, decimation rate, and conversion time

Clock	Decimation ratio	Update rate	Conversion time	Clock	Decimation ratio	Update rate	Conversion time
2.4 MHz	512	2.26 kHz	0.442 ms	4.8 MHz	512	4.38 kHz	0.228 ms
	1024	1.15 kHz	0.868 ms		1024	2.26 kHz	0.442 ms
	2048	580 Hz	1.722 ms		2048	1.15 kHz	0.868 ms
	4096	290 Hz	3.428 ms		4096	580 Hz	1.722 ms

The decimation filter can be enabled (Sinc1 and Sinc2) or disabled; the examples given above are with the filter enabled.

Section 4.2

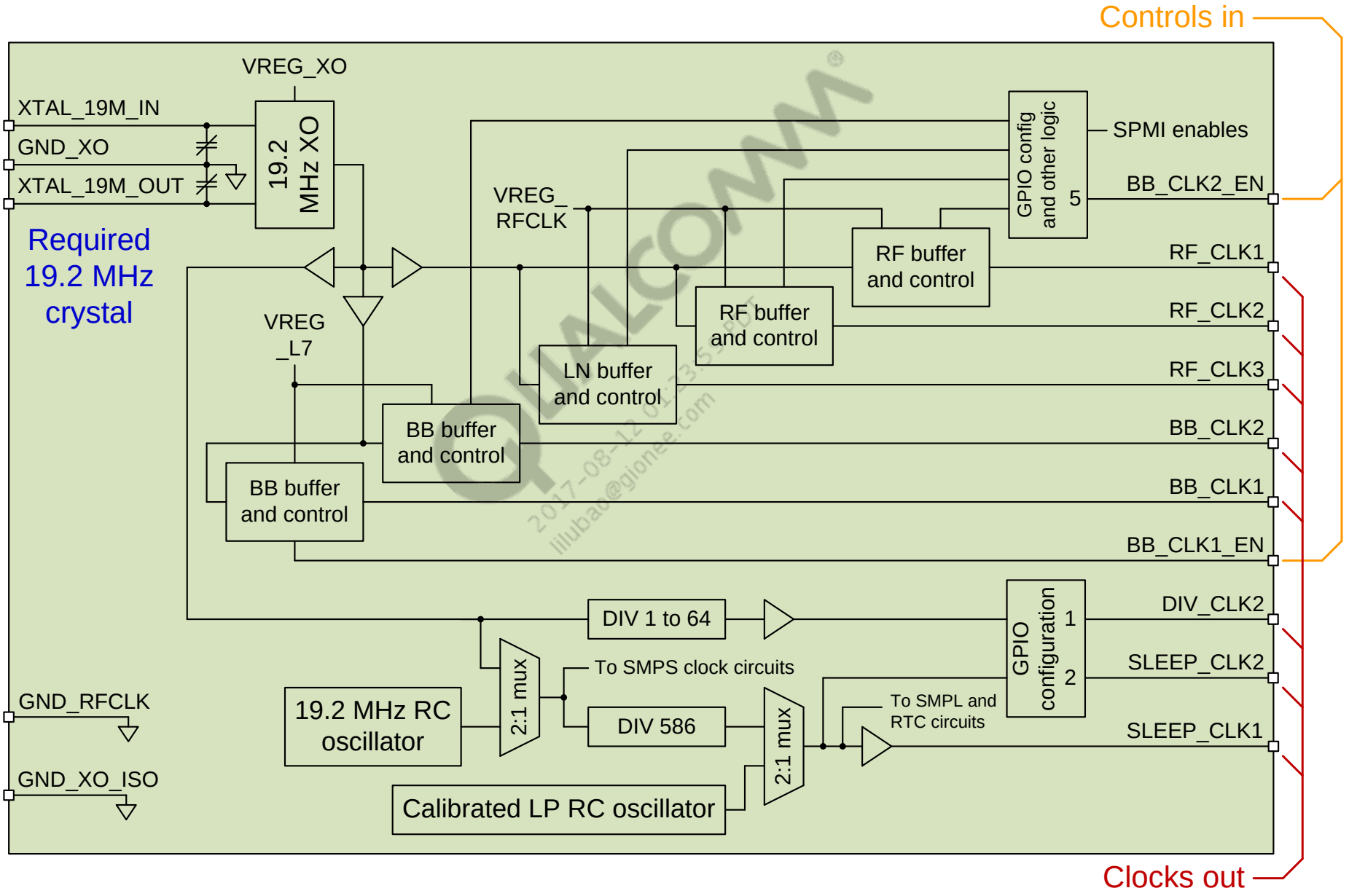
Clock Sources, Uses, and Distributions

PM8937/PM8940 Clocks (1 of 2)

Several PM8937/PM8940 clocks and clock outputs are used for general housekeeping functions and elsewhere throughout the system.

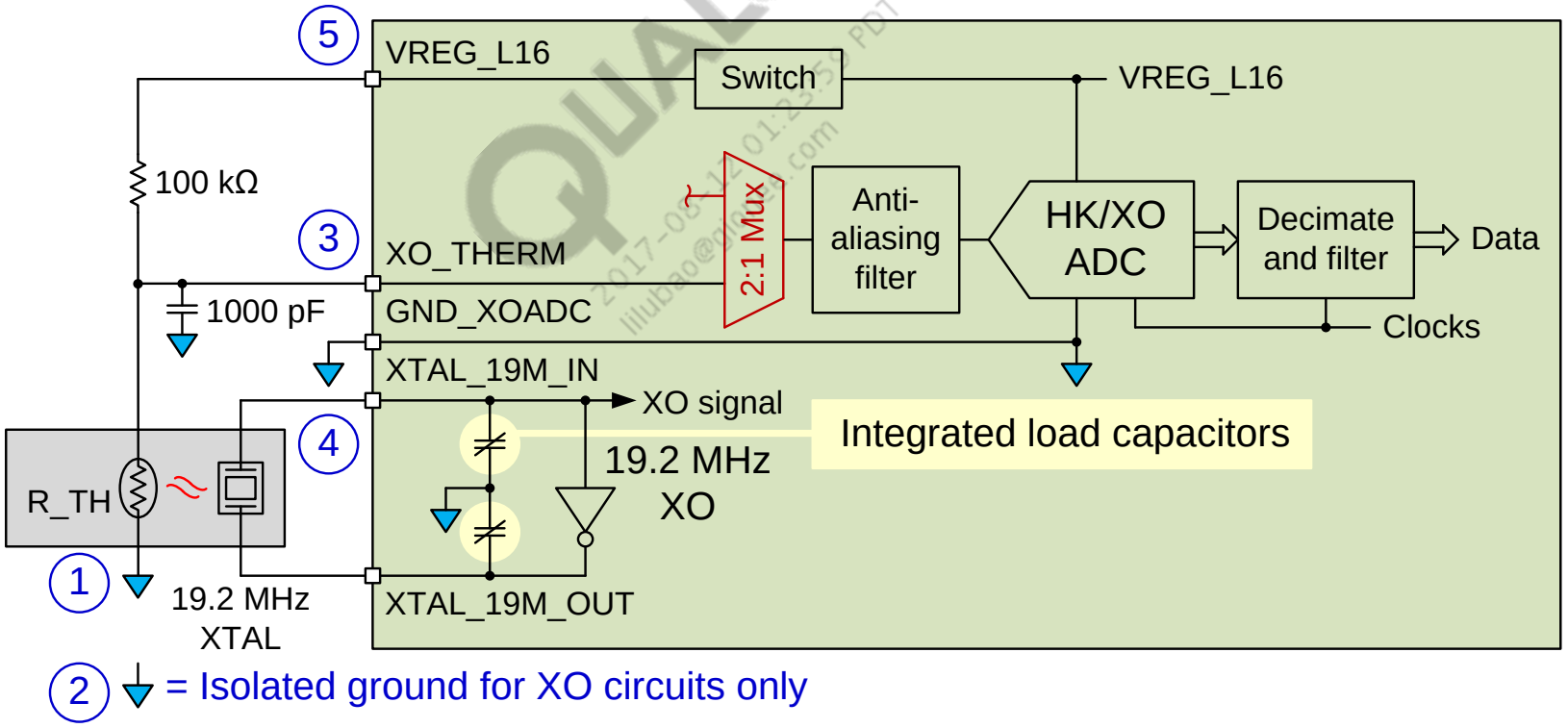
- 19.2 MHz crystal oscillator (XO) circuit, the systems master clock
- Several system clock controller/buffer circuits
  - Two for RF circuits (RF_CLK1 and RF_CLK2 for WTRs, WCN, and so forth.)
  - Two for low-power digital baseband circuits (BB_CLK1 for MSM digital system CXO input, BB_CLK2 for NFC, and so forth.)
  - One low-noise baseband clock (LN_BB_CLK)
- Divided and buffered clocks support internal functions (SMPS, sampling, and so forth.)
- Divided and buffered clocks are available at high-speed GPIO ports [1:0]
- 19.2 MHz RC oscillator for power-up and emergency backup
- Calibrated low-frequency RF oscillator
- The sleep clock is divided down from the XO or uses a calibrated low-frequency RC oscillator (also supports the RTC)
- Buffered SLEEP clock output, plus configurable GPIOs for additional ports

PM8937/PM8940 Clocks (2 of 2)



19.2 MHz XO Source – Schematic

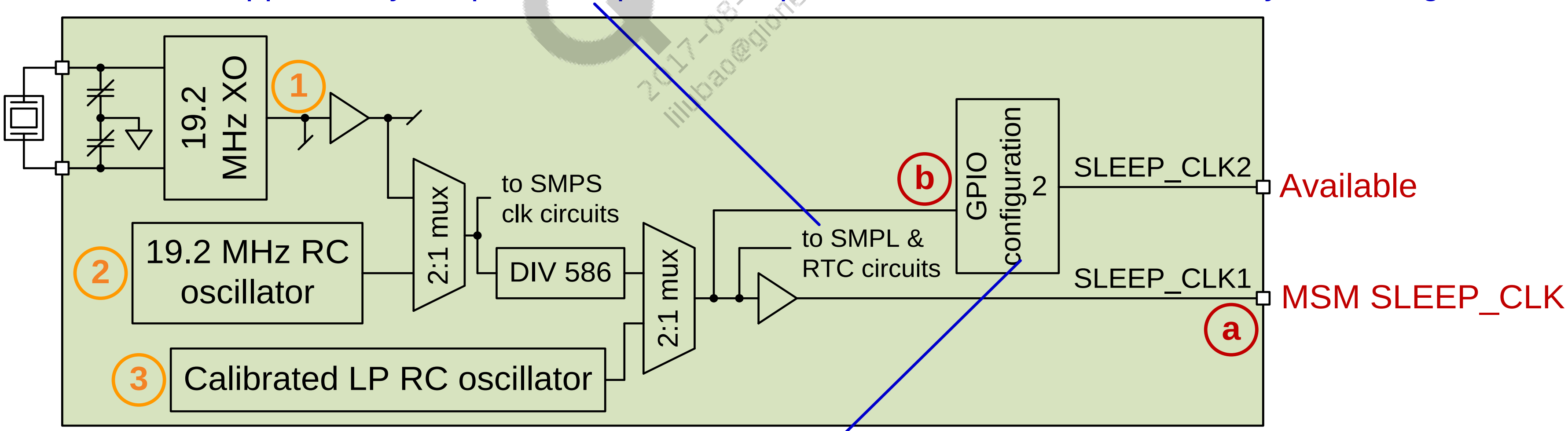
1. The thermistor is integrated into the same package as the crystal.
2. Ground connections are critical to thermal management (refer to the layout guidelines document).
3. The output of the thermistor network is XO_THERM – the node between the resistor and the thermistor; this analog voltage is routed directly to the XO/HK ADC.
4. The XTAL_19M_IN and XTAL_19M_OUT nodes must not be loaded by external circuits. The PMIC provides other outputs for driving external loads.
5. The thermistor network and ADC circuits use the same voltage (VREG_L16).



1. Output options (red; a and b below)
   - A. A dedicated output pin (SLEEP_CLK1) for the modem IC; it toggles only when the PMIC is on and stays low when the device is off, even though the oscillator continues to run.
   - B. GPIOs can be configured as sleep clock outputs to support other functions.
2. Source options (orange) – listed in order of best accuracy
   - A. 19.2 MHz XO (1)
   - B. 19.2 MHz RC oscillator (2)
   - C. Calibrated low-power RC oscillator (3)

See the System-wide Clock Distribution slide or more information.

- SMPL is supported even if the only power source is a keep-alive capacitor at VCOIN.
- RTC is not supported by keep-alive capacitor; requires coin cell when main battery is missing.



GPIO pad voltages are configurable; two GPIOs are designed to support high clock rates and fast transitions; see the *Configurable I/Os* section.

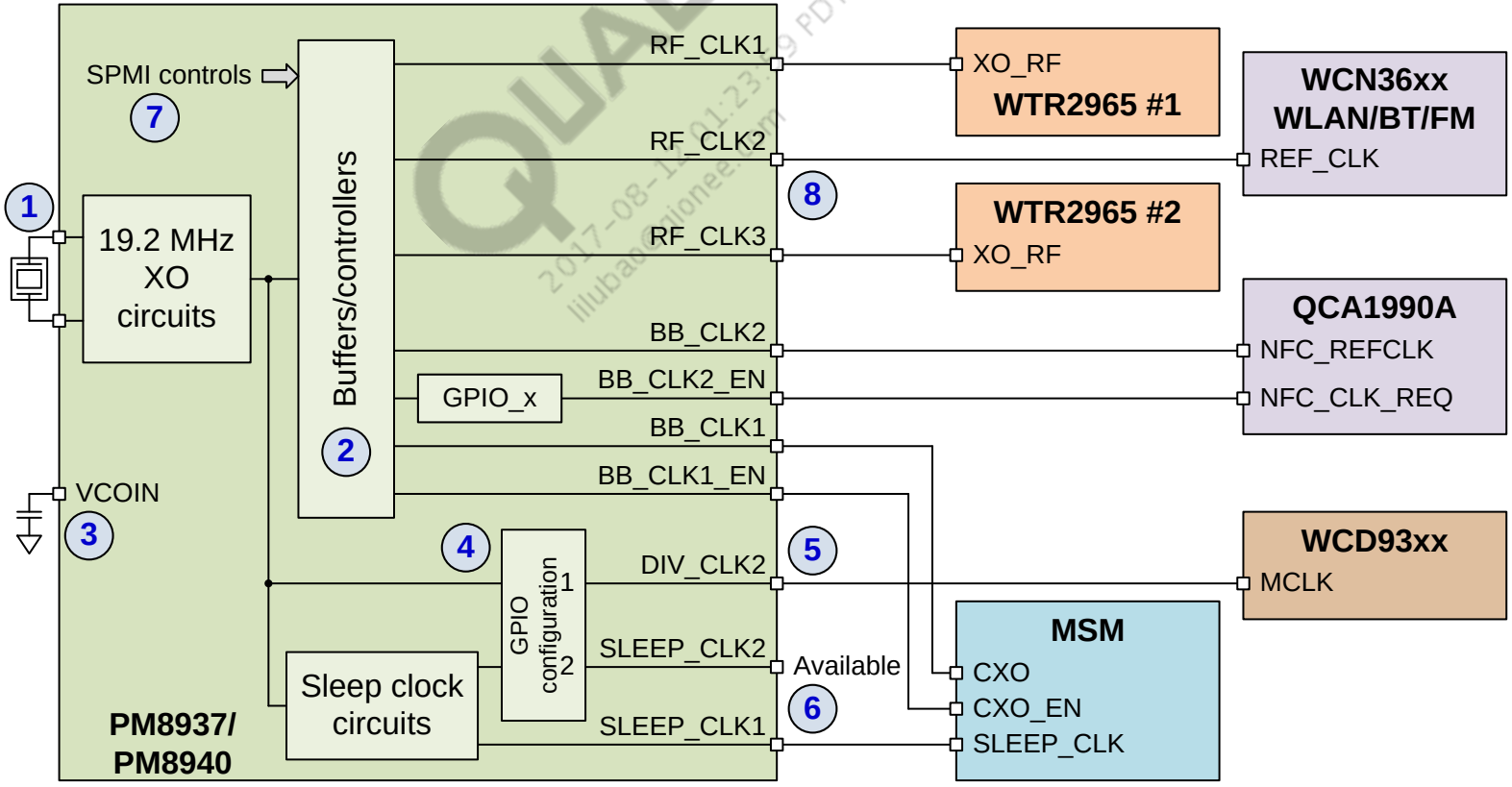
External Clock Components

The reference designs use the NDK America EXS00A-CS04338 as the 19.2 MHz crystal with an integrated thermistor. Refer to the document *19.2 MHz Modem Crystal Qualification Requirements and Approved Suppliers* (80-V9690-19) for the following information:

- Data needed from crystal suppliers to demonstrate compliance
- Approved suppliers for different crystal configurations
  - 2.0 mm × 1.6 mm package with integrated thermistor
  - 2.5 mm × 2.0 mm package with integrated thermistor
  - 2.5 mm × 2.0 mm package with pin 2 ground, pin 4 floating
  - 2.5 mm × 2.0 mm package with pins 2 and 4 ground
  - 3.2 mm × 2.5 mm package
- Discussion of various schematic options

System-wide Clock Distribution

1. A single 19.2 MHz crystal can be a source for the entire system.
2. Clock drivers have a 50 Ω output impedance.
3. The RTC is backed up with a coin cell or capacitor.
4. More clocks are available at GPIO ports than were used in this example.
5. DIV_CLK outputs are available at the 19.2 MHz XO rate, or divided by 1, 2, 4, 8,16, 32, and 64.
6. Low-power baseband clocks have tight duty cycle values near 50%.
7. The clock outputs can be controlled by software (via SPMI) or by dedicated hardware enable signals.
8. Low-noise clocks are available for RF circuits, such as WTR and WCN ICs.



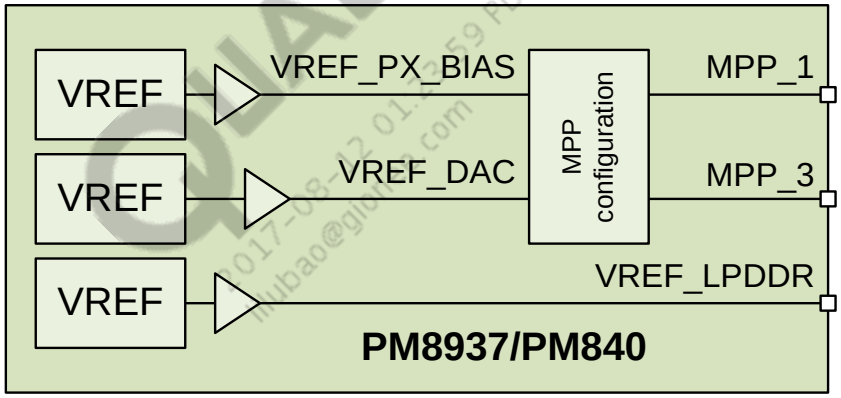
Section 4.3

Voltage Reference and Overtemperature Protection

Voltage Reference Outputs

Certain pins can be configured as reference outputs. This figure provides a block diagram of the available references.

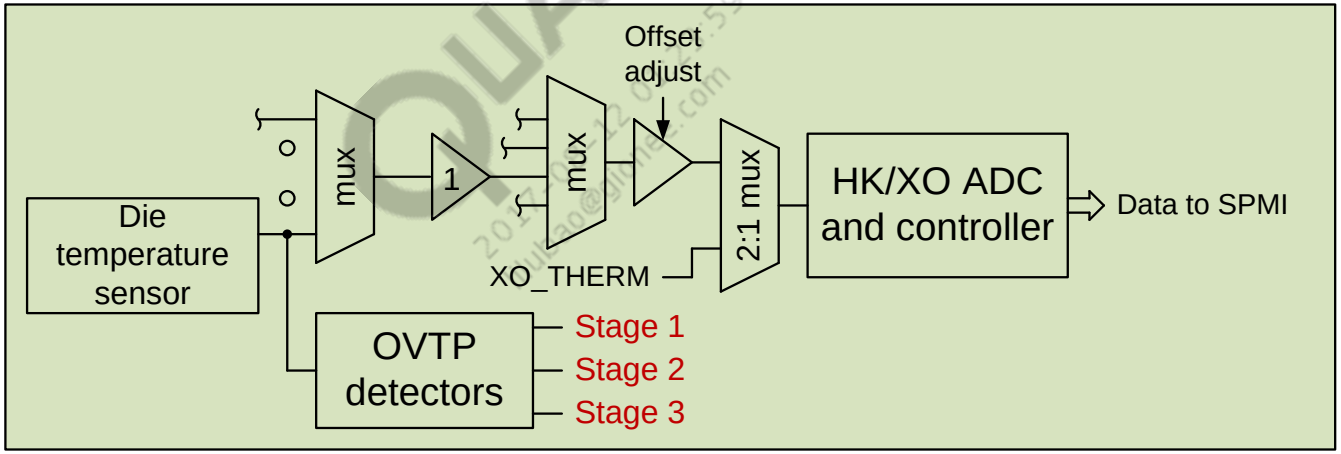
Only odd numbered MPPs can be used as buffered reference voltage outputs.



Overtemperature Protection

Each PMIC provides overtemperature protection in stages, depending on the level of urgency as the die temperature rises.

- Stage 0: Normal operating conditions (less than 110°C); no interrupt is generated
- Stage 1: 110°C–130°C; interrupt sent to the modem IC without shutting down any PM circuits
- Stage 2: 130°C–150°C; an interrupt is sent to the modem IC, and high-current drivers (LED drivers, backlight drivers, and so forth.) are shut down.
- Stage 3: Greater than 150°C; an interrupt is sent to the modem IC, and PM functions are completely shut down.



Temperature hysteresis is incorporated so the die temperature can cool significantly before the device can be powered on again.

- If any start signals are present while at stage 3, they are ignored until stage 0 is reached.
- When the device cools enough to reach stage 0 and a start signal is present, the PM circuits power up immediately.

AFP

The AFP feature protects the system from damage due to a catastrophic event such as:

- Water leakage into the handset
- Handset overheating due to component failure

In AFP mode, the PMI reverses the direction of the BATFET's body diode, thereby isolating VPH_PWR from VBAT and preventing any power delivery to the system. The PMIC can be put into AFP mode by the software or the hardware.

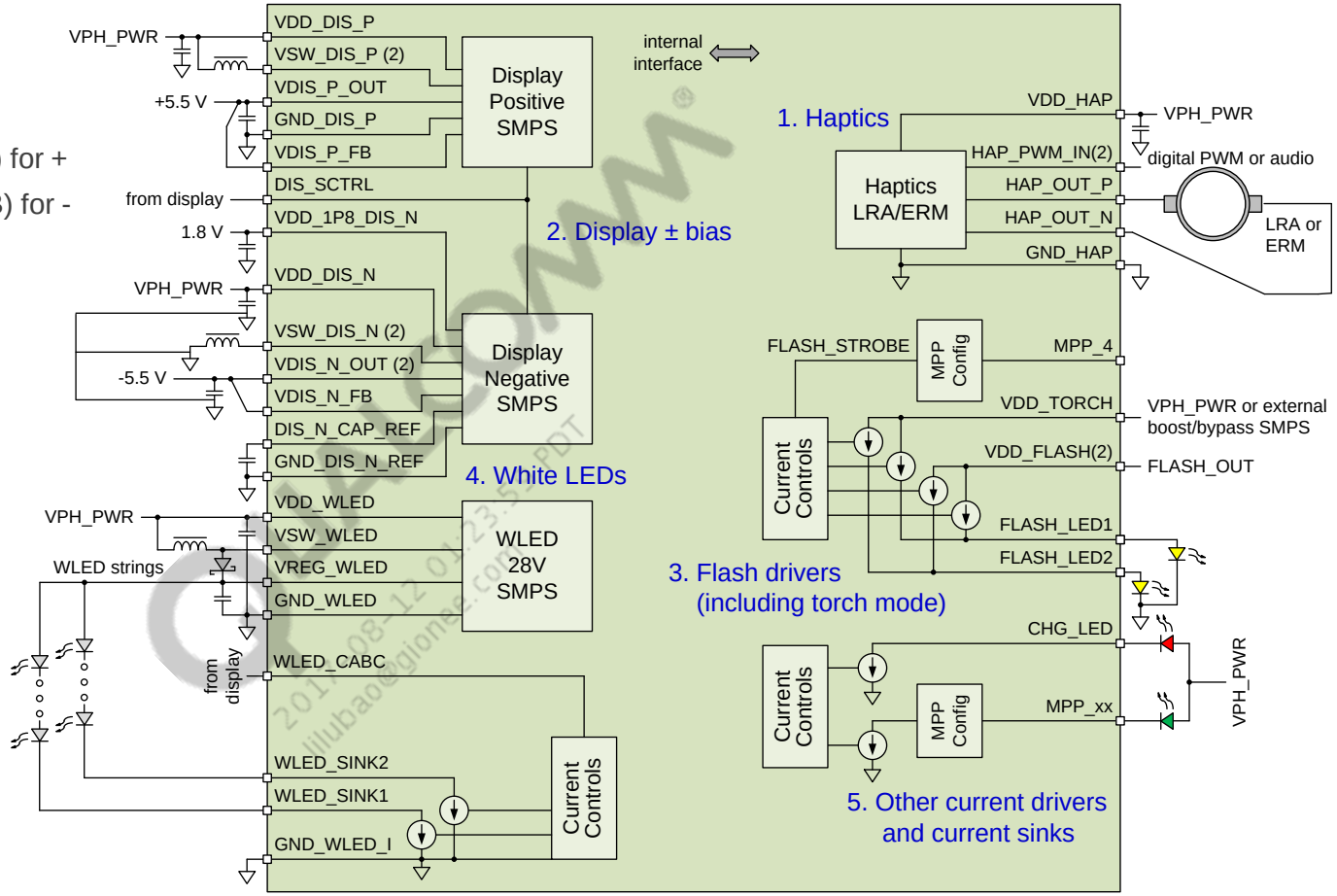
- Upon detection of a fault, the software can force the PMIC to enter AFP mode.
- If software is nonoperational, the PMIC can still enter AFP mode via the watchdog timer.

Section 5

PMI8937/PMI8940 User Interfaces

User Interfaces

1. Haptics
2. Display ±bias
   A. LCD/AMOLED boost (LAB) for +
   B. B.Inverting buck/boost (IBB) for -
3. Flash and torch drivers, independent supplies
4. White LED
   A. SMPS
   B. Current sinks
5. Other current sinks/drivers
   A. Charging indicator driver
   B. MPPs as current sinks



Note: Display bias is not available in PMI8937

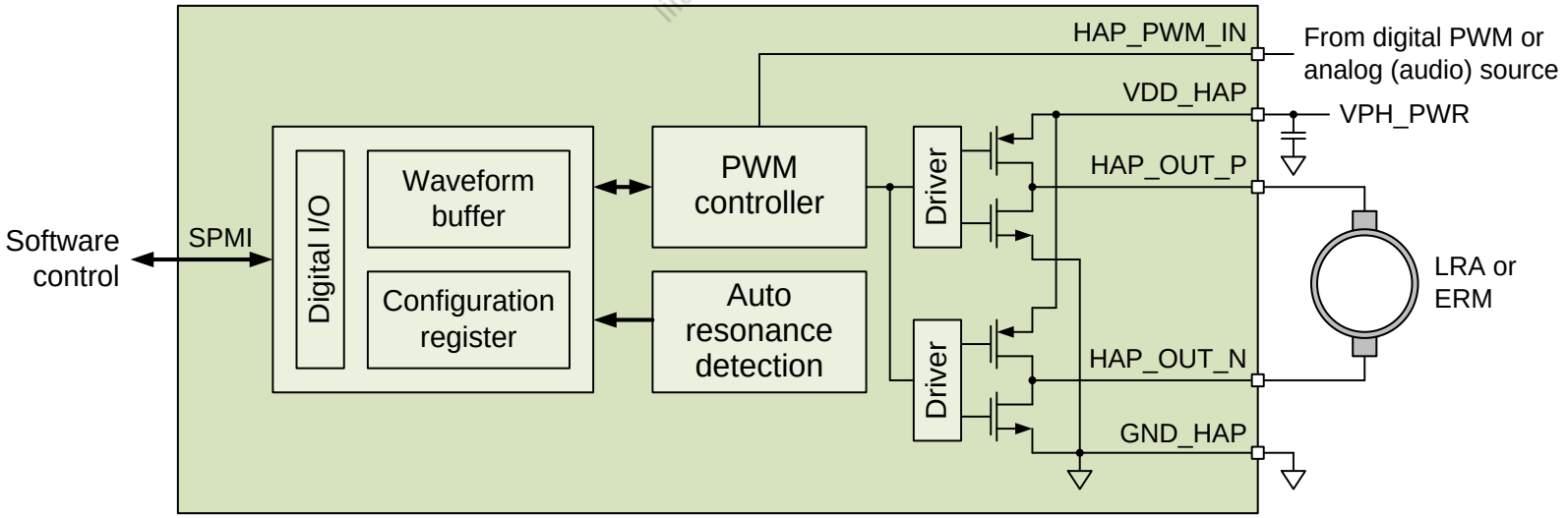
Section 6

Haptics

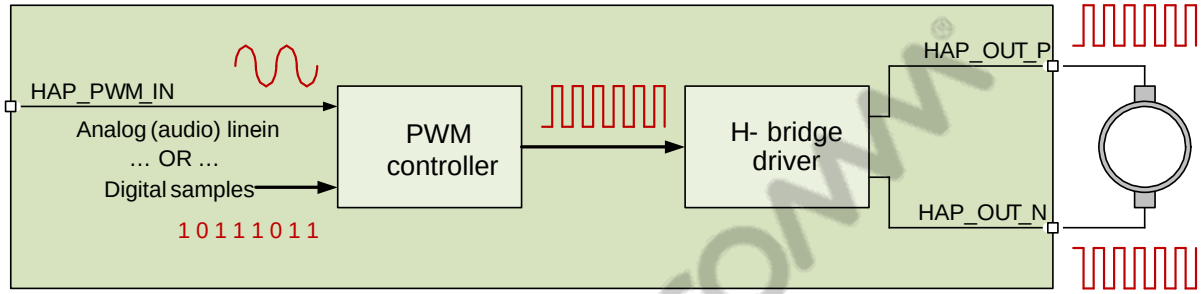
Haptics

Haptics uses vibration to communicate an event or action through human touch. In a mobile phone, haptics is used to simulate the feeling of a real mechanical key by providing tactile feedback to the user as confirmation of touch screen contact, or dynamic feedback to enhance the users gaming experience. Key features include:

- Software-selectable linear resonant actuator (LRA)/eccentric rotating mass (ERM)
- Supply voltage correction for direct connect to phone power; wide input voltage range from 2.5–5.5 V
- Dedicated pin for analog line input and external PWM
- PWM H-bridge drive with 500 mΩ (typical) RDS_ON for high efficiency, programmable from 250–1000 kHz
- Programmable maximum output driver voltage from 1.2–3.6 V to cover wide range of ERM/LRA
- 8 bytes internal waveform buffer for storing and playing haptics patterns; loop function for repeating patterns
- Auto resonance detection for LRA with wide tracking range; programmable range from 50–300 Hz
- Overcurrent/short-circuit protection
- Improved starts and stops with overdrive and reverse braking



Haptics Control (1 of 4)

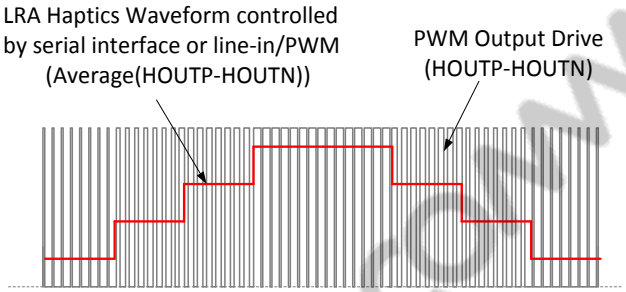


- H-bridge driver can set a PWM output with a configurable amplitude of 1.2–3.6 V. This allows simple vibration and/or complex patterns, depending on the product's needs
- Waveform input as digital samples from buffer or as analog signal from line-in, converted to a PWM signal
- ERM is a DC motor with off-centered mass – requires DC drive signal
- LRA is a resonator – requires AC drive signal
- Haptics driver automatically configures signaling based on software-selected actuator type; enables the same software-generated patterns for both LRA and ERM
- Software only controls the haptics waveform pattern; it is the haptics controller that generates the actual drive signal

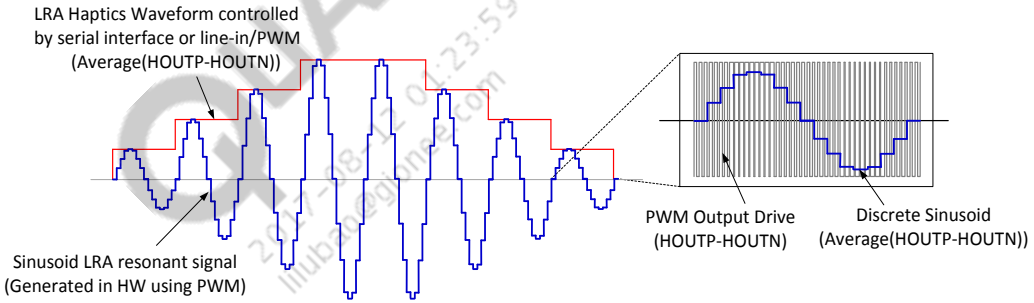
For LRA, haptics driver supports both sinusoid and square drive signal which can be configured from SW. Sinusoid signal is discrete in nature with 4 levels per quadrant.

Haptics Control (2 of 4)

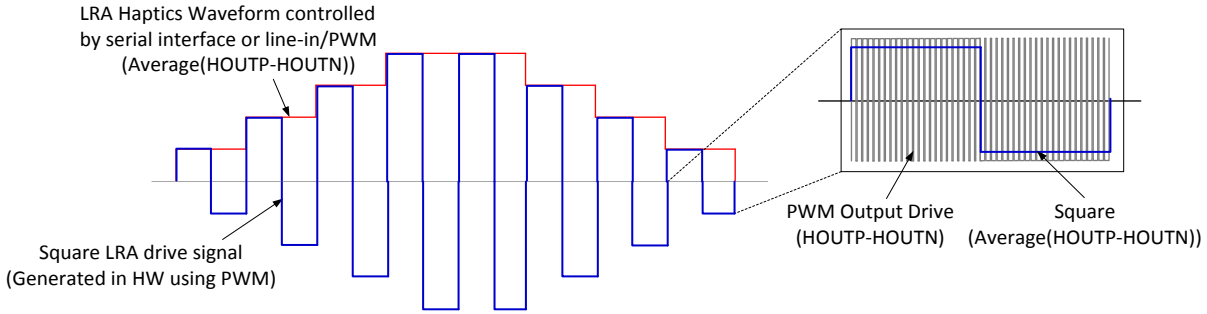
ERM signaling



LRA signaling with discrete sinusoid drive



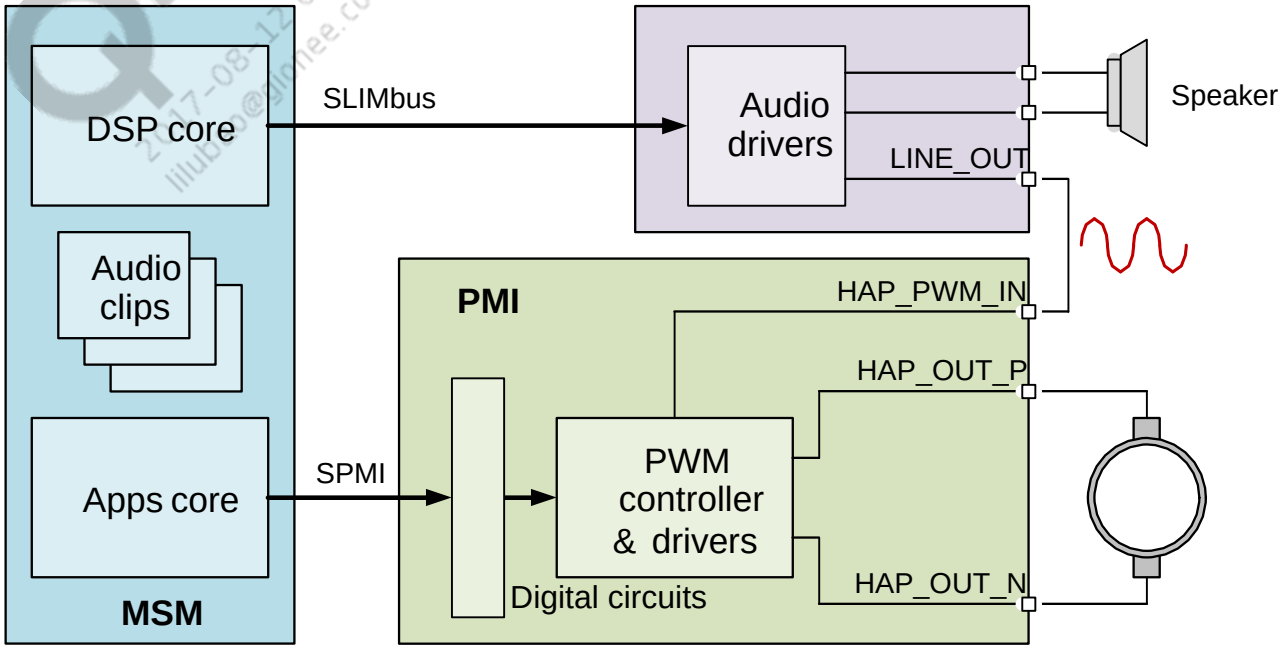
LRA signaling with square drive



Haptics Control (3 of 4)

Audio line-in mode

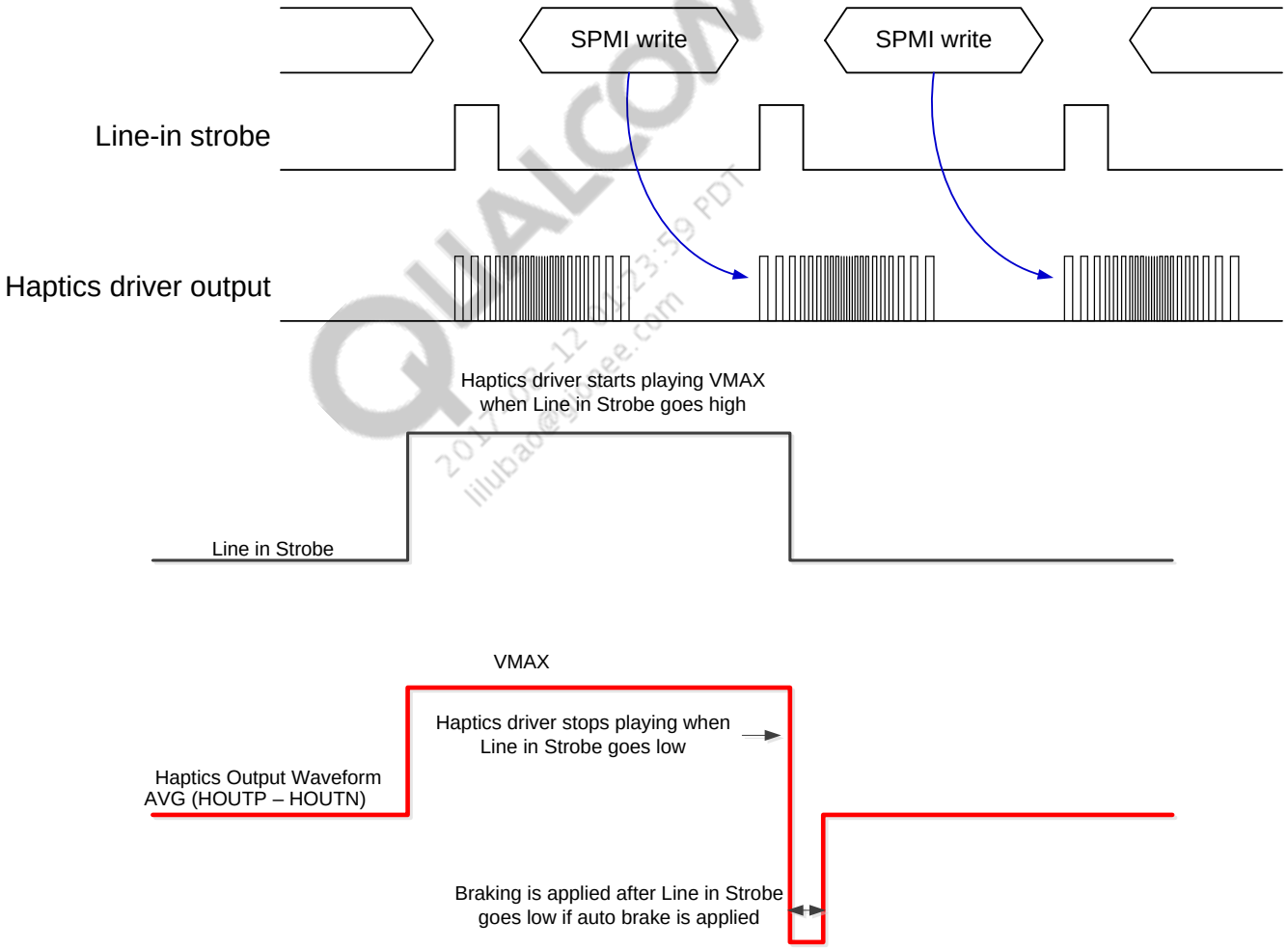
- Stored haptics waveforms (low frequency content audio clips) are played through the audio codec.
- For synchronization, the low-pass filtered version of the audio file being played on the speaker is also played on haptics.
- Haptics configured through SPMI, but the waveform comes from the codec.
- Applications
  - Synchronized haptics and audio for typing and enhanced gaming experience
  - Using ring tone as vibration pattern in silent mode
  - Playing bass sounds on haptics for enhanced music experience



Haptics Control (4 of 4)

Line-in strobe mode

- The PMIs PWM input can also be configured to strobe either the SPMI waveform buffer or VMAX setting.
- This allows software to write waveform from SPMI but controls the play timing from external source.

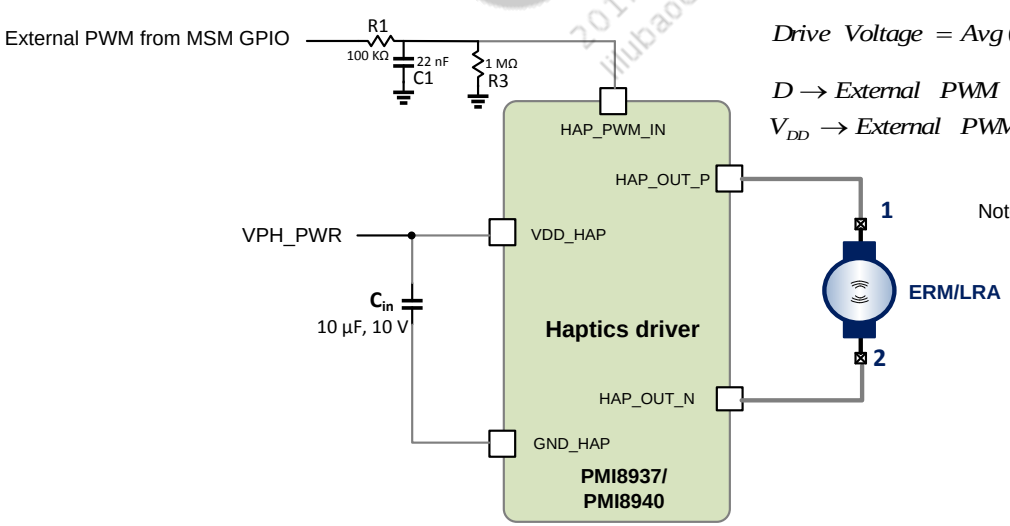


HAP_PWM_IN Used as External PWM with RC Low Pass Filter

- When HAP_PWM_IN is used as external PWM with RC low pass filter, it can support any arbitrary frequency.
- By using RC filter, duty cycle information of PWM is converted into DC voltage which allows haptics driven to be used in analog line-in waveform source mode with external PWM.
- Full scale voltage in analog line-in mode is 0-625 mV, duty cycle range should be selected based on VDD level of external PWM and values of R1 and R3 (which form the voltage divider at filter output). If using full duty cycle range of 0 to 100%, then R3 can be adjusted to scale the output voltage down to 625 mV for 100% duty cycle.
- R1 and C1 values are chosen according to the following condition.

$$\frac{External\ PWM\ frequency}{100} > \text{RC LPF cut off frequency} > 10 \times Haptics\ pattern\ frequency$$

- R3 is not needed if MSM GPIO has internal pull down.



$$Drive\ \ Voltage\ = Avg\,(HOUTP\ \ - HOUTN\ \ ) = D \cdot V_{DD} \cdot \left(\frac{V_{\max}}{0.625}\right)\left(\frac{R_3}{R_1 + R_3}\right)$$

$D \rightarrow External\ \ PWM\ \ duty\ \ cycle$

$V_{DD} \rightarrow External\ \ PWM\ \ high\ level\ \ voltage$

Note: Vmax is configured from haptics driver register VMAX_CFG

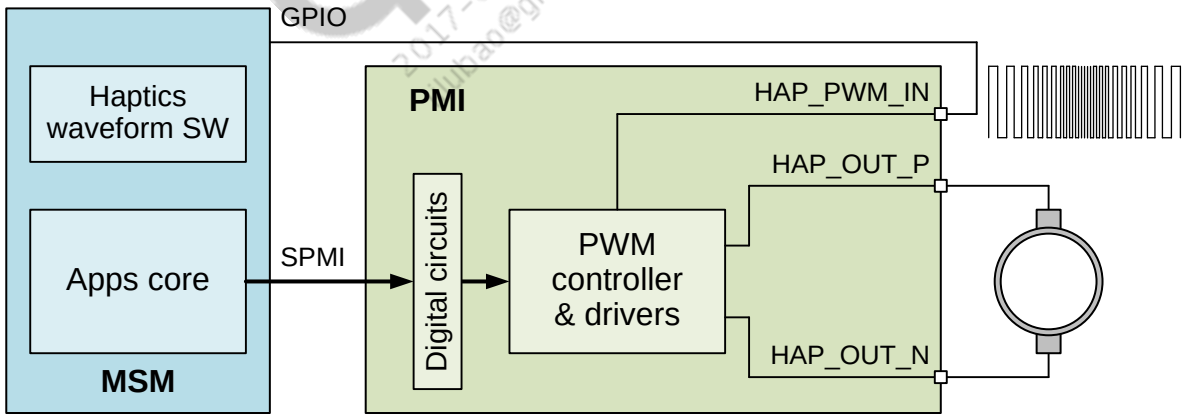
Haptics Control Modes (2 of 2)

External PWM mode

- The haptics pattern information in contained within a GPIOs duty cycle and applied to the PWM input
- The haptics driver allows four discrete PWM frequencies: 25, 50, 75, and 100 kHz (software-configurable)
- The external PWM signal is generated by the MSM or any third-party source
- Actuator is driven in either forward or reverse direction by controlling the duty cycle above or below 50%
- The relationship between output drive voltage and PWM duty cycle is expressed as:

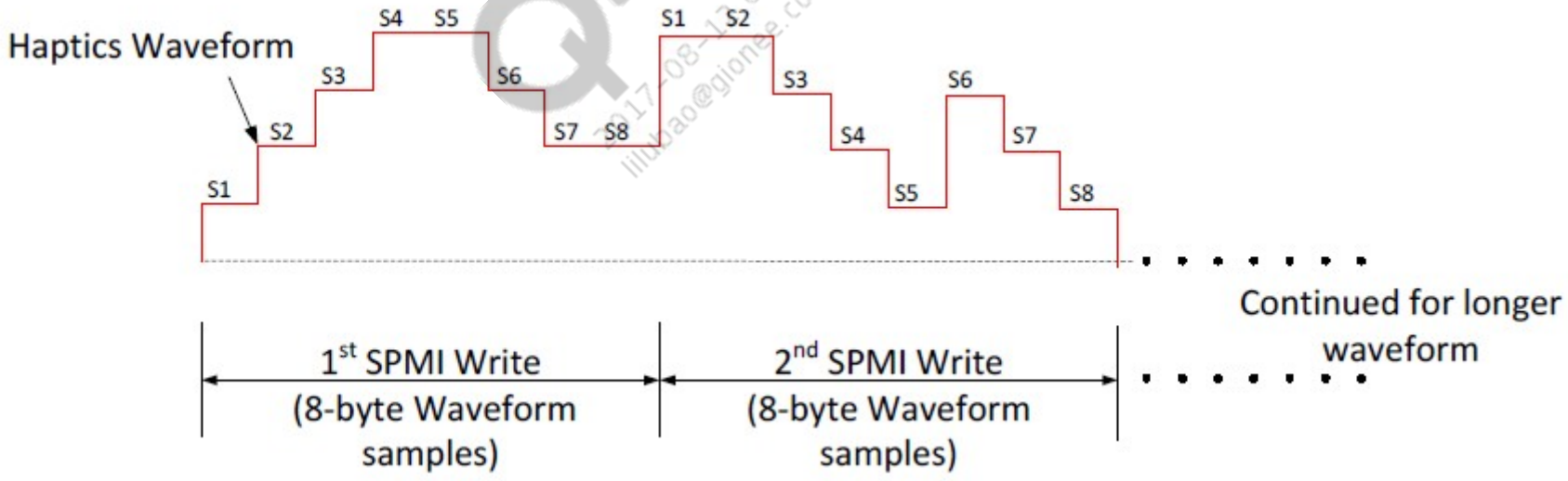
  HAP_OUT_P – HAP_OUT_N = (2·D – 1) x V_MAX where V_MAX is typically 3.6 V

  The output drive voltage is automatically clamped to V_MAX when less than 3.6 V



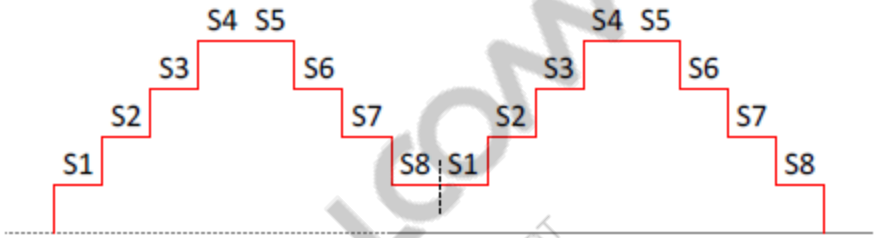
Writing Haptics Waveform Through SPMI (1 of 2)

- Waveform samples (8-bytes, S1 to S8) are sent over SPMI and stored in the haptics waveform buffer
- Each byte is played at the specified rate
- For LRA, the samples are played at the LRA resonance period and each waveform sample contains the amplitude of resonance signal
- The fastest rate for reading each sample byte is 3.33 ms, yielding a total time of about 27 ms to play the 8-byte waveform buffer
- To play a unique waveform with every 8-byte packet, software needs to continuously write the pattern



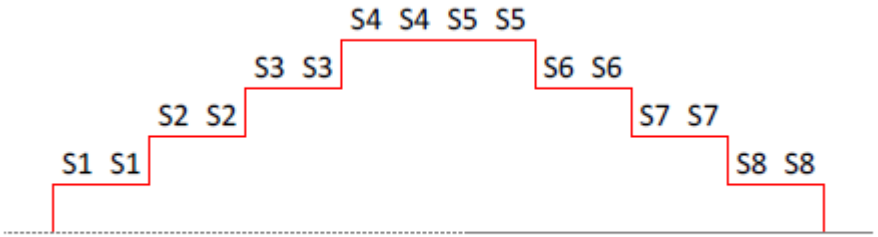
Writing Haptics Waveform Through SPMI (2 of 2)

- To play one waveform multiple times with only one SPMI write, the hardware loops back to the buffer without requiring multiple writes



SPMI write with 2x waveform repetition

- Each waveform sample can also be repeated if the waveform needs to be elongated

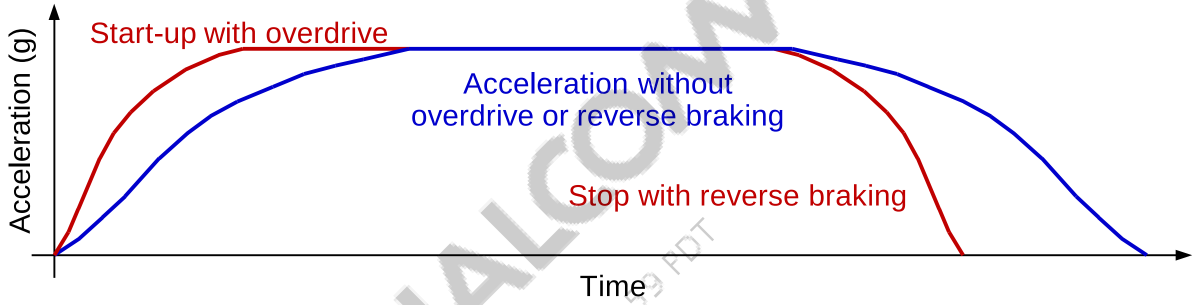


SPMI write with 2x sample repetition

Overdrive and Active Reverse Braking

LRA/ERM devices have sluggish startup and stop characteristics

The PMI improves starts and stops by applying overdrive and active reverse braking



Overdrive

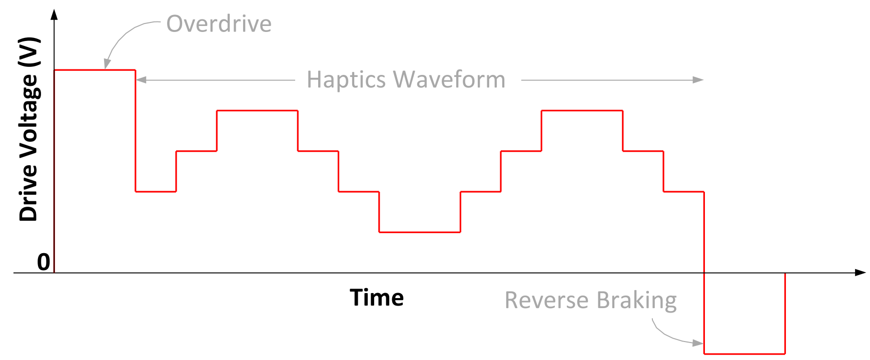
Achieved by applying up to twice the voltage across the actuators for a short duration (5 to 10ms)

If required overdrive voltage is more than haptics driver supply, actuator is simply driven at 100% duty

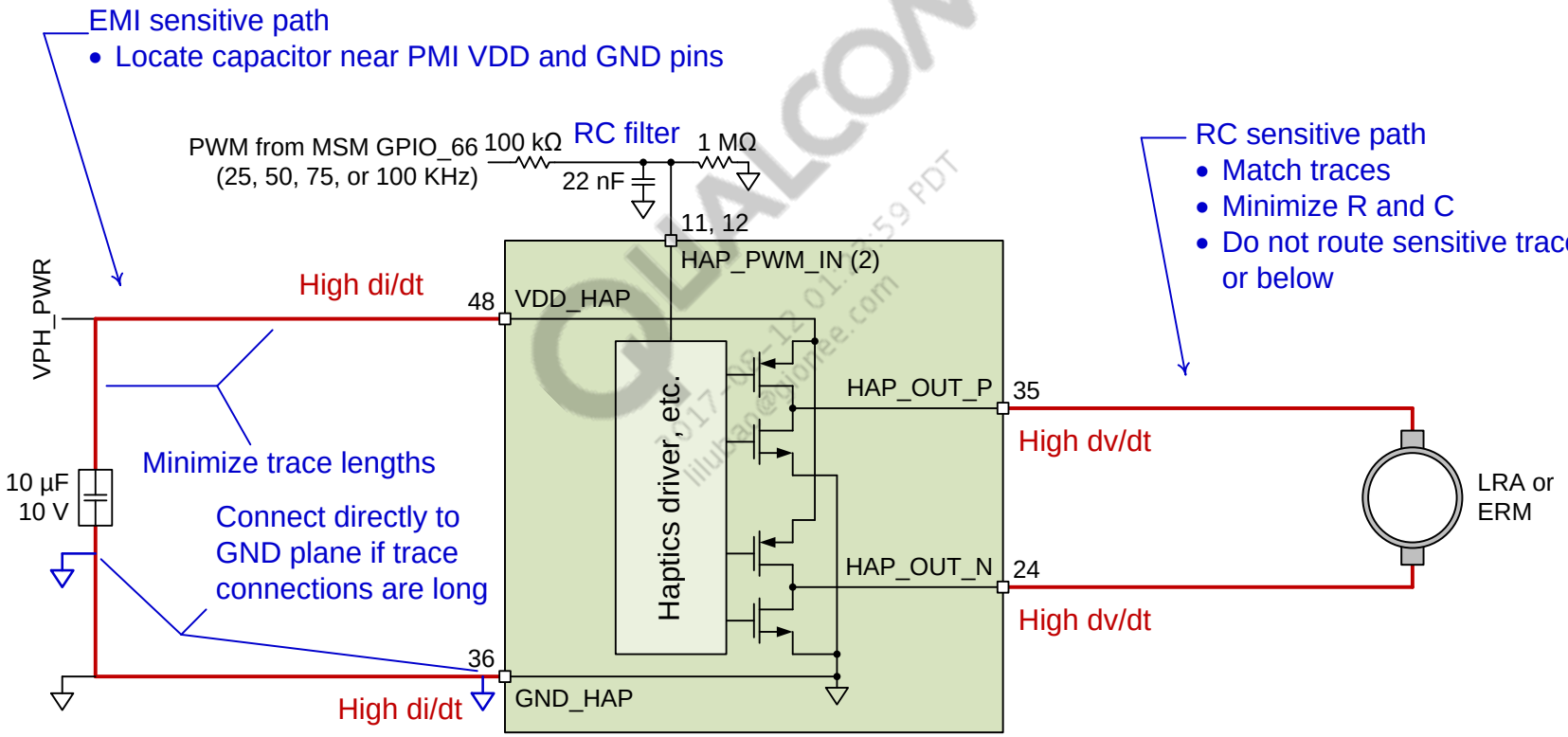
- Example 1: actuator nominal drive voltage = 2 V and haptics supply is 3.6 V → duty cycle of PWM output signal during normal drive is ~55% (2/3.6) and during overdrive it is 100%
- Example 2: input supply is 5 V → normal drive duty cycle is ~40% (2/5) and during overdrive it is ~80% (4/5)

Reverse braking

Achieved by driving the actuator in reverse direction at the end of haptics waveform



Haptics Schematic



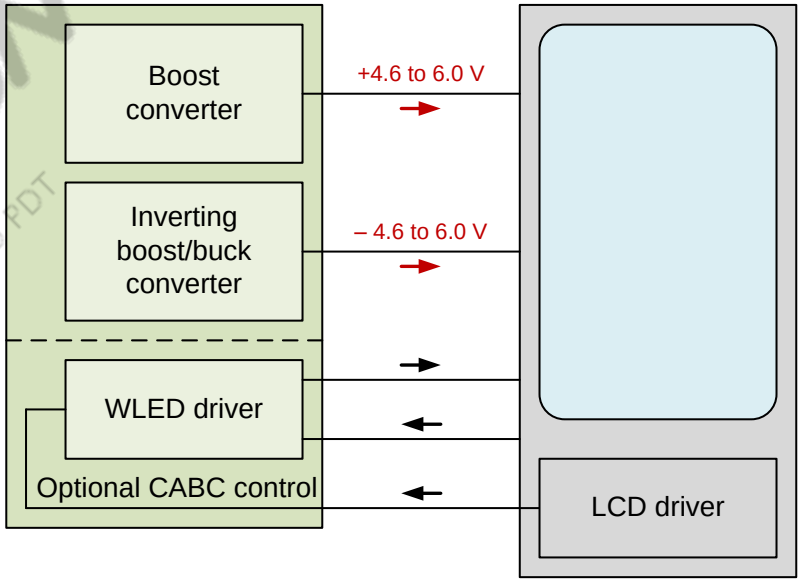
Section 7

Display ± Bias

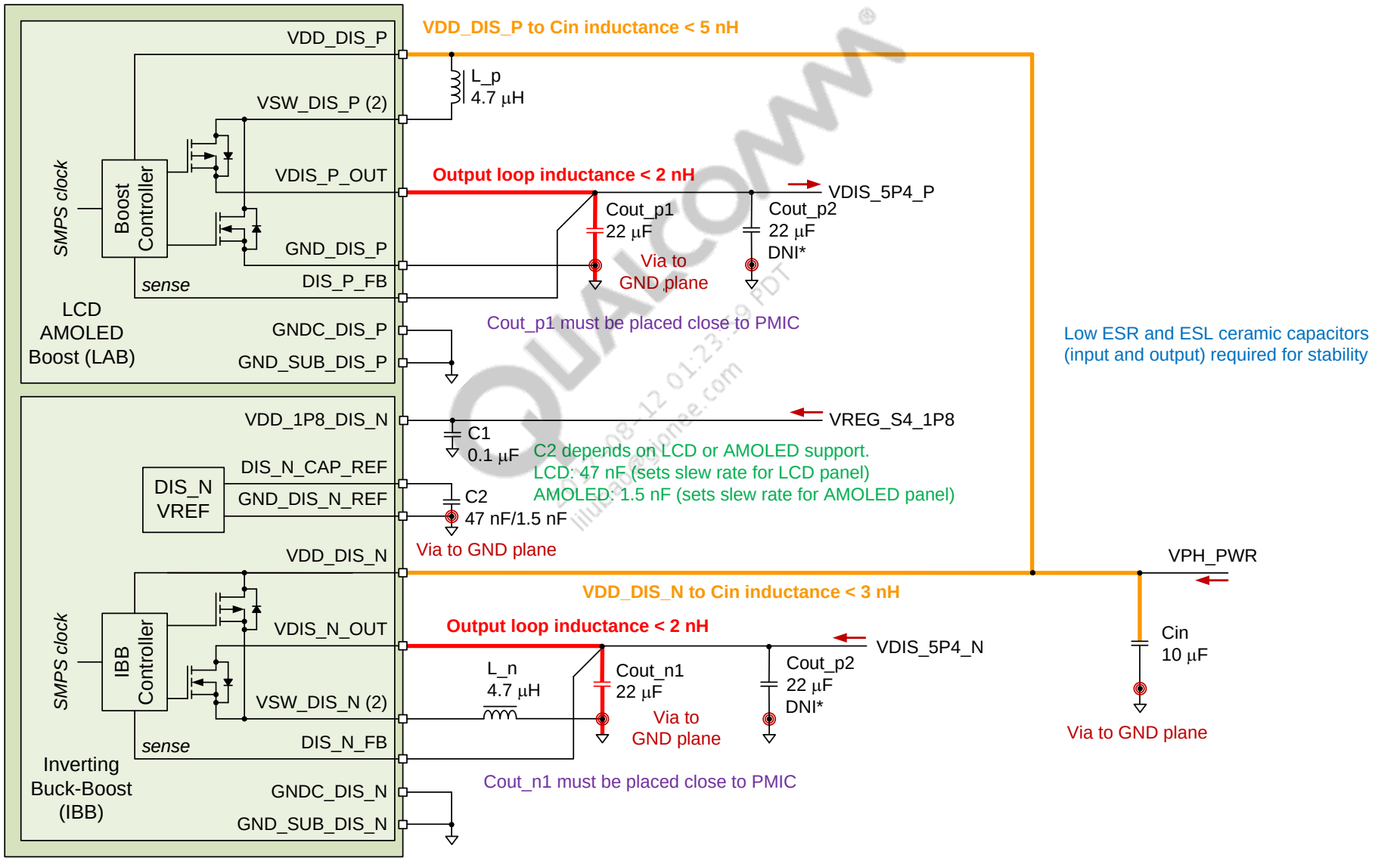
Display ± Bias

Features

- Dual synchronous DC/DC converter topology
- Supports LCD (user-settable hardware/software configuration)
- 86% efficiency converters for both rails with a compact BOM
- 2.5–4.75 V input voltage range
- Independently-programmable positive and negative output voltages
- Programmable output voltage range of ±4.6 to ±6.0 V (±5.5 V default)
- 100 mV resolution on both bias rails
- Up to 150 mA (LCD) output current for both rails
- Auto output disconnect and active discharge on module shutdown
- Short circuit protection with optional external switch
- Auto power sequencing on module enable/disable
- DCM anti-ringing on both rails
- Light load mode for high efficiency



Display ± Bias Schematic

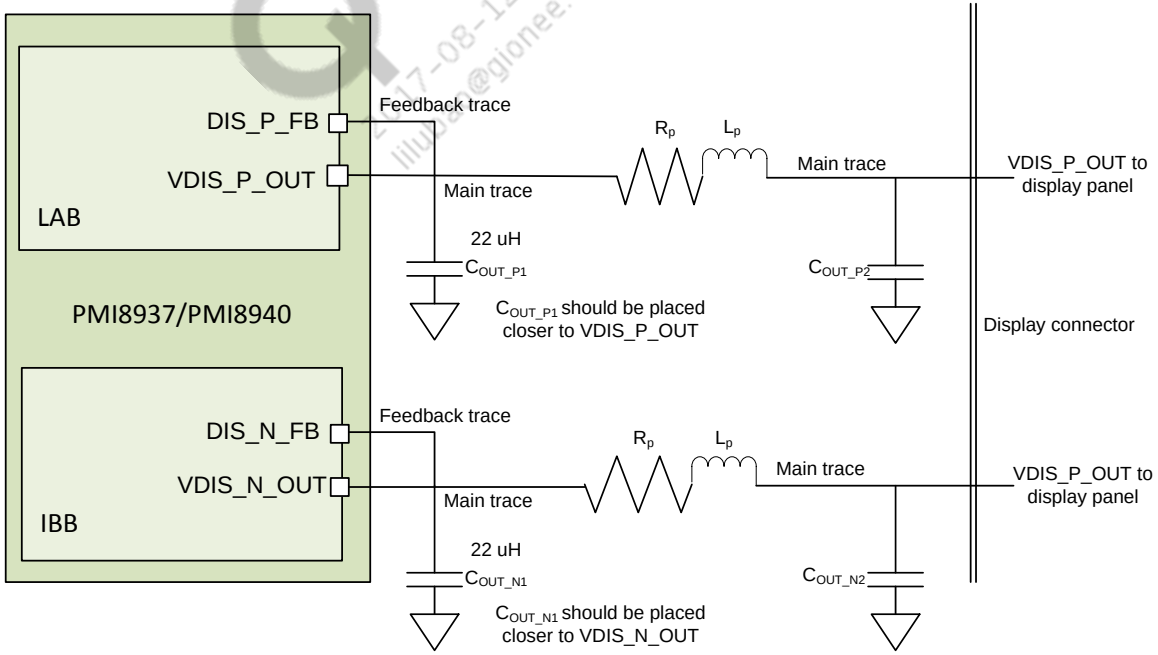


Using Remote Capacitors on VDIS_P_OUT/VDIS_N_OUT

- In addition to local output capacitor (C_{OUT_P1} , C_{OUT_N1}), remote capacitors (C_{OUT_P2} , C_{OUT_N2}) may be required on VDIS_P_OUT/VDIS_N_OUT output connecting to display connector if traces are long and voltage accuracy requirement is tight.
- Since long traces have parasitic resistance (R_P) and inductance (L_P), when terminated with capacitor, it may exhibit resonance which may fall around switching frequency and amplify the output ripple.
- In order to avoid resonance, the remote cap value should be chosen according to the following formula.

$$C_{OUT\_P2/N2} \geq 2 \times \frac{L_P}{R_P^2}$$

- Feedback (DIS_P_FB , DIS_N_FB) should be connected to local capacitor (C_{OUT_P1} , C_{OUT_N1}) as remote feedback (connected to C_{OUT_P2} , C_{OUT_N2}) may cause instability due to additional phase shift.



Section 7.1

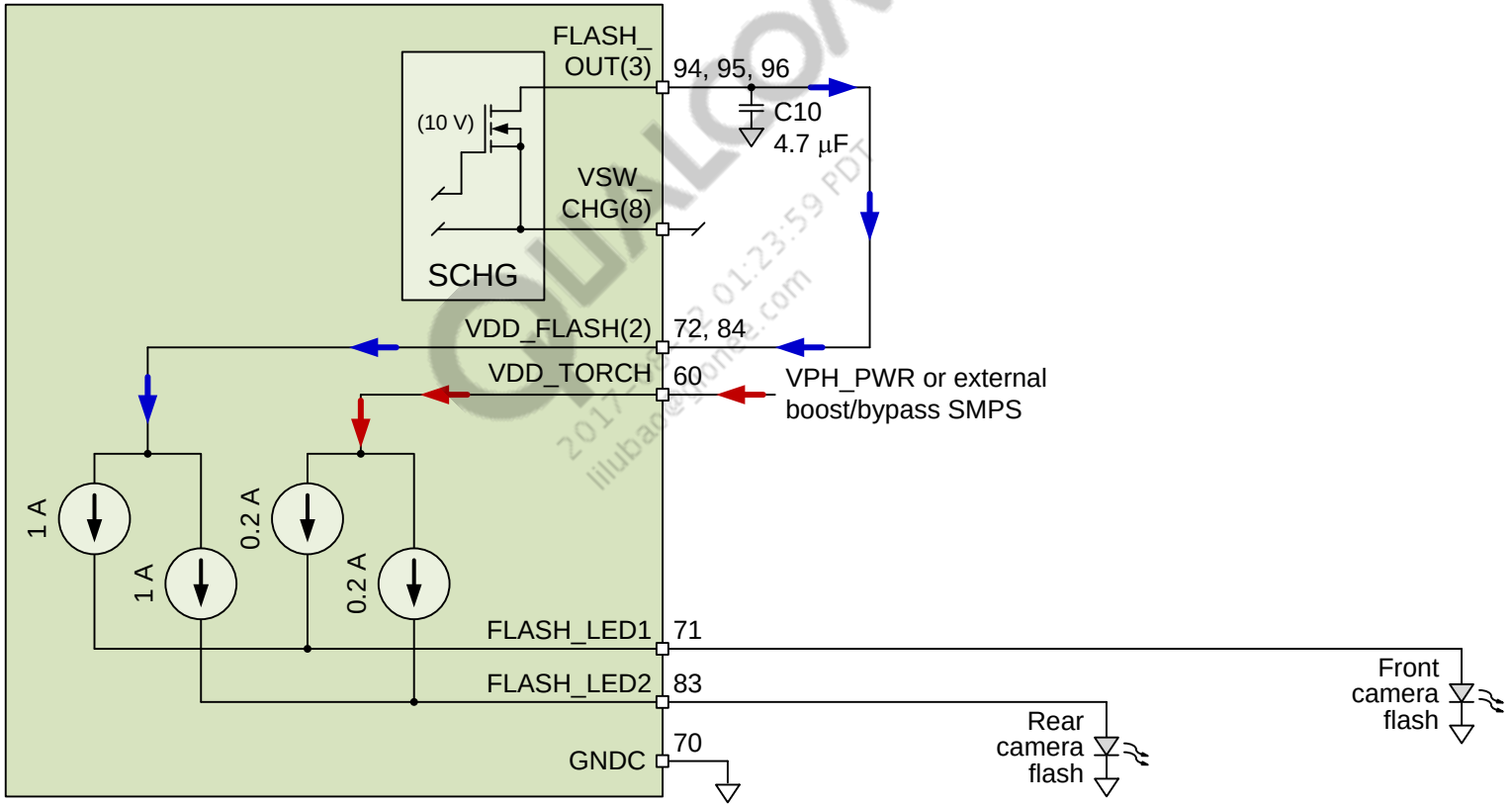
Flash/Torch Drivers

Flash/Torch Drivers

- Camera flash with optional torch mode
- Supply-referenced current drivers
- Flash at 2 A; torch at 400 mA (totals)

Torch mode supply is VPH_PWR (video lighting)

Flash mode supply is SCHG in reverse boost mode (camera lighting)



2 × 1 A Flash Driver Feature Summary

- Two LED channels
- 2 × 1 A high-side current driver for flash
  - Flash driver uses an internal switched mode battery charger as a boost regulator
  - Boost adaptively regulates supply rail (FLASH_OUT) to a minimum headroom of 500 mV across the two current sources
- 2 × 200 mA high-side current driver for video
  - Torch driver uses VPH_PWR or external boost/bypass; torch mode requires 3.6 V at VDD_TORCH in order to provide enough headroom for LEDs
- Supports hardware-controlled (MPP_4) or software-controlled flash triggering
- Low battery voltage monitoring
  - Monitors VPH_PWR at the PMIC pin and ramps down and clips LED current if the Vdip threshold is crossed
- Safety features
  - Flash timeout, video watchdog timer, open LED/short LED fault detection, thermal derating during flash

Section 7.2

LCD Backlight (White LED)

White LED (WLED) Support

The integrated boost SMPS generates the high voltage needed for white LEDs.

High-voltage requirement: with eight LEDs in series, VREG_WLED needs to be about +24.5 V (assume 3 V per LED and 0.5 V sink headroom).

Two low-side current sinks

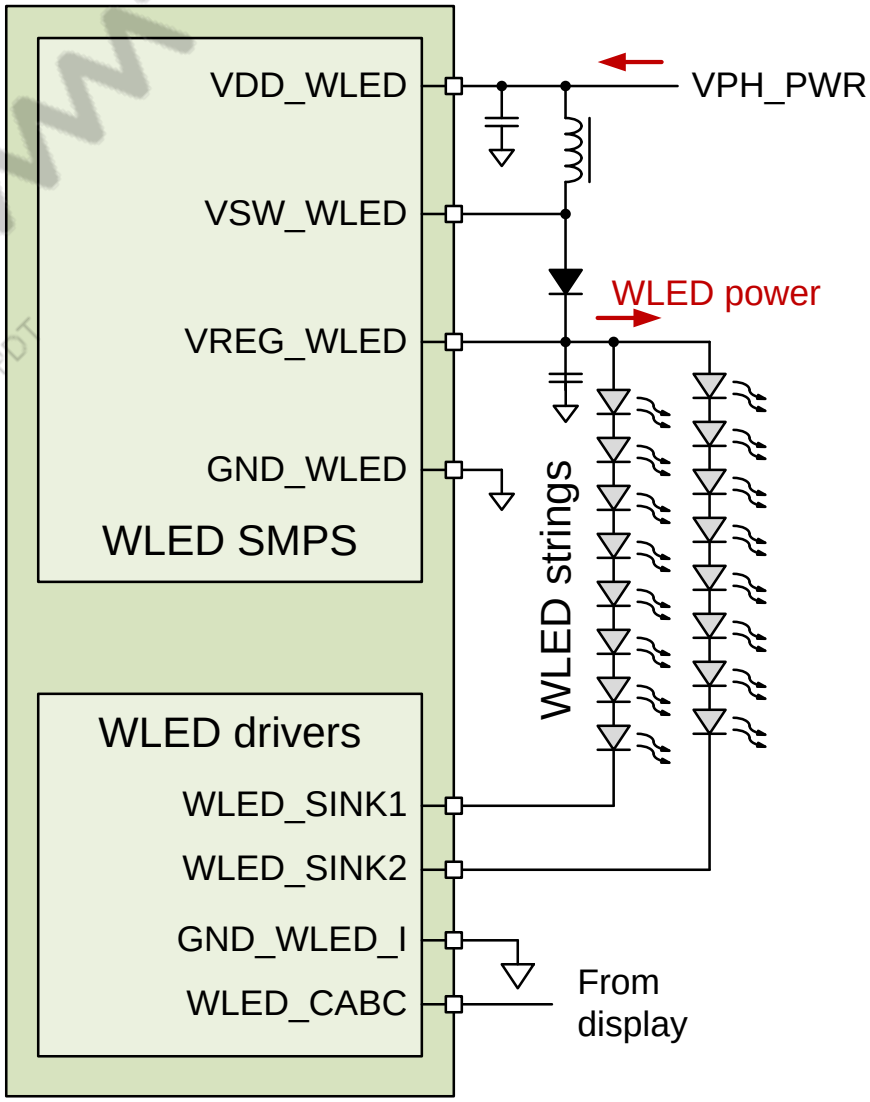
- Each supports a string of up to eight LEDs
- Up to 30 mA each
- Dedicated ground pin

White LED content adaptive backlight control (CABC) is supported.

- Connect the WLED_CABC pin to ground through a 100 kΩ resistor if not used.
- Supports 12-bit analog and 9-bit digital dimming resolution

Switching frequency for the WLED boost is configurable: 600 kHz, 800 kHz, or 1.6 MHz.

The recommended switching frequency for the WLED boost is 800 kHz.



WLED Drivers

- Two current sinks capable of up to 30 mA each, independently programmable in 2.5 mA steps
- Each current sink can be independently controlled via a combination of:
  - Brightness control register (for example, 50%)
  - Full-scale current setting register (for example, 25 mA)
  - External CABC PWM input (for example, 80% duty)
- Using the example values, the resulting LED current is (25 mA) × (50%) × (80%) = 10 mA
- Dimming control – a new hybrid mode allows analog dimming at higher LED currents and digital dimming at lower LED currents
  - Takes advantage of better digitally controlled current accuracy under low brightness conditions
  - Mitigates EMI concerns by switching to analog dimming at higher brightness conditions
  - Switchover threshold is programmable, but typically set to 6.25% of full scale current (about 1.9 mA for the given 30 mA full-scale current)

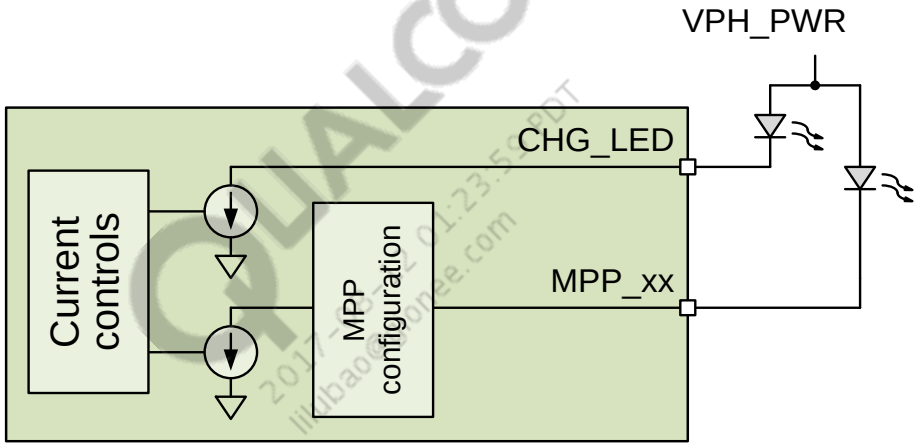
Section 7.3

Other Current Sinks

Other Current Sinks

Current driver for charging indication

- CHG_LED allows different patterns (solid, blinking pattern 1, and blinking pattern 2) and off to indicate charging
- 5 mA–20 mA sink (not software configurable) depending on operating conditions such as VPH_PWR level
- Total series resistance from CHG_LED through driver to ground is 170 Ω ± 30%



Configurable MPPs are available as current sinks

- MPP drivers are ground-referenced current sinks; available on even-numbered MPPs only
- Low output voltage compliance
- Design must provide current path from high voltage
- Use ballast resistors when driving multiple LEDs if necessary
- Applied voltage is limited to VDD (VPH_PWR)
- 5 mA–40 mA in 5 mA steps or tri-state (off)

Section 8

PM8937/PM8940 Audio Codec

PM8937/PM8940 Audio Codec

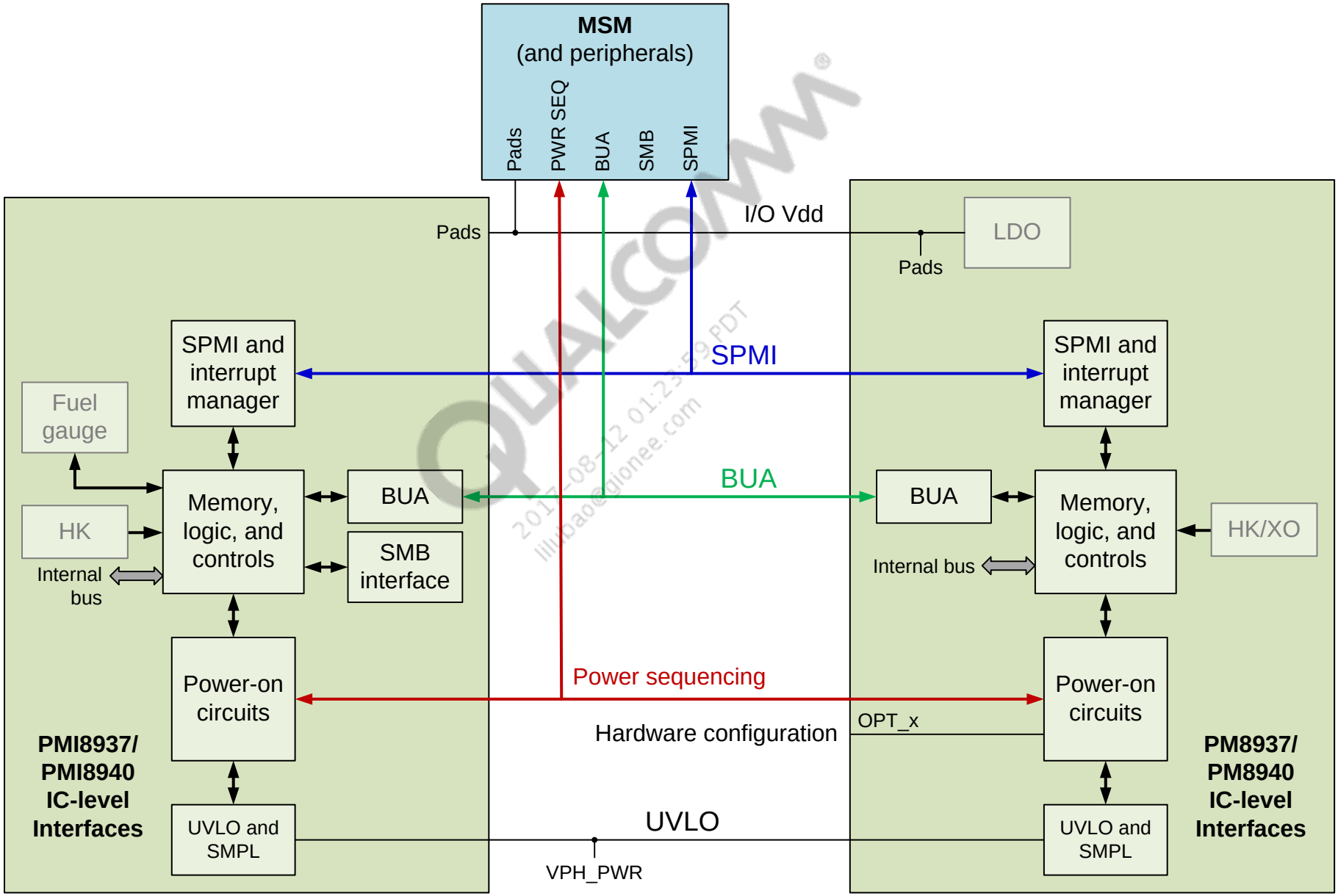
MSM8937 chipset split audio functions between the modem IC for digital processing and either the PM8937/PM8940 device or the dedicated WCD9326 audio codec for analog processing. Each solution has a dedicated design guidelines document:

- *MSM8937/PM8937 Chipset Audio Hardware Design Guidelines/Training Slides* (80-P2564-5C)
- *MSM8937 Chipset Audio Hardware Design Guidelines/Training Slides* (80-P2468-5C)
- *WCD9326 Audio Codec Design Guidelines* (80-NT793-5)

Section 9

IC-level Interfaces

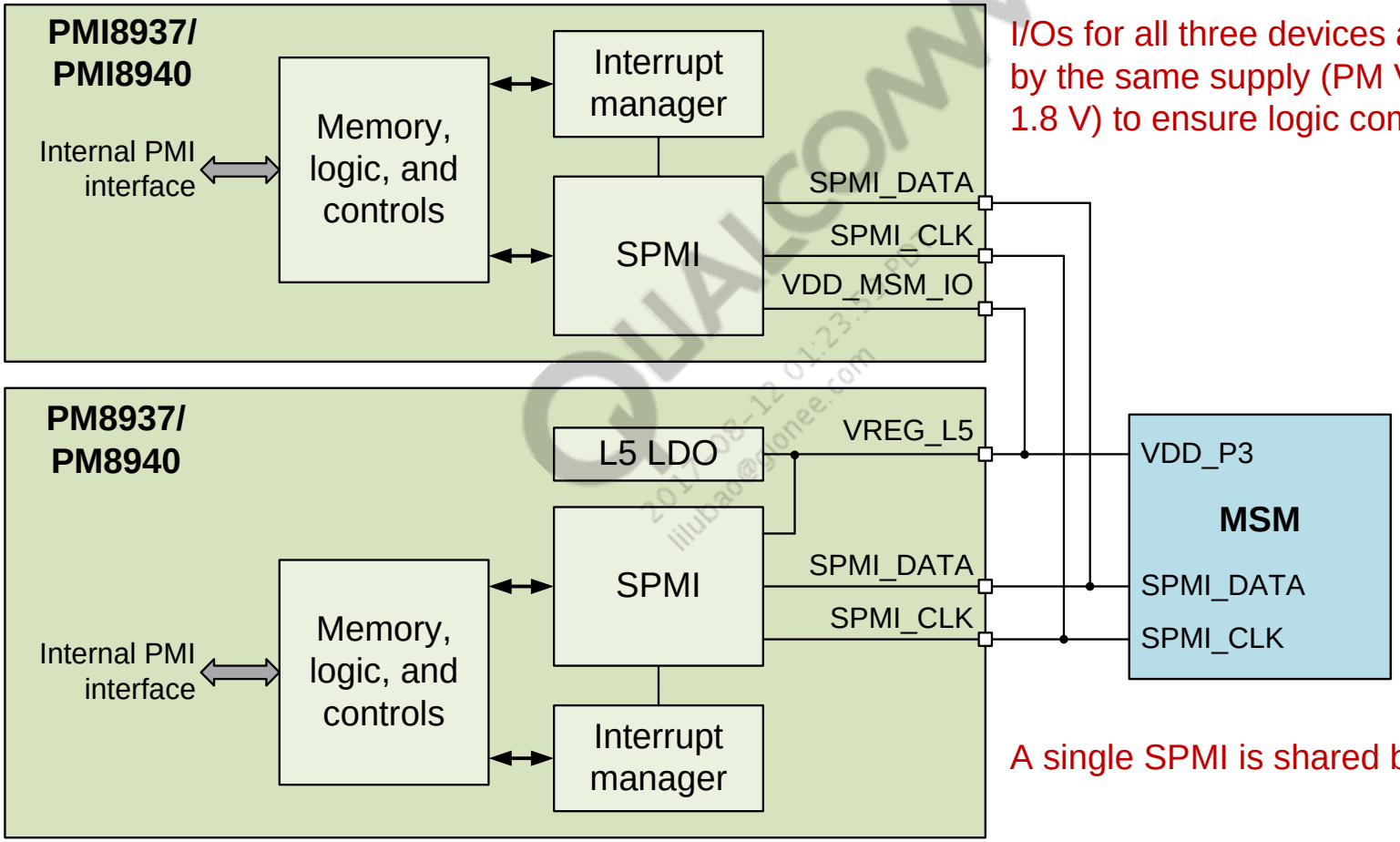
IC-level Interfaces Introduction



Section 9.1

Chipset Interfaces and PMIC Coordination

SPMI and Interrupt Manager (1 of 2)



I/Os for all three devices are powered by the same supply (PM VREG_L5, 1.8 V) to ensure logic compatibility.

A single SPMI is shared by both PMICs

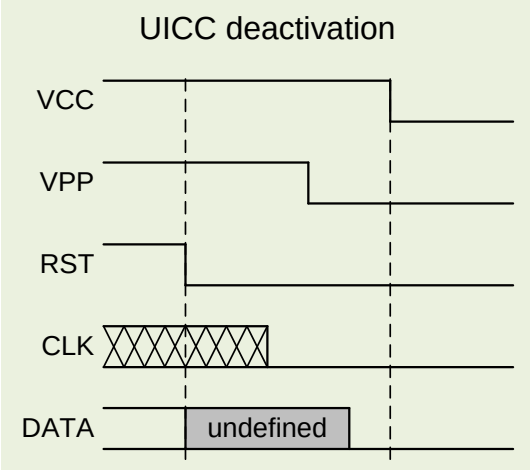
SPMI and Interrupt Manager (2 of 2)

- The serial power management interface (SPMI) is the primary IC-level interface for efficient initialization, status, and control communications.
- Application programming interface (API) is used to program the PMIC, indirectly exercising the SPMI.
- The PM8937/PM8940 coin cell backs up several of its SPMI registers; at power-up, SPMI defaults are restored, except bits backed up by the coin cell – they are only restored to default values if the coin cell expired.
- The interrupt manager receives internal reports on numerous functions and conveys status signals to the modem device, thereby supporting its interrupt processing.
- Each interrupt event has the following associated SPMI bits:
  - Interrupt mask (read/write) – allows the modem IC to ignore event; latched status hidden and interrupt is not asserted
  - Interrupt real-time status (read only) – follows real-time interrupt status (active or inactive) for standard configuration interrupts; special configuration interrupts are defined further below
  - Interrupt latched status (read only) – set when event is active and interrupt mask bit is cleared; stays set until clear bit is set
  - Interrupt clear (read/write) – clears latched status automatically after latched status is read
- Unmasked interrupts notify the modem device that at least one interrupt has occurred.

BUA Interface

To support UIM card removal detection/battery removal detection, a new, low-latency, bidirectional interface was created called the battery UICC alarm (BUA) interface.

- ISO-7816-3 requires that a smart card (UICC/UIM) be powered down in a controlled and predefined manner.
- BUA is a bidirectional interface between the PMICs and the MSM device that allows a controlled power down of the UICC when either the battery or the UICC is removed.
- System interconnect (see next slide)
  - UICC DATA/CLK/RST pins are connected directly between the SIM and the MSM device.
  - UICC power is supplied by the PM8937/PM8940 device.
  - BUA circuits are within the PMI8937/PMI8940 and PM8937/PM8940 devices.
- The PMI8937/PMI8940 device alerts the MSM device over the bidirectional interface when a battery is removed so that the UICC can be deactivated while the system is still powered by capacitors.
- The MSM device alerts the PMICs over the bidirectional interface when a UICC removal is initiated so that the UICC can be deactivated before it is completely removed.
- The alarm and deactivation are based in hardware; no software intervention is required.



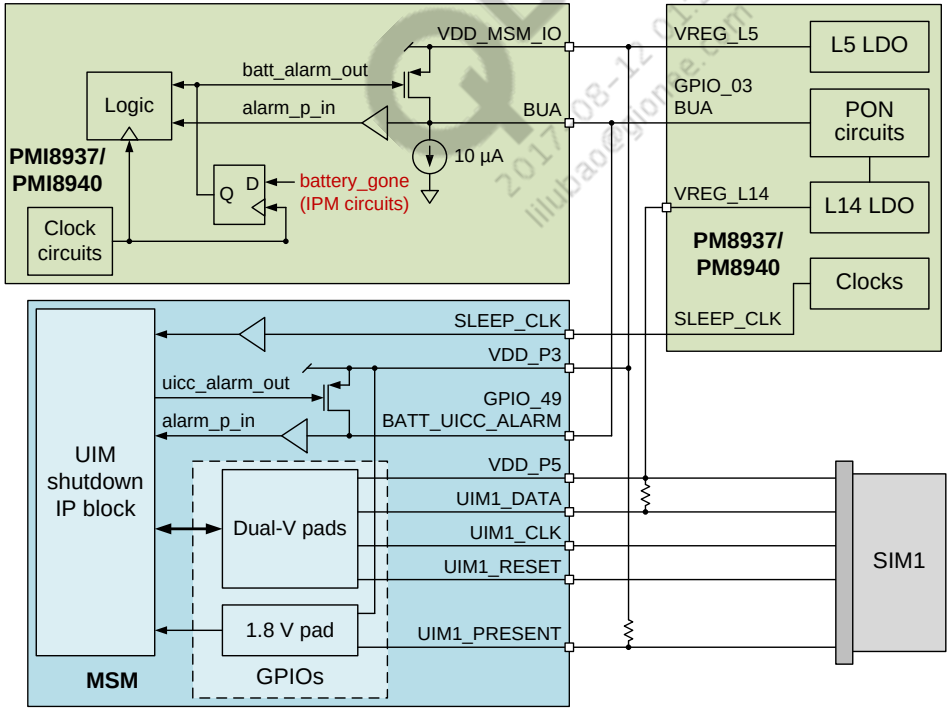
BUA Operation

Battery removal

- The PMI8937/PMI8940 device detects battery removal and triggers the alarm to the PM8937/PM8940 device and the MSM device (pulls BUA high).
- The PM8937/PM8940 device waits the known duration while the MSM device shuts down DATA/CLK/RST and then turns off the UICC LDOs.
- Deactivation is complete in ~ 1.2 µs (nominal).

UICCx removal

- The MSM device detects UICCx removal via the SIM's mechanical switch and UIM1_PRESENT.
- The MSM device shuts down DATA/CLK/RST, and then triggers the alarm using its own BUA signal (GPIO_101).
- The PM8937/PM8940 device decodes the alarm and powers down the UICCx LDO.
- Deactivation is complete in ~ 1565 µs (nominal).



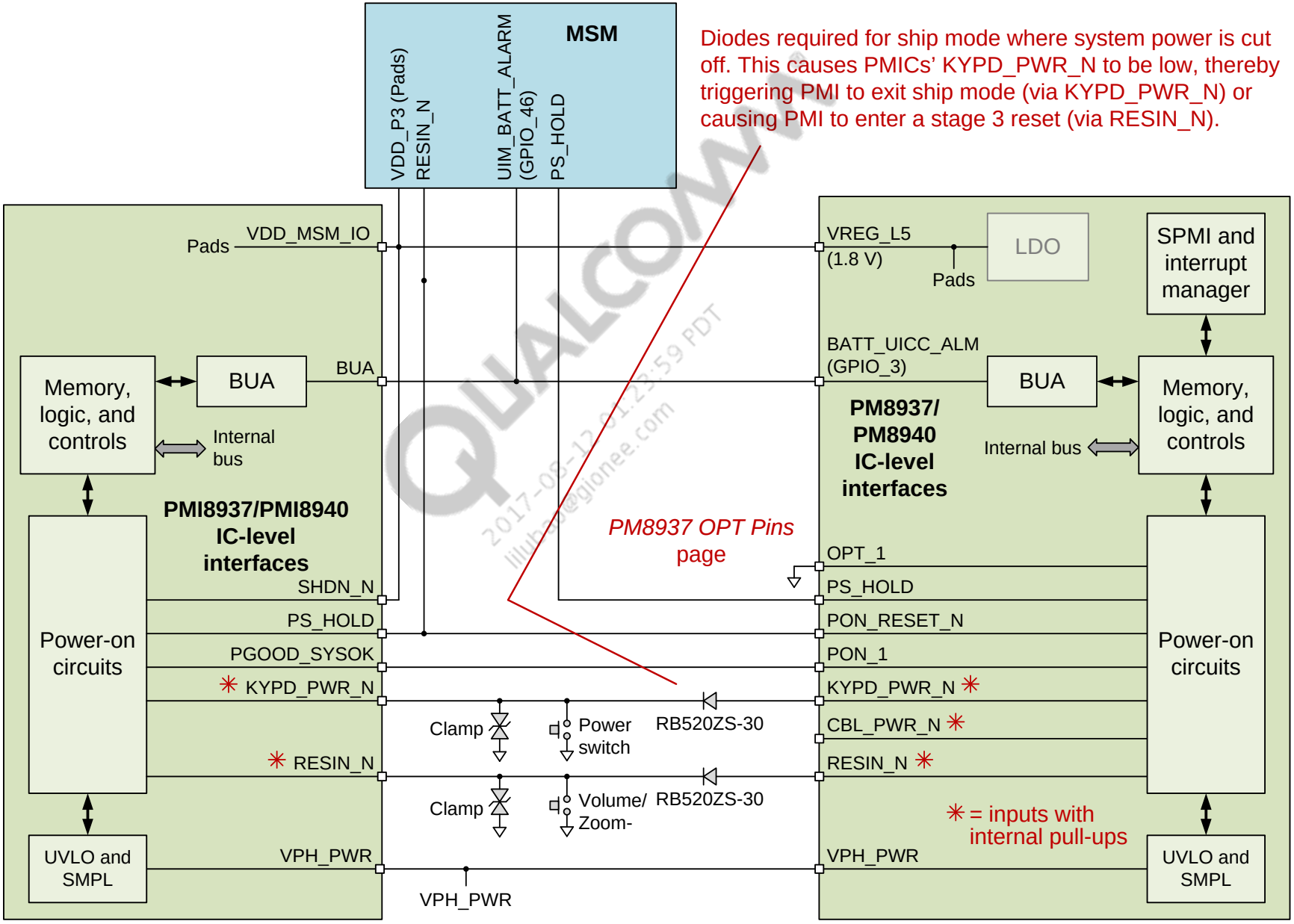
Section 9.2

Power Sequencing and PBS

Section 9.2.1

Power on and PBS

Power-on Circuits



Power-on Circuits

- Dedicated PM8937/PM8940 device circuits continuously monitor events that might trigger a power-on sequence.
- If an event occurs, these circuits power on the IC, determine the handset's available power sources, enable the correct source, enable the PMI8937/PMI8940 device, and take the modem IC out of reset.
- To power up immediately on battery insertion, tie CBL_PWR_N to ground.
  - In this case, the PMIC is always on and the modem IC should clear the xxxPWR_PU bit to turn off the internal pull-up resistor, thereby reducing the PMIC quiescent current.
- OPT = hardwired connections
  - Ground, open, or VDD
  - Sets some PMIC features
  - See the PM8937/PM8940 OPT Pins slide for more information
- Key power-on signals are listed and described next; power triggering events (on and off) are then listed and described.
- Power-on circuit functions, which have not been discussed elsewhere:
  - They generate internal PMIC power supplies (aVdd and dVdd) and the ultimate digital system power-on resets.
  - They generate PMIC device operation reset signals.
  - They enable the band gap reference and connection of the input power source to system power bus.
  - They initiate PBS functions.

Turn On and Off Trigger Events (1 of 2)

Turn-on events

- The PM8937/PM8940 device is responsible for detection of all system turn on events including:
  - KYPD_PWR_N (after debounce, 0–2 s)
  - RESIN_N (after debounce, 0–2 s)
  - CBL_PWR_N (after debounce, 15.625 ms–2 s)
    - Battery insertion can trigger a power-on event by shorting CBL_PWR_N to ground
  - RTC alarm
  - PON_1 (general-purpose ON, positive trigger used for the charger attach turn-on trigger)
  - System restart after triggering events (like WDOG, PS_HOLD, and RESIN_N if configured to do so)

PMIC reset and power-off events

- Software-initiated shutdown – software writes the value 0x80 to PM8937/PM8940 device register address 0x085B
- Software-managed shutdown – processor-initiated shutdown is triggered by deassertion of PS_HOLD
- KYPD_PWR_N – grounding of the KYPD_PWR_N input (after debounce)
- RESIN_N – grounding of the RESIN_N input
- Combination of KPD_PWR_N and RESIN_N – simultaneous grounding of both KPD_PWR_N and RESIN_N
- Overtemperature stage 3 – PMIC temperature exceeds the OTS3 value
- WDOG expiration – PMIC_WDOG or TFT_WDOG timer expires
- Low battery voltage – VPH_PWR drops below the UVLO threshold without SMPL recovery

Turn On and Off Trigger Events (2 of 2)

KYPD_PWR_N as PON trigger

- KYPD_PWR_N need not be kept low until PS_HOLD is asserted by baseband circuit to turn on PM8937/PM8940.
- KYPD_PWR_N needs to be held low until LDO L5 of PM8937/PM8940 comes up. The time taken for L5 to come up after PON trigger is ~65 ms.
  - Hence, KYPD_PWR_N needs to be asserted for only ~65 ms for PON to proceed to completion.
- L5 is the PON trigger for PMI8937/PMI8940.
- In order to register the correct PON reason of KYPD_PWR_N in 0x00000808 PON_PON_REASON1 of PM8937/PM8940, KYPD_PWR_N must be held low until at least PS_HOLD is asserted by the MSM device.

USB insertion as PON trigger

- On inserting USB, PGOOD_SYSOK of PMI8937/PMI8940 gets asserted. This is connected to PON_1 of PM8937/PM8940.
- In this case, PON_1 acts as PON trigger for PM8937/PM8940.
- L5 continues to be the PON trigger for PMI8937/PMI8940.

PM8937/PM8940 OPT Pins

- The PM8937/PM8940 device includes one optional configuration pin OPT_1 that must be hardwired to ground or VPH_PWR or be left open (in a high-impedance state or Hi-Z). The settings of this pin define or influence the power-on sequence (customized for specific chipsets); (see the table below):
- On each chipset that uses the PM8937/PM8940 device, the OPT pin must be set correctly for their particular application; the MSM8937 device-based reference design uses these settings: OPT_1 = GND.

OPT_1	Configuration
GND	Default configuration

Key Power Sequencing Pins – PM8937/PM8940

Pin name	Description	Purpose
PON_1	Active-high power-on trigger from the PMI8937/PMI8940 device's charger	Initiates the PM8937/PM8940 device's power-on sequence
KYPD_PWR_N	Active-low poweron/off trigger from external button	Initiates the PM8937/PM8940 device's power-on sequence
PON_RESET_N	Active-low output to the MSM and PMI8937/PMI8940 devices to indicate that PON complete	Allows the MSM device to come out of reset and the PMI8937/PMI8940 device to complete its power-on sequence
VREG_L5	1.8 V output that enables during the power-on sequence	When off, allows the PMI8937/PMI8940 device's charger to enter a low-power state; at a keypad power-on event, VREG_L5 goes high, indicating to the PMI8937/PMI8940 device's charger to exit low-power mode
VPH_PWR	PM8937/PM8940 device power	Main power input from the PMI8937/PMI8940 device's charger; if voltage is below the UVLO level, power on is not possible
BUA (GPIO_3)	Active-high BUA signal input from the PMI8937/PMI8940 device	Supports BUA operation to ensure that UICC is not corrupted
CBL_PWR_N	Tying this pin to ground initiates a power on whenever a valid power source is detected (including battery insertion)	To power on when a battery is inserted

Key Power Sequencing Pins – PMI8937/PMI8940

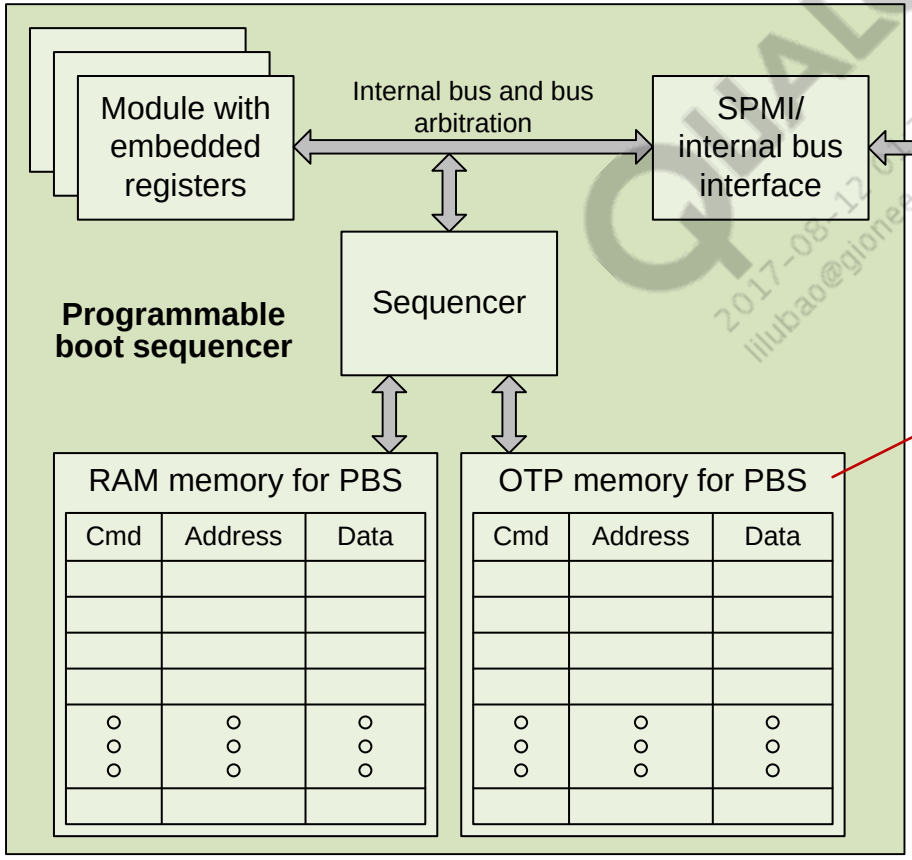
Pin name	Description	Purpose
PGOOD_SYSOK	Programmable open-drain or push-pull output	Used as the power on trigger to the PM8937/PM8940 device (PON_1) when a valid power source is inserted; also triggers a graceful PM8937/PM8940 device shutdown when battery voltage falls below Vlowbatt
SYSON	+5 V regulated output voltage	Powers high-side boot driver and goes high when a valid power source is inserted, or when the SCHG is in reverse boost mode; can be programmed to enable immediately after the source is valid (enabling external USB switch), or after APSD is complete
SHDN_N	Active high input to the PMI to initiate a power on	The **ONLY** PMI power-on trigger; connected to the PM8937/PM8940 device's VREG_L5 output that goes high during the power-on sequence; when input power is absent and SHDN_N is low, the charger enters a low-power shutdown mode
BUA	Raw open-drain comparator output indicating when the battery is missing	Connected to the PM8937/PM8940 and MSM devices; supports BUA operation to ensure that UICC is not corrupted
KYPD_PWR_N	Active-low trigger from external button to exit ship mode	Exits ship mode when pressed; does **NOT** trigger PMI8937/PMI8940 device power on
PS_HOLD	Dedicated pin used as a power-off trigger or warm reset trigger; configurable by software	Reset trigger to power-on circuits; needs to be asserted high to complete the PMI8937/PMI8940 device's power-on sequence; low forces the PMI8937/PMI8940 device to either shutdown or initiate warm reset per software

Section 9.2.2

Resets

Programmable Boot Sequence (PBS)

- The PM8937/PM8940 devices support custom PBSs configured with OTP and RAM
- Implemented as a series of address and data transactions that mimic normal software control
- Programmable control of any PMIC resource in any order with any available programmable configuration
- Support for API-like routines are implemented with OTP-defined sequences; routines are initiated via SPMI writes to address pointer or via hardware trigger
- Support for a limited command set of executable functions



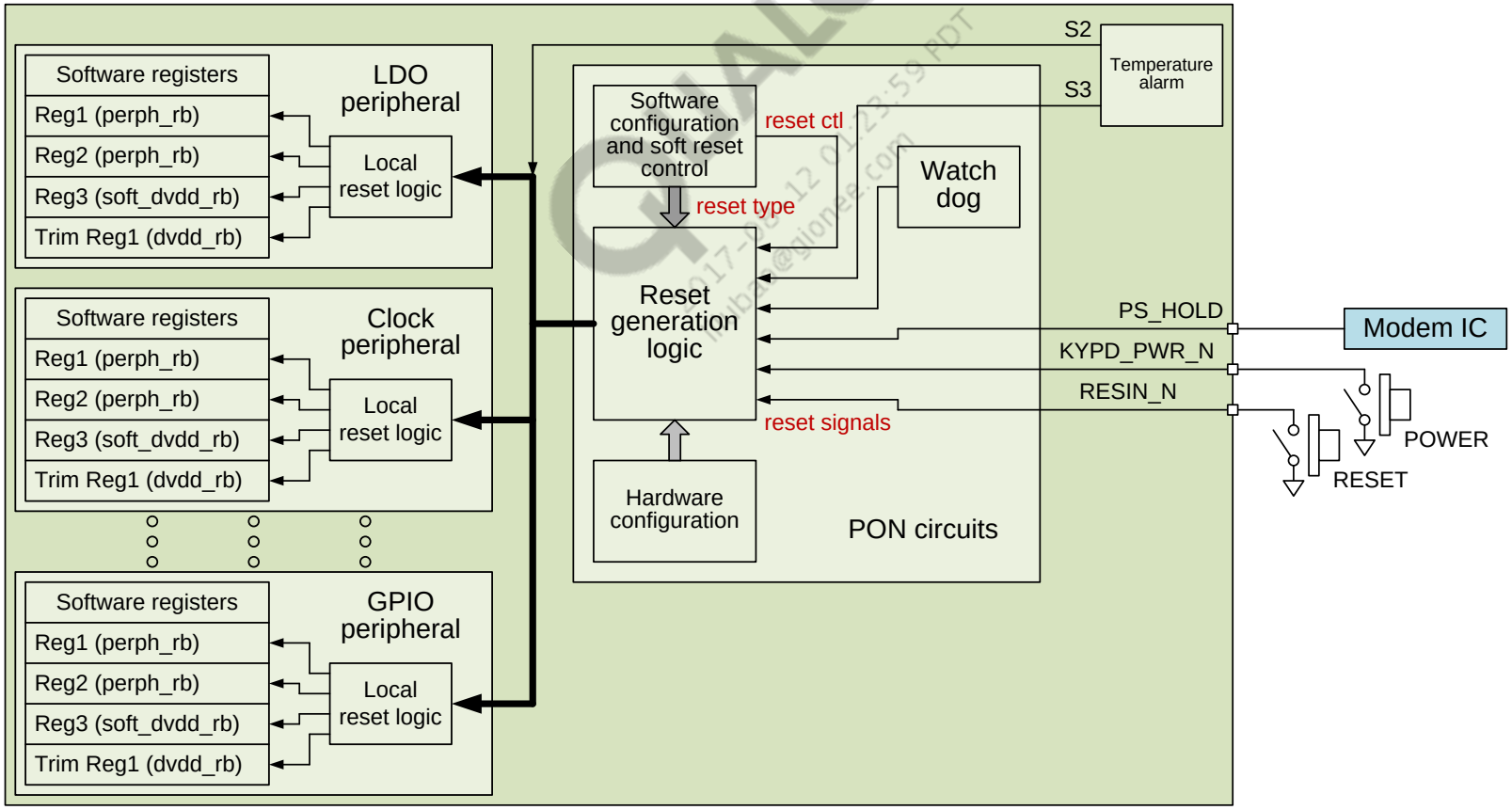
PBS command set

- Write/read
- Delay
- Compare
- End-of-sequence
- Up to 256 commands supported in RAM
- Up to ~232 commands supported in ROM (OTP) with some space reserved for PTE, version control

Reset Architecture and Introduction

Multiple reset triggers are supported

- Examples include power-on button, overtemperature, PS_HOLD, and dedicated reset button.
- By default, all peripherals follow all resets.
- Software can individually configure each peripheral to ignore each reset trigger individually via masking.
  - Maintain core supply voltages during watchdog reset (for debug)
  - Maintain LCD backlight during reset (maintain LCD content through reset)



Resets – Nomenclature

- Reset triggers
  - Internal and external triggers that are routed to the PMIC's power-on module; the module decides what action should be taken based on these triggers (stage 3 overtemperature, KYPD_PWR_N, RESIN_N, and PS_HOLD)
- Reset types
  - Describes the behavior of the PMIC during a reset or shutdown event (like a warm reset or hard reset event)
  - The type of reset event is determined by configuration registers in the power-on module and broadcast throughout the PMIC using reset signals
- Reset signals
  - Signals that are generated in the power-on module and broadcast throughout the PMIC (e.g., xVdd_rb, dVdd_rb, global_soft_rb, and shutdown1_rb).
  - (Register) reset domains
  - Several reset domains exist to allow some PMIC registers to maintain state throughout certain reset events
- Reset stages
  - Three stages of resets: software configurable bark, software configurable reset, and failsafe reset

Three-stage Reset and External Resets

Stage 1 reset: Software-configurable bark

- The PMIC generates an interrupt, giving the MSM device the opportunity to fix the problem or gracefully reset the system. Example events that can cause a bark include:
  - Overtemperature indicates that the system is getting too hot.
  - The PMIC watchdog indicates that it has not kicked.

Stage 2: Software-configurable bite

- If reset is ignored, the PMIC forces a reset event (selectable by software).

Stage 3: Hardware mandatory bite

- The user can generate a mandatory reset by a long keypress of RESIN_N, KYPD_PWR_N or RESIN_N plus KYPD_PWR_N in combination.
- The standalone or combination of reset triggers can also be selected as SBL by directly writing to the appropriate registers.
- Other comments:
  - Stage 3 cannot be disabled by software.
  - It resets the PMIC back to the factory default.
  - Stage 3 is a backup option if stages 1 and 2 fail.

External sources of reset (programmable)

- Power button (KYPD_PWR_N)
- Reset button (RESIN_N)
- Power button + reset button
- Applications processor (PS_HOLD)
- Keypad combination (up to three keys)
- Software write
- PMIC watchdog
- PMIC overtemperature sensor
- UVLO (mandatory immediate shutdown)

Reset Timers

#	Reset trigger	Stage 1 reset (debounce) timer	Stage 2 reset (delay) timer	Stage 3 reset timer
1	KYPD_PWR_N	0–10.256 s	0–2 s	0 s 2–128 s
2	RESIN_N	0–10.256 s	0–2 s	0 s 2–128 s
3	KYPD_PWR_N + RESIN_N	0–10.256 s	0–2 s	0 s 2–128 s
4	Keypad press	0–10.256 s	0–2 s	0 s 2–128 s
5	PMIC watchdog	0–127 s	0–127 s	–
6	PS_HOLD	–	–	–
7	Global reset	–	–	–
8	Overtemperature reset	–	–	–

Notes:

- Refer Reset Scheme for the configuration of these reset triggers in PM89xx and PMI89xx.
- The default values of the debounce and the delay timers for the watchdog reset are 31 s and 32 s, respectively.

Reset Scheme

- All key press based resets on PMI89xx should be disabled except S3
  - PMI RESIN_N & KYPD_PWR_N S2 Reset = Disabled
  - PMI RESIN_N S2 Reset = Disabled
  - PMI KYPD_PWR_N S2 Reset = Disabled
- Only PM89xx should initiate all key press based resets
- PMI89xx PS_HOLD is used for all SW initiated and long key-press resets
- PMI89xx S3 timer should be set thrice as long as PM to ensure it is triggered only when intended
- Warm reset is not supported in mission mode

PON Recommendations (1 of 3)

System level reset trigger	Reset type	PM reset setting (S1, S2 and type)	PMI reset setting (S1, S2 and type)	PM8004 reset setting (S1, S2 and type)	Notes (sequence of events)
Config at boot (by SW for production)		PS_HOLD = dVdd_HR	PS_HOLD = xVdd_SD	PS_HOLD = xVdd_SD	PMI and PM8004 set to xVdd_SD to support fail safe reset.
		KYPD_PWR_N S2 = dVdd HR	All S2 reset disabled.	RESIN_N S2 = WR	
				All other S2 reset disabled	
Power key	dVdd hard reset	KYPD_PWR_N S2 = dVdd HR	xVdd SD will occur	WR then xVdd SD will occur	KYPD_PWR_N press-> PM8952 PON_RST_N goes low -> triggers PMI xVdd SD and PM8004 WR.
	Warm reset	KYPD_PWR_N S2 = WR	xVdd SD will occur	WR will occur	After WR and dump collection, MSM must issue a hard reset via PS_HOLD.
MSM PS_HOLD	dVdd hard reset	PS_HOLD S2 = dVdd HR	PS_HOLD S2 = dVdd SD	WR then xVdd SD will occur	
	Hard reset	PS_HOLD S2 = HR	PS_HOLD S2 = SD	WR then xVdd SD will occur	
	Warm reset	PS_HOLD S2 = WR	PS_HOLD S2 = WR	WR will occur	After WR and dump collection, MSM must issue a hard reset via PS_HOLD.
	Shutdown	PS_HOLD S2 = SD	PS_HOLD S2 = SD	WR then xVdd SD will occur	
	dVdd shutdown	PS_HOLD S2 = dVdd SD	PS_HOLD S2 = dVdd SD	WR then xVdd SD will occur	
WR: Warm reset SD: Shutdown					

PON Recommendations (2 of 3)

System level reset trigger	Reset type	PM reset setting (S1, S2 and type)	PMI reset setting (S1, S2 and type)	PM8004 reset setting (S1, S2 and type)	Notes (sequence of events)
RESIN_N	dVdd hard reset	RESIN_N S2 = dVdd HR	xVdd SD will occur	WR then xVdd SD will occur	
	Warm reset	RESIN_NN S2 = WR	xVdd SD will occur	WR will occur	After WR and dump collection, MSM must issue a hard reset via PS_HOLD.
Key combo (Power key + volume down)	dVdd hard reset	KYPD_PWR_N + RESIN_N S2 = dVdd HR	xVdd SD will occur	WR then xVdd SD will occur	
	Warm reset	KYPD_PWR_N + RESIN_N S2 = dVdd HR	xVdd SD will occur	WR will occur	After WR and dump collection, MSM must issue a hard reset via PS_HOLD.
Fail safe (S3) reset	KYPD_PWR_N	Timer = X	Timer >= 3X	Timer >= 3X	Master PMIC S3 timer will always expire first. This will cause xVdd SD on all slave PMICs via PS_HOLD. Fail safe reset will occur at time X and user should never need to hold the button long enough to trigger slave PMIC S3.
	RESIN_N	Timer = X	Timer >= 3X	Timer >= 3X	
	KYPD_PWR_N and RESIN_N	Timer = X	Timer >= 3X	Timer >= 3X	
PM over temperature reset (Internal)	No API	Normal SD occurs	xVdd SD occurs	WR then xVdd SD will occur	
WR: Warm reset SD: Shutdown					

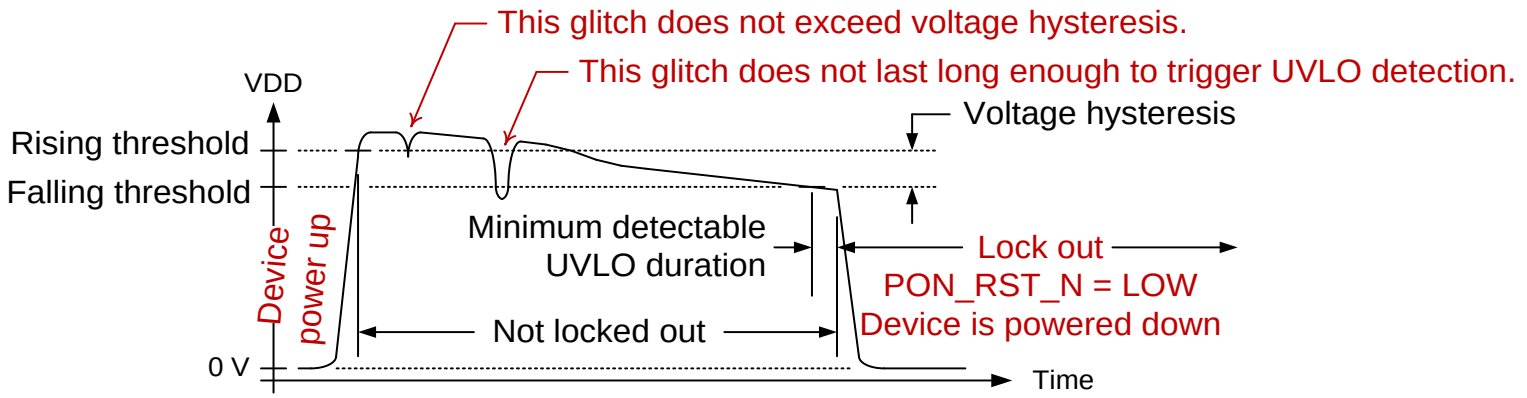
PON Recommendations (3 of 3)

System level reset trigger	Reset type	PM reset setting (S1, S2 and type)	PMI reset setting (S1, S2 and type)	PM8004 reset setting (S1, S2 and type)	Notes (sequence of events)
PMI over temperature reset (Internal)	No API	PMIC will stay on unless MSM shutdown the phone based on IRQ	PMI sends IRQ to MSM and performs normal SD	WR then xVdd SD will occur if core PMIC powers down	
PMI AFP reset (Internal)	No API	Charger will pull SYSOK low. PM GP1 triggers xVdd SD	AFP (HW default config: disable) If customer wants to enable this feature, they can configure this to SD	WR then xVdd SD will occur	Charger will pull SYSOK low. PM GP1 triggers xVdd SD
WR: Warm reset SD: Shutdown					

UVLO

The UVLO circuit automatically turns off the PMIC at severely low VDD conditions. Although UVLO is a hardware feature, it allows for software interaction to realize additional features, such as SMPL recovery, power-on sequence abort, and watchdog timeout soft reset.

- Operation
  - At power-up, VDD must exceed a rising threshold to initiate the power-on sequence.
  - Voltage hysteresis (300 mV default) and delays prevent minor glitches from being detected as UVLO events.
  - If VDD drops below the falling threshold (UVLO rising threshold minus voltage hysteresis) for a sufficient duration, a valid UVLO event is detected.
    - PON_RESET_N is cleared (LOW) and the device is powered down.
- The UVLO rising threshold voltage is programmable (1.675 V–3.225 V, in 50 mV increments).
  - Other than this programmable threshold, software is not involved in UVLO detection.
  - Hysteresis and time delays are not programmable, and UVLO events do not generate interrupts; they are reported to the modem IC via PON_RESET_N as part of power-down.

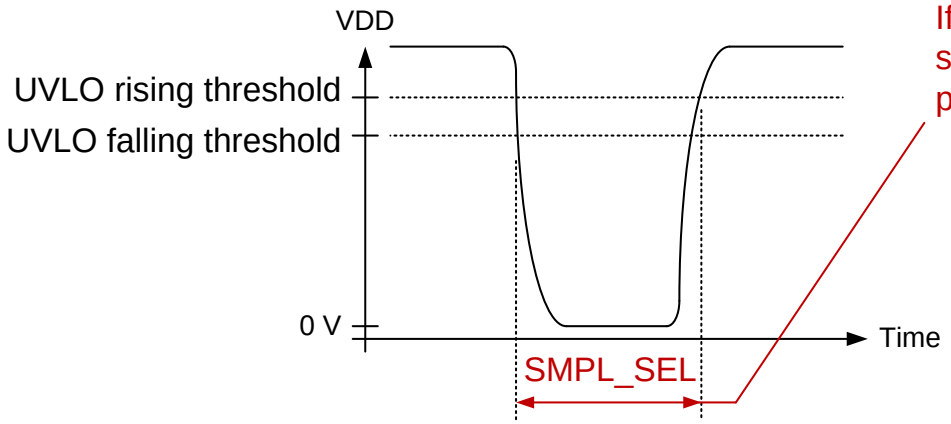


SMPL

When enabled by software → immediate and automatic recovery from a momentary PMIC power loss.

If VDD drops out of range (< 2.475 V nominal), then it returns in-range within a programmable interval of between 0.5 s–2.0 s, and the recovery is executed.

- Some operational details:
  - The UVLO event clears PON_RST_N; the PMIC is powered down.
  - A super capacitor or coin cell takes over as the SMPL power source.
  - If VDD returns to its valid range before timeout, a power-on sequence is initiated without software intervention, and an interrupt is sent to the modem IC indicating: 1) power was momentarily lost, 2) RTC is corrupted due to insufficient voltage, and 3) current PMIC actions are not a normal power sequence.
  - If SMPL times out without VDD returning to its valid range, the handset must undergo a normal power-on sequence whenever the next initializing event occurs.
  - SMPL operation must be enabled by software and requires a coin cell or keep-alive capacitor at VCOIN.
  - For a normal power-down, SMPL must be disabled via software before deasserting PS_HOLD to avoid an inadvertent SMPL override.



If VDD recovers within this programmed interval a power-on sequence is immediately and automatically initiated by power management circuits without software intervention.

If RTC support is not needed when the battery is removed, a backup capacitor can be used on the VCOIN pin. A ceramic capacitor with an effective capacitance of 10 µF can support SMPL for up to 2 s.

Section 10

Configurable I/Os

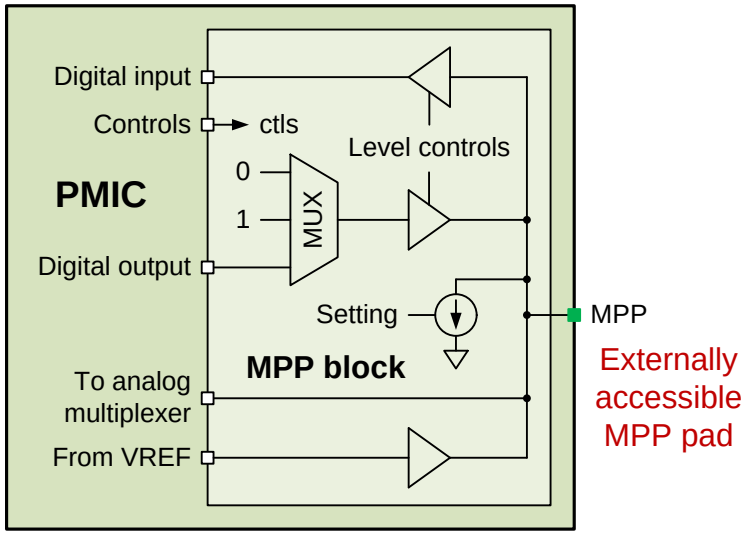
PMIC General Purpose I/O Pins

- The PM8937/PM8940 device has eight GPIOs.
- Standard GPIOs are the same on both PMICs.
- Two PM8937/PM8940 device high-speed GPIOs (GPIO [2:1], sometimes designated GPIOc) are available for driving clock outputs.
- PM8937/PM8940 device custom GPIO features (special connections that can only exist in specific GPIO locations):
  - Sleep clock driver (four dedicated)
  - Divided clock for codec
  - Battery and UICC alarm
  - External regulator enable (two dedicated)
- Custom features share GPIO pins, and therefore have concurrency limitations – see the GPIO Special Functions slide for availability.
- GPIO pairs include:
  - Each GPIO pin is assigned as a member of a pair
  - Each pair is a combination of sequential odd and even GPIO pins (GPIO_1 is paired with GPIO_2, etc.)
  - Each member can be assigned a different supply, so each pair can be used as a digital-level translator

PMIC Multipurpose Pins

The PM8937/PM8940 device has four MPPs; the PMI8937/PMI8940 device has three MPPs.

- The following configurations are available in MPPs with some exceptions:
  - Digital input: digital inputs applied to the pin can be read via software, can trigger an interrupt, or can be routed to another MPP (making this pin the input side of a level translator or current sink controller). The logic level is programmable, providing compliance between I/Os running off different power supplies.
  - Digital output: the output signal can be set via software to logic LOW or HIGH, can come from this pin's complementary MPP (making this pin the output side of a level translator), or can be tri-stated for use as a switch. The logic level is programmable, providing compliance between I/Os running off different supplies.
  - Bidirectional I/O: the two MPPs making up a complementary pair can be jointly configured as a bidirectional, level-translating pair. This is not supported by the PMI8937/PMI8940 device.
  - Analog input: inputs are routed to the analog multiplexer switch network; if selected, and that analog voltage is routed to the HK/XO ADC for digitization.
    - The PMI8937/PMI8940 device only has one ADC input (MPP1)
  - Analog output is a buffered version of on-chip voltage reference (VREF).
    - This is for odd MPPs only.
  - Programmable current sink is for driving LEDs.
    - This is for even MPPs only.



GPIO Special Functions

Pins	Function name	Description	GPIO SF1	GPIO SF2
GPIO01	CODEC_DIV_CLK	External regulator enable OR codec MCLK(9.6 MHz)	DIV_CLK2	SCAN_OUT<2>
GPIO02	SDCARD_DET_N	Internal debug purpose	SLEEP_CLK2	SCAN_OUT<3>
GPIO03	BATT_UICC_ALARM	Battery UICC alarm. Only acts as UIM alarm on PM8937/PM8940.	BATT_ALARM_OUT	SCAN_OUT<4>
GPIO04	BOOST_BYP_MODE_CTL	External boost-bypass control	GND	SCAN_OUT<5>
GPIO05	NFC_CLK_REQ (BBCLK2_EN)	NFC_CLK request OR BBCLK2 enable	GND	SCAN_OUT<6>
GPIO06	WLAN_SAD	Switched antenna diversity for WLAN	PWM_LPG	SCAN_OUT<7>
GPIO07	WCD9326 eLDO EN or BAT_ALARM_IN	External codec eLDO EN or BAT_ALARM_IN	GND	None
GPIO08	DSI-HDMI bridge chip 1.8 V eLDO6_EN	DSI-HDMI bridge chip	GND	SCAN_OUT<8>

PM8937/PM8940 MPP Special Functions

MPP	Function name	Description
MPP01	VDD_PX_BIAS	1.25 V reference voltage for MSM pads
MPP02	PA_Therm2	PA therm 2 - for second WAN chain
MPP03	VREF_DAC	1.25 V reference voltage
MPP04	QUIET_Therm or WLED_PWM_CTRL or HR_LED_sink	QUIET THERM or WLED Control PWM output or Home row

Section 11

Top-level Design Topics

PCB Stack-up, Parts Placement, and Routing Guidelines

PMI8937/PMI8940 and PM8937/PM8940 device PCB stack-up, parts placement, and routing guidelines are presented in the *MSM8937 Chipset Layout Guidelines* (80-P2468-3) and *MSM8940 Chipset Layout Guidelines* (80-P4978-3).

Unused Pin Terminations

Unused pin terminations can be found in the upcoming chipset schematic checklist:

- *MSM8937* + *PM8937* + *PMI8952/PMI8937 Schematic Review Checklist* (80-P2468-111)
- MSM8940 + PM8940 + PMI8952/PMI8940 *Schematic Review Checklist* (80-P4978-111)

Power Management Troubleshooting Techniques

The recommended troubleshooting sequence for an initial dual-PMIC power-up is as follows:

1. Check the PMI device charger input power supply voltage (USB_IN).
2. Check the PMI device charger output voltage (CHG_OUT).
3. Check the other input power pins (VDD_xxx) at both PMICs.
4. Verify the logic levels at the external control pins:
   - PM device: CBL_PWR_N
   - KYPD_PWR_N at both PMICs
   - RESIN_N at both PMICs
5. Check the internal reference voltages by probing the REF_BYP pin on both PMICs.
6. Check the regulated voltages that default to their ON state.
7. Each of these should settle to within 5% to 10% of their target voltage before the PMIC continues its power-on sequence by initiating the next regulator. The devices shut down if any of these default regulators do not turn on and settle properly.
8. If a device shuts down due to a failed regulator output, the start signal must be removed and re-applied to attempt another power up.
9. Monitor the PM device's PON_RESET_N; verify that it goes to logic high after all the default regulators power up correctly.
10. Monitor the PM device's PS_HOLD; verify that it is at logic high. It can transition between logic states throughout the power-on sequence but must be stable at logic high within hundreds of milliseconds after the PON_RESET_N signal went high. Confirm that this signal is applied to the PMI device's PS_HOLD pin.
11. If any of the first nine steps are not completed successfully, one of the installed PMICs has failed. If step 10 fails, there may be a problem with the modem device, one of the PMICs, or their interconnections.

Questions?

For additional information or to submit technical questions, go to:
https://createpoint.qti.qualcomm.com