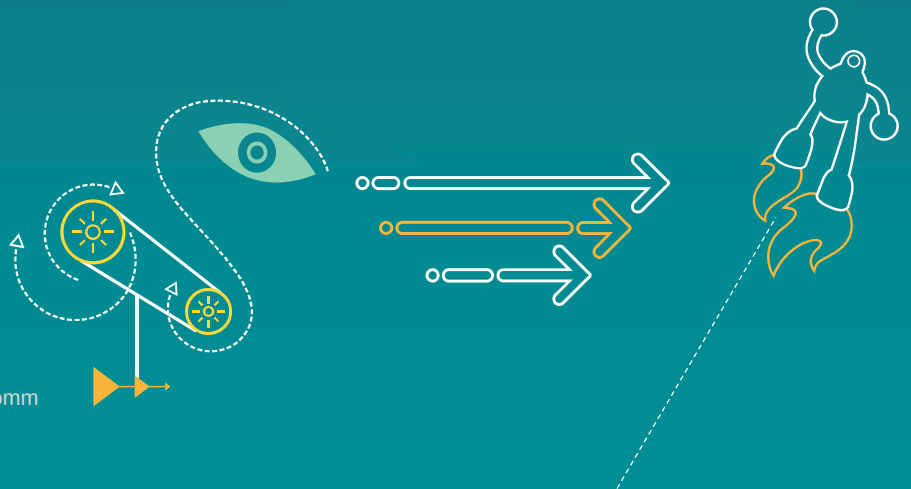
Design Guidelines – Digital Baseband

MSM8x74/MSM8x74AB

Qualcomm Technologies, Inc.



80-NA437-5B Rev. H

Qualcomm Technologies, Inc.
5775 Morehouse Drive
San Diego, CA 92121
U.S.A.

Revision History (1 of 5)

Revision	Date	Description
A	July 2012	Initial release
B	October 2012	Slide 18: Corrected the Adreno 330 features Slide 22–25: Added new slides about JTAG ID Slide 32: Corrected the DDr controller frequency and some features Slide 33: Updated the diagram for 1.2 and 1.8 V power supply Slide 39: Added bus frequencies Slide 43: Removed reference to sleep clock crystal Slide 44: Corrected VDD_MEM voltage to 0.95 V Slide 46: Removed MPM entry sequence table Slide 47: Removed MPM exit sequence table Slide 49: Corrected the boot sequence in diagram Slide 51–54: Updated slides with new information on security Slide 55: ▪ Corrected note about FORCE_USB_BOOT fuse ▪ Removed reference to OTG Slide 56: Cleaned up the diagram for boot_config Slide 57: Removed bullet at the bottom about VDD_QFPROM_PRG Slide 60: Updated QFPROM PON sequence Slide 62: Added info on QFPROM regions Slide 63: Added new slide about new QFUSES Slide 65–68, 71, and 72: Added new slides on security Slide 79: Corrected information on power supplies for modem Slide 80: Added new slide on UIM controller Slide 82: Removed bullet about virtualization Slide 83: Changed CPU maximum frequency to 2.3 GHz; changed the AHB bus to 64-bit Slide 84: Explained aSMP Slide 85: Updated diagram showing inductors Slide 86: Added new slide about Krait voltage control Slide 88: Updated the diagram showing more details about LPASS Slide 89: Added new slide containing details about LPASS Slide 90: Added new slide showing voice call data path Slide 96: Added info on NoC and configuration Noc Slide 100: Added bullet about VPE Slide 101: Corrected Adreno 330 features Slide 106: Added new slide about VPE

Revision History (2 of 5)

Revision	Date	Description
B (cont.)	October 2012	Slide 107: Corrected DSI controller version and data rate Slide 109: Added clarification for VDD_MIPI_DSI_0P4 trace, corrected the DSI clock frequency to 750 MHz Slide 113: Removed TBD Slide 114: Added new slide on eDP schematic connection Slide 122: Removed reference to VDD_MIPI_DSI_0P4 Slide 125: Corrected the data flow for different use cases Slide 131: Removed reference to 8960 feature Slide 132: Corrected Adreno 330 features Slide 135: Corrected typo on SDC voltage Slide 138: Removed bullet about drive strength Slide 139: Updated the USB diagram with data path Slide 140: Removed reference to OTG Slide 141: Corrected typo to show USB 2.0 port as secondary port Slide 143: Added new guidelines on USB signal routing Slide 144: Clarified unused USB termination Slide 150: Added more info on BLSP Slide 154: Added sub bullet on slow IrDA support Slide 157: Change UIM voltage to 2.95V Slide 167: Corrected SPI max frequency Slide 170: Added GPIO_92 and GPIO_95 to MPM capable GPIOs Slide 171: Corrected diagram on GPIO initialization Slide 179–180: Change pad size Slide 183: Added VDD_GFX pins Slide 192–193: Added note about star routing Slide 194: Added new slide on star routing recommendation Slide 195: Added VDD_GFX routing Slide 196: Updated the PDN targets and added PDN target for VDD_DDR_CORE_1P2/VDD_P1/VDD_P4 Slide 197–198: Corrected ohm symbol and added SMPS inductors Slide 201: Updated recommendation for unused pins

Revision History (3 of 5)

Revision	Date	Description
C	April 2013	Slide 8: Corrected the title of one of the document references Slides 13, 15, 16, 17, and 101: Updated the MIPI_CSI spec Removed the *MSM8x74 Variants* slide Slide 17: Updated the Krait microprocessor core frequency to 2.2 GHz Added slide 22: *BDP Package Outline* Removed the *Example: MSM8x74 Product Variants* slide Slide 30: Updated the Samsung model # for the *32 GB (x32) embedded NAND flash* memory component Slide 46: Updated the *Entering MPM Power-Saving Mode* flowchart Slide 53: Added note regarding external pulls and secure boot Removed the *Air Interfaces Supported* slide Slide 79: Updated all contents Slide 84: Updated several bullets Slide 108 and 121: Removed calibration voltage from layout guidelines Slide 112: Updated clock and data rate information Slide 117 and 119: Added a new camera interface Slide 117, 124, and 127: Removed “in-line” from the description of the JPEG image-processing feature Slide 122: Updated a CSI2 lane information Slide 141: Updated the schematic diagram Slide 142: Added note to the *90 Ω differential…* bullet Slide 143: Updated all contents Slide 150: Updated all contents Slide 160: Added note regarding GPIO_19/20 as a dedicated I2C for camera only Slide 186: Updated the *Current Consumption Data* document reference to 80-NA437-7 Slide 195: Updated the AC specification for VDD_CORE Slide 196 and 197: Added new slides to show the change in VDD_CORE AC specification Slide 198: Updated the diagram Slide 201: Updated this slide Slide 202: Added this slide (*TXDAC1 and ETDAC Connections for Different RF Configurations*)
D	July 2013	Slide 18: Updated Krait µP core frequency Slide 46: Added new slide: *Design Guidelines for SPMI* Slide 47: Added new slide: *Design Guidelines for XO_OUT_D0* Slide 137: Updated description and parameters of secure digital controller Slide 139: Updated schematic for secure digital controller Slide 140: Updated SDC1 and SDC2 layout guidelines Slide 143: Updated HS USB architecture diagram Slide 144: Updated SS USB schematic diagram Slide 145: Updated SS-USB guidelines

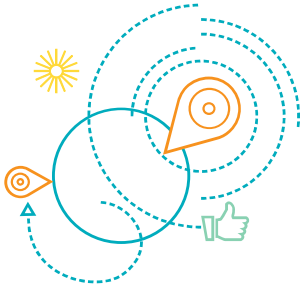
Revision History (4 of 5)

Revision	Date	Description
D (cont.)	July 2013	Slide 146: Added comment referencing application note for information regarding eye diagram tuning by software Slide 152: Added trace spacing constraint for SLIMbus Slide 162: Changed the pull-up on the UIM detect line from 10k to 100k Slide 170: Added trace spacing constraint between SLIMbus and other signals Slide 173: Added new slide: *Switch for MIPI RFFE Devices* Slide 203: Updated VDD_KRAIT power supply routing diagram Slide 204: Updated VDD_CORE and VDD_GFX power supply routing diagram Slide 208: Deleted WTR1625(L) related information since the MSM8974 does not support WTR1625(L)
E	December 2013	Updated document title to include MSM8x74AB Slide 22: Added MSM8x74AB new features Slide 25: Removed old JTAG Convention page Slides 25 and 26: Removed “planned” from the slides’ title Slide 31: Updated slide with MSM8x74/MSM8974AB Available LPDDR3 PoP Memory Slide 33: Added DDR controller clock with up to 933 MHz for MSM8974AB Slide 34: Updated the slide with MSM8x74AB and eMMC5.0 devices Slide 46, 47, and 48: Updated Design Guidelines for SPMI Slide 50: Removed the external LDO for VDD_ALWAYS_ON as it is not needed Removed the Run-time Integrity Testing slide Slides 85, 86, and 89: Updated the Krait information Slide 124: Updated MIPI Camera Serial Interfaces – Layout Guidelines (4-lane Example) Slide 137: Updated Secure Digital Controller features with new added MSM8x74AB eMMC5.0 feature Slides 140 and 141: Updated SDC1 layout guidelines Slide 146: Updated DIFFCLK signals routing recommendation to 90 Ω differential impedance and added board level guidelines Slide 147: Removed routing guideline for XO_OUT_D0 Slide 163: Added note for the external ESD diodes on UIM signals for protection Slide 174: Updated the reference document list for more information on existing issues in switch for MIPI RFFE devices Slide 201: Added a note on power distribution network requirements Slide 204: Updated the block diagram with the added inductors Slide 209: Updated the table TXDAC1 and ETDAC Connections for Different RF Configurations with WTR1625 configurations

Revision History (5 of 5)

Revision	Date	Description
F	March 2014	Slide 23, removed the eMMC5 software support timeline since the information is out of date Slides 35 and 140, updated the SDC1 block diagram reflecting to the latest reference schematic Slide 47, added the MSM8x74AB CS SPMI routing guideline Slide 112, updated VDD_MIPI_DSI_0P4 DC resistance to < 50 mΩ Slide 141, corrected the typo and added an additional bullet for SDC1 and SDC2 layout guidelines Slide 142, added the note for eMMC4.5/eMMC5.0 routing guideline Slide 149, reworded the slide for terminating unused USB pins for clarity Deleted the Power Routing and Bypassing – Example of Others slide Added Power Routing and Bypassing – 1.2 V DDR Supply slides (202, 203, and 204)
G	June 2014	Slide 19: Corrected the QDSP frequency of modem and LPASS to match the frequency from the clock plan Added slide 165: USB UICC
H	November 2014	Slide 126: Updated the application examples and added invalid configuration diagrams on the *MSM8x74 MIPI CSI Flexibility* slide Slide 177: Updated the graphic on the *Configurable GPIO Ports and MPM Support* slide

Contents



Sec. 1

Documentation Overview

Design Guidelines and Training Slides

Topic-specific design guidelines (some may be pending release)

80-NA437-5A	*MSM8274/MSM8674/MSM8974 Chipset Design Guidelines – Introduction*
80-NA437-5B (this doc)	*MSM8x74/MSM8x74AB Chipset Design Guidelines – Digital Baseband*
80-NA437-5C	*MSM8274/MSM8674/MSM8974 Chipset Design Guidelines – System Topics*
80-N5420-5A	*WTR1605(L) RF Transceiver with MSM8x74/MDM9x25 Design Guidelines*
80-N5420-5B	*WTR1605-based SVD for MSM8x74/MDM9x25 Design Guidelines*
80-NA555-5	*PM8841 and PM8941 Power Management Design Guidelines*
80-WL300-5	*WLAN/Bluetooth/FM Design Guidance and Training using WCN3660, WCN3660A, or WCN3680 Design Guidelines*
80-NA556-5	*WCD9320 Audio Codec IC Design Guidelines*
80-NA805-5A	*WTR1625L RF Transceiver and WFR1620 RF Receiver Design Guidelines/ Training Slides*

Chipset training slides with embedded audio

- AU80-xxxxx-xx
  - Most topic-specific design guidelines documents will have a corresponding set of training slides with embedded audio.
  - The document number's suffix will depend upon the recorded language.
  - Audio training slides are available on Documents and Downloads within each chipset folder.

Chipset-wide design guidelines

- Collection of topic-specific design guidelines within a single folder on Documents and Downloads
- Refer to the following few pages for further explanation.

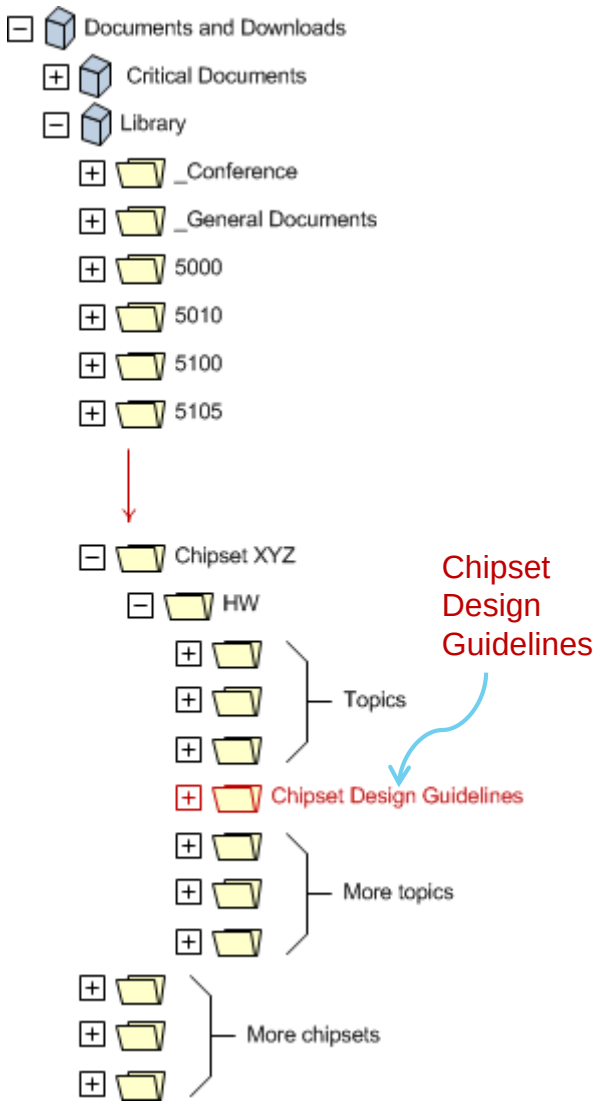
Chipset-wide Design Guidelines

The chipset-wide design guidelines are a collection of topic-specific design guidelines that share a single folder under Documents and Downloads.

Navigation steps:

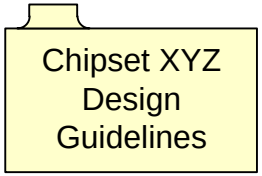
1. https://support.cdmatech.com
2. → Docs & Downloads
3. → Documents and Downloads
4. → Library
5. → Desired chipset (example: Chipset XYZ)
6. → HW
7. → Chipset Design Guidelines

Refer to the next two pages for instructions on downloading the chipset-wide design guidelines and enabling chipset-wide word-search capabilities.

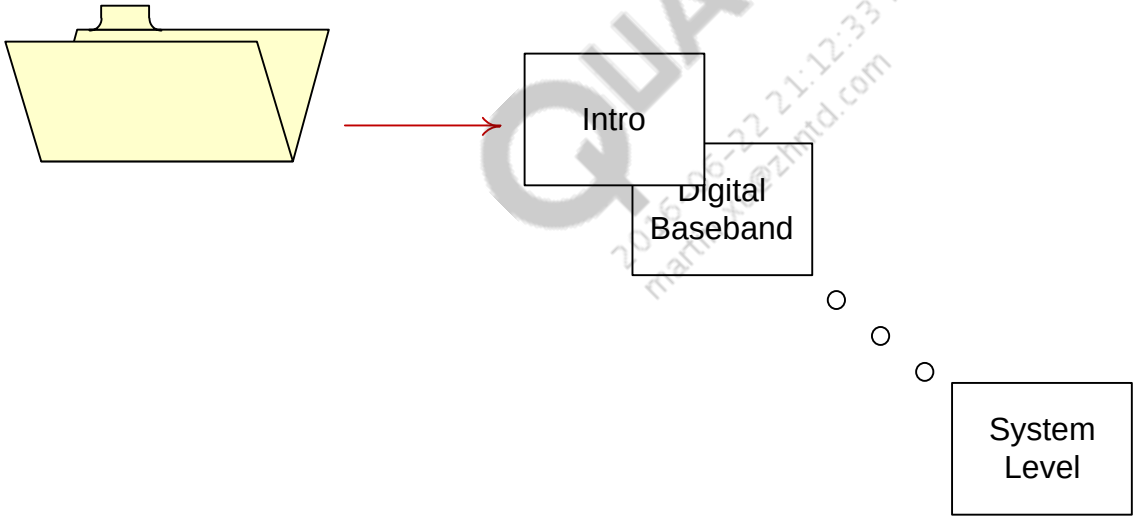


Downloading the Chipset-wide Design Guidelines

1. Create a folder on your computer into which the PDF files will be downloaded.



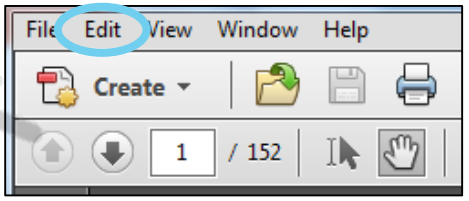
2. Access the Documents and Downloads chipset design guidelines folder as explained on the previous slide.
3. Select all the PDF files within the Documents and Downloads chipset design guidelines folder.
4. Right-click to download; specify the created folder as the download destination.
5. Confirm that all PDF files were downloaded into the created folder as desired.

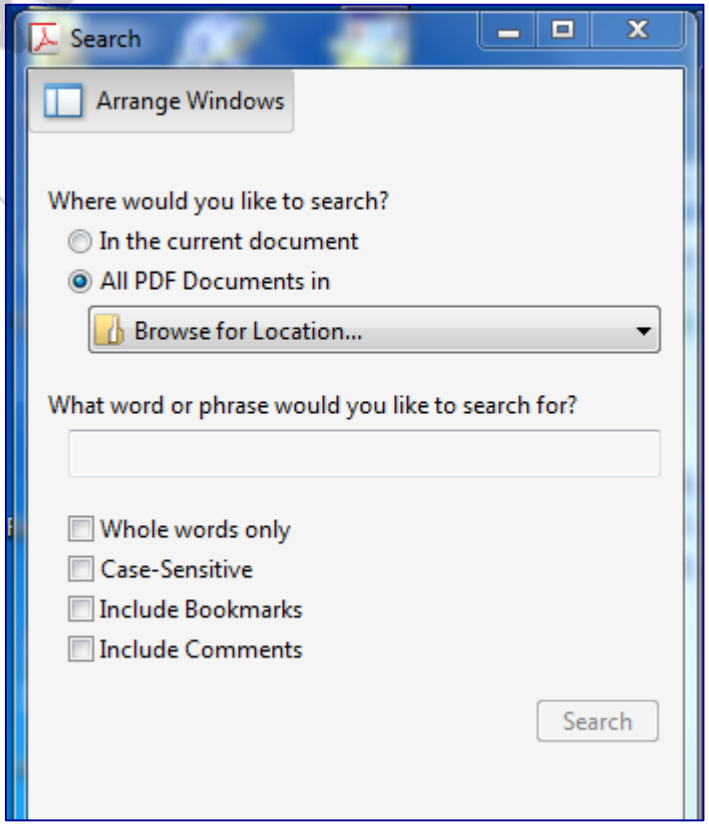


The contents of this folder make up the chipset-wide design guidelines “document.”

Enabling Chipset-wide Word-search Capability

1. Open the Chipset XYZ Design Guidelines folder on your computer.
2. Double-click any PDF to open it.
3. Use the **Edit** pull-down menu to select **Advanced Search**.
   - The Search window opens.
4. In the **Search** window, select the option to browse for the search domain.
5. Locate the Chipset XYZ Design Guidelines folder.
6. After selecting the folder as the search domain, enter the desired word or phrase to search for.
   - All PDF documents in the folder will be searched for that word or phrase.
   - The selected search domain will remain the default option for all the PDF files in the folder until all files are closed – whenever the Advanced Search feature is used.





Design Guidelines vs. Training Slides

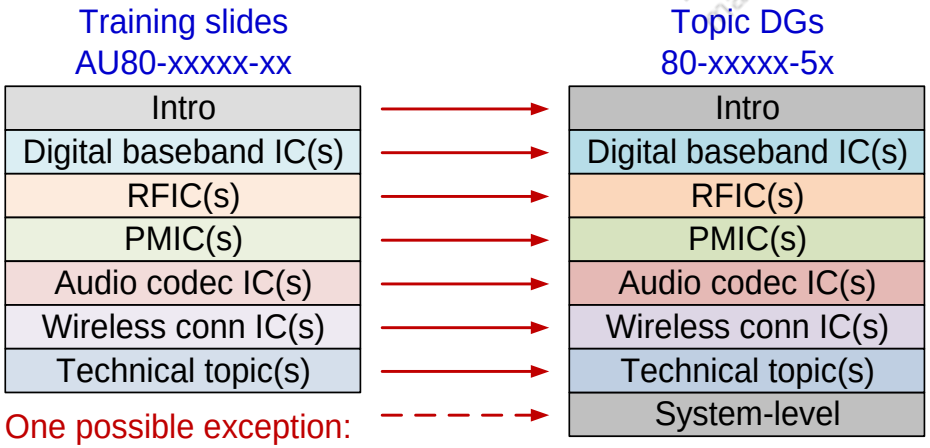
Differences between slides and design guidelines (DGs):

- DGs do not include embedded audio – training slides include embedded audio with multiple languages.
- Slides are released as needed to support training seminars only – they are not updated continuously.
- DGs are maintained with the most up-to-date information (always download the latest DGs).
- Slides include only the topics that are presented at training seminars.
- DGs are more complete – they contain more topics and greater detail (as appropriate).

Individual vs. chipset-wide DGs:

- Each topic-specific DG is the same, whether it is downloaded by itself or as part of the chipset-wide DG.
- Benefits of the chipset-wide DG folder on Documents and Downloads include:
  - All pertinent DG material is located in one easy to access location.
  - The entire chipset-wide DG can be searched for any topic of interest (via the PDF word search explained earlier).

Generally, there will be a 1-to-1 correlation between training slides with embedded audio and topic-specific design guidelines.



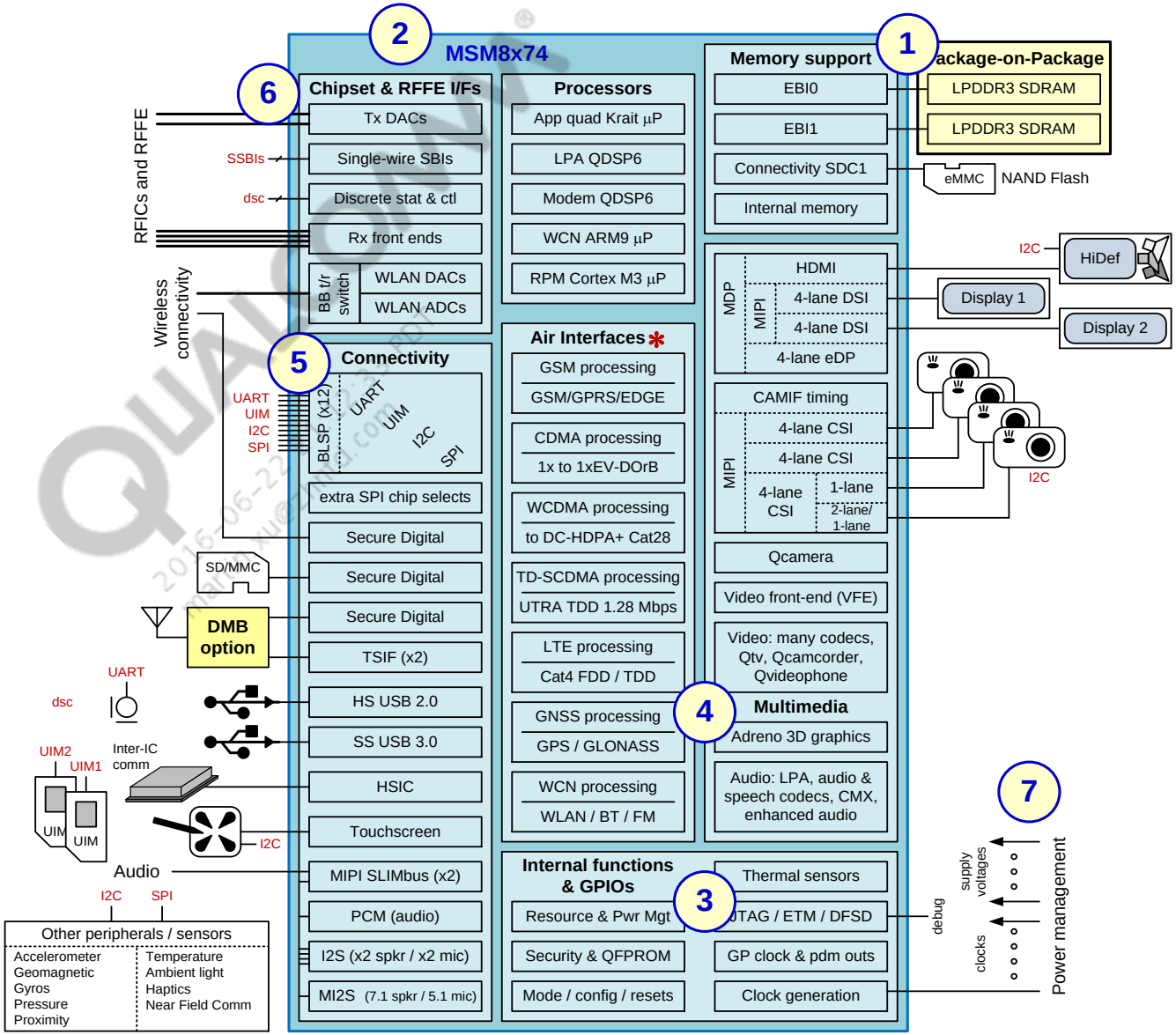
One possible exception:
the system-level topic might not be included in the training slides.

The digital baseband system and MSM™ ICs are introduced next …

… and then the remaining digital baseband material is split into seven major sections:

1) Memory support
2) Overall IC architecture
   - Processors
   - Systems & subsystems
   - Bus systems
   - Air interfaces
3) Other key internal functions
4) Multimedia
5) Connectivity
6) Chipset & RFFE interfaces
7) Top-level topics
   - Parts placement
   - DC power distribution
   - Grounds
   - Unused pins
   - Thermal considerations

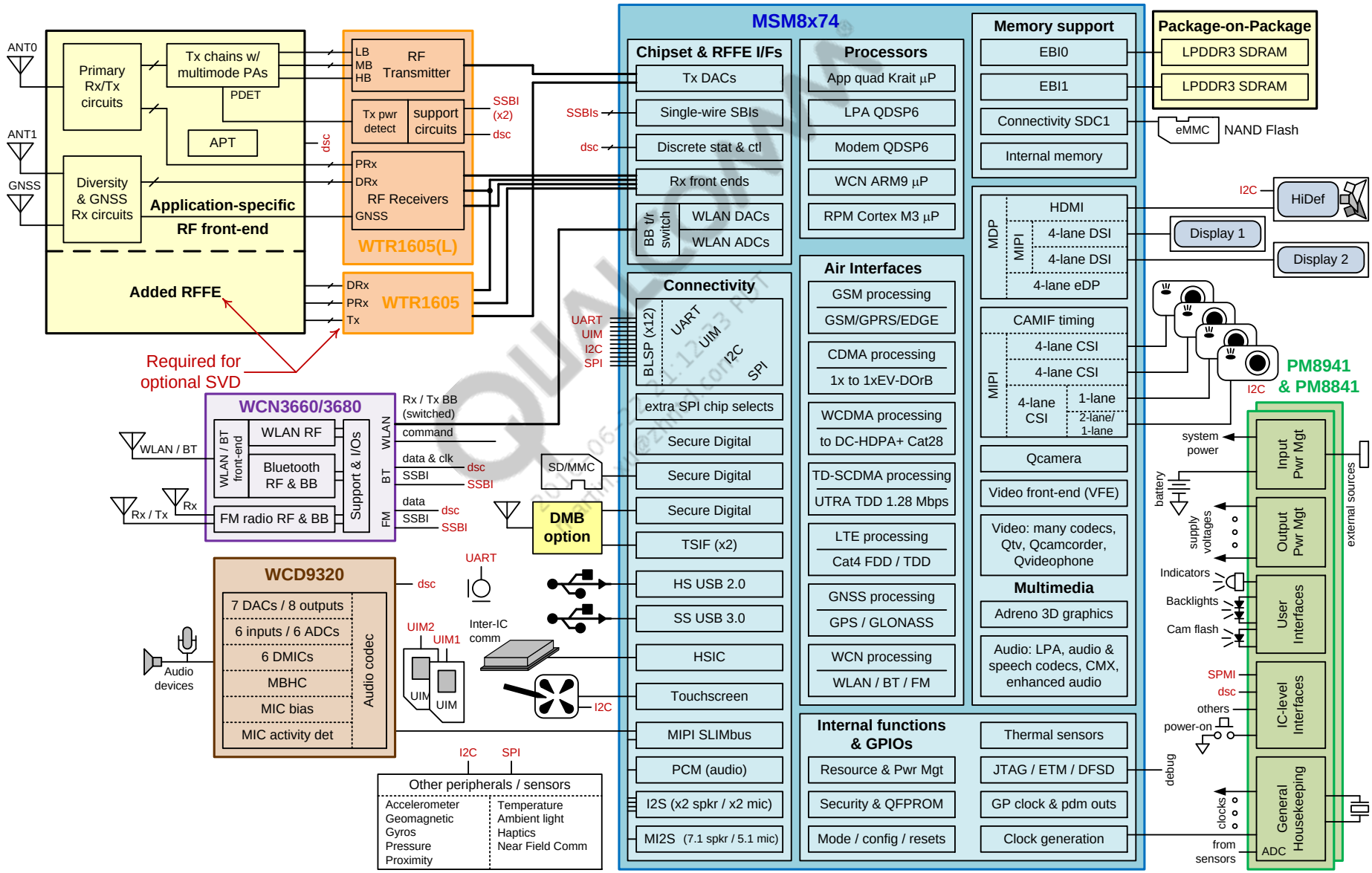
* Air interface, display, and camera support features are the primary factors defining MSM variants – MSM8274, MSM8674, or MSM8974.



Sec. 2

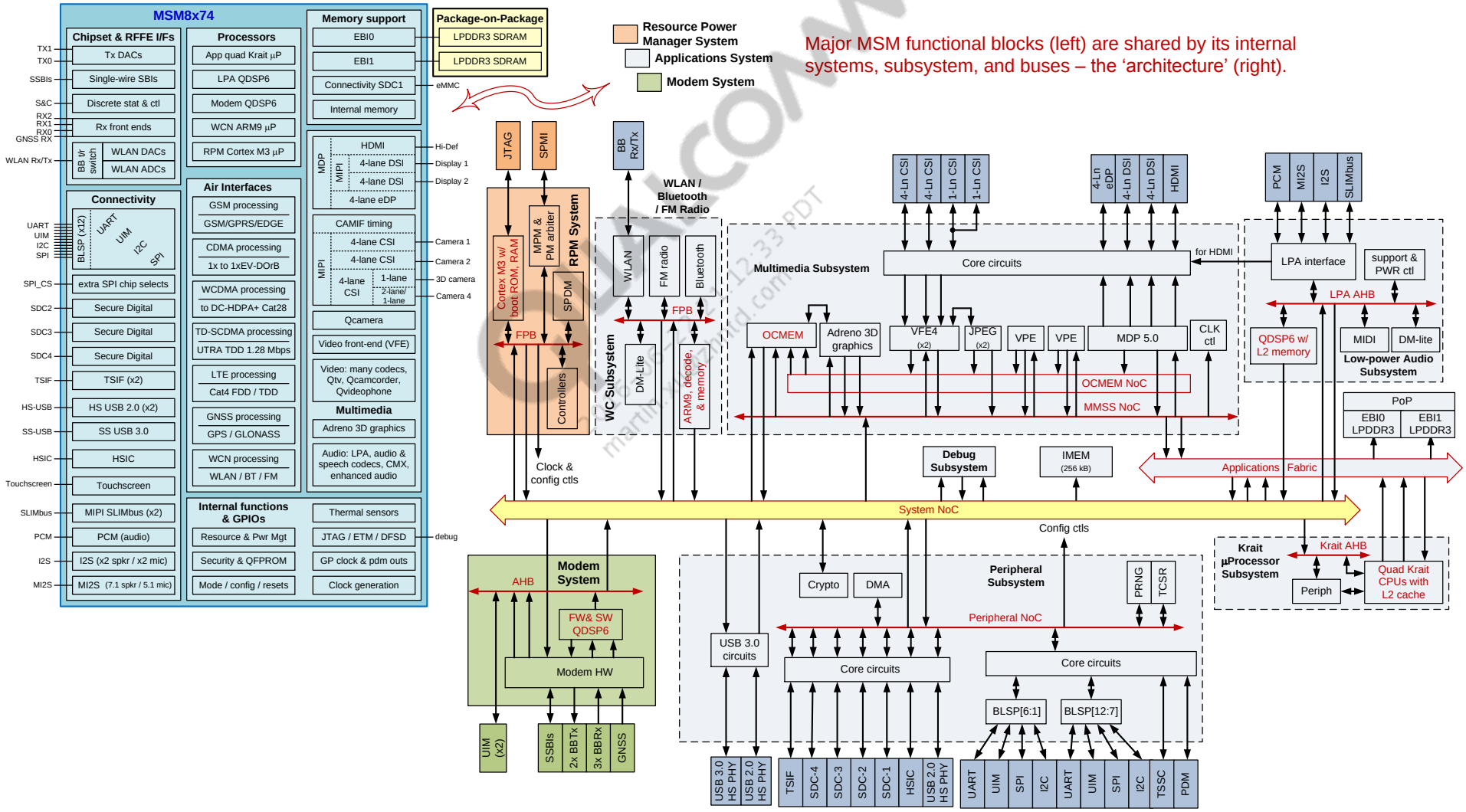
Digital Baseband System and IC Overview

Example Application



Digital Baseband Material – Architecture and Hardware Content

This document includes ‘architecture’ (internal MSM details) and external MSM design guidelines (hardware details).



MSM Chipset Features (1 of 4)

Feature	MSM8x74 capability
Processors	
Applications	Four Krait µP cores up to 2+ GHz; 2 MB L2 cache
Modem system	QDSP6 v5 core at up to 787.2 MHz 16k L1 instruction; 32k L1 data; 256k L2 caches
RPM system	Cortex M3 - primary boot processor – Better suited for code certification and warm boot – Brings up secure root of trust (SROT) Krait uP quickly The only master of the modem power manager (MPM) MPM coordinates shutdown/wakeup, clock rates, and VDDs Boot flow is RPM / applications processor-based
Low-power audio	QDSP6 v5 core at 680 MHz; 16k/32k L1 and 256k L2 caches
WLAN/Bluetooth/FM	ARM9
Memory support	
System memory via PoP & EBI	2x LPDDR3 SDRAM; 32-bit wide; up to 800 MHz
Other internal memory	1.5 MB unified SRAM pool on-chip memory (OCMEM)
External memory	
Via SDC1	eMMC/SD NAND flash devices
Via SPI	NOR memory devices (user-modified SW)
RF support	
RF operating bands	Defined by WTR device
Air interfaces	 GSM CDMA WCDMA TD-SCDMA LTE WLAN/BT/FM
GNSS – gpsOne™ engine	Gen 8B; GPS and GLONASS
Multimedia	
Display support	Up to three concurrent displays; two panels + external
MIPI_DSI	Two; 4-lane + 4-lane
HDMI	Yes; v1.4
eDP	Yes; v1.2 4-lane
Example combinations	(2560 x 2048) + (1080p external) (2048 x 1536) + (1920 x 1200) + (1080p external) (2048 x 1536) + (4k x 2k external)
General display features	Color depth – 24-bit pp; TFT, LTPS, CSTN, OLED panels
Camera interfaces	Qcamera; dual ISP
MIPI_CSI	Three 4-lane or four at 4 + 4 + 1 or 2 + 1 lanes; 1.5 Gbps per lane
2D performance	32 MP at 15 fps; 16 MP at 30 fps
3D performance	12 MP at 15 to 24 fps; 8 MP at 30 fps
General camera features	Pixel manipulations, camera modes, image effects, and post-processing techniques, including defective pixel correction VFE raw dump of CSI data at line rate to LPDDR3 SMIA++ support I2C or SPI controls

MSM Chipset Features (2 of 4)

Feature	MSM8x74 capability
Multimedia (cont.)	
Mobile display processor	MDP 5
Video applications performance	
Encode	1080p at 96 fps; 4kx2k at 30 fps; 4x 1080p at 30 fps – H.264/263, MPEG4, VP8 1080p at 60 fps 2-view – MVC
Decode	1080p at 120 fps; 4kx2k at 30 fps; 4x 1080p at 30 fps – H.264/263, MPEG4/2, WMV9, VC1, VP6/8, DivX, XVID 1080p at 60 fps 2-view – MVC
Graphics	Adreno™ 330 450 MHz 3D graphics accelerator 3600 M peak 3D pixels/sec APIs include OpenGL ES 1.1/2.0/3.0, DX9.3
Audio	
Codec	Integrated within the WCD9320 device 7 DACs, 8 outputs; 6 inputs, 6 ADCs; 6 digital MICs Multi-button headset control; MIC activity detection
Low-power audio	Low power, low complexity; 7.1 surround sound Versatile – many audio playback & voice modes; encoders for audio & FM recording; many concurrency modes
Voice codec support	SILK; QCELP, EVRC, EVRC-B, EVRC-WB; G.711, G.729A/AB; GSM-FR, -EFR, -HR; AMR-NB, -WB
Audio codec support	MP3; AAC, +, eAAC; WMA 9/Pro; Dolby AC-3, eAC-3, DTS
Enhanced audio	Surround sound: Dolby TrueHD; DTS-HD; DTS Express 7.1 Fluence ™ Noise Cancellation; enhanced speaker protection QAudioFX/Qconcert/Qensemble
A/V output – HDMI Rev 1.4a	Yes Integrated HDMI Tx core and HDMI PHY 1080p at 60 Hz refresh; 24-bit RGB color Up to 8-channel audio for 7.1 surround sound Dolby Digital Plus, Dolby True-HD, & DTS-HD Master
Web technologies	V8 JavaScript Engine optimizations Webkit browser JPEG hardware decode acceleration Networking Stack IP and HTTP tuning Flash 10.1 & Video Processor decode optimization
Messaging	Text messages; text encoding for SMS Multimedia messaging services – combined video (MPEG4), still image (JPEG), voice tag (AMR), text sent as message
Digital Mobile Broadcast (DMB)	External IC required; dual-TSIF for 12 segment ISDB-T
Connectivity	
BLSP ports	12, 4 bits each; multiplexed serial interface functions
UART	Yes – up to 4 MHz
UIM	Yes – SIM, USIM, CSIM; dual V (1.8/2.85) is available 1x
I2C	Yes – cameras, sensors, near field communicator (NFC), etc.
SPI (master only)	Yes – cameras, sensors, etc.; NOR memory with SW mods
UIM (other than via BLSP)	One – dual voltage (1.8/2.85 V)

MSM Chipset Features (3 of 4)

Feature	MSM8x74 capability
Connectivity (cont.)	
USB	Two – one USB 2.0 high-speed and one USB 3.0/USB 2.0
HSIC	MSM to/from external application processor
Dual-voltage (1.2/1.8)	Easy integration, low-power, & low processor loading
Secure digital interfaces	Up to 4 ports; one 8-bit and three 4-bit; SD 3.0
SDC1 and SDC2 are dual-V	SD/MMC card; eMMC NAND; DMB; WLAN; eSD/eMMC boot
TSIF	Up to two ports; DMB support
Audio interfaces	
SLIMbus	Highly multiplexed, high-speed; baseline WCD interface
I2S	Up to 4 ports (primary & secondary speakers & mics)
MI2S	Microphone & speaker functions, including 7.1 audio for HDMI
PCM	One port is available
Wireless connectivity	WCN3660 or WCN3680
WLAN	Both WCNs support 802.11a/b/g/n; WCN3680 adds 802.11/ac
Bluetooth	Bluetooth 4.0 LE and earlier
FM radio	Worldwide broadcast
Touchscreen support	Capacitive panels via external IC (I2C, SPI, & interrupts)
DMB support	Via external DMB device (SDC or TSIF)
Configurable GPIOs	
Number of GPIO ports	146 – GPIO_0 to GPIO_145
Input configurations	Pull-up, pull-down, keeper, or no pull
Output configurations	Programmable drive current
Top-level mode multiplexer	Provides a convenient way to program groups of GPIOs
Internal functions	
Security	
General security features	Secure boot, SFS, ARM® TrustZone, SEE, secure debug, Microsoft WM DRM10, HDCP for HDMI
Crypto engine	New Crypto version 5; Increased crypto throughput via increased frequencies and a new internal AXI based data master; Support for multiple execution environments per Crypto; Algorithm accelerate file system encryption (AES-XTS), IPSec & SSL (HMAC-SHA, CCM, CMAC)
QFPROM	Large fuse array, replaces previous-generation Qfuse chains, Non-volatile memory with faster and simpler programming
Security controller	Chip-wide configuration for security, feature enable, & debug Persistent storage of ID numbers and sensitive key data Support for the HDCP standard needed for HDMI Secure HDCP key provisioning and secure debug facility Primary and secondary hardware key blocking for SFS
Boot sequence	1) RPM system, 2) application system, 3) modem system Emergency boot over HS-USB Poweron boot to carrier splash screen < 0.4 seconds (target) Poweron boot to network access < 20 seconds (target)
PLLs and clocks	Multiple clock regimes; watchdog & sleep timers Inputs: 19.2 M CXO, 48 M WCN_XO for 5 GHz WLAN, 32.768 k sleep (optional) General-purpose outputs: M/N counter, PDM

MSM Chipset Features (4 of 4)

Feature	MSM8x74 capability
Internal functions (cont.)	
Resource and power manager	Fundamental to bootup and power management Key blocks: RPM core, Cortex M3, security controller, MPM Improved efficiency via clock control, split-rail power collapse & voltage scaling; several low-power sleep modes
Debug	JTAG, Design for Software Debug (DFSD), & ETM (all cores)
Others	Thermal sensors; modes & resets; peripheral subsystem
Chipset and RF front-end (RFFE) interface features	
WTR RF transceivers	
Baseband data	4 Rx & 2 Tx analog interfaces
Status & control	2 SSBIs for each RFIC, plus other lines as needed via GPIOs
Power management	2-line SPMI; plus other lines as needed via GPIOs
WCD audio codec	
SLIMbus	Highly muxed, high-speed audio data plus status & control
Legacy	Optional I2S for audio data plus I2C for status & control
Others	Status, control, & clock lines as needed via GPIOs
WCN wireless connectivity	
WLAN baseband data	Multiplexed Rx/Tx analog interface
WLAN status & control	Secure digital
Bluetooth	2-line data interface plus dedicated SSBI
FM radio	1-line data interface plus dedicated SSBI
Fabrication technology and package	
Digital die	28 nm HPm CMOS
Small, thermally efficient package	990 PNSP: 15 x 15 x 0.91 mm (w/o memory device on top)
Bottom pin array of PoP	Same as 990-pin nanoscale package (990 NSP); 0.4 mm pitch
Top pin array of PoP	Same as 216-pin chip-scale package (216 CSP); 0.5 mm pitch

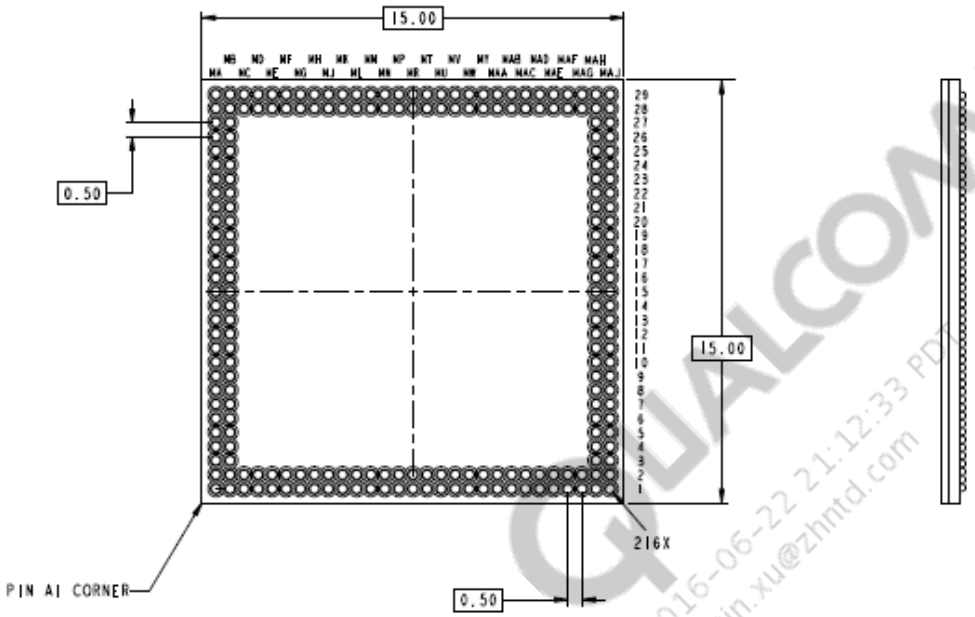
MSM8x74AB Features

The MSM8x74AB chipset will include the following changes from the MSM8x74 chipset:

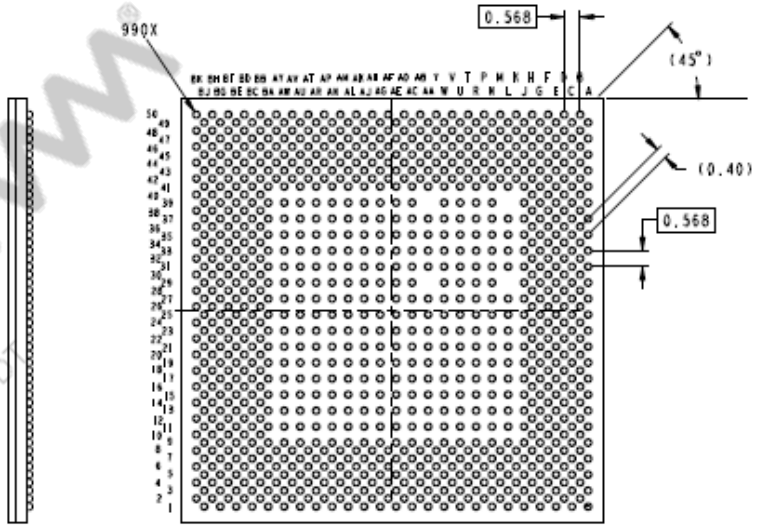
- Adreno 330 @ 578 MHz
- eMMC5
- LPDDR3 – 931.2 MHz
- ISP increase to 465 MHz
- WTR1625 RF support only
- Integrated DSDA, LTE/G+G DSDS – support in March ’14
  - Supported on LA3.0 with WTR1625L only
- DSDS (W/G+G) – support in January ’14
- MSM8x74AB will support BDP only (no MLP)
- MSM8x74AB chipset will have a -AA variant that will run at lower frequencies as shown below
- MSM8x74AB chipset will have a -AC variant that will run at a higher Krait frequency of 2.45 GHz as shown below

Feature code (BB)	CPU (GHz)	GPU (MHz)	ISP (MHz)	DDR (MHz)	ADSP (MHz)	RF transceiver
AC	2.45	578	465	931.2	800	WTR1625(L)
AB	2.26	578	465	931.2	800	WTR1625(L)
AA	2.26	450	320	800	680	WTR1605(L) or WTR1625(L)

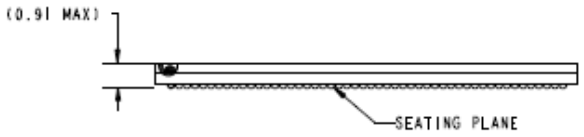
MLP Package Outline



TOP VIEW

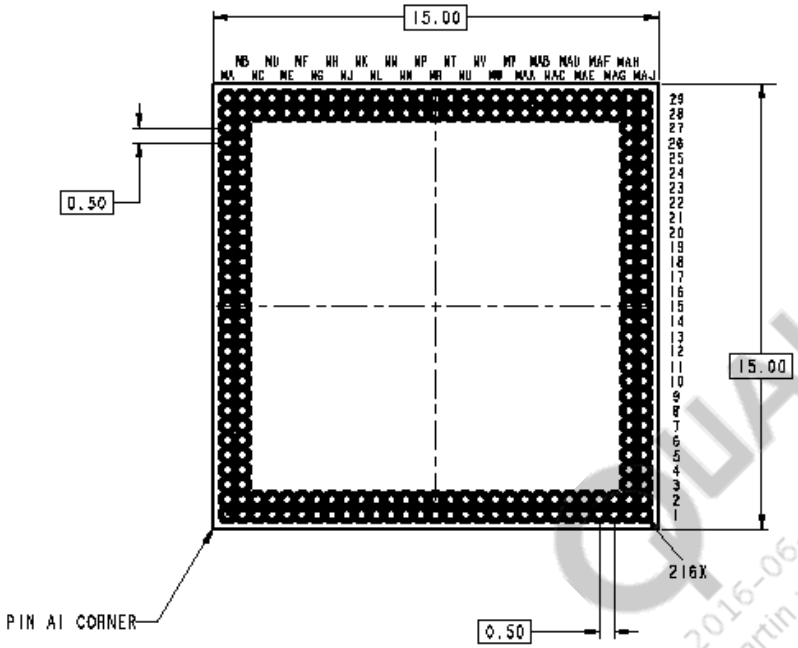


BOTTOM VIEW

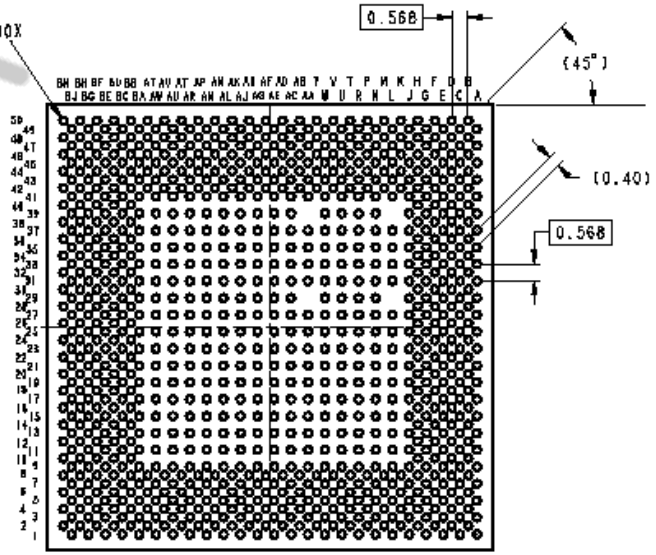


SECTION

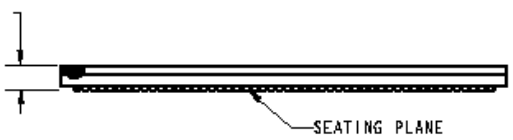
BDP Package Outline



TOP VIEW



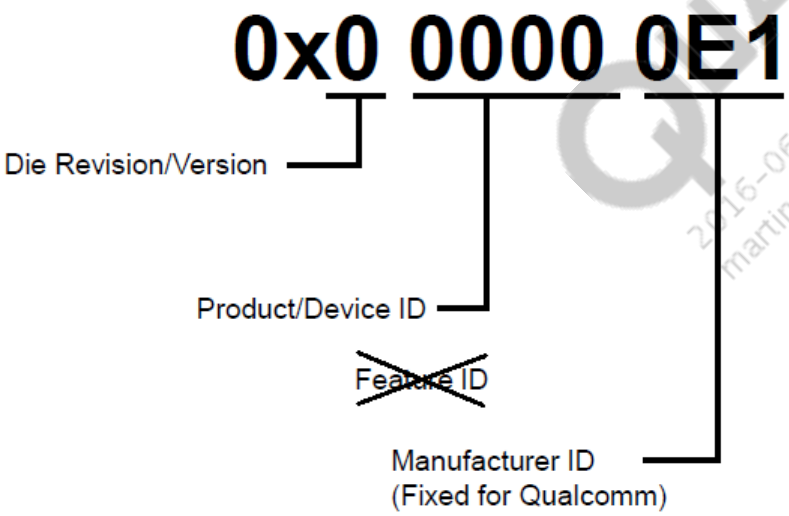
BOTTOM VIEW



SECTION

JTAG Convention for MSM8x74

- Move Feature ID field outside JTAG ID.
- Create a Product ID per family instead of per device.

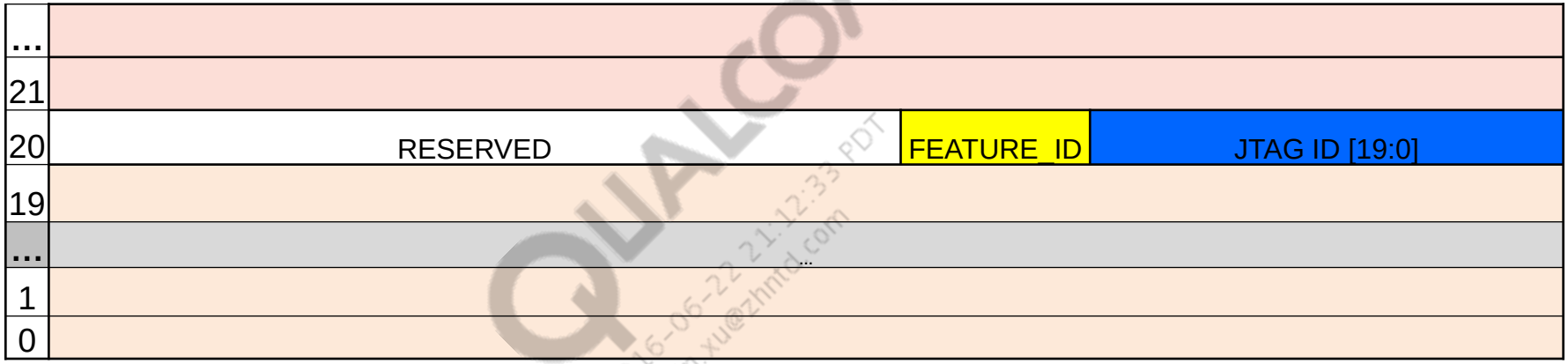


Fuse Location for Feature ID

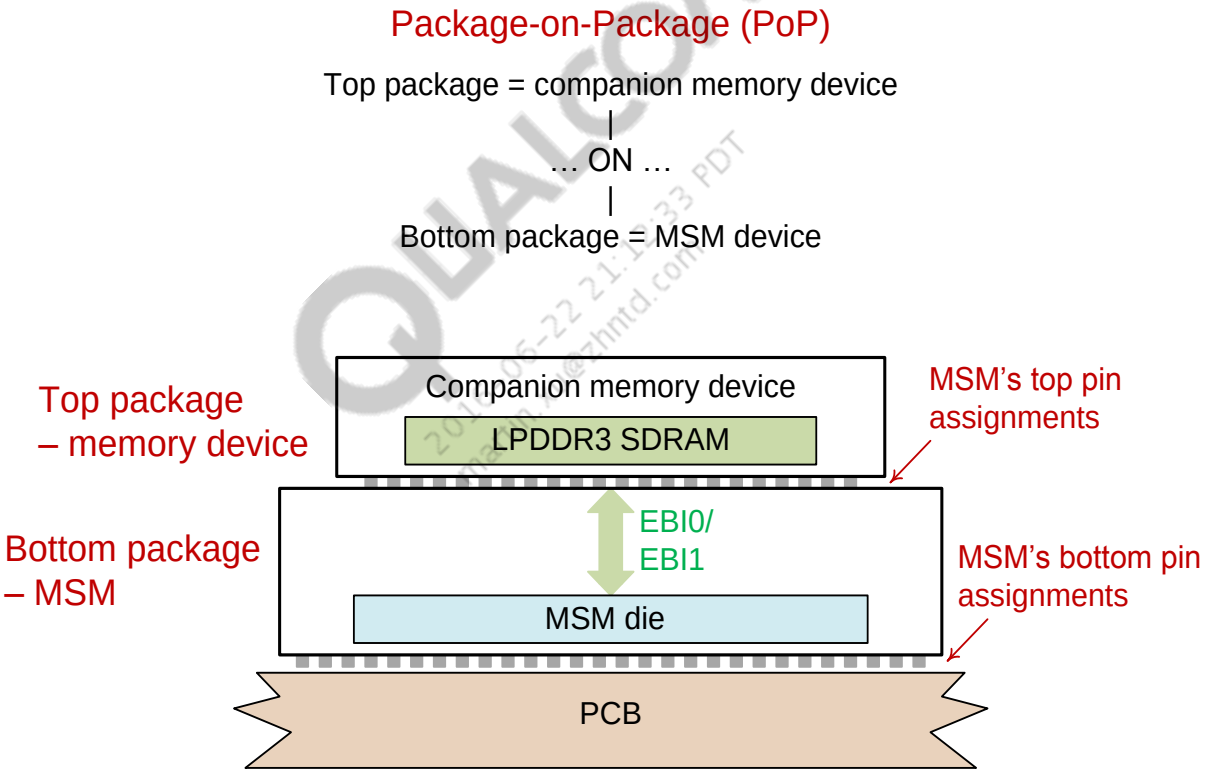
Place feature ID information in eight unused fuses of QFPROM row 20.

Fuse information can be read through the raw register:

QFPROM_RAW_JTAG_ID_LSB



Package-on-Package LPDDR3 SDRAM

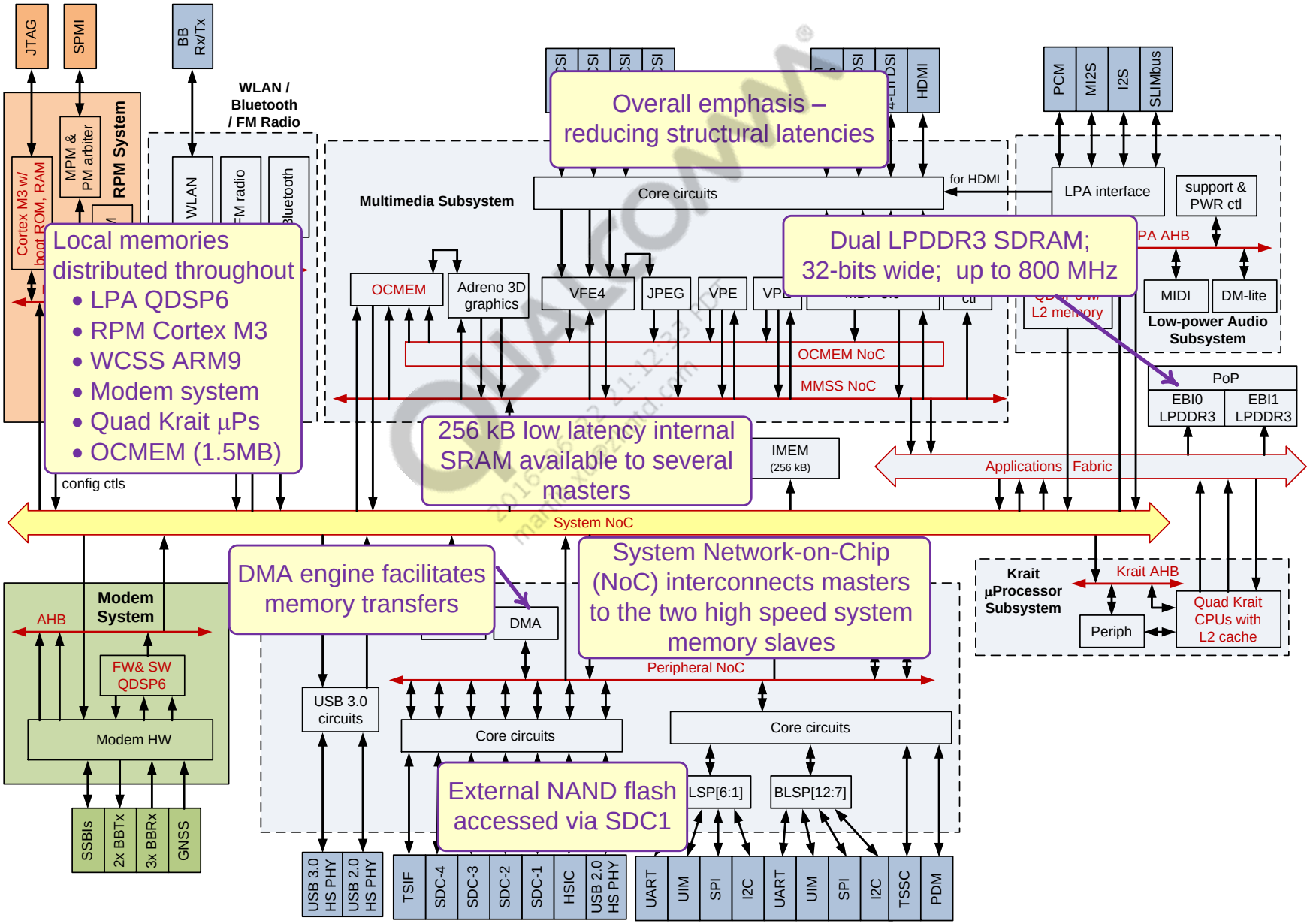


Sec. 3

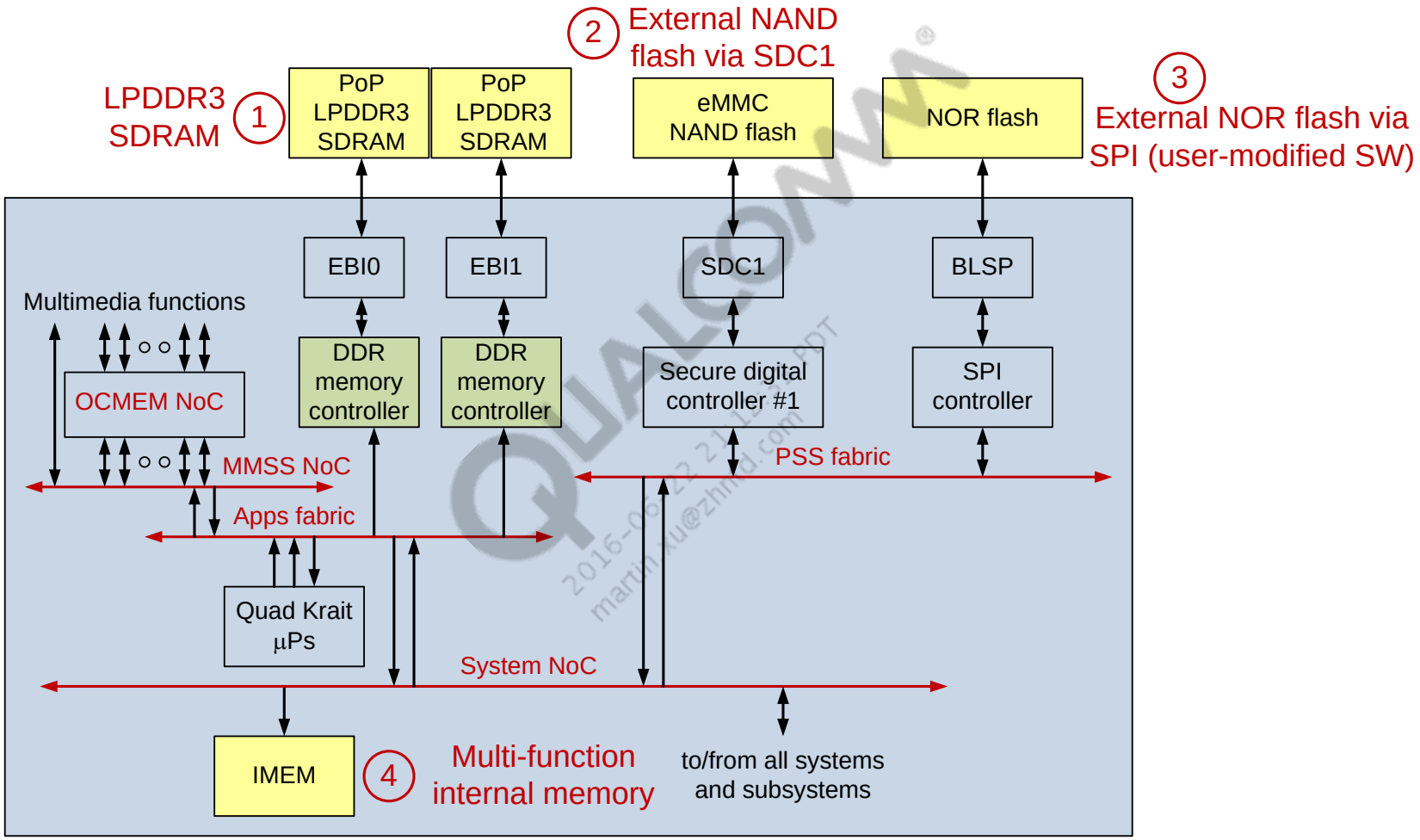
Memory Support

Note: *The MSM on-chip, package-on-package, and external memories are used by all its systems and subsystems, which are discussed in later architecture sections. Therefore, this section is presented first.*

Memory Support Architectural Overview



Memory Support Section Outline



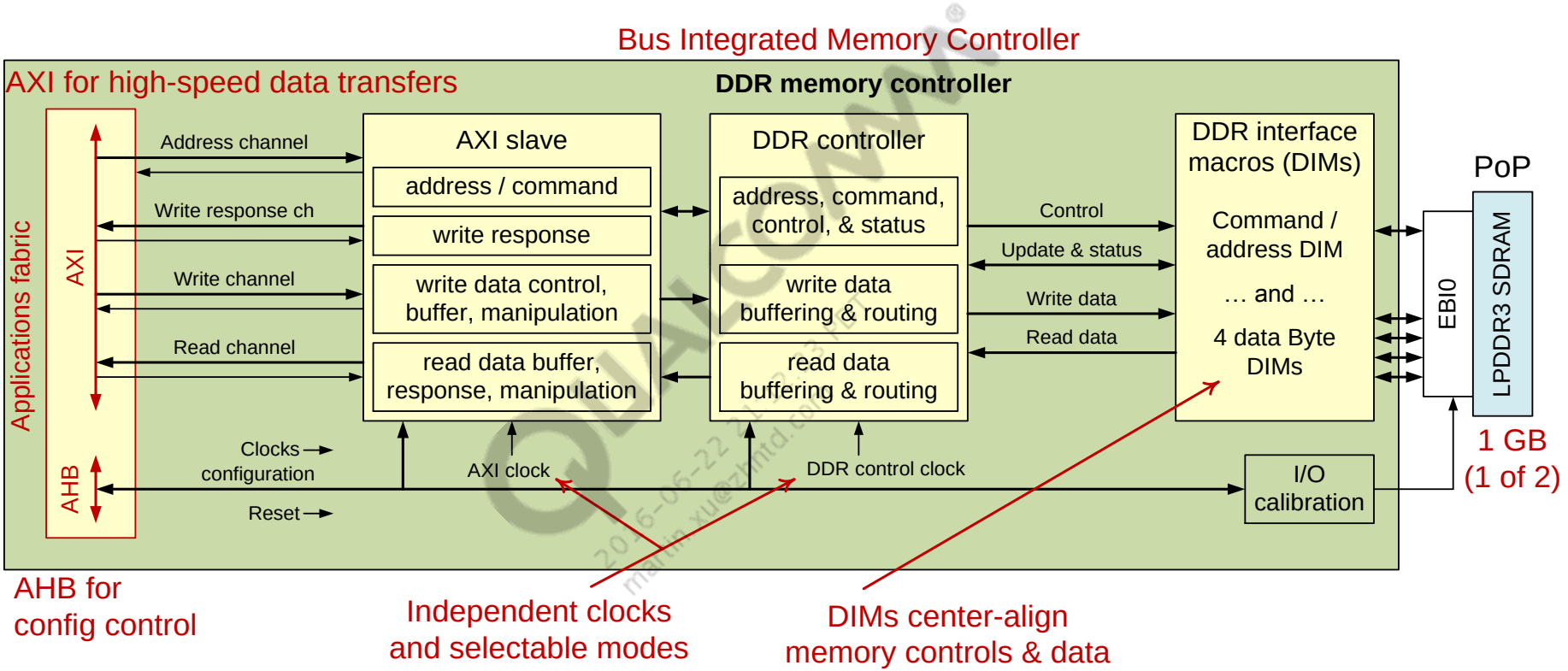
Additional memory support details that follow:

- Supported memory configurations and devices
- System memory map
- DDR memory controller & LPDDR3 (#1 above)
- SDC1 for NAND flash (#2 above)
- SPI for NOR flash (#3 above)
- External memory layout guidelines
- Internal memory (#4 above)

MSM8x74/MSM8974AB Available LPDDR3 PoP Memory

Refer to the *Qualcomm Test Criteria and FAQ for MSM8274/MSM8674/MSM8974 Package-on-Package Memory Application Note* (80-NA437-18)

DDR Memory Controller and LPDDR3



Key DDR Memory Controller Features

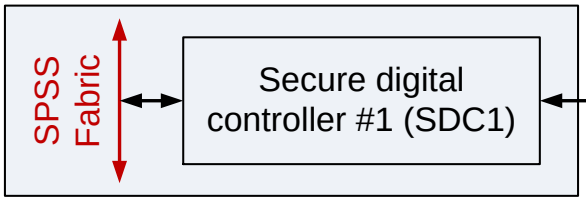
Two major clock domains

- AXI slave (up to 800 MHz)
- DDR controller (up to 800 MHz for MSM8x74 and up to 933 MHz for MSM8x74AB)

Multiple AXI-to-DDR clock modes

- Synchronous (1:1); iso-synchronous (1:2); asynchronous
  - Dual channel EBI1 system memory with 32-bit LPDDR3; support for two ranks
  - Channel interleaving at 1 KB boundary
  - Maximum density at 1 GB LPDDR3 per CS (software can currently only support 3.875 GB total)
  - Flexible memory page management with various page open/close policies
  - Out-of-order command execution and read data return
  - Sequential burst support; no interleave burst support
  - Auto-refresh, temperature adjusted auto-refresh, posted auto-refresh, and self-timed refresh
  - I/O calibration
  - DIMs handle center-aligning of memory controls and data
  - Performance monitors with event outputs to SPDM
  - Powerdown and deep powerdown (DPD) support

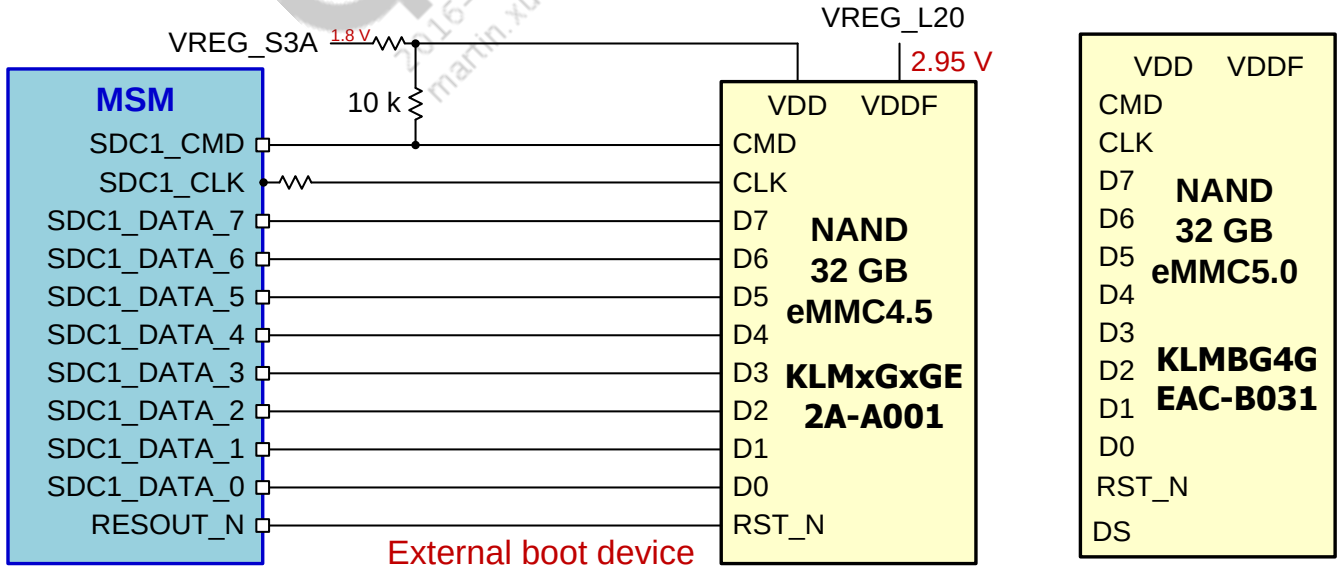
External eMMC NAND Flash on SDC1



See the *Connectivity* section for SDC details.

eMMC is used for boot; see the *Resource and Power Management System* pages.

- Fourth generation SD card controller (SDCC4) for MSM8x74 and SDCC5 for MSM8x74AB
- Supports eMMC v4.51 for MSM8x74 and eMMC5.0 for MSMx74AB
  – eMMC will be tested on QTI evaluation platforms.
- Up to 200 MHz (SDR) and 50 MHz (DDR) clock speeds for MSM8x74 and up to 200MHz (DDR) for MSM8x74AB
  – Only a few controllers support these speeds; see *Connectivity* section for details.
- Internal pull-up resistors can be used if power consumption and BOM count are concerns.
- For MSM8x74AB, pin AT50 (NC pin for MSM8x74) is used with eMMC5.0 device as SDC1_RCLK, connect it to DS pin of eMMC 5.0 devices.

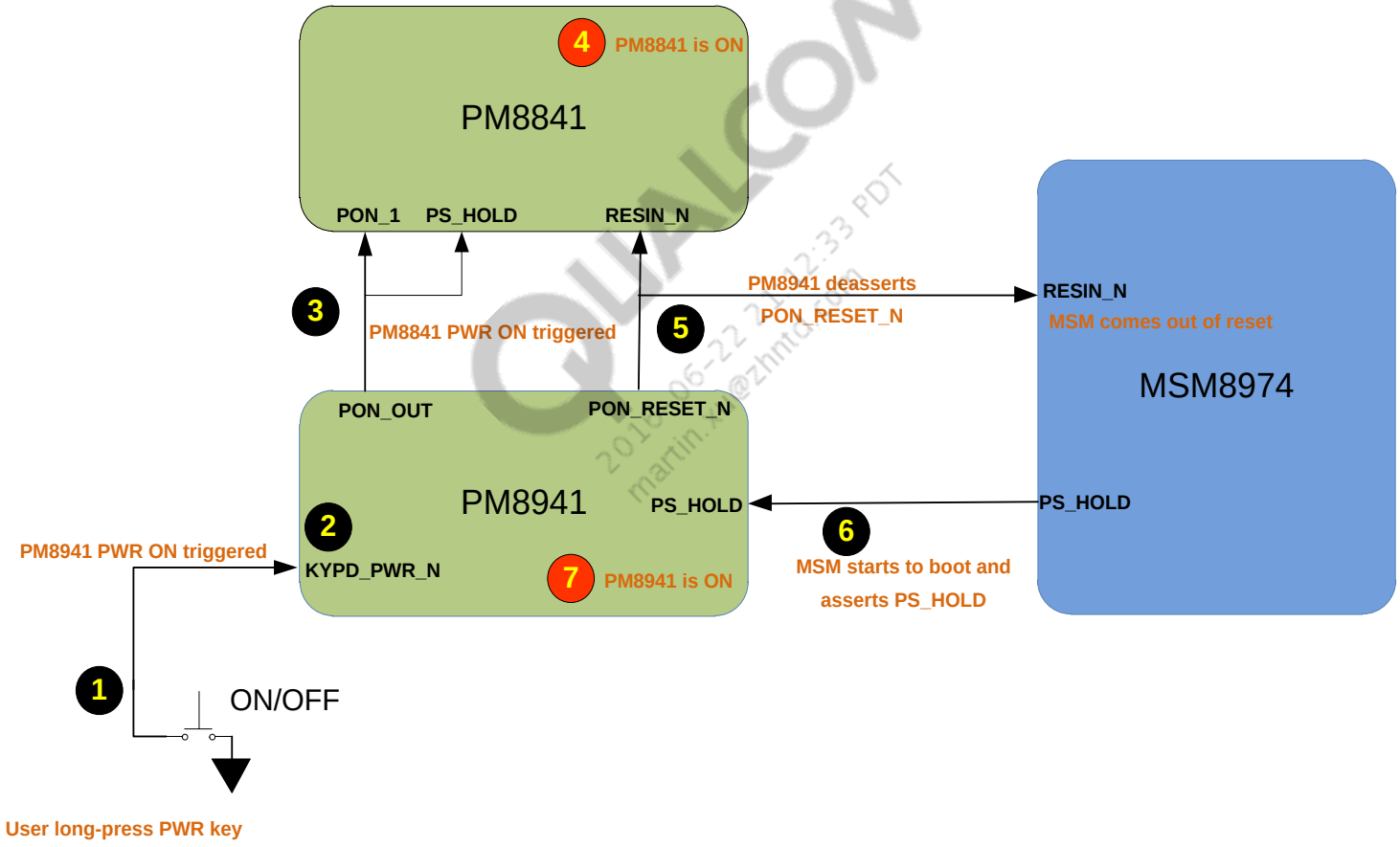


Sec. 4

Power/Reset Sequence

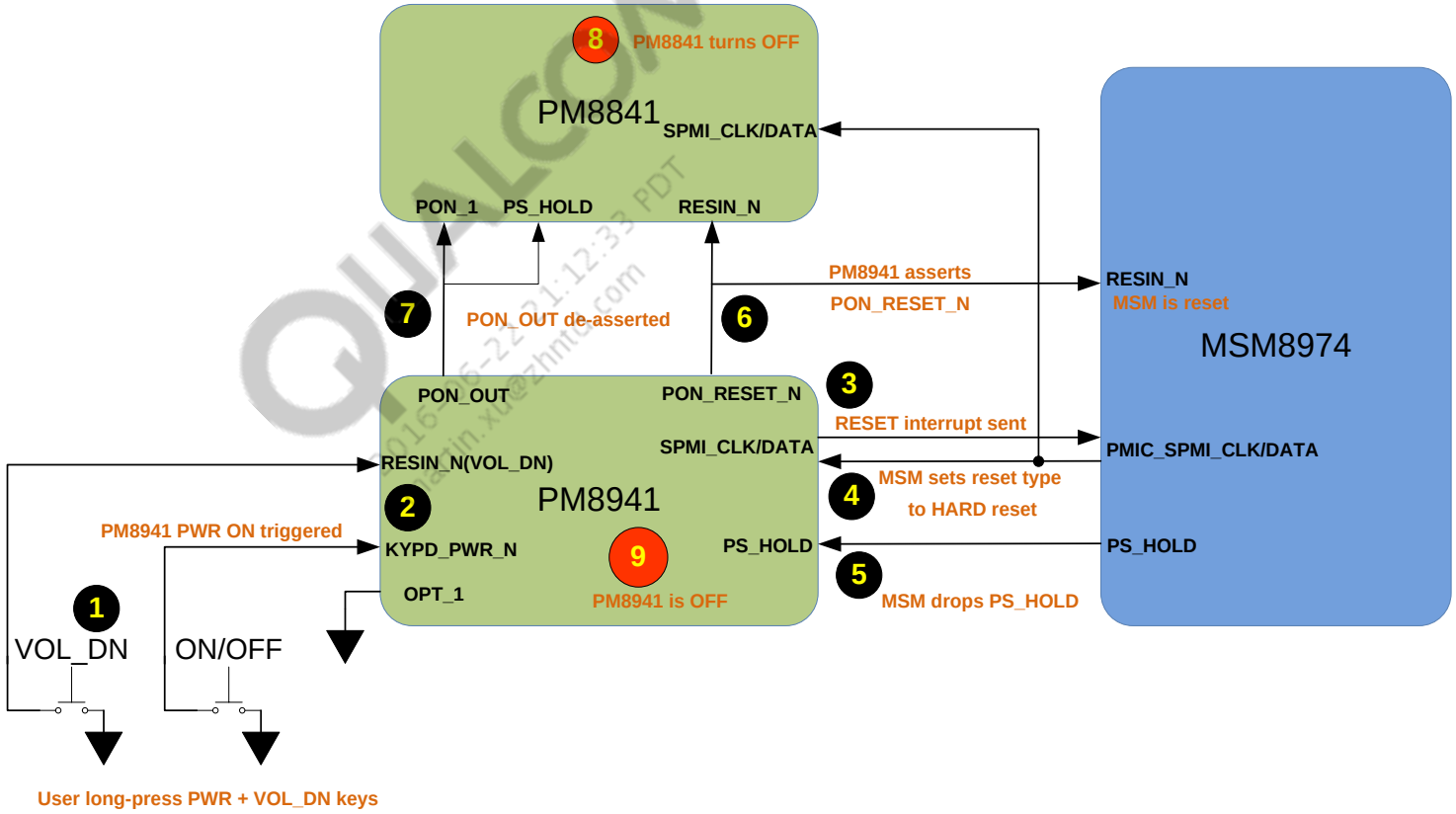
Poweron Sequence

Refer to *PM8841 and PM8941 Power Management Design Guidelines* (80-NA555-5) for more information.



Hard Reset

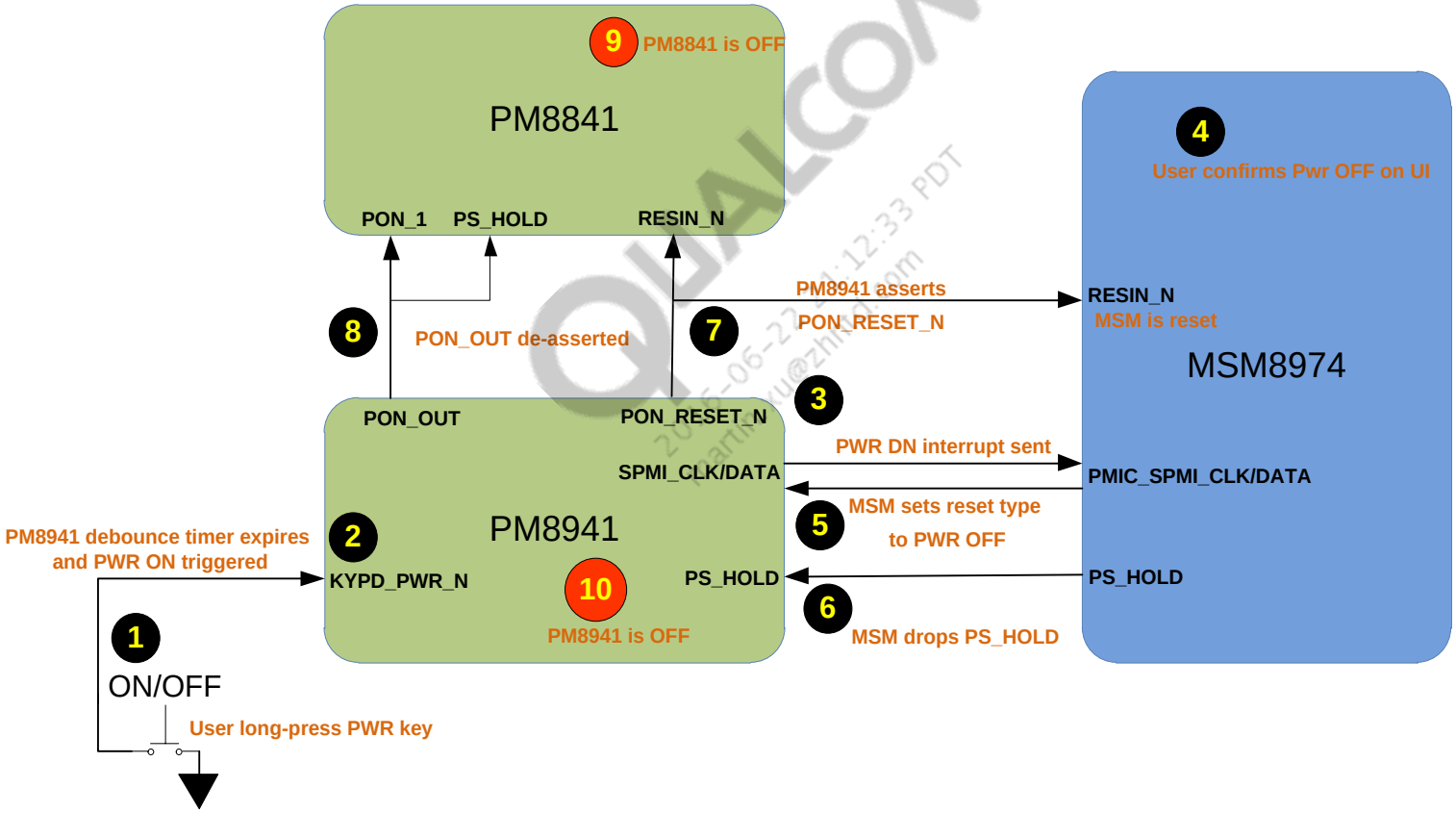
Refer to *PM8841 and PM8941 Power Management Design Guidelines* (80-NA555-5) for more information.



NOTE: If user presses only the VOL_DN key, then RESIN_N on PMIC is used as a GPIO for volume control.

Poweroff Sequence

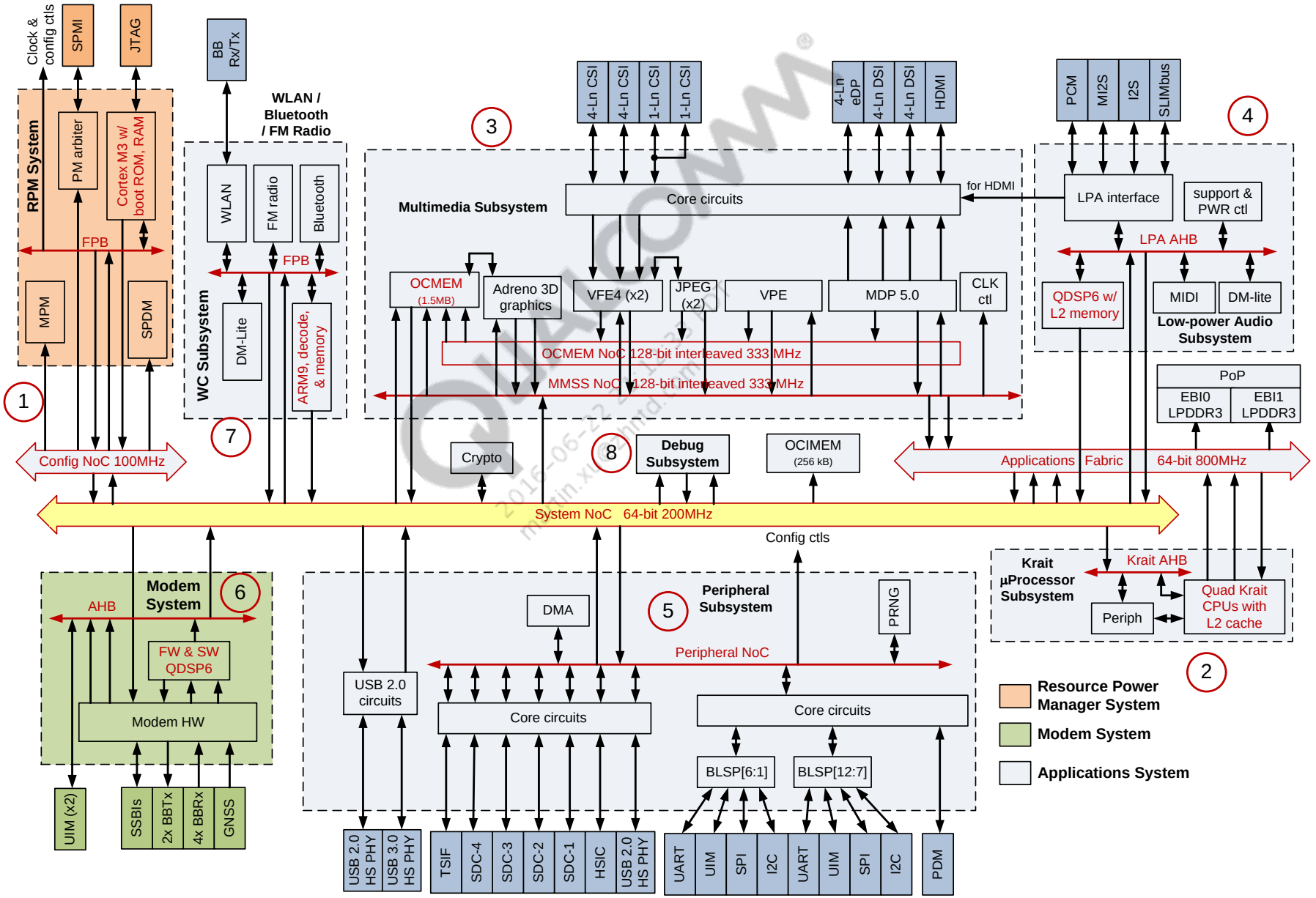
Refer to *PM8841 and PM8941 Power Management Design Guidelines* (80-NA555-5) for more information.



Sec. 5

MSM Architecture

MSM Architecture Overview



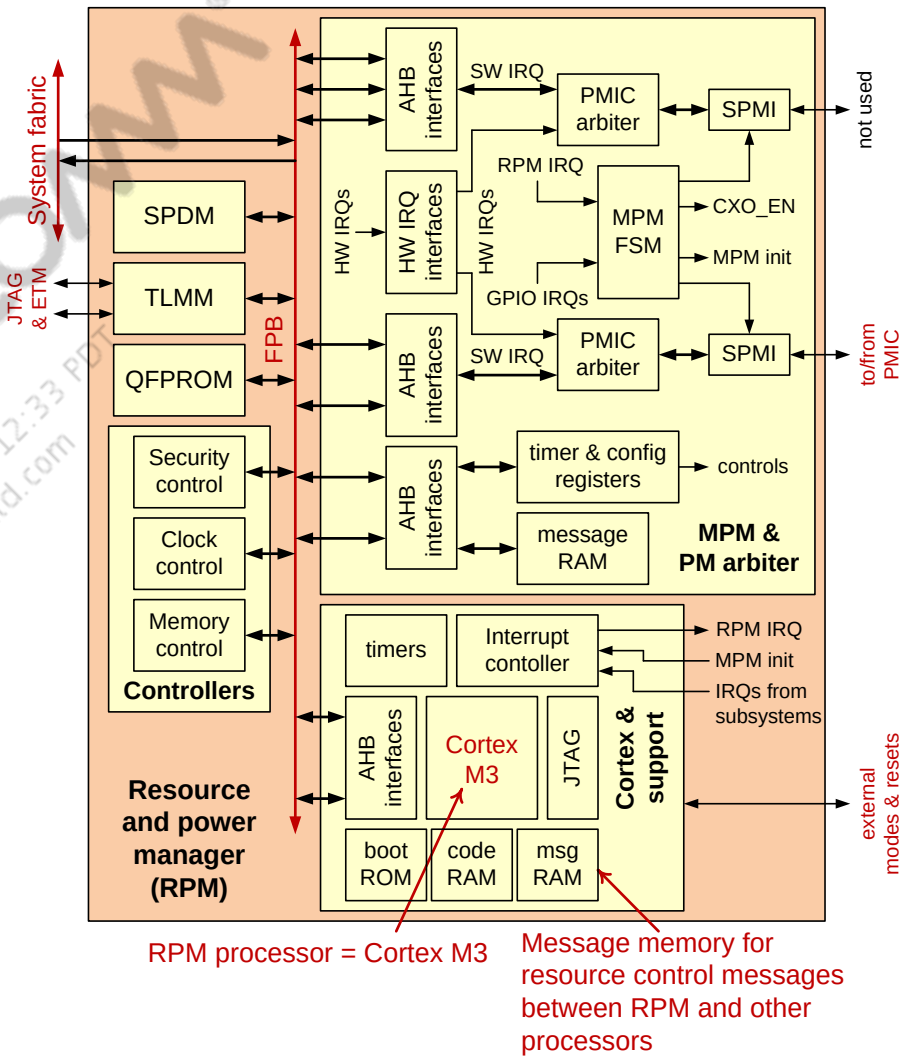
Architecture Topics Outline

- Resource and Power Management System (RPM)
  - Features, modem power management (MPM), security, boot
- Modem System and Air Interfaces Supported
- Applications System
  - Overview
  - Krait Microprocessor Subsystem (KMSS)
  - Multimedia Subsystem (MMSS)
  - Low-power Audio Subsystem (LPASS)
  - Peripheral Subsystem (PSS)
  - Wireless Connectivity Subsystem (WCSS)
  - Debug Subsystem (DSS)
- Bus System – (buses that support the systems and subsystems)
  - Overview, system NoC, applications fabric
- Internal functions that are integral to the MSM architecture
  - Distributed throughout this section

Main RPM objective: lower the IC's average power consumption – static (1) and dynamic (2)

1. Static power management (primarily to limit leakage current):
   - Avoids using the high-powered processor.
   - Executes code exclusively from internal RAM.
   - Enables reduced logic supply.

2. Dynamic power management:
   - Rapidly configures shared system resources and power-level configurations without impacting active processes and workloads.
   - Achieves optimal clock rate and supply voltage settings according to workload.
   - Improves overall system power efficiency, while maintaining quality-of-service.
   - Minimizes overhead and latency needed to make voltage and clock change decisions.



Key RPM Features

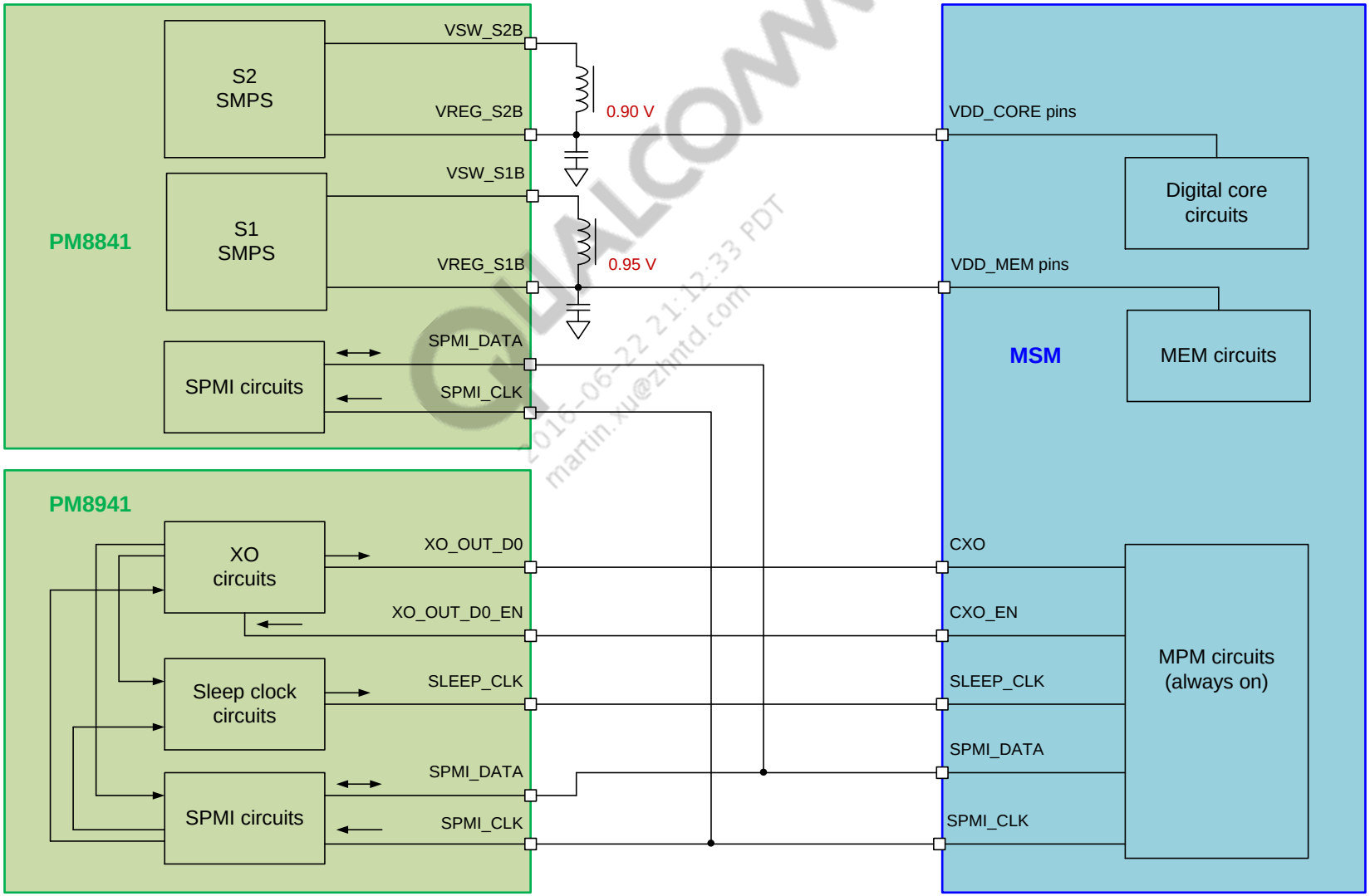
- Fast response times, low latency – less than 1 ms for clock frequency requests, 10 ms for supply voltage requests.
- Autonomous and coordinated controls.
  - Adjusts frequency, voltage, and resource usage without impacting other subsystems.
  - Controls shared resources without other subsystems being active.
  - Supports voting mechanisms for resource management.
- Security – RPM is trusted at all times.
  - Authenticates, validates trust level of subsystems calling RPM.
  - Employs QFPROM.
  - The Krait applications processor is assumed to be the secure root-of-trust (SROT) after initial boot.
- Performs initial boot, coordinates other subsystems' boot-ups.
- Resources controlled include: power management; clock sources and routing (CXO and sleep); supply voltages; clock frequencies; PoP memory; temperature compensation; and elements of the other MSM subsystems.

Power Optimization – Modem Power Management (1 of 2)

- RPM manages active power and resources for MSM, while MPM manages the sleep power for an MSM device.
- The modem power manager (MPM) function allows a sleep mode to help minimize DC power dissipation during long periods of inactivity. This sleep mode's power is reduced by the following:
  - Turn off the clocks to unused blocks.
  - Turn off the non-essential PMIC regulators.
  - Reduce the MSM essential CORE/MEM voltages.
  - Run the system using SLEEP_CLK
  - Maintain the SPMI communication link with the PMIC to enable and disable the XO functions and voltage regulators.
  - Monitor interrupts during sleep.
- The new MPM block for MSM8974 supports three modes.
  - Shut down of XO at the CXO pad of the MSM.
  - Shut down of XO at CXO pad of MSM and also at PMIC output XO_OUT_D0.
  - Lower VDD_CORE, VDD_MEM, in addition to turning OFF the clocks.

Power Optimization – Modem Power Management (2 of 2)

- MSM-to-PMIC connections required for MPM support are shown below.
- Typically VDD_CORE is minimized before VDD_MEM.



Design Guidelines for SPMI (1 of 3)

For additional protection against SPMI switching noise and to provide a way to tune signal integrity according to the specific board properties, the following board-level modifications are required:

- For the MSM8x74 Rev. 2.2 and MSM8x74AB ES 1.0 devices:
  - Add the board-level capacitor to SPMI_DATA
    - 15 pF (±10%) shunt capacitor to GND on the SPMI data (INSTALL) as close as possible to MSM with trace parameters: L ≤ 1.65 nH, R ≤ 70 mΩ
    - Routing order: MSM <=> capacitor <=> PMIC (capacitor placed between MSM and PMIC)
    - Recommended placement of the cap on the SPMI trace without stub
  - SPMI data SEN_EN = 0, SPMI clock SEN_EN = 0
  - PMIC SPMI drive strength setting = 11
- For the MSM8x74 Rev. 2.1 and MSM8x74AB ES 1.1/CS devices:
  - No board-level capacitor to SPMI_DATA
  - SPMI data capacitance (trace + device) 5 pF ≤ C_{T+D} ≤ 20 pF
  - SPMI data SEN_EN = 1, SPMI clock SEN_EN = 0
  - PMIC SPMI drive strength setting = 01
- Use following layout guidelines:
  - SPMI traces **must** be controlled with 50 Ω impedance with 10% tolerance
  - Trace spacing for SPMI_CLK/DATA should be at least three times the trace width from each other, and from other signals; so as to avoid cross-talk
  - The trace length mismatching between the SPMI data and clock should be ≤ 2 mm
  - SPMI data and SPMI clock trace interconnect topology as depicted in the diagram on following page
- Reference:
  - *MSM8274/MSM8274AB, MSM8674/MSM8674AB, and MSM8974/MSM8974AB Baseband Reference Schematic* (80-NA437-41 Rev. M or later)

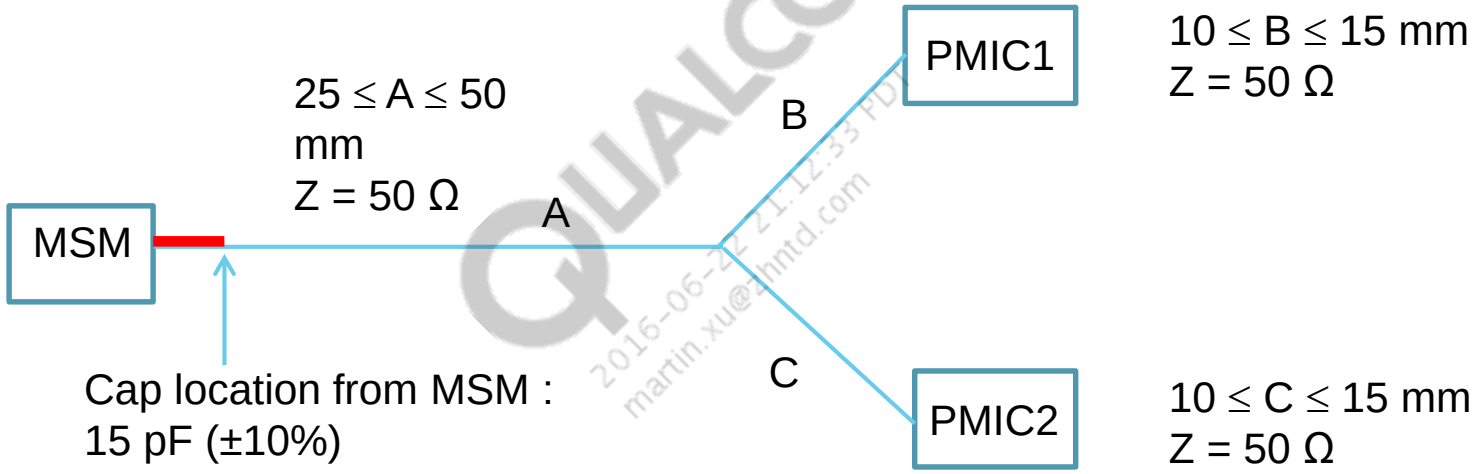
Note: Following the layout guidelines with the board level capacitors is the recommended solution for the SPMI SSC™ false detection.

Design Guidelines for SPMI (2 of 3)

Required Hardware Modification – Suggested Routing and Requirements

For additional protection against SPMI switching noise and to provide a way to tune signal integrity according to the specific board properties, the following board-level modifications are required.

Characteristic impedance of 50 Ω has ±10% of tolerance.



The trace length mismatching between the traces B and C should be ≤ 0.5 mm.

Test points, if required, are recommended to be placed closer to PMICs without stubs on the traces.

Design Guidelines for SPMI (3 of 3)

MSM8x74 version	Default software setting for MSM SPMI_DATA SEN_EN	Software setting for PMIC SPMI drive strength setting	15 pF capacitor on SPMI_DATA
Rev. 2.1	1	01	DNI
Rev. 2.2	DON'T CARE (parameter has no effect on this revision)	11	INSTALL

MSM8x74AB version	Default software setting for MSM SPMI_DATA SEN_EN	Software setting for PMIC SPMI drive strength setting	15 pF capacitor on SPMI_DATA
ES 1.0	DON'T CARE (parameter has no effect on this revision)	11	INSTALL
ES 1.1	1	01	DNI

Note: In order to further mitigate the potential false SSC detection, the use of PMIC interrupts is recommended to be minimized by using MSM interrupts when necessary.

Design Guidelines of XO_OUT_D0

It is strongly recommended to add a termination resistor in series with XO_OUT_D0 close to the PM8941.

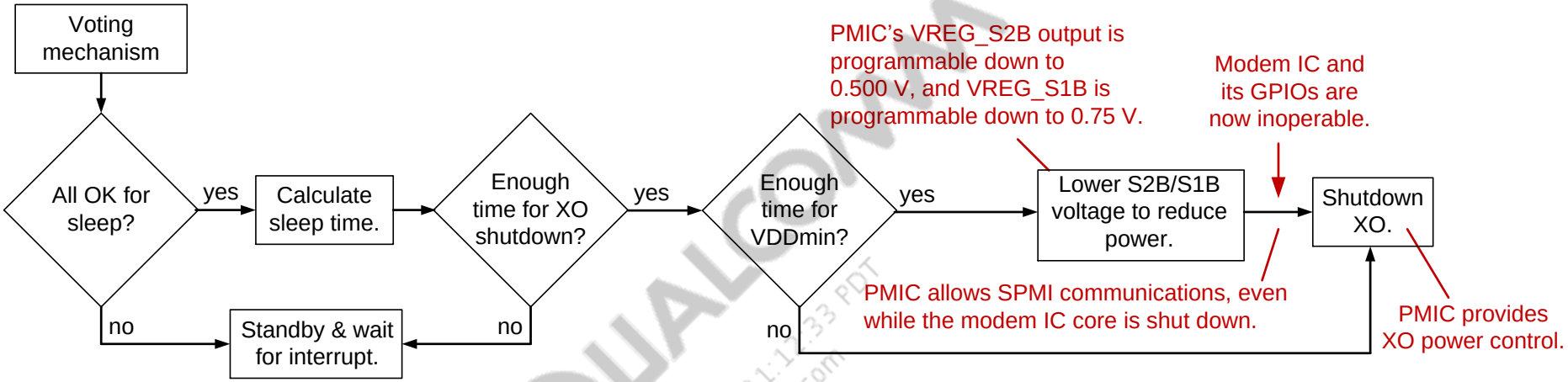
The XO_OUT_D0 trace layout from the PM8941 to the MSM8974 should be optimized. Refer to *Application Note: PM8941 Baseband Clock Layout Guidelines* (80-NA555-14) for more information.

VDD_ALWAYS_ON

The MSM8974 device has a pin AD48 – VDD_ALWAYS_ON.

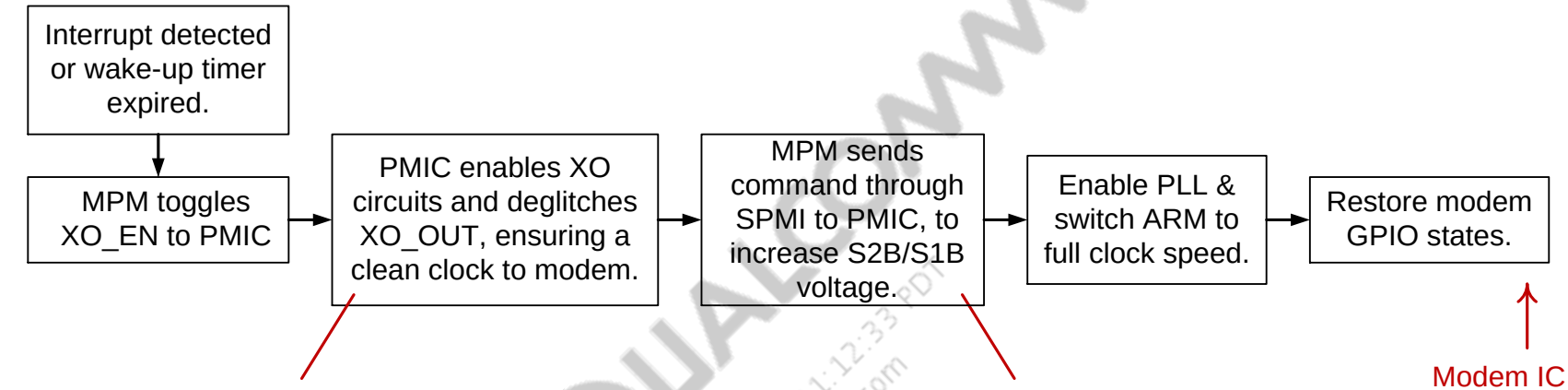
The VDD_ALWAYS_ON of the MSM8974 device is a backup power supply for the internal LDO, which powers the MPM (always ON) block of the MSM8974 device.

Entering MPM Power-Saving Mode



Note: If an interrupt is detected during the entering-shutdown process, it is saved, and the wakeup process starts as soon as the shutdown procedure concludes.

Exiting MPM Power-Saving Mode



Modem ICs cannot tolerate runt pulses; the PM8941 ensures a synchronized and glitch-free XO signal to the MSM device.

Modem GPIOs are not operable yet; the SPMI must be used.

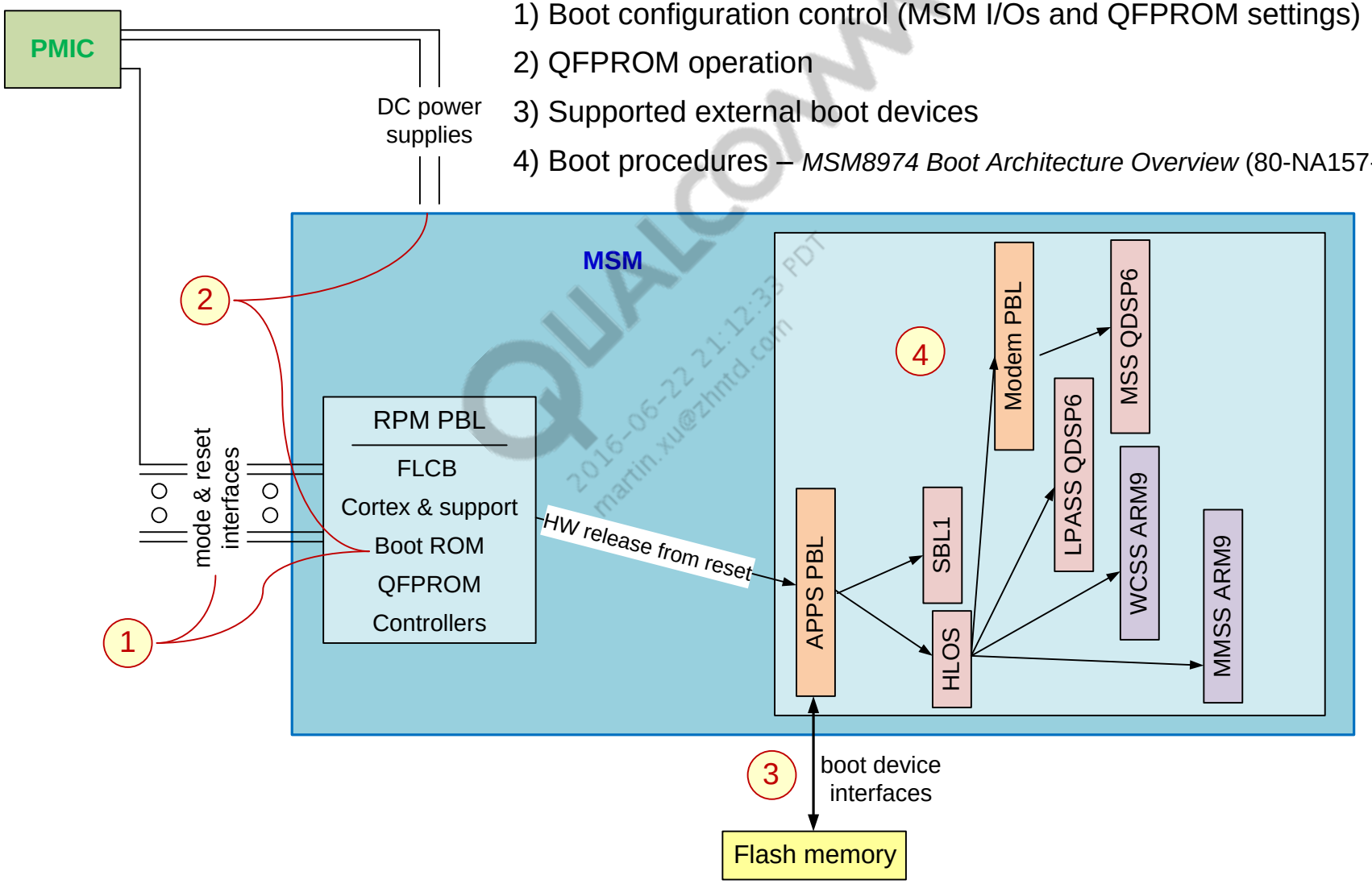
Modem IC and its GPIOs become operable at this point.

Security and Boot Introduction

- As the modem IC is powered up and initialized, it determines what boot-up procedure to execute, and concurrently defines its security conditions.
- This section begins with boot.
  - Boot overview introducing the hardware and firmware components.
  - Design issues that must be decided and implemented before executing boot.
    - Boot configuration control
    - QFPROM overview and programming
    - External boot devices
  - Secure boot.
- Security features.

Boot involves hardware and firmware:

1) Boot configuration control (MSM I/Os and QFPROM settings)
2) QFPROM operation
3) Supported external boot devices
4) Boot procedures – *MSM8974 Boot Architecture Overview* (80-NA157-7)



Secure Boot

- MSM8x74 uses Secure Boot 3.0; see *MSM8974 Boot Architecture Overview* (80-NA157-7) for more details.
- Ensures that QCT code and OEM code cannot be modified by another entity.
- Two types of secure boot configurations – application based boot segments and modem based boot segments.
- Gains control of system immediately after reset – RPM/apps code within its boot ROM.
- RPM/apps code creates root of trust:
  - Responsible for validating that code image.
  - Responsible for validating boot code stored in external memory.
  - Confirms that the code originated from a trusted authority (authenticity).
  - Verifies that the code is in its original form (integrity).
  - Digital signatures validate external code image and establish system security level.
  - Verifies code image version (compares signed version label to value in Qfuses).
  - Version control ensures an old revoked code image is unusable.
- Efficient and flexible handling of multiple processors and multiple execution environments (EEs):
  - Boot includes multiple authentication stages, where each stage is responsible for authenticating the following boot stage.
- Refer to the *MSM8274/MSM8674/MSM8974/APQ8074 QFPROM Programming Reference Spreadsheet* (80-NA437-97) for more details.
- Verisign code signing service:
  - Hash for public keys stored in external flash resides in the on-chip boot ROM.
  - Secure because public keys can be checked against hash values before use, and hash values are unalterable to an attacker.
  - OEM provides up to 256-bit hash for their public keys.

Boot Configuration (1 of 2)

There are two types of Boot related fuses.

- **Fast Boot Fuses** - These fuses are used by the boot code to determine which device the chip should be booting from.
- **Secure Boot Fuses** - In order to ensure that the code running on Qualcomm Technologies, Inc. (QTI) chips is from a trusted source, encryption is used. There are fuses for up to 28 different code authentication schemes. The software registers that hold the read-only settings for these schemes are named SECURE_BOOT1 through SECURE_BOOT28.

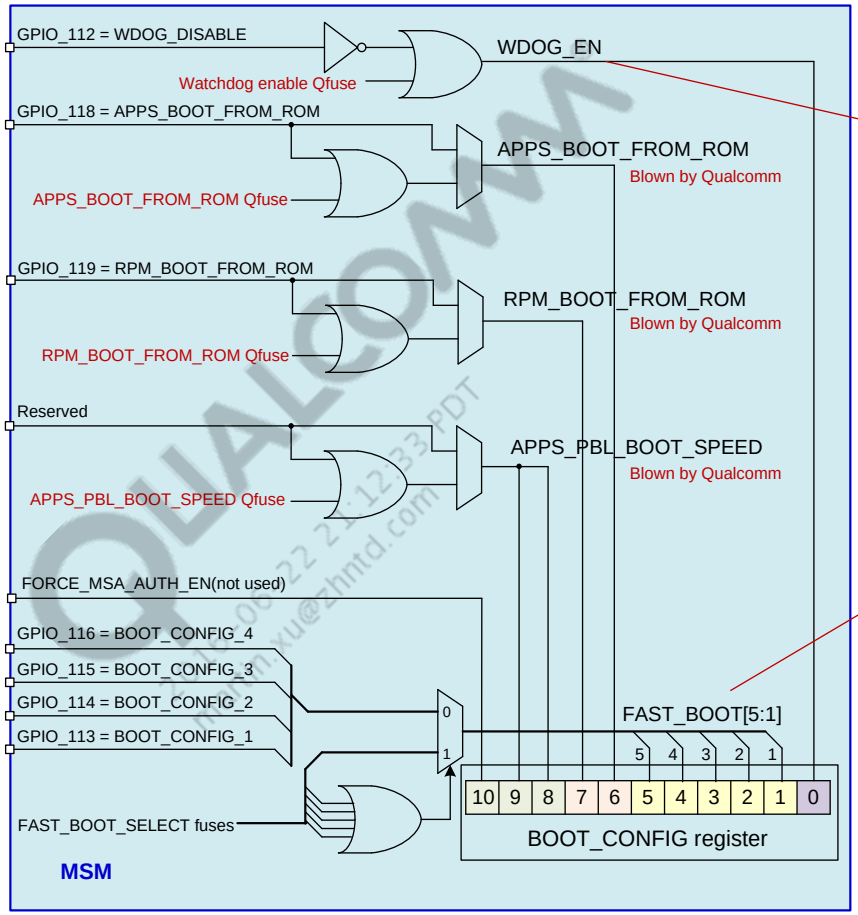
Important considerations for secure boot:

1. There are two types of secure boot configurations – an applications PBL boot ROM and a modem boot ROM. Secure boot region 1 is for apps boot and secure boot regions 2 and 3 are for modem boot.
2. There are a total of 28 secure boot spaces. 4-28 are not used in this design. OEMs can use any of these unused secure boot spaces to authenticate some new piece of code or some existing boot image. However, it is the OEMs responsibility to develop and validate the SW.
3. FAST_BOOT_SELECT fuses are located in the QFPROM rows "SECURITY_CONTROL_CORE_QFPROM_RAW_OEM_CONFIG_ROW0_LSB" and SECURITY_CONTROL_CORE_QFPROM_CORR_ OEM_CONFIG_ROW0_LSB".

Refer to *MSM8274/MSM8674/MSM8974/APQ8074 Software Interface for OEMs* (80-NA437-2) for more details.

Boot Configuration (2 of 2)

- BOOT_CONFIG[4:1] is MSB-aligned with FAST_BOOT[4:1]. FAST_BOOT[5] is not used.
- Both secure boot and fast boot can be configured by fuses or BOOT_CONFIG pins.
- Provides flexibility in the development phase.
- QTI recommends that fuses be blown for production devices.
- The tables on the next two pages provide details.



Enable/disable watchdog timer
- Watchdog enable Qfuse = 1
  → Watchdog timer enabled
- Watchdog enable Qfuse = 0
  → Allow GPIO_112 to control
  – 0 = enable
  – 1 = disable

eMMC boot is the default boot option

Selects external boot device	
FAST_BOOT	Boot device / comments
0x0	**SDC1 followed by SDC2**
0x1	SDC2 followed by SDC1
0x2	SDC1
0x3	HS USB

Secure-Boot Mapping Table

Boot segment	Feature	GPIOs	Function
Apps boot segment (region 1)	AP_AUTH_EN	GPIO[131]	Selects authentication enable for apps segments.
	AP_PK_HASH_IN_FUSE	GPIO[130]	Selects the public key hash from fuse for apps boot segment.
MSA boot segment (region 2 and 3)	MSA_AUTH_EN	GPIO[127]	Selects authentication enable for MSA segments.
	MSA_PK_HASH_IN_FUSE	GPIO[126]	Selects the public key hash from fuses for MSA boot segment.
Common to both MSA and Apps boot segment	PK_HASH_INDEX_SRC	GPIO[122]	Selects public key hash index source.
	ALL_USE_SERIAL_NUMBER	GPIO[123]	Selects the SERIAL_NUMBER.

Note: Make sure there are no external pulls on these GPIOs if secure boot is not required, since the external pulls can force the MSM to enter secure boot.

Fast-Boot Mapping Table

GPIOs	Corresponding fuse	Function	Description
GPIO[113]	FAST_BOOT[1]	BOOT_CONFIG[1]	The fast boot options configure the external boot device used to boot from, as shown in the table below. Development board - BOOT_CONFIG GPIOs should be used Production board - FAST_BOOT fuses should be blown
GPIO[114]	FAST_BOOT[2]	BOOT_CONFIG[2]	
GPIO[115]	FAST_BOOT[3]	BOOT_CONFIG[3]	
GPIO[116]	FAST_BOOT[4]	BOOT_CONFIG[4]	

BOOT_CONFIG[4:1]	Boot device
0b00000	eMMC (default) at SDC1, followed by USB from SDC2
0b00001	SDC2 followed by SDC1
0b00010	eMMC at SDC1
0b00011	USB

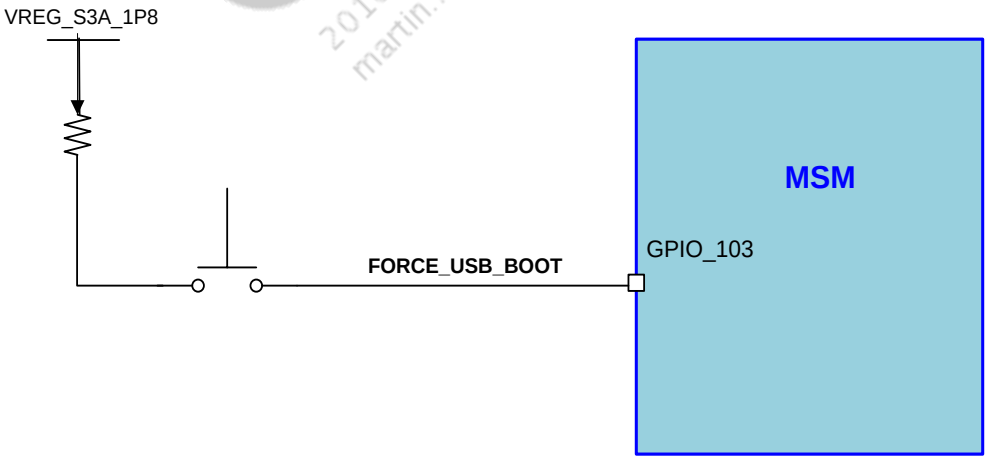
Force USB Boot

During development or factory production, boot from USB_HS1 port can be forced by using GPIO_103.

Irrespective of the state of the BOOT_CONFIG GPIOs or FAST_BOOT_SEL fuses, FORCE_USB_BOOT always takes precedence.

FORCE_USB_BOOT (GPIO_103) is checked first during the boot device detection prior to BOOT_CONFIG GPIOs.

- GPIO_103 = 1 will force the MSM to boot from USB_HS1 port.
- The fuse FORCE_USB_BOOT_DISABLE can be blown to disable the feature to force USB boot using GPIO_103.

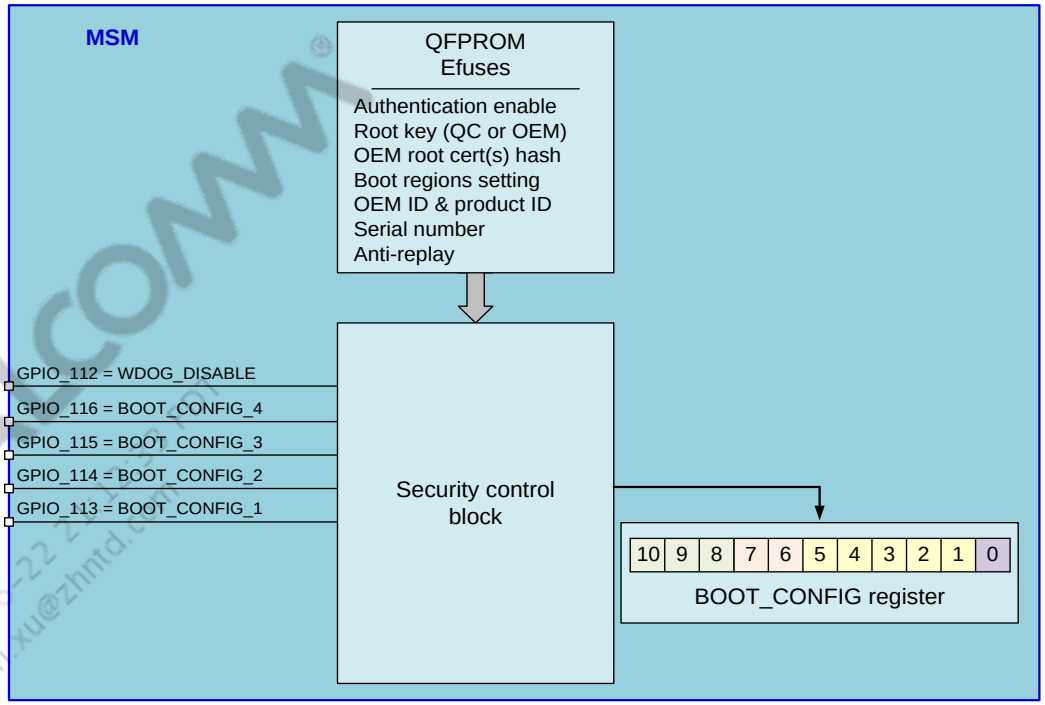


Boot Configuration Control

Special boot-related GPIO features:

- They are sensed for boot-purposes during IC reset (during fuse sense).
- For normal GPIO use, they are always configured as outputs.
- After boot, they can be used for normal GPIO functions.

For details on the boot configuration options, refer to the previous slides.



QFPROM Overview

QFPROM = Qualcomm fuse programmable read-only memory

- MSM8x74 is part of HPm technology node family of devices, and uses metal fuses.
- 2-dimensional array of fuses that is like a memory in structure and function.
- Capacity of at least 16 K fuses, with additional 4 K hidden rows for redundancy in 28 nm HPm design.
- There are two QFPROM instances, each having 128 rows of 64 bits. Total of 16 K.
- New shadow redundancy scheme introduced, in addition to FEC (forward error correction) method.
  - Shadow redundancy provides additional security for the fuses, over the life-time of a chip.
  - FEC is optional in regions where shadow redundancy is not available.
  - 63/56 FEC scheme is used. FEC values are auto calculated in the *MSM8274/MSM8674/MSM8974/APQ8074 QFPROM Programming Reference Spreadsheet* (80-NA437-97).
  - The last page of 80-NA437-97 provides the algorithm to calculate FEC for reference.
  - FEC_EN should be blown last, after all the other bits are blown.

Access to QFPROM data bits

- Bits that control hardware features are sensed at powerup:
  - Sent to registers so that they can drive the desired circuits.
  - Available in registers for software reads.
- Other bits are not sensed at powerup, and are not stored in registers:
  - Software requests result in reads directly from the QFPROM itself.
  - Memory protection (similar to XPU) ensures that only trusted masters can access (read or write) certain QFPROM locations.

QFPROM Fuse Map

The entire QFPROM region map is given in the *MSM8274/MSM8674/MSM8974/APQ8074 QFPROM Programming Reference Spreadsheet* (80-NA437-97).

QFPROM Region Map

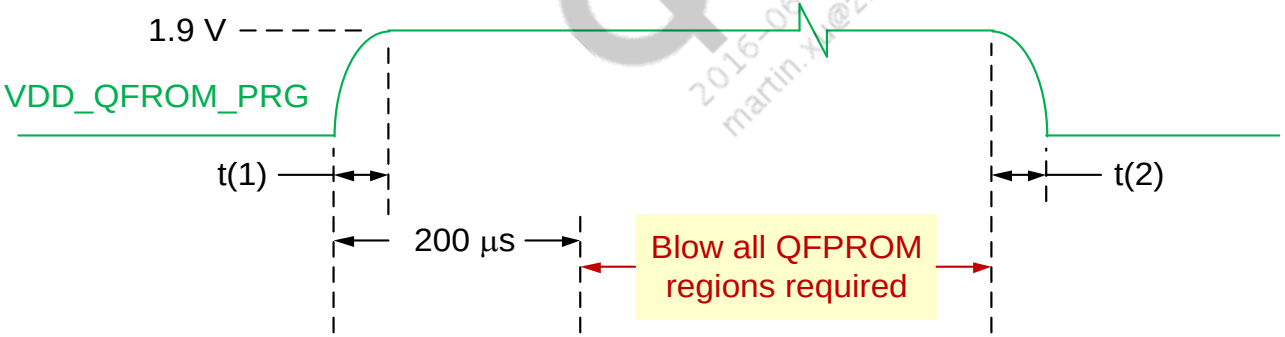
Row	63	62 61 60 59 58 57 56	55 54 53 52 51 50 49 48	47 46 45 44 43 42 41 40	39 38 37 36 35 34 33 32	31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0
255	0	FEC	UNUSED			Customer Private Key1 [2047:2016]
254	0	FEC	Customer Private Key1 [2015:1960]			
253	0	FEC	Customer Private Key1 [1959:1904]			
...	...					
221	0	FEC	Customer Private Key1 [167:112]			
220	0	FEC	Customer Private Key1 [111:56]			
219	0	FEC	Customer Private Key1 [55:0]			
218	0	FEC	UNUSED			Customer Private Key0 [2047:2016]
217	0	FEC	Customer Private Key0 [2015:1960]			
216	0	FEC	Customer Private Key0 [1959:1904]			
...	...					
184	0	FEC	Customer Private Key0 [167:112]			
183	0	FEC	Customer Private Key0 [111:56]			
182	0	FEC	Customer Private Key0 [55:0]			
181	0	FEC	Reserved			
180	0	FEC	Reserved			
179	0	FEC	Reserved			
...	...					
144	0	FEC	Reserved			
143	0	FEC	Reserved			
142	0	FEC	Reserved			
141	0	FEC	UNUSED		KSV [39:0]	
140	RESERVED					
139	RESERVED					
138	RESERVED					
137	RESERVED					
136	RESERVED					
135	0	FEC	UNUSED	USB VID/PID [47:0]		
134	0	FEC	Reserved			
133	0	FEC	Reserved			
132	0	FEC	Reserved			
131	0	FEC	Reserved			
130	0	FEC	OEM Secure Boot [223:168]			
129	0	FEC	OEM Secure Boot [167:112]			
128	0	FEC	OEM Secure Boot [111:56]			
127	0	FEC	OEM Secure Boot [55:0]			

QFPROM Programming

- The VDD_QFPROM_PRG pin of MSM device MUST be connected to a VREG_L12 (1.9 V) of PM8941. See *MSM8274/MSM8274AB, MSM8674/MSM8674AB, and MSM8974/MSM8974AB Baseband Reference Schematic* (80-NA437-41) for details.
  - The MSM8974 uses a new QFPROM architecture, which supports using a shared power supply for VDD_QFPROM_PRG.
- Typical value of current required to blow a fuse is 39.4 mA.
- Typical time required to blow a fuse is 12 µs.

Note: When a QTI API is used to blow fuses, the above current and timing requirements are taken care of.

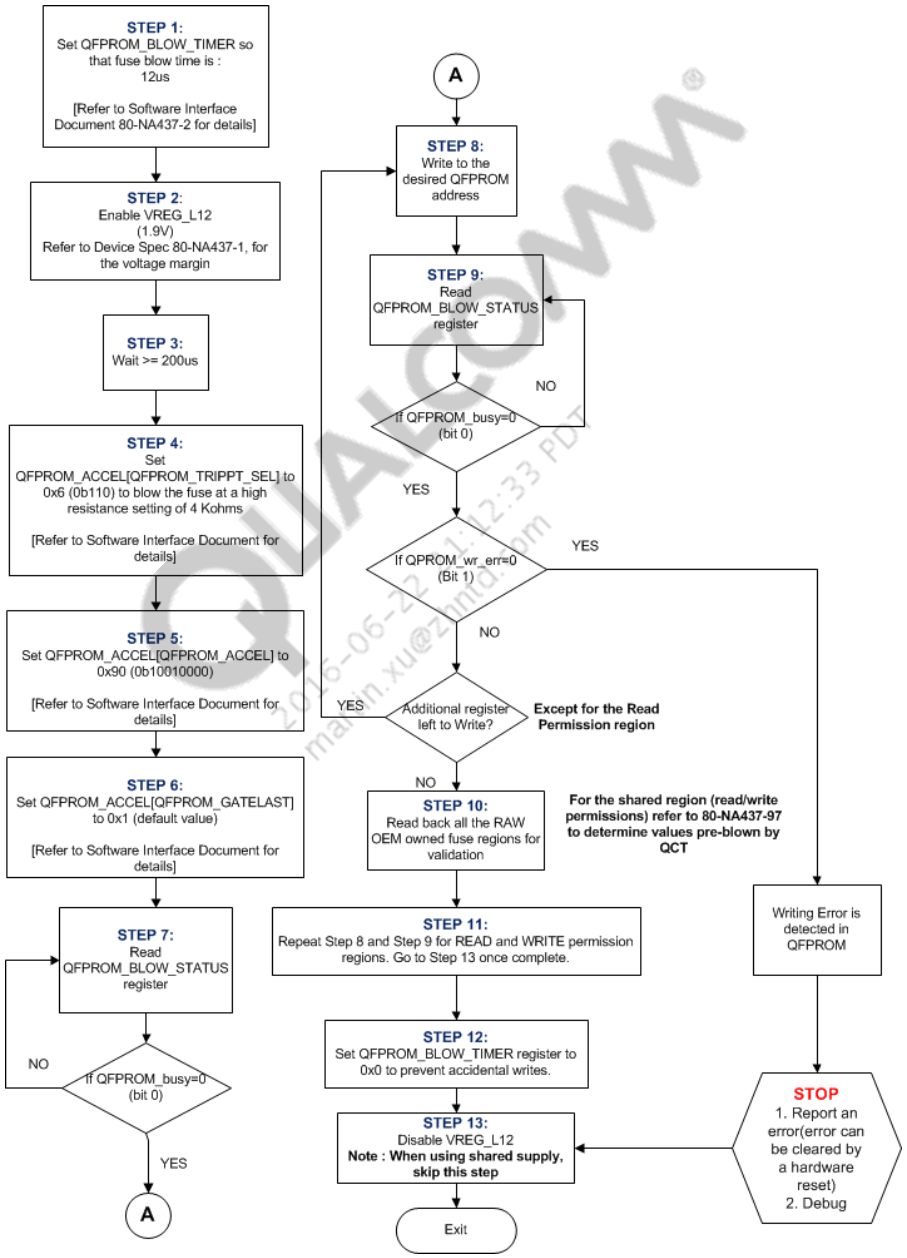
- Fuses must be blown at room temperature (within 25 °C–85 °C).
- The required power sequence for QFPROM programming is shown below.



t(1)=rise time; t(2)=fall time

Note: Refer to the PM8941 training slides for timing details.

QFPROM Programming PON sequence



Summary of Important QFPROM Keys

Primary key derivation key (256-bit)

- Modem SFS encryption/decryption
- Uniquely provisioned by QTI before shipping, including the read permission bit
- Cannot be read by software directly
- Only usable by CE3 at secure software launch

Secondary key derivation key function (256-bit)

- Applications SFS encryption/decryption
- Provisioned by OEM; can be configured as un-readable, by blowing the read permission bit
- Routed through hardware to HLOS crypto core (CE1 and CE2)
- Can be read after secure processor's invasive debugs (JTAG_DISABLE) have been disabled

Customer private key (general-purpose 2048-bit for use by OEMs or carriers)

- Provisioned by the customer
- Can be read after secure processor's invasive debugs (JTAG_DISABLE) have been disabled
- Software protections rely on trusted master handling boot configurations of XPUs

Customer key (256-bit) FEC 63/56 format

- General-purpose key for customers
- Can be read after secure processor's invasive debugs (JTAG_DISABLE) have been disabled
- Software protections rely on trusted master handling boot configurations of XPUs

OEM PK hash (256-bit) FEC 63/56 format

- OEM public key hash is stored in this region
- Used for encryption of the OEM downloadable image

For JTAG_DISABLE fuses, refer to the following slides: *Secure Debug* and *Debug Fuses that Must be Blown for End-to-End Secure Solution*

Summary of Important QFPROM Regions

1. OEM Secure Boot
   - OEM controlled secure boot setting
   - Refer to slide 48, secure boot mapping table
2. OEM configuration
   - Stores the different OEM controlled configuration fuses
3. USB VID/PID
   - Stores the USB Vendor ID and Product ID
4. Read Permissions
   - Used to control reading from each region by region read permissions
5. Write Permissions
   - Used to control any further write to each region by region write permissions
6. FEC Enables
   - All the Forward Error correction enable bits for all regions are stored in this one location. The enable bit should be blown at the end, after all the bits for that region where FEC is enabled are blown
7. OEM PK Hash
   - Stores the Public key hash of the OEM, in fuses
8. Serial Number
   - Stores the Serial number of the chip. Read only for OEM, already blown by QTI before shipping

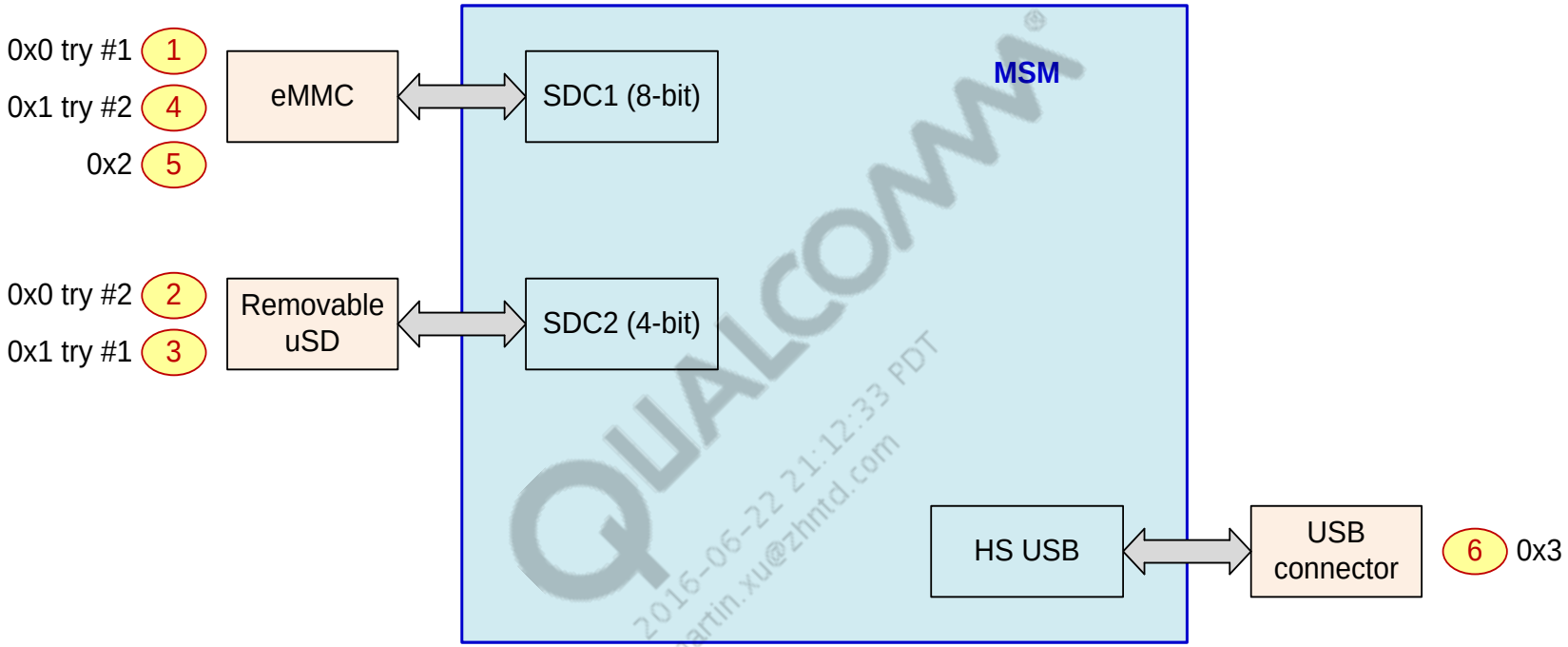
New Qfuses Introduced in MSM8974

SDP_ENUM_SKIP fuse and its function

- In MSM8974, there is a new fuse in the OEM Config region, called SDP_ENUM_SKIP fuse. This is an optional fuse, and OEMs who want to use a non-standard USB charger solution, can blow this fuse and will be able to boot up using the non-standard charger.
- When any non-standard USB charger is used (i.e., USB wall chargers that have D+ and D- open), it gets detected as SDP (standard downstream port) or in other words as USB PC, thereby causing Primary Boot Loader to initiate an enumeration. Since this is a non-standard charger, the enumeration will not happen and the PBL waits for 90 seconds here before proceeding to charge the device with 100mA (PMIC hardware ATC).
- By blowing the SDP_ENUM_SKIP fuse, the OEM can bypass this enumeration step for all USB charger types and immediately proceed to boot up. However, once this fuse is blown, the USB compliance requirements will NOT be met anymore.

Note: Refer to the *MSM8274/MSM8674/MSM8974/APQ8074 QFPROM Programming Reference Spreadsheet* (80-NA437-97) for all of the Qfuse bit details.

External Boot Devices



FAST_BOOT	Boot device / comments
0x00	Default boot – SDC1 (1) then SDC2 (2)
0x01	SDC2 (3) then SDC1 (4)
0x02	SDC1 (5)
0x03	HS USB (6)

Cryptographic Accelerators and Pseudo Random Number Generators

Cryptographic Accelerators

- The MSM8974 IC security subsystem incorporates 3 Crypto5 cores, also known as crypto engines (CE), for use as cryptographic accelerators. Two general purpose CE for secure operations and one dedicated crypto inside modem subsystem.
- Primary HW key to each CE engine is random and unique when the device is in non secure state. This key is blown by QTI before shipping.
- Primary HW key to each CE engine is random and unique when the device is in secure state, and this has to be different comparing to the key in the non-secure state. This key is blown by QTI before shipping.
- Secondary HW key to each CE engine is derived from secondary key derivation key in fuses when the device is in non-secure state.
- Secondary key derivation key in fuses is wired directly to CE instances when the design is in secure mode.
- Identical constant key shall be used for debug for all CE instances when the device is under debug, including OEM debug and QC debug.

Pseudo Random Number Generators (PRNGs)

- MSM8974 uses a pseudo random number generator.
- The PRNG core generates cryptographic random numbers through the use of multiple LFSRs using a non-deterministic ring oscillator as its input.

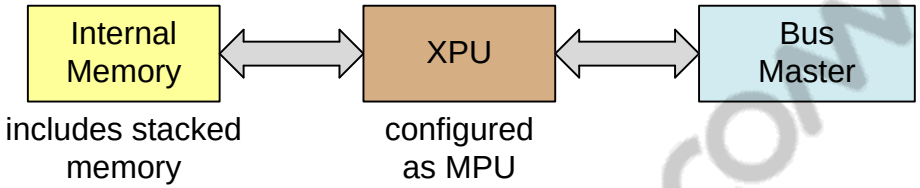
Embedded Memory Protection Unit (XPU)

- The xPU2 is a combination of multiple security blocks known as "Protection Units". In particular, the xPU2 combines the functionality of a Memory Protection Unit (MPU), a Register Protection Unit (RPU), and an Address Protection Unit (APU). Its function is to conditionally grant access by a master, or group of masters, to a set of resource groups based on a security attribute of the master and a set of programmable access control registers (ACRs).

- A resource group is defined as a software defined area of memory (in the case of a MPU), a pre-decoded address region (in the case of an APU), or a resource/register(s) (in the case of a RPU). If access to the resource group is denied, the xPU2 optionally asserts an error output signal and/or an interrupt request signal.

Internal Memory and External DDR Memory Protection

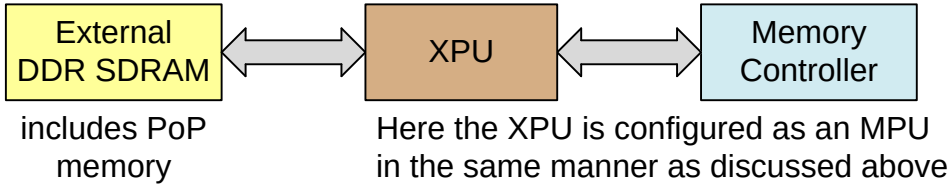
Internal Memory Protection



Bus master types include:
- Processors
- Data movers
- Bus access managers

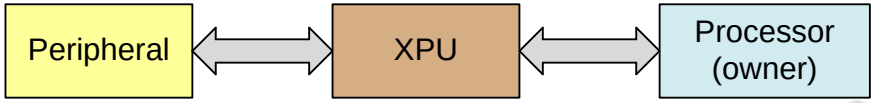
- Each bus master is assigned a unique ID by the bus arbiter
- Master IDs and sub-master IDs are mapped into a security identifier called the virtual master ID (VMID)
- The XPU uses VMID to enforce permissions
- Each intelligent master – each processor – is assigned at least one VMID
- The secure side of the Krait processor is the secure root of trust
  – Its APROTNS bit is used by the VMID mapper to generate unique VMIDs for secure and non-secure operations
- The RPM ARM7 is also considered a secure entity and may have many of the same rights as the Krait TrustZone software

External DDR Memory Protection



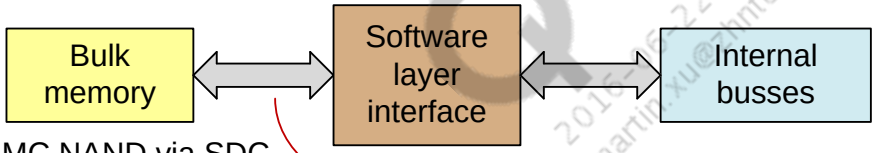
External Bulk Memory, Peripherals and GPIO Protection

Peripheral Protection



- Although it's not a requirement, peripherals are usually "owned" by a single processor
- Corresponding XPUs are configured to allow "single-VMID" access permissions
  - A single VMID is configured so that it is able to write to the peripheral
  - Another single VMID is configured so that it is able to read from the peripheral
- When a single peripheral is accessed by multiple masters, those masters must coordinate with each other to avoid contention

External Bulk Memory Protection

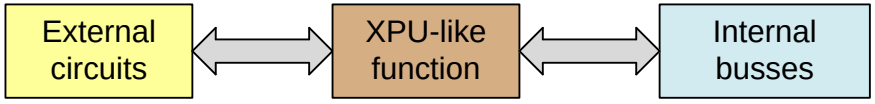


- eMMC NAND via SDC
- NOR via SPI
- etcetera

- Direct access is not allowed
- A software layer interface is required

- If external bulk memory is to be used by trusted and non-trusted execution environments (EEs), then partitioning is needed that keeps the trusted EE from the storage device and from the non-trusted EE
- This partitioning is provided by secure software running within the trusted EE

GPIO/TLMM Protection



- A function similar to an XPU protects GPIOs from non-secure software
- Unique GPIO requirements will not allow standard XPU protection (for example: banked registers used for fast power collapse and restore)

Data Encryption and Power Protection

This will be added to a future revision of this document.

Secure Debug

The following debug functions can be independently disabled via Qfuses. Refer to *MSM8274/MSM8674/MSM8974/APQ8074 QFPROM Programming Reference Spreadsheet* (80-NA437-97) for details on the DEBUG_DISABLE fuses.

- RPM ARM7 debug modem
- Krait, secure, invasive debug
- Krait, non-secure, invasive debug
- MSS Secure and non-secure invasive debug
- DAP (Debug Access Port) debug

- Each debug function can be disabled by Qfuses in both the QCOM configuration area within the QFPROM and its OEM configuration area.
- Qfuses within the QCOM area are given priority.
  - If QTI disables a debug, an OEM cannot re-enable that debug port.
- **It is strongly recommended that the ALL_DEBUG_DISABLE fuse is not blown – this permanently disables all debug capability and makes RMA impossible**.
- If an OEM disables a debug, that OEM may be able to re-enable that debug port using one-time writable debug override registers.
  - If the TrustZone image is signed with debug enabled, TrustZone re-enables JTAG debug by writing 1's to the override registers.
  - If the TrustZone image is signed with debug disabled, TrustZone does not re-enable JTAG debug – it writes0s to the override registers.

See the *MSM8274/MSM8674/MSM8974/APQ8074 Software Interface for OEMs* (80-NA437-2) for override register details.

Debug Fuses that Must be Blown for End-to-End Secure Solution

To enable an end to end secure solution in MSM8974, the following processor debug disable fuses must be blown by the OEM.

- DAP_DEVICEEN_DISABLE
- APPS_SPIDEN_DISABLE
- APPS_SPNIDEN_DISABLE
- DAP_SPIDEN_DISABLE
- DAP_SPNIDEN_DISABLE
- MSS_DBGEN_DISABLE
- MSS_NIDEN_DISABLE
- RPM_DAPEN_DISABLE
- RPM_DBGEN_DISABLE
- LPASS_DBGEN_DISABLE
- WCSS_DBGEN_DISABLE
- VENUS_0_DBGEN_DISABLE

Once the HW keys are programmed by the OEM, the write permission for the Secondary Key Derivation Key should also be blown to protect any further writes. The Primary Key Derivation Key is programmed by QTI including the read/write permissions as well.

Trusted Execution Environments

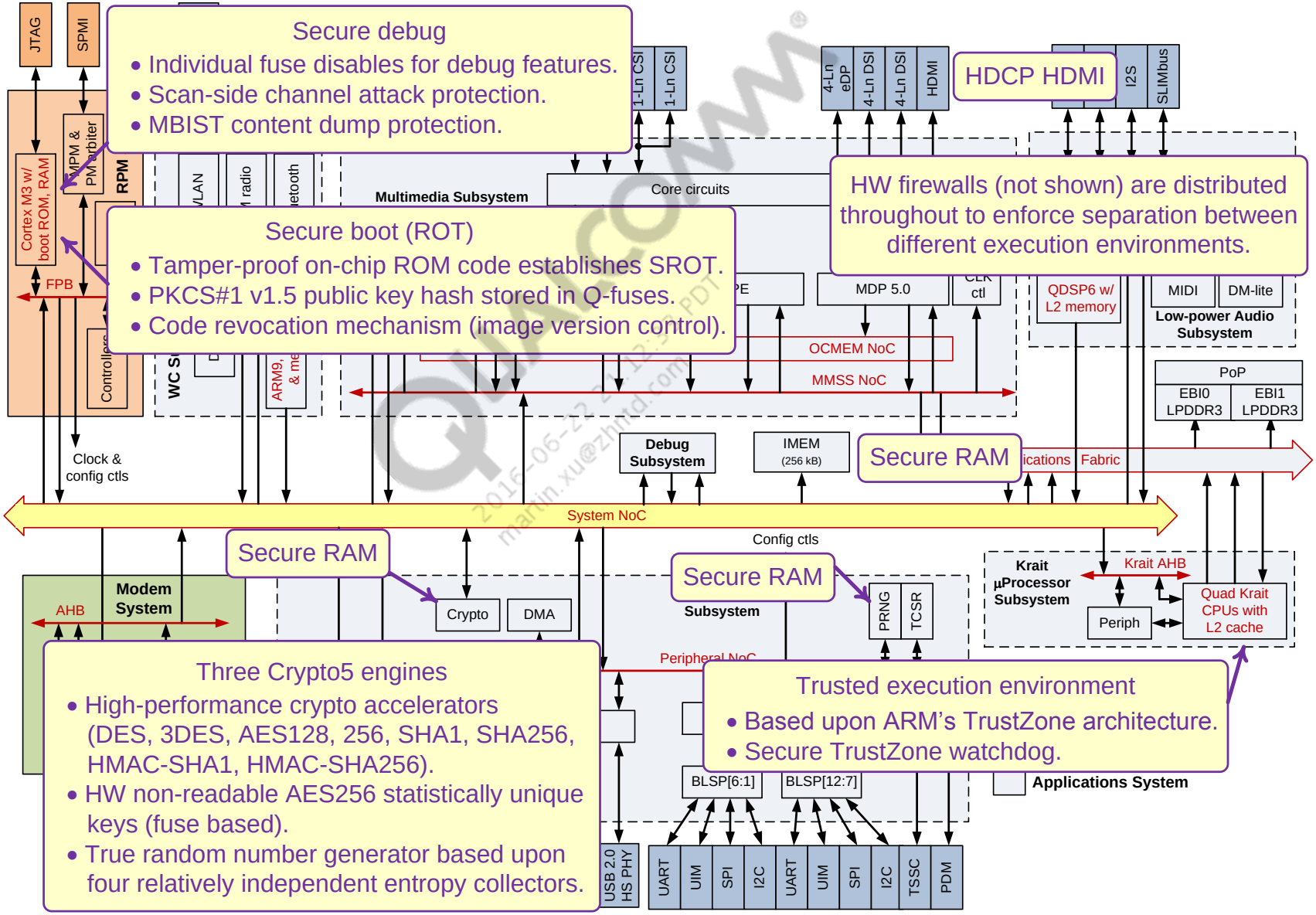
Execution environment (EE) – an isolated environment that allows independent code execution.

- The high-level operating system (HLOS) and its applications run in one EE, while a separate, trusted EE (TEE) is provided for other applications and services that require higher levels of assurance.
- Code running within a TEE is much more protected, more secure, and less likely to be compromised (compared to the HLOS environment).
- Even if the HLOS is compromised, secure applications running within a TEE are not.

- The MSM ICs provide the following TEEs:
  - lResource and power manager system
  - lKrait – the chipset's memory hardware firewall and secure boot provides the main platform's TEE
  - lModem system

- Implementation details for all TEEs are handled by QTI.

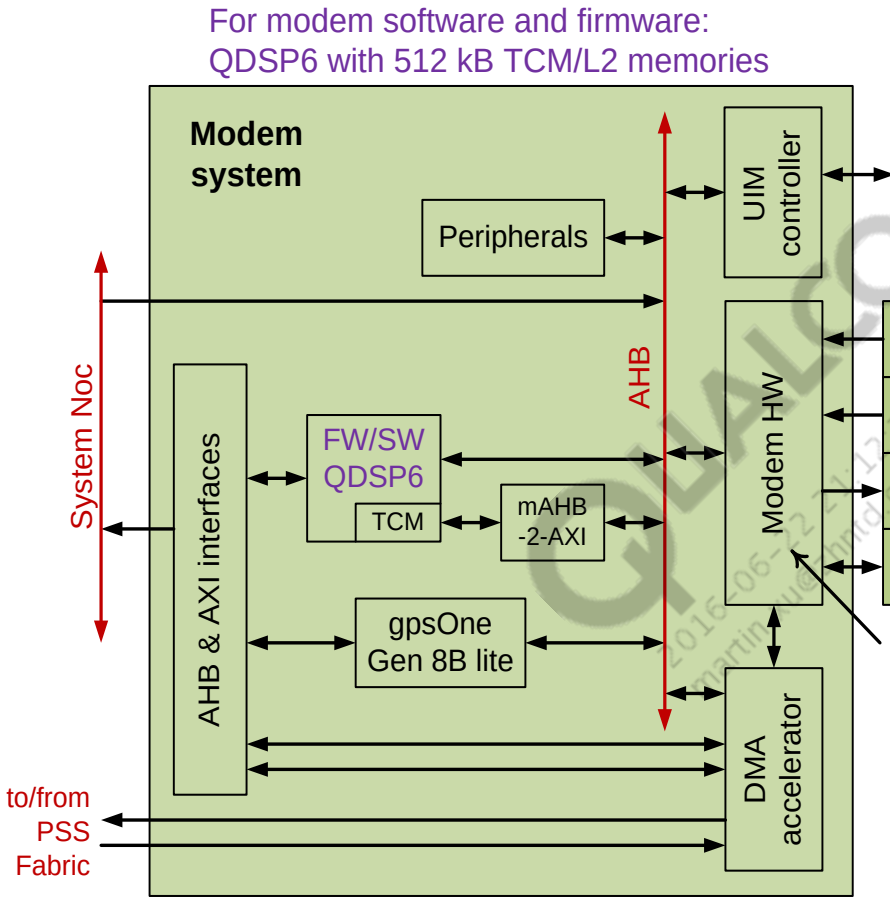
Security Highlights



Security Features (in Addition to Secure Boot)

- Top-level security goals:
  - Enforce protection of modem operation – make it sufficiently hard for an attacker to launch a successful software-based or physical attack that would gain any degree of control over modem functionality.
  - Enable secure implementation of digital rights management (DRM) applications – also protect against unauthorized copying or otherwise misusing audio or video DRM content.
  - Enable secure implementation of M-commerce applications – also protect against access to a user's financial information, or otherwise compromise M-commerce protocols.
  - Be compatible with Federal Information Processing Standard (FIPS) Level 2 (L2) security requirements.
- Building blocks that create services for OEMs, network operators, content providers, and end users:
  - Secure boot and code-signing infrastructure (discussed earlier)
  - Cryptographic accelerator and true random number generator (TRNG)
  - Memory and hardware resource separations – hardware firewalls
  - Secure debugging environment
  - Multiple trusted execution environments (TEEs)
  - Secure one-time programmable (OTP) electrical fuses – Qfuses within the QFPROM
- These building blocks allow implementation of security services such as:
  - Run-time integrity checking of secure code
  - Secure file system (SFS)

Modem System



Modem System Details

Modem processor based on QDSP6

- Modem firmware and software on a single Q6 core
- Controls clocks, timers, power, interrupts

Supports different RF architectures

- SVLTE (simultaneous 1x+ LTE)
- SVDO (simultaneous 1x+ DO)
- IRAT (inter radio access technology)
  - GSM, C2K, UMTS, LTE
- WLAN/LTE coexistence
- Navigation

Integrated UIM controller for supporting dual SIM

Air interface via BBRX ADC (input) and TX DAC (output)

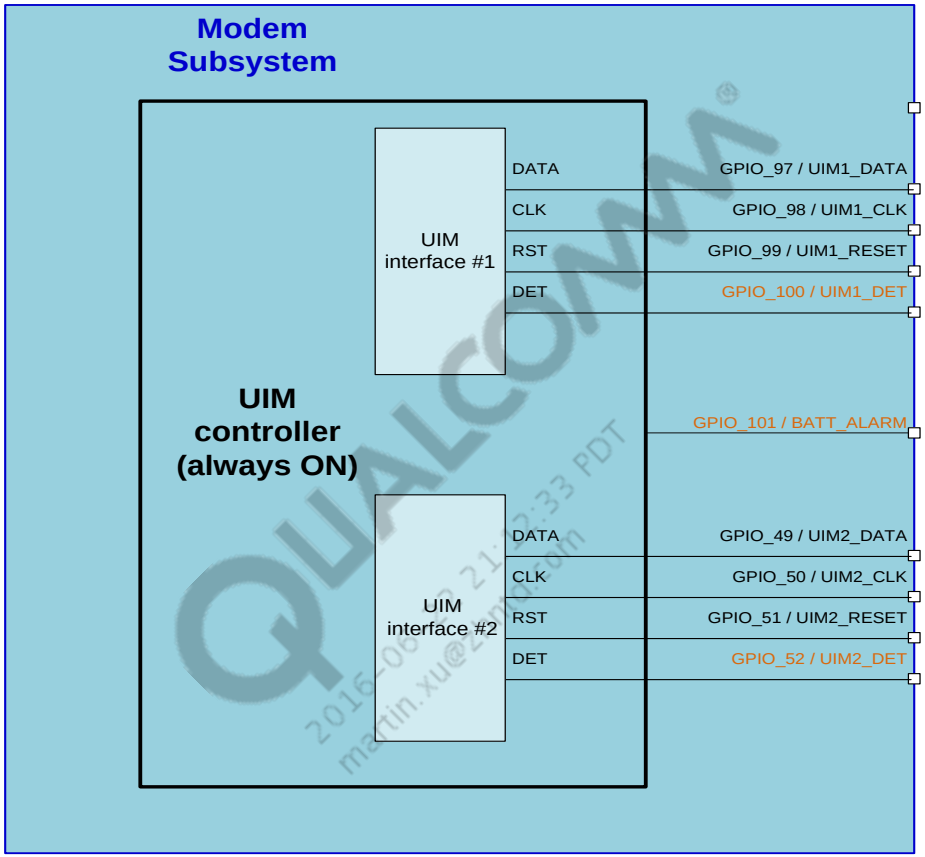
Control of external RF components

- WTR control via SSBI
- RF front-end control via RFFE and GRFC

Power supplies

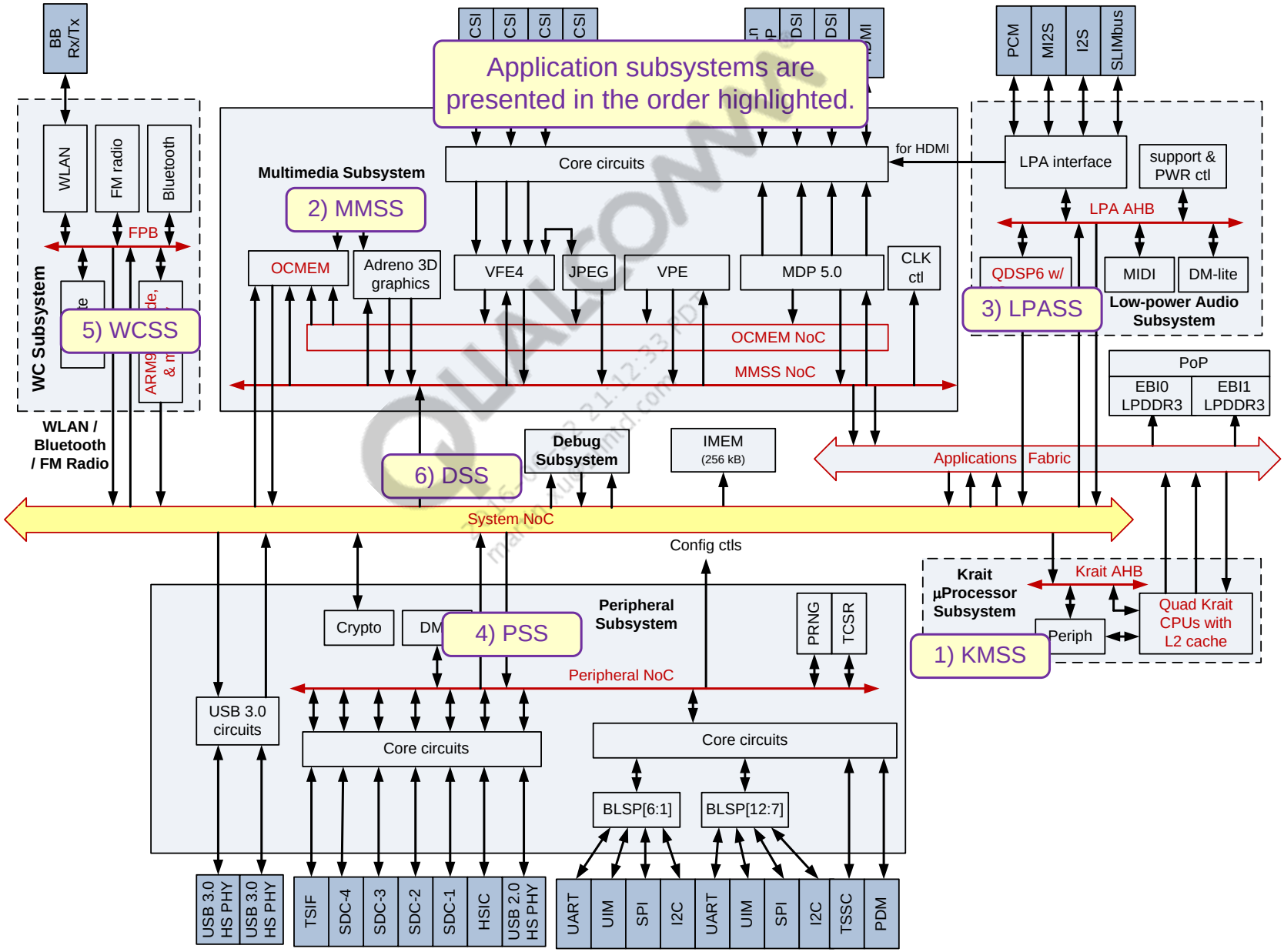
- VDD_MODEM for modem core/QDSP6
- VDD_A1, VDD_A2 for analog domains
- VDD_MEM for local memory

UIM Controller



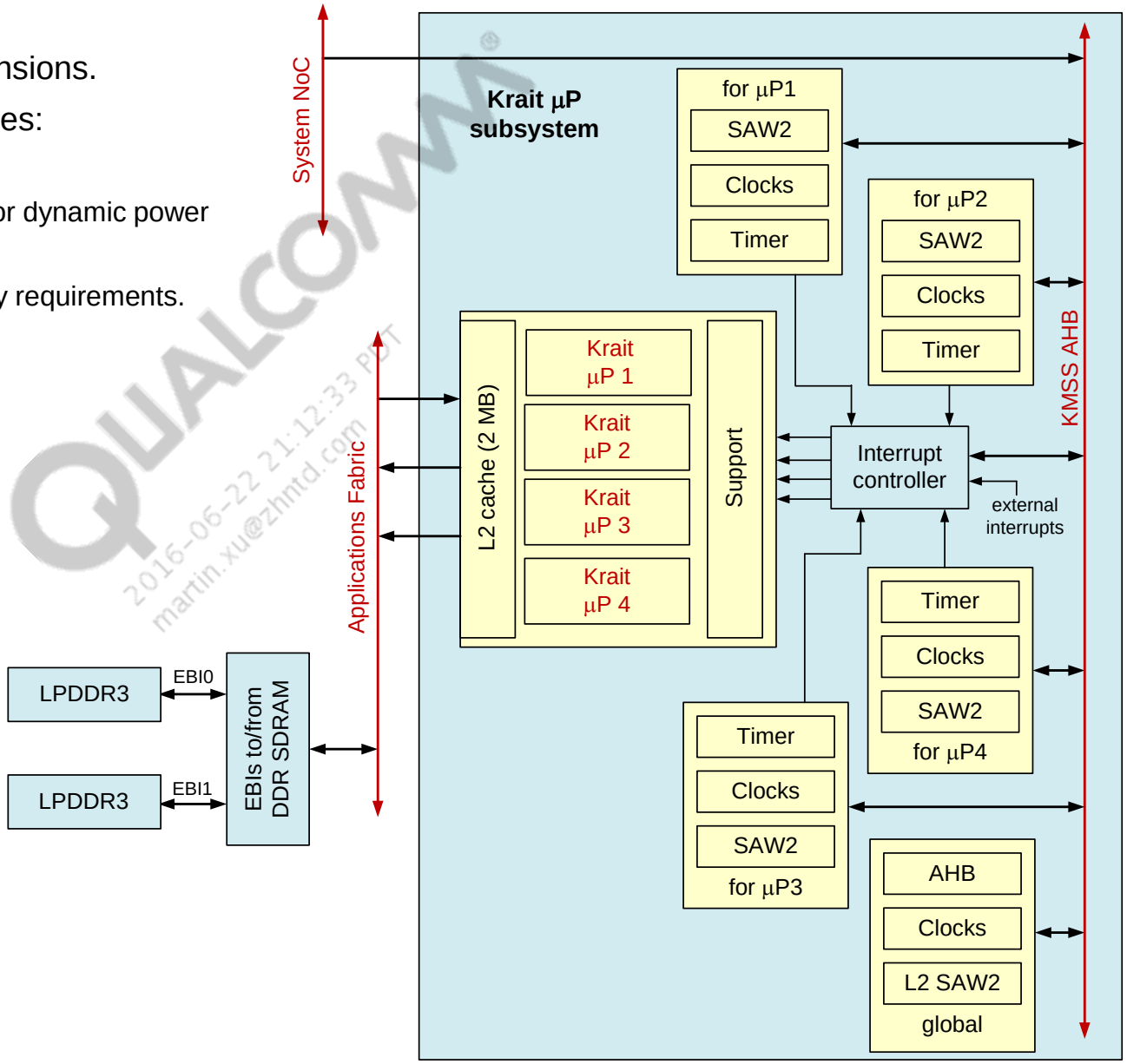
- The UIM controller belongs to the *always on* domain of the MSM device.
- The UIMx_DATA/CLK/RESET pads of the MSM device are capable of handling dual-voltage UIM: 2.95 V / 1.8 V.
- The three GPIOs (100, 101, and 52) are routed to the 64-bit MPM register indirectly through the UIM controller.
- The UIMx_DET signal indicates the insertion/removal of the UIM card to the UIM controller.
- The BATT_ALARM signal is bidirectional for the following two purposes:
  - The PMIC indicates MSM UIM controller for a low-voltage battery or battery removal.
  - The MSM UIM controller indicates PMIC of UIM removal by outputting a different clock frequency for each UIM interface removal.

Applications System



Krait Microprocessor Subsystem (1 of 2)

- Newer, faster Krait cores.
- Latest ARM v7 architecture extensions.
- QGIC2 interrupt controller includes:
  - ARM generic timer (Qtimer).
  - Second-generation SAW (SAW2) for dynamic power management.
  - New address map supports security requirements.

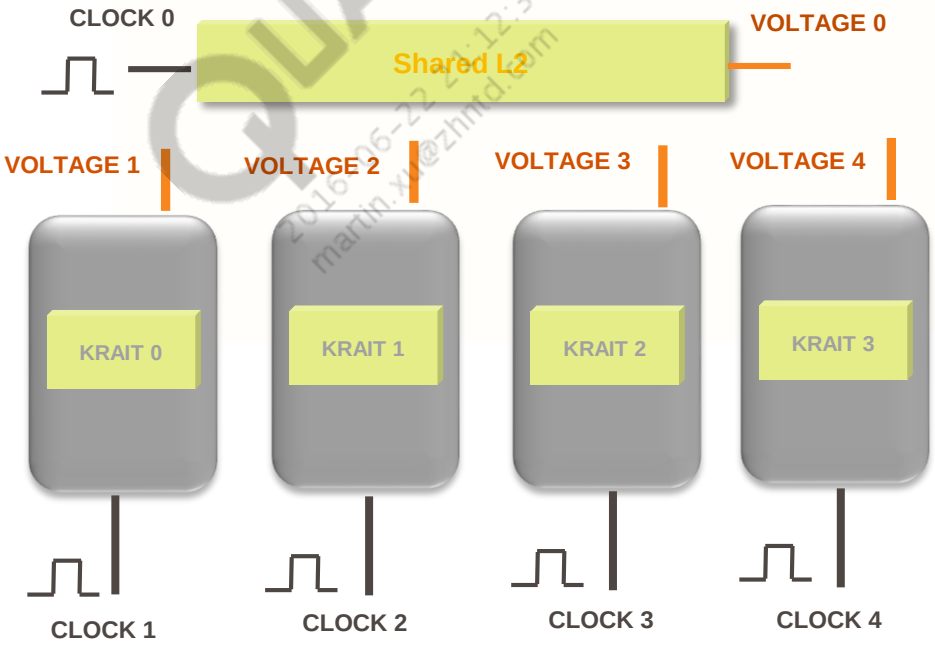


Krait Microprocessor Subsystem (2 of 2)

- Quad Krait CPUs, each with:
  - Up to 2.5 GHz
  - 2 MB L2 cache
  - 4 kB L0 & 16 kB L1 instruction & data caches
  - ARM v7 compliant
  - TrustZone support
  - VeNum 128-bit SIMD MM coprocessor
- PoP LPDDR3 memory on dual-channel EBI:
  - See *Memory Support* section:
    - Low-latency paths from CPUs to memory
    - High-speed memory controller with reordering
    - Priority control for CPU accesses
- Shared L2 cache:
  - 2 MB, 8-way set associative with ECC
  - HW-enforced coherency, including slave port
  - Dual interleaved AXI master ports increase memory bandwidth
  - L2 lines individually lockable for virtual TCM
- KMSS AHB:
  - 64-bit
  - Local connections from CPUs to memory
  - High-bandwidth multimedia traffic mostly localized to separate multimedia fabric
  - Tiered arbitration to enable efficient bus/memory sharing with priority CPUs
- Multiple power and clock domains:
  - Independent domains for each μP & memories
  - L2 data retention enables CPU power collapse
  - Independently scalable clocks for each core & L2

aSMP Architecture for Krait

- aSMP (Asynchronous Symmetric Multi Processing) – QTI's low power technology.
- Independent voltage and frequency control of each CPU core as well as the L2 cache.
- Optimal performance/power efficiency is based on workload.
  - Scheduling is done by load balancer
- Cores can be completely collap
- Power savings is more than 20



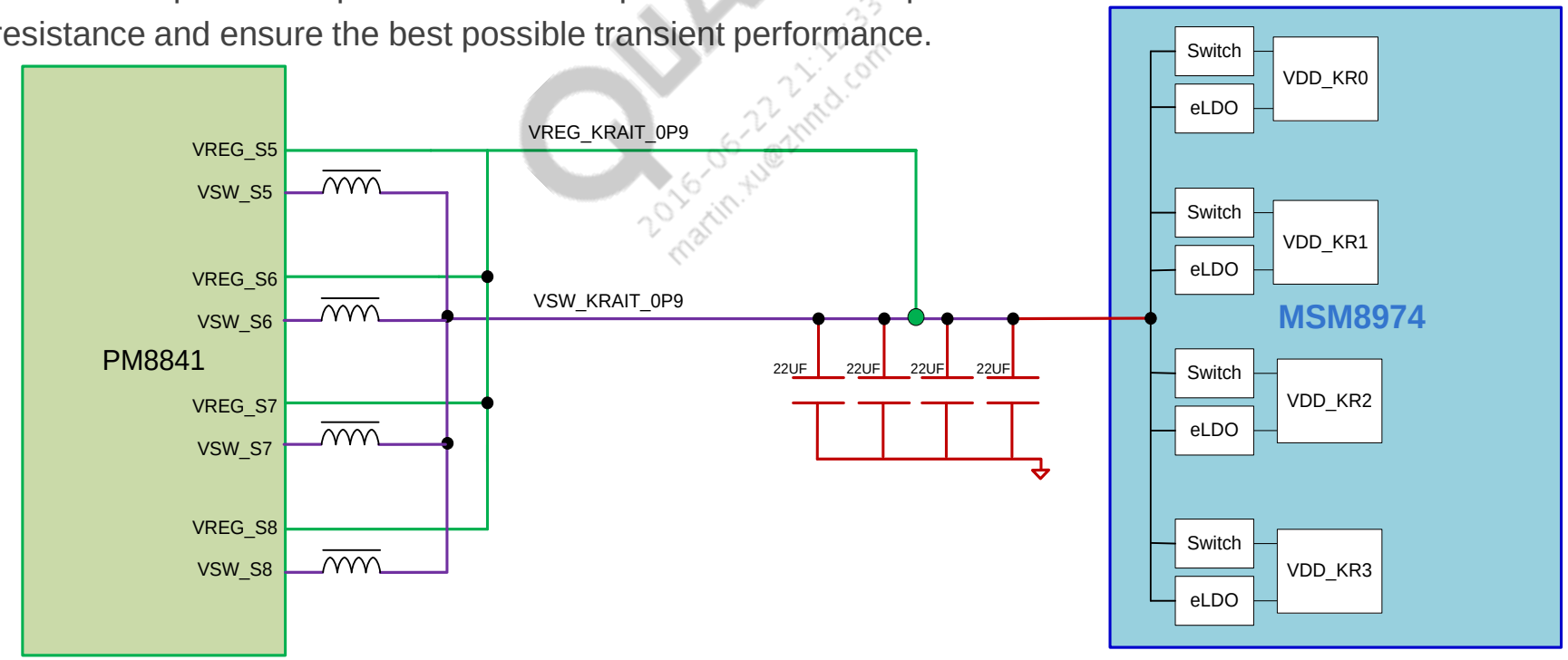
Krait Power Supply

All four SMPS (S5B–S8B) outputs are tied together at PMIC and routed as single trace to the MSM device.

Each Krait core inside the MSM device has a block head switch (BHS) and an eLDO that supplies power to the Krait core.

- The switch turns **on**/**off** the SMPS voltage to the Krait core in bypass mode.
  - All Krait cores in BHS mode will have the same voltage as the SMPS output.
- The LDO is used if a voltage less than SMPS output is required by a Krait core.
- The MP-DCVS algorithms determine the efficient voltage/frequency for each Krait core.

The four output bulk capacitors should be placed as close as possible to the MSM device to reduce series resistance and ensure the best possible transient performance.



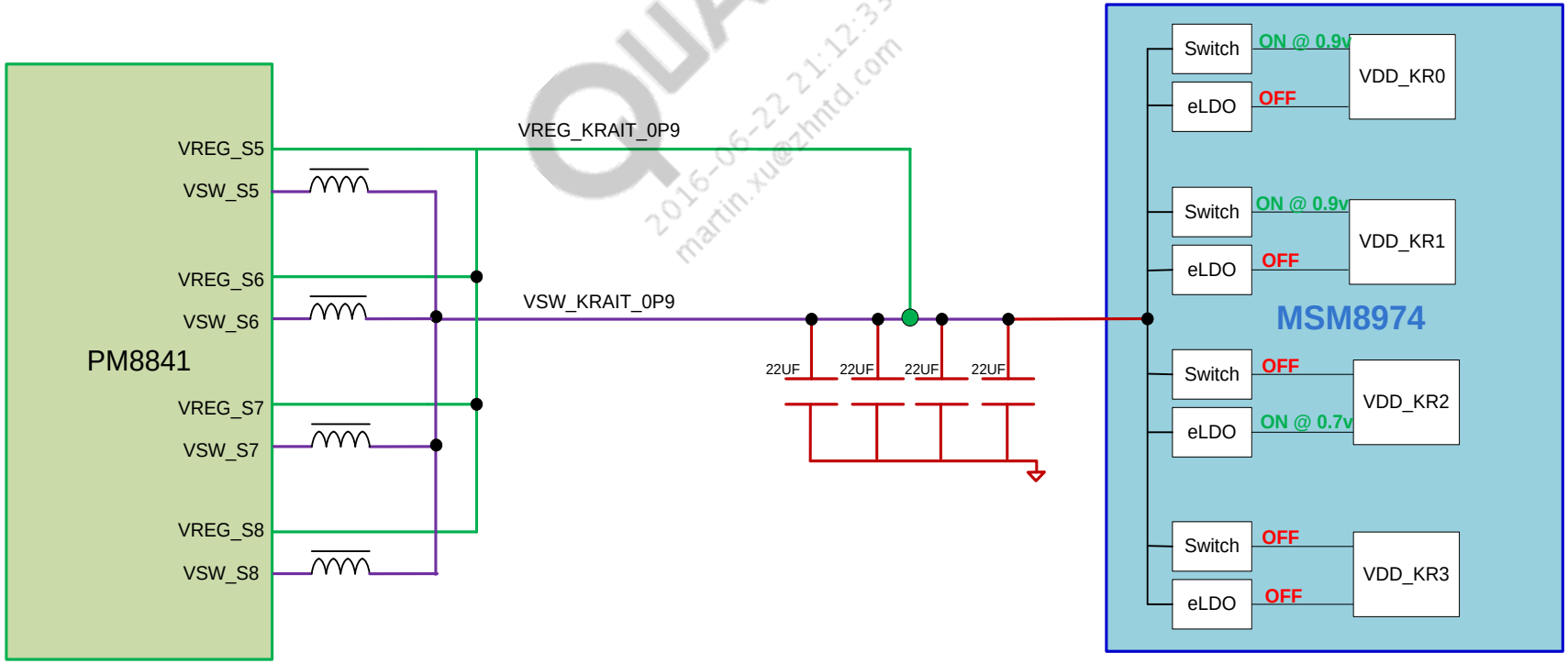
Krait Power Supply – Example Use Case

For example, In certain use case lets assume the following voltages are required by the four Kraits:

- Krait 0 -> 0.9 V
- Krait 1 -> 0.9 V
- Krait 2 -> 0.7 V
- Krait 3 -> OFF

The above voltages are implemented as shown in the diagram.

By default only VREG_S5 is turned ON. Based on the current requirement, the MSM will turn ON other SMPS using SPMI commands.

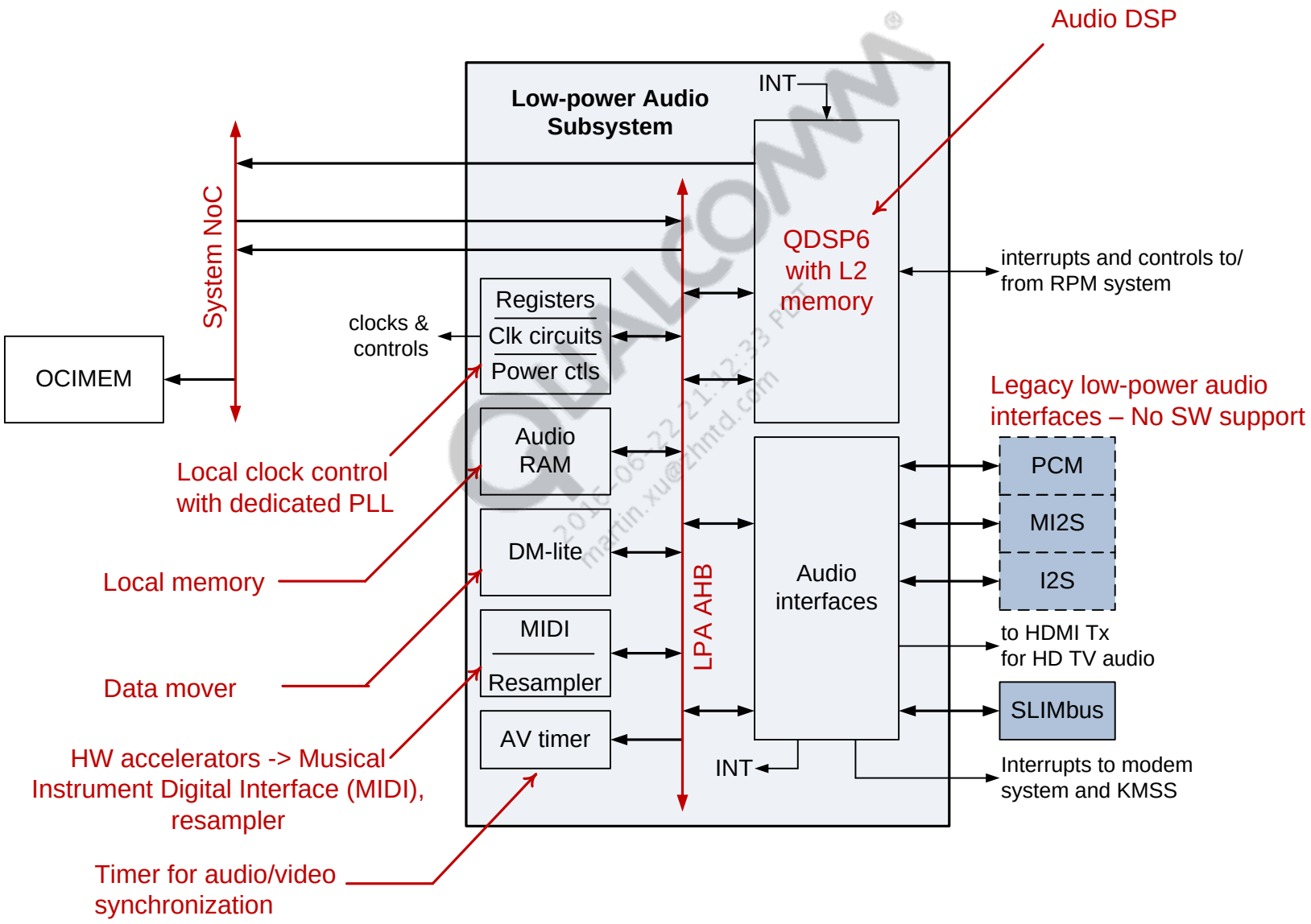


Krait Performance

The table below provides an estimate of performance using Krait 28 HPm.

Feature	Krait 28 HPm
Maximum frequency (28 HPm, TT, 0.9 V, 90°C)	Up to 2.5 GHz
Maximum performance	7820 DMIPS
Total power at normalized DMIPS (@ 5780 DMIPS)	445 mW
DMIPS at normalized power (@ 660 mW)	6713 DMIPS

Low-Power Audio Subsystem (1 of 3)



Low-Power Audio Subsystem (2 of 3)

LPASS is used for:

- Route audio/voice from/to Audio codec
- Realtime voice and audio processing
- Circuit switch voice processing with low round-trip latency
- Support non-realtime audio encode/decode/processing requirements off loaded from HLOS
  - Audio/video synchronization

Provide current playback time information back to the HLOS for use in adjusting playback progress bars.

Power control

- Uses LPASS core powered by VDD_CORE , using a BHS, unlike previous chipsets with dedicated LDO
- QDSP6 powered by VDD_CORE using a BHS
- LPASS local memory (64 kB SRAM) powered by VDD_MEM

LPASS has access to OCMEM (1.5 MB) of Multimedia SS

Audio Interfaces

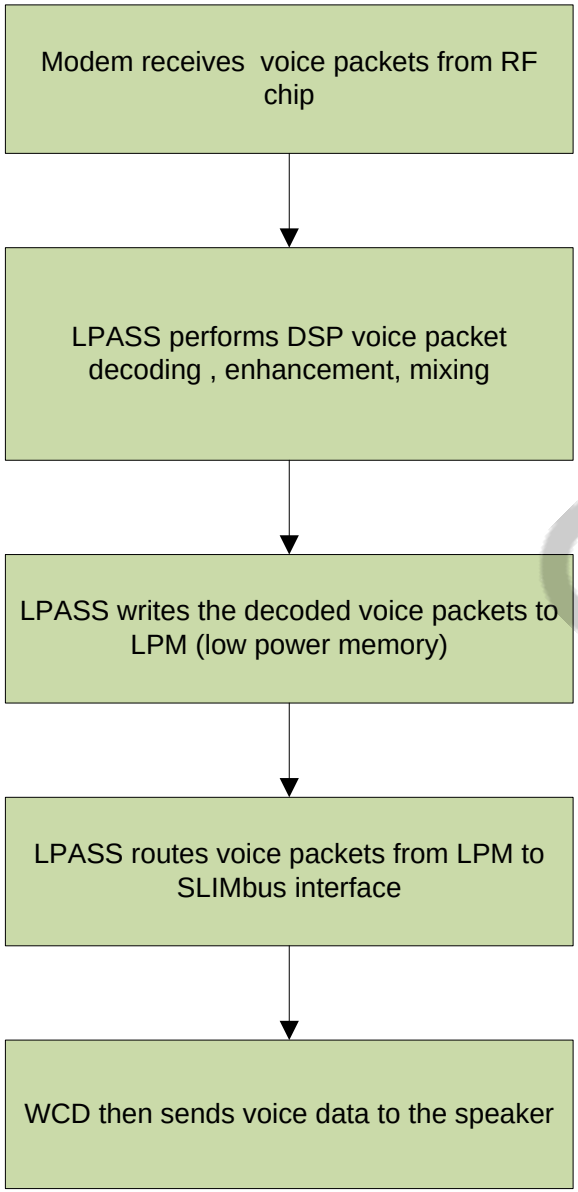
- SLIMbus (WCD9320)
- HDMI audio
- I2S
- MI2S
- PCM signals are multiplexed with MI2S signals

Low-Power Audio Subsystem (3 of 3)

- Low-power features:
  - Power-efficient processing for voice and multimedia audio applications.
  - Power gating within LPASS core.
  - QDSP6v5 supports L2 cache data retention during power collapse.
  - Supported modes: ACTIVE/IDLE/DORMANT/OFF.
- Audio QDSP6v5
  - 16 k L1 instruction; 32 k L1 data; 256 k L2 caches.
  - 600 MHz effective clock rate.
  - Separate voltage domain is scaled with performance requirements.
- Dedicated 64 kB low-power memory – bit-stream buffer, PCM buffers, DSP OS
- Primary audio interface
  - SLIMbus (24 ports) for the WCD9320 codec IC
- Legacy audio interfaces
  - I2S and PCM for the Sony Philips digital interconnect format (SPDIF)
  - MI2S
  - Internal HDMI Tx connection to the MMSS
- Musical Instrument Digital Interface (MIDI)
  - Acceleration HW
  - 128-poly MIDI processing
- LPASS support by other modem IC subsystems
  - Krait microprocessors for data transfers from memory and/or file system.
  - Other subsystems (PSS, WCSS) for WCN interfaces:
    - Eliminates AUX_PCM routing for Bluetooth SCO, UART for Bluetooth A2DP, and I2S for FM.
    - PCM samples for Bluetooth and FM are routed internally and processed by the WCSS.

See WCD9320 material for more details

Example Data Path: Circuit-Switch Voice Call



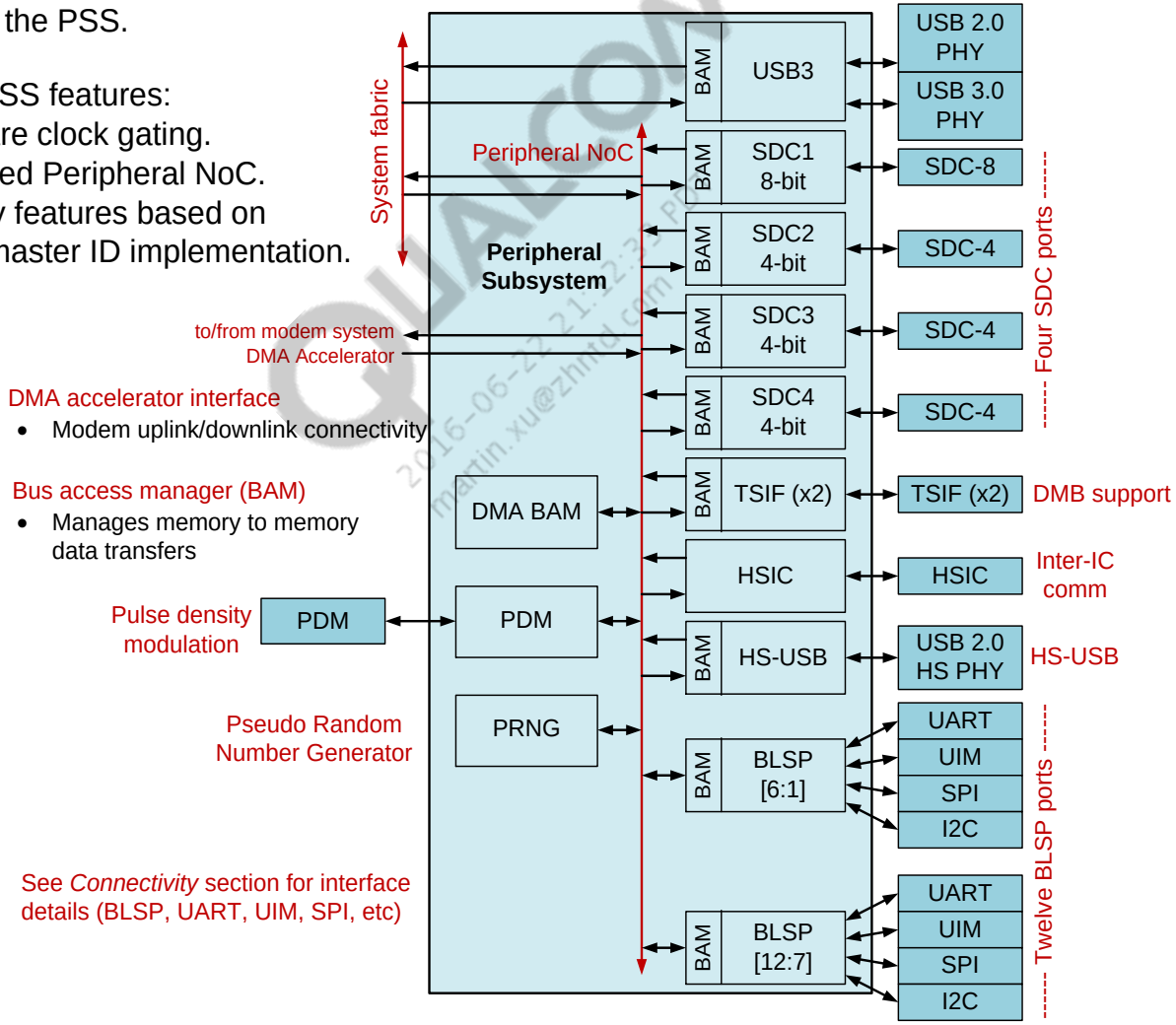
Peripheral Subsystem

Improves peripheral operations requiring significant main CPU and system IMEM involvement (high loading) – power-optimized architecture for higher throughput at lower power dissipation.

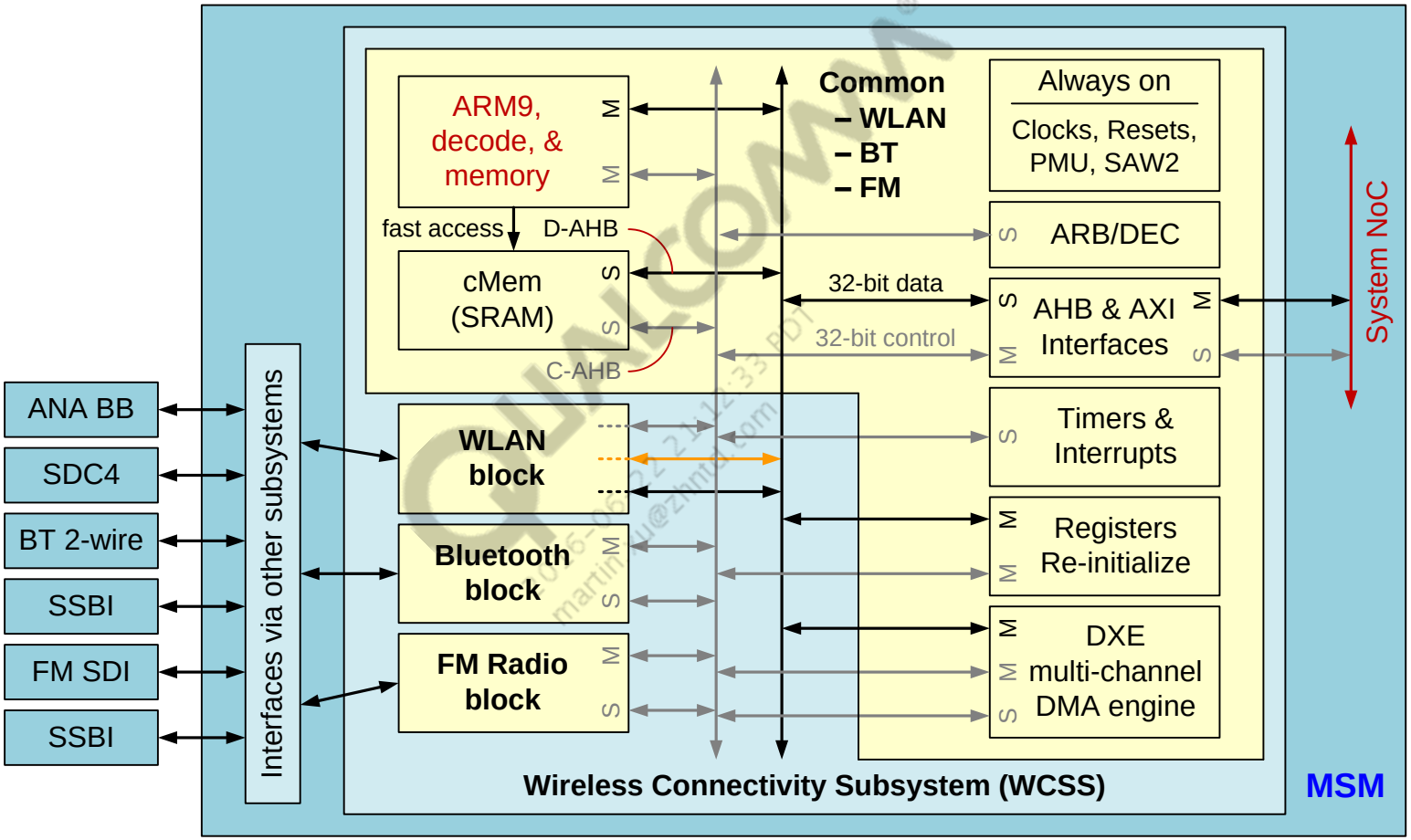
- Decentralized, very scalable architecture.
- High-throughput peripheral devices are concentrated in a semi-autonomous subsystem.
- New peripheral NoC bus architecture to provide master and slave AHB bus connectivity to the peripheral cores in the PSS.

General PSS features:

- Hardware clock gating.
- Dedicated Peripheral NoC.
- Security features based on virtual master ID implementation.



Wireless Connectivity Subsystem (1 of 2)



See WCN material for more details

Wireless Connectivity Subsystem (2 of 2)

Key use cases:

WLAN:

- Beacon-mode power save
- File upload/download (50 Mbps and 200 Mbps)
- Streaming video
- VoIP call
- WLAN standby (OOS searching)
- Soft AP
- Location services over WLAN

Bluetooth:

- Inquiry/page scan
- Low-power page scan
- Sniff
- Audio playback + Bluetooth A2DP
- Low-power audio playback + Bluetooth A2DP
- WAN voice call + Bluetooth SCO (HV3)
- File upload/download

FM radio:

- FM receive
- FM Rx recording
- Low-power audio playback + FM Tx

Concurrency:

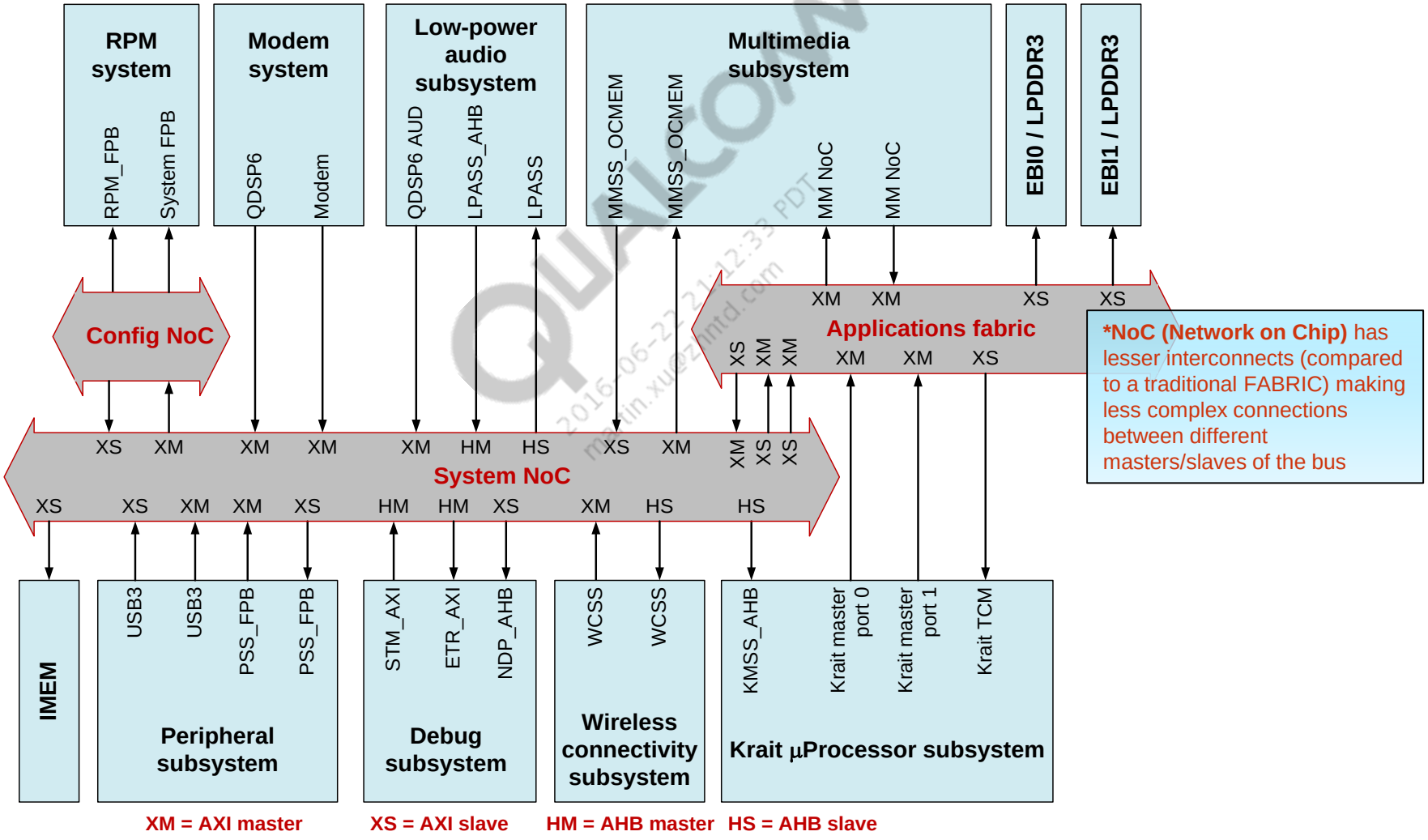
- FM receive + Bluetooth A2DP
- WAN VoIP call + Bluetooth SCO (HV3)
- WLAN music streaming + Bluetooth A2DP
- LT/Bluetooth/WLAN coexistence
  - WLAN file transfer + Bluetooth SCO
  - WLAN file transfer + Bluetooth A2DP
  - LTE file transfer + Bluetooth SCO
  - LTE file transfer + Bluetooth A2DP
  - LTE file transfer + WLAN SoftAP

Debug Subsystem (QDSS)

- QDSS is capable of accessing the following sub-systems.
  - All four Krait cores
  - RPM Cortex M3
  - Modem QDSP6
  - LPA QDSP6
  - WCN ARM926
- The QDSS trace subsystem accepts ATB trace bus data from all trace sources in the system.
- This trace data is upsized to the maximum trace bus width within QDSS (128 bits).
- Support for sinking trace data to:
  - Two 18-pin ETM trace ports
  - One 6-pin ETM trace over SDC2
  - JTAG
  - System memory (main memory) – LPDDR3
  - USB3.0 via ETR (embedded trace router)
- QDSS timestamp subsystem is responsible for generating and transporting a master 64-bit timestamp synchronously to all subsystems.

Bus System

- The Config NoC is the interconnect at the top-level off of which the configuration ports for the chip (clock controller, TLMM, etc.), subsystems, and the NoCs are connected.
- The separate NoC for configuration isolates configuration ports to reduce the loading on the System NoC.



Sec. 6

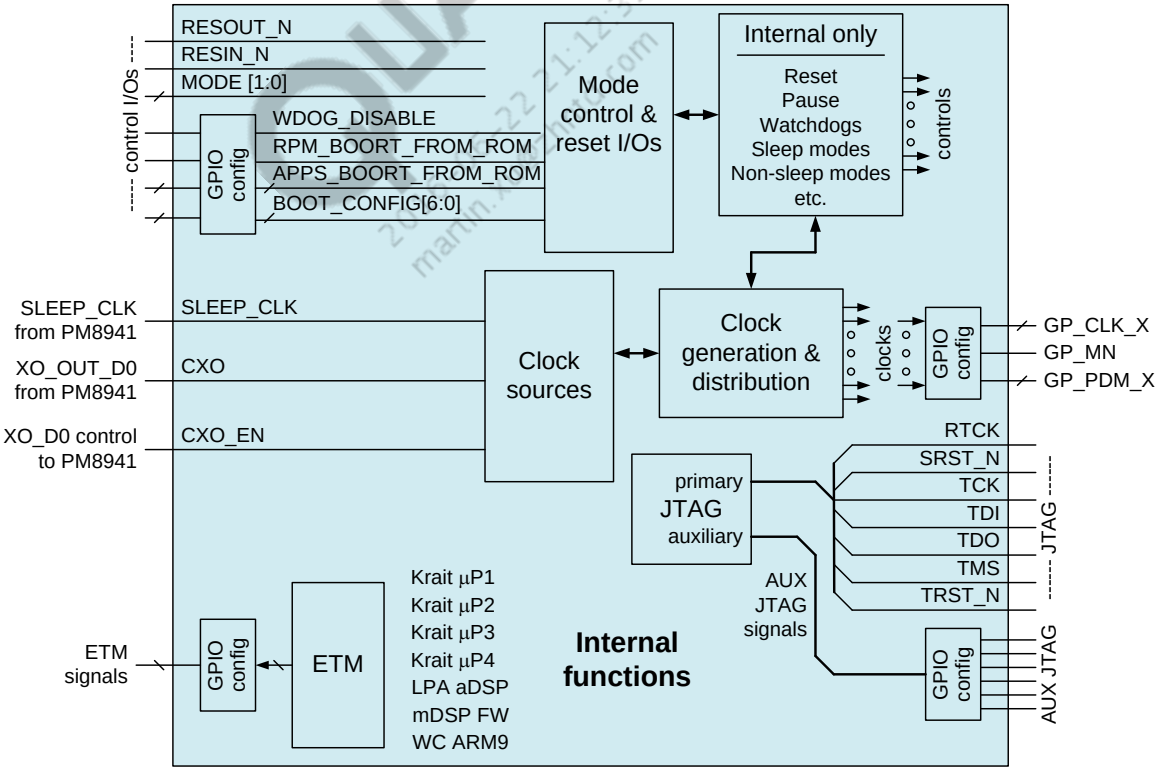
Other Key Internal Functions

Other Key Internal Functions Overview

Explanation – the MSM architecture presented in the *MSM Architecture* section uses circuits that are included within the IC's *Internal functions* block; the internal functions circuits not previously discussed are the focus of this page.

Internal functions not previously discussed:

- Watchdog timers
- System reset
- Sleep modes
- Test & debug
- Raw clock sources, on-chip clocks, etc.
- Thermal sensors

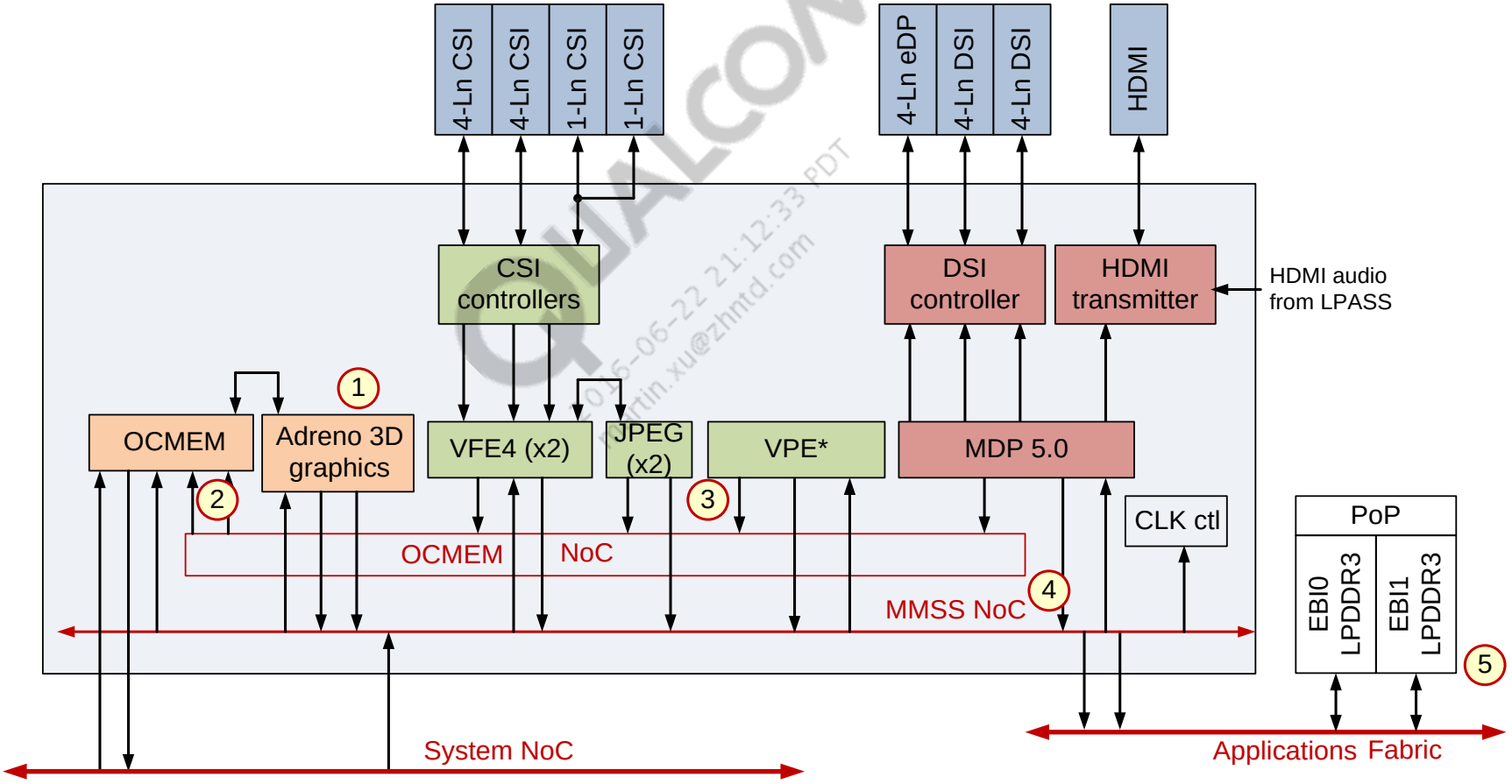


Sec. 7

Multimedia

Multimedia Architectural Overview

Major blocks: Display support (red) → Two, 4-lane DSI, HDMI TV display, eDP + MDP 5.0 processing
Image processing (green) → 4-(x2)/1-(x2) lane CSI + VFE/JPEG/VPE processing
Graphics (orange) → Adreno 330 with on chip memory
Audio → see LPASS and WCD9320 content



*VPE (video processing engine) is a new block that integrates video codec, bus interface (VBIF), and ARM9; based CPU sub systems.

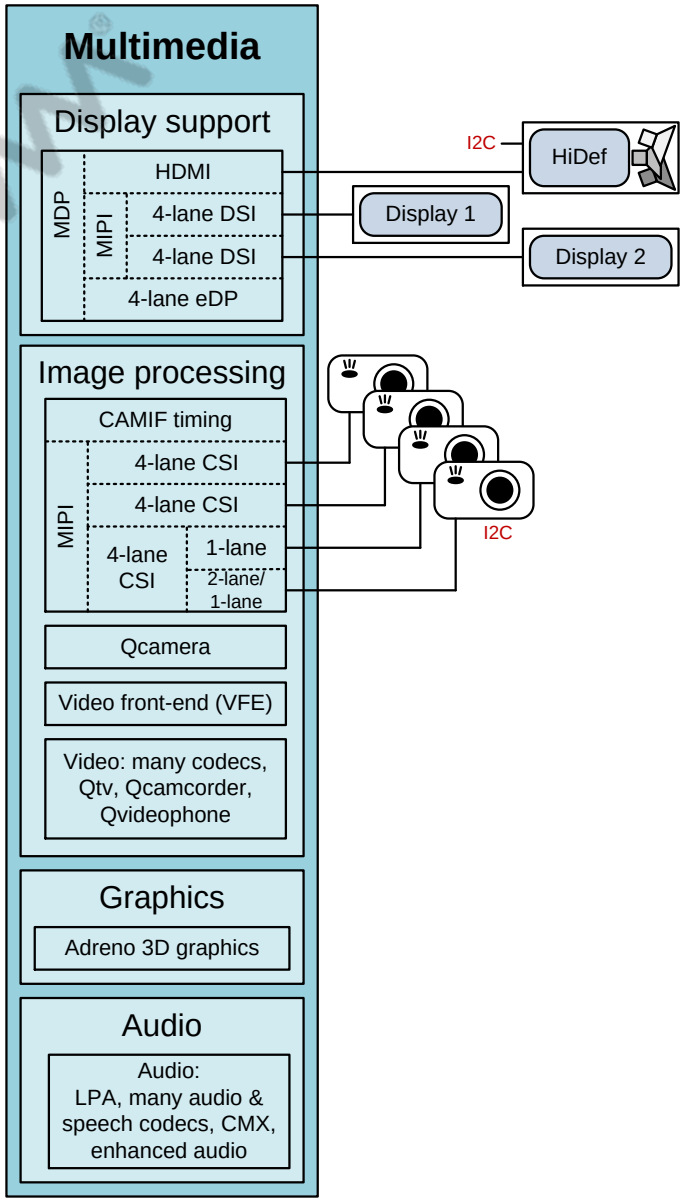
Multimedia Subsystem

1. Adreno 330 graphics acceleration HW
   - Adreno 330 450 MHz 3D graphics accelerator
   - APIs include OpenGL ES 1.1/2.0/3.0, DX9.3
2. On-chip memory (OCMEM) and the OCMEM bus (OCMEM NoC)
   - 1.5 MB unified SRAM reduces the bandwidth to external memory, minimizes latency for critical traffic and reduces power.
   - 128-bit wide OCMEM NoC allows a number of AXI clients from the MMSS to share access to the OCMEM.
3. Other multimedia acceleration HW
   - JPEG encode & JPEG decode
   - Video pre-processing (VPE)
   - Display pre-processing
   - Display engine with in-line processing for HDMI support
4. Multimedia subsystem NoC
   - 128-bit wide NoC for high-BW access to local multimedia memories (333 MHz).
   - Next generation system interconnect increases bus utilization.
5. Multimedia DDR memory
   - Low latency memory accesses for latency-sensitive MM cores
   - High DDR efficiency by decoupling multimedia and system memory accesses
   - Opportunities for power savings with independent MM power and clock domains

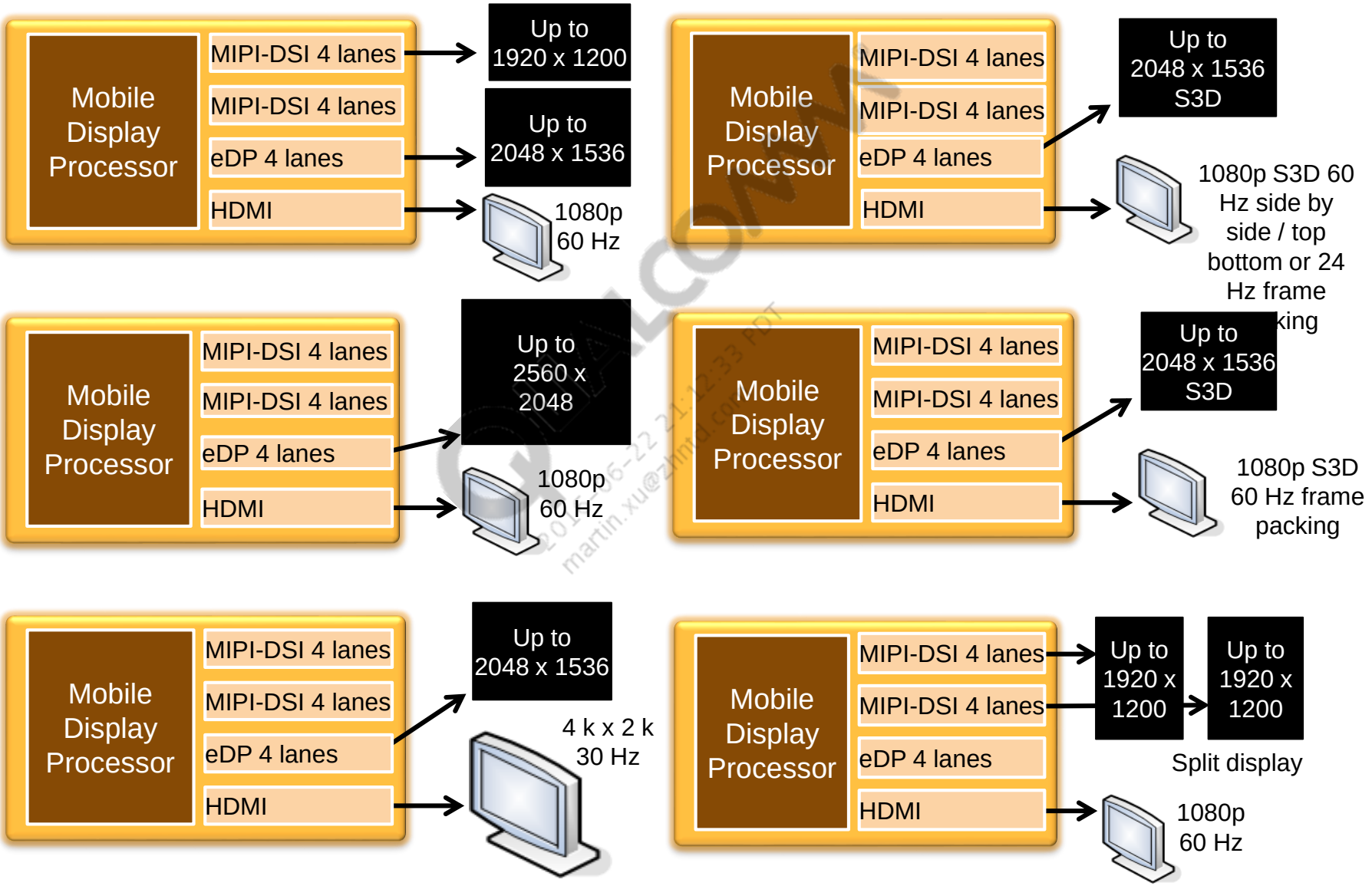
Multimedia Topics

Four major multimedia blocks:

1. Display support
   - A. MDP 5.0
   - B. MIPI display serial interface
     - Two, 4-lane DSIs
   - C. HDMI
   - D. embedded Display Port (eDP)
     - eDP v2.1, 4-lane
2. Image processing
   - A. MIPI camera serial interface
     - i. up to 4 CSIs
     - ii. 4-lane CSI0, CSI1, and CSI2
   - B. Camera timing signals & operational data flows
   - C. Video
     - Video front-end (VFE), in-line JPEG, video preprocessing engine
3. Graphics
   - A. Adreno 330 graphics
4. Audio (material not included in this section)
   - A. LPASS, as discussed in the *MSM Architecture* section
   - B. Companion WCD9320 audio codec – see *WCD9320* training for details



Display Support Overview

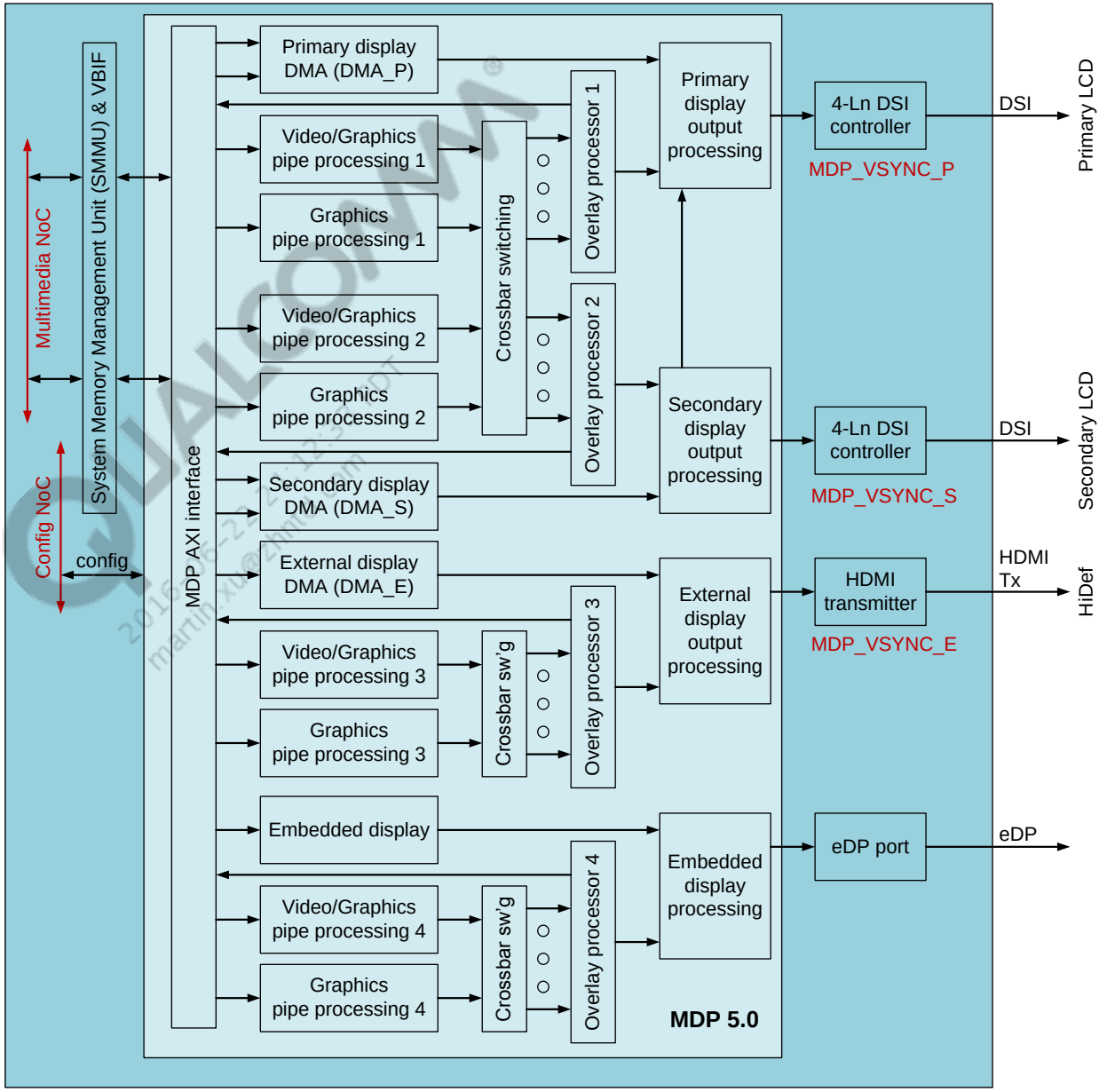


Note: APICAL does not support displays beyond 1920 × 1200

Mobile Display Processor (1 of 2)

The MDP 5.0 is the new 5th-generation MDP hardware accelerator; it supports all displays:

- Dedicated accelerator HW for transferring updated images from memory to display interfaces.
- While MDP transfers an image, it performs a final set of operations to that image.
- Reduces circuit redundancy, offloads ARM and aDSP, improves system efficiency, and saves DC power.



Mobile Display Processor (2 of 2)

Key MDP 5.0 features

Graphics layer	
Input format	16/24/32-bit Alpha RGB
Scaling	1x/8 to 20x
Filtering	horizontal and vertical
• Bit-depth promotion	• Source cropping

Blending	
V / G layer alignment	arbitrary
Blend order constraints	none
Color keying	Video and graphics
Layer allocation for 3 displays	6 layers, each can be allocated to primary or secondary display
• Pre-multiplied alpha support	

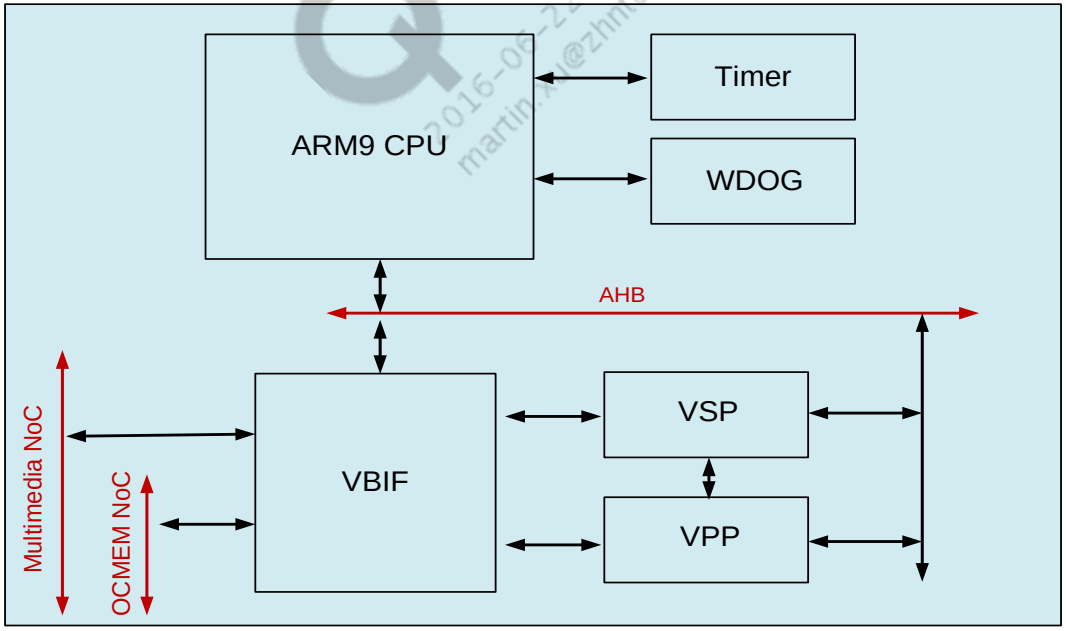
Video layer	
Input format	1/2-plane YUV
Scaling	1x/8 to 20x
Filtering	horizontal and vertical
• Source cropping	• De-interlacing
• Sharpening	• Histogram data collect
• Noise inject (dithering)	• Contrast enhancement
• Noise filtering	

LCD processing	
• Integrated LCD controller	• HW cursor support (64 x 64 max)
• Gamma correction	• Up to 24 bits per pixel
• Color correction	• Dithering
• Histogram data collection	• HW-based ABL for power savings
• Background color	• Wrtie back blended output to memory

Video Processing Engine (VPE)

VPE is a new block that integrates:

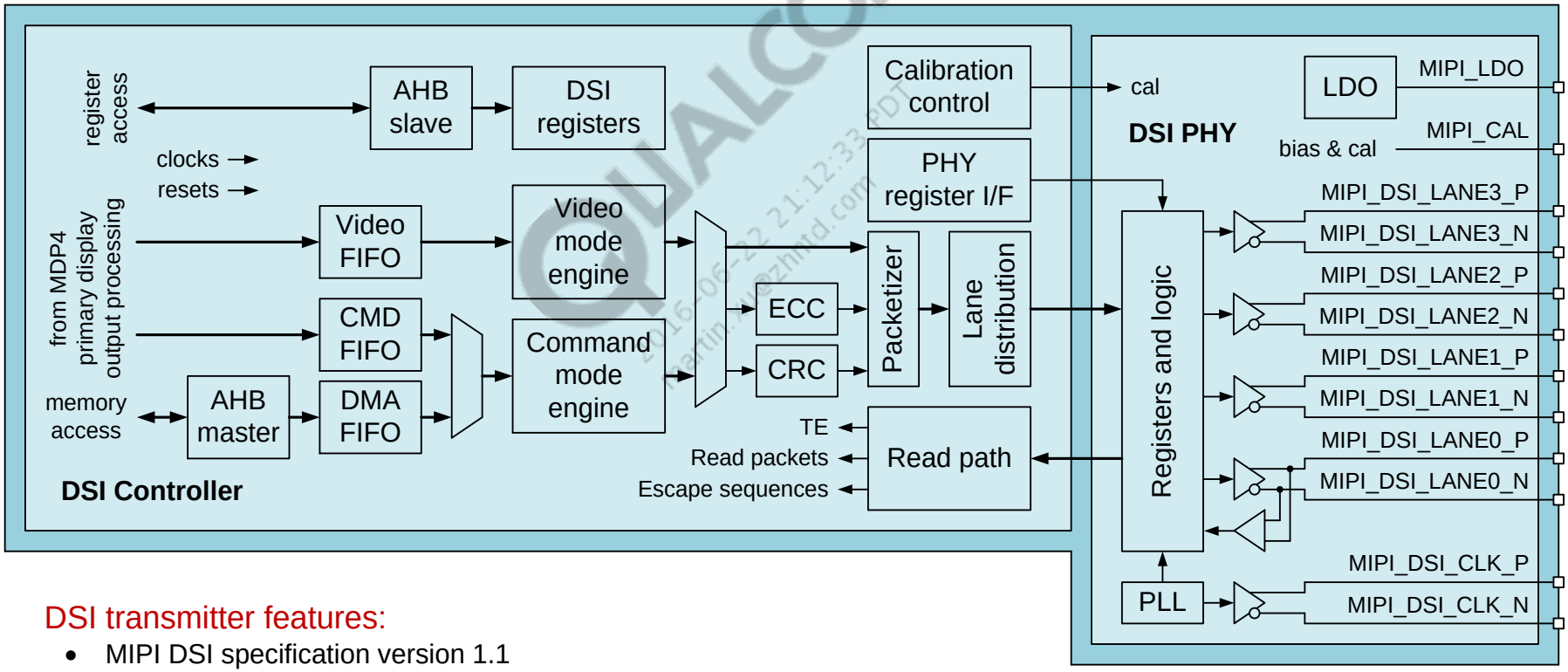
- Video codec for video pre/post processing
  - Video stream processing
  - Video pixel processing
- VBIF video bus interface for efficient access of video data to codec
- ARM9 based processor at 256 MHz:
  - Processing interrupts, timer/reset control
  - Off- loads MIPS from the Apps processor
  - Provides access to the external AHB bus



Display serial interfaces:

- Per Mobile Industry Processor Interface (MIPI) specification
- One high-speed clock lane and one to four data lanes
- Low-voltage differential signaling (LVDS)
- PHY block provides physical interface to display device

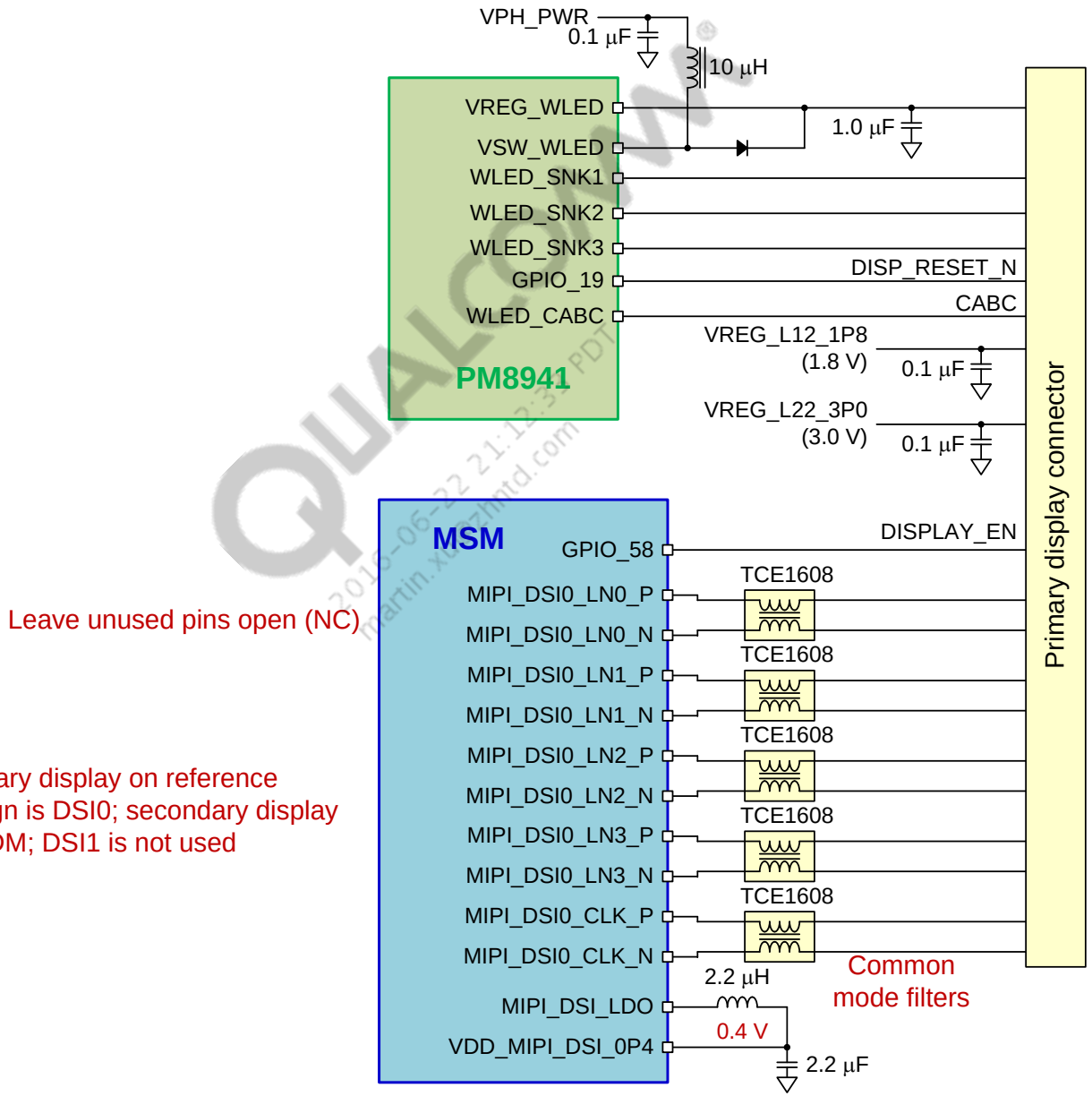
MSM8x74 has two 4-lane DSI (one shown here)



DSI transmitter features:

- MIPI DSI specification version 1.1
- MIPI D-PHY specification versions 0.65, 0.81, and 0.90
- Video and command modes
  - Four data lanes, up to four virtual channels
- Up to 1.5 Gbps per lane high-speed mode bandwidth
- Video color depths
  - 24-bpp RGB888
  - 18-bpp RGB666 loose or packed
  - 16-bpp RGB565

MIPI Display Serial Interfaces – Schematic Diagram



Leave unused pins open (NC)

Primary display on reference design is DSI0; secondary display is HDM; DSI1 is not used

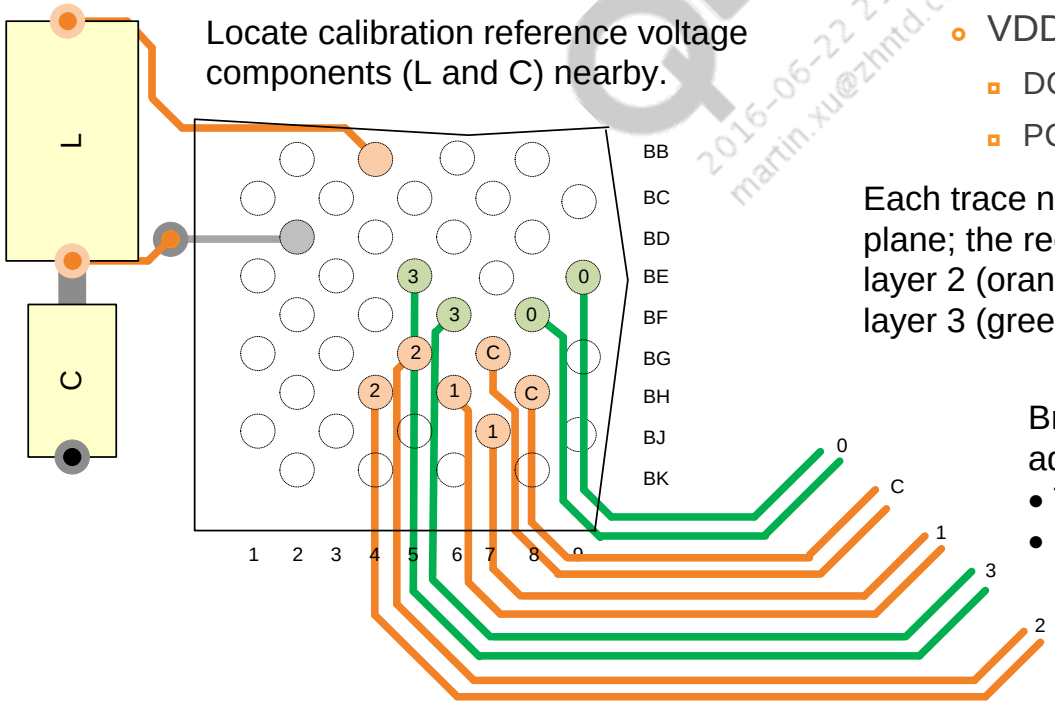
MIPI Display Serial Interfaces – Layout Guidelines

In addition to the guidelines presented here, see the MIPI Alliance Specification for D-PHY; it has extensive inter-pair and intra-pair isolation requirements that must be met.

- DSI signals are very high speed.
- Protect sensitive signals from DSI corruption.
- Protect DSI signals from noisy signals (clocks, SMPS, etc.).

Other comments and guidelines:

- 750 MHz clock rate; 1.5 GHz data rate
- Differential pairs, 100 Ω nominal, ± 10%
- Total routing length < 305 mm
- Intra-pair length matching < 5 ps (0.67 mm)
- Clock – data length matching < 10 ps (1.3 mm)
- Lane-to-lane trace spacing = 3x line width
- Spacing to all other signals = 4x line width
- VDD_MIPI_DSI_0P4
  - DC resistance < 50 mΩ
  - PCB trace loop inductance < 0.9 nH



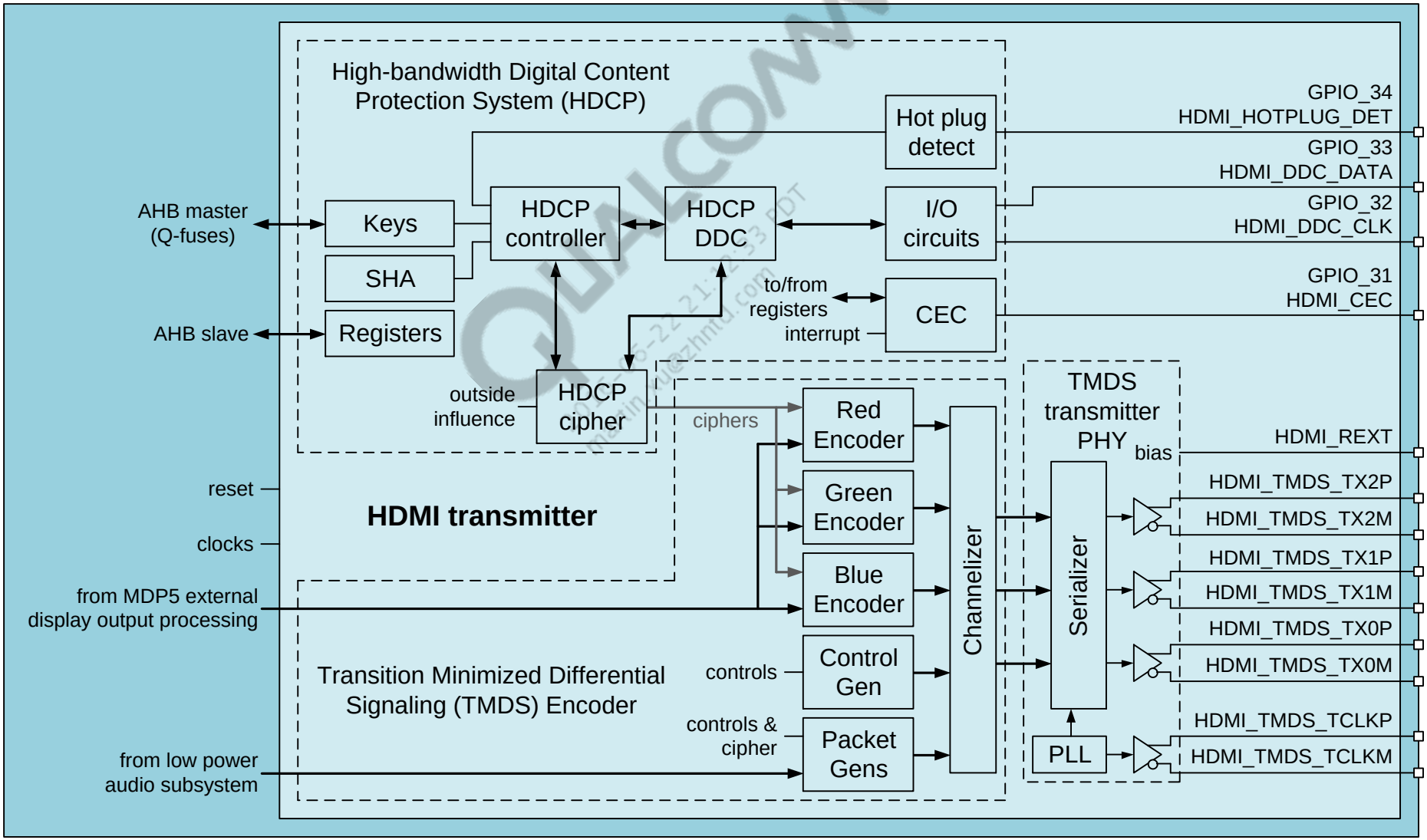
Each trace needs to be adjacent to a ground plane; the recommended implementation uses layer 2 (orange), next to layer 1 ground plane and layer 3 (green, next to layer 4 ground plane).

Broadside coupling occurs when traces on adjacent layers overlap or nearly overlap.

- This is unavoidable near MSM during breakout.
- But once routed away, force traces for each pair to separate from others to minimize coupling.

High-definition multimedia interface (HDMI) transmitter

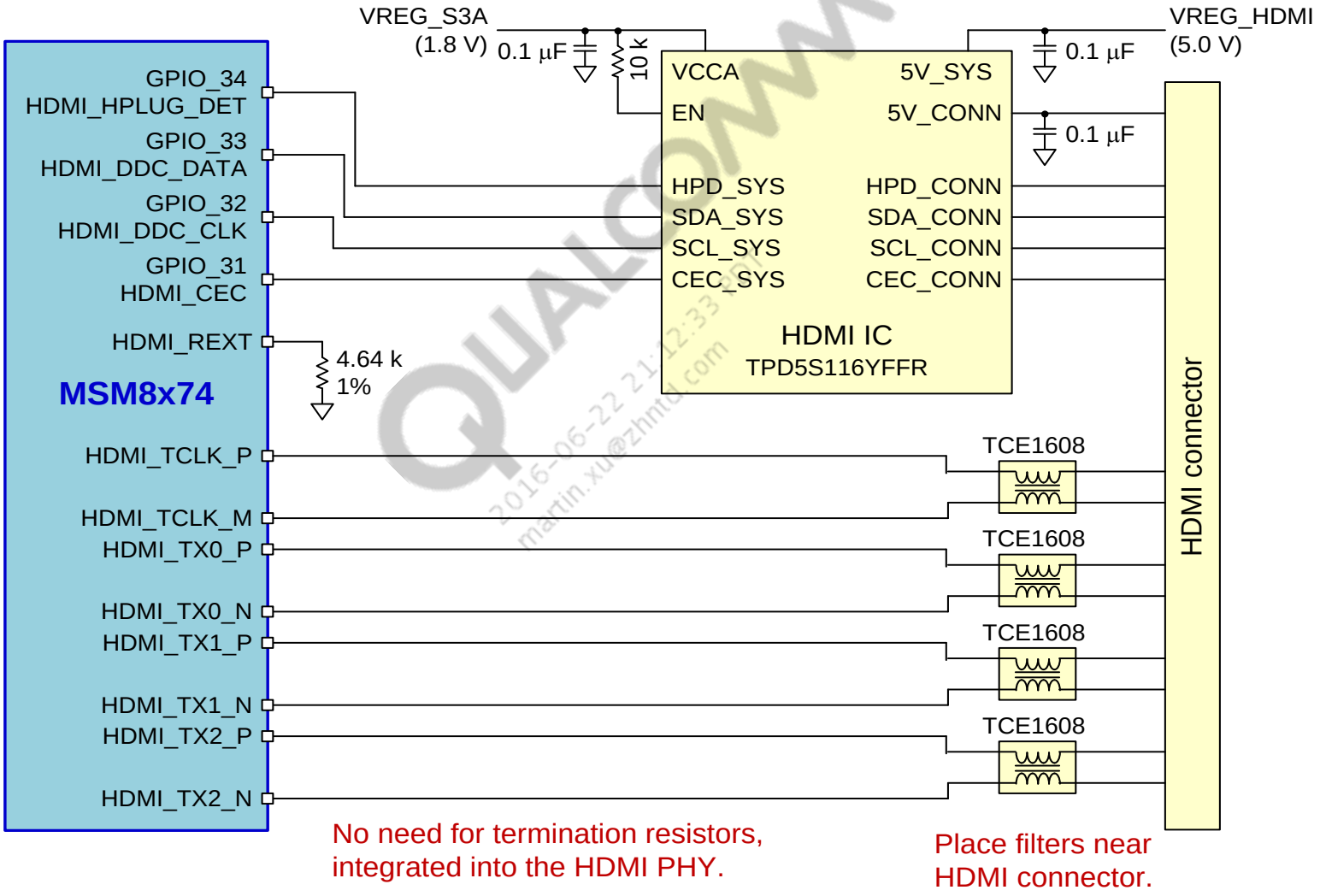
– Drives television sets, projectors, etc.



HDMI Transmitter – Features

- Supported specifications: HDMI version 1.4a with 3D
- Video pixel encoding: RGB444
- Video color depth: 24 bpp
- Video formats per CEA-861-D:
  - 640 × 480p, 1920 × 1080i, 720 × 480p, 720(1440) × 480i, all at 60 Hz
  - 1920 × 1080i, 720 × 576p, 720 (1440) × 576i, all at 50 Hz
  - 1280 × 720p, 1920 × 1080p at 24, 25, 30, 50, and 60 Hz
  - 4 k × 2 k at 30 fps
- Audio channels supported:
  - 2 (L, R; 2 channel L-PCM)
  - 8 (7.1 surround sound; 8 channel L-PCM 24-bit/192 kHz)
- Audio sample rates: 32, 44.1, 48, 88.2, 96, 144, 176.4, and 192 kHz

HDMI Transmitter – Schematic Diagram



HDMI Transmitter – Layout Guidelines

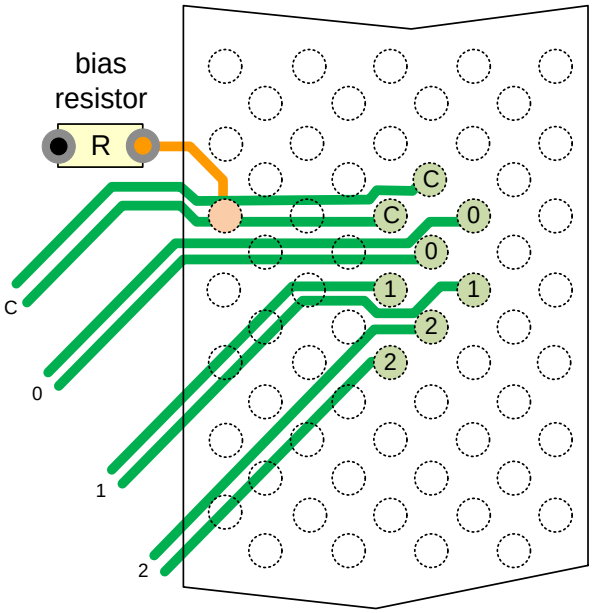
Primary HDMI signals are very high-speed:

- Protect sensitive signals from HDMI corruption.
- Protect HDMI signals from noisy signals.

Other comments and guidelines:

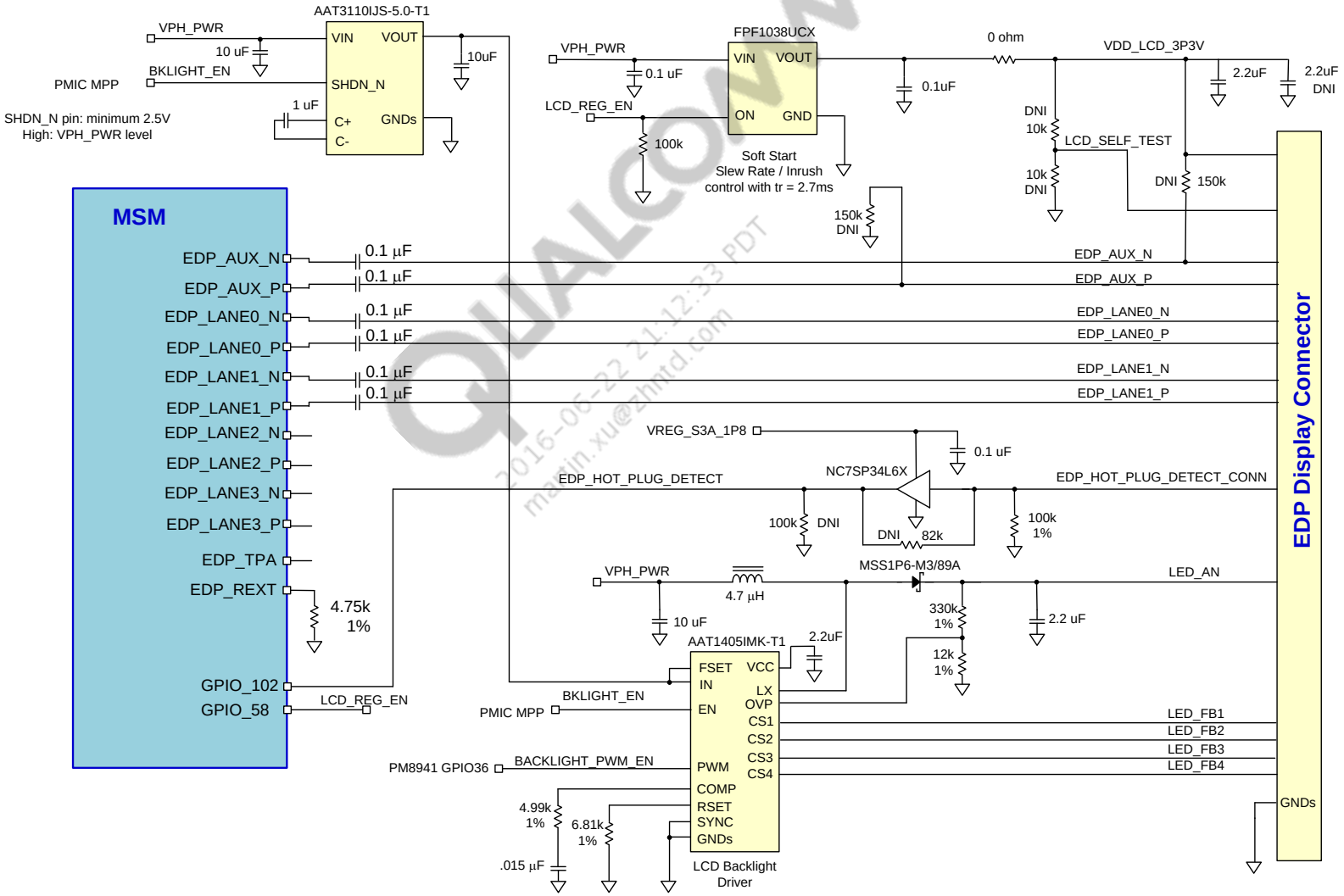
- 25 to 297 MHz clock; 2.97 Gbps data rate per channel
- Differential pairs, 100 Ω nominal, ±10%
- Spacing to all other signals = 4x line width
- TMDS data guidelines
  - Intra-pair length matching < 0.7mm (5ps)
  - Inter-pair length matching < 2mm (15ps)
  - Cross-talk isolation < 40 dB up to 1 GHz; < 30 dB up to 5 GHz
  - Lane-to-lane trace spacing = 3x line width
- TMDS clock guidelines
  - Intra-pair length matching < 0.7mm (5ps)
  - Inter-pair length matching < 2mm (15ps)
  - Cross-talk isolation < 40 dB up to 1 GHz; < 30 dB up to 5 GHz
  - Data-to-clock trace spacing = 3x line width
  - Source termination (differential) = 240 Ω integrated in PHY
- DDC and CEC guidelines
  - DDC max loading < 50 pF (excludes cable)
  - DDC-to-other trace spacing = 2x line width
  - CEC max loading < 200 pF (excludes cable)

Each trace needs to be adjacent to a ground plane; the recommended implementation uses layer 3 (green), next to layer 4 ground plane.



eDP – Schematic Diagram

eDP is used for large resolutions (24-bit 2560 ∗ 2048 @ 60 Hz).



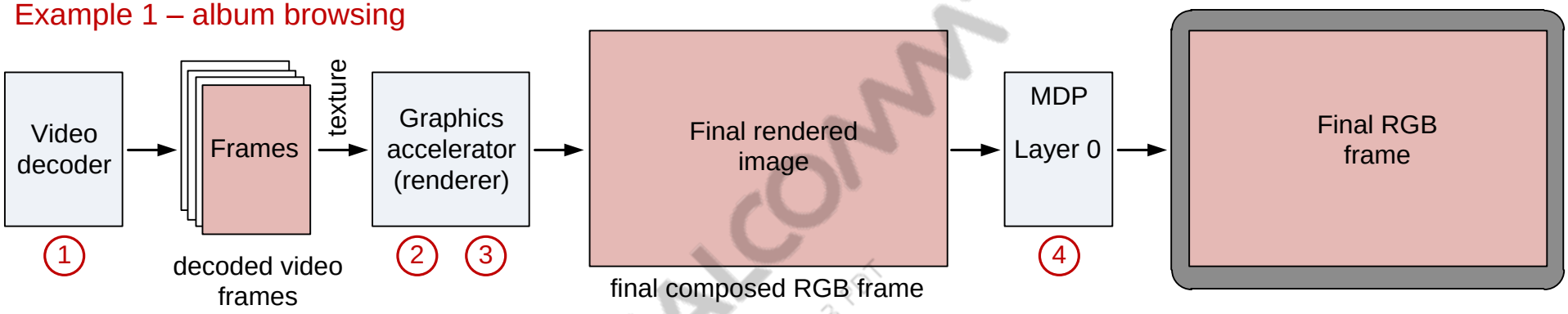
eDP – Layout Guidelines

In addition to the guidelines presented here, see the eDP specification v1.2.

- eDP signals are very high-speed.
- Protect sensitive signals from eDP corruption.
- Protect eDP signals from noisy signals.
- 2.7 Gbps data rate per lane
- Differential pairs, 100 Ω nominal, ±10%
- Total routing length < 305 mm
- ESD/EMI cap load < 1.5 ps
- AC coupling cap = 75–200 nF
- Main link guidelines:
  - Unit interval = 370 ps
  - Intra-pair skew < 1.5 ps, 0.2 mm
  - Inter-pair skew < 10 mm
- Aux link guidelines:
  - Unit interval = 400–600 ps
  - Intra-pair skew < 60 ps
  - Inter-pair skew < 10 mm

Example Display Uses (1 of 2)

Example 1 – album browsing



1) Video decoder generates video frames for album browsing.

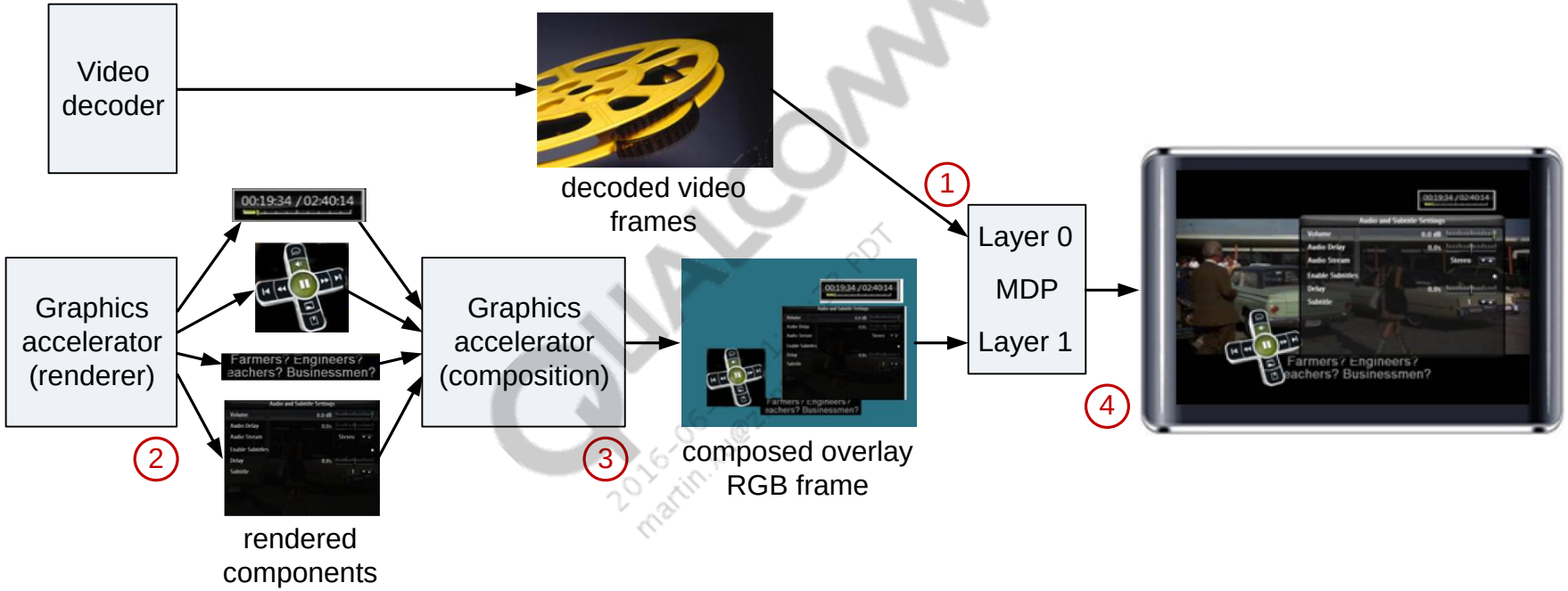
2) Graphics accelerator accepts video frames as texture.

3) Graphics accelerator composes final rendered image.

4) MDP sends final RGB frame to display.

Example Display Uses (2 of 2)

Example 2 – movie playback



1) MDP sends video frames directly to display (minimizes bus accesses).

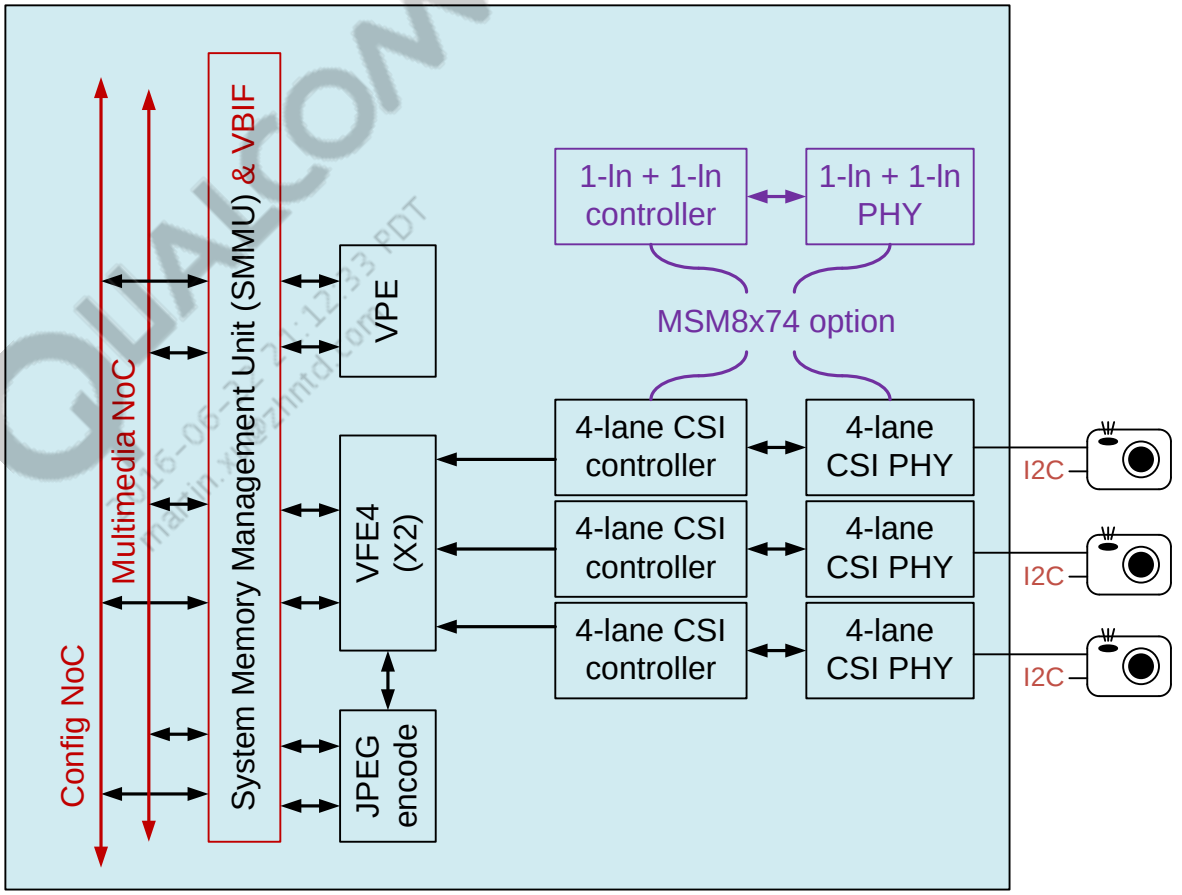
2) Graphics accelerator renders individual RGB overlay components.

3) Graphics accelerator composes all RGB overlay components into single frame.

4) RGB overlay frame is added on top of video frame as it is sent to display.

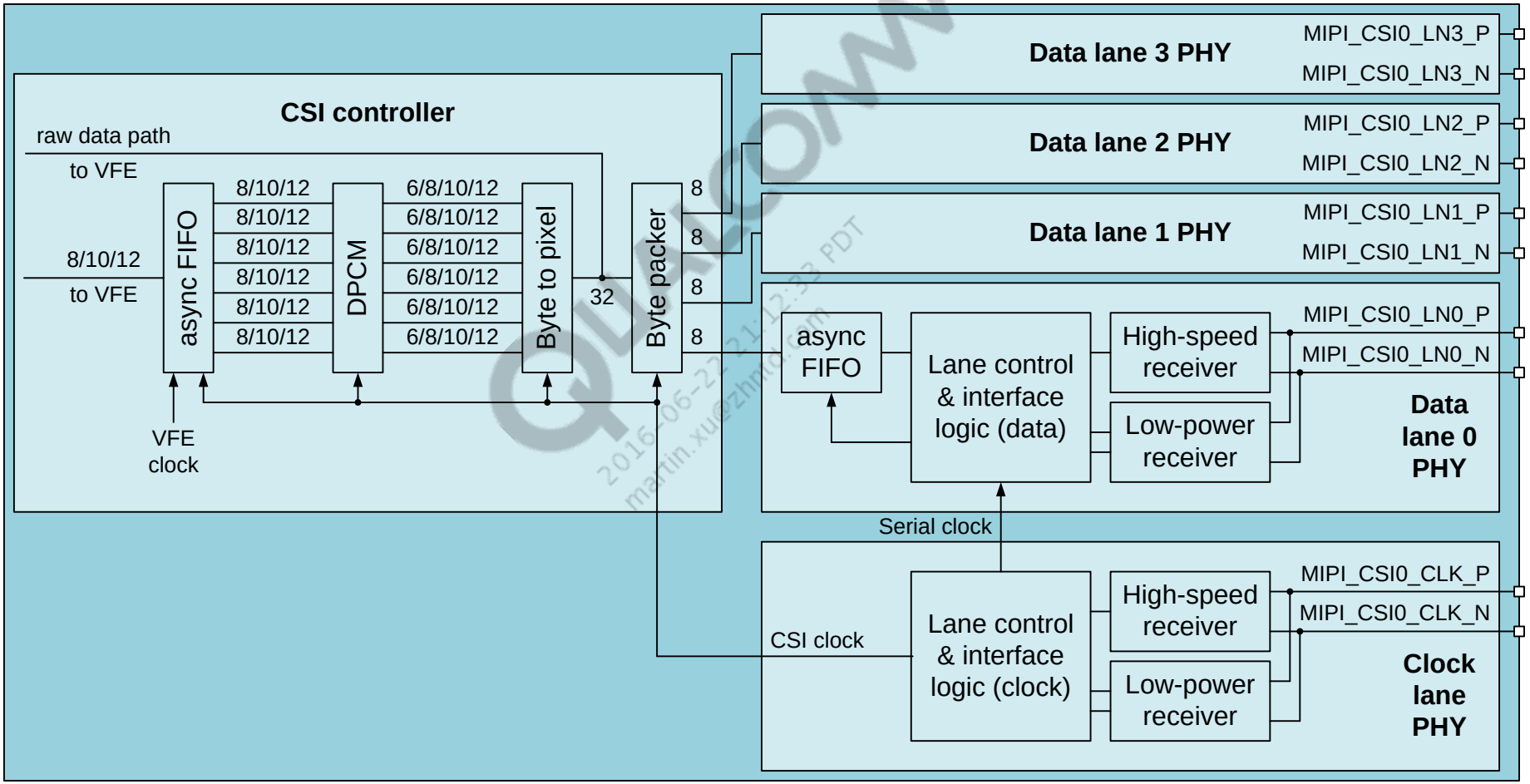
Image Processing Overview

- MIPI camera serial interface (CSI)
  - 4-lane plus 4-lane plus 4-lane
  - 4-lane plus 4-lane plus 1-lane plus 1-lane
  - 4-lane plus 4-lane plus 2-lane plus 1-lane
  - 4-lane plus 4-lane plus 2-lane
- Camera operation data flow examples
- Video front-end (VFE)
- JPEG
- VPE
- Image processing examples



MIPI Camera Serial Interfaces – Architecture

One 4-lane CSI shown here:

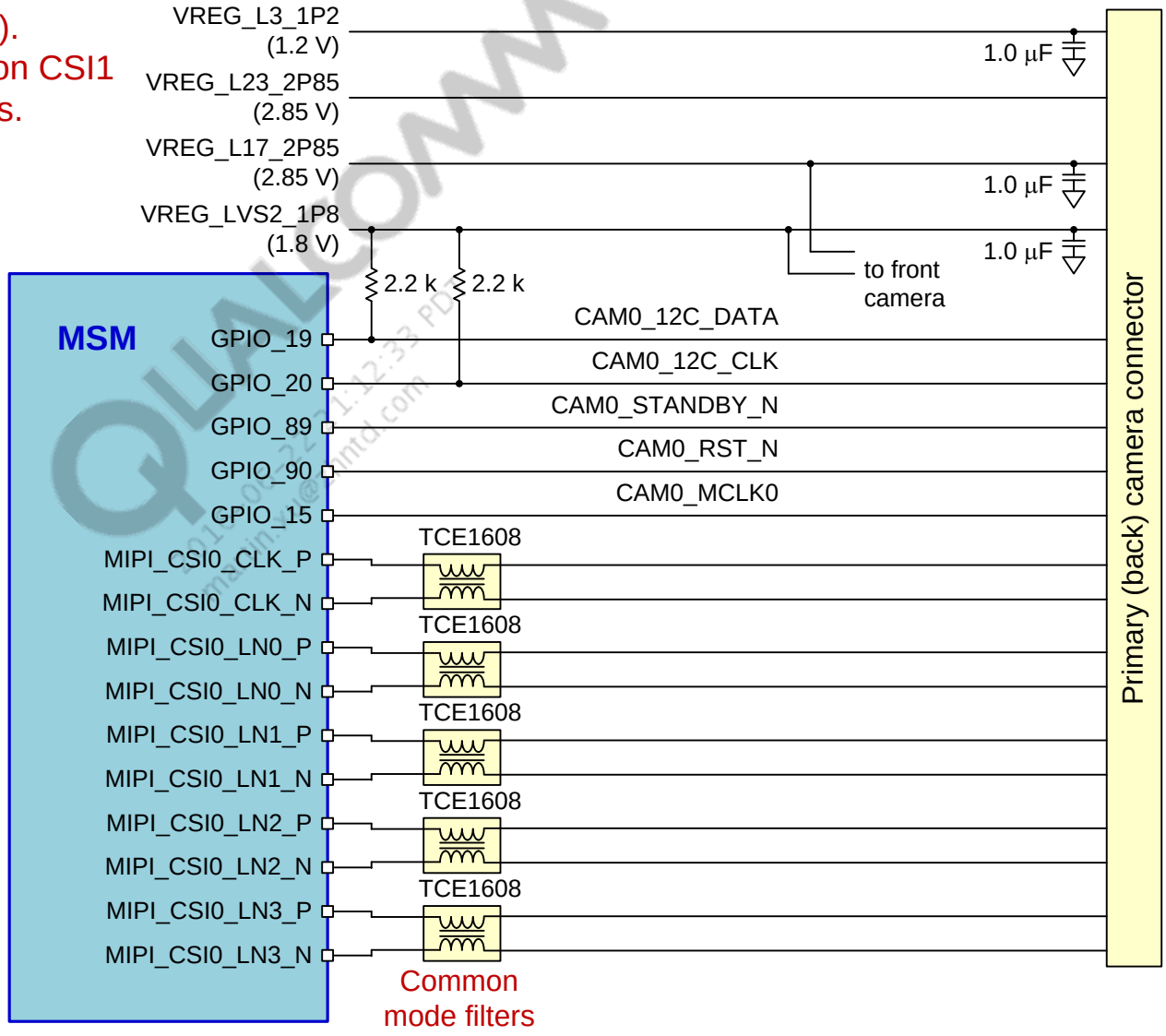


MIPI Camera Serial Interfaces – Features

- Per Mobile Industry Processor Interface (MIPI) specification
- One high-speed clock lane and one to four data lanes
- Low-voltage differential signaling (LVDS)
- PHY block provides physical interface to camera sensor
- Camera interfaces:
  - 4-lane plus 4-lane plus 4-lane
  - 4-lane plus 4-lane plus 1-lane plus 1-lane
  - 4-lane plus 4-lane plus 2-lane plus 1-lane
  - 4-lane plus 4-lane plus 2-lane
- Other characteristics:
  - Dual image signal processing (ISP) – 32 MP at 15 fps, 16 MP at 30 fps, and integrated S3D camera
  - 2D performance – 32 MP at 15 fps; 16 MP at 30 fps
  - Sensor input rate – 750 MHz
  - Sensor pixel depth – 8/10/12 bits per pixel
  - Supported input formats – Bayer RGB; YCbCr 4:2:2 interleaved; 12-8, 12-6, 10-8, 10-6 MIPI compression; 8/10/12 MIPI raw

MIPI Camera Serial Interfaces – Schematic Diagram (4-lane)

Primary camera (back) on reference design is CSI0 (shown below). Secondary camera (front) is on CSI1 and uses only 2 of the 4 lanes.



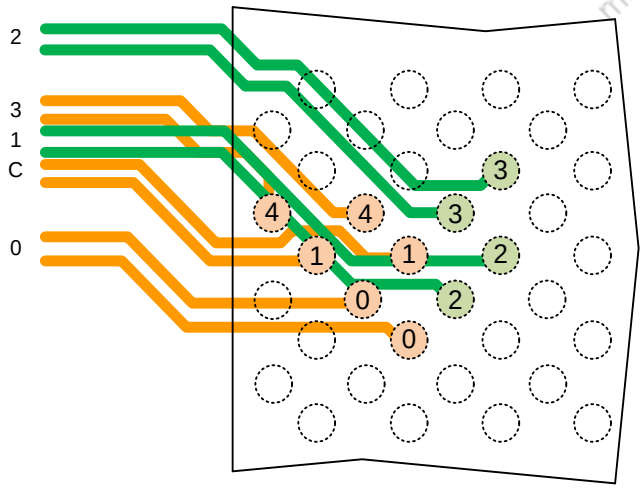
MIPI Camera Serial Interfaces – Layout Guidelines (4-lane Example)

In addition to the guidelines presented here, see the *MIPI Alliance Specification* for D-PHY; it has extensive inter-pair and intra-pair isolation requirements that must be met.

- CSI signals are very high-speed.
- Protect sensitive signals from DSI corruption.
- Protect CSI signals from noisy signals (clocks, SMPS, etc.).

- 750 MHz clock rate; 1.5 GHz data rate
- Differential pairs, 100 Ω nominal, ±10%
  - Flex cables also need 100 Ω nominal, ± 10%
- Total routing length < 305 mm
- Intra-pair length matching < 5 ps (0.67 mm)
- Clock – data length matching < 10 ps (1.3 mm)
- Lane-to-lane trace spacing = 3x line width
- Spacing to all other signals = 4x line width
- MCLK (from the GPIO) must be isolated from other signals, especially from the antennas

Other comments and guidelines



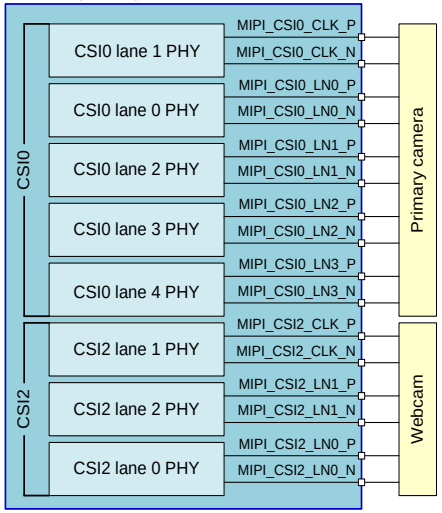
Each trace needs to be adjacent to a ground plane; the recommended implementation uses layer 2 (orange), next to layer 1 ground plane and layer 3 (green), next to layer 4 ground plane.

Broadside coupling occurs when traces on adjacent layers overlap or nearly overlap.

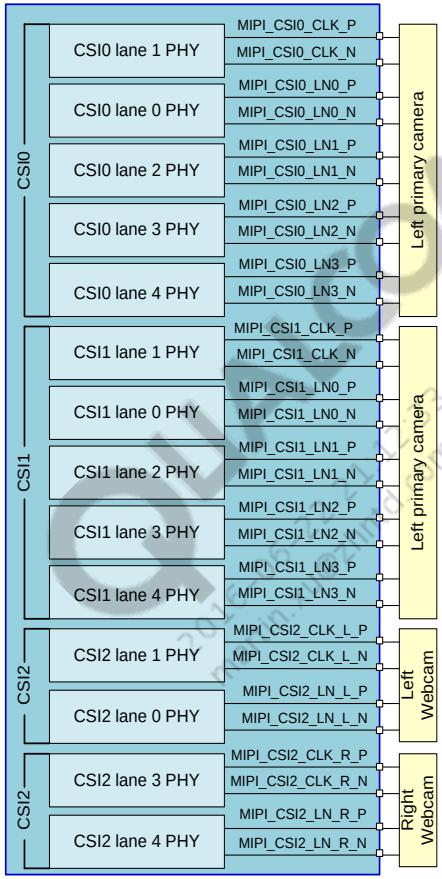
- This is unavoidable near MSM during breakout.
- But once routed away, force traces for each pair to separate from others to minimize coupling.

MSM8x74 MIPI CSI Flexibility

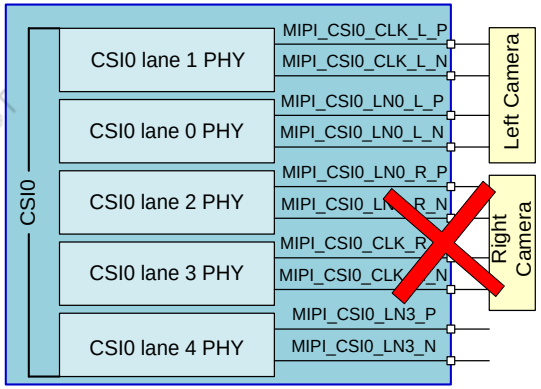
Application example 1:
4-lane primary camera + 2-lane webcam



Application example 2:
3D 4-lane primary camera + 3D 1-lane webcam

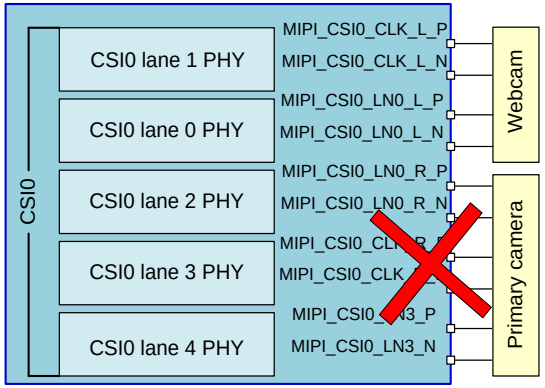


Invalid Configuration



When *lane 3* is being used as a clock, it can only be used with lane 4

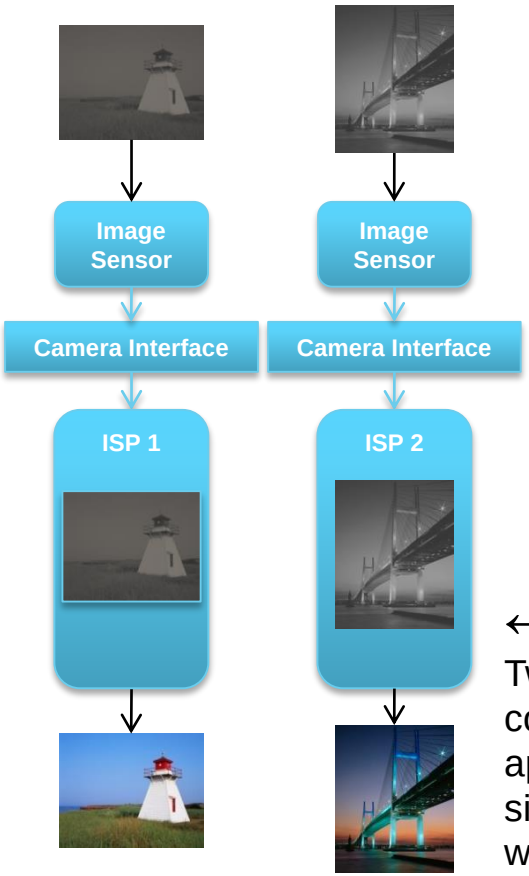
Invalid Configuration



Camera Details

Next gen camera solution: dual image signal processing (ISP)

- ISPs can be used in parallel for high throughput OR used individually for concurrent processing.
  - Single ISP capability ~266 MP/sec
  - Dual ISP up to 532 MP/sec throughput



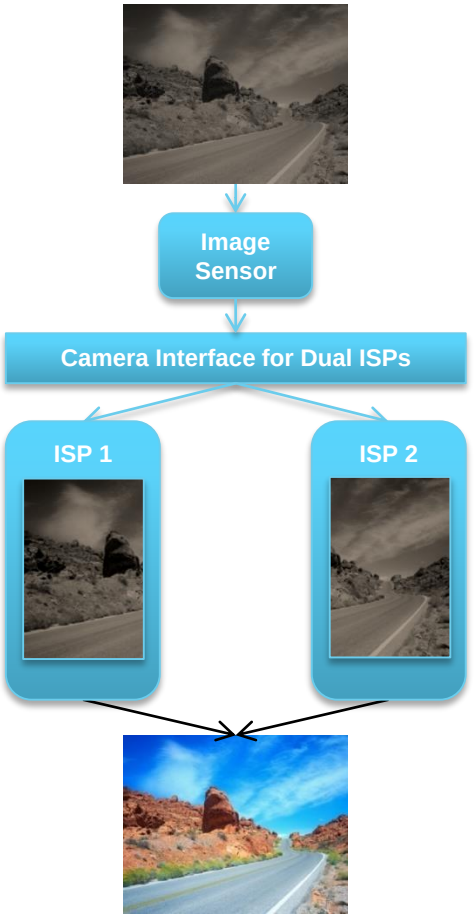
Dual ISP Modes	Description
Tandem	Two cameras in tandem providing simultaneous short/long exposures for HJR/HDR or focus positions for EDOF.
3D imaging	Two cameras in tandem providing stereo 3D.
Concurrent front / back cameras	Two cameras operating concurrently for simultaneous video telephony with camera.
High Performance	One camera using both ISP pipelines to support high megapixel sensors at high frame rates.

←

Two ISP pipelines for concurrent camera applications like simultaneous camera with video telephony.

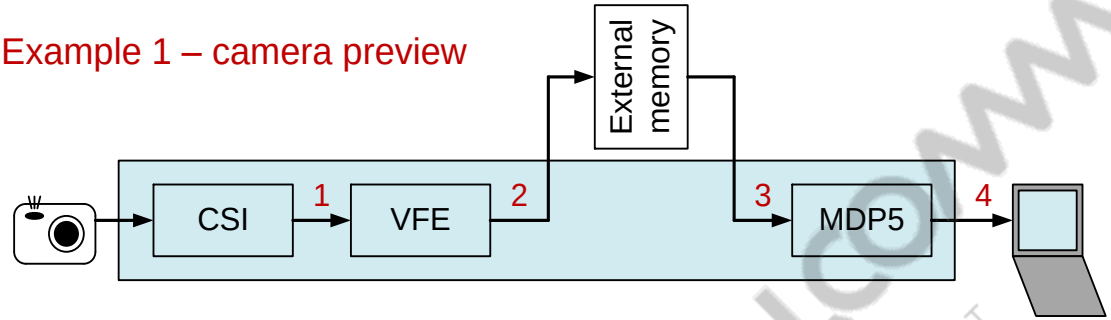
→

Two ISP pipelines for increased pixel processing throughput; Also supports much larger megapixels.

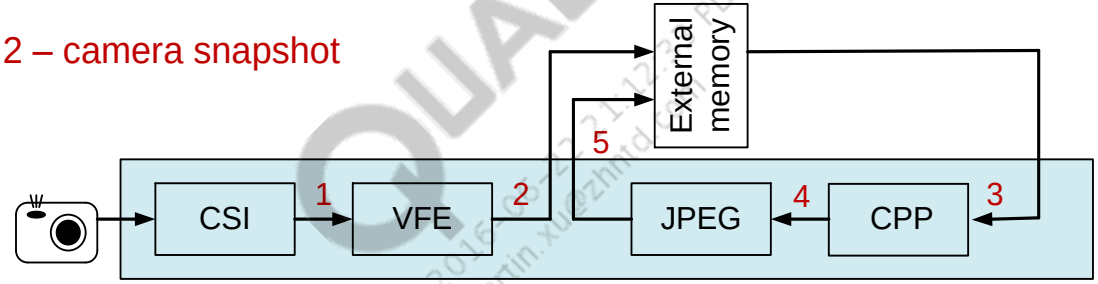


Camera Operation Data Flows

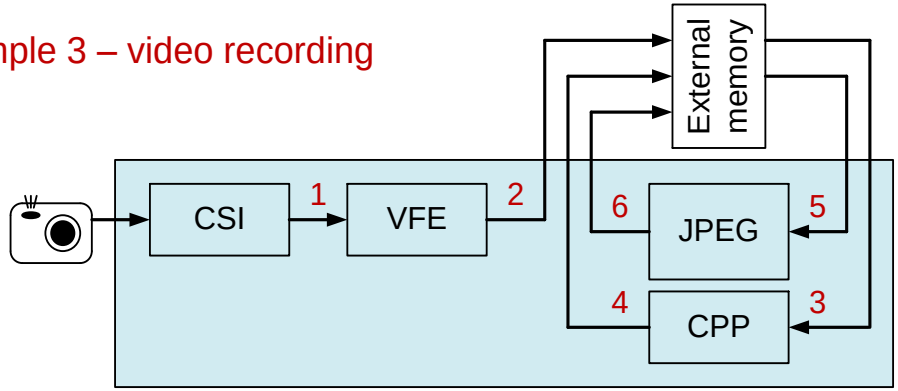
Example 1 – camera preview



Example 2 – camera snapshot



Example 3 – video recording



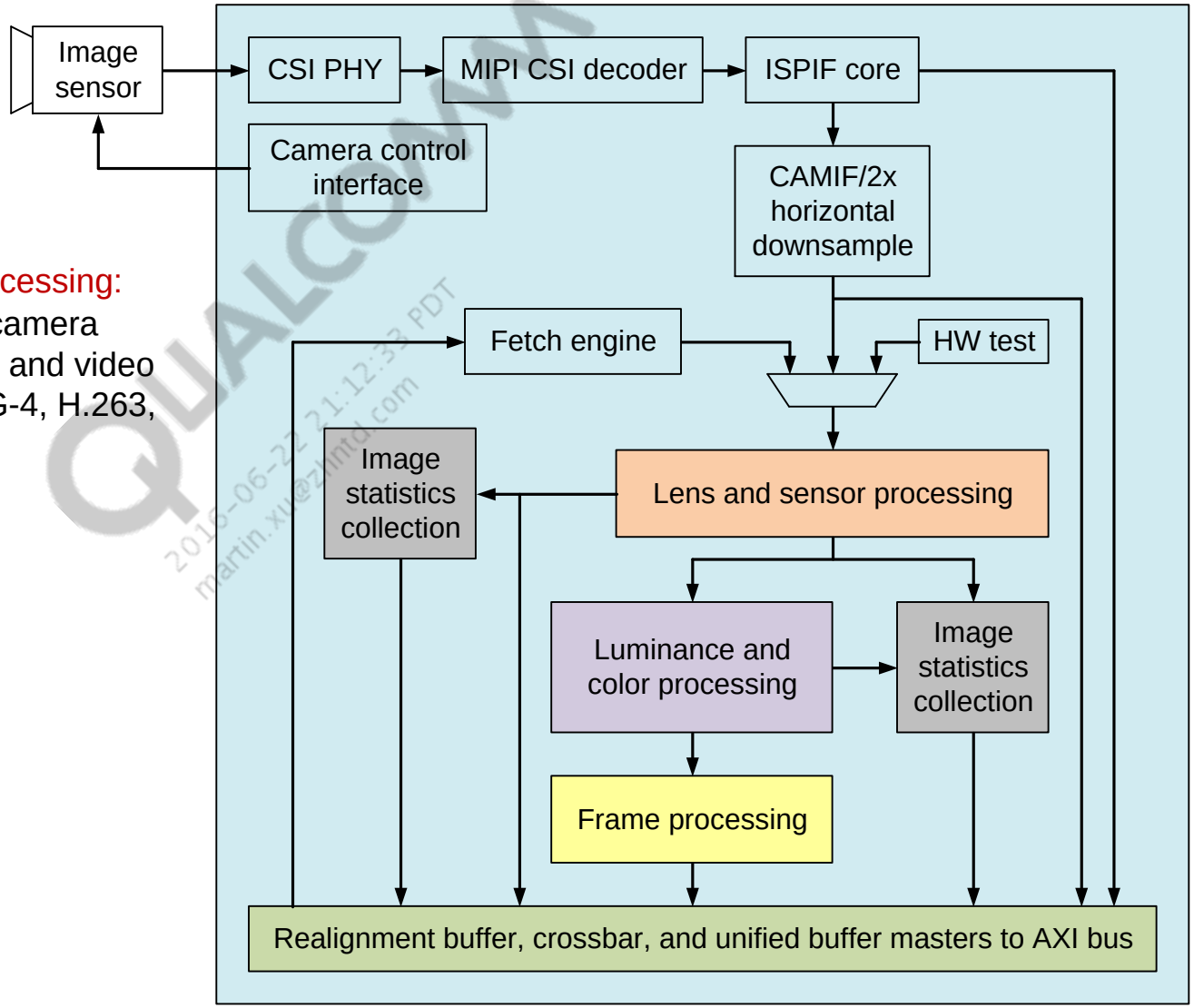
Processing details presented next:

- VFE
- JPEG
- VPE
- Camera Post Processor (CPP)

Video Front-end Architecture

Video front-end (VFE) image processing:

– A common interface between camera sensors and a variety of image and video compression standards (MPEG-4, H.263, & others).



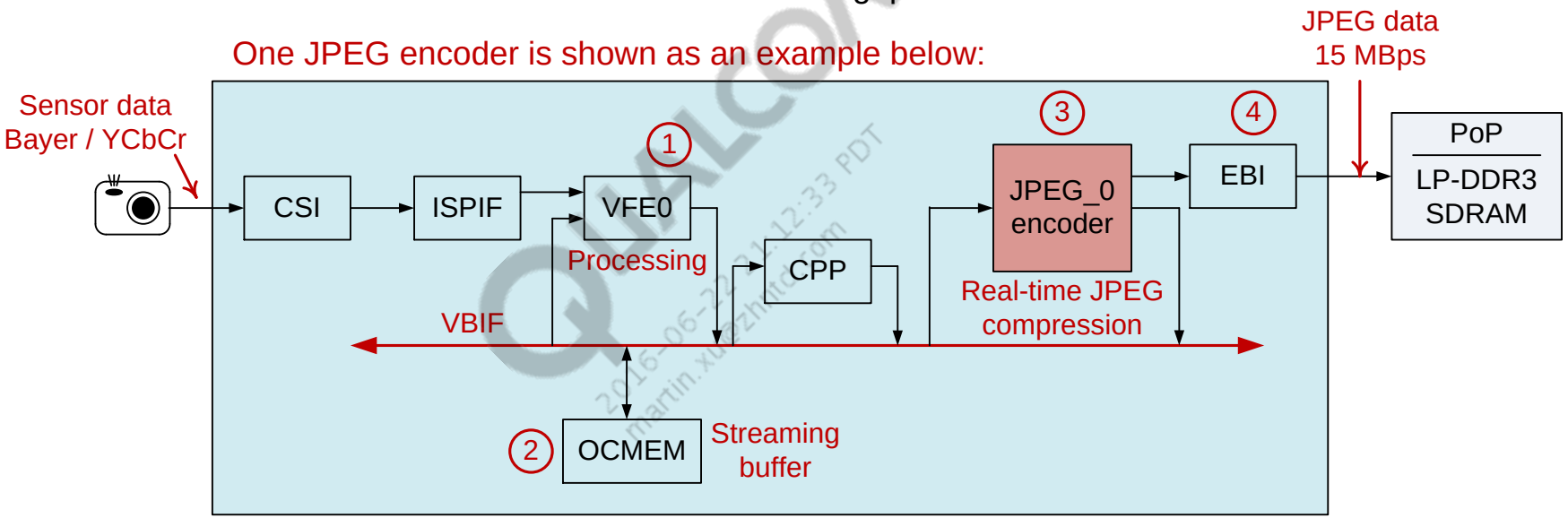
Video Front-end 4.0 Features

- Dedicated hardware blocks – like true DSC
- ISP mP runs at 266 MHz in normal mode and 320 MHz in high-clock mode
- Comprehensive adjustments throughout the entire image-processing pipe yields improved image quality according to user specification and preference
- High-resolution, flexible image statistics for accurate and robust AWB/AE/AF
- AWB/color-conversion statistics are collected and used to control VFE blocks
- AE/AF statistics for sensor compensation through I2C
- ISP bypass capability concurrent with full image-processing via direct memory dump to external memory for bandwidth-efficient offline processing

JPEG encoders:

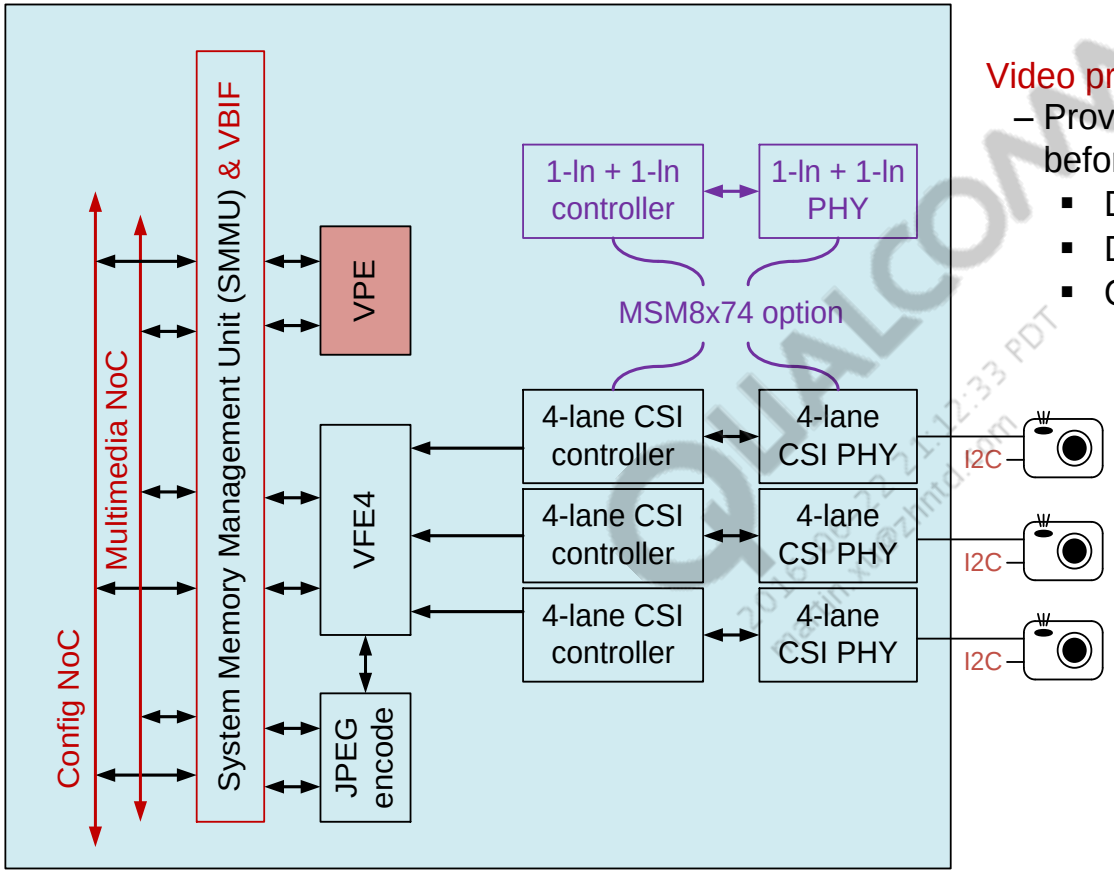
- Reduce latency; useful as a frame-based encoder for encoding rotated pictures and for frame-based processing
- Two JPEG encoders with 266 MP/s of throughput
- One JPEG decoder with 166 MP/s of throughput

One JPEG encoder is shown as an example below:



1) The VFE output is routed to on-chip memory (OCMEM).
   - The following mutually exclusive operations are supported:
     - Graphics, JPEG, and video codec.
2) OCMEM is used as a streaming buffer to temporarily queue the sensor data from the VFE.
   - OCMEM is supported in parallel with the EBI / LP-DDR3 accesses.
3) As the VFE fills the OCMEM buffer, the JPEG core is simultaneously reading data.
   - This data rate is different due to the removal of blanking areas.
4) The JPEG core outputs the encoded JPEG to an EBI buffer.
   - Estimated bandwidth is 15 MBps based upon a typical 10-to-1 compression ratio.

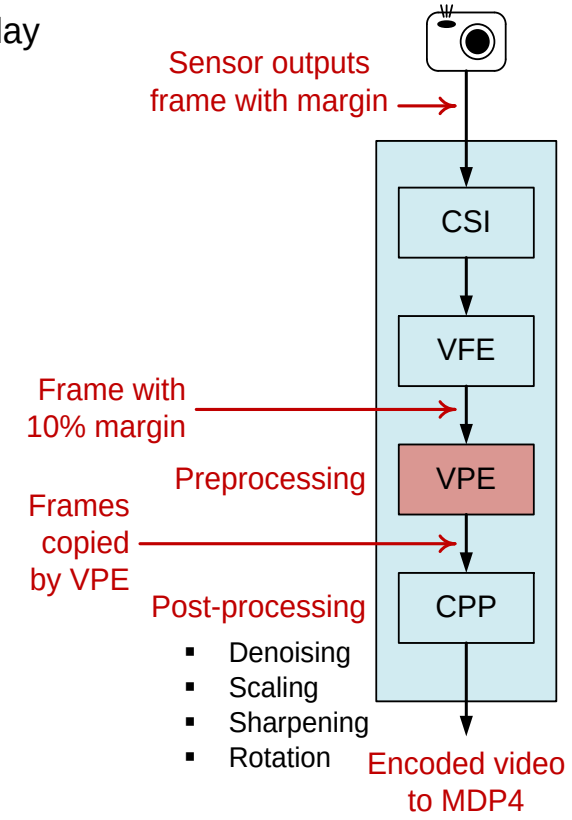
Video Preprocessing Engine



Video preprocessing engine (VPE)

– Provides processing in real-time before encoding, including:

- Digital image stabilization
- Digital zoom
- Overlay



MSM8x74 Image-Processing Capabilities

Features		MSM8974 capability
Preprocessing	Digital zoom	Up to 20x–continuous
	Rotation	90, 180, 270, mirroring
	Digital video stabilization	Yes (VFE statistics based)
	Deinterlacing	Yes
	Video path format (read, for VPE/Encoder)	NV12, NV21 (co-site and off-site) YCbCr 4 × 4 tiled format (pseudo-planar) VYUY, YVYU, UYVY, YUYV (YCbCr–4:2:2 Interleaved) RGB565, BGR565 RGB888, BGR888
	Down scaled output	Down to 1/8–continuous (NV12)
Post-processing	Error concealment	Yes (simple copy)
	Decoder output format	NV12, NV21 YCbCr 4 × 4 tiled format (pseudo-planar)
	Downscalar	Down to 1/8–continuous
Other	Multichannel support	Up to 8 with max frame rate of 240 combined performance of all channels up to 1080p 120 fps
	Transcoding	1080p 60 fps decode and encode

Video Comparison Summary

	MSM8974
Performance	1080p 120 fps decode/96 fps encode, 100 Mbps 4 k × 2 k 30 fps decode/24 fps encode (H.264 only) Up to 8 video instances, e.g. 2 × 1080p 60 fps 4 × 1080p 30 fps 8 × 720p 30 fps
Encoders (HW accelerated)	H.264 High MPEG-4 H.263 MVC VP8
Decoders (HW accelerated)	H.264 High MPEG-4 ASP VC-1 – All Profiles MPEG-2 Main H.263 MVC (1080p 30) VP8 Sorenson Spark
Preprocessing	Integrated to video core
Post-processing	Error concealment Downscaler

Note: The green text indicates enhancements to the MSM8974 from previous chipsets.

Graphics and Audio

Graphics – Adreno 330:

Performance improvements:

- Better shader performance – double-rate half-precision ALUs
- Better pixel performance and more graphics memory – supports higher resolutions and double pixel/texel throughput

Performance summary:

Parameter	MSM8x74 capability
Clock	450 MHz (3D)
Fill rate	3600 megapixels/seconds
Dedicated hardware for 2D	No
APIs provided	OpenGL ES 1.1 OpenGL ES 2.0 OpenGL ES 3.0 DirectX 9.3

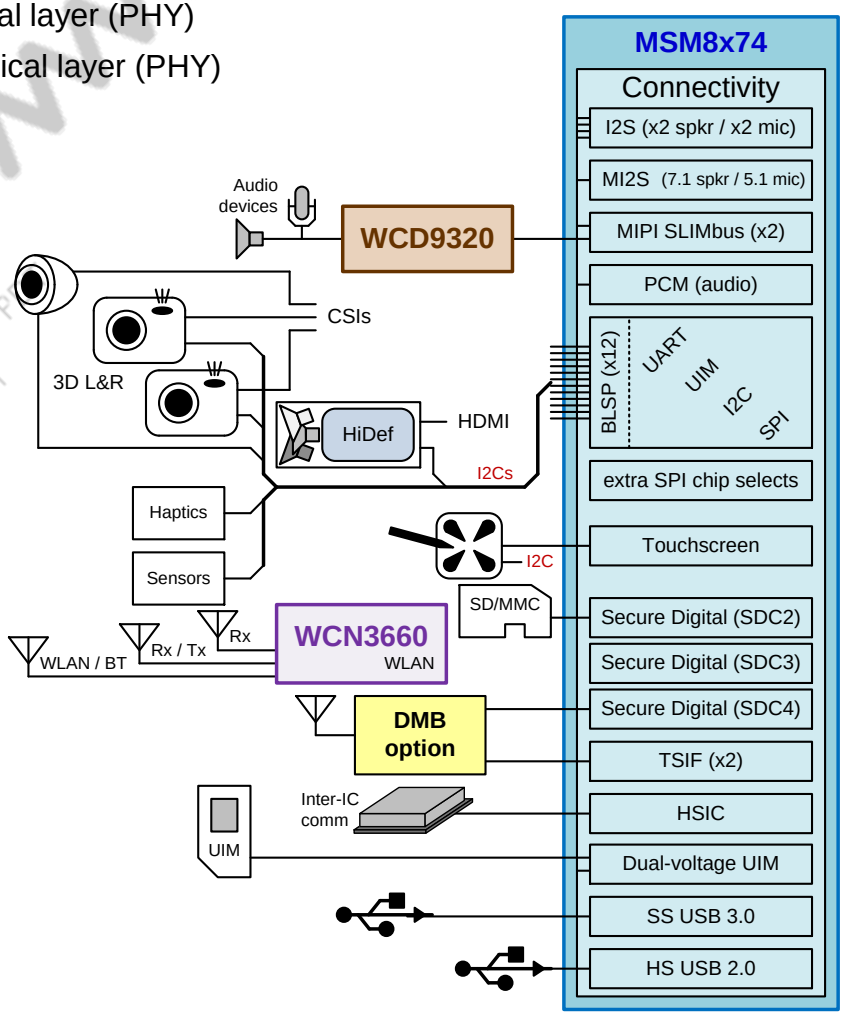
Audio: See the WCD9320 material.

Sec. 8

Connectivity

Connectivity Overview and Section Outline

- Dedicated connectivity ports:
  - Secure digital controllers 1 (used for eMMC – see *Memory Support* section) and 2
  - High-speed universal serial bus (HS-USB) with integrated physical layer (PHY)
  - Super- speed universal serial bus (SS-USB) with integrated physical layer (PHY)
- Via non-BLSP GPIOs:
  - Secure digital controllers 3 and 4
  - High-speed inter-chip (HSIC) bus interface
  - Transport Stream Interface (no details given)
  - Touchscreen (no details given)
  - Inter-IC sound (I2S) ports
  - MIPI SLIMbus audio
  - Pulse-code modulation (PCM) audio port
- Via BLSP ports (x12):
  - Universal asynchronous receiver transmitter (UART)
  - User identity module (UIM)
  - Inter-integrated circuit (I2C)
  - Serial peripheral interface (SPI)



Secure Digital Controller – Features

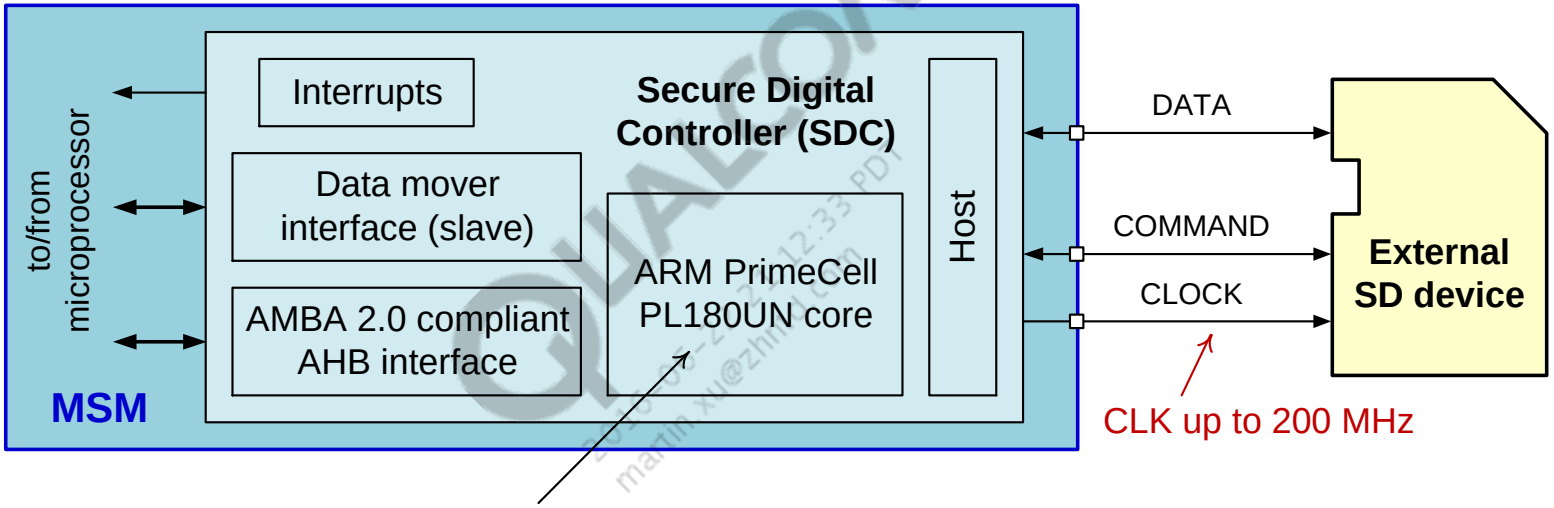
Up to four SD interfaces are available to provide the following features or functions:

- Clock output up to 200 MHz on SDC1 and SDC2; up to 100 MHz on the other interfaces
- 1.8 V/2.95 V dual-voltage operation on SDC2; 1.8 V operation on SDC1, SDC3, and SDC4
- Support for SDIO host mode
- SDIO compatible WLAN (802.11)
- Interface with SD/MMC memory cards up to 2 TB
- 10 kΩ pull-up resistor is required on the command pin for MMC/eMMC

SDC	Function	Width	Voltage	Max clock rate	Supported modes
1	eMMC	8 bits	1.8 V	200 MHz SDR* 50 MHz DDR 200MHz DDR*	DS, HS SDR, HS DDR, HS200*, HS400*
2	SD/MMC	4 bits	1.8 V/2.95 V	200 MHz SDR 50 MHz DDR	DS, HS, SDR12, SDR25, SDR50, SDR104, DDR50
3	WLAN	4 bits	1.8 V	100 MHz SDR 50 MHz DDR	SDR12, SDR25, DS, HS, SDR50, DDR50
4	DMB	4 bits	1.8 V	100 MHz SDR 50 MHz DDR	SDR12, SDR25, DS, HS, SDR50, DDR50

* MSM8x74 only: HS200 is configured to run at 200 MHz (default). However, this may exceed FMAX due to clock jitter. To avoid this, customers may elect to run at 171 MHz. Refer to *eMMC Clock (SDC1_CLK) in HS200 Mode Application Note* (80-NA437-19).
* MSM8x74AB only: HS200 and HS400 are configured to run at 192 MHz (default) to avoid exceeding FMAX due to clock jitter. However, customers may elect to run at 200 MHz if they choose.
* HS400 mode is only supported on MSM8x74AB.

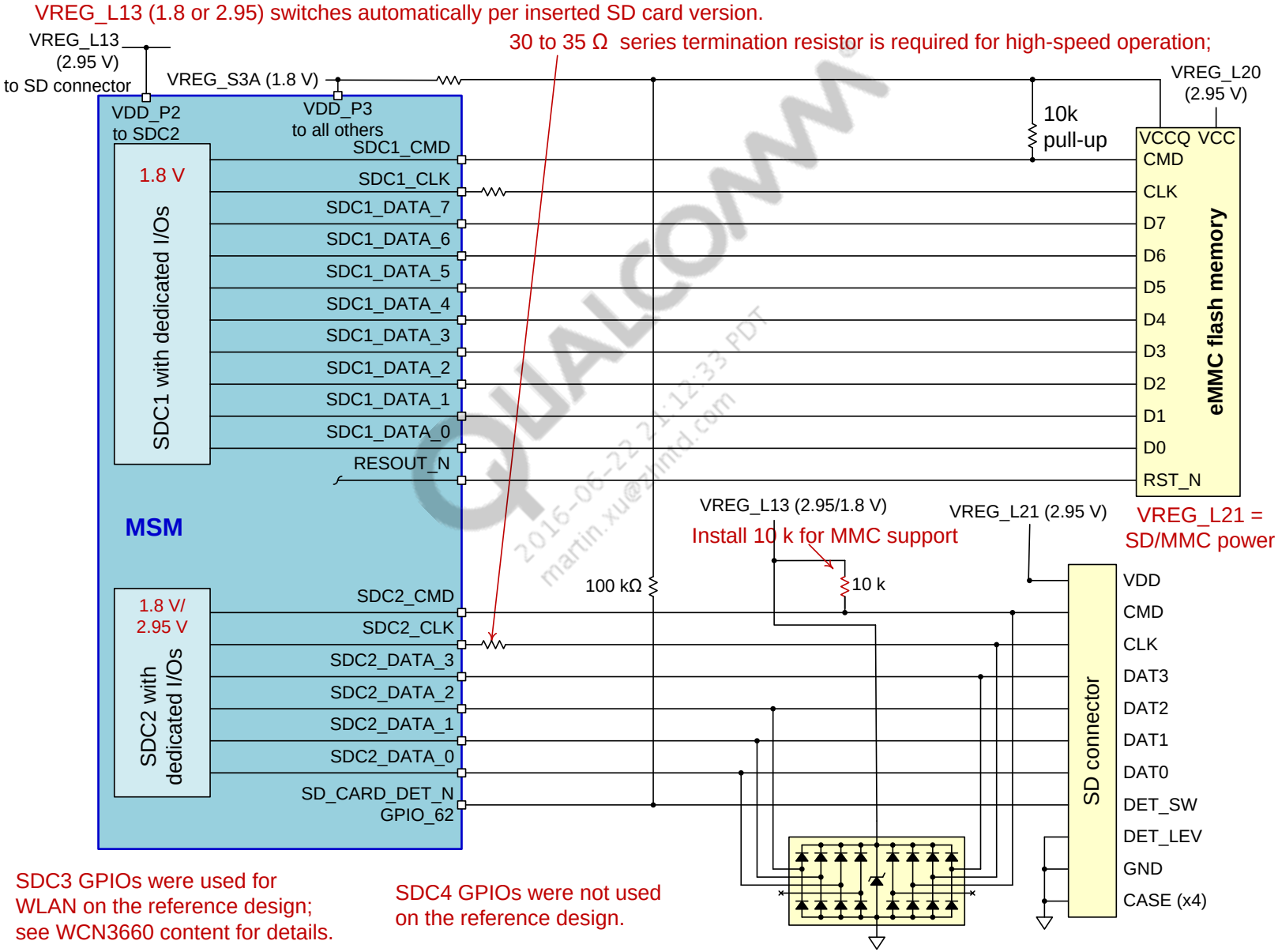
Secure Digital Controller – Architecture



PL180 core provides de-serialization of data, and buffering between the SD card and the applications subsystem. Features include:

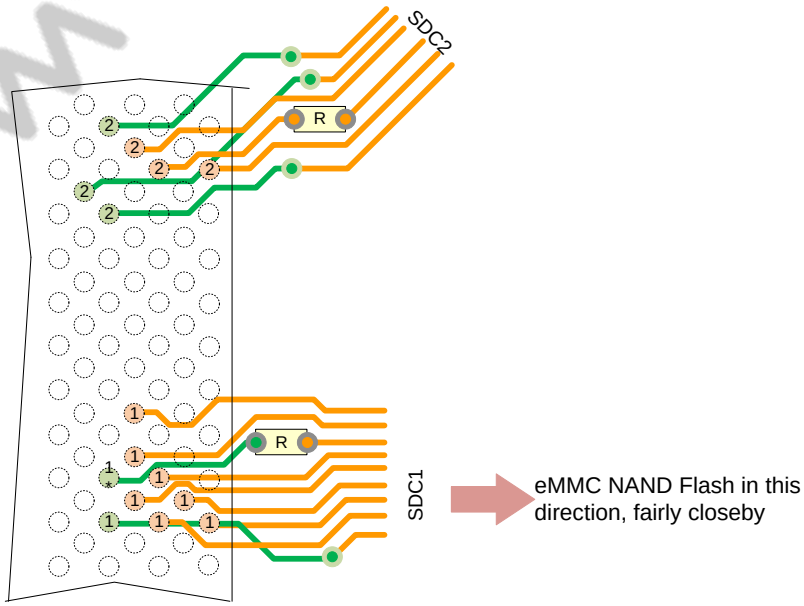
- Flow control – clock stopping when the apps subsystem is not able to keep up with the SD bus.
- SDIO support – primarily passing interrupts from the SDIO device to the processor.
- DM interface and support – a rate-controlled request / acknowledge interface for the data mover.

Secure Digital Controller – Schematic Diagram



SDC1 and SDC2 – Layout Guidelines (1 of 2)

- SDC1 and SDC2 signals are very high-speed.
  - Protect other sensitive signals/circuits from SDC corruption.
  - Protect SDC signals from noisy signals (clocks, SMPS, etc.).
- Other comments and guidelines:
  - Up to 200 MHz clock rate; SDC1 has up to 200 Mbps data rate for MSM8x74 and up to 400 Mbps data rate for MSM8x74AB
  - 50 Ω nominal, ±10% trace impedance
  - Total routing length < 50 mm recommended
  - CLK to DATA/CMD length matching < 1 mm
  - 30~35 Ω termination resistor on SDC2 clock line near the MSM device
  - Routing distance from the MSM clock pin to termination resistor < 5 mm
  - Spacing to all other signals = 2x line width
  - Loading capacitance < 14 pF
  - VDD_PX7 (SDC1 pad power) and VDD_PX2 (SDC2 pad power) loop inductance < 3 nH
  - Place no stub for test points or external pull-up resistors on SDC1/2 signals



SDC1 and SDC2 – Layout Guidelines (2 of 2)

MSM8x74 SDC1 with eMMC4.5 devices:

1. SDC1_CLK drive strength = 16 mA
2. OVERRIDE_0* software register = 0x0 (default, no writes required)
3. SDC1_CLK termination resistor = 33 Ω ±5%
4. Loading capacitance = 8 pF board + 6 pF load = 14 pF (maximum)

MSM8x74AB SDC1 with eMMC4.5/eMMC5.0 devices:

1. SDC1_CLK drive strength =16 mA

2A. OVERRIDE_0* software register = 0x0; for HS200 (default, no writes required)

2B. OVERRIDE_0* software register = 0x3; for HS400 (one-time-writeable register per power cycle)

3. SDC1_CLK termination resistor = 24 Ω ±1%
4. Loading capacitance = 8 pF board + 6 pF load = 14 pF (max)

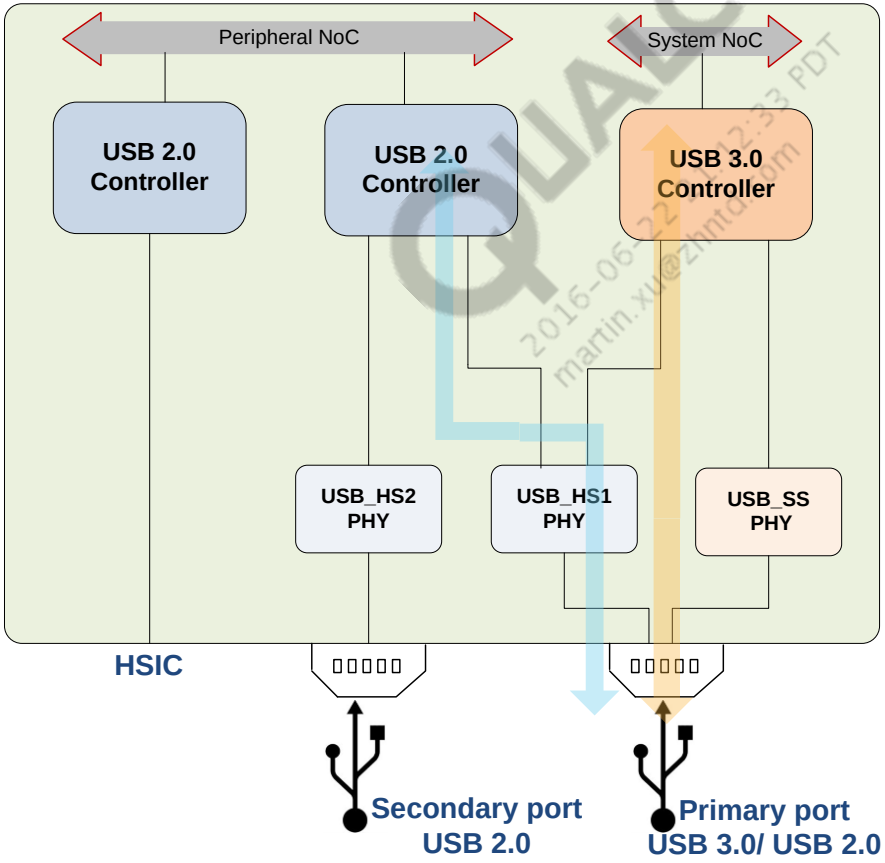
* OVERRIDE_0= 0xFC4BE0B0 SECURITY_CONTROL_CORE_OVERRIDE_0 bits1:0

Note: The above recommendation is based on worst case, with loading capacitance = 14 pF. Customer designs with smaller loading capacitance may use a different termination resistor value and a smaller drive strength.

USB

MSM8974 has two USB ports; one USB 3.0 port and one USB 2.0 port.

- The primary USB is a USB 3.0 port.
  - USB 3.0 is a combination of high-speed (USB_HS1) PHY and super-speed (USB_SS) PHY.
  - Either a USB 3.0 cable or USB 2.0 cable can be used with this port.
    - The USB 3.0 controller can also be used for USB 2.0 mode.
- The secondary USB is a USB 2.0 port (USB_HS2).



indicates the data flow for:

- Emergency boot
- *Debugging using QTI tools, such as QPST/QXDM ,etc.
- *Flashing boot code
- *RAM dumps

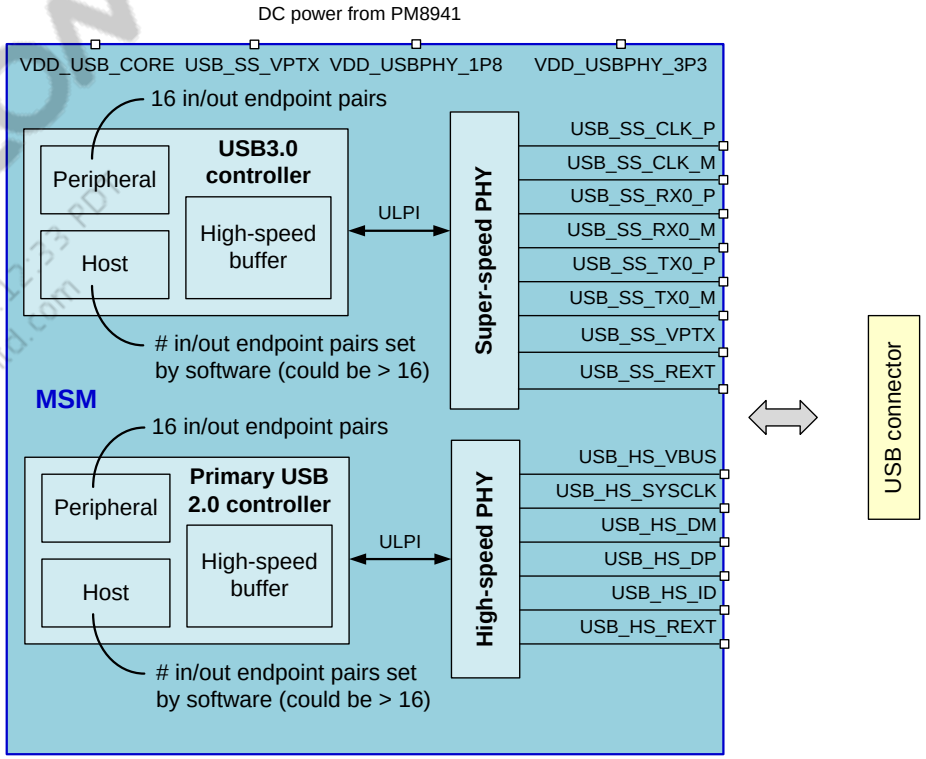
** Until USB 3.0 SW support available*

indicates the data flow for:

- Primary USB port for all other uses cases used in both USB 3.0 and USB 2.0 mode

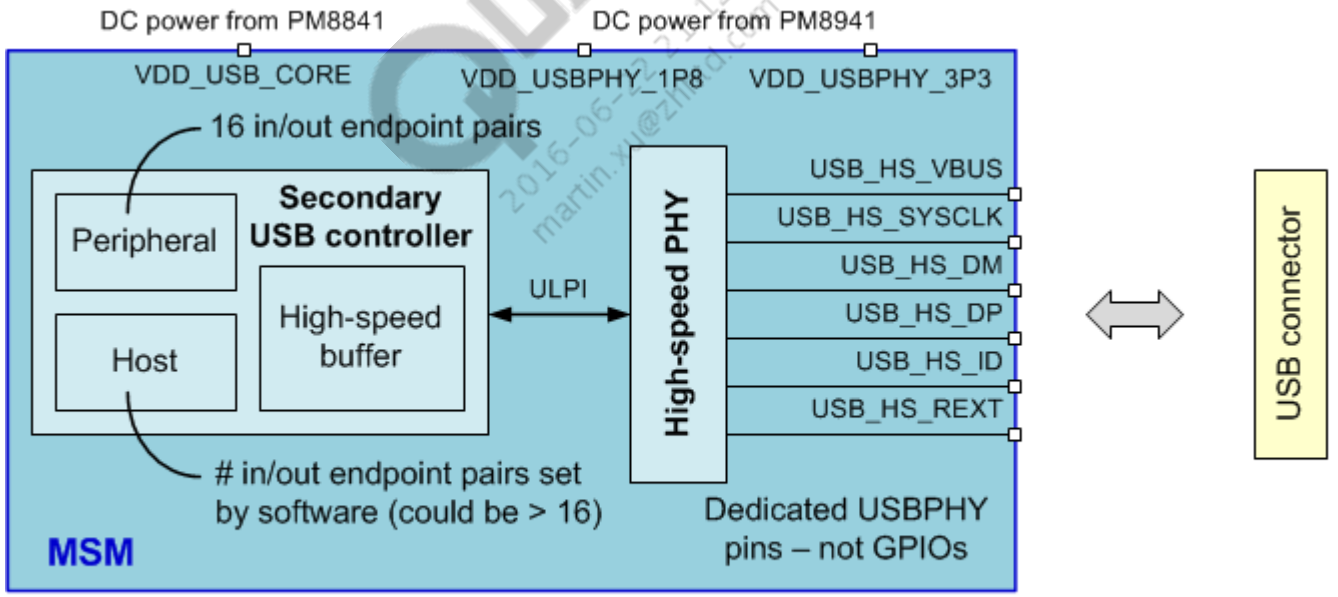
USB 3.0 SS-USB with PHY – Architecture and Features

- SS-USB port with an integrated physical layer (PHY):
  - Capable of supporting USB operations at super-speed.
  - Additional USB information is available at www.usb.org/developers/.
- HS-USB port with an integrated physical layer (PHY):
  - Also capable of supporting USB operations at low-speed and full-speed.
  - Additional USB information is available at www.usb.org/developers/.
- Supported applications:
  - Debugging using QTI tools
  - Flashing boot code
  - Emergency boot over HS1 interface
  - Charging using integrated OVP of PMIC



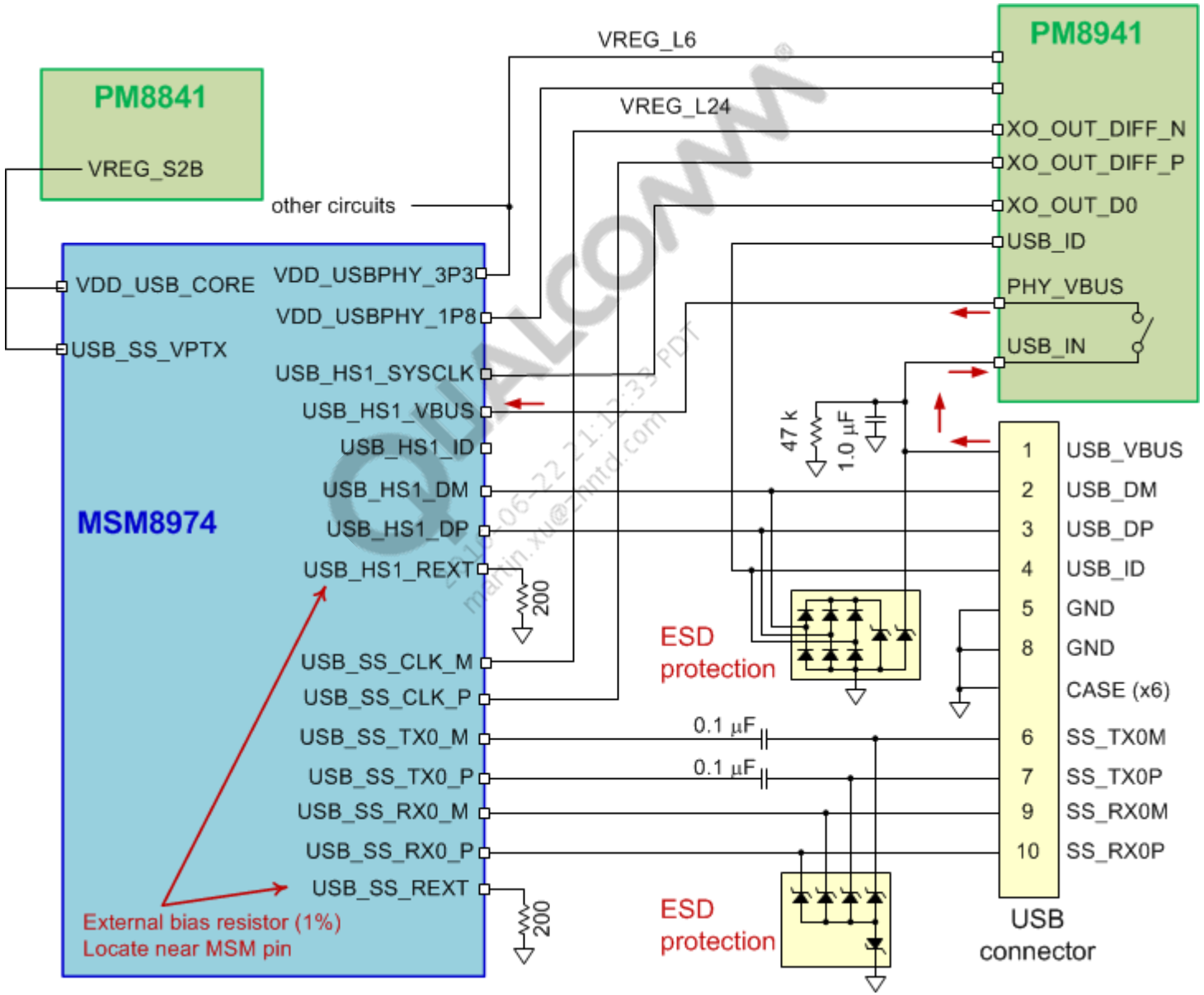
USB 2.0 HS-USB with PHY – Architecture and Features

- HS-USB port with an integrated physical layer (PHY):
  - Also capable of supporting USB operations at low-speed and full-speed.
  - Additional USB information is available at www.usb.org/developers/.
- Supported applications:
  - Peripheral mode – mass storage; MTP for music and video content transfers, CDC/ACM for modem; CDC/ECM for data services; CDC/OBEX for NMEA and diagnostic, SICD for PictBridge
  - Host mode – HID supporting keyboard, mouse and gamepad controller connectivity; mass storage supporting USB flash drive and HDD connectivity
  - Charging will require external OVP circuit



Each host or peripheral endpoint can be configured for control, interrupt, or bulk. Isochronous endpoints are supported in hardware, but have not been used by software applications.

SS-USB and HS-USB with PHY – Schematic Diagram



SS-USB and HS-USB with PHY– Layout Guidelines (1 of 2)

HS-USB guidelines:

- Up to 480 Mbps data rate
- 90 Ω differential, ± 10% trace impedance
- Trace delay < 4 ns
- Data jitter = 60 ps
- Differential data pair matching < 6.6 mm (50 ps)

SS-USB guidelines:

- Up to 5 Gbps data rate
- 90 Ω differential, ± 15% Ω trace impedance
  (Note: Flex cables and board-to-board connectors can have an impact on signal integrity.)
- AC coupling capacitor – 75–200 nF
- Tx differential pair length matching < 5 mil (0.127 mm)
- Rx differential pair length matching < 5 mil (0.127 mm)
- AC coupling capacitor should be placed away from the MSM. This is to ensure signal integrity of the long stripline USB super-speed Tx signals. Once coming to the surface (top/bottom layer), place the AC cap as close to the via as possible
- Tx and Rx differential pair maximum length is recommended to be less than 6 inches
- If third-party components are required for signal improvement, place them closer to the USB connector
- Route DIFFCLK signals with 100 Ω ± 10% Ω differential trace impedance. They should have a matched length < 100 mil (2.5 mm)
- Maintain good isolation between USB3.0 connector and RF antennas (especially 2.4 GHz)
- Route the RF signals operating at 2.4 GHz frequency to have the highest isolation possible from USB_SS_TX/RX traces
- Route USB_SS_TX/RX in the inner layers and do not add test point or common mode filters on the USB_SS_TX/RX signals
- USB_SS_TX0_P/M and USB_SS_RX0_P/M differential pairs must have GND isolation from other adjacent traces
  - The minimum width of the GND trace must be 2x the width of the USB 3.0 traces
- It is recommend not to share the vias of decoupling capacitors USB1_VBUS with any other decoupling/filtering cap

SS-USB and HS-USB with PHY– Layout Guidelines (2 of 2)

Other comments and guidelines:

- External components should be located near the USB connector.
- Relatively fast edge rates, so they should be routed away from sensitive circuits and signals (RF, audio, and 19.2 MHz XO).
- If USB connector is used as charger input:
  - USB_VBUS node must be routed to the PMIC using extremely wide traces or sub-planes.
  - Detailed recommendations are provided in the *PMIC* training.
- Even if the USB connector is not used for charging, USB_VBUS can be used as the power bus for the USB. This trace width must be sized depending on the length of VBUS and the expected current.
  - USB peripheral currents will be about 200 mA.
- Please refer to *Application Note: Tuning the 28 nm USB Phy Eye Diagram and Receiver Sensitivity* (80-NA648-1) for information regarding eye diagram tuning by software.

Terminating Unused USB Pins

If both SS and HS on USB port 1 are not used

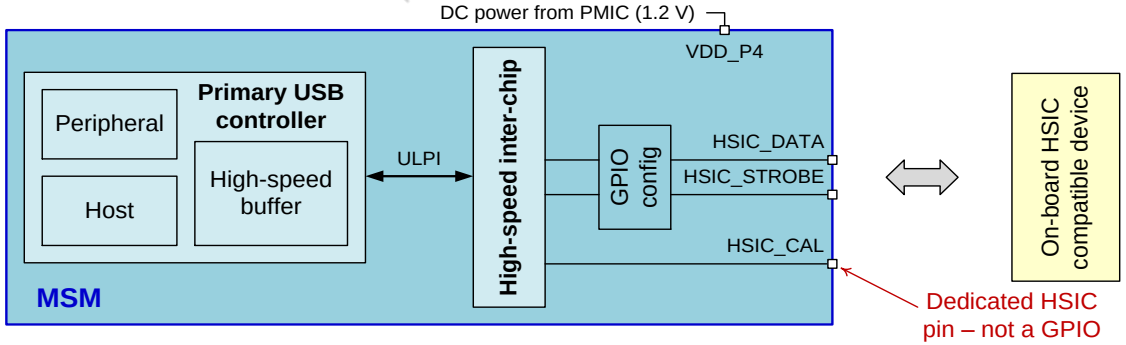
If SS on USB port 1 is not used, but HS1 is used

If USB port 2 is not used

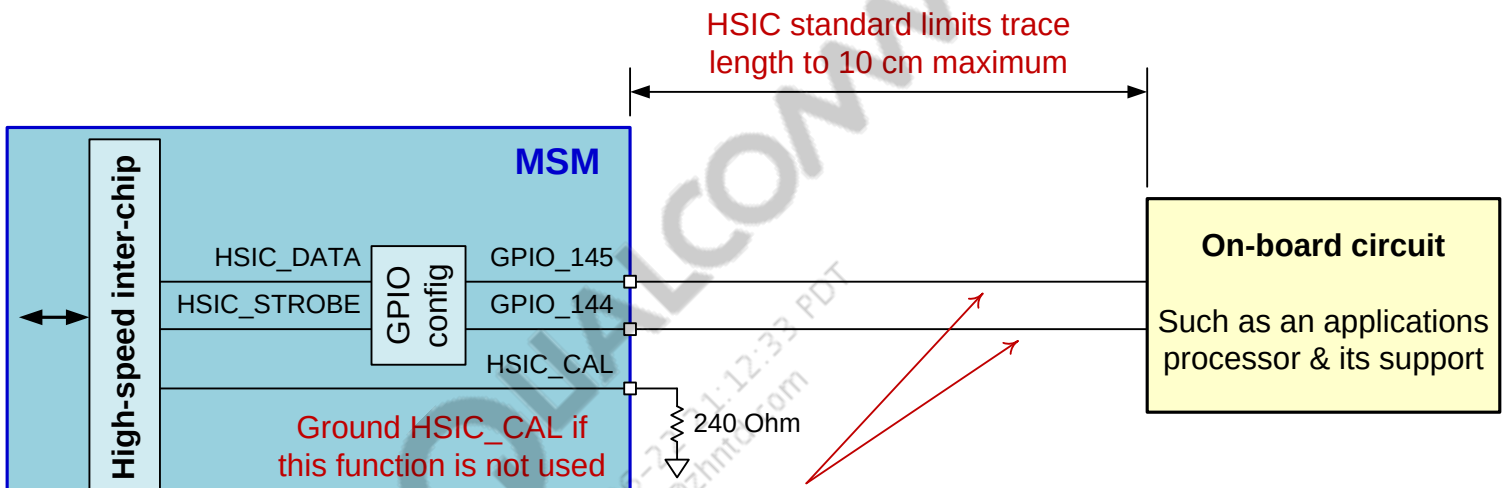
Signal	Unused pin state
USB SS	
USB_SS_CLK_M	Floating
USB_SS_CLK_P	Floating
USB_SS_RX0_M	Floating
USB_SS_RX0_P	Floating
USB_SS_TX0_M	Floating
USB_SS_TX0_P	Floating
USB_SS_REXT	Floating
VDD_USB_CORE (0.9 V) – pin J5	Connected to power supply
VDD_USB_1P8 (1.8 V) – pin K4	Connected to power supply
USB_SS_VPTX (0.9 V) – pin L7	Connected to power supply
USB HS1	
USB_HS1_DP	Floating
USB_HS1_DM	Floating
USB_HS1_ID	Floating
USB_HS1_SYSCLK	Floating
USB_HS1_VBUS	Floating
USB_HS1_REXT	Floating
VDD_USB_3P3 – pin J1	GND
VDD_USB_1P8 – pin F2	GND
VDD_USB_CORE – pin F6	Connected to power supply
USB SS not used but HS1 used	
USB_SS_CLK_M	CONNECT to DIFFCLK_M pin of PM8941 if USB3.0 controller is used; floating if USB2.0 controller is used
USB_SS_CLK_P	CONNECT to DIFFCLK_P pin of PM8941 if USB3.0 controller is used; floating if USB2.0 controller is used
USB_SS_RX0_M	Floating
USB_SS_RX0_P	Floating
USB_SS_TX0_M	Floating
USB_SS_TX0_P	Floating
USB_SS_REXT	200 Ω ±1% installed
VDD_USB_CORE (0.9 V) – pin J5	Connected to power supply
VDD_USB_1P8 (1.8 V) – pin K4	Connected to power supply
USB_SS_VPTX (0.9 V) – pin L7	Connected to power supply
USB_HS2	
VDD_USB_3P3 – pin R3	GND
VDD_USB_1P8 – pin P4	GND
VDD_USB_CORE – pin T4	GND
USB_HS2_DP	Floating
USB_HS2_DM	Floating
USB_HS2_ID	Floating
USB_HS2_SYSCLK	Floating
USB_HS2_VBUS	Floating
USB_HS2_REXT	Floating

HSIC – Architecture and Features

- The USB interface is designed to drive up to 5 meters of cable, so it is overkill for on-board, inter-chip connections. The high-speed inter-chip (HSIC) interface was created to supplement the USB 2.0 specification and better serve chip-to-chip uses.
- Characteristics:
  - Two lines (strobe and data).
  - Source-synchronous serial interface
  - 240 MHz DDR signaling provides a 480 Mbps interface
  - 1.2 V LVCMOS logic levels
  - Both lines are bidirectional with non-return-to-zero inverted (NRZI) encoding
- Additional information is available in the *High-Speed Inter-Chip Supplement* to the *USB 2.0 Specification* from www.usb.org/developers/.



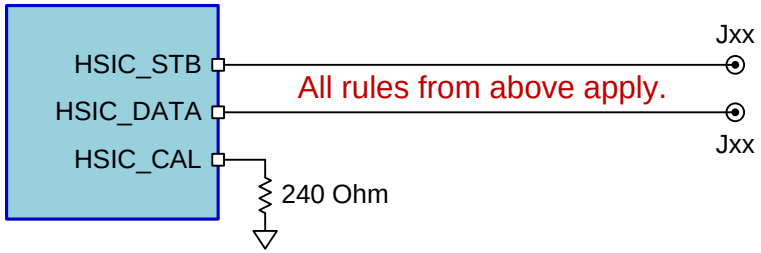
HSIC – Schematic Diagram and Layout Guidelines



50-ohm controlled-impedance routing (microstrip and/or stripline)

- Do not allow stubs on external traces (minimizes signal reflections).
- Single-ended traces must be matched length.
- Maintain isolation between the data and strobe lines – they do not form a differential signal.

Test considerations

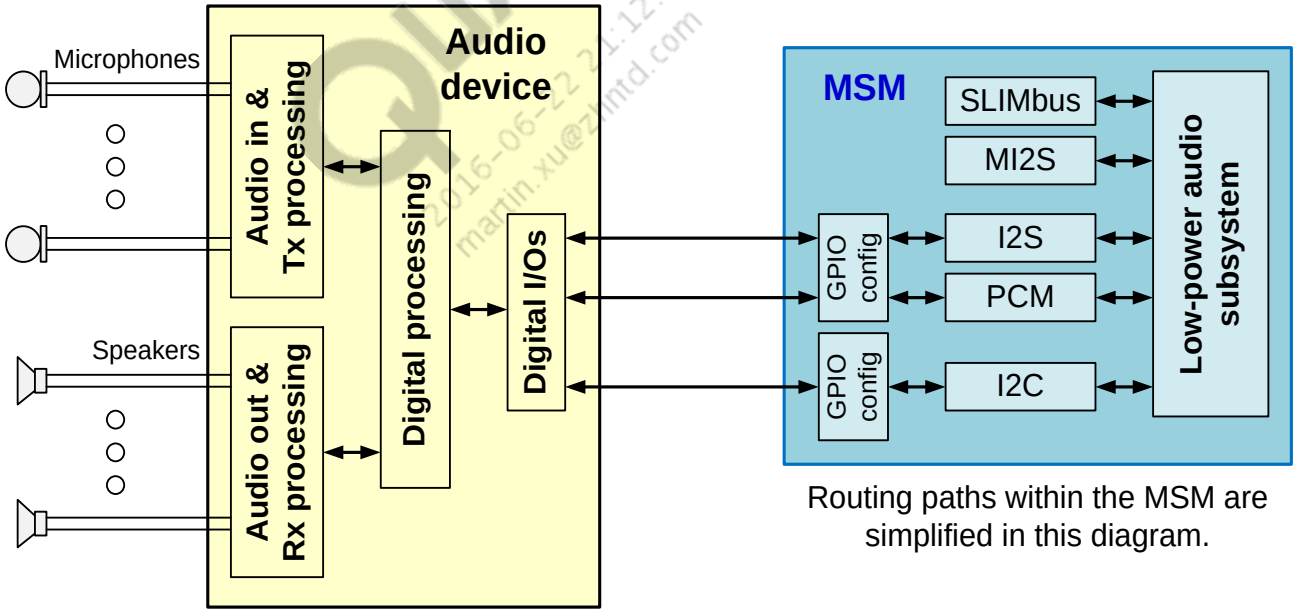


Additional test comments:

- Boards should use exposed traces or zero-ohm resistors to allow probing of the signal for test/debug measurements.
- The measurement point for a transmitter source should be at the far end (receiver load); measuring at the transmitter can introduce significant reflections.
- In a test environment, an RF connector should be used to connect HSIC circuits on separate boards.
  – MMCX-type is recommended (cable availability and durability).

I2S and PCM Introduction

- Audio data could be transferred back and forth (Rx and Tx) using legacy digital audio interfaces.
  - Inter-IC sound (I2S) ports
  - Pulse-code modulation (PCM) audio ports
- Digital microphones are supported only by using the WCD9320 IC.
- See the audio/WCD9320 content for more details.

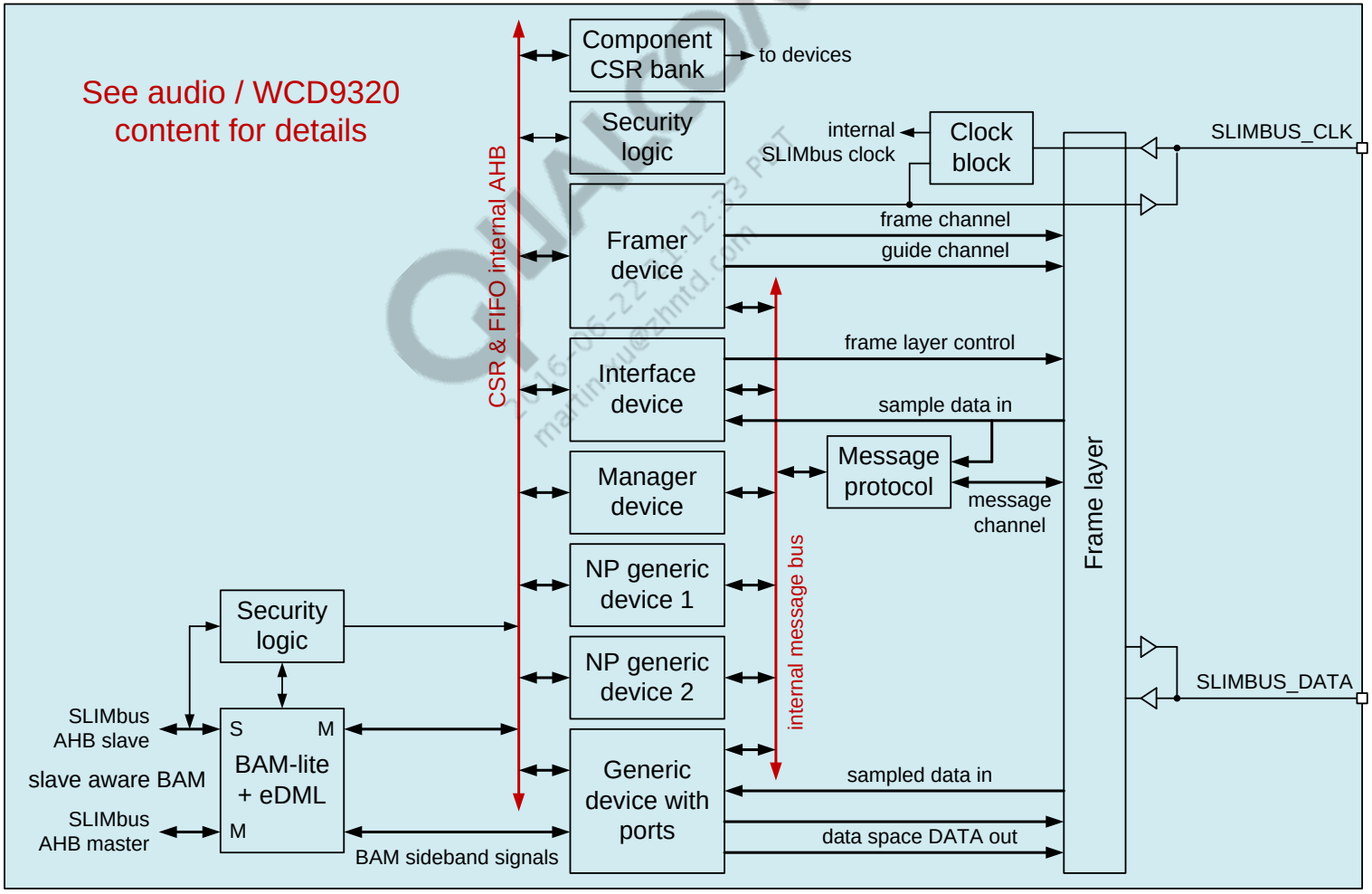


Routing paths within the MSM are simplified in this diagram.

SLIMbus Introduction (1 of 2)

Serial low-power inter-chip media bus (SLIMbus):

- 2-wire, multi-drop interface supports wide range of digital audio and control solutions for mobile terminals.
- Defined by the MIPI Alliance.
- External framer mode is not supported.



SLIMbus Introduction (2 of 2)

- SLIMbus features:
  - Audio, data, and control on single bus
  - Lower pin count
  - Supports 10+ components at typical bus lengths and speeds
  - Supports multiple high-quality audio channels
  - Multiple concurrent sample rates on one bus
  - Efficient peer-to-peer communications
  - Standardized message set
  - Improved software reuse
  - Increased interoperability
  - Dynamic clock rates for optimizing power; maximum SLIMbus clock = 28.8 MHz
- Architecture comments:
  - Manager device – configures and manages the SLIMbus under SW command.
  - Framer device – generates the SLIMbus clock and the framing and guide channels.
  - Generic ported devices – allows data transfers between host system and SLIMbus devices.
  - Generic non-ported devices – allows secure, independent access of different Execution Environments (EE) to the message channel.
  - EE to EE messaging through SLIMbus.
  - BAM interface – allows interchange of data and messages between the SLIMbus Component and the host system.
  - SLIMbus component supports a maximum of 24 concurrent data flows and allows access of up to 3 EEs to the SLIMbus resource.
- SLIMbus layout guideline
  - Keep at least 3x trace width between SLIMBUS_DATA and SLIMBUS_CLK, and at least 3x trace width between SLIMbus traces and other signal traces also to avoid cross-talk.

BLSP Overview

12 bus access manager (BAM) based low-speed peripheral (BLSP) interface ports are available.

Each is four bits wide – BLSPx_[3:0].

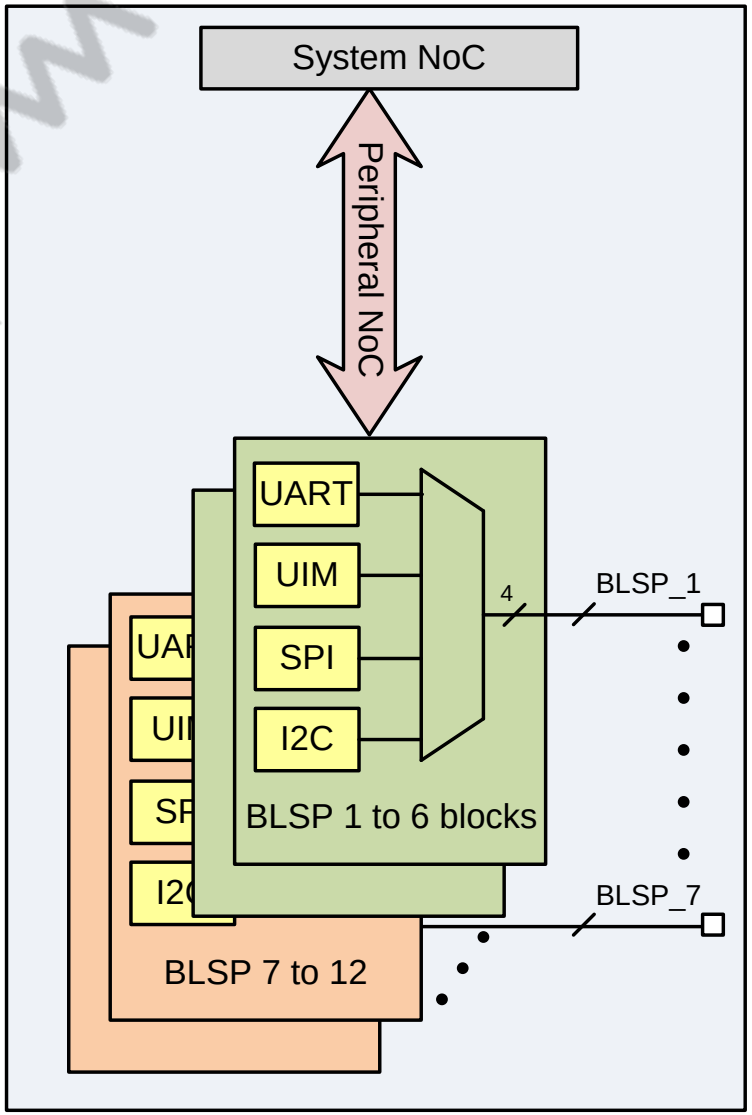
Each BLSP can support the following serial bus protocols:

- UART
- UIM
- SPI
- I2C

BLSPs are implemented within the peripheral subsystem.

BLSP (BAM low speed peripheral)

- Multiple SPI, I2C (QUP core), and UART cores are controlled using one BAM-lite instance.
- Simpler SW control:
  - SW only sets up transfers; the BAM moves data in/out of the slow peripheral devices.



BLSP Configurations

Option	Configuration	BLSP bit 3	BLSP bit 2	BLSP bit 1	BLSP bit 0
	BLSP1 GPIO pins =	GPIO_0	GPIO_1	GPIO_2	GPIO_3
	BLSP2 GPIO pins =	GPIO_4	GPIO_5	GPIO_6	GPIO_7
	BLSP3 GPIO pins =	GPIO_8	GPIO_9	GPIO_10	GPIO_11
	BLSP4 GPIO pins =	GPIO_19	GPIO_20	GPIO_21	GPIO_22
	BLSP5 GPIO pins =	GPIO_23	GPIO_24	GPIO_25	GPIO_26
	BLSP6 GPIO pins =	GPIO_27	GPIO_28	GPIO_29	GPIO_30
	BLSP7 GPIO pins =	GPIO_41	GPIO_42	GPIO_43	GPIO_44
	BLSP8 GPIO pins =	GPIO_45	GPIO_46	GPIO_47	GPIO_48
	BLSP9 GPIO pins =	GPIO_49	GPIO_50	GPIO_51	GPIO_52
	BLSP10 GPIO pins =	GPIO_53	GPIO_54	GPIO_55	GPIO_56
	BLSP11 GPIO pins =	GPIO_81	GPIO_82	GPIO_83	GPIO_84
	BLSP12 GPIO pins =	GPIO_85	GPIO_86	GPIO_87	GPIO_88
1	4-pin UART	UART_TX DO 4-pin UART transmit data	UART_RX DI 4-pin UART receive data	UART_CTS_N DI 4-pin UART clear-to-send	UART_RFR_N DO 4-pin UART ready-for-receive
2	2-pin UART + 2-pin I2C	UART_TX DO 2-pin UART transmit data	UART_RX DI 2-pin UART receive data	I2C_SDA B I2C serial data	I2C_SCL B I2C serial clock
3	4-pin SPI	SPI_DATA_MOSI B 4-pin SPI master out/slave in	SPI_DATA_MISO B 4-pin SPI master in/slave out	SPI_CS_N B 4-pin SPI chip select	SPI_CLK B 4-pin SPI clock
4	2-pin UIM + 2-pin I2C	UIM_DATA B UIM data	UIM_CLK DO UIM clock	I2C_SDA B I2C serial data	I2C_SCL B I2C serial clock
5	2-pin UIM + 2 GPIO	UIM_DATA B UIM data	UIM_CLK DO UIM clock	GPIO_XX B Configurable I/O	GPIO_XX B Configurable I/O
6	2-pin I2C + 2 GPIOs	GPIO_XX B Configurable I/O	GPIO_XX B Configurable I/O	I2C_SDA B I2C serial data	I2C_SCL B I2C serial clock
7	4 GPIOs	GPIO_XX B Configurable I/O	GPIO_XX B Configurable I/O	GPIO_XX B Configurable I/O	GPIO_XX B Configurable I/O
8	2-pin UART + 2 GPIOs	UART_TX DO 2-pin UART transmit data	UART_RX DI 2-pin UART receive data	GPIO_XX B Configurable I/O	GPIO_XX B Configurable I/O
		Note: The three rows within shaded cells are: 1) pad function; 2) pad type; and 3) functional description.			

BLSP ADM CRCI Sharing

In any BLSP, the SPI and I2C share same FIFO/ ADM CRCI interface and UART/UIM share same FIFO and ADM CRCI interface.

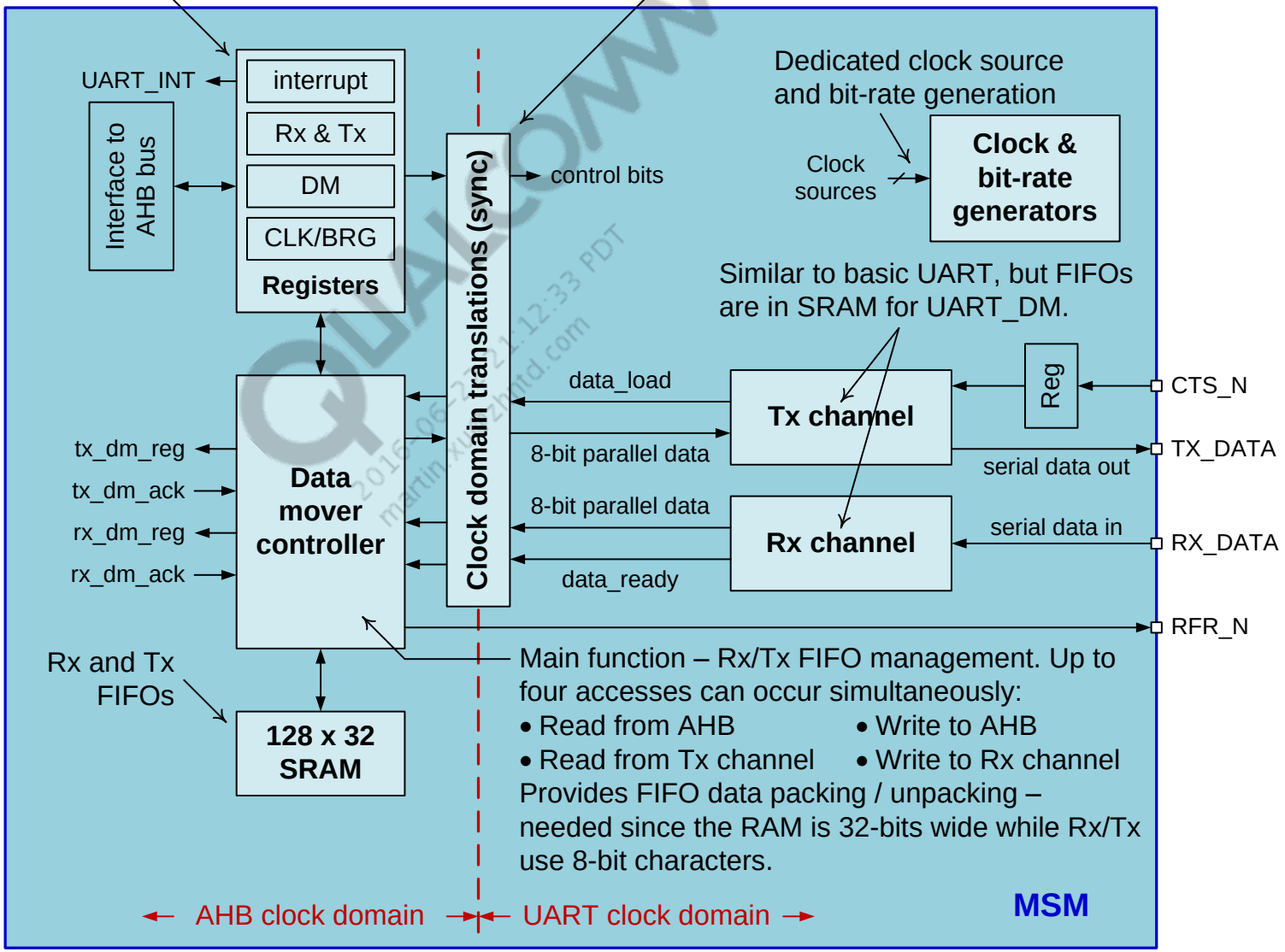
- As a result from one BLSP, SPI and I2C cannot be used at same time.
- Similarly UART and UIM cannot be used simultaneously from one BLSP.
- Two 2-pin UART cannot be used simultaneously from one BLSP.
- Two 12C cannot be used simultaneously from one BLSP.

These rules apply across all 12 BLSPs.

UART – Architecture

The registers are an AHB slave.
Write and read transactions are enabled from the AHB bus to the registers and to the Tx/Rx FIFOs (one SRAM).

Provides synchronization between the two clock domains:
- SRAM, registers, and controller run off the AHB clock.
- Rx and Tx channels run off the UART clock.

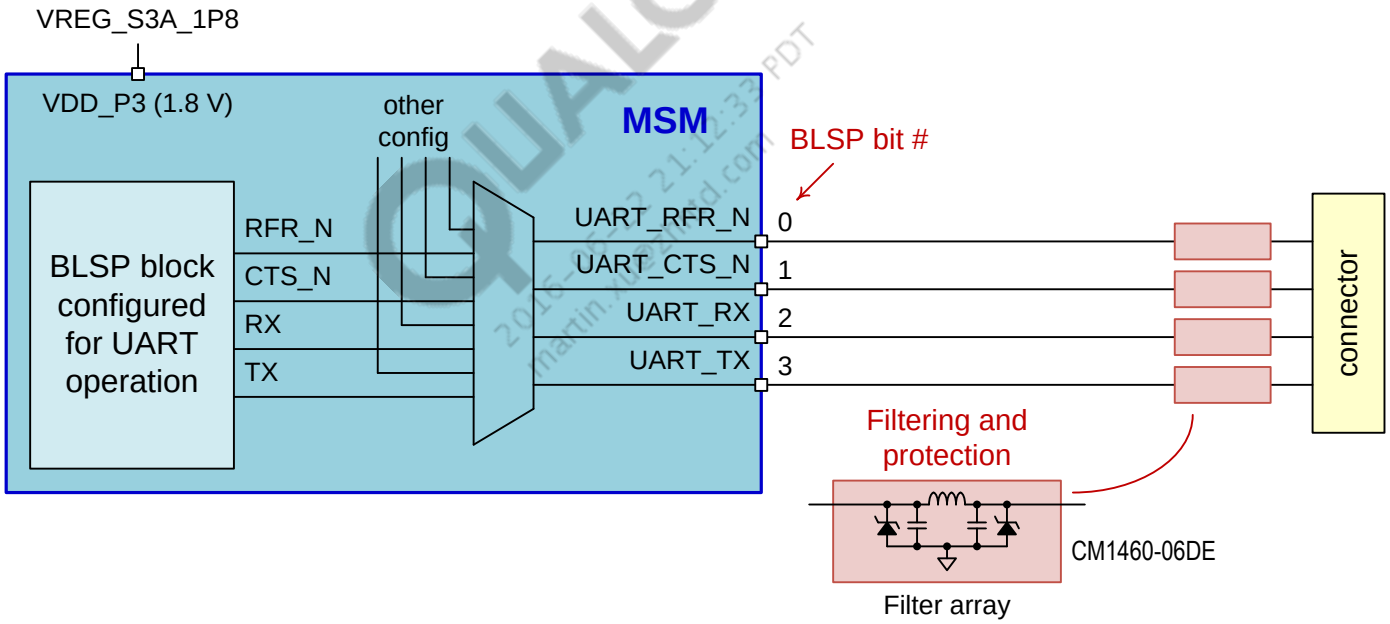


UART – Features

- The UART_DM is used to support high-speed UART operation up to 4 Mbps.
  - Only slow IrDA is supported.
- Advantages of the UART_DM block include:
  - Rate-controlled data mover with separate CRCI channels for Rx and Tx
  - Larger Rx and Tx FIFOs that are implemented in one SRAM
  - Access to the fast peripheral bus (32-bit wide AHB interface) rather than the slow bus
  - Maintains traditional level interrupts directly to the microprocessor when the data mover is not available
- Note that the UART_DM Tx and Rx channels are similar to the basic UART channels, except that the FIFOs are implemented in SRAM and the FIFO controls and IRQ generation are in the DM controller block.

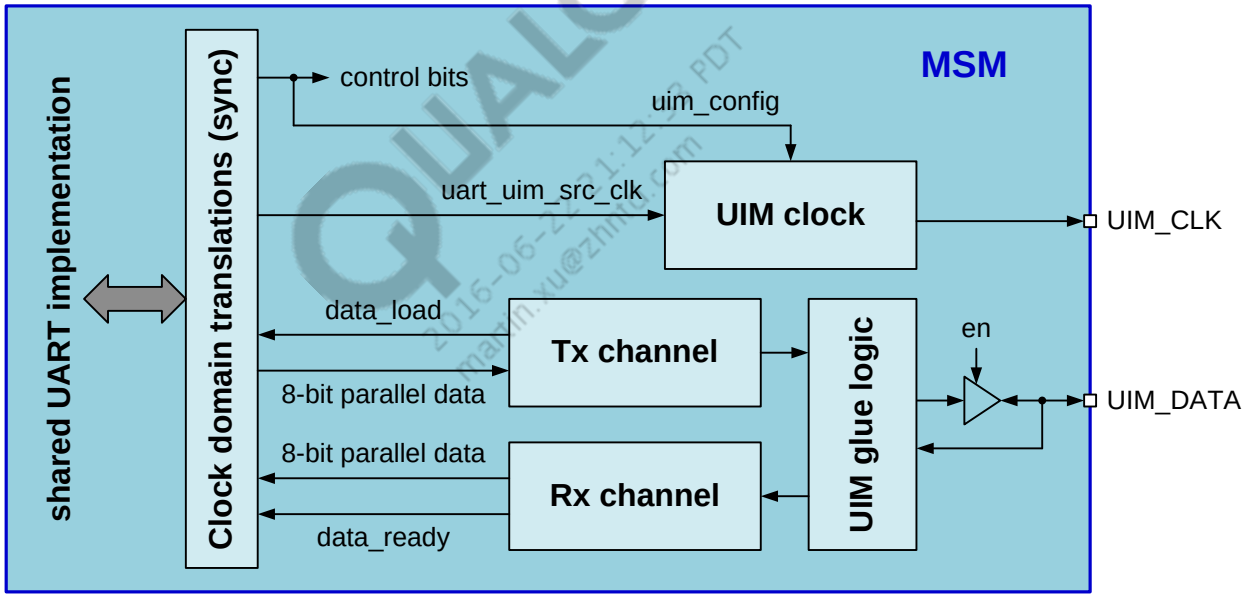
UART – Schematic Diagram

- The reference designs did not use any UART ports.
- A generic example is shown below.



UIM – Architecture and Features

- UIM functions use most of the UART circuits.
- UART circuits are supplemented by UIM-specific glue logic and clock circuitry.
- See the *UART* pages for back-end details.



UIM Controller (non-BLSP)

- A dedicated UIM controller is integrated in to the Modem Subsystem to support dual UIM operation.
- The UIM controller interfaces with the UARTDM module and the UIM ports.
- The UIM controller is an always ON power domain which can route the interrupts from its GPIOs to the MPM block.
- The three interrupt capable GPIOs controlled by UIM controller:
  - GPIO_100 -> UIM1_DETECT
  - GPIO_52 -> UIM2_DETECT
  - GPIO_101 -> BATT_ALARM
- The MSM8974 device supports the hot-swap feature, which will enable it to recognize and initialize a UIM not only during its powerup sequence, but also during regular operation.
  - This feature is enabled using UIMx_DETECT GPIOs, which are routed to the UIM controller that is always ON.
  - Whenever UIM is inserted or removed (even during sleep), the detect GPIOs will trigger an interrupt to initialize or shutdown the UIM interface.
- Features:
  - Data rates up to 4 MHz (in Fast mode+)
  - Dual-voltage 1.8 or 2.95 V support:
    - UIM1 is powered off VDD_P5; connect to VREG_L9, and program for 1.8 V or 2.95 V as desired.
    - UIM2 is powered off VDD_P6; connect to VREG_L10, and program for 1.8 V or 2.95 V as desired.

Note: PMIC level translation is not needed to support dual-voltage UIM modules.

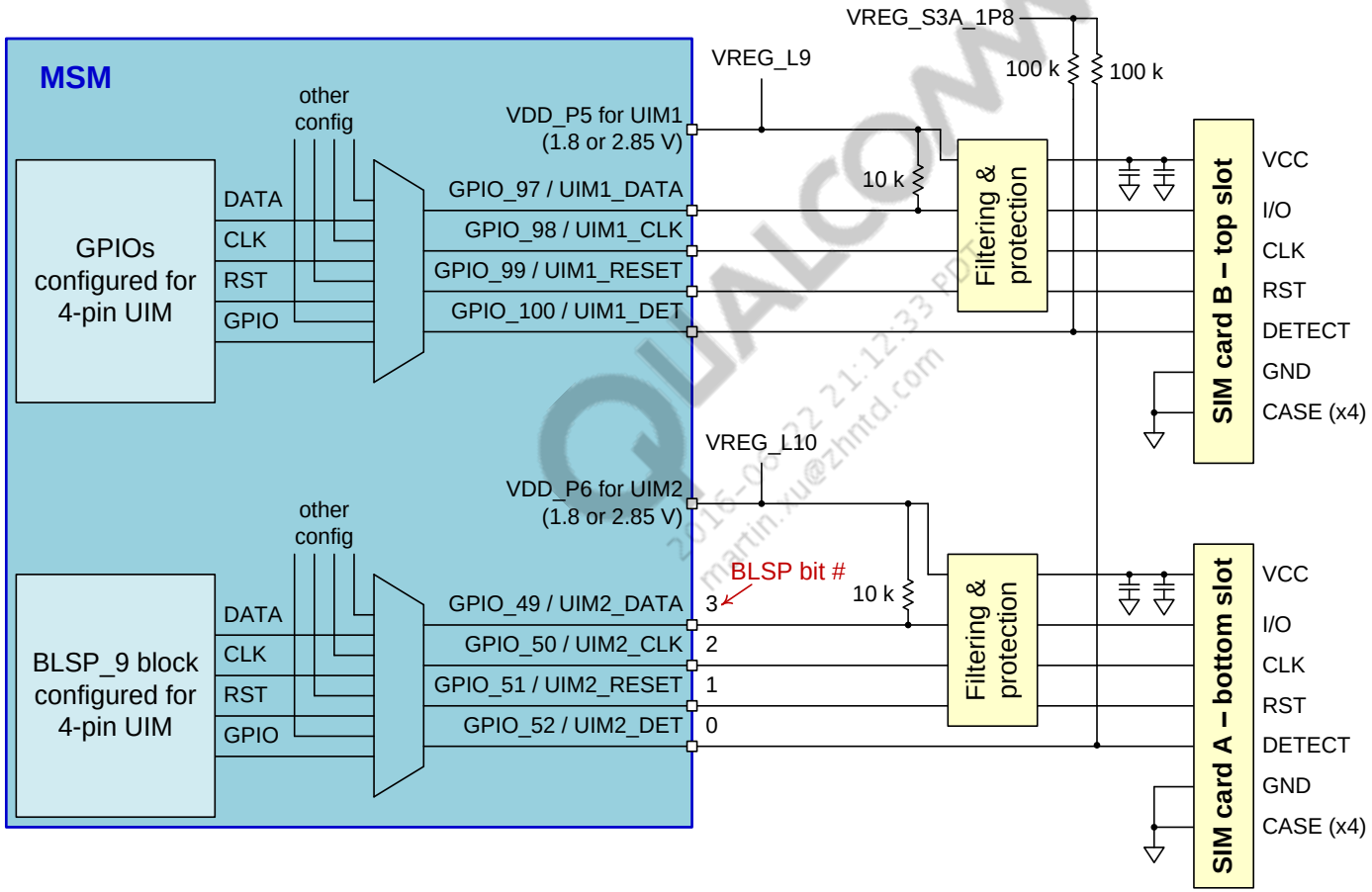
UIM – Initialization

During UIM initialization, the UIM clock and data lines are active as they execute their initialization process one UIM slot at a time (if more than one is used). After initialization, the slots' operation depends on whether a module is detected.

- If a module is detected:
  - The data line stays active, even if data is not being transmitted (between accesses). It maintains its marking state (logic high) between accesses.
  - The clock is only active during accesses; it is turned off between accesses to save power. The state of the clock when off is programmable, and must be selected to support the module's characteristics.
  - Even though the clock is turned off between accesses, the interface is still active. The data, reset, and power lines all remain high (assuming an active-low reset).
  - Note that the interface stays on once the module is detected, even during MSM sleep modes; the current consumption continues.
- If a module is not detected (module not inserted or not recognized, broken connection, etc.):
  - The interface is deactivated.

UIM – Schematic Diagram

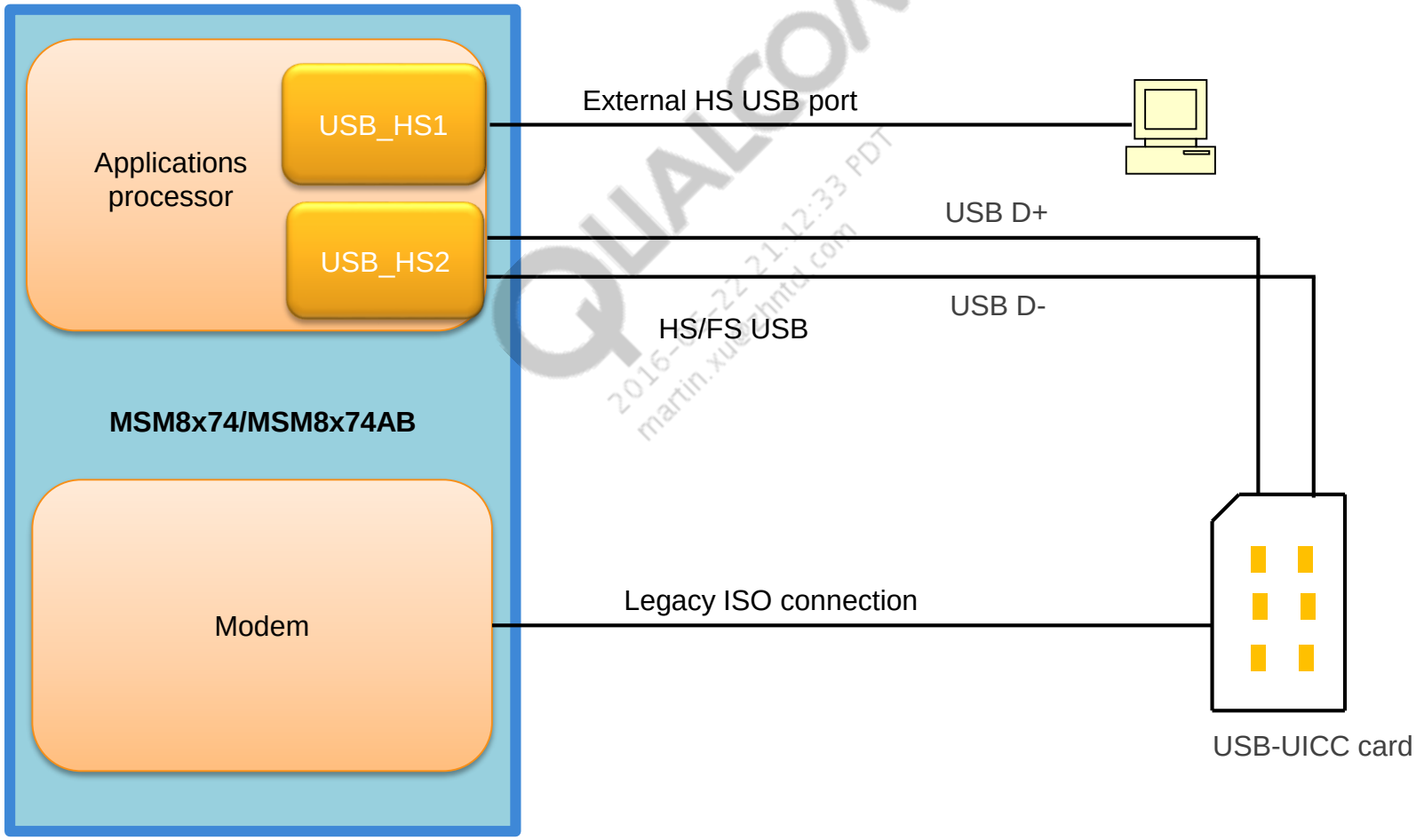
- The reference design supports dual-UIM ports.
- Details are shown below.



ESD is recommended in the UIM interface.

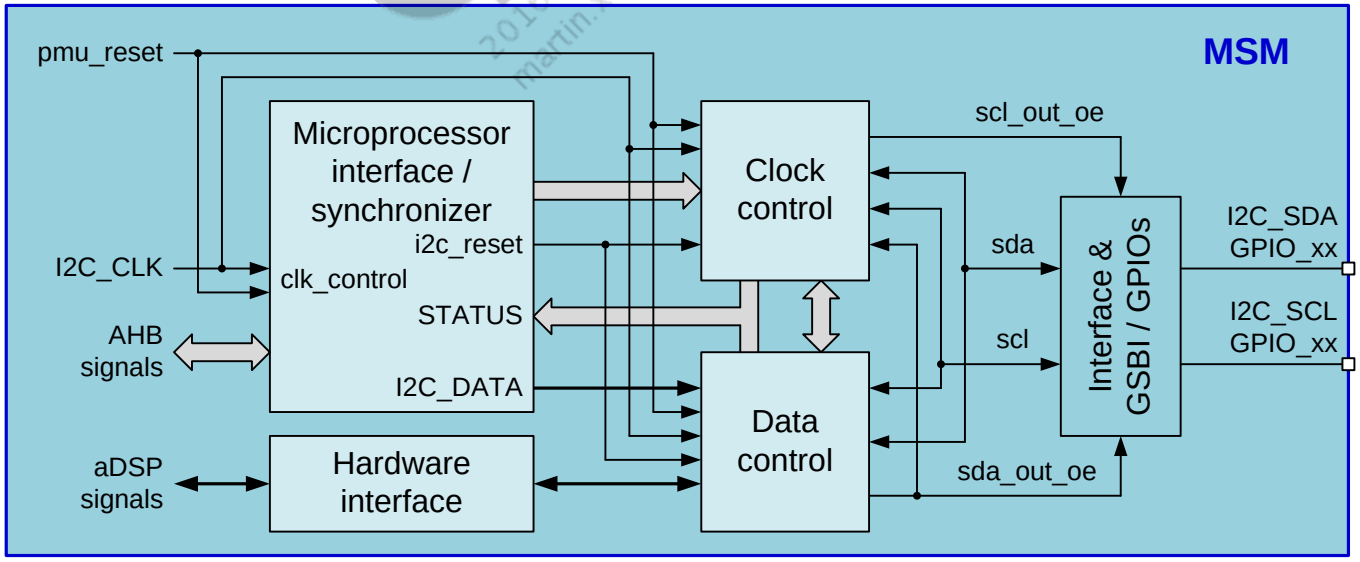
USB UICC

USB UICC is now supported on the MSM8x74/MSM8x74AB chipset. The secondary USB port (USB_HS2) is used for the USB UICC connection.

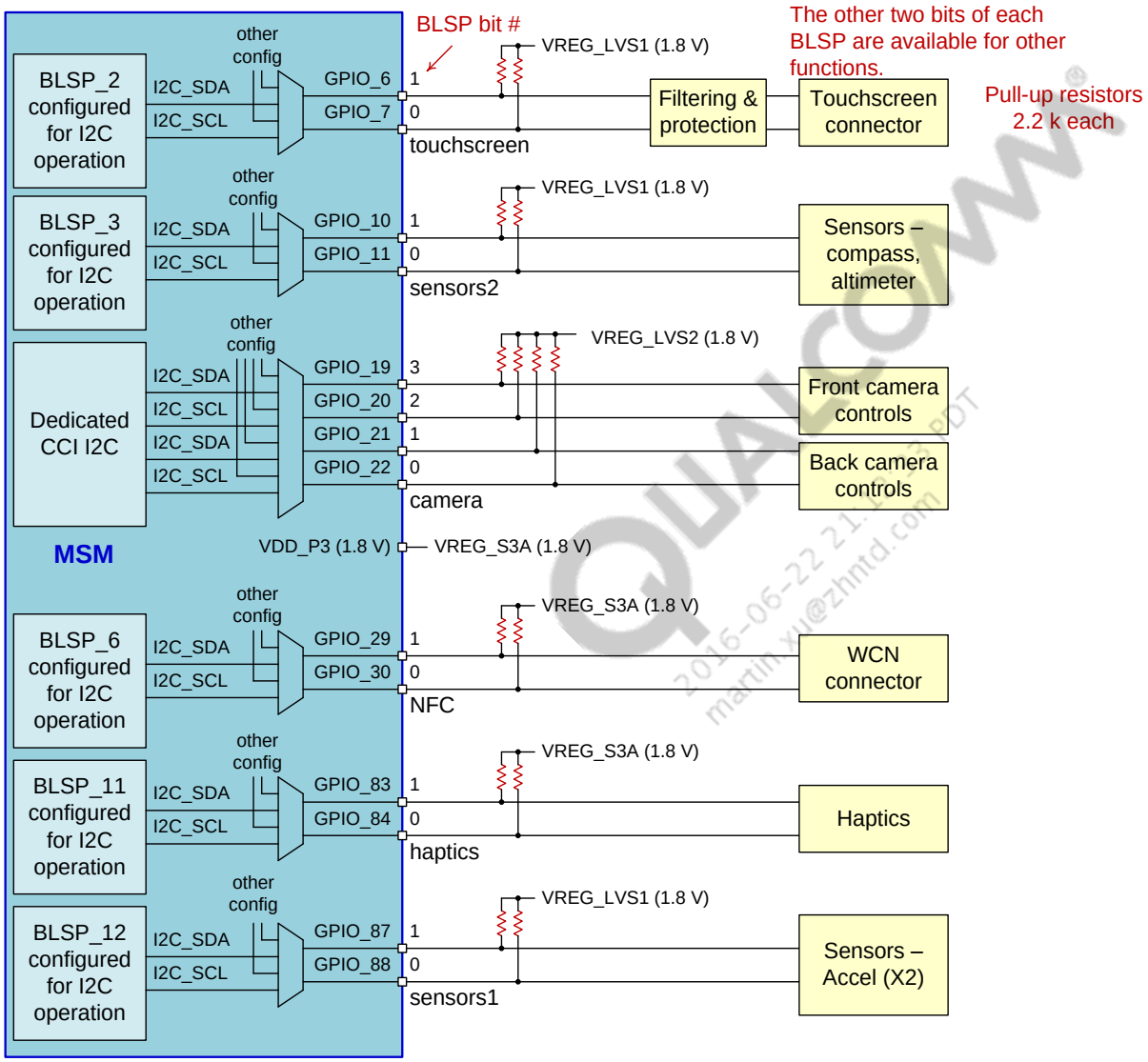


I2C – Architecture and Features

- Two-wire bus for inter-IC communications supports any IC fabrication process.
  - Each device is recognized by a unique address and can operate as either a transmitter or receiver, depending on the device function.
- The I2C controller provides an interface between the PSS peripheral NoC, an advanced high-performance bus (AHB), and the industry standard I2C serial bus.
  - Handles the I2C protocol and frees up the on-chip processor (and AHB) to handle other operations.
  - It is I2C-compliant, high-speed mode (HS-mode)-compliant, and a master-only device.
- I2C pins use GPIOs configured as open-drain outputs; the pull-up resistor is provided by the slave.
- Camera auto-focus control via I2C originates with the aDSP; a separate hardware request port is required at the I2C controller.



I2C – Schematic Diagram

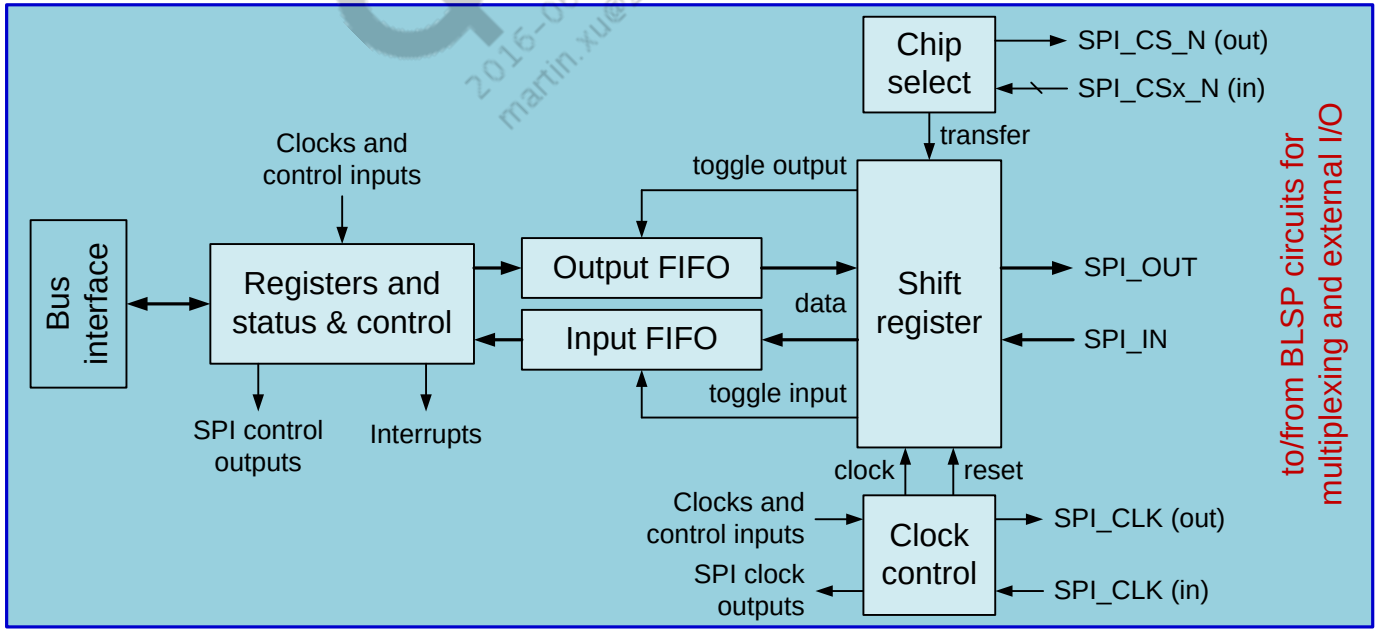


Note: GPIO_19 and GPIO_20 are dedicated I2C for camera only. They cannot be used as a general-purpose I2C for other applications.

SPI – Architecture

Major SPI blocks:

- Register bank and status & control – provides internal bus interface, software register interface, and overall core control.
- Output FIFO – holds all data to be output, and provides output data mover interface.
- Shift register – provides serial-to-parallel and parallel-to-serial conversions necessary for external transfers, and provides loop-back.
  - Toggle output signal indicates to output FIFO that an output value has been loaded for shifting.
  - Likewise, toggle input signal indicates to input FIFO that an input value is available for loading.
- Input FIFO – holds all data to be input and provides the input data mover interface.
- Clock control – provides master clock and reset signal to shift register.
- Chip-select – MSM is SPI master-only, so it drives the chip-select signals; provides an spi_transfer signal to tell the shift register that a shift operation should take place.

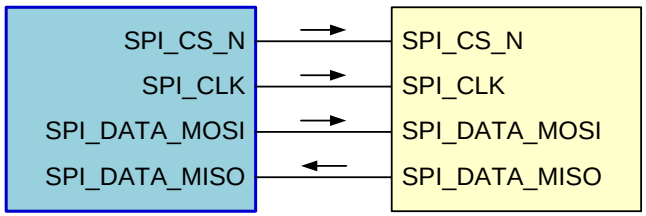


SPI – Features and Configurations

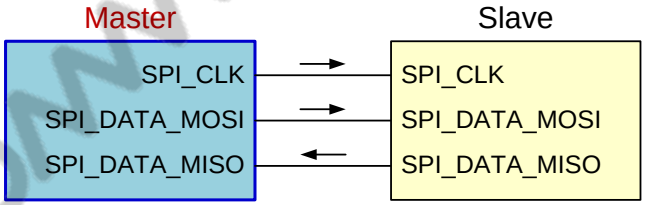
- 4-bit synchronous serial data link
- Master-only mode
- Up to 52 MHz on all SPI interfaces
- Master device initiates data transfers; multiple slave devices are supported by using chip-selects
- No explicit communication framing, error checking, or defined data word lengths, so the transfers are strictly at the “raw” bit level
- As an SPI master, the core supports several SPI system configurations (as defined by the SPI protocol):
  - Configurations 1, 2, 4, and 5 are supported, though configurations 4 and 5 are software dependent.
  - Configuration 3 and the multi-master configuration are not supported.
- Configurations are shown on the next page.

SPI Configurations

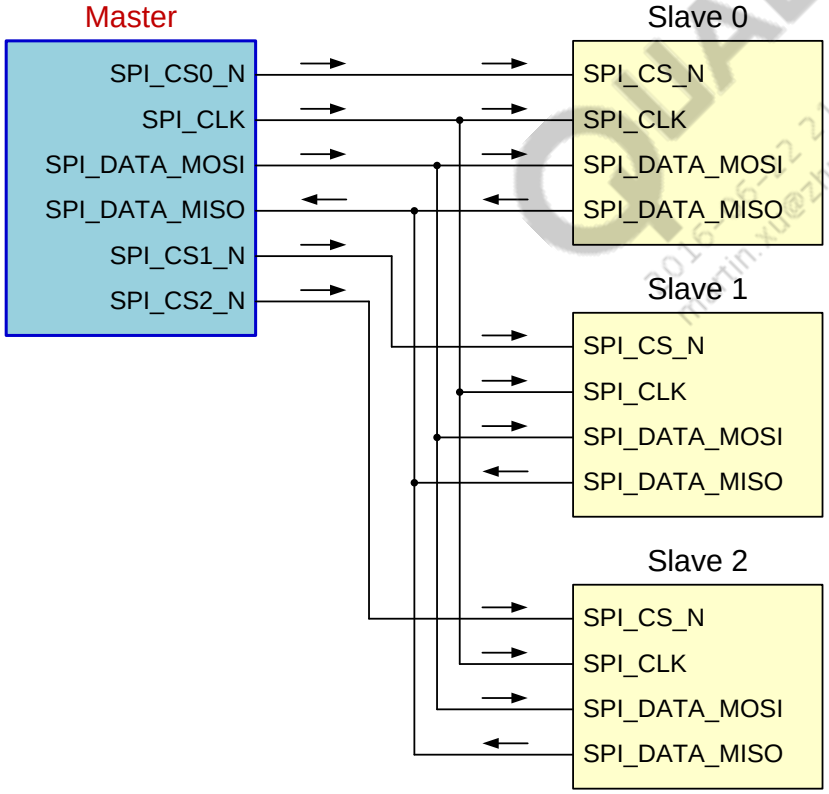
SPI system configuration 1



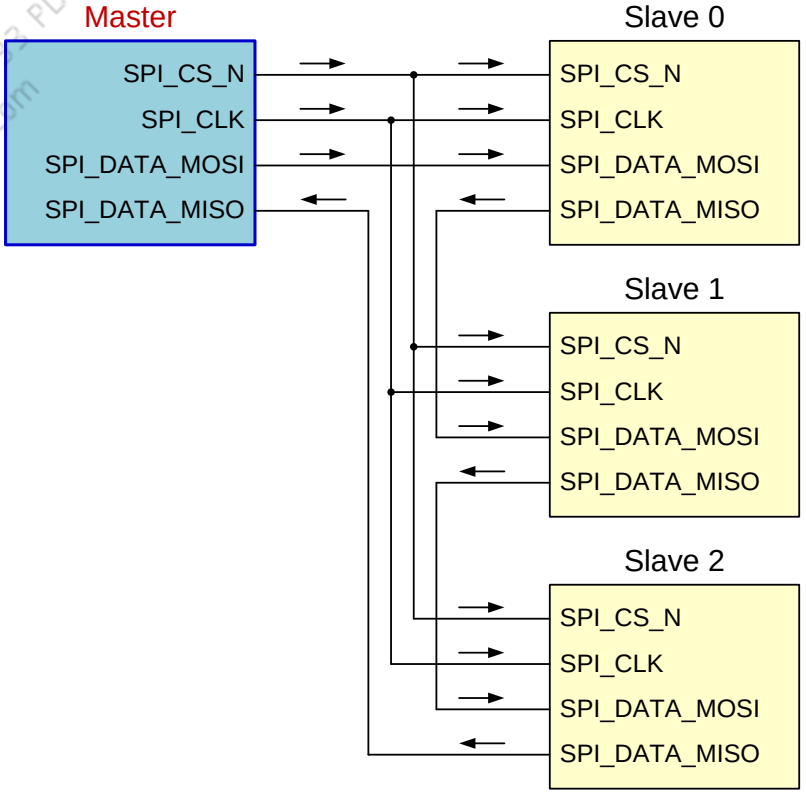
SPI system configuration 2
Dedicated one-to-one connection; no chip select



SPI system configuration 4



SPI system configuration 5

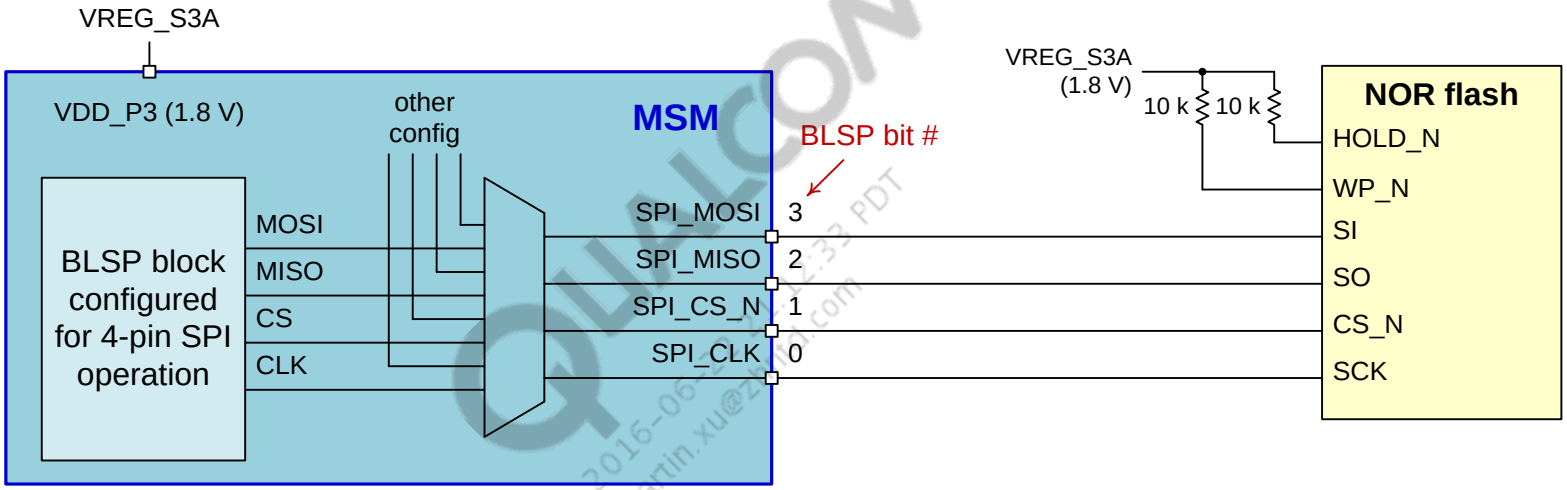


SPI Protocol Requirements

1. As an SPI master, the core supports several SPI system configurations (1, 2, 4, and 5).
2. As an SPI master, the core supports SPI_CS0_N, SPI_CS1_N, SPI_CS2_N, and SPI_CS3_N.
3. As an SPI master, the core supports SPI_CLK.
4. As an SPI master, when no transfers are taking place (IDLE), the core supports SPI_CLK_IDLE_LOW and SPI_CLK_IDLE_HIGH.
5. As an SPI master, the core supports leaving the SPI_CLK running when no SPI_CS#_N is asserted (during IDLE).
6. As an SPI master, the core supports SPI_MOSI tri-state during IDLE (optional).
7. As an SPI master, the core supports Input_First_Mode.
8. As an SPI master, the core supports Output_First_Mode.
9. As an SPI master, the core supports any value of N between 4 and 32.
10. As an SPI master or slave, the core supports the following half-duplex modes (MSM is master-only):
    A. SPI_MOSI only with SPI_MISO held low.
    B. SPI_MISO only with SPI_MOSI held low.
11. As an SPI master, the core supports a mechanism to control the number of SPI_CLK ticks between the assertion of different SPI_CS signals. Even though there is no formal flow control mechanism, a slave may require dead time between SPI_CS assertions – this capability meets that potential requirement.
12. As an SPI master, the core supports the QTI SPI_CS_N master requirements.
13. As an SPI master, the core supports assertion of SPI_CS#_N between each transfer of size N (CS is normally de-asserted). As an option, SPI_CS#_N can be asserted for a “first transfer” and left asserted for T transfers through the “last transfer” T. Under this option, requirement #11 above still applies, but the SPI_CLK is turned off every N bits while SPI_CS#_N is left asserted. This corresponds to the multi-transfer chip-select (MX_CS).
14. As an SPI master, the core supports configuring SPI_CS#_N as active high (optional).

SPI – Schematic Diagram

- The reference design did not support any SPI interfaces.
- A generic example is shown below.



Connectivity Layout Guidelines (other than USB, SDC, and HSIC)

I2S, PCM, and SLIMbus audio interfaces:

- See the WCD9320/audio content for guidance.
- It is recommended to implement 3x trace width spacing between SLIMbus and other signals to avoid cross-talk.

UART, UIM, I2C, and SPI interfaces:

- Routed using usual digital bus design rules and considerations. Operating frequencies should be considered during routing; each interface's maximum frequency is listed below.
  - UART = up to 4 MHz
  - UIM = 4 MHz
  - I2C = 1 MHz (fast mode+)
  - SPI = 52 MHz

Other recommendations:

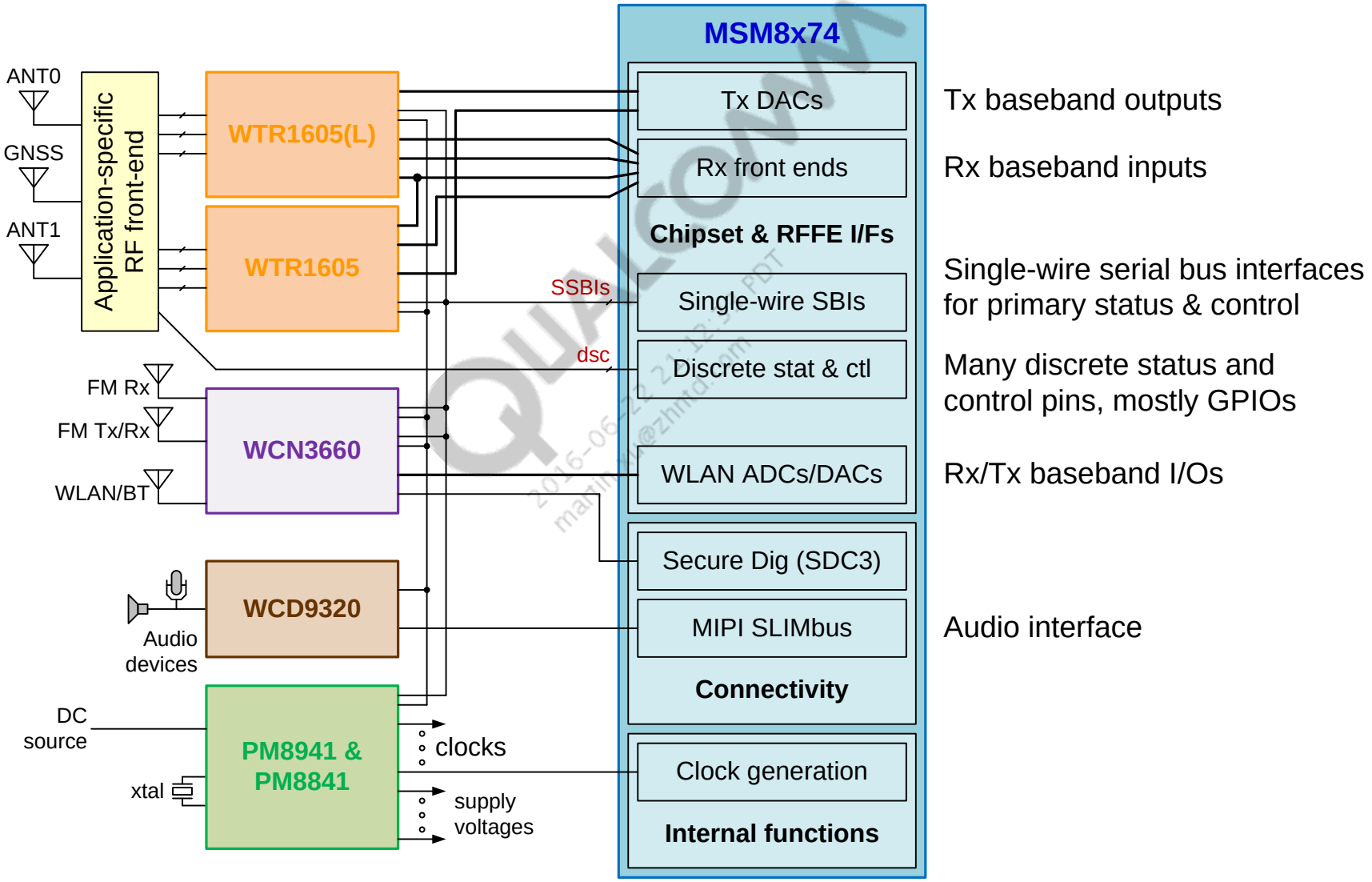
- Each of these buses should be routed on an inner layer to avoid injecting noise into the system.
- Each bus should be routed as a group whenever possible.
- Keep the buses away from sensitive functions and traces (RF, audio, and the 19.2 MHz XO).
- Since the SPI runs at the highest frequency, it should be given priority over the others.

Sec. 9

Chipset and RFFE Interfaces; MSM Configurable I/Os

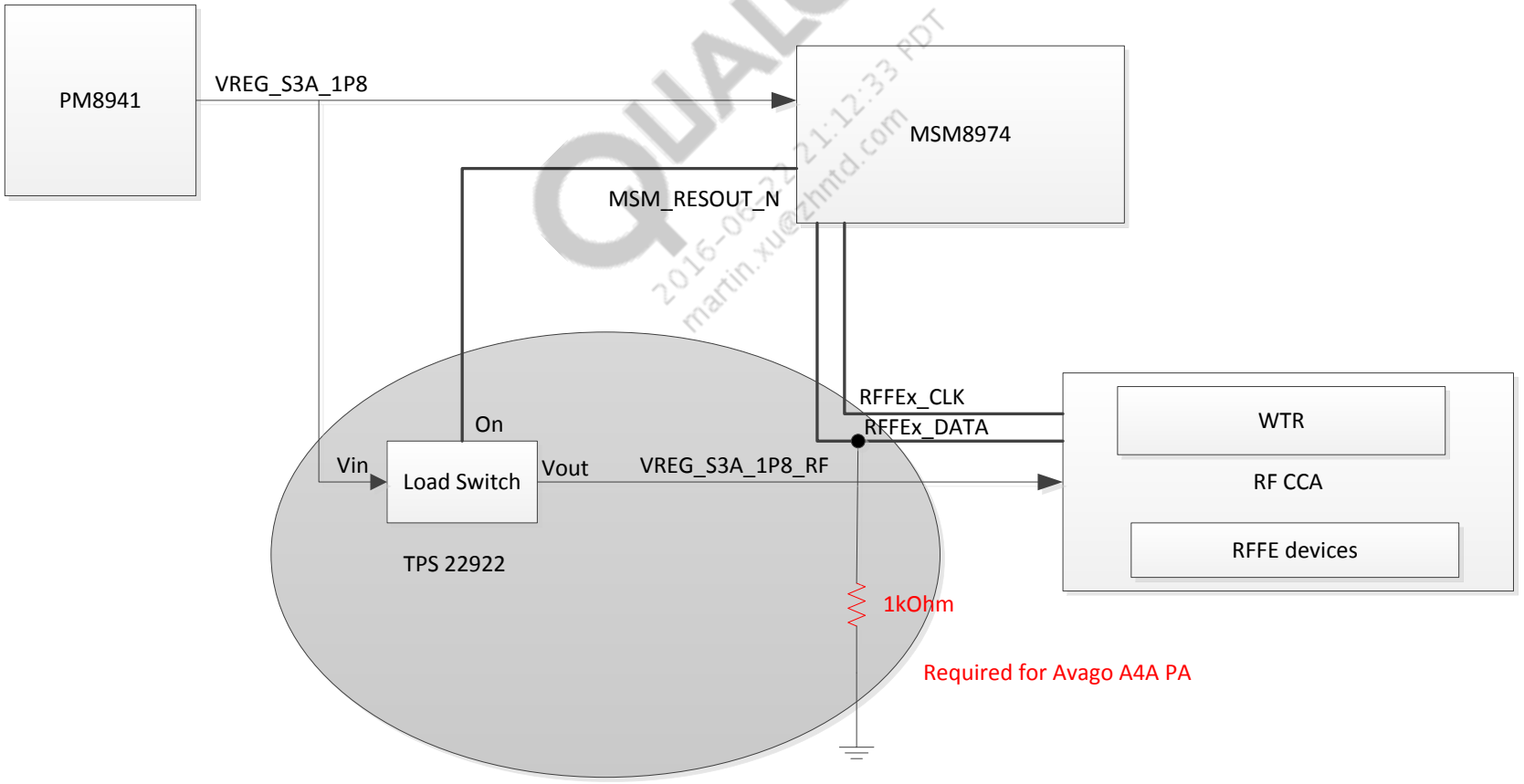
Chipset & RFFE Interfaces Overview

MSM I/O functions depend on the RF design being supported (see the following pages).



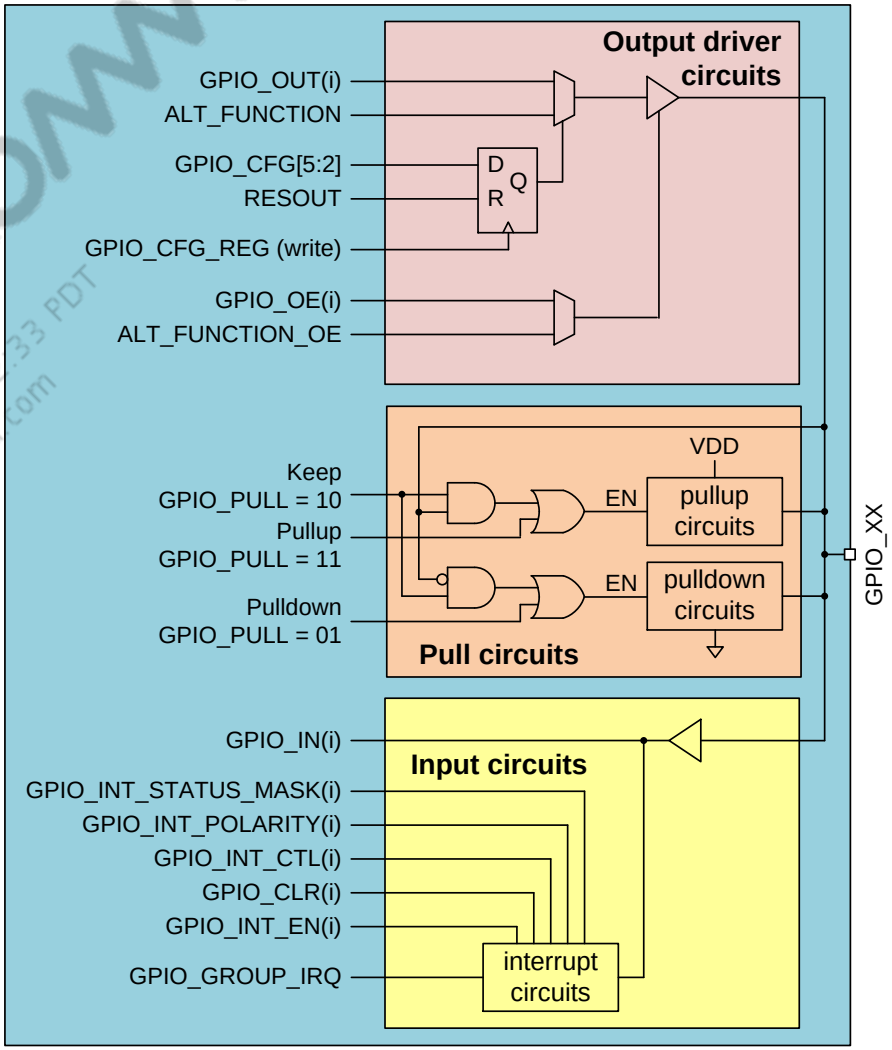
Switch for MIPI RFFE devices

- A load switch TPS22922 should be added on the VREG_S3A_1P8 power rail to the VIO of the MIPI RFFE devices.
- For more information, refer to Issue 19 in the *MSM8274/MSM8674/MSM8974 Device Revision Guide* (80-NA437-4) and Issue 1 in the *MSM8274AB/MSM8674AB/MSM8974AB Device Revision Guide* (80-NA437-4A).



Configurable GPIO Ports and MPM Support

- 146 general-purpose input/output (GPIO) ports.
- Configuration options are shown at right, and are described on the following pages.
- Software assigns functions to the GPIOs, and their configurations are set accordingly.
- If MPM is enabled by software to reduce power consumption, only these select GPIO pins can be used to wake up the MSM device.
  - 1, 5, 9, 18, 20, 24, 27, 28, 34, 35, 37, 42, 44, 46, 50, 54, 59, 61, 62, 64–68, 71–75, 77, 79, 80, 82, 86, 92, 93, 95, 102, 144.
  - 52, 100, 101 controlled UIM controller
  - And none of the other GPIO pins can be used as a wake-up interrupt
- If MPM is used, external pulls should not be used on digital pads because:
  - During MPM operation, all digital pads are held by a keeper.
  - If the external pull is in the opposite direction, DC current will flow (highly undesirable during a low-power sleep mode).
- The PCB layout must avoid excessive crosstalk on the wakeup GPIOs; coupling might cause an unintentional trigger.



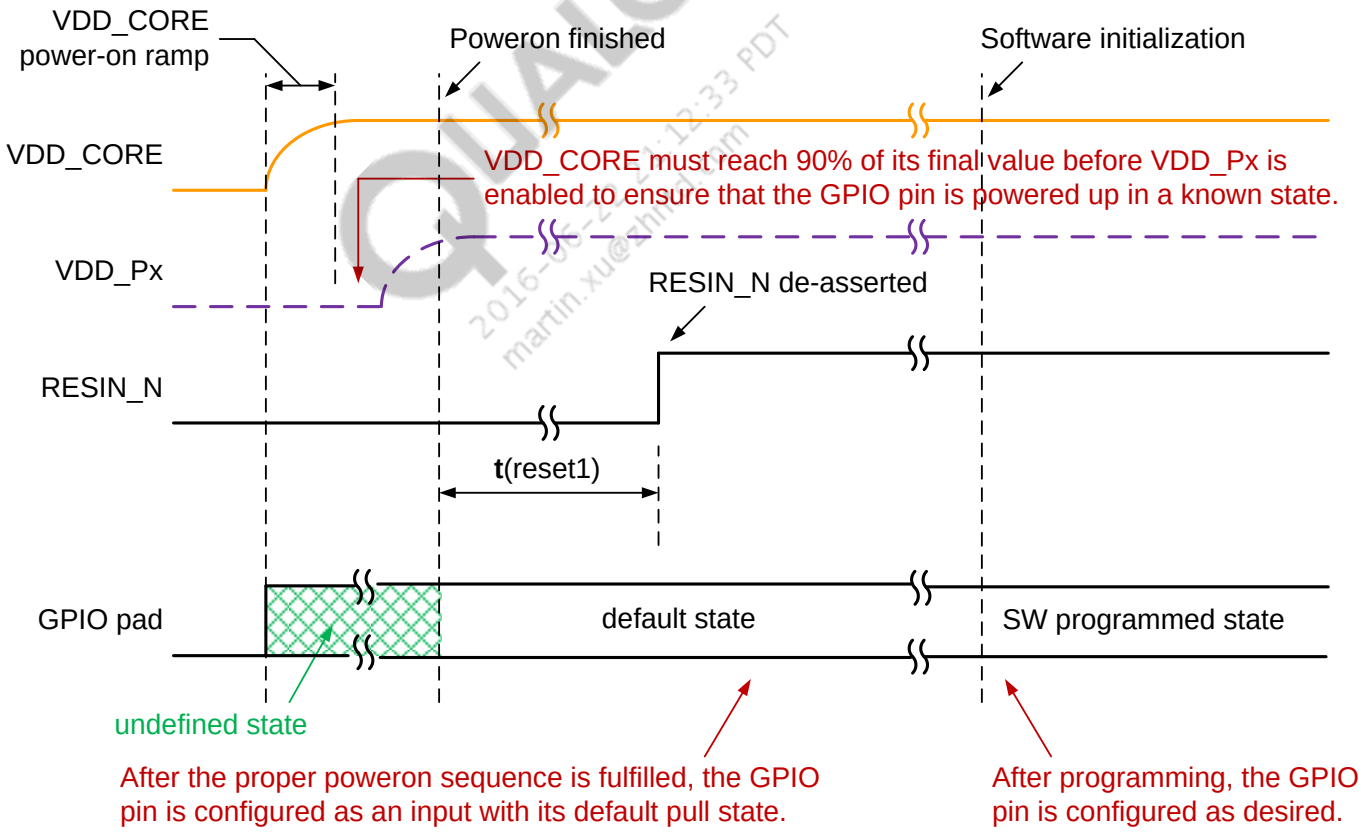
GPIO Initialization

To avoid GPIO problems, a specific supply sequence is required when powering up the MSM device.

The core supply (VDD_CORE) must turn on and reach 90% of its programmed value before any of the pad supplies (VDD_Px) are enabled.

If this sequence and timing relationships are not achieved, the GPIO pads might come up in undefined states.

The PMIC ensures the proper supply sequence and timing.



GPIO Programmable Configurations – Outputs

Three types of outputs are supported:

- Normal
  - Uses GPIO_OUT(i) and GPIO_OE(i).
  - To drive the output pad as a GP output signal, configure the GPIO for non-alternate function, write the GPIO_OUT_X register with the desired value, and then set the corresponding bit in the GPIO_OE_X register to enable the output path.
- Alternate
  - Uses ALT_FUNCTION and ALT_FUNCTION_OE.
  - A procedure similar to the one just described is used, but the alternate functions are exercised rather than the normal functions.
- Special
  - Functions, such as ETM, can override other GPIO functions (software-implemented).

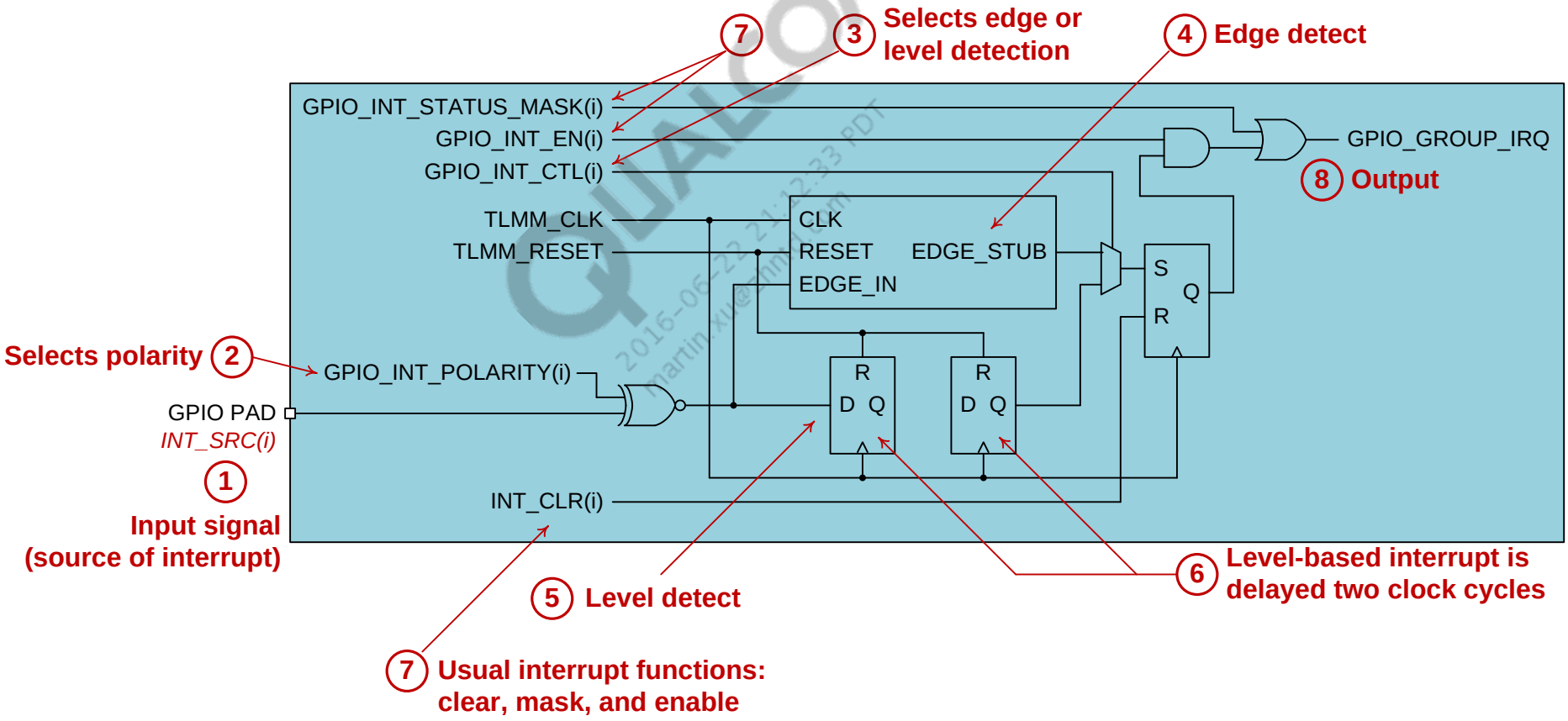
Programmable output drive strength:

- Use the GPIO_PAD_HDRIVE_MSEL_n register bits 2:0.
  - 000 = 2 mA to 111 = 16 mA, 2 mA per LSB.
  - The stated 2 to 16 mA settings apply when the associated pad supply voltage is 1.8 V.
- Higher supply voltage results in a slightly higher drive current; see *MSM8274/MSM8274AB, MSM8674/MSM8674AB, MSM8974/MSM8974AB Device Specification* (80-NA437-1) for details.

GPIO Programmable Configurations – Inputs

Two types of input configurations are supported:

- Buffer – A standard CMOS input buffer; its output is GPIO_IN(i).
- Interrupt – An interrupt circuit allows the input signal's level or edge, with selectable polarity, to generate an interrupt.



GPIO Programmable Configurations – Pulls and Multiplexing

Three types of pulls are supported:

- Pull-up – to the pad voltage defined within *MSM8274/MSM8274AB, MSM8674/MSM8674AB, MSM8974/MSM8974AB Device Specification* (80-NA437-1).
- Pull-down – to ground.
- Keeper – maintains the pad's last valid logic level, regardless of whether it was an input or an output.
  - Keepers are weak drivers that cannot drive an external bus.
  - Internal pulls are implemented using JFETs; strengths vary between devices, but are not expected to be weaker than 100 k.

GPIO multiplexing:

- A paging scheme is used to address individual GPIOs and to configure their alternate functions, pulls, and drive strengths.
- Before a particular GPIO can be configured using the GPIOx_CFG register, its index must be written to the GPIOx_PAGE register.
- Non-selected interfaces are gated in the GPIOx_CFG register, thereby forcing their inputs low.

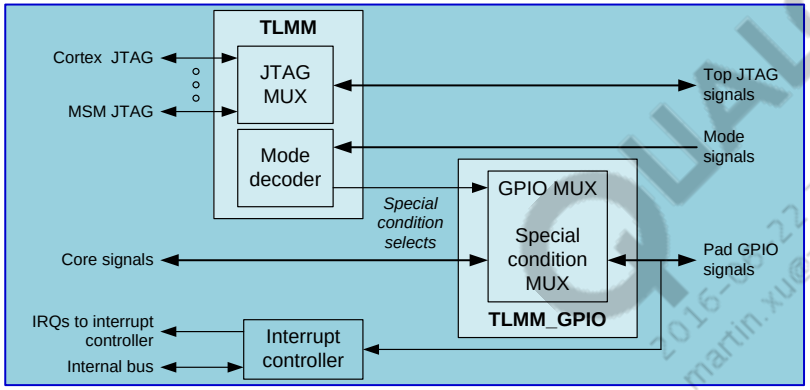
There are four GPIO register types:

- Output read/write registers (4) – GPIO_OUT_X; each bit corresponds to a specific GPIO.
- Output enable write registers (4) – GPIO_OE_X; each bit corresponds to a specific GPIO.
- Input read registers (4) – GPIO_IN_X; each bit corresponds to a specific GPIO's input value.
- Selection registers – GPIOx_PAGE and GPIOx_CFG.
  - GPIOx_PAGE is a 7-bit register whose content determines which GPIO is being programmed.
  - GPIOx_CFG is a 6-bit register that is used to configure the settings of the GPIO selected by the GPIOx_PAGE register; it contains the pin's function (bits 5:2) and pull (bits 1:0).

Refer to *MSM8274/MSM8674/MSM8974/APQ8074 Software Interface* (80-NA437-2) for more register info.

Top-level Mode Multiplexer

- The top-level mode multiplexer (TLMM) provides a convenient mechanism for sharing multiple internal functions on the same sets of GPIO pads.
- The mode assignment for each set of GPIOs is specified using a combination of input pin settings (such as MODE[1:0]) and software-programmable register settings.
- Using the TLMM method allows higher-level instructions, resulting in faster and easier GPIO assignments.
- Without the TLMM, each GPIO pad would require individual programming.



There are two multiplexing (and de-multiplexing) modes.

1. Standard – Most GPIOs fall into this category.
   - They are configured as inputs at power-on, and then are set by software to their desired functionality.
   - Some example uses include GPIOs supporting different feature sets, such as a phone manufacturer choosing to use the UIM in lieu of UART.

2. EBI – assume their default EBI functions at power-on.
   - The TLMM module receives mode-select control from mode pins and software-writable registers (used to control the GPIO configuration – drive strength, pull direction, and keeper).
     - GPIO pin values are readable directly as a register-mapped read.
     - All registers controlling pad configuration and control are asynchronously reset to ensure immediate pad control at power-on without clock dependency.

Sec. 10

MSM Top-level Layout and Power, Ground, and Unused Pins

MSM Layout and Power, Ground, and Unused Pins Overview

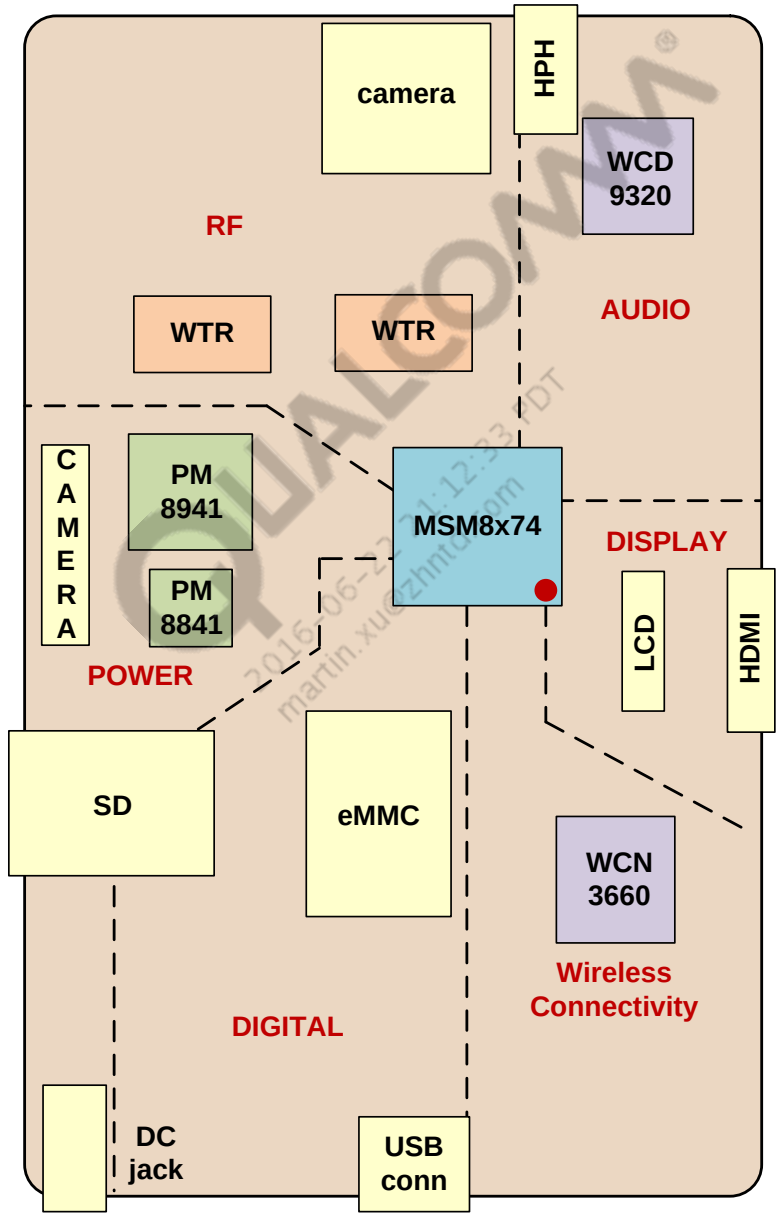
MSM general layout topics:

- MSM top-level parts placement.
- Top-level layout recommendations.
  - Stack-up and routing rules
  - Routing between pads, microvias, and core vias
  - Digital signal breakout
  - Power & ground breakout

MSM power, ground, and unused pin topics:

- MSM DC power grid
- Current consumption data release schedule
- DC power distribution to the MSM IC
- DC power routing and bypassing
- Also refer to the *PMIC* training for more power-supply routing guidelines
- MSM ground connections
- Handling unused MSM pins

Board-level Parts Placement

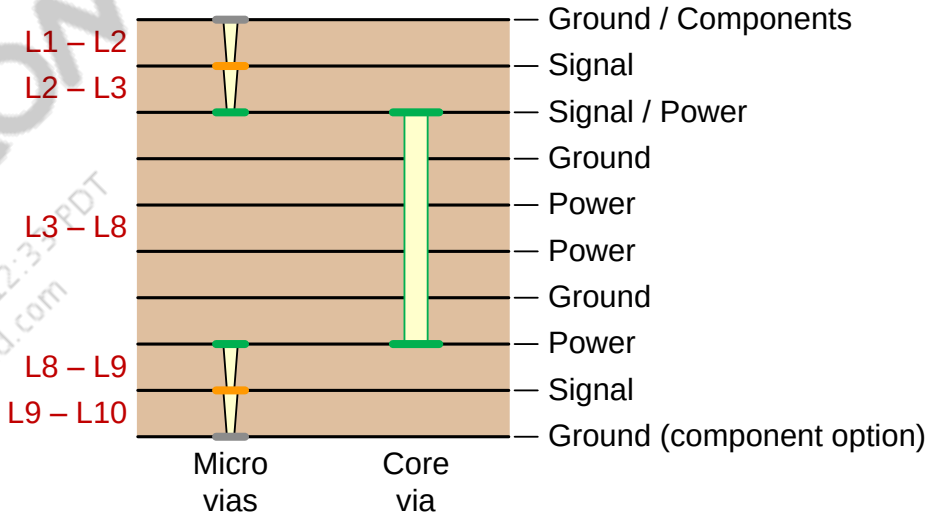


Stackup and Design Rules

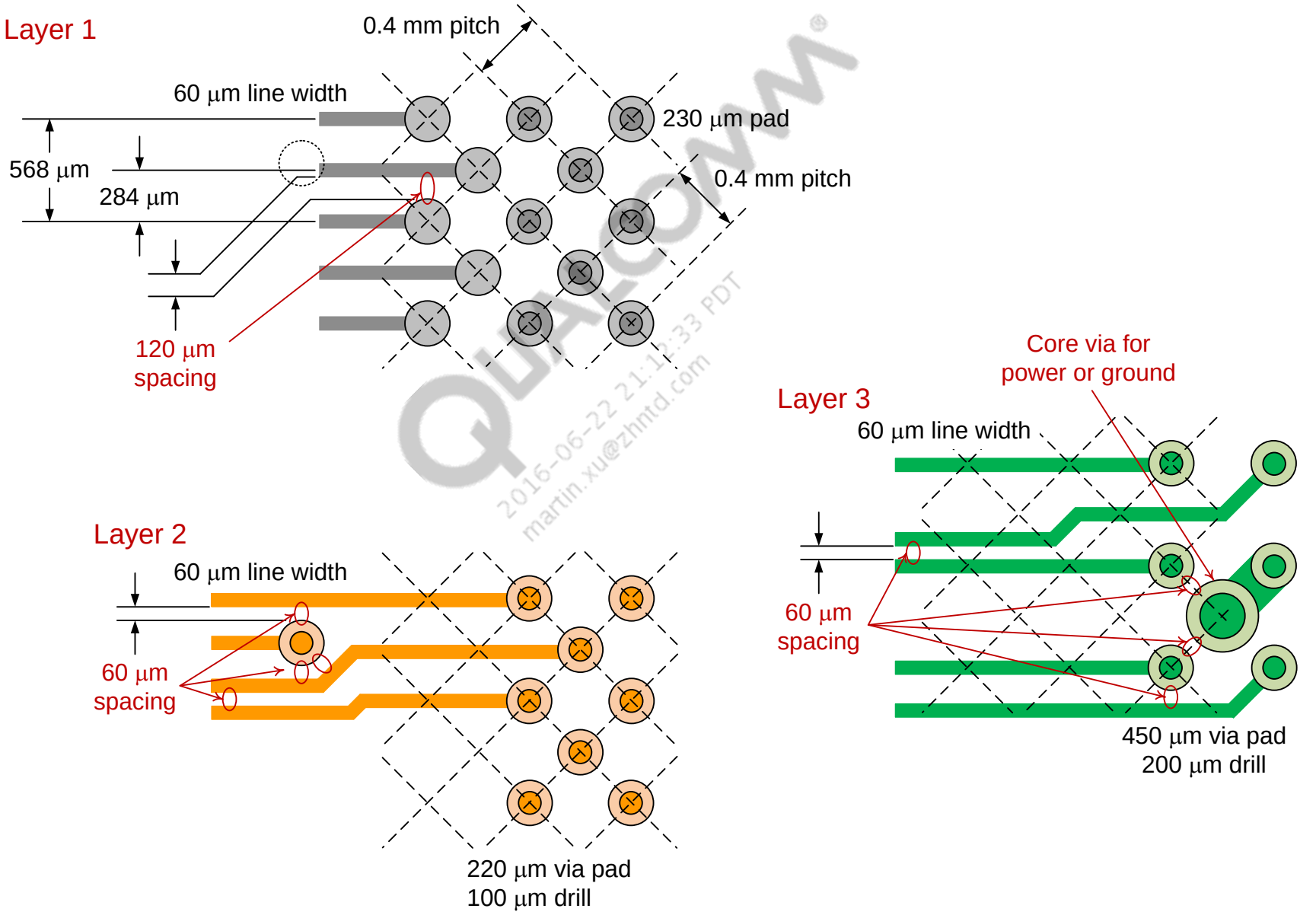
- Line width and spacing:
  - 60 μm under MSM device and breakout.
  - Expand to desired trace width and spacing 75 μm once routed to more open areas.
- Pad size/clearance:
  - 230 μm/120 μm
- Microvia pad size/drill hole/clearance:
  - 220 μm/100 μm/60 μm
- Core via pad size/drill hole/clearance
  - 450 μm/200 μm/75 μm
- Each signal layer is adjacent to a ground layer, thereby ensuring good return paths.
- Breakout guidelines below and around the MSM device are given on the following pages.
- Route sensitive signals carefully to avoid exceeding crosstalk budgets.

2-6-2 stackup → 10 layers total

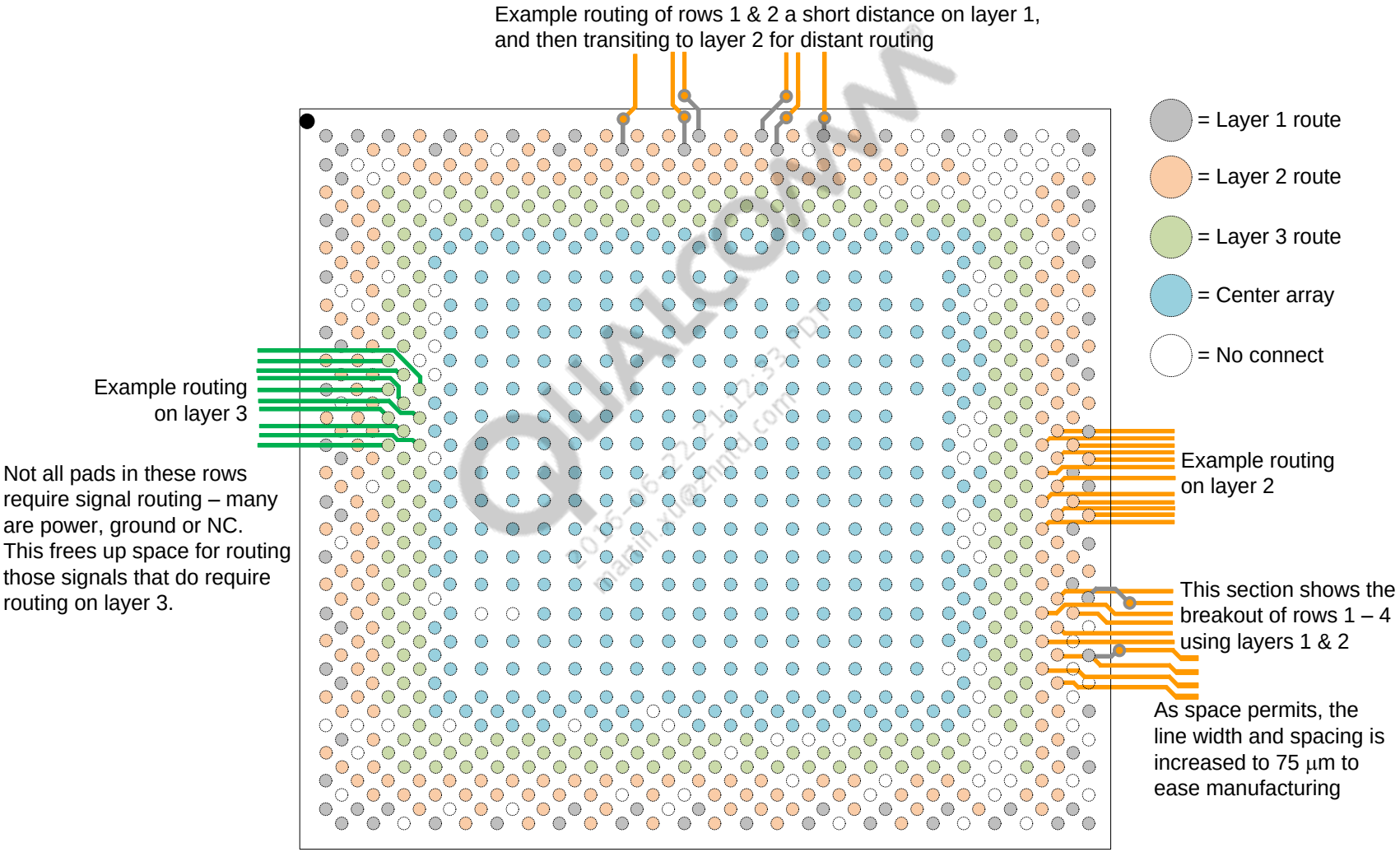
Example PCB stackup



Routing Between Pads, Microvias, and Core Vias

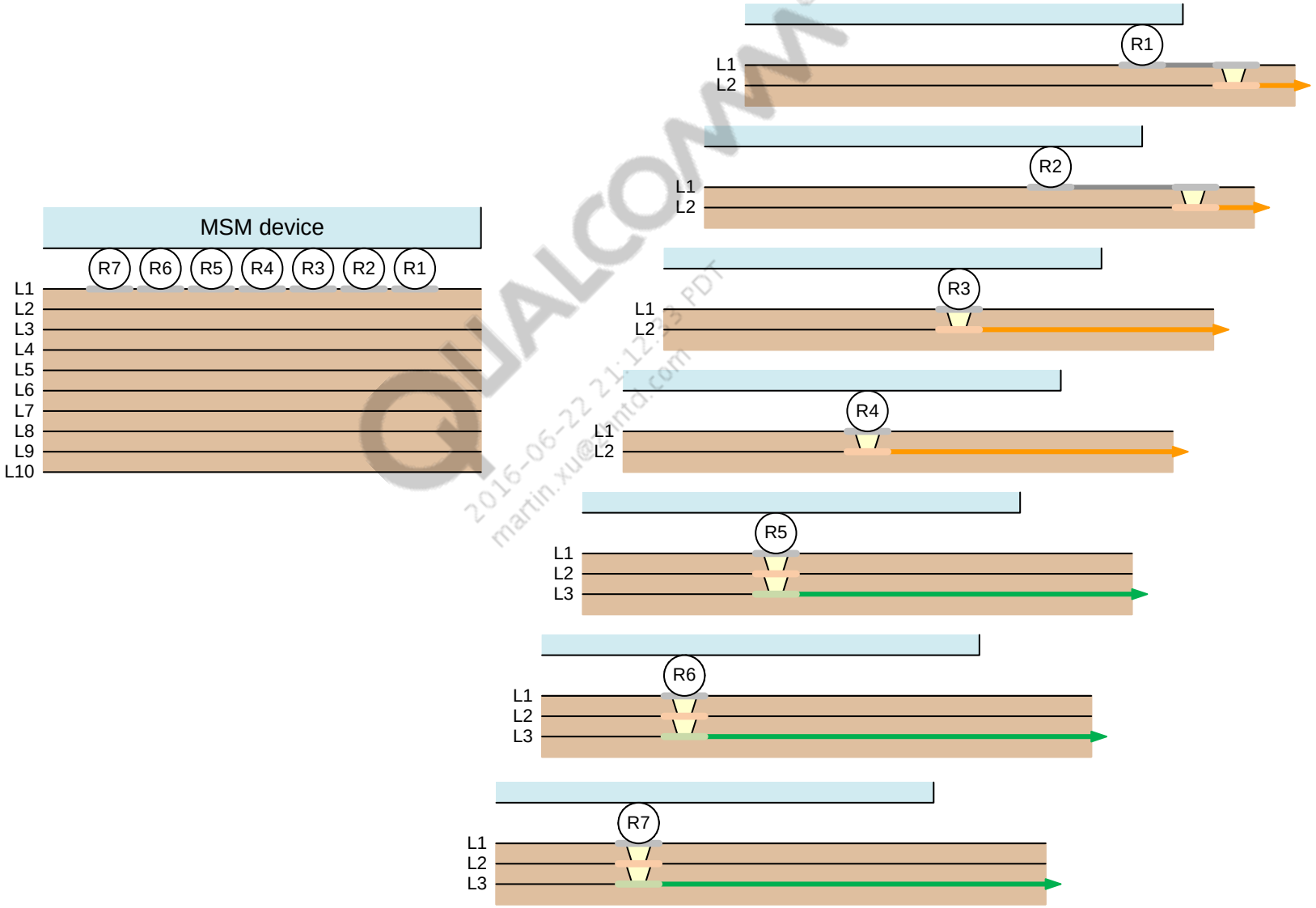


Digital Signal Breakout – Top View



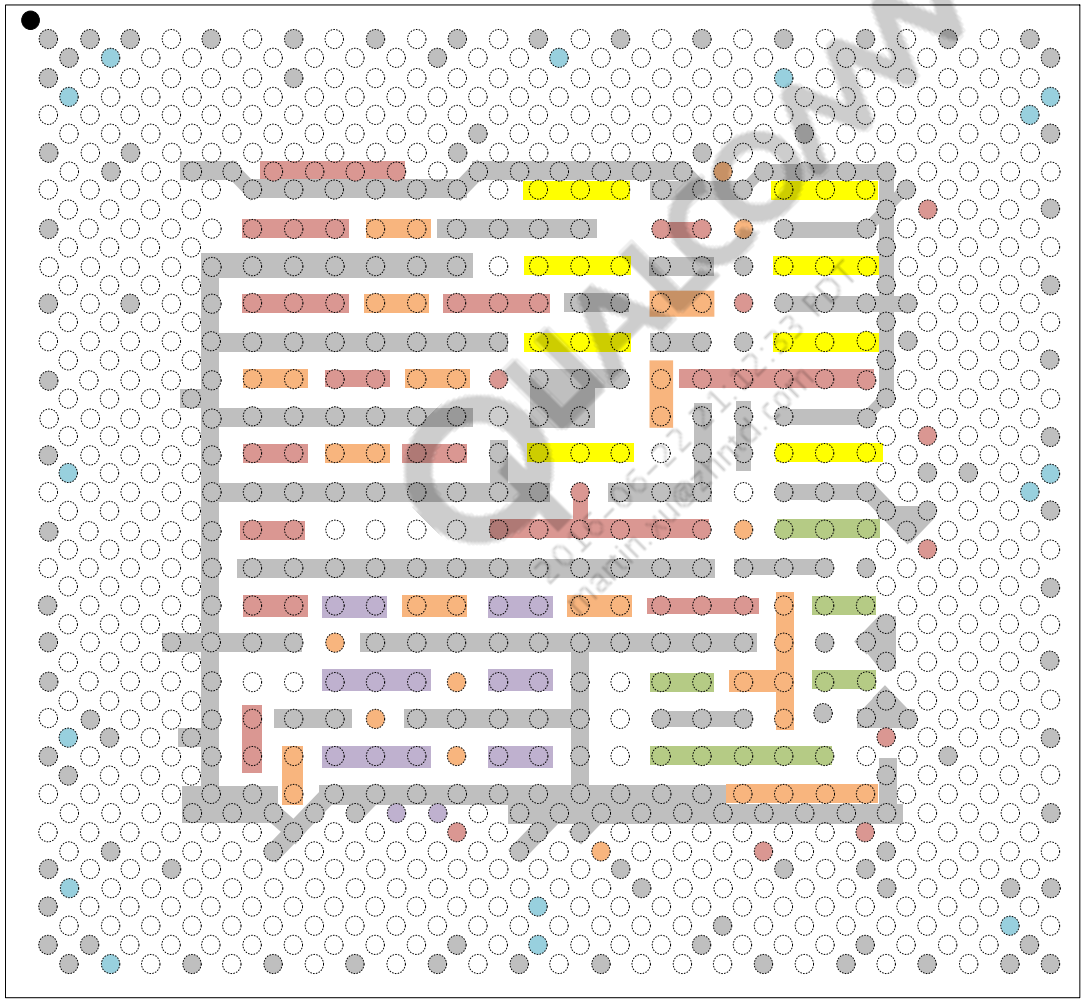
- 60 μm line width and spacing are used for signal breakout.
- Tighter rules might simplify routing if supported by your PCB vendors.
- After routing away from the MSM device, trace width and spacing can be increased to 75 μm to ease manufacturing.

Digital Signal Breakout – Cross-section View



Power & Ground Breakout – Top View Layer 2

The center array is primarily used for power and ground. Once power and ground routing reaches the core vias, routing can continue on any available layer. This page and the next show example routing up to the core vias.



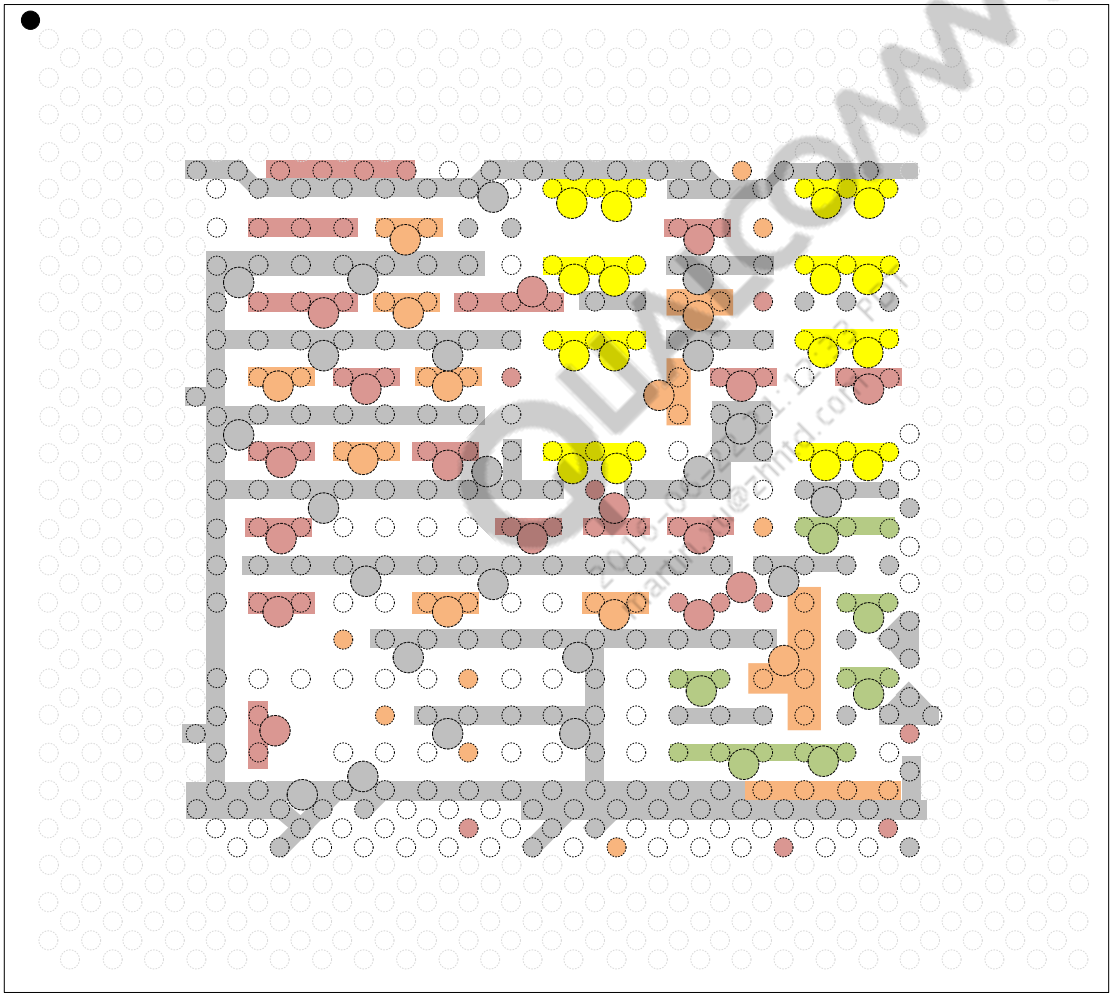
Only the main power busses that use the center array are shown in this example.

- = VDD_CORE
- = VDD_MEM
- = VDD_KRAIT
- = VDD_MODEM
- = VDD_DDR_CORE_x
- = ground
- = VDD_GFX

Common voltage and ground pins are grouped together on layer 2 as shown. Microvias are used to transition all areas to layer 3 (next).

Power & Ground Breakout – Top View Layer 3

Many layer 1-2 microvias are repeated between layers 2 and 3, but not all. Since microvias cannot be stacked on top of core vias, some of the possible layer 2-3 microvias are omitted to make room for the core vias that begin on layer 3.

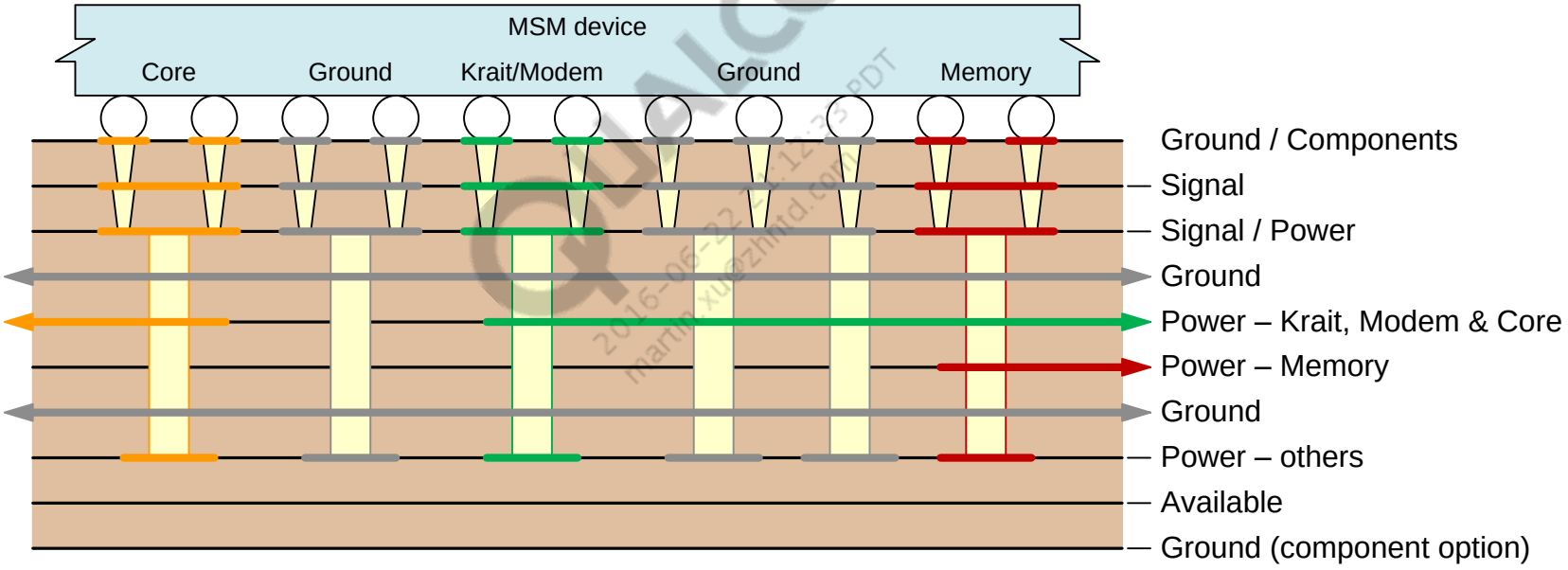


Locate ground core vias as close as possible to the power core vias.

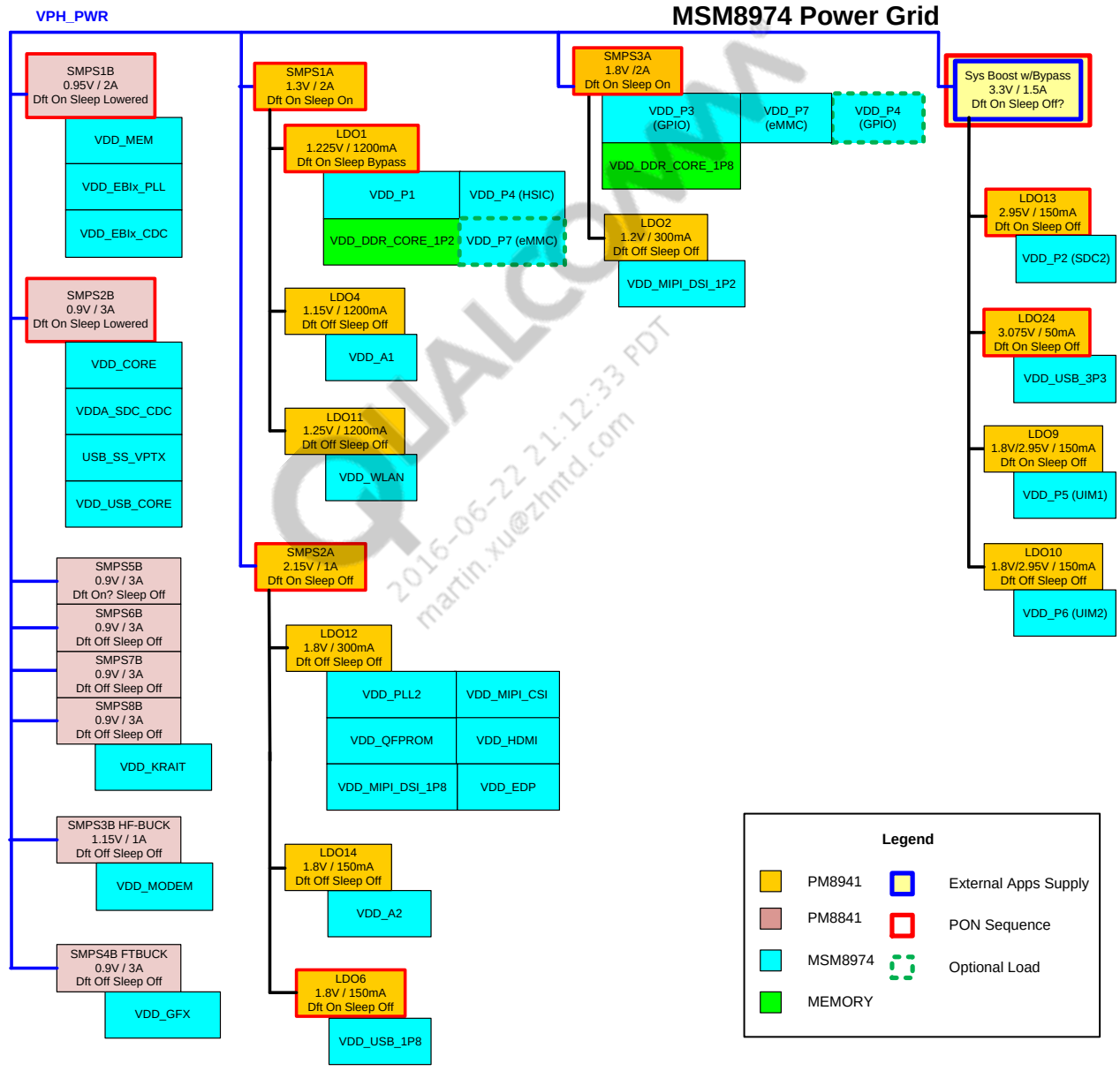
= VDD_CORE
= VDD_MEM
= VDD_KRAIT
= VDD_MODEM
= ground

Only center array pins that are used for the major power buses are shown.

Power & Ground Breakout – Cross-section View



MSM DC Power Grid



Current-Consumption Data Release Schedule

- *MSM8974 Linux Android Current Consumption Data* (80-NA437-7) is for MSM devices running in key operating modes, as directed by its software. Note that current consumption is highly dependent on software optimization.
- These documents' revision and release schedules are synchronized with key hardware and software delivery dates (see table below). Note that the type of values published depend upon the event milestone (estimated values or measured values; battery-level or by power rail).

	Event milestone	Data provided in this document
↓ Time	Engineering samples (hardware)	Battery-level estimate values
	3 weeks after feature-complete software release	Battery-level measured values and measured values for key power rails
	2 weeks after each subsequent significant software release	Battery-level measured values
	3 weeks after commercial software release	Battery-level measured values and measured values for key power rails

- Included information:
  - Test setups
  - Test definitions
  - Chipset current consumption
  - Target values – top-level
  - Measured values – top-level
  - Measured values – sleep mode
  - Measured values – various operating modes
  - Heat dissipation modeling

DC Power Distribution to the MSM IC – Comments

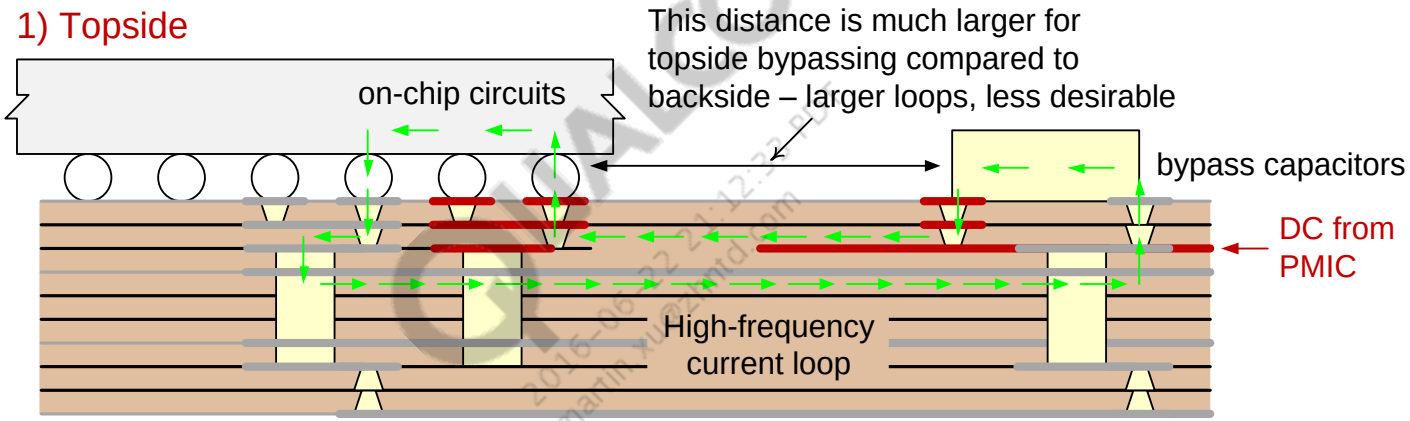
Determine the minimum trace width for DC distribution using the following:

1. Find the maximum current (I_{MAX}) conducted by the trace – the sum of maximum currents expected for all its loads.
2. Define the regulator's operating output voltage (V_{REG}).
3. Calculate the maximum tolerable trace resistance (R_{MAX}) assuming a 1% IR drop:
   - $R_{MAX} = 0.01 \times V_{REG} / I_{MAX}$
4. Estimate total trace length (L) based upon the preliminary layout.
5. Determine the copper thickness (T): 1 ounce copper foil thickness is 1.34 mil – scale as needed for thicknesses other than 1 ounce.
6. Calculate the minimum trace width (W_{MIN}) allowed.
   - $W_{MIN} = \rho \times L / (R_{MAX} \times T)$ where ρ = copper resistivity (1.7×10^{-8} Ω-m)

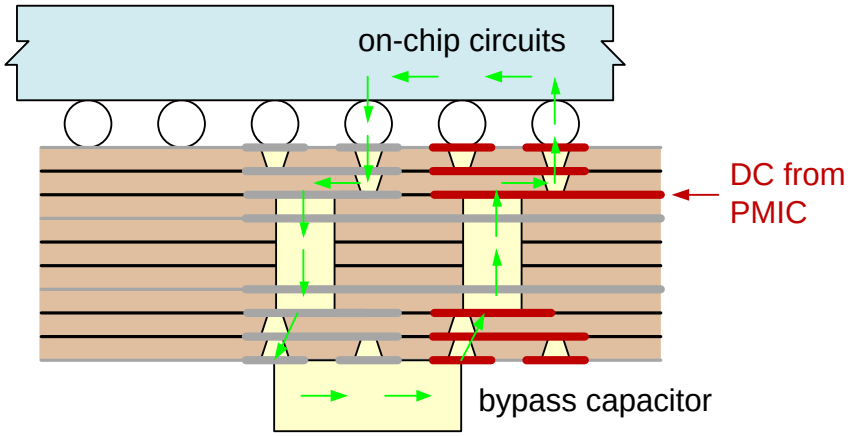
Topside vs. Backside Bypass Capacitors

- Bypass capacitors can be located on the same side as the MSM (topside) or on the opposite side (backside).
- Both are supported by the MSM IC.
- Backside is better – as illustrated – and easier to implement.
- Design examples are shown using topside (the more difficult routing).

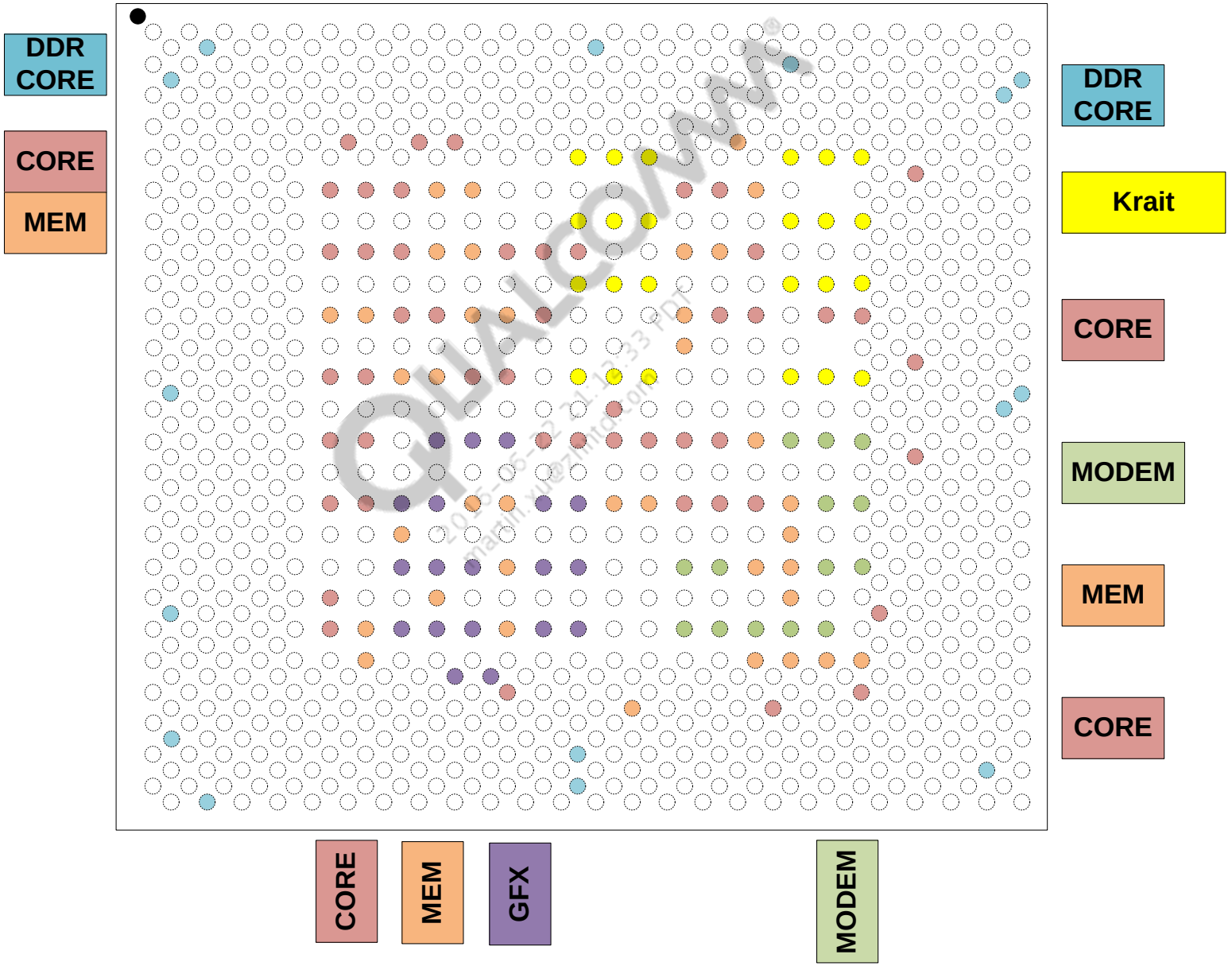
1) Topside



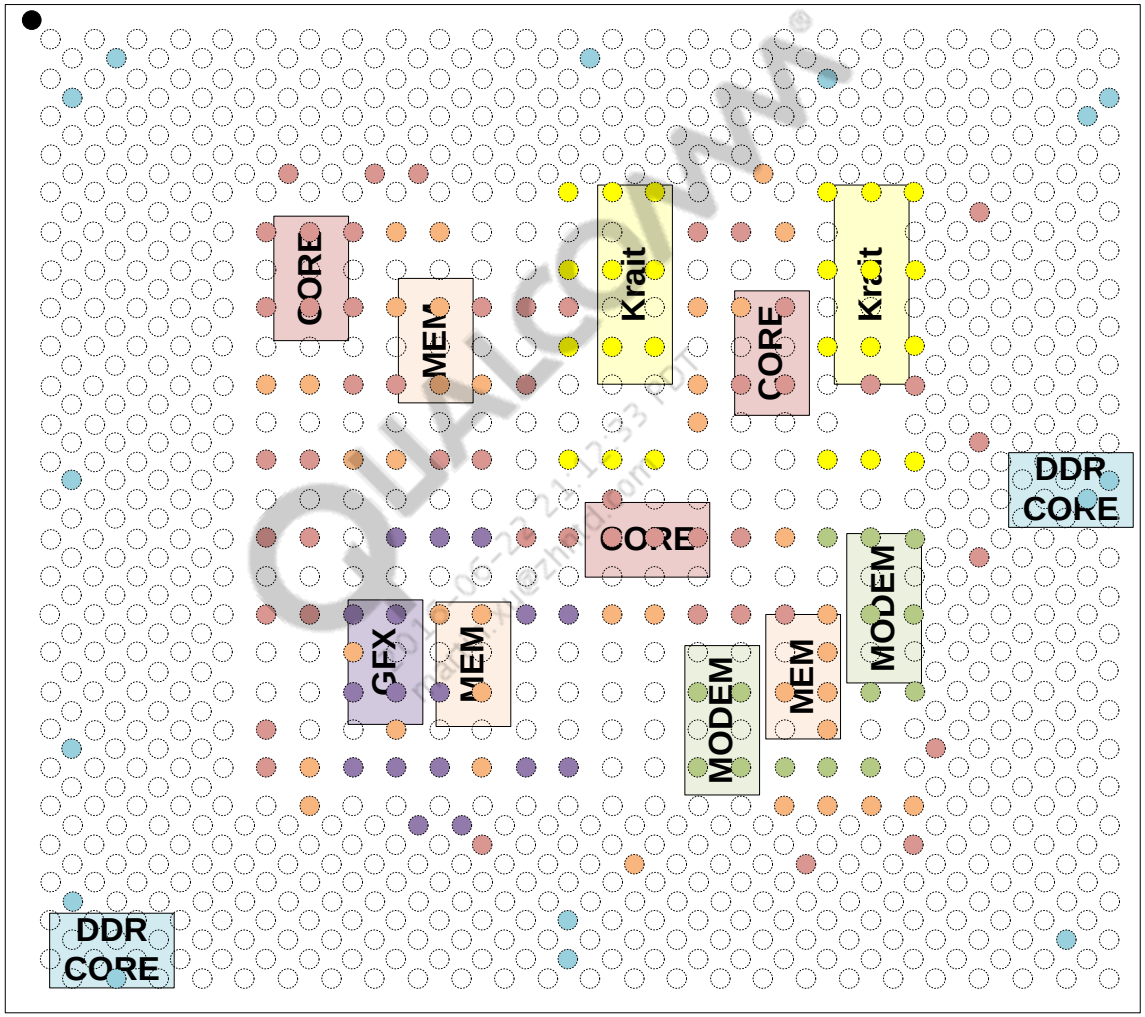
2) Backside – smaller loop



Recommended Capacitor Placement – Topside



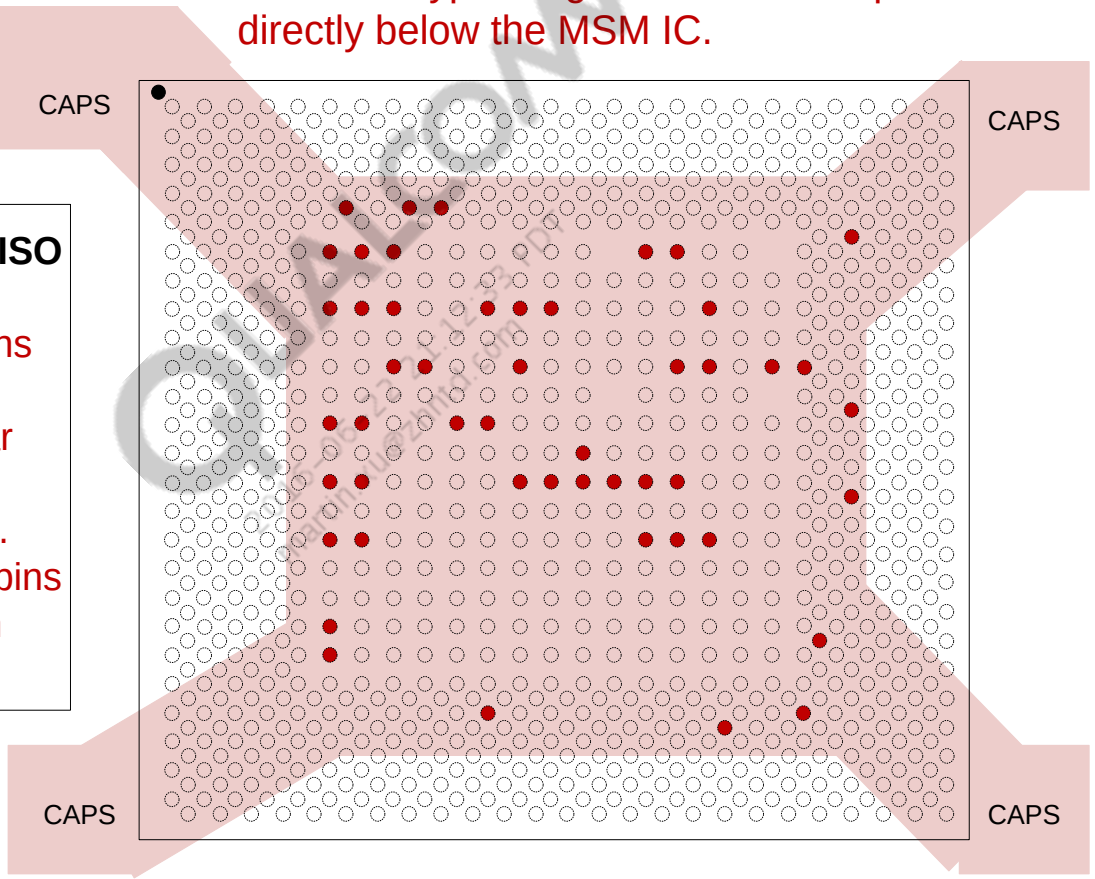
Recommended Capacitor Placement – Backside



Power Routing and Bypassing – Core Supply

- Recommended capacitor locations for topside bypassing – near the package corners.
- Backside bypassing would locate capacitors directly below the MSM IC.

Core power from PMIC



VREG_S2B_0P9_ISO Routing

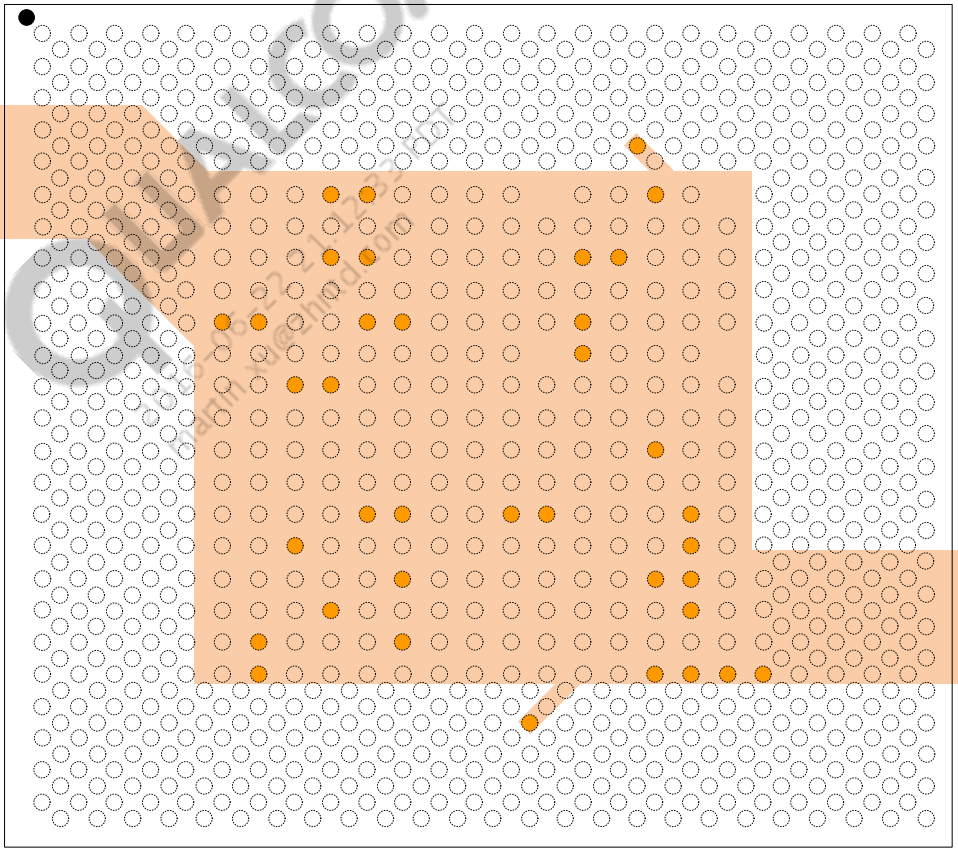
- It is critical the pins VDD_SDC_CDC, VDD_PLL1 are star routed to the VDD_CORE plane.
- Do not short the pins directly to the main VDD_CORE plane

Power Routing and Bypassing – Memory Supply

- Recommended capacitor locations for topside bypassing – near two package corners.
- Backside bypassing would locate capacitors directly below the MSM IC.

Memory power from PMIC

CAPS

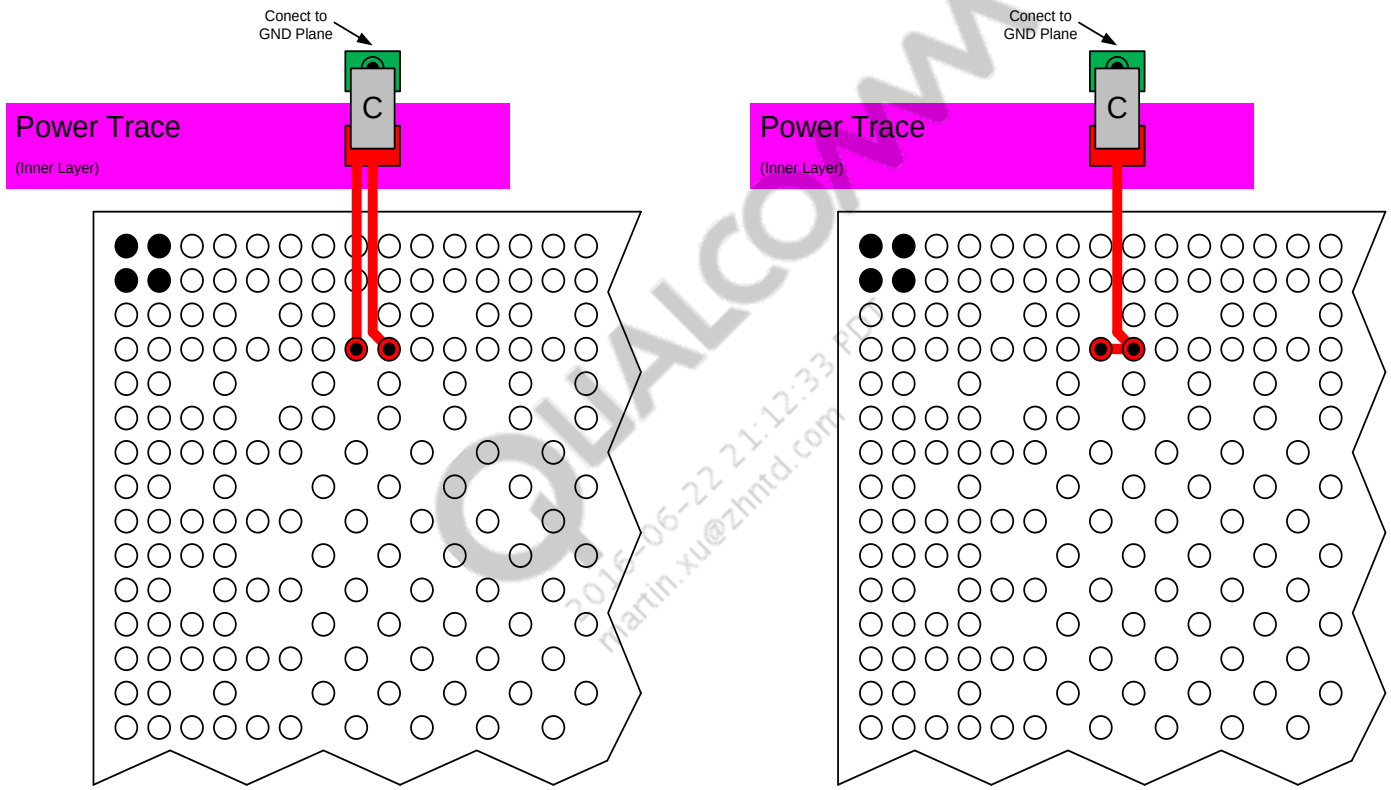


CAPS

VREG_S1B_0P95_ISO Routing

- It is critical the pins VDD_EBIx_PLL, VDD_EBIx_CDC, VDD_MEM(pin BD28) are star routed to the VDD_MEM plane.
- Do not short the pins directly to the main VDD_MEM plane

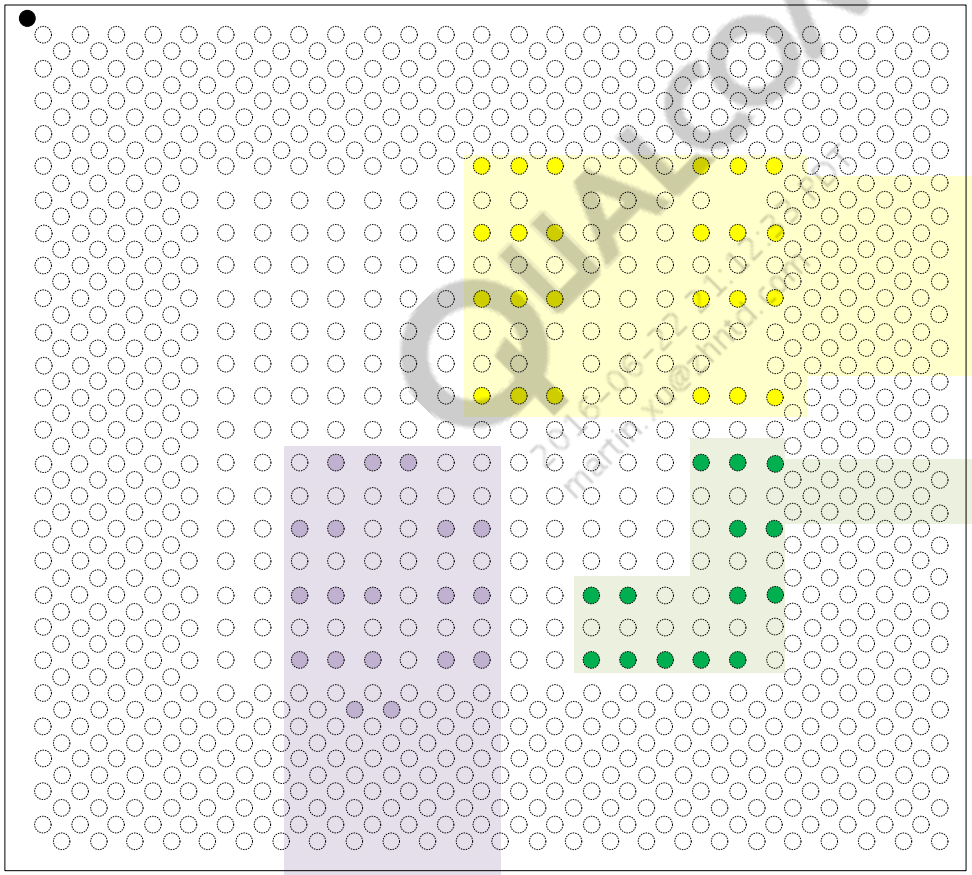
Star Routing Recommendation



CORRECT **INCORRECT**

Power Routing and Bypassing – Krait and Modem Supplies

- Recommended capacitor locations for topside bypassing – in line, near the package edges.
- Backside bypassing would locate capacitors directly below the MSM IC.



Krait power from PMIC

Modem power from PMIC

GFX power from PMIC

Power Routing and Bypassing – 1.2 V DDR Supply (1 of 3)

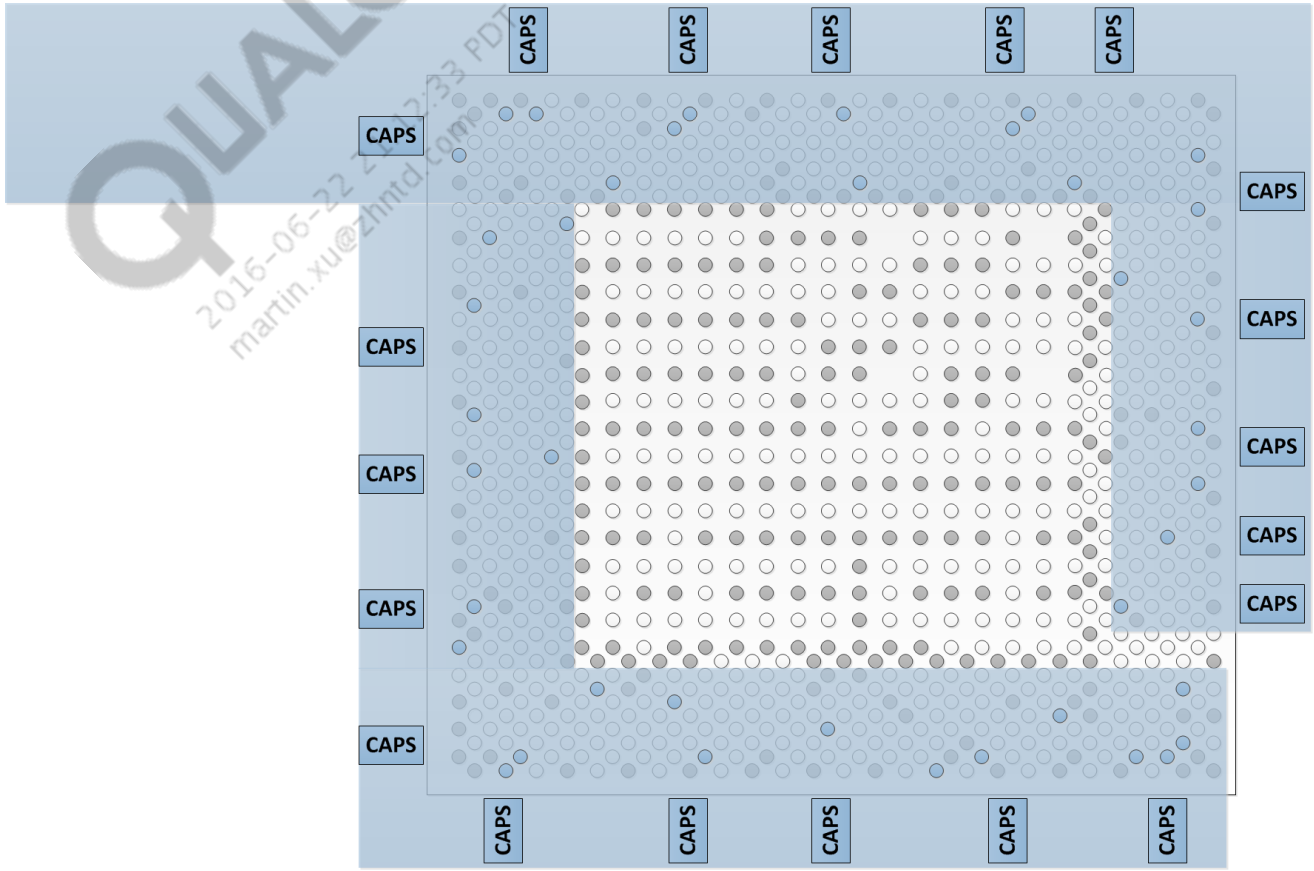
A wide power trace is required to route VDD_DDR_CORE/VDD_P1/VDD_P4 from PMIC to MSM to meet the PDN DC specification.

Each pin is required to have a decoupling capacitor close by.

A wide ring shape is required to cover all VDD_DDR_CORE/VDD_P1/VDD_P4 pins and capacitors.

- Ring is open at the far end to avoid RF radiation.
- Two branches should be equal length.

Power from PMIC

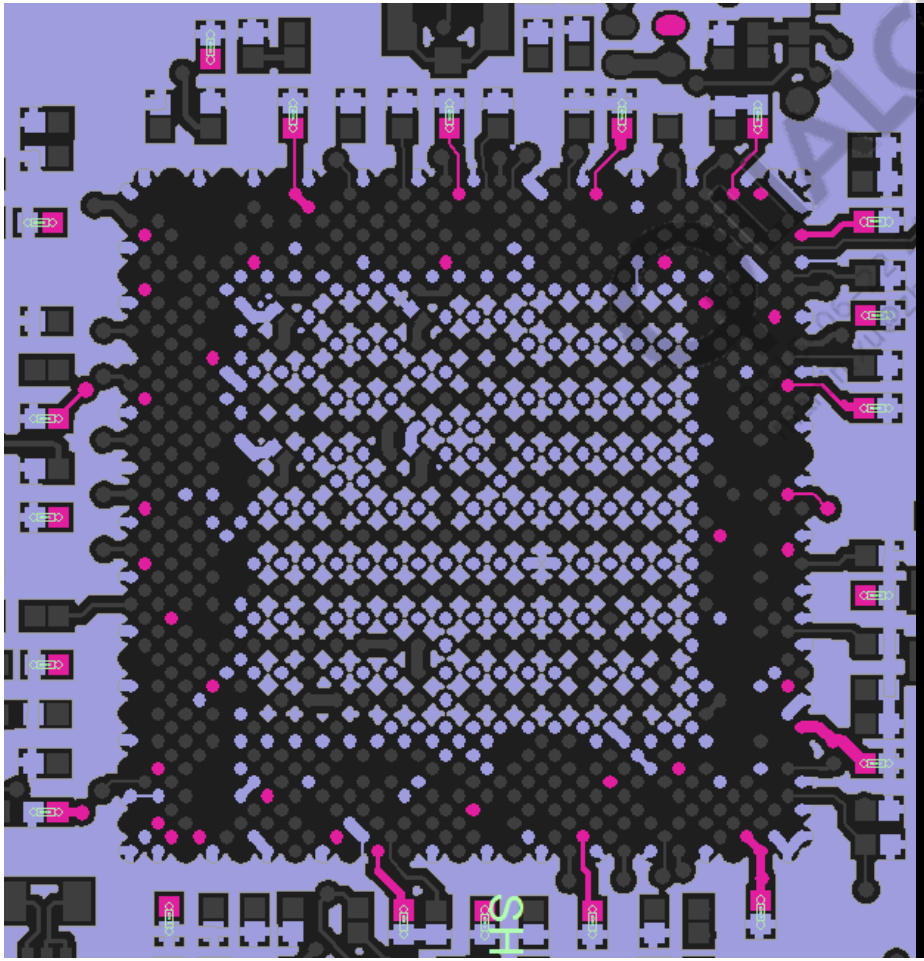


Power Routing and Bypassing – 1.2 V DDR Supply (2 of 3)

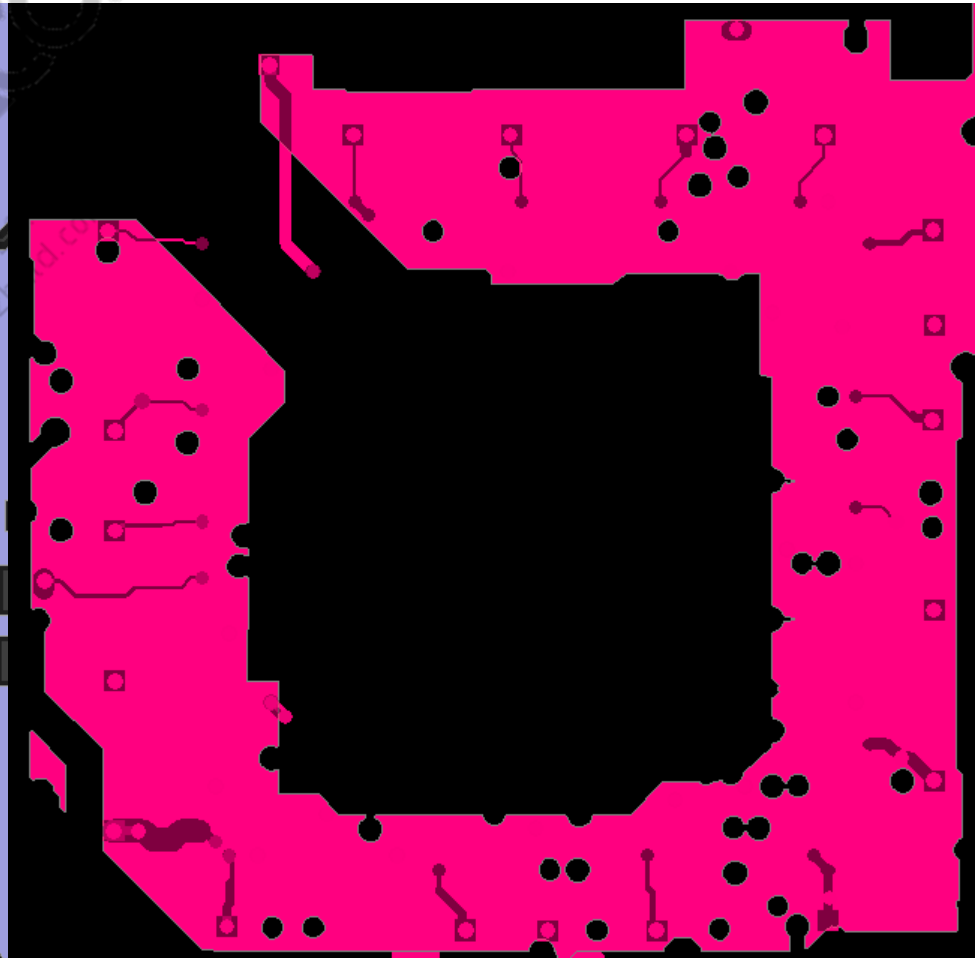
Layout example from the *Design Package, MSM8x74 ORCAD Library Symbol* (DP25-NA437-1).

- A wide ring to cover all power pins and decoupling capacitors
- Open at far end
- Two equal branches

Top layer and decoupling capacitor placement



Power shape across all layers

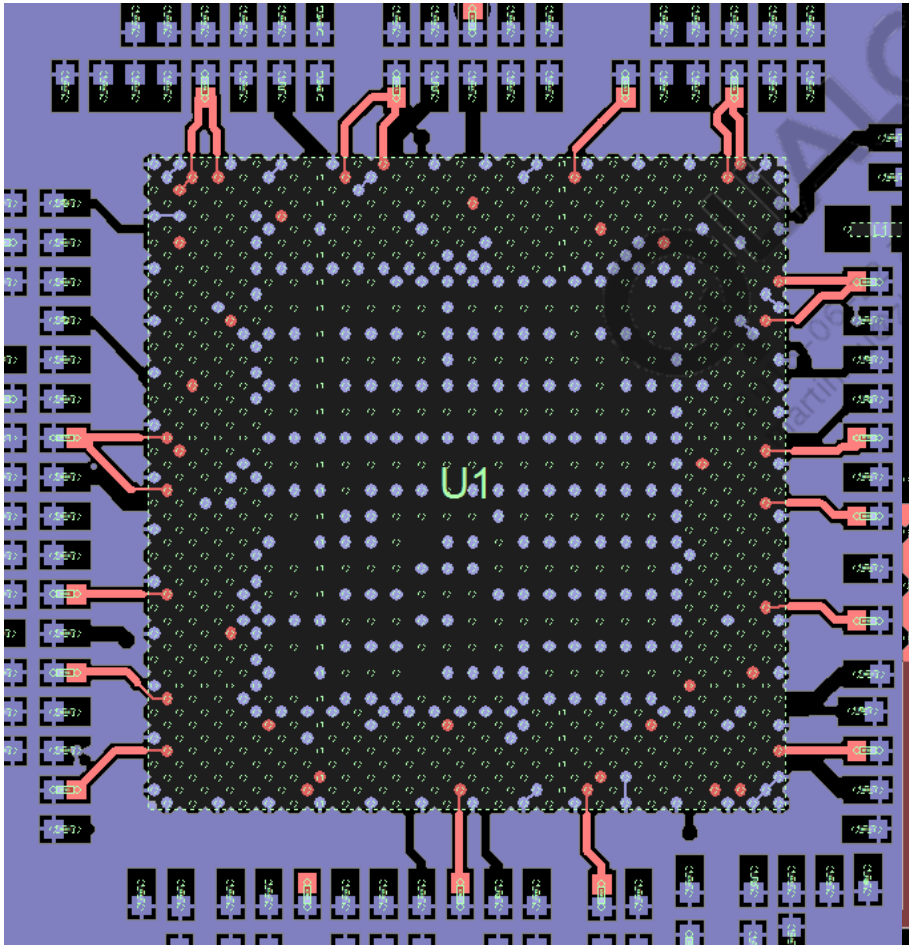


Power Routing and Bypassing – 1.2 V DDR Supply (3 of 3)

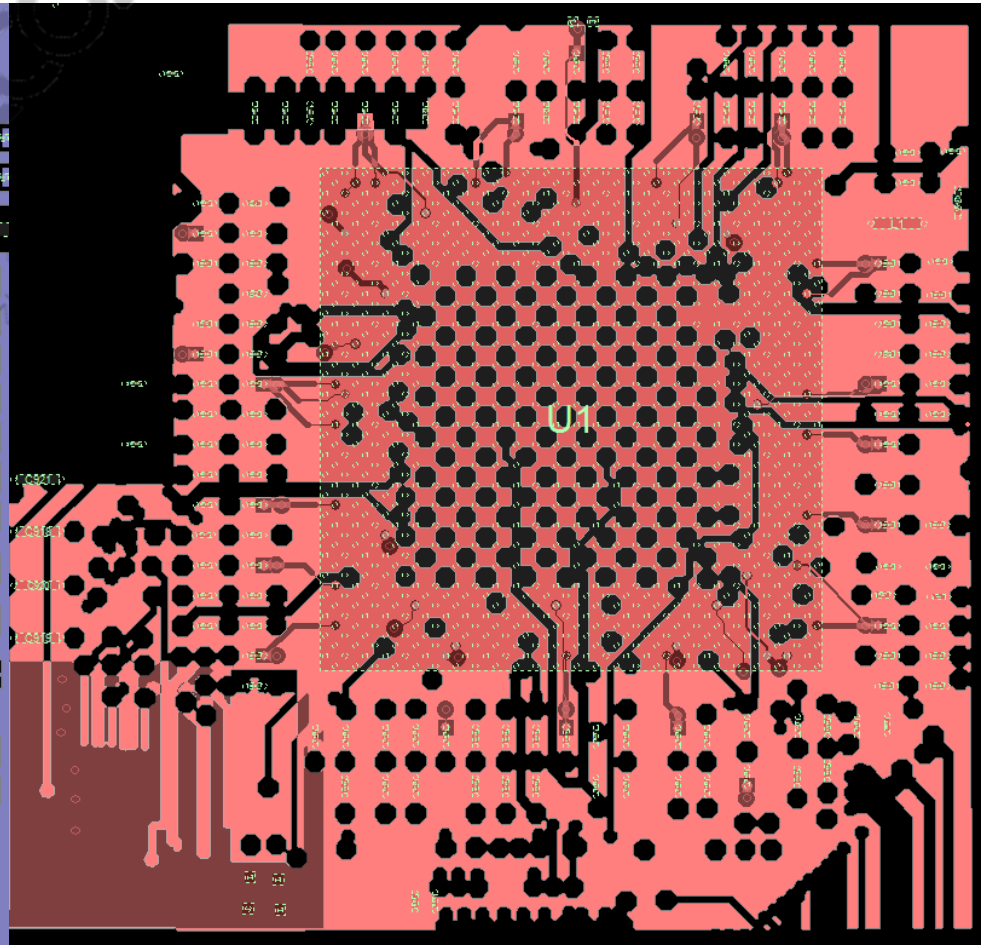
Layout example from the *Design Package, MSM8974 Breakout Study* (DP25-NA437-2).

- A large and solid power plane to cover all power pins and decoupling capacitors
- Better than ring-shape topology, but need more space

Top layer and decoupling capacitor placement



Power shape across all layers



Power Distribution Network Requirements

- PDN requirements are listed below.

Power domain	Max impedance DC to 10 Hz	Max impedance 10 Hz to 25 MHz
VDD_CORE	10 mΩ	Refer to the next slide.
VDD_GFX	10 mΩ	56 mΩ
VDD_KRAIT	2 mΩ	17 mΩ
VDD_MEM	10 mΩ	18 mΩ
VDD_MODEM	10 mΩ	57 mΩ
VDD_DDR_CORE_1P2/VDD_P1/VDD_P4	11 mΩ	14 mΩ

- Design guidelines are provided in the *Power Delivery Network Design* (80-VT310-13).

- The PDN spec for VDD_DDR_CORE_1P2/VDD_P1/VDD_P4 applies only for the MSM domain powered by VREG_L1_1P2.

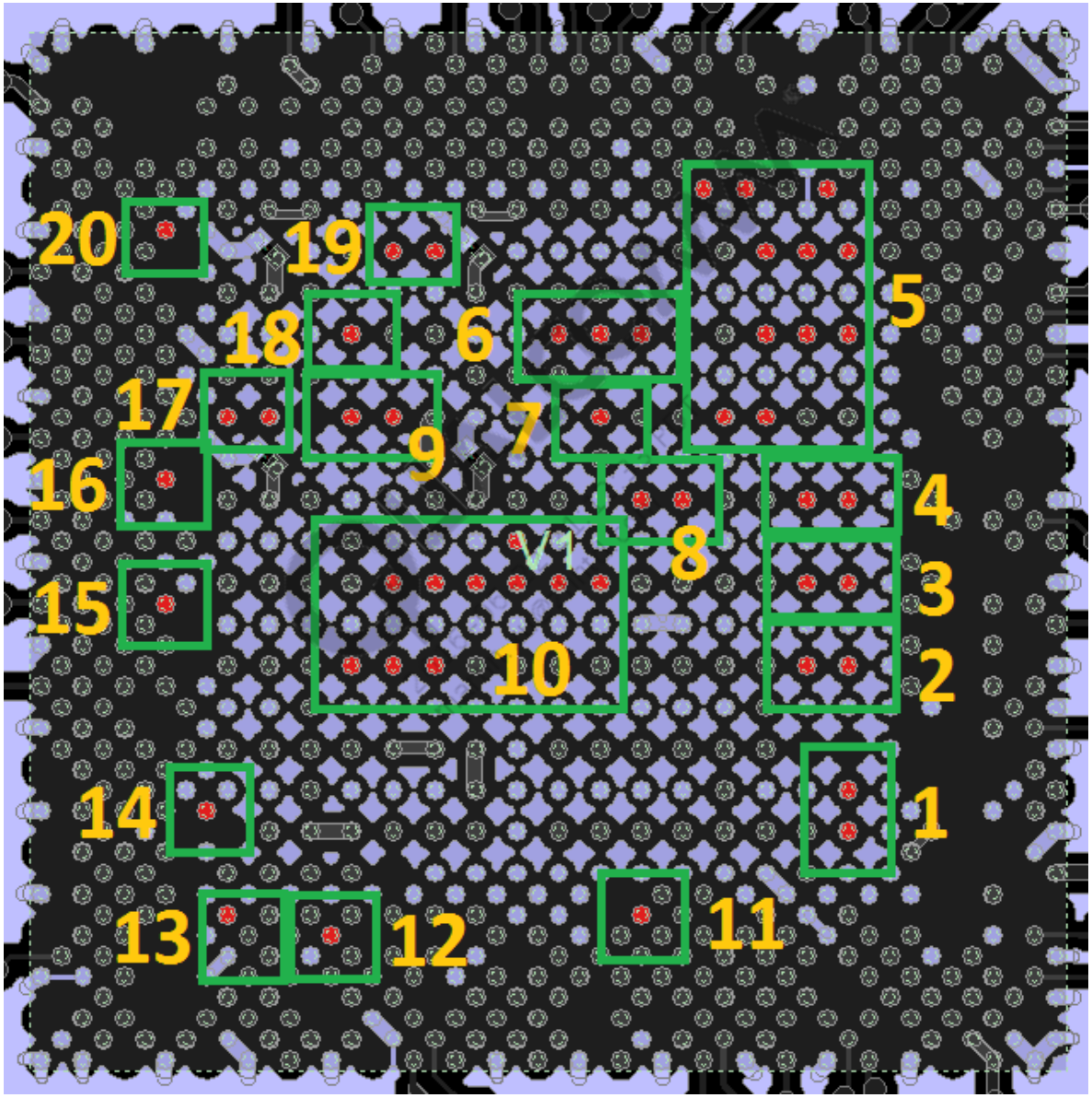
Note: 3-terminal caps are not recommended for the VDD1_P1/VDD_DDR_CORE_1P2 pins because the pins are distributed around the MSM chipset. It is strongly recommended to use 1 µF caps and place them close to the VDD pins for better performance.

VDD_CORE PDN AC Specification

Port number	Pin number of positive ports (VDD_CORE pins)	Pin number of negative ports (GND pins)	Max impedance
			10 Hz – 25 MHz
1	AU11, AW11	AR9, AU9, AU13, AW9, BA9, BA11,	55 mΩ
2	AL11, AL13	AJ9, AJ11, AJ13, AJ15, AL9, AN9, AN11, AN13	55 mΩ
3	AG11, AG13	AE9, AE11, AE13, AG9, AJ9, AJ11, AJ13, AJ15	55 mΩ
4	AC11, AC13	AA9, AA11, AA13, AA15, AC9, AE9, AE11, AE13, AE15	55 mΩ
5	H12, H16, H18, L11, L13, L15, R11, R13, R15, W15, W17	G13, H10, J11, J13, J15, J17, J19, N9, N11, N13, N15, N17, N19, R9, U9, U11, U13, U15, U17, U19, W9, AA9, AA11, AA13, AA15, AA17, AA19	55 mΩ
6	R21, R23, R25	N19, N21, R27, U19, U21, U23	55 mΩ
7	W23	U21, U23, W23, W25 AA21, AA25	55 mΩ
8	AC19, AC21	AA17, AA19, AA21, AC23, AE17, AE19, AE21, AE23	55 mΩ
9	W33, W35	U31, U33, U35, AA33, AA35, AA37	55 mΩ
10	AG23, AG25, AG27, AG29, AG31, AG33, AE27, AL31, AL33, AL35,	AC23, AC33, AC35, AE23, AE25, AE29, AE31, AE33, AJ23, AJ25, AJ27, AJ29, AJ31, AJ33, AJ35, AN23, AN25, AN27, AN29, AN31, AN33, AN35	55 mΩ
11	BC21	BA19, BA21, BA23	80 mΩ
12	BD36	BB34, BB36, BB37, BB38	80 mΩ
13	BC41	BB40, BB42, BD42	80 mΩ
14	AV42	AU41, AU43, AT42	80 mΩ
15	AH44	AF44, AG43, AJ41	80 mΩ
16	AB44	Y42, AA41, AD44	80 mΩ
17	W39, W41	V42, Y42	80 mΩ
18	R35	N35, R37, U35	80 mΩ
19	L31, L33	J31, J33, N31, N33	80 mΩ
20	K44	J43, K42, M42	80 mΩ

This is an update, replacing the original PDN AC spec of 22 mΩ for VDD_CORE listed in 80-NA437-1.

Port Assignments

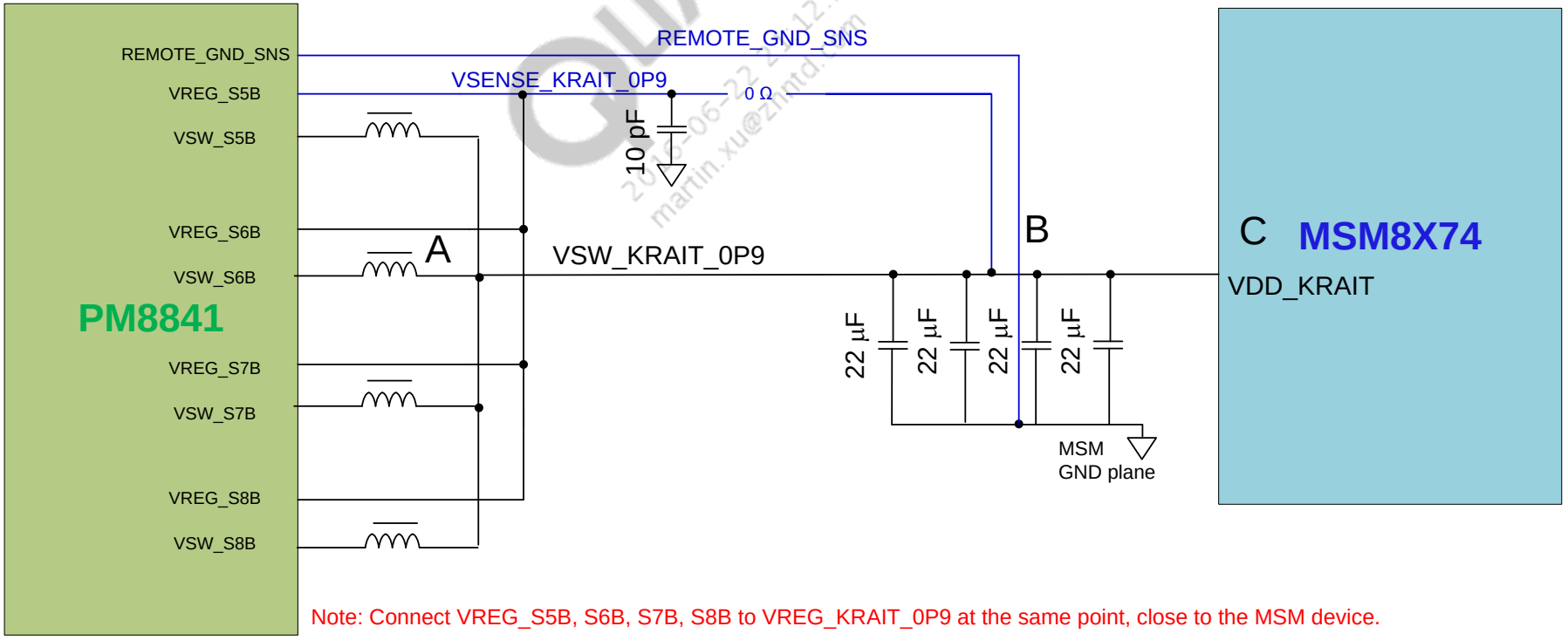


The positive terminal of each port above is highlighted in red.

Power Routing – VDD_KRAIT Power Supplies

- The feedback pins for S5B to S8B should be shorted together (point A) close to the PMIC side, and routed to a center point in the VDD_KRAIT area fill close to the MSM side.
- The REMOTE_GND_SNS pin of the PMIC should be routed to a center point in the GND area fill or plane close to the MSM side.
- The 2 mW PDN specification for VDD_KRAIT is from point B to C.
- The bulk capacitor placed close to the MSM device will help with better transient response.
- Remote sensing at the bulk capacitor close to the MSM device will help compensate for the DC resistance.

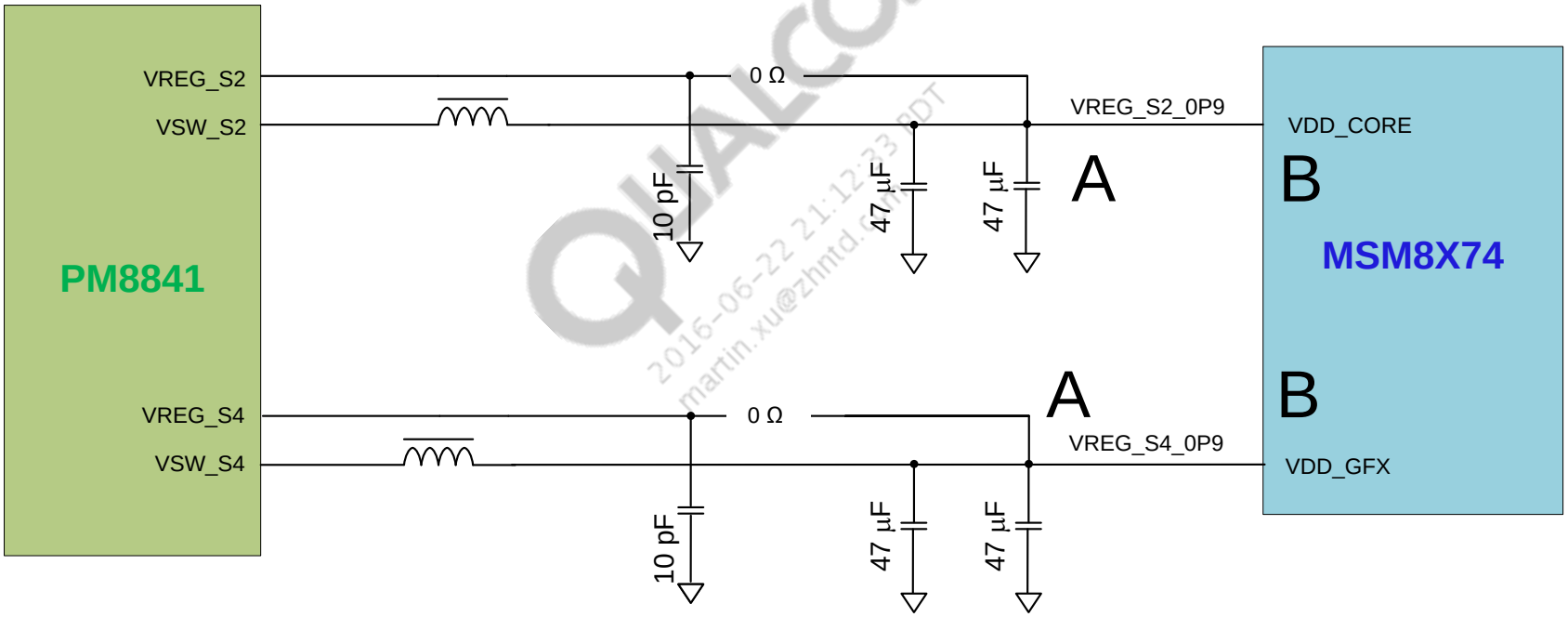
VSENSE_KRAIT_0P9 and REMOTE_GND_SNS need to be routed **differentially,** as shown in the following diagram.



Note: Connect VREG_S5B, S6B, S7B, S8B to VREG_KRAIT_0P9 at the same point, close to the MSM device.

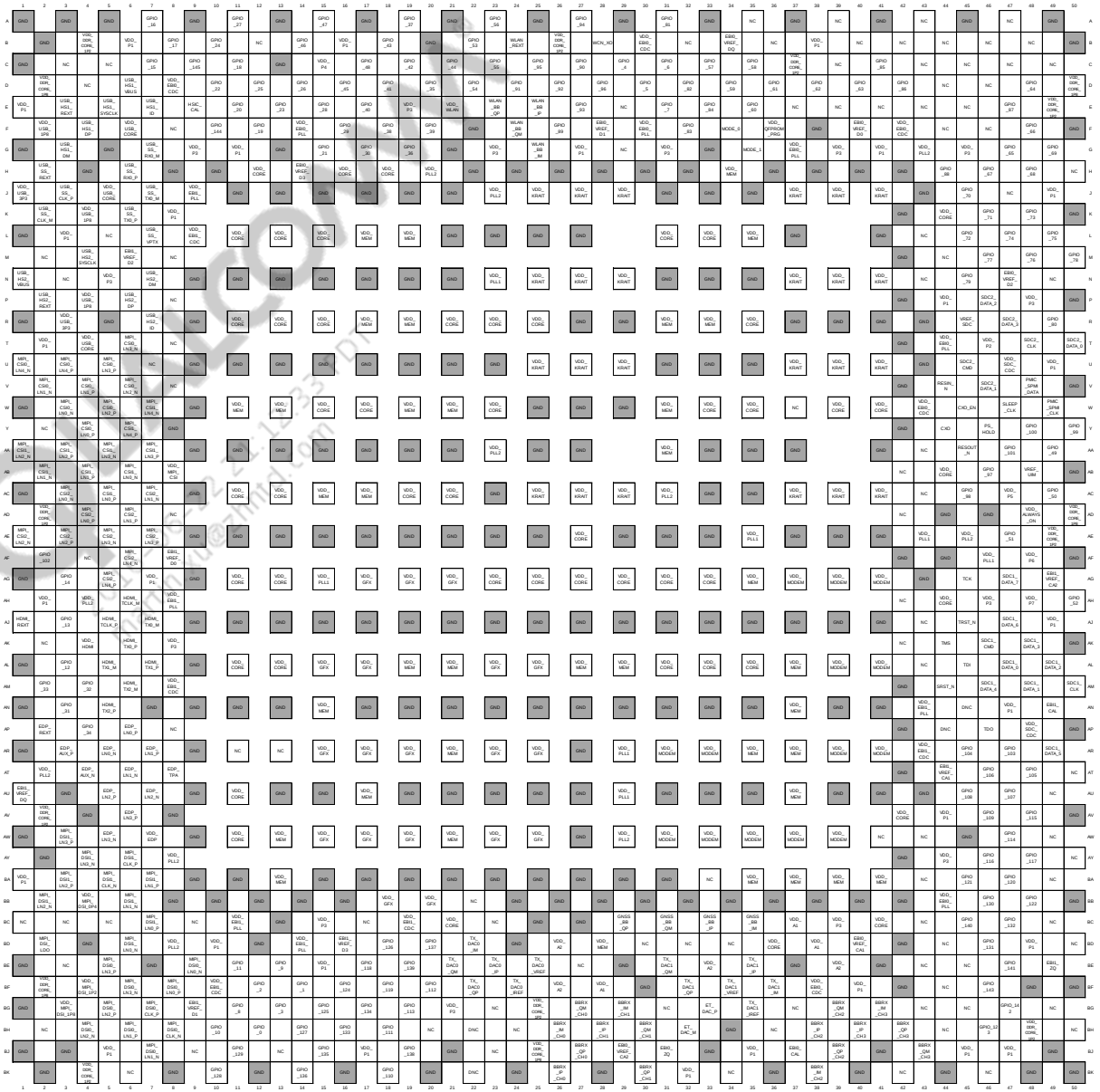
VDD_CORE and VDD_GFX Routing for MSM8974

- The 10 mΩ PDN spec for VDD_CORE/VDD_GFX is from point A to B.
- The bulk capacitors for VREG_S2 and VREG_S4 should be placed close to the MSM device.
- The bulk capacitor placed close to the MSM device will help with better transient response.
- Remote sensing at the bulk capacitor close to MSM device will help to compensate for the DC resistance.



MSM Ground Connections

- All grounds are shared and can be tied together on any layers.
- Microvia to layers 2 and 3 from top.
- Microvia to layers 9 and 8 from bottom.
- Core vias connect layers 3 and 8 to inner layers.
- Primary ground layers are 4 and 7.
- Connect lots of metal on multiple layers for best thermal conduction.



Handling Unused MSM Pins

Signal	Unused pin state	Comments
HDMI		
HDMI_TCLK_x	Floating	
HDMI_TXx_x	Floating	
HDMI_CEC	Floating	or as regular GPIO
HDMI_DDC_CLK	Floating	or as regular GPIO
HDMI_DDC_DATA	Floating	or as regular GPIO
HDMI_HOT_PLUG_DETECT	Floating	or as regular GPIO
HDMI_REXT	Floating	
VDD_HDMI	Floating	
CSI		
MIPI_CSIx_LNx_x	Floating	
VDD_MIPI_CSI	GND	Only when ALL CSI ports are not used
DSI		
MIPI_DSIx_LNx_x	Floating	
MIPI_DSIx_CLK_x	Floating	
VDD_MIPI_DSI_1P2	GND	Only when ALL DSI ports are not used
VDD_MIPI_DSI_1P8	GND	Only when ALL DSI ports are not used
VDD_MIPI_DSI_0P4	GND	Only when ALL DSI ports are not used
MIPI_DSI_LDO	GND	Only when ALL DSI ports are not used
UIM/HSIC		
VDD_P5 UIM1	VREG_S3A_1P8	GPIOs can be used as regular GPIO
VDD_P6 UIM2	VREG_S3A_1P8	GPIOs can be used as regular GPIO
VDD_P4 HSIC	VREG_S3A_1P8	GPIOs can be used as regular GPIO
eDP		
EDP_AUX_x	Floating	
EDP_LANEx_x	Floating	
EDP_REXT	Floating	
VDD_EDP	Floating	

Signal	Unused pin state	Comments
BBRX		
BBRX_IP/IM_CHx	Floating	
BBRX_QP/QM_CHx	Floating	
VDD_A2 pin BD26	Connected to power supply	
VDD_A1 pin BF28	Connected to power supply	
VDD_A2 pin BE39	Connected to power supply	
VDD_A1 pin BD38	Connected to power supply	
GNSS		
GNSS_BB_IP/IM	Floating	
GNSS_BB_QP/QM	Floating	
VDD_A1 pin BC37	GND	If WTR1605L GPS solution is not used
WLAN		
WLAN_BB_IP/IM	GND	
WLAN_BB_QP/QM	GND	
WCN_XO	GND	
WLAN_REXT	GND	
VDD_WLAN	GND	

TXDAC1 and ETDAC Connections for Different RF Configurations

All use cases below use TXDAC0 dedicated for WTR0.

		VDD_A2 pin BE33	TX_DAC1 I/Q	ETDAC_P/M	TX_DAC1_IREF	TX_DAC1_VREF
Single WTR designs such as ATT CSFB (with one WTR1605L/WTR125L) or Carrier Aggregation (CA) with WTR1625L + WFR1620						
TX_DAC1_I/Q Unused	**ET Unused**	GND	GND	Floating	GND	GND
TX_DAC1_I/Q Unused	**ET Used**	PM8941 VREG_L14	GND	QFE1100 AMP_INP/M	PM8941 VREG_L14	PM8941 MPP_03
Two WTR designs such as CA (WTR1605L + WTR1605L), or SVLTE (WTR1605L + WTR1605) or SVLTE (WTR1625L + WTR1625)						
TX_DAC1_I/Q Used	**ET Unused**	PM8941 VREG_L14	WTR1_I/Q	Floating	WTR1_DAC_IREF	PM8941 MPP_03
TX_DAC1_I/Q Used	**ET Used**	PM8941 VREG_L14	WTR1_I/Q	QFE1100 AMP_INP/M	WTR1_DAC_IREF	PM8941 MPP_03

	TXDAC1_IP/IM	TXDAC1_QP/QM	VDD_A2 pin BE33	ETDAC_P/M	TX_DAC1_IREF	TX_DAC1_VREF
Two WTR SGLTE design with WTR1625L + WTR2100						
ET Unused	GND	WTR2100 TX_BB_QP/QM	PM8941 VREG_L14	Floating	WTR1_DAC_IREF	PM8941 MPP_03
ET Used	GND	WTR2100 TX_BB_QP/QM	PM8941 VREG_L14	QFE1100 AMP_INP/M	WTR1_DAC_IREF	PM8941 MPP_03

Note: WTR1625(L) is **only** supported by the MSM8974AB chipset.

Questions?

https://support.cdmatech.com