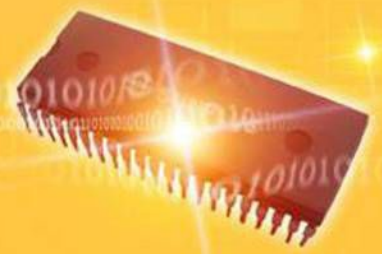
嵌入式系统工程师



s5pv210中断控制系统

大纲

- s5pv210中断概述
- s5pv210中断工作过程
- 相关寄存器使用说明
- 应用举例——外部中断事件

s5pv210中断控制系统

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s5pv210中断概述

- 外设与CPU之间数据请求方式有以下三种:
  - **查询方式:**

    CPU不断查询外设状态，如果外设准备就绪就开始传输数据，如果外设还没有准备好，就继续循环查询
  - **中断方式:**

    当外设准备好与CPU进行数据交换时，首先向CPU提出中断请求，CPU接到中断请求并在一定条件下，暂停原来的程序，转去执行中断服务程序，完成数据传输过程，执行完成后再次返回到原程序继续执行
  - **DMA方式:**

    不经过CPU而直接按照事前约定的方式进行数据传输

s5pv210中断概述

- 中断定义:

  当CPU正在执行程序时，系统发生了一件急需处理的事件，CPU把正在执行的程序暂停，转去处理相应的事件，事件处理完后，CPU再返回继续执行原来的程序，这种情况称为中断

- 中断源及中断事件:

  能够引起CPU产生中断，并且与CPU当前所执行的程序无直接关系的系统内部模块或外部硬件，叫中断源；引起中断的事件，叫中断事件

s5pv210中断概述

- 中断的分类
  - IRQ，普通中断，用于处理一般事件
  - FIQ，快速中断，一般用于实时性要求较高的情况
- 中断的管理
  - s5pv210通过4个TZIC(TrustZone Interrupt Controller)和4个VIC(Vectored Interrupt Controller)进行中断管理。TZIC为中断的安全访问得到了保证
- 中断的仲裁
  - s5pv210的中断仲裁过程交给了硬件去做，直接将中断服务函数入口和VICnVECTADDRm寄存器绑定即可，无需设置中断向量表，使得中断编程更加方便灵活

s5pv210中断概述

- 中断源介绍
  - s5pv210中断共有93个中断源，被分成4组，所对应的中断号以及应用领域详情可参考page560
  - 237个IO口中有178个(除GPI、MP0)都支持中断
  - GPH0-3做为专用外部中断(共32个外部中断，17个中断源)，有着自己独立的中断控制寄存器,而其它146个GPIO中断共享同一中断源（VIC0的30号）
  - 其余中断源作为系统内部各个模块请求信号，由相应模块控制寄存器共同配置，如：ADC、TIMER、UART等等

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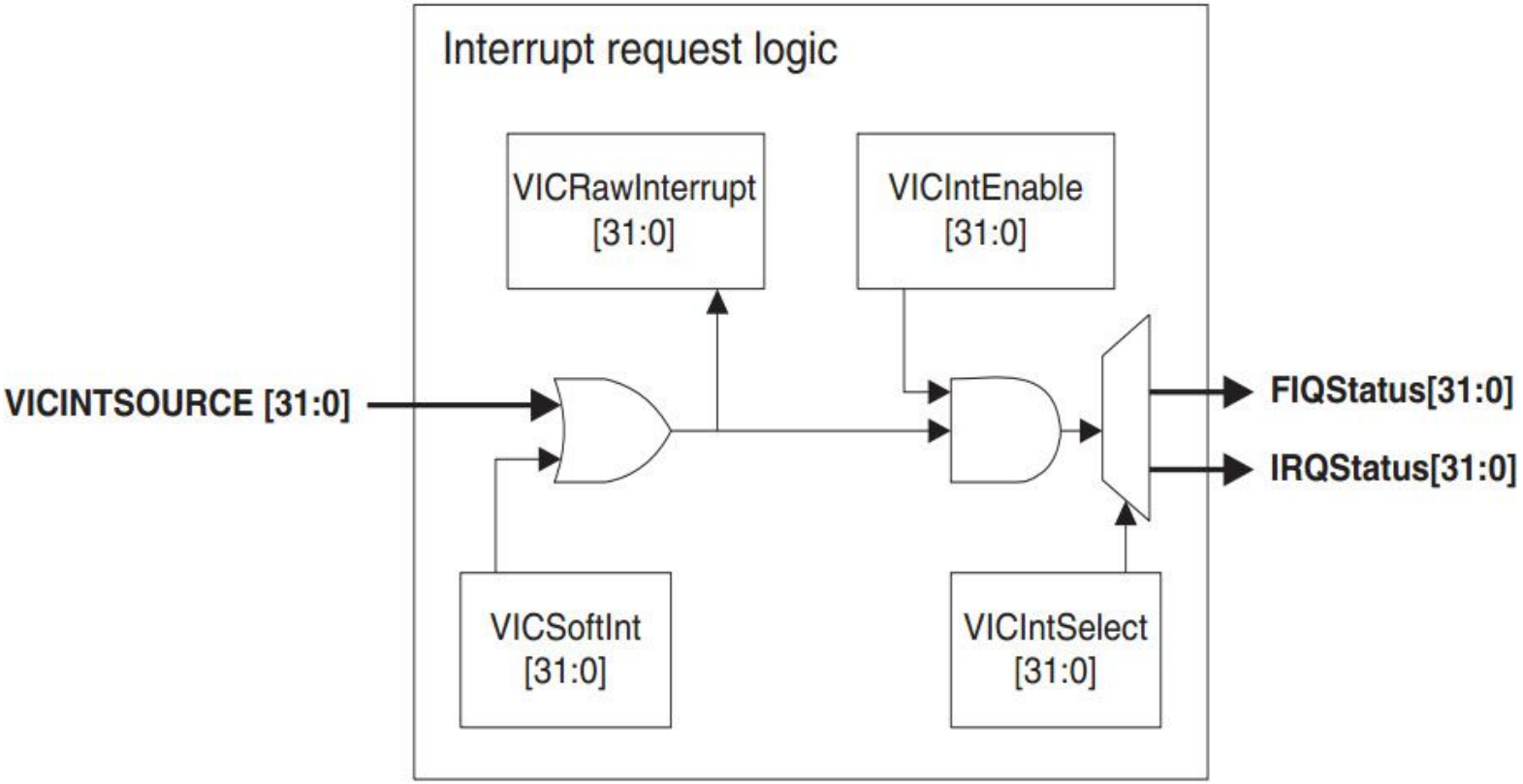
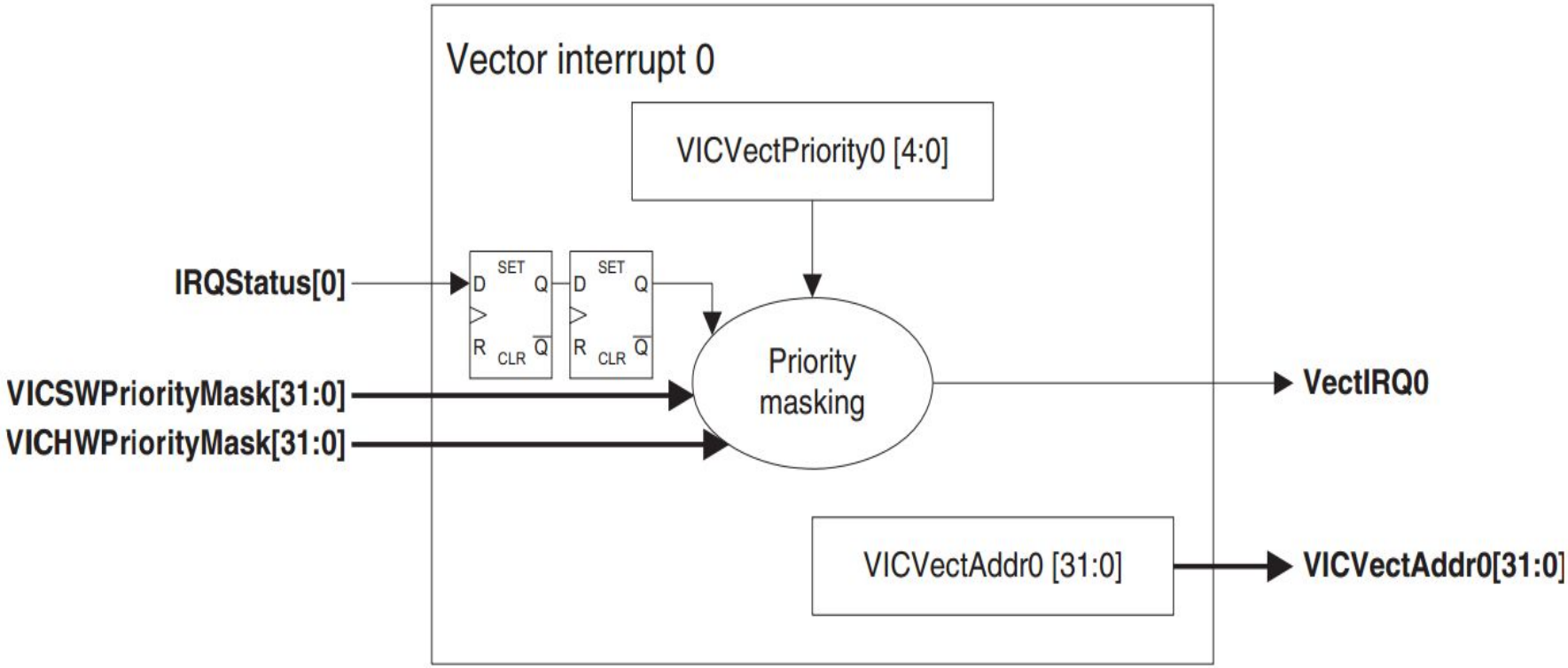
s5pv210中断工作过程

➢ 中断请求逻辑



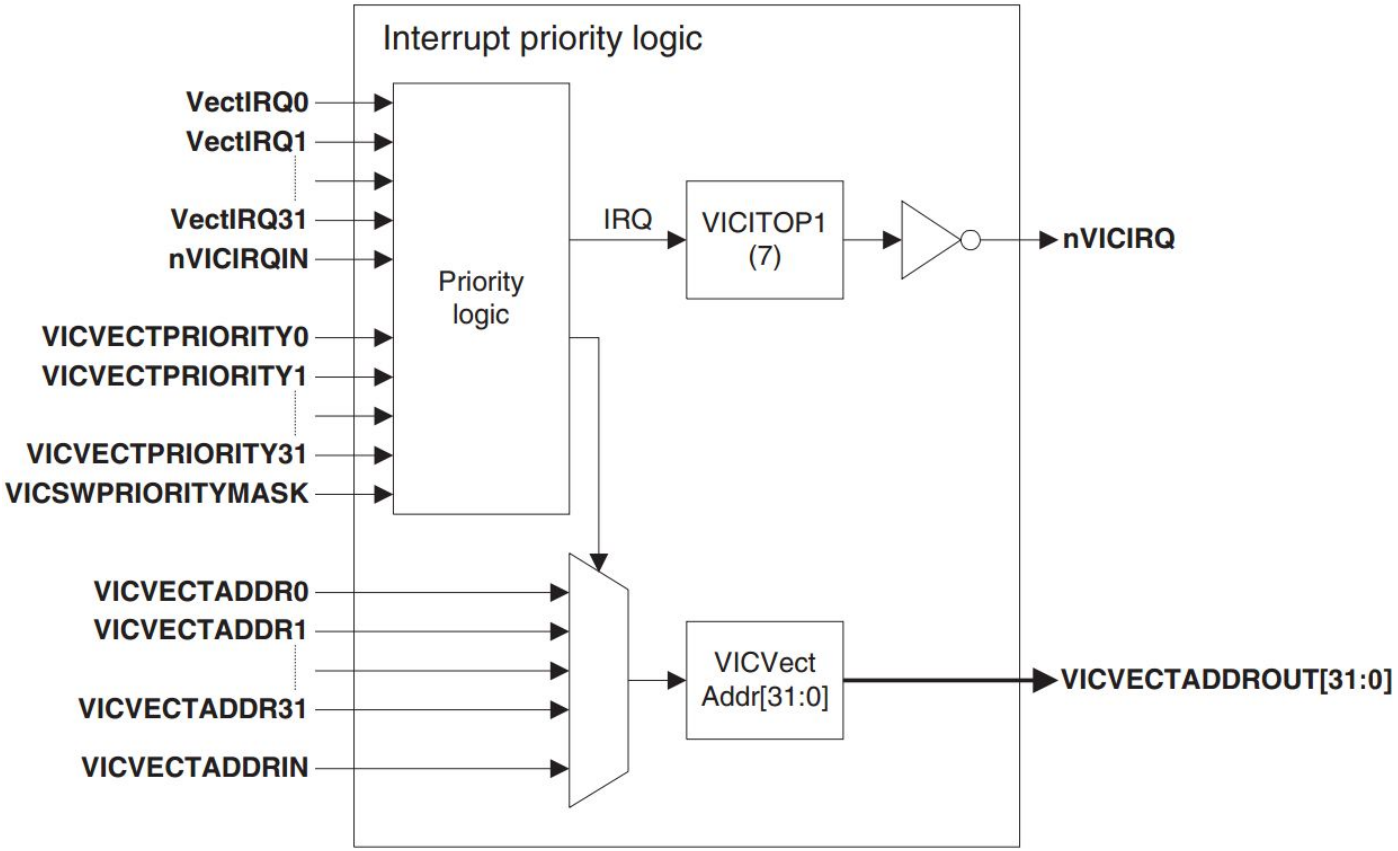
s5pv210中断工作过程

➢ IRQ中断响应过程



s5pv210中断工作过程

➢中断优先级逻辑结构



s5pv210中断工作过程

- 注意事项：
  - 中断优先级只针对IRQ中断进行设置
  - 当不同优先级中断同时被触发时，高优先级的中断先得到服务
  - IRQ中断被分成16个中断优先级，默认所有中断在同一优先级（page581）
  - IRQ中断不能嵌套，即使高优先级也必须等到当前中断服务结束才能被处理，又称硬件屏蔽
  - 当相同优先级中断被触发时，由硬件裁决，中断号0最高，31号最低
  - 中断服务程序的回调是通过VIC中断向量控制器自动实现的

s5pv210中断工作过程

- 中断响应过程总结： 中断源->VIC->CPU

中断源	中断控制器	CPU处理
中断源配置，使得中断源可以正常触发中断事件	对产生的中断事件进行裁决(使能/类型/优先级/中断服务入口地址)	设置总中断开关，执行中断服务程序

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相关寄存器使用说明

- VICSOFTINT：通过该寄存器可以通过软件触发中断请求，完成后还要清除掉(类似PENDING)

1.4.1.7 Software Interrupt Register
(VICSOFTINT, R/W, Address=0xF200_0018, 0xF210_0018, 0xF220_0018, 0xF230_0018)

VICSOFTINT	Bit	Description	Initial State
SoftInt	[31:0]	Setting a bit HIGH generates a software interrupt for the selected source before interrupt masking. Read: 0 = Software interrupt inactive 1 = Software interrupt active Write: 0 = No effect 1 = Enables Software interrupt There is one bit of the register for each interrupt source.	0x00000000

1.4.1.8 Software Interrupt Clear Register
(VICSOFTINTCLEAR, W, Address=0xF200_001C, 0xF210_001C, 0xF220_001C, 0xF230_001C)

VICSOFTINTCLEAR	Bit	Description	Initial State
SoftIntClear	[31:0]	Clears corresponding bits in the VICSOFTINT Register: 0 = No effect 1 = Disables Software interrupt in the VICSOFTINT Register. There is one bit of the register for each interrupt source.	-

相关寄存器使用说明

- VICRAWINTR：只读，记录经过中断源屏蔽选择后保留下来的原始中断

1.4.1.3 Raw Interrupt Status Register
(VICRAWINTR, R, Address=0xF200_0008, 0xF210_0008, 0xF220_0008, 0xF230_0008)

VICRAWINTR	Bit	Description	Initial State
RawInterrupt	[31:0]	Shows the status of the FIQ interrupts before masking by the VICINTENABLE and VICINTSELECT Registers: 0 = Interrupt is inactive before masking 1 = Interrupt is active before masking Because this register provides a direct view of the raw interrupt inputs, the reset value is unknown. There is one bit of the register for each interrupt source.	-

相关寄存器使用说明

- VICINTENABLE：中断向量使能寄存器，只能用于使能中断，即决定中断将来能否被送到处理器执行

1.4.1.5 Interrupt Enable Register
(VICINTENABLE, R/W, Address=0xF200_0010, 0xF210_0010, 0xF220_0010, 0xF230_0010)

VICINTENABLE	Bit	Description	Initial State
IntEnable	[31:0]	Enables the interrupt request lines, which allows the interrupts to reach the processor. Read: 0 = Disables Interrupt 1 = Enables Interrupt Use this register to enable interrupt. The VICINTENCLEAR Register must be used to disable the interrupt enable. Write: 0 = No effect 1 = Enables Interrupt. On reset, all interrupts are disabled. There is one bit of the register for each interrupt source.	0x00000000

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相关寄存器使用说明

- VICINTENCLEAR：禁止相关中断请求，使得VICINTENABLE寄存器对应位为0，禁止中断继续往上提交

1.4.1.6 Interrupt Enable Clear
(VICINTENCLEAR, W, Address=0xF200_0014, 0xF210_0014, 0xF220_0014, 0xF230_0014)

VICINTENCLEAR	Bit	Description	Initial State
IntEnable Clear	[31:0]	Clears corresponding bits in the VICINTENABLE Register: 0 = No effect 1 = Disables Interrupt in VICINTENABLE Register. There is one bit of the register for each interrupt source.	-

相关寄存器使用说明

- VICINTSELECT：中断类型选择寄存器，类似于2440中的中断模式寄存器，选择该中断为IRQ还是FIQ

1.4.1.4 Interrupt Select Register
(VICINTSELECT, R/W, Address=0xF200_000C, 0xF210_000C, 0xF220_000C, 0xF230_000C)

VICINTSELECT	Bit	Description	Initial State
IntSelect	[31:0]	Selects interrupt type for interrupt request: 0 = IRQ interrupt 1 = FIQ interrupt There is one bit of the register for each interrupt source.	0x00000000

相关寄存器使用说明

- VICIRQSTATUS：IRQ中断状态寄存器，只读，由VICINTENABLE和VICINTSELECT选通，通过后的状态位由VICRAWINTR决定

1.4.1.1 IRQ Status Register
(VICIRQSTATUS, R, Address=0xF200_0000, 0xF210_0000, 0xF220_0000, 0XF230_0000)

VICIRQSTATUS	Bit	Description	Initial State
IRQStatus	[31:0]	Shows the status of the interrupts after masking by the VICINTENABLE and VICINTSELECT Registers: 0 = Interrupt is inactive 1 = Interrupt is active. There is one bit of the register for each interrupt source.	0x00000000

1.4.1.2 FIQ Status Register
(VICFIQSTATUS, R, Address=0xF200_0004, 0xF210_0004, 0xF220_0004, 0xF230_0004)

VICFIQSTATUS	Bit	Description	Initial State
FIQStatus	[31:0]	Shows the status of the FIQ interrupts after masking by the VICINTENABLE and VICINTSELECT Registers: 0 = Interrupt is inactive 1 = Interrupt is active. There is one bit of the register for each interrupt source.	0x00000000

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相关寄存器使用说明

- 中断服务程序入口地址，用户可以通过这个寄存器配置各中断源中断入口地址

1.4.1.12 Vector Address Registers (VICVECTADDR[0-31], R/W, Address=0xF200_0100~017C, 0xF210_0100~017C, 0xF220_0100~017C, 0xF230_0100~017C)

VICVECTADDR[0-31]	Bit	Description	Initial State
VectorAddr 0-31	[31:0]	Contains ISR vector addresses.	0x00000000

- 设定中断源优先级，93个中断源共享16个优先级

1.4.1.13 Vector Priority Registers (VICVECTPRIORITY[0-31] and VICVECTPRIORITYDAISY, R/W, Address=0xF200_0200~027C, 0xF210_0200~027C, 0xF220_0200~027C, 0xF230_0200~027C)

VICVECTPRIORITY[0-31] and VICVECTPRIORITYDAISY	Bit	Description	Initial State
Reserved	[31:4]	Reserved, read as 0, do not modify.	0x0
VectPriority	[3:0]	Selects vectored interrupt priority level. You can select any of the 16 vectored interrupt priority levels by programming the register with the hexadecimal value of the priority level required, from 0-15.	0xF

相关寄存器使用说明

- 中断向量地址寄存器，可以通过该寄存器，读取当前正在被执行的中断服务程序的入口地址，写0可以清除当前中断，否则下次将不再响应

1.4.1.10 Vector Address Register
(VICADDRESS, R/W, Address=0xF200_0F00, 0xF210_0F00, 0xF220_0F00, 0xF230_0F00)

VICADDRESS	Bit	Description	Initial State
VectAddr	[31:0]	Contains the address of the currently active ISR, with reset value 0x00000000. A read of this register returns the address of the ISR and sets the current interrupt as being serviced. A read must be performed while there is an active interrupt. A write of any value to this register clears the current interrupt. A write must only be performed at the end of an interrupt service routine.	0x00000000

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外部中断事件

- 专用外部中断（32个）- GPH[3:0],它们有自己独立的中断控制寄存器组，分别是:
  - EXT_INT_x_MASK: 中断屏蔽寄存器，0使能，1屏蔽
  - EXT_INT_x_PEND: 中断挂起寄存器，0表示没有发生中断，1表示产生了中断请求，写1可以清除中断标志
  - EXT_INT_x_CON: 主要配置各组中各个中断触发方式(低电平、高电平、上升、下降、双沿)
  - EXT_INT_x_FLTCONx: 中断滤波控制寄存器，是否开起数字滤波功能，开启后会更加稳定
  - 【注】: x=0-3，每一组寄存器配置8个端口

外部中断事件

2.2.60.13 External Interrupt Control Registers (EXT_INT_0_MASK, R/W, Address = 0xE020_0F00)

EXT_INT_0_MASK	Bit	Description	Initial State
Reserved	[31:8]	Reserved	0
EXT_INT_0_MASK[7]	[7]	0 = Enables Interrupt 1 = Masked	1
EXT_INT_0_MASK[6]	[6]	0 = Enables Interrupt 1 = Masked	1
EXT_INT_0_MASK[5]	[5]	0 = Enables Interrupt 1 = Masked	1
EXT_INT_0_MASK[4]	[4]	0 = Enables Interrupt	1

2.2.60.17 External Interrupt Control Registers (EXT_INT_0_PEND, R/W, Address = 0xE020_0F40)

EXT_INT_0_PEND	Bit	Description	Initial State
Reserved	[31:8]	Reserved	0
EXT_INT_0_PEND[7]	[7]	0 = Not occur 1 = Occur interrupt	0
EXT_INT_0_PEND[6]	[6]	0 = Not occur 1 = Occur interrupt	0
EXT_INT_0_PEND[5]	[5]	0 = Not occur 1 = Occur interrupt	0

外部中断事件

2.2.60.1 External Interrupt Control Registers (EXT_INT_0_CON, R/W, Address = 0xE020_0E00)

EXT_INT_0_CON	Bit	Description	Initial State
Reserved	[31]	Reserved	0
EXT_INT_0_CON[7]	[30:28]	Sets the signaling method of EXT_INT[7] 000 = Low level 001 = High level 010 = Falling edge triggered 011 = Rising edge triggered 100 = Both edge triggered 101 ~ 111 = Reserved	000
Reserved	[27]	Reserved	0
EXT_INT_0_CON[6]	[26:24]	Sets the signaling method of EXT_INT[6]	000

2.2.60.5 External Interrupt Control Registers (EXT_INT_0_FLTCON0, R/W, Address = 0xE020_0E80)

EXT_INT_0_FLTCON0	Bit	Description	Initial State
FLTEN_0[3]	[31]	Filter Enable for EXT_INT[3] 0 = Disables 1 = Enables	1
FLTSEL_0[3]	[30]	Filter Selection for EXT_INT[3] 0 = Delay filter 1 = Digital filter (clock count)	0
FLTWIDTH_0[3]	[29:24]	Filtering width of EXT_INT[3] This value is valid when FLTSEL30 is 1.	0

外部中断事件

➢ 总结：

中断源	中断控制器	CPU核处理
GPIO(EINT) GPxyCON EXT_INT_n_PEND EXT_INT_n_MASK 其它中断源类似	VICnRAWINTR(R) VICnENABLE VICnSELECT STATUS(irq/fiq) VICnVECTPRIORITYm VICnADDRESS(高优先级的VICnVECTADDRm)	CPSR I-bit PC=VICnADDRESS

外部中断事件

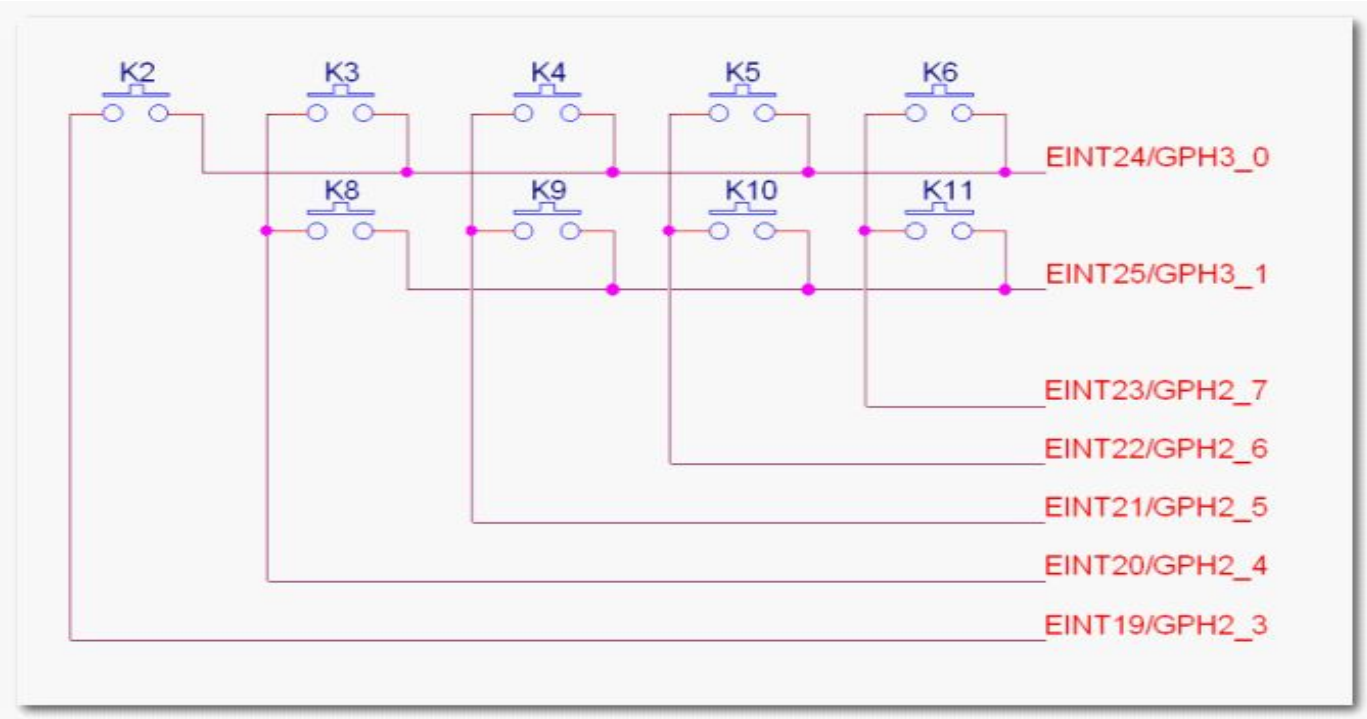
- 中断初始化步骤： 中断源->VIC->CPU
  01. 将IO配置成中断模式及上下拉使能
  02. 设置中断触发方式
  03. 清除中断挂起标志位
  04. 外部中断屏蔽位禁止
  05. 清除中断向量地址VICnADDRESS
  06. 绑定中断服务程序入口地址VICnVECTADDRm
  07. 设置中断优先级（可选，一般默认即可）
  08. 选择中断模式（IRQ或FIQ，默认为IRQ）
  09. 使能中断向量（VICINTENABLE）
  10. 使能IRQ（设置CPSR中的I位）

外部中断事件

- 中断服务函数:
  1. 设置中断模式下堆栈指针SP(也可以提前设置)
  2. 保护现场寄存器（压栈）
  3. 清除中断向量地址（否则不再进入中断）
  4. 清除中断挂起标志位（否则反复进入中断）
  5. 执行中断服务程序
  6. 恢复现场寄存器（出栈）
  7. 退出中断服务程序

外部中断事件

- 练习：
  - 将例子中的按键任意更换一个
  - 完成1*5中断按键



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