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Application Note

Battery Connection Transients

80-VC603-11 Rev. A

March 23, 2012

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Revision history

Revision	Date	Description
A	March 2012	Initial release

1 Introduction

When a battery is connected to a PMIC, the resulting transient voltage may propagate through the power management system and appear as a glitch on the supply voltages of circuits powered by the PMIC. Several points are worth emphasizing before presenting a more specific description:

- Connecting a battery to an actual product is a relatively rare occurrence.
  - Furthermore, the battery-connect transient does not cause an output glitch every time it is attached, making it even more rare.
- A smaller output glitch occurs when a charger (such as a USB or wall charger) is connected (a much more frequent event).
- The root cause is understood and is explained in Chapter 2.
- Example scenarios, complete with representative voltage waveforms, are given in Chapter 3.
- The slew rate of the battery-connect transient is an important aspect of this phenomenon (as demonstrated in Chapter 3).
  - A fast slew rate (high voltage change versus time) creates more severe output glitches.
  - A slow slew rate (low voltage change versus time) creates insignificant output glitches.
- Three factory test workarounds are available for eliminating or minimizing the output glitch generated by existing PMICs (all three are described further in Section 4.1):
  - The output glitch is not created when a battery is connected after a valid charger has established the primary phone power (VPH_PWR or VDD).
  - The output glitch is limited using a two-step voltage initialization: (1) start the supply voltage at 1.8 V and (2) allow dVdd to settle. Any output glitches that might occur will be limited to less than 1.8 V. After a slight delay, change the supply voltage to its desired (final) setting.
  - The output glitch is minimized when a discharged battery is connected. This method might be particularly useful for products that include an embedded battery.
- All affected PMIC designs will be updated to prevent glitches from appearing on any circuit supply voltages generated by the PMIC. This is the identified final solution, as described in Section 4.2.

1.1 Intended audience

This application note is intended for design and development engineering teams that create wireless products utilizing Qualcomm chipsets.

2 Problem Description

When a battery is attached to the product's PCB, a power supply transient is created that might propagate through the PMIC to other circuits that are powered by the PMIC. A high-level diagram of the propagation path is shown and explained in Figure 1.

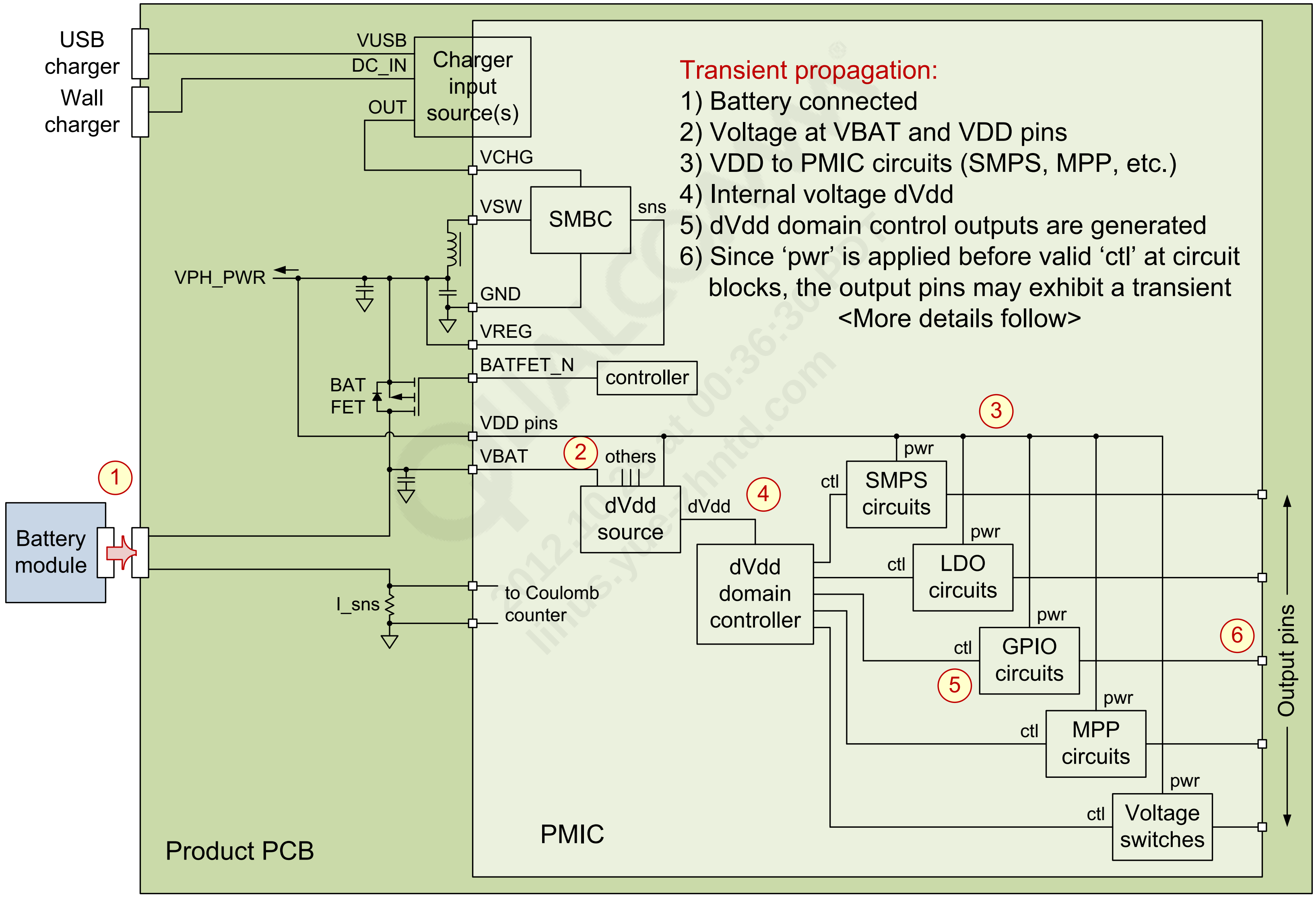

Figure 1 Power transient propagation path

The root cause of the output glitch is the undefined states of PMIC level shifter circuits (as explained in Figure 2). The PMIC circuits controlled by the level shifter outputs include, but are not limited to, SMPS and MPP circuits; these two circuits are described further in Chapter 3 as example scenarios.

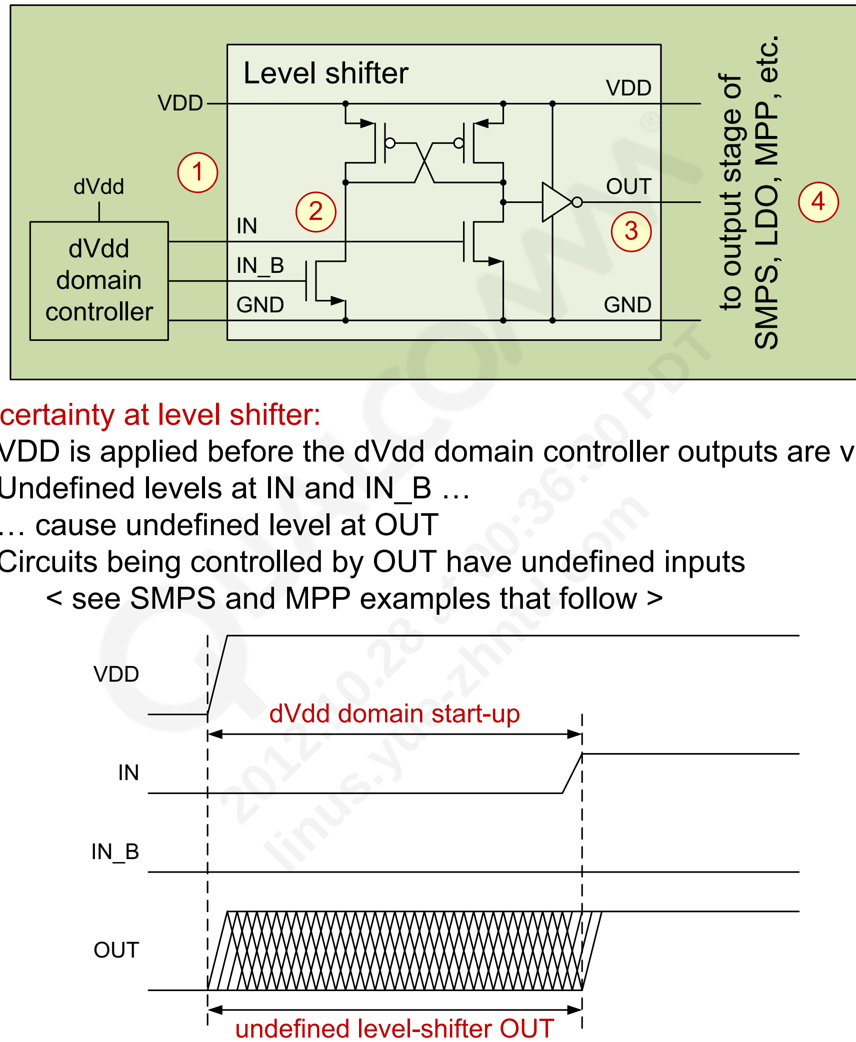

Figure 2 Level shifter temporarily undefined inputs and outputs

3 Example Scenarios and Voltage Waveforms

Before presenting the SMPS and MPP circuits as examples, example waveforms showing the input voltage (VDD) and output glitches explained in Section 3.1.

3.1 Example voltage waveform

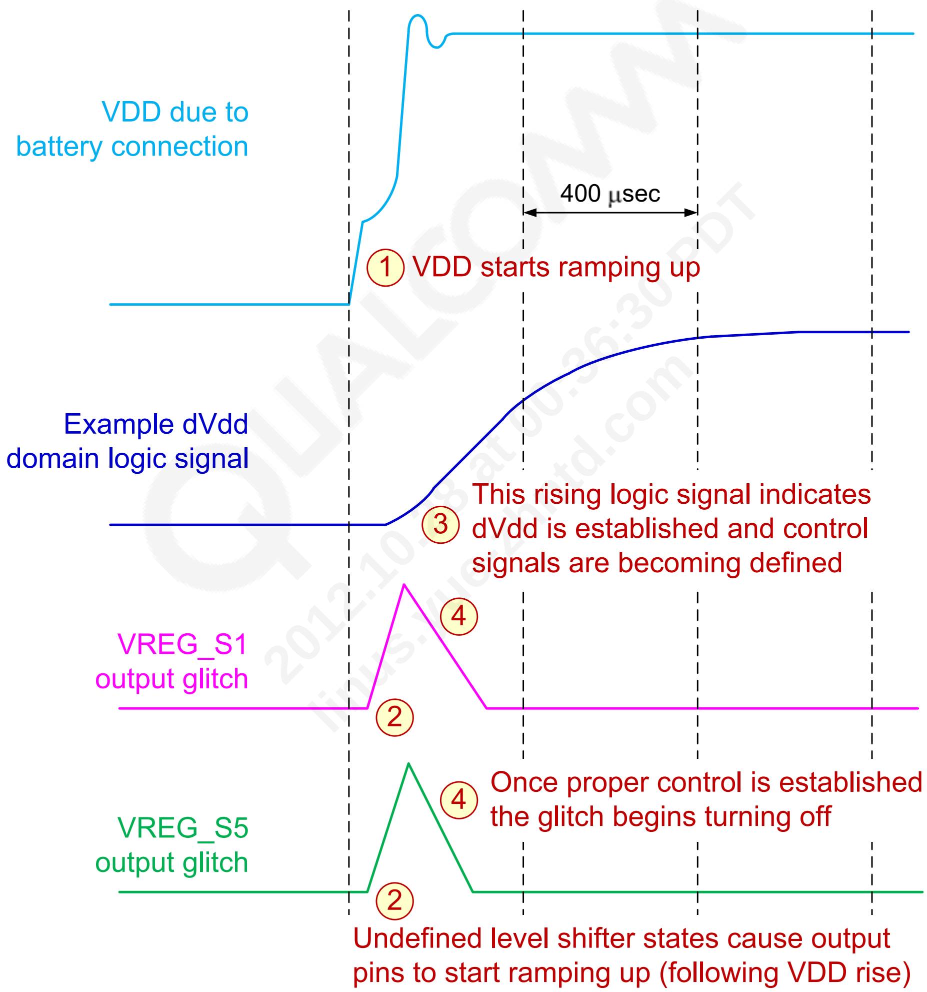

Figure 3 Example VDD input and output glitch waveforms

3.2 SMPS example

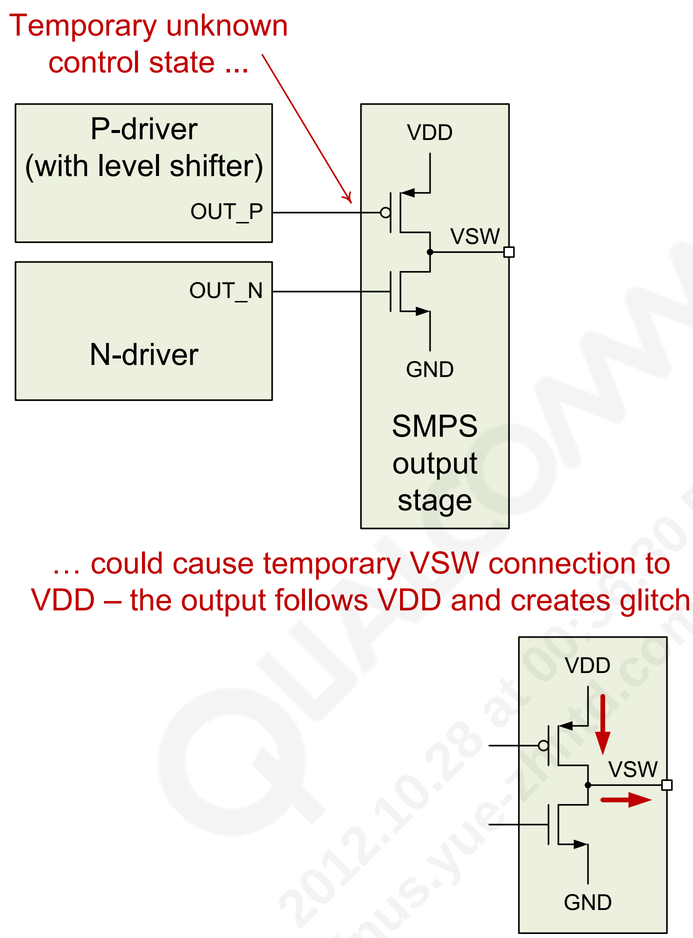

Figure 4 Example 1 – SMPS circuit

3.3 MPP example

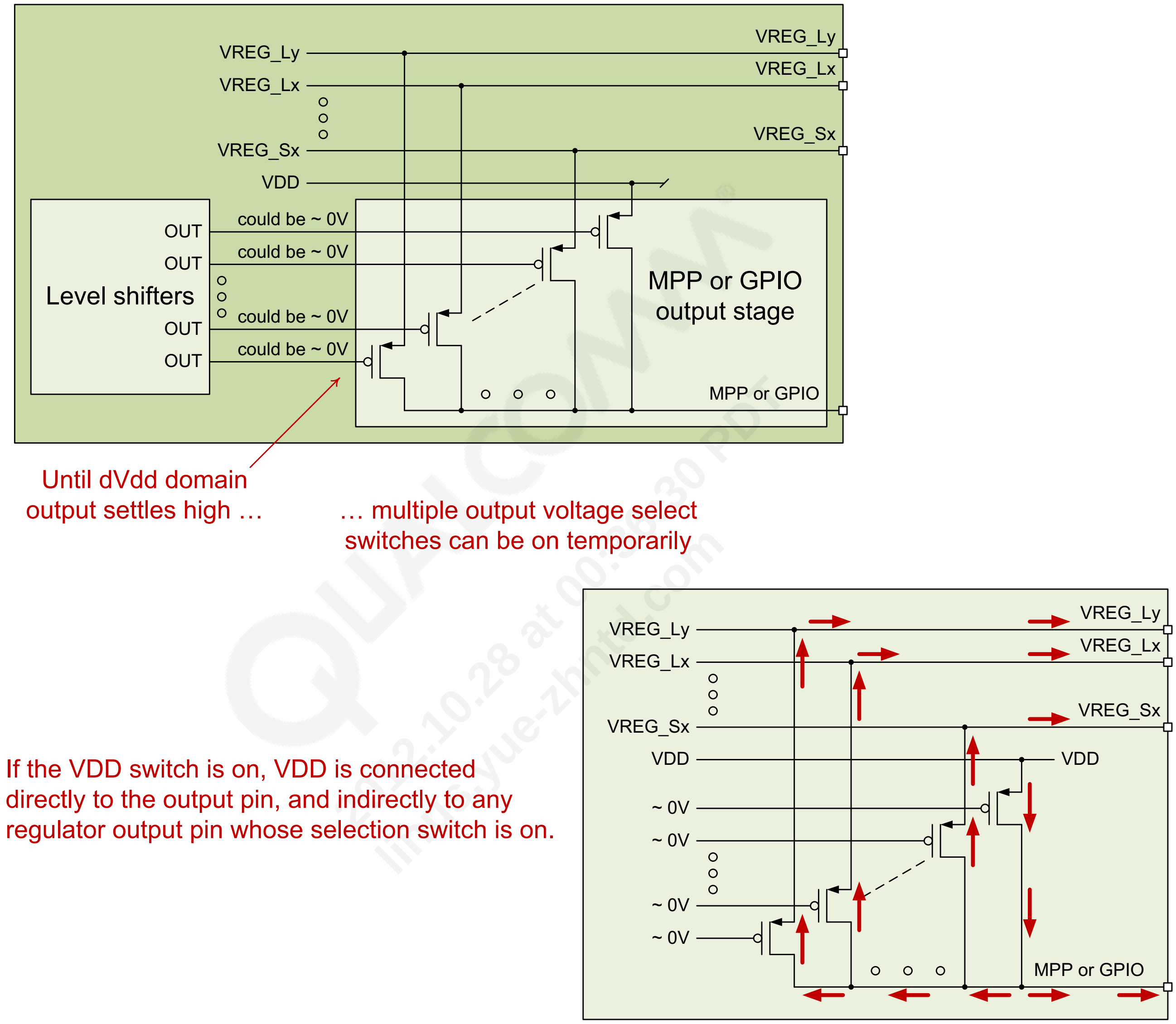

Figure 5 Example 2 – MPP leakage path to VREG outputs

3.4 Battery-connect VDD slew rate

Figure 6, shows how a slow slew rate prevents the battery-connect transient from generating a high output voltage. The interval during which the output stage is tracking VDD occurs when VDD is too low to be of any significant concern. The dVdd logic is established and turns off the output before its voltage rises too high.

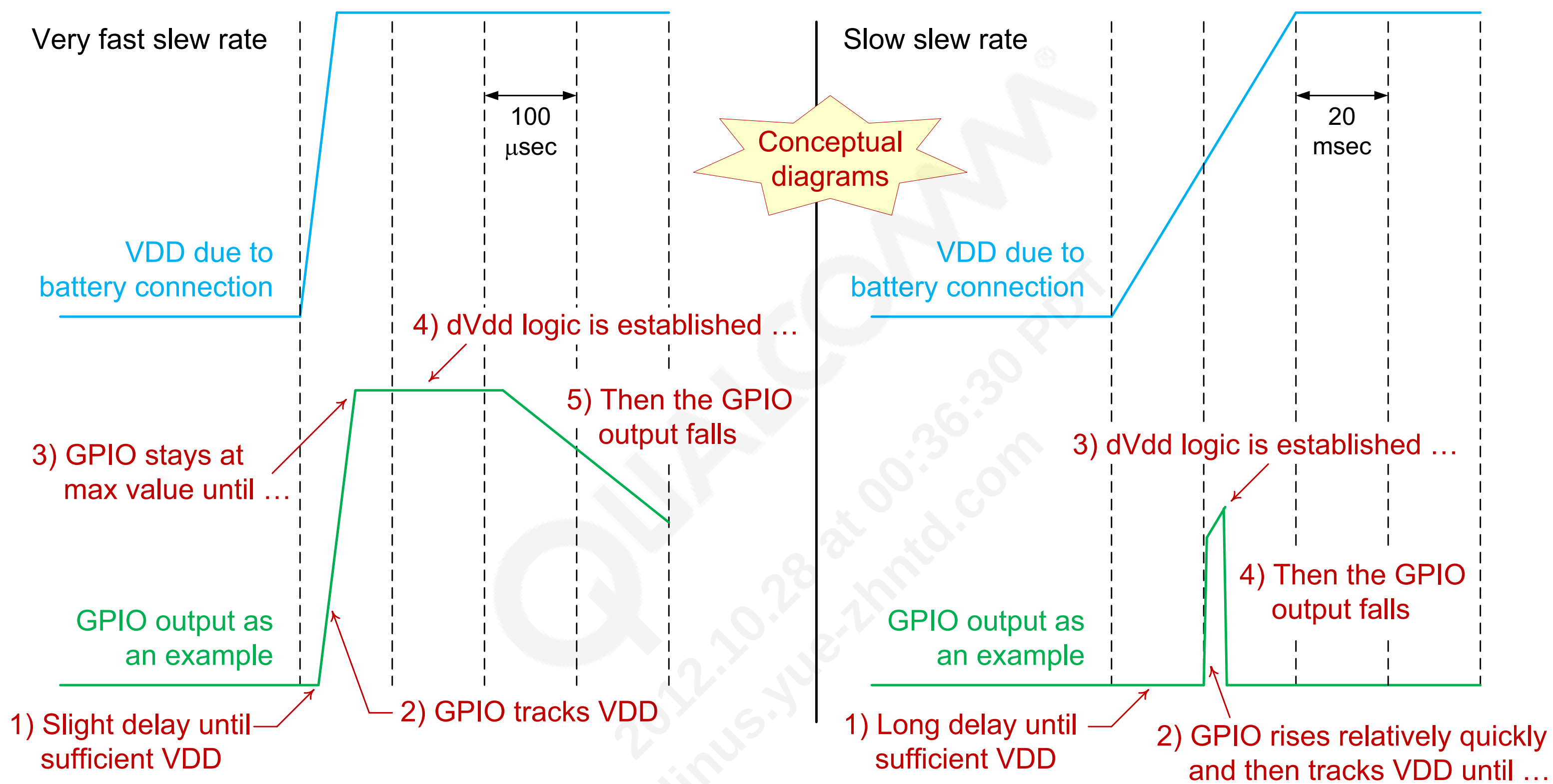

Figure 6 Battery-connect VDD slew rate

4 Solutions

There are two possible solutions:

1. Factory techniques that can be used immediately (Section 4.1) – techniques that avoid the battery-connect transient during factory testing.
2. The long-term, final solution (Section 4.2) that will eliminate the battery-connect transients entirely from future PMICs.

4.1 Factory testing of products using existing PMICs

Either of three recommended solutions can be used for near-term factory testing:

1. Connect an external charger

   With an external charger connected (USB or wall charger), the SMBC circuit generates the VPH_PWR voltage, and that voltage is used to establish the dVdd domain. The corresponding functional block diagram is included within Figure 1. Connecting a battery after the dVdd domain is established (via the charger) does not generate glitches at any PMIC output pins.

2. Use a two-step voltage initialization

   Start the supply voltage at 1.8 V and allow dVdd to settle. Any output glitches that might occur will be limited to less than 1.8 V. After a slight delay, change the supply voltage to its desired (final) setting. As stated in solution 1 above, connecting a battery after the dVdd domain is established does not generate glitches at any PMIC output pins.

   This solution can be used whether the PMIC includes an integrated charger or not.

3. Discharged the embedded battery

   If the product undergoing testing includes an embedded battery, that battery should be discharged before being installed. The output glitch is still created; however, it is minimized because the VDD level, while dVdd is being established, is too low to be a concern.

4.2 Final solution for all products using future PMICs

All affected PMIC designs will be updated to prevent glitches from appearing on any circuit supply voltages being generated by the PMIC. Elements of the solution include:

- The level shifter designs within circuits of concern (SMPS, LDO, MPP, GPIO, and voltage switches) are changed such that the internal dVdd domain must be established before those level shifters are enabled.
- The internal dVdd voltage is monitored; when dVdd is on and stable, a level shifter ‘enable’ signal is generated and routed to the level shifter circuits.