

# PM8841 Power Management IC

Software Interface 80-NA554-2 Rev. A February 2013

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# **Preface**

# **Technical assistance**

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# **Revision history**

Revision A, February 2013, initial release



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70/3:08:76:108:109:100.210 20/3:08:76:108:100:210

# **PMIC Register Mapping**

#### 1.1 Addressing structure

Each PMIC consists of two slave IDs. Each slave ID has 64 K addresses, which are subdivided into 256 groups of 256 addresses. Each group is known as a peripheral. The map can support up to 512 peripherals because each PMIC has two slave IDs, but the MSM can only support up to 256 peripherals.

Splitting the map into 256 peripherals with 256 addresses provides a convenient way of subdividing the 16-bit register addresses. The top eight bits are the peripheral address and the bottom eight bits are the register offset. If there are two identical peripherals (for example, LDOs), they will have different peripheral IDs, but their registers will be located at the same register offset. The unique slave ID (USID) allows the MSM to access more peripherals by effectively increasing the available register map.

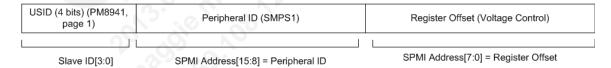


Figure 1-1 Addressing structure

Peripheral IDs are predefined and are specified.

#### 1.2 Slave ID

Each PMIC has two unique slave IDs (USID).

- USID 0 and 1 are reserved for the primary PMIC (i.e., the PM8941 device)
- USID 2 and 3 are reserved for a stand-alone Qualcomm PMIC charger
- USID 4 and 5 are reserved for the first slave PMIC (i.e., the PM8841 device)

Internally, the USID is translated into a local slave ID (LSID).

- The first USID maps to LSID 0
- The second USID maps to LSID 1

The PMIC can have up to four LSIDs, but the SPMI bus can address only the first two.

# 1.3 PMIC register maps

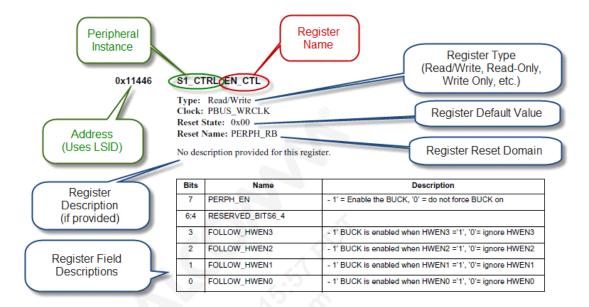


Figure 1-2 PMIC register map

The address is broken down into LSID, PID, and register offset.

For example, in the address 0x11446:

- ♦ The unique slave ID is in red
- ♦ The peripheral ID is in green
- ♦ The register offset is in purple

The LSID is provided in all the register maps. In most applications, where the PMIC is accessed from the SPMI bus, the USID is used.

- ♦ For PM8941 add 0x00000 to the address (no change).
- ♦ For PM8841 add 0x40000 to the address.

# 1.4 Peripheral register map

Each peripheral has 256 registers that are subdivided into different sections.

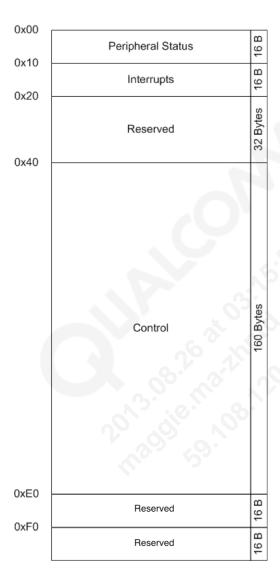


Figure 1-3 Peripheral register map

The subsections of the peripheral register map are

- ♦ Peripheral status
- ♦ Interrupts
- ♦ Control
- ♦ Reserved

# 1.5 Peripheral interrupts

The interrupts for each peripheral are in its peripheral register map. Each register is reserved for a different function. Each bit defines a different interrupt.

For example, bit 0 is reserved for the GPIO\_IN interrupt:

- 0x10[0] holds the real-time status of the GPIO\_IN interrupt
- 0x11[0] defines the type (level/edge) for GPIO\_IN
- ♦ 0x12[0] defines the polarity for GPIO\_IN

This setup reduces the number of transactions required to service interrupts. All real-time status bits for the interrupts in the module can be read with a single read of the INT\_RT\_STS register. Similarly, the latched interrupts status can be acquired with a single read of the INT\_LATCHED\_STS register.

Sample interrupt register map Table 1-1

Addr_ offset	Register_name	Field_ MSB	Field_ LSB	Field_name	Default	Description
0x10	INT_RT_STS	1	1	GPIO_HI_RT_STS	0	Interrupt real time status bits
		0	0	GPIO_IN_RT_STS	0	
0x12	INT_POLARITY_HIGH	1	1	GPIO_HI_HIGH	0	1: Interrupt will trigger on a level high (rising edge) event
		0	0	GPIO_IN_HIGH	0	0: Level HIGH triggering is disabled
0x13	INT_POLARITY_LOW	1	1	GPIO_HI_LOW	0	1: Interrupt will trigger on a level low (falling edge) event
		0	0	GPIO_IN_LOW	0	0: Level low triggering is disabled
0x14	INT_LATCHED_CLR	1	1	GPIO_HI_LATCHED_CLR	0	Writing a 1 to this interrupt rearms the interrupt when an interrupt is pending. It
		0	0	GPIO_IN_LATCHED_CLR	00	clears the internal latched status.
0x15	INT_EN_SET	1	1	GPIO_HI_EN_SET	0	Writing 0 to this register has no effect.
		0	0	GPIO_IN_EN_SET	0	Writing a 1 enables the corresponding interrupt. Reading this register reads back enable status
0x16	INT_EN_CLR	1	1	GPIO_HI_EN_CLR	0	Writing 0 to this register has no effect.
		0	0	GPIO_IN_EN_CLR	0	Writing a 1 disables the corresponding interrupt. Reading this register reads back enable status
0x18	INT_LATCHED_STS	1	1	GPIO_HI_LATCHED_STS	0	Latched Interrupt.
		0	0	GPIO_IN_LATCHED_STS	1 indicates that the interrupt has triggered. When the cleared by writing the clear bit.	1 indicates that the interrupt has triggered. When the latched bit is set it can only be cleared by writing the clear bit.
0x19	INT_PENDING_STS	1	1	GPIO_HI_PENDING_STS	0	Pending is set if interrupt has been sent but not cleared.
		0	0	GPIO_IN_PENDING_STS	0	
0x1A	INT_MID_SEL	1	0	INT_MID_SEL	0	Selects the MID that will receive the interrupt
0x1B	INT_PRIORITY	0	0	INT_PRIORITY	0	SR = 0 A = 1

# 1.6 Interrupt configuration

# 1.6.1 Set and forget registers

- ♦ INT\_MID\_SEL 0x00 for every peripheral because the MSM is the only master.
- ♦ INT\_PRIORITY The SPMI supports two levels of priority. Every interrupt uses low priority. No high priority use cases have been identified.

# 1.6.2 Enabling interrupts

Interrupts default to disabled. To enable an interrupt, set the TYPE, PRIORITY\_HIGH, and PRORITY\_LOW fields. Use read-modify-write to control these registers.

After the interrupts are configured, they can be enabled. INT\_EN has two registers: INT\_EN\_SET and INT\_EN\_CLR. To set these registers:

- Enable the interrupt by setting the corresponding bit in INT\_EN\_SET.
- Disable the interrupt by setting the corresponding bit in INT\_EN\_CLR.

The INT\_EN registers do not require read-modify-write. Writing 0 to these registers has no effect. Reading either register will read back the enable status.

# 1.6.3 Interrupt detection

Interrupts are sent to the master using the SPMI master write command. The interrupt message includes the peripheral ID and the interrupt that fired. All interrupt information is communicated to the MSM in one message.

Interrupt Message from slave (USID is identified during arbitration)

O MID Command (8 bits)
Master Write = 00010110

Master that should
receive the interrupt

Peripheral ID (Charger) INT7 INT6 INT5 INT4 INT3 INT2 INT1 INT0

SPMI Address = Peripheral ID SPMI Data = Interrupts

Note: SPMI signaling/parity bits not shown, Arbitration not shown

Figure 1-4 PMIC interrupt message

# 1.6.4 Clearing interrupts

Assume an interrupt is fired by GPIO\_01 (peripheral id 0x25).

- 1. The interrupt is generated in the PMIC. The message is sent to the peripheral owner (i.e., RPM) via SPMI and the PMIC arbiter (in the MSM device). The message indicates that the interrupt came from GPIO\_01 (PID = 0x25) and that the VREG\_OK interrupt triggered.
- 2. Optional: The software does a 6-byte read starting at address 0x2510. The software can read status, type (level/edge), en\_high, en\_low, and enable state in a single read.
- 3. The software does a 1-byte write of 0x01 to register 0x2516 only to disable the interrupt.
- 4. The interrupt handler takes care of the interrupt.
- 5. When the software is ready, a 2-byte write of 0x0101 to 0x2514 clears the interrupt and then re-enables the interrupt.



# 2 REVID\_REVID\_PM8841

# 0x103 REVID\_REVISION4

**Type:** read-only

Clock: PBUS\_WRCLK Reset State: 0x01 Reset Name: N/A

HW Version Register [31:24]

# REVID\_REVISION4

Bits	Name	Type	Description
7:0	ALL_LAYER	read- only	This number is incremented every time there is an all layer revision of the chip $0x01 = ES1$ $0x02 = ES2$

# 0x104 REVID\_PERPH\_TYPE

**Type:** read-only

Clock: PBUS\_WRCLK Reset State: 0x51 Reset Name: N/A

Peripheral Type

#### REVID\_PERPH\_TYPE

Bits	Name	Туре	Description
7:0	TYPE	read- only	REV_ID (This tells you that you are talking to a PMIC)

# 0x105 REVID\_PERPH\_SUBTYPE

**Type:** read-only

Clock: PBUS\_WRCLK Reset State: 0x02 Reset Name: N/A

Peripheral SubType

#### REVID\_PERPH\_SUBTYPE

Bits	Name	Type	Description
7:0	SUBTYPE	read- only	This is PM8841

# 0x108 REVID\_STATUS1

**Type:** read-only

Clock: PBUS\_WRCLK Reset State: 0x00 Reset Name: N/A

Status Registers

#### **REVID\_STATUS1**

Bits	Name	Type	Description
7:6	OP4	read- only	Option Pin State 11: VDD 10: HiZ 00: GND
5:4	OP3	read- only	Option Pin State 11: VDD 10: HiZ 00: GND
3:2	OP2	read- only	Option Pin State 11: VDD 10: HiZ 00: GND
1:0	OP1	read- only	Option Pin State 11: VDD 10: HiZ 00: GND

# 3 PON\_PON

# 0x804 PON PERPH TYPE

**Type:** read-only

Clock: PBUS\_WRCLK Reset State: 0x01 Reset Name: N/A

Peripheral Type

# PON\_PERPH\_TYPE

Bits		Name	Туре	Description
7:0	TYPE	08:10	read- only	PON

# 0x805 PON\_PERPH\_SUBTYPE

**Type:** read-only

Clock: PBUS\_WRCLK Reset State: 0x01 Reset Name: N/A

Peripheral SubType

#### PON\_PERPH\_SUBTYPE

Bits	Name	Туре	Description
7:0	SUBTYPE	read- only	PNP PON

# 0x807 PON\_PON\_PBL\_STATUS

**Type:** read-only

Clock: PBUS\_WRCLK
Reset State: Undefined
Reset Name: N/A

Stage 2 reset generation and register access error status.

#### PON\_PON\_PBL\_STATUS

Bits	Name	Туре	Description
7	DVDD_RB_OCCURRED	read- only	DVDD_RB was asserted during the last power cycle
6	XVDD_RB_OCCURRED	read- only	XVDD_RB was asserted during the last power cycle
5	REG_WRITE_ERROR	read- only	A register field write was attempted when a block was enabled. Writing to this address clears field.
4	REG_RESET_ERROR	read- only	A register field write was attempted when reset was asserted. Writing to this address clears field.
3	REG_SYNC_ERROR	read- only	Indicates a synchronized register field was over written before it's contents were latched by logic. Writing to this address clears field.,,,,'

# 0x808 PON\_PON\_REASON1

**Type:** read-only

Clock: PBUS\_WRCLK
Reset State: Undefined
Reset Name: raw\_xVdd\_rb

Reasons that the PMIC left the off state. All zeros mean that no trigger received

#### PON\_PON\_REASON1

Bits	Name	Туре	Description
7	KPDPWR_N	read- only	Triggered from new KPDPWR press
6	CBLPWR_N	read- only	Triggered from CBL_PWR1_N
5	PON1	read- only	Triggered from PON1
4	USB_CHG	read- only	Triggered from USB charger
3	DC_CHG	read- only	Triggered from DC charger

#### PON\_PON\_REASON1 (Continued)

Bits	Name	Туре	Description
2	RTC	read- only	Triggered from RTC
1	SMPL	read- only	Triggered from SMPL
0	HARD_RESET	read- only	Triggered from a Hard Reset event (check POFF reason for the trigger)

# 0x80A PON\_WARM\_RESET\_REASON1

**Type:** read-only

Clock: PBUS\_WRCLK
Reset State: Undefined
Reset Name: raw\_xVdd\_rb

Reasons that PMIC entered the Warm Reset state (pst\_13). This register is automatically reset when the PMIC turns on (i.e. PON\_WARM\_REASON\_CLEAR register field 1) or by writing to this address.

#### PON\_WARM\_RESET\_REASON1

Bits	Name	Type	Description
7	KPDPWR_N	read- only	Triggered by KPDPWR_N
6	RESIN_N	read- only	Triggered by RESIN_N
5	KPDPWR_AND_RESIN	read- only	Triggered by simultaneous KPDPWR_N + RESIN_N
4	GP2	read- only	Triggered by Keypad_Reset2
3	GP1	read- only	Triggered by Keypad_Reset1
2	PMIC_WD	read- only	Triggered by PMIC Watchdog
1	PS_HOLD	read- only	Triggered by PS_HOLD
0	SOFT	read- only	Triggered by Software

#### 0x80B PON WARM RESET REASON2

Type: read-only Clock: PBUS\_WRCLK Reset State: Undefined Reset Name: raw\_xVdd\_rb

Reasons that PMIC entered the Warm Reset state (pst\_13). This register is automatically reset when the PMIC turns on (i.e. PON\_WARM\_REASON\_CLEAR register field 1) or by writing to

WARM\_RESET\_REASON1 register address.

#### PON\_WARM\_RESET\_REASON2

Bits	Name	Туре	Description
4	AFP	read- only	Triggered AFP

#### 0x80C PON\_POFF\_REASON1

Type: read-only Clock: PBUS\_WRCLK Reset State: Undefined Reset Name: raw\_xVdd\_rb

Reasons that the PMIC left the on state and commenced a shutdown sequence. All zeros mean that no trigger received or a master bandgap or phone power fault occurred.

#### PON POFF REASON1

Bits	Name	Туре	Description
7	KPDPWR_N	read- only	Triggered by KPDPWR_N
6	RESIN_N	read- only	Triggered by RESIN_N
5	KPDPWR_AND_RESIN	read- only	Triggered by simultaneous KPDPWR_N + RESIN_N
4	GP2	read- only	Triggered by Keypad_Reset2
3	GP1	read- only	Triggered by Keypad_Reset1
2	PMIC_WD	read- only	Triggered by PMIC Watchdog
1	PS_HOLD	read- only	Triggered by PS_HOLD
0	SOFT	read- only	Triggered by Software

#### 0x80D PON\_POFF\_REASON2

**Type:** read-only

Clock: PBUS\_WRCLK
Reset State: Undefined
Reset Name: raw\_xVdd\_rb

Reasons that the PMIC left the on state and commenced a shutdown sequence. All zeros mean that no trigger received or a master bandgap or phone power fault occurred.

#### PON\_POFF\_REASON2

Bits	Name	Туре	Description
7	STAGE3	read- only	Triggered by stage3 reset
6	OTST3	read- only	Triggered by Overtemp
5	UVLO	read- only	Triggered by UVLO
4	AFP	read- only	Triggered AFP

# 0x80E PON\_SOFT\_RESET\_REASON1

**Type:** read-only

Clock: PBUS\_WRCLK
Reset State: Undefined
Reset Name: raw\_xVdd\_rb

Reasons that the PMIC registers were reset. All zeros mean that no trigger received. Clear the soft reason registers by writing to this register

#### PON\_SOFT\_RESET\_REASON1

Bits	Name	Туре	Description
7	KPDPWR_N	read- only	Triggered by KPDPWR_N
6	RESIN_N	read- only	Triggered by RESIN_N
5	KPDPWR_AND_RESIN	read- only	Triggered by simultaneous KPDPWR_N + RESIN_N
4	GP2	read- only	Triggered by Keypad_Reset2
3	GP1	read- only	Triggered by Keypad_Reset1

#### PON\_SOFT\_RESET\_REASON1 (Continued)

Bits	Name	Туре	Description
2	PMIC_WD	read- only	Triggered by PMIC Watchdog
1	PS_HOLD	read- only	Triggered by PS_HOLD
0	SOFT	read- only	Triggered by Software

#### 0x80F PON\_SOFT\_RESET\_REASON2

Type: read-only Clock: PBUS\_WRCLK Reset State: Undefined Reset Name: raw\_xVdd\_rb

Reasons that the PMIC registers were reset. All zeros mean that no trigger received. Clear the soft reason registers by writing to the SOFT\_RESET\_REASON1 register

#### PON\_SOFT\_RESET\_REASON2

Bits	Nam	туре Туре	Description
4	AFP	read- only	Triggered AFP

# 0x810 PON\_INT\_RT\_STS

Type: read-only Clock: PBUS\_WRCLK Reset State: Undefined Reset Name: N/A

**Interrupt Real Time Status Bits** 

#### PON INT RT STS

Bits	Name	Туре	Description
6	PMIC_WD_BARK	read- only	warning that a reset event has been triggered by the PMIC Watchdog timer
5	K_R_BARK	read- only	warning that a reset event has been triggered by asserting RESIN_N and KPDPWR_N simultaneously
4	RESIN_BARK	read- only	warning that a reset event has been triggered by RESIN_N
3	KPDPWR_BARK	read- only	warning that a reset event has been triggered by KPDPWR_N

#### PON\_INT\_RT\_STS (Continued)

Bits	Name	Туре	Description
2	CBLPWR_ON	read- only	CBLPWR_N has changed states for longer than his debounce timer
1	RESIN_ON	read- only	RESIN_N has changed states for longer than his debounce timer
0	KPDPWR_ON	read- only	KPDPWR_N has changed states for longer than his debounce timer

# 0x811 PON\_INT\_SET\_TYPE

Type: read-write Clock: PBUS\_WRCLK Reset State: 0x00 Reset Name: perph\_rb

0 = use level trigger interrupts, 1 = use edge trigger interrupts

# PON\_INT\_SET\_TYPE

Bits	Name	Туре	Description
6	PMIC_WD_BARK	read- write	5. <sup>2</sup>
5	K_R_BARK	read- write	
4	RESIN_BARK	read- write	
3	KPDPWR_BARK	read- write	
2	CBLPWR_ON	read- write	
1	RESIN_ON	read- write	
0	KPDPWR_ON	read- write	

# 0x812 PON\_INT\_POLARITY\_HIGH

Type: read-write Clock: PBUS\_WRCLK Reset State: 0x00 Reset Name: perph\_rb

1= Interrupt will trigger on a level high (rising edge) event, 0 = level high triggering is disabled

#### PON\_INT\_POLARITY\_HIGH

Bits	Name	Туре	Description
6	PMIC_WD_BARK	read- write	
5	K_R_BARK	read- write	
4	RESIN_BARK	read- write	
3	KPDPWR_BARK	read- write	
2	CBLPWR_ON	read- write	
1	RESIN_ON	read- write	7. 180
0	KPDPWR_ON	read- write	(5. °C)

# 0x813 PON\_INT\_POLARITY\_LOW

Type: read-write Clock: PBUS\_WRCLK Reset State: 0x00 Reset Name: perph\_rb

1' = Interrupt will trigger on a level low (falling edge) event, '0' = level low triggering is disabled

#### PON\_INT\_POLARITY\_LOW

Bits	Name	Туре	Description
6	PMIC_WD_BARK	read- write	
5	K_R_BARK	read- write	
4	RESIN_BARK	read- write	
3	KPDPWR_BARK	read- write	
2	CBLPWR_ON	read- write	
1	RESIN_ON	read- write	
0	KPDPWR_ON	read- write	

#### 0x814 PON\_INT\_LATCHED\_CLR

Type: write-only Clock: PBUS\_WRCLK Reset State: 0x00 Reset Name: perph\_rb

Writing a '1' to this interrupt will rearm the interrupt when an interrupt is pending. It clears the

internal sticky and sent bits

#### PON\_INT\_LATCHED\_CLR

Bits	Name	Туре	Description
6	PMIC_WD_BARK	write- only	
5	K_R_BARK	write- only	80,
4	RESIN_BARK	write- only	.50
3	KPDPWR_BARK	write- only	COLL
2	CBLPWR_ON	write- only	2/0
1	RESIN_ON	write- only	0.
0	KPDPWR_ON	write- only	

#### 0x815 PON\_INT\_EN\_SET

Type: read-write Clock: PBUS\_WRCLK Reset State: 0x00 Reset Name: perph\_rb

Writing '0' to this register has no effect. Writing a '1' will enable the corresponding interrupt. Reading this register will readback enable status

PMIC\_SET\_MASK

#### PON\_INT\_EN\_SET

Bits	Name	Туре	Description
6	PMIC_WD_BARK	read- write	
5	K_R_BARK	read- write	

#### PON\_INT\_EN\_SET (Continued)

Bits	Name	Туре	Description
4	RESIN_BARK	read- write	
3	KPDPWR_BARK	read- write	
2	CBLPWR_ON	read- write	
1	RESIN_ON	read- write	
0	KPDPWR_ON	read- write	

# 0x816 PON\_INT\_EN\_CLR

Type: read-write Clock: PBUS\_WRCLK Reset State: 0x00 Reset Name: perph\_rb

Writing '0' to this register has no effect. Writing a '1' will disable the corresponding interrupt. Reading this register will readback enable status

PMIC\_CLR\_MASK=INT\_EN\_SET

# PON\_INT\_EN\_CLR

Bits	Name	Туре	Description
6	PMIC_WD_BARK	read- write	
5	K_R_BARK	read- write	
4	RESIN_BARK	read- write	
3	KPDPWR_BARK	read- write	
2	CBLPWR_ON	read- write	
1	RESIN_ON	read- write	
0	KPDPWR_ON	read- write	

#### 0x818 PON\_INT\_LATCHED\_STS

**Type:** read-only

Clock: PBUS\_WRCLK Reset State: Undefined Reset Name: N/A

Debug: Latched (Sticky) Interrupt. '1' indicates that the interrupt has triggered. Once the latched bit is set it can only be cleared by writing the clear bit.

#### PON\_INT\_LATCHED\_STS

Bits	Name	Туре	Description
6	PMIC_WD_BARK	read- only	
5	K_R_BARK	read- only	160
4	RESIN_BARK	read- only	
3	KPDPWR_BARK	read- only	CON
2	CBLPWR_ON	read- only	10
1	RESIN_ON	read- only	0.
0	KPDPWR_ON	read- only	

# 0x819 PON\_INT\_PENDING\_STS

**Type:** read-only

Clock: PBUS\_WRCLK Reset State: Undefined Reset Name: N/A

Debug: Pending is set if interrupt has been sent but not cleared.

#### PON\_INT\_PENDING\_STS

Bits	Name	Туре	Description
6	PMIC_WD_BARK	read- only	
5	K_R_BARK	read- only	
4	RESIN_BARK	read- only	

#### PON\_INT\_PENDING\_STS (Continued)

Bits	Name	Туре	Description
3	KPDPWR_BARK	read- only	
2	CBLPWR_ON	read- only	
1	RESIN_ON	read- only	
0	KPDPWR_ON	read- only	

# 0x81A PON\_INT\_MID\_SEL

Type: read-write Clock: PBUS\_WRCLK Reset State: 0x00 Reset Name: perph\_rb

Selects the MID that will receive the interrupt

#### PON\_INT\_MID\_SEL

Bits	Name	Туре	Description
1:0	INT_MID_SEL	read- write	26.

# 0x81B PON\_INT\_PRIORITY

Type: read-write Clock: PBUS\_WRCLK Reset State: 0x00 Reset Name: perph\_rb

SR=0 A=1

#### PON\_INT\_PRIORITY

Bits	Name	Туре	Description
0	INT_PRIORITY	read- write	

#### 0x840 PON\_KPDPWR\_N\_RESET\_S1\_TIMER

Type: read-write Clock: PBUS\_WRCLK Reset State: 0x0F

Reset Name: soft\_dVdd\_rb

Stage 1 (Bark) Timer. Bark cannot be disabled, but interrupt can be disabled if necessary

# PON\_KPDPWR\_N\_RESET\_S1\_TIMER

Bits	Name	Туре	Description
3:0	Name S1_TIMER	read- write	Time that the debounced trigger must be held before bark is sent to MSM 0: 0 ms 1: 32 ms 2: 56 ms 3: 80 ms 4: 128 ms 5: 184 ms 6: 272 ms
	2013.08.26 1013.08.26	100. 0.17.12	7: 408 ms 8: 608 ms 9: 904 ms 10: 1352 ms 11: 2048 ms 12: 3072 ms 13: 4480 ms 14: 6720 ms 15: 10256 ms  This field can only be updated when block is disabled (i.e.
	10,000		This field can only be updated when block is disabled (i. 10 sleep clock cycles after writing 0 to S2_RESET_EN and PON_TRIGGER_EN:KPDPWR_N fields).

# 0x841 PON\_KPDPWR\_N\_RESET\_S2\_TIMER

Type: read-write Clock: PBUS\_WRCLK Reset State: 0x07

**Reset Name:** soft\_dVdd\_rb

Stage 2 (bite) configuration

# PON\_KPDPWR\_N\_RESET\_S2\_TIMER

Bits	Name	Туре	Description
2:0	S2_TIMER	read- write	Time that debounced trigger must be held before S2 reset occurs {0ms, 10ms, 50ms, 100ms, 250ms, 500ms, 1s, 2s}  This field can only be updated when block is disabled (i.e. 10 sleep clock cycles after writing 0 to S2_RESET_EN field).

# 0x842 PON\_KPDPWR\_N\_RESET\_S2\_CTL

Type: read-write Clock: PBUS\_WRCLK Reset State: 0x04

**Reset Name:** soft\_dVdd\_rb

Stage 2 (bite) configuration

#### PON\_KPDPWR\_N\_RESET\_S2\_CTL

Bits	Name	Туре	Description
7	S2_RESET_EN	read- write	Enable Stage 2 reset
3:0	RESET_TYPE	read- write	0000 = Reserved for soft reset, 0001 = warm reset, 0010 = Reserved for immediate xVdd shutdown 0011 = Reserved (default to xVdd Shutdown) 0100 = Shutdown (Normal Shutdown) 0101 = dVdd Shutdown (Shutdown + dVdd_rb), 0110 = xVdd Shutdown (Shutdown + dVdd_rb + xVdd_rb), 0111 = Hard reset (Shutdown + Automatic power up) 1000 = Reserved for dVdd Hard reset (Shutdown + dVdd_rb + Automatic power up), 1001 = Reserved for xVdd Hard reset (Shutdown + dVdd_rb + xVdd_rb + Automatic power up), 1010 = Reserved for warm reset + dvdd shutdown 1011 = Reserved for warm reset + xVdd shutdown 1100 = Reserved for warm reset + Shutdown 1101 = Reserved for warm reset then Hard reset 1110 = Reserved for warm reset then dVdd Hard reset 1111 = Reserved for warm reset then xVdd Hard reset This field can only be updated when block is disabled (i.e. 10 sleep clock cycles after writing 0 to S2_RESET_EN field).

#### 0x844 PON\_RESIN\_N\_RESET\_S1\_TIMER

Type: read-write Clock: PBUS\_WRCLK Reset State: 0x0F

Reset Name: soft\_dVdd\_rb

Stage 1 (Bark) Timer. Bark cannot be disabled, but interrupt can be disabled if necessary

# PON\_RESIN\_N\_RESET\_S1\_TIMER

Bits	Name	Туре	Description
3:0	S1_TIMER	read- write	Time that the debounced trigger must be held before bark is sent to MSM
			0: 0 ms
			1: 32 ms
			2: 56 ms
			3: 80 ms
			4: 128 ms
			5: 184 ms
			6: 272 ms
		(2)	7: 408 ms
			8: 608 ms
		0	9: 904 ms
			10: 1352 ms
	8.	2	11: 2048 ms
			12: 3072 ms
	7/3 ·0·	28.	13: 4480 ms
	0,0 40)	10	14: 6720 ms
	200, 70		15: 10256 ms
			This field can only be updated when block is disabled (i.e. 10 sleep clock cycles after writing 0 to S2_RESET_EN field).

# 0x845 PON\_RESIN\_N\_RESET\_S2\_TIMER

Type: read-write Clock: PBUS\_WRCLK Reset State: 0x07

**Reset Name:** soft\_dVdd\_rb

Stage 2 (bite) configuration

# PON\_RESIN\_N\_RESET\_S2\_TIMER

Bits	Name	Туре	Description
2:0	S2_TIMER	read- write	Time that debounced trigger must be held before S2 reset occurs {0ms, 10ms, 50ms, 100ms, 250ms, 500ms, 1s, 2s}  This field can only be updated when block is disabled (i.e. 10 sleep clock cycles after writing 0 to S2_RESET_EN field).

# 0x846 PON\_RESIN\_N\_RESET\_S2\_CTL

Type: read-write Clock: PBUS\_WRCLK Reset State: 0x04

Reset Name: soft\_dVdd\_rb

Stage 2 (bite) configuration

# PON\_RESIN\_N\_RESET\_S2\_CTL

Bits	Name	Туре	Description
7	S2_RESET_EN	read- write	Enable Stage 2 reset
3:0	RESET_TYPE	read- write	0000 = Reserved for soft reset, 0001 = warm reset, 0010 = Reserved for immediate xVdd shutdown 0011 = Reserved (default to xVdd Shutdown) 0100 = Shutdown (Normal Shutdown) 0101 = dVdd Shutdown (Shutdown + dVdd_rb), 0110 = xVdd Shutdown (Shutdown + dVdd_rb + xVdd_rb), 0111 = Hard reset (Shutdown + Automatic power up) 1000 = Reserved for dVdd Hard reset (Shutdown + dVdd_rb + Automatic power up), 1001 = Reserved for xVdd Hard reset (Shutdown + dVdd_rb + xVdd_rb+ Automatic power up), 1010 = Reserved for warm reset + dvdd shutdown 1011 = Reserved for warm reset + xVdd shutdown 1100 = Reserved for warm reset + Shutdown 1101 = Reserved for warm reset then Hard reset 1110 = Reserved for warm reset then dVdd Hard reset 1111 = Reserved for warm reset then xVdd Hard reset This field can only be updated when block is disabled (i.e. 10 sleep clock cycles after writing 0 to S2_RESET_EN field).

#### 0x848 PON\_RESIN\_AND\_KPDPWR\_RESET\_S1\_TIMER

Type: read-write Clock: PBUS\_WRCLK Reset State: 0x0F

Reset Name: soft\_dVdd\_rb

Stage 1 (Bark) Timer. Bark cannot be disabled, but interrupt can be disabled if necessary

#### PON\_RESIN\_AND\_KPDPWR\_RESET\_S1\_TIMER

Bits	Name	Туре	Description
3:0	Name S1_TIMER	Type read- write	Time that the debounced trigger must be held before bark is sent to MSM 0: 0 ms 1: 32 ms 2: 56 ms 3: 80 ms 4: 128 ms 5: 184 ms 6: 272 ms 7: 408 ms 8: 608 ms 9: 904 ms 10: 1352 ms 11: 2048 ms 12: 3072 ms 13: 4480 ms 14: 6720 ms 15: 10256 ms
			This field can only be updated when block is disabled (i.e. 10 sleep clock cycles after writing 0 to S2_RESET_EN field).

#### 0x849 PON\_RESIN\_AND\_KPDPWR\_RESET\_S2\_TIMER

Type: read-write Clock: PBUS\_WRCLK Reset State: 0x07

**Reset Name:** soft\_dVdd\_rb

Stage 2 (bite) configuration

# PON\_RESIN\_AND\_KPDPWR\_RESET\_S2\_TIMER

Bits	Name	Туре	Description
2:0	S2_TIMER	read- write	Time that debounced trigger must be held before S2 reset occurs {0ms, 10ms, 50ms, 100ms, 250ms, 500ms, 1s, 2s}  This field can only be updated when block is disabled (i.e. 10 sleep clock cycles after writing 0 to S2_RESET_EN field).

# 0x84A PON\_RESIN\_AND\_KPDPWR\_RESET\_S2\_CTL

Type: read-write Clock: PBUS\_WRCLK Reset State: 0x04

Reset Name: soft\_dVdd\_rb

Stage 2 (bite) configuration

# PON\_RESIN\_AND\_KPDPWR\_RESET\_S2\_CTL

Bits	Name	Туре	Description
7	S2_RESET_EN	read- write	Enable Stage 2 reset
3:0	RESET_TYPE	read- write	0000 = Reserved for soft reset, 0001 = warm reset, 0010 = Reserved for immediate xVdd shutdown 0011 = Reserved (default to xVdd Shutdown) 0100 = Shutdown (Normal Shutdown) 0101 = dVdd Shutdown (Shutdown + dVdd_rb), 0110 = xVdd Shutdown (Shutdown + dVdd_rb + xVdd_rb), 0111 = Hard reset (Shutdown + Automatic power up) 1000 = Reserved for dVdd Hard reset (Shutdown + dVdd_rb + Automatic power up), 1001 = Reserved for xVdd Hard reset (Shutdown + dVdd_rb + xVdd_rb+ Automatic power up), 1010 = Reserved for warm reset + dvdd shutdown 1011 = Reserved for warm reset + xVdd shutdown 1100 = Reserved for warm reset + Shutdown 1101 = Reserved for warm reset then Hard reset 1110 = Reserved for warm reset then dVdd Hard reset 1111 = Reserved for warm reset then xVdd Hard reset This field can only be updated when block is disabled (i.e. 10 sleep clock cycles after writing 0 to S2_RESET_EN field).

#### 0x84C PON\_GP2\_RESET\_S1\_TIMER

Type: read-write Clock: PBUS\_WRCLK Reset State: 0x0F

Reset Name: soft\_dVdd\_rb

Stage 1 (Bark) Timer. Bark cannot be disabled, but interrupt can be disabled if necessary

# PON\_GP2\_RESET\_S1\_TIMER

Bits	Name	Туре	Description
3:0	S1_TIMER	read- write	Time that the debounced trigger must be held before bark is sent to MSM
			0: 0 ms
			1: 32 ms
			2: 56 ms
			3: 80 ms
			4: 128 ms
			5: 184 ms
			6: 272 ms
		(2)	7: 408 ms
			8: 608 ms
	6	0	9: 904 ms
			10: 1352 ms
	8.	2	11: 2048 ms
			12: 3072 ms
	7/3 10.	29.	13: 4480 ms
	00 400	10	14: 6720 ms
	100		15: 10256 ms
			This field can only be updated when block is disabled (i.e. 10 sleep clock cycles after writing 0 to S2_RESET_EN field).

# 0x84D PON\_GP2\_RESET\_S2\_TIMER

Type: read-write Clock: PBUS\_WRCLK Reset State: 0x07

**Reset Name:** soft\_dVdd\_rb

Stage 2 (bite) configuration

# PON\_GP2\_RESET\_S2\_TIMER

Bits	Name	Туре	Description
2:0	S2_TIMER	read- write	Time that debounced trigger must be held before S2 reset occurs {0ms, 10ms, 50ms, 100ms, 250ms, 500ms, 1s, 2s}  This field can only be updated when block is disabled (i.e. 10 sleep clock cycles after writing 0 to S2_RESET_EN field).

# 0x84E PON\_GP2\_RESET\_S2\_CTL

Type: read-write Clock: PBUS\_WRCLK Reset State: 0x04

**Reset Name:** soft\_dVdd\_rb Stage 2 (bite) configuration

# PON\_GP2\_RESET\_S2\_CTL

Bits	Name	Туре	Description
7	S2_RESET_EN	read- write	Enable Stage 2 reset
3:0	RESET_TYPE	read- write	0000 = Reserved soft reset, 0001 = warm reset, 0010 = Reserved for immediate xVdd shutdown 0011 = Reserved (default to xVdd Shutdown) 0100 = Shutdown (Normal Shutdown) 0101 = dVdd Shutdown (Shutdown + dVdd_rb), 0110 = xVdd Shutdown (Shutdown + dVdd_rb + xVdd_rb), 0111 = Hard reset (Shutdown + Automatic power up) 1000 = Reserved for dVdd Hard reset (Shutdown + dVdd_rb + Automatic power up), 1001 = Reserved for xVdd Hard reset (Shutdown + dVdd_rb + xVdd_rb + Automatic power up), 1010 = Reserved for warm reset + dvdd shutdown 1011 = Reserved for warm reset + xVdd shutdown 1100 = Reserved for warm reset + Shutdown 1101 = Reserved for warm reset then Hard reset 1110 = Reserved for warm reset then dVdd Hard reset 1111 = Reserved for warm reset then xVdd Hard reset This field can only be updated when block is disabled (i.e. 10 sleep clock cycles after writing 0 to S2_RESET_EN field).

## 0x850 PON\_GP1\_RESET\_S1\_TIMER

Type: read-write Clock: PBUS\_WRCLK Reset State: 0x0F

Reset Name: soft\_dVdd\_rb

Stage 1 (Bark) Timer. Bark cannot be disabled, but interrupt can be disabled if necessary

## PON\_GP1\_RESET\_S1\_TIMER

Bits	Name	Туре	Description
3:0	Name S1_TIMER	Type read- write	Time that the debounced trigger must be held before bark is sent to MSM 0: 0 ms 1: 32 ms 2: 56 ms 3: 80 ms 4: 128 ms 5: 184 ms 6: 272 ms 7: 408 ms 8: 608 ms 9: 904 ms
	70/3.08.h	708.	10: 1352 ms 11: 2048 ms 12: 3072 ms 13: 4480 ms 14: 6720 ms 15: 10256 ms  This field can only be updated when block is disabled (i.e. 10 sleep clock cycles after writing 0 to S2_RESET_EN field).

## 0x851 PON\_GP1\_RESET\_S2\_TIMER

Type: read-write Clock: PBUS\_WRCLK Reset State: 0x07

**Reset Name:** soft\_dVdd\_rb

Stage 2 (bite) configuration

## PON\_GP1\_RESET\_S2\_TIMER

Bits	Name	Туре	Description
2:0	S2_TIMER	read- write	Time that debounced trigger must be held before S2 reset occurs {0ms, 10ms, 50ms, 100ms, 250ms, 500ms, 1s, 2s}  This field can only be updated when block is disabled (i.e. 10 sleep clock cycles after writing 0 to S2_RESET_EN field).

## 0x852 PON\_GP1\_RESET\_S2\_CTL

Type: read-write Clock: PBUS\_WRCLK Reset State: 0x04

**Reset Name:** soft\_dVdd\_rb Stage 2 (bite) configuration

## PON\_GP1\_RESET\_S2\_CTL

Bits	Name	Type	Description
7	S2_RESET_EN	read- write	Enable Stage 2 reset
3:0	RESET_TYPE	read- write	0000 = Reserved for soft reset, 0001 = warm reset, 0010 = Reserved for immediate xVdd shutdown 0011 = Reserved (default to xVdd Shutdown) 0100 = Shutdown (Normal Shutdown) 0101 = dVdd Shutdown (Shutdown + dVdd_rb), 0110 = xVdd Shutdown (Shutdown + dVdd_rb + xVdd_rb), 0111 = Hard reset (Shutdown + Automatic power up) 1000 = Reserved for dVdd Hard reset (Shutdown + dVdd_rb + Automatic power up), 1001 = Reserved for xVdd Hard reset (Shutdown + dVdd_rb + xVdd_rb + Automatic power up), 1010 = Reserved for warm reset + dvdd shutdown 1011 = Reserved for warm reset + xVdd shutdown 1100 = Reserved for warm reset + Shutdown 1101 = Reserved for warm reset then Hard reset 1110 = Reserved for warm reset then dVdd Hard reset 1111 = Reserved for warm reset then xVdd Hard reset This field can only be updated when block is disabled (i.e. 10 sleep clock cycles after writing 0 to S2_RESET_EN field).

## 0x854 PON\_PMIC\_WD\_RESET\_S1\_TIMER

Type: read-write Clock: PBUS\_WRCLK Reset State: 0x1F

Reset Name: soft\_dVdd\_rb

Stage 1 (Bark) Timer. Bark cannot be disabled, but interrupt can be disabled if necessary

#### PON\_PMIC\_WD\_RESET\_S1\_TIMER

Bits	Name	Туре	Description
6:0	S1_TIMER	read- write	Time that the debounced trigger must be held before bark is sent to MSM (seconds) 0 ? 127 seconds, default 31 seconds. Program hex value of decimal count desired (not binary coded).  This field can only be updated when block is disabled (i.e. 10 sleep clock cycles after writing 0 to S2_RESET_EN field).

## 0x855 PON\_PMIC\_WD\_RESET\_S2\_TIMER

Type: read-write Clock: PBUS\_WRCLK Reset State: 0x01

Reset Name: soft\_dVdd\_rb

Stage 2 (bite) configuration

## PON\_PMIC\_WD\_RESET\_S2\_TIMER

Bits	Name	Туре	Description
6:0	S2_TIMER	read- write	Time that debounced trigger must be held before S2 reset occurs 0 ? 127 seconds (default = 32 seconds). Program hex value of decimal count desired (Not binary coded). Timer starts after WD bark expires  This field can only be updated when block is disabled (i.e. 10 sleep clock cycles after writing 0 to S2_RESET_EN field).

## 0x856 PON\_PMIC\_WD\_RESET\_S2\_CTL

Type: read-write Clock: PBUS\_WRCLK Reset State: 0x86

Reset Name: soft\_dVdd\_rb

## Stage 2 (bite) configuration

## PON\_PMIC\_WD\_RESET\_S2\_CTL

Bits	Name	Туре	Description
7	S2_RESET_EN	read- write	Enable Stage 2 reset
3:0	RESET_TYPE	readwrite	0000 = Reserved for soft reset, 0001 = warm reset, 0010 = Reserved for immediate xVdd shutdown 0011 = Reserved (default to xVdd Shutdown) 0100 = Shutdown (Normal Shutdown) 0101 = dVdd Shutdown (Shutdown + dVdd_rb), 0110 = xVdd Shutdown (Shutdown + dVdd_rb + xVdd_rb), 0111 = Hard reset (Shutdown + Automatic power up) 1000 = Reserved for dVdd Hard reset (Shutdown + dVdd_rb + Automatic power up), 1001 = Reserved for xVdd Hard reset (Shutdown + dVdd_rb + xVdd_rb + Automatic power up), 1010 = Reserved for warm reset + dvdd shutdown 1011 = Reserved for warm reset + xVdd shutdown 1100 = Reserved for warm reset + Shutdown 1101 = Reserved for warm reset then Hard reset 1110 = Reserved for warm reset then dVdd Hard reset 1111 = Reserved for warm reset then xVdd Hard reset This field can only be updated when block is disabled (i.e. 10 sleep clock cycles after writing 0 to S2_RESET_EN field).

## 0x857 PON\_PMIC\_WD\_RESET\_PET

Type: write-only Clock: PBUS\_WRCLK Reset State: 0x00

Reset Name: soft\_dVdd\_rb

Stage 2 (bite) configuration

## PON\_PMIC\_WD\_RESET\_PET

Bits	Name	Туре	Description
0	WATCHDOG_PET	write- only	Writing '1' to this bit will clear the PMIC WD timer. Writing '0' has no effect.

## 0x85A PON\_PS\_HOLD\_RESET\_CTL

**Type:** read-write **Clock:** PBUS\_WRCLK **Reset State:** 0x84

**Reset Name:** soft\_dVdd\_rb

## PON\_PS\_HOLD\_RESET\_CTL

Bits	Name	Туре	Description
7	S2_RESET_EN	read- write	Enable reset
3:0	RESET_TYPE	read- write	0000 = Reserved for soft reset, 0001 = warm reset, 0010 = Reserved for immediate xVdd shutdown 0011 = Reserved (default to xVdd Shutdown) 0100 = Shutdown (Normal Shutdown) 0101 = dVdd Shutdown (Shutdown + dVdd_rb), 0110 = xVdd Shutdown (Shutdown + dVdd_rb + xVdd_rb), 0111 = Hard reset (Shutdown + Automatic power up) 1000 = Reserved for dVdd Hard reset (Shutdown + dVdd_rb + Automatic power up), 1001 = Reserved for xVdd Hard reset (Shutdown + dVdd_rb + xVdd_rb + Automatic power up), 1010 = Reserved for warm reset + dvdd shutdown 1011 = Reserved for warm reset + Shutdown 1100 = Reserved for warm reset + Shutdown 1101 = Reserved for warm reset then Hard reset 1110 = Reserved for warm reset then XVdd Hard reset 1111 = Reserved for warm reset then xVdd Hard reset 1111 = Reserved for warm reset then xVdd Hard reset This field can only be updated when block is disabled (i.e. 10 sleep clock cycles after writing 0 to S2_RESET_EN field).

## 0x862 PON\_SW\_RESET\_S2\_CTL

Type: read-write Clock: PBUS\_WRCLK Reset State: 0x00

Reset Name: soft\_dVdd\_rb

Software initiated shutdown (AFP)

## PON\_SW\_RESET\_S2\_CTL

Bits	Name	Туре	Description
7	SW_RESET_EN	read- write	Enable SW reset

## PON\_SW\_RESET\_S2\_CTL (Continued)

Bits	Name	Type	Description
3:0	RESET_TYPE	read-	0000 = soft reset,
		write	0001 = warm reset,
			0010 = Reserved for immediate xVdd shutdown
			0011 = Reserved (default to xVdd Shutdown)
			0100 = Shutdown (Normal Shutdown)
			0101 = dVdd Shutdown (Shutdown + dVdd_rb),
			$0110 = xVdd Shutdown (Shutdown + dVdd_rb + xVdd_rb),$
			0111 = Hard reset (Shutdown + Automatic power up)
			1000 = Reserved for dVdd Hard reset (Shutdown +
			dVdd_rb + Automatic power up),
			1001 = Reserved for xVdd Hard reset (Shutdown + dVdd_rb + xVdd_rb+ Automatic power up),
			1010 = Reserved for warm reset + dvdd shutdown
			1011 = Reserved for warm reset + xVdd shutdown
			1100 = Reserved for warm reset + Shutdown
	4		1101 = Reserved for warm reset then Hard reset
			1110 = Reserved for warm reset then dVdd Hard reset
			1111 = Reserved for warm reset then xVdd Hard reset
			This field can only be updated when block is disabled (i.e.
		100	10 sleep clock cycles after writing 0 to SW_RESET_EN field).

## 0x863 PON\_SW\_RESET\_GO

Type: write-only Clock: PBUS\_WRCLK Reset State: 0x00

Reset Name: soft\_dVdd\_rb

Initiate SW Reset by writing 0xA5 to this register

## PON\_SW\_RESET\_GO

Bits	Name	Type	Description
7:0	SW_RESET_GO	write- only	Initiate SW Reset by writing 0xA5 to this register

## 0x866 PON\_OVERTEMP\_RESET\_CTL

Type: read-write Clock: PBUS\_WRCLK Reset State: 0x84

Reset Name: soft\_dVdd\_rb

## PON\_OVERTEMP\_RESET\_CTL

Bits	Name	Туре	Description
7	S2_RESET_EN	read- write	Enable stage 2 reset
3:0	RESET_TYPE	read- write	0000 = Reserved for soft reset, 0001 = warm reset, 0010 = Reserved for immediate xVdd shutdown 0011 = Reserved (default to xVdd Shutdown) 0100 = Shutdown (Normal Shutdown) 0101 = dVdd Shutdown (Shutdown + dVdd_rb), 0110 = xVdd Shutdown (Shutdown + dVdd_rb + xVdd_rb), 0111 = Hard reset (Shutdown + Automatic power up) 1000 = Reserved for dVdd Hard reset (Shutdown + dVdd_rb + Automatic power up), 1001 = Reserved for xVdd Hard reset (Shutdown + dVdd_rb + xVdd_rb + Automatic power up), 1010 = Reserved for warm reset + dvdd shutdown 1011 = Reserved for warm reset + xVdd shutdown 1100 = Reserved for warm reset + Shutdown 1101 = Reserved for warm reset then Hard reset 1110 = Reserved for warm reset then dVdd Hard reset 1111 = Reserved for warm reset then xVdd Hard reset 1111 = Reserved for warm reset then xVdd Hard reset 1115 field can only be updated when block is disabled (i.e. 10 sleep clock cycles after writing 0 to S2_RESET_EN field).

## 0x86A PON\_AFP\_RESET\_CTL

Type: read-write Clock: PBUS\_WRCLK Reset State: 0x04

**Reset Name:** soft\_dVdd\_rb

## PON\_AFP\_RESET\_CTL

Bits	Name	Type	Description
7	S2_RESET_EN	read- write	Enable stage 2reset

## PON\_AFP\_RESET\_CTL (Continued)

Bits	Name	Type	Description
3:0	RESET_TYPE	read-	0000 = Reserved for soft reset,
		write	0001 = warm reset,
			0010 = Reserved for immediate xVdd shutdown
			0011 = Reserved (default to xVdd Shutdown)
			0100 = Shutdown (Normal Shutdown)
			0101 = dVdd Shutdown (Shutdown + dVdd_rb),
			0110 = xVdd Shutdown (Shutdown + dVdd_rb + xVdd_rb),
			0111 = Hard reset (Shutdown + Automatic power up)
			1000 = Reserved for dVdd Hard reset (Shutdown +
			dVdd_rb + Automatic power up),
			1001 = Reserved for xVdd Hard reset (Shutdown + dVdd_rb + xVdd_rb+ Automatic power up),
			1010 = Reserved for warm reset + dvdd shutdown
			1011 = Reserved for warm reset + xVdd shutdown
			1100 = Reserved for warm reset + Shutdown
	4		1101 = Reserved for warm reset then Hard reset
			1110 = Reserved for warm reset then dVdd Hard reset
			1111 = Reserved for warm reset then xVdd Hard reset
		4	This field can only be updated when block is disabled (i.e.
		100	10 sleep clock cycles after writing 0 to S2_RESET_EN field).

## 0x870 PON\_PULL\_CTL

Type: read-write Clock: PBUS\_WRCLK Reset State: 0x0F

Reset Name: soft\_dVdd\_rb

## PON\_PULL\_CTL

Bits	Name	Туре	Description
3	PON1_PD_EN	read- write	
2	CBLPWR_N_PU_EN	read- write	
1	KPDPWR_N_PU_EN	read- write	
0	RESIN_N_PU_EN	read- write	

## 0x871 PON\_DEBOUNCE\_CTL

Type: read-write Clock: PBUS\_WRCLK Reset State: 0x00

**Reset Name:** soft\_dVdd\_rb

## PON\_DEBOUNCE\_CTL

Bits	Name	Туре	Description
2:0	DEBOUNCE	read- write	KPD/CBL/GP_DLY/RESIN/RESIN_AND_KPD/GP1/GP2: Time delay for KPD, CBL, General Purpose PON, RESIN, RESIN_AND_KPD, GP1 and GP2 state change interrupt and triggering. Delay = (1/1024)* 2^ (x+4)  This is a synchronized field. For reliable hardware operation, the minimum time allowed between write accesses is 10 sleep clock cycles.

## 0x875 PON\_RESET\_S3\_TIMER

Type: read-write Clock: PBUS\_WRCLK Reset State: 0x06

Reset Name: raw\_xVdd\_rb

Time that debounced trigger must be held before S3 reset occurs (seconds)

## PON\_RESET\_S3\_TIMER

Bits	Name	Туре	Description
2:0	S3_TIMER	read- write	Time that debounced trigger must be held before S3 reset occurs.  000 = Instant, else 2^(x) seconds (2 to 128)  This is a synchronized field. For reliable hardware operation, the minimum time allowed between write accesses is 10 sleep clock cycles.

## 0x880 PON\_PON\_TRIGGER\_EN

Type: read-write Clock: PBUS\_WRCLK Reset State: 0xF8

**Reset Name:** soft\_dVdd\_rb

Power on trigger enables.

## PON\_PON\_TRIGGER\_EN

Bits	Name	Type	Description
7	KPDPWR_N	read- write	Enable PON trigger for new KPDPWR press
6	CBLPWR_N	read- write	Enable PON trigger for CBL_PWR_N
5	PON1	read- write	Enable PON trigger for PON1
4	USB_CHG	read- write	Enable PON trigger for USB CHG
3	DC_CHG	read- write	Enable PON trigger for DC CHG
2	RTC	read- write	Enable PON trigger for RTC
1	SMPL	read- write	Enable PON trigger for SMPL

## 0x888 PON\_UVLO

Type: read-write
Clock: PBUS\_WRCLK
Reset State: 0x05

Reset Name: soft\_dVdd\_rb

**UVLO** Delay

## PON\_UVLO

Bits	Name	Туре	Description
2:0	UVLO_DLY	read- write	Time delay for UVLO detection.  if X = 0 then delay = 0, else delay = (1/1024) seconds * 2 X-1  where X = value of bits <2:0>  This is a synchronized field. For reliable hardware operation, the minimum time allowed between write accesses is 10 sleep clock cycles.

## 0x88C PON\_PERPH\_RB\_SPARE

Type: read-write Clock: PBUS\_WRCLK Reset State: 0x00 Reset Name: perph\_rb Extra registers for SW to keep information through resets

#### PON\_PERPH\_RB\_SPARE

Bits	Name	Туре	Description
7:0	SPARE	read- write	SPARE registers for SW

## 0x88D PON\_DVDD\_RB\_SPARE

Type: read-write Clock: PBUS\_WRCLK Reset State: 0x00 Reset Name: dVdd\_rb

Extra registers for SW to keep information through resets

#### PON DVDD RB SPARE

Bits	Name	Туре	Description
7:0	SPARE	read- write	SPARE registers for SW

## 0x88E PON XVDD RB SPARE

Type: read-write Clock: PBUS\_WRCLK Reset State: 0x00 Reset Name: xVdd\_rb

Extra registers for SW to keep information through resets

## PON\_XVDD\_RB\_SPARE

Bits	Name	Туре	Description
7:0	SPARE	read- write	SPARE registers for SW

## 0x88F PON\_SOFT\_RB\_SPARE

Type: read-write Clock: PBUS\_WRCLK Reset State: 0x00

Reset Name: soft\_dVdd\_rb

Extra registers for SW to keep information through resets

## PON\_SOFT\_RB\_SPARE

Bits	Name	Туре	Description
7:0	SPARE	read- write	SPARE registers for SW

## 0x890 PON\_PON1\_INTERFACE

Type: read-write Clock: PBUS\_WRCLK Reset State: 0x00

Reset Name: shutdown2\_rb

PON module interface signalling.

## PON\_PON1\_INTERFACE

Bits	Name	Туре	Description
7	PON_OUT	read- write	Field drives primary PMIC PON output buffer input.

# 4 TEMP\_ALARM\_TEMP\_ALARM

## 0x2404 TEMP ALARM PERPH TYPE

**Type:** read-only

Clock: PBUS\_WRCLK Reset State: 0x09 Reset Name: N/A

Peripheral Type

## TEMP\_ALARM\_PERPH\_TYPE

Bits		Name	Туре	Description
7:0	TYPE	08.1	read- only	Alarm

## 0x2405 TEMP\_ALARM\_PERPH\_SUBTYPE

**Type:** read-only

Clock: PBUS\_WRCLK Reset State: 0x08 Reset Name: N/A

Peripheral SubType

## TEMP\_ALARM\_PERPH\_SUBTYPE

Bits	Name	Type	Description
7:0	SUBTYPE	read- only	Temp Alarm

## 0x2408 TEMP\_ALARM\_STATUS1

Type: read-only Clock: PBUS\_WRCLK Reset State: 0x00 Reset Name: N/A

**Status Registers** 

#### TEMP\_ALARM\_STATUS1

Bits	Name	Туре	Description
7	TEMP_ALARM_OK	read- only	1: TEMP ALARM enabled 0: TEMP ALARM disabled
3	ST3_SHUTDOWN_STS	read- only	Stage 3 shutdown occurred, writing 1 to ST3_SHUTDOWN_CLR clears this bit
2	ST2_SHUTDOWN_STS	read- only	Stage 2 shutdown occurred, writing 1 to ST2_SHUTDOWN_CLR clears this bit
1:0	TEMP_ALARM_FSM_STA TE	read- only	TEMP_ALARM_FSM_STATE  00 = STAGE 0  01 = STAGE 1  10 = STAGE 2  11 = STAGE 3

## 0x2410 TEMP\_ALARM\_INT\_RT\_STS

**Type:** read-only

Clock: PBUS\_WRCLK Reset State: 0x00 Reset Name: N/A

**Interrupt Real Time Status Bits** 

#### TEMP\_ALARM\_INT\_RT\_STS

В	Bits	Name	Туре	Description
	0	TEMP_ALARM_RT_STS	read- only	

## 0x2411 TEMP\_ALARM\_INT\_SET\_TYPE

Type: read-write Clock: PBUS\_WRCLK Reset State: 0x00

Reset Name: PERPH\_RB

0 =use level trigger interrupts, 1 =use edge trigger interrupts

#### TEMP\_ALARM\_INT\_SET\_TYPE

Bits	Name	Туре	Description
0	TEMP_ALARM_TYPE	read- write	

## 0x2412 TEMP\_ALARM\_INT\_POLARITY\_HIGH

Type: read-write Clock: PBUS\_WRCLK Reset State: 0x00 Reset Name: PERPH RB

1= Interrupt will trigger on a level high (rising edge) event, 0 = level high triggering is disabled

#### TEMP\_ALARM\_INT\_POLARITY\_HIGH

Bits	Name	Туре	Description
0	TEMP_ALARM_HIGH	read- write	CONT

## 0x2413 TEMP\_ALARM\_INT\_POLARITY\_LOW

Type: read-write Clock: PBUS\_WRCLK Reset State: 0x00 Reset Name: PERPH\_RB

1' = Interrupt will trigger on a level low (falling edge) event, '0' = level low triggering is disabled

#### TEMP ALARM INT POLARITY LOW

Bits	Name	Туре	Description
0	TEMP_ALARM_LOW	read- write	

## 0x2414 TEMP\_ALARM\_INT\_LATCHED\_CLR

Type: write-only Clock: PBUS\_WRCLK Reset State: 0x00 Reset Name: PERPH\_RB

Writing a '1' to this interrupt will rearm the interrupt when an interrupt is pending. It clears the

internal sticky and sent bits

#### TEMP\_ALARM\_INT\_LATCHED\_CLR

Bit	s Name	Type	Description
0	TEMP_ALARM_LATCHE D_CLR	write- only	

## 0x2415 TEMP\_ALARM\_INT\_EN\_SET

Type: read-write Clock: PBUS\_WRCLK Reset State: 0x00 Reset Name: PERPH RB

Writing '0' to this register has no effect. Writing a '1' will enable the corresponding interrupt.

Reading this register will readback enable status

PMIC\_SET\_MASK

#### TEMP\_ALARM\_INT\_EN\_SET

Bits	Name	Туре	Description
0	TEMP_ALARM_EN_SET	read- write	17/12 2/10

## 0x2416 TEMP ALARM INT EN CLR

Type: read-write Clock: PBUS\_WRCLK Reset State: 0x00

**Reset Name:** PERPH\_RB

Writing '0' to this register has no effect. Writing a '1' will disable the corresponding interrupt.

Reading this register will readback enable status

PMIC\_CLR\_MASK=INT\_EN\_SET

## TEMP\_ALARM\_INT\_EN\_CLR

Bits	Name	Туре	Description
0	TEMP_ALARM_EN_CLR	read- write	

#### 0x2418 TEMP\_ALARM\_INT\_LATCHED\_STS

**Type:** read-only

Clock: PBUS\_WRCLK Reset State: 0x00 Reset Name: N/A

Debug: Latched (Sticky) Interrupt. '1' indicates that the interrupt has triggered. Once the latched

bit is set it can only be cleared by writing the clear bit.

#### TEMP\_ALARM\_INT\_LATCHED\_STS

Bits	Name	Туре	Description
0	TEMP_ALARM_LATCHE D_STS	read- only	

## 0x2419 TEMP\_ALARM\_INT\_PENDING\_STS

**Type:** read-only

Clock: PBUS\_WRCLK Reset State: 0x00 Reset Name: N/A

Debug: Pending is set if interrupt has been sent but not cleared.

## TEMP\_ALARM\_INT\_PENDING\_STS

Bits	Name	Type	Description
0	TEMP_ALARM_PENDING _STS	read- only	

## 0x241A TEMP\_ALARM\_INT\_MID\_SEL

Type: read-write Clock: PBUS\_WRCLK

Reset State: 0x00

Reset Name: PERPH\_RB

Selects the MID that will receive the interrupt

#### TEMP\_ALARM\_INT\_MID\_SEL

Bits	Name	Туре	Description
1:0	INT_MID_SEL	read- write	

## 0x241B TEMP\_ALARM\_INT\_PRIORITY

Type: read-write Clock: PBUS\_WRCLK Reset State: 0x00 Reset Name: PERPH\_RB

SR=0 A=1

#### TEMP\_ALARM\_INT\_PRIORITY

Bits	Name	Туре	Description
0	INT_PRIORITY	read- write	

## 0x2440 TEMP ALARM SHUTDOWN CTL1

Type: read-write Clock: PBUS\_WRCLK Reset State: 0x01

Reset Name: PERPH\_RB

#### TEMP\_ALARM\_SHUTDOWN\_CTL1

Bits	Name	Туре	Description
7	OVRD_ST3_EN	read- write	OVRD_ST3_EN : Override automatic shutdown in stage 3
6	OVRD_ST2_EN	read- write	OVRD_ST2_EN : Override partial automatic shutdown in stage 2
1:0	TEMP_THRESH_CNTRL	read- write	TEMP_THRESH_CNTRL  0 = {105, 125, 145}  1 = {110, 130, 150}  2 = {115, 135, 155}  3 = {120, 140, 160}

## 0x2442 TEMP\_ALARM\_SHUTDOWN\_CTL2

Type: write-only
Clock: PBUS\_WRCLK
Reset State: 0x00

**Reset Name:** PERPH\_RB

#### TEMP\_ALARM\_SHUTDOWN\_CTL2

Bits	Name	Туре	Description
7	ST3_SHUTDOWN_CLR	write- only	writing 1 clears ST3_SHUTDOWN_STS bit

## TEMP\_ALARM\_SHUTDOWN\_CTL2 (Continued)

Bits	Name	Туре	Description
6	ST2_SHUTDOWN_CLR	write- only	writing 1 clears ST2_SHUTDOWN_STS bit

## 0x2446 TEMP\_ALARM\_EN\_CTL1

Type: read-write Clock: PBUS\_WRCLK Reset State: 0x01 Reset Name: PERPH\_RB

## TEMP\_ALARM\_EN\_CTL1

Bits	Name	Туре	Description
7	TEMP_ALARM_EN	read- write	force enable TEMP ALARM     con't force enable TEMP ALARM
0	FOLLOW_TEMP_ALARM _HW_EN	read- write	1: follow TEMP_ALARM_HW_EN 0: disable TEMP ALARM



# 5 CLK\_DIST\_CLK\_DIST

## 0x5904 CLK DIST PERPH TYPE

**Type:** read-only

Clock: PBUS\_WRCLK Reset State: 0x06 Reset Name: N/A

Peripheral Type

## CLK\_DIST\_PERPH\_TYPE

Bits		Name	Туре	Description
7:0	TYPE	08.15	read- only	Clock

## 0x5905 CLK\_DIST\_PERPH\_SUBTYPE

**Type:** read-only

Clock: PBUS\_WRCLK Reset State: 0x02 Reset Name: N/A

Peripheral SubType

## CLK\_DIST\_PERPH\_SUBTYPE

Bits	Name	Туре	Description
7:0	SUBTYPE	read- only	Clock Dist

## 0x5908 CLK\_DIST\_STATUS1

**Type:** read-only

Clock: PBUS\_WRCLK Reset State: 0x00 Reset Name: N/A

**Status Registers** 

#### CLK\_DIST\_STATUS1

Bits	Name	Туре	Description
7	RC19M_OK	read- only	0 = 19M2 RC is off 1 =19M2 RC is on

## 0x5910 CLK\_DIST\_INT\_RT\_STS

**Type:** read-only

Clock: PBUS\_WRCLK Reset State: 0x00 Reset Name: N/A

**Interrupt Real Time Status Bits** 

## CLK\_DIST\_INT\_RT\_STS

Bits	Name	Туре	Description
0	XO19M2_HALT_DET_RT _STS	read- only	19M2_XO HALT detected

## 0x5911 CLK\_DIST\_INT\_SET\_TYPE

**Type:** read-write **Clock:** PBUS\_WRCLK **Reset State:** 0x00

Reset Name: PERPH\_RB

0 =use level trigger interrupts, 1 =use edge trigger interrupts

#### CLK\_DIST\_INT\_SET\_TYPE

Bits	Name	Type	Description
0	XO19M2_HALT_DET_TY PE	read- write	

#### 0x5912 CLK DIST INT POLARITY HIGH

Type: read-write Clock: PBUS\_WRCLK Reset State: 0x00 Reset Name: PERPH\_RB

1= Interrupt will trigger on a level high (rising edge) event, 0 = level high triggering is disabled

#### CLK\_DIST\_INT\_POLARITY\_HIGH

Bits	Name	Туре	Description
0	XO19M2_HALT_DET_HIG H	read- write	

## 0x5913 CLK\_DIST\_INT\_POLARITY\_LOW

Type: read-write Clock: PBUS\_WRCLK Reset State: 0x00

Reset Name: PERPH RB

1' = Interrupt will trigger on a level low (falling edge) event, '0' = level low triggering is disabled

#### CLK\_DIST\_INT\_POLARITY\_LOW

Bits	Name	Type	Description
0	XO19M2_HALT_DET_LO W	read- write	

## 0x5914 CLK\_DIST\_INT\_LATCHED\_CLR

**Type:** write-only **Clock:** PBUS\_WRCLK **Reset State:** 0x00

Reset Name: PERPH RB

Writing a '1' to this interrupt will rearm the interrupt when an interrupt is pending. It clears the internal sticky and sent bits

#### CLK\_DIST\_INT\_LATCHED\_CLR

Bits	Name	Type	Description
0	XO19M2_HALT_DET_LAT CHED_CLR	write- only	

## 0x5915 CLK\_DIST\_INT\_EN\_SET

Type: read-write Clock: PBUS\_WRCLK Reset State: 0x00 Reset Name: PERPH\_RB

0' = interrupt is disabled (or masked), 1 = interrupt is enabled

PMIC\_SET\_MASK

#### CLK\_DIST\_INT\_EN\_SET

Bits	Name	Туре	Description
0	XO19M2_HALT_DET_EN _SET	read- write	

## 0x5916 CLK\_DIST\_INT\_EN\_CLR

Type: read-write Clock: PBUS\_WRCLK Reset State: 0x00

Reset Name: PERPH\_RB

0' = interrupt is disabled (or masked), 1 = interrupt is enabled

PMIC\_CLR\_MASK=INT\_EN\_SET

## CLK\_DIST\_INT\_EN\_CLR

Bits	Name	Туре	Description
0	XO19M2_HALT_DET_EN _CLR	read- write	

## 0x5918 CLK\_DIST\_INT\_LATCHED\_STS

**Type:** read-only

Clock: PBUS\_WRCLK Reset State: 0x00 Reset Name: N/A

Latched (Sticky) Interrupt. '1' indicates that the interrupt has triggered. Once the latched bit is set it can only be cleared by writing the clear bit.

#### CLK\_DIST\_INT\_LATCHED\_STS

Bits	Name	Туре	Description
0	XO19M2_HALT_DET_LAT CHED_STS	read- only	

## 0x5919 CLK\_DIST\_INT\_PENDING\_STS

Type: read-only Clock: PBUS\_WRCLK Reset State: 0x00 Reset Name: N/A

Debug: Pending is set if interrupt has been sent but not cleared.

## CLK\_DIST\_INT\_PENDING\_STS

Bits	Name	Туре	Description
0	XO19M2_HALT_DET_PE NDING_STS	read- only	CONTRACTOR

## 0x591A CLK\_DIST\_INT\_MID\_SEL

Type: read-write Clock: PBUS\_WRCLK Reset State: 0x00 Reset Name: PERPH\_RB

Selects the MID that will receive the interrupt

#### CLK\_DIST\_INT\_MID\_SEL

Bit	s Name	Type	Description
1:0	NT_MID_SEL	read- write	

## 0x591B CLK\_DIST\_INT\_PRIORITY

Type: read-write Clock: PBUS\_WRCLK Reset State: 0x00 Reset Name: PERPH\_RB

SR=0 A=1

## CLK\_DIST\_INT\_PRIORITY

Bits	Name	Type	Description
0	INT_PRIORITY	read- write	

## 0x5940 CLK\_DIST\_CLK\_CTL1

Type: read-write Clock: PBUS\_WRCLK Reset State: 0x15 Reset Name: PERPH\_RB

## CLK\_DIST\_CLK\_CTL1

Bits	Name	Type	Description
5:4	SMPS_CLK_SEL	read- write	00: (XO_OUTBUFF_EN_DLY AND 19M2_HALT_b) 1=19.2 MHz XO, 0=19.2 MHz RC 01: Force 19.2 MHz RC osc as source 10: Force 19.2 MHz XO osc as source 11: Follow 19.2 MHz osc halt Halt = 1 : RC Halt = 0 : XO
3:2	GPCLK_19M2_SEL	read- write	00: (XO_OUTBUFF_EN_DLY AND 19M2_HALT_b) 1=19.2 MHz XO, 0=19.2 MHz RC 01: Force 19.2 MHz RC osc as source 10: Force 19.2 MHz XO osc as source 11: Follow 19.2 MHz osc halt Halt = 1 : RC Halt = 0 : XO
1:0	XORC19M2_CLK_SEL	read- write	00: (XO_OUTBUFF_EN_DLY AND 19M2_HALT_b) 1=19.2 MHz XO, 0=19.2 MHz RC 01: Force 19.2 MHz RC osc as source 10: Force 19.2 MHz XO osc as source 11: Follow 19.2 MHz osc halt Halt = 1 : RC Halt = 0 : XO

## 0x5941 CLK\_DIST\_CLK\_CTL2

Type: read-write Clock: PBUS\_WRCLK Reset State: 0x00 Reset Name: PERPH\_RB

## CLK\_DIST\_CLK\_CTL2

Bits	Name	Туре	Description
0	SEL_ALT_SC	read- write	When high, enables xo/586 clock & changes sleep clock source in the clocks module to xo/586. ORed with xxx bit This pRvides the low power sleep clock output. Enables the XO and sets sleep clock mux to output XO / 586 thRugh ripple divider.

## 0x5942 CLK\_DIST\_CLK\_CTL3

Type: read-write Clock: PBUS\_WRCLK Reset State: 0x00 Reset Name: dVdd\_rb

## CLK\_DIST\_CLK\_CTL3

Bits	Name	Туре	Description
0	SEL_ALT_RTC	read- write	7°CO,

## 0x5943 CLK\_DIST\_CLK\_CTL4

Type: read-write Clock: PBUS\_WRCLK Reset State: 0x02 Reset Name: xVdd\_rb

## CLK\_DIST\_CLK\_CTL4

Bits	Name	Type	Description
1	CLK_32K_RC	read- write	CLK_32K_RC: This bit along with SEL_ALT_SC abd SEL_ALT_RTC fRm CLK_CTRL2??? register sets the source of the sleep clock and RTC clock.  0 = The state of SEL_ALT_SC and SEL_ALT_RTC determines the source of 32K clock (either one of the 32K clock source or divided down clock source)  1 = Forces the divided down (XO or RC) / 586 as 32K clock source  ** This bit also affects the 32K, 1K and 1 Hz clock outputs. See note 1 for more details.
0	XO32K_CLK_SEL	read- write	Selects between CalRC/LFRC and 32K XO/external 32K source

## 0x5945 CLK\_DIST\_HALT\_CTL

Type: read-write Clock: PBUS\_WRCLK Reset State: 0x00 Reset Name: PERPH\_RB

## CLK\_DIST\_HALT\_CTL

Bits	Name	Туре	Description
7	XO19M2_HALT_DET_EN	read- write	XO19M2_HALT_DET_EN 1=Enable the 19.2 MHz halt detector. 0=Disable the 19.2 MHz halt detector.
6	FORCE_XO19M2_OSC_ HALT	read- write	FORCE_19M2_OSC_HALT Forces 19.2 MHz halt detect output = 1
0	HOLD_XO19M2_OSC_H ALT	read- write	HOLD_19M2_OSC_HALT  1 = Hold the 19.2 MHz halt detector output once it goes high  0 = Clear the 19.2 MHz halt detector output if it is high.

## 0x5946 CLK DIST RC CTL

Type: read-write Clock: PBUS\_WRCLK Reset State: 0x01 Reset Name: PERPH\_RB

RC\_EN=FORCE\_RC19M2\_OSC\_ON OR(RC19M2\_OSC\_HW\_CTL AND HW\_CTL).

Writing zero to this register will disable the RC osc

#### CLK\_DIST\_RC\_CTL

Bits	Name	Туре	Description
7	FORCE_RC19M2_OSC_ ON	read- write	RC19M2RC_OSC_ON: Force relaxation oscillator ON (higher priority than FORCE_RC19M2_OSC_ON)
0	RC19M2_OSC_HW_CTL	read- write	RC oscillator state follows HW requests.

## 0x5948 CLK\_DIST\_PD\_CTL

Type: read-write Clock: PBUS\_WRCLK Reset State: 0x80 Reset Name: PERPH\_RB

## CLK\_DIST\_PD\_CTL

Bits	Name	Туре	Description
7	PD_EN	read- write	1' = Enable the pulldown on SYS_CLK pad (used only on the slave pmic)





# 6 PBS\_CLIENTn

## 6.1 Overview

Table 6-1 Blocks

	Name				
PBS_CLIENT0	0				
PBS_CLIENT1	V. C.				
PBS_CLIENT2	73° CO				
PBS_CLIENT3	A. "9."				
PBS_CLIENT4					
PBS_CLIENT5					
PBS_CLIENT6	100 Vis 150				
PBS_CLIENT7	V 2 . 6				

# 6.2 PBS\_CLIENTO\_PBS\_CLIENT

## 0x7104 PBS\_CLIENT0\_PERPH\_TYPE

**Type:** read-only

Clock: PBUS\_WRCLK Reset State: 0x16 Reset Name: N/A

Peripheral Type

#### PBS\_CLIENTO\_PERPH\_TYPE

Bits	Name	Туре	Description
7:0	TYPE	read- only	PBS Reset State: 0x16

#### 0x7105 PBS CLIENTO PERPH SUBTYPE

**Type:** read-only

Clock: PBUS\_WRCLK Reset State: 0x08 Reset Name: N/A

Peripheral SubType

## PBS\_CLIENTO\_PERPH\_SUBTYPE

Bits	Name	Туре	Description
7:0	SUBTYPE	read- only	Client 0 Reset State: 0x08

## 0x7108 PBS\_CLIENT0\_STATUS0

**Type:** read-only

Clock: PBUS\_WRCLK
Reset State: 0bXXXXX000

**Reset Name:** N/A

Status Registers

#### PBS\_CLIENTO\_STATUS0

Bits	Name	Туре	Description
7	TRIG_EN_STATUS	read- only	Overall trigger-sequence enable state

## PBS\_CLIENT0\_STATUS0 (Continued)

Bits	Name	Туре	Description
5:4	COMP_STATUS	read- only	These bits show the completion state of this client trigger-sequence pair.
			00 = In execution.
			01 = Normal completion
			10 = Error completion.
			11= Abort completion.
2:0	TRIG_FSM_STATUS	read- only	Show state of trigger slice FSM.

## 0x7110 PBS\_CLIENT0\_INT\_RT\_STS

**Type:** read-only

Clock: PBUS\_WRCLK Reset State: 0x00

Reset Name: PBS\_CORE\_PERPH\_RB

**Interrupt Real Time Status Bits** 

## PBS\_CLIENTO\_INT\_RT\_STS

Bits	Name	Type	Description
1	SEQ_ENDED_RT_STS	read- only	
0	SEQ_ERROR_RT_STS	read- only	

## 0x7111 PBS\_CLIENT0\_INT\_SET\_TYPE

Type: read-write Clock: PBUS\_WRCLK Reset State: 0x00

Reset Name: PBS\_CORE\_PERPH\_RB

0 =use level trigger interrupts, 1 =use edge trigger interrupts

## PBS\_CLIENTO\_INT\_SET\_TYPE

Bits	Name	Туре	Description
1	SEQ_ENDED_TYPE	read- write	
0	SEQ_ERROR_TYPE	read- write	

#### 0x7112 PBS CLIENTO INT POLARITY HIGH

Type: read-write Clock: PBUS\_WRCLK Reset State: 0x00

Reset Name: PBS\_CORE\_PERPH\_RB

1= Interrupt will trigger on a level high (rising edge) event, 0 = level high triggering is disabled

#### PBS\_CLIENT0\_INT\_POLARITY\_HIGH

Bits	Name	Туре	Description
1	SEQ_ENDED_HIGH	read- write	
0	SEQ_ERROR_HIGH	read- write	

## 0x7113 PBS\_CLIENT0\_INT\_POLARITY\_LOW

Type: read-write Clock: PBUS\_WRCLK Reset State: 0x00

Reset Name: PBS\_CORE\_PERPH\_RB

1' = Interrupt will trigger on a level low (falling edge) event, '0' = level low triggering is disabled

## PBS\_CLIENT0\_INT\_POLARITY\_LOW

Bits	Name	Туре	Description
1	SEQ_ENDED_LOW	read- write	
0	SEQ_ERROR_LOW	read- write	

## 0x7114 PBS\_CLIENT0\_INT\_LATCHED\_CLR

Type: write-only Clock: PBUS\_WRCLK Reset State: 0x00

**Reset Name:** PBS\_CORE\_PERPH\_RB

Writing a '1' to this interrupt will rearm the interrupt when an interrupt is pending. It clears the

internal sticky and sent bits

#### PBS\_CLIENT0\_INT\_LATCHED\_CLR

Bits	Name	Туре	Description
1	SEQ_ENDED_LATCHED_ CLR	write- only	
0	SEQ_ERROR_LATCHED _CLR	write- only	

## 0x7115 PBS\_CLIENT0\_INT\_EN\_SET

Type: read-write Clock: PBUS\_WRCLK

**Reset State:** 0x00

Reset Name: PBS\_CORE\_PERPH\_RB

Writing '0' to this register has no effect. Writing a '1' will enable the corresponding interrupt. Reading this register will readback enable status

PMIC\_SET\_MASK

#### PBS CLIENTO INT EN SET

Bits	Name	Type	Description
1	SEQ_ENDED_EN_SET	read- write	2.
0	SEQ_ERROR_EN_SET	read- write	

## 0x7116 PBS CLIENTO INT EN CLR

Type: read-write Clock: PBUS\_WRCLK Reset State: 0x00

**Reset Name:** PBS\_CORE\_PERPH\_RB

Writing '0' to this register has no effect. Writing a '1' will disable the corresponding interrupt.

Reading this register will readback enable status

PMIC\_CLR\_MASK=INT\_EN\_SET

#### PBS\_CLIENTO\_INT\_EN\_CLR

Bits	Name	Туре	Description
1	SEQ_ENDED_EN_CLR	read- write	

## PBS\_CLIENT0\_INT\_EN\_CLR (Continued)

Bits	Name	Type	Description
0	SEQ_ERROR_EN_CLR	read- write	

## 0x7118 PBS\_CLIENT0\_INT\_LATCHED\_STS

**Type:** read-only

Clock: PBUS\_WRCLK Reset State: 0x00

Reset Name: PBS\_CORE\_PERPH\_RB

Debug: Latched (Sticky) Interrupt. '1' indicates that the interrupt has triggered. Once the latched bit is set it can only be cleared by writing the clear bit.

#### PBS\_CLIENTO\_INT\_LATCHED\_STS

Bits	Name	Туре	Description
1	SEQ_ENDED_LATCHED_ STS	read- only	CON
0	SEQ_ERROR_LATCHED _STS	read- only	

# 0x7119 PBS\_CLIENT0\_INT\_PENDING\_STS

Type: read-only

Clock: PBUS\_WRCLK Reset State: 0x00

Reset Name: PBS\_CORE\_PERPH\_RB

Debug: Pending is set if interrupt has been sent but not cleared.

## PBS\_CLIENTO\_INT\_PENDING\_STS

Bits	Name	Туре	Description
1	SEQ_ENDED_PENDING_ STS	read- only	
0	SEQ_ERROR_PENDING _STS	read- only	

## 0x711A PBS\_CLIENT0\_INT\_MID\_SEL

Type: read-write Clock: PBUS\_WRCLK Reset State: 0x00

**Reset Name:** PBS\_CORE\_PERPH\_RB

Selects the MID that will receive the interrupt

#### PBS\_CLIENT0\_INT\_MID\_SEL

Bits	Name	Туре	Description
1:0	INT_MID_SEL	read- write	

## 0x711B PBS CLIENTO INT PRIORITY

Type: read-write Clock: PBUS\_WRCLK Reset State: 0x00

Reset Name: PBS\_CORE\_PERPH\_RB

SR=0 A=1

#### PBS\_CLIENT0\_INT\_PRIORITY

В	its	Name	Туре	Description
	0	INT_PRIORITY	read- write	

# 0x7140 PBS\_CLIENT0\_TRIG\_CFG

Type: read-write Clock: PBUS\_WRCLK Reset State: 0x80

Reset Name: PBS\_CORE\_PERPH\_RB

**Trigger Configuration** 

PMIC\_SYNC=pbs\_clk:pbs\_rb

#### PBS\_CLIENT0\_TRIG\_CFG

Bits	Name	Туре	Description
7	TRIGGER_RE_EN	read- write	1 = Enable Rising Edge Trigger 0 = Disable Falling Edge Trigger

# PBS\_CLIENT0\_TRIG\_CFG (Continued)

Bits	Name	Туре	Description
6	TRIGGER_FE_EN	read- write	1 = Enable Falling Edge Trigger 0 = Disable Falling Edge Trigger

# 0x7142 PBS\_CLIENT0\_TRIG\_CTL

Type: write-only Clock: PBUS\_WRCLK Reset State: 0x00

Reset Name: PBS\_CORE\_PERPH\_RB

## PBS\_CLIENT0\_TRIG\_CTL

Bits	Name	Туре	Description
0	SW_TRIGGER	write- only	Writing 0x01 to this register will immediately create a trigger pulse.

# 0x7146 PBS\_CLIENT0\_EN\_CTL

Type: read-write Clock: PBUS\_WRCLK Reset State: 0x80

Reset Name: PBS\_CORE\_PERPH\_RB

PMIC\_SYNC=pbs\_clk:pbs\_rb

## PBS\_CLIENTO\_EN\_CTL

Bits	Name	Туре	Description
7	TRIGGER_EN	read- write	Must be set to 1 to enable all triggers in the peripheral

# 6.3 PBS\_CLIENT1\_PBS\_CLIENT

# 0x7204 PBS\_CLIENT1\_PERPH\_TYPE

**Type:** read-only

Clock: PBUS\_WRCLK Reset State: 0x16 Reset Name: N/A

Peripheral Type

#### PBS\_CLIENT1\_PERPH\_TYPE

Bits	Name	Туре	Description
7:0	TYPE	read- only	PBS Reset State: 0x16

#### 0x7205 PBS CLIENT1 PERPH SUBTYPE

**Type:** read-only

Clock: PBUS\_WRCLK Reset State: 0x08 Reset Name: N/A

Peripheral SubType

## PBS\_CLIENT1\_PERPH\_SUBTYPE

Bits	Name	Туре	Description
7:0	SUBTYPE	read- only	Client 1 Reset State: 0x08

## 0x7208 PBS\_CLIENT1\_STATUS0

**Type:** read-only

Clock: PBUS\_WRCLK
Reset State: 0bXXXXX000

**Reset Name:** N/A

Status Registers

#### PBS\_CLIENT1\_STATUS0

Bits	Name	Туре	Description
7	TRIG_EN_STATUS	read- only	Overall trigger-sequence enable state

## PBS\_CLIENT1\_STATUS0 (Continued)

Bits	Name	Туре	Description
5:4	COMP_STATUS	read- only	These bits show the completion state of this client trigger-sequence pair.
			00 = In execution.
			01 = Normal completion
			10 = Error completion.
			11= Abort completion.
2:0	TRIG_FSM_STATUS	read- only	Show state of trigger slice FSM.

# 0x7210 PBS\_CLIENT1\_INT\_RT\_STS

**Type:** read-only

Clock: PBUS\_WRCLK Reset State: 0x00

Reset Name: PBS\_CORE\_PERPH\_RB

**Interrupt Real Time Status Bits** 

# PBS\_CLIENT1\_INT\_RT\_STS

Bits	Name	Type	Description
1	SEQ_ENDED_RT_STS	read- only	
0	SEQ_ERROR_RT_STS	read- only	

## 0x7211 PBS\_CLIENT1\_INT\_SET\_TYPE

Type: read-write Clock: PBUS\_WRCLK Reset State: 0x00

Reset Name: PBS\_CORE\_PERPH\_RB

0 =use level trigger interrupts, 1 =use edge trigger interrupts

## PBS\_CLIENT1\_INT\_SET\_TYPE

Bits	Name	Туре	Description
1	SEQ_ENDED_TYPE	read- write	
0	SEQ_ERROR_TYPE	read- write	

#### 0x7212 PBS CLIENT1 INT POLARITY HIGH

Type: read-write Clock: PBUS\_WRCLK Reset State: 0x00

Reset Name: PBS\_CORE\_PERPH\_RB

1= Interrupt will trigger on a level high (rising edge) event, 0 = level high triggering is disabled

#### PBS\_CLIENT1\_INT\_POLARITY\_HIGH

Bits	Name	Туре	Description
1	SEQ_ENDED_HIGH	read- write	
0	SEQ_ERROR_HIGH	read- write	

# 0x7213 PBS\_CLIENT1\_INT\_POLARITY\_LOW

Type: read-write Clock: PBUS\_WRCLK Reset State: 0x00

Reset Name: PBS\_CORE\_PERPH\_RB

1' = Interrupt will trigger on a level low (falling edge) event, '0' = level low triggering is disabled

## PBS\_CLIENT1\_INT\_POLARITY\_LOW

Bits	Name	Туре	Description
1	SEQ_ENDED_LOW	read- write	
0	SEQ_ERROR_LOW	read- write	

## 0x7214 PBS\_CLIENT1\_INT\_LATCHED\_CLR

**Type:** write-only **Clock:** PBUS\_WRCLK **Reset State:** 0x00

**Reset Name:** PBS\_CORE\_PERPH\_RB

Writing a '1' to this interrupt will rearm the interrupt when an interrupt is pending. It clears the

internal sticky and sent bits

#### PBS\_CLIENT1\_INT\_LATCHED\_CLR

Bits	Name	Туре	Description
1	SEQ_ENDED_LATCHED_ CLR	write- only	
0	SEQ_ERROR_LATCHED _CLR	write- only	

## 0x7215 PBS\_CLIENT1\_INT\_EN\_SET

**Type:** read-write **Clock:** PBUS\_WRCLK

Reset State: 0x00 Reset Name: PBS\_CORE\_PERPH\_RB

Writing '0' to this register has no effect. Writing a '1' will enable the corresponding interrupt.

Reading this register will readback enable status

PMIC\_SET\_MASK

#### PBS CLIENT1 INT EN SET

Bits	Name	Type	Description
1	SEQ_ENDED_EN_SET	read- write	2.
0	SEQ_ERROR_EN_SET	read- write	

## 0x7216 PBS CLIENT1 INT EN CLR

Type: read-write Clock: PBUS\_WRCLK Reset State: 0x00

**Reset Name:** PBS\_CORE\_PERPH\_RB

Writing '0' to this register has no effect. Writing a '1' will disable the corresponding interrupt.

Reading this register will readback enable status

PMIC\_CLR\_MASK=INT\_EN\_SET

#### PBS\_CLIENT1\_INT\_EN\_CLR

Bits	Name	Type	Description
1	SEQ_ENDED_EN_CLR	read- write	

# PBS\_CLIENT1\_INT\_EN\_CLR (Continued)

Bits	Name	Type	Description
0	SEQ_ERROR_EN_CLR	read- write	

## 0x7218 PBS\_CLIENT1\_INT\_LATCHED\_STS

**Type:** read-only

Clock: PBUS\_WRCLK Reset State: 0x00

Reset Name: PBS\_CORE\_PERPH\_RB

Debug: Latched (Sticky) Interrupt. '1' indicates that the interrupt has triggered. Once the latched bit is set it can only be cleared by writing the clear bit.

## PBS\_CLIENT1\_INT\_LATCHED\_STS

Bits	Name	Туре	Description
1	SEQ_ENDED_LATCHED_ STS	read- only	CONT
0	SEQ_ERROR_LATCHED _STS	read- only	

# 0x7219 PBS\_CLIENT1\_INT\_PENDING\_STS

Type: read-only

Clock: PBUS\_WRCLK Reset State: 0x00

Reset Name: PBS\_CORE\_PERPH\_RB

Debug: Pending is set if interrupt has been sent but not cleared.

## PBS\_CLIENT1\_INT\_PENDING\_STS

Bits	Name	Туре	Description
1	SEQ_ENDED_PENDING_ STS	read- only	
0	SEQ_ERROR_PENDING _STS	read- only	

# 0x721A PBS\_CLIENT1\_INT\_MID\_SEL

Type: read-write Clock: PBUS\_WRCLK Reset State: 0x00

**Reset Name:** PBS\_CORE\_PERPH\_RB

Selects the MID that will receive the interrupt

## PBS\_CLIENT1\_INT\_MID\_SEL

Bits	Name	Туре	Description
1:0	INT_MID_SEL	read- write	

# 0x721B PBS\_CLIENT1\_INT\_PRIORITY

Type: read-write Clock: PBUS\_WRCLK Reset State: 0x00

Reset Name: PBS\_CORE\_PERPH\_RB

SR=0 A=1

#### PBS\_CLIENT1\_INT\_PRIORITY

Bits	Name	Туре	Description
0	INT_PRIORITY	read- write	

# 0x7240 PBS\_CLIENT1\_TRIG\_CFG

Type: read-write Clock: PBUS\_WRCLK Reset State: 0x80

Reset Name: PBS\_CORE\_PERPH\_RB

**Trigger Configuration** 

PMIC\_SYNC=pbs\_clk:pbs\_rb

#### PBS\_CLIENT1\_TRIG\_CFG

Bits	Name	Туре	Description
7	TRIGGER_RE_EN	read- write	1 = Enable Rising Edge Trigger 0 = Disable Falling Edge Trigger

# PBS\_CLIENT1\_TRIG\_CFG (Continued)

Bits	Name	Туре	Description
6	TRIGGER_FE_EN	read- write	1 = Enable Falling Edge Trigger 0 = Disable Falling Edge Trigger

# 0x7242 PBS\_CLIENT1\_TRIG\_CTL

Type: write-only Clock: PBUS\_WRCLK Reset State: 0x00

Reset Name: PBS\_CORE\_PERPH\_RB

## PBS\_CLIENT1\_TRIG\_CTL

Bits	Name	Туре	Description
0	SW_TRIGGER	write- only	Writing 0x01 to this register will immediately create a trigger pulse.

## 0x7246 PBS\_CLIENT1\_EN\_CTL

Type: read-write Clock: PBUS\_WRCLK Reset State: 0x80

Reset Name: PBS\_CORE\_PERPH\_RB

PMIC\_SYNC=pbs\_clk:pbs\_rb

## PBS\_CLIENT1\_EN\_CTL

Bits	Name	Туре	Description
7	TRIGGER_EN	read- write	Must be set to 1 to enable all triggers in the peripheral

# 6.4 PBS\_CLIENT2\_PBS\_CLIENT

# 0x7304 PBS\_CLIENT2\_PERPH\_TYPE

**Type:** read-only

Clock: PBUS\_WRCLK Reset State: 0x16 Reset Name: N/A

Peripheral Type

#### PBS\_CLIENT2\_PERPH\_TYPE

Bits	Name	Туре	Description
7:0	TYPE	read- only	PBS Reset State: 0x16

#### 0x7305 PBS CLIENT2 PERPH SUBTYPE

**Type:** read-only

Clock: PBUS\_WRCLK Reset State: 0x08 Reset Name: N/A

Peripheral SubType

## PBS\_CLIENT2\_PERPH\_SUBTYPE

Bits	Name	Туре	Description
7:0	SUBTYPE	read- only	Client 2 Reset State: 0x08

## 0x7308 PBS\_CLIENT2\_STATUS0

**Type:** read-only

Clock: PBUS\_WRCLK
Reset State: 0bXXXXX000

**Reset Name:** N/A

Status Registers

#### PBS\_CLIENT2\_STATUS0

Bits	Name	Type	Description
7	TRIG_EN_STATUS	read- only	Overall trigger-sequence enable state

## PBS\_CLIENT2\_STATUS0 (Continued)

Bits	Name	Туре	Description
5:4	COMP_STATUS	read- only	These bits show the completion state of this client trigger-sequence pair.
			00 = In execution.
			01 = Normal completion
			10 = Error completion.
			11= Abort completion.
2:0	TRIG_FSM_STATUS	read- only	Show state of trigger slice FSM.

# 0x7310 PBS\_CLIENT2\_INT\_RT\_STS

**Type:** read-only

Clock: PBUS\_WRCLK Reset State: 0x00

Reset Name: PBS\_CORE\_PERPH\_RB

**Interrupt Real Time Status Bits** 

# PBS\_CLIENT2\_INT\_RT\_STS

Bits	Name	Type	Description
1	SEQ_ENDED_RT_STS	read- only	2
0	SEQ_ERROR_RT_STS	read- only	

# 0x7311 PBS\_CLIENT2\_INT\_SET\_TYPE

Type: read-write Clock: PBUS\_WRCLK Reset State: 0x00

Reset Name: PBS\_CORE\_PERPH\_RB

0 =use level trigger interrupts, 1 =use edge trigger interrupts

## PBS\_CLIENT2\_INT\_SET\_TYPE

Bits	Name	Туре	Description
1	SEQ_ENDED_TYPE	read- write	
0	SEQ_ERROR_TYPE	read- write	

#### 0x7312 PBS CLIENT2 INT POLARITY HIGH

Type: read-write Clock: PBUS\_WRCLK Reset State: 0x00

Reset Name: PBS\_CORE\_PERPH\_RB

1= Interrupt will trigger on a level high (rising edge) event, 0 = level high triggering is disabled

#### PBS\_CLIENT2\_INT\_POLARITY\_HIGH

Bits	Name	Туре	Description
1	SEQ_ENDED_HIGH	read- write	
0	SEQ_ERROR_HIGH	read- write	

# 0x7313 PBS\_CLIENT2\_INT\_POLARITY\_LOW

Type: read-write Clock: PBUS\_WRCLK Reset State: 0x00

Reset Name: PBS\_CORE\_PERPH\_RB

1' = Interrupt will trigger on a level low (falling edge) event, '0' = level low triggering is disabled

## PBS\_CLIENT2\_INT\_POLARITY\_LOW

Bits	Name	Туре	Description
1	SEQ_ENDED_LOW	read- write	
0	SEQ_ERROR_LOW	read- write	

## 0x7314 PBS\_CLIENT2\_INT\_LATCHED\_CLR

Type: write-only Clock: PBUS\_WRCLK Reset State: 0x00

**Reset Name:** PBS\_CORE\_PERPH\_RB

Writing a '1' to this interrupt will rearm the interrupt when an interrupt is pending. It clears the

internal sticky and sent bits

#### PBS\_CLIENT2\_INT\_LATCHED\_CLR

Bits	Name	Туре	Description
1	SEQ_ENDED_LATCHED_ CLR	write- only	
0	SEQ_ERROR_LATCHED _CLR	write- only	

## 0x7315 PBS\_CLIENT2\_INT\_EN\_SET

Type: read-write Clock: PBUS\_WRCLK

**Reset State:** 0x00

Reset Name: PBS\_CORE\_PERPH\_RB

Writing '0' to this register has no effect. Writing a '1' will enable the corresponding interrupt. Reading this register will readback enable status

PMIC\_SET\_MASK

#### PBS CLIENT2 INT EN SET

Bits	Name	Type	Description
1	SEQ_ENDED_EN_SET	read- write	2.
0	SEQ_ERROR_EN_SET	read- write	

## 0x7316 PBS CLIENT2 INT EN CLR

Type: read-write Clock: PBUS\_WRCLK Reset State: 0x00

**Reset Name:** PBS\_CORE\_PERPH\_RB

Writing '0' to this register has no effect. Writing a '1' will disable the corresponding interrupt.

Reading this register will readback enable status

PMIC\_CLR\_MASK=INT\_EN\_SET

#### PBS\_CLIENT2\_INT\_EN\_CLR

Bits	Name	Type	Description
1	SEQ_ENDED_EN_CLR	read- write	

#### PBS\_CLIENT2\_INT\_EN\_CLR (Continued)

Bits	Name	Type	Description
0	SEQ_ERROR_EN_CLR	read- write	

## 0x7318 PBS\_CLIENT2\_INT\_LATCHED\_STS

**Type:** read-only

Clock: PBUS\_WRCLK Reset State: 0x00

Reset Name: PBS\_CORE\_PERPH\_RB

Debug: Latched (Sticky) Interrupt. '1' indicates that the interrupt has triggered. Once the latched bit is set it can only be cleared by writing the clear bit.

## PBS\_CLIENT2\_INT\_LATCHED\_STS

Bits	Name	Туре	Description
1	SEQ_ENDED_LATCHED_ STS	read- only	CONT
0	SEQ_ERROR_LATCHED _STS	read- only	

# 0x7319 PBS\_CLIENT2\_INT\_PENDING\_STS

Type: read-only

Clock: PBUS\_WRCLK Reset State: 0x00

Reset Name: PBS\_CORE\_PERPH\_RB

Debug: Pending is set if interrupt has been sent but not cleared.

## PBS\_CLIENT2\_INT\_PENDING\_STS

Bits	Name	Туре	Description
1	SEQ_ENDED_PENDING_ STS	read- only	
0	SEQ_ERROR_PENDING _STS	read- only	

# 0x731A PBS\_CLIENT2\_INT\_MID\_SEL

Type: read-write Clock: PBUS\_WRCLK Reset State: 0x00

**Reset Name:** PBS\_CORE\_PERPH\_RB

Selects the MID that will receive the interrupt

#### PBS\_CLIENT2\_INT\_MID\_SEL

Bits	Name	Туре	Description
1:0	INT_MID_SEL	read- write	

# 0x731B PBS\_CLIENT2\_INT\_PRIORITY

Type: read-write Clock: PBUS\_WRCLK Reset State: 0x00

Reset Name: PBS\_CORE\_PERPH\_RB

SR=0 A=1

#### PBS\_CLIENT2\_INT\_PRIORITY

Bits	Name	Туре	Description
0	INT_PRIORITY	read- write	

# 0x7340 PBS\_CLIENT2\_TRIG\_CFG

Type: read-write Clock: PBUS\_WRCLK Reset State: 0x80

Reset Name: PBS\_CORE\_PERPH\_RB

**Trigger Configuration** 

PMIC\_SYNC=pbs\_clk:pbs\_rb

#### PBS\_CLIENT2\_TRIG\_CFG

Bits	Name	Туре	Description
7	TRIGGER_RE_EN	read- write	1 = Enable Rising Edge Trigger 0 = Disable Falling Edge Trigger

# PBS\_CLIENT2\_TRIG\_CFG (Continued)

Bits	Name	Туре	Description
6	TRIGGER_FE_EN	read- write	1 = Enable Falling Edge Trigger 0 = Disable Falling Edge Trigger

# 0x7342 PBS\_CLIENT2\_TRIG\_CTL

Type: write-only Clock: PBUS\_WRCLK Reset State: 0x00

Reset Name: PBS\_CORE\_PERPH\_RB

## PBS\_CLIENT2\_TRIG\_CTL

Bits	Name	Туре	Description
0	SW_TRIGGER	write- only	Writing 0x01 to this register will immediately create a trigger pulse.

## 0x7346 PBS\_CLIENT2\_EN\_CTL

Type: read-write Clock: PBUS\_WRCLK Reset State: 0x80

Reset Name: PBS\_CORE\_PERPH\_RB

PMIC\_SYNC=pbs\_clk:pbs\_rb

## PBS\_CLIENT2\_EN\_CTL

Bits	Name	Туре	Description
7	TRIGGER_EN	read- write	Must be set to 1 to enable all triggers in the peripheral

# 6.5 PBS\_CLIENT3\_PBS\_CLIENT

# 0x7404 PBS\_CLIENT3\_PERPH\_TYPE

**Type:** read-only

Clock: PBUS\_WRCLK Reset State: 0x16 Reset Name: N/A

Peripheral Type

#### PBS\_CLIENT3\_PERPH\_TYPE

Bits	Name	Туре	Description
7:0	TYPE	read- only	PBS Reset State: 0x16

#### 0x7405 PBS CLIENT3 PERPH SUBTYPE

**Type:** read-only

Clock: PBUS\_WRCLK Reset State: 0x08 Reset Name: N/A

Peripheral SubType

## PBS\_CLIENT3\_PERPH\_SUBTYPE

Bits	Name	Туре	Description
7:0	SUBTYPE	read- only	Client 3 Reset State: 0x08

## 0x7408 PBS\_CLIENT3\_STATUS0

**Type:** read-only

Clock: PBUS\_WRCLK
Reset State: 0bXXXXX000

**Reset Name:** N/A

Status Registers

#### PBS\_CLIENT3\_STATUS0

Bits	Name	Туре	Description
7	TRIG_EN_STATUS	read- only	Overall trigger-sequence enable state

## PBS\_CLIENT3\_STATUS0 (Continued)

Bits	Name	Туре	Description
5:4	COMP_STATUS	read- only	These bits show the completion state of this client trigger-sequence pair.
			00 = In execution.
			01 = Normal completion
			10 = Error completion.
			11= Abort completion.
2:0	TRIG_FSM_STATUS	read- only	Show state of trigger slice FSM.

# 0x7410 PBS\_CLIENT3\_INT\_RT\_STS

**Type:** read-only

Clock: PBUS\_WRCLK Reset State: 0x00

Reset Name: PBS\_CORE\_PERPH\_RB

**Interrupt Real Time Status Bits** 

# PBS\_CLIENT3\_INT\_RT\_STS

Bits	Name	Type	Description
1	SEQ_ENDED_RT_STS	read- only	
0	SEQ_ERROR_RT_STS	read- only	

## 0x7411 PBS\_CLIENT3\_INT\_SET\_TYPE

Type: read-write Clock: PBUS\_WRCLK Reset State: 0x00

Reset Name: PBS\_CORE\_PERPH\_RB

0 =use level trigger interrupts, 1 =use edge trigger interrupts

## PBS\_CLIENT3\_INT\_SET\_TYPE

Bits	Name	Туре	Description
1	SEQ_ENDED_TYPE	read- write	
0	SEQ_ERROR_TYPE	read- write	

#### 0x7412 PBS\_CLIENT3\_INT\_POLARITY\_HIGH

Type: read-write Clock: PBUS\_WRCLK Reset State: 0x00

Reset Name: PBS\_CORE\_PERPH\_RB

1= Interrupt will trigger on a level high (rising edge) event, 0 = level high triggering is disabled

#### PBS\_CLIENT3\_INT\_POLARITY\_HIGH

Bits	Name	Туре	Description
1	SEQ_ENDED_HIGH	read- write	
0	SEQ_ERROR_HIGH	read- write	

# 0x7413 PBS\_CLIENT3\_INT\_POLARITY\_LOW

Type: read-write Clock: PBUS\_WRCLK Reset State: 0x00

Reset Name: PBS\_CORE\_PERPH\_RB

1' = Interrupt will trigger on a level low (falling edge) event, '0' = level low triggering is disabled

## PBS\_CLIENT3\_INT\_POLARITY\_LOW

Bits	Name	Туре	Description
1	SEQ_ENDED_LOW	read- write	
0	SEQ_ERROR_LOW	read- write	

## 0x7414 PBS\_CLIENT3\_INT\_LATCHED\_CLR

Type: write-only Clock: PBUS\_WRCLK Reset State: 0x00

**Reset Name:** PBS\_CORE\_PERPH\_RB

Writing a '1' to this interrupt will rearm the interrupt when an interrupt is pending. It clears the

internal sticky and sent bits

#### PBS\_CLIENT3\_INT\_LATCHED\_CLR

Bits	Name	Туре	Description
1	SEQ_ENDED_LATCHED_ CLR	write- only	
0	SEQ_ERROR_LATCHED _CLR	write- only	

## 0x7415 PBS\_CLIENT3\_INT\_EN\_SET

Type: read-write Clock: PBUS\_WRCLK

**Reset State:** 0x00

Reset Name: PBS\_CORE\_PERPH\_RB

Writing '0' to this register has no effect. Writing a '1' will enable the corresponding interrupt. Reading this register will readback enable status

Reading this register will readback chable

PMIC\_SET\_MASK

#### PBS CLIENT3 INT EN SET

Bits	Name	Type	Description
1	SEQ_ENDED_EN_SET	read- write	2.
0	SEQ_ERROR_EN_SET	read- write	

## 0x7416 PBS CLIENT3 INT EN CLR

Type: read-write Clock: PBUS\_WRCLK Reset State: 0x00

**Reset Name:** PBS\_CORE\_PERPH\_RB

Writing '0' to this register has no effect. Writing a '1' will disable the corresponding interrupt.

Reading this register will readback enable status

PMIC\_CLR\_MASK=INT\_EN\_SET

#### PBS\_CLIENT3\_INT\_EN\_CLR

Bits	Name	Type	Description
1	SEQ_ENDED_EN_CLR	read- write	

## PBS\_CLIENT3\_INT\_EN\_CLR (Continued)

Bits	Name	Туре	Description
0	SEQ_ERROR_EN_CLR	read- write	

## 0x7418 PBS\_CLIENT3\_INT\_LATCHED\_STS

**Type:** read-only

Clock: PBUS\_WRCLK Reset State: 0x00

Reset Name: PBS\_CORE\_PERPH\_RB

Debug: Latched (Sticky) Interrupt. '1' indicates that the interrupt has triggered. Once the latched bit is set it can only be cleared by writing the clear bit.

#### PBS\_CLIENT3\_INT\_LATCHED\_STS

Bits	Name	Туре	Description
1	SEQ_ENDED_LATCHED_ STS	read- only	CONT
0	SEQ_ERROR_LATCHED _STS	read- only	

# 0x7419 PBS\_CLIENT3\_INT\_PENDING\_STS

Type: read-only

Clock: PBUS\_WRCLK Reset State: 0x00

Reset Name: PBS\_CORE\_PERPH\_RB

Debug: Pending is set if interrupt has been sent but not cleared.

## PBS\_CLIENT3\_INT\_PENDING\_STS

Bits	Name	Туре	Description
1	SEQ_ENDED_PENDING_ STS	read- only	
0	SEQ_ERROR_PENDING _STS	read- only	

## 0x741A PBS\_CLIENT3\_INT\_MID\_SEL

Type: read-write Clock: PBUS\_WRCLK Reset State: 0x00

**Reset Name:** PBS\_CORE\_PERPH\_RB

Selects the MID that will receive the interrupt

#### PBS\_CLIENT3\_INT\_MID\_SEL

Bits	Name	Туре	Description
1:0	INT_MID_SEL	read- write	

# 0x741B PBS\_CLIENT3\_INT\_PRIORITY

Type: read-write Clock: PBUS\_WRCLK Reset State: 0x00

Reset Name: PBS\_CORE\_PERPH\_RB

SR=0 A=1

#### PBS\_CLIENT3\_INT\_PRIORITY

В	its	Name	Туре	Description
	0	INT_PRIORITY	read- write	

# 0x7440 PBS\_CLIENT3\_TRIG\_CFG

Type: read-write Clock: PBUS\_WRCLK Reset State: 0x80

Reset Name: PBS\_CORE\_PERPH\_RB

**Trigger Configuration** 

PMIC\_SYNC=pbs\_clk:pbs\_rb

#### PBS\_CLIENT3\_TRIG\_CFG

Bits	Name	Туре	Description
7	TRIGGER_RE_EN	read- write	1 = Enable Rising Edge Trigger 0 = Disable Falling Edge Trigger

# PBS\_CLIENT3\_TRIG\_CFG (Continued)

Bits	Name	Туре	Description
6	TRIGGER_FE_EN	read- write	1 = Enable Falling Edge Trigger 0 = Disable Falling Edge Trigger

# 0x7442 PBS\_CLIENT3\_TRIG\_CTL

Type: write-only Clock: PBUS\_WRCLK Reset State: 0x00

Reset Name: PBS\_CORE\_PERPH\_RB

## PBS\_CLIENT3\_TRIG\_CTL

Bits	Name	Туре	Description
0	SW_TRIGGER	write- only	Writing 0x01 to this register will immediately create a trigger pulse.

## 0x7446 PBS\_CLIENT3\_EN\_CTL

Type: read-write Clock: PBUS\_WRCLK Reset State: 0x80

Reset Name: PBS\_CORE\_PERPH\_RB

PMIC\_SYNC=pbs\_clk:pbs\_rb

## PBS\_CLIENT3\_EN\_CTL

Bits	Name	Туре	Description
7	TRIGGER_EN	read- write	Must be set to 1 to enable all triggers in the peripheral

# 6.6 PBS\_CLIENT4\_PBS\_CLIENT

# 0x7504 PBS\_CLIENT4\_PERPH\_TYPE

**Type:** read-only

Clock: PBUS\_WRCLK Reset State: 0x16 Reset Name: N/A

Peripheral Type

#### PBS\_CLIENT4\_PERPH\_TYPE

Bits	Name	Туре	Description
7:0	TYPE	read- only	PBS Reset State:0x16

#### 0x7505 PBS CLIENT4 PERPH SUBTYPE

**Type:** read-only

Clock: PBUS\_WRCLK Reset State: 0x08 Reset Name: N/A

Peripheral SubType

## PBS\_CLIENT4\_PERPH\_SUBTYPE

Bits	Name	Туре	Description
7:0	SUBTYPE	read- only	Client 4 Reset State: 0x08

## 0x7508 PBS\_CLIENT4\_STATUS0

**Type:** read-only

Clock: PBUS\_WRCLK
Reset State: 0bXXXXX000

**Reset Name:** N/A

Status Registers

#### PBS\_CLIENT4\_STATUS0

Bits	Name	Туре	Description
7	TRIG_EN_STATUS	read- only	Overall trigger-sequence enable state

## PBS\_CLIENT4\_STATUS0 (Continued)

Bits	Name	Туре	Description
5:4	COMP_STATUS	read- only	These bits show the completion state of this client trigger-sequence pair.
			00 = In execution.
			01 = Normal completion
			10 = Error completion.
			11= Abort completion.
2:0	TRIG_FSM_STATUS	read- only	Show state of trigger slice FSM.

# 0x7510 PBS\_CLIENT4\_INT\_RT\_STS

**Type:** read-only

Clock: PBUS\_WRCLK Reset State: 0x00

Reset Name: PBS\_CORE\_PERPH\_RB

**Interrupt Real Time Status Bits** 

# PBS\_CLIENT4\_INT\_RT\_STS

Bits	Name	Type	Description
1	SEQ_ENDED_RT_STS	read- only	2
0	SEQ_ERROR_RT_STS	read- only	

## 0x7511 PBS\_CLIENT4\_INT\_SET\_TYPE

Type: read-write Clock: PBUS\_WRCLK Reset State: 0x00

Reset Name: PBS\_CORE\_PERPH\_RB

0 =use level trigger interrupts, 1 =use edge trigger interrupts

## PBS\_CLIENT4\_INT\_SET\_TYPE

Bits	Name	Туре	Description
1	SEQ_ENDED_TYPE	read- write	
0	SEQ_ERROR_TYPE	read- write	

# 0x7512 PBS\_CLIENT4\_INT\_POLARITY\_HIGH

Type: read-write Clock: PBUS\_WRCLK Reset State: 0x00

Reset Name: PBS\_CORE\_PERPH\_RB

1= Interrupt will trigger on a level high (rising edge) event, 0 = level high triggering is disabled

#### PBS\_CLIENT4\_INT\_POLARITY\_HIGH

Bits	Name	Туре	Description
1	SEQ_ENDED_HIGH	read- write	
0	SEQ_ERROR_HIGH	read- write	

# 0x7513 PBS\_CLIENT4\_INT\_POLARITY\_LOW

Type: read-write Clock: PBUS\_WRCLK Reset State: 0x00

Reset Name: PBS\_CORE\_PERPH\_RB

1' = Interrupt will trigger on a level low (falling edge) event, '0' = level low triggering is disabled

## PBS\_CLIENT4\_INT\_POLARITY\_LOW

Bits	Name	Туре	Description
1	SEQ_ENDED_LOW	read- write	
0	SEQ_ERROR_LOW	read- write	

## 0x7514 PBS\_CLIENT4\_INT\_LATCHED\_CLR

Type: write-only Clock: PBUS\_WRCLK Reset State: 0x00

**Reset Name:** PBS\_CORE\_PERPH\_RB

Writing a '1' to this interrupt will rearm the interrupt when an interrupt is pending. It clears the

internal sticky and sent bits

#### PBS\_CLIENT4\_INT\_LATCHED\_CLR

Bits	Name	Туре	Description
1	SEQ_ENDED_LATCHED_ CLR	write- only	
0	SEQ_ERROR_LATCHED _CLR	write- only	

## 0x7515 PBS\_CLIENT4\_INT\_EN\_SET

Type: read-write Clock: PBUS\_WRCLK

**Reset State:** 0x00

Reset Name: PBS\_CORE\_PERPH\_RB

Writing '0' to this register has no effect. Writing a '1' will enable the corresponding interrupt. Reading this register will readback enable status

PMIC\_SET\_MASK

#### PBS CLIENT4 INT EN SET

Bits	Name	Type	Description
1	SEQ_ENDED_EN_SET	read- write	2.
0	SEQ_ERROR_EN_SET	read- write	

## 0x7516 PBS CLIENT4 INT EN CLR

Type: read-write Clock: PBUS\_WRCLK Reset State: 0x00

**Reset Name:** PBS\_CORE\_PERPH\_RB

Writing '0' to this register has no effect. Writing a '1' will disable the corresponding interrupt.

Reading this register will readback enable status

PMIC\_CLR\_MASK=INT\_EN\_SET

## PBS\_CLIENT4\_INT\_EN\_CLR

Bits	Name	Type	Description
1	SEQ_ENDED_EN_CLR	read- write	

# PBS\_CLIENT4\_INT\_EN\_CLR (Continued)

Bits	Name	Type	Description
0	SEQ_ERROR_EN_CLR	read- write	

## 0x7518 PBS\_CLIENT4\_INT\_LATCHED\_STS

**Type:** read-only

Clock: PBUS\_WRCLK Reset State: 0x00

Reset Name: PBS\_CORE\_PERPH\_RB

Debug: Latched (Sticky) Interrupt. '1' indicates that the interrupt has triggered. Once the latched bit is set it can only be cleared by writing the clear bit.

#### PBS\_CLIENT4\_INT\_LATCHED\_STS

Bits	Name	Туре	Description
1	SEQ_ENDED_LATCHED_ STS	read- only	CON
0	SEQ_ERROR_LATCHED _STS	read- only	

# 0x7519 PBS\_CLIENT4\_INT\_PENDING\_STS

**Type:** read-only

Clock: PBUS\_WRCLK Reset State: 0x00

Reset Name: PBS\_CORE\_PERPH\_RB

Debug: Pending is set if interrupt has been sent but not cleared.

## PBS\_CLIENT4\_INT\_PENDING\_STS

Bits	Name	Туре	Description
1	SEQ_ENDED_PENDING_ STS	read- only	
0	SEQ_ERROR_PENDING _STS	read- only	

# 0x751A PBS\_CLIENT4\_INT\_MID\_SEL

Type: read-write Clock: PBUS\_WRCLK Reset State: 0x00

**Reset Name:** PBS\_CORE\_PERPH\_RB

Selects the MID that will receive the interrupt

## PBS\_CLIENT4\_INT\_MID\_SEL

Bits	Name	Туре	Description
1:0	INT_MID_SEL	read- write	

## 0x751B PBS CLIENT4 INT PRIORITY

Type: read-write Clock: PBUS\_WRCLK Reset State: 0x00

Reset Name: PBS\_CORE\_PERPH\_RB

SR=0 A=1

#### PBS\_CLIENT4\_INT\_PRIORITY

В	its	Name	Туре	Description
	0	INT_PRIORITY	read- write	

# 0x7540 PBS\_CLIENT4\_TRIG\_CFG

Type: read-write Clock: PBUS\_WRCLK Reset State: 0x00

Reset Name: PBS\_CORE\_PERPH\_RB

**Trigger Configuration** 

PMIC\_SYNC=pbs\_clk:pbs\_rb

#### PBS\_CLIENT4\_TRIG\_CFG

Bits	Name	Туре	Description
7	TRIGGER_RE_EN	read- write	1 = Enable Rising Edge Trigger 0 = Disable Falling Edge Trigger

# PBS\_CLIENT4\_TRIG\_CFG (Continued)

Bits	Name	Туре	Description
6	TRIGGER_FE_EN	read- write	1 = Enable Falling Edge Trigger 0 = Disable Falling Edge Trigger

# 0x7542 PBS\_CLIENT4\_TRIG\_CTL

**Type:** write-only **Clock:** PBUS\_WRCLK **Reset State:** 0x00

Reset Name: PBS\_CORE\_PERPH\_RB

## PBS\_CLIENT4\_TRIG\_CTL

Bits	Name	Туре	Description
0	SW_TRIGGER	write- only	Writing 0x01 to this register will immediately create a trigger pulse.

## 0x7546 PBS\_CLIENT4\_EN\_CTL

Type: read-write Clock: PBUS\_WRCLK Reset State: 0x00

Reset Name: PBS\_CORE\_PERPH\_RB

PMIC\_SYNC=pbs\_clk:pbs\_rb

## PBS\_CLIENT4\_EN\_CTL

Bits	Name	Туре	Description
7	TRIGGER_EN	read- write	Must be set to 1 to enable all triggers in the peripheral

# 6.7 PBS\_CLIENT5\_PBS\_CLIENT

# 0x7604 PBS\_CLIENT5\_PERPH\_TYPE

**Type:** read-only

Clock: PBUS\_WRCLK Reset State: 0x16 Reset Name: N/A

Peripheral Type

#### PBS\_CLIENT5\_PERPH\_TYPE

Bits	Name	Туре	Description
7:0	TYPE	read- only	PBS Reset State: 0x16

#### 0x7605 PBS CLIENT5 PERPH SUBTYPE

**Type:** read-only

Clock: PBUS\_WRCLK Reset State: 0x08 Reset Name: N/A

Peripheral SubType

## PBS\_CLIENT5\_PERPH\_SUBTYPE

Bits	Name	Туре	Description
7:0	SUBTYPE	read- only	Client 5 Reset State: 0x08

## 0x7608 PBS\_CLIENT5\_STATUS0

**Type:** read-only

Clock: PBUS\_WRCLK
Reset State: 0bXXXXX000

**Reset Name:** N/A

Status Registers

#### PBS\_CLIENT5\_STATUS0

Bits	Name	Type	Description
7	TRIG_EN_STATUS	read- only	Overall trigger-sequence enable state

## PBS\_CLIENT5\_STATUS0 (Continued)

Bits	Name	Туре	Description
5:4	COMP_STATUS	read- only	These bits show the completion state of this client trigger-sequence pair.
			00 = In execution.
			01 = Normal completion
			10 = Error completion.
			11= Abort completion.
2:0	TRIG_FSM_STATUS	read- only	Show state of trigger slice FSM.

# 0x7610 PBS\_CLIENT5\_INT\_RT\_STS

**Type:** read-only

Clock: PBUS\_WRCLK Reset State: 0x00

Reset Name: PBS\_CORE\_PERPH\_RB

**Interrupt Real Time Status Bits** 

# PBS\_CLIENT5\_INT\_RT\_STS

Bits	Name	Type	Description
1	SEQ_ENDED_RT_STS	read- only	
0	SEQ_ERROR_RT_STS	read- only	

# 0x7611 PBS\_CLIENT5\_INT\_SET\_TYPE

Type: read-write Clock: PBUS\_WRCLK Reset State: 0x00

Reset Name: PBS\_CORE\_PERPH\_RB

0 =use level trigger interrupts, 1 =use edge trigger interrupts

## PBS\_CLIENT5\_INT\_SET\_TYPE

Bits	Name	Туре	Description
1	SEQ_ENDED_TYPE	read- write	
0	SEQ_ERROR_TYPE	read- write	

#### 0x7612 PBS\_CLIENT5\_INT\_POLARITY\_HIGH

Type: read-write Clock: PBUS\_WRCLK Reset State: 0x00

Reset Name: PBS\_CORE\_PERPH\_RB

1= Interrupt will trigger on a level high (rising edge) event, 0 = level high triggering is disabled

#### PBS\_CLIENT5\_INT\_POLARITY\_HIGH

Bits	Name	Туре	Description
1	SEQ_ENDED_HIGH	read- write	
0	SEQ_ERROR_HIGH	read- write	

# 0x7613 PBS\_CLIENT5\_INT\_POLARITY\_LOW

Type: read-write Clock: PBUS\_WRCLK Reset State: 0x00

Reset Name: PBS\_CORE\_PERPH\_RB

1' = Interrupt will trigger on a level low (falling edge) event, '0' = level low triggering is disabled

## PBS\_CLIENT5\_INT\_POLARITY\_LOW

Bits	Name	Туре	Description
1	SEQ_ENDED_LOW	read- write	
0	SEQ_ERROR_LOW	read- write	

## 0x7614 PBS\_CLIENT5\_INT\_LATCHED\_CLR

Type: write-only Clock: PBUS\_WRCLK Reset State: 0x00

**Reset Name:** PBS\_CORE\_PERPH\_RB

Writing a '1' to this interrupt will rearm the interrupt when an interrupt is pending. It clears the

internal sticky and sent bits

#### PBS\_CLIENT5\_INT\_LATCHED\_CLR

Bits	Name	Туре	Description
1	SEQ_ENDED_LATCHED_ CLR	write- only	
0	SEQ_ERROR_LATCHED _CLR	write- only	

## 0x7615 PBS\_CLIENT5\_INT\_EN\_SET

Type: read-write Clock: PBUS\_WRCLK

**Reset State:** 0x00

Reset Name: PBS\_CORE\_PERPH\_RB

Writing '0' to this register has no effect. Writing a '1' will enable the corresponding interrupt. Reading this register will readback enable status

PMIC\_SET\_MASK

#### PBS CLIENT5 INT EN SET

Bits	Name	Type	Description
1	SEQ_ENDED_EN_SET	read- write	2.
0	SEQ_ERROR_EN_SET	read- write	

## 0x7616 PBS CLIENT5 INT EN CLR

Type: read-write Clock: PBUS\_WRCLK Reset State: 0x00

**Reset Name:** PBS\_CORE\_PERPH\_RB

Writing '0' to this register has no effect. Writing a '1' will disable the corresponding interrupt.

Reading this register will readback enable status

PMIC\_CLR\_MASK=INT\_EN\_SET

#### PBS\_CLIENT5\_INT\_EN\_CLR

Bits	Name	Туре	Description
1	SEQ_ENDED_EN_CLR	read- write	

## PBS\_CLIENT5\_INT\_EN\_CLR (Continued)

Bits	Name	Type	Description
0	SEQ_ERROR_EN_CLR	read- write	

## 0x7618 PBS\_CLIENT5\_INT\_LATCHED\_STS

**Type:** read-only

Clock: PBUS\_WRCLK Reset State: 0x00

Reset Name: PBS\_CORE\_PERPH\_RB

Debug: Latched (Sticky) Interrupt. '1' indicates that the interrupt has triggered. Once the latched bit is set it can only be cleared by writing the clear bit.

#### PBS\_CLIENT5\_INT\_LATCHED\_STS

Bits	Name	Туре	Description
1	SEQ_ENDED_LATCHED_ STS	read- only	CONT
0	SEQ_ERROR_LATCHED _STS	read- only	

# 0x7619 PBS\_CLIENT5\_INT\_PENDING\_STS

Type: read-only

Clock: PBUS\_WRCLK Reset State: 0x00

Reset Name: PBS\_CORE\_PERPH\_RB

Debug: Pending is set if interrupt has been sent but not cleared.

## PBS\_CLIENT5\_INT\_PENDING\_STS

Bits	Name	Туре	Description
1	SEQ_ENDED_PENDING_ STS	read- only	
0	SEQ_ERROR_PENDING _STS	read- only	

## 0x761A PBS\_CLIENT5\_INT\_MID\_SEL

Type: read-write Clock: PBUS\_WRCLK Reset State: 0x00

**Reset Name:** PBS\_CORE\_PERPH\_RB

Selects the MID that will receive the interrupt

#### PBS\_CLIENT5\_INT\_MID\_SEL

Bits	Name	Туре	Description
1:0	INT_MID_SEL	read- write	

# 0x761B PBS\_CLIENT5\_INT\_PRIORITY

Type: read-write Clock: PBUS\_WRCLK Reset State: 0x00

Reset Name: PBS\_CORE\_PERPH\_RB

SR=0 A=1

#### PBS\_CLIENT5\_INT\_PRIORITY

Bits	Name	Туре	Description
0	INT_PRIORITY	read- write	

# 0x7640 PBS\_CLIENT5\_TRIG\_CFG

Type: read-write Clock: PBUS\_WRCLK Reset State: 0x00

Reset Name: PBS\_CORE\_PERPH\_RB

**Trigger Configuration** 

PMIC\_SYNC=pbs\_clk:pbs\_rb

#### PBS\_CLIENT5\_TRIG\_CFG

Bits	Name	Туре	Description
7	TRIGGER_RE_EN	read- write	1 = Enable Rising Edge Trigger 0 = Disable Falling Edge Trigger

### PBS\_CLIENT5\_TRIG\_CFG (Continued)

Bits	Name	Туре	Description
6	TRIGGER_FE_EN	read- write	1 = Enable Falling Edge Trigger 0 = Disable Falling Edge Trigger

# 0x7642 PBS\_CLIENT5\_TRIG\_CTL

**Type:** write-only **Clock:** PBUS\_WRCLK **Reset State:** 0x00

Reset Name: PBS\_CORE\_PERPH\_RB

#### PBS\_CLIENT5\_TRIG\_CTL

Bits	Name	Туре	Description
0	SW_TRIGGER	write- only	Writing 0x01 to this register will immediately create a trigger pulse.

#### 0x7646 PBS\_CLIENT5\_EN\_CTL

Type: read-write Clock: PBUS\_WRCLK Reset State: 0x00

Reset Name: PBS\_CORE\_PERPH\_RB

PMIC\_SYNC=pbs\_clk:pbs\_rb

#### PBS\_CLIENT5\_EN\_CTL

Bits	Name	Туре	Description
7	TRIGGER_EN	read- write	Must be set to 1 to enable all triggers in the peripheral

# 6.8 PBS\_CLIENT6\_PBS\_CLIENT

# 0x7704 PBS\_CLIENT6\_PERPH\_TYPE

**Type:** read-only

Clock: PBUS\_WRCLK Reset State: 0x16 Reset Name: N/A

Peripheral Type

#### PBS\_CLIENT6\_PERPH\_TYPE

Bits	Name	Туре	Description
7:0	TYPE	read- only	PBS Reset State: 0x16

#### 0x7705 PBS CLIENT6 PERPH SUBTYPE

**Type:** read-only

Clock: PBUS\_WRCLK Reset State: 0x08 Reset Name: N/A

Peripheral SubType

#### PBS\_CLIENT6\_PERPH\_SUBTYPE

Bits	Name	Type	Description
7:0	SUBTYPE	read- only	Client 6 Reset State: 0x08

#### 0x7708 PBS\_CLIENT6\_STATUS0

**Type:** read-only

Clock: PBUS\_WRCLK
Reset State: 0bXXXXX000

**Reset Name:** N/A

Status Registers

#### PBS\_CLIENT6\_STATUS0

Bits	Name	Type	Description
7	TRIG_EN_STATUS	read- only	Overall trigger-sequence enable state

#### PBS\_CLIENT6\_STATUS0 (Continued)

Bits	Name	Туре	Description
5:4	COMP_STATUS	read- only	These bits show the completion state of this client trigger-sequence pair.
			00 = In execution.
			01 = Normal completion
			10 = Error completion.
			11= Abort completion.
2:0	TRIG_FSM_STATUS	read- only	Show state of trigger slice FSM.

# 0x7710 PBS\_CLIENT6\_INT\_RT\_STS

**Type:** read-only

Clock: PBUS\_WRCLK Reset State: 0x00

Reset Name: PBS\_CORE\_PERPH\_RB

**Interrupt Real Time Status Bits** 

# PBS\_CLIENT6\_INT\_RT\_STS

Bits	Name	Type	Description
1	SEQ_ENDED_RT_STS	read- only	
0	SEQ_ERROR_RT_STS	read- only	

# 0x7711 PBS\_CLIENT6\_INT\_SET\_TYPE

Type: read-write Clock: PBUS\_WRCLK Reset State: 0x00

Reset Name: PBS\_CORE\_PERPH\_RB

0 =use level trigger interrupts, 1 =use edge trigger interrupts

#### PBS\_CLIENT6\_INT\_SET\_TYPE

Bits	Name	Type	Description
1	SEQ_ENDED_TYPE	read- write	
0	SEQ_ERROR_TYPE	read- write	

#### 0x7712 PBS\_CLIENT6\_INT\_POLARITY\_HIGH

Type: read-write Clock: PBUS\_WRCLK Reset State: 0x00

Reset Name: PBS\_CORE\_PERPH\_RB

1= Interrupt will trigger on a level high (rising edge) event, 0 = level high triggering is disabled

#### PBS\_CLIENT6\_INT\_POLARITY\_HIGH

Bits	Name	Туре	Description
1	SEQ_ENDED_HIGH	read- write	
0	SEQ_ERROR_HIGH	read- write	

# 0x7713 PBS\_CLIENT6\_INT\_POLARITY\_LOW

Type: read-write Clock: PBUS\_WRCLK Reset State: 0x00

Reset Name: PBS\_CORE\_PERPH\_RB

1' = Interrupt will trigger on a level low (falling edge) event, '0' = level low triggering is disabled

#### PBS\_CLIENT6\_INT\_POLARITY\_LOW

Bits	Name	Туре	Description
1	SEQ_ENDED_LOW	read- write	
0	SEQ_ERROR_LOW	read- write	

#### 0x7714 PBS\_CLIENT6\_INT\_LATCHED\_CLR

Type: write-only Clock: PBUS\_WRCLK Reset State: 0x00

**Reset Name:** PBS\_CORE\_PERPH\_RB

Writing a '1' to this interrupt will rearm the interrupt when an interrupt is pending. It clears the

internal sticky and sent bits

#### PBS\_CLIENT6\_INT\_LATCHED\_CLR

Bits	Name	Туре	Description
1	SEQ_ENDED_LATCHED_ CLR	write- only	
0	SEQ_ERROR_LATCHED _CLR	write- only	

#### 0x7715 PBS\_CLIENT6\_INT\_EN\_SET

Type: read-write Clock: PBUS\_WRCLK

**Reset State:** 0x00

Reset Name: PBS\_CORE\_PERPH\_RB

Writing '0' to this register has no effect. Writing a '1' will enable the corresponding interrupt. Reading this register will readback enable status

PMIC\_SET\_MASK

#### PBS CLIENT6 INT EN SET

Bits	Name	Type	Description
1	SEQ_ENDED_EN_SET	read- write	2.
0	SEQ_ERROR_EN_SET	read- write	

#### 0x7716 PBS CLIENT6 INT EN CLR

Type: read-write Clock: PBUS\_WRCLK Reset State: 0x00

**Reset Name:** PBS\_CORE\_PERPH\_RB

Writing '0' to this register has no effect. Writing a '1' will disable the corresponding interrupt. Reading this register will readback enable status

Reading this register will readback chable su

PMIC\_CLR\_MASK=INT\_EN\_SET

#### PBS\_CLIENT6\_INT\_EN\_CLR

Bits	Name	Type	Description
1	SEQ_ENDED_EN_CLR	read- write	

### PBS\_CLIENT6\_INT\_EN\_CLR (Continued)

Bits	Name	Type	Description
0	SEQ_ERROR_EN_CLR	read- write	

#### 0x7718 PBS\_CLIENT6\_INT\_LATCHED\_STS

**Type:** read-only

Clock: PBUS\_WRCLK Reset State: 0x00

Reset Name: PBS\_CORE\_PERPH\_RB

Debug: Latched (Sticky) Interrupt. '1' indicates that the interrupt has triggered. Once the latched bit is set it can only be cleared by writing the clear bit.

#### PBS\_CLIENT6\_INT\_LATCHED\_STS

Bits	Name	Туре	Description
1	SEQ_ENDED_LATCHED_ STS	read- only	CON
0	SEQ_ERROR_LATCHED _STS	read- only	

# 0x7719 PBS\_CLIENT6\_INT\_PENDING\_STS

Type: read-only

Clock: PBUS\_WRCLK Reset State: 0x00

Reset Name: PBS\_CORE\_PERPH\_RB

Debug: Pending is set if interrupt has been sent but not cleared.

#### PBS\_CLIENT6\_INT\_PENDING\_STS

Bits	Name	Туре	Description
1	SEQ_ENDED_PENDING_ STS	read- only	
0	SEQ_ERROR_PENDING _STS	read- only	

### 0x771A PBS\_CLIENT6\_INT\_MID\_SEL

Type: read-write Clock: PBUS\_WRCLK Reset State: 0x00

**Reset Name:** PBS\_CORE\_PERPH\_RB

Selects the MID that will receive the interrupt

#### PBS\_CLIENT6\_INT\_MID\_SEL

Bits	Name	Туре	Description
1:0	INT_MID_SEL	read- write	

# 0x771B PBS\_CLIENT6\_INT\_PRIORITY

Type: read-write Clock: PBUS\_WRCLK Reset State: 0x00

Reset Name: PBS\_CORE\_PERPH\_RB

SR=0 A=1

#### PBS\_CLIENT6\_INT\_PRIORITY

Bits	Name	Туре	Description
0	INT_PRIORITY	read- write	

#### 0x7740 PBS\_CLIENT6\_TRIG\_CFG

Type: read-write Clock: PBUS\_WRCLK Reset State: 0x00

Reset Name: PBS\_CORE\_PERPH\_RB

**Trigger Configuration** 

PMIC\_SYNC=pbs\_clk:pbs\_rb

#### PBS\_CLIENT6\_TRIG\_CFG

Bits	Name	Туре	Description
7	TRIGGER_RE_EN	read- write	1 = Enable Rising Edge Trigger 0 = Disable Falling Edge Trigger

### PBS\_CLIENT6\_TRIG\_CFG (Continued)

Bits	Name	Туре	Description
6	TRIGGER_FE_EN	read- write	1 = Enable Falling Edge Trigger 0 = Disable Falling Edge Trigger

# 0x7742 PBS\_CLIENT6\_TRIG\_CTL

Type: write-only Clock: PBUS\_WRCLK Reset State: 0x00

Reset Name: PBS\_CORE\_PERPH\_RB

#### PBS\_CLIENT6\_TRIG\_CTL

Bits	Name	Туре	Description
0	SW_TRIGGER	write- only	Writing 0x01 to this register will immediately create a trigger pulse.

#### 0x7746 PBS\_CLIENT6\_EN\_CTL

Type: read-write Clock: PBUS\_WRCLK Reset State: 0x00

Reset Name: PBS\_CORE\_PERPH\_RB

PMIC\_SYNC=pbs\_clk:pbs\_rb

#### PBS\_CLIENT6\_EN\_CTL

Bits	Name	Туре	Description
7	TRIGGER_EN	read- write	Must be set to 1 to enable all triggers in the peripheral

# 6.9 PBS\_CLIENT7\_PBS\_CLIENT

# 0x7804 PBS\_CLIENT7\_PERPH\_TYPE

**Type:** read-only

Clock: PBUS\_WRCLK Reset State: 0x16 Reset Name: N/A

Peripheral Type

#### PBS\_CLIENT7\_PERPH\_TYPE

Bits	Name	Туре	Description
7:0	TYPE	read- only	PBS Reset State: 0x16

#### 0x7805 PBS CLIENT7 PERPH SUBTYPE

**Type:** read-only

Clock: PBUS\_WRCLK Reset State: 0x08 Reset Name: N/A

Peripheral SubType

#### PBS\_CLIENT7\_PERPH\_SUBTYPE

Bits	Name	Туре	Description
7:0	SUBTYPE	read- only	Client 7 Reset State: 0x08

#### 0x7808 PBS\_CLIENT7\_STATUS0

**Type:** read-only

Clock: PBUS\_WRCLK
Reset State: 0bXXXXX000

**Reset Name:** N/A

Status Registers

#### PBS\_CLIENT7\_STATUS0

Bits	Name	Type	Description
7	TRIG_EN_STATUS	read- only	Overall trigger-sequence enable state

#### PBS\_CLIENT7\_STATUS0 (Continued)

Bits	Name	Туре	Description
5:4	COMP_STATUS	read- only	These bits show the completion state of this client trigger-sequence pair.
			00 = In execution.
			01 = Normal completion
			10 = Error completion.
			11= Abort completion.
2:0	TRIG_FSM_STATUS	read- only	Show state of trigger slice FSM.

# 0x7810 PBS\_CLIENT7\_INT\_RT\_STS

Type: read-only Clock: PBUS\_WRCLK Reset State: 0x00

Reset Name: PBS\_CORE\_PERPH\_RB

**Interrupt Real Time Status Bits** 

# PBS\_CLIENT7\_INT\_RT\_STS

Bits	Name	Туре	Description
1	SEQ_ENDED_RT_STS	read- only	
0	SEQ_ERROR_RT_STS	read- only	000

# 0x7811 PBS\_CLIENT7\_INT\_SET\_TYPE

Type: read-write Clock: PBUS\_WRCLK Reset State: 0x00

Reset Name: PBS\_CORE\_PERPH\_RB

0 =use level trigger interrupts, 1 =use edge trigger interrupts

#### PBS\_CLIENT7\_INT\_SET\_TYPE

Bits	Name	Туре	Description
1	SEQ_ENDED_TYPE	read- write	
0	SEQ_ERROR_TYPE	read- write	

#### 0x7812 PBS CLIENT7 INT POLARITY HIGH

Type: read-write Clock: PBUS\_WRCLK Reset State: 0x00

Reset Name: PBS\_CORE\_PERPH\_RB

1= Interrupt will trigger on a level high (rising edge) event, 0 = level high triggering is disabled

#### PBS\_CLIENT7\_INT\_POLARITY\_HIGH

Bits	Name	Туре	Description
1	SEQ_ENDED_HIGH	read- write	
0	SEQ_ERROR_HIGH	read- write	

# 0x7813 PBS\_CLIENT7\_INT\_POLARITY\_LOW

Type: read-write Clock: PBUS\_WRCLK Reset State: 0x00

Reset Name: PBS\_CORE\_PERPH\_RB

1' = Interrupt will trigger on a level low (falling edge) event, '0' = level low triggering is disabled

### PBS\_CLIENT7\_INT\_POLARITY\_LOW

Bits	Name	Туре	Description
1	SEQ_ENDED_LOW	read- write	
0	SEQ_ERROR_LOW	read- write	

### 0x7814 PBS\_CLIENT7\_INT\_LATCHED\_CLR

Type: write-only Clock: PBUS\_WRCLK Reset State: 0x00

**Reset Name:** PBS\_CORE\_PERPH\_RB

Writing a '1' to this interrupt will rearm the interrupt when an interrupt is pending. It clears the

internal sticky and sent bits

#### PBS\_CLIENT7\_INT\_LATCHED\_CLR

Bits	Name	Туре	Description
1	SEQ_ENDED_LATCHED_ CLR	write- only	
0	SEQ_ERROR_LATCHED _CLR	write- only	

#### 0x7815 PBS\_CLIENT7\_INT\_EN\_SET

Type: read-write Clock: PBUS\_WRCLK Reset State: 0x00

Reset Name: PBS\_CORE\_PERPH\_RB

Writing '0' to this register has no effect. Writing a '1' will enable the corresponding interrupt.

Reading this register will readback enable status

PMIC\_SET\_MASK

#### PBS CLIENT7 INT EN SET

Bits	Name	Type	Description
1	SEQ_ENDED_EN_SET	read- write	130.
0	SEQ_ERROR_EN_SET	read- write	00

#### 0x7816 PBS CLIENT7 INT EN CLR

Type: read-write Clock: PBUS\_WRCLK Reset State: 0x00

**Reset Name:** PBS\_CORE\_PERPH\_RB

Writing '0' to this register has no effect. Writing a '1' will disable the corresponding interrupt.

Reading this register will readback enable status

PMIC\_CLR\_MASK=INT\_EN\_SET

# PBS\_CLIENT7\_INT\_EN\_CLR

Bits	Name	Туре	Description
1	SEQ_ENDED_EN_CLR	read- write	

### PBS\_CLIENT7\_INT\_EN\_CLR (Continued)

Bits	Name	Type	Description
0	SEQ_ERROR_EN_CLR	read- write	

#### 0x7818 PBS\_CLIENT7\_INT\_LATCHED\_STS

**Type:** read-only

Clock: PBUS\_WRCLK Reset State: 0x00

Reset Name: PBS\_CORE\_PERPH\_RB

Debug: Latched (Sticky) Interrupt. '1' indicates that the interrupt has triggered. Once the latched bit is set it can only be cleared by writing the clear bit.

#### PBS\_CLIENT7\_INT\_LATCHED\_STS

Bits	Name	Туре	Description
1	SEQ_ENDED_LATCHED_ STS	read- only	CONT
0	SEQ_ERROR_LATCHED _STS	read- only	

# 0x7819 PBS\_CLIENT7\_INT\_PENDING\_STS

Type: read-only

Clock: PBUS\_WRCLK Reset State: 0x00

Reset Name: PBS\_CORE\_PERPH\_RB

Debug: Pending is set if interrupt has been sent but not cleared.

#### PBS\_CLIENT7\_INT\_PENDING\_STS

Bits	Name	Туре	Description
1	SEQ_ENDED_PENDING_ STS	read- only	
0	SEQ_ERROR_PENDING _STS	read- only	

### 0x781A PBS\_CLIENT7\_INT\_MID\_SEL

Type: read-write Clock: PBUS\_WRCLK Reset State: 0x00

**Reset Name:** PBS\_CORE\_PERPH\_RB

Selects the MID that will receive the interrupt

#### PBS\_CLIENT7\_INT\_MID\_SEL

Bits	Name	Туре	Description
1:0	INT_MID_SEL	read- write	

# 0x781B PBS\_CLIENT7\_INT\_PRIORITY

Type: read-write Clock: PBUS\_WRCLK Reset State: 0x00

Reset Name: PBS\_CORE\_PERPH\_RB

SR=0 A=1

#### PBS\_CLIENT7\_INT\_PRIORITY

Bits	Name	Туре	Description
0	INT_PRIORITY	read- write	

# 0x7840 PBS\_CLIENT7\_TRIG\_CFG

Type: read-write Clock: PBUS\_WRCLK Reset State: 0x00

Reset Name: PBS CORE PERPH RB

**Trigger Configuration** 

PMIC\_SYNC=pbs\_clk:pbs\_rb

#### PBS\_CLIENT7\_TRIG\_CFG

Bits	Name	Туре	Description
7	TRIGGER_RE_EN	read- write	1 = Enable Rising Edge Trigger 0 = Disable Falling Edge Trigger

### PBS\_CLIENT7\_TRIG\_CFG (Continued)

Bits	Name	Туре	Description
6	TRIGGER_FE_EN	read- write	1 = Enable Falling Edge Trigger 0 = Disable Falling Edge Trigger

# 0x7842 PBS\_CLIENT7\_TRIG\_CTL

Type: write-only Clock: PBUS\_WRCLK Reset State: 0x00

Reset Name: PBS\_CORE\_PERPH\_RB

#### PBS\_CLIENT7\_TRIG\_CTL

Bits	Name	Туре	Description
0	SW_TRIGGER	write- only	Writing 0x01 to this register will immediately create a trigger pulse.

#### 0x7846 PBS\_CLIENT7\_EN\_CTL

Type: read-write Clock: PBUS\_WRCLK Reset State: 0x00

Reset Name: PBS\_CORE\_PERPH\_RB

PMIC\_SYNC=pbs\_clk:pbs\_rb

#### PBS\_CLIENT7\_EN\_CTL

Bits	Name	Туре	Description
7	TRIGGER_EN	read- write	Must be set to 1 to enable all triggers in the peripheral



# 7 MPPn

# 7.1 Overview

Table 7-1 Blocks

	Name	
MPP1		
MPP2	13. 10	
MPP3	~2. co	
MPP4	× 0.0	

# 7.2 MPP1\_MPP

# 0xA004 MPP1\_PERPH\_TYPE

**Type:** read-only

Clock: PBUS\_WRCLK Reset State: 0x11 Reset Name: N/A

Peripheral Type

#### MPP1\_PERPH\_TYPE

Bits	Name	Туре	Description
7:0	TYPE	read- only	MPP

# 0xA005 MPP1\_PERPH\_SUBTYPE

**Type:** read-only

Clock: PBUS\_WRCLK Reset State: 0x05 Reset Name: N/A

Peripheral SubType

#### MPP1\_PERPH\_SUBTYPE

Bits	Name	Туре	Description
7:0	SUBTYPE	read- only	MPP

# 0xA008 MPP1\_STATUS1

**Type:** read-only

Clock: PBUS\_WRCLK Reset State: Undefined Reset Name: N/A

Status Registers

#### MPP1\_STATUS1

Bit	S Name	Type	Description
7	MPP_OK	read- only	0 = GPIO is disabled 1 = GPIO is enabled

#### MPP1\_STATUS1 (Continued)

Bits	Name	Туре	Description
0	MPP_VAL	read- only	Value read by the input buffer, if enabled

#### 0xA010 MPP1\_INT\_RT\_STS

**Type:** read-only

Clock: PBUS\_WRCLK Reset State: 0x00 Reset Name: N/A

**Interrupt Real Time Status Bits** 

#### MPP1\_INT\_RT\_STS

Bits	Name	Туре	Description
0	MPP_IN_STS	read- only	3.10.00

#### 0xA011 MPP1\_INT\_SET\_TYPE

Type: read-write

Clock: PBUS\_WRCLK Reset State: 0x00

Reset Name: PERPH\_RB

0 =use level trigger interrupts, 1 =use edge trigger interrupts

#### MPP1\_INT\_SET\_TYPE

Bits	Name	Туре	Description
0	MPP_IN_TYPE	read- write	

#### 0xA012 MPP1\_INT\_POLARITY\_HIGH

**Type:** read-write **Clock:** PBUS\_WRCLK **Reset State:** 0x00

Reset Name: PERPH RB

1= Interrupt will trigger on a level high (rising edge) event, 0 = level high triggering is disabled

#### MPP1\_INT\_POLARITY\_HIGH

Bi	ts	Name	Type	Description
0	)	MPP_IN_HIGH	read- write	

# 0xA013 MPP1\_INT\_POLARITY\_LOW

Type: read-write Clock: PBUS\_WRCLK Reset State: 0x00 Reset Name: PERPH RB

1' = Interrupt will trigger on a level low (falling edge) event, '0' = level low triggering is disabled

#### MPP1\_INT\_POLARITY\_LOW

Bits	Name	Туре	Description
0	MPP_IN_LOW	read- write	CONT

### 0xA014 MPP1\_INT\_LATCHED\_CLR

Type: write-only Clock: PBUS\_WRCLK Reset State: 0x00 Reset Name: PERPH\_RB

Writing a '1' to this interrupt will rearm the interrupt when an interrupt is pending. It clears the internal sticky and sent bits

#### MPP1\_INT\_LATCHED\_CLR

Bits	Name	Туре	Description
0	MPP_IN_LATCHED_CLR	write- only	

#### 0xA015 MPP1\_INT\_EN\_SET

Type: read-write Clock: PBUS\_WRCLK Reset State: 0x00 Reset Name: PERPH\_RB

Writing '0' to this register has no effect. Writing a '1' will enable the corresponding interrupt. Reading this register will readback enable status

#### PMIC\_SET\_MASK

#### MPP1\_INT\_EN\_SET

Bits	Name	Туре	Description
0	MPP_IN_EN_SET	read- write	

#### 0xA016 MPP1\_INT\_EN\_CLR

Type: read-write
Clock: PBUS\_WRCLK
Reset State: 0x00

Reset Name: PERPH\_RB

Writing '0' to this register has no effect. Writing a '1' will disable the corresponding interrupt. Reading this register will readback enable status

PMIC\_CLR\_MASK=INT\_EN\_SET

#### MPP1\_INT\_EN\_CLR

E	Bits	Name	Туре	Description
	0	MPP_IN_EN_CLR	read- write	120.1

### 0xA018 MPP1\_INT\_LATCHED\_STS

Type: read-only Clock: PBUS\_WRCLK Reset State: 0x00 Reset Name: N/A

Latched (Sticky) Interrupt. '1' indicates that the interrupt has triggered. Once the latched bit is set it can only be cleared by writing the clear bit.

#### MPP1\_INT\_LATCHED\_STS

Bits	Name	Туре	Description
0	MPP_IN_LATCHED_STS	read- only	

#### 0xA019 MPP1\_INT\_PENDING\_STS

**Type:** read-only

Clock: PBUS\_WRCLK Reset State: 0x00 Reset Name: N/A

Debug: Pending is set if interrupt has been sent but not cleared.

#### MPP1\_INT\_PENDING\_STS

Bits	Name	Туре	Description
0	MPP_IN_PENDING_STS	read- only	

#### 0xA01A MPP1 INT MID SEL

Type: read-write

Clock: PBUS\_WRCLK Reset State: 0x00

Reset Name: PERPH\_RB

Selects the MID that will receive the interrupt

#### MPP1\_INT\_MID\_SEL

Bits	Name	Туре	Description
1:0	INT_MID_SEL	read- write	

# 0xA01B MPP1\_INT\_PRIORITY

Type: read-write Clock: PBUS\_WRCLK Reset State: 0x00

Reset Name: PERPH RB

SR=0 A=1

#### **MPP1 INT PRIORITY**

Bits	Name	Type	Description
0	INT_PRIORITY	read- write	

# 0xA040 MPP1\_MODE\_CTL

Type: read-write
Clock: PBUS\_WRCLK
Reset State: 0x00
Perset Name: PERPH PH

Reset Name: PERPH\_RB

MPP Mode allows you to switch from one mode to another mode in a single register write.

#### MPP1\_MODE\_CTL

Bits	Name	Туре	Description
6:4	MODE	read- write	MPP Type: 0: Digital Input 1: Digital Output 2: Digital Input and Digital Output 3: Bidirectional Logic 4: Analog Input 5: Analog Output 6: Current Sink 7: Reserved
	2013	36.26 R	7. Neserveu

# MPP1\_MODE\_CTL (Continued)

Bits	Name	Type	Description
	N_AND_SOURCE_SEL	read-write	When configured as a digital output Source select:  0000 = 0 0001 = 1 0010 = paired MPP 0011 = inverted paired MPP 0100 = Reserved 0101 = Reserved 0101 = Reserved 0111 = Reserved 1000 = DTEST1 1001 = inverted DTEST2 1011 = inverted DTEST3 1101 = inverted DTEST3 1101 = inverted DTEST4 1111 = inverted DTEST4  Enable control when configured as Bidirectional, AIN, AOUT, or Current Sink. MPP is enable whenever the selected condition is true. 0000 = 0 (mpp is always disabled) 0001 = 1 (mpp is always Enabled) 0010 = paired MPP 0011 = inverted paired MPP 0100 = Reserved 0111 = Reserved 0111 = Reserved 0111 = Reserved 1000 = DTEST1 1001 = inverted DTEST1 1001 = inverted DTEST1 1001 = inverted DTEST2 1101 = inverted DTEST3

# 0xA041 MPP1\_DIG\_VIN\_CTL

Type: read-write Clock: PBUS\_WRCLK Reset State: 0x00 Reset Name: PERPH\_RB

#### MPP1\_DIG\_VIN\_CTL

Bits	Name	Туре	Description
2:0	VOLTAGE_SEL	read-	Digital I/O mode:
		write	000 = VIN0 (refer to the objective spec.)
			001 = VIN1 (refer to the objective spec.)
			010 = VIN2 (refer to the objective spec.)*
			011 = VIN3 (refer to the objective spec.)
			100 = VIN4 (refer to the objective spec.)*
			101 = VIN5 (refer to the objective spec.)
			110 = VIN6 (refer to the objective spec.)
			111 = VIN7 (refer to the objective spec.)
1		l	

#### 0xA042 MPP1\_DIG\_PULL\_CTL

Type: read-write Clock: PBUS\_WRCLK Reset State: 0x00 Reset Name: PERPH\_RB

#### MPP1\_DIG\_PULL\_CTL

Bits	Name	Туре	Description
2:0	PULLUP_SEL	read- write	Pullup Resistor Control in bidirectional mode only. 00: 0.6k? ** 01: 10 k? 10: 30 k? 11: Open (infinite resistance) *

### 0xA046 MPP1\_EN\_CTL

Type: read-write
Clock: PBUS\_WRCLK
Reset State: 0x00
Percet Name: PERPH P

**Reset Name:** PERPH\_RB

#### MPP1\_EN\_CTL

Bits	Name	Туре	Description
7	PERPH_EN	read- write	MPP Master enable 0 = puts MPP_PAD at high Z and disables the block 1 = MPP is enabled

#### 0xA048 MPP1\_ANA\_OUT\_CTL

Type: read-write Clock: PBUS\_WRCLK Reset State: 0x00 Reset Name: PERPH\_RB

#### MPP1\_ANA\_OUT\_CTL

Bits	Name	Туре	Description
2:0	REF_SEL	read- write	Analog Output Control 0: Output = vref_1V25 = REF_BYP pin, typically 1.25 Volts

#### 0xA04A MPP1\_ANA\_IN\_CTL

Type: read-write Clock: PBUS\_WRCLK Reset State: 0x00 Reset Name: PERPH\_RB

#### MPP1\_ANA\_IN\_CTL

Bits	Name	Туре	Description
2:0	ROUTE_SEL	read-	AMUX Channel Control
	0,0	write	0: Route to AMUX5
	3.	0-1	1: Route to AMUX6
	0,000	.00	2: Route to AMUX7
	1, 90		3: Route to AMUX8
	2000		4 to 7: Reserved

# 0xA04C MPP1\_SINK\_CTL

Type: read-write Clock: PBUS\_WRCLK Reset State: 0x00

Reset Name: PERPH\_RB

# MPP1\_SINK\_CTL

Bits	Name	Туре	Description
2:0	CURRENT_SEL	read-	Current Sink Output Control
		write	0: Output = 5 mA
			1: Output = 10 mA
			2: Output = 15 mA
			3: Output = 20 mA
			4: Output = 25 mA
			5: Output = 30 mA
			6: Output = 35 mA
			7: Output = 40 mA

# 7.3 MPP2\_MPP

# 0xA104 MPP2\_PERPH\_TYPE

**Type:** read-only

Clock: PBUS\_WRCLK Reset State: 0x11 Reset Name: N/A

Peripheral Type

#### MPP2\_PERPH\_TYPE

Bits	Name	Туре	Description
7:0	TYPE	read- only	MPP

# 0xA105 MPP2\_PERPH\_SUBTYPE

**Type:** read-only

Clock: PBUS\_WRCLK Reset State: 0x03 Reset Name: N/A

Peripheral SubType

#### MPP2\_PERPH\_SUBTYPE

Bits	Name	Туре	Description
7:0	SUBTYPE	read- only	MPP

# 0xA108 MPP2\_STATUS1

**Type:** read-only

Clock: PBUS\_WRCLK Reset State: Undefined Reset Name: N/A

Status Registers

#### MPP2\_STATUS1

Bits	Name	Type	Description
7	MPP_OK	read- only	0 = GPIO is disabled 1 = GPIO is enabled

#### MPP2\_STATUS1 (Continued)

Bits	Name	Туре	Description
0	MPP_VAL	read- only	Value read by the input buffer, if enabled

#### 0xA110 MPP2\_INT\_RT\_STS

**Type:** read-only

Clock: PBUS\_WRCLK Reset State: 0x00 Reset Name: N/A

**Interrupt Real Time Status Bits** 

#### MPP2\_INT\_RT\_STS

Bits	Name	Туре	Description
0	MPP_IN_STS	read- only	0: 10 · 0/1

# 0xA111 MPP2\_INT\_SET\_TYPE

Type: read-write

Clock: PBUS\_WRCLK
Reset State: 0x00

Reset Name: PERPH\_RB

0 =use level trigger interrupts, 1 =use edge trigger interrupts

#### MPP2\_INT\_SET\_TYPE

Bits	Name	Туре	Description
0	MPP_IN_TYPE	read- write	

# 0xA112 MPP2\_INT\_POLARITY\_HIGH

Type: read-write Clock: PBUS\_WRCLK Reset State: 0x00

Reset Name: PERPH RB

1= Interrupt will trigger on a level high (rising edge) event, 0 = level high triggering is disabled

#### MPP2\_INT\_POLARITY\_HIGH

Bits	Name	Type	Description
0	MPP_IN_HIGH	read- write	

# 0xA113 MPP2\_INT\_POLARITY\_LOW

Type: read-write Clock: PBUS\_WRCLK Reset State: 0x00 Reset Name: PERPH RB

1' = Interrupt will trigger on a level low (falling edge) event, '0' = level low triggering is disabled

#### MPP2\_INT\_POLARITY\_LOW

Bits	Name	Туре	Description
0	MPP_IN_LOW	read- write	CONT

#### 0xA114 MPP2\_INT\_LATCHED\_CLR

Type: write-only Clock: PBUS\_WRCLK Reset State: 0x00 Reset Name: PERPH\_RB

Writing a '1' to this interrupt will rearm the interrupt when an interrupt is pending. It clears the internal sticky and sent bits

#### MPP2\_INT\_LATCHED\_CLR

Bits	Name	Туре	Description
0	MPP_IN_LATCHED_CLR	write- only	

#### 0xA115 MPP2\_INT\_EN\_SET

Type: read-write Clock: PBUS\_WRCLK Reset State: 0x00 Reset Name: PERPH\_RB

Writing '0' to this register has no effect. Writing a '1' will enable the corresponding interrupt. Reading this register will readback enable status

#### PMIC\_SET\_MASK

#### MPP2\_INT\_EN\_SET

Bits	Name	Туре	Description
0	MPP_IN_EN_SET	read- write	

#### 0xA116 MPP2\_INT\_EN\_CLR

Type: read-write Clock: PBUS\_WRCLK Reset State: 0x00

Reset Name: PERPH\_RB

Writing '0' to this register has no effect. Writing a '1' will disable the corresponding interrupt. Reading this register will readback enable status

PMIC\_CLR\_MASK=INT\_EN\_SET

#### MPP2\_INT\_EN\_CLR

Bits	Name	Туре	Description
0	MPP_IN_EN_CLR	read- write	120.1

### 0xA118 MPP2\_INT\_LATCHED\_STS

Type: read-only Clock: PBUS\_WRCLK Reset State: 0x00 Reset Name: N/A

Latched (Sticky) Interrupt. '1' indicates that the interrupt has triggered. Once the latched bit is set it can only be cleared by writing the clear bit.

#### MPP2\_INT\_LATCHED\_STS

Bits	Name	Туре	Description
0	MPP_IN_LATCHED_STS	read- only	

#### 0xA119 MPP2\_INT\_PENDING\_STS

**Type:** read-only

Clock: PBUS\_WRCLK Reset State: 0x00 Reset Name: N/A

Debug: Pending is set if interrupt has been sent but not cleared.

#### MPP2\_INT\_PENDING\_STS

Bits	Name	Туре	Description
0	MPP_IN_PENDING_STS	read- only	

# 0xA11A MPP2\_INT\_MID\_SEL

Type: read-write Clock: PBUS\_WRCLK Reset State: 0x00

Reset Name: PERPH RB

Selects the MID that will receive the interrupt

#### MPP2\_INT\_MID\_SEL

Bits	Name	Туре	Description
1:0	INT_MID_SEL	read- write	

# 0xA11B MPP2\_INT\_PRIORITY

Type: read-write Clock: PBUS\_WRCLK Reset State: 0x00

Reset Name: PERPH RB

SR=0 A=1

#### MPP2 INT PRIORITY

Bits	Name	Type	Description
0	INT_PRIORITY	read- write	

# 0xA140 MPP2\_MODE\_CTL

Type: read-write Clock: PBUS\_WRCLK Reset State: 0x00 Reset Name: PERPH\_RB

MPP Mode allows you to switch from one mode to another mode in a single register write.

#### MPP2\_MODE\_CTL

Bits	Name	Туре	Description
6:4	MODE	read-	MPP Type:
		write	0: Digital Input
			1: Digital Output
			2: Digital Input and Digital Output
			3: Bidirectional Logic
			4: Analog Input
			5: Analog Output
			6: Current Sink
			7: Reserved

# MPP2\_MODE\_CTL (Continued)

Bits	Name	Туре	Description
3:0	EN_AND_SOURCE_SEL	read-	When configured as a digital output Source select:
		write	0000 = 0
			0001 = 1
			0010 = paired MPP
			0011 = inverted paired MPP
			0100 = Reserved
			0101 = Reserved
			0110 = Reserved
			0111 = Reserved
			1000 = DTEST1
			1001 = inverted DTEST1
			1010 = DTEST2
			1011 = inverted DTEST2
			1100 = DTEST3
			1101 = inverted DTEST3
			1110 = DTEST4
			1111 = inverted DTEST4
		, O3	Enable control when configured as Bidirectional, AIN, AOUT, or Current Sink. MPP is enable whenever the selected condition is true.
	00		0000 = 0 (mpp is always disabled)
			0001 = 1 (mpp is always Enabled)
	000	0 (	0010 = paired MPP
	3.	0-1	0011 = inverted paired MPP
	-0,, 110	' Qo.	0100 = Reserved
	V .000		0101 = Reserved
		) "	0110 = Reserved
			0111 = Reserved
			1000 = DTEST1
			1001 = inverted DTEST1
			1010 = DTEST2
			1011 = inverted DTEST2
			1100 = DTEST3
			1101 = inverted DTEST3
			1110 = DTEST4

# 0xA141 MPP2\_DIG\_VIN\_CTL

Type: read-write Clock: PBUS\_WRCLK Reset State: 0x00 Reset Name: PERPH\_RB

#### MPP2\_DIG\_VIN\_CTL

Bits	Name	Туре	Description
2:0	VOLTAGE_SEL	read- write	Digital I/O mode:  000 = VIN0 (refer to the objective spec.)  001 = VIN1 (refer to the objective spec.)  010 = VIN2 (refer to the objective spec.)*  011 = VIN3 (refer to the objective spec.)  100 = VIN4 (refer to the objective spec.)*  101 = VIN5 (refer to the objective spec.)
			110 = VIN6 (refer to the objective spec.) 111 = VIN7 (refer to the objective spec.)

# 0xA142 MPP2\_DIG\_PULL\_CTL

Type: read-write Clock: PBUS\_WRCLK Reset State: 0x00 Reset Name: PERPH\_RB

#### MPP2\_DIG\_PULL\_CTL

Bits	Name	Туре	Description
2:0	PULLUP_SEL	read- write	Pullup Resistor Control in bidirectional mode only. 00: 0.6k? ** 01: 10 k? 10: 30 k? 11: Open (infinite resistance) *

# 0xA146 MPP2\_EN\_CTL

Type: read-write Clock: PBUS\_WRCLK Reset State: 0x00 Reset Name: PERPH\_RB

#### MPP2\_EN\_CTL

Bits	Name	Туре	Description
7	PERPH_EN	read- write	MPP Master enable 0 = puts MPP_PAD at high Z and disables the block 1 = MPP is enabled

#### 0xA148 MPP2\_ANA\_OUT\_CTL

Type: read-write Clock: PBUS\_WRCLK Reset State: 0x00 Reset Name: PERPH\_RB

#### MPP2\_ANA\_OUT\_CTL

Bits	Name	Туре	Description
2:0	REF_SEL	read- write	Analog Output Control 0: Output = vref_1V25 = REF_BYP pin, typically 1.25 Volts

# 0xA14A MPP2\_ANA\_IN\_CTL

Type: read-write Clock: PBUS\_WRCLK Reset State: 0x00 Reset Name: PERPH\_RB

#### MPP2\_ANA\_IN\_CTL

Bits	Name	Туре	Description
2:0	ROUTE_SEL	read-	AMUX Channel Control
	0,0	write	0: Route to AMUX5
	3.	0-1	1: Route to AMUX6
	0,000	.00	2: Route to AMUX7
	1, 90		3: Route to AMUX8
	2000		4 to 7: Reserved

# 0xA14C MPP2\_SINK\_CTL

Type: read-write Clock: PBUS\_WRCLK Reset State: 0x00

**Reset Name:** PERPH\_RB

# MPP2\_SINK\_CTL

Bits	Name	Туре	Description
2:0	CURRENT_SEL	read-	Current Sink Output Control
		write	0: Output = 5 mA
			1: Output = 10 mA
			2: Output = 15 mA
			3: Output = 20 mA
			4: Output = 25 mA
			5: Output = 30 mA
			6: Output = 35 mA
			7: Output = 40 mA

# 7.4 MPP3\_MPP

# 0xA204 MPP3\_PERPH\_TYPE

**Type:** read-only

Clock: PBUS\_WRCLK Reset State: 0x11 Reset Name: N/A

Peripheral Type

#### MPP3\_PERPH\_TYPE

Bits	Name	Туре	Description
7:0	TYPE	read- only	MPP

# 0xA205 MPP3\_PERPH\_SUBTYPE

**Type:** read-only

Clock: PBUS\_WRCLK Reset State: 0x05 Reset Name: N/A

Peripheral SubType

#### MPP3\_PERPH\_SUBTYPE

Bits	Name	Туре	Description
7:0	SUBTYPE	read- only	MPP

# 0xA208 MPP3\_STATUS1

**Type:** read-only

Clock: PBUS\_WRCLK
Reset State: Undefined
Reset Name: N/A

Status Registers

#### MPP3\_STATUS1

Bit	S Name	Type	Description
7	MPP_OK	read- only	0 = GPIO is disabled 1 = GPIO is enabled

#### MPP3\_STATUS1 (Continued)

Bits	Name	Туре	Description
0	MPP_VAL	read- only	Value read by the input buffer, if enabled

### 0xA210 MPP3\_INT\_RT\_STS

**Type:** read-only

Clock: PBUS\_WRCLK Reset State: 0x00 Reset Name: N/A

**Interrupt Real Time Status Bits** 

### MPP3\_INT\_RT\_STS

Bits	Name	Туре	Description
0	MPP_IN_STS	read- only	3.10.00

## 0xA211 MPP3\_INT\_SET\_TYPE

Type: read-write

Clock: PBUS\_WRCLK Reset State: 0x00

Reset Name: PERPH\_RB

0 =use level trigger interrupts, 1 =use edge trigger interrupts

### MPP3\_INT\_SET\_TYPE

Bits	Name	Туре	Description
0	MPP_IN_TYPE	read- write	

### 0xA212 MPP3\_INT\_POLARITY\_HIGH

Type: read-write Clock: PBUS\_WRCLK Reset State: 0x00

Reset Name: PERPH RB

1= Interrupt will trigger on a level high (rising edge) event, 0 = level high triggering is disabled

#### MPP3\_INT\_POLARITY\_HIGH

Bits	Name	Туре	Description
0	MPP_IN_HIGH	read- write	

# 0xA213 MPP3\_INT\_POLARITY\_LOW

Type: read-write Clock: PBUS\_WRCLK Reset State: 0x00 Reset Name: PERPH RB

1' = Interrupt will trigger on a level low (falling edge) event, '0' = level low triggering is disabled

#### MPP3\_INT\_POLARITY\_LOW

Bits	Name	Туре	Description
0	MPP_IN_LOW	read- write	CON

#### 0xA214 MPP3\_INT\_LATCHED\_CLR

Type: write-only Clock: PBUS\_WRCLK Reset State: 0x00 Reset Name: PERPH\_RB

Writing a '1' to this interrupt will rearm the interrupt when an interrupt is pending. It clears the internal sticky and sent bits

#### MPP3\_INT\_LATCHED\_CLR

Bits	Name	Туре	Description
0	MPP_IN_LATCHED_CLR	write- only	

## 0xA215 MPP3\_INT\_EN\_SET

Type: read-write Clock: PBUS\_WRCLK Reset State: 0x00 Reset Name: PERPH\_RB

Writing '0' to this register has no effect. Writing a '1' will enable the corresponding interrupt. Reading this register will readback enable status

#### PMIC\_SET\_MASK

#### MPP3\_INT\_EN\_SET

Bits	Name	Туре	Description
0	MPP_IN_EN_SET	read- write	

### 0xA216 MPP3\_INT\_EN\_CLR

Type: read-write Clock: PBUS\_WRCLK Reset State: 0x00

Reset Name: PERPH\_RB

Writing '0' to this register has no effect. Writing a '1' will disable the corresponding interrupt. Reading this register will readback enable status

PMIC\_CLR\_MASK=INT\_EN\_SET

#### MPP3\_INT\_EN\_CLR

Bits	Name	Туре	Description
0	MPP_IN_EN_CLR	read- write	120.1

## 0xA218 MPP3\_INT\_LATCHED\_STS

Type: read-only Clock: PBUS\_WRCLK Reset State: 0x00 Reset Name: N/A

Latched (Sticky) Interrupt. '1' indicates that the interrupt has triggered. Once the latched bit is set it can only be cleared by writing the clear bit.

### MPP3\_INT\_LATCHED\_STS

Bits	Name	Туре	Description
0	MPP_IN_LATCHED_STS	read- only	

## 0xA219 MPP3\_INT\_PENDING\_STS

**Type:** read-only

Clock: PBUS\_WRCLK Reset State: 0x00 Reset Name: N/A

Debug: Pending is set if interrupt has been sent but not cleared.

#### MPP3\_INT\_PENDING\_STS

Bits	Name	Туре	Description
0	MPP_IN_PENDING_STS	read- only	

# 0xA21A MPP3\_INT\_MID\_SEL

Type: read-write Clock: PBUS\_WRCLK

**Reset State:** 0x00

Reset Name: PERPH\_RB

Selects the MID that will receive the interrupt

#### MPP3\_INT\_MID\_SEL

Bits	Name	Туре	Description
1:0	INT_MID_SEL	read- write	

# 0xA21B MPP3\_INT\_PRIORITY

Type: read-write Clock: PBUS\_WRCLK Reset State: 0x00

Reset Name: PERPH RB

SR=0 A=1

#### MPP3 INT PRIORITY

Bits	Name	Type	Description
0	INT_PRIORITY	read- write	

# 0xA240 MPP3\_MODE\_CTL

Type: read-write
Clock: PBUS\_WRCLK
Reset State: 0x00

Reset Name: PERPH\_RB

MPP Mode allows you to switch from one mode to another mode in a single register write.

# MPP3\_MODE\_CTL

Bits	Name	Туре	Description
6:4	MODE	read-	MPP Type:
		write	0: Digital Input
			1: Digital Output
			2: Digital Input and Digital Output
			3: Bidirectional Logic
			4: Analog Input
			5: Analog Output
			6: Current Sink
			7: Reserved

# MPP3\_MODE\_CTL (Continued)

Bits	Name	Туре	Description
3:0	EN_AND_SOURCE_SEL	read-	When configured as a digital output Source select:
		write	0000 = 0
			0001 = 1
			0010 = paired MPP
			0011 = inverted paired MPP
			0100 = Reserved
			0101 = Reserved
			0110 = Reserved
			0111 = Reserved
			1000 = DTEST1
			1001 = inverted DTEST1
			1010 = DTEST2
			1011 = inverted DTEST2
			1100 = DTEST3
			1101 = inverted DTEST3
			1110 = DTEST4
			1111 = inverted DTEST4
		, O3	Enable control when configured as Bidirectional, AIN, AOUT, or Current Sink. MPP is enable whenever the selected condition is true.
	00		0000 = 0 (mpp is always disabled)
			0001 = 1 (mpp is always Enabled)
	000	0 (	0010 = paired MPP
	3.	0-1	0011 = inverted paired MPP
	-0,, 110	' Qo.	0100 = Reserved
	V .000		0101 = Reserved
		) "	0110 = Reserved
			0111 = Reserved
			1000 = DTEST1
			1001 = inverted DTEST1
			1010 = DTEST2
			1011 = inverted DTEST2
			1100 = DTEST3
			1101 = inverted DTEST3
			1110 = DTEST4

# 0xA241 MPP3\_DIG\_VIN\_CTL

Type: read-write Clock: PBUS\_WRCLK Reset State: 0x00 Reset Name: PERPH\_RB

# MPP3\_DIG\_VIN\_CTL

Bits	Name	Туре	Description
2:0	VOLTAGE_SEL	read- write	Digital I/O mode:  000 = VIN0 (refer to the objective spec.)  001 = VIN1 (refer to the objective spec.)  010 = VIN2 (refer to the objective spec.)*  011 = VIN3 (refer to the objective spec.)  100 = VIN4 (refer to the objective spec.)*  101 = VIN5 (refer to the objective spec.)
			110 = VIN6 (refer to the objective spec.) 111 = VIN7 (refer to the objective spec.)

# 0xA242 MPP3\_DIG\_PULL\_CTL

Type: read-write Clock: PBUS\_WRCLK Reset State: 0x00 Reset Name: PERPH\_RB

#### MPP3\_DIG\_PULL\_CTL

Bits	Name	Туре	Description
2:0	PULLUP_SEL	read- write	Pullup Resistor Control in bidirectional mode only. 00: 0.6k? ** 01: 10 k? 10: 30 k? 11: Open (infinite resistance) *

## 0xA246 MPP3\_EN\_CTL

Type: read-write Clock: PBUS\_WRCLK Reset State: 0x00 Reset Name: PERPH\_RB

# MPP3\_EN\_CTL

Bits	Name	Туре	Description
7	PERPH_EN	read- write	MPP Master enable 0 = puts MPP_PAD at high Z and disables the block 1 = MPP is enabled

## 0xA248 MPP3\_ANA\_OUT\_CTL

Type: read-write Clock: PBUS\_WRCLK Reset State: 0x00 Reset Name: PERPH\_RB

# MPP3\_ANA\_OUT\_CTL

Bits	Name	Туре	Description
2:0	REF_SEL	read- write	Analog Output Control 0: Output = vref_1V25 = REF_BYP pin, typically 1.25 Volts

# 0xA24A MPP3\_ANA\_IN\_CTL

Type: read-write Clock: PBUS\_WRCLK Reset State: 0x00 Reset Name: PERPH\_RB

### MPP3\_ANA\_IN\_CTL

Bits	Name	Type	Description
2:0	ROUTE_SEL	read-	AMUX Channel Control
	3.	write	0: Route to AMUX5
	0/10/10/	. 00.	1: Route to AMUX6
	7 69		2: Route to AMUX7
	1000	) *	3: Route to AMUX8
	6		4 to 7: Reserved

# 0xA24C MPP3\_SINK\_CTL

**Type:** read-write **Clock:** PBUS\_WRCLK **Reset State:** 0x00

Reset Name: PERPH\_RB

# MPP3\_SINK\_CTL

Bits	Name	Туре	Description
2:0	CURRENT_SEL	read-	Current Sink Output Control
		write	0: Output = 5 mA
			1: Output = 10 mA
			2: Output = 15 mA
			3: Output = 20 mA
			4: Output = 25 mA
			5: Output = 30 mA
			6: Output = 35 mA
			7: Output = 40 mA

# 7.5 MPP4\_MPP

# 0xA304 MPP4\_PERPH\_TYPE

**Type:** read-only

Clock: PBUS\_WRCLK Reset State: 0x11 Reset Name: N/A

Peripheral Type

#### MPP4 PERPH TYPE

Bits	Name	Туре	Description
7:0	TYPE	read- only	MPP

# 0xA305 MPP4\_PERPH\_SUBTYPE

**Type:** read-only

Clock: PBUS\_WRCLK Reset State: 0x03 Reset Name: N/A

Peripheral SubType

#### MPP4\_PERPH\_SUBTYPE

Bits	Name	Туре	Description
7:0	SUBTYPE	read- only	MPP

# 0xA308 MPP4\_STATUS1

**Type:** read-only

Clock: PBUS\_WRCLK
Reset State: Undefined
Reset Name: N/A

Status Registers

#### MPP4\_STATUS1

Bits	Name	Type	Description
7	MPP_OK	read- only	0 = GPIO is disabled 1 = GPIO is enabled

#### MPP4\_STATUS1 (Continued)

Bits	Name	Туре	Description
0	MPP_VAL	read- only	Value read by the input buffer, if enabled

### 0xA310 MPP4\_INT\_RT\_STS

**Type:** read-only

Clock: PBUS\_WRCLK Reset State: 0x00 Reset Name: N/A

**Interrupt Real Time Status Bits** 

### MPP4\_INT\_RT\_STS

Bits	Name	Туре	Description
0	MPP_IN_STS	read- only	3:15:00

#### 0xA311 MPP4\_INT\_SET\_TYPE

Type: read-write

Clock: PBUS\_WRCLK
Reset State: 0x00

Reset Name: PERPH\_RB

0 =use level trigger interrupts, 1 =use edge trigger interrupts

### MPP4\_INT\_SET\_TYPE

Bits	Name	Туре	Description
0	MPP_IN_TYPE	read- write	

### 0xA312 MPP4\_INT\_POLARITY\_HIGH

Type: read-write Clock: PBUS\_WRCLK Reset State: 0x00

Reset Name: PERPH RB

1= Interrupt will trigger on a level high (rising edge) event, 0 = level high triggering is disabled

#### MPP4\_INT\_POLARITY\_HIGH

Bi	ts	Name	Type	Description
0	)	MPP_IN_HIGH	read- write	

# 0xA313 MPP4\_INT\_POLARITY\_LOW

Type: read-write Clock: PBUS\_WRCLK Reset State: 0x00 Reset Name: PERPH RB

1' = Interrupt will trigger on a level low (falling edge) event, '0' = level low triggering is disabled

#### MPP4\_INT\_POLARITY\_LOW

Bits	Name	Туре	Description
0	MPP_IN_LOW	read- write	CON

# 0xA314 MPP4\_INT\_LATCHED\_CLR

Type: write-only Clock: PBUS\_WRCLK Reset State: 0x00 Reset Name: PERPH\_RB

Writing a '1' to this interrupt will rearm the interrupt when an interrupt is pending. It clears the internal sticky and sent bits

#### MPP4\_INT\_LATCHED\_CLR

Bits	Name	Туре	Description
0	MPP_IN_LATCHED_CLR	write- only	

## 0xA315 MPP4\_INT\_EN\_SET

Type: read-write Clock: PBUS\_WRCLK Reset State: 0x00 Reset Name: PERPH\_RB

Writing '0' to this register has no effect. Writing a '1' will enable the corresponding interrupt. Reading this register will readback enable status

## PMIC\_SET\_MASK

#### MPP4\_INT\_EN\_SET

Bits	Name	Туре	Description
0	MPP_IN_EN_SET	read- write	

### 0xA316 MPP4\_INT\_EN\_CLR

Type: read-write Clock: PBUS\_WRCLK Reset State: 0x00

Reset Name: PERPH\_RB

Writing '0' to this register has no effect. Writing a '1' will disable the corresponding interrupt. Reading this register will readback enable status

PMIC\_CLR\_MASK=INT\_EN\_SET

#### MPP4\_INT\_EN\_CLR

Bits	Name	Туре	Description
0	MPP_IN_EN_CLR	read- write	20.1

## 0xA318 MPP4\_INT\_LATCHED\_STS

Type: read-only Clock: PBUS\_WRCLK Reset State: 0x00 Reset Name: N/A

Latched (Sticky) Interrupt. '1' indicates that the interrupt has triggered. Once the latched bit is set it can only be cleared by writing the clear bit.

### MPP4\_INT\_LATCHED\_STS

Bits	Name	Туре	Description
0	MPP_IN_LATCHED_STS	read- only	

# 0xA319 MPP4\_INT\_PENDING\_STS

**Type:** read-only

Clock: PBUS\_WRCLK Reset State: 0x00 Reset Name: N/A

Debug: Pending is set if interrupt has been sent but not cleared.

#### MPP4\_INT\_PENDING\_STS

Bits	Name	Туре	Description
0	MPP_IN_PENDING_STS	read- only	

# 0xA31A MPP4\_INT\_MID\_SEL

Type: read-write Clock: PBUS\_WRCLK Reset State: 0x00

Reset Name: PERPH RB

Selects the MID that will receive the interrupt

### MPP4\_INT\_MID\_SEL

Bits	Name	Туре	Description
1:0	INT_MID_SEL	read- write	

# 0xA31B MPP4\_INT\_PRIORITY

Type: read-write Clock: PBUS\_WRCLK Reset State: 0x00

Reset Name: PERPH RB

SR=0 A=1

#### MPP4\_INT\_PRIORITY

Bits	Name	Туре	Description
0	INT_PRIORITY	read- write	

# 0xA340 MPP4\_MODE\_CTL

Type: read-write Clock: PBUS\_WRCLK Reset State: 0x00 Reset Name: PERPH\_RB

MPP Mode allows you to switch from one mode to another mode in a single register write.

#### MPP4\_MODE\_CTL

Bits	Name	Туре	Description	
6:4	MODE	read- write	MPP Type: 0: Digital Input 1: Digital Output 2: Digital Input and Digital Output 3: Bidirectional Logic 4: Analog Input 5: Analog Output 6: Current Sink 7: Reserved	
	2013		7: Reserved	

# MPP4\_MODE\_CTL (Continued)

Bits	Name	Туре	Description
3:0	EN_AND_SOURCE_SEL	readwrite	When configured as a digital output Source select:  0000 = 0  0001 = 1  0010 = paired MPP  0011 = inverted paired MPP  0100 = Reserved  0101 = Reserved  0111 = Reserved  1010 = DTEST1  1001 = inverted DTEST1  1010 = DTEST3  1101 = DTEST4  1111 = inverted DTEST4  Enable control when configured as Bidirectional, AIN, AOUT, or Current Sink. MPP is enable whenever the selected condition is true.  0000 = 0 (mpp is always disabled)  0001 = 1 (mpp is always Enabled)  0010 = paired MPP  0011 = inverted DTEST1  1001 = Reserved  0111 = Reserved  0111 = Reserved  0111 = Reserved  1010 = DTEST1  1001 = inverted DTEST1  1001 = inverted DTEST1  1001 = inverted DTEST1  1001 = inverted DTEST2  1011 = inverted DTEST2  1011 = inverted DTEST3  1101 = DTEST3  1101 = inverted DTEST3  1101 = DTEST4  1111 = inverted DTEST4

# 0xA341 MPP4\_DIG\_VIN\_CTL

Type: read-write Clock: PBUS\_WRCLK Reset State: 0x00 Reset Name: PERPH\_RB

### MPP4\_DIG\_VIN\_CTL

Bits	Name	Туре	Description
2:0	VOLTAGE_SEL	read- write	Digital I/O mode:  000 = VIN0 (refer to the objective spec.)  001 = VIN1 (refer to the objective spec.)  010 = VIN2 (refer to the objective spec.)*  011 = VIN3 (refer to the objective spec.)  100 = VIN4 (refer to the objective spec.)*  101 = VIN5 (refer to the objective spec.)
			110 = VIN6 (refer to the objective spec.) 111 = VIN7 (refer to the objective spec.)

# 0xA342 MPP4\_DIG\_PULL\_CTL

Type: read-write Clock: PBUS\_WRCLK Reset State: 0x00 Reset Name: PERPH\_RB

#### MPP4\_DIG\_PULL\_CTL

Bits	Name	Туре	Description
2:0	PULLUP_SEL	read- write	Pullup Resistor Control in bidirectional mode only. 00: 0.6k? ** 01: 10 k? 10: 30 k? 11: Open (infinite resistance) *

### 0xA346 MPP4\_EN\_CTL

Type: read-write
Clock: PBUS\_WRCLK
Reset State: 0x00
Percet Name: PERPH P

**Reset Name:** PERPH\_RB

### MPP4\_EN\_CTL

Bits	Name	Туре	Description
7	PERPH_EN	read- write	MPP Master enable 0 = puts MPP_PAD at high Z and disables the block 1 = MPP is enabled

## 0xA348 MPP4\_ANA\_OUT\_CTL

Type: read-write Clock: PBUS\_WRCLK Reset State: 0x00 Reset Name: PERPH\_RB

### MPP4\_ANA\_OUT\_CTL

Bits	Name	Туре	Description
2:0	REF_SEL	read- write	Analog Output Control 0: Output = vref_1V25 = REF_BYP pin, typically 1.25 Volts

# 0xA34A MPP4\_ANA\_IN\_CTL

Type: read-write Clock: PBUS\_WRCLK Reset State: 0x00 Reset Name: PERPH\_RB

### MPP4\_ANA\_IN\_CTL

Bits	Name	Type	Description
2:0	ROUTE_SEL	read-	AMUX Channel Control
	3.	write	0: Route to AMUX5
	0,000	. 000	1: Route to AMUX6
	7 60		2: Route to AMUX7
		) *	3: Route to AMUX8
			4 to 7: Reserved

# 0xA34C MPP4\_SINK\_CTL

**Type:** read-write **Clock:** PBUS\_WRCLK **Reset State:** 0x00

Reset Name: PERPH\_RB

# MPP4\_SINK\_CTL

Bits	Name	Туре	Description
2:0	CURRENT_SEL	read-	Current Sink Output Control
		write	0: Output = 5 mA
			1: Output = 10 mA
			2: Output = 15 mA
			3: Output = 20 mA
			4: Output = 25 mA
			5: Output = 30 mA
			6: Output = 35 mA
			7: Output = 40 mA



# 8 Sn

# 8.1 Overview

Table 8-1 Blocks

	Name
S1_CTRL	
S1_PS	1,3, 10
S1_FREQ	23. CO
S2_CTRL	1, 10.
S2_PS	6 76 70
S2_FREQ	
S3_CTRL	0, 0, 10
S3_PS	N.5. '6., '8.,
S3_FREQ	Jo 70, 10
S4_CTRL	
S4_PS	
S4_FREQ	
S5_CTRL	
S5_PS	
S5_FREQ	
S6_CTRL	
S6_PS	
S6_FREQ	
S7_CTRL	
S7_PS	
S7_FREQ	
S8_CTRL	
S8_PS	
S8_FREQ	

# 8.2 S1\_CTRL\_HFBUCK2\_CTRL

# 0x11404 S1\_CTRL\_PERPH\_TYPE

**Type:** read-only

Clock: PBUS\_WRCLK Reset State: 0x03 Reset Name: N/A

Peripheral Type

#### S1\_CTRL\_PERPH\_TYPE

Bits	Name	Туре	Description
7:0	TYPE	read- only	SMPS

# 0x11405 S1\_CTRL\_PERPH\_SUBTYPE

**Type:** read-only

Clock: PBUS\_WRCLK Reset State: 0x08 Reset Name: N/A

Peripheral SubType

#### S1\_CTRL\_PERPH\_SUBTYPE

Bits	Name	Туре	Description
7:0	SUBTYPE	read- only	2A HF BUCK

# 0x11408 S1\_CTRL\_STATUS

**Type:** read-only

Clock: PBUS\_WRCLK Reset State: Undefined Reset Name: N/A

Status Registers

### S1\_CTRL\_STATUS

Bits	Name	Туре	Description
7	VREG_OK	read- only	0 = VREG output voltage is below VREG_OK threshold 1 = VREG output voltage is above VREG_OK threshold

### S1\_CTRL\_STATUS (Continued)

Bits	Name	Туре	Description
5	ILS	read- only	Illegal Limit Stop. This is triggered when UL_Voltage < LL_Voltage
4	UL_VOLTAGE	read- only	Last voltage set was above or equal to UL_Voltage
3	LL_VOLTAGE	read- only	Last voltage set was below or equal to LL_Voltage
2	PS_TRUE	read- only	0 = buck is not pulse skipping 1 = buck is pulse skipping
1	NPM_TRUE	read- only	1 = VREG_OK and BUCK is in NPM
0	STEPPER_DONE	read- only	1 = stepper is done

# 0x11410 S1\_CTRL\_INT\_RT\_STS

Type: read-only Clock: PBUS WRCLK

Reset State: 0x00

**Reset Name:** PERPH\_RB

Interrupt Real Time Status Bits

### S1\_CTRL\_INT\_RT\_STS

Bits	Name	Туре	Description
1	LIMIT_ERR_INT	read- only	Last voltage set was above UL or below LL
0	VREG_OK_INT	read- only	Regulator has been successfully enabled

# 0x11411 S1\_CTRL\_INT\_SET\_TYPE

Type: read-write
Clock: PBUS\_WRCLK
Reset State: 0x00

**Reset Name:** PERPH\_RB

0 = use level trigger interrupts, 1 = use edge trigger interrupts

### S1\_CTRL\_INT\_SET\_TYPE

Bits	Name	Туре	Description
1	LIMIT_ERR_INT	read- write	
0	VREG_OK_INT	read- write	

# 0x11412 S1\_CTRL\_INT\_POLARITY\_HIGH

Type: read-write

Clock: PBUS\_WRCLK Reset State: 0x00

Reset Name: PERPH\_RB

1= Interrupt will trigger on a level high (rising edge) event, 0 = level high triggering is disabled

### S1\_CTRL\_INT\_POLARITY\_HIGH

Bits	Name	Туре	Description
1	LIMIT_ERR_INT	read- write	2/0
0	VREG_OK_INT	read- write	9.

### 0x11413 S1\_CTRL\_INT\_POLARITY\_LOW

Type: read-write

Clock: PBUS\_WRCLK Reset State: 0x00

Reset Name: PERPH\_RB

1' = Interrupt will trigger on a level low (falling edge) event, '0' = level low triggering is disabled

## S1\_CTRL\_INT\_POLARITY\_LOW

Bits	Name	Туре	Description
1	LIMIT_ERR_INT	read- write	
0	VREG_OK_INT	read- write	

#### 0x11414 S1 CTRL INT LATCHED CLR

**Type:** write-only Clock: PBUS\_WRCLK Reset State: 0x00 Reset Name: PERPH RB

Writing a '1' to this interrupt will rearm the interrupt when an interrupt is pending. It clears the

internal sticky and sent bits

#### S1\_CTRL\_INT\_LATCHED\_CLR

Bits	Name	Туре	Description
1	LIMIT_ERR_INT	write- only	
0	VREG_OK_INT	write- only	

#### 0x11415 S1\_CTRL\_INT\_EN\_SET

**Type:** read-write Clock: PBUS\_WRCLK Reset State: 0x00

Reset Name: PERPH RB

Writing '0' to this register has no effect. Writing a '1' will enable the corresponding interrupt.

Reading this register will readback enable status

PMIC SET MASK

#### S1\_CTRL\_INT\_EN\_SET

Bits	Name	Туре	Description
1	LIMIT_ERR_INT	read- write	
0	VREG_OK_INT	read- write	

#### 0x11416 S1\_CTRL\_INT\_EN\_CLR

**Type:** read-write Clock: PBUS\_WRCLK **Reset State:** 0x00

Reset Name: PERPH\_RB

Writing '0' to this register has no effect. Writing a '1' will disable the corresponding interrupt.

Reading this register will readback enable status

#### PMIC\_CLR\_MASK=INT\_EN\_SET

#### S1\_CTRL\_INT\_EN\_CLR

Bits	Name	Туре	Description
1	LIMIT_ERR_INT	read- write	
0	VREG_OK_INT	read- write	

# 0x11418 S1\_CTRL\_INT\_LATCHED\_STS

Type: read-only Clock: PBUS\_WRCLK Reset State: 0x00

Reset Name: PERPH\_RB

Debug: Latched (Sticky) Interrupt. '1' indicates that the interrupt has triggered. Once the latched bit is set it can only be cleared by writing the clear bit.

#### S1 CTRL INT LATCHED STS

Bits	Name	Type	Description
1	LIMIT_ERR_INT	read- only	2.
0	VREG_OK_INT	read- only	

### 0x11419 S1 CTRL INT PENDING STS

**Type:** read-only

Clock: PBUS\_WRCLK Reset State: 0x00

Reset Name: PERPH\_RB

Debug: Pending is set if interrupt has been sent but not cleared.

#### S1\_CTRL\_INT\_PENDING\_STS

Bits	Name	Туре	Description
1	LIMIT_ERR_INT	read- only	
0	VREG_OK_INT	read- only	

# 0x1141A S1\_CTRL\_INT\_MID\_SEL

Type: read-write Clock: PBUS\_WRCLK Reset State: 0x00 Reset Name: PERPH RB

Selects the MID that will receive the interrupt

### S1\_CTRL\_INT\_MID\_SEL

Bits	Name	Туре	Description
1:0	INT_MID_SEL	read- write	

# 0x1141B S1\_CTRL\_INT\_PRIORITY

Type: read-write Clock: PBUS\_WRCLK Reset State: 0x00 Reset Name: PERPH\_RB

### S1\_CTRL\_INT\_PRIORITY

Bits	Name	Туре	Description
0	INT_PRIORITY	read- write	SR=0 A=1

### 0x11440 S1 CTRL VOLTAGE CTL1

Type: read-write Clock: PBUS\_WRCLK Reset State: 0x00 Reset Name: PERPH\_RB

PMIC\_LATCHED\_WRITE=VOLTAGE\_CTL2

#### S1\_CTRL\_VOLTAGE\_CTL1

Bits	Name	Туре	Description
0	RANGE	read- write	0: 0.375 to 1.5625 V at steps of 12.5 mV (Vmin = 0.375 V, Vstep = 12.5 mV)
			1 : 1.550 to 3.1250 V at steps of 25.0 mV (Vmin = 1.550 V, Vstep = 25.0 mV)

# 0x11441 S1\_CTRL\_VOLTAGE\_CTL2

Type: read-write Clock: PBUS\_WRCLK Reset State: 0x2E Reset Name: PERPH\_RB

### S1\_CTRL\_VOLTAGE\_CTL2

Bits	Name	Туре	Description
6:0	V_SET	read- write	Voltage = Vmin + VSET*(Vstep)

# 0x11445 S1\_CTRL\_MODE\_CTL

Type: read-write Clock: PBUS\_WRCLK Reset State: 0x80

Reset Name: PERPH\_RB

**Define Buck Mode Transitions** 

### S1\_CTRL\_MODE\_CTL

Bits	Name	Туре	Description
7	PWM	read- write	Force PWM
6	AUTO_MODE	read- write	1=Automatically enter NPM based on current
4	FOLLOW_PMIC_AWAKE	read- write	NPM when PMIC_AWAKE (SLEEP_B) = '1'
3	FOLLOW_HWEN3	read- write	1' BUCK is in NPM when HWEN3 ='1', '0'= ignore HWEN3
2	FOLLOW_HWEN2	read- write	1' BUCK is in NPM when HWEN2 ='1', '0'= ignore HWEN2
1	FOLLOW_HWEN1	read- write	1' BUCK is in NPM when HWEN1 ='1', '0'= ignore HWEN1
0	FOLLOW_HWEN0	read- write	1' BUCK is in NPM when HWEN0 ='1', '0'= ignore HWEN0

#### 

Type: read-write Clock: PBUS\_WRCLK Reset State: 0x00

Reset Name: PERPH\_RB

# S1\_CTRL\_EN\_CTL

Bits	Name	Туре	Description
7	PERPH_EN	read- write	1' = Enable the BUCK, '0' = do not force BUCK on
3	FOLLOW_HWEN3	read- write	1' BUCK is enabled when HWEN3 ='1', '0'= ignore HWEN3
2	FOLLOW_HWEN2	read- write	1' BUCK is enabled when HWEN2 ='1', '0'= ignore HWEN2
1	FOLLOW_HWEN1	read- write	1' BUCK is enabled when HWEN1 ='1', '0'= ignore HWEN1
0	FOLLOW_HWEN0	read- write	1' BUCK is enabled when HWEN0 ='1', '0'= ignore HWEN0

# 0x11448 S1\_CTRL\_PD\_CTL

Type: read-write Clock: PBUS\_WRCLK Reset State: 0x80

Reset Name: PERPH\_RB

### S1\_CTRL\_PD\_CTL

Bits	Name	Туре	Description
7	PD_EN	read- write	1' = Enable the pulldown when the regulator is disabled, '0' = pulldown is always disabled. Preset by trim register

# 8.3 S1\_FREQ\_BCLK\_GEN\_CLK

# 0x11604 S1\_FREQ\_PERPH\_TYPE

**Type:** read-only

Clock: PBUS\_WRCLK Reset State: 0x1D Reset Name: N/A

Peripheral Type

#### S1\_FREQ\_PERPH\_TYPE

Bits	Name	Туре	Description
7:0	TYPE	read- only	BCLK GEN

# 0x11605 S1\_FREQ\_PERPH\_SUBTYPE

**Type:** read-only

Clock: PBUS\_WRCLK Reset State: 0x09 Reset Name: N/A

Peripheral SubType

#### S1\_FREQ\_PERPH\_SUBTYPE

Bits	Name	Туре	Description
7:0	SUBTYPE	read- only	BCLK GEN CLK

# 0x11646 S1\_FREQ\_CLK\_ENABLE

Type: read-write Clock: PBUS\_WRCLK Reset State: 0x01

Reset Name: PERPH\_RB

#### S1\_FREQ\_CLK\_ENABLE

Bits	Name	Туре	Description
7	EN_CLK_INT	read- write	0 = do not force the clock on 1 = enable the clock
0	FOLLOW_CLK_SX_REQ	read- write	0 = ignore smps_clk_req <x> 1 = clock is enabled when the clocks request is high smps_clk_req<x>='1'</x></x>

# 0x11650 S1\_FREQ\_CLK\_DIV

Type: read-write
Clock: PBUS\_WRCLK
Reset State: 0x05

**Reset Name:** PERPH\_RB

PMIC\_GANGED

### S1\_FREQ\_CLK\_DIV

Bits	Name	Туре	Description
3:0	CLK_DIV	read- write	clock_ frequency = 19.2MHz / (CLK_DIV + 1) FTS2 Buck supports 3.2, 4.8, 6.4 and 9.6 MHz HF2 Buck supports 1.6, 2.4, 2.74, 3.2, 3.8, 4.8, and 6.4 MHz CLK_DIV = 0 is not supported, it will generate 9.6 MHz

# 0x11651 S1\_FREQ\_CLK\_PHASE

Type: read-write Clock: PBUS\_WRCLK Reset State: 0x05 Reset Name: PERPH\_RB

### S1\_FREQ\_CLK\_PHASE

Bits	Name	Туре	Description
3:0	CLK_PHASE	read- write	Distributed clock phase select: clock phase delay = clock period * (CLK_PHASE / 16)

# 0x116C0 S1\_FREQ\_GANG\_CTL1

**Type:** read-write **Clock:** PBUS\_WRCLK **Reset State:** 0x00

Reset Name: PERPH\_RB

#### S1\_FREQ\_GANG\_CTL1

Bits	Name	Туре	Description
7:0	GANG_LEADER_PID	read- write	When GANG_EN (GANG_CTL2[7]) is set, this peripheral will write the same data that is written to the gang leader Peripheral ID. Reads to the gang leader Peripheral ID are ignored by this peripheral. Ganged peripherals must reside within the same Slave ID

# 0x116C1 S1\_FREQ\_GANG\_CTL2

Type: read-write Clock: PBUS\_WRCLK Reset State: 0x00 Reset Name: PERPH\_RB

# S1\_FREQ\_GANG\_CTL2

Bits	Name	Туре	Description
7	GANG_EN	read- write	0 = disable 1 = enable When enabled, this peripheral will write the same data that is written to the gang leader PID. Reads to the gang leader PID are ignored by this peripheral

# 8.4 S2\_CTRL\_FTS2\_CTRL

# 0x11704 S2\_CTRL\_PERPH\_TYPE

**Type:** read-only

Clock: PBUS\_WRCLK Reset State: 0x03 Reset Name: N/A

Peripheral Type

# **\$2\_CTRL\_PERPH\_TYPE**

Bits	Name	Туре	Description
7:0	TYPE	read- only	FTS2 Control Reset State: 0x03

# 0x11705 S2\_CTRL\_PERPH\_SUBTYPE

**Type:** read-only

Clock: PBUS\_WRCLK Reset State: 0x08 Reset Name: N/A

Peripheral SubType

#### S2\_CTRL\_PERPH\_SUBTYPE

Bits	Name	Туре	Description
7:0	SUBTYPE	read- only	

#### 

Type: read-only

Clock: PBUS\_WRCLK Reset State: Undefined Reset Name: N/A

Status Registers

#### S2\_CTRL\_STATUS\_1

Bits	Name	Туре	Description
7	VREG_OK_FLAG	read- only	Indicates that VREG_SNS has reached a value that is greater than or equal to the threshold of the comparator tasked for VREG_SNS monitoring

# S2\_CTRL\_STATUS\_1 (Continued)

Bits	Name	Туре	Description
6	VREG_FAULT_FLAG	read- only	Indicates a probable short circuit condition at VREG_SNS since VREG_SNS is below the VREG fault voltage level and the softstart ramp is done. Current limit foldback is in use.
1	NPM_FLAG	read- only	Indicates normal power mode is in use
0	STEPPER_DONE_FLAG	read- only	Softstart stepper and voltage stepper done

# 0x11709 S2\_CTRL\_STATUS\_2

**Type:** read-only

Clock: PBUS\_WRCLK
Reset State: Undefined
Reset Name: N/A

Status Registers

# S2\_CTRL\_STATUS\_2

Bits	Name	Туре	Description
4	ILS_FLAG	read- only	Either of the following:  => Both limit stops have been enabled, but the upper limit stop VSET_ULS has been programmed to a value below the lower limit stop VSET_LLS  => Both limit stops have been enabled, but the lower limit stop VSET_LLS has been programmed to a value above the upper limit stop VSET_ULS
3	ULS_FLAG	read- only	Indicates that the voltage setpoint has been programmed to a value that is greater than or equal to the upper limit stop VSET_ULS
2	LLS_FLAG	read- only	Indicates that the voltage setpoint has been programmed to a value that is less than or equal to the lower limit stop VSET_LLS
1	GPL_HI_FLAG	read- only	Indicates that the voltage setpoint has reached a value that is greater than or equal to the high general purpose limit VSET_GPL_HI
0	GPL_LO_FLAG	read- only	Indicates that the voltage setpoint has reached a value that is less than or equal to the low general purpose limit VSET_GPL_LO

## 0x11710 S2\_CTRL\_INT\_RT\_STS

**Type:** read-only

Clock: PBUS\_WRCLK
Reset State: Undefined
Reset Name: PERPH\_RB

**Interrupt Real Time Status Bits** 

### S2\_CTRL\_INT\_RT\_STS

Bits	Name	Туре	Description
2	VREG_FAULT_INT	read- only	
1	LIMIT_ERR_INT	read- only	
0	VREG_OK_INT	read- only	51

## 0x11711 S2\_CTRL\_INT\_SET\_TYPE

Type: read-write Clock: PBUS\_WRCLK Reset State: 0x00

Reset Name: PERPH\_RB

0 =use level trigger interrupts, 1 =use edge trigger interrupts

### **S2 CTRL INT SET TYPE**

Bits	Name	Туре	Description
2	VREG_FAULT_INT	read- write	
1	LIMIT_ERR_INT	read- write	
0	VREG_OK_INT	read- write	

### 0x11712 S2\_CTRL\_INT\_POLARITY\_HIGH

Type: read-write Clock: PBUS\_WRCLK Reset State: 0x00 Reset Name: PERPH\_RB

1= Interrupt will trigger on a level high (rising edge) event, 0 = level high triggering is disabled

### S2\_CTRL\_INT\_POLARITY\_HIGH

Bits	Name	Туре	Description
2	VREG_FAULT_INT	read- write	
1	LIMIT_ERR_INT	read- write	
0	VREG_OK_INT	read- write	

## 0x11713 S2\_CTRL\_INT\_POLARITY\_LOW

Type: read-write Clock: PBUS\_WRCLK Reset State: 0x00 Reset Name: PERPH\_RB

1' = Interrupt will trigger on a level low (falling edge) event, '0' = level low triggering is disabled

### S2\_CTRL\_INT\_POLARITY\_LOW

Bits	Name	Туре	Description
2	VREG_FAULT_INT	read- write	70.
1	LIMIT_ERR_INT	read- write	0,00
0	VREG_OK_INT	read- write	

### 0x11714 S2\_CTRL\_INT\_LATCHED\_CLR

Type: write-only Clock: PBUS\_WRCLK Reset State: 0x00 Reset Name: PERPH\_RB

Writing a '1' to this interrupt will rearm the interrupt when an interrupt is pending. It clears the

internal sticky and sent bits

### S2\_CTRL\_INT\_LATCHED\_CLR

Bits	Name	Туре	Description
2	VREG_FAULT_INT	write- only	

### S2\_CTRL\_INT\_LATCHED\_CLR (Continued)

Bits	Name	Туре	Description
1	LIMIT_ERR_INT	write- only	
0	VREG_OK_INT	write- only	

### 0x11715 S2\_CTRL\_INT\_EN\_SET

Type: read-write Clock: PBUS\_WRCLK Reset State: 0x00 Reset Name: PERPH\_RB

Writing '0' to this register has no effect. Writing a '1' will enable the corresponding interrupt. Reading this register will readback enable status

PMIC\_SET\_MASK

### S2\_CTRL\_INT\_EN\_SET

Bits	Name	Туре	Description
2	VREG_FAULT_INT	read- write	0.7
1	LIMIT_ERR_INT	read- write	
0	VREG_OK_INT	read- write	

## 0x11716 S2\_CTRL\_INT\_EN\_CLR

Type: read-write Clock: PBUS\_WRCLK Reset State: 0x00 Reset Name: PERPH RB

Writing '0' to this register has no effect. Writing a '1' will disable the corresponding interrupt. Reading this register will readback enable status

PMIC\_CLR\_MASK=INT\_EN\_SET

### S2\_CTRL\_INT\_EN\_CLR

Bits	Name	Туре	Description
2	VREG_FAULT_INT	read- write	

### S2\_CTRL\_INT\_EN\_CLR (Continued)

Bits	Name	Туре	Description
1	LIMIT_ERR_INT	read- write	
0	VREG_OK_INT	read- write	

## 0x11718 S2\_CTRL\_INT\_LATCHED\_STS

Type: read-only Clock: PBUS\_WRCLK Reset State: 0x00 Reset Name: PERPH\_RB

Debug: Latched (Sticky) Interrupt. '1' indicates that the interrupt has triggered. Once the latched bit is set it can only be cleared by writing the clear bit.

### S2\_CTRL\_INT\_LATCHED\_STS

Bits	Name	Туре	Description
2	VREG_FAULT_INT	read- only	This No
1	LIMIT_ERR_INT	read- only	720.
0	VREG_OK_INT	read- only	0,90

### 0x11719 S2\_CTRL\_INT\_PENDING\_STS

Type: read-only Clock: PBUS\_WRCLK Reset State: 0x00 Reset Name: PERPH RB

Debug: Pending is set if interrupt has been sent but not cleared.

### S2\_CTRL\_INT\_PENDING\_STS

Bits	Name	Туре	Description
2	VREG_FAULT_INT	read- only	
1	LIMIT_ERR_INT	read- only	
0	VREG_OK_INT	read- only	

#### 0x1171A S2\_CTRL\_INT\_MID\_SEL

**Type:** read-write Clock: PBUS\_WRCLK **Reset State:** 0x00 Reset Name: PERPH\_RB

Selects the MID that will receive the interrupt

### S2\_CTRL\_INT\_MID\_SEL

Bits	Name	Туре	Description
1:0	INT_MID_SEL	read- write	-

#### 0x1171B **S2 CTRL INT PRIORITY**

**Type:** read-write Clock: PBUS\_WRCLK Reset State: 0x00

Reset Name: PERPH\_RB

SR=0 A=1

#### S2\_CTRL\_INT\_PRIORITY

Bits	Name	Туре	Description
0	INT_PRIORITY	read- write	

#### 0x11740 S2\_CTRL\_VOLTAGE\_CTL1

**Type:** read-write Clock: PBUS WRCLK **Reset State:** 0x00 Reset Name: PERPH\_RB

PMIC\_GANGED

### S2\_CTRL\_VOLTAGE\_CTL1

Bits	Name	Туре	Description
0	MV_RANGE	read- write	0 = Use low voltage range as specified by VSET and PFM_VOFFSET
			1 = Use medium voltage range as specified by VSET and PFM_VOFFSET

## 0x11741 S2\_CTRL\_VOLTAGE\_CTL2

Type: read-write Clock: PBUS\_WRCLK Reset State: 0xB4 Reset Name: PERPH\_RB

PMIC\_GANGED

### S2\_CTRL\_VOLTAGE\_CTL2

Bits	Name	Туре	Description
7:0	VSET	read- write	Output voltage set point in PWM mode and in PFM mode if the PFM_VOFFSET_EN bit is not asserted
		S	For MV_RANGE = 0: VSET => 0.005V * m + 0.080V, where m = <7:0> For MV_RANGE = 1: VSET => 0.010V * m + 0.160V, where m = <7:0> If PFM_VOFFSET_EN is asserted and in PFM mode, add PFM_VOFFSET

## 0x11742 S2\_CTRL\_VSET\_VALID

Type: read-only Clock: PBUS\_WRCLK Reset State: Undefined Reset Name: PERPH\_RB

## S2\_CTRL\_VSET\_VALID

Bits	Name	Туре	Description
7:0	VSET_VALID	read- only	Readback the valid output voltage setpoint value

## 0x11744 S2\_CTRL\_VOLTAGE\_CTL3

Type: read-write Clock: PBUS\_WRCLK Reset State: 0x00

Reset Name: PERPH\_RB

## S2\_CTRL\_VOLTAGE\_CTL3

Bits	Name	Туре	Description
7	PFM_VOFFSET_EN	read- write	When in PFM mode  0 = Use VSET for output voltage set point  1 = Use VSET + PFM_VOFFSET for output voltage set point
1:0	PFM_VOFFSET	read- write	When in PFM mode and PFM_VOFFSET_EN is asserted, add a positive output voltage offset  For MV_RANGE = 0:  VOFFSET = 0.005V * 2 * m, where m = <1:0>  For MV_RANGE = 1:  VOFFSET = 0.010V * 2 * m, where m = <1:0>

## 0x11745 S2\_CTRL\_MODE\_CTL

Type: read-write
Clock: PBUS\_WRCLK
Reset State: 0xC0

Reset Name: PERPH\_RB

PMIC\_GANGED

### S2\_CTRL\_MODE\_CTL

Bits	Name	Type	Description
7	NPM	read- write	FTS NON-AUTO mode control 0 = Low power mode (LPM) unless AUTO_MODE is asserted 1 = Normal power mode (PWM)
6	AUTO_MODE	read- write	When asserted, FTS automatically enters and exits low power mode (PFM) based on load current qualifying triggers  0 = AUTO mode is disabled  1 = AUTO mode is enabled

#### 

Type: read-write Clock: PBUS\_WRCLK Reset State: 0x00 Reset Name: PERPH\_RB

Reset Maine. 1 Livi 11\_IND

### S2\_CTRL\_EN\_CTL

Bits Name Type	Description
write 0 = Off	ble control
write 0 = Off 1 = On	

#### 

Type: read-write Clock: PBUS\_WRCLK Reset State: 0x80 Reset Name: PERPH\_RB

### S2\_CTRL\_PD\_CTL

Bits	Name	Туре	Description
7	PD_EN	read- write	0 = Strong pulldown is always disabled 1 = Strong pulldown is enabled when the regulator is disabled
6	WEAK_PD_EN	read- write	0 = Weak pulldown is not enabled in OFF state 1 = Weak pulldown is enabled in OFF state
5	WEAK_PD_PFM	read- write	0 = Weak pulldown is not enabled in PFM mode 1 = Weak pulldown is enabled in PFM mode
4	WEAK_PD_PWM	read- write	0 = Weak pulldown is not enabled in PWM mode (and in HCPFM mode) 1 = Weak pulldown is enabled in PWM mode (and in HCPFM mode)

## 0x11754 S2\_CTRL\_PHASE\_CNT

Type: read-write Clock: PBUS\_WRCLK Reset State: 0x00

**Reset Name:** PERPH\_RB

### S2\_CTRL\_PHASE\_CNT

Bits	Name	Type	Description
1:0	PHASE_CNT	read- write	When MULTIPHASE_EN is asserted, the number of operating phases is  00 = Number of operating phases is 1  01 = Number of operating phases is 2  10 = Number of operating phases is 4  11 = Number of operating phases is 4

## 0x11760 S2\_CTRL\_SS\_CTL

Type: read-write Clock: PBUS\_WRCLK Reset State: 0x08

Reset Name: PERPH\_RB

PMIC\_GANGED

## S2\_CTRL\_SS\_CTL

Bits	Name	Туре	Description
4:3	SS_STEP	read- write	Softstart voltage step size 00 = SS voltage step of 1 * LSB of VPROG
		V.	01 = SS voltage step of 2 * LSB
	7/13 10.	28.	10 = SS voltage step of 4 * LSB
	1,000	10	11 = SS voltage step of 8 * LSB
2:0	SS_DELAY	read- write	Softstart delay between steps = $2 \land (m + 3) / Fsys$ , where $m = \langle 2:0 \rangle$ (Fsys = 19.2 MHz):
			000 = 8-clock cycles (417ns)
			001 = 16-clock cycles
			010 = 32-clock cycles
			011 = 64-clock cycles
			100 = 128-clock cycles (6.67us)
			101 = 256-clock cycles
			110 = 512-clock cycles
			111 = 1024-clock cycles (53.3us)

## 0x11761 S2\_CTRL\_VS\_CTL

Type: read-write
Clock: PBUS\_WRCLK
Reset State: 0x00
Paget Name: PERPLIA

Reset Name: PERPH\_RB

### S2\_CTRL\_VS\_CTL

Bits	Name	Type	Description
7	VS_EN	read-	Voltage stepping control
		write	0 = VS is disabled
			1 = VS is enabled
4:3	VS_STEP	read-	Voltage stepping voltage step size
		write	00 = VS voltage step of 1 * LSB of VPROG
			01 = VS voltage step of 2 * LSB
			10 = VS voltage step of 4 * LSB
			11 = VS voltage step of 8 * LSB
2:0	VS_DELAY	read-	Voltage stepping delay between steps = 2 ^ (m + 3) /
	wr	write	Fsys, where m = <2:0> (Assuming Fsys = 19.2 MHz):
			Desired default is 1.67us
			000 = 8-clock cycles (417ns)
			001 = 16-clock cycles
			010 = 32-clock cycles
			011 = 64-clock cycles
			100 = 128-clock cycles (6.67us)
			101 = 256-clock cycles
			110 = 512-clock cycles
		8	111 = 1024-clock cycles (53.3us)

# 0x1176A S2\_CTRL\_ULS\_VALID

Type: read-only Clock: PBUS\_WRCLK

Reset State: Undefined
Reset Name: PERPH\_RB

### S2\_CTRL\_ULS\_VALID

Bits	Name	Туре	Description
7:0	ULS_VALID	read- only	Readback the valid upper limit stop value

## 0x1176C S2\_CTRL\_LLS\_VALID

**Type:** read-only

Clock: PBUS\_WRCLK Reset State: Undefined Reset Name: PERPH\_RB

## S2\_CTRL\_LLS\_VALID

Bits	Name	Туре	Description
7:0	LLS_VALID	read- only	Readback the valid lower limit stop value



# 8.5 S2\_PS\_FTS2\_PS

## 0x11804 S2\_PS\_PERPH\_TYPE

**Type:** read-only

Clock: PBUS\_WRCLK Reset State: 0x1C Reset Name: N/A

Peripheral Type

### S2\_PS\_PERPH\_TYPE

Bits	Name	Туре	Description
7:0	TYPE	read- only	FTS2 Power Stage Reset State: 0x1C

### 0x11805 S2\_PS\_PERPH\_SUBTYPE

**Type:** read-only

Clock: PBUS\_WRCLK Reset State: 0x08 Reset Name: N/A

Peripheral SubType

### S2\_PS\_PERPH\_SUBTYPE

Bits	Name	Type	Description
7:0	SUBTYPE	read- only	

## 0x11840 S2\_PS\_VOLTAGE\_CTL1

Type: read-write
Clock: PBUS\_WRCLK
Reset State: 0x00

Reset Name: PERPH\_RB

### S2\_PS\_VOLTAGE\_CTL1

Bits	Name	Туре	Description
0	MV_RANGE	read- write	0 = Use low voltage range as specified by VSET and PFM_VOFFSET 1 = Use medium voltage range as specified by VSET and PFM_VOFFSET

## 0x11841 S2\_PS\_VOLTAGE\_CTL2

Type: read-write Clock: PBUS\_WRCLK Reset State: 0xB4 Reset Name: PERPH\_RB

PMIC\_GANGED

### S2\_PS\_VOLTAGE\_CTL2

Bits	Name	Type	Description
7:0	VSET	read- write	Output voltage set point in PWM mode and in PFM mode if the PFM_VOFFSET_EN bit is not asserted
		80.	For MV_RANGE = 0:
			VSET => 0.005V * m + 0.080V, where $m = <7:0>$
	V, 2.	.0	For MV_RANGE = 1:
	20.		VSET => 0.010V * m + 0.160V, where m = <7:0>
	Mar	69	If PFM_VOFFSET_EN is asserted and in PFM mode, add PFM_VOFFSET

#### 

Type: read-write Clock: PBUS\_WRCLK Reset State: 0x00 Reset Name: PERPH\_RB

PMIC\_GANGED, PMIC\_SYNC=clk\_19p2:phase\_cnt\_rb

## S2\_PS\_PHASE\_CNT

Bits	Name	Туре	Description
1:0	PHASE_CNT	read- write	When MULTIPHASE_EN is asserted, the number of operating phases is  00 = Number of operating phases is 1  01 = Number of operating phases is 2  10 = Number of operating phases is 4  11 = Number of operating phases is 4

# 8.6 S2\_FREQ\_BCLK\_GEN\_CLK

## 0x11904 S2\_FREQ\_PERPH\_TYPE

**Type:** read-only

Clock: PBUS\_WRCLK Reset State: 0x1D Reset Name: N/A

Peripheral Type

## \$2\_FREQ\_PERPH\_TYPE

Bits	Name	Туре	Description
7:0	TYPE	read- only	BCLK GEN

## 0x11905 S2\_FREQ\_PERPH\_SUBTYPE

**Type:** read-only

Clock: PBUS\_WRCLK Reset State: 0x09 Reset Name: N/A

Peripheral SubType

### S2\_FREQ\_PERPH\_SUBTYPE

Bits	Name	Туре	Description
7:0	SUBTYPE	read- only	BCLK GEN CLK

## 0x11946 S2\_FREQ\_CLK\_ENABLE

Type: read-write Clock: PBUS\_WRCLK Reset State: 0x01

**Reset Name:** PERPH\_RB

#### S2\_FREQ\_CLK\_ENABLE

Bits	Name	Type	Description
7	EN_CLK_INT	read- write	0 = do not force the clock on 1 = enable the clock
0	FOLLOW_CLK_SX_REQ	read- write	0 = ignore smps_clk_req <x> 1 = clock is enabled when the clocks request is high smps_clk_req<x>='1'</x></x>

## 0x11950 S2\_FREQ\_CLK\_DIV

Type: read-write
Clock: PBUS\_WRCLK
Reset State: 0x05

**Reset Name:** PERPH\_RB

PMIC\_GANGED

### S2\_FREQ\_CLK\_DIV

Bits	Name	Туре	Description
3:0	CLK_DIV	read- write	clock_ frequency = 19.2MHz / (CLK_DIV + 1) FTS2 Buck supports 3.2, 4.8, 6.4 and 9.6 MHz HF2 Buck supports 1.6, 2.4, 2.74, 3.2, 3.8, 4.8, and 6.4 MHz CLK_DIV = 0 is not supported, it will generate 9.6 MHz

## 0x11951 S2\_FREQ\_CLK\_PHASE

Type: read-write Clock: PBUS\_WRCLK Reset State: 0x01

**Reset Name:** PERPH\_RB

### S2\_FREQ\_CLK\_PHASE

Bits	Name	Туре	Description
3:0	CLK_PHASE	read- write	Distributed clock phase select: clock phase delay = clock period * (CLK_PHASE / 16)

## 0x119C0 S2\_FREQ\_GANG\_CTL1

Type: read-write Clock: PBUS\_WRCLK Reset State: 0x17

**Reset Name:** PERPH\_RB

### S2\_FREQ\_GANG\_CTL1

Bits	Name	Туре	Description
7:0	GANG_LEADER_PID	read- write	When GANG_EN (GANG_CTL2[7]) is set, this peripheral will write the same data that is written to the gang leader Peripheral ID. Reads to the gang leader Peripheral ID are ignored by this peripheral. Ganged peripherals must reside within the same Slave ID

## 0x119C1 S2\_FREQ\_GANG\_CTL2

Type: read-write Clock: PBUS\_WRCLK Reset State: 0x80 Reset Name: PERPH\_RB

### S2\_FREQ\_GANG\_CTL2

Bits	Name	Туре	Description
7	GANG_EN	read- write	0 = disable 1 = enable When enabled, this peripheral will write the same data that is written to the gang leader PID. Reads to the gang leader PID are ignored by this peripheral

# 8.7 S3\_CTRL\_HFBUCK2\_CTRL

## 0x11A04 S3\_CTRL\_PERPH\_TYPE

**Type:** read-only

Clock: PBUS\_WRCLK Reset State: 0x03 Reset Name: N/A

Peripheral Type

#### S3\_CTRL\_PERPH\_TYPE

Bits	Name	Туре	Description
7:0	TYPE	read- only	SMPS

## 0x11A05 S3\_CTRL\_PERPH\_SUBTYPE

**Type:** read-only

Clock: PBUS\_WRCLK Reset State: 0x08 Reset Name: N/A

Peripheral SubType

### S3\_CTRL\_PERPH\_SUBTYPE

Bits	Name	Туре	Description
7:0	SUBTYPE	read- only	2A HF BUCK

## 0x11A08 S3\_CTRL\_STATUS

**Type:** read-only

Clock: PBUS\_WRCLK Reset State: Undefined Reset Name: N/A

Status Registers

### S3\_CTRL\_STATUS

Bits	Name	Туре	Description
7	VREG_OK	read- only	0 = VREG output voltage is below VREG_OK threshold 1 = VREG output voltage is above VREG_OK threshold

### S3\_CTRL\_STATUS (Continued)

Bits	Name	Туре	Description
5	ILS	read- only	Illegal Limit Stop. This is triggered when UL_Voltage < LL_Voltage
4	UL_VOLTAGE	read- only	Last voltage set was above or equal to UL_Voltage
3	LL_VOLTAGE	read- only	Last voltage set was below or equal to LL_Voltage
2	PS_TRUE	read- only	0 = buck is not pulse skipping 1 = buck is pulse skipping
1	NPM_TRUE	read- only	1 = VREG_OK and BUCK is in NPM
0	STEPPER_DONE	read- only	1 = stepper is done

## 0x11A10 S3\_CTRL\_INT\_RT\_STS

Type: read-only

Clock: PBUS\_WRCLK Reset State: 0x00

Reset Name: PERPH\_RB

Interrupt Real Time Status Bits

### S3\_CTRL\_INT\_RT\_STS

Bits	Name	Туре	Description
1	LIMIT_ERR_INT	read- only	Last voltage set was above UL or below LL
0	VREG_OK_INT	read- only	Regulator has been successfully enabled

## 0x11A11 S3\_CTRL\_INT\_SET\_TYPE

Type: read-write
Clock: PBUS\_WRCLK
Reset State: 0x00

**Reset Name:** PERPH\_RB

0 = use level trigger interrupts, 1 = use edge trigger interrupts

### S3\_CTRL\_INT\_SET\_TYPE

Bits	Name	Туре	Description
1	LIMIT_ERR_INT	read- write	
0	VREG_OK_INT	read- write	

### 0x11A12 S3\_CTRL\_INT\_POLARITY\_HIGH

**Type:** read-write

Clock: PBUS\_WRCLK Reset State: 0x00

Reset Name: PERPH\_RB

1= Interrupt will trigger on a level high (rising edge) event, 0 = level high triggering is disabled

### S3\_CTRL\_INT\_POLARITY\_HIGH

Bits	Name	Туре	Description
1	LIMIT_ERR_INT	read- write	2/20
0	VREG_OK_INT	read- write	9.5

## 0x11A13 S3\_CTRL\_INT\_POLARITY\_LOW

Type: read-write Clock: PBUS WRCLK

**Reset State:** 0x00 **Reset Name:** PERPH\_RB

1' = Interrupt will trigger on a level low (falling edge) event, '0' = level low triggering is disabled

## S3\_CTRL\_INT\_POLARITY\_LOW

Bits	Name	Туре	Description
1	LIMIT_ERR_INT	read- write	
0	VREG_OK_INT	read- write	

### 0x11A14 S3 CTRL INT LATCHED CLR

Type: write-only Clock: PBUS\_WRCLK Reset State: 0x00 Reset Name: PERPH RB

Writing a '1' to this interrupt will rearm the interrupt when an interrupt is pending. It clears the

internal sticky and sent bits

### S3\_CTRL\_INT\_LATCHED\_CLR

Bits	Name	Туре	Description
1	LIMIT_ERR_INT	write- only	P .
0	VREG_OK_INT	write- only	

## 0x11A15 S3\_CTRL\_INT\_EN\_SET

Type: read-write Clock: PBUS\_WRCLK Reset State: 0x00

Reset Name: PERPH\_RB

Writing '0' to this register has no effect. Writing a '1' will enable the corresponding interrupt.

Reading this register will readback enable status

PMIC SET MASK

#### S3\_CTRL\_INT\_EN\_SET

Bits	Name	Туре	Description
1	LIMIT_ERR_INT	read- write	
0	VREG_OK_INT	read- write	

### 0x11A16 S3\_CTRL\_INT\_EN\_CLR

Type: read-write Clock: PBUS\_WRCLK Reset State: 0x00 Reset Name: PERPH\_RB

Writing '0' to this register has no effect. Writing a '1' will disable the corresponding interrupt.

Reading this register will readback enable status

### PMIC\_CLR\_MASK=INT\_EN\_SET

### S3\_CTRL\_INT\_EN\_CLR

Bits	Name	Туре	Description
1	LIMIT_ERR_INT	read- write	
0	VREG_OK_INT	read- write	

## 0x11A18 S3\_CTRL\_INT\_LATCHED\_STS

Type: read-only Clock: PBUS\_WRCLK Reset State: 0x00

Reset Name: PERPH\_RB

Debug: Latched (Sticky) Interrupt. '1' indicates that the interrupt has triggered. Once the latched bit is set it can only be cleared by writing the clear bit.

### S3\_CTRL\_INT\_LATCHED\_STS

Bits	Name	Type	Description
1	LIMIT_ERR_INT	read- only	2.
0	VREG_OK_INT	read- only	

### 0x11A19 S3 CTRL INT PENDING STS

**Type:** read-only

Clock: PBUS\_WRCLK Reset State: 0x00

Reset Name: PERPH\_RB

Debug: Pending is set if interrupt has been sent but not cleared.

### S3\_CTRL\_INT\_PENDING\_STS

Bits	Name	Туре	Description
1	LIMIT_ERR_INT	read- only	
0	VREG_OK_INT	read- only	

## 0x11A1A S3\_CTRL\_INT\_MID\_SEL

Type: read-write Clock: PBUS\_WRCLK Reset State: 0x00 Reset Name: PERPH\_RB

Selects the MID that will receive the interrupt

### S3\_CTRL\_INT\_MID\_SEL

Bits	Name	Type	Description
1:0	INT_MID_SEL	read- write	

## 0x11A1B S3\_CTRL\_INT\_PRIORITY

Type: read-write Clock: PBUS\_WRCLK Reset State: 0x00 Reset Name: PERPH\_RB

## S3\_CTRL\_INT\_PRIORITY

Bits	Name	Type	Description
0	INT_PRIORITY	read- write	SR=0 A=1

### 0x11A40 S3 CTRL VOLTAGE CTL1

Type: read-write Clock: PBUS\_WRCLK Reset State: 0x00 Reset Name: PERPH\_RB

PMIC\_LATCHED\_WRITE=VOLTAGE\_CTL2

## S3\_CTRL\_VOLTAGE\_CTL1

Bits	Name	Туре	Description
0	RANGE	read- write	0: 0.375 to 1.5625 V at steps of 12.5 mV (Vmin = 0.375 V, Vstep = 12.5 mV)
			1 : 1.550 to 3.1250 V at steps of 25.0 mV (Vmin = 1.550 V, Vstep = 25.0 mV)

## 0x11A41 S3\_CTRL\_VOLTAGE\_CTL2

Type: read-write Clock: PBUS\_WRCLK Reset State: 0x3E Reset Name: PERPH\_RB

### S3\_CTRL\_VOLTAGE\_CTL2

Bits	Name	Туре	Description
6:0	V_SET	read- write	Voltage = Vmin + VSET*(Vstep)

## 0x11A45 S3\_CTRL\_MODE\_CTL

Type: read-write Clock: PBUS\_WRCLK Reset State: 0x80

Reset Name: PERPH\_RB

**Define Buck Mode Transitions** 

### S3\_CTRL\_MODE\_CTL

Bits	Name	Type	Description
7	PWM	read- write	Force PWM
6	AUTO_MODE	read- write	1=Automatically enter NPM based on current
4	FOLLOW_PMIC_AWAKE	read- write	NPM when PMIC_AWAKE (SLEEP_B) = '1'
3	FOLLOW_HWEN3	read- write	1' BUCK is in NPM when HWEN3 ='1', '0'= ignore HWEN3
2	FOLLOW_HWEN2	read- write	1' BUCK is in NPM when HWEN2 ='1', '0'= ignore HWEN2
1	FOLLOW_HWEN1	read- write	1' BUCK is in NPM when HWEN1 ='1', '0'= ignore HWEN1
0	FOLLOW_HWEN0	read- write	1' BUCK is in NPM when HWEN0 ='1', '0'= ignore HWEN0

## 0x11A46 S3\_CTRL\_EN\_CTL

Type: read-write
Clock: PBUS\_WRCLK
Reset State: 0x00

Reset Name: PERPH\_RB

## S3\_CTRL\_EN\_CTL

Bits	Name	Туре	Description
7	PERPH_EN	read- write	1' = Enable the BUCK, '0' = do not force BUCK on
3	FOLLOW_HWEN3	read- write	1' BUCK is enabled when HWEN3 ='1', '0'= ignore HWEN3
2	FOLLOW_HWEN2	read- write	1' BUCK is enabled when HWEN2 ='1', '0'= ignore HWEN2
1	FOLLOW_HWEN1	read- write	1' BUCK is enabled when HWEN1 ='1', '0'= ignore HWEN1
0	FOLLOW_HWEN0	read- write	1' BUCK is enabled when HWEN0 ='1', '0'= ignore HWEN0

## 0x11A48 S3\_CTRL\_PD\_CTL

Type: read-write Clock: PBUS\_WRCLK Reset State: 0x80

Reset Name: PERPH\_RB

### S3\_CTRL\_PD\_CTL

Bits	Name	Туре	Description
7	PD_EN	read- write	1' = Enable the pulldown when the regulator is disabled, '0' = pulldown is always disabled. Preset by trim register

# 8.8 S3\_FREQ\_BCLK\_GEN\_CLK

## 0x11C04 S3\_FREQ\_PERPH\_TYPE

**Type:** read-only

Clock: PBUS\_WRCLK Reset State: 0x1D Reset Name: N/A

Peripheral Type

## S3\_FREQ\_PERPH\_TYPE

Bi	its	Name	Туре	Description
7:	':0	TYPE	read- only	BCLK GEN

## 0x11C05 S3\_FREQ\_PERPH\_SUBTYPE

**Type:** read-only

Clock: PBUS\_WRCLK Reset State: 0x09 Reset Name: N/A

Peripheral SubType

### S3\_FREQ\_PERPH\_SUBTYPE

Bits	Name	Туре	Description
7:0	SUBTYPE	read- only	BCLK GEN CLK

## 0x11C46 S3\_FREQ\_CLK\_ENABLE

Type: read-write Clock: PBUS\_WRCLK Reset State: 0x01

Reset Name: PERPH\_RB

#### S3\_FREQ\_CLK\_ENABLE

Bits	Name	Type	Description
7	EN_CLK_INT	read- write	0 = do not force the clock on 1 = enable the clock
0	FOLLOW_CLK_SX_REQ	read- write	0 = ignore smps_clk_req <x> 1 = clock is enabled when the clocks request is high smps_clk_req<x>='1'</x></x>

## 0x11C50 S3\_FREQ\_CLK\_DIV

Type: read-write
Clock: PBUS\_WRCLK
Reset State: 0x05

**Reset Name:** PERPH\_RB

PMIC\_GANGED

### S3\_FREQ\_CLK\_DIV

Bits	Name	Туре	Description
3:0	CLK_DIV	read- write	clock_ frequency = 19.2MHz / (CLK_DIV + 1) FTS2 Buck supports 3.2, 4.8, 6.4 and 9.6 MHz HF2 Buck supports 1.6, 2.4, 2.74, 3.2, 3.8, 4.8, and 6.4 MHz CLK_DIV = 0 is not supported, it will generate 9.6 MHz

## 0x11C51 S3\_FREQ\_CLK\_PHASE

Type: read-write Clock: PBUS\_WRCLK Reset State: 0x07 Reset Name: PERPH\_RB

## S3\_FREQ\_CLK\_PHASE

Bits	Name	Туре	Description
3:0	CLK_PHASE	read- write	Distributed clock phase select: clock phase delay = clock period * (CLK_PHASE / 16)

## 0x11CC0 S3\_FREQ\_GANG\_CTL1

Type: read-write
Clock: PBUS\_WRCLK
Reset State: 0x00

**Reset Name:** PERPH\_RB

### S3\_FREQ\_GANG\_CTL1

Bits	Name	Туре	Description
7:0	GANG_LEADER_PID	read- write	When GANG_EN (GANG_CTL2[7]) is set, this peripheral will write the same data that is written to the gang leader Peripheral ID. Reads to the gang leader Peripheral ID are ignored by this peripheral. Ganged peripherals must reside within the same Slave ID

## 0x11CC1 S3\_FREQ\_GANG\_CTL2

Type: read-write Clock: PBUS\_WRCLK Reset State: 0x00 Reset Name: PERPH\_RB

### S3\_FREQ\_GANG\_CTL2

Bits	Name	Туре	Description
7	GANG_EN	read- write	0 = disable 1 = enable When enabled, this peripheral will write the same data that is written to the gang leader PID. Reads to the gang leader PID are ignored by this peripheral

# 8.9 S4\_CTRL\_FTS2\_CTRL

## 0x11D04 S4\_CTRL\_PERPH\_TYPE

**Type:** read-only

Clock: PBUS\_WRCLK Reset State: 0x03 Reset Name: N/A

Peripheral Type

#### S4\_CTRL\_PERPH\_TYPE

Bits	Name	Туре	Description
7:0	TYPE	read- only	FTS2 Control Reset State: 0x03

## 0x11D05 S4\_CTRL\_PERPH\_SUBTYPE

**Type:** read-only

Clock: PBUS\_WRCLK Reset State: 0x08 Reset Name: N/A

Peripheral SubType

### S4\_CTRL\_PERPH\_SUBTYPE

Bits	Name	Туре	Description
7:0	SUBTYPE	read- only	

## 0x11D08 S4\_CTRL\_STATUS\_1

**Type:** read-only

Clock: PBUS\_WRCLK Reset State: Undefined Reset Name: N/A

Status Registers

### S4\_CTRL\_STATUS\_1

Bits	Name	Туре	Description
7	VREG_OK_FLAG	read- only	Indicates that VREG_SNS has reached a value that is greater than or equal to the threshold of the comparator tasked for VREG_SNS monitoring

## S4\_CTRL\_STATUS\_1 (Continued)

Bits	Name	Туре	Description
6	VREG_FAULT_FLAG	read- only	Indicates a probable short circuit condition at VREG_SNS since VREG_SNS is below the VREG fault voltage level and the softstart ramp is done. Current limit foldback is in use.
1	NPM_FLAG	read- only	Indicates normal power mode is in use
0	STEPPER_DONE_FLAG	read- only	Softstart stepper and voltage stepper done

## 0x11D09 S4\_CTRL\_STATUS\_2

**Type:** read-only

Clock: PBUS\_WRCLK Reset State: Undefined Reset Name: N/A

Status Registers

## S4\_CTRL\_STATUS\_2

Bits	Name	Туре	Description
4	ILS_FLAG	read- only	Either of the following:  => Both limit stops have been enabled, but the upper limit stop VSET_ULS has been programmed to a value below the lower limit stop VSET_LLS  => Both limit stops have been enabled, but the lower limit stop VSET_LLS has been programmed to a value above the upper limit stop VSET_ULS
3	ULS_FLAG	read- only	Indicates that the voltage setpoint has been programmed to a value that is greater than or equal to the upper limit stop VSET_ULS
2	LLS_FLAG	read- only	Indicates that the voltage setpoint has been programmed to a value that is less than or equal to the lower limit stop VSET_LLS
1	GPL_HI_FLAG	read- only	Indicates that the voltage setpoint has reached a value that is greater than or equal to the high general purpose limit VSET_GPL_HI
0	GPL_LO_FLAG	read- only	Indicates that the voltage setpoint has reached a value that is less than or equal to the low general purpose limit VSET_GPL_LO

## 0x11D10 S4\_CTRL\_INT\_RT\_STS

**Type:** read-only

Clock: PBUS\_WRCLK
Reset State: Undefined
Reset Name: PERPH\_RB

**Interrupt Real Time Status Bits** 

### S4\_CTRL\_INT\_RT\_STS

Bits	Name	Туре	Description
2	VREG_FAULT_INT	read- only	
1	LIMIT_ERR_INT	read- only	
0	VREG_OK_INT	read- only	.51

## 0x11D11 S4\_CTRL\_INT\_SET\_TYPE

Type: read-write Clock: PBUS\_WRCLK Reset State: 0x00 Reset Name: PERPH\_RB

0 =use level trigger interrupts, 1 =use edge trigger interrupts

### S4 CTRL INT SET TYPE

Bits	Name	Туре	Description
2	VREG_FAULT_INT	read- write	
1	LIMIT_ERR_INT	read- write	
0	VREG_OK_INT	read- write	

### 0x11D12 S4\_CTRL\_INT\_POLARITY\_HIGH

Type: read-write Clock: PBUS\_WRCLK Reset State: 0x00 Reset Name: PERPH\_RB

1= Interrupt will trigger on a level high (rising edge) event, 0 = level high triggering is disabled

### **S4\_CTRL\_INT\_POLARITY\_HIGH**

Bits	Name	Туре	Description
2	VREG_FAULT_INT	read- write	
1	LIMIT_ERR_INT	read- write	
0	VREG_OK_INT	read- write	

## 0x11D13 S4\_CTRL\_INT\_POLARITY\_LOW

Type: read-write Clock: PBUS\_WRCLK Reset State: 0x00 Reset Name: PERPH\_RB

1' = Interrupt will trigger on a level low (falling edge) event, '0' = level low triggering is disabled

### S4\_CTRL\_INT\_POLARITY\_LOW

Bits	Name	Туре	Description
2	VREG_FAULT_INT	read- write	1,70.
1	LIMIT_ERR_INT	read- write	0,90
0	VREG_OK_INT	read- write	

### 0x11D14 S4\_CTRL\_INT\_LATCHED\_CLR

Type: write-only Clock: PBUS\_WRCLK Reset State: 0x00 Reset Name: PERPH\_RB

Writing a '1' to this interrupt will rearm the interrupt when an interrupt is pending. It clears the

internal sticky and sent bits

### S4\_CTRL\_INT\_LATCHED\_CLR

Bits	Name	Туре	Description
2	VREG_FAULT_INT	write- only	

## S4\_CTRL\_INT\_LATCHED\_CLR (Continued)

Bits	Name	Туре	Description
1	LIMIT_ERR_INT	write- only	
0	VREG_OK_INT	write- only	

### 0x11D15 S4\_CTRL\_INT\_EN\_SET

Type: read-write Clock: PBUS\_WRCLK Reset State: 0x00 Reset Name: PERPH\_RB

Writing '0' to this register has no effect. Writing a '1' will enable the corresponding interrupt. Reading this register will readback enable status

PMIC\_SET\_MASK

### S4\_CTRL\_INT\_EN\_SET

Bits	Name	Туре	Description
2	VREG_FAULT_INT	read- write	0.7
1	LIMIT_ERR_INT	read- write	
0	VREG_OK_INT	read- write	

## 0x11D16 S4\_CTRL\_INT\_EN\_CLR

Type: read-write Clock: PBUS\_WRCLK Reset State: 0x00 Reset Name: PERPH RB

Writing '0' to this register has no effect. Writing a '1' will disable the corresponding interrupt. Reading this register will readback enable status

PMIC\_CLR\_MASK=INT\_EN\_SET

### S4\_CTRL\_INT\_EN\_CLR

Bits	Name	Туре	Description
2	VREG_FAULT_INT	read- write	

### S4\_CTRL\_INT\_EN\_CLR (Continued)

Bits	Name	Туре	Description
1	LIMIT_ERR_INT	read- write	
0	VREG_OK_INT	read- write	

## 0x11D18 S4\_CTRL\_INT\_LATCHED\_STS

Type: read-only Clock: PBUS\_WRCLK Reset State: 0x00 Reset Name: PERPH\_RB

Debug: Latched (Sticky) Interrupt. '1' indicates that the interrupt has triggered. Once the latched bit is set it can only be cleared by writing the clear bit.

### S4\_CTRL\_INT\_LATCHED\_STS

Bits	Name	Туре	Description
2	VREG_FAULT_INT	read- only	Trito No
1	LIMIT_ERR_INT	read- only	720.
0	VREG_OK_INT	read- only	<i>9</i> 2.

## 0x11D19 S4\_CTRL\_INT\_PENDING\_STS

Type: read-only Clock: PBUS\_WRCLK Reset State: 0x00 Reset Name: PERPH RB

Debug: Pending is set if interrupt has been sent but not cleared.

### S4\_CTRL\_INT\_PENDING\_STS

Bits	Name	Туре	Description
2	VREG_FAULT_INT	read- only	
1	LIMIT_ERR_INT	read- only	
0	VREG_OK_INT	read- only	

## 0x11D1A S4\_CTRL\_INT\_MID\_SEL

Type: read-write Clock: PBUS\_WRCLK Reset State: 0x00 Reset Name: PERPH\_RB

Selects the MID that will receive the interrupt

### S4\_CTRL\_INT\_MID\_SEL

Bits	Name	Туре	Description
1:0	INT_MID_SEL	read- write	-

## 0x11D1B S4\_CTRL\_INT\_PRIORITY

Type: read-write Clock: PBUS\_WRCLK Reset State: 0x00

Reset Name: PERPH\_RB

SR = 0 A = 1

## S4\_CTRL\_INT\_PRIORITY

В	its	Name	Туре	Description
	0	INT_PRIORITY	read- write	

## 0x11D40 S4\_CTRL\_VOLTAGE\_CTL1

Type: read-write Clock: PBUS\_WRCLK Reset State: 0x00 Reset Name: PERPH\_RB

PMIC\_GANGED

### S4\_CTRL\_VOLTAGE\_CTL1

Bits	Name	Туре	Description
0	MV_RANGE	read- write	0 = Use low voltage range as specified by VSET and PFM_VOFFSET
			1 = Use medium voltage range as specified by VSET and PFM_VOFFSET

## 0x11D41 S4\_CTRL\_VOLTAGE\_CTL2

Type: read-write Clock: PBUS\_WRCLK Reset State: 0xB4 Reset Name: PERPH\_RB

PMIC\_GANGED

### S4\_CTRL\_VOLTAGE\_CTL2

Bits	Name	Туре	Description
7:0	VSET	read- write	Output voltage set point in PWM mode and in PFM mode if the PFM_VOFFSET_EN bit is not asserted
		S	For MV_RANGE = 0: VSET => 0.005V * m + 0.080V, where m = <7:0> For MV_RANGE = 1: VSET => 0.010V * m + 0.160V, where m = <7:0> If PFM_VOFFSET_EN is asserted and in PFM mode, add PFM_VOFFSET

## 0x11D42 S4\_CTRL\_VSET\_VALID

Type: read-only Clock: PBUS\_WRCLK Reset State: Undefined Reset Name: PERPH\_RB

### S4\_CTRL\_VSET\_VALID

Bits	Name	Туре	Description
7:0	VSET_VALID	read- only	Readback the valid output voltage setpoint value

## 0x11D44 S4\_CTRL\_VOLTAGE\_CTL3

**Type:** read-write **Clock:** PBUS\_WRCLK **Reset State:** 0x00

Reset Name: PERPH\_RB

# S4\_CTRL\_VOLTAGE\_CTL3

Bits	Name	Туре	Description
7	PFM_VOFFSET_EN	read- write	When in PFM mode  0 = Use VSET for output voltage set point  1 = Use VSET + PFM_VOFFSET for output voltage set point
1:0	PFM_VOFFSET	read- write	When in PFM mode and PFM_VOFFSET_EN is asserted, add a positive output voltage offset  For MV_RANGE = 0:  VOFFSET = 0.005V * 2 * m, where m = <1:0>  For MV_RANGE = 1:  VOFFSET = 0.010V * 2 * m, where m = <1:0>

# 0x11D45 S4\_CTRL\_MODE\_CTL

Type: read-write Clock: PBUS\_WRCLK Reset State: 0x80

Reset Name: PERPH\_RB

PMIC\_GANGED

### S4\_CTRL\_MODE\_CTL

Bits	Name	Туре	Description
7	NPM	read- write	FTS NON-AUTO mode control 0 = Low power mode (LPM) unless AUTO_MODE is asserted 1 = Normal power mode (PWM)
6	AUTO_MODE	read- write	When asserted, FTS automatically enters and exits low power mode (PFM) based on load current qualifying triggers  0 = AUTO mode is disabled  1 = AUTO mode is enabled

# 0x11D46 S4\_CTRL\_EN\_CTL

Type: read-write
Clock: PBUS\_WRCLK
Reset State: 0x00
Reset Name: PERPIT DI

Reset Name: PERPH\_RB

### S4\_CTRL\_EN\_CTL

Bits Name Type	Description
write 0 = Off	ble control
write 0 = Off 1 = On	

# 0x11D48 S4\_CTRL\_PD\_CTL

Type: read-write Clock: PBUS\_WRCLK Reset State: 0x80 Reset Name: PERPH\_RB

### S4\_CTRL\_PD\_CTL

Bits	Name	Туре	Description
7	PD_EN	read- write	0 = Strong pulldown is always disabled 1 = Strong pulldown is enabled when the regulator is disabled
6	WEAK_PD_EN	read- write	0 = Weak pulldown is not enabled in OFF state 1 = Weak pulldown is enabled in OFF state
5	WEAK_PD_PFM	read- write	0 = Weak pulldown is not enabled in PFM mode 1 = Weak pulldown is enabled in PFM mode
4	WEAK_PD_PWM	read- write	0 = Weak pulldown is not enabled in PWM mode (and in HCPFM mode) 1 = Weak pulldown is enabled in PWM mode (and in HCPFM mode)

# 0x11D54 S4\_CTRL\_PHASE\_CNT

Type: read-write
Clock: PBUS\_WRCLK
Reset State: 0x00
Reset Name: PERBLI PA

Reset Name: PERPH\_RB

### S4\_CTRL\_PHASE\_CNT

Bits	Name	Туре	Description
1:0	PHASE_CNT	read- write	When MULTIPHASE_EN is asserted, the number of operating phases is  00 = Number of operating phases is 1  01 = Number of operating phases is 2  10 = Number of operating phases is 4  11 = Number of operating phases is 4

# 0x11D60 S4\_CTRL\_SS\_CTL

Type: read-write Clock: PBUS\_WRCLK Reset State: 0x08

Reset Name: PERPH\_RB

PMIC\_GANGED

# S4\_CTRL\_SS\_CTL

Bits	Name	Туре	Description
4:3	SS_STEP	read- write	Softstart voltage step size  00 = SS voltage step of 1 * LSB of VPROG  01 = SS voltage step of 2 * LSB  10 = SS voltage step of 4 * LSB  11 = SS voltage step of 8 * LSB
2:0	SS_DELAY	read- write	Softstart delay between steps = 2 ^ (m + 3) / Fsys, where m = <2:0> (Fsys = 19.2 MHz):  000 = 8-clock cycles (417ns)  001 = 16-clock cycles  010 = 32-clock cycles  011 = 64-clock cycles  100 = 128-clock cycles (6.67us)  101 = 256-clock cycles  110 = 512-clock cycles  111 = 1024-clock cycles (53.3us)

# 0x11D61 S4\_CTRL\_VS\_CTL

Type: read-write
Clock: PBUS\_WRCLK
Reset State: 0x00
Paget Name: PERPLIA

Reset Name: PERPH\_RB

### S4\_CTRL\_VS\_CTL

Bits	Name	Туре	Description
7	VS_EN	read-	Voltage stepping control
		write	0 = VS is disabled
			1 = VS is enabled
4:3	VS_STEP	read-	Voltage stepping voltage step size
		write	00 = VS voltage step of 1 * LSB of VPROG
			01 = VS voltage step of 2 * LSB
			10 = VS voltage step of 4 * LSB
			11 = VS voltage step of 8 * LSB
2:0	VS_DELAY	read-	Voltage stepping delay between steps = 2 ^ (m + 3) /
		write	Fsys, where m = <2:0> (Assuming Fsys = 19.2 MHz):
			Desired default is 1.67us
			000 = 8-clock cycles (417ns)
			001 = 16-clock cycles
			010 = 32-clock cycles
			011 = 64-clock cycles
			100 = 128-clock cycles (6.67us)
			101 = 256-clock cycles
		1	110 = 512-clock cycles
		~6°	111 = 1024-clock cycles (53.3us)

# 0x11D6A S4\_CTRL\_ULS\_VALID

Type: read-only
Clock: PBUS\_WRCLK
Reset State: Undefined
Reset Name: PERPH\_RB

S4\_CTRL\_ULS\_VALID

Bits	Name	Туре	Description
7:0	ULS_VALID	read- only	Readback the valid upper limit stop value

# 0x11D6C S4\_CTRL\_LLS\_VALID

Type: read-only Clock: PBUS\_WRCLK Reset State: Undefined Reset Name: PERPH\_RB

# S4\_CTRL\_LLS\_VALID

Bits	Name	Туре	Description
7:0	LLS_VALID	read- only	Readback the valid lower limit stop value

# 8.10 S4\_PS\_FTS2\_PS

# 0x11E04 S4\_PS\_PERPH\_TYPE

**Type:** read-only

Clock: PBUS\_WRCLK Reset State: 0x1C Reset Name: N/A

Peripheral Type

#### S4\_PS\_PERPH\_TYPE

Bits	Name	Туре	Description
7:0	TYPE	read- only	FTS2 Power Stage Reset State: 0x1C

#### 0x11E05 S4 PS PERPH SUBTYPE

**Type:** read-only

Clock: PBUS\_WRCLK Reset State: 0x08 Reset Name: N/A

Peripheral SubType

#### S4\_PS\_PERPH\_SUBTYPE

Bits	Name	Type	Description
7:0	SUBTYPE	read- only	

# 0x11E40 S4\_PS\_VOLTAGE\_CTL1

Type: read-write Clock: PBUS\_WRCLK Reset State: 0x00

Reset Name: PERPH\_RB

### S4\_PS\_VOLTAGE\_CTL1

Bits	Name	Туре	Description
0	MV_RANGE	read- write	0 = Use low voltage range as specified by VSET and PFM_VOFFSET 1 = Use medium voltage range as specified by VSET and PFM_VOFFSET

# 0x11E41 S4\_PS\_VOLTAGE\_CTL2

Type: read-write Clock: PBUS\_WRCLK Reset State: 0xB4 Reset Name: PERPH\_RB

PMIC\_GANGED

### S4\_PS\_VOLTAGE\_CTL2

Bits	Name	Type	Description
7:0	VSET	read- write	Output voltage set point in PWM mode and in PFM mode if the PFM_VOFFSET_EN bit is not asserted
		8.0	For MV_RANGE = 0:
			VSET => 0.005V * m + 0.080V, where $m = <7:0>$
	Y, 2,		For MV_RANGE = 1:
	20.0		VSET => 0.010V * m + 0.160V, where m = <7:0>
	W.	(2)	If PFM_VOFFSET_EN is asserted and in PFM mode, add PFM_VOFFSET

### 0x11E54 S4\_PS\_PHASE\_CNT

Type: read-write Clock: PBUS\_WRCLK Reset State: 0x00 Reset Name: PERPH\_RB

PMIC\_GANGED, PMIC\_SYNC=clk\_19p2:phase\_cnt\_rb

# S4\_PS\_PHASE\_CNT

Bits	Name	Туре	Description
1:0	PHASE_CNT	read- write	When MULTIPHASE_EN is asserted, the number of operating phases is  00 = Number of operating phases is 1  01 = Number of operating phases is 2  10 = Number of operating phases is 4  11 = Number of operating phases is 4

# 8.11 S4\_FREQ\_BCLK\_GEN\_CLK

# 0x11F04 S4\_FREQ\_PERPH\_TYPE

**Type:** read-only

Clock: PBUS\_WRCLK Reset State: 0x1D Reset Name: N/A

Peripheral Type

#### S4\_FREQ\_PERPH\_TYPE

Bits	Name	Туре	Description
7:0	TYPE	read- only	BCLK GEN

# 0x11F05 S4\_FREQ\_PERPH\_SUBTYPE

**Type:** read-only

Clock: PBUS\_WRCLK Reset State: 0x09 Reset Name: N/A

Peripheral SubType

#### S4\_FREQ\_PERPH\_SUBTYPE

Bits	Name	Туре	Description
7:0	SUBTYPE	read- only	BCLK GEN CLK

# 0x11F46 S4\_FREQ\_CLK\_ENABLE

Type: read-write Clock: PBUS\_WRCLK Reset State: 0x01

Reset Name: PERPH\_RB

#### S4\_FREQ\_CLK\_ENABLE

Bits	Name	Туре	Description
7	EN_CLK_INT	read- write	0 = do not force the clock on 1 = enable the clock
0	FOLLOW_CLK_SX_REQ	read- write	0 = ignore smps_clk_req <x> 1 = clock is enabled when the clocks request is high smps_clk_req<x>='1'</x></x>

# 0x11F50 S4\_FREQ\_CLK\_DIV

Type: read-write Clock: PBUS\_WRCLK Reset State: 0x05 Reset Name: PERPH\_RB

PMIC\_GANGED

### S4\_FREQ\_CLK\_DIV

Bits	Name	Туре	Description
3:0	CLK_DIV	read- write	clock_ frequency = 19.2MHz / (CLK_DIV + 1) FTS2 Buck supports 3.2, 4.8, 6.4 and 9.6 MHz HF2 Buck supports 1.6, 2.4, 2.74, 3.2, 3.8, 4.8, and 6.4 MHz CLK_DIV = 0 is not supported, it will generate 9.6 MHz

# 0x11F51 S4\_FREQ\_CLK\_PHASE

Type: read-write Clock: PBUS\_WRCLK Reset State: 0x03 Reset Name: PERPH\_RB

### S4\_FREQ\_CLK\_PHASE

Bits	Name	Туре	Description
3:0	CLK_PHASE	read- write	Distributed clock phase select: clock phase delay = clock period * (CLK_PHASE / 16)

# 0x11FC0 S4\_FREQ\_GANG\_CTL1

Type: read-write Clock: PBUS\_WRCLK Reset State: 0x1D Reset Name: PERPH\_RB

#### S4\_FREQ\_GANG\_CTL1

Bits	Name	Туре	Description
7:0	GANG_LEADER_PID	read- write	When GANG_EN (GANG_CTL2[7]) is set, this peripheral will write the same data that is written to the gang leader Peripheral ID. Reads to the gang leader Peripheral ID are ignored by this peripheral. Ganged peripherals must reside within the same Slave ID

# 0x11FC1 S4\_FREQ\_GANG\_CTL2

Type: read-write Clock: PBUS\_WRCLK Reset State: 0x80 Reset Name: PERPH\_RB

# S4\_FREQ\_GANG\_CTL2

Bits	Name	Туре	Description
7	GANG_EN	read- write	0 = disable 1 = enable When enabled, this peripheral will write the same data that is written to the gang leader PID. Reads to the gang leader PID are ignored by this peripheral

# 8.12 S5\_CTRL\_FTS2\_CTRL

# 0x12004 S5\_CTRL\_PERPH\_TYPE

**Type:** read-only

Clock: PBUS\_WRCLK Reset State: 0x03 Reset Name: N/A

Peripheral Type

#### S5\_CTRL\_PERPH\_TYPE

Bits	Name	Туре	Description
7:0	TYPE	read- only	FTS2 Control Reset State: 0x03

# 0x12005 S5\_CTRL\_PERPH\_SUBTYPE

**Type:** read-only

Clock: PBUS\_WRCLK Reset State: 0x08 Reset Name: N/A

Peripheral SubType

#### S5\_CTRL\_PERPH\_SUBTYPE

Bits	Name	Туре	Description
7:0	SUBTYPE	read- only	

#### 

**Type:** read-only

Clock: PBUS\_WRCLK Reset State: Undefined Reset Name: N/A

Status Registers

#### S5\_CTRL\_STATUS\_1

Bits	Name	Туре	Description
7	VREG_OK_FLAG	read- only	Indicates that VREG_SNS has reached a value that is greater than or equal to the threshold of the comparator tasked for VREG_SNS monitoring

# S5\_CTRL\_STATUS\_1 (Continued)

Bits	Name	Туре	Description
6	VREG_FAULT_FLAG	read- only	Indicates a probable short circuit condition at VREG_SNS since VREG_SNS is below the VREG fault voltage level and the softstart ramp is done. Current limit foldback is in use.
1	NPM_FLAG	read- only	Indicates normal power mode is in use
0	STEPPER_DONE_FLAG	read- only	Softstart stepper and voltage stepper done

#### 

**Type:** read-only

Clock: PBUS\_WRCLK Reset State: Undefined Reset Name: N/A

Status Registers

# S5\_CTRL\_STATUS\_2

Bits	Name	Туре	Description
4	ILS_FLAG	read- only	Either of the following:  => Both limit stops have been enabled, but the upper limit stop VSET_ULS has been programmed to a value below the lower limit stop VSET_LLS  => Both limit stops have been enabled, but the lower limit stop VSET_LLS has been programmed to a value above the upper limit stop VSET_ULS
3	ULS_FLAG	read- only	Indicates that the voltage setpoint has been programmed to a value that is greater than or equal to the upper limit stop VSET_ULS
2	LLS_FLAG	read- only	Indicates that the voltage setpoint has been programmed to a value that is less than or equal to the lower limit stop VSET_LLS
1	GPL_HI_FLAG	read- only	Indicates that the voltage setpoint has reached a value that is greater than or equal to the high general purpose limit VSET_GPL_HI
0	GPL_LO_FLAG	read- only	Indicates that the voltage setpoint has reached a value that is less than or equal to the low general purpose limit VSET_GPL_LO

## 0x12010 S5\_CTRL\_INT\_RT\_STS

**Type:** read-only

Clock: PBUS\_WRCLK Reset State: Undefined Reset Name: PERPH\_RB

**Interrupt Real Time Status Bits** 

#### S5\_CTRL\_INT\_RT\_STS

Bits	Name	Туре	Description
2	VREG_FAULT_INT	read- only	
1	LIMIT_ERR_INT	read- only	
0	VREG_OK_INT	read- only	.51

# 0x12011 S5\_CTRL\_INT\_SET\_TYPE

Type: read-write Clock: PBUS\_WRCLK Reset State: 0x00

Reset Name: PERPH\_RB

0 =use level trigger interrupts, 1 =use edge trigger interrupts

### S5 CTRL INT SET TYPE

Bits	Name	Туре	Description
2	VREG_FAULT_INT	read- write	
1	LIMIT_ERR_INT	read- write	
0	VREG_OK_INT	read- write	

### 0x12012 S5\_CTRL\_INT\_POLARITY\_HIGH

Type: read-write Clock: PBUS\_WRCLK Reset State: 0x00 Reset Name: PERPH\_RB

1= Interrupt will trigger on a level high (rising edge) event, 0 = level high triggering is disabled

### **S5\_CTRL\_INT\_POLARITY\_HIGH**

Bits	Name	Туре	Description
2	VREG_FAULT_INT	read- write	
1	LIMIT_ERR_INT	read- write	
0	VREG_OK_INT	read- write	

### 0x12013 S5\_CTRL\_INT\_POLARITY\_LOW

Type: read-write Clock: PBUS\_WRCLK Reset State: 0x00 Reset Name: PERPH\_RB

1' = Interrupt will trigger on a level low (falling edge) event, '0' = level low triggering is disabled

### S5\_CTRL\_INT\_POLARITY\_LOW

Bits	Name	Туре	Description
2	VREG_FAULT_INT	read- write	1,70.
1	LIMIT_ERR_INT	read- write	0,90
0	VREG_OK_INT	read- write	

### 0x12014 S5\_CTRL\_INT\_LATCHED\_CLR

Type: write-only Clock: PBUS\_WRCLK Reset State: 0x00 Reset Name: PERPH\_RB

Writing a '1' to this interrupt will rearm the interrupt when an interrupt is pending. It clears the

internal sticky and sent bits

### S5\_CTRL\_INT\_LATCHED\_CLR

Bits	Name	Туре	Description
2	VREG_FAULT_INT	write- only	

#### S5\_CTRL\_INT\_LATCHED\_CLR (Continued)

Bits	Name	Туре	Description
1	LIMIT_ERR_INT	write- only	
0	VREG_OK_INT	write- only	

### 0x12015 S5\_CTRL\_INT\_EN\_SET

Type: read-write Clock: PBUS\_WRCLK Reset State: 0x00 Reset Name: PERPH\_RB

Writing '0' to this register has no effect. Writing a '1' will enable the corresponding interrupt. Reading this register will readback enable status

PMIC\_SET\_MASK

### S5\_CTRL\_INT\_EN\_SET

Bits	Name	Туре	Description
2	VREG_FAULT_INT	read- write	o's
1	LIMIT_ERR_INT	read- write	
0	VREG_OK_INT	read- write	

# 0x12016 S5\_CTRL\_INT\_EN\_CLR

Type: read-write Clock: PBUS\_WRCLK Reset State: 0x00 Reset Name: PERPH RB

Writing '0' to this register has no effect. Writing a '1' will disable the corresponding interrupt. Reading this register will readback enable status

PMIC\_CLR\_MASK=INT\_EN\_SET

#### S5\_CTRL\_INT\_EN\_CLR

Bits	Name	Туре	Description
2	VREG_FAULT_INT	read- write	

### S5\_CTRL\_INT\_EN\_CLR (Continued)

Bits	Name	Туре	Description
1	LIMIT_ERR_INT	read- write	
0	VREG_OK_INT	read- write	

### 0x12018 S5\_CTRL\_INT\_LATCHED\_STS

Type: read-only Clock: PBUS\_WRCLK Reset State: 0x00 Reset Name: PERPH\_RB

Debug: Latched (Sticky) Interrupt. '1' indicates that the interrupt has triggered. Once the latched bit is set it can only be cleared by writing the clear bit.

### S5\_CTRL\_INT\_LATCHED\_STS

Bits	Name	Туре	Description
2	VREG_FAULT_INT	read- only	This No
1	LIMIT_ERR_INT	read- only	720.
0	VREG_OK_INT	read- only	0,90

# 0x12019 S5\_CTRL\_INT\_PENDING\_STS

Type: read-only Clock: PBUS\_WRCLK Reset State: 0x00 Reset Name: PERPH\_RB

Debug: Pending is set if interrupt has been sent but not cleared.

#### S5\_CTRL\_INT\_PENDING\_STS

Bits	Name	Type	Description
2	VREG_FAULT_INT	read- only	
1	LIMIT_ERR_INT	read- only	
0	VREG_OK_INT	read- only	

#### 0x1201A S5\_CTRL\_INT\_MID\_SEL

**Type:** read-write Clock: PBUS\_WRCLK **Reset State:** 0x00 Reset Name: PERPH\_RB

Selects the MID that will receive the interrupt

### S5\_CTRL\_INT\_MID\_SEL

Bits	Name	Туре	Description
1:0	INT_MID_SEL	read- write	-

#### 0x1201B **S5 CTRL INT PRIORITY**

**Type:** read-write Clock: PBUS\_WRCLK Reset State: 0x00

Reset Name: PERPH\_RB

SR=0 A=1

#### S5\_CTRL\_INT\_PRIORITY

В	its	Name	Туре	Description
	0	INT_PRIORITY	read- write	

#### 0x12040 S5\_CTRL\_VOLTAGE\_CTL1

**Type:** read-write Clock: PBUS WRCLK **Reset State:** 0x00 Reset Name: PERPH\_RB

PMIC\_GANGED

#### S5\_CTRL\_VOLTAGE\_CTL1

Bits	Name	Туре	Description
0	MV_RANGE	read- write	0 = Use low voltage range as specified by VSET and PFM_VOFFSET
			1 = Use medium voltage range as specified by VSET and PFM_VOFFSET

# 0x12041 S5\_CTRL\_VOLTAGE\_CTL2

Type: read-write Clock: PBUS\_WRCLK Reset State: 0xB4 Reset Name: PERPH\_RB

PMIC\_GANGED

### S5\_CTRL\_VOLTAGE\_CTL2

Bits	Name	Туре	Description
7:0	VSET	read- write	Output voltage set point in PWM mode and in PFM mode if the PFM_VOFFSET_EN bit is not asserted
		S	For MV_RANGE = 0: VSET => 0.005V * m + 0.080V, where m = <7:0> For MV_RANGE = 1: VSET => 0.010V * m + 0.160V, where m = <7:0> If PFM_VOFFSET_EN is asserted and in PFM mode, add PFM_VOFFSET

# 0x12042 S5\_CTRL\_VSET\_VALID

Type: read-only Clock: PBUS\_WRCLK Reset State: Undefined Reset Name: PERPH\_RB

#### S5\_CTRL\_VSET\_VALID

Bits	Name	Туре	Description
7:0	VSET_VALID	read- only	Readback the valid output voltage setpoint value

# 0x12044 S5\_CTRL\_VOLTAGE\_CTL3

Type: read-write
Clock: PBUS\_WRCLK
Reset State: 0x00

Reset Name: PERPH\_RB

# S5\_CTRL\_VOLTAGE\_CTL3

Bits	Name	Туре	Description
7	PFM_VOFFSET_EN	read- write	When in PFM mode  0 = Use VSET for output voltage set point  1 = Use VSET + PFM_VOFFSET for output voltage set point
1:0	PFM_VOFFSET	read- write	When in PFM mode and PFM_VOFFSET_EN is asserted, add a positive output voltage offset  For MV_RANGE = 0:  VOFFSET = 0.005V * 2 * m, where m = <1:0>  For MV_RANGE = 1:  VOFFSET = 0.010V * 2 * m, where m = <1:0>

# 0x12045 S5\_CTRL\_MODE\_CTL

Type: read-write Clock: PBUS\_WRCLK

Reset State: 0x80

Reset Name: PERPH\_RB

PMIC\_GANGED

### S5\_CTRL\_MODE\_CTL

Bits	Name	Type	Description
7	NPM	read- write	FTS NON-AUTO mode control 0 = Low power mode (LPM) unless AUTO_MODE is asserted 1 = Normal power mode (PWM)
6	AUTO_MODE	read- write	When asserted, FTS automatically enters and exits low power mode (PFM) based on load current qualifying triggers  0 = AUTO mode is disabled  1 = AUTO mode is enabled

# 0x12046 S5\_CTRL\_EN\_CTL

Type: read-write
Clock: PBUS\_WRCLK
Reset State: 0x00

Reset Name: PERPH\_RB

### S5\_CTRL\_EN\_CTL

Bits Name Type	Description
write 0 = Off	ble control
write 0 = Off 1 = On	

# 0x12048 S5\_CTRL\_PD\_CTL

Type: read-write Clock: PBUS\_WRCLK Reset State: 0x80 Reset Name: PERPH\_RB

### S5\_CTRL\_PD\_CTL

Bits	Name	Туре	Description
7	PD_EN	read- write	0 = Strong pulldown is always disabled 1 = Strong pulldown is enabled when the regulator is disabled
6	WEAK_PD_EN	read- write	0 = Weak pulldown is not enabled in OFF state 1 = Weak pulldown is enabled in OFF state
5	WEAK_PD_PFM	read- write	0 = Weak pulldown is not enabled in PFM mode 1 = Weak pulldown is enabled in PFM mode
4	WEAK_PD_PWM	read- write	0 = Weak pulldown is not enabled in PWM mode (and in HCPFM mode) 1 = Weak pulldown is enabled in PWM mode (and in HCPFM mode)

# 0x12054 S5\_CTRL\_PHASE\_CNT

Type: read-write Clock: PBUS\_WRCLK Reset State: 0x00 Reset Name: PERPH\_RB

### S5\_CTRL\_PHASE\_CNT

Bits	Name	Туре	Description
1:0	PHASE_CNT	read- write	When MULTIPHASE_EN is asserted, the number of operating phases is  00 = Number of operating phases is 1  01 = Number of operating phases is 2  10 = Number of operating phases is 4  11 = Number of operating phases is 4

# 0x12060 S5\_CTRL\_SS\_CTL

Type: read-write Clock: PBUS\_WRCLK Reset State: 0x00 Reset Name: PERPH\_RB

PMIC\_GANGED

# S5\_CTRL\_SS\_CTL

Bits	Name	Туре	Description
4:3	SS_STEP	read- write	Softstart voltage step size 00 = SS voltage step of 1 * LSB of VPROG
		V.	01 = SS voltage step of 2 * LSB
	7/13 10.	28.	10 = SS voltage step of 4 * LSB
	1,000	10	11 = SS voltage step of 8 * LSB
2:0	SS_DELAY	read- write	Softstart delay between steps = $2 \land (m + 3) / Fsys$ , where m = $<2:0> (Fsys = 19.2 MHz)$ :
			000 = 8-clock cycles (417ns)
			001 = 16-clock cycles
			010 = 32-clock cycles
			011 = 64-clock cycles
			100 = 128-clock cycles (6.67us)
			101 = 256-clock cycles
			110 = 512-clock cycles
			111 = 1024-clock cycles (53.3us)

#### 

Type: read-write Clock: PBUS\_WRCLK Reset State: 0x00 Reset Name: PERPH\_RB

### S5\_CTRL\_VS\_CTL

Bits	Name	Туре	Description
7	VS_EN	read-	Voltage stepping control
		write	0 = VS is disabled
			1 = VS is enabled
4:3	VS_STEP	read-	Voltage stepping voltage step size
		write	00 = VS voltage step of 1 * LSB of VPROG
			01 = VS voltage step of 2 * LSB
			10 = VS voltage step of 4 * LSB
			11 = VS voltage step of 8 * LSB
2:0	VS_DELAY	read-	Voltage stepping delay between steps = 2 ^ (m + 3) /
		write	Fsys, where m = <2:0> (Assuming Fsys = 19.2 MHz):
			Desired default is 1.67us
			000 = 8-clock cycles (417ns)
			001 = 16-clock cycles
			010 = 32-clock cycles
			011 = 64-clock cycles
			100 = 128-clock cycles (6.67us)
			101 = 256-clock cycles
		1	110 = 512-clock cycles
		~6°	111 = 1024-clock cycles (53.3us)

# 0x1206A S5\_CTRL\_ULS\_VALID

Type: read-only Clock: PBUS\_WRCLK

Reset State: Undefined
Reset Name: PERPH\_RB

### S5\_CTRL\_ULS\_VALID

Bits	Name	Туре	Description
7:0	ULS_VALID	read- only	Readback the valid upper limit stop value

# 0x1206C S5\_CTRL\_LLS\_VALID

**Type:** read-only

Clock: PBUS\_WRCLK
Reset State: Undefined
Reset Name: PERPH\_RB

# S5\_CTRL\_LLS\_VALID

Bits	Name	Туре	Description
7:0	LLS_VALID	read- only	Readback the valid lower limit stop value

# 8.13 S5\_PS\_FTS2\_PS

# 0x12104 S5\_PS\_PERPH\_TYPE

**Type:** read-only

Clock: PBUS\_WRCLK Reset State: 0x1C Reset Name: N/A

Peripheral Type

#### S5\_PS\_PERPH\_TYPE

Bits	Name	Туре	Description
7:0	TYPE	read- only	FTS2 Power Stage Reset State: 0x1C

#### 0x12105 S5 PS PERPH SUBTYPE

**Type:** read-only

Clock: PBUS\_WRCLK Reset State: 0x08 Reset Name: N/A

Peripheral SubType

#### S5\_PS\_PERPH\_SUBTYPE

Bits	Name	Туре	Description
7:0	SUBTYPE	read- only	

# 0x12140 S5\_PS\_VOLTAGE\_CTL1

Type: read-write Clock: PBUS\_WRCLK Reset State: 0x00

Reset Name: PERPH\_RB

### S5\_PS\_VOLTAGE\_CTL1

Bits	Name	Туре	Description
0	MV_RANGE	read- write	0 = Use low voltage range as specified by VSET and PFM_VOFFSET 1 = Use medium voltage range as specified by VSET and PFM_VOFFSET

# 0x12141 S5\_PS\_VOLTAGE\_CTL2

Type: read-write Clock: PBUS\_WRCLK Reset State: 0xB4 Reset Name: PERPH\_RB

PMIC\_GANGED

### S5\_PS\_VOLTAGE\_CTL2

Bits	Name	Type	Description
7:0	VSET	read- write	Output voltage set point in PWM mode and in PFM mode if the PFM_VOFFSET_EN bit is not asserted
		83.1	For MV_RANGE = 0:
			VSET => 0.005V * m + 0.080V, where $m = <7:0>$
	V. 3.	. 0	For MV_RANGE = 1:
	20.0		VSET => 0.010V * m + 0.160V, where m = <7:0>
	Co.	, 60	If PFM_VOFFSET_EN is asserted and in PFM mode, add PFM_VOFFSET

#### 

Type: read-write Clock: PBUS\_WRCLK Reset State: 0x00 Reset Name: PERPH\_RB

PMIC\_GANGED, PMIC\_SYNC=clk\_19p2:phase\_cnt\_rb

# S5\_PS\_PHASE\_CNT

Bits	Name	Туре	Description
1:0	PHASE_CNT	read- write	When MULTIPHASE_EN is asserted, the number of operating phases is  00 = Number of operating phases is 1  01 = Number of operating phases is 2  10 = Number of operating phases is 4  11 = Number of operating phases is 4

# 8.14 S5\_FREQ\_BCLK\_GEN\_CLK

# 0x12204 S5\_FREQ\_PERPH\_TYPE

**Type:** read-only

Clock: PBUS\_WRCLK Reset State: 0x1D Reset Name: N/A

Peripheral Type

# S5\_FREQ\_PERPH\_TYPE

Bits	Name	Туре	Description
7:0	TYPE	read- only	BCLK GEN

# 0x12205 S5\_FREQ\_PERPH\_SUBTYPE

**Type:** read-only

Clock: PBUS\_WRCLK Reset State: 0x09 Reset Name: N/A

Peripheral SubType

#### S5\_FREQ\_PERPH\_SUBTYPE

Bits	Name	Туре	Description
7:0	SUBTYPE	read- only	BCLK GEN CLK

# 0x12246 S5\_FREQ\_CLK\_ENABLE

Type: read-write Clock: PBUS\_WRCLK Reset State: 0x01

Reset Name: PERPH\_RB

#### S5\_FREQ\_CLK\_ENABLE

Bits	Name	Type	Description
7	EN_CLK_INT	read- write	0 = do not force the clock on 1 = enable the clock
0	FOLLOW_CLK_SX_REQ	read- write	0 = ignore smps_clk_req <x> 1 = clock is enabled when the clocks request is high smps_clk_req<x>='1'</x></x>

### 0x12250 S5\_FREQ\_CLK\_DIV

Type: read-write Clock: PBUS\_WRCLK Reset State: 0x02 Reset Name: PERPH\_RB

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PMIC\_GANGED

### S5\_FREQ\_CLK\_DIV

Bits	Name	Туре	Description
3:0	CLK_DIV	read- write	clock_ frequency = 19.2MHz / (CLK_DIV + 1) FTS2 Buck supports 3.2, 4.8, 6.4 and 9.6 MHz HF2 Buck supports 1.6, 2.4, 2.74, 3.2, 3.8, 4.8, and 6.4 MHz CLK_DIV = 0 is not supported, it will generate 9.6 MHz

# 0x12251 S5\_FREQ\_CLK\_PHASE

Type: read-write Clock: PBUS\_WRCLK Reset State: 0x00 Reset Name: PERPH\_RB

### S5\_FREQ\_CLK\_PHASE

Bits	Name	Туре	Description
3:0	CLK_PHASE	read- write	Distributed clock phase select: clock phase delay = clock period * (CLK_PHASE / 16)

# 0x122C0 S5\_FREQ\_GANG\_CTL1

**Type:** read-write **Clock:** PBUS\_WRCLK **Reset State:** 0x20

**Reset Name:** PERPH\_RB

#### S5\_FREQ\_GANG\_CTL1

Bits	Name	Туре	Description
7:0	GANG_LEADER_PID	read- write	When GANG_EN (GANG_CTL2[7]) is set, this peripheral will write the same data that is written to the gang leader Peripheral ID. Reads to the gang leader Peripheral ID are ignored by this peripheral. Ganged peripherals must reside within the same Slave ID

# 0x122C1 S5\_FREQ\_GANG\_CTL2

Type: read-write Clock: PBUS\_WRCLK Reset State: 0x80 Reset Name: PERPH\_RB

### S5\_FREQ\_GANG\_CTL2

Bits	Name	Туре	Description
7	GANG_EN	read- write	0 = disable 1 = enable When enabled, this peripheral will write the same data that is written to the gang leader PID. Reads to the gang leader PID are ignored by this peripheral

# 8.15 S6\_CTRL\_FTS2\_CTRL

# 0x12304 S6\_CTRL\_PERPH\_TYPE

**Type:** read-only

Clock: PBUS\_WRCLK Reset State: 0x03 Reset Name: N/A

Peripheral Type

#### S6\_CTRL\_PERPH\_TYPE

Bits	Name	Туре	Description
7:0	TYPE	read- only	FTS2 Control Reset State: 0x03

# 0x12305 S6\_CTRL\_PERPH\_SUBTYPE

**Type:** read-only

Clock: PBUS\_WRCLK Reset State: 0x08 Reset Name: N/A

Peripheral SubType

#### S6\_CTRL\_PERPH\_SUBTYPE

Bits	Name	Туре	Description
7:0	SUBTYPE	read- only	

# 0x12308 S6\_CTRL\_STATUS\_1

**Type:** read-only

Clock: PBUS\_WRCLK Reset State: Undefined Reset Name: N/A

Status Registers

#### S6\_CTRL\_STATUS\_1

Bits	Name	Туре	Description
7	VREG_OK_FLAG	read- only	Indicates that VREG_SNS has reached a value that is greater than or equal to the threshold of the comparator tasked for VREG_SNS monitoring

# S6\_CTRL\_STATUS\_1 (Continued)

Bits	Name	Туре	Description
6	VREG_FAULT_FLAG	read- only	Indicates a probable short circuit condition at VREG_SNS since VREG_SNS is below the VREG fault voltage level and the softstart ramp is done. Current limit foldback is in use.
1	NPM_FLAG	read- only	Indicates normal power mode is in use
0	STEPPER_DONE_FLAG	read- only	Softstart stepper and voltage stepper done

# 0x12309 S6\_CTRL\_STATUS\_2

**Type:** read-only

Clock: PBUS\_WRCLK
Reset State: Undefined
Reset Name: N/A

Status Registers

# S6\_CTRL\_STATUS\_2

Bits	Name	Туре	Description
4	ILS_FLAG	read- only	Either of the following:  => Both limit stops have been enabled, but the upper limit stop VSET_ULS has been programmed to a value below the lower limit stop VSET_LLS  => Both limit stops have been enabled, but the lower limit stop VSET_LLS has been programmed to a value above the upper limit stop VSET_ULS
3	ULS_FLAG	read- only	Indicates that the voltage setpoint has been programmed to a value that is greater than or equal to the upper limit stop VSET_ULS
2	LLS_FLAG	read- only	Indicates that the voltage setpoint has been programmed to a value that is less than or equal to the lower limit stop VSET_LLS
1	GPL_HI_FLAG	read- only	Indicates that the voltage setpoint has reached a value that is greater than or equal to the high general purpose limit VSET_GPL_HI
0	GPL_LO_FLAG	read- only	Indicates that the voltage setpoint has reached a value that is less than or equal to the low general purpose limit VSET_GPL_LO

## 0x12310 S6\_CTRL\_INT\_RT\_STS

**Type:** read-only

Clock: PBUS\_WRCLK Reset State: Undefined Reset Name: PERPH\_RB

**Interrupt Real Time Status Bits** 

#### S6\_CTRL\_INT\_RT\_STS

Bits	Name	Туре	Description
2	VREG_FAULT_INT	read- only	
1	LIMIT_ERR_INT	read- only	
0	VREG_OK_INT	read- only	.51

# 0x12311 S6\_CTRL\_INT\_SET\_TYPE

Type: read-write Clock: PBUS\_WRCLK Reset State: 0x00 Reset Name: PERPH\_RB

0 =use level trigger interrupts, 1 =use edge trigger interrupts

### S6 CTRL INT SET TYPE

Bits	Name	Туре	Description
2	VREG_FAULT_INT	read- write	
1	LIMIT_ERR_INT	read- write	
0	VREG_OK_INT	read- write	

### 0x12312 S6\_CTRL\_INT\_POLARITY\_HIGH

Type: read-write Clock: PBUS\_WRCLK Reset State: 0x00 Reset Name: PERPH\_RB

1= Interrupt will trigger on a level high (rising edge) event, 0 = level high triggering is disabled

### **S6\_CTRL\_INT\_POLARITY\_HIGH**

Bits	Name	Туре	Description
2	VREG_FAULT_INT	read- write	
1	LIMIT_ERR_INT	read- write	
0	VREG_OK_INT	read- write	

### 0x12313 S6\_CTRL\_INT\_POLARITY\_LOW

Type: read-write Clock: PBUS\_WRCLK Reset State: 0x00

Reset Name: PERPH\_RB

1' = Interrupt will trigger on a level low (falling edge) event, '0' = level low triggering is disabled

### S6\_CTRL\_INT\_POLARITY\_LOW

Bits	Name	Туре	Description
2	VREG_FAULT_INT	read- write	70.
1	LIMIT_ERR_INT	read- write	0,00
0	VREG_OK_INT	read- write	

### 0x12314 S6\_CTRL\_INT\_LATCHED\_CLR

Type: write-only Clock: PBUS\_WRCLK Reset State: 0x00 Reset Name: PERPH\_RB

Writing a '1' to this interrupt will rearm the interrupt when an interrupt is pending. It clears the

internal sticky and sent bits

### S6\_CTRL\_INT\_LATCHED\_CLR

Bits	Name	Туре	Description
2	VREG_FAULT_INT	write- only	

#### S6\_CTRL\_INT\_LATCHED\_CLR (Continued)

Bits	Name	Туре	Description
1	LIMIT_ERR_INT	write- only	
0	VREG_OK_INT	write- only	

### 0x12315 S6\_CTRL\_INT\_EN\_SET

Type: read-write Clock: PBUS\_WRCLK Reset State: 0x00 Reset Name: PERPH\_RB

Writing '0' to this register has no effect. Writing a '1' will enable the corresponding interrupt. Reading this register will readback enable status

PMIC\_SET\_MASK

### S6\_CTRL\_INT\_EN\_SET

Bits	Name	Туре	Description
2	VREG_FAULT_INT	read- write	9. <sup>1</sup>
1	LIMIT_ERR_INT	read- write	
0	VREG_OK_INT	read- write	

## 0x12316 S6\_CTRL\_INT\_EN\_CLR

Type: read-write Clock: PBUS\_WRCLK Reset State: 0x00 Reset Name: PERPH\_RB

Writing '0' to this register has no effect. Writing a '1' will disable the corresponding interrupt. Reading this register will readback enable status

PMIC\_CLR\_MASK=INT\_EN\_SET

#### S6\_CTRL\_INT\_EN\_CLR

Bits	Name	Туре	Description
2	VREG_FAULT_INT	read- write	

### S6\_CTRL\_INT\_EN\_CLR (Continued)

Bits	Name	Туре	Description
1	LIMIT_ERR_INT	read- write	
0	VREG_OK_INT	read- write	

## 0x12318 S6\_CTRL\_INT\_LATCHED\_STS

Type: read-only Clock: PBUS\_WRCLK Reset State: 0x00 Reset Name: PERPH\_RB

Debug: Latched (Sticky) Interrupt. '1' indicates that the interrupt has triggered. Once the latched bit is set it can only be cleared by writing the clear bit.

### S6\_CTRL\_INT\_LATCHED\_STS

Bits	Name	Туре	Description
2	VREG_FAULT_INT	read- only	This No
1	LIMIT_ERR_INT	read- only	720.
0	VREG_OK_INT	read- only	0,90

# 0x12319 S6\_CTRL\_INT\_PENDING\_STS

Type: read-only Clock: PBUS\_WRCLK Reset State: 0x00 Reset Name: PERPH RB

Debug: Pending is set if interrupt has been sent but not cleared.

#### S6\_CTRL\_INT\_PENDING\_STS

Bits	Name	Type	Description
2	VREG_FAULT_INT	read- only	
1	LIMIT_ERR_INT	read- only	
0	VREG_OK_INT	read- only	

#### 0x1231A S6\_CTRL\_INT\_MID\_SEL

**Type:** read-write Clock: PBUS\_WRCLK **Reset State:** 0x00 Reset Name: PERPH\_RB

Selects the MID that will receive the interrupt

## S6\_CTRL\_INT\_MID\_SEL

Bits	Name	Туре	Description
1:0	INT_MID_SEL	read- write	-

#### 0x1231B **S6 CTRL INT PRIORITY**

**Type:** read-write Clock: PBUS\_WRCLK Reset State: 0x00

Reset Name: PERPH\_RB

SR=0 A=1

#### S6\_CTRL\_INT\_PRIORITY

В	its	Name	Туре	Description
	0	INT_PRIORITY	read- write	

#### 0x12340 S6\_CTRL\_VOLTAGE\_CTL1

**Type:** read-write Clock: PBUS WRCLK **Reset State:** 0x00 Reset Name: PERPH\_RB

PMIC\_GANGED

#### S6\_CTRL\_VOLTAGE\_CTL1

Bits	Name	Туре	Description
0	MV_RANGE	read- write	0 = Use low voltage range as specified by VSET and PFM_VOFFSET
			1 = Use medium voltage range as specified by VSET and PFM_VOFFSET

## 0x12341 S6\_CTRL\_VOLTAGE\_CTL2

Type: read-write Clock: PBUS\_WRCLK Reset State: 0xB4 Reset Name: PERPH\_RB

PMIC\_GANGED

## S6\_CTRL\_VOLTAGE\_CTL2

Bits	Name	Туре	Description
7:0	VSET	read- write	Output voltage set point in PWM mode and in PFM mode if the PFM_VOFFSET_EN bit is not asserted
		S	For MV_RANGE = 0: VSET => 0.005V * m + 0.080V, where m = <7:0> For MV_RANGE = 1: VSET => 0.010V * m + 0.160V, where m = <7:0> If PFM_VOFFSET_EN is asserted and in PFM mode, add PFM_VOFFSET

## 0x12342 S6\_CTRL\_VSET\_VALID

Type: read-only Clock: PBUS\_WRCLK Reset State: Undefined Reset Name: PERPH\_RB

## S6\_CTRL\_VSET\_VALID

Bits	Name	Туре	Description
7:0	VSET_VALID	read- only	Readback the valid output voltage setpoint value

## 0x12344 S6\_CTRL\_VOLTAGE\_CTL3

**Type:** read-write **Clock:** PBUS\_WRCLK **Reset State:** 0x00

Reset Name: PERPH\_RB

## S6\_CTRL\_VOLTAGE\_CTL3

Bits	Name	Туре	Description
7	PFM_VOFFSET_EN	read- write	When in PFM mode  0 = Use VSET for output voltage set point  1 = Use VSET + PFM_VOFFSET for output voltage set point
1:0	PFM_VOFFSET	read- write	When in PFM mode and PFM_VOFFSET_EN is asserted, add a positive output voltage offset  For MV_RANGE = 0:  VOFFSET = 0.005V * 2 * m, where m = <1:0>  For MV_RANGE = 1:  VOFFSET = 0.010V * 2 * m, where m = <1:0>

## 0x12345 S6\_CTRL\_MODE\_CTL

Type: read-write Clock: PBUS\_WRCLK Reset State: 0x80

Reset Name: PERPH\_RB

PMIC\_GANGED

## S6\_CTRL\_MODE\_CTL

Bits	Name	Type	Description
7	NPM	read- write	FTS NON-AUTO mode control 0 = Low power mode (LPM) unless AUTO_MODE is asserted 1 = Normal power mode (PWM)
6	AUTO_MODE	read- write	When asserted, FTS automatically enters and exits low power mode (PFM) based on load current qualifying triggers  0 = AUTO mode is disabled  1 = AUTO mode is enabled

## 0x12346 S6\_CTRL\_EN\_CTL

Type: read-write Clock: PBUS\_WRCLK Reset State: 0x00 Reset Name: PERPH\_RB

## S6\_CTRL\_EN\_CTL

Bits Name Type	Description
write 0 = Off	ble control
write 0 = Off 1 = On	

## 0x12348 S6\_CTRL\_PD\_CTL

Type: read-write Clock: PBUS\_WRCLK Reset State: 0x00 Reset Name: PERPH\_RB

## S6\_CTRL\_PD\_CTL

Bits	Name	Туре	Description
7	PD_EN	read- write	0 = Strong pulldown is always disabled 1 = Strong pulldown is enabled when the regulator is disabled
6	WEAK_PD_EN	read- write	0 = Weak pulldown is not enabled in OFF state 1 = Weak pulldown is enabled in OFF state
5	WEAK_PD_PFM	read- write	0 = Weak pulldown is not enabled in PFM mode 1 = Weak pulldown is enabled in PFM mode
4	WEAK_PD_PWM	read- write	0 = Weak pulldown is not enabled in PWM mode (and in HCPFM mode) 1 = Weak pulldown is enabled in PWM mode (and in HCPFM mode)

## 0x12354 S6\_CTRL\_PHASE\_CNT

Type: read-write Clock: PBUS\_WRCLK Reset State: 0x00

Reset Name: PERPH\_RB

## S6\_CTRL\_PHASE\_CNT

Bits	Name	Туре	Description
1:0	PHASE_CNT	read- write	When MULTIPHASE_EN is asserted, the number of operating phases is  00 = Number of operating phases is 1  01 = Number of operating phases is 2  10 = Number of operating phases is 4  11 = Number of operating phases is 4

#### 

Type: read-write Clock: PBUS\_WRCLK Reset State: 0x00 Reset Name: PERPH\_RB

PMIC\_GANGED

## S6\_CTRL\_SS\_CTL

Bits	Name	Туре	Description
4:3	SS_STEP	read- write	Softstart voltage step size  00 = SS voltage step of 1 * LSB of VPROG  01 = SS voltage step of 2 * LSB  10 = SS voltage step of 4 * LSB  11 = SS voltage step of 8 * LSB
2:0	SS_DELAY	read- write	Softstart delay between steps = 2 ^ (m + 3) / Fsys, where m = <2:0> (Fsys = 19.2 MHz):  000 = 8-clock cycles (417ns)  001 = 16-clock cycles  010 = 32-clock cycles  011 = 64-clock cycles  100 = 128-clock cycles (6.67us)  101 = 256-clock cycles  110 = 512-clock cycles  111 = 1024-clock cycles (53.3us)

#### 

Type: read-write
Clock: PBUS\_WRCLK
Reset State: 0x00
Reset Name: PERBLI P

Reset Name: PERPH\_RB

## S6\_CTRL\_VS\_CTL

Bits	Name	Туре	Description
7	VS_EN	read-	Voltage stepping control
		write	0 = VS is disabled
			1 = VS is enabled
4:3	VS_STEP	read-	Voltage stepping voltage step size
		write	00 = VS voltage step of 1 * LSB of VPROG
			01 = VS voltage step of 2 * LSB
			10 = VS voltage step of 4 * LSB
			11 = VS voltage step of 8 * LSB
2:0	VS_DELAY	read-	Voltage stepping delay between steps = 2 ^ (m + 3) /
		write	Fsys, where m = <2:0> (Assuming Fsys = 19.2 MHz):
			Desired default is 1.67us
			000 = 8-clock cycles (417ns)
			001 = 16-clock cycles
			010 = 32-clock cycles
			011 = 64-clock cycles
			100 = 128-clock cycles (6.67us)
			101 = 256-clock cycles
		1	110 = 512-clock cycles
		~6°	111 = 1024-clock cycles (53.3us)

# 0x1236A S6\_CTRL\_ULS\_VALID

**Type:** read-only

Clock: PBUS\_WRCLK
Reset State: Undefined
Reset Name: PERPH\_RB

## S6\_CTRL\_ULS\_VALID

Bits	Name	Туре	Description
7:0	ULS_VALID	read- only	Readback the valid upper limit stop value

## 0x1236C S6\_CTRL\_LLS\_VALID

**Type:** read-only

Clock: PBUS\_WRCLK
Reset State: Undefined
Reset Name: PERPH\_RB

## S6\_CTRL\_LLS\_VALID

Bits	Name	Туре	Description
7:0	LLS_VALID	read- only	Readback the valid lower limit stop value

# 8.16 S6\_PS\_FTS2\_PS

## 0x12404 S6\_PS\_PERPH\_TYPE

**Type:** read-only

Clock: PBUS\_WRCLK Reset State: 0x1C Reset Name: N/A

Peripheral Type

#### S6\_PS\_PERPH\_TYPE

Bits	Name	Туре	Description
7:0	TYPE	read- only	FTS2 Power Stage Reset State: 0x1C

## 0x12405 S6\_PS\_PERPH\_SUBTYPE

**Type:** read-only

Clock: PBUS\_WRCLK Reset State: 0x08 Reset Name: N/A

Peripheral SubType

## S6\_PS\_PERPH\_SUBTYPE

Bits	Name	Type	Description
7:0	SUBTYPE	read- only	

## 0x12440 S6\_PS\_VOLTAGE\_CTL1

Type: read-write
Clock: PBUS\_WRCLK
Reset State: 0x00

Reset Name: PERPH\_RB

## S6\_PS\_VOLTAGE\_CTL1

Bits	Name	Туре	Description
0	MV_RANGE	read- write	0 = Use low voltage range as specified by VSET and PFM_VOFFSET 1 = Use medium voltage range as specified by VSET and PFM_VOFFSET

## 0x12441 S6\_PS\_VOLTAGE\_CTL2

Type: read-write
Clock: PBUS\_WRCLK
Reset State: 0xB4
Perset Name: PERPH PE

**Reset Name:** PERPH\_RB

PMIC\_GANGED

## S6\_PS\_VOLTAGE\_CTL2

Bits	Name	Type	Description
7:0	VSET	read- write	Output voltage set point in PWM mode and in PFM mode if the PFM_VOFFSET_EN bit is not asserted
		80.	For MV_RANGE = 0:
			VSET => 0.005V * m + 0.080V, where $m = <7:0>$
	V, 2.	.0	For MV_RANGE = 1:
	20.		VSET => 0.010V * m + 0.160V, where m = <7:0>
	Mar	69	If PFM_VOFFSET_EN is asserted and in PFM mode, add PFM_VOFFSET

## 0x12454 S6\_PS\_PHASE\_CNT

Type: read-write Clock: PBUS\_WRCLK Reset State: 0x00 Reset Name: PERPH\_RB

Reset Numer 1 ERI 11\_RD

 $PMIC\_GANGED, PMIC\_SYNC = clk\_19p2: phase\_cnt\_rb$ 

## S6\_PS\_PHASE\_CNT

Bits	Name	Туре	Description
1:0	PHASE_CNT	read- write	When MULTIPHASE_EN is asserted, the number of operating phases is  00 = Number of operating phases is 1  01 = Number of operating phases is 2  10 = Number of operating phases is 4  11 = Number of operating phases is 4

# 8.17 S6\_FREQ\_BCLK\_GEN\_CLK

## 0x12504 S6\_FREQ\_PERPH\_TYPE

**Type:** read-only

Clock: PBUS\_WRCLK Reset State: 0x1D Reset Name: N/A

Peripheral Type

## S6\_FREQ\_PERPH\_TYPE

Bi	its	Name	Туре	Description
7:	':0	TYPE	read- only	BCLK GEN

## 0x12505 S6\_FREQ\_PERPH\_SUBTYPE

**Type:** read-only

Clock: PBUS\_WRCLK Reset State: 0x09 Reset Name: N/A

Peripheral SubType

#### S6\_FREQ\_PERPH\_SUBTYPE

Bits	Name	Туре	Description
7:0	SUBTYPE	read- only	BCLK GEN CLK

## 0x12546 S6\_FREQ\_CLK\_ENABLE

Type: read-write Clock: PBUS\_WRCLK Reset State: 0x01

**Reset Name:** PERPH\_RB

#### S6\_FREQ\_CLK\_ENABLE

Bits	Name	Туре	Description
7	EN_CLK_INT	read- write	0 = do not force the clock on 1 = enable the clock
0	FOLLOW_CLK_SX_REQ	read- write	0 = ignore smps_clk_req <x> 1 = clock is enabled when the clocks request is high smps_clk_req<x>='1'</x></x>

## 0x12550 S6\_FREQ\_CLK\_DIV

Type: read-write Clock: PBUS\_WRCLK Reset State: 0x02 Reset Name: PERPH\_RB

PMIC\_GANGED

## S6\_FREQ\_CLK\_DIV

Bits	Name	Туре	Description
3:0	CLK_DIV	read- write	clock_ frequency = 19.2MHz / (CLK_DIV + 1) FTS2 Buck supports 3.2, 4.8, 6.4 and 9.6 MHz HF2 Buck supports 1.6, 2.4, 2.74, 3.2, 3.8, 4.8, and 6.4 MHz CLK_DIV = 0 is not supported, it will generate 9.6 MHz

## 0x12551 S6\_FREQ\_CLK\_PHASE

Type: read-write Clock: PBUS\_WRCLK Reset State: 0x04 Reset Name: PERPH\_RB

## S6\_FREQ\_CLK\_PHASE

Bits	Name	Туре	Description
3:0	CLK_PHASE	read- write	Distributed clock phase select: clock phase delay = clock period * (CLK_PHASE / 16)

## 0x125C0 S6\_FREQ\_GANG\_CTL1

Type: read-write Clock: PBUS\_WRCLK Reset State: 0x20

Reset Name: PERPH\_RB

#### S6\_FREQ\_GANG\_CTL1

Bits	Name	Туре	Description
7:0	GANG_LEADER_PID	read- write	When GANG_EN (GANG_CTL2[7]) is set, this peripheral will write the same data that is written to the gang leader Peripheral ID. Reads to the gang leader Peripheral ID are ignored by this peripheral. Ganged peripherals must reside within the same Slave ID

## 0x125C1 S6\_FREQ\_GANG\_CTL2

Type: read-write Clock: PBUS\_WRCLK Reset State: 0x80 Reset Name: PERPH\_RB

## S6\_FREQ\_GANG\_CTL2

Bits	Name	Туре	Description
7	GANG_EN	read- write	0 = disable 1 = enable When enabled, this peripheral will write the same data that is written to the gang leader PID. Reads to the gang leader PID are ignored by this peripheral

# 8.18 S7\_CTRL\_FTS2\_CTRL

## 0x12604 S7\_CTRL\_PERPH\_TYPE

**Type:** read-only

Clock: PBUS\_WRCLK Reset State: 0x03 Reset Name: N/A

Peripheral Type

#### S7\_CTRL\_PERPH\_TYPE

Bits	Name	Туре	Description
7:0	TYPE	read- only	FTS2 Control Reset State: 0x03

## 0x12605 S7\_CTRL\_PERPH\_SUBTYPE

**Type:** read-only

Clock: PBUS\_WRCLK Reset State: 0x08 Reset Name: N/A

Peripheral SubType

#### S7\_CTRL\_PERPH\_SUBTYPE

Bits	Name	Туре	Description
7:0	SUBTYPE	read- only	

## 0x12608 S7\_CTRL\_STATUS\_1

**Type:** read-only

Clock: PBUS\_WRCLK Reset State: Undefined Reset Name: N/A

Status Registers

#### S7\_CTRL\_STATUS\_1

Bits	Name	Туре	Description
7	VREG_OK_FLAG	read- only	Indicates that VREG_SNS has reached a value that is greater than or equal to the threshold of the comparator tasked for VREG_SNS monitoring

## S7\_CTRL\_STATUS\_1 (Continued)

Bits	Name	Туре	Description
6	VREG_FAULT_FLAG	read- only	Indicates a probable short circuit condition at VREG_SNS since VREG_SNS is below the VREG fault voltage level and the softstart ramp is done. Current limit foldback is in use.
1	NPM_FLAG	read- only	Indicates normal power mode is in use
0	STEPPER_DONE_FLAG	read- only	Softstart stepper and voltage stepper done

## 0x12609 S7\_CTRL\_STATUS\_2

**Type:** read-only

Clock: PBUS\_WRCLK
Reset State: Undefined
Reset Name: N/A

Status Registers

## S7\_CTRL\_STATUS\_2

Bits	Name	Туре	Description
4	ILS_FLAG	read- only	Either of the following:  => Both limit stops have been enabled, but the upper limit stop VSET_ULS has been programmed to a value below the lower limit stop VSET_LLS  => Both limit stops have been enabled, but the lower limit stop VSET_LLS has been programmed to a value above the upper limit stop VSET_ULS
3	ULS_FLAG	read- only	Indicates that the voltage setpoint has been programmed to a value that is greater than or equal to the upper limit stop VSET_ULS
2	LLS_FLAG	read- only	Indicates that the voltage setpoint has been programmed to a value that is less than or equal to the lower limit stop VSET_LLS
1	GPL_HI_FLAG	read- only	Indicates that the voltage setpoint has reached a value that is greater than or equal to the high general purpose limit VSET_GPL_HI
0	GPL_LO_FLAG	read- only	Indicates that the voltage setpoint has reached a value that is less than or equal to the low general purpose limit VSET_GPL_LO

## 0x12610 S7\_CTRL\_INT\_RT\_STS

**Type:** read-only

Clock: PBUS\_WRCLK Reset State: Undefined Reset Name: PERPH\_RB

**Interrupt Real Time Status Bits** 

#### S7\_CTRL\_INT\_RT\_STS

Bits	Name	Туре	Description
2	VREG_FAULT_INT	read- only	
1	LIMIT_ERR_INT	read- only	
0	VREG_OK_INT	read- only	.51

## 0x12611 S7\_CTRL\_INT\_SET\_TYPE

Type: read-write Clock: PBUS\_WRCLK Reset State: 0x00

Reset Name: PERPH\_RB

0 =use level trigger interrupts, 1 =use edge trigger interrupts

## S7 CTRL INT SET TYPE

Bits	Name	Туре	Description
2	VREG_FAULT_INT	read- write	
1	LIMIT_ERR_INT	read- write	
0	VREG_OK_INT	read- write	

## 0x12612 S7\_CTRL\_INT\_POLARITY\_HIGH

Type: read-write Clock: PBUS\_WRCLK Reset State: 0x00 Reset Name: PERPH\_RB

1= Interrupt will trigger on a level high (rising edge) event, 0 = level high triggering is disabled

## S7\_CTRL\_INT\_POLARITY\_HIGH

Bits	Name	Туре	Description
2	VREG_FAULT_INT	read- write	
1	LIMIT_ERR_INT	read- write	
0	VREG_OK_INT	read- write	

## 0x12613 S7\_CTRL\_INT\_POLARITY\_LOW

Type: read-write Clock: PBUS\_WRCLK Reset State: 0x00 Reset Name: PERPH\_RB

1' = Interrupt will trigger on a level low (falling edge) event, '0' = level low triggering is disabled

## S7\_CTRL\_INT\_POLARITY\_LOW

Bits	Name	Туре	Description
2	VREG_FAULT_INT	read- write	1,70.
1	LIMIT_ERR_INT	read- write	0,90
0	VREG_OK_INT	read- write	

## 0x12614 S7\_CTRL\_INT\_LATCHED\_CLR

Type: write-only Clock: PBUS\_WRCLK Reset State: 0x00 Reset Name: PERPH\_RB

Writing a '1' to this interrupt will rearm the interrupt when an interrupt is pending. It clears the

internal sticky and sent bits

## S7\_CTRL\_INT\_LATCHED\_CLR

Bits	Name	Туре	Description
2	VREG_FAULT_INT	write- only	

## S7\_CTRL\_INT\_LATCHED\_CLR (Continued)

Bits	Name	Туре	Description
1	LIMIT_ERR_INT	write- only	
0	VREG_OK_INT	write- only	

## 0x12615 S7\_CTRL\_INT\_EN\_SET

Type: read-write Clock: PBUS\_WRCLK Reset State: 0x00 Reset Name: PERPH\_RB

Writing '0' to this register has no effect. Writing a '1' will enable the corresponding interrupt. Reading this register will readback enable status

PMIC\_SET\_MASK

## S7\_CTRL\_INT\_EN\_SET

Bits	Name	Туре	Description
2	VREG_FAULT_INT	read- write	9.J.
1	LIMIT_ERR_INT	read- write	
0	VREG_OK_INT	read- write	

## 0x12616 S7\_CTRL\_INT\_EN\_CLR

Type: read-write Clock: PBUS\_WRCLK Reset State: 0x00 Reset Name: PERPH RB

Writing '0' to this register has no effect. Writing a '1' will disable the corresponding interrupt. Reading this register will readback enable status

PMIC\_CLR\_MASK=INT\_EN\_SET

#### S7\_CTRL\_INT\_EN\_CLR

Bits	Name	Туре	Description
2	VREG_FAULT_INT	read- write	

## S7\_CTRL\_INT\_EN\_CLR (Continued)

Bits	Name	Туре	Description
1	LIMIT_ERR_INT	read- write	
0	VREG_OK_INT	read- write	

## 0x12618 S7\_CTRL\_INT\_LATCHED\_STS

Type: read-only Clock: PBUS\_WRCLK Reset State: 0x00 Reset Name: PERPH\_RB

Debug: Latched (Sticky) Interrupt. '1' indicates that the interrupt has triggered. Once the latched bit is set it can only be cleared by writing the clear bit.

## S7\_CTRL\_INT\_LATCHED\_STS

Bits	Name	Туре	Description
2	VREG_FAULT_INT	read- only	July 210
1	LIMIT_ERR_INT	read- only	120.
0	VREG_OK_INT	read- only	020.

## 0x12619 S7\_CTRL\_INT\_PENDING\_STS

Type: read-only Clock: PBUS\_WRCLK Reset State: 0x00 Reset Name: PERPH\_RB

Debug: Pending is set if interrupt has been sent but not cleared.

#### S7\_CTRL\_INT\_PENDING\_STS

Bits	Name	Type	Description
2	VREG_FAULT_INT	read- only	
1	LIMIT_ERR_INT	read- only	
0	VREG_OK_INT	read- only	

## 0x1261A S7\_CTRL\_INT\_MID\_SEL

Type: read-write Clock: PBUS\_WRCLK Reset State: 0x00 Reset Name: PERPH\_RB

Selects the MID that will receive the interrupt

## S7\_CTRL\_INT\_MID\_SEL

Bits	Name	Туре	Description
1:0	INT_MID_SEL	read- write	-

## 0x1261B S7\_CTRL\_INT\_PRIORITY

Type: read-write Clock: PBUS\_WRCLK Reset State: 0x00

Reset Name: PERPH\_RB

SR = 0 A = 1

#### S7\_CTRL\_INT\_PRIORITY

В	its	Name	Туре	Description
	0	INT_PRIORITY	read- write	

## 0x12640 S7\_CTRL\_VOLTAGE\_CTL1

Type: read-write Clock: PBUS\_WRCLK Reset State: 0x00 Reset Name: PERPH\_RB

PMIC\_GANGED

#### S7\_CTRL\_VOLTAGE\_CTL1

Bits	Name	Туре	Description
0	MV_RANGE	read- write	0 = Use low voltage range as specified by VSET and PFM_VOFFSET
			1 = Use medium voltage range as specified by VSET and PFM_VOFFSET

## 0x12641 S7\_CTRL\_VOLTAGE\_CTL2

Type: read-write Clock: PBUS\_WRCLK Reset State: 0xB4 Reset Name: PERPH\_RB

PMIC\_GANGED

## S7\_CTRL\_VOLTAGE\_CTL2

Bits	Name	Туре	Description
7:0	VSET	read- write	Output voltage set point in PWM mode and in PFM mode if the PFM_VOFFSET_EN bit is not asserted
		S	For MV_RANGE = 0: VSET => 0.005V * m + 0.080V, where m = <7:0> For MV_RANGE = 1: VSET => 0.010V * m + 0.160V, where m = <7:0> If PFM_VOFFSET_EN is asserted and in PFM mode, add PFM_VOFFSET

## 0x12642 S7\_CTRL\_VSET\_VALID

Type: read-only Clock: PBUS\_WRCLK Reset State: Undefined Reset Name: PERPH\_RB

#### S7\_CTRL\_VSET\_VALID

Bits	Name	Туре	Description
7:0	VSET_VALID	read- only	Readback the valid output voltage setpoint value

## 0x12644 S7\_CTRL\_VOLTAGE\_CTL3

Type: read-write Clock: PBUS\_WRCLK Reset State: 0x00

Reset Name: PERPH\_RB

## S7\_CTRL\_VOLTAGE\_CTL3

Bits	Name	Туре	Description
7	PFM_VOFFSET_EN	read- write	When in PFM mode  0 = Use VSET for output voltage set point  1 = Use VSET + PFM_VOFFSET for output voltage set point
1:0	PFM_VOFFSET	read- write	When in PFM mode and PFM_VOFFSET_EN is asserted, add a positive output voltage offset  For MV_RANGE = 0:  VOFFSET = 0.005V * 2 * m, where m = <1:0>  For MV_RANGE = 1:  VOFFSET = 0.010V * 2 * m, where m = <1:0>

## 0x12645 S7\_CTRL\_MODE\_CTL

Type: read-write Clock: PBUS\_WRCLK Reset State: 0x80

Reset Name: PERPH\_RB

PMIC\_GANGED

## S7\_CTRL\_MODE\_CTL

Bits	Name	Type	Description
7	NPM	read- write	FTS NON-AUTO mode control 0 = Low power mode (LPM) unless AUTO_MODE is asserted 1 = Normal power mode (PWM)
6	AUTO_MODE	read- write	When asserted, FTS automatically enters and exits low power mode (PFM) based on load current qualifying triggers  0 = AUTO mode is disabled  1 = AUTO mode is enabled

## 0x12646 S7\_CTRL\_EN\_CTL

Type: read-write
Clock: PBUS\_WRCLK
Reset State: 0x00

Reset Name: PERPH\_RB

## S7\_CTRL\_EN\_CTL

Bits	Name	Туре	Description
7	PERPH_EN	read- write	FTS enable control 0 = Off 1 = On

## 0x12648 S7\_CTRL\_PD\_CTL

Type: read-write Clock: PBUS\_WRCLK Reset State: 0x00

Reset Name: PERPH\_RB

## S7\_CTRL\_PD\_CTL

Bits	Name	Туре	Description
7	PD_EN	read- write	0 = Strong pulldown is always disabled 1 = Strong pulldown is enabled when the regulator is disabled
6	WEAK_PD_EN	read- write	0 = Weak pulldown is not enabled in OFF state 1 = Weak pulldown is enabled in OFF state
5	WEAK_PD_PFM	read- write	0 = Weak pulldown is not enabled in PFM mode 1 = Weak pulldown is enabled in PFM mode
4	WEAK_PD_PWM	read- write	0 = Weak pulldown is not enabled in PWM mode (and in HCPFM mode) 1 = Weak pulldown is enabled in PWM mode (and in HCPFM mode)

## 0x12654 S7\_CTRL\_PHASE\_CNT

Type: read-write Clock: PBUS\_WRCLK Reset State: 0x00

**Reset Name:** PERPH\_RB

## S7\_CTRL\_PHASE\_CNT

Bits	Name	Туре	Description
1:0	PHASE_CNT	read- write	When MULTIPHASE_EN is asserted, the number of operating phases is  00 = Number of operating phases is 1  01 = Number of operating phases is 2  10 = Number of operating phases is 4  11 = Number of operating phases is 4

## 0x12660 S7\_CTRL\_SS\_CTL

Type: read-write Clock: PBUS\_WRCLK Reset State: 0x00 Reset Name: PERPH\_RB

Reset Name. FERFII\_

PMIC\_GANGED

## S7\_CTRL\_SS\_CTL

Bits	Name	Туре	Description
4:3	SS_STEP	read- write	Softstart voltage step size  00 = SS voltage step of 1 * LSB of VPROG  01 = SS voltage step of 2 * LSB  10 = SS voltage step of 4 * LSB  11 = SS voltage step of 8 * LSB
2:0	SS_DELAY	read- write	Softstart delay between steps = 2 ^ (m + 3) / Fsys, where m = <2:0> (Fsys = 19.2 MHz):  000 = 8-clock cycles (417ns)  001 = 16-clock cycles  010 = 32-clock cycles  011 = 64-clock cycles  100 = 128-clock cycles (6.67us)  101 = 256-clock cycles  110 = 512-clock cycles  111 = 1024-clock cycles (53.3us)

#### 

Type: read-write
Clock: PBUS\_WRCLK
Reset State: 0x00
Reset Name: PERBLI Di

Reset Name: PERPH\_RB

## S7\_CTRL\_VS\_CTL

Bits	Name	Туре	Description
7	VS_EN	read-	Voltage stepping control
		write	0 = VS is disabled
			1 = VS is enabled
4:3	VS_STEP	read-	Voltage stepping voltage step size
		write	00 = VS voltage step of 1 * LSB of VPROG
			01 = VS voltage step of 2 * LSB
			10 = VS voltage step of 4 * LSB
			11 = VS voltage step of 8 * LSB
2:0	VS_DELAY	read-	Voltage stepping delay between steps = 2 ^ (m + 3) /
		write	Fsys, where $m = \langle 2:0 \rangle$ (Assuming Fsys = 19.2 MHz):
			Desired default is 1.67us
			000 = 8-clock cycles (417ns)
			001 = 16-clock cycles
			010 = 32-clock cycles
			011 = 64-clock cycles
			100 = 128-clock cycles (6.67us)
			101 = 256-clock cycles
			110 = 512-clock cycles
		000	111 = 1024-clock cycles (53.3us)

# 0x1266A S7\_CTRL\_ULS\_VALID

**Type:** read-only

Clock: PBUS\_WRCLK
Reset State: Undefined
Reset Name: PERPH\_RB

## S7\_CTRL\_ULS\_VALID

Bits	Name	Туре	Description
7:0	ULS_VALID	read- only	Readback the valid upper limit stop value

## 0x1266C S7\_CTRL\_LLS\_VALID

**Type:** read-only

Clock: PBUS\_WRCLK
Reset State: Undefined
Reset Name: PERPH\_RB

## S7\_CTRL\_LLS\_VALID

Bits	Name	Туре	Description
7:0	LLS_VALID	read- only	Readback the valid lower limit stop value

# 8.19 S7\_PS\_FTS2\_PS

## 0x12704 S7\_PS\_PERPH\_TYPE

**Type:** read-only

Clock: PBUS\_WRCLK Reset State: 0x1C Reset Name: N/A

Peripheral Type

#### S7\_PS\_PERPH\_TYPE

Bits	Name	Туре	Description
7:0	TYPE	read- only	FTS2 Power Stage Reset State: 0x1C

#### 0x12705 S7 PS PERPH SUBTYPE

**Type:** read-only

Clock: PBUS\_WRCLK Reset State: 0x08 Reset Name: N/A

Peripheral SubType

#### S7\_PS\_PERPH\_SUBTYPE

Bits	Name	Type	Description
7:0	SUBTYPE	read- only	

## 0x12740 S7\_PS\_VOLTAGE\_CTL1

Type: read-write Clock: PBUS\_WRCLK Reset State: 0x00

Reset Name: PERPH\_RB

## S7\_PS\_VOLTAGE\_CTL1

Bits	Name	Туре	Description
0	MV_RANGE	read- write	0 = Use low voltage range as specified by VSET and PFM_VOFFSET 1 = Use medium voltage range as specified by VSET and PFM_VOFFSET

## 0x12741 S7\_PS\_VOLTAGE\_CTL2

Type: read-write Clock: PBUS\_WRCLK Reset State: 0xB4 Reset Name: PERPH\_RB

PMIC\_GANGED

## S7\_PS\_VOLTAGE\_CTL2

Bits	Name	Type	Description
7:0	VSET	read- write	Output voltage set point in PWM mode and in PFM mode if the PFM_VOFFSET_EN bit is not asserted
		83.1	For MV_RANGE = 0:
			VSET => 0.005V * m + 0.080V, where $m = <7:0>$
	V. 3.	. 0	For MV_RANGE = 1:
	20.0		VSET => 0.010V * m + 0.160V, where m = <7:0>
	Co.	, 60	If PFM_VOFFSET_EN is asserted and in PFM mode, add PFM_VOFFSET

#### 

Type: read-write Clock: PBUS\_WRCLK Reset State: 0x00 Reset Name: PERPH\_RB

PMIC\_GANGED, PMIC\_SYNC=clk\_19p2:phase\_cnt\_rb

## S7\_PS\_PHASE\_CNT

Bits	Name	Туре	Description
1:0	PHASE_CNT	read- write	When MULTIPHASE_EN is asserted, the number of operating phases is  00 = Number of operating phases is 1  01 = Number of operating phases is 2  10 = Number of operating phases is 4  11 = Number of operating phases is 4

# 8.20 S7\_FREQ\_BCLK\_GEN\_CLK

## 0x12804 S7\_FREQ\_PERPH\_TYPE

**Type:** read-only

Clock: PBUS\_WRCLK Reset State: 0x1D Reset Name: N/A

Peripheral Type

#### S7\_FREQ\_PERPH\_TYPE

Bits	Name	Туре	Description
7:0	TYPE	read- only	BCLK GEN

## 0x12805 S7\_FREQ\_PERPH\_SUBTYPE

**Type:** read-only

Clock: PBUS\_WRCLK Reset State: 0x09 Reset Name: N/A

Peripheral SubType

#### S7\_FREQ\_PERPH\_SUBTYPE

Bits	Name	Туре	Description
7:0	SUBTYPE	read- only	BCLK GEN CLK

## 0x12846 S7\_FREQ\_CLK\_ENABLE

Type: read-write Clock: PBUS\_WRCLK Reset State: 0x01

Reset Name: PERPH\_RB

#### S7\_FREQ\_CLK\_ENABLE

Bits	Name	Туре	Description
7	EN_CLK_INT	read- write	0 = do not force the clock on 1 = enable the clock
0	FOLLOW_CLK_SX_REQ	read- write	0 = ignore smps_clk_req <x> 1 = clock is enabled when the clocks request is high smps_clk_req<x>='1'</x></x>

## 0x12850 S7\_FREQ\_CLK\_DIV

Type: read-write
Clock: PBUS\_WRCLK
Reset State: 0x02
Reset Name: PERPH PH

**Reset Name:** PERPH\_RB

PMIC\_GANGED

## S7\_FREQ\_CLK\_DIV

Bits	Name	Туре	Description
3:0	CLK_DIV	read- write	clock_ frequency = 19.2MHz / (CLK_DIV + 1) FTS2 Buck supports 3.2, 4.8, 6.4 and 9.6 MHz HF2 Buck supports 1.6, 2.4, 2.74, 3.2, 3.8, 4.8, and 6.4 MHz CLK_DIV = 0 is not supported, it will generate 9.6 MHz

## 0x12851 S7\_FREQ\_CLK\_PHASE

Type: read-write Clock: PBUS\_WRCLK Reset State: 0x08 Reset Name: PERPH\_RB

## S7\_FREQ\_CLK\_PHASE

Bits	Name	Туре	Description
3:0	CLK_PHASE	read- write	Distributed clock phase select: clock phase delay = clock period * (CLK_PHASE / 16)

## 0x128C0 S7\_FREQ\_GANG\_CTL1

Type: read-write Clock: PBUS\_WRCLK Reset State: 0x20

**Reset Name:** PERPH\_RB

#### S7\_FREQ\_GANG\_CTL1

Bits	Name	Туре	Description
7:0	GANG_LEADER_PID	read- write	When GANG_EN (GANG_CTL2[7]) is set, this peripheral will write the same data that is written to the gang leader Peripheral ID. Reads to the gang leader Peripheral ID are ignored by this peripheral. Ganged peripherals must reside within the same Slave ID

## 0x128C1 S7\_FREQ\_GANG\_CTL2

Type: read-write Clock: PBUS\_WRCLK Reset State: 0x80 Reset Name: PERPH\_RB

## S7\_FREQ\_GANG\_CTL2

Bits	Name	Туре	Description
7	GANG_EN	read- write	0 = disable 1 = enable When enabled, this peripheral will write the same data that is written to the gang leader PID. Reads to the gang leader PID are ignored by this peripheral

# 8.21 S8\_CTRL\_FTS2\_CTRL

## 0x12904 S8\_CTRL\_PERPH\_TYPE

**Type:** read-only

Clock: PBUS\_WRCLK Reset State: 0x03 Reset Name: N/A

Peripheral Type

#### S8\_CTRL\_PERPH\_TYPE

Bits	Name	Туре	Description
7:0	TYPE	read- only	FTS2 Control Reset State: 0x03

## 0x12905 S8\_CTRL\_PERPH\_SUBTYPE

**Type:** read-only

Clock: PBUS\_WRCLK Reset State: 0x08 Reset Name: N/A

Peripheral SubType

#### S8\_CTRL\_PERPH\_SUBTYPE

Bits	Name	Туре	Description
7:0	SUBTYPE	read- only	

#### 

**Type:** read-only

Clock: PBUS\_WRCLK Reset State: Undefined Reset Name: N/A

Status Registers

#### S8\_CTRL\_STATUS\_1

Bits	Name	Туре	Description
7	VREG_OK_FLAG	read- only	Indicates that VREG_SNS has reached a value that is greater than or equal to the threshold of the comparator tasked for VREG_SNS monitoring

## S8\_CTRL\_STATUS\_1 (Continued)

Bits	Name	Туре	Description
6	VREG_FAULT_FLAG	read- only	Indicates a probable short circuit condition at VREG_SNS since VREG_SNS is below the VREG fault voltage level and the softstart ramp is done. Current limit foldback is in use.
1	NPM_FLAG	read- only	Indicates normal power mode is in use
0	STEPPER_DONE_FLAG	read- only	Softstart stepper and voltage stepper done

#### 

**Type:** read-only

Clock: PBUS\_WRCLK Reset State: Undefined Reset Name: N/A

Status Registers

## S8\_CTRL\_STATUS\_2

Bits	Name	Туре	Description
4	ILS_FLAG	read- only	Either of the following:  => Both limit stops have been enabled, but the upper limit stop VSET_ULS has been programmed to a value below the lower limit stop VSET_LLS  => Both limit stops have been enabled, but the lower limit stop VSET_LLS has been programmed to a value above the upper limit stop VSET_ULS
3	ULS_FLAG	read- only	Indicates that the voltage setpoint has been programmed to a value that is greater than or equal to the upper limit stop VSET_ULS
2	LLS_FLAG	read- only	Indicates that the voltage setpoint has been programmed to a value that is less than or equal to the lower limit stop VSET_LLS
1	GPL_HI_FLAG	read- only	Indicates that the voltage setpoint has reached a value that is greater than or equal to the high general purpose limit VSET_GPL_HI
0	GPL_LO_FLAG	read- only	Indicates that the voltage setpoint has reached a value that is less than or equal to the low general purpose limit VSET_GPL_LO

## 0x12910 S8\_CTRL\_INT\_RT\_STS

**Type:** read-only

Clock: PBUS\_WRCLK Reset State: Undefined Reset Name: PERPH\_RB

**Interrupt Real Time Status Bits** 

#### S8\_CTRL\_INT\_RT\_STS

Bits	Name	Туре	Description
2	VREG_FAULT_INT	read- only	
1	LIMIT_ERR_INT	read- only	
0	VREG_OK_INT	read- only	.51

## 0x12911 S8\_CTRL\_INT\_SET\_TYPE

Type: read-write Clock: PBUS\_WRCLK Reset State: 0x00 Reset Name: PERPH\_RB

0 =use level trigger interrupts, 1 =use edge trigger interrupts

## **S8 CTRL INT SET TYPE**

Bits	Name	Туре	Description
2	VREG_FAULT_INT	read- write	
1	LIMIT_ERR_INT	read- write	
0	VREG_OK_INT	read- write	

## 0x12912 S8\_CTRL\_INT\_POLARITY\_HIGH

Type: read-write Clock: PBUS\_WRCLK Reset State: 0x00 Reset Name: PERPH\_RB

1= Interrupt will trigger on a level high (rising edge) event, 0 = level high triggering is disabled

#### S8\_CTRL\_INT\_POLARITY\_HIGH

Bits	Name	Туре	Description
2	VREG_FAULT_INT	read- write	
1	LIMIT_ERR_INT	read- write	
0	VREG_OK_INT	read- write	

## 0x12913 S8\_CTRL\_INT\_POLARITY\_LOW

Type: read-write Clock: PBUS\_WRCLK Reset State: 0x00 Reset Name: PERPH\_RB

1' = Interrupt will trigger on a level low (falling edge) event, '0' = level low triggering is disabled

## S8\_CTRL\_INT\_POLARITY\_LOW

Bits	Name	Туре	Description
2	VREG_FAULT_INT	read- write	1,70.
1	LIMIT_ERR_INT	read- write	0,90
0	VREG_OK_INT	read- write	

## 0x12914 S8\_CTRL\_INT\_LATCHED\_CLR

Type: write-only Clock: PBUS\_WRCLK Reset State: 0x00 Reset Name: PERPH\_RB

Writing a '1' to this interrupt will rearm the interrupt when an interrupt is pending. It clears the

internal sticky and sent bits

## S8\_CTRL\_INT\_LATCHED\_CLR

Bits	Name	Туре	Description
2	VREG_FAULT_INT	write- only	

#### S8\_CTRL\_INT\_LATCHED\_CLR (Continued)

Bits	Name	Туре	Description
1	LIMIT_ERR_INT	write- only	
0	VREG_OK_INT	write- only	

#### 0x12915 S8\_CTRL\_INT\_EN\_SET

Type: read-write Clock: PBUS\_WRCLK Reset State: 0x00 Reset Name: PERPH\_RB

Writing '0' to this register has no effect. Writing a '1' will enable the corresponding interrupt. Reading this register will readback enable status

PMIC\_SET\_MASK

#### S8\_CTRL\_INT\_EN\_SET

Bits	Name	Туре	Description
2	VREG_FAULT_INT	read- write	o's
1	LIMIT_ERR_INT	read- write	
0	VREG_OK_INT	read- write	

#### 0x12916 S8\_CTRL\_INT\_EN\_CLR

Type: read-write Clock: PBUS\_WRCLK Reset State: 0x00 Reset Name: PERPH RB

Writing '0' to this register has no effect. Writing a '1' will disable the corresponding interrupt. Reading this register will readback enable status

PMIC\_CLR\_MASK=INT\_EN\_SET

#### S8\_CTRL\_INT\_EN\_CLR

Bits	Name	Туре	Description
2	VREG_FAULT_INT	read- write	

#### S8\_CTRL\_INT\_EN\_CLR (Continued)

Bits	Name	Туре	Description
1	LIMIT_ERR_INT	read- write	
0	VREG_OK_INT	read- write	

#### 0x12918 S8\_CTRL\_INT\_LATCHED\_STS

Type: read-only Clock: PBUS\_WRCLK Reset State: 0x00 Reset Name: PERPH\_RB

Debug: Latched (Sticky) Interrupt. '1' indicates that the interrupt has triggered. Once the latched bit is set it can only be cleared by writing the clear bit.

#### S8\_CTRL\_INT\_LATCHED\_STS

Bits	Name	Туре	Description
2	VREG_FAULT_INT	read- only	This No
1	LIMIT_ERR_INT	read- only	720.
0	VREG_OK_INT	read- only	0,90

# 0x12919 S8\_CTRL\_INT\_PENDING\_STS

Type: read-only Clock: PBUS\_WRCLK Reset State: 0x00 Reset Name: PERPH\_RB

Debug: Pending is set if interrupt has been sent but not cleared.

#### S8\_CTRL\_INT\_PENDING\_STS

Bits	Name	Туре	Description
2	VREG_FAULT_INT	read- only	
1	LIMIT_ERR_INT	read- only	
0	VREG_OK_INT	read- only	

#### 0x1291A S8\_CTRL\_INT\_MID\_SEL

Type: read-write Clock: PBUS\_WRCLK Reset State: 0x00 Reset Name: PERPH\_RB

Selects the MID that will receive the interrupt

#### S8\_CTRL\_INT\_MID\_SEL

Bits	Name	Туре	Description
1:0	INT_MID_SEL	read- write	-

### 0x1291B S8\_CTRL\_INT\_PRIORITY

Type: read-write Clock: PBUS\_WRCLK Reset State: 0x00

**Reset Name:** PERPH\_RB

SR = 0 A = 1

#### S8\_CTRL\_INT\_PRIORITY

Bi	ts	Name	Туре	Description
0	INT	_PRIORITY	read- write	

### 0x12940 S8\_CTRL\_VOLTAGE\_CTL1

Type: read-write Clock: PBUS\_WRCLK Reset State: 0x00 Reset Name: PERPH\_RB

PMIC\_GANGED

# S8\_CTRL\_VOLTAGE\_CTL1

Bits	Name	Туре	Description
0	MV_RANGE	read- write	0 = Use low voltage range as specified by VSET and PFM_VOFFSET
			1 = Use medium voltage range as specified by VSET and PFM_VOFFSET

### 0x12941 S8\_CTRL\_VOLTAGE\_CTL2

Type: read-write Clock: PBUS\_WRCLK Reset State: 0xB4 Reset Name: PERPH\_RB

PMIC\_GANGED

#### S8\_CTRL\_VOLTAGE\_CTL2

Bits	Name	Туре	Description
7:0	VSET	read- write	Output voltage set point in PWM mode and in PFM mode if the PFM_VOFFSET_EN bit is not asserted
		S	For MV_RANGE = 0: VSET => 0.005V * m + 0.080V, where m = <7:0> For MV_RANGE = 1: VSET => 0.010V * m + 0.160V, where m = <7:0> If PFM_VOFFSET_EN is asserted and in PFM mode, add PFM_VOFFSET

### 0x12942 S8\_CTRL\_VSET\_VALID

Type: read-only Clock: PBUS\_WRCLK Reset State: Undefined Reset Name: PERPH\_RB

#### S8\_CTRL\_VSET\_VALID

Bits	Name	Туре	Description
7:0	VSET_VALID	read- only	Readback the valid output voltage setpoint value

### 0x12944 S8\_CTRL\_VOLTAGE\_CTL3

Type: read-write
Clock: PBUS\_WRCLK
Reset State: 0x00

Reset Name: PERPH\_RB

### S8\_CTRL\_VOLTAGE\_CTL3

Bits	Name	Туре	Description
7	PFM_VOFFSET_EN	read- write	When in PFM mode  0 = Use VSET for output voltage set point  1 = Use VSET + PFM_VOFFSET for output voltage set point
1:0	PFM_VOFFSET	read- write	When in PFM mode and PFM_VOFFSET_EN is asserted, add a positive output voltage offset  For MV_RANGE = 0:  VOFFSET = 0.005V * 2 * m, where m = <1:0>  For MV_RANGE = 1:  VOFFSET = 0.010V * 2 * m, where m = <1:0>

### 0x12945 S8\_CTRL\_MODE\_CTL

Type: read-write Clock: PBUS\_WRCLK Reset State: 0x80

Reset Name: PERPH\_RB

PMIC\_GANGED

#### S8\_CTRL\_MODE\_CTL

Bits	Name	Type	Description
7	NPM	read- write	FTS NON-AUTO mode control 0 = Low power mode (LPM) unless AUTO_MODE is asserted 1 = Normal power mode (PWM)
6	AUTO_MODE	read- write	When asserted, FTS automatically enters and exits low power mode (PFM) based on load current qualifying triggers  0 = AUTO mode is disabled  1 = AUTO mode is enabled

# 0x12946 S8\_CTRL\_EN\_CTL

Type: read-write
Clock: PBUS\_WRCLK
Reset State: 0x00

Reset Name: PERPH\_RB

#### S8\_CTRL\_EN\_CTL

Bits	Name	Туре	Description
7	PERPH_EN	read- write	FTS enable control 0 = Off
		Willo	1 = On

### 0x12948 S8\_CTRL\_PD\_CTL

Type: read-write Clock: PBUS\_WRCLK Reset State: 0x00 Reset Name: PERPH\_RB

## S8\_CTRL\_PD\_CTL

Bits	Name	Туре	Description
7	PD_EN	read- write	0 = Strong pulldown is always disabled 1 = Strong pulldown is enabled when the regulator is disabled
6	WEAK_PD_EN	read- write	0 = Weak pulldown is not enabled in OFF state 1 = Weak pulldown is enabled in OFF state
5	WEAK_PD_PFM	read- write	0 = Weak pulldown is not enabled in PFM mode 1 = Weak pulldown is enabled in PFM mode
4	WEAK_PD_PWM	read- write	0 = Weak pulldown is not enabled in PWM mode (and in HCPFM mode) 1 = Weak pulldown is enabled in PWM mode (and in HCPFM mode)

### 0x12954 S8\_CTRL\_PHASE\_CNT

Type: read-write Clock: PBUS\_WRCLK Reset State: 0x00 Reset Name: PERPH\_RB

\_

#### S8\_CTRL\_PHASE\_CNT

Bits	Name	Туре	Description
1:0	PHASE_CNT	read- write	When MULTIPHASE_EN is asserted, the number of operating phases is 00 = Number of operating phases is 1 01 = Number of operating phases is 2 10 = Number of operating phases is 4 11 = Number of operating phases is 4

#### 

Type: read-write Clock: PBUS\_WRCLK Reset State: 0x00 Reset Name: PERPH\_RB

PMIC\_GANGED

### S8\_CTRL\_SS\_CTL

Bits	Name	Туре	Description
4:3	SS_STEP	read- write	Softstart voltage step size  00 = SS voltage step of 1 * LSB of VPROG  01 = SS voltage step of 2 * LSB  10 = SS voltage step of 4 * LSB  11 = SS voltage step of 8 * LSB
2:0	SS_DELAY	read- write	Softstart delay between steps = 2 ^ (m + 3) / Fsys, where m = <2:0> (Fsys = 19.2 MHz):  000 = 8-clock cycles (417ns)  001 = 16-clock cycles  010 = 32-clock cycles  011 = 64-clock cycles  100 = 128-clock cycles (6.67us)  101 = 256-clock cycles  110 = 512-clock cycles  111 = 1024-clock cycles (53.3us)

#### 

Type: read-write
Clock: PBUS\_WRCLK
Reset State: 0x00
Reset Name: PERPIT DI

**Reset Name:** PERPH\_RB

#### S8\_CTRL\_VS\_CTL

Bits	Name	Type	Description
7	VS_EN	read-	Voltage stepping control
		write	0 = VS is disabled
			1 = VS is enabled
4:3	VS_STEP	read-	Voltage stepping voltage step size
		write	00 = VS voltage step of 1 * LSB of VPROG
			01 = VS voltage step of 2 * LSB
			10 = VS voltage step of 4 * LSB
			11 = VS voltage step of 8 * LSB
2:0	VS_DELAY	read-	Voltage stepping delay between steps = 2 ^ (m + 3) /
		write	Fsys, where m = <2:0> (Assuming Fsys = 19.2 MHz):
			Desired default is 1.67us
			000 = 8-clock cycles (417ns)
			001 = 16-clock cycles
			010 = 32-clock cycles
			011 = 64-clock cycles
			100 = 128-clock cycles (6.67us)
			101 = 256-clock cycles
			110 = 512-clock cycles
		8	111 = 1024-clock cycles (53.3us)

# 0x1296A S8\_CTRL\_ULS\_VALID

Type: read-only
Clock: PBUS\_WRCLK
Reset State: Undefined

Reset State: Undefined Reset Name: PERPH\_RB

#### S8\_CTRL\_ULS\_VALID

Bits	Name	Туре	Description
7:0	ULS_VALID	read- only	Readback the valid upper limit stop value

# 0x1296C S8\_CTRL\_LLS\_VALID

**Type:** read-only

Clock: PBUS\_WRCLK Reset State: Undefined Reset Name: PERPH\_RB

### S8\_CTRL\_LLS\_VALID

Bits	Name	Туре	Description
7:0	LLS_VALID	read- only	Readback the valid lower limit stop value



# 8.22 S8\_PS\_FTS2\_PS

### 0x12A04 S8\_PS\_PERPH\_TYPE

**Type:** read-only

Clock: PBUS\_WRCLK Reset State: 0x1C Reset Name: N/A

Peripheral Type

#### S8\_PS\_PERPH\_TYPE

Bits	Name	Туре	Description
7:0	TYPE	read- only	FTS2 Power Stage Reset State: 0x1C

#### 0x12A05 S8\_PS\_PERPH\_SUBTYPE

**Type:** read-only

Clock: PBUS\_WRCLK Reset State: 0x08 Reset Name: N/A

Peripheral SubType

#### S8\_PS\_PERPH\_SUBTYPE

Bits	Name	Туре	Description
7:0	SUBTYPE	read- only	

# 0x12A40 S8\_PS\_VOLTAGE\_CTL1

Type: read-write
Clock: PBUS\_WRCLK
Reset State: 0x00

Reset Name: PERPH\_RB

#### S8\_PS\_VOLTAGE\_CTL1

Bits	Name	Туре	Description
0	MV_RANGE	read- write	0 = Use low voltage range as specified by VSET and PFM_VOFFSET 1 = Use medium voltage range as specified by VSET and PFM_VOFFSET

### 0x12A41 S8\_PS\_VOLTAGE\_CTL2

Type: read-write Clock: PBUS\_WRCLK Reset State: 0xB4 Reset Name: PERPH\_RB

PMIC\_GANGED

#### S8\_PS\_VOLTAGE\_CTL2

Bits	Name	Type	Description
7:0	VSET	read- write	Output voltage set point in PWM mode and in PFM mode if the PFM_VOFFSET_EN bit is not asserted
		83.1	For MV_RANGE = 0:
			VSET => 0.005V * m + 0.080V, where $m = <7:0>$
	V. 3.	. 0	For MV_RANGE = 1:
	20.0		VSET => 0.010V * m + 0.160V, where m = <7:0>
	Co.	, 60	If PFM_VOFFSET_EN is asserted and in PFM mode, add PFM_VOFFSET

#### 0x12A54 S8\_PS\_PHASE\_CNT

Type: read-write Clock: PBUS\_WRCLK Reset State: 0x00 Reset Name: PERPH\_RB

PMIC\_GANGED, PMIC\_SYNC=clk\_19p2:phase\_cnt\_rb

### S8\_PS\_PHASE\_CNT

Bits	Name	Туре	Description
1:0	PHASE_CNT	read- write	When MULTIPHASE_EN is asserted, the number of operating phases is  00 = Number of operating phases is 1  01 = Number of operating phases is 2  10 = Number of operating phases is 4  11 = Number of operating phases is 4

# 8.23 S8\_FREQ\_BCLK\_GEN\_CLK

### 0x12B04 S8\_FREQ\_PERPH\_TYPE

**Type:** read-only

Clock: PBUS\_WRCLK Reset State: 0x1D Reset Name: N/A

Peripheral Type

### S8\_FREQ\_PERPH\_TYPE

E	Bits	Name	Туре	Description
-	7:0	TYPE	read- only	BCLK GEN

#### 0x12B05 S8\_FREQ\_PERPH\_SUBTYPE

**Type:** read-only

Clock: PBUS\_WRCLK Reset State: 0x09 Reset Name: N/A

Peripheral SubType

#### S8\_FREQ\_PERPH\_SUBTYPE

Bits	Name	Туре	Description
7:0	SUBTYPE	read- only	BCLK GEN CLK

### 0x12B46 S8\_FREQ\_CLK\_ENABLE

Type: read-write Clock: PBUS\_WRCLK Reset State: 0x01

Reset Name: PERPH\_RB

#### S8\_FREQ\_CLK\_ENABLE

Bits	Name	Туре	Description
7	EN_CLK_INT	read- write	0 = do not force the clock on 1 = enable the clock
0	FOLLOW_CLK_SX_REQ	read- write	0 = ignore smps_clk_req <x> 1 = clock is enabled when the clocks request is high smps_clk_req<x>='1'</x></x>

#### 0x12B50 S8\_FREQ\_CLK\_DIV

Type: read-write Clock: PBUS\_WRCLK Reset State: 0x02 Reset Name: PERPH\_RB

PMIC\_GANGED

#### S8\_FREQ\_CLK\_DIV

Bits	Name	Туре	Description
3:0	CLK_DIV	read- write	clock_ frequency = 19.2MHz / (CLK_DIV + 1) FTS2 Buck supports 3.2, 4.8, 6.4 and 9.6 MHz HF2 Buck supports 1.6, 2.4, 2.74, 3.2, 3.8, 4.8, and 6.4 MHz CLK_DIV = 0 is not supported, it will generate 9.6 MHz

### 0x12B51 S8\_FREQ\_CLK\_PHASE

Type: read-write Clock: PBUS\_WRCLK Reset State: 0x0C Reset Name: PERPH\_RB

#### S8\_FREQ\_CLK\_PHASE

Bits	Name	Туре	Description
3:0	CLK_PHASE	read- write	Distributed clock phase select: clock phase delay = clock period * (CLK_PHASE / 16)

### 0x12BC0 S8\_FREQ\_GANG\_CTL1

Type: read-write Clock: PBUS\_WRCLK Reset State: 0x20

Reset Name: PERPH\_RB

#### S8\_FREQ\_GANG\_CTL1

Bits	Name	Туре	Description
7:0	GANG_LEADER_PID	read- write	When GANG_EN (GANG_CTL2[7]) is set, this peripheral will write the same data that is written to the gang leader Peripheral ID. Reads to the gang leader Peripheral ID are ignored by this peripheral. Ganged peripherals must reside within the same Slave ID

# 0x12BC1 S8\_FREQ\_GANG\_CTL2

Type: read-write Clock: PBUS\_WRCLK Reset State: 0x80 Reset Name: PERPH\_RB

#### S8\_FREQ\_GANG\_CTL2

Bits	Name	Туре	Description
7	GANG_EN	read- write	0 = disable 1 = enable When enabled, this peripheral will write the same data that is written to the gang leader PID. Reads to the gang leader PID are ignored by this peripheral



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