QUALCOMM CDMA Technologies

REDEFINING MOBILITY

Thermal Design Checklist

80-VU794-21 Rev. B

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Revision History

Revision	Date	Description
A	March 4, 2011	Initial release
B	June 16, 2011	▪ Added Slide 8 for a thermal design example of the thin form factor. ▪ Added Slide 13 for a thermal design recommendation of 19.2 MHz XO. ▪ Added a document on the list of references.

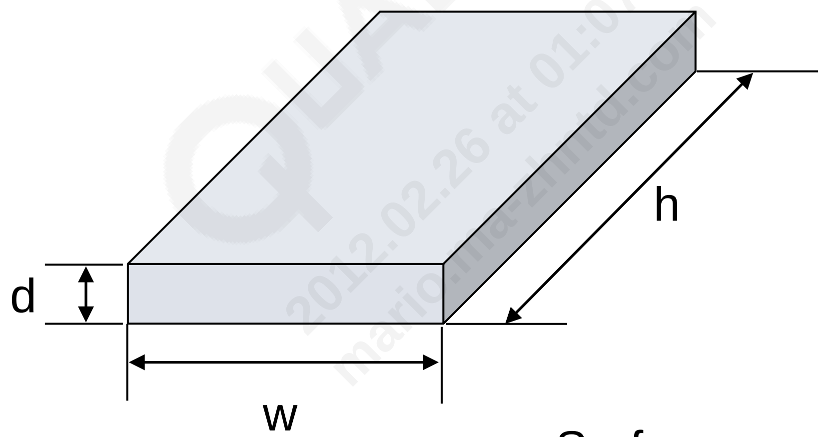
Table of contents

1. Introduction

- This document provides a checklist of the crucial elements that make up a solid thermal design, when using the Qualcomm MSM™, APQ™, or MDM™ series of chipsets.
- Each slide focuses on a thermal design consideration for different phases of the overall design effort.
  - Industrial design
  - Part placement
  - PCB routing
- This document is intended to focus on wireless handset development.

2. How big is the surface area of the industrial design?

- Industrial design is the key factor of thermal design.
- Increase the surface area of the housing with consideration to industrial design goals.

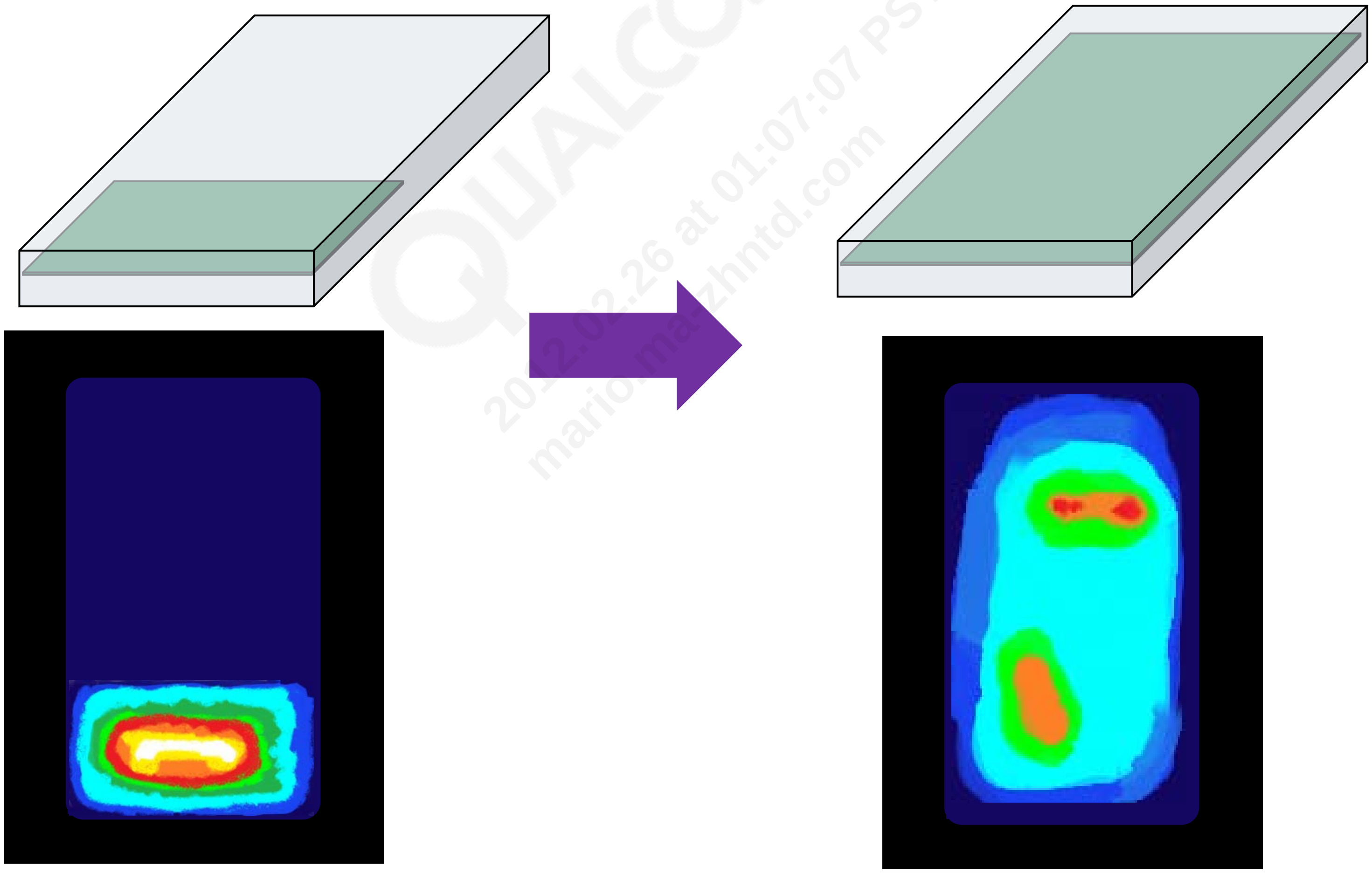


Surface area = 2dw + 2dh + 2hw

- Calculate the temperature rise on a handset surface:
  - Refer to the *Thermal Design Considerations Application Note* (80-VU794-5, Rev. D), slides 14–15

3. How big is the area of the PWB?

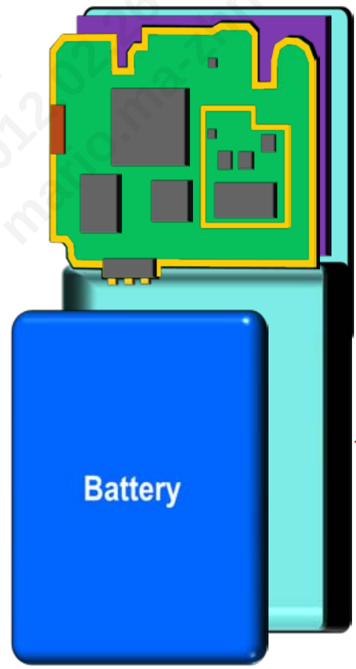
- Increase the PWB area to maximize the area where heat can be dissipated over the surface of the handset.



4. How to achieve a thin form factor without thermal risk?

Side view, cross-sectional

- LCD glass
- Solid metal frame (i.e., Mg-alloy)
- High thermal conductivity material foam (i.e., graphite foam sheet)
- Components (heat sources)
- PCB

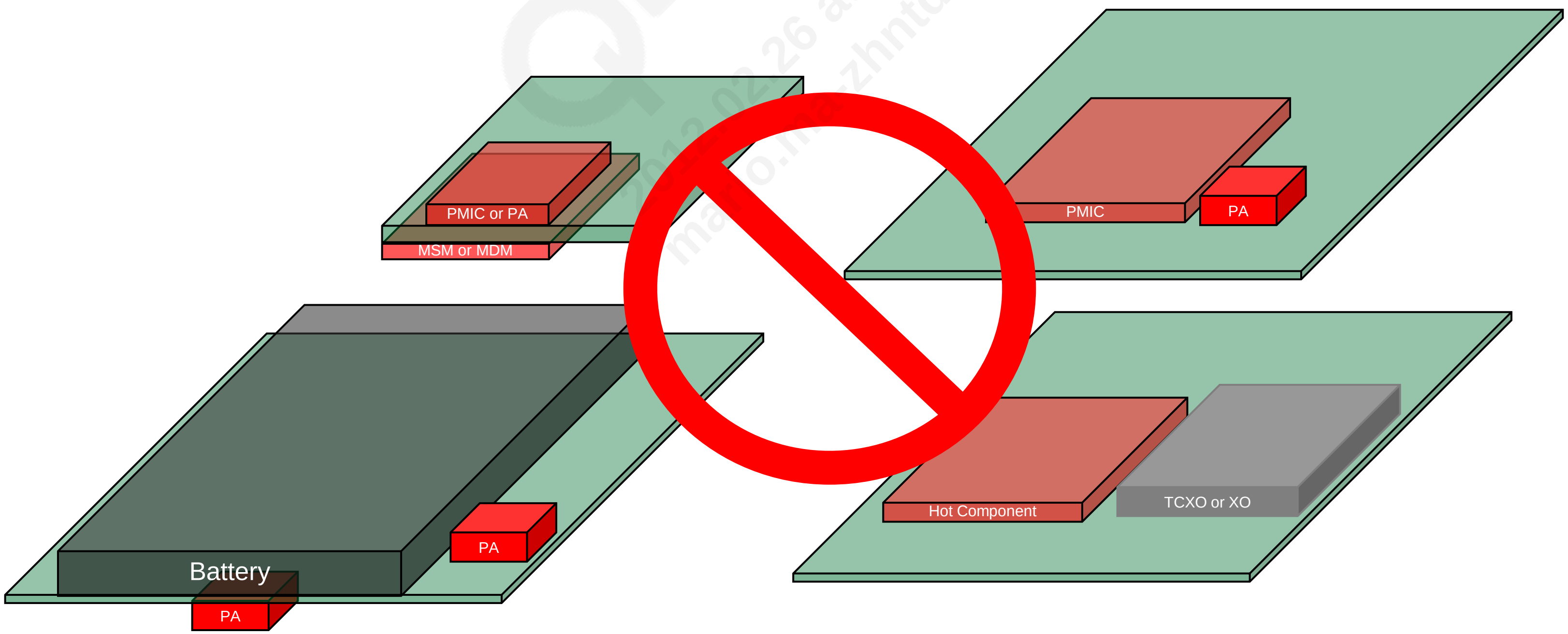


Solid metal frame and high thermal conductivity material foam can help to transfer heat over the UE housing, easing the risk of the hot spots.

Negative engraving for battery compartment Is recommended to maximize thermal distribution.

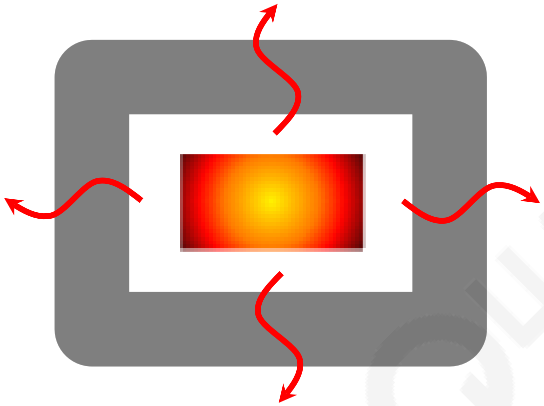
5. How much distance is needed between adjacent heat sources?

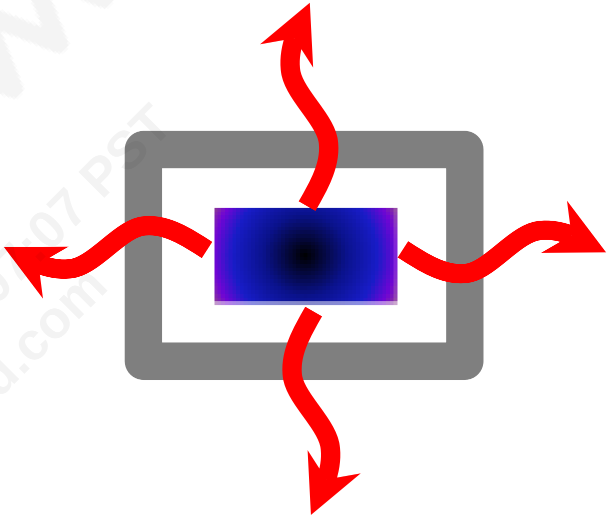
- Avoid co-locating high-power density parts side-by-side or front-to-back on the single PWB or face-to-face on two parallel PWBs.
  - Keep the PA away from other heat sources.
  - Keep very hot components away from a battery.
  - Keep the PMIC away from the MDM device.
  - Keep the TCXO or any XO away from heat sources/gradients.



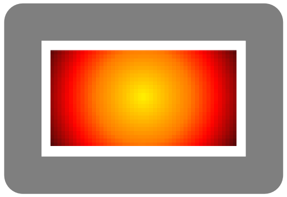
6. How is the mechanical design constrained?

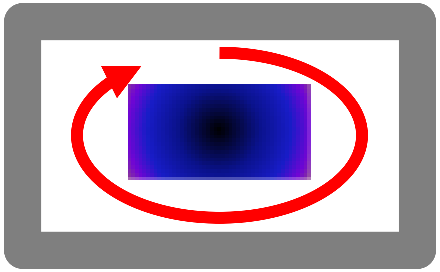
- Thermal resistance is proportional to wall thickness.





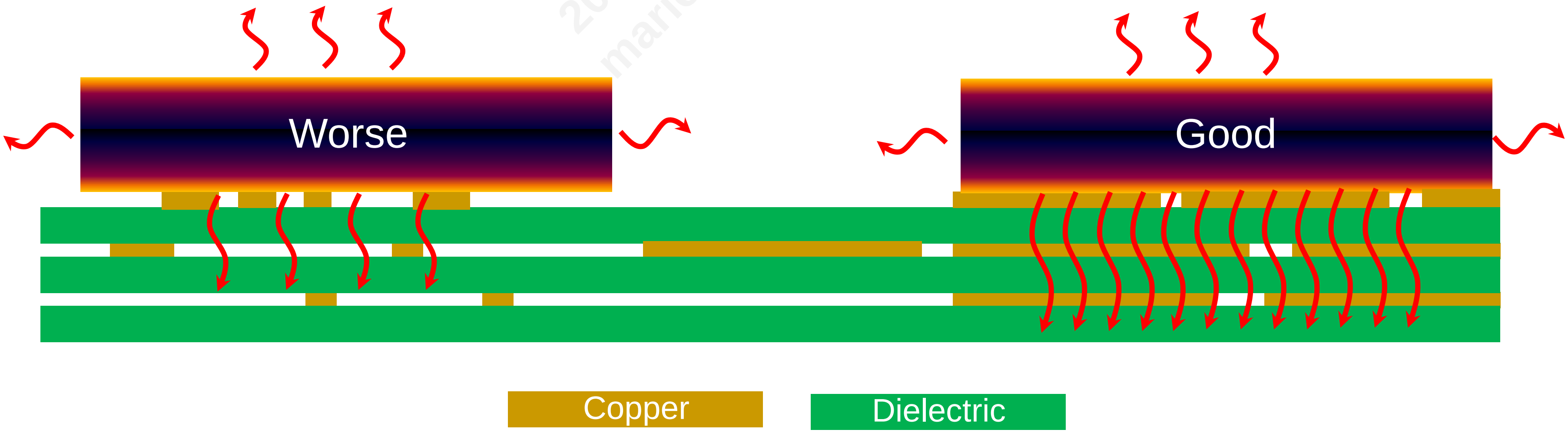
- Better air flow inside the housing can provide effective convection.





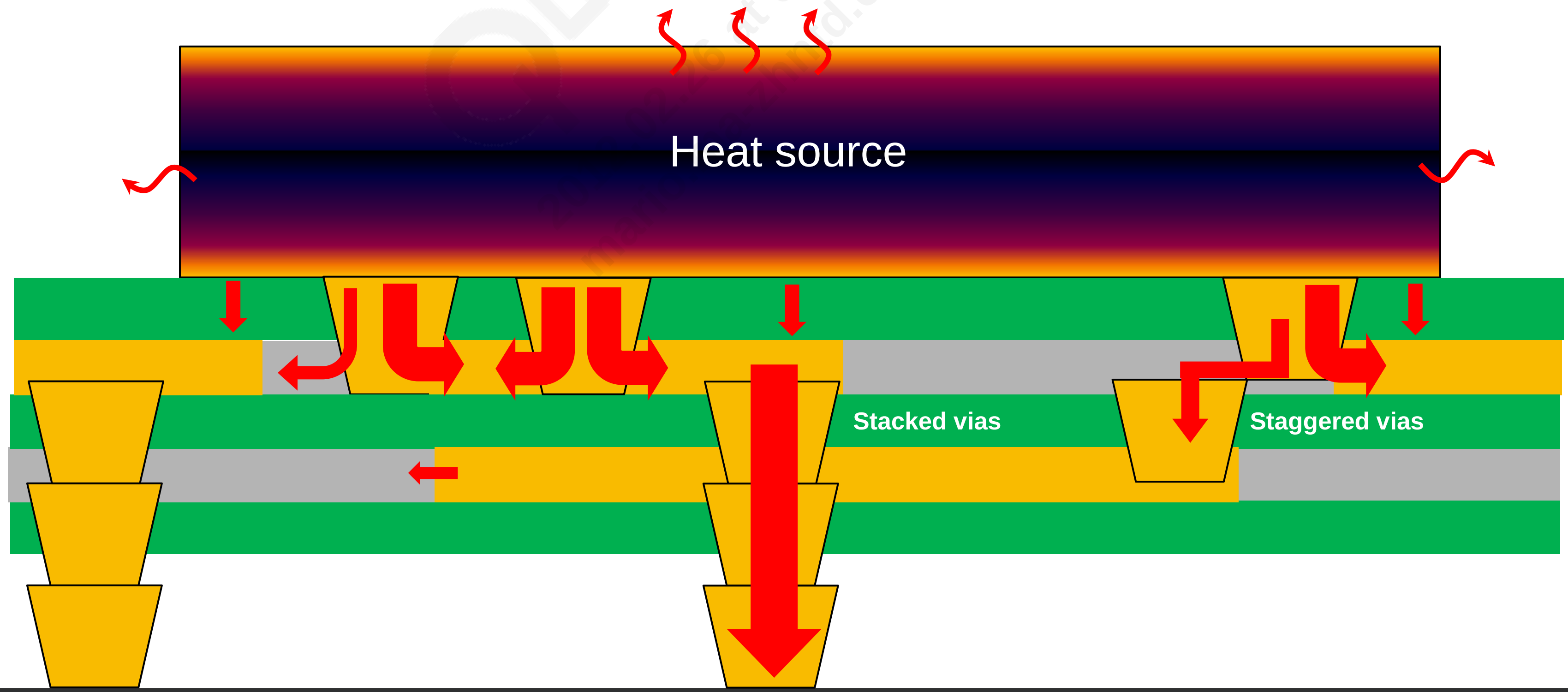
7. How well can heat flow under the hot components?

- Increase the conductivity of the PWB with added layers and high copper density on each layer.
- A higher copper density provides better thermal relief/heat transport.
  - Do not rely on air dissipation only for RF power amplifiers. A large amount of copper in the PWB is necessary to help heat-sink the thermal load.
  - Fill empty board layers with copper wherever possible.
  - Filling the heat source mount side with copper is very important.
  - Increase the copper using thick traces as much as possible. This is especially recommended for voltage rails that consume high current.



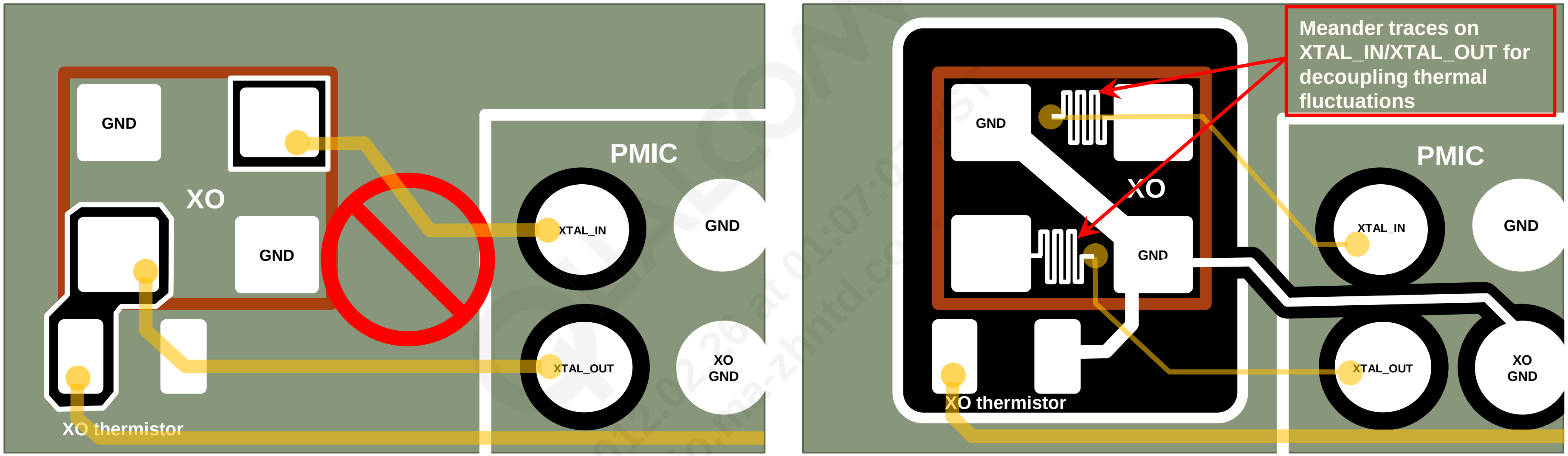
7. How well can heat flow under the hot components (cont.)?

- Add ample PWB vias under or near the hot spots.
  - Visa should go to a large radiating plane for better heat dissipation.
  - Via material is very important. Solid copper is better than paste.
  - Stacked vias are better than staggered.
  - Vias in the PA ground pad are very important. Use as many as possible.



8. What are thermal design considerations for the XO?

- Thermal isolation to the 19.2 MHz XO and XO thermistor from other devices is required.



- Keep the 19.2 MHz XO and XO thermistor away from any heat source on the PCB.
- Minimize thermal coupling on XTAL_IN/XTAL_OUT using a meandering trace.
- Meandering traces of XTAL_IN/XTAL_OUT might be critical for a GPS function with a 19.2 MHz XO on a small PCB area area, in case the length of the traces is less than 10 mm without meandering.
- APQ devices might not require thermal design considerations.
- Refer to *Enhanced guidelines to implement 19.2 MHz Crystal for Small PCB/High Thermal Layouts* (80-VP447-10) for more details.

9. References

- *Thermal Design Considerations Application Note* (80-VU794-5)
- *Thermal Protection Algorithm Overview* (80-VT344-1)
- *Enhanced Guidelines to Implement 19.2 MHzCrystal for Small PCB/High Thermal Layouts* (80-VP447-10)

Questions?

https://support.cdmatech.com

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