Qualcomm
TECHNOLOGIES, INC

MSM8274/MSM8674/MSM8974

Device Specification

80-NA437-1 Rev. H

May 3, 2013

Submit technical questions at:
https://support.cdmatech.com

Confidential and Proprietary – Qualcomm Technologies, Inc.

Qualcomm Technologies, Inc.
5775 Morehouse Drive
San Diego, CA 92121
U.S.A.

Revision history

Revision	Date	Description
A	April 2012	Initial release
B	June 2012	■ Removed “Advance Information” from the document title ■ Revised WCN details and HS USB 2.0 details in Figure 1-1, *MSM8x74 functional block diagram and example application* ■ Updated GNSS to Gen 8B in Section 1.2, *MSM8x74 introduction* and Section 1.3.3, *Summary of MSM8x74 features* ■ Revised UIM and USB details in Section 1.3.3, *Summary of MSM8x74 features* ■ Updated the following pins in Figure 2-3, *High-level view of MSM8x74 bottom pin assignments* and in Table 2-12, *Pin descriptions – power supply pins* □ G29 – Changed from GND to DNC □ BD28 – Changed from VDD_A2 to VDD_MEM ■ Revised Table 2-3, *Pin descriptions – multimedia functions*, through Table 2-10, *Pin descriptions – general-purpose input/output ports* □ Revised the pad type from B- to BH- (bidirectional, high-voltage tolerant) for pad voltages P2, P5, and P6 □ Revised the pad type from BH- to B- for all other pad voltages ■ Revised Table 2-4, *Pin descriptions – connectivity functions* □ Removed touch screen signals □ Corrected SLIMBUS_MCLK, SPKR_I2S_MCLK, and BLSP8_2 pad numbers □ Added audio PCM interface information □ Revised SDC1 and SDC2 interface pad type details ■ Revised Table 2-6, *Pin descriptions – internal functions* and Table 2-10, *Pin descriptions – general-purpose input/output ports* □ Added ETM signals □ Revised the functional description for BOOT_CONFIG_0 through BOOT_CONFIG_4 to include WDOG_DISABLE and FAST_BOOT_SEL[0] through FAST_BOOT_SEL[3] □ Removed BOOT_CONFIG_5 through BOOT_CONFIG_15 ■ Revised Table 2-7, *MSM8x74 wakeup pins for modem power management (MPM)* □ Corrected the GPIO_46 pad number □ Replaced pad voltage and pad type TBDs with values ■ Removed all RFFE switch control signals from Table 2-9, *Pin descriptions – RF front-end functions*

Revision	Date	Description
B (cont.)	June 2012	■ Revised Table 2-10, *Pin descriptions – general-purpose input/output ports* □ Added audio PCM interface information □ Changed the GPIO_145 pad type to B-PD:nppukp □ Changed the GPIO_144 pad type to B-PD:nppukp □ Corrected pad names – SDC1_DATA1 to SDC1_DATA_1 – SDC1_DATA3 to SDC1_DATA_3 – SDC2_DATA1 to SDC2_DATA_1 – SDC2_DATA3 to SDC2_DATA_3 ■ Corrected VDD_GFX and VDD_USB_CORE pad numbers in Table 2-12, *Pin descriptions – power supply pins* ■ Corrected GND pad numbers in Table 2-13, *Pin descriptions – ground pins* ■ Added Chapter 3, *Electrical Specifications* ■ Added Section 4.2, *Part marking* through Section 4.5, *Thermal characteristics* ■ Added Chapter 5, *Carrier, Storage, & Handling Information* ■ Added Chapter 6, *PCB Mounting Guidelines* ■ Added Section 7.2, *Qualification sample description*
C	September 2012	■ Changed the signal label from SSBIs to SPMI on the PMIC block in Figure 1-1, *MSM8x74 functional block diagram and example application* ■ Removed the optional 32.768 k sleep clock and some graphics details from SEction 1.3.3, *Summary of MSM8x74 features* ■ Changed the G29 label from NC to DNC in Figure 2-3, *High-level view of MSM8x74 bottom pin assignments* ■ Revised BLSP details in Section 2.2.2, *Pin descriptions – MSM bottom* ■ Added Table 2-8, *MODE[1:0] settings* ■ Revised the PMIC_SPMI_CLK (pin W49) pad type from DI to DO in Table 2-9, *Pin descriptions – chipset interface functions* ■ Added global general purpose clock signals to Table 2-11, *Pin descriptions – general-purpose input/output ports* ■ Added G29 to Table 2-12, *Pin descriptions – no connection, do not connect, and reserved pins* ■ Added EBI0 to VDD_P1 parameter details and revised several typical values in Table 3-2, *Recommended operating conditions* ■ Revised the maximum impedances, revised the frequencies in the maximum impedance column, and added the power domains VDD_DDR_CORE_1P2, VDD_P1, and VDD_P4 to Table 3-3, *Power distribution network impedance vs. frequency* ■ Added a note to regarding the DD_DDR_CORE_1P2, VDD_P1, and VDD_P4 domains to Section 3.3, *Power distribution network* ■ Changed UICC to UIM, changed GSBI to BLSP, and removed dual voltage for UIM in BLSP in Section 3.10, *Connectivity* ■ Revised the supply source code and assembly site code in Table 4-1, *MSM8x74 device marking line definitions* ■ Revised Table 4-2, *Device identification code / ordering information details* ■ Removed Table 4-3, *Source configuration code*

Revision	Date	Description
D	January 2013	■ Updated Section 1.2 to include Bare Die PoP (BDP) package information and correct the release number for LTE Cat4 from 9 to 10 ■ Table 1-3, added new acronym Bare Die PoP (BDP), Bare Die Package-on-package Nanoscale Package (BPNSP), Molded Laser PoP (MLP), and Process Voltage Scaling (PVS) ■ Updated Section 1.3.3 □ Corrected 2.85 V to 2.95 V for BLSP ports and UIM □ Added MLP and BDP information ■ Table 2-4, added new rows for pad # BH10, SPI_CS3_N_BLSP1 ■ Table 2-5, added a new row for Configuration 2-pin UART+ 2 GPIOs ■ Updated note under Table 2-5, added CS3 option for BLSP1 ■ Table 2-7, added GPIO_92 and GPIO_95 information; made other minor updates to wakeup function descriptions. ■ Table 2-11, updated GPIO_9, GPIO_10, and GPIO_11 information to include SPI_CS information ■ Table 2-15, updated pad # A16 to AH16 ■ Updated Table 3-2: □ VDD_WLAN typical value updated from 1.25 V to 1.3 V □ VDD_KRAIT updated to include PVS information ■ Updated Section 3.2 to include KRAIT PVS information ■ Table 3-3, updated maximum impedance value for VDD_DDR_CORE_1P2/VDD_P1/VDD_P4 ■ Updated Section 3.8.1 and Section 3.8.1.1 to include information on EBI0 and EBI1 ■ Updated Section 4.1 to include BDP package information ■ Added Figure 4-2, 990B PNSP (15 x 15 x 0.74 mm) outline drawing ■ Updated Tabvle 4-2 to include BDP package device identification code ■ Updated Figure 4-4 to include BDP package ordering example ■ Updated Section 6.2.1 to include 990B-PNSP land/stencil drawing information ■ Updated Section 6.2.2 to include MLP and BDP production assembly information ■ Updated Section 6.3 to include BDP Daisy Chain information
E	February 2013	■ Updated list of device identification code/ordering information details in Table 4-2
F	March 2013	■ Updated Section 1.2 to include additional complementary ICs within the MSM8x74 chipset ■ Updated Table 2-1 to change values from 2.85 V to 2.95 V ■ Updated Table 3-2 to include maximum and minimum voltage rail specifications on a number of rails ■ Updated Table 3-19 to include the MSM variation for SLIMbus ■ Updated Table 3-29 note to included appropriate specifications ■ Updated Table 4-2 to include the latest MSM device identification code/ordering information details ■ Updated Section 6.2.2 to include reference to *MSM8274/MSM8674/MSM8974 Package-on-package Guide* (80-NA437-54)

Revision	Date	Description
G	April 2013	■ Updated Table 2-3 to make it clear that camera control interface I2C is dedicated only for the camera. ■ Updated Table 2-4 to remove notes on different interfaces supported by BLSP. Customer should refer Table 2-5 as specified for details on the interfaces supported by BLSP. ■ Updated Table 2-11 to note CODEC interrupt 1 as alternate function of GPIO_72. ■ Updated Table 3-3 and added Table 3-4 to provide updated PDN spec for VDD_CORE. ■ Updated Section 3.4 to include reference and document number for the current consumption application note. ■ Updated Table 4-2 to include the most recent device identification codes. ■ Updated Figure 4-4 to include a more recent example of ordering information.
H	May 2013	■ Updated Figure 1-1 audio interface from I2S to sterio bi-directional MI2S (x3) ■ Updated Section 1.3 to change the Modem QDSP6 frequency to 800 MHz ■ Updated Table 1-2 audio interface information ■ Updated Table 2-1 EBI pad description ■ Updated Table 2-7 to have SD card detect at GPIO_62 ■ Updated Table 2-11 to remove CODEC_MAD_INT from GPIO_72 as this is implemented in software ■ Updated Table 3-2 minimum and maximum operational voltage information that was previously TBD ■ Updated Table 3-5 digital I/O characterization information that was previously TBD ■ Updated Table 3-6 digital I/O characterization information that was previously TBD ■ Added Table 3-7 for digital I/O characteristics for 1.2 V SDC1 ■ Added Table 3-8 for digital I/O characteristics for 1.8 V SDC1 ■ Added Table 3-9 for digital I/O characteristics for 1.8 V SD and UIM ■ Updated Table 3-10 digital I/O characterization information that was previously TBD ■ Updated Section 3.8.1 EBI pad drive strength information ■ Updated Table 3-11 DDR clock frequency minimum from TBD to "–" and updated the clock crossover-point to TBDs ■ Updated Table 3-12 clock crossover-point to TBDs ■ Updated Table 3-14 MIPI_CSI feature exceptions from TBD to none ■ Updated Table 3-20 to include the USB rail, minimum and maximum voltages that were previously TBD ■ Updated Table 3-25 t(pdout) maximum parameter from 350 ns to 60 ns ■ Updated Table 3-31 SPI timing numbers ■ Updated Table 3-34 JTAG timing numbers ■ Updated Section 7.1 to include reliability summary ■ Updated Section 7.2 to include BDP and MLP device characteristic information

Contents

Figures

Tables

1 Introduction

1.1 Documentation overview

This device specification defines three mobile station modem devices: MSM8274, MSM8674, and MSM8974. Throughout this document, the devices are referred to as the MSM8x74 when material being presented applies to all of them. The main difference between the MSM™ variants is the air interface standards that are supported, as summarized in Section 1.2.1.

Technical information for these devices is primarily covered by the documents listed in Table 1-1. All documents should be studied for a thorough understanding of the device and its applications. Released MSM8x74 documents are available for download at https://support.cdmatech.com (the CDMA Tech Support website).

NOTE This current revision is an early release to support initial product developers. The content is subject to change without advance notice.

Table 1-1 Primary MSM8x74 documentation

Document number	Title/description
80-NA437-1 (this document)	*MSM8274/MSM8674/MSM8974 Device Specification* Provides all MSM8x74 electrical specifications and mechanical information. Additional material includes pin assignments; shipping, storage, and handling instructions; PCB mounting guidelines; and part reliability. This document can be used by company purchasing departments to facilitate procurement.
80-NA437-1A	*MSM8274/MSM8674/MSM8974 Pin Assignment Spreadsheet* A Microsoft Excel spreadsheet listing all MSM8x74 pad numbers (in alphanumeric order), pad names, pad voltages, pad types, and functional descriptions. This can be used to help build the IC's CAD library symbol, or for quick reference for a particular pad's functional assignment.
80-NA437-1B	*MSM8274/MSM8674/MSM8974 GPIO Configuration Spreadsheet* A Microsoft Excel spreadsheet listing all MSM8x74 GPIOs (in numeric order), pad numbers, pad voltages, pull states, and available configurations. This can be used to help designers define their products' GPIO assignments.
80-NA437-2	*MSM8274/MSM8674/MSM8974 Software Interface* Provides detailed information about the MSM8x74 software interface and its clocks, security, user interface, and registers.
80-NA437-4	*MSM8274/MSM8674/MSM8974 Device Revision Guide* Provides a history of MSM8x74 revisions, explains how to identify the various device revisions, and discusses known issues (or bugs) for each revision and how to work around them.

Table 1-1 Primary MSM8x74 documentation (cont.)

Document number	Title/description
80-NA437-5	*MSM8x74 Chipset (WTR1605/1605L, PM8841, PM8941, WCD9320, WCN3660/3680) Design Guidelines* ■ Detailed functional and interface descriptions for all ICs within the chipsets: □ **MSM8274, MSM8674, or MSM8974 IC** □ WTR1605/WTR1605L RF transceiver IC □ PM8841 and PM8941 power management ICs □ WCD9320 audio codec IC □ WCN3660 wireless connectivity IC ■ Key design guidelines for the chipset are illustrated and explained, including: □ Technology overviews □ DC power distribution □ Interface schematic details □ PCB layout guidelines □ External-component recommendations □ Ground and shielding recommendations

This MSM8x74 device specification is organized as follows:

Chapter 1 Provides an overview of the MSM8x74 documentation, gives a high-level functional description of the device, lists the device features, and defines marking conventions, terms, and acronyms used throughout this document.

Chapter 2 Defines the device pin assignments.

Chapter 3 Defines the device electrical performance specifications, including absolute maximum ratings and recommended operating conditions.

Chapter 4 Provides IC mechanical information, including dimensions, markings, ordering information, moisture sensitivity, and thermal characteristics.

Chapter 5 Discusses shipping, storage, and handling of the MSM8x74.

Chapter 6 Presents procedures and specifications for mounting the MSM8x74 onto printed circuit boards (PCBs).

Chapter 7 Presents MSM8x74 reliability data, including a definition of the qualification samples and a summary of qualification test results.

1.2 MSM8x74 introduction

Mobile devices continue to integrate more and increasingly complex functions, and support more operating bands while maintaining performance, board space, and cost.

These demands are met by Qualcomm's MSM8x74 (Figure 1-1) – with its quad-Krait application processors – which further expand mass-market chipset capabilities by making 3G/4G high-speed data and rich multimedia features accessible to more consumers in developed and developing countries. This multimode solution supports the latest air interface standards including 1xEV-DOrB, 1x Advanced, DC-HSPA+ Cat28, and LTE Cat4 (FDD and TDD) – depending on the IC variant. These air interface technologies achieve downlink and uplink data rates as high as 150 Mbps and 50 Mbps, respectively. Three baseband receiver ports and two baseband transmitter ports enable simultaneous voice and data operation for user multi-tasking. The new MSM8x74 leverages Qualcomm's airlink and multimedia technology leadership to significantly lower the cost of high-performance mobile devices.

The MSM8x74 has a high level of integration that reduces the bill-of-material (BOM), which delivers board-area savings. The package-on-package implementation adds LPDDR3 SDRAM memory without increasing the device's footprint or PCB area. The cost and time-to-market advantages of this IC will help drive wireless broadband adoption in mass markets around the world.

Wireless products based on the MSM8x74 may include:

- Voice and data phones, smartphones, and tablets
- Support for the latest, most-popular operating systems
- Music player-enabled devices and applications
- Camera phones
- Multimedia phones with gaming, streaming video, and video conferencing features
- GPS and GNSS for global location-based services
- Wireless connectivity – Bluetooth, WLAN, FM transceiver with RDS/RBDS, near-field communicator (NFC – via a third-party solution), and digital mobile broadcast (DMB – via a third-party solution)

The MSM8x74 benefits are applied to each of these product types and include:

- Higher integration to reduce PCB surface area, time-to-market, and BOM costs while adding capabilities and processing power
- Integrated quad application processors and hardware cores eliminate multimedia coprocessors, providing superior image quality and resolution for mobile devices while extending application times
  - Higher computational power for high-end features
  - DC power savings enable longer run times
- Position location and navigation systems are supported via the WTR's global navigation satellite system (GNSS) receiver
  - The MSM8x74 supports Gen 8B (GPS and GLONASS) operation supporting Beidou/compass
- Single platform that provides dedicated support for all market-leading codecs and other multimedia formats to support carrier deployments around the world
- DC power reduction using innovative techniques

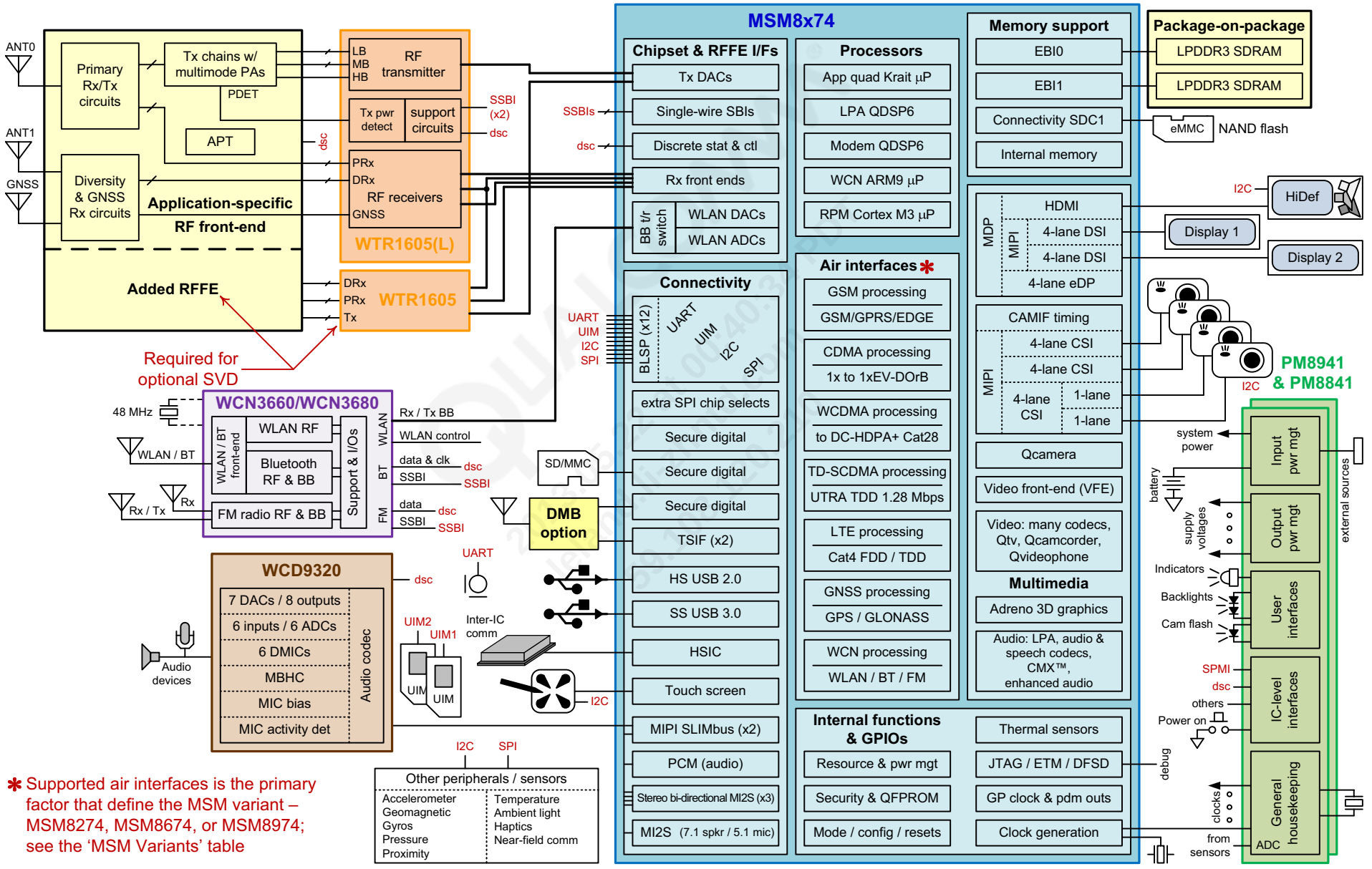


Figure 1-1 MSM8x74 functional block diagram and example application

The MSM8x74 is fabricated using the advanced 28 nm HPm CMOS process, and is available in the the 990B PNSP; a 15 × 15 × 0.74 mm package-on-package (PoP) system (height dimension does not include the memory device) and a 990 PNSP; a 15 × 15 × 0.91 mm package-on-package (PoP) system (height dimension does not include the memory device). Its bottom footprint is equivalent to a 990-pin nanoscale package (990 NSP), and it accepts memory modules from above that are equivalent to a 216-pin chip-scale package (216 CSP) as specified in 80-VP300-5 *Pop Memory for MSM8974 Specification*. The bottom includes many ground pins for improved electrical grounding, mechanical strength, and thermal continuity. See Chapter 2 for pin assignment details and
Chapter 4 for mechanical information.

The MSM8x74 supports high-performance applications worldwide using a variety of wireless networks:

- GERAN MSC 33 (GSM/GPRS/EDGE)
- CDMA 1x, 1x Advanced, 1xEV-DOr0, 1xEV-DOrA, and 1xEV-DOrB
- WCDMA, including Rel 9 DC-HSUPA and Rel 9 DC + MIMO + 64-QAM HSDPA
- TD-SCDMA UTRA TDD (4.2/2.2 Mbps)
- Release 10 LTE Cat4 FDD and TDD
- LTE inter-RAT with WCDMA, TD-SCMDA, GERAN, eHRPD, and 1x
- Simultaneous voice and data (SVD), including SV-LTE and SV-DO
- Carrier aggregation
  - Up to a maximum of two DL carriers paired with one UL carrier
  - FDD LTE
  - Inter-band only
  - Maximum aggregated bandwidth of 20 MHz
- GPS and GNSS

Complementary ICs within the MSM8x74 chipset include:

- Wafer-level RF transceiver: WTR1605 and/or WTR1605L (80-N5420-x documents)
  - Second WTR is added for simultaneous voice and data or LTE carrier aggregation
- Wafer-level RF transceiver: WTR1625 and/or WTR1625L (80-NA805-x documents)
- Wafer-level RF receiver: WFR1620 (80-NA806-x documents)
  - Add LTE carrier aggregation function to WTR1625L
- PA power management: QFE1100/QFE1101 (80-NA681-x documents)
- Power management: PM8841 and PM8941 (80-NA554-x and 80-NA555-x docs, respectively)
- Wireless connectivity, including WLAN, Bluetooth, and FM radio: WCN3660/3680 (80-WL300-x documents)
- Audio codec: WCD9320 (80-NA556-x documents)

The MSM8x74 chipset and system software solution supports the Convergence Platform for mobile applications by leveraging Qualcomm's years of systems expertise and field experience with CDMA, WCDMA, LTE, GSM, TD-SCMDA, and GNSS technologies. Qualcomm works with its partners to develop products that meet the exact needs of the growing wireless market, providing its customers with complete, verifiable solutions, including fully segmented product families, systems software, testing, and support.

Since the MSM8x74 includes so many diverse functions, its operation is more easily understood by considering major functional blocks individually. Therefore, the MSM8x74 document set is organized according to the following block partitioning:

- Architecture and baseband processors
- Memory support
- Air interfaces
- Multimedia
- Connectivity
- Internal functions
- Interfaces to other functions (including the other ICs within the chipset)
- Configurable general-purpose input/output (GPIO) ports

Most of the information contained in this device specification is organized accordingly – including the circuit groupings within its functional block diagram (Figure 1-1), pin descriptions (Chapter 2), and detailed electrical specifications (Chapter 3). Refer to *MSM8x74 Chipset (WTR1605/1605L, PM8841, PM8941, WCD9320, WCN3660/3680) Design Guidelines* (80-NA437-5) for more detailed descriptions of each MSM8x74 function and interface, plus guidelines for implementing your design.

1.2.1 Device variants

The only difference between the MSM variants is the combination of air interfaces supported. All variants are summarized in Table 4-2.

1.3 MSM8x74 features

NOTE Some of the hardware features integrated within the MSM8x74 must be enabled by software. Refer to the latest version of the applicable software release notes to identify the enabled MSM8x74 features.

1.3.1 New features integrated into the MSM8x74

The following new features are integrated into the MSM8x74:

- Quad 2+ GHz Krait application processors with 2 MB L2 cache
- 28 nm HPm process for lower active power dissipation, and faster peak CPU performance
- Dual-channel PoP high-speed memory – LPDDR3 SDRAM up to 800 MHz clock rate
- Two QDSP6 v5 processors (LPASS and modem) at up to 600 MHz core for LPASS and 800 MHz for modem; 200 MHz thread
- 1.5 MB unified SRAM pool on-chip memory (OCMEM)
- Latest air interfaces (including 1x Advanced, 1xEV-DOrB, Rel 9 HSUPA and HSDPA, and Rel 10 LTE Cat4)
- More RF operating bands are supported via the WTR1605/WTR1605L
- Support for three concurrent displays
- Embedded display port (eDP) – v1.2 4-lane
- Support for three 4-lane camera interfaces or up to four camera interfaces (two 4-lane and two 1-lane MIPI_CSIs)
- Dual image signal processing (ISP) – 32 MP at 15 fps, 16 MP at 30 fps, and integrated S3D camera
- Improved video performance – 1080p at 120 fps HD decode, 2 x 1080p at 60 fps encode and decode
- Adreno™ 330 graphics processing unit (GPU)
- Integrated WLAN (a/b/g/n/ac), BT 4.0, FM Rx/Tx (with WCN3660/WCN3680)
- Super-speed USB 3.0
- Previous-generation general serial bus interface (GSBI) ports are replaced by Bus Access Manager (BAM) based low-speed peripheral interface ports (or BLSP interface ports)

1.3.2 Air interface features

This information will be included in future revisions of this document.

1.3.3 Summary of MSM8x74 features

Features of the MSM8x74 are listed in Table 1-2.

Table 1-2 Summary of MSM8x74 features

Feature	MSM8x74 capability
Processors	
Applications	Four Krait µP cores up to 2+ GHz; 2 MB L2 cache
Modem system	QDSP6 v5 core at up to 800 MHz 16k L1 instruction; 32k L1 data; 256k L2 caches
RPM system	Cortex M3 - primary boot processor – Better suited for code certification and warm boot – Brings up secure root of trust (SROT) Krait µP quickly The only master of the modem power manager (MPM) MPM coordinates shutdown/wakeup, clock rates, and VDDs Boot flow is RPM/applications processor-based
Low-power audio	QDSP6 v5 core at 600 MHz; 16k/32k L1 and 256k L2 caches
WLAN/BT/FM	ARM9
Memory support	
System memory via PoP and EBI	2x LPDDR3 SDRAM; 32-bit wide; up to 800 MHz
Other internal memory	1.5 MB unified SRAM pool on-chip memory (OCMEM)
External memory	
Via SDC1	eMMC/SD NAND flash devices
Via SPI	NOR memory devices (user-modified SW)
RF support	
RF operating bands	Defined by WTR device
Air interfaces	See 'Air interface features' section for details
GSM	Yes – all
CDMA	Yes – MSM8674, MSM8974 type 2
WCDMA	Yes – all (supported data rates depend upon MSM variant)
TD-SCDMA	Yes – MSM8274 (both types), MSM8974 type 1
LTE	Yes – MSM8974 (both types)
WLAN/BT/FM	Yes – all (with WCN3660)
GNSS – gpsOne™ engine	Gen 8B; GPS and GLONASS
Multimedia	
Display support	Up to three concurrent displays; two panels + external
MIPI_DSI	Two; 4-lane + 4-lane
HDMI	Yes; v1.4

Table 1-2 Summary of MSM8x74 features (cont.)

Feature	MSM8x74 capability
eDP	Yes; v1.2 4-lane
Example combinations	(2560 × 2048) + (1080p external) (2048 × 1536) + (1920 × 1200) + (1080p external) (2048 × 1536) + (4k × 2k external)
General display features	Color depth – 24-bit pp; TFT, LTPS, CSTN, OLED panels
Camera interfaces	Qcamera; dual ISP
MIPI_CSI	Three 4-lane; 1.5 Gbps per lane
2D performance	32 MP at 15 fps; 16 MP at 30 fps
3D performance	12 MP at 15 to 24 fps; 8 MP at 30 fps
General camera features	Pixel manipulations, camera modes, image effects, and post- processing techniques, including defective pixel correction VFE raw dump of CSI data at line rate to LPDDR3 SMIA++ support I2C or SPI controls
Mobile display processor	MDP 5
Video applications performance	
Encode	1080p at 96 fps; 4kx2k at 30 fps; 4x 1080p at 30 fps – H.264/263, MPEG4, VP8 1080p at 60 fps 2-view – MVC
Decode	1080p at 120 fps; 4kx2k at 30 fps; 4x 1080p at 30 fps – H.264/263, MPEG4/2, WMV9, VC1, VP6/8, DivX, XVID 1080p at 60 fps 2-view – MVC
Graphics	Adreno 330 450 MHz 3D graphics accelerator 3600 M peak 3D pixels/sec APIs include OpenGL ES 1.1/2.0/3.0, DX9.3
Audio	
Codec	Integrated within the WCD9320 device: 7 DACs, 8 outputs; 6 inputs, 6 ADCs; 6 digital MICs Multibutton headset control; MIC activity detection
Low-power audio	Low-power, low-complexity; 7.1 surround sound Versatile – many audio playback & voice modes; encoders for audio AND FM recording; many concurrency modes
Voice codec support	SILK; QCELP, EVRC, EVRC-B, EVRC-WB; G.711, G.729A/AB; GSM-FR, -EFR, -HR; AMR-NB, -WB
Audio codec support	MP3; AAC, +, eAAC; WMA 9/Pro; Dolby AC-3, eAC-3, DTS
Enhanced audio	Surround sound: Dolby TrueHD; DTS-HD; DTS Express 7.1 Fluence™ Noise Cancellation; enhanced speaker protection QAudioFX™ / Qconcert™ / QEnsemble

Table 1-2 Summary of MSM8x74 features (cont.)

Feature	MSM8x74 capability
A/V output – HDMI Rev 1.4a	Yes Integrated HDMI Tx core and HDMI PHY 1080p at 60 Hz refresh; 24-bit RGB color Up to 8-channel audio for 7.1 surround sound Dolby Digital Plus, Dolby True-HD, & DTS-HD Master
Web technologies	V8 JavaScript engine optimizations Webkit browser JPEG hardware decode acceleration Networking Stack IP and HTTP tuning Flash 10.1 and video processor decode optimization
Messaging	Text messages; text encoding for SMS Multimedia messaging services – combined video (MPEG4), still image (JPEG), voice tag (AMR), text sent as message
Digital Mobile Broadcast (DMB)	External IC required; dual-TSIF for 12 segment ISDB-T
Connectivity	
BLSP ports	12, 4 bits each; multiplexed serial interface functions
UART	Yes – up to 4 MHz
UIM	Yes – SIM, USIM, CSIM; dual V (1.8/2.85) is available 1x
I2C	Yes – cameras, sensors, near field communicator (NFC), etc.
SPI (master only)	Yes – cameras, sensors, etc.; NOR memory with SW mods
UIM (other than via BLSP)	Two – dual voltage (1.8/2.85 V)
USB	Two – one USB 2.0 high-speed and one USB 3.0 super-speed/USB 2.0 high-speed compliant
HSIC	MSM to/from external application processor
Dual-voltage (1.2/1.8)	Easy integration, low-power, and low processor loading
Secure digital interfaces	Up to 4 ports; one 8-bit and three 4-bit; SD 3.0
SDC1 and SDC2 are dual-V	SD/MMC card; eMMC NAND; DMB; WLAN; eSD/eMMC boot
TSIF	Up to two ports; DMB support
Audio interfaces	
SLIMbus	Highly multiplexed, high-speed; baseline WCD interface
I2S	Bi-directional stereo MI2S (x3)
MI2S	Up to 8 channels for multi channel audio applications
PCM	Short and long sync PCM support

Table 1-2 Summary of MSM8x74 features (cont.)

Feature	MSM8x74 capability
Wireless connectivity	WCN3660 or WCN3680
WLAN	Both WCNs support 802.11a/b/g/n; WCN3680 adds 802.11/ac
Bluetooth	BT 4.0 LE and earlier
FM radio	Worldwide broadcast
Touchscreen support	Capacitive panels via ext IC (I2C, SPI, & interrupts)
DMB support	Via external DMB device (SDC or TSIF)
Configurable GPIOs	
Number of GPIO ports	146 – GPIO_0 to GPIO_145
Input configurations	Pull-up, pull-down, keeper, or no pull
Output configurations	Programmable drive current
Top-level mode multiplexer	Provides a convenient way to program groups of GPIOs
Internal functions	
Security	
General security features	Secure boot, SFS, OMA DRM 1.0/2.1, ARM TrustZone, SEE, secure debug, Microsoft WM DRM10, HDCP for HDMI
Crypto engine	V4; algorithm accelerate file system encryption (AES-XTS) and IPSec and SSL (HMAC-SHA, CCM, CBCMAC)
QFPROM	Large fuse array, replaces previous-generation Qfuse chains Nonvolatile memory with faster and simpler programming
Security controller	Chip-wide configuration for security, feature enable, & debug Persistent storage of ID numbers and sensitive key data Support for the HDCP standard needed for HDMI Secure HDCP key provisioning and secure debug facility Gateway for all software and JTAG accesses to the QFPROM Primary and secondary hardware key blocking for SFS
Boot sequence	1) RPM system, 2) application system, 3) modem system Emergency boot over HS-USB Poweron boot to carrier splash screen < 0.4 seconds (target) Poweron boot to network access < 20 seconds (target)
PLLs and clocks	Multiple clock regimes; watchdog & sleep timers Inputs: 19.2 M CXO, 48M WCN_XO for 5 GHz WLAN General-purpose outputs: M/N counter, PDM
Resource and power manager	Fundamental to bootup and power management Key blocks: RPM core, Cortex M3, security controller, MPM Improved efficiency via clock control, split-rail power collapse and voltage scaling; several low-power sleep modes
Debug	JTAG, Design for Software Debug (DFSD), and ETM (all cores)
Others	Thermal sensors; modes & resets; peripheral subsystem

Table 1-2 Summary of MSM8x74 features (cont.)

Feature	MSM8x74 capability
Chipset and RF front-end (RFFE) interface features	
WTR RF transceivers	
Baseband data	4 Rx and 2 Tx analog interfaces
Status and control	2 SSBIs for each RFIC, plus other lines as needed via GPIOs
Power management	2-line SPMI; plus other lines as needed via GPIOs
WCD audio codec	
SLIMbus	Highly muxed, high-speed audio data plus status & control
Legacy	Optional I2S for audio data plus I2C for status & control
Others	Status, control, & clock lines as needed via GPIOs
WCN wireless connectivity	
WLAN baseband data	Multiplexed Rx/Tx analog interface
WLAN status & control	Secure digital
Bluetooth	2-line data interface plus dedicated SSBI
FM radio	1-line data interface plus dedicated SSBI
Fabrication technology and package	
Digital die	28 nm HPm CMOS
Moulded Laser PoP - small, thermally efficient package	990 PNSP: 15 × 15 × 0.91 mm (w/o memory device on top)
Bottom pin array of PoP	Same as 990-pin nanoscale pkg (990 NSP); 0.4 mm pitch
Top pin array of PoP	Same as 216-pin chipscale pkg (216 CSP); 0.5 mm pitch
Bare Die PoP - small, thermally efficient package	990B PNSP: 15 × 15 × 0.74 mm (w/o memory device on top)
Bottom pin array of PoP	Same as 990-pin nanoscale pkg (990 NSP); 0.4 mm pitch
Top pin array of PoP	Same as 216-pin chipscale pkg (216 CSP); 0.5 mm pitch

1.4 Terms and acronyms

Table 1-3 defines terms and acronyms commonly used throughout this document.

Table 1-3 Terms and acronyms

Term	Definition
ADC	Analog-to-digital converter
AGC	Automatic gain control
BDP	Bare Die PoP
BER	Bit error rate
bps	Bits per second
BPNSP	Bare Die Package-on-package Nanoscale Package
BT	Bluetooth
CDMA	Code division multiple access
CRC	Cyclic redundancy code
CSI	Camera serial interface
DAC	Digital-to-analog converter
DC-HSPA+	Dual-carrier HSPA+
DDR	Double data rate
DMB	Digital mobile broadcast
DRM	Digital Rights Management
DSI	Display serial interface
DSP	Digital signal processor
EBI	External bus interface
EDGE	Enhanced data rates for GSM evolution
EDR	Enhanced data rate
ETM	Embedded trace macrocell
EV-DO	Evolution data optimized
FDD	Frequency division duplex
GLONASS	Global orbiting navigation satellite system
GNSS	Global navigation satellite system
GPIO	General-purpose input/output
GPRS	General packet radio services
GPS	Global positioning system
GPU	Graphics processing unit
GRFC	Generic RF controller
GSM	Global system for mobile communications
HDCP	High-bandwidth digital content protection
HDMI	High-definition multimedia interface

Table 1-3 Terms and acronyms (cont.)

Term	Definition
HSDPA	High-speed downlink packet access
HSIC	High-speed inter-chip
HSPA+	High-speed packet access
HSUPA	High-speed uplink packet access
I2C	Inter-integrated circuit
I2S	Inter-IC sound
ISP	Image signal processing
JPEG	Joint Photographic Experts Group
JTAG	Joint Test Action Group (ANSI/ICEEE Std. 1149.1-1990)
kbps	kilobits per second
LCD	Liquid crystal display
LPA	Low-power audio
LPASS	Low-power audio subsystem
LPDDR	Low-power DDR
LSB	Defines whether the LSB is the least significant bit or least significant byte. All instances of LSB used in this manual are assumed to be LSByte, unless otherwise specified.
MBP	Mobile broadcast platform
MDP	Mobile display processor
MIPI	Mobile industry processor interface
MLP	Molded Laser PoP
MMC	Multimedia card
MPM	Modem power management
MSB	Defines whether the MSB is the most significant bit or most significant byte. All instances of MSB used in this manual are assumed to be MSByte, unless otherwise specified.
MTP	Modem Test Platform
NFC	Near field communicator
NSP	Nanoscale package
OMA	Open Mobile Alliance
PA	Power amplifier
PDM	Pulse-density modulation
PM	Power management
PNSP	Package-on-package nanoscale package
PoP	Package-on-package
PVS	Process Voltage Scaling
QTI	Qualcomm Technologies, Inc.
QFPROM	Qualcomm fuse programmable read-only memory

Table 1-3 Terms and acronyms (cont.)

Term	Definition
QLIC	Quasi-linear interference cancellation
radioOne™	Zero-IF (ZIF) radio architecture
RBDS	Radio broadcast data system
RDS	Radio data system
RGB	Red-green-blue
RLP	Radio link protocol
RPM	Resource power manager
SBI	Serial bus interface
SD	Secure digital
SDC	Secure digital controller
SEE	Secure Execution Environment
SFS	Secure file system
SIM	Subscriber identity module
SMT	Surface mount technology
SPI	Serial peripheral interface
sps	Symbols per second (or samples per second)
SPSS	Smart peripheral subsystem
SSBI	Single-wire SBI
TAP	Test access port
TCXO	Temperature-compensated crystal oscillator
TDD	Time division duplexing
TSIF	Transport stream interface
UART	Universal asynchronous receiver transmitter
UICC	Universal integrated circuit card
UIM	User identity module
UMTS	Universal mobile telecommunications system
USB	Universal serial bus
USB-OTG	Universal serial bus on-the-go
USIM	UMTS subscriber identity module
WCDMA	Wideband code division multiple access
WCN	Wireless connectivity network
WLAN	Wireless local area network
WTR	Wafer-scale RF transceiver
XO	Crystal oscillator
ZIF	Zero intermediate frequency

1.5 Special marks

Table 1-4 defines special marks used in this document.

Table 1-4 Special marks

Mark	Definition
[ ]	Brackets ([ ]) sometimes follow a pin, register, or bit name. These brackets enclose a range of numbers. For example, DATA[7:4] may indicate a range that is 4 bits in length, or DATA[7:0] may refer to all eight DATA pins.
_N	A suffix of _N indicates an active low signal. For example, RESIN_N.
0x0000	Hexadecimal numbers are identified with an x in the number (for example, 0x0000). All numbers are decimal (base 10) unless otherwise specified. Non-obvious binary numbers have the term binary enclosed in parentheses at the end of the number; for example, 0011 (binary).
|	A blue vertical bar in the outside margin of a page indicates that a change was made since the previous revision of this document.

2 Pin Definitions

The MSM8x74 is the lower device within a package-on-package system, as illustrated and explained in Figure 2-1.

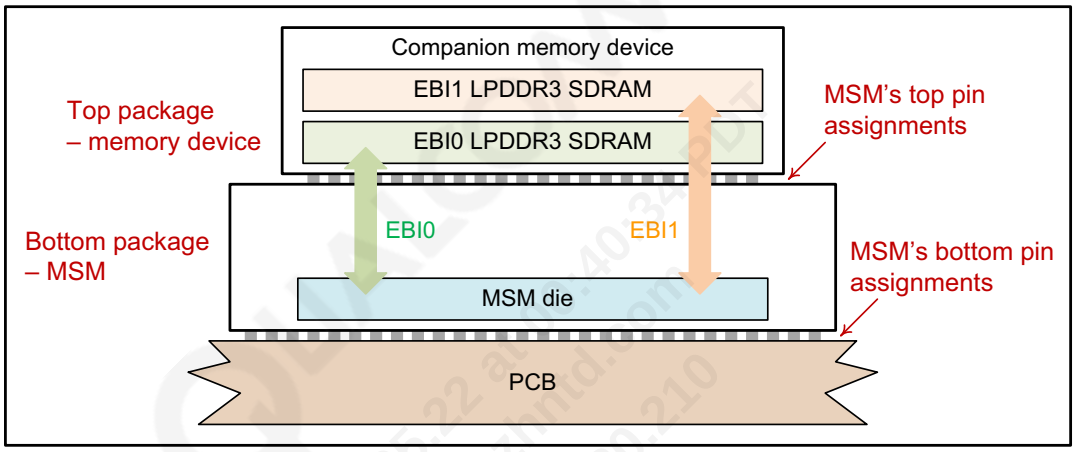


Figure 2-1 Package-on-package system pin assignments

Two sets of pin assignment details are presented in this chapter:

- MSM8x74 bottom pins (Section 2.2)
- MSM8x74 top pins (Section 2.3)

2.1 I/O parameter definitions

Table 2-1 I/O description (pad type) parameters

Symbol	Description
Pad attribute	
AI	Analog input (does not include pad circuitry)
AO	Analog output (does not include pad circuitry)
B	Bidirectional digital with CMOS input
DI	Digital input (CMOS)
DO	Digital output (CMOS)
H	High-voltage tolerant
S	Schmitt trigger input
Z	High-impedance (high-Z) output
Pad pull details for digital I/Os	
nppdpukp	Programmable pull resistor. The default pull direction is indicated using capital letters and is a prefix to other programmable options: NP: pdpukp = default no-pull with programmable options following the colon (:) PD: nppukp = default pull-down with programmable options following the colon (:) PU: nppdkp = default pull-up with programmable options following the colon (:) KP: nppdpu = default keeper with programmable options following the colon (:)
KP	Contains an internal weak keeper device (keepers cannot drive external buses)
NP	Contains no internal pull
PU	Contains an internal pull-up device
PD	Contains an internal pull-down device
Pad voltage groupings for baseband circuits	
P1	Pad group 1 (EBI for PoP memory); tied to VDD_P1 pins (1.2 V only)
P2	Pad group 2 (SDC2); tied to VDD_P2 pins (1.8 V or 2.95 V)
P3	Pad group 3 (most peripherals); tied to VDD_P3 pins (1.8 V only)
P4	Pad group 4 (HSIC); tied to VDD_P4 pins (1.2 V or 1.8 V)
P5	Pad group 5 (UIM1); tied to VDD_P5 pins (1.8 V or 2.95 V)
P6	Pad group 6 (UIM2); tied to VDD_P6 pins (1.8 V or 2.95 V)
P7	Pad group 7 (SDC1); tied to VDD_P7 pins (1.2 V or 1.8 V)
CSI	Supply voltage for MIPI_CSI circuits and I/Os; tied to VDD_MIPI_CSI (1.8 V only)
DSI	Supply voltage for MIPI_DSI I/Os; tied to VDD_MIPI_DSI_1P8 (1.8 V only)
Output current drive strength	
EBI pads	Pads for EBI are tailored for 1.2 V interfaces and are source terminated. These pads can support output impedances from 24 Ω to 80 Ω as specified in the Jedec standard. See Section 3.8.1 for more details.
3.0 V (H) pads	Programmable drive strength, for UIM1 and UIM2 1.5 to 12 mA in steps of 1.5 mA

Table 2-1 I/O description (pad type) parameters (cont.)

Symbol	Description
UIM pads (1.8 V)	Programmable drive strength, 1 to 8 mA in 1 mA steps
Others [1]	Programmable drive strength, 2 to 16 mA in 2 mA steps

1. Digital pads other than EBI pads or high-voltage tolerant pads.

2.2 Pin assignments – MSM bottom

2.2.1 Pin map – MSM bottom

The MSM8x74 uses the 990 PNSP package; its bottom surface is equivalent to the 990 NSP. See Chapter 4 for package details, and Section 2.3 for information about the top pin assignments. A high-level view of the bottom pin assignments is shown in Figure 2-3. The pins are colored to indicate which function type they support, as defined in Figure 2-2.

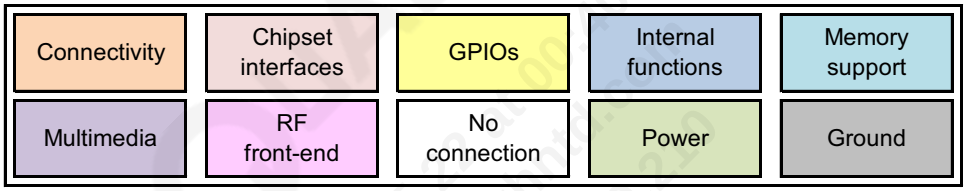


Figure 2-2 MSM8x74 bottom pin assignments – legend

The text within Figure 2-3 is difficult to read when viewing an 8½" × 11" hard copy. Other viewing options are available:

- Print that one page on a 11" × 17" sheet.
- View the graphic soft copy and zoom in – the resolution is sufficient for comfortable reading.
- Download the *MSM8274/MSM8674/MSM8974 Pin Assignment Spreadsheet* (80-NA437-1A) – this Microsoft Excel spreadsheet lists all MSM8x74 pad numbers (in alphanumeric order), pad names, pad voltages, pad types, and functional descriptions.

NOTE Click the link below to download the pin assignment spreadsheet (80-N7379-1A) from the CDMATech Support Website.

This link will be included in future revisions of this document.

If you have permission to view the document, a prompt will be presented for initiating the download.

NOTE Subscribe to the pin assignment spreadsheet to be notified of any changes.

Click the **Help** button to download the latest revision of *Using CDMATech Support Documents and Downloads User Guide* (80-V7273-1). This document includes subscription instructions.

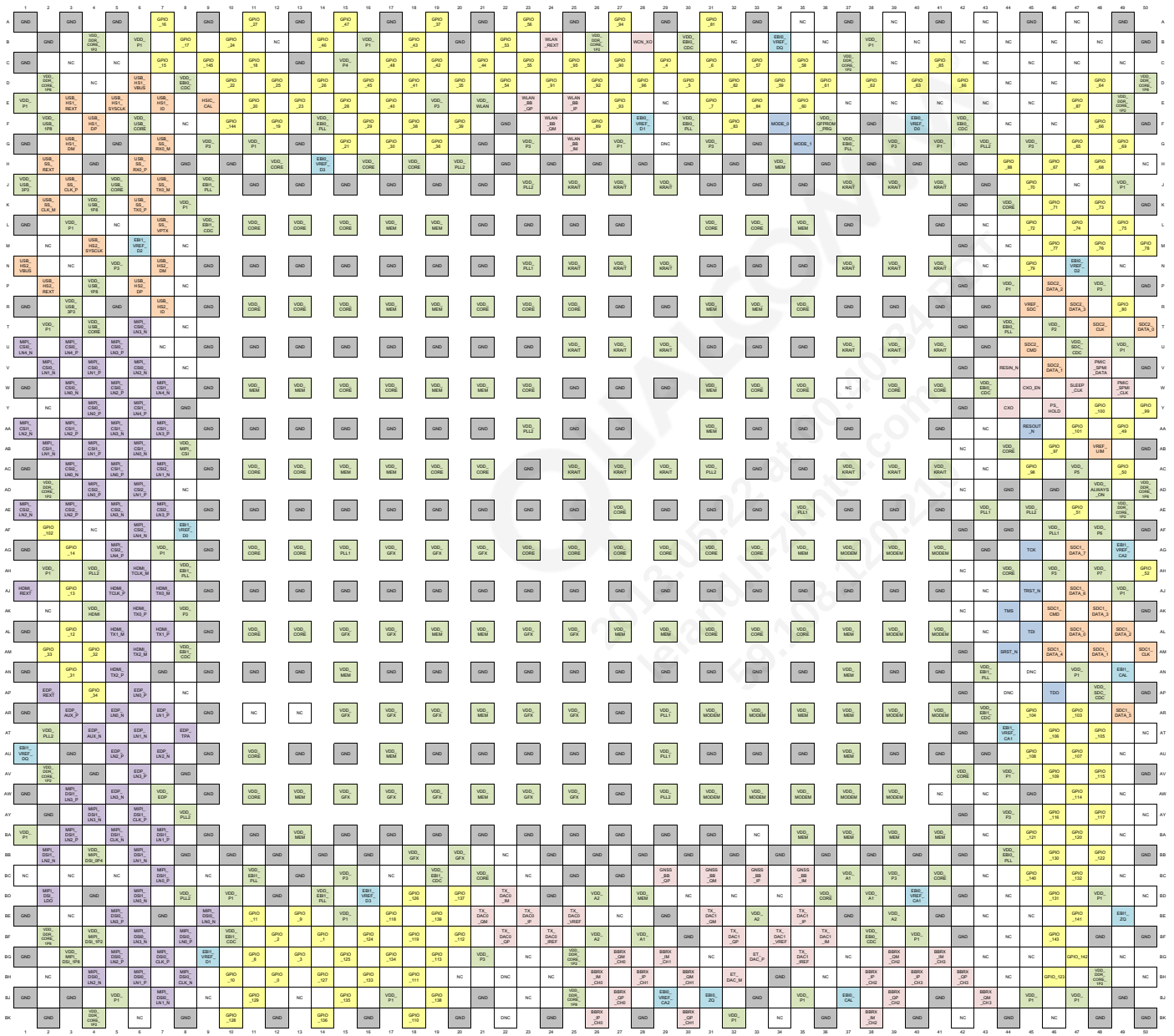


Figure 2-3 High-level view of MSM8x74 bottom pin assignments

2.2.2 Pin descriptions – MSM bottom

Descriptions of bottom pins are presented in the following tables, organized by functional group:

Table 2-2: Memory support functions

Table 2-3: Multimedia functions

Table 2-4: Connectivity functions

Table 2-5: BLSP configurations

Table 2-6: Internal functions

Table 2-7: Wakeup pins for modem power management

Table 2-9: Chipset interface functions

Table 2-10: RF front-end interface functions

Table 2-11: General-purpose input/output ports

Table 2-12: No connection, do not connect, and reserved pins

Table 2-13: Power supply pins

Table 2-14: Ground pins

Table 2-2 Pin descriptions – memory support functions

Pad #	Pad name and/or function	Pad name or alt function	Pad characteristics [1]		Functional description
			Voltage	Type	
EBI0 for PoP LPDDR3 SDRAM					
BJ37	EBI0_CAL		–	AI	EBI0 LPDDR3 calibration resistor
BD40	EBI0_VREF_CA1		–	AI	EBI0 LPDDR3 CA reference voltage (bottom)
BJ29	EBI0_VREF_CA2		–	AI	EBI0 LPDDR3 CA reference voltage (top)
B34	EBI0_VREF_DQ		–	AI	EBI0 LPDDR3 DQ reference voltage
H14	EBI0_VREF_D3		–	AI	EBI0 LPDDR3 D3 reference voltage
N47	EBI0_VREF_D2		–	AI	EBI0 LPDDR3 D2 reference voltage
F28	EBI0_VREF_D1		–	AI	EBI0 LPDDR3 D1 reference voltage
F40	EBI0_VREF_D0		–	AI	EBI0 LPDDR3 D0 reference voltage
BJ31	EBI0_ZQ		–	AI	EBI0 LPDDR3 ZQ resistor
EBI1 for PoP LPDDR3 SDRAM					
AN49	EBI1_CAL		–	AI	EBI1 LPDDR3 calibration resistor
AT44	EBI1_VREF_CA1		–	AI	EBI1 LPDDR3 CA reference voltage (bottom)
AG49	EBI1_VREF_CA2		–	AI	EBI1 LPDDR3 CA reference voltage (top)
AU1	EBI1_VREF_DQ		–	AI	EBI1 LPDDR3 reference voltage for PoP
BD16	EBI1_VREF_D3		–	AI	EBI1 LPDDR3 D3 reference voltage
M6	EBI1_VREF_D2		–	AI	EBI1 LPDDR3 D2 reference voltage
BG9	EBI1_VREF_D1		–	AI	EBI1 LPDDR3 D1 reference voltage
AF8	EBI1_VREF_D0		–	AI	EBI1 LPDDR3 D0 reference voltage

Table 2-2 Pin descriptions – memory support functions (cont.)

Pad #	Pad name and/or function	Pad name or alt function	Pad characteristics [1]		Functional description
			Voltage	Type	
BE49	EBI1_ZQ		–	AI	EBI1 LPDDR3 ZQ resistor
SDC1 is available for eMMC NAND flash – see Table 2-4					

1. Refer to Table 2-1 for parameter and acronym definitions.

Table 2-3 Pin descriptions – multimedia functions

Pad #	Pad name and/or function	Pad name or alt function	Pad characteristics [1]		Functional description
			Voltage	Type	
Camera serial interface – 4-lane MIPI_CSI0					
U3	MIPI_CSI0_LN4_P		CSI	AI, AO	MIPI camera serial interface 0 lane 4 – positive
U1	MIPI_CSI0_LN4_N		CSI	AI, AO	MIPI camera serial interface 0 lane 4 – negative
U5	MIPI_CSI0_LN3_P		CSI	AI, AO	MIPI camera serial interface 0 lane 3 – positive
T6	MIPI_CSI0_LN3_N		CSI	AI, AO	MIPI camera serial interface 0 lane 3 – negative
W5	MIPI_CSI0_LN2_P		CSI	AI, AO	MIPI camera serial interface 0 lane 2 – positive
V6	MIPI_CSI0_LN2_N		CSI	AI, AO	MIPI camera serial interface 0 lane 2 – negative
V4	MIPI_CSI0_LN1_P	 MIPI_CSI0_CLK_P	CSI CSI	AI, AO AI	MIPI camera serial interface 0 lane 1 – positive MIPI camera serial interface 0 clock – positive
V2	MIPI_CSI0_LN1_N	 MIPI_CSI0_CLK_N	CSI CSI	AI, AO AI	MIPI camera serial interface 0 lane 1 – negative MIPI camera serial interface 0 clock – negative
Y4	MIPI_CSI0_LN0_P		CSI	AI, AO	MIPI camera serial interface 0 lane 0 – positive
W3	MIPI_CSI0_LN0_N		CSI	AI, AO	MIPI camera serial interface 0 lane 0 – negative
Camera serial interface – 4-lane MIPI_CSI1					
Y6	MIPI_CSI1_LN4_P		CSI	AI, AO	MIPI camera serial interface 1 lane 4 – positive
W7	MIPI_CSI1_LN4_N		CSI	AI, AO	MIPI camera serial interface 1 lane 4 – negative
AA7	MIPI_CSI1_LN3_P		CSI	AI, AO	MIPI camera serial interface 1 lane 3 – positive
AA5	MIPI_CSI1_LN3_N		CSI	AI, AO	MIPI camera serial interface 1 lane 3 – negative
AA3	MIPI_CSI1_LN2_P		CSI	AI, AO	MIPI camera serial interface 1 lane 2 – positive
AA1	MIPI_CSI1_LN2_N		CSI	AI, AO	MIPI camera serial interface 1 lane 2 – negative
AB4	MIPI_CSI1_LN1_P	 MIPI_CSI1_CLK_P	CSI CSI	AI, AO AI	MIPI camera serial interface 1 lane 1 – positive MIPI camera serial interface 1 clock – positive
AB2	MIPI_CSI1_LN1_N	 MIPI_CSI1_CLK_N	CSI CSI	AI, AO AI	MIPI camera serial interface 1 lane 1 – negative MIPI camera serial interface 1 clock – negative
AC5	MIPI_CSI1_LN0_P		CSI	AI, AO	MIPI camera serial interface 1 lane 0 – positive
AB6	MIPI_CSI1_LN0_N		CSI	AI, AO	MIPI camera serial interface 1 lane 0 – negative
Camera serial interface – 4-lane MIPI_CSI2					
AG5	MIPI_CSI2_LN4_P		CSI	AI, AO	MIPI camera serial interface 2 lane 4 – positive
AF6	MIPI_CSI2_LN4_N		CSI	AI, AO	MIPI camera serial interface 2 lane 4 – negative
AE7	MIPI_CSI2_LN3_P		CSI	AI, AO	MIPI camera serial interface 2 lane 3 – positive
AE5	MIPI_CSI2_LN3_N		CSI	AI, AO	MIPI camera serial interface 2 lane 3 – negative
AE3	MIPI_CSI2_LN2_P		CSI	AI, AO	MIPI camera serial interface 2 lane 2 – positive
AE1	MIPI_CSI2_LN2_N		CSI	AI, AO	MIPI camera serial interface 2 lane 2 – negative

Table 2-3 Pin descriptions – multimedia functions (cont.)

Pad #	Pad name and/or function	Pad name or alt function	Pad characteristics [1]		Functional description
			Voltage	Type	
AD6	MIPI_CSI2_LN1_P	MIPI_CSI2_CLK_P	CSI CSI	AI, AO AI	MIPI camera serial interface 2 lane 1 – positive MIPI camera serial interface 2 clock – positive
AC7	MIPI_CSI2_LN1_N	MIPI_CSI2_CLK_N	CSI CSI	AI, AO AI	MIPI camera serial interface 2 lane 1 – negative MIPI camera serial interface 2 clock – negative
AD4	MIPI_CSI2_LN0_P		CSI	AI, AO	MIPI camera serial interface 2 lane 0 – positive
AC3	MIPI_CSI2_LN0_N		CSI	AI, AO	MIPI camera serial interface 2 lane 0 – negative
Camera serial interface – MIPI_CSI1 reconfigured to support 1-lane + 1-lane					
This information will be included in future revisions of this document.					
Camera-related timing signals					
C7	CAM_MCLK0	GPIO_15	P3	DO B-PD:nppukp	Camera master clock 0 Configurable I/O
A7	CAM_MCLK1	GPIO_16	P3	DO B-PD:nppukp	Camera master clock 1 Configurable I/O
B8	CAM_MCLK2	GPIO_17	P3	DO B-PD:nppukp	Camera master clock 2 Configurable I/O
C11	CAM_MCLK3	GPIO_18	P3	DO B-PD:nppukp	Camera master clock 3 Configurable I/O
F12	CCI_I2C0_SDA	GPIO_19	P3	DO B-PD:nppukp	Dedicated camera control interface I2C 0 serial data Configurable I/O
E11	CCI_I2C0_SCL	GPIO_20	P3	DO B-PD:nppukp	Dedicated camera control interface I2C 0 clock Configurable I/O
G15	CCI_I2C1_SDA	GPIO_21	P3	DO B-PD:nppukp	Dedicated camera control interface I2C 1 serial data Configurable I/O
D10	CCI_I2C1_SCL	GPIO_22	P3	DO B-PD:nppukp	Dedicated camera control interface I2C 1 clock Configurable I/O
E13	CCI_TIMER0	GPIO_23	P3	DO B-PD:nppukp	Camera control interface timer 0 Configurable I/O
B10	CCI_TIMER1	GPIO_24	P3	DO B-PD:nppukp	Camera control interface timer 1 Configurable I/O
D12	CCI_TIMER2	GPIO_25	P3	DO B-PD:nppukp	Camera control interface timer 2 Configurable I/O
D14	CCI_TIMER3	GPIO_26	P3	DO B-PD:nppukp	Camera control interface timer 3 Configurable I/O
A11	CCI_TIMER4	GPIO_27	P3	DO B-PD:nppukp	Camera control interface timer 4 Configurable I/O
E15	CCI_ASYNC0	GPIO_28	P3	DI B-PD:nppukp	Camera control interface async 0 Configurable I/O
D14	CCI_ASYNC1	GPIO_26	P3	DI B-PD:nppukp	Camera control interface async 1 Configurable I/O
A11	CCI_ASYNC2	GPIO_27	P3	DI B-PD:nppukp	Camera control interface async 2 Configurable I/O

Table 2-3 Pin descriptions – multimedia functions (cont.)

Pad #	Pad name and/or function	Pad name or alt function	Pad characteristics [1]		Functional description
			Voltage	Type	
Mobile display processor (MDP) vertical sync					
AL3	MDP_VSYNC_P	GPIO_12	P3	DI B-PD:nppukp	MDP vertical sync – primary Configurable I/O
AJ3	MDP_VSYNC_S	GPIO_13	P3	DI B-PD:nppukp	MDP vertical sync – secondary Configurable I/O
AG3	MDP_VSYNC_E	GPIO_14	P3	DI B-PD:nppukp	MDP vertical sync – external Configurable I/O
Display serial interface – 4-lane MIPI_DSI0					
BG7	MIPI_DSI0_CLK_P		DSI	AO	MIPI display serial interface 0 clock – positive
BH8	MIPI_DSI0_CLK_N		DSI	AO	MIPI display serial interface 0 clock – negative
BE5	MIPI_DSI0_LN3_P		DSI	AI, AO	MIPI display serial interface 0 lane 3 – positive
BF6	MIPI_DSI0_LN3_N		DSI	AI, AO	MIPI display serial interface 0 lane 3 – negative
BG5	MIPI_DSI0_LN2_P		DSI	AI, AO	MIPI display serial interface 0 lane 2 – positive
BH4	MIPI_DSI0_LN2_N		DSI	AI, AO	MIPI display serial interface 0 lane 2 – negative
BH6	MIPI_DSI0_LN1_P		DSI	AI, AO	MIPI display serial interface 0 lane 1 – positive
BJ7	MIPI_DSI0_LN1_N		DSI	AI, AO	MIPI display serial interface 0 lane 1 – negative
BF8	MIPI_DSI0_LN0_P		DSI	AI, AO	MIPI display serial interface 0 lane 0 – positive
BE9	MIPI_DSI0_LN0_N		DSI	AI, AO	MIPI display serial interface 0 lane 0 – negative
BD2	MIPI_DSI_LDO		DSI	AI, AO	MIPI DSI low-dropout regulator (DSI0/DSI1 shared)
Display serial interface – 4-lane MIPI_DSI1					
AY6	MIPI_DSI1_CLK_P		DSI	AO	MIPI display serial interface 1 clock – positive
BA5	MIPI_DSI1_CLK_N		DSI	AO	MIPI display serial interface 1 clock – negative
AW3	MIPI_DSI1_LN3_P		DSI	AI, AO	MIPI display serial interface 1 lane 3 – positive
AY4	MIPI_DSI1_LN3_N		DSI	AI, AO	MIPI display serial interface 1 lane 3 – negative
BA3	MIPI_DSI1_LN2_P		DSI	AI, AO	MIPI display serial interface 1 lane 2 – positive
BB2	MIPI_DSI1_LN2_N		DSI	AI, AO	MIPI display serial interface 1 lane 2 – negative
BA7	MIPI_DSI1_LN1_P		DSI	AI, AO	MIPI display serial interface 1 lane 1 – positive
BB6	MIPI_DSI1_LN1_N		DSI	AI, AO	MIPI display serial interface 1 lane 1 – negative
BC7	MIPI_DSI1_LN0_P		DSI	AI, AO	MIPI display serial interface 1 lane 0 – positive
BD6	MIPI_DSI1_LN0_N		DSI	AI, AO	MIPI display serial interface 1 lane 0 – negative
BD2	MIPI_DSI_LDO		DSI	AI, AO	MIPI DSI low-dropout regulator (DSI0/DSI1 shared)
High-definition multimedia interface (HDMI)					
AJ5	HDMI_TCLK_P		–	AO	HDMI differential clock – plus
AH6	HDMI_TCLK_M		–	AO	HDMI differential clock – minus
AN5	HDMI_TX2_P		–	AO	HDMI differential transmit 2 – plus
AM6	HDMI_TX2_M		–	AO	HDMI differential transmit 2 – minus
AL7	HDMI_TX1_P		–	AO	HDMI differential transmit 1 – plus
AL5	HDMI_TX1_M		–	AO	HDMI differential transmit 1 – minus
AK6	HDMI_TX0_P		–	AO	HDMI differential transmit 0 – plus
AJ7	HDMI_TX0_M		–	AO	HDMI differential transmit 0 – minus

Table 2-3 Pin descriptions – multimedia functions (cont.)

Pad #	Pad name and/or function	Pad name or alt function	Pad characteristics [1]		Functional description
			Voltage	Type	
AJ1	HDMI_REXT		–	AI, AO	HDMI external calibration resistor
AN3	HDMI_CEC	GPIO_31	P3	B B-PU:nppdkp	HDMI consumer electronics control Configurable I/O
AM4	HDMI_DDC_CLK	GPIO_32	P3	B B-PU:nppdkp	HDMI display data channel – clock Configurable I/O
AM2	HDMI_DDC_DATA	GPIO_33	P3	B B-PU:nppdkp	HDMI display data channel – data Configurable I/O
AP4	HDMI_HPLUG_DET	GPIO_34	P3	DI B-PD:nppukp	HDMI hot plug detect Configurable I/O
Embedded display port (eDP)					
AR3	EDP_AUX_P		–	AI, AO	Embedded display port auxiliary channel – positive
AT4	EDP_AUX_N		–	AI, AO	Embedded display port auxiliary channel – negative
AV6	EDP_LN3_P		–	AI, AO	Embedded display port lane 3 – positive
AW5	EDP_LN3_N		–	AI, AO	Embedded display port lane 3 – negative
AU5	EDP_LN2_P		–	AI, AO	Embedded display port lane 2 – positive
AU7	EDP_LN2_N		–	AI, AO	Embedded display port lane 2 – negative
AR7	EDP_LN1_P		–	AI, AO	Embedded display port lane 1 – positive
AT6	EDP_LN1_N		–	AI, AO	Embedded display port lane 1 – negative
AP6	EDP_LN0_P		–	AI, AO	Embedded display port lane 0 – positive
AR5	EDP_LN0_N		–	AI, AO	Embedded display port lane 0 – negative
AP2	EDP_REXT		–	AI, AO	Embedded display port – external resistor
AT8	EDP_TPA		–	AI, AO	Embedded display port – test adaptor
Also see Table 2-4 for connectivity ports that are used for multimedia applications: *Audio – SLIMbus, I2S, MI2S, PCM; DMB – TSIF, SDC; controls – I2C, SPI*					

1. Refer to Table 2-1 for parameter and acronym definitions.

NOTE GPIO pins can support multiple functions. To assign GPIOs to particular functions (such as the options listed in the table above), designers must identify all their application's requirements and map each GPIO to its function – carefully avoiding conflicts in GPIO assignments. Refer to Table 2-11 for a list of all supported functions for each GPIO.

Table 2-4 Pin descriptions – connectivity functions

Pad #	Pad name and/or function	Pad name or alt function	Pad characteristics [2]		Functional description
			Voltage	Type	
Super-speed USB 3.0 (USB_SS)					
J3	USB_SS_CLK_P		–	AI	USB super-speed clock – plus
K2	USB_SS_CLK_M		–	AI	USB super-speed clock – minus
H6	USB_SS_RX0_P		–	AI	USB super-speed receive – plus
G7	USB_SS_RX0_M		–	AI	USB super-speed receive – minus
K6	USB_SS_TX0_P		–	AO	USB super-speed transmit – plus

Table 2-4 Pin descriptions – connectivity functions (cont.)

Pad #	Pad name and/or function	Pad name or alt function	Pad characteristics [2]		Functional description
			Voltage	Type	
J7	USB_SS_TX0_M		–	AO	USB super-speed transmit – minus
L7	USB_SS_VPTX		–	AI	USB super-speed transmit – quiet Tx supply
H2	USB_SS_REXT		–	AI, AO	USB super-speed transmit – external resistor
High-speed USB 2.0 (USB_HS1)					
F4	USB_HS1_DP		–	AI, AO	USB high-speed 1 data – plus
G3	USB_HS1_DM		–	AI, AO	USB high-speed 1 data – minus
D6	USB_HS1_VBUS		–	AI	USB high-speed 1 data – bus voltage (5 V)
E7	USB_HS1_ID		–	AI	USB high-speed 1 data – ID (mini A or B plug)
E5	USB_HS1_SYSCLK		–	DI	USB high-speed 1 data – system clock
E3	USB_HS1_REXT		–	AI	USB high-speed 1 data – external resistor
High-speed USB 2.0 (USB_HS2)					
P6	USB_HS2_DP		–	AI, AO	USB high-speed 2 data – plus
N7	USB_HS2_DM		–	AI, AO	USB high-speed 2 data – minus
N1	USB_HS2_VBUS		–	AI	USB high-speed 2 data – bus voltage (5 V)
R7	USB_HS2_ID		–	AI	USB high-speed 2 data – ID (mini A or B plug)
M4	USB_HS2_SYSCLK		–	DI	USB high-speed 2 data – system clock
P2	USB_HS2_REXT		–	AI	USB high-speed 2 data – external resistor
HSIC interface					
C9	HSIC_DATA	GPIO_145	P4	DO B-PD:nppukp	HSIC data Configurable I/O
F10	HSIC_STROBE	GPIO_144	P4	DO B-PD:nppukp	HSIC strobe Configurable I/O
E9	HSIC_CAL		P4	B	Calibration pad for HSIC port
Secure digital controller interfaces – common to all four					
R45	VREF_SDC		–	AI	Reference for SDC I/O pads
Secure digital controller 1 (SDC1) interface – supports dual-voltage eMMC NAND					
AG47	SDC1_DATA_7		P7	B B-PD:nppukp	Secure digital controller 1 data bit 7
AJ47	SDC1_DATA_6		P7	B B-PD:nppukp	Secure digital controller 1 data bit 6
AR49	SDC1_DATA_5		P7	B B-PD:nppukp	Secure digital controller 1 data bit 5
AM46	SDC1_DATA_4		P7	B B-PD:nppukp	Secure digital controller 1 data bit 4
AK48	SDC1_DATA_3		P7	B B-PD:nppukp	Secure digital controller 1 data bit 3
AL49	SDC1_DATA_2		P7	B B-PD:nppukp	Secure digital controller 1 data bit 2
AM48	SDC1_DATA_1		P7	B B-PD:nppukp	Secure digital controller 1 data bit 1
AL47	SDC1_DATA_0		P7	B B-PD:nppukp	Secure digital controller 1 data bit 0

Table 2-4 Pin descriptions – connectivity functions (cont.)

Pad #	Pad name and/or function	Pad name or alt function	Pad characteristics [2]		Functional description
			Voltage	Type	
AK46	SDC1_CMD		P7	B B-PD:nppukp	Secure digital controller 1 command
AM50	SDC1_CLK		P7	B B-NP:pdpukp	Secure digital controller 1 clock
Secure digital controller 2 (SDC2) interface – supports dual-voltage SD 3.0					
R47	SDC2_DATA_3	QDSS_SDC2_TRDATA_3	P2	BH-PD:nppukp DO	Secure digital controller 2 data bit 3 ETM trace data bit 3 over SDC2
P46	SDC2_DATA_2	QDSS_SDC2_TRDATA_2	P2	BH-PD:nppukp DO	Secure digital controller 2 data bit 2 ETM trace data bit 2 over SDC2
V46	SDC2_DATA_1	QDSS_SDC2_TRDATA_1	P2	BH-PD:nppukp DO	Secure digital controller 2 data bit 1 ETM trace data bit 1 over SDC2
T50	SDC2_DATA_0	QDSS_SDC2_TRDATA_0	P2	BH-PD:nppukp DO	Secure digital controller 2 data bit 0 ETM trace data bit 0 over SDC2
U45	SDC2_CMD	QDSS_SDC2_TRSYNC	P2	BH-PD:nppukp DO	Secure digital controller 2 command ETM trace sync over SDC2
T48	SDC2_CLK	QDSS_SDC2_TRCLK	P2	BH-NP:pdpukp DO	Secure digital controller 2 clock ETM trace clock over SDC2
Secure digital controller 3 (SDC3) interface – supports SDIO					
D20	SDC3_DATA_3	GPIO_35	P3	B B-PD:nppukp	Secure digital controller 3 data bit 3 Configurable I/O
G19	SDC3_DATA_2	GPIO_36	P3	B B-PD:nppukp	Secure digital controller 3 data bit 2 Configurable I/O
A19	SDC3_DATA_1	GPIO_37	P3	B B-PD:nppukp	Secure digital controller 3 data bit 1 Configurable I/O
F18	SDC3_DATA_0	GPIO_38	P3	B B-PD:nppukp	Secure digital controller 3 data bit 0 Configurable I/O
F20	SDC3_CMD	GPIO_39	P3	B B-PD:nppukp	Secure digital controller 3 command Configurable I/O
E17	SDC3_CLK	GPIO_40	P3	DO B-PD:nppukp	Secure digital controller 3 clock Configurable I/O
Secure digital controller 4 (SDC4) interface – supports SDIO					
D26	SDC4_DATA_3	GPIO_92	P3	B B-PD:nppukp	Secure digital controller 4 data bit 3 Configurable I/O
A27	SDC4_DATA_2	GPIO_94	P3	B B-PD:nppukp	Secure digital controller 4 data bit 2 Configurable I/O
C25	SDC4_DATA_1	GPIO_95	P3	B B-PD:nppukp	Secure digital controller 4 data bit 1 Configurable I/O
D28	SDC4_DATA_0	GPIO_96	P3	B B-PD:nppukp	Secure digital controller 4 data bit 0 Configurable I/O
D24	SDC4_CMD	GPIO_91	P3	B B-PD:nppukp	Secure digital controller 4 command Configurable I/O
E27	SDC4_CLK	GPIO_93	P3	DO B-PD:nppukp	Secure digital controller 4 clock Configurable I/O

Table 2-4 Pin descriptions – connectivity functions (cont.)

Pad #	Pad name and/or function	Pad name or alt function	Pad characteristics [2]		Functional description
			Voltage	Type	
Transport stream interface 1 (TSIF1)					
D24	TSIF1_DATA	GPIO_91	P3	DI B-PD:nppukp	Transport stream interface 1 data Configurable I/O
F26	TSIF1_CLK	GPIO_89	P3	DI B-PD:nppukp	Transport stream interface 1 clock Configurable I/O
D26	TSIF1_SYNC	GPIO_92	P3	DI B-PD:nppukp	Transport stream interface 1 sync Configurable I/O
C27	TSIF1_EN	GPIO_90	P3	DI B-PD:nppukp	Transport stream interface 1 enable Configurable I/O
Transport stream interface 2 (TSIF2)					
C25	TSIF2_DATA	GPIO_95	P3	DI B-PD:nppukp	Transport stream interface 2 data Configurable I/O
E27	TSIF2_CLK	GPIO_93	P3	DI B-PD:nppukp	Transport stream interface 2 clock Configurable I/O
D28	TSIF2_SYNC	GPIO_96	P3	DI B-PD:nppukp	Transport stream interface 2 sync Configurable I/O
A27	TSIF2_EN	GPIO_94	P3	DI B-PD:nppukp	Transport stream interface 2 enable Configurable I/O
Audio SLIMbus – bidirectional multiplexed audio					
G49	SLIMBUS_MCLK	GPIO_69	P3	DO B-PD:nppukp	SLIMbus master clock Configurable I/O
J45	SLIMBUS_CLK	GPIO_70	P3	DO B-PD:nppukp	SLIMbus clock Configurable I/O
K46	SLIMBUS_DATA	GPIO_71	P3	DO B-PD:nppukp	SLIMbus data Configurable I/O
Audio I2S interface – speaker					
G49	SPKR_I2S_MCLK	GPIO_69	P3	DO B-PD:nppukp	Speaker I2S master clock Configurable I/O
J45	SPKR_I2S_SCK	GPIO_70	P3	DO B-PD:nppukp	Speaker I2S bit clock Configurable I/O
K46	SPKR_I2S_DOUT	GPIO_71	P3	DO B-PD:nppukp	Speaker I2S data output Configurable I/O
L45	SPKR_I2S_WS	GPIO_72	P3	DO B-PD:nppukp	Speaker I2S word select (L/R) Configurable I/O
Audio MI2S interface #1					
D48	MI2S_1_MCLK	GPIO_64	P3	B B-PD:nppukp	MI2S #1 master clock Configurable I/O
G47	MI2S_1_SCLK	GPIO_65	P3	B B-PD:nppukp	MI2S #1 bit clock Configurable I/O
F48	MI2S_1_WS	GPIO_66	P3	B B-PD:nppukp	MI2S #1 word select (L/R) Configurable I/O
H46	MI2S_1_D0	GPIO_67	P3	B B-PD:nppukp	MI2S #1 serial data channel 0 Configurable I/O
H48	MI2S_1_D1	GPIO_68	P3	B B-PD:nppukp	MI2S #1 serial data channel 1 Configurable I/O

Table 2-4 Pin descriptions – connectivity functions (cont.)

Pad #	Pad name and/or function	Pad name or alt function	Pad characteristics [2]		Functional description
			Voltage	Type	
Audio MI2S interface #2					
M50	MI2S_2_MCLK	GPIO_78	P3	B B-PD:nppukp	MI2S #2 master clock Configurable I/O
N45	MI2S_2_SCLK	GPIO_79	P3	B B-PD:nppukp	MI2S #2 bit clock Configurable I/O
R49	MI2S_2_WS	GPIO_80	P3	B B-PD:nppukp	MI2S #2 word select (L/R) Configurable I/O
A31	MI2S_2_D0	GPIO_81	P3	B B-PD:nppukp	MI2S #2 serial data channel 0 Configurable I/O
D32	MI2S_2_D1	GPIO_82	P3	B B-PD:nppukp	MI2S #2 serial data channel 1 Configurable I/O
Audio MI2S interface #3					
K48	MI2S_3_MCLK	GPIO_73	P3	B B-PD:nppukp	MI2S #3 master clock Configurable I/O
L47	MI2S_3_SCLK	GPIO_74	P3	B B-PD:nppukp	MI2S #3 bit clock Configurable I/O
L49	MI2S_3_WS	GPIO_75	P3	B B-PD:nppukp	MI2S #3 word select (L/R) Configurable I/O
M48	MI2S_3_D0	GPIO_76	P3	B B-PD:nppukp	MI2S #3 serial data channel 0 Configurable I/O
M46	MI2S_3_D1	GPIO_77	P3	B B-PD:nppukp	MI2S #3 serial data channel 1 Configurable I/O
Audio MI2S interface #4					
C33	MI2S_4_MCLK	GPIO_57	P3	DO B-PD:nppukp	MI2S #4 master clock Configurable I/O
C35	MI2S_4_SCLK	GPIO_58	P3	B B-PD:nppukp	MI2S #4 bit clock Configurable I/O
D34	MI2S_4_WS	GPIO_59	P3	B B-PD:nppukp	MI2S #4 word select (L/R) Configurable I/O
E35	MI2S_4_D0	GPIO_60	P3	B B-PD:nppukp	MI2S #4 serial data channel 0 Configurable I/O
D36	MI2S_4_D1	GPIO_61	P3	B B-PD:nppukp	MI2S #4 serial data channel 1 Configurable I/O
D38	MI2S_4_D2	GPIO_62	P3	B B-PD:nppukp	MI2S #4 serial data channel 2 Configurable I/O
D40	MI2S_4_D3	GPIO_63	P3	B B-PD:nppukp	MI2S #4 serial data channel 3 Configurable I/O
Primary audio PCM interface (only one of the two ports can be configured as PCM)					
G47	AUDIO_PCM_CLK	GPIO_65	P3	B B-PD:nppukp	Audio PCM clock (port 1) Configurable I/O
F48	AUDIO_PCM_SYNC	GPIO_66	P3	B B-PD:nppukp	Audio PCM sync (port 1) Configurable I/O
H46	AUDIO_PCM_DIN	GPIO_67	P3	B B-PD:nppukp	Audio PCM data input (port 1) Configurable I/O
H48	AUDIO_PCM_DOUT	GPIO_68	P3	B B-PD:nppukp	Audio PCM data output (port 1) Configurable I/O

Table 2-4 Pin descriptions – connectivity functions (cont.)

Pad #	Pad name and/or function	Pad name or alt function	Pad characteristics [2]		Functional description
			Voltage	Type	
L47	AUDIO_PCM_CLK	GPIO_74	P3	B B-PD:nppukp	Audio PCM clock (port 2) Configurable I/O
L49	AUDIO_PCM_SYNC	GPIO_75	P3	B B-PD:nppukp	Audio PCM sync (port 2) Configurable I/O
M48	AUDIO_PCM_DIN	GPIO_76	P3	B B-PD:nppukp	Audio PCM data input (port 2) Configurable I/O
M46	AUDIO_PCM_DOUT	GPIO_77	P3	B B-PD:nppukp	Audio PCM data output (port 2) Configurable I/O
Secondary audio PCM interface (only one of the two ports can be configured as PCM)					
N45	AUDIO_PCM_CLK	GPIO_79	P3	B B-PD:nppukp	Audio PCM clock (port 1) Configurable I/O
R49	AUDIO_PCM_SYNC	GPIO_80	P3	B B-PD:nppukp	Audio PCM sync (port 1) Configurable I/O
A31	AUDIO_PCM_DIN	GPIO_81	P3	B B-PD:nppukp	Audio PCM data input (port 1) Configurable I/O
D32	AUDIO_PCM_DOUT	GPIO_82	P3	B B-PD:nppukp	Audio PCM data output (port 1) Configurable I/O
C35	AUDIO_PCM_CLK	GPIO_58	P3	B B-PD:nppukp	Audio PCM clock (port 2) Configurable I/O
D34	AUDIO_PCM_SYNC	GPIO_59	P3	B B-PD:nppukp	Audio PCM sync (port 2) Configurable I/O
E35	AUDIO_PCM_DIN	GPIO_60	P3	B B-PD:nppukp	Audio PCM data input (port 2) Configurable I/O
D36	AUDIO_PCM_DOUT	GPIO_61	P3	B B-PD:nppukp	Audio PCM data output (port 2) Configurable I/O
User interface module (UIM) interfaces – common reference voltage					
AB48	VREF_UIM		–	AI	Reference for UIM I/O pads
BAM-based low-speed peripheral interface 1 – see Table 2-5 for application-specific pin assignments					
BH12	BLSP1_3	GPIO_0	P3	B B-PD:nppukp	BLSP 1 bit 3; Configurable I/O
BF14	BLSP1_2	GPIO_1	P3	B B-PD:nppukp	BLSP 1 bit 2; Configurable I/O
BF12	BLSP1_1	GPIO_2	P3	B B-PD:nppukp	BLSP 1 bit 1; Configurable I/O
BG13	BLSP1_0	GPIO_3	P3	B B-PD:nppukp	BLSP 1 bit 0; Configurable I/O
BAM-based low-speed peripheral interface 2 – see Table 2-5 for application-specific pin assignments					
C29	BLSP2_3	GPIO_4	P3	B B-PD:nppukp	BLSP 2 bit 3; Configurable I/O
D30	BLSP2_2	GPIO_5	P3	B B-PD:nppukp	BLSP 2 bit 2; Configurable I/O
C31	BLSP2_1	GPIO_6	P3	B B-PD:nppukp	BLSP 2 bit 1; Configurable I/O
E31	BLSP2_0	GPIO_7	P3	B B-PD:nppukp	BLSP 2 bit 0; Configurable I/O

Table 2-4 Pin descriptions – connectivity functions (cont.)

Pad #	Pad name and/or function	Pad name or alt function	Pad characteristics [2]		Functional description
			Voltage	Type	
BAM-based low-speed peripheral interface 3 – see Table 2-5 for application-specific pin assignments					
BG11	BLSP3_3	GPIO_8	P3	B B-PD:nppukp	BLSP 3 bit 3; Configurable I/O
BE13	BLSP3_2	GPIO_9	P3	B B-PD:nppukp	BLSP 3 bit 2; Configurable I/O
BH10	BLSP3_1	GPIO_10	P3	B B-PD:nppukp	BLSP 3 bit 1; Configurable I/O
BE11	BLSP3_0	GPIO_11	P3	B B-PD:nppukp	BLSP 3 bit 0; Configurable I/O
BAM-based low-speed peripheral interface 4 – see Table 2-5 for application-specific pin assignments					
F12	BLSP4_3	GPIO_19	P3	B B-PD:nppukp	BLSP 4 bit 3; Configurable I/O
E11	BLSP4_2	GPIO_20	P3	B B-PD:nppukp	BLSP 4 bit 2; Configurable I/O
G15	BLSP4_1	GPIO_21	P3	B B-PD:nppukp	BLSP 4 bit 1; Configurable I/O
D10	BLSP4_0	GPIO_22	P3	B B-PD:nppukp	BLSP 4 bit 0; Configurable I/O
BAM-based low-speed peripheral interface 5 – see Table 2-5 for application-specific pin assignments					
E13	BLSP5_3	GPIO_23	P3	B B-PD:nppukp	BLSP 5 bit 3; Configurable I/O
B10	BLSP5_2	GPIO_24	P3	B B-PD:nppukp	BLSP 5 bit 2; Configurable I/O
D12	BLSP5_1	GPIO_25	P3	B B-PD:nppukp	BLSP 5 bit 1; Configurable I/O
D14	BLSP5_0	GPIO_26	P3	B B-PD:nppukp	BLSP 5 bit 0; Configurable I/O
BAM-based low-speed peripheral interface 6 – see Table 2-5 for application-specific pin assignments					
A11	BLSP6_3	GPIO_27	P3	B B-PD:nppukp	BLSP 6 bit 3; Configurable I/O
E15	BLSP6_2	GPIO_28	P3	B B-PD:nppukp	BLSP 6 bit 2; Configurable I/O
F16	BLSP6_1	GPIO_29	P3	B B-PD:nppukp	BLSP 6 bit 1; Configurable I/O
G17	BLSP6_0	GPIO_30	P3	B B-PD:nppukp	BLSP 6 bit 0; Configurable I/O
BAM-based low-speed peripheral interface 7 – see Table 2-5 for application-specific pin assignments					
D18	BLSP7_3	GPIO_41	P3	B B-PD:nppukp	BLSP 7 bit 3; Configurable I/O
C19	BLSP7_2	GPIO_42	P3	B B-PD:nppukp	BLSP 7 bit 2; Configurable I/O
B18	BLSP7_1	GPIO_43	P3	B B-PD:nppukp	BLSP 7 bit 1; Configurable I/O
C21	BLSP7_0	GPIO_44	P3	B B-PD:nppukp	BLSP 7 bit 0; Configurable I/O

Table 2-4 Pin descriptions – connectivity functions (cont.)

Pad #	Pad name and/or function	Pad name or alt function	Pad characteristics [2]		Functional description
			Voltage	Type	
BAM-based low-speed peripheral interface 8 – see Table 2-5 for application-specific pin assignments					
D16	BLSP8_3	GPIO_45	P3	B B-PD:nppukp	BLSP 8 bit 3; Configurable I/O
B14	BLSP8_2	GPIO_46	P3	B B-PD:nppukp	BLSP 8 bit 2; Configurable I/O
A15	BLSP8_1	GPIO_47	P3	B B-PD:nppukp	BLSP 8 bit 1; Configurable I/O
C17	BLSP8_0	GPIO_48	P3	B B-PD:nppukp	BLSP 8 bit 0; Configurable I/O
BAM-based low-speed peripheral interface 9 – see Table 2-5 for application-specific pin assignments					
AA49	BLSP9_3	GPIO_49	P6	B BH-PD:nppukp	BLSP 9 bit 3; Configurable I/O
AC49	BLSP9_2	GPIO_50	P6	B BH-PD:nppukp	BLSP 9 bit 2; Configurable I/O
AE47	BLSP9_1	GPIO_51	P6	B BH-PD:nppukp	BLSP 9 bit 1; Configurable I/O
AH50	BLSP9_0	GPIO_52	P3	B B-PD:nppukp	BLSP 9 bit 0; Configurable I/O
BAM-based low-speed peripheral interface 10 – see Table 2-5 for application-specific pin assignments					
B22	BLSP10_3	GPIO_53	P3	B B-PD:nppukp	BLSP 10 bit 3; Configurable I/O
D22	BLSP10_2	GPIO_54	P3	B B-PD:nppukp	BLSP 10 bit 2; Configurable I/O
C23	BLSP10_1	GPIO_55	P3	B B-PD:nppukp	BLSP 10 bit 1; Configurable I/O
A23	BLSP10_0	GPIO_56	P3	B B-PD:nppukp	BLSP 10 bit 0; Configurable I/O
BAM-based low-speed peripheral interface 11 – see Table 2-5 for application-specific pin assignments					
A31	BLSP11_3	GPIO_81	P3	B B-PD:nppukp	BLSP 11 bit 3; Configurable I/O
D32	BLSP11_2	GPIO_82	P3	B B-PD:nppukp	BLSP 11 bit 2; Configurable I/O
F32	BLSP11_1	GPIO_83	P3	B B-PD:nppukp	BLSP 11 bit 1; Configurable I/O
E33	BLSP11_0	GPIO_84	P3	B B-PD:nppukp	BLSP 11 bit 0; Configurable I/O
BAM-based low-speed peripheral interface 12 – see Table 2-5 for application-specific pin assignments					
C41	BLSP12_3	GPIO_85	P3	B B-PD:nppukp	BLSP 12 bit 3; Configurable I/O
D42	BLSP12_2	GPIO_86	P3	B B-PD:nppukp	BLSP 12 bit 2; Configurable I/O
E47	BLSP12_1	GPIO_87	P3	B B-PD:nppukp	BLSP 12 bit 1; Configurable I/O
H44	BLSP12_0	GPIO_88	P3	B B-PD:nppukp	BLSP 12 bit 0; Configurable I/O

Table 2-4 Pin descriptions – connectivity functions (cont.)

Pad #	Pad name and/or function	Pad name or alt function	Pad characteristics [2]		Functional description
			Voltage	Type	
Serial peripheral interface (SPI) extra chip selects (supplements BLSP ports configured for SPI protocol) signals [1]					
BG11	SPI_CS1_N_BLSP1	GPIO_8	P3	DO-Z B-PD:nppukp	Chip select 1 for SPI on BLSP #1 Configurable I/O
BE13	SPI_CS2A_N_BLSP1	GPIO_9	P3	DO-Z B-PD:nppukp	Chip select 2A for SPI on BLSP #1 Configurable I/O
BH10	SPI_CS3_N_BLSP1	GPIO_10	P3	DO-Z B-PD:nppukp	Chip select 3 for SPI on BLSP #1 Configurable I/O
BE11	SPI_CS2B_N_BLSP1	GPIO_11	P3	DO-Z B-PD:nppukp	Chip select 2B for SPI on BLSP #1 Configurable I/O
B22	SPI_CS1A_N_BLSP2	GPIO_53	P3	DO-Z B-PD:nppukp	Chip select 1A for SPI on BLSP #2 Configurable I/O
D38	SPI_CS1B_N_BLSP2	GPIO_62	P3	DO-Z B-PD:nppukp	Chip select 1B for SPI on BLSP #2 Configurable I/O
D22	SPI_CS2A_N_BLSP2	GPIO_54	P3	DO-Z B-PD:nppukp	Chip select 2A for SPI on BLSP #2 Configurable I/O
D40	SPI_CS2B_N_BLSP2	GPIO_63	P3	DO-Z B-PD:nppukp	Chip select 2B for SPI on BLSP #2 Configurable I/O
F48	SPI_CS3_N_BLSP2	GPIO_66	P3	DO-Z B-PD:nppukp	Chip select 3 for SPI on BLSP #2 Configurable I/O
A15	SPI_CS1A_N_BLSP10	GPIO_47	P3	DO-Z B-PD:nppukp	Chip select 1A for SPI on BLSP #10 Configurable I/O
H46	SPI_CS1B_N_BLSP10	GPIO_67	P3	DO-Z B-PD:nppukp	Chip select 1B for SPI on BLSP #10 Configurable I/O
C17	SPI_CS2A_N_BLSP10	GPIO_48	P3	DO-Z B-PD:nppukp	Chip select 2A for SPI on BLSP #10 Configurable I/O
H48	SPI_CS2B_N_BLSP10	GPIO_68	P3	DO-Z B-PD:nppukp	Chip select 2B for SPI on BLSP #10 Configurable I/O
C27	SPI_CS3_N_BLSP10	GPIO_90	P3	DO-Z B-PD:nppukp	Chip select 3 for SPI on BLSP #10 Configurable I/O

1. GPIO 'A/B' multiplexing is explained in Figure 2-4.
2. Refer to Table 2-1 for parameter and acronym definitions.

NOTE GPIO pins can support multiple functions. To assign GPIOs to particular functions (such as the options listed in the table above), designers must identify all their application's requirements and map each GPIO to its function – carefully avoiding conflicts in GPIO assignments. Refer to Table 2-11 for a list of all supported functions for each GPIO.

NOTE Twelve 4-pin sets of GPIOs are available as BAM-based low-speed peripheral (BLSP) interface ports that can be configured for UART, UIM, SPI, or I2C operation. Detailed pin assignments are presented in Table 2-5 for each configuration.

Table 2-5 Example BLSP configurations

Option	Configuration	BLSP bit 3	BLSP bit 2	BLSP bit 1	BLSP bit 0
	BLSP1 GPIO pins =	GPIO_0	GPIO_1	GPIO_2	GPIO_3
	BLSP2 GPIO pins =	GPIO_4	GPIO_5	GPIO_6	GPIO_7
	BLSP3 GPIO pins =	GPIO_8	GPIO_9	GPIO_10	GPIO_11
	BLSP4 GPIO pins =	GPIO_19	GPIO_20	GPIO_21	GPIO_22
	BLSP5 GPIO pins =	GPIO_23	GPIO_24	GPIO_25	GPIO_26
	BLSP6 GPIO pins =	GPIO_27	GPIO_28	GPIO_29	GPIO_30
	BLSP7 GPIO pins =	GPIO_41	GPIO_42	GPIO_43	GPIO_44
	BLSP8 GPIO pins =	GPIO_45	GPIO_46	GPIO_47	GPIO_48
	BLSP9 GPIO pins =	GPIO_49	GPIO_50	GPIO_51	GPIO_52
	BLSP10 GPIO pins =	GPIO_53	GPIO_54	GPIO_55	GPIO_56
	BLSP11 GPIO pins =	GPIO_81	GPIO_82	GPIO_83	GPIO_84
	BLSP12 GPIO pins =	GPIO_85	GPIO_86	GPIO_87	GPIO_88
1	4-pin UART	UART_TX DO 4-pin UART transmit data	UART_RX DI 4-pin UART receive data	UART_CTS_N DI 4-pin UART clear-to-send	UART_RFR_N DO 4-pin UART ready-for-receive
2	2-pin UART + 2-pin I2C	UART_TX DO 2-pin UART transmit data	UART_RX DI 2-pin UART receive data	I2C_SDA B I2C serial data	I2C_SCL B I2C serial clock
3	2-pin UART + 2-GPIOs	UART_TX DO 2-pin UART transmit data	UART_RX DI 2-pin UART receive data	GPIO_XX B Configurable I/O	GPIO_XX B Configurable I/O
4	4-pin SPI	SPI_DATA_MOSI B 4-pin SPI master out/slave in	SPI_DATA_MISO B 4-pin SPI master in/slave out	SPI_CS_N B 4-pin SPI chip select	SPI_CLK B 4-pin SPI clock
5	2-pin UIM + 2-pin I2C	UIM_DATA B UIM data	UIM_CLK DO UIM clock	I2C_SDA B I2C serial data	I2C_SCL B I2C serial clock
6	2-pin UIM + 2 GPIO	UIM_DATA B UIM data	UIM_CLK DO UIM clock	GPIO_XX B Configurable I/O	GPIO_XX B Configurable I/O
7	2-pin I2C + 2 GPIOs	GPIO_XX B Configurable I/O	GPIO_XX B Configurable I/O	I2C_SDA B I2C serial data	I2C_SCL B I2C serial clock
8	4 GPIOs	GPIO_XX B Configurable I/O	GPIO_XX B Configurable I/O	GPIO_XX B Configurable I/O	GPIO_XX B Configurable I/O
		Note: The three rows within shaded cells are: 1) pad function; 2) pad type; and 3) functional description.			

As noted throughout these pin definition tables, GPIO assignments must be done carefully to avoid conflicts, and to ensure that the desired functionality is achieved. For GPIOs that can be used as BLSPs, three additional factors should be considered when making functional assignments:

1. Extra chip selects are available when certain BLSPs are used for SPI:
   - BLSP1 has extra CS1, CS2A, CS2B, and CS3 for its SPI.
   - BLSP2 has extra CS1A, CS1B, CS2A, CS2B, and CS3 for its SPI.
   - BLSP10 has extra CS1A, CS1B, CS2A, CS2B, and CS3 for its SPI.
2. The dual-voltage UIM2 port is multiplexed with a set of BLSP pins:
   - The UIM2 port is powered by pad group 6 (VDD_P6) to allow 1.8 V or 2.85 V operation; its four pins are multiplexed with BLSP 9 (and other functions).
3. BLSPs that are configured for SPI or I2C or UART functionality require data mover access to achieve their higher throughput rates. In any BLSP, the SPI and I2C share the same FIFO/ADM CRCI interface and the UART/UIM share the same FIFO and ADM CRCI interface.
4. I2C can use only BLSP bits [0] and [1]. UIM can use only BLSP bits [2] and [3]. UART_RX and UART_TX are also only available on bits [2] and [3], as shown in Table 2-5. These rules apply across all 12 BLSPs.

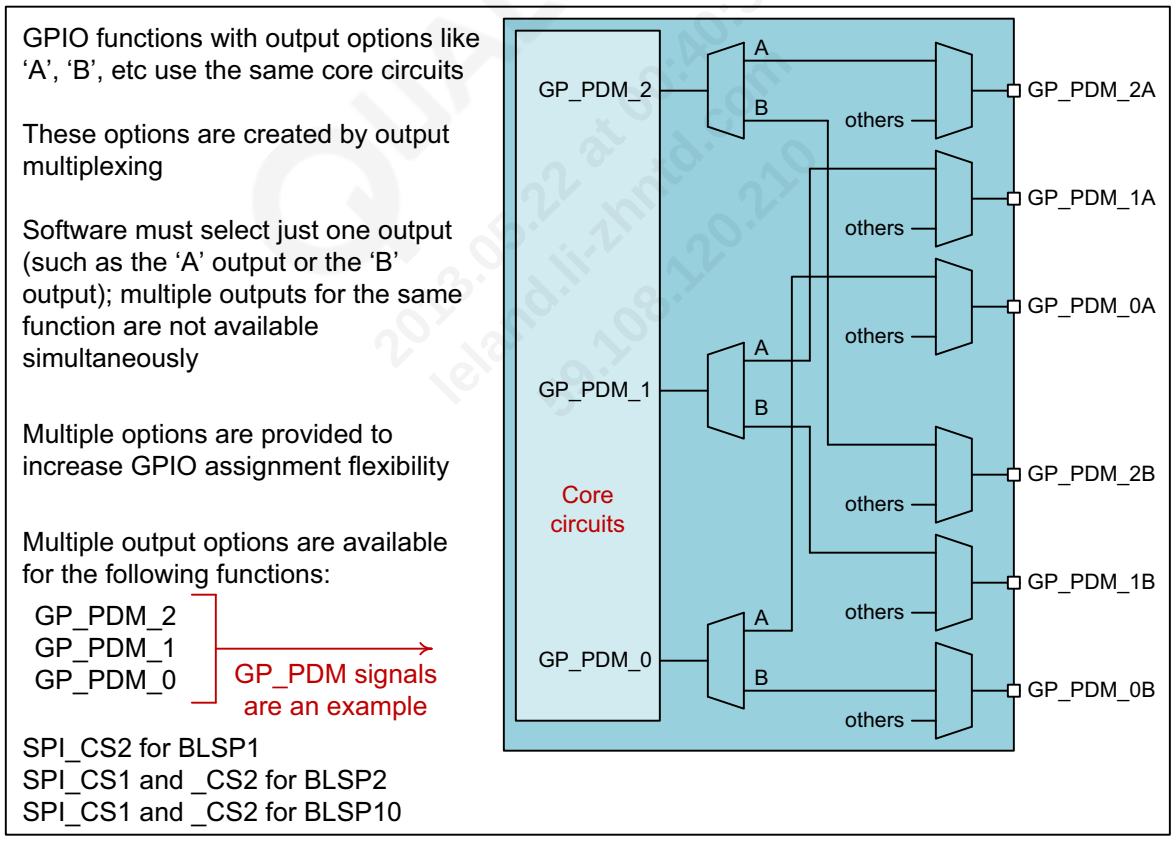


Figure 2-4 GPIO 'A/B' multiplexing

Table 2-6 Pin descriptions – internal functions

Pad #	Pad name and/or function	Pad name or alt function	Pad characteristics [2]		Functional description
			Voltage	Type	
Clocks and related signals [1]					
Also see Table 2-9 for clock and related functions that interface with the PMIC (SLEEP_CLK, CXO, CXO_EN)					
F16	GP_MN	GPIO_29	P3	DO B-PD:nppukp	General-purpose M/N:D counter output Configurable I/O
H48	GP_PDM_0A	GPIO_68	P3	DO B-PD:nppukp	General-purpose PDM 0A output Configurable I/O
D22	GP_PDM_0B	GPIO_54	P3	DO B-PD:nppukp	General-purpose PDM 0B output Configurable I/O
D42	GP_PDM_1A	GPIO_86	P3	DO B-PD:nppukp	General-purpose PDM 1A output Configurable I/O
L47	GP_PDM_1B	GPIO_74	P3	DO B-PD:nppukp	General-purpose PDM 1B output Configurable I/O
N45	GP_PDM_2A	GPIO_79	P3	DO B-PD:nppukp	General-purpose PDM 2A output Configurable I/O
D40	GP_PDM_2B	GPIO_63	P3	DO B-PD:nppukp	General-purpose PDM 2B output Configurable I/O
Resets and mode controls – see the list of MSM8x74 pins (Table 2-7) that can wake up the device (thereby supporting MPM)					
Also see Table 2-9 for reset and mode-control functions that interface with the PMIC (RESIN_N, PS_HOLD)					
G35	MODE_1		P3	DISH-PD	Mode control bit 1 – unconnected for native mode
F34	MODE_0		P3	DISH-PD	Mode control bit 0 – unconnected for native mode
AA45	RESOUT_N		P3	DO	Reset output
AR47	FORCED_USB_BOOT	GPIO_103	P3	DI B-PD:nppukp	USB boot is forced Configurable I/O
BF20	BOOT_CONFIG_0	GPIO_112	P3	DI B-PD:nppukp	Boot configuration control bit 0 for WDOG_DISABLE Configurable I/O
BG19	BOOT_CONFIG_1	GPIO_113	P3	DI B-PD:nppukp	Boot configuration control bit 1 for FAST_BOOT_SEL[0] Configurable I/O
AW47	BOOT_CONFIG_2	GPIO_114	P3	DI B-PD:nppukp	Boot configuration control bit 2 for FAST_BOOT_SEL[1] Configurable I/O
AV48	BOOT_CONFIG_3	GPIO_115	P3	DI B-PD:nppukp	Boot configuration control bit 3 for FAST_BOOT_SEL[2] Configurable I/O
AY46	BOOT_CONFIG_4	GPIO_116	P3	DI B-PD:nppukp	Boot configuration control bit 4 for FAST_BOOT_SEL[3] Configurable I/O
JTAG interface					
AM44	SRST_N		P3	DI	JTAG reset for debug
AG45	TCK		P3	DI	JTAG clock input
AL45	TDI		P3	DI	JTAG data input
AP46	TDO		P3	DO-Z	JTAG data output
AK44	TMS		P3	DI	JTAG mode select input
AJ45	TRST_N		P3	DI	JTAG reset

Table 2-6 Pin descriptions – internal functions (cont.)

Pad #	Pad name and/or function	Pad name or alt function	Pad characteristics [2]		Functional description
			Voltage	Type	
ETM interfaces for Krait, RPM, and QDSP6					
C7	QDSS_ETM_TRDATA_15B	GPIO_15	P3	DO B-PD:nppukp	ETM trace data bit 15B Configurable I/O
A7	QDSS_ETM_TRDATA_14B	GPIO_16	P3	DO B-PD:nppukp	ETM trace data bit 14B Configurable I/O
B8	QDSS_ETM_TRDATA_13B	GPIO_17	P3	DO B-PD:nppukp	ETM trace data bit 13B Configurable I/O
C11	QDSS_ETM_TRDATA_12B	GPIO_18	P3	DO B-PD:nppukp	ETM trace data bit 12B Configurable I/O
F12	QDSS_ETM_TRDATA_11B	GPIO_19	P3	DO B-PD:nppukp	ETM trace data bit 11B Configurable I/O
E11	QDSS_ETM_TRDATA_10B	GPIO_20	P3	DO B-PD:nppukp	ETM trace data bit 10B Configurable I/O
G15	QDSS_ETM_TRDATA_9B	GPIO_21	P3	DO B-PD:nppukp	ETM trace data bit 9B Configurable I/O
D10	QDSS_ETM_TRDATA_8B	GPIO_22	P3	DO B-PD:nppukp	ETM trace data bit 8B Configurable I/O
E13	QDSS_ETM_TRDATA_7B	GPIO_23	P3	DO B-PD:nppukp	ETM trace data bit 7B Configurable I/O
B10	QDSS_ETM_TRDATA_6B	GPIO_24	P3	DO B-PD:nppukp	ETM trace data bit 6B Configurable I/O
D12	QDSS_ETM_TRDATA_5B	GPIO_25	P3	DO B-PD:nppukp	ETM trace data bit 5B Configurable I/O
D14	QDSS_ETM_TRDATA_4B	GPIO_26	P3	DO B-PD:nppukp	ETM trace data bit 4B Configurable I/O
A11	QDSS_ETM_TRDATA_3B	GPIO_27	P3	DO B-PD:nppukp	ETM trace data bit 3B Configurable I/O
E15	QDSS_ETM_TRDATA_2B	GPIO_28	P3	DO B-PD:nppukp	ETM trace data bit 2B Configurable I/O
C27	QDSS_ETM_TRDATA_1B	GPIO_90	P3	DO B-PD:nppukp	ETM trace data bit 1B Configurable I/O
D24	QDSS_ETM_TRDATA_0B	GPIO_91	P3	DO B-PD:nppukp	ETM trace data bit 0B Configurable I/O
F26	QDSS_ETM_TRCLK_B	GPIO_89	P3	DO B-PD:nppukp	ETM trace clock B Configurable I/O
D26	QDSS_ETM_TRSYNC_B	GPIO_92	P3	DO B-PD:nppukp	ETM trace sync B Configurable I/O
D18	QDSS_ETM_TRDATA_15A	GPIO_41	P3	DO B-PD:nppukp	ETM trace data bit 15A Configurable I/O
C19	QDSS_ETM_TRDATA_14A	GPIO_42	P3	DO B-PD:nppukp	ETM trace data bit 14A Configurable I/O
B18	QDSS_ETM_TRDATA_13A	GPIO_43	P3	DO B-PD:nppukp	ETM trace data bit 13A Configurable I/O
C21	QDSS_ETM_TRDATA_12A	GPIO_44	P3	DO B-PD:nppukp	ETM trace data bit 12A Configurable I/O
D16	QDSS_ETM_TRDATA_11A	GPIO_45	P3	DO B-PD:nppukp	ETM trace data bit 11A Configurable I/O

Table 2-6 Pin descriptions – internal functions (cont.)

Pad #	Pad name and/or function	Pad name or alt function	Pad characteristics [2]		Functional description
			Voltage	Type	
B14	QDSS_ETM_TRDATA_10A	GPIO_46	P3	DO B-PD:nppukp	ETM trace data bit 10A Configurable I/O
A15	QDSS_ETM_TRDATA_9A	GPIO_47	P3	DO B-PD:nppukp	ETM trace data bit 9A Configurable I/O
C17	QDSS_ETM_TRDATA_8A	GPIO_48	P3	DO B-PD:nppukp	ETM trace data bit 8A Configurable I/O
AN3	QDSS_ETM_TRDATA_7A	GPIO_31	P3	DO B-PD:nppukp	ETM trace data bit 7A Configurable I/O
AM4	QDSS_ETM_TRDATA_6A	GPIO_32	P3	DO B-PD:nppukp	ETM trace data bit 6A Configurable I/O
AM2	QDSS_ETM_TRDATA_5A	GPIO_33	P3	DO B-PD:nppukp	ETM trace data bit 5A Configurable I/O
AP4	QDSS_ETM_TRDATA_4A	GPIO_34	P3	DO B-PD:nppukp	ETM trace data bit 4A Configurable I/O
D20	QDSS_ETM_TRDATA_3A	GPIO_35	P3	DO B-PD:nppukp	ETM trace data bit 3A Configurable I/O
G19	QDSS_ETM_TRDATA_2A	GPIO_36	P3	DO B-PD:nppukp	ETM trace data bit 2A Configurable I/O
A19	QDSS_ETM_TRDATA_1A	GPIO_37	P3	DO B-PD:nppukp	ETM trace data bit 1A Configurable I/O
F18	QDSS_ETM_TRDATA_0A	GPIO_38	P3	DO B-PD:nppukp	ETM trace data bit 0A Configurable I/O
E17	QDSS_ETM_TRCLK_A	GPIO_40	P3	DO B-PD:nppukp	ETM trace clock A Configurable I/O
F20	QDSS_ETM_TRSYNC_A	GPIO_39	P3	DO B-PD:nppukp	ETM trace sync A Configurable I/O
R47	QDSS_SDC2_TRDATA_3	SDC2_DATA_3	P2	DO BH-PD:nppukp	ETM trace data bit 3 over SDC2 Configurable I/O
P46	QDSS_SDC2_TRDATA_2	SDC2_DATA_2	P2	DO BH-PD:nppukp	ETM trace data bit 2 over SDC2 Configurable I/O
V46	QDSS_SDC2_TRDATA_1	SDC2_DATA_1	P2	DO BH-PD:nppukp	ETM trace data bit 1over SDC2 Configurable I/O
T50	QDSS_SDC2_TRDATA_0	SDC2_DATA_0	P2	DO BH-PD:nppukp	ETM trace data bit 0 over SDC2 Configurable I/O
T48	QDSS_SDC2_TRCLK	SDC2_CLK	P2	DO DO	ETM trace clock over SDC2 Configurable I/O
U45	QDSS_SDC2_TRSYNC	SDC2_CMD	P2	DO BH-PD:nppukp	ETM trace sync over SDC2 Configurable I/O

1. GPIO 'A/B' multiplexing is explained in Figure 2-4.
2. Refer to Table 2-1 for parameter and acronym definitions.

NOTE GPIO pins can support multiple functions. To assign GPIOs to particular functions (such as the options listed in the table above), designers must identify all their application's requirements and map each GPIO to its function – carefully avoiding conflicts in GPIO assignments. Refer to Table 2-11 for a list of all supported functions for each GPIO.

Table 2-7 MSM8x74 GPIO wakeup pins for modem power management (MPM)

Pad #	Pad name	Pad characteristics [1]		Wakeup functional description
		Voltage	Type	
BF14	GPIO_1	P3	B-PD:nppukp	UART Rx
D30	GPIO_5	P3	B-PD:nppukp	UART Rx
BE13	GPIO_9	P3	B-PD:nppukp	UART Rx
C11	GPIO_18	P3	B-PD:nppukp	General-purpose
E11	GPIO_20	P3	B-PD:nppukp	UART Rx
B10	GPIO_24	P3	B-PD:nppukp	UART Rx
A11	GPIO_27	P3	B-PD:nppukp	General-purpose
E15	GPIO_28	P3	B-PD:nppukp	UART Rx
AP4	GPIO_34	P3	B-PD:nppukp	HDMI hot plug detect
D20	GPIO_35	P3	B-PD:nppukp	General-purpose
A19	GPIO_37	P3	B-PD:nppukp	SDIO
C19	GPIO_42	P3	B-PD:nppukp	UART Rx
C21	GPIO_44	P3	B-PD:nppukp	General-purpose
B14	GPIO_46	P3	B-PD:nppukp	UART Rx
AC49	GPIO_50	P6	BH-PD:nppukp	UART Rx
D22	GPIO_54	P3	B-PD:nppukp	UART Rx
D34	GPIO_59	P3	B-PD:nppukp	General-purpose
D36	GPIO_61	P3	B-PD:nppukp	Sensors – proximity interrupt
D38	GPIO_62	P3	B-PD:nppukp	SD card detect
D48	GPIO_64	P3	B-PD:nppukp	General-purpose
G47	GPIO_65	P3	B-PD:nppukp	Sensors – accelerometer interrupt 2
F48	GPIO_66	P3	B-PD:nppukp	Sensors – gyro interrupt
H46	GPIO_67	P3	B-PD:nppukp	Sensors – magnetometer interrupt
H48	GPIO_68	P3	B-PD:nppukp	General-purpose
K46	GPIO_71	P3	B-PD:nppukp	SLIMbus data
L45	GPIO_72	P3	B-PD:nppukp	WCD9320 IRQ
K48	GPIO_73	P3	B-PD:nppukp	Sensors – accelerometer interrupt 1
L47	GPIO_74	P3	B-PD:nppukp	Sensors – fingerprint interrupt
L49	GPIO_75	P3	B-PD:nppukp	Sensors – pressure interrupt
M46	GPIO_77	P3	B-PD:nppukp	General-purpose
N45	GPIO_79	P3	B-PD:nppukp	Sensors – ALS interrupt
R49	GPIO_80	P3	B-PD:nppukp	General-purpose
D32	GPIO_82	P3	B-PD:nppukp	UART Rx
D42	GPIO_86	P3	B-PD:nppukp	UART Rx
D26	GPIO_92	P3	B-PD:nppukp	SD card detect
E27	GPIO_93	P3	B-PD:nppukp	Microphone activity detection
C25	GPIO_95	P3	B-PD:nppukp	SDIO
AF2	GPIO_102	P3	B-PD:nppukp	eDP hot plug detect
F10	GPIO_144	P4	B-PD:nppukp	HSIC IRQ

Table 2-7 MSM8x74 GPIO wakeup pins for modem power management (MPM) (cont.)

Pad #	Pad name	Pad characteristics [1]		Wakeup functional description
		Voltage	Type	
AM48	SDC1_DATA_1	P7	B-PD:nppukp	SDIO
AK48	SDC1_DATA_3	P7	B-PD:nppukp	SD card detect
V46	SDC2_DATA_1	P2	BH-PD:nppukp	SDIO
R47	SDC2_DATA_3	P2	BH-PD:nppukp	SD card detect
AM44	SRST_N	P3	DI	JTAG

1. Refer to Table 2-1 for parameter and acronym definitions.

Table 2-8 MODE[1:0] settings

MODE[1:0]	Usage
00	Native mode
11	Boundary-scan mode
Others	Test modes

Table 2-9 Pin descriptions – chipset interface functions

Pad #	Pad name and/or function	Pad name or alt function	Pad characteristics [1]		Functional description
			Voltage	Type	
WTR1605/WTR1605L – Rx baseband interfaces					
BK26	BBRX_IP_CH0		–	AI	Baseband receiver input, in-phase plus, channel 0
BH26	BBRX_IM_CH0		–	AI	Baseband receiver input, in-phase minus, channel 0
BJ27	BBRX_QP_CH0		–	AI	Baseband receiver input, quadrature plus, channel 0
BG27	BBRX_QM_CH0		–	AI	Baseband receiver input, quadrature minus, channel 0
BH28	BBRX_IP_CH1		–	AI	Baseband receiver input, in-phase plus, channel 1
BG29	BBRX_IM_CH1		–	AI	Baseband receiver input, in-phase minus, channel 1
BK30	BBRX_QP_CH1		–	AI	Baseband receiver input, quadrature plus, channel 1
BH30	BBRX_QM_CH1		–	AI	Baseband receiver input, quadrature minus, channel 1
BH38	BBRX_IP_CH2		–	AI	Baseband receiver input, in-phase plus, channel 2
BK38	BBRX_IM_CH2		–	AI	Baseband receiver input, in-phase minus, channel 2
BJ39	BBRX_QP_CH2		–	AI	Baseband receiver input, quadrature plus, channel 2
BG39	BBRX_QM_CH2		–	AI	Baseband receiver input, quadrature minus, channel 2
BH40	BBRX_IP_CH3		–	AI	Baseband receiver input, in-phase plus, channel 3
BG41	BBRX_IM_CH3		–	AI	Baseband receiver input, in-phase minus, channel 3
BH42	BBRX_QP_CH3		–	AI	Baseband receiver input, quadrature plus, channel 3
BJ43	BBRX_QM_CH3		–	AI	Baseband receiver input, quadrature minus, channel 3
WTR1605/WTR1605L – GNSS Rx baseband interface					
BC33	GNSS_BB_IP		–	AI	GNSS receiver baseband input, in-phase plus
BC35	GNSS_BB_IM		–	AI	GNSS receiver baseband input, in-phase minus
BC29	GNSS_BB_QP		–	AI	GNSS receiver baseband input, quadrature plus

Table 2-9 Pin descriptions – chipset interface functions (cont.)

Pad #	Pad name and/or function	Pad name or alt function	Pad characteristics [1]		Functional description
			Voltage	Type	
BC31	GNSS_BB_QM		–	AI	GNSS receiver baseband input, quadrature minus
WTR1605/WTR1605L – Tx baseband interfaces					
BE23	TX_DAC0_IP		–	AO	Transmitter DAC 0 output, in-phase plus
BD22	TX_DAC0_IM		–	AO	Transmitter DAC 0 output, in-phase minus
BF22	TX_DAC0_QP		–	AO	Transmitter DAC 0 output, quadrature plus
BE21	TX_DAC0_QM		–	AO	Transmitter DAC 0 output, quadrature minus
BF24	TX_DAC0_IREF		–	AI	Transmitter DAC 0 current reference
BE25	TX_DAC0_VREF		–	AI	Transmitter DAC 0 voltage reference
BE35	TX_DAC1_IP		–	AO	Transmitter DAC 1 output, in-phase plus
BF36	TX_DAC1_IM		–	AO	Transmitter DAC 1 output, in-phase minus
BF32	TX_DAC1_QP		–	AO	Transmitter DAC 1 output, quadrature plus
BE31	TX_DAC1_QM		–	AO	Transmitter DAC 1 output, quadrature minus
BG35	TX_DAC1_IREF		–	AI	Transmitter DAC 1 current reference
BF34	TX_DAC1_VREF		–	AI	Transmitter DAC 1 voltage reference
Envelope tracking control signals					
BG33	ET_DAC_P		–	AO	Envelope tracking DAC output, plus
BH32	ET_DAC_M		–	AO	Envelope tracking DAC output, minus
WTR1605/WTR1605L – GSM transmit phase adjust signals					
BD20	GSM_TX_PHASE_D2	GPIO_137	P3	DO-Z B-PD:nppukp	GSM transmit phase adjust data bit 2 Configurable I/O
BJ19	GSM_TX_PHASE_D1	GPIO_138	P3	DO-Z B-PD:nppukp	GSM transmit phase adjust data bit 1 Configurable I/O
BE19	GSM_TX_PHASE_D0	GPIO_139	P3	DO-Z B-PD:nppukp	GSM transmit phase adjust data bit 0 Configurable I/O
WTR1605/WTR1605L – status and control signals					
BH16	SSBI1_RFIC0	GPIO_133	P3	B B-PD:nppukp	SSBI 1 for RFIC 0 Configurable I/O
BG17	SSBI2_RFIC0	GPIO_134	P3	B B-PD:nppukp	SSBI 2 for RFIC 0 Configurable I/O
BJ15	SSBI1_RFIC1	GPIO_135	P3	B B-PD:nppukp	SSBI 1 for RFIC 1 Configurable I/O
BK14	SSBI2_RFIC1	GPIO_136	P3	B B-PD:nppukp	SSBI 2 for RFIC 1 Configurable I/O
BH18	RF_ON0	GPIO_111	P3	DO B-PD:nppukp	RFIC 0 on/off control Configurable I/O
BG15	RF_ON1	GPIO_125	P3	DO B-PD:nppukp	RFIC 1 on/off control Configurable I/O
BK18	RX_ON0	GPIO_110	P3	DO B-PD:nppukp	RF receiver 0 on/off control Configurable I/O
BF16	RX_ON1	GPIO_124	P3	DO B-PD:nppukp	RF receiver 1 on/off control Configurable I/O

Table 2-9 Pin descriptions – chipset interface functions (cont.)

Pad #	Pad name and/or function	Pad name or alt function	Pad characteristics [1]		Functional description
			Voltage	Type	
PMIC interfaces					
W47	SLEEP_CLK		P3	DI	Sleep clock
Y44	CXO		P3	DI	Core crystal oscillator (system clock at 19.2 MHz)
W45	CXO_EN		P3	DO	Core crystal oscillator enable
V44	RESIN_N		P3	DI	Reset input
V48	PMIC_SPMI_DATA		P3	B	Slave and PBUS interface for PMICs – data
W49	PMIC_SPMI_CLK		P3	DO	Slave and PBUS interface for PMICs – clock
Y46	PS_HOLD		P3	DO	Power-supply hold signal to PMIC
WCN3660 – WLAN signals					
E25	WLAN_BB_IP		–	AI, AO	WLAN baseband Rx/Tx switched, in-phase plus
G25	WLAN_BB_IM		–	AI, AO	WLAN baseband Rx/Tx switched, in-phase minus
E23	WLAN_BB_QP		–	AI, AO	WLAN baseband Rx/Tx switched, quadrature plus
F24	WLAN_BB_QM		–	AI, AO	WLAN baseband Rx/Tx switched, quadrature minus
B24	WLAN_REXT		–	AI	WLAN external resistor
G19	WLAN_DATA_2	GPIO_36	P3	B B-PD:nppukp	WLAN data bit 2 Configurable I/O
A19	WLAN_DATA_1	GPIO_37	P3	B B-PD:nppukp	WLAN data bit 1 Configurable I/O
F18	WLAN_DATA_0	GPIO_38	P3	B B-PD:nppukp	WLAN data bit 0 Configurable I/O
F20	WLAN_SET	GPIO_39	P3	DO-Z B-PD:nppukp	WLAN set Configurable I/O
E17	WLAN_CLK	GPIO_40	P3	DO-Z B-PD:nppukp	WLAN data clock Configurable I/O
WCN3660 – Bluetooth signals					
D20	BT_SSBI	GPIO_35	P3	B B-PD:nppukp	Bluetooth SSBI Configurable I/O
B18	BT_CTL	GPIO_43	P3	DO B-PD:nppukp	Bluetooth control Configurable I/O
C21	BT_DATA_STROBE	GPIO_44	P3	B B-PD:nppukp	Bluetooth dual function: data and strobe Configurable I/O
WCN3660 – FM radio signals					
D18	FM_SSBI	GPIO_41	P3	B B-PD:nppukp	FM-radio SSBI Configurable I/O
C19	FM_SDI	GPIO_42	P3	B B-PD:nppukp	FM-radio serial data interface Configurable I/O
WCN3660 – shared WLAN / BT / FM radio signals					
B28	WCN_XO		P3	DI	Shared XO for the wireless connectivity subsystem
BC47	WCN_TX_COEX_LTE	GPIO_132	P3	DI B-PD:nppukp	WCN transmitter sync for coexistence with LTE Configurable I/O
BD46	LTE_TX_COEX_WCN	GPIO_131	P3	DO B-PD:nppukp	LTE transmitter sync for coexistence with WCN Configurable I/O

Table 2-9 Pin descriptions – chipset interface functions (cont.)

Pad #	Pad name and/or function	Pad name or alt function	Pad characteristics [1]		Functional description
			Voltage	Type	
WCD9320 interfaces					
–	*See Table 2-4 for SLIMbus bidirectional multiplexed audio.*				
–	*Also see Table 2-4 for I2S and I2C connectivity ports that can be used as an alternative.*				
Qualcomm RFFE interfaces					
AY46	TX_GTR_THRESH	GPIO_116	P3	DO B-PD:nppukp	Transmit level is greater than the threshold for QFE Configurable I/O
AV46	SSBI_PA	GPIO_109	P3	B B-PD:nppuk	SSBI for QFE power amplifier Configurable I/O
BC45	RFFE1_CLK	GPIO_140	P3	B B-PD:nppuk	RF front-end 1 interface clock Configurable I/O
BE47	RFFE1_DATA	GPIO_141	P3	B B-PD:nppuk	RF front-end 1 interface data Configurable I/O
BG47	RFFE2_CLK	GPIO_142	P3	B B-PD:nppuk	RF front-end 2 interface clock Configurable I/O
BF46	RFFE2_DATA	GPIO_143	P3	B B-PD:nppuk	RF front-end 2 interface data Configurable I/O
AU45	SSBI_ANT_TUNER1	GPIO_108	P3	B B-PD:nppukp	SSBI for QFE antenna tuner 1 Configurable I/O

1. Refer to Table 2-1 for parameter and acronym definitions.

NOTE GPIO pins can support multiple functions. To assign GPIOs to particular functions (such as the options listed in the table above), designers must identify all their application's requirements and map each GPIO to its function – carefully avoiding conflicts in GPIO assignments. Refer to Table 2-11 for a list of all supported functions for each GPIO.

Table 2-10 Pin descriptions – RF front-end functions

Pad #	Pad name and/or function	Pad name or alt function	Pad characteristics [1]		Functional description
			Voltage	Type	
Power amplifier controls					
AR45	PA_ON0	GPIO_104	P3	DO B-PD:nppukp	PA 0 on/off control Configurable I/O
AT48	PA_ON1	GPIO_105	P3	DO B-PD:nppukp	PA 1 on/off control Configurable I/O
AT46	PA_ON2	GPIO_106	P3	DO B-PD:nppukp	PA 2 on/off control Configurable I/O
AU47	PA_ON3	GPIO_107	P3	DO B-PD:nppukp	PA 3 on/off control Configurable I/O
AU45	PA_ON4	GPIO_108	P3	DO B-PD:nppukp	PA 4 on/off control Configurable I/O
AV46	PA_ON5	GPIO_109	P3	DO B-PD:nppukp	PA 5 on/off control Configurable I/O
BF46	PA_ON6	GPIO_143	P3	DO B-PD:nppukp	PA 6 on/off control Configurable I/O

Table 2-10 Pin descriptions – RF front-end functions (cont.)

Pad #	Pad name and/or function	Pad name or alt function	Pad characteristics [1]		Functional description
			Voltage	Type	
BF20	PA0_RANGE0	GPIO_112	P3	DO B-PD:nppukp	PA set 0 range control bit 0 Configurable I/O
BG19	PA0_RANGE1	GPIO_113	P3	DO B-PD:nppukp	PA set 0 range control bit 1 Configurable I/O
BE17	PA1_RANGE0	GPIO_118	P3	DO B-PD:nppukp	PA set 1 range control bit 0 Configurable I/O
BF18	PA1_RANGE1	GPIO_119	P3	DO B-PD:nppukp	PA set 1 range control bit 1 Configurable I/O
AY48	PA_INDICATOR	GPIO_117	P3	DO B-PD:nppukp	PA indicator Configurable I/O
General RF control (GRFC) signals					
AR45	GRFC_0	GPIO_104	P3	DO B-PD:nppukp	Generic RF controller bit 0 Configurable I/O
AT48	GRFC_1	GPIO_105	P3	DO B-PD:nppukp	Generic RF controller bit 1 Configurable I/O
AT46	GRFC_2	GPIO_106	P3	DO B-PD:nppukp	Generic RF controller bit 2 Configurable I/O
AU47	GRFC_3	GPIO_107	P3	DO B-PD:nppukp	Generic RF controller bit 3 Configurable I/O
AU45	GRFC_4	GPIO_108	P3	DO B-PD:nppukp	Generic RF controller bit 4 Configurable I/O
AV46	GRFC_5	GPIO_109	P3	DO B-PD:nppukp	Generic RF controller bit 5 Configurable I/O
BK18	GRFC_6	GPIO_110	P3	DO B-PD:nppukp	Generic RF controller bit 6 Configurable I/O
BH18	GRFC_7	GPIO_111	P3	DO B-PD:nppukp	Generic RF controller bit 7 Configurable I/O
BF20	GRFC_8	GPIO_112	P3	DO B-PD:nppukp	Generic RF controller bit 8 Configurable I/O
BG19	GRFC_9	GPIO_113	P3	DO B-PD:nppukp	Generic RF controller bit 9 Configurable I/O
AW47	GRFC_10	GPIO_114	P3	DO B-PD:nppukp	Generic RF controller bit 10 Configurable I/O
AV48	GRFC_11	GPIO_115	P3	DO B-PD:nppukp	Generic RF controller bit 11 Configurable I/O
AY46	GRFC_12	GPIO_116	P3	DO B-PD:nppukp	Generic RF controller bit 12 Configurable I/O
AY48	GRFC_13	GPIO_117	P3	DO B-PD:nppukp	Generic RF controller bit 13 Configurable I/O
BE17	GRFC_14	GPIO_118	P3	DO B-PD:nppukp	Generic RF controller bit 14 Configurable I/O
BF18	GRFC_15	GPIO_119	P3	DO B-PD:nppukp	Generic RF controller bit 15 Configurable I/O
BA47	GRFC_16	GPIO_120	P3	DO B-PD:nppukp	Generic RF controller bit 16 Configurable I/O
BA45	GRFC_17	GPIO_121	P3	DO B-PD:nppukp	Generic RF controller bit 17 Configurable I/O

Table 2-10 Pin descriptions – RF front-end functions (cont.)

Pad #	Pad name and/or function	Pad name or alt function	Pad characteristics [1]		Functional description
			Voltage	Type	
BB48	GRFC_18	GPIO_122	P3	DO B-PD:nppukp	Generic RF controller bit 18 Configurable I/O
BH46	GRFC_19	GPIO_123	P3	DO B-PD:nppukp	Generic RF controller bit 19 Configurable I/O
BF16	GRFC_20	GPIO_124	P3	DO B-PD:nppukp	Generic RF controller bit 20 Configurable I/O
BG15	GRFC_21	GPIO_125	P3	DO B-PD:nppukp	Generic RF controller bit 21 Configurable I/O
BD18	GRFC_22	GPIO_126	P3	DO B-PD:nppukp	Generic RF controller bit 22 Configurable I/O
BH14	GRFC_23	GPIO_127	P3	DO B-PD:nppukp	Generic RF controller bit 23 Configurable I/O
BK10	GRFC_24	GPIO_128	P3	DO B-PD:nppukp	Generic RF controller bit 24 Configurable I/O
BK14	GRFC_25	GPIO_136	P3	DO B-PD:nppukp	Generic RF controller bit 25 Configurable I/O
BD20	GRFC_26	GPIO_137	P3	DO B-PD:nppukp	Generic RF controller bit 26 Configurable I/O
BE47	GRFC_27	GPIO_141	P3	DO B-PD:nppukp	Generic RF controller bit 27 Configurable I/O
BF46	GRFC_28	GPIO_143	P3	DO B-PD:nppukp	Generic RF controller bit 28 Configurable I/O

1. Refer to Table 2-1 for parameter and acronym definitions.

NOTE GPIO pins can support multiple functions. To assign GPIOs to particular functions (such as the options listed in the table above), designers must identify all their application's requirements and map each GPIO to its function – carefully avoiding conflicts in GPIO assignments. Refer to Table 2-11 for a list of all supported functions for each GPIO.

NOTE Handset designers must examine each GPIO's external connection and programmed configuration, and take steps necessary to avoid excessive leakage current. Combinations of the following factors must be controlled properly:

- GPIO configuration
  - Input versus output
  - Pull-up or pull-down
- External connections
  - Unused inputs
  - Connections to high-impedance (tri-state) outputs
  - Connections to external devices that may not be attached

To help designers define their products' GPIO assignments, Qualcomm provides an Excel spreadsheet that lists all MSM8x74 GPIOs (in numeric order), pad numbers, pad voltages, pull states, and available configurations.

NOTE Click the link below to download the *MSM8274/MSM8674/MSM8974 GPIO Configuration Spreadsheet* (80-NA437-1B) from the CDMATech Support Website.

This link will be included in future revisions of this document.

If you have permission to view the document, a prompt will be presented for initiating the download.

NOTE Subscribe to the pin assignment spreadsheet to be notified of any changes.

Click the **Help** button to download the latest revision of *Using CDMATech Support Documents and Downloads User Guide* (80-V7273-1). This document includes subscription instructions.

Table 2-11 Pin descriptions – general-purpose input/output ports

Pad #	Pad name	Configurable function	Pad characteristics [1]		Functional description
			Voltage	Type	
C9	GPIO_145	HSIC_DATA	P4	B-PD:nppukp DO	Configurable I/O HSIC data
F10	GPIO_144	HSIC_STROBE	P4	B-PD:nppukp DO	Configurable I/O HSIC strobe
BF46	GPIO_143	GRFC_28 RFFE2_DATA PA_ON6	P3	B-PD:nppukp DO B DO	Configurable I/O Generic RF controller bit 28 RF front-end 2 interface data PA 6 on/off control
BG47	GPIO_142	RFFE2_CLK	P3	B-PD:nppukp DO	Configurable I/O RF front-end 2 interface clock
BE47	GPIO_141	GRFC_27 RFFE1_DATA	P3	B-PD:nppukp DO B	Configurable I/O Generic RF controller bit 27 RF front-end 1 interface data
BC45	GPIO_140	RFFE1_CLK	P3	B-PD:nppukp DO	Configurable I/O RF front-end 1 interface clock
BE19	GPIO_139	GSM_TX_PHASE_D0	P3	B-PD:nppukp DO-Z	Configurable I/O GSM transmit phase adjust data bit 0
BJ19	GPIO_138	GSM_TX_PHASE_D1	P3	B-PD:nppukp DO-Z	Configurable I/O GSM transmit phase adjust data bit 1
BD20	GPIO_137	GRFC_26 GSM_TX_PHASE_D2	P3	B-PD:nppukp DO DO-Z	Configurable I/O Generic RF controller bit 26 GSM transmit phase adjust data bit 2
BK14	GPIO_136	GRFC_25 SSBI2_RFIC1	P3	B-PD:nppukp DO B	Configurable I/O Generic RF controller bit 25 SSBI 2 for RFIC 1
BJ15	GPIO_135	SSBI1_RFIC1	P3	B-PD:nppukp B	Configurable I/O SSBI 1 for RFIC 1
BG17	GPIO_134	SSBI2_RFIC0	P3	B-PD:nppukp B	Configurable I/O SSBI 2 for RFIC 0

Table 2-11 Pin descriptions – general-purpose input/output ports (cont.)

Pad #	Pad name	Configurable function	Pad characteristics [1]		Functional description
			Voltage	Type	
BH16	GPIO_133	SSBI1_RFIC0	P3	B-PD:nppukp B	Configurable I/O SSBI 1 for RFIC 0
BC47	GPIO_132	WCN_TX_COEX_LTE	P3	B-PD:nppukp DI	Configurable I/O WCN transmitter sync for coexistence with LTE
BD46	GPIO_131	LTE_TX_COEX_WCN	P3	B-PD:nppukp DO	Configurable I/O LTE transmitter sync for coexistence with WCN
BB46	GPIO_130	LTE_ACTIVE	P3	B-PD:nppukp DO	Configurable I/O LTE transmitter is active
BJ11	GPIO_129	GNSS_TX_AGGRESSOR	P3	B-PD:nppukp DI	Configurable I/O Tx level may degrade GNSS receiver
BK10	GPIO_128	GRFC_24 EXT_GNSS_LNA_EN	P3	B-PD:nppukp DO DO	Configurable I/O Generic RF controller bit 24 External GNSS LNA enable
BH14	GPIO_127	GRFC_23 BC1_SW_SEL1	P3	B-PD:nppukp DO DO	Configurable I/O Generic RF controller bit 23 BC1 switch select bit 1
BD18	GPIO_126	GRFC_22 ANT_SW_SEL4	P3	B-PD:nppukp DO DO	Configurable I/O Generic RF controller bit 22 Antenna switch select bit 4
BG15	GPIO_125	GRFC_21 RF_ON1	P3	B-PD:nppukp DO DO	Configurable I/O Generic RF controller bit 21 RFIC 1 on/off control
BF16	GPIO_124	GRFC_20 RX_ON1	P3	B-PD:nppukp DO DO	Configurable I/O Generic RF controller bit 20 RF receiver 1 on/off control
BH46	GPIO_123	GRFC_19 1X_MRD_SW_SEL	P3	B-PD:nppukp DO DO	Configurable I/O Generic RF controller bit 19 1x mobile receive diversity switch select
BB48	GPIO_122	GRFC_18 PRX_SW_SEL1	P3	B-PD:nppukp DO DO	Configurable I/O Generic RF controller bit 18 Primary receiver switch selection bit 1
BA45	GPIO_121	GRFC_17 PRX_SW_SEL0	P3	B-PD:nppukp DO DO	Configurable I/O Generic RF controller bit 17 Primary receiver switch selection bit 0
BA47	GPIO_120	GRFC_16 1X_BC0_BC1_SEL	P3	B-PD:nppukp DO DO	Configurable I/O Generic RF controller bit 16 Selects 1x BC0 or BC1
BF18	GPIO_119	GRFC_15 PA1_RANGE1	P3	B-PD:nppukp DO DO	Configurable I/O Generic RF controller bit 15 PA set 1 range control bit 1
BE17	GPIO_118	GRFC_14 PA1_RANGE0	P3	B-PD:nppukp DO DO	Configurable I/O Generic RF controller bit 14 PA set 1 range control bit 0
AY48	GPIO_117	GRFC_13 PA_INDICATOR SDC1_EMMC_1P2_EN	P3	B-PD:nppukp DO DO DI	Configurable I/O Generic RF controller bit 13 PA indicator Enables 1.2 V I/O for eMMC on SDC1

Table 2-11 Pin descriptions – general-purpose input/output ports (cont.)

Pad #	Pad name	Configurable function	Pad characteristics [1]		Functional description
			Voltage	Type	
AY46	GPIO_116		P3	B-PD:nppukp	Configurable I/O
		GRFC_12		DO	Generic RF controller bit 12
		TX_GTR_THRESH		DO	Transmit level is greater than the threshold for QFE
		BOOT_CONFIG_4		DI	Boot configuration control bit 4 for FAST_BOOT_SEL[3]
AV48	GPIO_115		P3	B-PD:nppukp	Configurable I/O
		GRFC_11		DO	Generic RF controller bit 11
		DRX_SW_SEL1		DO	Diversity receiver switch selection bit 1
		BOOT_CONFIG_3		DI	Boot configuration control bit 3 for FAST_BOOT_SEL[2]
AW47	GPIO_114		P3	B-PD:nppukp	Configurable I/O
		GRFC_10		DO	Generic RF controller bit 10
		DRX_SW_SEL0		DO	Diversity receiver switch selection bit 0
		BOOT_CONFIG_2		DI	Boot configuration control bit 2 for FAST_BOOT_SEL[1]
BG19	GPIO_113		P3	B-PD:nppukp	Configurable I/O
		GRFC_9		DO	Generic RF controller bit 9
		PA0_RANGE1		DO	PA set 0 range control bit 1
		BOOT_CONFIG_1		DI	Boot configuration control bit 1 for FAST_BOOT_SEL[0]
BF20	GPIO_112		P3	B-PD:nppukp	Configurable I/O
		GRFC_8		DO	Generic RF controller bit 8
		PA0_RANGE0		DO	PA set 0 range control bit 0
		BOOT_CONFIG_0		DI	Boot configuration control bit 0 for WDOG_DISABLE
BH18	GPIO_111		P3	B-PD:nppukp	Configurable I/O
		GRFC_7		DO	Generic RF controller bit 7
		RF_ON0		DO	RFIC 0 on/off control
BK18	GPIO_110		P3	B-PD:nppukp	Configurable I/O
		GRFC_6		DO	Generic RF controller bit 6
		RX_ON0		DO	RF receiver 0 on/off control
AV46	GPIO_109		P3	B-PD:nppukp	Configurable I/O
		GRFC_5		DO	Generic RF controller bit 5
		PA_ON5		DO	PA 5 on/off control
		SSBI_PA		B	SSBI for QFE power amplifier
AU45	GPIO_108		P3	B-PD:nppukp	Configurable I/O
		GRFC_4		DO	Generic RF controller bit 4
		PA_ON4		DO	PA 4 on/off control
		SSBI_ANT_TUNER1		B	SSBI for QFE antenna tuner 1
AU47	GPIO_107		P3	B-PD:nppukp	Configurable I/O
		GRFC_3		DO	Generic RF controller bit 3
		PA_ON3		DO	PA 3 on/off control
AT46	GPIO_106		P3	B-PD:nppukp	Configurable I/O
		GRFC_2		DO	Generic RF controller bit 2
		PA_ON2		DO	PA 2 on/off control
AT48	GPIO_105		P3	B-PD:nppukp	Configurable I/O
		GRFC_1		DO	Generic RF controller bit 1
		PA_ON1		DO	PA 1 on/off control
AR45	GPIO_104		P3	B-PD:nppukp	Configurable I/O
		GRFC_0		DO	Generic RF controller bit 0
		PA_ON0		DO	PA 0 on/off control
AR47	GPIO_103		P3	B-PD:nppukp	Configurable I/O
		FORCED_USB_BOOT		DI	Forced USB boot
AF2	GPIO_102		P3	B-PD:nppukp	Configurable I/O
		EDP_HOT_PLUG_DET		DI	EDP hot plug detect

Table 2-11 Pin descriptions – general-purpose input/output ports (cont.)

Pad #	Pad name	Configurable function	Pad characteristics [1]		Functional description
			Voltage	Type	
AA47	GPIO_101	UIM_BATT_ALARM	P3	B-PD:nppukp DI	Configurable I/O UIM battery alarm
Y48	GPIO_100	UIM1_DET	P3	B-PD:nppukp DI	Configurable I/O UIM1 detect
Y50	GPIO_99	UIM1_RESET	P5	BH-PD:nppukp DO	Configurable I/O UIM1 reset (dual-voltage)
AC45	GPIO_98	UIM1_CLK	P5	BH-PD:nppukp DO	Configurable I/O UIM1 clock (dual-voltage)
AB46	GPIO_97	UIM1_DATA	P5	BH-PD:nppukp B	Configurable I/O UIM1 data (dual-voltage)
D28	GPIO_96	TSIF2_SYNC SDC4_DATA_0	P3	B-PD:nppukp DI B	Configurable I/O Transport stream interface 2 sync Secure digital controller 4 data bit 0
C25	GPIO_95	TSIF2_DATA SDC4_DATA_1	P3	B-PD:nppukp DI B	Configurable I/O Transport stream interface 2 data Secure digital controller 4 data bit 1
A27	GPIO_94	TSIF2_EN SDC4_DATA_2	P3	B-PD:nppukp DI B	Configurable I/O Transport stream interface 2 enable Secure digital controller 4 data bit 2
E27	GPIO_93	TSIF2_CLK SDC4_CLK	P3	B-PD:nppukp DI DO	Configurable I/O Transport stream interface 2 clock Secure digital controller 4 clock
D26	GPIO_92	TSIF1_SYNC SDC4_DATA_3 QDSS_ETM_TRSYNC_B	P3	B-PD:nppukp DI B DO	Configurable I/O Transport stream interface 1 sync Secure digital controller 4 data bit 3 ETM trace data sync B
D24	GPIO_91	TSIF1_DATA SDC4_CMD QDSS_ETM_TRDATA_0B	P3	B-PD:nppukp DI B DO	Configurable I/O Transport stream interface 1 data Secure digital controller 4 command ETM trace data bit 0B
C27	GPIO_90	TSIF1_EN SPI_CS3_N_BLSP10 QDSS_ETM_TRDATA_1B	P3	B-PD:nppukp DI DO-Z DO	Configurable I/O Transport stream interface 1 enable Chip select 3 for SPI on BLSP #10 ETM trace data bit 1B
F26	GPIO_89	TSIF1_CLK QDSS_ETM_TRCLK_B	P3	B-PD:nppukp DI DO	Configurable I/O Transport stream interface 1 clock ETM trace data clock B
H44	GPIO_88	BLSP12_0	P3	B-PD:nppukp B	Configurable I/O BLSP #12 bit 0;
E47	GPIO_87	BLSP12_1	P3	B-PD:nppukp B	Configurable I/O BLSP #12, bit 1;
D42	GPIO_86	BLSP12_2 GP_PDM_1A	P3	B-PD:nppukp B DO	Configurable I/O BLSP #12, bit 2; General-purpose PDM 1A output
C41	GPIO_85	BLSP12_3	P3	B-PD:nppukp B	Configurable I/O BLSP #12, bit 3;C
E33	GPIO_84	BLSP11_0	P3	B-PD:nppukp B	Configurable I/O BLSP #11 bit 0;C
F32	GPIO_83	BLSP11_1	P3	B-PD:nppukp B	Configurable I/O BLSP #11, bit 1;

Table 2-11 Pin descriptions – general-purpose input/output ports (cont.)

Pad #	Pad name	Configurable function	Pad characteristics [1]		Functional description
			Voltage	Type	
D32	GPIO_82		P3	B-PD:nppukp	Configurable I/O
		BLSP11_2		B	BLSP #11, bit 2;
		MI2S_2_SD1		B	MI2S #2 serial data channel 1
		AUDIO_PCM_DOUT		B	Secondary audio PCM data output (port 1)
		GCC_GP_CLK_3B		DO	Global general purpose clock 3B
A31	GPIO_81		P3	B-PD:nppukp	Configurable I/O
		BLSP11_3		B	BLSP #11, bit 3;
		MI2S_2_SD0		B	MI2S #2 serial data channel 0
		AUDIO_PCM_DIN		B	Secondary audio PCM data input (port 1)
		GCC_GP_CLK_2B		DO	Global general purpose clock 2B
R49	GPIO_80		P3	B-PD:nppukp	Configurable I/O
		MI2S_2_WS		B	MI2S #2 word select (L/R)
		AUDIO_PCM_SYNC		B	Secondary audio PCM sync (port 1)
N45	GPIO_79		P3	B-PD:nppukp	Configurable I/O
		MI2S_2_SCLK		B	MI2S #2 bit clock
		GP_PDM_2A		DO	General-purpose PDM 2A output
		AUDIO_PCM_CLK		B	Secondary audio PCM clock (port 1)
M50	GPIO_78		P3	B-PD:nppukp	Configurable I/O
		MI2S_2_MCLK		DO	MI2S #2 master clock
		GCC_GP_CLK_1B		DO	Global general purpose clock 1B
M46	GPIO_77		P3	B-PD:nppukp	Configurable I/O
		MI2S_3_SD1		B	MI2S #3 serial data channel 1
		AUDIO_PCM_DOUT		B	Primary audio PCM data output (port 2)
M48	GPIO_76		P3	B-PD:nppukp	Configurable I/O
		MI2S_3_SD0		B	MI2S #3 serial data channel 0
		AUDIO_PCM_DIN		B	Primary audio PCM data input (port 2)
L49	GPIO_75		P3	B-PD:nppukp	Configurable I/O
		MI2S_3_WS		B	MI2S #3 word select (L/R)
		AUDIO_PCM_SYNC		B	Primary audio PCM sync (port 2)
L47	GPIO_74		P3	B-PD:nppukp	Configurable I/O
		MI2S_3_SCLK		B	MI2S #3 bit clock
		GP_PDM_1B		DO	General-purpose PDM 1B output
		AUDIO_PCM_CLK		B	Primary audio PCM clock (port 2)
K48	GPIO_73		P3	B-PD:nppukp	Configurable I/O
		MI2S_3_MCLK		DO	MI2S #3 master clock
L45	GPIO_72		P3	B-PD:nppukp	Configurable I/O
		SPKR_I2S_WS		B	Speaker I2S word select (L/R)
K46	GPIO_71		P3	B-PD:nppukp	Configurable I/O
		SLIMBUS_DATA		DO	SLIMbus data
		SPKR_I2S_DOUT		DO	Speaker I2S data output
J45	GPIO_70		P3	B-PD:nppukp	Configurable I/O
		SLIMBUS_CLK		DO	SLIMbus clock
		SPKR_I2S_SCK		B	Speaker I2S bit clock
G49	GPIO_69		P3	B-PD:nppukp	Configurable I/O
		SLIMBUS_MCLK		DO	SLIMbus master clock
		SPKR_I2S_MCLK		DO	Speaker I2S master clock
H48	GPIO_68		P3	B-PD:nppukp	Configurable I/O
		MI2S_1_SD1		B	MI2S #1 serial data channel 1
		SPI_CS2B_N_BLSP10		DO-Z	Chip select 2B for SPI on BLSP #10
		GP_PDM_0A		DO	General-purpose PDM output 0A
		AUDIO_PCM_DOUT		B	Primary audio PCM data output (port 1)

Table 2-11 Pin descriptions – general-purpose input/output ports (cont.)

Pad #	Pad name	Configurable function	Pad characteristics [1]		Functional description
			Voltage	Type	
H46	GPIO_67		P3	B-PD:nppukp	Configurable I/O
		MI2S_1_SD0		B	MI2S #1 serial data channel 0
		SPI_CS1B_N_BLSP10		DO-Z	Chip select 1B for SPI on BLSP #10
		AUDIO_PCM_DIN		B	Primary audio PCM data input (port 1)
F48	GPIO_66		P3	B-PD:nppukp	Configurable I/O
		MI2S_1_WS		B	MI2S #1 word select (L/R)
		SPI_CS3_N_BLSP2		DO-Z	Chip select 3 for SPI on BLSP #2
		AUDIO_PCM_SYNC		B	Primary audio PCM sync (port 1)
G47	GPIO_65		P3	B-PD:nppukp	Configurable I/O
		MI2S_1_SCLK		B	MI2S #1 bit clock
		AUDIO_PCM_CLK		B	Primary audio PCM clock (port 1)
D48	GPIO_64		P3	B-PD:nppukp	Configurable I/O
		MI2S_1_MCLK		DO	MI2S #1 master clock
D40	GPIO_63		P3	B-PD:nppukp	Configurable I/O
		MI2S_4_SD3		B	MI2S #4 serial data channel 3
		SPI_CS2B_N_BLSP2		DO-Z	Chip select 2B for SPI on BLSP #2
		GP_PDM_2B		DO	General-purpose PDM output 2B
D38	GPIO_62		P3	B-PD:nppukp	Configurable I/O
		MI2S_4_SD2		B	MI2S #4 serial data channel 2
		SPI_CS1B_N_BLSP2		DO-Z	Chip select 1B for SPI on BLSP #2
D36	GPIO_61		P3	B-PD:nppukp	Configurable I/O
		MI2S_4_SD1		B	MI2S #4 serial data channel 1
		AUDIO_PCM_DOUT		B	Secondary audio PCM data output (port 2)
E35	GPIO_60		P3	B-PD:nppukp	Configurable I/O
		MI2S_4_SD0		B	MI2S #4 serial data channel 0
		AUDIO_PCM_DIN		B	Secondary audio PCM data input (port 2)
D34	GPIO_59		P3	B-PD:nppukp	Configurable I/O
		MI2S_4_WS		B	MI2S #4 word select (L/R)
		AUDIO_PCM_SYNC		B	Secondary audio PCM sync (port 2)
		GCC_GP_CLK_3A		DO	Global general purpose clock 3A
C35	GPIO_58		P3	B-PD:nppukp	Configurable I/O
		MI2S_4_SCLK		B	MI2S #4 bit clock
		AUDIO_PCM_CLK		B	Secondary audio PCM clock (port 2)
		GCC_GP_CLK_2A		DO	Global general purpose clock 2A
C33	GPIO_57		P3	B-PD:nppukp	Configurable I/O
		MI2S_4_MCLK		DO	MI2S #4 master clock
		GCC_GP_CLK_1A		DO	Global general purpose clock 1A
A23	GPIO_56		P3	B-PD:nppukp	Configurable I/O
		BLSP10_0		B	BLSP #10, bit 0
C23	GPIO_55		P3	B-PD:nppukp	Configurable I/O
		BLSP10_1		B	BLSP #10, bit 1
D22	GPIO_54		P3	B-PD:nppukp	Configurable I/O
		BLSP10_2		B	BLSP #10, bit 2
		SPI_CS2A_N_BLSP2		DO-Z	Chip select 2A for SPI on BLSP #2
		GP_PDM_0B		DO	General-purpose PDM output 0B
B22	GPIO_53		P3	B-PD:nppukp	Configurable I/O
		BLSP10_3		B	BLSP #10, bit 3
		SPI_CS1A_N_BLSP2		DO-Z	Chip select 1A for SPI on BLSP #2
AH50	GPIO_52		P3	B-PD:nppukp	Configurable I/O
		BLSP9_0		B	BLSP #9, bit 0
		UIM2_DET		DI	UIM2 detect

Table 2-11 Pin descriptions – general-purpose input/output ports (cont.)

Pad #	Pad name	Configurable function	Pad characteristics [1]		Functional description
			Voltage	Type	
AE47	GPIO_51		P6	BH-PD:nppukp	Configurable I/O
		BLSP9_1		B	BLSP #9, bit 1
		UIM2_RESET		DO	UIM2 reset (dual-voltage)
AC49	GPIO_50		P6	BH-PD:nppukp	Configurable I/O
		BLSP9_2		B	BLSP #9, bit 2
		UIM2_CLK		DO	UIM2 clock (dual-voltage)
AA49	GPIO_49		P6	BH-PD:nppukp	Configurable I/O
		BLSP9_3		B	BLSP #9, bit 3
		UIM2_DATA		B	UIM2 data (dual-voltage)
C17	GPIO_48		P3	B-PD:nppukp	Configurable I/O
		BLSP8_0		B	BLSP #8, bit 0
		SPI_CS2A_N_BLSP10		DO-Z	Chip select 2A for SPI on BLSP #10
		QDSS_ETM_TRDATA_8A		DO	ETM trace data bit 8A
A15	GPIO_47		P3	B-PD:nppukp	Configurable I/O
		BLSP8_1		B	BLSP #8, bit 1
		SPI_CS1A_N_BLSP10		DO-Z	Chip select 1A for SPI on BLSP #10
		QDSS_ETM_TRDATA_9A		DO	ETM trace data bit 9A
B14	GPIO_46		P3	B-PD:nppukp	Configurable I/O
		BLSP8_2		B	BLSP #8, bit 2
		QDSS_ETM_TRDATA_10A		DO	ETM trace data bit 10A
D16	GPIO_45		P3	B-PD:nppukp	Configurable I/O
		BLSP8_3		B	BLSP #8, bit 3
		QDSS_ETM_TRDATA_11A		DO	ETM trace data bit 11A
C21	GPIO_44		P3	B-PD:nppukp	Configurable I/O
		BLSP7_0		B	BLSP #7, bit 0
		BT_DATA_STROBE		B	Bluetooth dual function: data and strobe
		QDSS_ETM_TRDATA_12A		DO	ETM trace data bit 12A
B18	GPIO_43		P3	B-PD:nppukp	Configurable I/O
		BLSP7_1		B	BLSP #7, bit 1
		BT_CTL		DO	Bluetooth control
		QDSS_ETM_TRDATA_13A		DO	ETM trace data bit 13A
C19	GPIO_42		P3	B-PD:nppukp	Configurable I/O
		BLSP7_2		B	BLSP #7, bit 2
		FM_SDI		B	FM-radio serial data interface
		QDSS_ETM_TRDATA_14A		DO	ETM trace data bit 14A
D18	GPIO_41		P3	B-PD:nppukp	Configurable I/O
		BLSP7_3		B	BLSP #7, bit 3
		FM_SSBI		B	FM-radio SSBI
		QDSS_ETM_TRDATA_15A		DO	ETM trace data bit 15A
E17	GPIO_40		P3	B-PD:nppukp	Configurable I/O
		WLAN_CLK		DO-Z	WLAN clock
		SDC3_CLK		DO	Secure digital controller 3 clock
		QDSS_ETM_TRCLK_A		DO	ETM trace data clk A
F20	GPIO_39		P3	B-PD:nppukp	Configurable I/O
		WLAN_SET		DO-Z	WLAN set
		SDC3_CMD		B	Secure digital controller 3 command
		QDSS_ETM_TRSYNC_A		DO	ETM trace data sync A
F18	GPIO_38		P3	B-PD:nppukp	Configurable I/O
		WLAN_DATA_0		B	WLAN data bit 0
		SDC3_DATA_0		B	Secure digital controller 3 data bit 0
		QDSS_ETM_TRDATA_0A		DO	ETM trace data bit 0A

Table 2-11 Pin descriptions – general-purpose input/output ports (cont.)

Pad #	Pad name	Configurable function	Pad characteristics [1]		Functional description
			Voltage	Type	
A19	GPIO_37		P3	B-PD:nppukp	Configurable I/O
		WLAN_DATA_1		B	WLAN data bit 1
		SDC3_DATA_1		B	Secure digital controller 3 data bit 1
		QDSS_ETM_TRDATA_1A		DO	ETM trace data bit 1A
G19	GPIO_36		P3	B-PD:nppukp	Configurable I/O
		WLAN_DATA_2		B	WLAN data bit 2
		SDC3_DATA_2		B	Secure digital controller 3 data bit 2
		QDSS_ETM_TRDATA_2A		DO	ETM trace data bit 2A
D20	GPIO_35		P3	B-PD:nppukp	Configurable I/O
		BT_SSBI		B	Bluetooth SSBI
		SDC3_DATA_3		B	Secure digital controller 3 data bit 3
		QDSS_ETM_TRDATA_3A		DO	ETM trace data bit 3A
AP4	GPIO_34		P3	B-PD:nppukp	Configurable I/O
		HDMI_HOT_PLUG_DET		DI	HDMI hot plug detect
		QDSS_ETM_TRDATA_4A		DO	ETM trace data bit 4A
AM2	GPIO_33		P3	B-PU:nppdkp	Configurable I/O
		HDMI_DDC_DATA		B	HDMI display data channel – data
		QDSS_ETM_TRDATA_5A		DO	ETM trace data bit 5A
AM4	GPIO_32		P3	B-PU:nppdkp	Configurable I/O
		HDMI_DDC_CLK		B	HDMI display data channel – clock
		QDSS_ETM_TRDATA_6A		DO	ETM trace data bit 6A
AN3	GPIO_31		P3	B-PU:nppdkp	Configurable I/O
		HDMI_CEC		B	HDMI consumer electronics control
		QDSS_ETM_TRDATA_7A		DO	ETM trace data bit 7A
G17	GPIO_30		P3	B-PD:nppukp	Configurable I/O
		BLSP6_0		B	BLSP #6, bit 0
F16	GPIO_29		P3	B-PD:nppukp	Configurable I/O
		BLSP6_1		B	BLSP #6, bit 1
		GP_MN		DO	General-purpose M/N:D counter output
E15	GPIO_28		P3	B-PD:nppukp	Configurable I/O
		BLSP6_2		B	BLSP #6, bit 2
		CCI_ASYNC0		DI	Camera control interface async 0
		QDSS_ETM_TRDATA_2B		DO	ETM trace data bit 2B
A11	GPIO_27		P3	B-PD:nppukp	Configurable I/O
		BLSP6_3		B	BLSP #6, bit 3
		CCI_TIMER4		DO	Camera control interface timer 4
		CCI_ASYNC2		DI	Camera control interface async 2
		GP_CLK1		DO	General-purpose clock 1
		QDSS_ETM_TRDATA_3B		DO	ETM trace data bit 3B
D14	GPIO_26		P3	B-PD:nppukp	Configurable I/O
		BLSP5_0		B	BLSP #5, bit 0
		CCI_TIMER3		DO	Camera control interface timer 3
		CCI_ASYNC1		DI	Camera control interface async 1
		GP_CLK0		DO	General-purpose clock 0
		QDSS_ETM_TRDATA_4B		DO	ETM trace data bit 4B
D12	GPIO_25		P3	B-PD:nppukp	Configurable I/O
		BLSP5_1		B	BLSP #5, bit 1
		CCI_TIMER2		DO	Camera control interface timer 2
		QDSS_ETM_TRDATA_5B		DO	ETM trace data bit 5B

Table 2-11 Pin descriptions – general-purpose input/output ports (cont.)

Pad #	Pad name	Configurable function	Pad characteristics [1]		Functional description
			Voltage	Type	
B10	GPIO_24		P3	B-PD:nppukp	Configurable I/O
		BLSP5_2		B	BLSP #5, bit 2
		CCI_TIMER1		DO	Camera control interface timer 1
		QDSS_ETM_TRDATA_6B		DO	ETM trace data bit 6B
E13	GPIO_23		P3	B-PD:nppukp	Configurable I/O
		BLSP5_3		B	BLSP #5, bit 3
		CCI_TIMER0		DO	Camera control interface timer 0
		QDSS_ETM_TRDATA_7B		DO	ETM trace data bit 7B
D10	GPIO_22		P3	B-PD:nppukp	Configurable I/O
		BLSP4_0		B	BLSP #4, bit 0
		CCI_I2C1_SCL		B	Dedicated camera control interface I2C 1 clock
		QDSS_ETM_TRDATA_8B		DO	ETM trace data bit 8B
G15	GPIO_21		P3	B-PD:nppukp	Configurable I/O
		BLSP4_1		B	BLSP #4, bit 1
		CCI_I2C1_SDA		B	Dedicated camera control interface I2C 1 serial data
		QDSS_ETM_TRDATA_9B		DO	ETM trace data bit 9B
E11	GPIO_20		P3	B-PD:nppukp	Configurable I/O
		BLSP4_2		B	BLSP #4, bit 2
		CCI_I2C0_SCL		B	Dedicated camera control interface I2C 0 clock
		QDSS_ETM_TRDATA_10B		DO	ETM trace data bit 10B
F12	GPIO_19		P3	B-PD:nppukp	Configurable I/O
		BLSP4_3		B	BLSP #4, bit 3
		CCI_I2C0_SDA		B	Dedicated camera control interface I2C 0 serial data
		QDSS_ETM_TRDATA_11B		DO	ETM trace data bit 11B
C11	GPIO_18		P3	B-PD:nppukp	Configurable I/O
		CAM_MCLK3		DO	Camera master clock 3
		QDSS_ETM_TRDATA_12B		DO	ETM trace data bit 12B
B8	GPIO_17		P3	B-PD:nppukp	Configurable I/O
		CAM_MCLK2		DO	Camera master clock 2
		QDSS_ETM_TRDATA_13B		DO	ETM trace data bit 13B
A7	GPIO_16		P3	B-PD:nppukp	Configurable I/O
		CAM_MCLK1		DO	Camera master clock 1
		QDSS_ETM_TRDATA_14B		DO	ETM trace data bit 14B
C7	GPIO_15		P3	B-PD:nppukp	Configurable I/O
		CAM_MCLK0		DO	Camera master clock 0
		QDSS_ETM_TRDATA_15B		DO	ETM trace data bit 15B
AG3	GPIO_14		P3	B-PD:nppukp	Configurable I/O
		MDP_VSYNC_E		DI	MDP vertical sync – external
AJ3	GPIO_13		P3	B-PD:nppukp	Configurable I/O
		MDP_VSYNC_S		DI	MDP vertical sync – secondary
AL3	GPIO_12		P3	B-PD:nppukp	Configurable I/O
		MDP_VSYNC_P		DI	MDP vertical sync – primary
BE11	GPIO_11		P3	B-PD:nppukp	Configurable I/O
		BLSP3_0		B	BLSP #3, bit 0
		SPI_CS2B_N_BLSP1		DO-Z	Chip select 2B for SPI on BLSP #1
BH10	GPIO_10		P3	B-PD:nppukp	Configurable I/O
		BLSP3_1		B	BLSP #3, bit 1
		SPI_CS3_N_BLSP1		DO-Z	Chip select 3 for SPI on BLSP #1
BE13	GPIO_9		P3	B-PD:nppukp	Configurable I/O
		BLSP3_2		B	BLSP #3, bit 2
		SPI_CS2A_N_BLSP1		DO-Z	Chip select 2A for SPI on BLSP #1

Table 2-11 Pin descriptions – general-purpose input/output ports (cont.)

Pad #	Pad name	Configurable function	Pad characteristics [1]		Functional description
			Voltage	Type	
BG11	GPIO_8	BLSP3_3	P3	B-PD:nppukpB	Configurable I/O BLSP #3, bit 3
E31	GPIO_7	BLSP2_0	P3	B-PD:nppukpB	Configurable I/O BLSP #2, bit 0
C31	GPIO_6	BLSP2_1	P3	B-PD:nppukpB	Configurable I/O BLSP #2, bit
D30	GPIO_5	BLSP2_2	P3	B-PD:nppukpB	Configurable I/O BLSP #2, bit 2
C29	GPIO_4	BLSP2_3	P3	B-PD:nppukpB	Configurable I/O BLSP #2, bit 3
BG13	GPIO_3	BLSP1_0	P3	B-PD:nppukpB	Configurable I/O BLSP #1, bit 0
BF12	GPIO_2	BLSP1_1	P3	B-PD:nppukpB	Configurable I/O BLSP #1, bit 1
BF14	GPIO_1	BLSP1_2	P3	B-PD:nppukpB	Configurable I/O BLSP #1, bit 2
BH12	GPIO_0	BLSP1_3	P3	B-PD:nppukpB	Configurable I/O BLSP #1, bit 3

1. Refer to Table 2-1 for parameter and acronym definitions.

Table 2-12 Pin descriptions – no connection, do not connect, and reserved pins

Pad #	Pad name	Functional description
E29, G29, AN45, AP44, BH22, BK22	DNC	Do not connect; connected internally, do not connect externally
A35, A39, A43, A47, B12, B32, B36, B40, B42, B44, B46, B48, C3, C5, C39, C43, C45, C47, C49, D4, D44, D46, E37, E39, E41, E43, E45, F8, F44, F46, H50, J47, L5, L43, M2, M8, M44, N3, N43, N49, P8, T8, U7, V8, W37, Y2, AA43, AB42, AC43, AD8, AD42, AF4, AH42, AJ43, AK2, AK42, AL43, AP8, AR11, AR13, AT50, AU49, AW41, AW43, AW49, AY50, BA33, BA43, BA49, BB22, BC1, BC3, BC5, BC9, BC17, BC23, BC43, BC49, BD30, BD32, BD34, BD44, BD50, BE3, BE27, BE43, BE45, BF44, BG23, BG31, BG37, BG43, BG45, BG49, BH2, BH20, BH24, BH36, BH44, BH50, BJ9, BJ13, BJ23, BK6, BK34, BK42, BK46	NC	No connect; not connected internally

Table 2-13 Pin descriptions – power supply pins

Pad #	Pad name	Functional description
BC37, BD38, BF28	VDD_A1	Power for analog circuits – low voltage
BD26, BE33, BE39, BF26	VDD_A2	Power for analog circuits – high voltage
AD48	VDD_ALWAYS_ON	Always-on power domain
H12, H16, H18, K44, L11, L13, L15, L31, L33, R11, R13, R15, R21, R23, R25, R35, W15, W17, W23, W33, W35, W39, W41, AB44, AC11, AC13, AC19, AC21, AE27, AG11, AG13, AG23, AG25, AG27, AG29, AG31, AG33, AH44, AL11, AL13, AL31, AL33, AL35, AU11, AV42, AW11, BC21, BC41, BD36	VDD_CORE	Power for digital core circuits
B30, D8, F42, W43, BF38	VDD_EBI0_CDC	Power for EBI0 calibration delay circuit

Table 2-13 Pin descriptions – power supply pins (cont.)

Pad #	Pad name	Functional description
F14, F30, G37, T44, BB44	VDD_EBI0_PLL	Power for EBI0 PLL
L9, AM8, AR43, BC19, BF10	VDD_EBI1_CDC	Power for EBI1 calibration delay circuit
J9, AH8, AN43, BC11, BD14	VDD_EBI1_PLL	Power for EBI1 PLL
J25, J27, J29, J37, J39, J41, N25, N27, N29, N37, N39, N41, U25, U27, U29, U37, U39, U41, AC25, AC27, AC29, AC37, AC39, AC41	VDD_KRAIT	Power for quad Krait applications microprocessors
H34, L17, L19, L35, R17, R19, R31, R33, W11, W13, W19, W21, W31, AA31, AC15, AC17, AG35, AL19, AL21, AL27, AL29, AL37, AN15, AN37, AR21, AR35, AR37, AU17, AU37, AW13, AW21, BA13, BA35, BA37, BA39, BA41, BD28	VDD_MEM	Power for on-chip memory
AG37, AG39, AG41, AL39, AL41, AR31, AR33, AR39, AR41, AW31, AW33, AW35, AW37, AW39	VDD_MODEM	Power for modem circuits, including the two QDSP6s
B6, B16, B38, E1, G11, G27, G41, J49, K8, L3, P44, T2, U49, AG7, AH2, AJ49, AN47, AV44, BA1, BD10, BD48, BE15, BF40, BJ5, BJ17, BJ35, BJ45, BJ47, BK32	VDD_P1	Power for pad group 1 – EBI1 pads and DDR memory I/O pads
T46	VDD_P2	Power for pad group 2 – SDC2 pads
E19, G9, G23, G31, G39, G45, N5, P48, AH46, AK8, AY44, BC15, BC39, BG21	VDD_P3	Power for pad group 3 – most I/O pads
C15	VDD_P4	Power for pad group 4 – HSIC pads
AC47	VDD_P5	Power for pad group 5 – UIM1 pads
AF48	VDD_P6	Power for pad group 6 – UIM2 pads
AH48	VDD_P7	Power for pad group 7 – SDC1 pads
B4, B26, C37, E49, AD2, AE49, AV2, BG25, BH48, BK4	VDD_DDR_CORE_1P2	Power for PoP DDR memory core – 1.2 V for VDD2
D2, D50, AD50, BF2, BJ25	VDD_DDR_CORE_1P8	Power for PoP DDR memory core – 1.8 V for VDD1
AW7	VDD_EDP	Power for EDP circuits
AG17, AG19, AG21, AL15, AL17, AL23, AL25, AR15, AR17, AR19, AR23, AR25, AW15, AW17, AW19, AW23, AW25, BB18, BB20	VDD_GFX	Power for graphics
AK4	VDD_HDMI	Power for HDMI circuits
AB8	VDD_MIPI_CSI	Power for MIPI_CSI I/Os
BB4	VDD_MIPI_DSI_0P4	Reference for MIPI_DSI circuits
BF4	VDD_MIPI_DSI_1P2	Power for MIPI_DSI core circuits
BG3	VDD_MIPI_DSI_1P8	Power for MIPI_DSI I/Os
N23, AE35, AE43, AF46, AG15, AR29, AU29	VDD_PLL1	Power for PLL circuits – low voltage
G43, H20, J23, AA23, AC31, AE45, AH4, AT2, AW29, AY8, BD8	VDD_PLL2	Power for PLL circuits – high voltage
F36	VDD_QFPROM_PRG	Power for programming the QFPROM; otherwise, ground
U47, AP48	VDD_SDC_CDC	Power for SDC calibration delay circuits
F2, K4, P4	VDD_USB_1P8	Power for USB HS1, HS2, SS – low voltage
J1, R3	VDD_USB_3P3	Power for USB HS1, HS2 – high voltage
F6, J5, T4	VDD_USB_CORE	Power for USB digital core circuits – HS1, HS2, SS
E21	VDD_WLAN	Power for WLAN ADC circuits

Table 2-14 Pin descriptions – ground pins

Pad #	Pad name	Functional description
A1, A3, A5, A9, A13, A17, A21, A25, A29, A33, A37, A41, A45, A49, B2, B20, B50, C1, C13, F22, F38, F50, G1, G5, G13, G21, G33, H4, H8, H10, H22, H24, H26, H28, H30, H32, H36, H38, H40, H42, J11, J13, J15, J17, J19, J21, J31, J33, J35, J43, K42, K50, L1, L21, L23, L25, L27, L37, L41, M42, N9, N11, N13, N15, N17, N19, N21, N31, N33, N35, P42, P50, R1, R5, R9, R27, R29, R37, R39, R41, R43, T42, U9, U11, U13, U15, U17, U19, U21, U23, U31, U33, U35, U43, V42, V50, W1, W9, W25, W27, W29, Y8, Y42, AA9, AA11, AA13, AA15, AA17, AA19, AA21, AA25, AA27, AA33, AA35, AA37, AA41, AB50, AC1, AC9, AC23, AC33, AC35, AD44, AD46, AE9, AE11, AE13, AE15, AE17, AE19, AE21, AE23, AE25, AE29, AE31, AE33, AE37, AE39, AE41, AF42, AF44, AF50, AG1, AG9, AG43, AJ9, AJ11, AJ13, AJ15, AJ17, AJ19, AJ21, AJ23, AJ25, AJ27, AJ29, AJ31, AJ33, AJ35, AJ37, AJ39, AJ41, AK50, AL1, AL9, AM42, AN1, AN7, AN9, AN11, AN13, AN17, AN19, AN21, AN23, AN25, AN27, AN29, AN31, AN33, AN35, AN39, AN41, AP42, AP50, AR1, AR9, AR27, AT42, AU3, AU9, AU13, AU15, AU19, AU21, AU23, AU25, AU27, AU31, AU33, AU35, AU39, AU41, AU43, AV4, AV8, AV50, AW1, AW9, AW27, AW45, AY2, AY42, BA9, BA11, BA15, BA17, BA19, BA21, BA23, BA25, BA27, BA29, BA31, BB8, BB10, BB12, BB14, BB16, BB24, BB26, BB28, BB30, BB32, BB34, BB36, BB38, BB40, BB42, BB50, BC13, BC25, BC27, BD4, BD12, BD24, BD42, BE1, BE7, BE29, BE37, BE41, BF30, BF42, BF48, BF50, BG1, BH34, BJ1, BJ3, BJ21, BJ33, BJ41, BJ49, BK2, BK8, BK12, BK16, BK20, BK24, BK28, BK36, BK40, BK44, BK48, BK50	GND	Ground

2.3 Pin assignments – MSM top

2.3.1 Pin map – MSM top

The MSM8x74 is available in the 990 PNSP package. Its top surface is implemented like a 216-pin chip-scale package (216 CSP). See Chapter 4 for package details, and Section 2.2 for information about the bottom pin assignments. A high-level view of the top pin assignments is shown in Figure 2-6. The pins are colored to indicate which function-type they support, as defined in Figure 2-5.

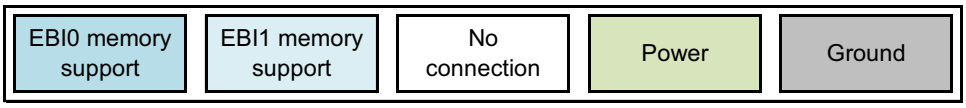
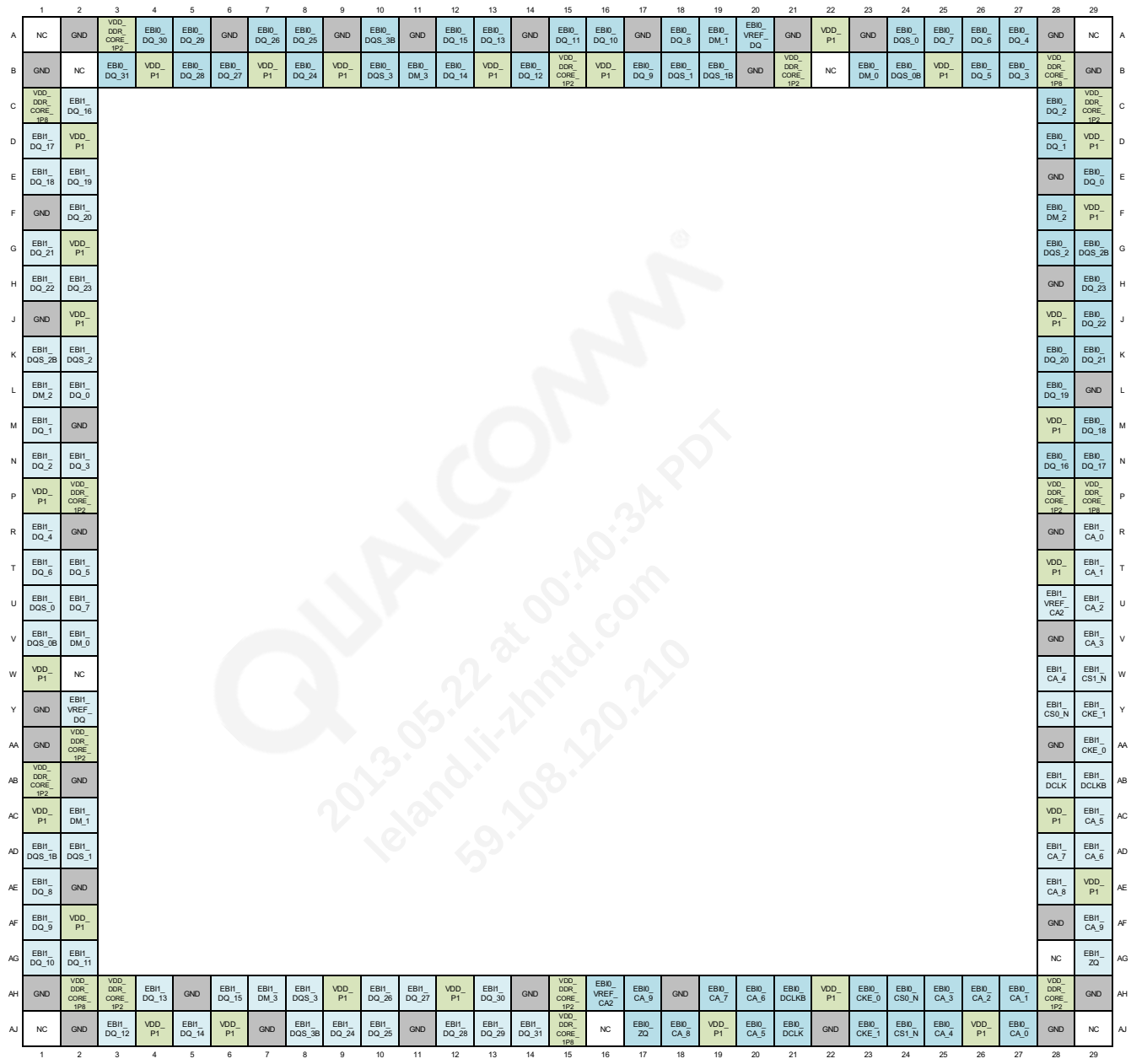


Figure 2-5 MSM8x74 top pin assignments – legend

The text within Figure 2-6 is difficult to read when viewing an 8½” × 11” hard copy. Other viewing options are available and defined in Section 2.2.1.



	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19	20	21	22	23	24	25	26	27	28	29	
A	NC	GND	VDD_DDR_CORE_1P2	EBI0_DQ_30	EBI0_DQ_29	GND	EBI0_DQ_26	EBI0_DQ_25	GND	EBI0_DQS_3B	GND	EBI0_DQ_15	EBI0_DQ_13	GND	EBI0_DQ_11	EBI0_DQ_10	GND	EBI0_DQ_8	EBI0_DM_1	EBI0_VREF_DQ	GND	VDD_P1	GND	EBI0_DQS_0	EBI0_DQ_7	EBI0_DQ_6	EBI0_DQ_4	GND	NC	A
B	GND	NC	EBI0_DQ_31	VDD_P1	EBI0_DQ_28	EBI0_DQ_27	VDD_P1	EBI0_DQ_24	VDD_P1	EBI0_DQS_3	EBI0_DM_3	EBI0_DQ_14	VDD_P1	EBI0_DQ_12	VDD_DDR_CORE_1P2	VDD_P1	EBI0_DQ_9	EBI0_DQS_1	EBI0_DQS_1B	GND	VDD_DDR_CORE_1P2	NC	EBI0_DM_0	EBI0_DQS_0B	VDD_P1	EBI0_DQ_5	EBI0_DQ_3	VDD_DDR_CORE_1P8	GND	B
C	VDD_DDR_CORE_1P8	EBI1_DQ_16																										EBI0_DQ_2	VDD_DDR_CORE_1P2	C
D	EBI1_DQ_17	VDD_P1																										EBI0_DQ_1	VDD_P1	D
E	EBI1_DQ_18	EBI1_DQ_19																										GND	EBI0_DQ_0	E
F	GND	EBI1_DQ_20																										EBI0_DM_2	VDD_P1	F
G	EBI1_DQ_21	VDD_P1																										EBI0_DQS_2	EBI0_DQS_2B	G
H	EBI1_DQ_22	EBI1_DQ_23																										GND	EBI0_DQ_23	H
J	GND	VDD_P1																										VDD_P1	EBI0_DQ_22	J
K	EBI1_DQS_2B	EBI1_DQS_2																										EBI0_DQ_20	EBI0_DQ_21	K
L	EBI1_DM_2	EBI1_DQ_0																										EBI0_DQ_19	GND	L
M	EBI1_DQ_1	GND																										VDD_P1	EBI0_DQ_18	M
N	EBI1_DQ_2	EBI1_DQ_3																										EBI0_DQ_16	EBI0_DQ_17	N
P	VDD_P1	VDD_DDR_CORE_1P2																										VDD_DDR_CORE_1P2	VDD_DDR_CORE_1P8	P
R	EBI1_DQ_4	GND																										GND	EBI1_CA_0	R
T	EBI1_DQ_6	EBI1_DQ_5																										VDD_P1	EBI1_CA_1	T
U	EBI1_DQS_0	EBI1_DQ_7																										EBI1_VREF_CA2	EBI1_CA_2	U
V	EBI1_DQS_0B	EBI1_DM_0																										GND	EBI1_CA_3	V
W	VDD_P1	NC																										EBI1_CA_4	EBI1_CS1_N	W
Y	GND	EBI1_VREF_DQ																										EBI1_CS0_N	EBI1_CKE_1	Y
AA	GND	VDD_DDR_CORE_1P2																										GND	EBI1_CKE_0	AA
AB	VDD_DDR_CORE_1P2	GND																										EBI1_DCLK	EBI1_DCLKB	AB
AC	VDD_P1	EBI1_DM_1																										VDD_P1	EBI1_CA_5	AC
AD	EBI1_DQS_1B	EBI1_DQS_1																										EBI1_CA_7	EBI1_CA_6	AD
AE	EBI1_DQ_8	GND																										EBI1_CA_8	VDD_P1	AE
AF	EBI1_DQ_9	VDD_P1																										GND	EBI1_CA_9	AF
AG	EBI1_DQ_10	EBI1_DQ_11																										NC	EBI1_ZQ	AG
AH	GND	VDD_DDR_CORE_1P8	VDD_DDR_CORE_1P2	EBI1_DQ_13	GND	EBI1_DQ_15	EBI1_DM_3	EBI1_DQS_3	VDD_P1	EBI1_DQ_26	EBI1_DQ_27	VDD_P1	EBI1_DQ_30	GND	VDD_DDR_CORE_1P2	EBI0_VREF_CA2	EBI0_CA_9	GND	EBI0_CA_7	EBI0_CA_6	EBI0_DCLKB	VDD_P1	EBI0_CKE_0	EBI0_CS0_N	EBI0_CA_3	EBI0_CA_2	EBI0_CA_1	VDD_DDR_CORE_1P2	GND	AH
AJ	NC	GND	EBI1_DQ_12	VDD_P1	EBI1_DQ_14	VDD_P1	GND	EBI1_DQS_3B	EBI1_DQ_24	EBI1_DQ_25	GND	EBI1_DQ_28	EBI1_DQ_29	EBI1_DQ_31	VDD_DDR_CORE_1P8	NC	EBI0_ZQ	EBI0_CA_8	VDD_P1	EBI0_CA_5	EBI0_DCLK	GND	EBI0_CKE_1	EBI0_CS1_N	EBI0_CA_4	VDD_P1	EBI0_CA_0	GND	NC	AJ
	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19	20	21	22	23	24	25	26	27	28	29	

Figure 2-6 High-level view of MSM8x74 top pin assignments

2.3.2 Pin descriptions – MSM top

Descriptions of top pins are presented in the following tables, organized by functional group:

Table 2-15: Memory support functions

Table 2-16: No connection, do not connect, and reserved pins

Table 2-17: Power-supply pins

Table 2-18: Ground pins

Table 2-15 Pin descriptions – memory support functions

Pad #	Pad name and/or function	Pad name or alt function	Pad characteristics [1]		Functional description
			Voltage	Type	
EBI0					
AH17	EBI0_CA_9		P1	DO	EBI0 LPDDR3 command / address bit 9
AJ18	EBI0_CA_8		P1	DO	EBI0 LPDDR3 command / address bit 8
AH19	EBI0_CA_7		P1	DO	EBI0 LPDDR3 command / address bit 7
AH20	EBI0_CA_6		P1	DO	EBI0 LPDDR3 command / address bit 6
AJ20	EBI0_CA_5		P1	DO	EBI0 LPDDR3 command / address bit 5
AJ25	EBI0_CA_4		P1	DO	EBI0 LPDDR3 command / address bit 4
AH25	EBI0_CA_3		P1	DO	EBI0 LPDDR3 command / address bit 3
AH26	EBI0_CA_2		P1	DO	EBI0 LPDDR3 command / address bit 2
AH27	EBI0_CA_1		P1	DO	EBI0 LPDDR3 command / address bit 1
AJ27	EBI0_CA_0		P1	DO	EBI0 LPDDR3 command / address bit 0
B3	EBI0_DQ_31		P1	B	EBI0 LPDDR3 data bit 31
A4	EBI0_DQ_30		P1	B	EBI0 LPDDR3 data bit 30
A5	EBI0_DQ_29		P1	B	EBI0 LPDDR3 data bit 29
B5	EBI0_DQ_28		P1	B	EBI0 LPDDR3 data bit 28
B6	EBI0_DQ_27		P1	B	EBI0 LPDDR3 data bit 27
A7	EBI0_DQ_26		P1	B	EBI0 LPDDR3 data bit 26
A8	EBI0_DQ_25		P1	B	EBI0 LPDDR3 data bit 25
B8	EBI0_DQ_24		P1	B	EBI0 LPDDR3 data bit 24
H29	EBI0_DQ_23		P1	B	EBI0 LPDDR3 data bit 23
J29	EBI0_DQ_22		P1	B	EBI0 LPDDR3 data bit 22
K29	EBI0_DQ_21		P1	B	EBI0 LPDDR3 data bit 21
K28	EBI0_DQ_20		P1	B	EBI0 LPDDR3 data bit 20
L28	EBI0_DQ_19		P1	B	EBI0 LPDDR3 data bit 19
M29	EBI0_DQ_18		P1	B	EBI0 LPDDR3 data bit 18
N29	EBI0_DQ_17		P1	B	EBI0 LPDDR3 data bit 17
N28	EBI0_DQ_16		P1	B	EBI0 LPDDR3 data bit 16
A12	EBI0_DQ_15		P1	B	EBI0 LPDDR3 data bit 15
B12	EBI0_DQ_14		P1	B	EBI0 LPDDR3 data bit 14
A13	EBI0_DQ_13		P1	B	EBI0 LPDDR3 data bit 13

Table 2-15 Pin descriptions – memory support functions (cont.)

Pad #	Pad name and/or function	Pad name or alt function	Pad characteristics [1]		Functional description
			Voltage	Type	
B14	EBI0_DQ_12		P1	B	EBI0 LPDDR3 data bit 12
A15	EBI0_DQ_11		P1	B	EBI0 LPDDR3 data bit 11
A16	EBI0_DQ_10		P1	B	EBI0 LPDDR3 data bit 10
B17	EBI0_DQ_9		P1	B	EBI0 LPDDR3 data bit 9
A18	EBI0_DQ_8		P1	B	EBI0 LPDDR3 data bit 8
A25	EBI0_DQ_7		P1	B	EBI0 LPDDR3 data bit 7
A26	EBI0_DQ_6		P1	B	EBI0 LPDDR3 data bit 6
B26	EBI0_DQ_5		P1	B	EBI0 LPDDR3 data bit 5
A27	EBI0_DQ_4		P1	B	EBI0 LPDDR3 data bit 4
B27	EBI0_DQ_3		P1	B	EBI0 LPDDR3 data bit 3
C28	EBI0_DQ_2		P1	B	EBI0 LPDDR3 data bit 2
D28	EBI0_DQ_1		P1	B	EBI0 LPDDR3 data bit 1
F29	EBI0_DQ_0		P1	B	EBI0 LPDDR3 data bit 0
AJ21	EBI0_DCLK		P1	DO	EBI0 LPDDR3 differential clock (+)
AH21	EBI0_DCLKB		P1	DO	EBI0 LPDDR3 differential clock (-)
AJ23	EBI0_CKE_1		P1	DO	EBI0 LPDDR3 clock enable 1
AH23	EBI0_CKE_0		P1	DO	EBI0 LPDDR3 clock enable 0
AJ24	EBI0_CS1_N		P1	DO	EBI0 LPDDR3 chip select 1
AH24	EBI0_CS0_N		P1	DO	EBI0 LPDDR3 chip select 0
B10	EBI0_DQS_3		P1	B	EBI0 LPDDR3 differential data strobe for byte 3 (+)
A10	EBI0_DQS_3B		P1	B	EBI0 LPDDR3 differential data strobe for byte 3 (-)
G28	EBI0_DQS_2		P1	B	EBI0 LPDDR3 differential data strobe for byte 2 (+)
G29	EBI0_DQS_2B		P1	B	EBI0 LPDDR3 differential data strobe for byte 2 (-)
B18	EBI0_DQS_1		P1	B	EBI0 LPDDR3 differential data strobe for byte 1 (+)
B19	EBI0_DQS_1B		P1	B	EBI0 LPDDR3 differential data strobe for byte 1 (-)
A24	EBI0_DQS_0		P1	B	EBI0 LPDDR3 differential data strobe for byte 0 (+)
B24	EBI0_DQS_0B		P1	B	EBI0 LPDDR3 differential data strobe for byte 0 (-)
B11	EBI0_DM_3		P1	DO	EBI0 LPDDR3 data mask for byte 3
F28	EBI0_DM_2		P1	DO	EBI0 LPDDR3 data mask for byte 2
A19	EBI0_DM_1		P1	DO	EBI0 LPDDR3 data mask for byte 1
B23	EBI0_DM_0		P1	DO	EBI0 LPDDR3 data mask for byte 0
AJ17	EBI0_ZQ		–	AI	EBI0 LPDDR3 calibration pad
AH16	EBI0_VREF_CA2		–	AI	EBI0 LPDDR3 CA reference voltage (top)
A20	EBI0_VREF_DQ		–	AI	EBI0 LPDDR3 DQ reference voltage

Table 2-15 Pin descriptions – memory support functions (cont.)

Pad #	Pad name and/or function	Pad name or alt function	Pad characteristics [1]		Functional description
			Voltage	Type	
EBI1					
AF29	EBI1_CA_9		P1	DO	EBI1 LPDDR3 command / address bit 9
AE28	EBI1_CA_8		P1	DO	EBI1 LPDDR3 command / address bit 8
AD28	EBI1_CA_7		P1	DO	EBI1 LPDDR3 command / address bit 7
AD29	EBI1_CA_6		P1	DO	EBI1 LPDDR3 command / address bit 6
AC29	EBI1_CA_5		P1	DO	EBI1 LPDDR3 command / address bit 5
W28	EBI1_CA_4		P1	DO	EBI1 LPDDR3 command / address bit 4
V20	EBI1_CA_3		P1	DO	EBI1 LPDDR3 command / address bit 3
U29	EBI1_CA_2		P1	DO	EBI1 LPDDR3 command / address bit 2
T29	EBI1_CA_1		P1	DO	EBI1 LPDDR3 command / address bit 1
R29	EBI1_CA_0		P1	DO	EBI1 LPDDR3 command / address bit 0
AJ14	EBI1_DQ_31		P1	B	EBI1 LPDDR3 data bit 31
AH13	EBI1_DQ_30		P1	B	EBI1 LPDDR3 data bit 30
AJ13	EBI1_DQ_29		P1	B	EBI1 LPDDR3 data bit 29
AJ12	EBI1_DQ_28		P1	B	EBI1 LPDDR3 data bit 28
AH11	EBI1_DQ_27		P1	B	EBI1 LPDDR3 data bit 27
AH10	EBI1_DQ_26		P1	B	EBI1 LPDDR3 data bit 26
AJ10	EBI1_DQ_25		P1	B	EBI1 LPDDR3 data bit 25
AJ9	EBI1_DQ_24		P1	B	EBI1 LPDDR3 data bit 24
H2	EBI1_DQ_23		P1	B	EBI1 LPDDR3 data bit 23
H1	EBI1_DQ_22		P1	B	EBI1 LPDDR3 data bit 22
G1	EBI1_DQ_21		P1	B	EBI1 LPDDR3 data bit 21
F2	EBI1_DQ_20		P1	B	EBI1 LPDDR3 data bit 20
E2	EBI1_DQ_19		P1	B	EBI1 LPDDR3 data bit 19
E1	EBI1_DQ_18		P1	B	EBI1 LPDDR3 data bit 18
D1	EBI1_DQ_17		P1	B	EBI1 LPDDR3 data bit 17
C2	EBI1_DQ_16		P1	B	EBI1 LPDDR3 data bit 16
AH6	EBI1_DQ_15		P1	B	EBI1 LPDDR3 data bit 15
AJ5	EBI1_DQ_14		P1	B	EBI1 LPDDR3 data bit 14
AH4	EBI1_DQ_13		P1	B	EBI1 LPDDR3 data bit 13
AJ3	EBI1_DQ_12		P1	B	EBI1 LPDDR3 data bit 12
AG2	EBI1_DQ_11		P1	B	EBI1 LPDDR3 data bit 11
AG1	EBI1_DQ_10		P1	B	EBI1 LPDDR3 data bit 10
AF1	EBI1_DQ_9		P1	B	EBI1 LPDDR3 data bit 9
AE1	EBI1_DQ_8		P1	B	EBI1 LPDDR3 data bit 8
U2	EBI1_DQ_7		P1	B	EBI1 LPDDR3 data bit 7
T1	EBI1_DQ_6		P1	B	EBI1 LPDDR3 data bit 6
T2	EBI1_DQ_5		P1	B	EBI1 LPDDR3 data bit 5
R1	EBI1_DQ_4		P1	B	EBI1 LPDDR3 data bit 4

Table 2-15 Pin descriptions – memory support functions (cont.)

Pad #	Pad name and/or function	Pad name or alt function	Pad characteristics [1]		Functional description
			Voltage	Type	
N2	EBI1_DQ_3		P1	B	EBI1 LPDDR3 data bit 3
N1	EBI1_DQ_2		P1	B	EBI1 LPDDR3 data bit 2
M1	EBI1_DQ_1		P1	B	EBI1 LPDDR3 data bit 1
L2	EBI1_DQ_0		P1	B	EBI1 LPDDR3 data bit 0
AB28	EBI1_DCLK		P1	DO	EBI1 LPDDR3 differential clock (+)
AB29	EBI1_DCLKB		P1	DO	EBI1 LPDDR3 differential clock (-)
Y29	EBI1_CKE_1		P1	DO	EBI1 LPDDR3 clock enable 1
AA29	EBI1_CKE_0		P1	DO	EBI1 LPDDR3 clock enable 0
W29	EBI1_CS1_N		P1	DO	EBI1 LPDDR3 chip select 1
Y28	EBI1_CS0_N		P1	DO	EBI1 LPDDR3 chip select 0
AH8	EBI1_DQS_3		P1	B	EBI1 LPDDR3 differential data strobe for byte 3 (+)
AJ8	EBI1_DQS_3B		P1	B	EBI1 LPDDR3 differential data strobe for byte 3 (-)
K2	EBI1_DQS_2		P1	B	EBI1 LPDDR3 differential data strobe for byte 2 (+)
K1	EBI1_DQS_2B		P1	B	EBI1 LPDDR3 differential data strobe for byte 2 (-)
AD2	EBI1_DQS_1		P1	B	EBI1 LPDDR3 differential data strobe for byte 1 (+)
AD1	EBI1_DQS_1B		P1	B	EBI1 LPDDR3 differential data strobe for byte 1 (-)
U1	EBI1_DQS_0		P1	B	EBI1 LPDDR3 differential data strobe for byte 0 (+)
V1	EBI1_DQS_0B		P1	B	EBI1 LPDDR3 differential data strobe for byte 0 (-)
AH7	EBI1_DM_3		P1	DO	EBI1 LPDDR3 data mask for byte 3
L1	EBI1_DM_2		P1	DO	EBI1 LPDDR3 data mask for byte 2
AC2	EBI1_DM_1		P1	DO	EBI1 LPDDR3 data mask for byte 1
V2	EBI1_DM_0		P1	DO	EBI1 LPDDR3 data mask for byte 0
AG29	EBI1_ZQ		–	AI	EBI1 LPDDR3 calibration pad
U28	EBI1_VREF_CA2		–	AI	EBI1 LPDDR3 CA reference voltage (top)
Y2	EBI1_VREF_DQ		–	AI	EBI1 LPDDR3 DQ reference voltage

1. Refer to Table 2-1 for parameter and acronym definitions.

Table 2-16 Pin descriptions – no connection, do not connect, and reserved pins

Pad #	Pad name	Functional description
A1, A29, B2, B22, W2, AG28, AJ1, AJ16, AJ29	NC	No connect; not connected internally.

Table 2-17 Pin descriptions – power supply pins

Pad #	Pad name	Functional description
A3, B15, B21, C29, P2, P28, AA2, AB1, AH3, AH15, AH28	VDD_DDR_CORE_1P2	Power for PoP DDR memory core (1.2 V for VDD2)
B28, C1, P29, AH2, AJ15	VDD_DDR_CORE_1P8	Power for PoP DDR memory core (1.8 V for VDD1)
A22, B4, B7, B9, B13, B16, B25, D2, D29, F29, G2, J2, J28, M28, P1, T28, W1, AC1, AC28, AE26, AF2, AH9, AH12, AH22, AJ4, AJ6, AJ19, AJ26	VDD_P1	Power for pad group 1 – EBI pads and DDR memory I/O pads

Table 2-18 Pin descriptions – ground pins

Pad #	Pad name	Functional description
A2, A6, A9, A11, A14, A17, A21, A23, A28, B1, B20, B29, E28, F1, H28, J1, L29, M2, R2, R28, V28, Y1, AA1, AA28, AB2, AE2, AF28, AH1, AH5, AH14, AH18, AH29, AJ2, AJ7, AJ11, AJ22, AJ28	GND	Ground

3 Electrical Specifications

NOTE Electrical specifications in this chapter are preliminary and subject to change without prior notice.

3.1 Absolute maximum ratings

Absolute maximum ratings (Table 3-1) reflect conditions that MSM8x74 devices may be exposed to outside of the operating limits, without experiencing immediate functional failure. They are limiting values to be considered individually when all other parameters are within their specified operating ranges. Functionality and long-term reliability can only be expected within the recommended operating conditions, as described in Section 3.2.

Table 3-1 Absolute maximum ratings

Parameter		Min	Max	Unit
Power supply voltages				
VDD_Ax	Analog circuits	–	1.5 x TYP [1]	V
VDD_CORE	Digital core circuits	–	1.65	V
VDD_DDR_CORE_x	PoP DDR memory	–	1.5 x TYP [1]	V
VDD_HDMI	HDMI circuits	–	TBD	V
VDD_KRAIT	Krait application microprocessors	–	1.80	V
VDD_MEM	On-chip memory	–	1.80	V
VDD_MIPI	MIPI circuits and I/Os (CSI and DSI)	–	TBD	V
VDD_Px	Digital pad circuits	–	1.5 x TYP [1]	V
VDD_PLLx	PLL circuits	–	TBD	V
VDD_QFPROM_PRG	QFPROM programming voltage	–	3.24	V
VDD_USBPHY_1P8	USB PHY low-voltage circuit	–	1.98	V
VDD_USBPHY_3P3	USB PHY high-voltage circuit	–	4.95	V
Signal pins				
VIN	Voltage on any nonpower input or output pin [2]	–	V_{XX} + 0.5	V
IIN	Latch-up current	-100	100	mA
ESD protection – see Section 7.1.				
Thermal conditions – see Section 4.5.				

1. The entry ‘TYP’ in this column refers to the corresponding typical supply voltage as defined within Table 3-2.
2. V_{XX} is the supply voltage associated with the input or output pin to which the test voltage is applied.

3.2 Recommended operating conditions

Operating conditions include parameters that are under the control of the design team: power supply voltage, power distribution impedances, and thermal conditions (Table 3-2). The MSM8x74 meets all performance specifications listed in Section 3.6 through Section 3.12, when used within the recommended operating conditions, unless otherwise noted in those sections (provided the absolute maximum ratings have never been exceeded).

NOTE The PVS fuse location bits in Table 3-2 for VDD_KRAIT refer to the register , SECURITY_CONTROL_CORE_QFPROM_CORR_PTE_LSB (0xFC4BC0B0). For more information, refer to *MSM8974 Software Interface* (80-NA437-2).

Table 3-2 Recommended operating conditions

Parameter		Min	Typ [1]	Max	Unit
Power supply voltages					
VDD_A1	Low-voltage analog circuits	1.15	1.225	1.30	V
VDD_A2	High-voltage analog circuits	1.72	1.80	1.90	V
VDD_CORE (Super turbo)	Digital baseband core circuits	0.96	1.05	1.13	V
VDD_CORE (Turbo)	Digital baseband core circuits	0.90	0.99	1.07	V
VDD_CORE (Nominal)	Digital baseband core circuits	0.82	0.90	1.00	V
VDD_CORE (SVS)	Digital baseband core circuits	0.74	0.815	0.90	V
VDD_DDR_CORE_1P8	High-voltage PoP DDR memory	1.70	1.80	1.90	V
VDD_DDR_CORE_1P2	Low-voltage PoP DDR memory	1.16	1.225	1.25	V
VDD_EBIx_CDC (Super turbo)	EBI1 calibration delay circuit	0.96	1.05	1.14	V
VDD_EBIx_CDC (Turbo)	EBI1 calibration delay circuit	0.96	1.05	1.14	V
VDD_EBIx_CDC (Nominal)	EBI1 calibration delay circuit	0.88	0.95	1.04	V
VDD_EBIx_CDC (SVS)	EBI1 calibration delay circuit	0.88	0.95	1.04	V

Table 3-2 Recommended operating conditions (cont.)

Parameter		Min	Typ [1]	Max	Unit
VDD_EBIx_PLL (Super turbo)	EBI1 PLL circuit	0.96	1.05	1.14	V
VDD_EBIx_PLL (Turbo)	EBI1 PLL circuit	0.96	1.05	1.14	V
VDD_EBIx_PLL (Nominal)	EBI1 PLL circuit	0.88	0.95	1.04	V
VDD_EBIx_PLL (SVS)	EBI1 PLL circuit	0.88	0.95	1.04	V
VDD_EDP	EDP circuits	1.70	1.80	1.90	V
VDD_GFX (Super turbo)	Graphics circuits	0.96	1.05	1.15	V
VDD_GFX (Turbo)	Graphics circuits	0.90	0.99	1.10	V
VDD_GFX (Nominal)	Graphics circuits	0.82	0.90	1.01	V
VDD_GFX (SVS)	Graphics circuits	0.74	0.815	0.92	V
VDD_HDMI	HDMI circuits	1.70	1.80	1.90	V
VDD_KRAIT	For Kraits operating at a maximum frequency of 2.2 GHz:				
	PVS fuse bits [8:6] = 3'b110	0.870	0.950	1.03	V
	PVS fuse bits [8:6] = 3'b101	0.895	0.975	1.055	V
	PVS fuse bits [8:6] = 3'b100	0.92	1.000	1.08	V
	PVS fuse bits [8:6] = 3'b011	0.945	1.025	1.105	V
	PVS fuse bits [8:6] = 3'b010	0.97	1.050	1.13	V
	PVS fuse bits [8:6] = 3'b001	0.995	1.075	TBD	V
	PVS fuse bits [8:6] = 3'b000	1.02	1.100	TBD	V
VDD_MEM (Super turbo)	On-chip memory	0.96	1.05	1.14	V
VDD_MEM (Turbo)	On-chip memory	0.96	1.05	1.14	V
VDD_MEM (Nominal)	On-chip memory	0.88	0.95	1.04	V
VDD_MEM (SVS)	On-chip memory	0.88	0.95	1.04	V
VDD_MIPI_CSI	MIPI CSI circuits and I/Os	1.70	1.80	1.90	V
VDD_MIPI_DSI_0P4	Reference for MIPI DSI circuits	TBD	0.40	TBD	V
VDD_MIPI_DSI_1P2	MIPI DSI core circuits	1.16	1.20	1.24	V
VDD_MIPI_DSI_1P8	MIPI DSI I/Os	1.70	1.80	1.90	V

Table 3-2 Recommended operating conditions (cont.)

Parameter		Min	Typ [1]	Max	Unit
VDD_MODEM (Super turbo)	Modem and QDSP6 circuits	0.96	1.05	1.14	V
VDD_MODEM (Turbo)	Modem and QDSP6 circuits	0.90	0.99	1.08	V
VDD_MODEM (Nominal)	Modem and QDSP6 circuits	0.82	0.90	1.00	V
VDD_MODEM (SVS)	Modem and QDSP6 circuits	0.74	0.815	0.91	V
VDD_P1	Digital pad circuits – EBI0/EBI1	1.16	1.225	1.25	V
VDD_P2	Digital pad circuits – SDC2				
	Low voltage	1.70	1.80	1.90	V
	High voltage	2.75	2.95	3.04	V
VDD_P3	Digital pad circuits – most I/Os	1.70	1.80	1.90	V
VDD_P4	Digital pad circuits – HSIC/GPIO				
	Used as HSIC	1.16	1.225	1.25	V
	Used as GPIO	1.70	1.80	1.90	V
VDD_P5	Digital pad circuits – UIM1 dual-voltage				
	Low voltage	1.70	1.80	1.90	V
	High voltage	2.75	2.95	3.04	V
VDD_P6	Digital pad circuits – UIM2 dual-voltage				
	Low voltage	1.70	1.80	1.90	V
	High voltage	2.75	2.95	3.04	V
VDD_P7	Digital pad circuits – SDC1				
	Low voltage	1.16	1.225	1.25	V
	High voltage	1.70	1.80	1.90	V
VDD_PLL1 (Super turbo)	Low-voltage PLL circuits	0.96	1.05	1.13	V
VDD_PLL1 (Turbo)	Low-voltage PLL circuits	0.90	0.99	1.07	V
VDD_PLL1 (Nominal)	Low-voltage PLL circuits	0.82	0.90	1.00	V
VDD_PLL1 (SVS)	Low-voltage PLL circuits	0.74	0.815	0.90	V
VDD_PLL2	High-voltage PLL circuits	1.70	1.80	1.90	V
VDD_QFPROM_PRG	QFPROM voltage				
	Programming	1.70	1.90	1.94	V
	Non-programming	1.70	1.80	1.90	V

Table 3-2 Recommended operating conditions (cont.)

Parameter		Min	Typ [1]	Max	Unit
VDD_SDC_CDC (Super turbo)	SDC calibration delay circuits	0.96	1.05	1.13	V
VDD_SDC_CDC (Turbo)	SDC calibration delay circuits	0.90	0.99	1.07	V
VDD_SDC_CDC (Nominal)	SDC calibration delay circuits	0.82	0.90	1.00	V
VDD_SDC_CDC (SVS)	SDC calibration delay circuits	0.74	0.815	0.90	V
VDD_USB_CORE (Super turbo)	USB PHY core circuits	0.96	1.05	1.13	V
VDD_USB_CORE (Turbo)	USB PHY core circuits	0.90	0.99	1.07	V
VDD_USB_CORE (Nominal)	USB PHY core circuits	0.82	0.90	1.00	V
VDD_USB_CORE (SVS)	USB PHY core circuits	0.74	0.815	0.90	V
VDD_USB_1P8	Low-voltage USB PHY circuits	1.70	1.80	1.90	V
VDD_USB_3P3	High-voltage USB PHY circuits [2]	2.97	3.075	3.63	V
VDD_WLAN	WLAN ADC circuits	1.22	1.30	1.34	V
Thermal conditions					
T_C	Device operating temperature (case)	-30	+25	+85	°C
	Fuse programming temperature (case)	+10	+25	+85	°C
T_A [3]	3GPP2-mode operating temperature (ambient)	-30	+25	+60	°C
	3GPP-mode operating temperature (ambient)	-20	+25	+60	°C

1. Typical voltages represent the recommended output settings of the companion PMIC device.
2. The PMIC sets VDD_USB_3P3 to 3.075 V by default due to power considerations. The product designs must ensure that at least 3.0 V is delivered to the VDD_USB_3P3 pin to meet USB PHY design requirements.
3. These temperature ranges are defined by the 3GPP and 3GPP2 system specifications.

NOTE A programmable voltage regulator (such as a companion Qualcomm PMIC) should be used as the VDD_CORE supply. This provides the best flexibility for using the same PCB design for future pin-compatible MSM devices that might require lower VDD_CORE voltages.

3.3 Power distribution network

The impedances of the distribution networks that deliver power to the MSM are critical to its supply voltages, not just at DC but over a wide range of frequencies. An inadequate PDN could cause the min/max values listed in Table 3-2 to be violated. The recommended performance of the PDN for key MSM supplies is listed in Table 3-3.

Table 3-3 Power distribution network impedance vs. frequency

Power domain	Max impedance	Max impedance
	DC to 10 Hz	10 Hz to 25 MHz
VDD_CORE	10 mΩ	See Table 3-4 for specification.
VDD_GFX	10 mΩ	56 mΩ
VDD_KRAIT	2 mΩ	17 mΩ
VDD_MEM	10 mΩ	18 mΩ
VDD_MODEM	10 mΩ	57 mΩ
VDD_DDR_CORE_1P2/VDD_P1/ VDD_P4	11 mΩ	14 mΩ

NOTE Design guidelines for the PDN are given in the *Training: Power Delivery Network Design* document (80-VT310-13). If PCB designers have difficulty meeting these impedances, please contact Qualcomm for assistance.

NOTE The power distribution network specification for VDD_DDR_CORE_1P2/ VDD_P1/VDD_P4 applies only for the MSM domain powered by VREG_L1_1P2.

Table 3-4 VDD_CORE PDN AC Specification

Port number	Pin number of positive ports (VDD_CORE pins)	Pin number of negative ports (GND pins)	Max impedance
			10 Hz to 25 MHz
1	AU11, AW11	AR9, AU9, AU13, AW9, BA9, BA11	55 mΩ
2	AL11, AL13	AJ9, AJ11, AJ13, AJ15, AL9, AN9, AN11, AN13	55 mΩ
3	AG11, AG13	AE9, AE11, AE13, AG9, AJ9, AJ11, AJ13, AJ15	55 mΩ
4	AC11, AC13	AA9, AA11, AA13, AA15, AC9, AE9, AE11, AE13, AE15	55 mΩ
5	H12, H16, H18, L11, L13, L15, R11, R13, R15, W15, W17	G13, H10, J11, J13, J15, J17, J19, N9, N11, N13, N15, N17, N19, R9, U9, U11, U13, U15, U17, U19, W9, AA9, AA11, AA13, AA15, AA17, AA19	55 mΩ
6	R21, R23, R25	N19, N21, R27, U19, U21, U23	55 mΩ
7	W23	U21, U23, W25, AA21, AA25	55 mΩ

Table 3-4 VDD_CORE PDN AC Specification

Port number	Pin number of positive ports (VDD_CORE pins)	Pin number of negative ports (GND pins)	Max impedance
			10 Hz to 25 MHz
8	AC19, AC21	AA17, AA19, AA21, AC23, AE17, AE19, AE21, AE23	55 mΩ
9	W33, W35	U31, U33, U35, AA33, AA35, AA37	55 mΩ
10	AG23, AG25, AG27, AG29, AG31, AG33, AE27, AL31, AL33, AL35	AC23, AC33, AC35, AE23, AE25, AE29, AE31, AE33, AJ23, AJ25, AJ27, AJ29, AJ31, AJ33, AJ35, AN23, AN25, AN27, AN29, AN31, AN33, AN35	55 mΩ
11	BC21	BA19, BA21, BA23	80 mΩ
12	BD36	BB34, BB36, BE37, BB38	80 mΩ
13	BC41	BB40, BB42, BD42	80 mΩ
14	AV42	AU41, AU43, AT42	80 mΩ
15	AH44	AF44, AG43, AJ41	80 mΩ
16	AB44	Y42, AA41, AD44	80 mΩ
17	W39,W41	V42, Y42	80 mΩ
18	R35	N35, R37, U35	80 mΩ
19	L31, L33	J31, J33, N31, N33	80 mΩ
20	K44	J43, K42, M42	80 mΩ

NOTE For additional details on VDD_CORE PDN AC specification, refer to *MSM8974 PDN Specification Updates Application Note* (80-NA437-17).

3.4 DC power characteristics

Detailed current consumption information and details about the operating modes tested are available in *AMSS 8974 Current Consumption Data for Linux Android* (80-NA437-7).

3.5 Power sequencing

The PMIC includes poweron circuits that provide the proper power sequencing for the entire MSM8x74 chipset. The supplies are turned on as groups of regulators that are selected by the hardware configuration of some PMIC pins. There will be a HW default sequence that can be used, however the Programmable Boot Sequence (PBS) module of the PMIC allows for programming of any other sequence required. Refer to the appropriate PMIC device specification for details, such as the *PM8941 Power Management IC Device Specification* (80-NA555-1) or the *PM8841 Power Management IC Device Specification* (80-NA554-1).

A high-level summary of the required default poweron sequence:

1. VDD_MEM (on-chip memory)
2. VDD_CORE (digital core circuits)
3. VREF_SDC (SDC reference voltage)
4. VDD_P3 (I/Os), VDD_P7 (SDC1), VDD_DDR_CORE_1P8 (DDR core 1.8 V)
5. VDD_USB_1P8 (USB 1.8 V circuits)
6. VDD_P1 (EBI and DDR I/Os), VDD_P4 (HSIC), VDD_DDR_CORE_1P2 (DDR core 1.2 V)
7. EBIx_VREF_CA2, EBIx_VREF_DQ (EBI0/1 CA and DQ LPDDR3 reference voltage)
8. VDD_USB_3P3 (USB 3.3 V circuits)
9. VDD_PLL2 (PLL circuits), VDD_QFPROM_PRG (QFPROM programming), VDD_P2 (SDC2)
10. VDD_KRAIT (Krait applications microprocessor)

Comments regarding this sequence:

- The core voltage (VDD_CORE) needs to power up before the pad circuits (VDD_PX) so that internal circuits can take control of the I/Os and pads.
  - If pad voltages power up first, the output drivers might be stuck in unknown states, and might cause large leakage currents until VDD_CORE powers on.
- The general-purpose pad voltage (VDD_P3) needs to precede the analog voltages (VDD_AX).
- Only the default regulator VREG_S5B for the VDD_KRAIT is turned on during initial boot. The other three regulators for VDD_KRAIT (VREG_S6B/S7B/S8B) can be powered up by software after the MSM has completed the boot process.
- Any other desired supplies can be powered on by software after the sequence is completed.
- Each domain needs to reach its 90% value before the next domain starts ramping up. For example, when VDD_CORE reaches 90% of its value, the VDD_P3 supply can start ramping up.

3.6 Digital logic characteristics

Specifications for the digital I/Os depend upon the pad voltage being used. Logic specifications are listed in Table 3-5, Table 3-6, Table 3-7, Table 3-8, Table 3-9, and Table 3-10 for VDD_PX = 1.8 V (most I/Os), VDD_PX = 1.2 V (EBI1), VDD_PX = 1.2 V (SDC1), VDD_PX = 1.8 V (SDC1), VDD_PX = 1.8 V (UIM1 and UIM2), and VDD_PX = 2.95 V (UIM1 and UIM2), respectively.

Table 3-5 Digital I/O characteristics for VDD_PX = 1.8 V nominal

Parameter		Comments	Min	Max	Unit
V_{IH}	High-level input voltage	CMOS/Schmitt	0.65 · V_{DD_Px}	V_{DD_Px} + 0.3	V
V_{IL}	Low-level input voltage	CMOS/Schmitt	-0.3	0.35 · V_{DD_Px}	V
V_{SHYS}	Schmitt hysteresis voltage		100	–	mV
I_{IH}	Input high leakage current [1]	No pull-down	–	1	µA
I_{IL}	Input low leakage current [2]	No pull-up	-1	–	µA
I_{IHPD}	Input high leakage current [1, 3]	With pull-down	5	30	µA
I_{ILPU}	Input low leakage current [2, 3]	With pull-up	-30	-5	µA
V_{OH}	High-level output voltage [4]	CMOS, at rated drive strength	V_{DD_Px} - 0.45	V_{DD_Px}	V
V_{OL}	Low-level output voltage [4]	CMOS, at rated drive strength	0	0.45	V
I_{OZH}	Tri-state leakage current [1]	Logic high out, no pull-down	–	1	µA
I_{OZL}	Tri-state leakage current [2]	Logic low out, no pull-up	-1	–	µA
I_{OZHPD}	Tri-state leakage current [1, 3]	Logic high out with pull-down	5	30	µA
I_{OZLPU}	Tri-state leakage current [2, 3]	Logic low out with pull-up	-30	-5	µA
I_{OZHKP}	Tri-state leakage current [1, 3]	Logic high out with keeper	-15	-3	µA
I_{OZLKP}	Tri-state leakage current [2, 3]	Logic low out with keeper	3	15	µA
I_{ISL}	Sleep crystal input leakage		TBD	TBD	µA
I_{IHVKP}	High-V tolerant input leakage	With keeper	TBD	–	µA
C_{IN}	Input capacitance [5]		–	TBD	pF

1. Pin voltage = V_{DD_PX} max. For keeper pins, pin voltage = V_{DD_PX} max - 0.45 V.
2. Pin voltage = GND and supply = V_{DD_Px} max. For keeper pins, pin voltage = 0.45 V and supply = V_{DD_Px} max.
3. Refer to Table 2-1 for pull-up, pull-down, and keeper details.
4. Refer to Table 2-1 for each output pin's drive strength (I_{OH} and I_{OL}); the drive strengths of many output pins are programmable and depend on the associated supply voltage.
5. Input capacitance is guaranteed by design but is not 100% tested.

Table 3-6 Digital I/O characteristics for VDD_P1 = 1.2 V nominal (EBI0/EBI1 interface)

Parameter		Comments	Min	Max	Unit
V_{REF}	Reference voltage		0.49 · V_{DD_PX}	0.51 · V_{DD_PX}	V
V_{IH}	High-level input voltage	CMOS	V_{REF} + 0.10	–	V

Table 3-6 Digital I/O characteristics for VDD_P1 = 1.2 V nominal (EBI0/EBI1 interface) (cont.)

Parameter		Comments	Min	Max	Unit
V_{IL}	Low-level input voltage	CMOS	–	V_{REF} - 0.10	V
I_{IH}	Input high leakage current [1]	No pull-down	–	2.0	µA
I_{IL}	Input low leakage current [2]	No pull-up	-2.0	–	µA
V_{OH}	High-level output voltage [3]	CMOS, at rated drive strength	0.9 · V_{DD_PX}	–	V
V_{OL}	Low-level output voltage [3]	CMOS, at rated drive strength	–	0.1 · V_{DD_PX}	V
I_{OZHPD}	Tri-state leakage current [1, 4]	Logic high out with pull-down	40	200	µA
I_{OZLPU}	Tri-state leakage current [2, 4]	Logic low out with pull-up	-200	-40	µA
I_{OZHKP}	Tri-state leakage current	Logic high with keeper	-120	-10	µA
I_{OZLKP}	Tri-state leakage current	Logic low with keeper	10	120	µA
C_{DIO}	Input output capacitance delta		–	0.2	pF
$C_{I/O}$	I/O capacitance [5]	I/O, DQS, DQ, or clock pins	1.0	1.8	pF

1. Pin voltage = V_{DD_PX} max.
2. Pin voltage = GND and supply = V_{DD_PX} max.
3. Refer to Table 2-1 for each output pin's drive strength (I_{OH} and I_{OL}); the drive strengths of many output pins are programmable and depend on the associated supply voltage.
4. Refer to Table 2-1 for pull-up and pull-down details.
5. Input and I/O capacitances are guaranteed by design but are not 100% tested.

Table 3-7 Digital I/O characteristics for VDD_PX = 1.2 V nominal (SDC1)

Parameter		Comments	Min	Max	Unit
V_{IL}	Input low voltage		V_{SS} - 0.3	0.35 · V_{DD_PX}	V
V_{IH}	Input high voltage		0.65 · V_{DD_PX}	V_{DD_PX} + 0.3	V
V_{OL}	Output low voltage		–	0.25 · V_{DD_PX}	V
V_{OH}	Output high voltage		0.75 · V_{DD_PX}	–	V

Table 3-8 Digital I/O characteristics for VDD_PX = 1.8 V nominal (SDC1)

Parameter		Comments	Min	Max	Unit
V_{IL}	Input low voltage		V_{SS} - 0.3	0.35 · V_{DD_PX}	V
V_{IH}	Input high voltage		0.65 · V_{DD_PX}	V_{DD_PX} + 0.3	V
V_{OL}	Output low voltage		–	0.45	V
V_{OH}	Output high voltage		V_{DD_PX} - 0.45	–	V

Table 3-9 Digital I/O characteristics for VDD_PX = 1.8 V nominal (UIM1 and UIM2 – Class C)

Parameter		Comments	Min	Max	Unit
V_{IH}	High-level input voltage [1]		0.7 · V_{DD_PX}	V_{DD_PX} + 0.3	V
V_{IL}	Low-level input voltage [1]		-0.3	0.2 · V_{DD_PX}	V
I_{IH}	Input high leakage current		-20	20	µA
I_{IL}	Input low leakage current		–	1000	µA
I_{OZH}	High-level, tri-state leakage current		–	5.0	µA
I_{OZL}	Low-level, tri-state leakage current		-5.0	–	µA
V_{OH}	High-level output voltage [2]		0.8 · V_{DD_PX}	V_{DD_PX}	V
V_{OL}	Low-level output voltage [2]		0	0.4	V

1. V_{IH} and V_{IL} are only applicable for I/O signal.
2. UICC specifies V_{OL} = 0.2 · V_{DD_PX} (RST, CLK) and 0.3 V (I/O) and V_{OH} = 0.8 · V_{DD_PX} (RST) and 0.7 · V_{DD_PX} (CLK, I/O). The worse case V_{OL} and V_{OH} are used in the table.

Table 3-10 Digital I/O characteristics for VDD_PX = 2.95 V nominal (UIM1 and UIM2 – Class B)

Parameter		Comments	Min	Max	Unit
V_{IH}	High-level input voltage [1]	CMOS/Schmitt	0.7 · V_{DD_PX}	V_{DD_PX} + 0.3	V
V_{IL}	Low-level input voltage [1]	CMOS/Schmitt	-0.3	0.2 · V_{DD_PX}	V
I_{IH}	Input high leakage current	No pull-down	-20	20	µA
I_{IL}	Input low leakage current	No pull-up	–	1000	µA
V_{OH}	High-level output voltage [2]	CMOS, at rated drive strength	0.8 · V_{DD_PX}	V_{DD_PX}	V
V_{OL}	Low-level output voltage [2]	CMOS, at rated drive strength	0	0.4	V
I_{OZH}	Tri-state leakage current	Logic high out, no pull-down	–	10	µA
I_{OZL}	Tri-state leakage current	Logic low out, no pull-up	-10	–	µA
C_{IN}	Input capacitance		–	TBD	pF

1. V_{IH} and V_{IL} are only applicable for I/O signal.
2. UICC specifies V_{OL} = 0.2 · V_{DD_PX} (RST, CLK) and 0.4 V (I/O) and V_{OH} = 0.8 · V_{DD_PX} (RST) and 0.7 · V_{DD_PX} (CLK, I/O). The worse-case V_{OL} and V_{OH} are used in the table.

In all digital I/O cases, V_{OL} and V_{OH} are linear functions (Figure 3-1) with respect to the drive current (drive currents are given in Table 2-1). They can be calculated using these relationships and based on numbers from Table 3-5:

$$Vol[\max] = \frac{\%drive \times 450}{100} mV$$

$$Voh[\min] = Vdd\_px - \left(\frac{\%drive \times 450}{100}\right) mV$$

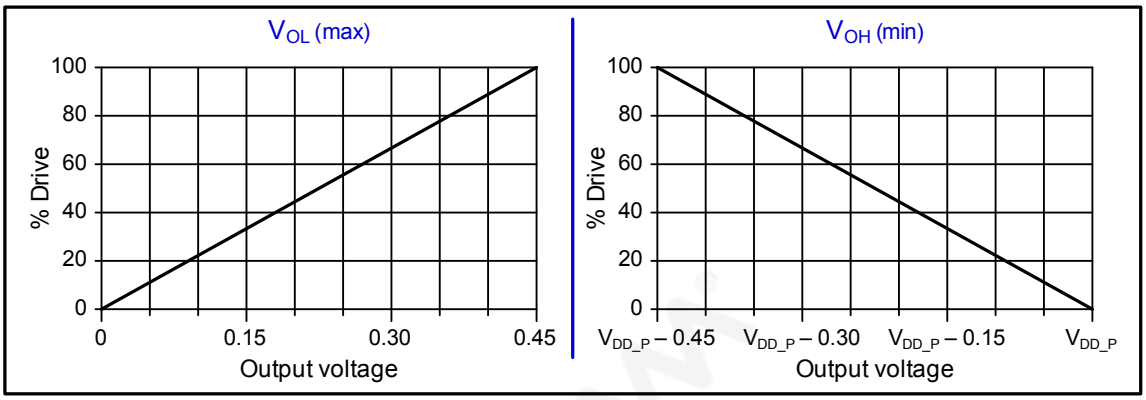


Figure 3-1 IV curve for V_{OL} and V_{OH} (valid for all V_{DD_PX})

3.7 Timing characteristics

Specifications for the device timing characteristics are included (where appropriate) under each function's section, along with all its other performance specifications. Some general comments about timing characteristics and pertinent pad design methodologies are included here.

NOTE All MSM8x74 devices are characterized with actively terminated loads, so all baseband timing parameters in this document assume no bus loading. This is discussed further in Section 3.7.2.

3.7.1 Timing diagram conventions

The conventions used within timing diagrams throughout this document are shown in Figure 3-2.

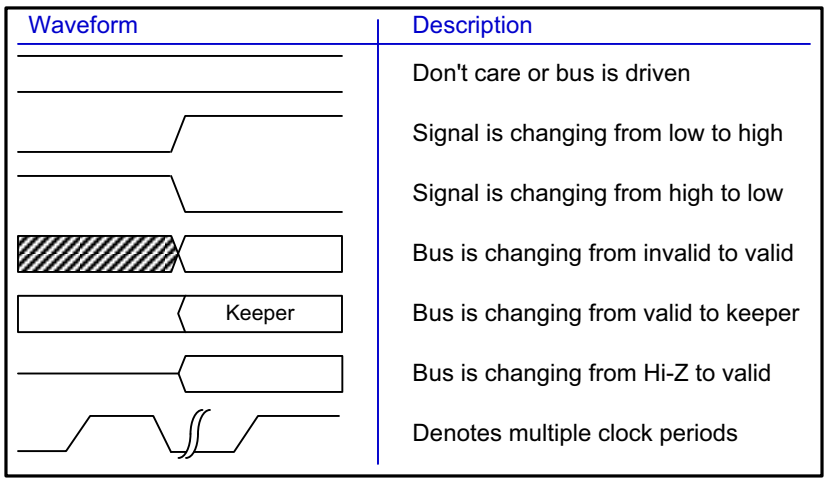


Figure 3-2 Timing diagram conventions

For each signal in the diagram:

- One clock period (T) extends from one rising clock edge to the next rising clock edge.
- The high level represents 1, the low level represents 0, and the middle level represents the floating (high-impedance) state.
- When both the high and low levels are shown over the same time interval, the meaning depends upon the signal type:
  - For a bus-type signal (multiple bits) – the processor or external interface is driving a value, but that value may or may not be valid.
  - For a single signal – indicates don't care.

3.7.2 Rise and fall time specifications

The testers that characterize MSM8x74 devices have actively terminated loads, making the rise and fall times quicker (mimicking a no-load condition). The impact that different external load conditions have on rise and fall times is shown in Figure 3-3.

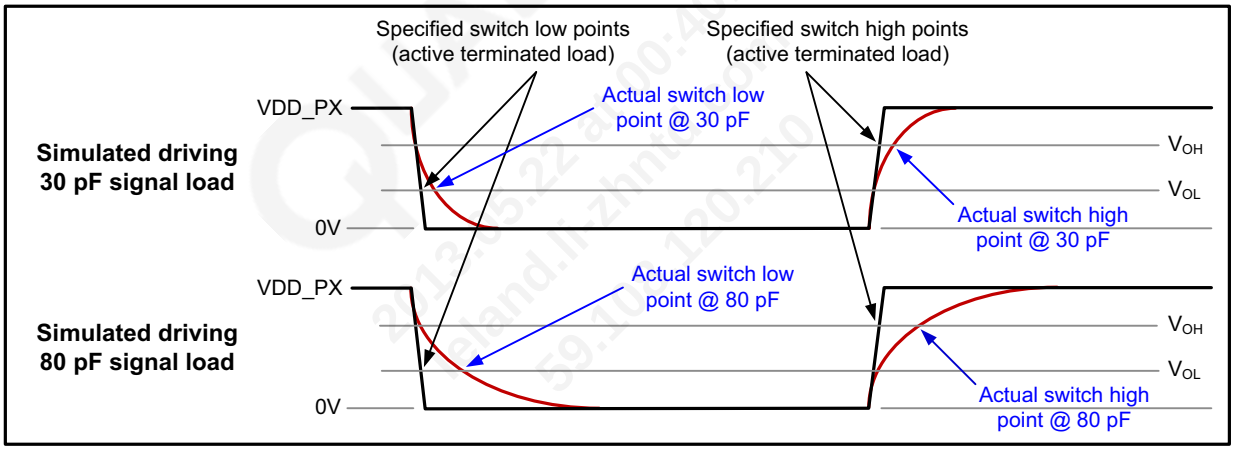


Figure 3-3 Rise and fall times under different load conditions

To account for external load conditions, rise or fall times must be added to parameters that start timing at the MSM device and terminate at an external device (or vice versa). Adding these rise and fall times is equivalent to applying capacitive load derating factors.

3.7.3 Pad design methodology

The MSM8x74 device uses a generic CMOS pad driver design. The intent of the pad design is to create pin response and behavior that is symmetric with respect to the associated V_{DD_PX} supply (Figure 3-4). The input switch point for pure input-only pads is designed to be $V_{DD\_PX}/2$ (or 50% of V_{DD_PX}). The documented switch points (guaranteed over worst-case combinations of process, voltage, and temperature by both design and characterization) are 35% of V_{DD_PX} for V_{IL} and 65% of V_{DD_PX} for V_{IH}.

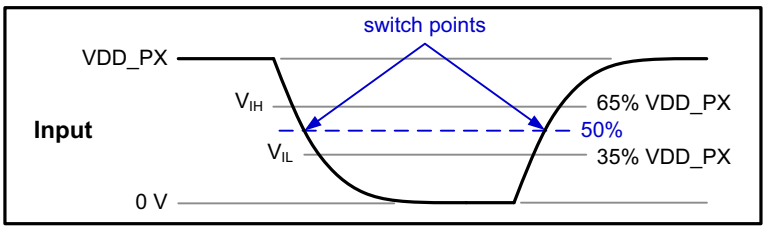


Figure 3-4 Digital input signal switch points

Outputs (address, chip selects, clocks, etc.) are designed and characterized to source or sink a large DC output current (several mA) at the documented V_{OH} (min) and V_{OL}(max) levels over worst-case process/voltage/temperature. Because the pad output structures (Figure 3-5) are essentially CMOS drivers that possibly have a small amount of IR loss (estimated at less than 50 mV under worst-case conditions), the expected *zero DC load* outputs are *estimated* to be:

- $V_{OH} \sim V_{DD\_PX}$ - 50 mV or more
- $V_{OL} \sim$ 50 mV or less

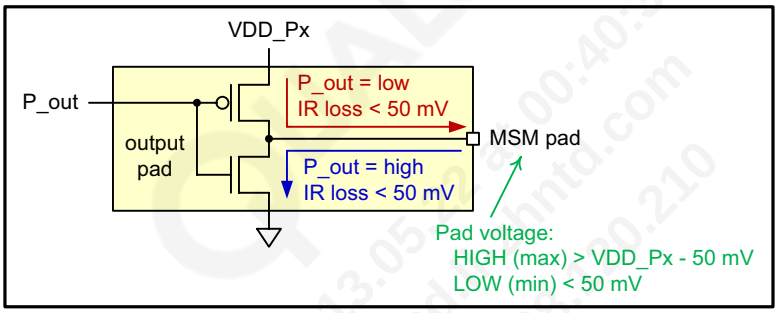


Figure 3-5 Output pad equivalent circuit

The DC output drive strength can be *approximated* by linear interpolations between V_{OH} (min) and V_{DD_PX} - 50 mV, and between V_{OL} (max) and 50 mV. For example, an output pad driving low that guarantees 4.5 mA at V_{OL} (max) will provide approximately 3.0 mA or more at 2/3 × [V_{OL} (max) - 50 mV], and 1.5 mA or more at 1/3 × [V_{OL} (max) - 50 mV]. Likewise, an output pad driving high that guarantees 2.5 mA at V_{OH} (min) will provide approximately 1.25 mA or more at ½ × [V_{DD_PX} - 50 mV + V_{OH} (min)].

The output pads are essentially CMOS outputs with a corresponding FET-type output voltage/current transfer function. When an output pad is shorted to the opposite power rail, the pad is capable of sourcing or sinking I_{SC} (SC = short-circuit) of current, where the magnitude of I_{SC} is larger than the current capability at the intended output logic levels.

Since the target application includes a radio, output pads are designed to *minimize* output slew rates. Decreased slew rates limit high-frequency spectral components that tend to desensitize the companion radio.

Output drivers' rise time (**t**(r)) and fall time (**t**(f)) values are functions of board loading. Bidirectional pins include both input and output pad structures, and behave accordingly when used as inputs or outputs within the system. Both input and output behaviors were described above.

In addition to being bidirectional, databus pins also include pad keepers. These keepers are weak flip-flops (easily over-driven by an external source) on the pad side of the structure to encourage an otherwise undriven pad voltage to migrate to a power or ground rail, either to help ensure hold-time requirements or to minimize power consumption within otherwise undriven pad structures. Keepers have the following impacts on the physical interface:

- External sources driving these pins must overcome the keepers to drive a logic level on such pins. The amount of current required must be greater than the *maximum* I_{OZLKP} values listed within the tables of Section 3.6.
- When an external source releases control of such a pin, the keeper tends to hold the pin's last logic level (subject to system-level leakages and capacitive loading effects). The *minimum* I_{OZLKP} current values may be sustained indefinitely without upsetting the keeper state.

3.8 Memory support

All timing parameters in this document assume no bus loading. Rise/fall time numbers must be factored into the numbers in this document. For example, setup time numbers will get worse and hold time numbers may get better.

3.8.1 EBI0 and EBI1 memory support

The EBI0 and EBI1 ports are dedicated to the PoP LPDDR3 SDRAM memory that is attached to the top of the MSM8x74 chipset. The memory pinout, package requirements are specified in 80-VP300-5 PoP Memory for MSM8974 Specification.

3.8.1.1 EBI0 and EBI1 pad drive strength

The pads for EBI0 and EBI1 are tailored for its 1.2 V interface and are source-terminated. These pads can support output impedances from 24 Ω to 80 Ω as specified in the Jedec standard.

3.8.1.2 LPDDR3 SDRAM clock

For any timing analysis, the measurement point for all signals is at 50% VDD_Px. All output timing parameters represent the point of the output signal transition; additional accounting for signal rise and fall times for specific bus loading is required.

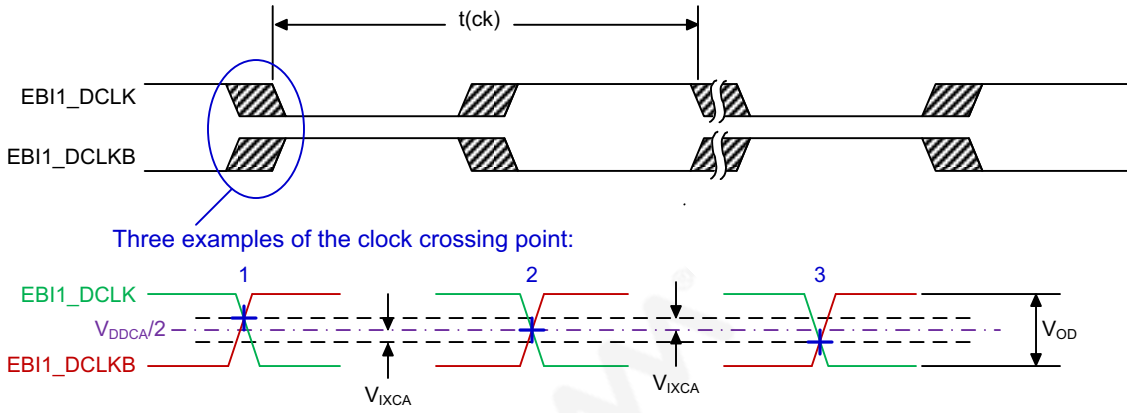


Figure 3-6 DDR SDRAM EBI1_DCLK and EBI1_DCLKB

Table 3-11 DDR SDRAM clock timing parameters

Parameter		Comments	Min	Typ	Max	Unit
$1/t_{CK}$	DDR clock frequency		–	–	800	MHz
	Duty cycle		45	–	55	%
V_{IXCA}	Clock crossover-point	± offset from $V_{DDCA}/2$	TBD	–	TBD	mV
V_{OD}	Differential output voltage		TBD	–	–	V

3.8.1.3 LPDDR3 SDRAM strobe

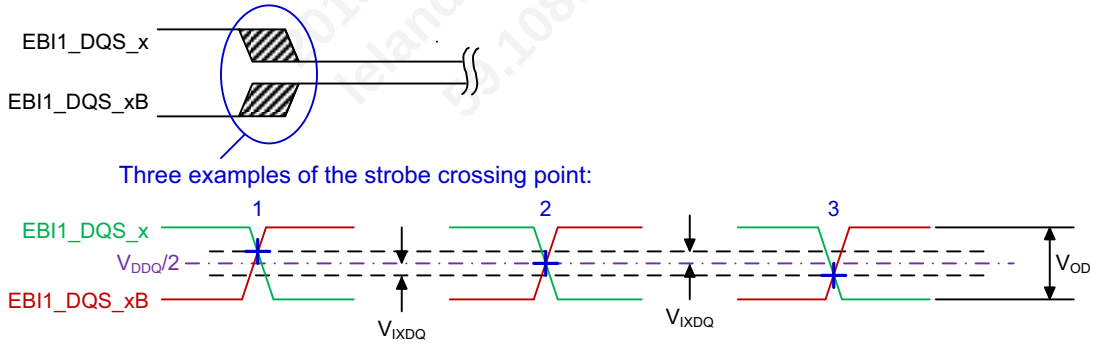


Figure 3-7 DDR SDRAM EBI1_DQS_x and EBI1_DQS_xB

Table 3-12 DDR SDRAM DQS timing parameters

Parameter		Comments	Min	Typ	Max	Unit
V_{IXDQ}	Clock crossover-point	± offset from $V_{DDQ}/2$	TBD	–	TBD	mV
V_{OD}	Differential output voltage		TBD	–	–	V

3.8.1.4 LPDDR3 SDRAM read and write timing

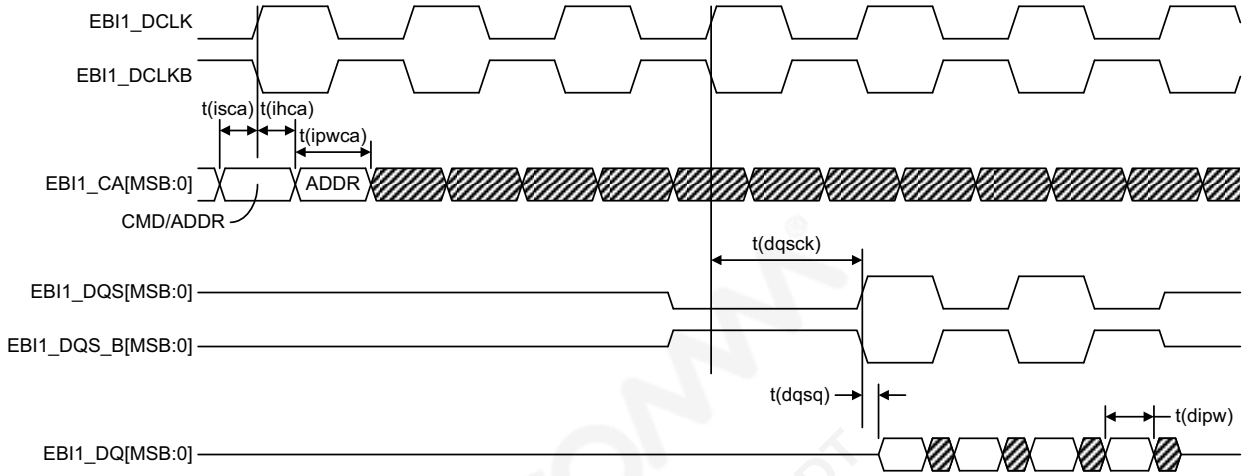


Figure 3-8 DDR SDRAM read timing

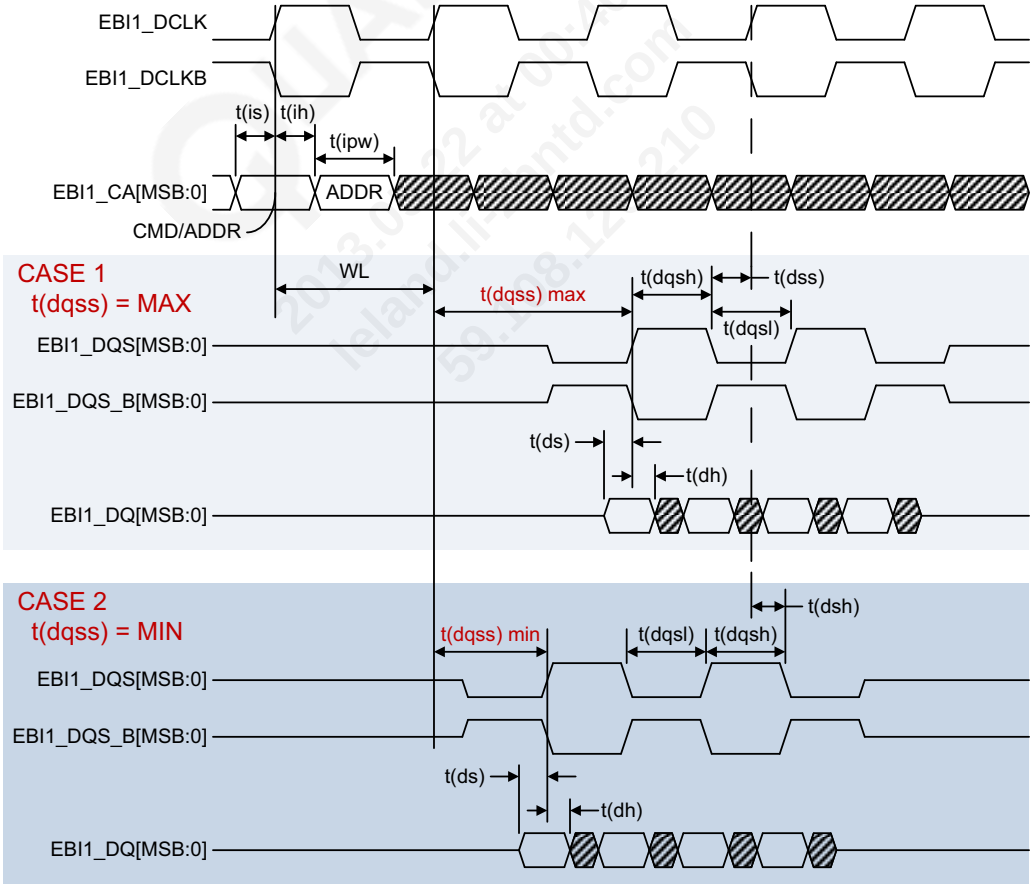


Figure 3-9 DDR SDRAM write timing

Table 3-13 DDR SDRAM read and write timing specifications

Parameter		Comments	Min	Typ	Max	Unit
LPDDR3 (800 MHz) – common to read and write						
t(isca) [1]	Address & control in setup time before CK		TBD	–	–	ps
t(ihca) [1]	Address & control input hold time after CK		TBD	–	–	ps
t(ipwca)	Address & control input pulse width		TBD	–	–	t(ck)
t(dipw)	DQ & DM pulse width		TBD	–	TBD	ns
t(iscs)	CS_n input setup time		TBD	–	TBD	ns
t(ihcs)	CS_n input hold time		TBD	–	TBD	ns
t(ipwcs)	CS_n input pulse width		TBD	–	–	t(ck)
t(tdiff)	Input transition slew rate from VIL to VIH	Differential clock	TBD	–	TBD	V/ns
t(t)	Input transition time from VIL to VIH	Other than diff clock	TBD	–	TBD	V/ns
LPDDR3 (800 MHz) – read cycle						
t(dqsck)	DQS access time from clock		TBD	–	TBD	ns
t(dqsq) [2]	DQS to DQ skew limit		TBD	–	TBD	ps
t(rpre) [3]	Read preamble		TBD	–	TBD	t(ck)
LPDDR3 (800 MHz) – write cycle						
t(ds) [1]	DQ and DM input setup time before DQS		TBD	–	–	ps
t(dh) [1]	DQ and DM input hold time after DQS		TBD	–	–	ps
t(dqsh) [2]	DQS input high-level width		TBD	–	TBD	t(ck)
t(dqsl) [2]	DQS input low-level width		TBD	–	TBD	t(ck)
t(dqss) [2]	First DQS latching transition		TBD	–	TBD	t(ck)
t(dss) [2]	DQS falling edge to CK setup time		TBD	–	TBD	t(ck)
t(dsh) [2]	DQS falling edge hold time after CK		TBD	–	TBD	t(ck)

1. This parameter is referenced to the fast slew rate value in the speed-appropriate LPDDR3 JESD209-3 specification.
2. DQS lines must be well isolated to reduce any noise induced into them.
3. This parameter is defined using CAS latency equal to 3 or CL = 3.

3.8.2 eMMC on SDC1

eMMC NAND flash can be supported via the SDC1 port. See Section 3.10.1 for secure digital interface details.

3.8.3 NOR memory on SPI

SPI can be used to support NOR memory devices with appropriate user-modified software. See Section 3.10.12 for serial peripheral interface details.

3.9 Multimedia

Multimedia parameters requiring performance specification are addressed in this section.

3.9.1 Camera interfaces

Camera support depends upon the MSM variant:

- MSM8x74 supports up to three 4-lane camera interfaces or up to four (two 4-lane and two 1-lane) camera interfaces.

Table 3-14 Supported MIPI_CSI standards and exceptions

Applicable standard	Feature exceptions	MSM variations
MIPI Alliance Specification v1.00 for Camera Serial Interface	None	None

3.9.2 Audio support

The MSM8x74 supports the WCD9320 audio codec IC to provide the system's audio functions. MSM audio-related interface options with the WCD include:

- SLIMbus – Section 3.10.4
- I2S – Section 3.10.5
- PCM – Section 3.10.6
- I2C – Section 3.10.11

See the *WCD9320 Device Specification* (80-NA556-1) for its performance characteristics.

The MSM8x74 also supports the audio portion of HDMI using MSM-internal connections – see Section 3.9.4 for supported HDMI specifications.

3.9.3 Display support

MSM8x74 supports two 4-lane MIPI_DSI interfaces and a 4-lane eDP interface.

Table 3-15 Supported MIPI_DSI standards and exceptions

Applicable standard	Feature exceptions	MSM variations
MIPI Alliance Specification v1.01 for Display Serial Interface	None	None
MIPI D-PHY Specification v0.65, v0.81, v0.90	None	None
eDP Specification v1.2	None	None

3.9.4 A/V outputs

The HDMI port is supported by the MSM8x74.

Table 3-16 Supported HDMI standards and exceptions

Applicable standard	Feature exceptions	MSM variations
HDMI Specification version 1.4a	None	None

3.9.5 DMB support

The MSM8x74 supports an external DMB IC solution using the following interface options:

- Up to two TSIF interfaces – Section 3.10.7
- SD – Section 3.10.1

3.10 Connectivity

The connectivity functions supported by the MSM8x74 that require electrical specifications include:

- Secure digital (SD), including SD cards and multimedia cards (MMC)
- High-speed universal serial bus/on-the-go (USB-OTG) with built-in physical layer (PHY)
- High-speed inter-chip (HSIC) bus interface
- User integrated module (UIM) ports, including dual-voltage options
- Serial low-power inter-chip media bus (SLIMbus) interface
- Inter-IC sound (I2S) interfaces
- Pulse-coded modulation (PCM) interfaces
- Transport stream interface (TSIF) interfaces
- Touch screen connections
- Through proper configuration of the twelve BLSP ports:
  - Universal asynchronous receiver/transmitter (UART) ports
  - User identity module (UIM) ports
  - Inter-integrated circuit (I2C) interfaces
  - Serial peripheral interface (SPI) ports

Pertinent specifications for these functions are stated below.

NOTE In addition to the following hardware specifications, please consult the latest software release notes for software-based performance features or limitations.

3.10.1 Secure digital interfaces

Table 3-17 Supported SD standards and exceptions

Applicable standard	Feature exceptions	MSM variations
Multimedia Card Host Specification version 4.5	None	Timing specifications – see Figure 3-10 and Table 3-18
Secure Digital: Physical Layer Specification version 3.0	None	
SDIO Card Specification version 3.0	None	

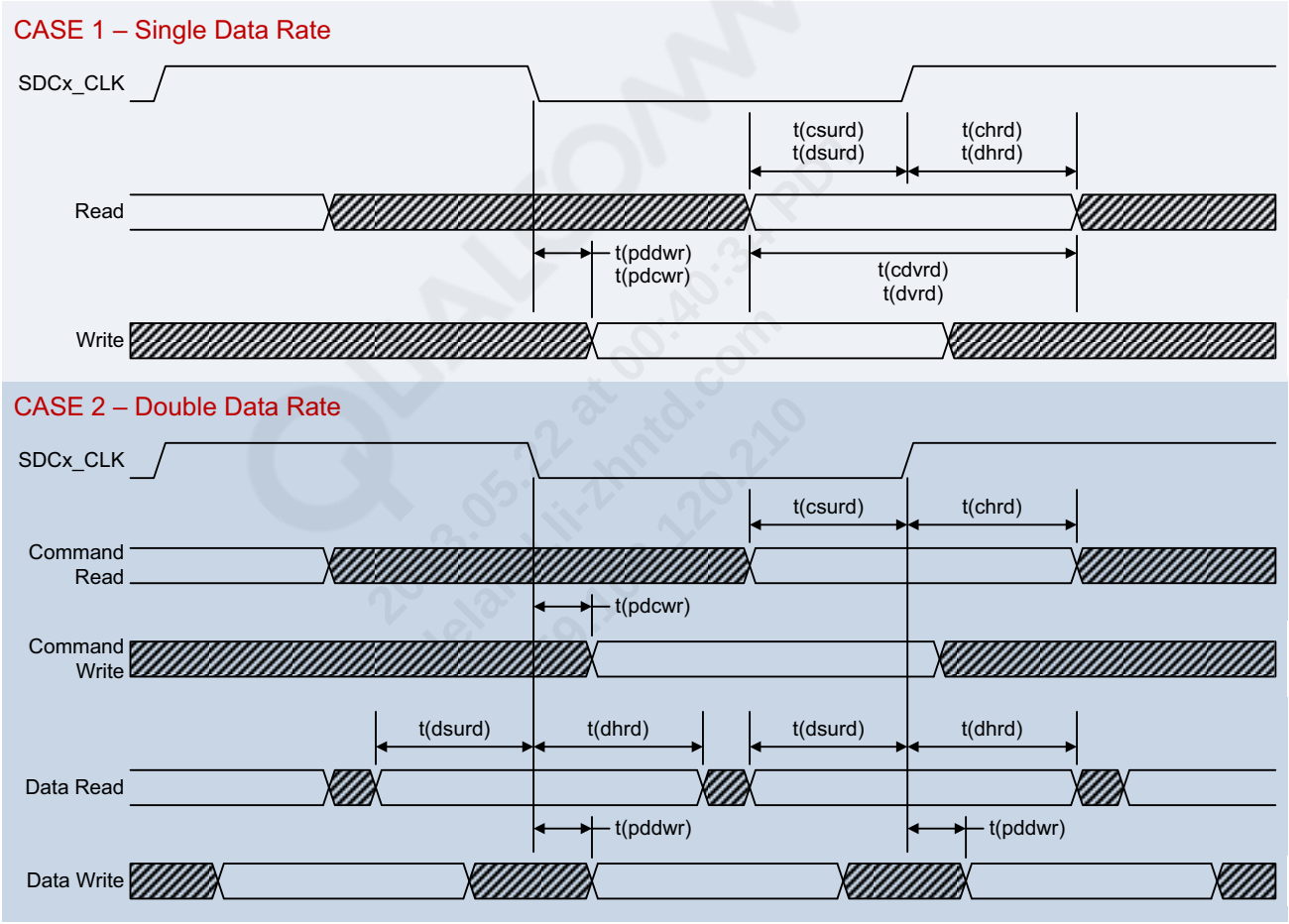


Figure 3-10 Secure digital interface timing

Table 3-18 Secure digital interface timing

Parameter		Comments [1]	Min	Typ	Max	Unit
Single data rate (SDR) mode – SDC1, SDC2, SDC3, and SDC4						
t(chrd)	Command hold		1.50	–	–	ns
t(csurd)	Command setup		2.50	–	–	ns
t(dhrd)	Data hold		1.50	–	–	ns
t(dsurd)	Data setup		2.50	–	–	ns
t(pddwr)	Propagation delay on data write		-3.70	–	TBD	ns
t(pdcwr)	Propagation delay on command write		-3.70	–	1.50	ns
SDR mode – SDC3 and SDC4						
t(cvdrd)	Command valid		2.50	–	–	ns
t(dvdrd)	Data valid		2.50	–	–	ns
t(pddwr)	Propagation delay on data write		-1.45	–	0.85	ns
t(pdcwr)	Propagation delay on command write		-1.45	–	0.85	ns
Double data rate (DDR) mode – SDC1 and SDC2						
t(chrd)	Command hold		1.50	–	–	ns
t(csurd)	Command setup		6.30	–	–	ns
t(dhrd)	Data hold		1.50	–	–	ns
t(dsurd)	Data setup		2.00	–	–	ns
t(pddwr)	Propagation delay on data write		0.80	–	6.00	ns
t(pdcwr)	Propagation delay on command write		-8.20	–	3.00	ns

1. Timing is characterized with the following clock rates:
   – TBD

3.10.2 USB interfaces

Table 3-19 Supported USB standards and exceptions

Applicable standard	Feature exceptions	MSM variations
Universal Serial Bus Specification, Revision 2.0 (April 27, 2000 or later)	None	Operating voltages, system clock, and VBUS – see Table 3-20
Universal Serial Bus Specification, Revision 3.0 (June 6, 2011 or later)	None	None
UTMI + Low Pin Interface (ULPI) Specification (October 20, 2004 Revision 1.1 or later)	None	None
On-The-Go Supplement to the USB 2.0 Specification (June 24, 2003, Revision 1.0A or later)	None	None

Table 3-20 MSM-specific USBPHY specifications

Parameter	Comments	Min	Typ	Max	Unit
USBPHY_SYSCLK					
Frequency	19.2 MHz clock is required	–	19.2	–	MHz
Clock deviation		-400	–	400	ppm
Jitter (peak-to-peak)	0.5 to 1.75 MHz	0	–	60	ps
Duty cycle		40	–	60	%
Low-level input voltage (V_{IL})		–	–	0.85	V
High-level input voltage (V_{IH})		1.27	–	–	V
USBPHY_VBUS					
Valid USB_HS_VBUS detection voltage		2.00	–	5.25	V

3.10.3 HSIC interface

Table 3-21 Supported HSIC standards and exceptions

Applicable standard	Feature exceptions	MSM variations
High-speed Inter-chip USB Electrical Specification, version 1.0	Device-mode not supported	None

3.10.4 SLIMbus interface

Table 3-22 Supported SLIMbus standards and exceptions

Applicable standard	Feature exceptions	MSM variations
MIPI Alliance Specification for Serial Low-power Interchip Media Bus Version 1.01.01	None	Maximum clock output slew rate might be greater than 20% * V_{DD} [V/ns] for 15 pF load condition.

3.10.5 I2S interfaces

There are two I2S interface types supported by the MSM8x74:

- Legacy I2S interfaces for primary and secondary microphones and speakers.
- The MI2S (multiple I2S) interface for microphone and speaker functions, including 7.1 audio for HDMI.

The following information applies to both interface types.

Table 3-23 Supported I2S standards and exceptions

Applicable standards	Feature exceptions	MSM variations
Phillips I2S Bus Specifications, revised June 5, 1996.	None	When an external SCK clock is used, a duty cycle between 45% to 55% is required.

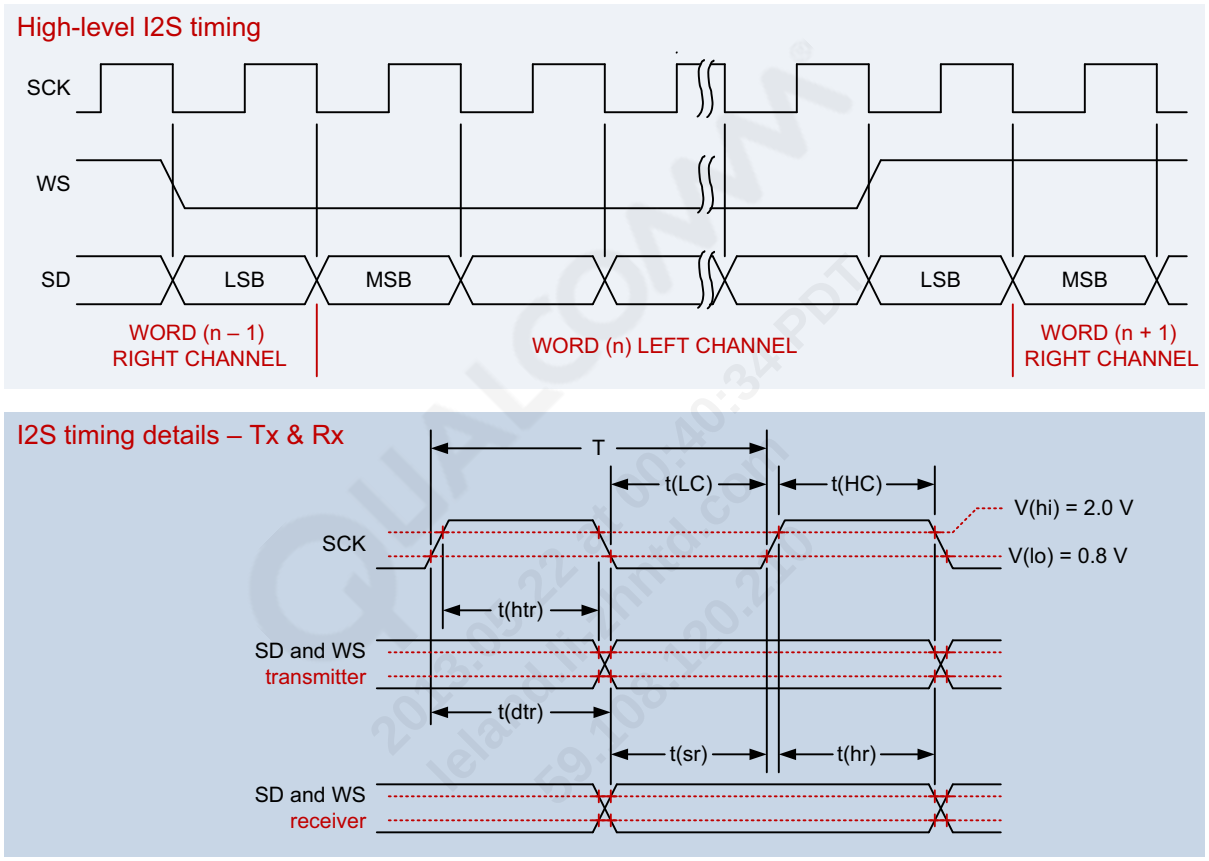


Figure 3-11 I2S timing diagram

Table 3-24 I2S interface timing

Parameter	Comments [1]	Min	Typ	Max	Unit
Using internal SCK					
Frequency		–	–	12.288	MHz
Clock period T		81.380	–	–	ns
Clock high t(HC)		0.45 · T	–	0.55 · T	ns
Clock low t(LC)		0.45 · T	–	0.55 · T	ns
SD & WS input setup time t(sr)		16.276	–	–	ns
SD & WS input hold time t(hr)		0	–	–	ns
SD & WS output delay t(dtr)		–	–	65.100	ns
SD & WS output hold time t(htr)		0	–	–	ns

Table 3-24 I2S interface timing (cont.)

Parameter	Comments [1]	Min	Typ	Max	Unit
Using external SCK					
Frequency		–	–	12.288	MHz
Clock period T		81.380	–	–	ns
Clock high t(HC)		0.45 · T	–	0.55 · T	ns
Clock low t(LC)		0.45 · T	–	0.55 · T	ns
SD & WS input setup time t(sr)		16.276	–	–	ns
SD & WS input hold time t(hr)		0	–	–	ns
SD & WS output delay t(dtr)		–	–	65.100	ns
SD & WS output hold time t(htr)		0	–	–	ns

1. Load capacitance between 10 to 40 pF.

3.10.6 External codec PCM interface

3.10.6.1 Primary PCM interface (2048 kHz clock)

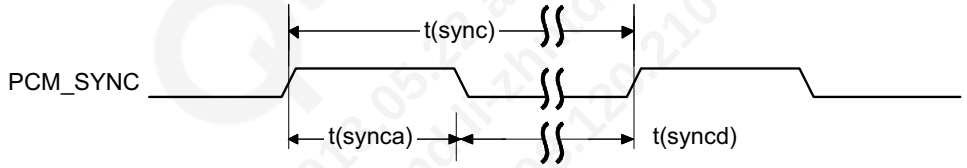


Figure 3-12 PCM_SYNC timing

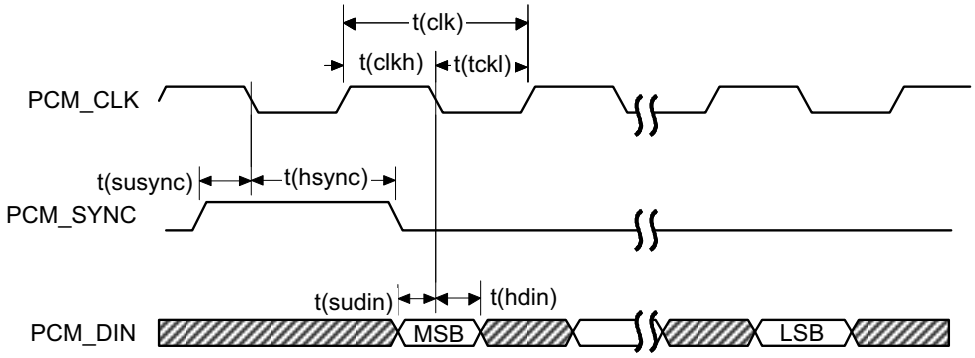


Figure 3-13 PCM_CODEC to MSM timing

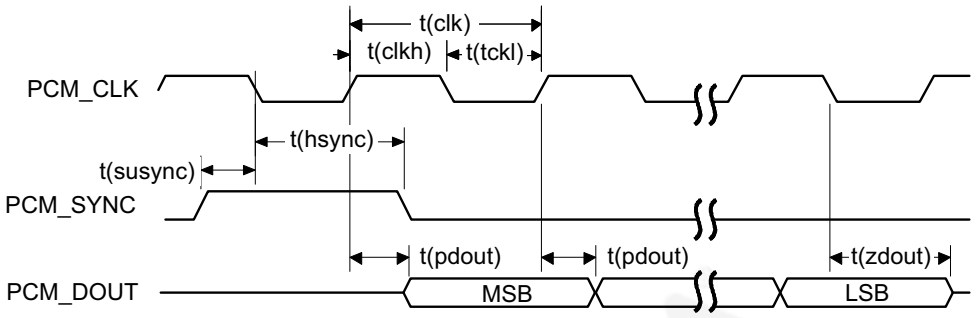


Figure 3-14 MSM to PCM_CODEC timing

Table 3-25 PCM_CODEC timing parameters

Parameter		Comments	Min	Typ	Max	Unit
t(sync)	PCM_SYNC cycle time		–	125	–	µs
t(synca)	PCM_SYNC asserted time		–	488	–	ns
t(syncd)	PCM_SYNC de-asserted time		–	124.5	–	µs
t(clk)	PCM_CLK cycle time		–	488	–	ns
t(clkh)	PCM_CLK high time		–	244	–	ns
t(clkl)	PCM_CLK low time		–	244	–	ns
t(susync)	PCM_SYNC offset time to PCM_CLK falling		–	122	–	ns
t(sudin)	PCM_DIN setup time to PCM_CLK falling		60	–	–	ns
t(hdin)	PCM_DIN hold time after PCM_CLK falling		10	–	–	ns
t(pdout)	Delay from PCM_CLK rising to PCM_DOUT valid		–	–	60	ns
t(zdout)	Delay from PCM_CLK falling to PCM_DOUT HIGH-Z		–	160	–	ns

3.10.6.2 Auxiliary PCM interface (128 kHz clock)

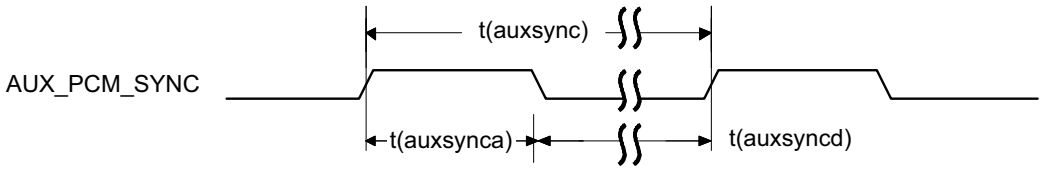


Figure 3-15 AUX_PCM_SYNC timing

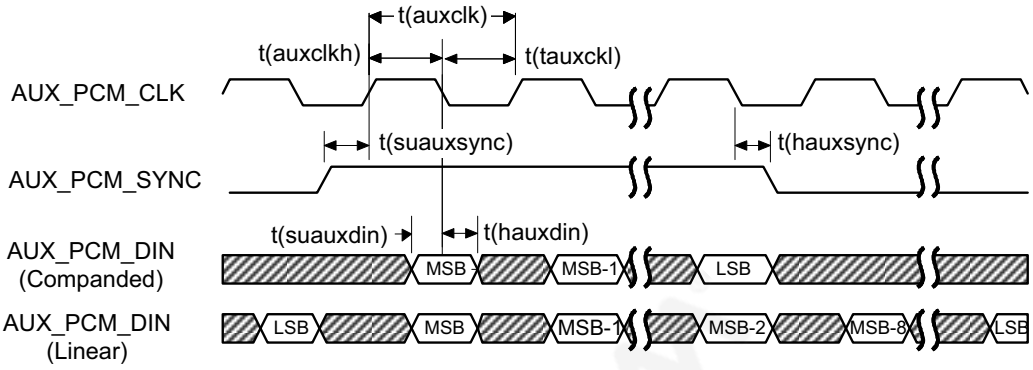


Figure 3-16 AUX_PCM_CODEC to MSM timing

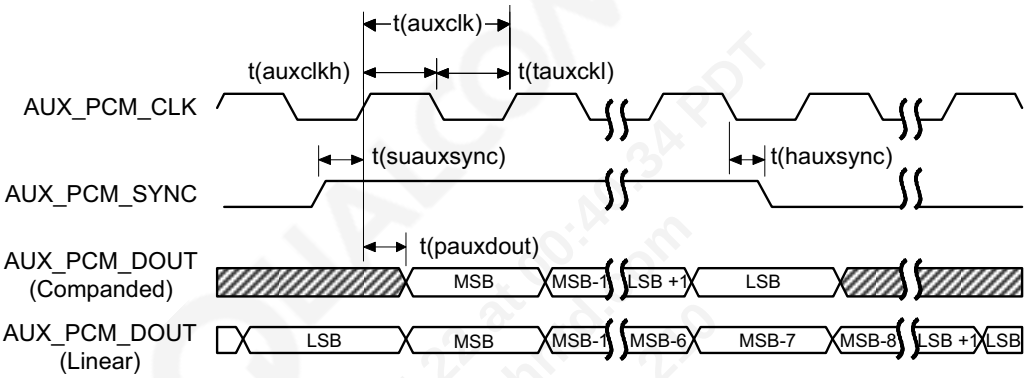


Figure 3-17 MSM to AUX_PCM_CODEC timing

Table 3-26 AUX_PCM_CODEC timing parameters

Parameter		Comments	Min	Typ	Max	Unit
t(auxsync) [1]	AUX_PCM_SYNC cycle time		–	125	–	µs
t(auxsynca) [1]	AUX_PCM_SYNC asserted time		62.4	62.5	–	µs
t(auxsyncd) [1]	AUX_PCM_SYNC de-asserted time		62.4	62.5	–	µs
t(auxclk) [1]	AUX_PCM_CLK cycle time		–	7.8	–	µs
t(auxclkh) [1]	AUX_PCM_CLK high time		3.8	3.9	–	µs
t(auxclkl) [1]	AUX_PCM_CLK low time		3.8	3.9	–	µs
t(suauxsync)	AUX_PCM_SYNC setup time to AUX_PCM_CLK rising		1.95	–	–	ns
t(hauxsync)	PCM_SYNC hold time after AUX_PCM_CLK rising		1.95	–	–	ns
t(suauxdin)	AUX_PCM_DIN setup time to AUX_PCM_CLK falling		70	–	–	ns
t(hauxdin)	AUX_PCM_DIN hold time after AUX_PCM_CLK falling		20	–	–	ns
t(pauxdout)	Delay from AUX_PCM_CLK to AUX_PCM_DOUT valid		–	–	50	ns

1. These values require that the CODEC_CTL is not being used to override the codec clock and sync operation.

3.10.7 Transport stream interface

Table 3-27 Supported TSIF standards and exceptions

Applicable standard	Feature exceptions	MSM variations
ITU-T H.222.0 Transport Stream (HTS); also known as ISO/IEC 13818-1	None	None

3.10.8 Touch screen connections

Touch screen panels are supported using I2C busses (Section 3.10.11) and GPIOs configured as discrete digital inputs (Section 3.6). Additional specifications are not required.

3.10.9 High-speed UART interface

Table 3-28 Supported UART standards and exceptions

Applicable standard	Feature exceptions	MSM variations
EIA RS232-C	None	None

3.10.10 UIM interface

Table 3-29 Supported UIM standards and exceptions

Applicable standard	Feature exceptions	MSM variations
ISO/IEC 7816-3 [1]	None	None

1. With proper GPIO configuration, the MSM8x74 supports dual-voltage (1.8 V and 2.85 V) user identity modules.

3.10.11 I2C interface

Table 3-30 Supported I2C standards and exceptions

Applicable standard	Feature exceptions	MSM variations
I2C Specification, version 3.0	None	None

3.10.12 Serial peripheral interface

The MSM8x74 supports SPI as a master only. Any one of the twelve BLSP ports can be configured as an SPI master, but its *maximum speed* is 52 MHz.

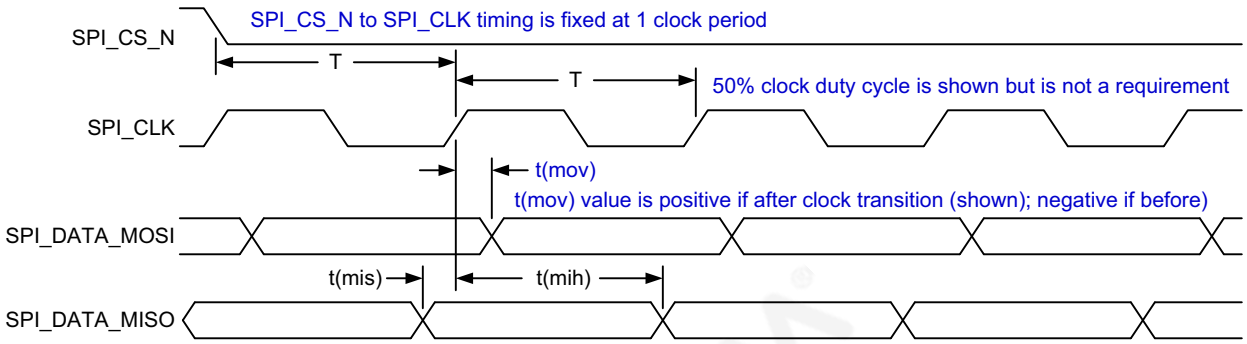


Figure 3-18 SPI master timing diagram

Table 3-31 SPI master timing characteristics

Parameter	Comments	Min	Typ	Max	Unit
T (SPI clock period) [1]	52 MHz max	19	–	–	ns
t(ch)	clock high	8	–	–	ns
t(cl)	clock low	8	–	–	ns
t(mov)	master output valid	-5	–	5	ns
t(mis)	master input setup	5	–	–	ns
t(mih)	master input hold	1	–	–	ns

1. The minimum clock period includes 1% jitter of maximum frequency.

3.11 Internal functions

Some internal functions require external interfaces to enable their operation. These include clock generation, modes and resets, and JTAG functions – as specified below.

3.11.1 Clocks

Clocks that are specific to particular functions are addressed in the corresponding sections of this document. Others are specified here.

3.11.1.1 19.2 MHz XO input

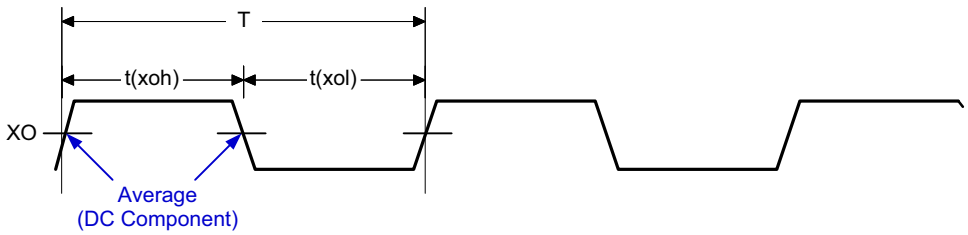


Figure 3-19 XO timing parameters

Table 3-32 XO timing parameters

Parameter		Comments [1]	Min	Typ	Max	Unit
t(xoh)	XO logic high		22.6	–	29.5	ns
t(xol)	XO logic low		22.6	–	29.5	ns
T	XO clock period		–	52.083	–	ns
1/T	Frequency	19.2 MHz must be used	–	19.2	–	MHz

1. See the *19.2 MHz Modem Crystal Qualification Requirements and Approved Suppliers* (80-V9690-19) and *GPS Quality, 19.2 MHz 2016 Package Size, TH+Xtal Mini-Specification* (80-V9690-26) documents for more information.

3.11.1.2 Sleep clock

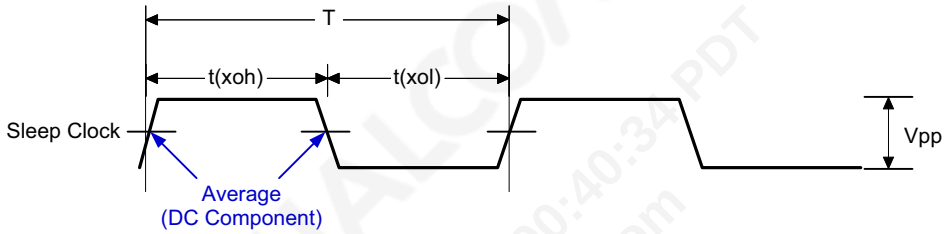


Figure 3-20 Sleep clock timing parameters

Table 3-33 Sleep clock timing parameters

Parameter		Comments	Min	Typ	Max	Unit
t(xoh)	Sleep clock logic high		4.58	–	25.94	µs
t(xol)	Sleep clock logic low		4.58	–	25.94	µs
T	Sleep clock period		–	30.518	–	µs
F	Sleep clock frequency	F = 1/T	–	32.768	–	kHz
Vpp	Peak-to-peak voltage		–	1.8	–	V

3.11.2 Modes and resets

Mode and reset functions are basic digital I/Os that meet the performance specifications presented in Section 3.6.

3.11.3 JTAG

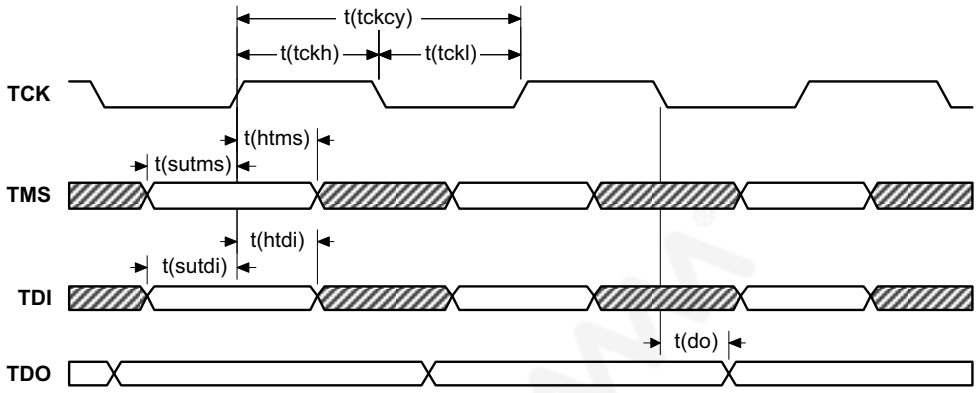


Figure 3-21 JTAG interface timing diagram

Table 3-34 JTAG interface timing characteristics

Parameter		Comments	Min	Typ	Max	Unit
t(tckcy)	TCK period		50	–	–	ns
t(tckh)	TCK pulse width high		20	–	–	ns
t(tckl)	TCK pulse width low		20	–	–	ns
t(sutms)	TMS input setup time		5	–	–	ns
t(htms)	TMS input hold time		20	–	–	ns
t(sutdi)	TDI input setup time		5	–	–	ns
t(htdi)	TDI input hold time		20	–	–	ns
t(do)	TDO data output delay		–	–	15	ns

3.12 RF and power management interfaces

The supported chipset and RFFE interfaces are listed in Table 2-9 and Table 2-10. The digital I/Os must meet the logic-level requirements specified in Section 3.6. The Rx and Tx baseband interfaces are proprietary, and therefore are not specified.

3.12.1 RF Front End (RFFE)

Table 3-35 Supported RFFE standards and exceptions

Applicable standard	Feature exceptions	MSM variations
MIPI Alliance Specification for RF Front-End Control Interface version 1.0	None	None

3.12.2 System Power Management Interface (SPMI)

Table 3-36 Supported SPMI standards and exceptions

Applicable standard	Feature exceptions	MSM variations
MIPI Alliance Specification for System Power Management Interface (SPMI) version 1.0	None	None

4 Mechanical Information

4.1 Device physical dimensions

The MSM8x74 chipset is available in the below mentioned Molded Laser PoP (MLP) and Bare Die PoP (BDP) 990-pin package-on-package nanoscale packages that includes dedicated ground pins for improved grounding, mechanical strength, and thermal continuity. The MLP 990 PNSP has a 15 mm × 15 mm body with a maximum height of 0.91 mm. The BDP 990B PNSP has a 15 mm × 15 mm body with a maximum height of 0.74 mm. Pin A1 is located by an indicator mark on the top of the package (after the PoP memory is attached), and by the ball pattern when viewed from below. A simplified version of the 990 PNSP outline drawing is shown in Figure 4-1 and the 990B PNSP outline drawing is shown in Figure 4-2.

NOTE Click the link below to download the 990 PNSP outline drawing (NT90-N9094-1) from the CDMA Tech Support website.

https://downloads.cdmatech.com/qdc/drl/objectId/09010014818a522a

If you have permission to view the document, a prompt will be presented for initiating the download.

NOTE Click the link below to download the 990B PNSP outline drawing (NT90-NC165-1) from the CDMA Tech Support website.

https://downloads.cdmatech.com/qdc/drl/objectId/0901001481dc5767

If you have permission to view the document, a prompt will be presented for initiating the download.

NOTE Subscribe to the package drawing to be notified of any changes.

Click the **Help** button to download the latest revision of the *Using CDMATech Support Documents and Downloads User Guide* (80-V7273-1). This document includes subscription instructions.

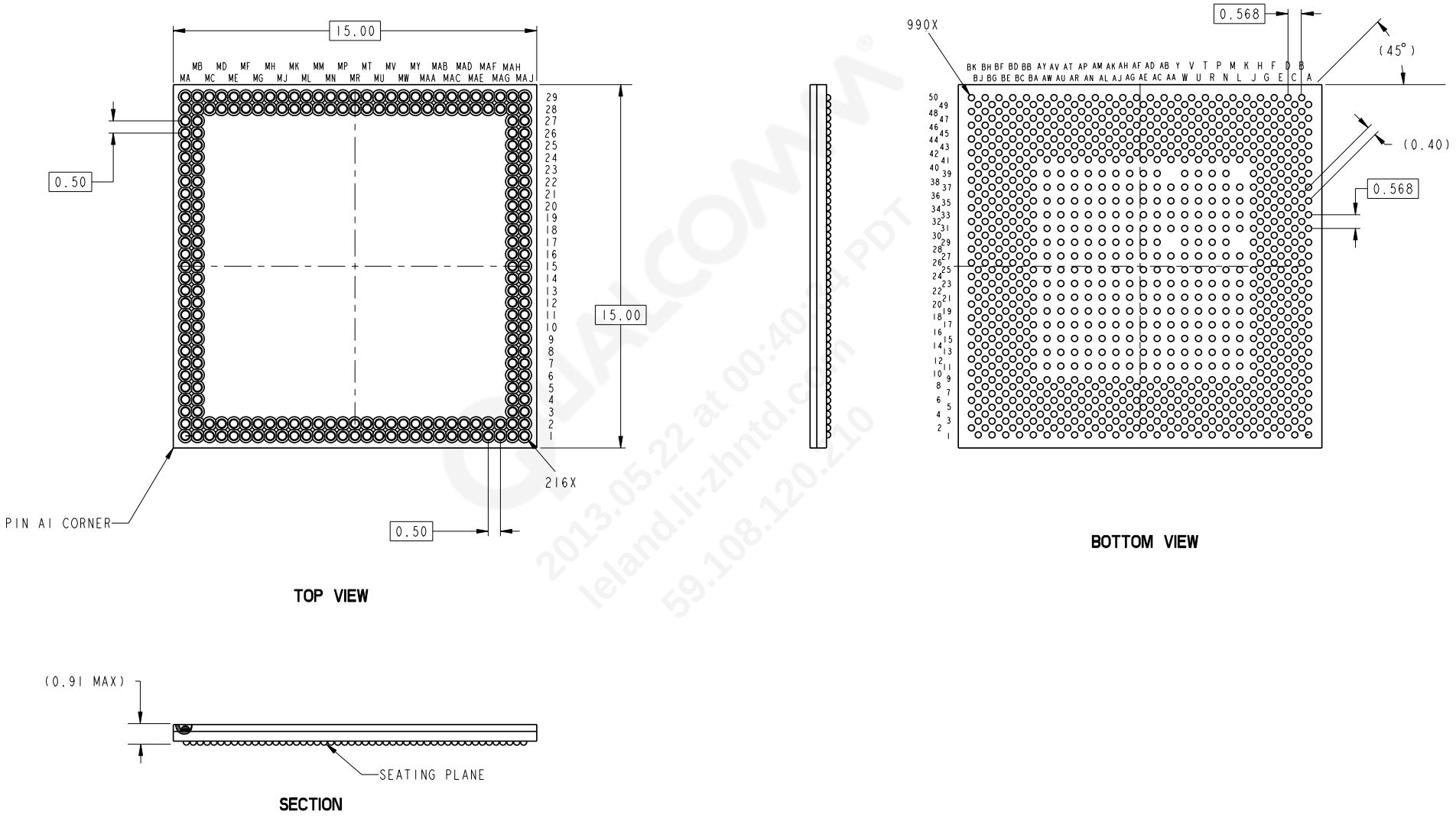


Figure 4-1 990-PNSP (15 × 15 × 0.91 mm) outline drawing

NOTE This is a simplified outline drawing. Click the link below to download the complete, up-to-date package outline drawing:

https://downloads.cdmatech.com/qdc/drl/objectId/09010014818a522a

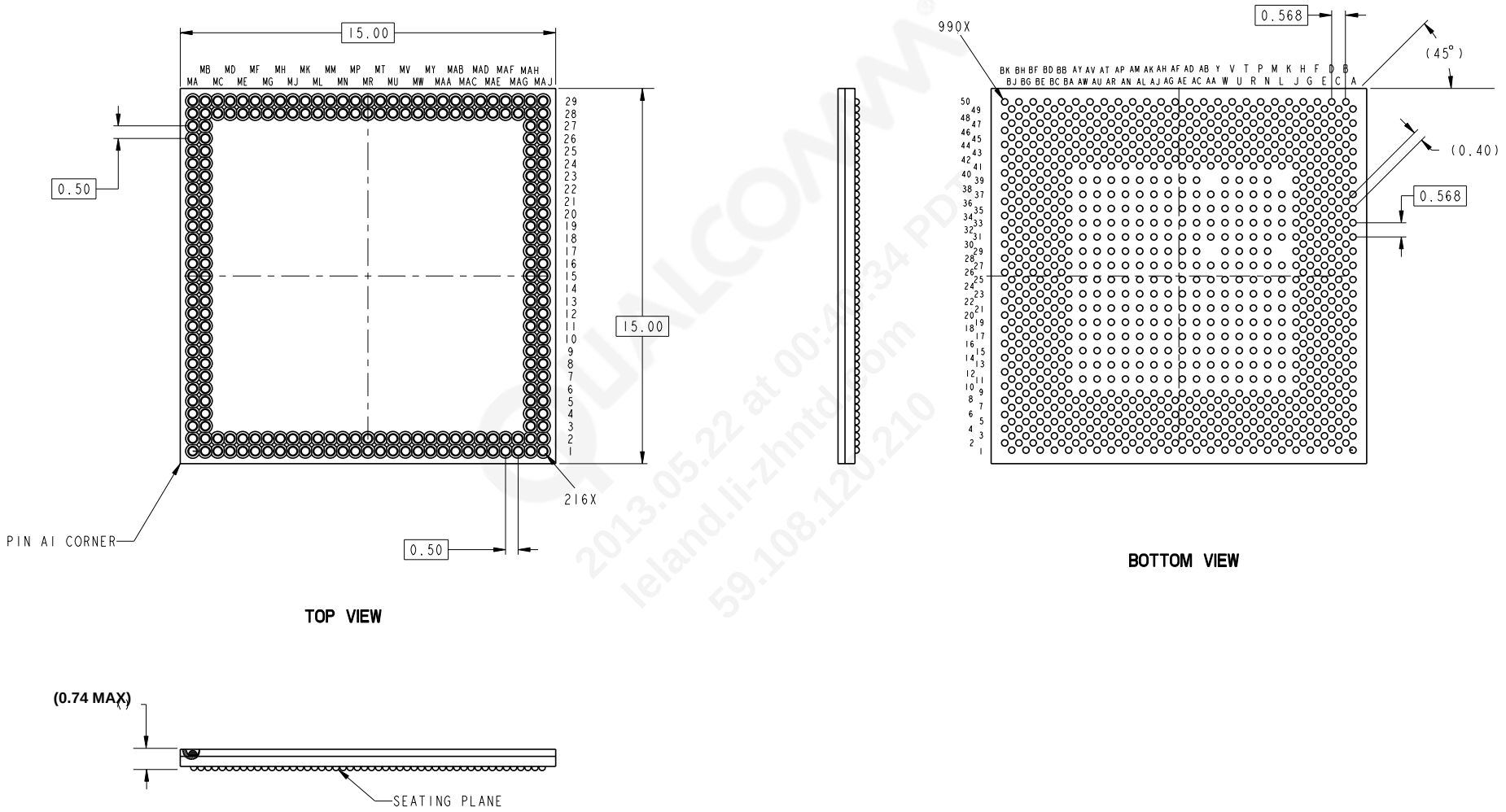


Figure 4-2 990B PNSP (15 × 15 × 0.74 mm) outline drawing1

NOTE This is a simplified outline drawing. Click the link below to download the complete, up-to-date package outline drawing:

https://downloads.cdmatech.com/qdc/drl/objectId/0901001481dc5767

4.2 Part marking

4.2.1 Specification compliant devices

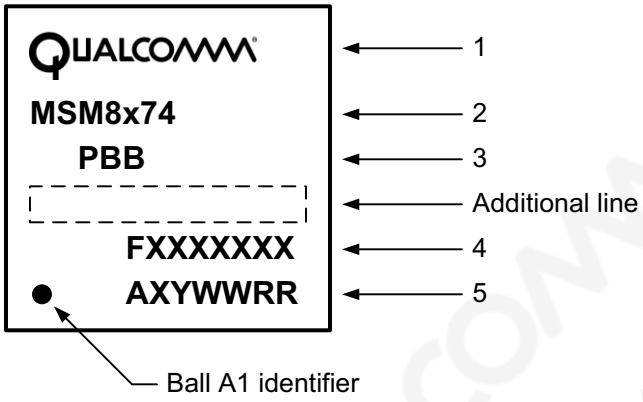


Figure 4-3 MSM8x74 device marking (top view, not to scale)

Table 4-1 MSM8x74 device marking line definitions

Line	Marking	Description
1	QUALCOMM	Qualcomm name or logo
2	MSM8X74	Qualcomm product name ■ X = 2, 6, or 9 (see Section 1.2.1 for differences)
3	PBB	P = product configuration code ■ See Table 4-2 for assigned values BB = feature code ■ See Table 4-2 for assigned values
An additional line may appear on the part marking for some samples; this is manufacturing information that is only relevant to Qualcomm and Qualcomm suppliers.		
4	FXXXXXXX	F = supply source code ■ F = A (for TSMC) XXXXXXX = traceability number
5	AXYWWRR	A = assembly site code ■ A = C (for Amkor K4) ■ A = K (for SPIL) ■ A = H (for SCK) X = traceability number Y = single-digit year WW = work week (based on calendar year) RR = product revision – refer to Table 4-2

NOTE For complete marking definitions of all MSM8x74 variants and revisions, refer to the *MSM8x74 Device Revision Guide* (80-NA437-4).

4.2.2 Daisy chain devices

This information will be included in future revisions of this document.

4.3 Device ordering information

4.3.1 Specification compliant devices

This device can be ordered using the identification code shown in Figure 4-4 and explained below.

Device ID code ►	AAA-AAAA	— P	— CCC	DDDDD	— EE	— RR	— S	— BB
Symbol definition ►	Product name	Config code	Number of pins	Package type	Shipping package	Product version	Source code	Feature code
Example ►	MSM-8974	— 0	— 990	PNSP	— TR	— 00	— 0	— VV
Example ►	MSM-8974	— 0	— 990	BPNSP	— TR	— 00	— 0	— VV
Example ►	MSM-8974	— 1	— 990	BPNSP	— TR	— 04	— 0	— VV

Feature code (BB) may not be included when identifying older devices.

Figure 4-4 Device identification code

Device ordering information details for all samples available to date are summarized in Table 4-2.

Table 4-2 Device identification code/ordering information details

Device	Product configuration code (P)	Product revision (RR)	Hardware revision #	Sample type	S value [1]	BB value [2]	Comments
MSM8974	0	01	0x1 07B0 0E1	ES 1.0	0	VV	2 GHz Quad Krait, LTE CAT4, DC-HSPA+ , DOrB, TD-SCDMA, without HDCP

Table 4-2 Device identification code/ordering information details

Device	Product configuration code (P)	Product revision (RR)	Hardware revision #	Sample type	S value [1]	BB value [2]	Comments
MSM8974	0	02	0x2 07B0 0E1	ES1.1	0	VV	2 GHz Quad Krait, MLP, LTE CAT4, DC-HSPA+ , DOrB, TD-SCDMA, without HDCP
	1	02	0x2 07B0 0E1	ES1.1	0	VV	2 GHz Quad Krait, MLP, LTE CAT4, DC-HSPA+ , DOrB, TD-SCDMA, with HDCP
	0	02	0x2 07B0 0E1	ES1.1	0	VV	2 GHz Quad Krait, BDP, LTE CAT4, DC-HSPA+ , DOrB, TD-SCDMA, without HDCP
	1	02	0x2 07B0 0E1	ES1.1	0	VV	2 GHz Quad Krait, BDP, LTE CAT4, DC-HSPA+ , DOrB, TD-SCDMA, with HDCP
MSM8974	0	03	0x4 07B0 0E1	ES2.0	0	VV	2 GHz Quad Krait, MLP, LTE CAT4 CA/DC-HSPA+ 42 Mbps/DORB/TD-SCDMA, without HDCP
	1	03	0x4 07B0 0E1	ES2.0	0	VV	2 GHz Quad Krait, MLP, LTE CAT4 CA/DC-HSPA+ 42 Mbps/DORB/ TD-SCDMA, with HDCP
	0	03	0x4 07B0 0E1	ES2.0	0	VV	2 GHz Quad Krait, BDP, LTE CAT4 CA/DC-HSPA+ 42 Mbps/DORB/ TD-SCDMA, without HDCP
	1	03	0x4 07B0 0E1	ES2.0	0	VV	2 GHz Quad Krait, BDP, LTE CAT4 CA/DC-HSPA+ 42 Mbps/DORB/TD-SCDMA, with HDCP

Table 4-2 Device identification code/ordering information details

Device	Product configuration code (P)	Product revision (RR)	Hardware revision #	Sample type	S value [1]	BB value [2]	Comments
MSM8274	0	04	0x5 07B2 0E1	ES2.0.1	0	VV	2 GHz Quad Krait, MLP, DC-HSPA+ 42 Mbps/ TD-SCDMA, without HDCP
	1	04	0x5 07B2 0E1	ES2.0.1	0	VV	2 GHz Quad Krait, MLP, DC-HSPA+ 42 Mbps/ TD-SCDMA, with HDCP
	2	04	0x5 07B2 0E1	ES2.0.1	0	VV	2 GHz Quad Krait, MLP, HSPA+ 21 Mbps/ TD-SCDMA, without HDCP
	3	04	0x5 07B2 0E1	ES2.0.1	0	VV	2 GHz Quad Krait, MLP, HSPA+ 21 Mbps/ TD-SCDMA, with HDCP
	0	04	0x5 07B2 0E1	ES2.0.1	0	VV	2 GHz Quad Krait, BDP, DC-HSPA+ 42 Mbps/ TD-SCDMA, without HDCP
	1	04	0x5 07B2 0E1	ES2.0.1	0	VV	2 GHz Quad Krait, BDP, DC-HSPA+ 42 Mbps/ TD-SCDMA ,with HDCP
	2	04	0x5 07B2 0E1	ES2.0.1	0	VV	2 GHz Quad Krait, BDP, DC-HSPA+ 21 Mbps/ TD-SCDMA, without HDCP
	3	04	0x5 07B2 0E1	ES2.0.1	0	VV	2 GHz Quad Krait, BDP, DC-HSPA+ 21 Mbps/ TD-SCDMA, with HDCP
MSM8674	0	04	0x5 07B1 0E1	ES2.0.1	0	VV	2 GHz Quad Krait, MLP, HSPA+ 21 Mbps/DORB, without HDCP
	1	04	0x5 07B1 0E1	ES2.0.1	0	VV	2 GHz Quad Krait, MLP, HSPA+ 21 Mbps/DORB, with HDCP
	0	04	0x5 07B1 0E1	ES2.0.1	0	VV	2 GHz Quad Krait, BDP, HSPA+ 21 Mbps/DORB, without HDCP
	1	04	0x5 07B1 0E1	ES2.0.1	0	VV	2 GHz Quad Krait, BDP, HSPA+ 21 Mbps/DORB, with HDCP

Table 4-2 Device identification code/ordering information details

Device	Product configuration code (P)	Product revision (RR)	Hardware revision #	Sample type	S value [1]	BB value [2]	Comments
MSM8974	0	04	0x5 07B0 0E1	ES2.0.1	0	VV	2 GHz Quad Krait,BDP,LTE CAT4CA/DC-HSPA+42MBPS/DORB/TD-SCDMA ,W/O HDCP
	1	04	0x5 07B0 0E1	ES2.0.1	0	VV	2 GHz Quad Krait,MLP,LTE CAT4CA/DC-HSPA+42MBPS/DORB/TD-SCDMA,W/HDCP
	6	04	0x5 07B0 0E1	ES2.0.1	0	VV	2 GHz Quad Krait,MLP, LTE CAT4 CA/DC-HSPA+ 42MBPS/TD-SCDMA , W/O HDCP
	7	04	0x5 07B0 0E1	ES2.0.1	0	VV	2 GHz Quad Krait,MLP, LTE CAT4 CA/DC-HSPA+ 42MBPS/TD-SCDMA , W/HDCP
	4	04	0x5 07B0 0E1	ES2.0.1	0	VV	2 GHz Quad Krait,MLP,LTE CAT4 NON CA/DC-HSPA+42MBPS/DORB/TD-SCDMA,W/OHDCP
	0	04	0x5 07B0 0E1	ES2.0.1	0	VV	2 GHz Quad Krait,BDP,LTE CAT4CA/DC-HSPA+42MBPS/DORB/TD-SCDMA ,W/O HDCP
	1	04	0x5 07B0 0E1	ES2.0.1	0	VV	2 GHz Quad Krait,BDP,LTE CAT4 CA/DC-HSPA+42MBPS/DORB/TD-SCDMA ,W/HDCP
	6	04	0x5 07B0 0E1	ES2.0.1	0	VV	2 GHz Quad Krait,BDP,LTE CAT4,CA/DC-HSPA+42MBPS/TD-SCDMA,,W/OHDCP

Table 4-2 Device identification code/ordering information details

Device	Product configuration code (P)	Product revision (RR)	Hardware revision #	Sample type	S value [1]	BB value [2]	Comments
MSM8974 (cont.)	7	04	0x5 07B0 0E1	ES2.0.1	0	VV	2 GHz Quad Krait,BDP,LTE CAT4,CA/DC-HSPA+42MBPS/TD-SCDMA, W/HDCP
	4	04	0x5 07B0 0E1	ES2.0.1	0	VV	2 GHz Quad Krait,BDP,LTE CAT4 NONCA/DC-HSPA+42MBPS/DORB/TD-SCDMA,W/OHDCP
	5	04	0x5 07B0 0E1	ES2.0.1	0	VV	2 GHz Quad Krait,BDP,LTE CAT4 NON CA/DC-HSPA+42MBPS/DORB/TD-SCDMA,W/HDCP
	8	04	0x5 07B0 0E1	ES2.0.1	0	VV	2 GHz Quad Krait,BDP,LTE CAT4 NON-CA/DC-HSPA+ 42MBPS/TD-SCDMA, W/OHDCP
	9	04	0x5 07B0 0E1	ES2.0.1	0	VV	2 GHz Quad Krait,BDP,LTE CAT4 NON CA/DC-HSPA+42MBPS/TD-SCDMA, W/HDCP
MSM8274	0	05	0x6 07B2 0E1	ES2.1	0	VV	2.2 GHz Quad Krait,BDP,DC-HSPA+42MBPS/TD-SCDMA W/O HDCP
	1	05	0x6 07B2 0E1	ES2.1	0	VV	2.2 GHz Quad Krait,BDP,DC-HSPA+42MBPS/TD-SCDMA W/HDCP
	2	05	0x6 07B2 0E1	ES2.1	0	VV	2.2 GHz Quad Krait,BDP,HSPA+21MBPS/TD-SCDMA W/O HDCP
	3	05	0x6 07B2 0E1	ES2.1	0	VV	2.2 GHz Quad Krait,BDP,HSPA+21MBPS/TD-SCDMA W/HDCP
MSM8674	0	05	0x6 07B1 0E1	ES2.1	0	VV	2.2 GHz Quad Krait,BDP,HSPA+21MBPS/DORB W/O HDCP
	1	05	0x6 07B1 0E1	ES2.1	0	VV	2.2 GHz Quad Krait,BDP,HSPA+21MBPS/DORB W/ HDCP

Table 4-2 Device identification code/ordering information details

Device	Product configuration code (P)	Product revision (RR)	Hardware revision #	Sample type	S value [1]	BB value [2]	Comments
MSM8974	0	05	0x6 07B0 0E1	ES2.1	0	VV	2.2 GHz Quad Krait,MLP,LTE CAT4 CA/DC-HSPA+42MBPS/DORB/TD-SCDMA W/O HDCP
	4	05	0x6 07B0 0E1	ES2.1	0	VV	2.2 GHz Quad Krait,MLP,LTE CAT4 NON CA/DC-HSPA+42MBPS/DORB/TD-SCDMA W/O HDCP,
	8	05	0x6 07B0 0E1	ES2.1	0	VV	2.2 GHz Quad Krait,MLP,LTE CAT4 NON CA/DC-HSPA+42MBPS/TD-SCDMA W/O HDCP
	9	05	0x6 07B0 0E1	ES2.1	0	VV	2.2 GHz Quad Krait,MLP,LTE CAT4 NON CA/DC-HSPA+42MBPS/TD-SCDMA W/HDCP
	0	05	0x6 07B0 0E1	ES2.1	0	VV	2.2 GHz Quad Krait,BDP,LTE CAT4 CA/DC-HSPA+42MBPS/DORB/TD-SCDMA W/OHDCP
	1	05	0x6 07B0 0E1	ES2.1	0	VV	2.2 GHz Quad Krait,BDP,LTE CAT4 CA/DC-HSPA+42MBPS/DORB/TD-SCDMA W/HDCP
	4	05	0x6 07B0 0E1	ES2.1	0	VV	2.2 GHz Quad Krait,BDP,LTE CAT4 NON CA/DC-HSPA+42MBPS/DORB/TD-SCDMA W/OHDCP
	5	05	0x6 07B0 0E1	ES2.1	0	VV	2.2 GHz Quad Krait,BDP,LTE CAT4 NON CA/DC-HSPA+42MBPS/DORB/TD-SCDMA W/HDCP,
	6	05	0x6 07B0 0E1	ES2.1	0	VV	2.2 GHz Quad Krait,BDP,LTE CAT4 CA/DC-HSPA+42MBPS/TD-SCDMA W/OHDCP
	7	05	0x6 07B0 0E1	ES2.1	0	VV	2.2 GHz Quad Krait,BDP,LTE CAT4 CA/DC-HSPA+42MBPS/TD-SCDMA W/HDCP

Table 4-2 Device identification code/ordering information details

Device	Product configuration code (P)	Product revision (RR)	Hardware revision #	Sample type	S value [1]	BB value [2]	Comments
MSM8974 (cont.)	8	05	0x6 07B0 0E1	ES2.1	0	VV	2.2 GHz Quad Krait,BDP,LTE CAT4 NON-CA/DC-HSPA+ 42MBPS/TD-SCDMA W/OHDCP
	9	05	0x6 07B0 0E1	ES2.1	0	VV	2.2 GHz Quad Krait,BDP,LTE CAT4 NON CA/DC-HSPA+42MBPS/TD-SCDMA W/HDCP

1. 'S' is the source configuration code that identifies all the qualified die fabrication source combinations available at the time a particular sample type were shipped.
2. 'BB' is the feature code that identifies an IC's specific feature set that distinguishes it from other versions or variants. Defined feature sets available at the time of this document's release are:
   – VV = null set; all devices available at this time have the same feature set.

4.3.2 Daisy chain devices

This information will be included in future revisions of this document.

4.4 Device moisture-sensitivity level

Plastic-encapsulated surface mount packages are susceptible to damage induced by absorbed moisture and high temperature. A package's moisture-sensitivity level (MSL) indicates its ability to withstand exposure after it is removed from its shipment bag, while it's on the factory floor awaiting PCB installation. A low MSL rating is better than a high rating; a low MSL device can be exposed on the factory floor longer than a high MSL device. All pertinent MSL ratings are summarized in Table 4-3.

Table 4-3 MSL ratings summary

MSL	Out-of-bag floor life	Comments
1	Unlimited	≤ 30°C / 85% RH
2	1 year	≤ 30°C / 60% RH
2a	4 weeks	≤ 30°C / 60% RH
3	168 hours	≤ 30°C / 60% RH; **MSM8x74 rating**
4	72 hours	≤ 30°C / 60% RH
5	48 hours	≤ 30°C / 60% RH
5a	24 hours	≤ 30°C / 60% RH
6	Mandatory bake before use. After bake, must be reflowed within the time limit specified on the label.	≤ 30°C / 60% RH

Qualcomm follows the latest IPC/JEDEC J-STD-020 standard revision for moisture-sensitivity qualification. ***The MSM8x74 devices are classified as MSL3; the qualification temperature was 255ºC.*** This qualification temperature (255°C) should not be confused with the peak temperature within the recommended solder reflow profile (see Section 6.2.4 for further discussion).

4.5 Thermal characteristics

Rather than provide thermal resistance values θ_{JC} and θ_{JA}, validated thermal package models are provided through Qualcomm's documents and download web site. A thermal model for each device is provided within the "Power_Thermal" subfolder for each chipset family. Designers can extract thermal resistance values by conducting their own thermal simulations.

NOTE Click the link below to download the MSM8x74 thermal package model from the CDMA Tech Support website.

This link will be included in future revisions of this document.

If you have permission to view the document, a prompt will be presented for initiating the download.

NOTE Subscribe to the MSM8x74 thermal package model to be notified of any changes.

Click the **Help** button to download the latest version of the *Using CDMATech Support Documents and Downloads User Guide* (80-V7273-1). This document includes subscription instructions.

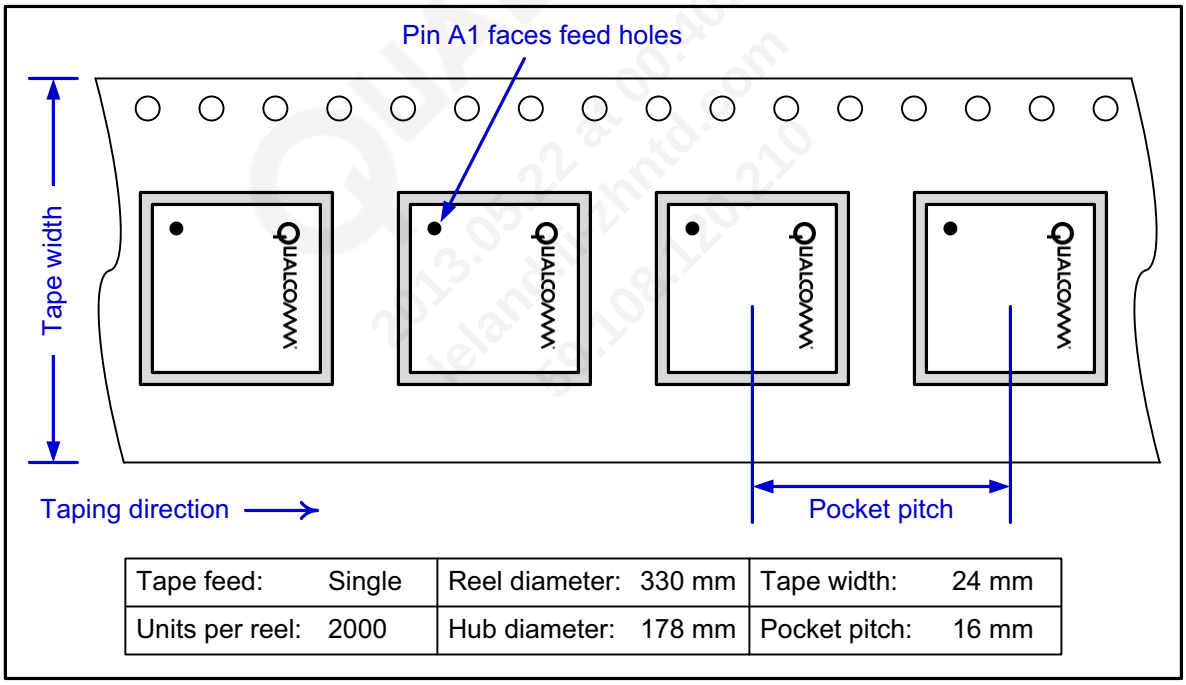
5 Carrier, Storage, & Handling Information

5.1 Carrier

5.1.1 Tape and reel information

All Qualcomm carrier tape systems conform to EIA-481 standards.

A simplified sketch of the MSM8x74 tape carrier is shown in Figure 5-1, including the proper part orientation, maximum number of devices per reel, and key dimensions.



Tape feed:	Single	Reel diameter:	330 mm	Tape width:	24 mm
Units per reel:	2000	Hub diameter:	178 mm	Pocket pitch:	16 mm

Figure 5-1 Carrier tape drawing with part orientation

Tape-handling recommendations are shown in Figure 5-2.

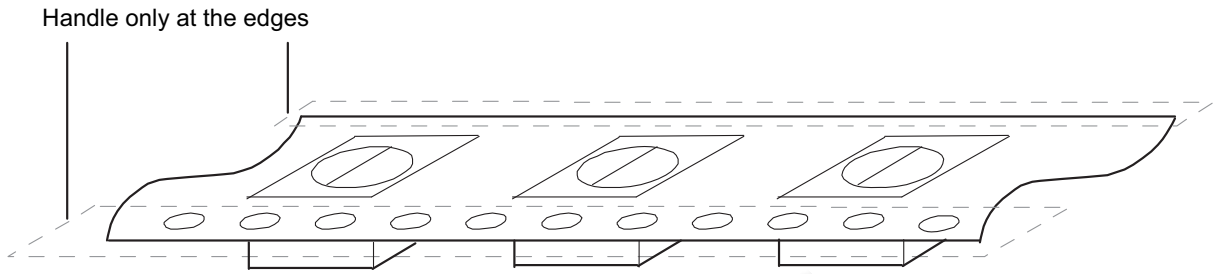


Figure 5-2 Tape handling

5.2 Storage

5.2.1 Bagged storage conditions

MSM8x74 devices delivered in tape and reel carriers must be stored in sealed, moisture barrier, anti-static bags. Refer to the *IC Packing Methods and Materials Specification* (80-VK055-1) for the expected shelf life.

5.2.2 Out-of-bag duration

The out-of-bag duration is the time a device can be on the factory floor before being installed onto a PCB. It is defined by the device MSL rating as discussed in Section 4.4.

5.3 Handling

Tape handling was discussed in Section 5.1.1. Other (IC-specific) handling guidelines are presented below.

5.3.1 Baking

It is **not necessary** to bake the MSM8x74 if the conditions specified in Section 5.2.1 and Section 5.2.2 have **not been exceeded**.

It is **necessary** to bake the MSM8x74 if any condition specified in Section 5.2.1 or Section 5.2.2 has **been exceeded**. The baking conditions are specified on the moisture-sensitive caution label attached to each bag; see the *IC Packing Methods and Materials Specification* (80-VK055-1) for details.

CAUTION If baking is required, the devices must be transferred into trays that can be baked to at least 125°C. Devices should not be baked in tape and reel carriers at any temperature.

5.3.2 Electrostatic discharge

Electrostatic discharge (ESD) occurs naturally in laboratory and factory environments. An established high-voltage potential is always at risk of discharging to a lower potential. If this discharge path is through a semiconductor device, destructive damage may result.

ESD countermeasures and handling methods must be developed and used to control the factory environment at each manufacturing site.

Qualcomm products must be handled according to the ESD Association standard: ANSI/ESD S20.20-1999, *Protection of Electrical and Electronic Parts, Assemblies, and Equipment*.

Refer to Section 7.1 for the MSM8x74 device ESD ratings.

5.4 Barcode label and packing for shipment

Refer to the *IC Packing Methods and Materials Specification* (80-VK055-1) for all packing-related information, including barcode-label details.

6 PCB Mounting Guidelines

6.1 RoHS compliance

The device is lead-free and RoHS-compliant. Its SnAgCu solder balls use SAC305 composition on the top and SAC125/Ni on the bottom. Qualcomm defines its lead-free (or Pb-free) semiconductor products as having a maximum lead concentration of 1000 ppm (0.1% by weight) in raw (homogeneous) materials and end products. Qualcomm package environmental programs, RoHS compliance details, and tables defining pertinent characteristics of all Qualcomm IC products are described in the *IC Package Environmental Roadmap* (80-V6921-1).

6.2 SMT parameters

This section describes Qualcomm board-level characterization process parameters. It is included to assist customers with their SMT process development; it is not intended to be a specification for their SMT processes.

6.2.1 Land pad and stencil design

The land pattern and stencil recommendations presented in this section are based upon Qualcomm internal characterizations for lead-free solder pastes on an eight layer PCB built primarily to the specifications described in JEDEC JESD22-B111.

Qualcomm recommends characterizing the land patterns according to each customer's processes, materials, equipment, stencil design, and reflow profile prior to PCB production. Optimizing the solder stencil pattern design and print process is critical to ensure print uniformity, decrease voiding, and increase board-level reliability.

General land pattern guidelines:

- Non-solder-mask-defined (NSMD) pads provide the best reliability.
- Keep the solderable area consistent for each pad, especially when mixing via-in-pad and non-via-in-pad in the same array.
- Avoid large solder mask openings over ground planes.
- Traces for external routing are recommended to be less than or equal to half the pad diameter to ensure consistent solder joint shapes.

One key parameter that should be evaluated is the ratio of aperture area to sidewall area, known as the area ratio (AR). Qualcomm recommends square apertures for optimal solder paste release. In this case, a simple equation can be used relating the side length of the aperture to the stencil thickness (as illustrated and explained in Figure 6-1). Larger area ratios enable better transfer of solder paste to the PCB, minimize defects, and ensure a more stable printing process. Inter-aperture spacing should be at least as thick as the stencil, otherwise paste deposits may bridge.

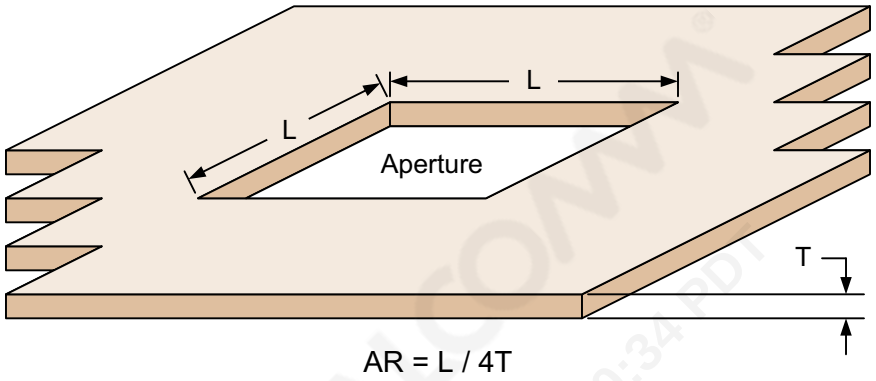


Figure 6-1 Stencil printing aperture AR

Guidelines for an acceptable relationship between L and T are listed below and illustrated in Figure 6-2:

- R = L/4T > 0.65 – best
- 0.60 ≤ R ≤ 0.65 – acceptable
- R < 0.60 – not acceptable

Stencil Aperture L (µm)	Stencil thickness, T (µm)							
	75	80	85	90	95	100	105	110
210	0.70	0.66	0.62	0.58	0.55	0.53	0.50	0.48
220	0.73	0.69	0.65	0.61	0.58	0.55	0.52	0.50
230	0.77	0.72	0.68	0.64	0.61	0.58	0.55	0.52
240	0.80	0.75	0.71	0.67	0.63	0.60	0.57	0.55
250	0.83	0.78	0.74	0.69	0.66	0.63	0..60	0.57
260	0.87	0.81	0.76	0.72	0.68	0.65	0.62	0.59

Figure 6-2 Acceptable solder paste geometries

Qualcomm provides an example PCB land pattern and stencil design for the 990-PNSP package.

NOTE Click the link below to download the 990-PNSP land/stencil drawing (LS90-N9094-1) from the CDMATech Support Website.

https://downloads.cdmatech.com/qdc/drl/objectId/090100148192b08d

If you have permission to view the document, a prompt will be presented for initiating the download.

NOTE Click the link below to download the 990B-PNSP land/stencil drawing (LS90-NC165-1) from the CDMATech Support Website.

https://downloads.cdmatech.com/qdc/drl/objectId/0901001481d6bc59

If you have permission to view the document, a prompt will be presented for initiating the download.

NOTE Subscribe to the land/stencil drawing to be notified of any changes.

Click the **Help** button to download the latest version of the *Using CDMATech Support Documents and Downloads User Guide* (80-V7273-1). This document includes subscription instructions.

6.2.2 Stacked package dip process

The MSM8x74 chipset is a PoP device that requires the memory package to be assembled using a paste or flux dip process; based upon internal development results, the dip flux process is recommended. For a MLP production assembly, the single-pass reflow is preferred over the pre-stacking the devices. For a BDP production assembly, pre-stacking the devices is preferred. The flux film depth should be adjusted to achieve a target thickness at least 50% of the solder ball height (Figure 6-3). The film thickness should be set based upon empirical measurement and not machine setpoints. Qualcomm internal characterizations were performed using a flux film thickness of 150 microns. Review the *MSM8274/MSM8674/MSM8974 Package-on-package Guide* (80-NA437-54) for more detailed information.

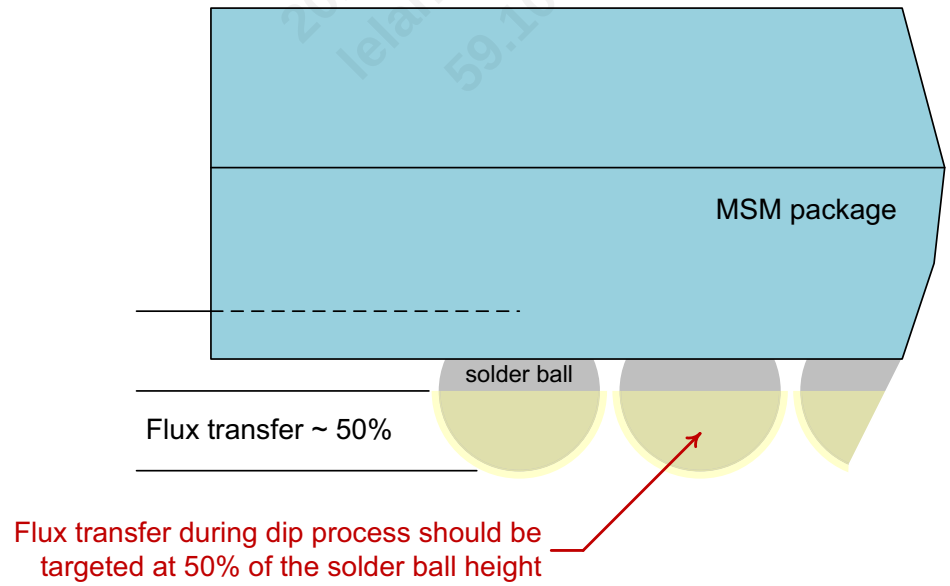


Figure 6-3 Flux transfer during dip process

6.2.3 Reflow profile

Reflow profile conditions typically used by Qualcomm for lead-free systems are listed in Table 6-1 and illustrated in Figure 6-4.

Table 6-1 Qualcomm typical SMT reflow profile conditions (for reference only)

Profile stage	Description	Temp range	Condition
Preheat	Initial ramp	< 150°C	3°C/sec max
Soak	Flux activation	150 to 190°C	60 to 75 sec
Ramp	Transition to liquidus (solder paste melting point)	190 to 220°C	< 30 sec
Reflow	Time above liquidus	220 to 245°C [1]	50 to 70 sec
Cool down	Cool rate – ramp to ambient	< 220°C	6°C/sec max

1. During the reflow process, the recommended peak temperature is 245°C (minimum). This temperature should not be confused with the peak temperature reached during MSL testing as discussed in Section 6.2.4.

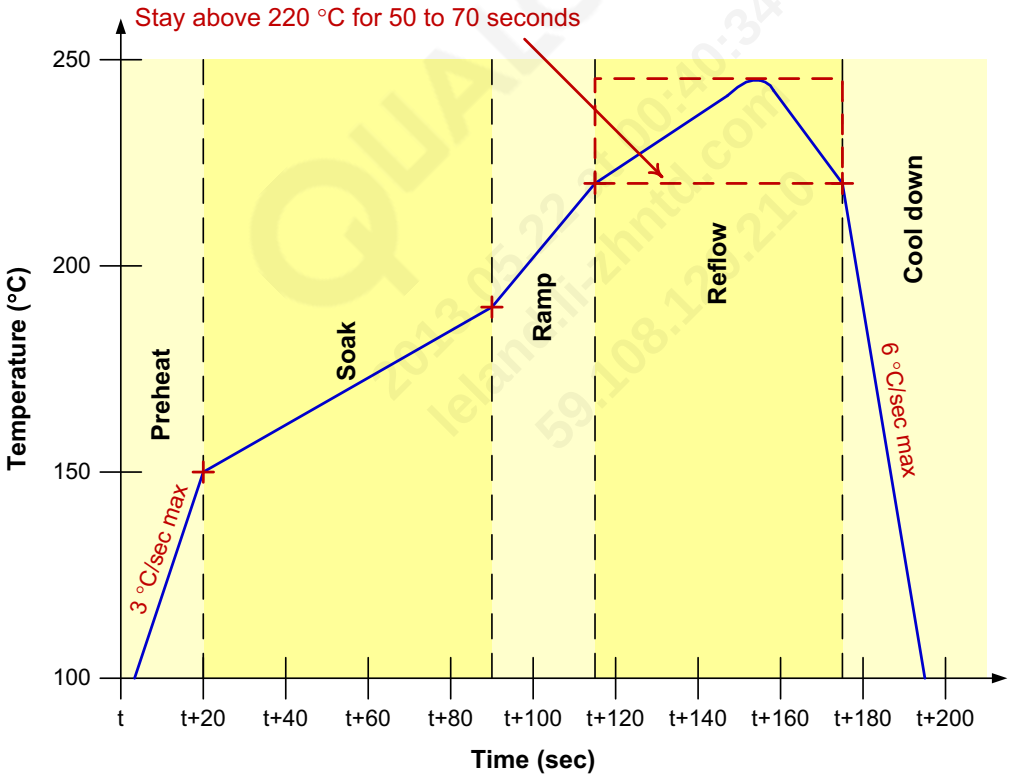


Figure 6-4 Qualcomm typical SMT reflow profile

6.2.4 SMT peak package body temperature

This document states a peak package body temperature in three other places within this document, and without explanation they may appear to conflict. The three places are listed below, along with an explanation of the stated value and its meaning within that section's context.

1. Section 4.4 – *Device moisture-sensitivity level*

   MSM8x74 devices are classified as MSL3@255°C. The temperature (255°C) included in this designation is the lower limit of the range stated for moisture resistance testing during the device qualification process as explained in #2 below.

2. Section 7.1 – *Reliability qualifications summary*

   One of the tests conducted for device qualification is the moisture resistance test. Qualcomm follows J-STD-020-C, and hits a peak reflow temperature that falls within the range of 260°C +0/-5°C (255°C to 260°C).

3. Section 6.2.2 – *Reflow profile*

   During a production board's reflow process, the temperature seen by the package must be controlled. Obviously the temperature must be high enough to melt the solder and provide reliable connections, but it must not go so high that the device might be damaged. The recommended peak temperature during production assembly is 245°C. This is comfortably above the solder melting point (220°C), yet well below the proven temperature reached during qualification (255°C or more).

6.2.5 SMT process verification

Qualcomm recommends verification of the SMT process prior to high-volume board assembly, including:

- In-line solder paste deposition monitoring
- Reflow profile measurement and verification
- Visual and x-ray inspection after soldering to confirm adequate alignment, solder voids, solder ball shape, and solder bridging
- Cross-section inspection of solder joints for wetting, solder ball shape, and voiding

6.3 Daisy-chain components

Daisy-chain packages use the same processes and materials as actual products; they are recommended for SMT characterization and board-level reliability testing. In fact, all SMT process recommendations discussed above can be performed using daisy-chain components.

Ordering information is given in Section 4.3.2.

Daisy-chain PCB routing recommendations are available for download.

NOTE Click the link below to download the 990-PNSP daisy chain interconnect drawing (DS90-N9094-1) from the CDMATech Support Website.

https://downloads.cdmatech.com/qdc/drl/objectId/0901001481900481

If you have permission to view the document, a prompt will be presented for initiating the download.

NOTE Click the link below to download the 990B-PNSP daisy chain interconnect drawing (DS90-NC165-1) from the CDMATech Support Website.

https://downloads.cdmatech.com/qdc/drl/objectId/0901001481e64260

If you have permission to view the document, a prompt will be presented for initiating the download.

NOTE Subscribe to the daisy-chain interconnect drawing to be notified of any changes.

Click the **Help** button to download the latest version of *Using CDMATech Support Documents and Downloads User Guide* (80-V7273-1). This document includes subscription instructions.

6.4 Board-level reliability

Qualcomm conducts characterization tests to assess the device's board-level reliability, including the following physical tests on evaluation boards:

- Drop shock (JESD22-B111)
- Temperature cycling (JESD22-A104)
- Cyclic bend testing – optional (JESD22-B113)

Board-level reliability data is available for download.

NOTE Click the link below to download the 990-PNSP board-level reliability data from the CDMATech Support Website.

This link will be included in future revisions of this document.

If you have permission to view the document, a prompt will be presented for initiating the download.

NOTE Subscribe to the board-level reliability document to be notified of any changes.

Click the **Help** button to download the latest version of *Using CDMATech Support Documents and Downloads User Guide* (80-V7273-1). This document includes subscription instructions.

6.5 High temperature warpage

Qualcomm measures high temperature warpage using a shadow moire system; the measured data is available for download.

NOTE Click the link below to download the 990-PNSP high temperature warpage data from the CDMATech Support Website.

This link will be included in future revisions of this document.

If you have permission to view the document, a prompt will be presented for initiating the download.

NOTE Subscribe to the high temperature warpage document to be notified of any changes.

Click the **Help** button to download the latest version of *Using CDMATech Support Documents and Downloads User Guide* (80-V7273-1). This document includes subscription instructions.

7 Part Reliability

7.1 Reliability qualifications summary

Table 7-1 Silicon reliability results

Tests, standards, and conditions	Sample size	Results
DPPM rate (ELFR) and average failure rate (AFR) in FIT (λ) failure in billion device-hours HTOL: JESD22-A108-A Use condition: Temperature: 85°C, voltage: 1.05 V (Total samples from see-through different wafer lots)	TBD	TBD
Mean time to failure (MTTF) t = 1/λ in million hours (Total samples from see-through different wafer lots)	TBD	TBD
ESD – HBM rating JESD22-A114-F, target: 2000 V (Total samples from one wafer lot)	Rev1.1 – 0F/3 Rev2.0 – 0F/3	Pass 2000 V Pass 2000 V
ESD – CDM rating JESD22-C101-D, target: 500 V (Total samples from one wafer lot)	Rev1.1 – 0F/3 Rev2.0 – 0F/3	Pass 500 V Pass 500 V
Latch-up (I-test): EIA/JESD78A Trigger current: ±100 mA; temperature: 85°C (Total samples from one wafer lot)	Rev1.1 – 0/6 Rev2.0 – 0/6	Pass Pass
Latch-up (Vsupply overvoltage): EIA/JESD78A Trigger voltage: Each VDD pin, stress at 1.5 × Vdd maximum per device specification; temperature: 85°C (Total samples from one wafer lot)	Rev1.1 – 0/6 Rev2.0 – 0/6	Pass Pass

Table 7-2 BDP (bare die pop) package reliability results

Tests, standards, and conditions	ATK assembly	SCK assembly	SPIL assembly	Results
MRT: J-STD-020 Reflow at 260°C+0/-5°C	779	768	790	Pass
Temperature cycle: JESD22-A104-D Temperature: -55°C to 125°C; number of cycles: 1000 Soak time at minimum/maximum temperature: 8–10 minutes Cycle rate: 2 cycles per hour (CPH) Preconditioning: JESD22-A113-F MSL 3, reflow temperature: 260°C+0/-5°C	TBD	TBD	TBD	
Unbiased highly accelerated stress test: JESD22-A118 130°C/85% RH and 96 hours duration Preconditioning: JESD22-A113-F MSL 3, reflow temperature: 260°C+0/-5°C	180	264	180	Pass
Biased highly accelerated stress test: JESD22-A110 130°C/85% RH and 96 hours duration Preconditioning: JESD22-A113-F MSL 3, reflow temperature: 260°C+0/-5°C	TBD	TBD	TBD	
High-temperature storage life: JESD22-A103-C Temperature 150°C, 500, 1000 hours	TBD	TBD	TBD	
Flammability UL-STD-94 UL-STD-94 Note: Flammability test – not required UL-STD-94 Qualcomm ICs are exempt from the flammability requirements due to their sizes per UL/EN 60950-1, as long as they are mounted on materials rated V-1 or better. Most PWBs onto which our ICs mounted are rated V-0 (better than V-1).	N/A	N/A	N/A	See note under test column
Physical dimensions: JESD22-B100-A Case outline drawing: Qualcomm internal document	TBD	TBD	TBD	
Solder ball shear: JESD22-B117	TBD	TBD	TBD	
Internal/external visual	TBD	TBD	TBD	

Table 7-3 MLP package reliability results

Tests, standards, and conditions	ATK assembly	SCK assembly	SPIL assembly	Results
MRT: J-STD-020 Reflow at 260°C+0/-5°C	TBD	TBD	TBD	
Temperature cycle: JESD22-A104-D Temperature: -55°C to 125°C; number of cycles: 1000 Soak time at minimum/maximum temperature: 8–10 minutes Cycle rate: 2 cycles per hour (CPH) Preconditioning: JESD22-A113-F MSL 3, reflow temperature: 260°C+0/-5°C	TBD	TBD	TBD	
Unbiased highly accelerated stress test: JESD22-A118 130°C/85% RH and 96 hours duration Preconditioning: JESD22-A113-F MSL 3, reflow temperature: 260°C+0/-5°C	TBD	TBD	TBD	
Biased highly accelerated stress test: JESD22-A110 130°C/85% RH and 96 hours duration Preconditioning: JESD22-A113-F MSL 3, reflow temperature: 260°C+0/-5°C	TBD	TBD	TBD	
High-temperature storage life: JESD22-A103-C Temperature 150°C, 500, 1000 hours	TBD	TBD	TBD	
Flammability UL-STD-94 UL-STD-94 Note: Flammability test – not required UL-STD-94 Qualcomm ICs are exempt from the flammability requirements due to their sizes per UL/EN 60950-1, as long as they are mounted on materials rated V-1 or better. Most PWBs onto which our ICs mounted are rated V-0 (better than V-1).	N/A	N/A	N/A	See note under test column
Physical dimensions: JESD22-B100-A Case outline drawing: Qualcomm internal document	TBD	TBD	TBD	
Solder ball shear: JESD22-B117	TBD	TBD	TBD	
Internal/external visual	TBD	TBD	TBD	

7.2 Qualification sample description

7.2.1 BDP device characteristics

Device name:	MSM8274, MSM8674, or MSM8974
Package type:	990B-PNSP
Package body size:	15 mm × 15 mm × 0.74 mm
Fab process:	28 nm CMOS
Fab sites:	TSMC
Assembly sites:	ATK, SCK, SPIL
Solder ball pitch:	0.4 mm

7.2.2 MLP device characteristics

Device name:	MSM8274, MSM8674, or MSM8974
Package type:	990-PNSP
Package body size:	15 mm × 15 mm × 0.91 mm
Fab process:	28 nm CMOS
Fab sites:	TSMC
Assembly sites:	ATK, SCK, SPIL
Solder ball pitch:	0.4 mm