Qualcomm
TECHNOLOGIES, INC

Application Note

Understanding High-Frequency and Fast-Transient Switched-Mode Power Supplies

80-VT310-124 Rev. A

September 16, 2014

Submit technical questions at:
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Revision history

Revision	Date	Description
A	September 2014	Initial release

1 Introduction

1.1 Switched-mode power supply circuits

Each Qualcomm Technologies, Inc. (QTI) power management IC (PMIC) includes multiple switched-mode power supply (SMPS) circuits. There are three major types of SMPS circuits: buck converters, boost converters, and buck-boost converters. This document addresses buck converters only.

A buck converter (Figure 1) is a highly efficient, high-current step-down switching regulator that generates programmable output voltages for high-speed, multi-processor, multi-voltage modem IC architectures. Two types of buck converter designs are used in QTI PMICs: high-frequency (HF-SMPS) and fast transient (FT-SMPS); each design-type is optimized for its intended applications and corresponding load requirements.

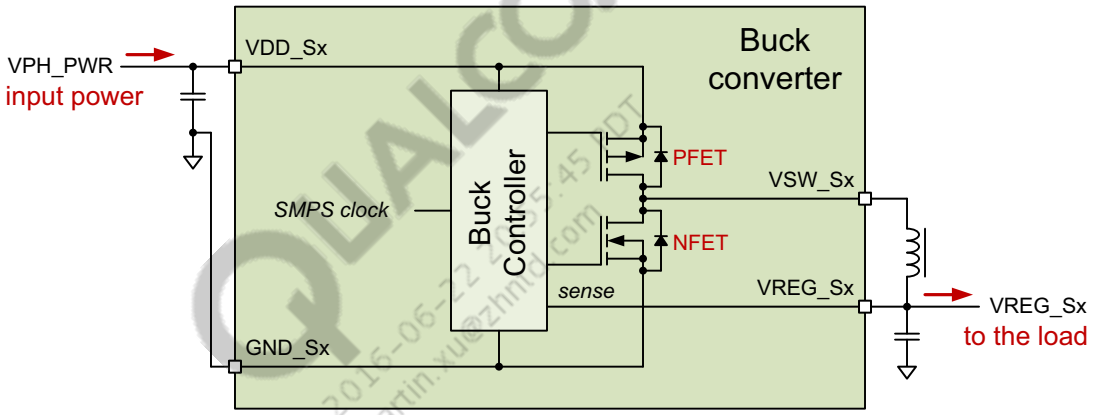

Figure 1 High-level buck converter block diagram

1.2 Scope of this document

This application note addresses questions that are most frequently asked during wireless product development and test. Its focus is HF-SMPS and FT-SMPS circuits' behavior and test methods. **The goal is to provide sufficiently detailed information to help readers understand HF and FT buck behavior without disclosing QTI-protected intellectual property.**

Other QTI documents provide design guidance; each PMIC is supported by a device specification, reference schematics, design guidelines/training slides, and layout guidelines documents. Readers are encouraged to study this document and each PMIC's design guidelines and layout guidelines documents before submitting cases or contacting QTI about their buck-related queries.

NOTE Except for the switch-nodes (VSW_Sx), which are taken with the full bandwidth, all waveform plots shown in this document have been taken with 20 MHz bandwidth oscilloscope setting.

1.3 Intended audience

Design and test engineers who are currently developing or troubleshooting wireless products that use a QTI PMIC.

2 HF-SMPS vs. FT-SMPS

The HF-SMPS is a robust and high-efficiency buck converter that is used to power sub-regulated PMIC LDOs, 1.8 V logic circuits, RFICs, and some of the external system loads.

On the other hand, the FT-SMPS has been designed for tight, high-resolution (5 mV) output voltage regulation, as well as an extremely fast transient response, making it a better choice for powering the application processor, modem, and graphic cores. Advantageous FT-SMPS features include:

- An advanced non-linear control system that can trigger 100% or 0% duty cycles (used when transient events are too fast for linear duty cycle control). This immediate 100% or 0% duty cycle response is followed by a smooth transition back into the linear control region.
- Multi-phase SMPS operation is supported to increase maximum current and improve transient performance.
- Remote sensing (differential feedback) allows the FT-SMPS to compensate for power delivery network (PDN) impedance variations and deliver the desired voltage level across the dynamic loads' terminals.

HF-SMPS and FT-SMPS characteristics are summarized in Table 1.

Table 1 HF-SMPS and FT-SMPS summary

Feature	HF-SMPS	FT-SMPS	Comments
Load capacitance	Local	Remote	HF-SMPS is sensitive to load capacitor placement
Remote sensing	No	Yes	
Relative layout complexity	Simple	Complex	FT-SMPS sense lines need good isolation from noise sources
Noise immunity	Robust	Sensitive	
Transient response	Fast	Very fast	
Output range	0.375 to 3.125 V	0.350 to 2.250 V	
Output resolution	12.5 and 25 mV	5 and 10 mV	
Multi-phase support	No	Yes	

NOTE While the FT-SMPS supports remote sensing, the HF-SMPS does not. Both local and remote sensing is shown in Figure 2. The HF-SMPS output capacitor must be placed close to the PMIC pins, input capacitor, and inductor. The HF control system uses the voltage drop between the switch-node (VSW_Sx) and the output capacitor (through the feedback point VREG_Sx) to estimate inductor current. Remote placement of the output capacitor adds resistance in series with the inductor DCR, which can introduce errors to the inductor current estimate.

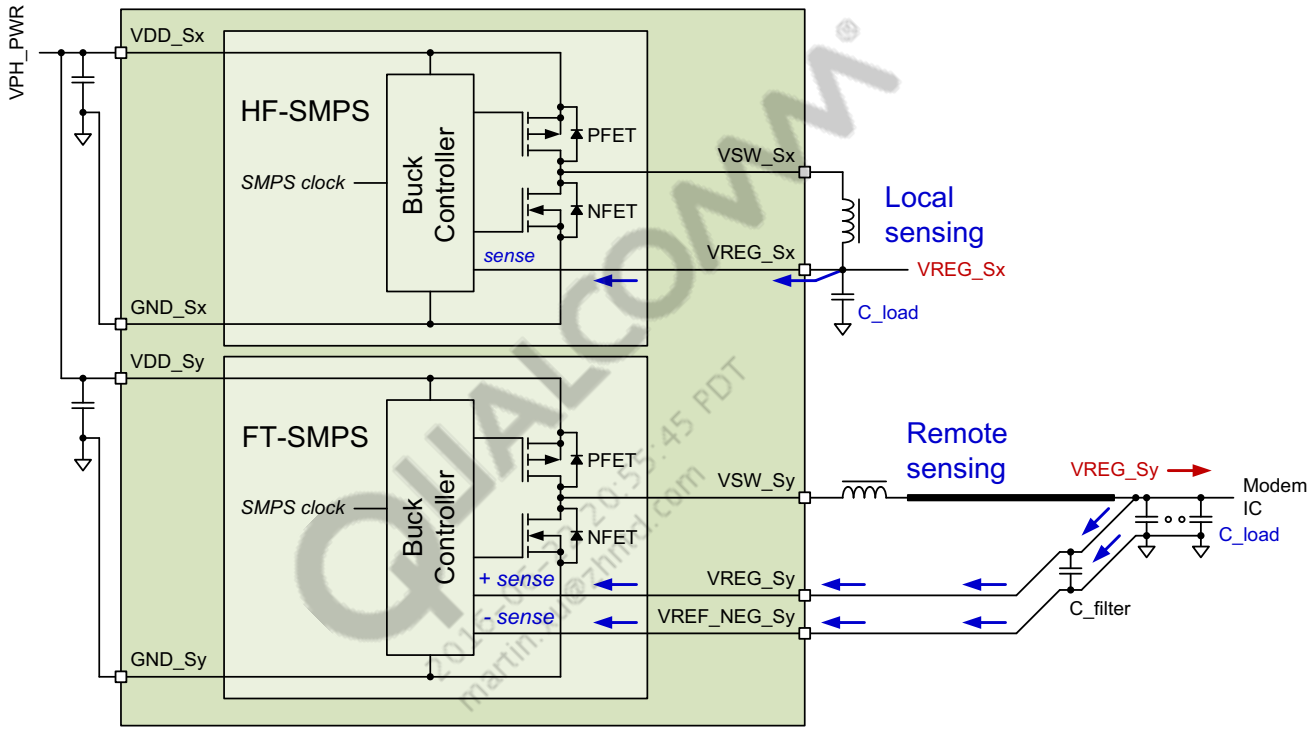

Figure 2 Local (HF-SMPS) and remote (FT-SMPS) sensing

3 Modes of Operation (With Example Waveforms)

Brief operating mode descriptions are provided, with illustrative example waveforms.

3.1 Pulse width modulation

During pulse width modulation (PWM) mode, which is used for medium- to high-range load currents, the switching frequency is constant. This frequency is chosen for optimum buck performance (transient response, ripple, efficiency, component selection/sizing, etc) over the range of PWM operation.

Depending upon the inductor current waveform during PWM operation, the buck can operate in either continuous conduction mode (CCM) or discontinuous conduction mode (DCM).

Typical switch-node voltage and inductor current waveforms are shown below:

- Figure 3 – CCM with Fsw = 2.13 MHz
  - Ch#1 = switch-node @ 2 V/div; Ch#2 = output voltage @ 10 mV/div and 1 V offset; Ch#4 = inductor current @ 200 mA/div
- Figure 4 – DCM with Fsw = 2.13 MHz
  - Ch#1 = switch-node @ 2 V/div; Ch#2 = output voltage @ 10 mV/div and 1 V offset; Ch#4 = inductor current @ 50 mA/div

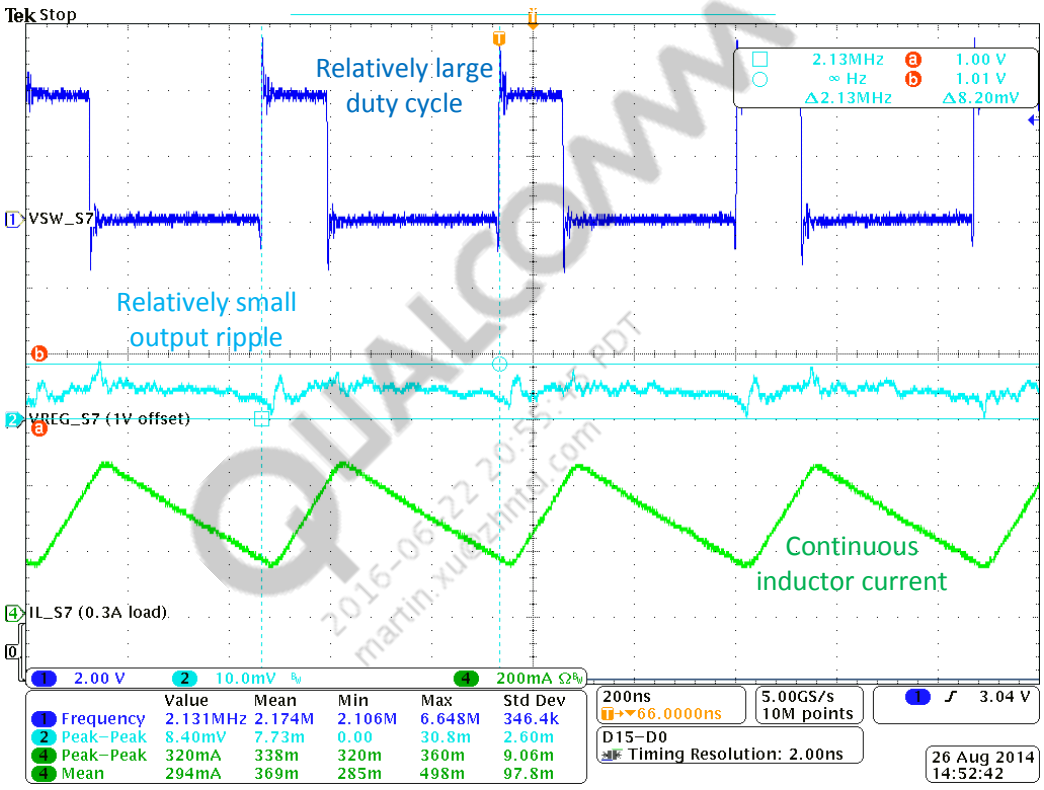

Figure 3 Waveforms of HF-SMPS in CCM PWM

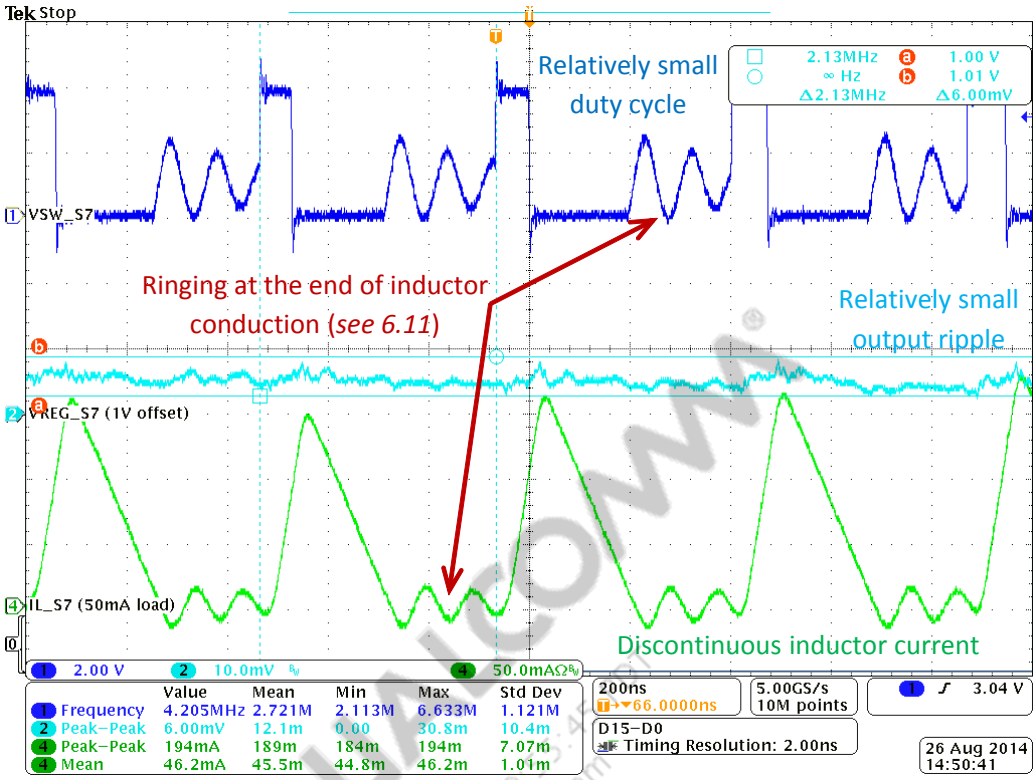

Figure 4 Waveforms of HF-SMPS in DCM PWM

3.2 Pulse-skip PWM

A major drawback of PWM switching is its poor efficiency under light load conditions, where switching losses are dominant. Efficiency is improved by skipping unnecessary PWM pulses, while maintaining low output ripple.

- Figure 5 – pulse-skip PWM with Fsw = 2.13 MHz
  - Ch#1 = switch-node @ 2 V/div; Ch#2 = output voltage @ 10 mV/div and 1 V offset; Ch#4 = inductor current @ 200 mA/div

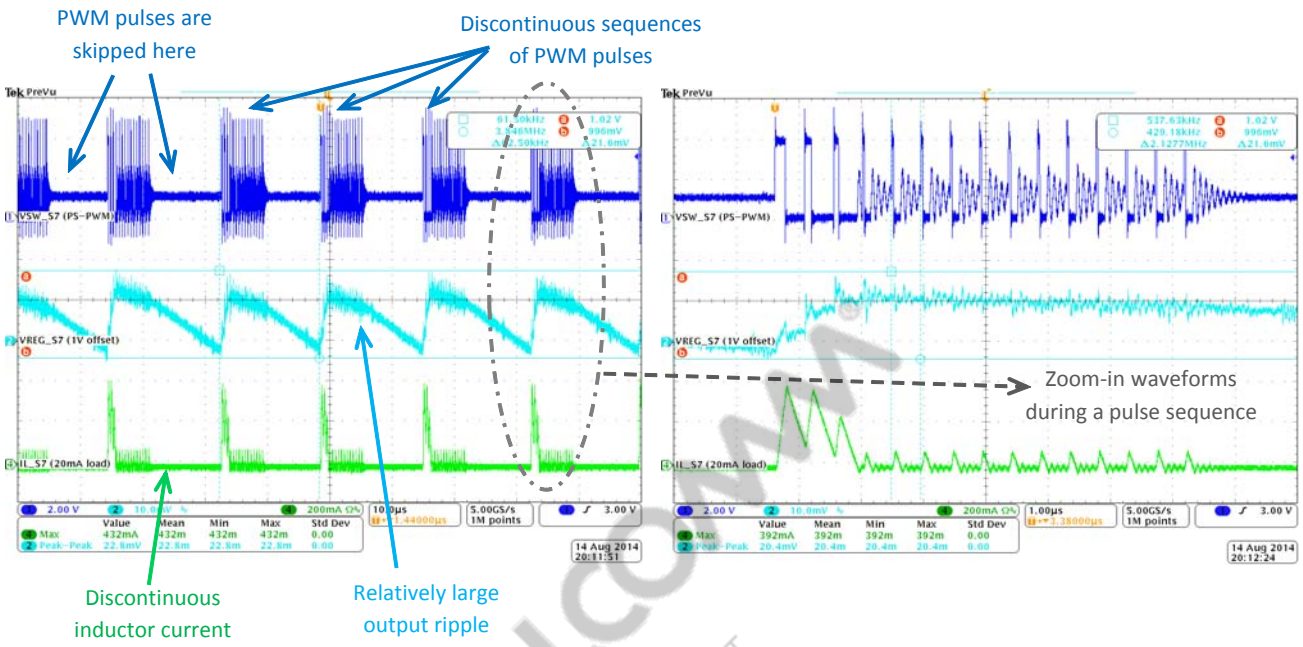

Figure 5 Waveforms of HF-SMPS in pulse-skip PWM

3.3 Pulse frequency modulation

Besides constant frequency pulse frequency modulation (PWM), the HF- and FT-SMPS circuits also support PFM where the buck monitors its output voltage, and only turns on the power switch when the output voltage dips below a certain threshold. The main advantage of PFM is its high efficiency at very light loads, achieved by simultaneous reductions in switching losses and buck ground current (unnecessary control functions are disabled). PFM disadvantages compared to PWM include larger output voltage ripple, inability to respond to large load transients, and varying switching frequency (spread noise spectrum).

- Figure 6 – PFM
  - Ch#1 = switch-node @ 2 V/div; Ch#2 = output voltage @ 10 mV/div and 1 V offset; Ch#4 = inductor current @ 200 mA/div

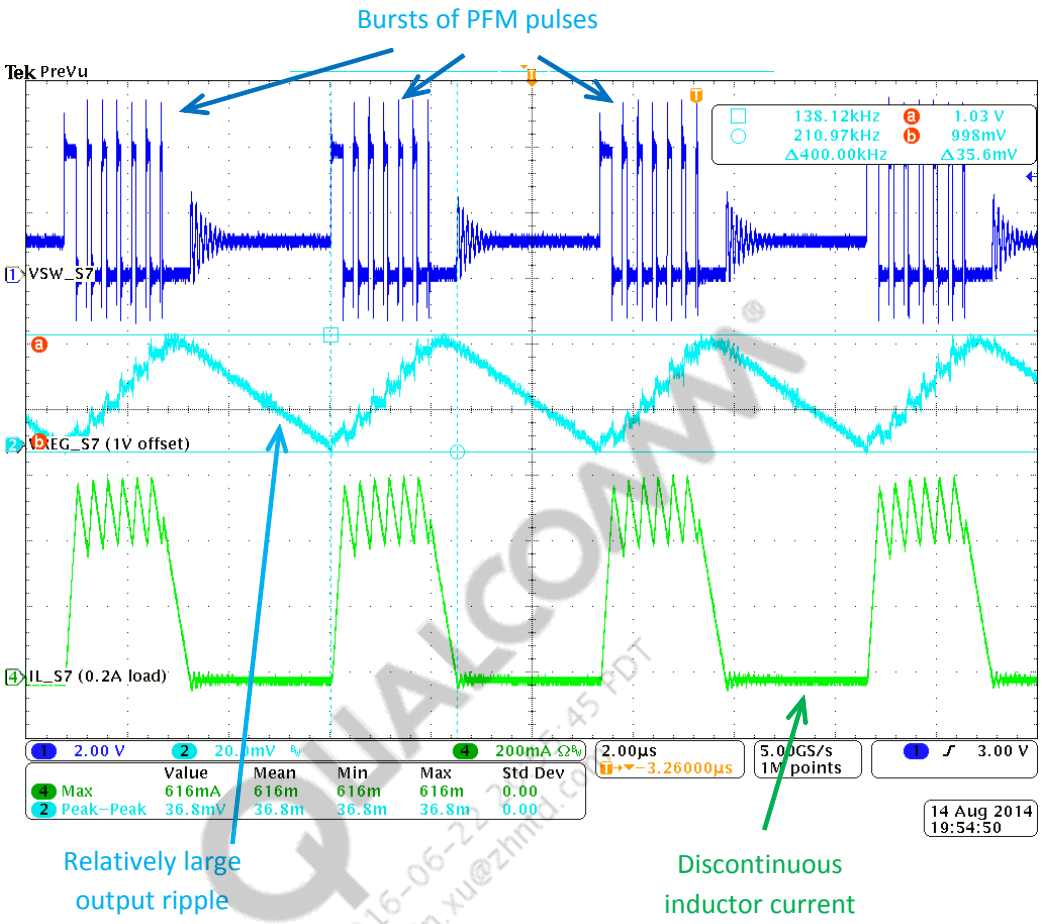

Figure 6 Waveforms of HF-SMPS in PFM

3.4 Auto-mode

The buck can always be forced into PWM and PFM modes by software or register commands, but the auto-mode feature automatically (without any software interaction or register command) switches between PFM and PWM modes based upon load current. During auto-mode, the buck constantly monitors load current and decides whether to operate in PFM (light load) or PWM (medium to high load).

- Figure 7 – HF-SMPS auto-mode transition
  - Transition due to attack and release of a 400 mA load on a 40 mA baseline current
  - Ch#2 = output voltage @ 20 mV/div and 1 V offset; Ch#4 = load current @ 200 mA/div
- The HF-SMPS transitions from PFM to PWM when a 400 mA load attacks, and then transitions back to PFM after the 400 mA is released.
- To prevent the output voltage from dipping too low in PFM, it is trimmed to be slightly higher than the PWM set-point. In the example shown, the PFM output voltage is about 10 mV higher than the PWM.

NOTE This higher PFM voltage trimming feature is only used for HF-SMPS.

- The FT-SMPS has a similar response to load steps in auto-mode, except that its average value output voltage does not change between PFM and PWM modes.

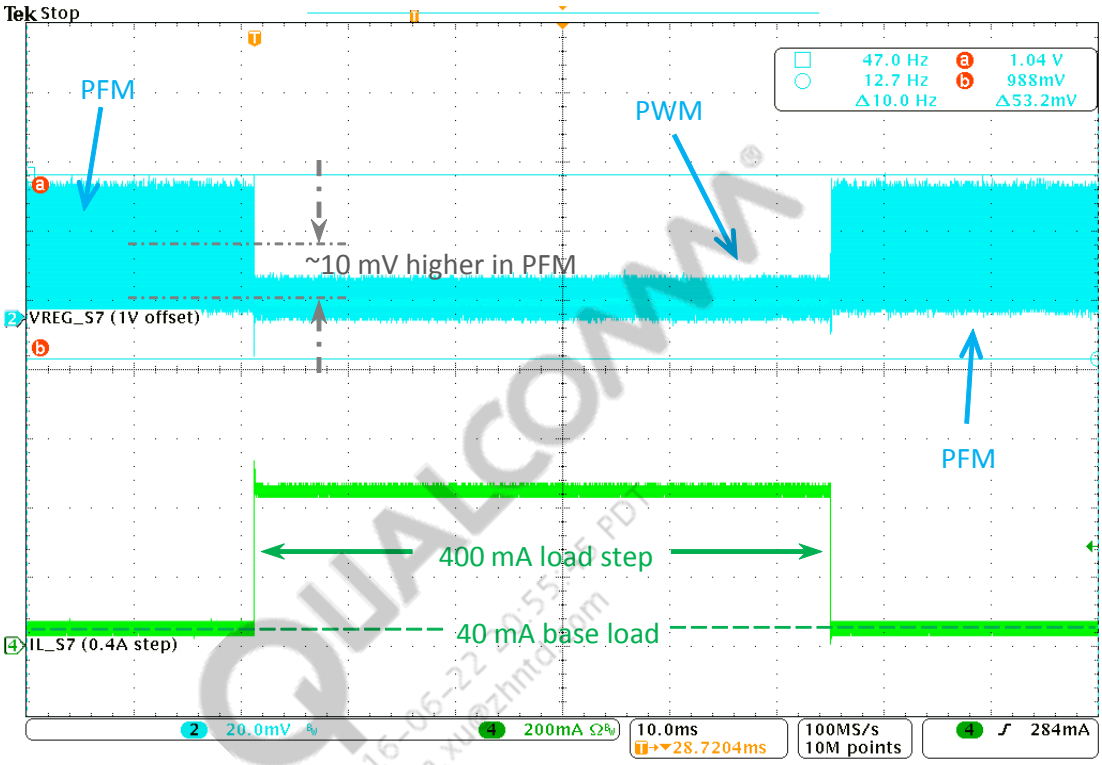

Figure 7 Waveforms of HF-SMPS auto-mode transition

3.5 High-current PFM

High-current PFM (HC-PFM) is a transitory PFM mode that occurs during normal PFM to PWM transitions that can be forced by a command or triggered by auto-mode. Either way, HC-PFM occurs.

For example, starting in auto-mode PFM, a sudden large increase in load current causes an output voltage dip, which indicates that the buck needs to exit PFM and enter PWM. However, it is impossible for the buck to transition instantaneously (or as fast as the load increases), since it takes some time for the PWM circuits to warm up and take control. To prevent the buck output voltage from drooping too low by staying with its initial mode and settings (while the PWM circuits are warming up), the PFM current can be programmed to an intermediate value between normal PFM and PWM current limits. When the intermediate current limit is engaged, the transitory PFM state is called HC-PFM. The HC-PFM duration is different depending upon SMPS type: 5 to 10 µsec for HF; a few tens of µsec for FT.

- Figure 8 – FT-SMPS during HC-PFM
  - HC-PFM operation is triggered by a 2.5 A load step
  - Ch#2 = output voltage @ 10 mV/div and 1 V offset; Ch#4 = load current @ 1 A/div

- The PMIC registers for current-limits and their set-point values are QTI-proprietary and not shared. Current limits shown in Figure 8 have been altered from their original values to illustrate the HC-PFM concept.
- Depending upon a buck's design and operating parameters (switching frequency, current rating, external components, etc), as well as system and load requirements, each buck may have its own unique current-limit settings.

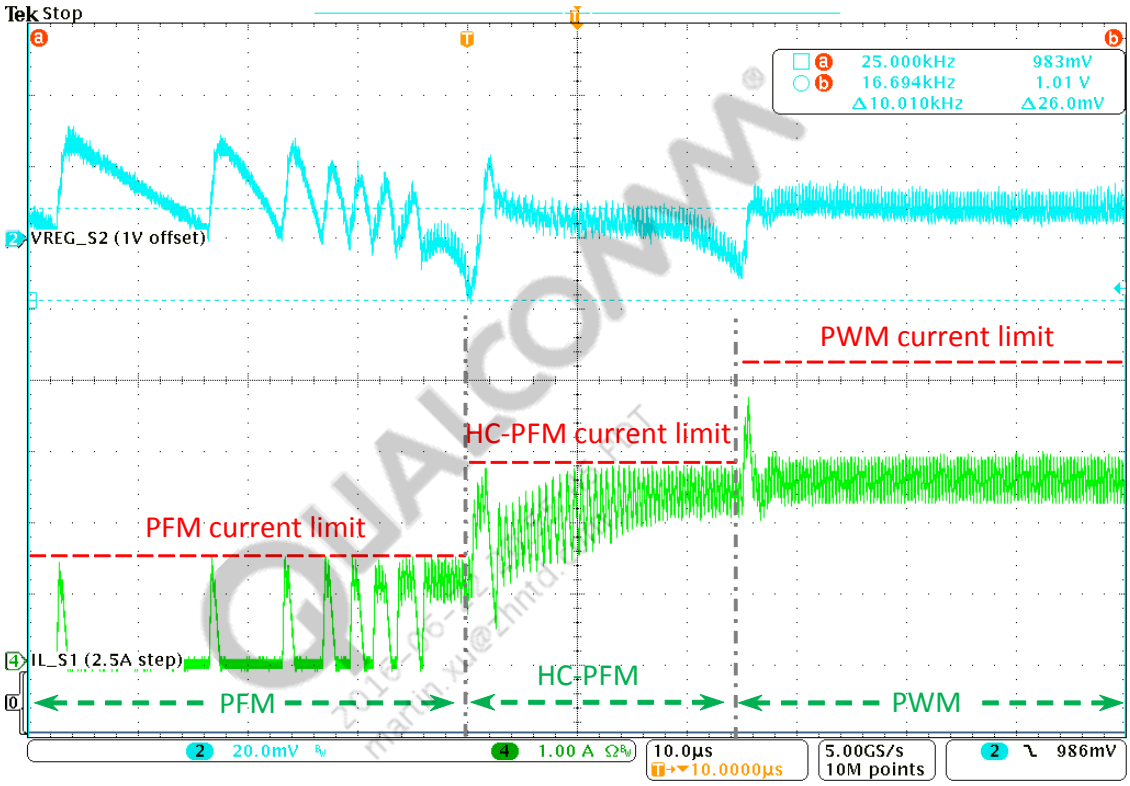

Figure 8 Waveforms of FT-SMPS during HC-PFM operation

4 Multi-phase FT-SMPS

Some FT-SMPS outputs can be grouped together to form a dual-, tri-, or quad-phase output. The additional phases (higher phase-count) can be turned on as needed, based upon the load condition. The newer FT-SMPS generation (called FTS2.5, and used within recent PMIC releases like the PM8994 and PMI8994) supports autonomous phase control (APC). Once APC is enabled during multi-phase operation, the phase-count is autonomously managed by hardware to select the appropriate number of phases (phase-count) for optimal efficiency based upon load current. The phase-count is enabled using a register offset of 0x54 relative to the lead phase. For example, register 0x12354 (S6_CTRL_PHASE_CNT) on the PMA8084.

During multi-phase operation:

- Inductor currents are monitored and balanced across the active phases (Figure 9).
  - Current sharing on a dual-phase FT-SMPS in response to attack and release of a 2 A load on a 5 mA baseline current
  - Ch#1 = phase-1 inductor current @ 1 A/div; Ch#2 = phase-2 inductor current @ 1 A/div
- The starting point of each switching cycle is phase-staggered to minimize ripple voltage and to spread out current surges drawn from the battery (Figure 10).
  - 180-degree phase-staggered switching pulses on a dual-phase FT-SMPS
  - Ch#1 = phase-1 switch-node @ 2 V/div; Ch#2 = phase-2 switch-node @ 2 V/div; Ch#3 = output voltage @ 10 mA/div and 1 V offset

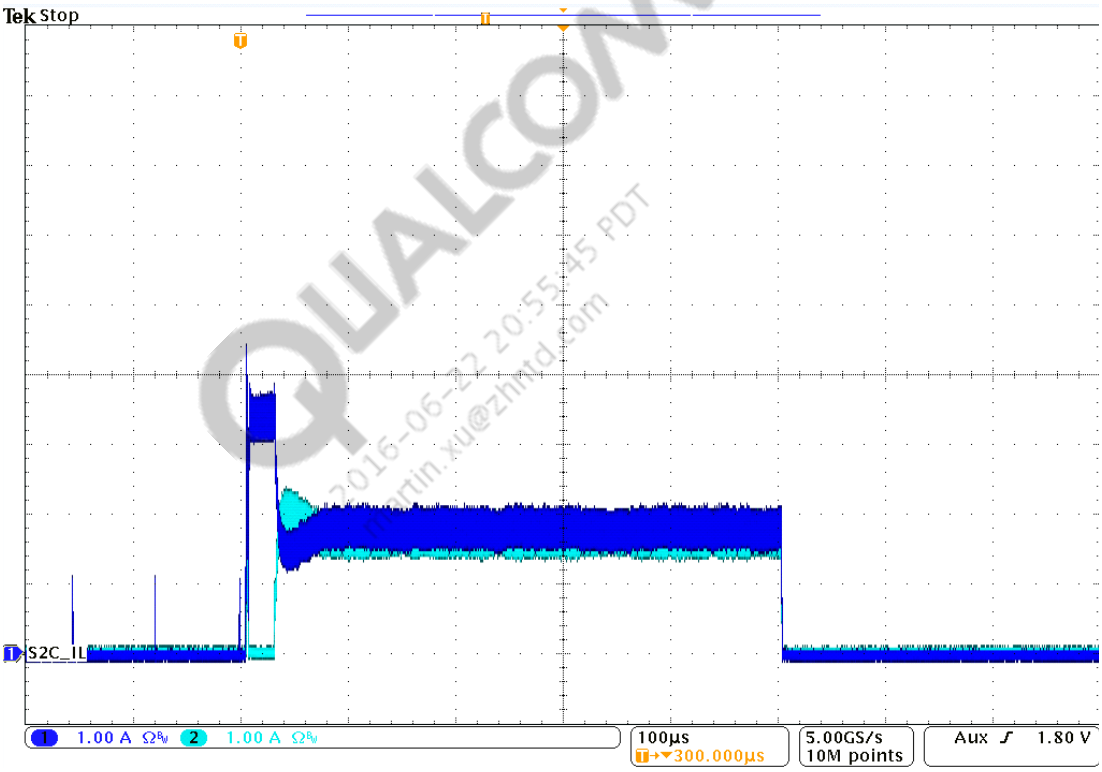

Figure 9 Current sharing on a dual-phase FT-SMPS

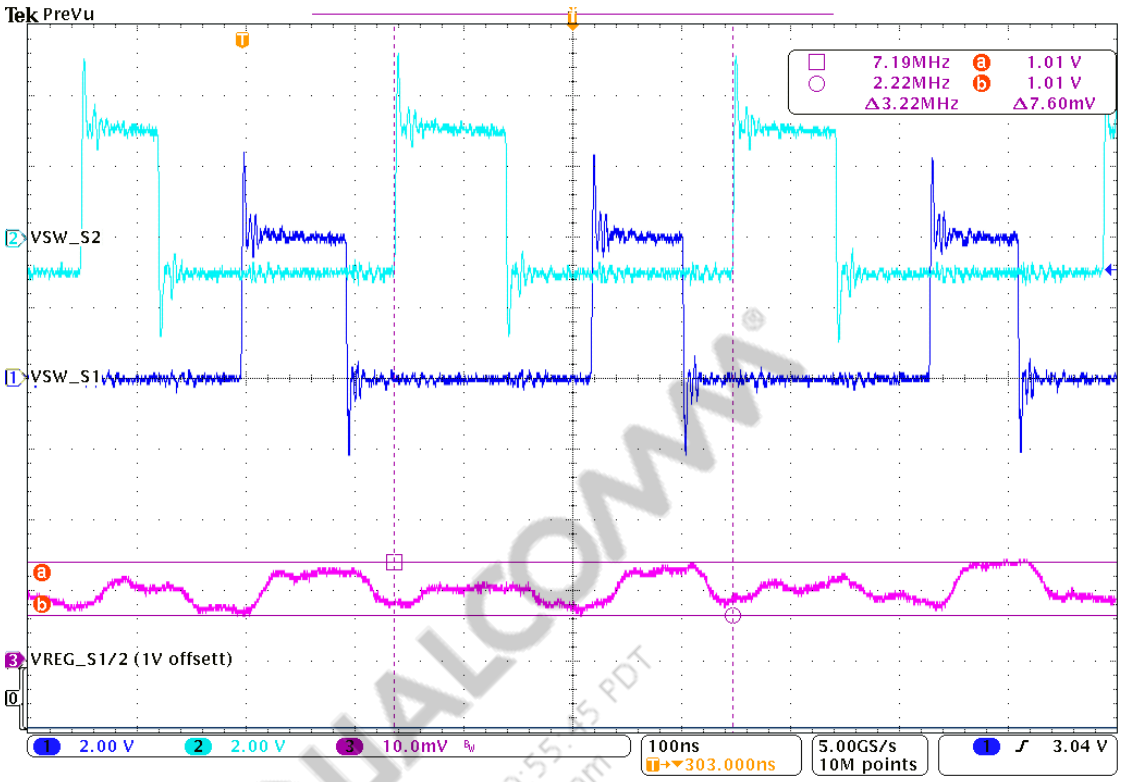

Figure 10 Phase-staggered switching pulses on a dual-phase FT-SMPS

5 SMPS Testing

5.1 Output voltage measurements

A buck's output voltage waveform is measured to characterize several parameters: ripple, accuracy, efficiency, load transients, start-up/discharge time, mode transients, load and line regulation, etc.

- The output voltage must be measured at the load capacitor (not at the load terminal).
  - For HF-SMPS, measure the output voltage between the output capacitor's positive (+) terminal and the GND_REF pin of the PMIC.
  - For FT-SMPS, measure the output voltage across the load capacitor's terminals (between its + and GND terminals).
- Use an RF connector, shielded cable, and a ground coil shield around the oscilloscope probe barrel to eliminate noise coupling (Figure 11). In case an RF connector jack is not mounted on the PCB, use a ground shielded oscilloscope for the output voltage measurement (Figure 12).
- Output voltage waveforms must be taken with the 20 MHz bandwidth oscilloscope setting.
- Ripple is measured as the largest ripple over a single switching cycle, not the difference between the overall minimum and maximum values of the buck output voltage (Figure 13).

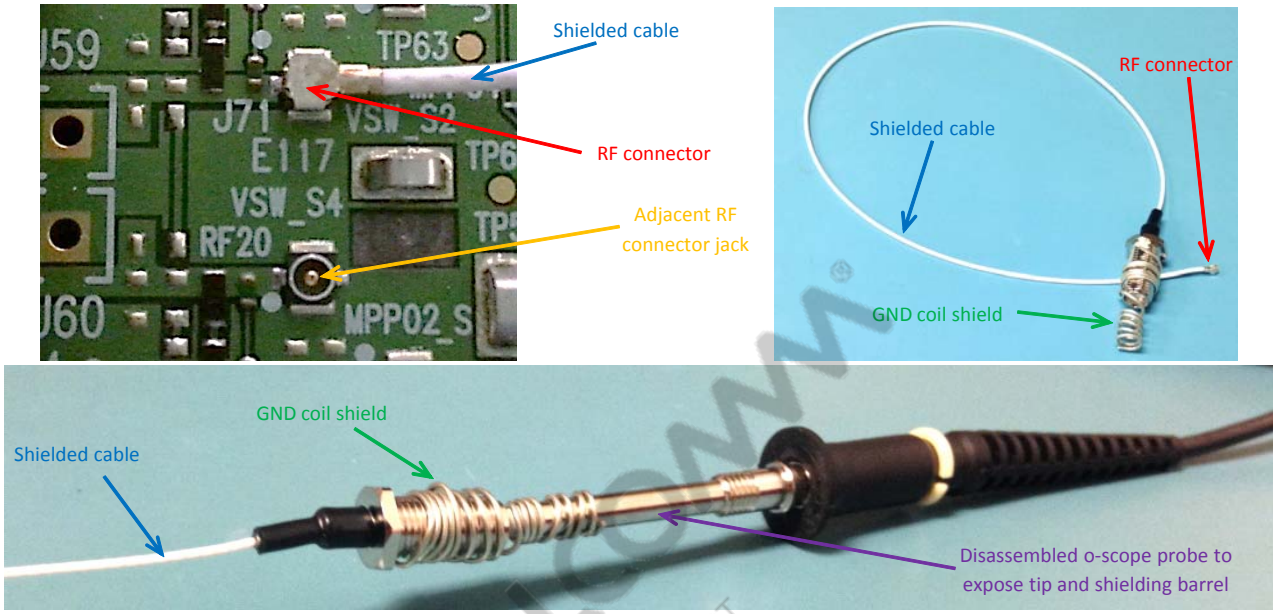

Figure 11 RF connector, shielded cable, ground coil shield, and oscilloscope probe for output voltage measurements

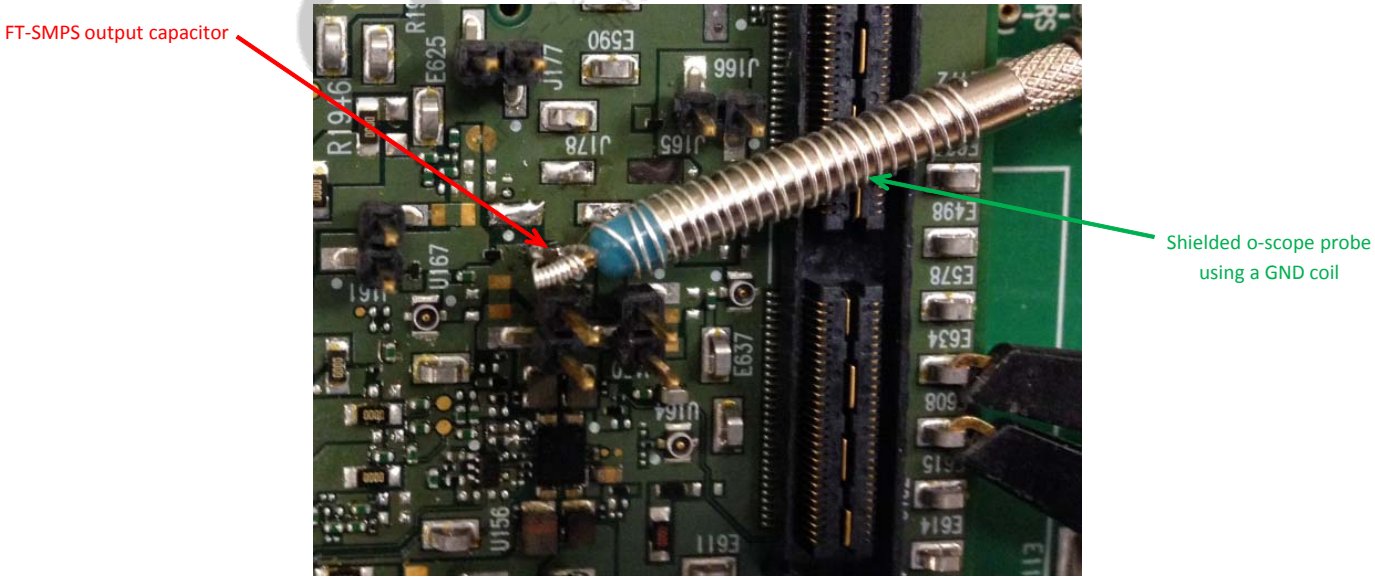

Figure 12 Output voltage measurement across FT-SMPS output capacitor using a ground coil and oscilloscope probe

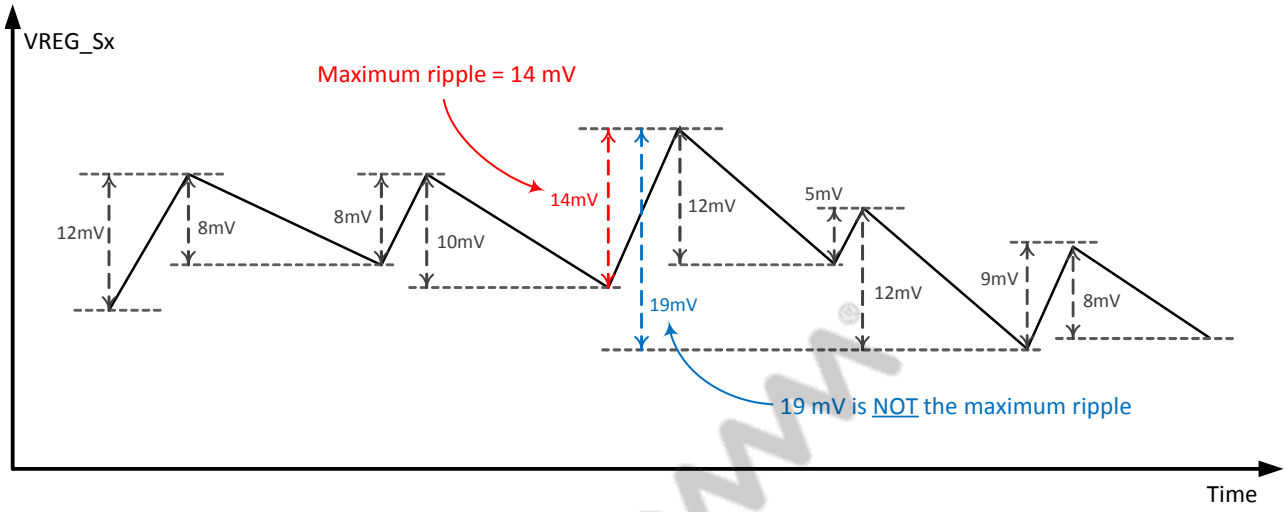

Figure 13 Maximum ripple measurement

5.2 Efficiency measurements

Efficiency measurements are very sensitive and require special precautions.

- Buck input voltage must be Kelvin-monitored at the input capacitor.
- 4-wire sensing must be used at the input capacitor terminals to compensate for IR drop losses (Figure 14).
- Local input voltage and current measurements must be used to calculate input power.
- The buck input current under any certain load can be calculated as the difference between the total PMIC current consumption before enabling the buck and after enabling and loading the buck. For example, a PMIC draws 5 mA from the power supply when the PMIC is on and its buck S1 is off. When buck S1 is turned on with a 1 A load, the PMIC input current increases to 550 mA. This means that the buck S1 input current under a 1 A load is 545 mA (550 - 5).
- Buck output voltage must be measured at the load capacitor for output power calculations.
- Several measurements (10 or more) should be taken at each operating point, and the resulting average logged as the efficiency value at that operating point.

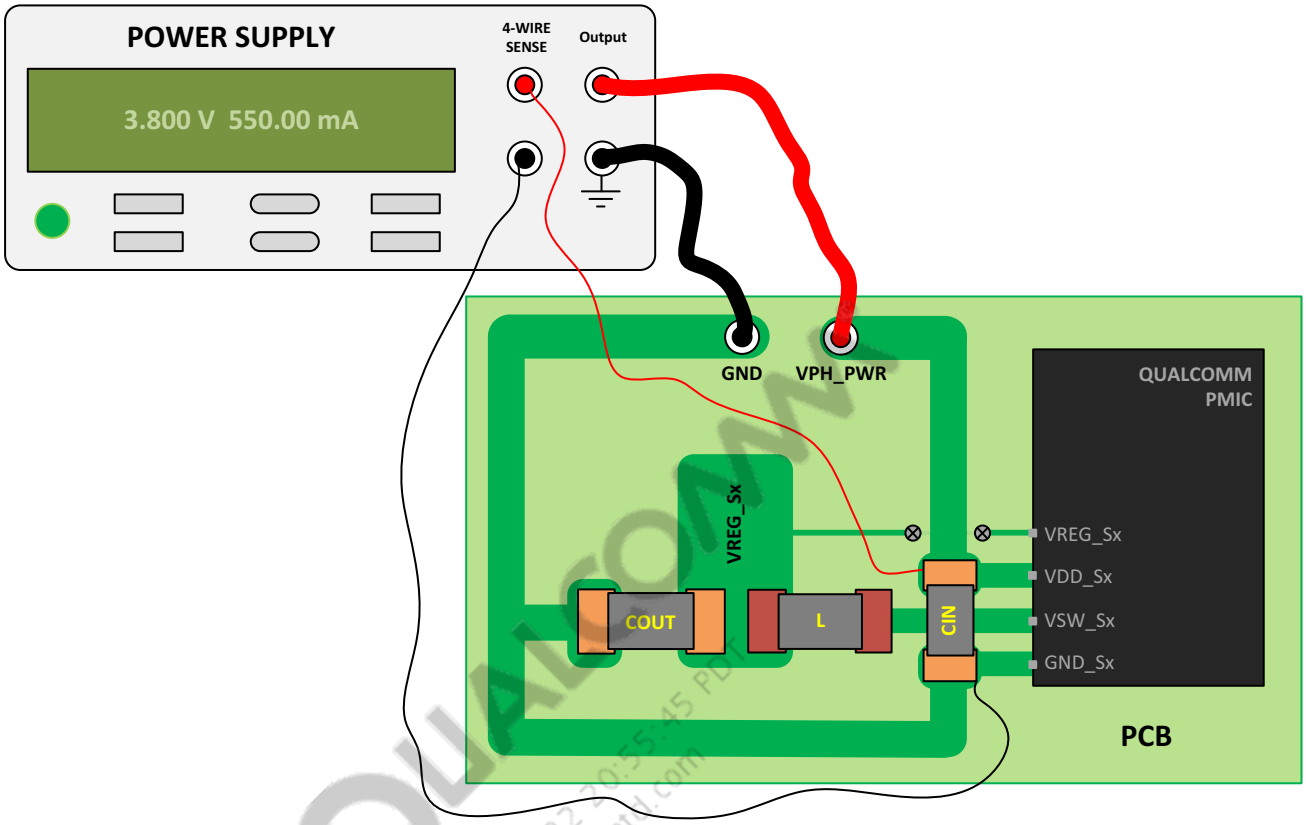

Figure 14 4-wire sensing at the input capacitor for efficiency measurements

5.3 Transient load measurements

A load step causes the output voltage to quickly over-shoot or dip (depending upon a load decrease or increase). If the transition is from high to low load, an over-shoot (or spike) in output voltage occurs, whereas a low to high load transition causes a dip in the output voltage. Typical auto-mode load transition waveforms of a HF-SMPS are shown below:

- Figure 15 – load transient dip measurement of HF-SMPS in auto-mode
  - 40 mA baseline current, step up to a 440 mA load
  - Ch#1 = switch-node @ 5 V/div; Ch#2 = output voltage @ 10 mV/div and 1 V offset; Ch#4 = load current @ 200 mA/div
- Figure 16 – load transient over-shoot measurement of HF-SMPS in auto-mode
  - 440 mA baseline current, step down to a 40 mA load
  - Ch#1 = switch-node @ 5 V/div; Ch#2 = output voltage @ 10 mV/div and 1 V offset; Ch#4 = load current @ 200 mA/div

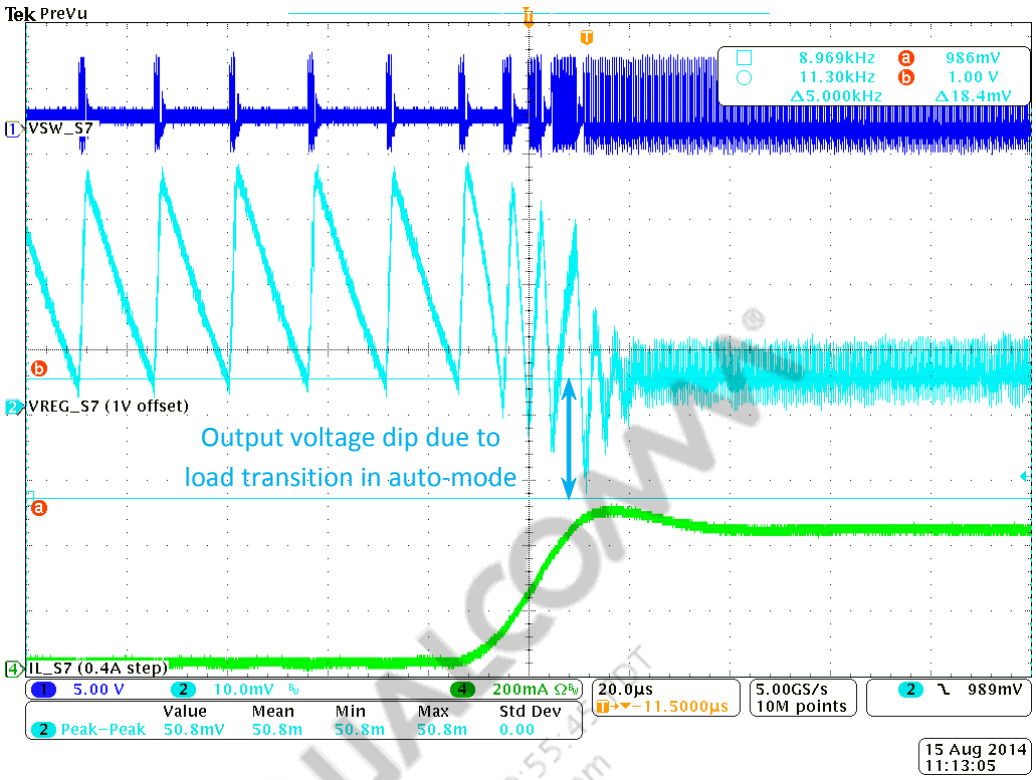

Figure 15 HF-SMPS load transient dip measurement

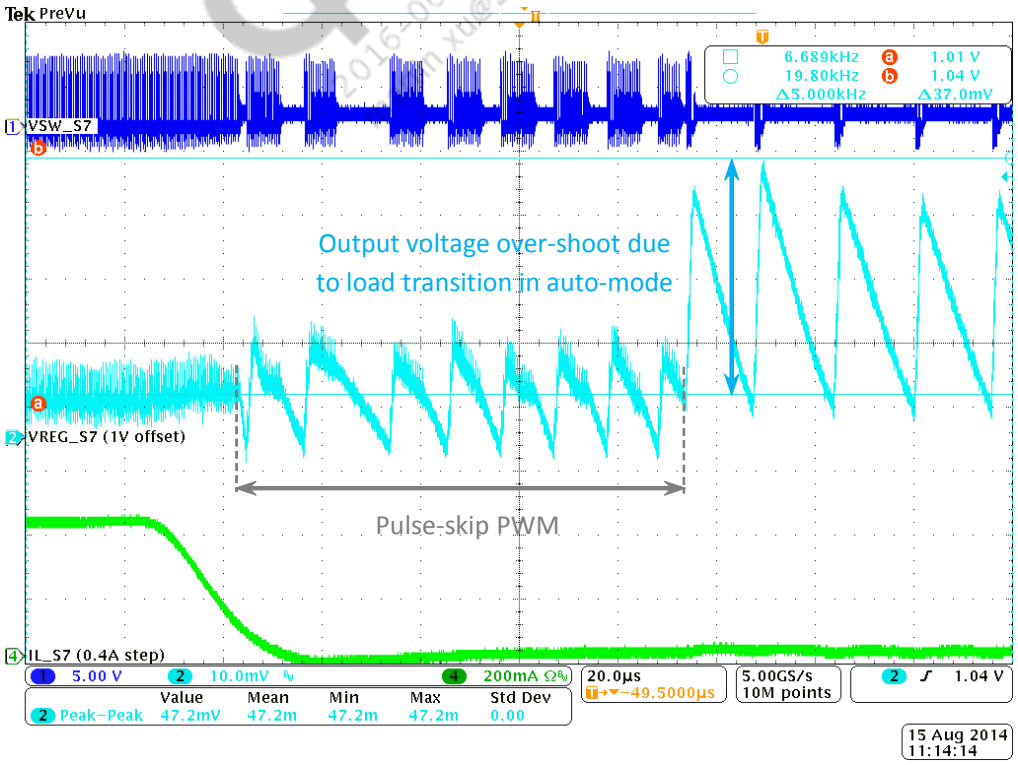

Figure 16 HF-SMPS load transient over-shoot measurement

Smaller dip and over-shoot values are expected when PWM is forced (when the buck is operating in PWM before and after the load change).

Note that the load transient dip and over-shoot are measured with respect to the average output voltage in PWM mode.

6 Frequently Asked Questions (FAQs)

6.1 Why is the buck output voltage different from its default value in the device specification?

The default value given in the device specification is the hardware default. After power-up, the buck output voltage can be set to other values by software. Software often changes the setting to a non-default value to optimize system performance or minimize power consumption.

6.2 Why does the buck output voltage change when the phone is on?

Depending upon the phone's operating mode and system requirements at any time, software dynamically changes the buck's output voltage setting and operating mode (auto-mode, PFM, or PWM) for optimal phone performance. Changing buck output voltages are expected.

6.3 How does the SMPS current-limit feature work?

Both HF- and FT-SMPS circuits monitor their inductor current, and limit the peaks by opening the buck's high-side PFET (see Figure 1). The peak inductor current-limit is configured in QTI software based upon the buck's current rating, operating mode, and projected load. The PMIC registers for current-limits and their set-point values are QTI-proprietary and not shared.

6.4 Does buck SMPS have over-current protection (OCP)?

Yes, both HF- and FT-SMPS circuits include OCP to protect them against short circuit and low-impedance faults.

The HF-SMPS detects an over-current event when either of these conditions are met:

- VREG_Sx drops below the fault voltage threshold (VREG_FAULT ~ 300 mV) combined with 4 or 8 (programmable) consecutive inductor current-limit hits.
- VREG_Sx remains below the fault voltage threshold until a 4 µs backup timer expires.

After an over-current event, the OCP turns off the HF-SMPS to protect it from damage. To recover, the HF-SMPS must be reset (disabled then re-enabled).

The FT-SMPS uses foldback protection to avoid over-current damage. The over-current event is detected when VREG_Sx drops below the fault voltage threshold (VREG_FAULT ~ 250 mV). Upon detection, the OCP opens the PFET (PFET off) and forces the inductor current to decay down to zero; after that, the PFET can turn on. The PFET turns off again when the inductor hits its current-limit. Hence, the fault current is limited to 50% of the inductor current-limit threshold. To recover from this condition, the VREG_Sx has to go above the fault voltage threshold.

In addition to the buck-level responses described above, the PMIC can also be configured to react to an over-current event by monitoring the bucks' OCP detection signals and running the corresponding programmed sequences. For example, the PM8994 is configured to shut down upon OCP detection on any of its HF- or FT-SMPS circuits; this is the PMIC's system-level response to a buck OCP detection.

6.5 Can I use a different buck capacitor or inductor than the one recommended in the QTI reference schematic?

It is strongly recommended that schematic's buck components be used. Recommended components are listed in the schematic's part list table. If not using a recommended part:

- Make sure that the alternate part meets or exceeds the recommended part's specifications.
- Test and validate the part themselves.

Also, see *Application Note: Switched-Mode Power Supply (SMPS) Inductor Selection* (80-VC603-9) for SMPS inductor selection guidelines.

6.6 Can QTI approve/test/characterize/validate my inductor and capacitor selections?

No. It is up to designers to test/characterize/validate their choice of non-recommended buck components. Refer to the previous question for additional comments.

6.7 Can I change the buck switching frequency?

Buck components and control parameters have been optimized for QTI's software-configured switching frequency. QTI has characterized and validated the buck performance at this switching frequency, and alternate settings are not recommended.

6.8 Why is the FT-SMPS PWM switching frequency different than expected?

This is due to the multi-pulsing issue, where two or more switching pulses can be observed within a single switching period. The FT-SMPS circuit's very fast response feature makes it more susceptible to capacitive and magnetic noise coupling onto its sense lines. Multi-pulsing appears as random pulses on the FT-SMPS switch-node (VSW_Sx) within a single switching cycle. The extra switching events introduce additional losses that could degrade FT-SMPS efficiency. Multi-pulsing can only occur on an FT-SMPS (does not occur on an HF-SMPS); an example waveform for a single-phase FT-SMPS is shown in Figure 17. The multi-pulsing issue has also been described in the applicable device revision guide document.

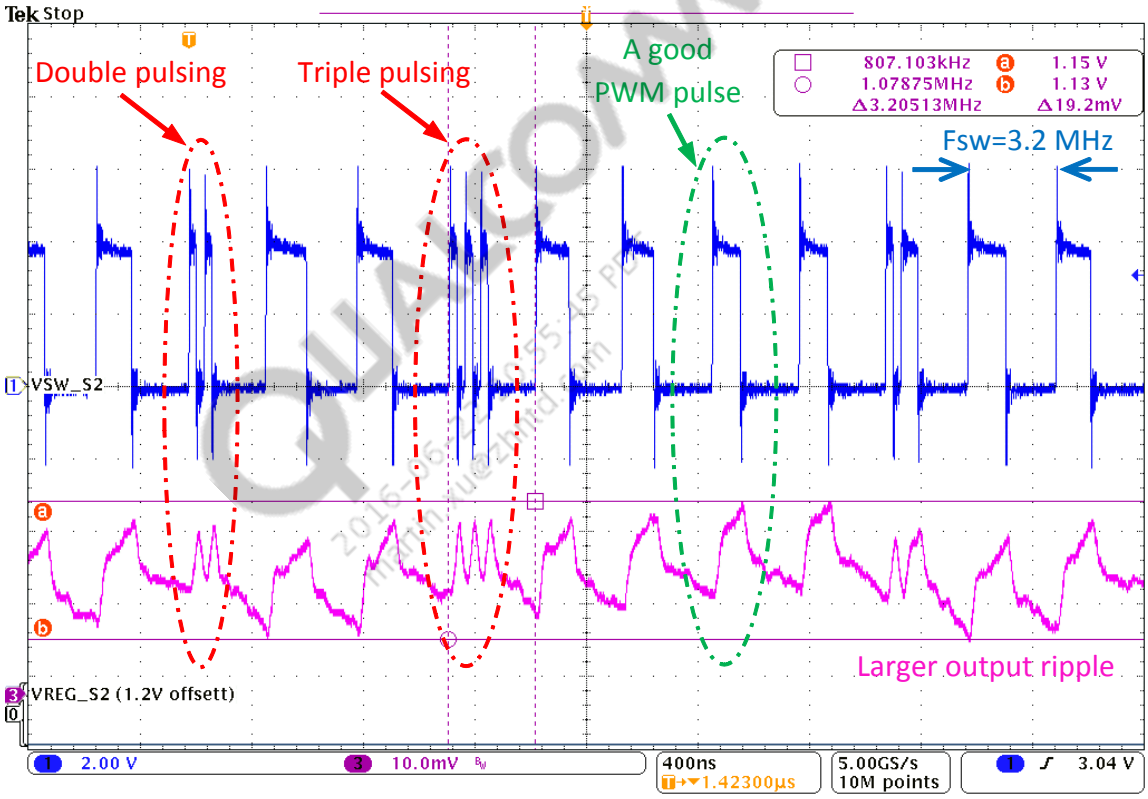

Figure 17 FT-SMPS multi-pulsing waveform

6.9 Why is the FT-SMPS PWM switching waveform distorted?

This is due to multi-pulsing; see Section 6.8 for an explanation.

6.10 What is the load current threshold for auto-mode transition?

There is no explicit current threshold for auto-mode transition. There are a number of factors that influence the actual threshold: switching frequency, actual inductor value, input and output voltage levels, type (FT or HF) and rating of the buck, as well as the buck register configurations. Although the exact criteria for switching between PFM and PWM in auto-mode is QTI proprietary, approximate ranges are provided:

- FT-SMPS PFM-to-PWM load current threshold: ~ 0.7 to 1.1 A
- HF-SMPS PFM-to-PWM load current threshold: ~ 0.1 to 0.3 A
- FT-SMPS PWM-to-PFM auto-mode transition: ~ 0.2 to 0.9 A
- HF-SMPS PWM-to-PFM auto-mode transition: ~ 0.05 to 0.2 A

6.11 Why do the inductor current and switch-node ring in DCM/PFM when the current conduction ends?

The ringing is due to an oscillation between the external components (L, C, and load circuits) and buck parasitic capacitance. For further explanation, refer to the waveforms and circuit diagrams within Figure 18.

1. **NFET conduction** – neglecting the buck's NFET forward voltage drop, the switch-node voltage is zero during NFET conduction (PFET is off), and the inductor current is larger than zero with a negative slope ($\Delta IL/\Delta t < 0$).
2. **DCM boundary** – the NFET opens at the DCM boundary, when the inductor current hits zero. At this moment, the switch-node voltage and inductor current are equal to zero (VSW_Sx = 0 and IL = 0), and the output voltage is assumed to be constant at the desired load voltage, Vo (output ripple neglected and VREG_Sx = Vo).
3. **Ringing and settling** – the load capacitor voltage (VREG_Sx = Vo) starts to discharge in the NFET's tiny parasitic capacitor (Cp) until the Cp voltage settles to the same voltage as the load capacitors (VSW_Sx = VREG_Sx = Vo). This oscillating response is dampened by the circuit's resistance (inductor DCR, PWB traces, parasitic resistances, etc), which causes ringing within the switch-node and the inductor current waveforms. It is normal to see some negative inductor current during the ringing.

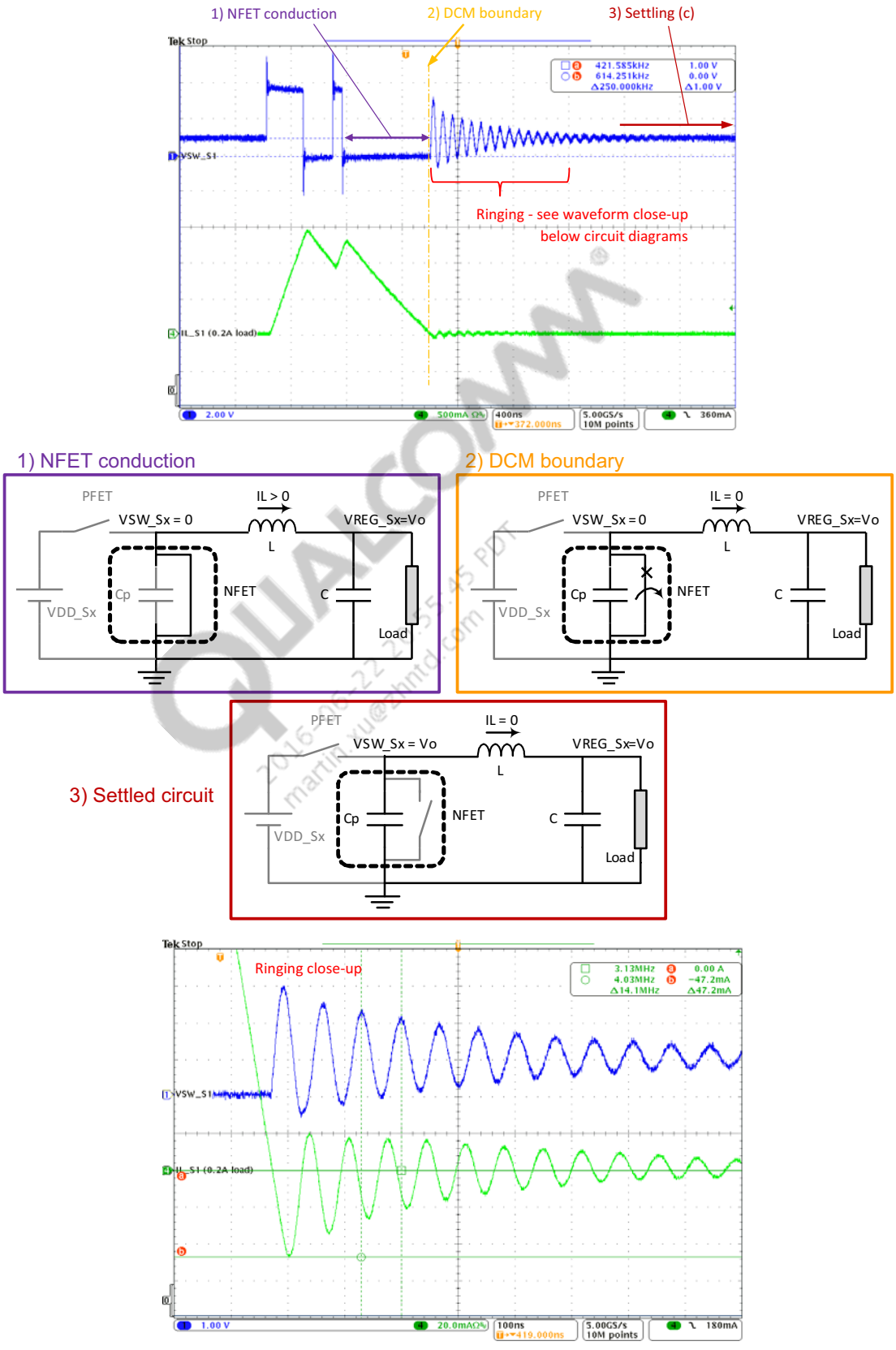

Figure 18 Switch-node ringing

6.12 Why is there negative inductor current, and how much is acceptable?

Both HF- and FT-SMPS have the zero-crossing detection feature, and turn the NFET off upon detecting zero inductor current. However, as explained in the previous answer, some amount of negative inductor current in the DCM/PFM mode is expected and cannot be avoided.

There is no specification (acceptable range) for the inductor negative current, but a few tens of mA is typically seen across the HF and FT bucks. In any case, this amount of negative current does not raise any reliability concerns, since a negative current as high as ~5 A is required to damage the power switches.

6.13 What is a buck's discharge time?

In general, a buck's discharge time depends on the time constant ($\tau = RC$) of its load circuit. HF- and FT-SMPS also have internal pull-down resistors that can be configured in parallel with their external load circuits to: a) expedite discharge of their load capacitor's voltage, and b) prevent their output voltage from floating during no-load conditions. If the buck's pull-down is not enabled, it may take several seconds for an unloaded buck to discharge. Enabling or disabling the pull-downs depends upon system considerations and each buck's load circuit requirements. For instance, to minimize system current consumption, software usually disables buck pull-downs if they frequently turn on and off during their operation. Once the pull-down is enabled, the typical discharge time constant of a buck can be calculated using its typical pull-down resistance value (25 Ω for HF-SMPS and 32 Ω for FT-SMPS) and the load capacitance.