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Configuration of Input Pins During Device Sleep
80-VN499-7 Rev. A

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Revision History

Revision	Date	Description
A	December 2008	Initial release

Definition of Terms

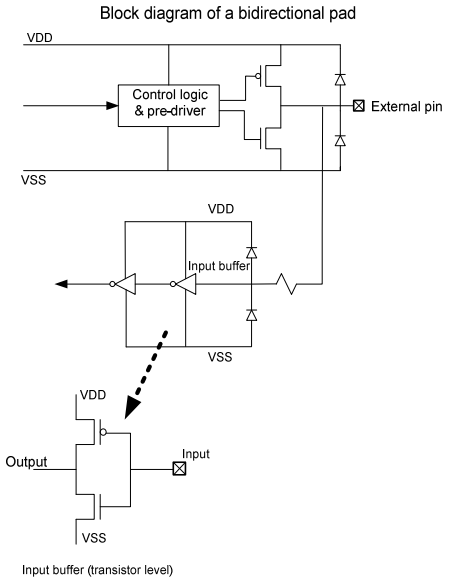
- BT – Bluetooth®
- GPIO – General-purpose input/output pin
- Input pin valid voltage (V) – Defined as $V \leq Vil_{max}$ and $V \geq Vih_{min}$
- SDIO – Secure digital input output interface
- Sleep – The lowest power state a Qualcomm baseband device can enter without powering off. This state typically occurs between network wake-up events and when no other processor interrupts have occurred. Input pins typically do not toggle during this state.
- TFlash – TransFlash™ interface
- Tri-state – High impedance state
- Vih_{min} – The minimum voltage on an input pin that is guaranteed to be interpreted as a logic high according to the device specification.
- Vil_{max} – The maximum voltage on an input pin that is guaranteed to be interpreted as a logic low according to the device specification.

Key Message

- **It is the responsibility of the customer's software and hardware design to ensure that every digital CMOS input pin has a valid voltage on it at all times during sleep to avoid the possibility of excess leakage current.**
- If these input pins are not held in a valid logic state by external circuits, the customer software must configure them using one of the following methods:
  - Configure floating input pins with an internal pull-up resistor.
  - Configure floating input pins with an internal pull-down resistor.
  - Configure floating input pins to be outputs **but only** if the pins are GPIOs that are not connected to any external circuit. The output can be either polarity.
- Examples of inputs that must be properly configured by the customer before entering sleep include:
  - Inputs that are not connected to any external circuit
  - Inputs that are connected to third-party devices that get tri-stated (BT, camera, etc.)
  - Inputs that are connected to peripheral devices that are not always installed (SDIO, TFlash, etc.)

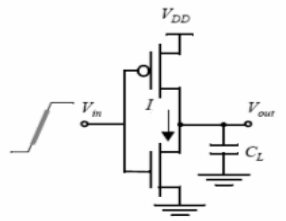
GPIO Input Pin Specification Violation

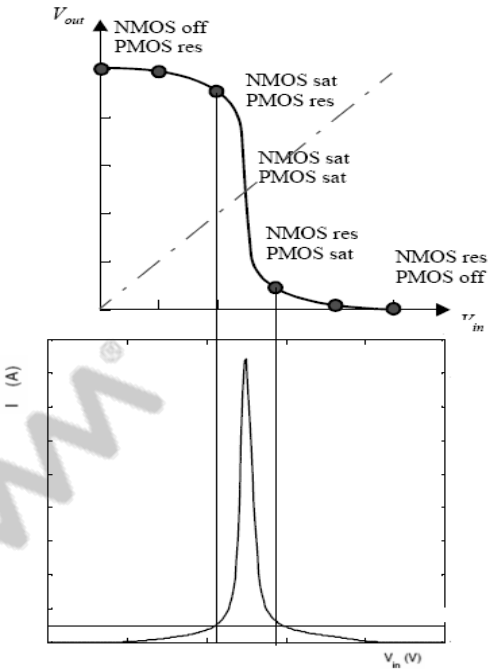
- If a GPIO that is configured as an input contains a voltage outside the device specification range during sleep, this can cause significant leakage current from pad V_{DD} to V_{SS}.
- QCT does not have the ability to predict how much leakage will occur when a GPIO input contains a voltage that violates the device specification's V_{ih} and V_{il} during sleep.
- The absolute value of the leakage current depends on the sub-threshold currents of the individual transistors and the ratio of effective resistances of PMOS and NMOS transistors in the disabled output buffer, which in turn varies with process, gate and body bias, and transistor size.
- Therefore, QCT cannot guarantee or specify the exact effect of violating valid logic levels for CMOS inputs during sleep.



CMOS Input Pin Transfer Function and Current Leakage

- This diagram illustrates relative leakage current that occurs as the voltage of a CMOS input pin changes.





- When the input voltage is between valid logic states, there is significant leakage current (I). The most leakage occurs when Vin = $V_{DD}/2$.

CMOS Input Truth Table

Input	Output	State
1	0	NMOS = on; PMOS = off No significant DC leakage
0	1	NMOS = off; PMOS = on No significant DC leakage
Floating between Vih_{min} and Vil_{max} (specification violation)	Undefined	NMOS = Partially on PMOS = Partially on Significant leakage from V_{DD} to V_{SS} is possible.

Key Message Summary

- Qualcomm software is developed on QCT internal hardware platforms that use pin configurations and GPIO assignments that are not guaranteed to match the end customer's GPIO assignments. Therefore, Qualcomm cannot directly control the proper configuration of the input pins on the customer's product.
- It is the responsibility of the customer's software and hardware design to ensure that every digital CMOS input pin has a valid voltage on it at all times during sleep to avoid the possibility of excess leakage current.

Questions?