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QUALCOMM CDMA Technologies

PM8841 and PM8941

Training Slides

80-NA555-21 Rev. B

QUALCOMM Incorporated
5775 Morehouse Drive
San Diego, CA 92121-1714
U.S.A.

Revision History

Revision	Date	Description
A	August 2012	Initial release
B	October 2012	Updated slides

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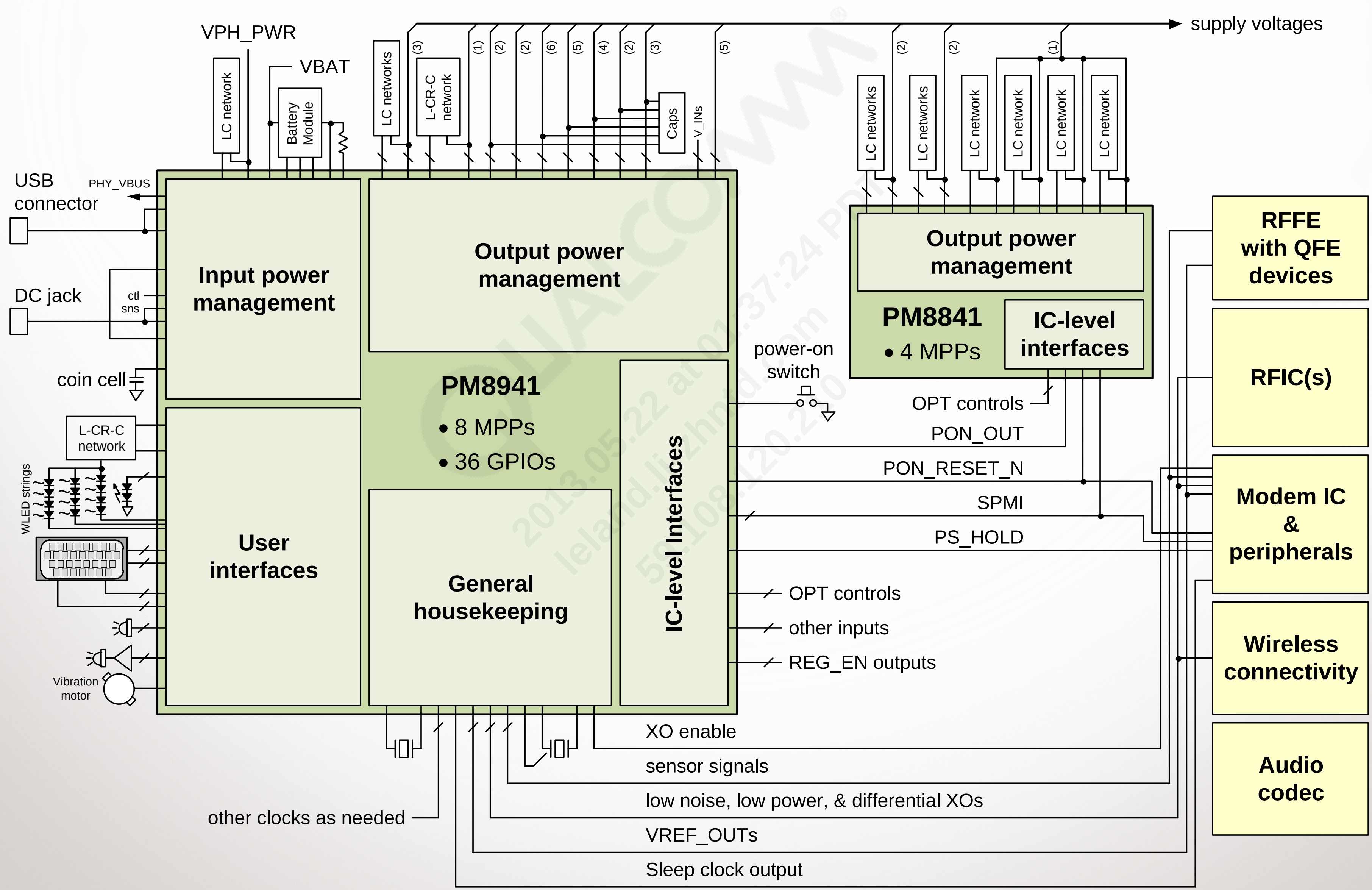
Power Management System and IC Overview

Power Management System Block Diagram



PM8x41 Features (1 of 4)

	Features	PM8921	PM8038	PM8x21	PM8x41
General metrics	Process	0.18 u	0.18 u	0.18 u	0.18 u
	Package size (mm)	7.8 × 7.8 61 mm²	5.96 × 5.96 35.5 mm²	7.8 × 7.8 2.8 × 2.4 67.7 mm²	6.15 × 5.82 4.45 × 3.58 51.72 mm²
	Package type	NSP	WLP	NSP+WLP	WLP x 2
	Package I/O (non common ground)	251	193	8921: 251 8821: 42	8941 : 229 8841 : 98
	PCB stackup	2N2	2N2	2N2	2N2
User interface and drivers	Keypad scanner	8 × 18	–	8 × 18	8 × 10
	MPP + AMUX channels	12	6	12 + 4	12 (8 + 4) + 8
	GPIO	44	12	44	36
	300 mA LED drivers	1	–	1	–
	40 mA LED drivers	3	3	3	–
	Matched RGB drivers	–	–	–	Yes
	LPG (light pattern generator)	8	5	8	8
	Vibrator driver	1	1	1	1
	Series white LED driver	-	Two strings Up to 32.5 V	-	Three strings Up to 32.5 V
	Camera flash driver	No	No	No	Yes : 2A

PM8x41 Features (2 of 4)

	Features	PM8921	PM8038	PM8x21	PM8x41
Input power management	Regulation type	Switch mode 2 A	Switch mode 2 A	Switch mode 2 A	Switch mode 3 A
	OVP	30 V	30 V	30 V	30 V/15 V
	Dual path	Yes	Yes	Yes	Yes
	Number of integrated OVP FETs	1	1	1	2
	BATFET	Ext	Ext	Ext	Int
	BMS (fuel gauge)	Yes	Yes	Yes	Yes
	BMS current sense	Ext	Ext	Ext	Int
Output Power Management	Buck regulators	2 × 2 A FTS 6 × 1.5 A HF	2 × 2 A FTS 4 × 1.5 A HF	(2 + 2) × 2 A FTS 6 × 1.5 A HF	6 × 3 A FTS Gen2 2 × 1 A HF 3 × 2 A HF
	# LDOs	5 × 1.2 A NLDO 2 × 600 mA PLDO 4 × 300 mA PLDO 9 × 150 mA PLDO 4 × 150 mA NLDO 2 × 50 mA PLDO 2 × 10 mA LNLDO	6 × 1.2 A NLDO 2 × 600 mA PLDO 5 × 300 mA PLDO 1 × 300 mA NLDO 3 × 150 mA PLDO 2 × 150 mA NLDO 5 × 50 mA PLDO 2 × 10 mA LNLDO	5 × 1.2 A NLDO 2 × 600 mA PLDO 4 × 300 mA PLDO 9 × 150 mA PLDO 4 × 150 mA NLDO 2 × 50 mA PLDO 2 × 10 mA LNLDO	3 × 1.2 A NLDO 2 × 300 mA NLDO 4 × 600 mA PLDO 4 × 300 mA PLDO 7 × 150 mA PLDO 2 × 50 mA PLDO 2 × 10 mA LNLDO
	Power switches	6 × 100 mA LVS 1 × 300 mA LVS 1 × OTG MVS 1 × HDMI MVS	2 × 100 mA LVS	6 × 100 mA LVS 1 × 300 mA LVS 1 × OTG MVS 1 × HDMI MVS	3 × 300 mA LVS 1 × OTG MVS 1 × HDMI MVS
	5 V boost regulator	No	No	No	1.3 A Sync
	Ext. buck/boost support	Yes	Yes	Yes	Yes
	Negative charge pump	1 × 200 mA NCP	–	1 × 200 mA NCP	–

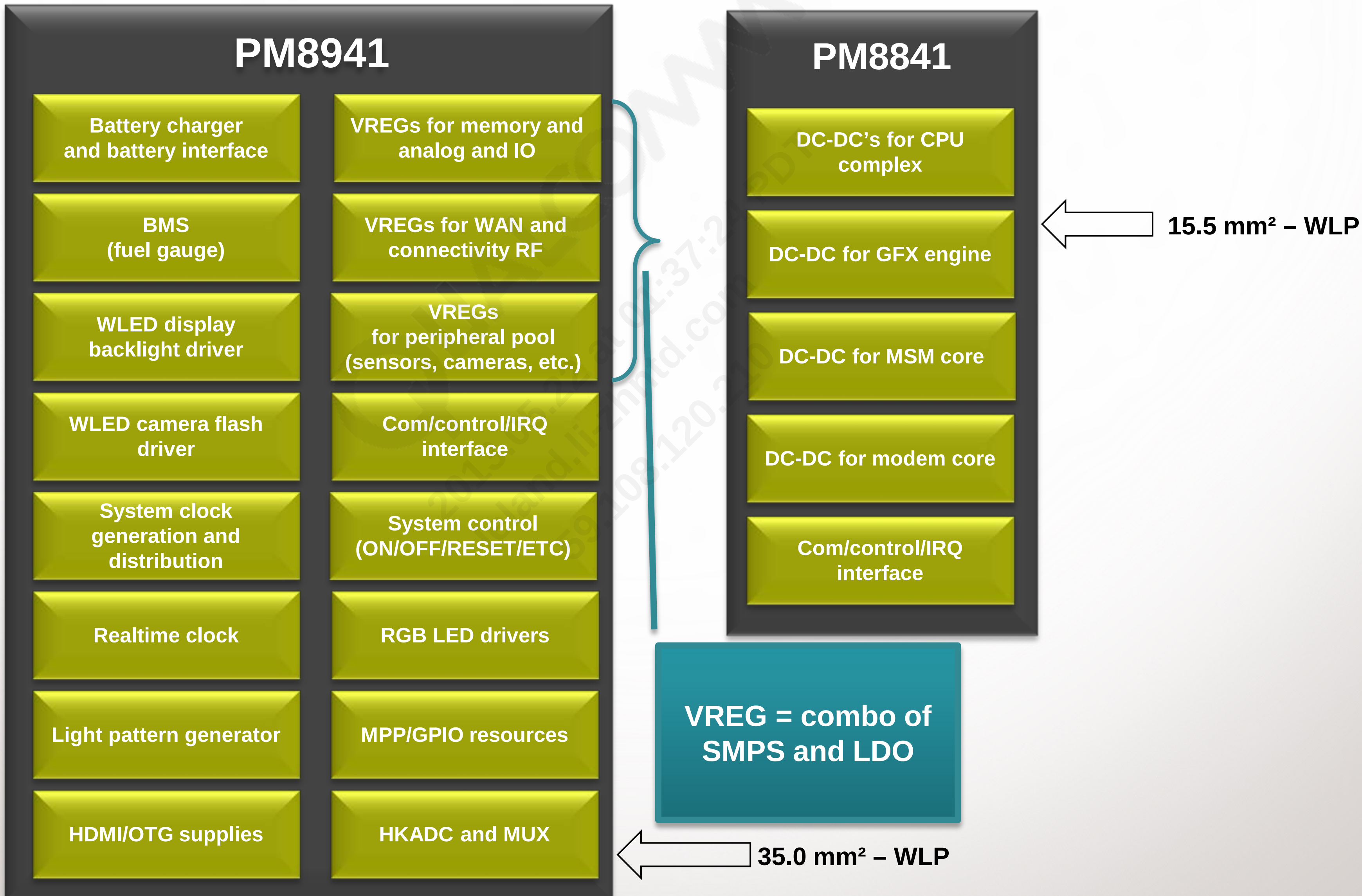
PM8x41 Features (3 of 4)

	Features	PM8921	PM8038	PM8x21	PM8x41
Housekeeping	System clock generation	19.2 XO	19.2 XO	19.2 XO	19.2 XO
	System clock buffers	5	5	5	3 RF 2 BB 1 differential
	Sleep clock generation	XO/586	XO/586	XO/586	XO/586
	32 kHz buffers	3	3	3	3
	RTC (XO/586 when device is on, cal RC when device is off)	Yes	Yes	Yes	Yes
	MP3 slow clock buffer	Yes	Yes	Yes	Yes
	HKADC/XOADC	Yes	Yes	Yes	Yes
	UICC level translator	2	–	2	–

PM8x41 Features (4 of 4)

	Features	PM8921	PM8038	PM8x21	PM8x41
IC interface and value added	IRQ manager	Secure	Secure	Secure	SPMI
	Serial I/F	SSBI 2.0	SSBI 2.0	SSBI 2.0	SPMI
	Plug and play compliant	–	–	–	Yes
	PBS (programmable boot sequencer)	–	–	–	Yes
	Cable detector	2	2	2	1
Audio	Loudspeaker driver	No	Mono 1W D+	No	No
	Speaker bypass	No	Yes	No	No
	OTHC (microphone bias)	3	–	3	–

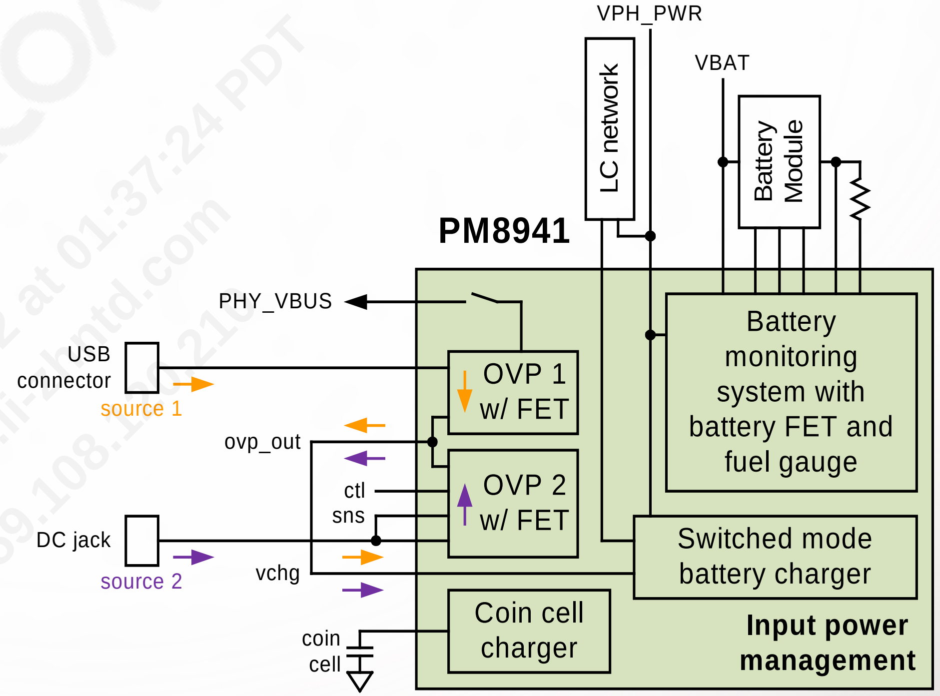
Functional Partitioning



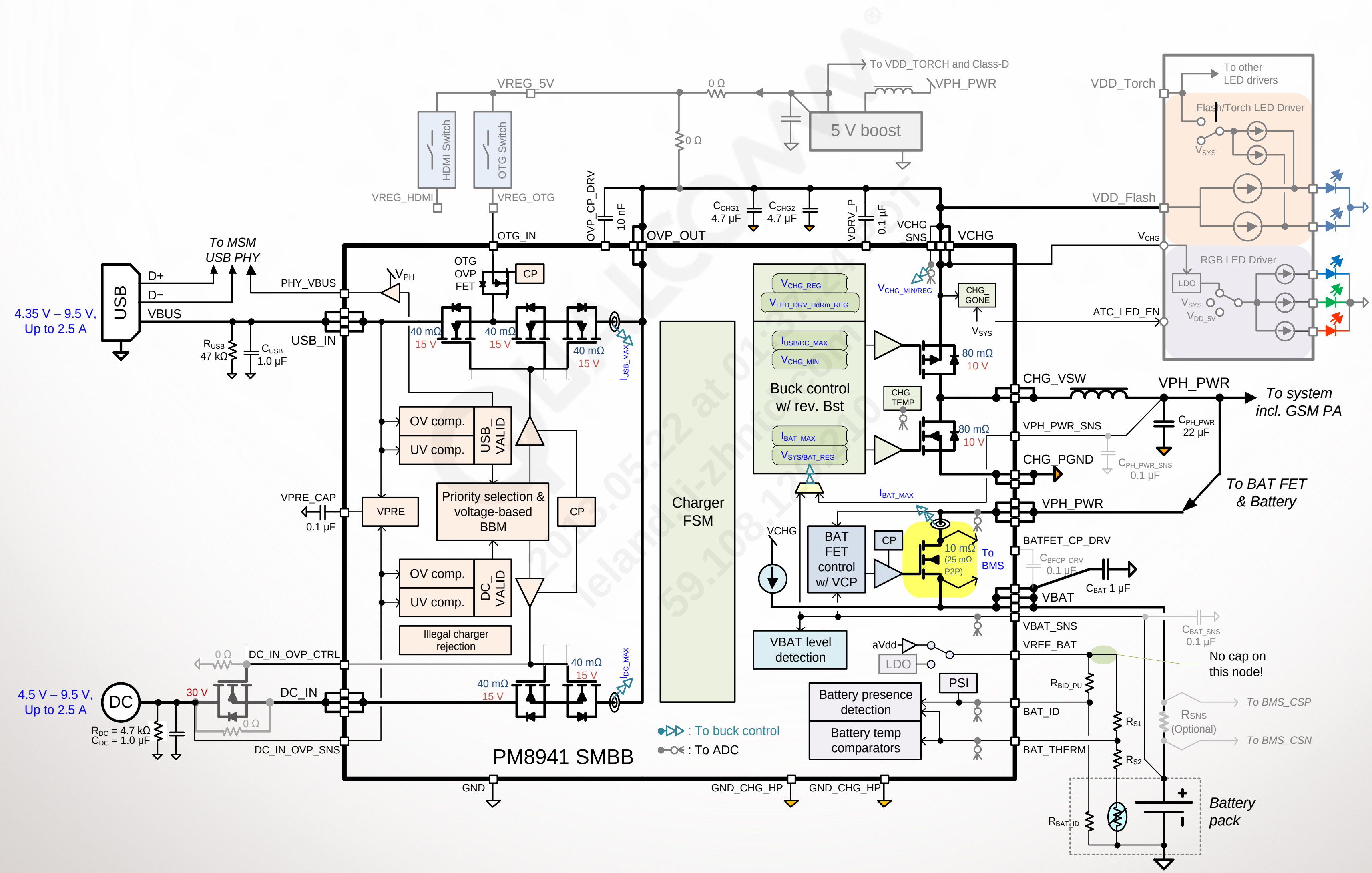
Input Power Management

Input Power Management Content

- Switch-mode battery charger with reverse boost (SMBB) architecture and summary
- Dual-charger support and overvoltage protection (OVP)
- Fast switching paths
- High-current IR drop compensation
- Charging flow diagram
- Autonomous charging
- Charger control loops
- Safety features
- Buck efficiency
- Reverse boost mode and efficiency
- SMBB schematic and layout
- Integrated battery FET
- Battery temperature monitoring (BTM)
- Battery presence detection (BPD)
- Voltage collapse protection (VCP)
- Battery monitoring system (BMS)



SMBB Architecture and Feature Summary (1 of 2)



SMBB Architecture and Feature Summary (2 of 2)

Dual charging paths with fast automatic charging path switching

- Fully integrated USB charging path with +30 V OVP FET; 4.35 V–9.5 V input; USB 2.0 and USB battery charging specification 1.2-compliant
- DC charging path with integrated +15 V OVP FET for input current sensing and reverse current blocking; 4.5 V–9.5 V input; allows an optional external OVP FET to support +30 V OVP

Fully integrated, high efficiency switch-mode charger for single-cell lithium-ion batteries

- Up to 3.0 A current to system plus battery
- 3.2 MHz switching frequency allows for a small-size inductor (i.e., 3225)
- Efficiency: 90% at 1.0 A I_{CHG_OUT}; 85% at 2.5 A I_{CHG_OUT}
- High-current charging IR drop compensation

Reverse-boosting mode to provide a 2 A max to V_{CHG}

- Supports USB OTG, HDMI switch, and LED drivers (torch, home row lighting, RGB)
- Also used for flash LED driver in an adaptive mode to minimize the thermal generation

Integrated BAT FET

- Battery current sensing across the BAT FET; eliminating the external R_{SENSE}
- HW battery presence detection and temperature monitoring with JEITA-specification compliance

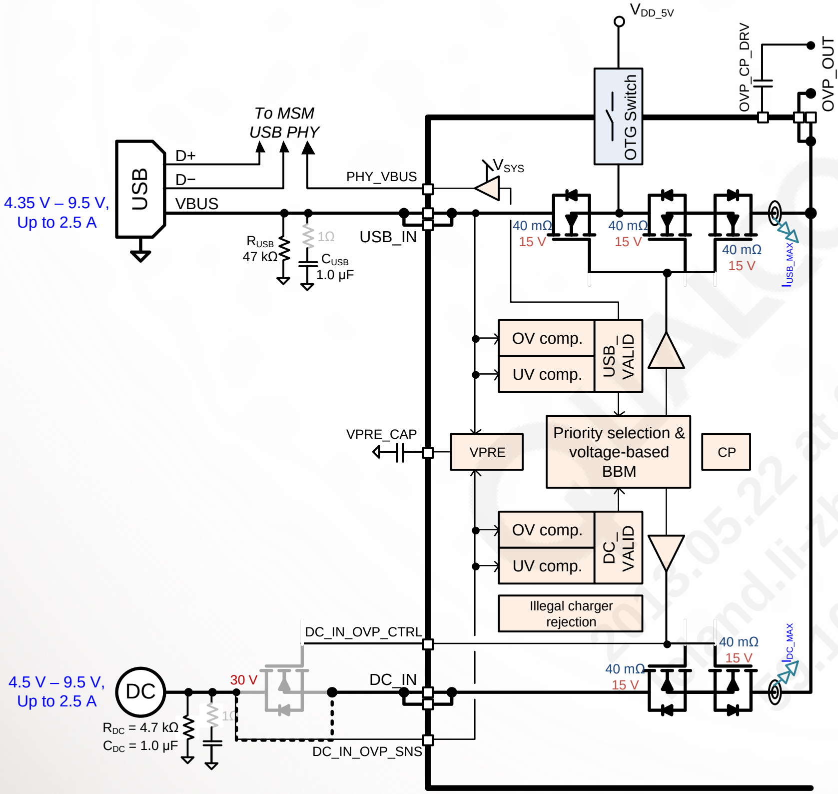
Charger FSM supports autonomous charging (trickle → CC/CV → termination → recharge)

- Software-initiated, hardware-managed charging; allows for hardware-controlled auto-trickle charge (ATC), if necessary
- Hardware timers for battery charging safety; one-time write registers, and battery overvoltage detection

USB support

- Integrated USB OTG switch supporting simultaneous DC charging and USB OTG
- USB R_{ID} detection with ACA support

Dual Charging Support and Over-Voltage Protection (OVP)



USB charging path

- Fully integrated 30 V OVP FET and control
- Pass up to 9.5 V for high-voltage charger
- Compliant to USB specification 2.0 and USB battery charging specification 1.2

DC charging path

- Integrated 15 V OVP FET for input current sensing and reverse current blocking for wireless charging application
- 30 V OVP with an optional external OVP FET
- If the external OVP is not used, then:
  - Float DC_IN_OVP_CTRL
  - Short DC_IN_OVP_SNS to DC_IN

External charger detection

- If external charger is used instead of SMBB, connect DC_IN_OVP_CTRL to GND

Automatic charging path selection with software-programmable priority

Fast-charging path switching

- To minimize the risk of a system brownout when switching the charging path with a weak battery

Fast Switching Between Charging Paths

SMBC hardware automatically switches between charging sources under the following conditions:

- A higher-priority source becomes available
- Software changes the priority when both sources are available
- The high-priority source is removed

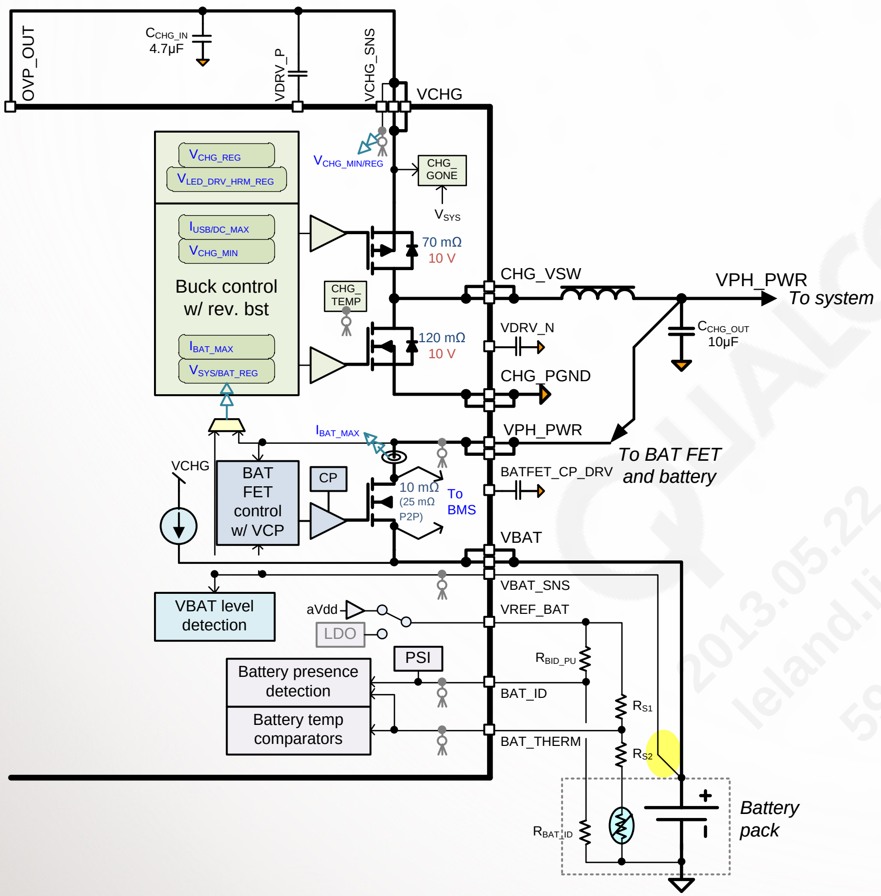
This fast-switching feature uses a voltage-based break-before-make scheme

- Addresses possible brownout (temporary system crash) when switching between sources during charging with a weak or disconnected battery

Charging source switching time
(whether from a low-voltage source to a high-voltage source or vice versa)

- Programmable from 60 to 120 μs in 20 μs steps
- With an 80 μs default, 50 μF capacitance on VPH_PWR is needed to prevent 4.2 V from dropping below 3.2 V (default weak battery threshold), during a charging source switchover, with a 1 A system load.

High-current Charging IR Drop Compensation



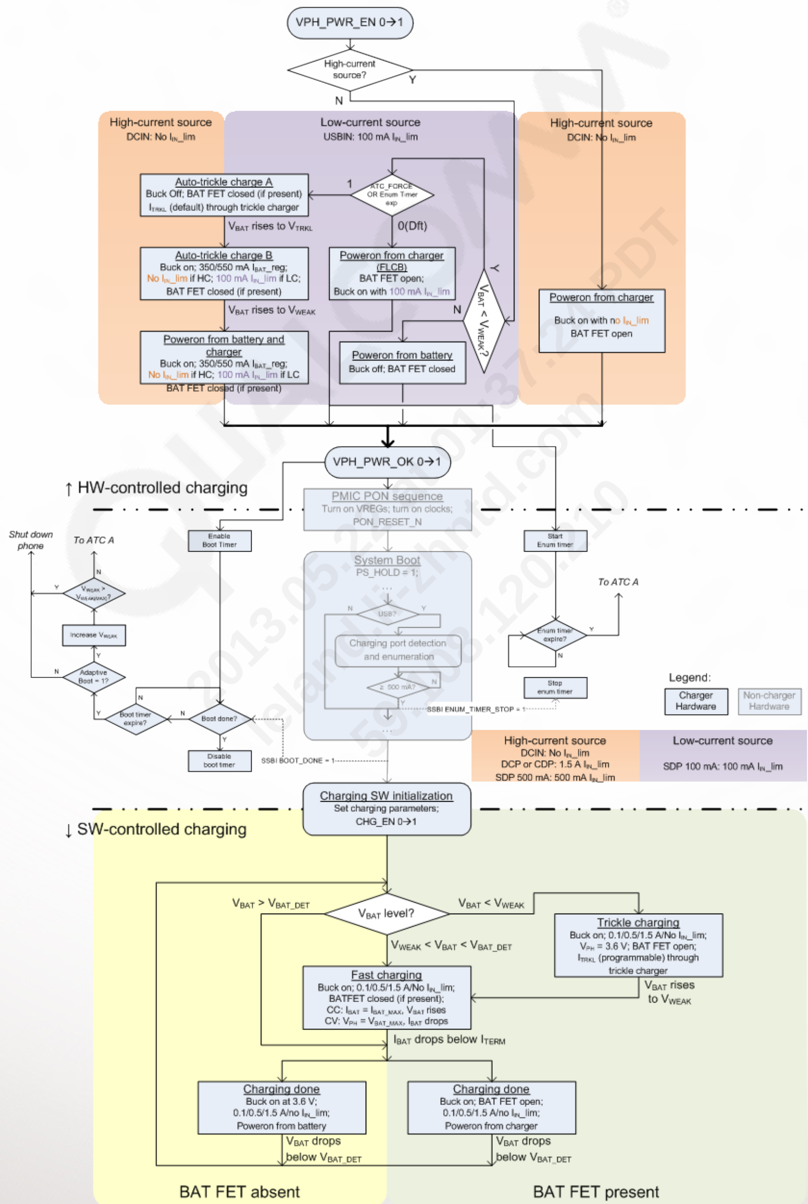
Issue description

- Extra resistance from the charger output to the battery can easily add up close to 100 mΩ PCB routing, BAT FET Rds(on), current sensing resistor, contact resistance, etc.
- 3 A charging current results in a 300 mV IR drop
- Charger leaves CC charging prematurely, resulting in a longer charge time

PM8941 solution:

- Charger regulates V_{BAT} (Kelvin-sensed) during CC/CV charging, instead of V_{SYS}

Charging Flow Diagram



Autonomous Charging (1 of 2)

Software-initiated, hardware-managed autonomous charging

- The charger does not start charging the battery until software initiation, unless an auto-trickle charge (ATC) is necessary.
- Once initiated, the charger FSM hardware autonomously manages the charging (trickle → CC → CV → termination → recharge) with software visibility/configurability/controllability.

Two-step ATC

- The battery voltage level (VTRKL), below which the battery has to be trickle-charged for safety reasons, is generally lower than the voltage level (VWEAK), above which the phone can boot.
- To save time spent in ATC, charge the battery with a higher current once VBAT rises above VTRKL:
  - ATC A:
    - Buck off, BAT FET open; the trickle charger charges the battery with ITRKL to VTRKL
    - ITRKL: 50 mA–200 mA programmable, 10 mA steps, ±10% of setting ±5 mA accuracy, 50 mA default
    - VTRKL: 2.05 V–2.8 V programmable, 50 mV steps, ±50 mV accuracy, 2.8 V default
  - ATC B:
    - Buck on, BAT FET closed; the main charger charges the battery with 300 mA/500 mA to VWEAK
    - VWEAK: 2.1 V–3.6 V programmable, 100 mV steps, ±50 mV accuracy, 3.2 V default

Autonomous Charging (2 of 2)

Trickle charging

- Necessary if coming from FLCB (with BAT FET)
- Buck on, BAT FET open, system ON, and supplied by charger
- Trickle charger charges the battery with ITRKL via VBAT pin, until VBAT rises to VWEAK

Fast charging

- Constant-current (CC) charging if VWEAK < VBAT < VBAT_MAX
  - Charger controller regulates the maximum current (IBAT_MAX) into the battery; VBAT rises
  - IBAT_MAX: 300 mA–3000 mA programmable, 50 mA steps, ±5% of setting ±50 mA accuracy, 300 mA default
- Constant-voltage (CV) charging if VBAT reaches VBAT_MAX
  - Charger controller regulates VPH_PWR = VDD_MAX; IBAT drops gradually
  - VDD_MAX: 3.4 V–4.5 V programmable, 20 mV steps, ±30 mV accuracy, 3.6 V default

Charging termination

- The current into the battery is continuously monitored; when sensing IBAT < ITERM (with deglitching), charging is terminated
  - ITERM: 35 mA–276 mA programmable, 17.28 mA steps, ±25 mA accuracy, 207 mA default
- With BAT FET, the buck remains on and supplies the system; BAT FET is open to isolate the fully charged battery.
- Without BAT FET, the system run from the battery; the buck remains on to prevent system brownout if the battery is removed.

Automatic recharge

- When detecting VBAT falls below a programmable threshold, FSM automatically recharges the battery.
  - VBAT_DET: 3.3 V–4.7 V programmable, 20 mV steps; ±30 mV accuracy, 4.1 V default

Charger Control Loops

Charger control loops

- VSYS/VBAT regulation during trickle or CV charging
  - VDD_MAX: 3.4 V–4.5 V programmable, 10 mV steps, monotonic ±30 mV accuracy, 3.6 V default
- Maximum IBAT regulation (sensed over BAT FET) to limit the maximum current into the battery during CC charging
  - IBAT_MAX: 300 mA–3000 mA programmable, 50 mA steps, ±5% ±50 mA accuracy, 300 mA default
- Minimum VIN limiting to prevent deep voltage collapse on current limited charger
  - VIN_MIN: 3.4 V–9.6 V programmable, 50/100 mV steps, ±2% accuracy, 4.5 V default
  - SMBB also provides support of hardware automatic input current limiting (AICL)
- Maximum IIN limiting to limit the maximum input current for USB compliance
  - IUSB_MAX: 100/150/200/300/400 to 2500 mA programmable, 100 mA default

Each loop converts the control variable (either a voltage or a current) to a duty cycle control input that drives the PFET and NFET output stages.

Not all control loops are active at any one time, though multiple loops can be active simultaneously.

Regardless of the number of loops that are active, the loop demanding the lowest duty cycle (lowest output voltage or current) is always selected – only one control loop is closed.

The two input control loops (USB current and charger voltage) limit the charger's input current, thereby preventing input voltage collapse.

Safety Features

Safety timers

- Hardware timers that limits the maximum time allowed for trickle charging and the complete charging cycle
- Stops charging (and generates interrupt) if the timer times out

Charger watchdog timer (one-time write register)

- Hardware timer to ensure the charging control software remains alive
- Stops charging (and generates interrupt) if the timer times out
- 0 to 32 sec programmable

VBAT_SAFE and IBAT_SAFE (one-time write registers)

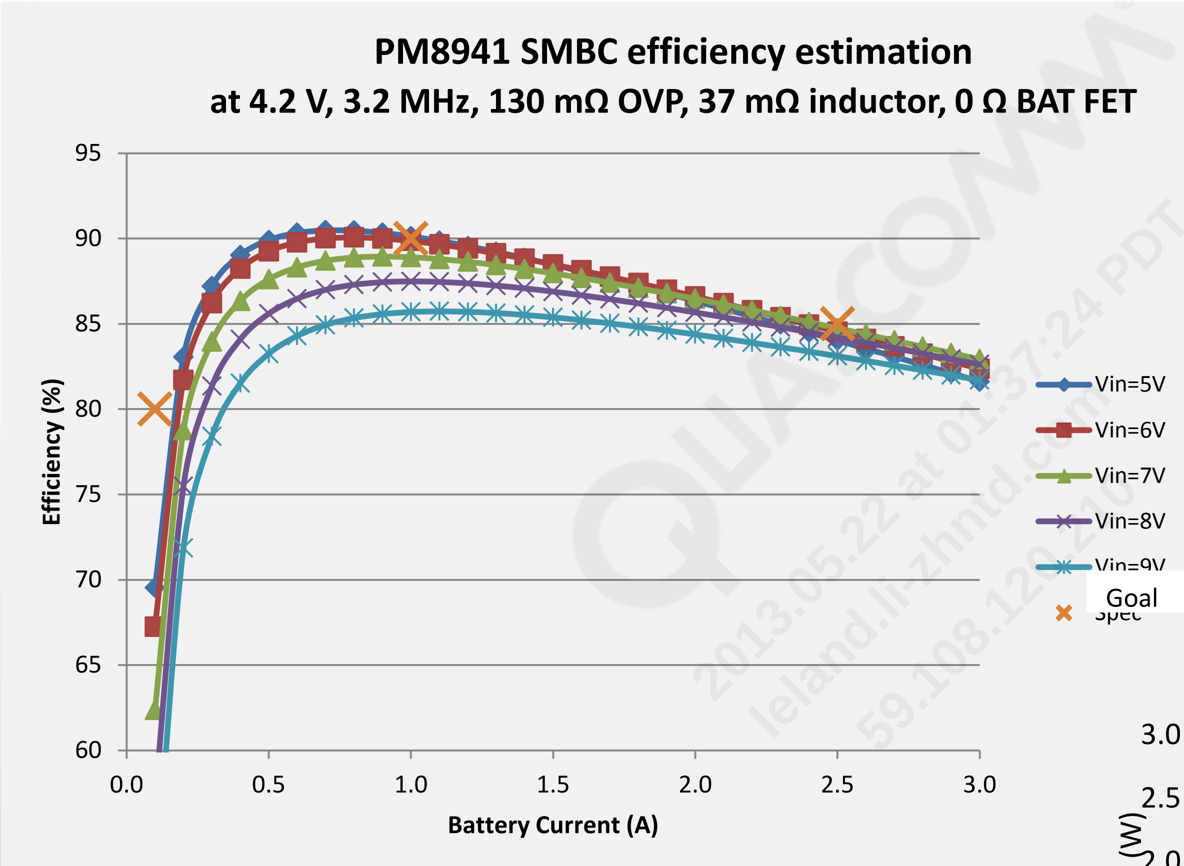
- To limit maximum allowed battery charging voltage/current, and prevent malware
- Write access to these registers are enabled after power on reset, and are disabled after being written once

Battery overvoltage detector

- VBAT_DET comparator is reused to monitor battery overvoltage condition during fast charging
- Interrupt is generated if the battery overvoltage condition is detected

Thermal management

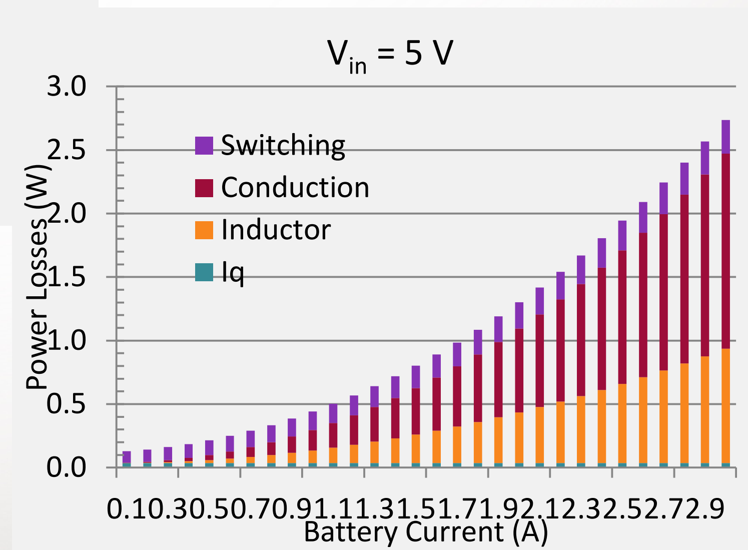
SMBB Buck Efficiency Estimation



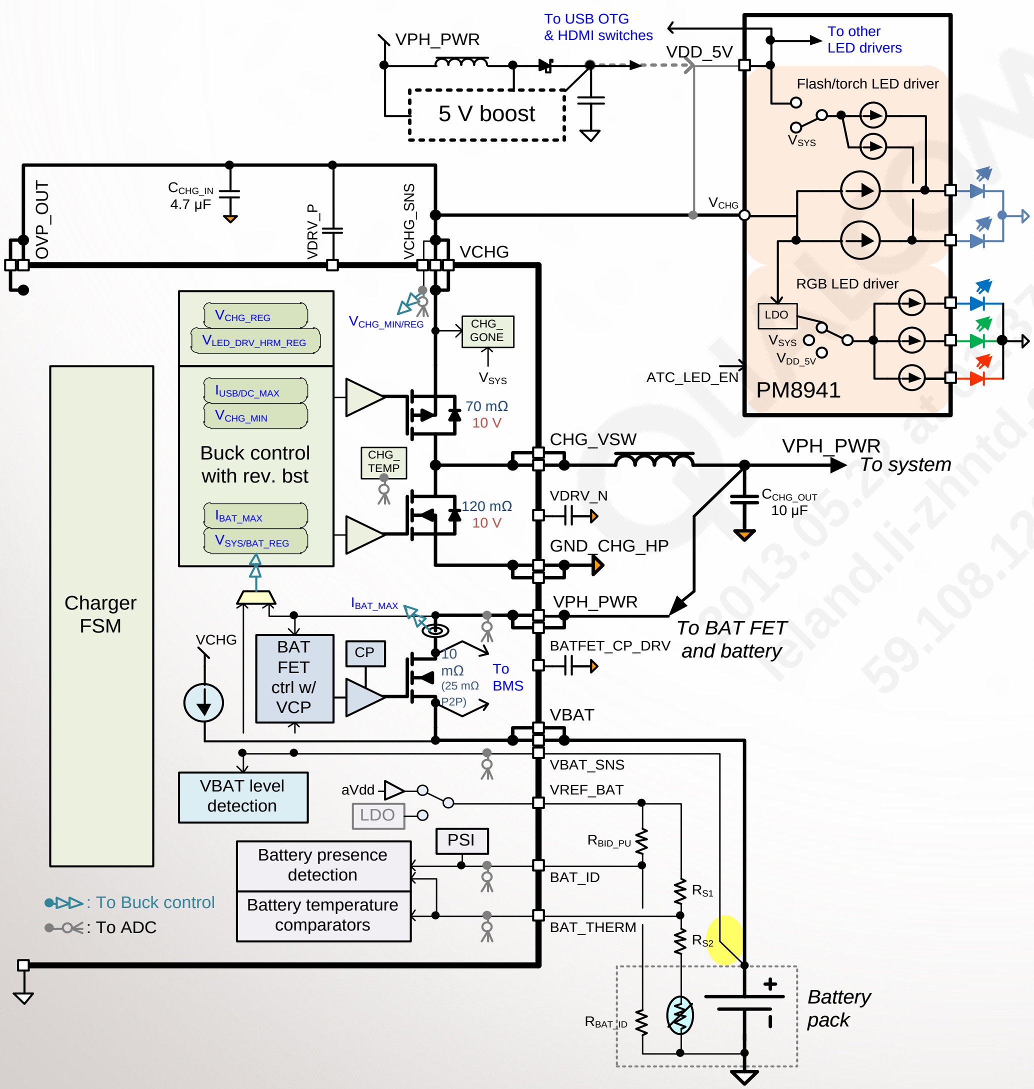
PM8941 SMBC efficiency goals:

- 80% at 100 mA I_{out}
- 90% at 1.0 A I_{out}
- 85% at 2.5 A I_{out}
- $V_{USBIN/DCIN}$ = 5 V, V_{SYS} = 4.2 V
- Typical part, room temperature

SMBC power-loss breakdown



SMBB Reverse Boost Mode



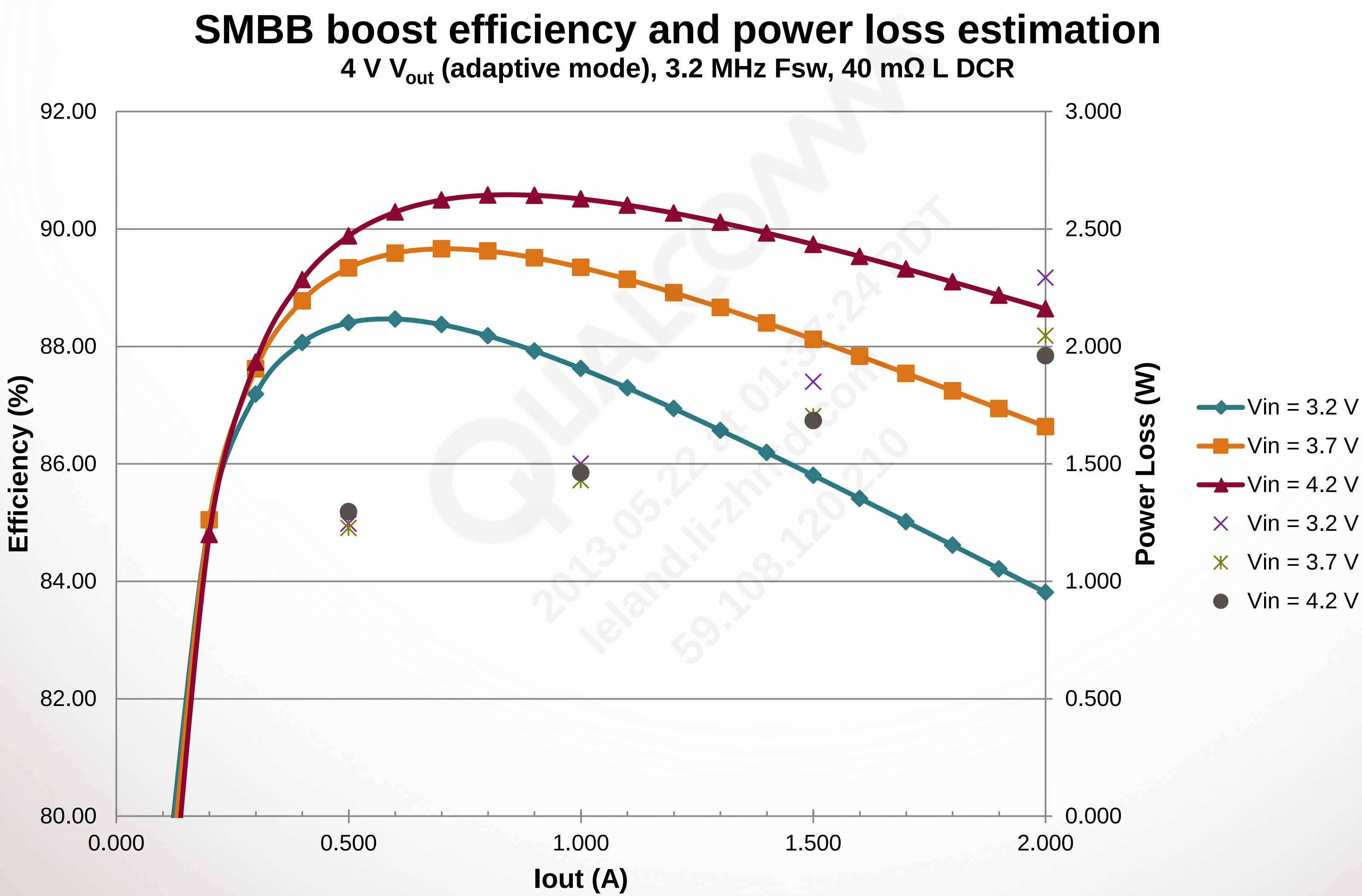
The SMBB runs in reverse boost mode to provide a 4 V to 5 V supply for:

- Flash LED driver
- Torch/home row lighting/RGB LED drivers
- USB OTG switch and HDMI switch

Supports an adaptive mode that regulates the maximum headroom of the Flash LED driver

- To minimize the voltage drop across the flash LED driver and its thermal consumption

SMBB Reverse Boost Efficiency and Power Loss Estimation (1 of 2)

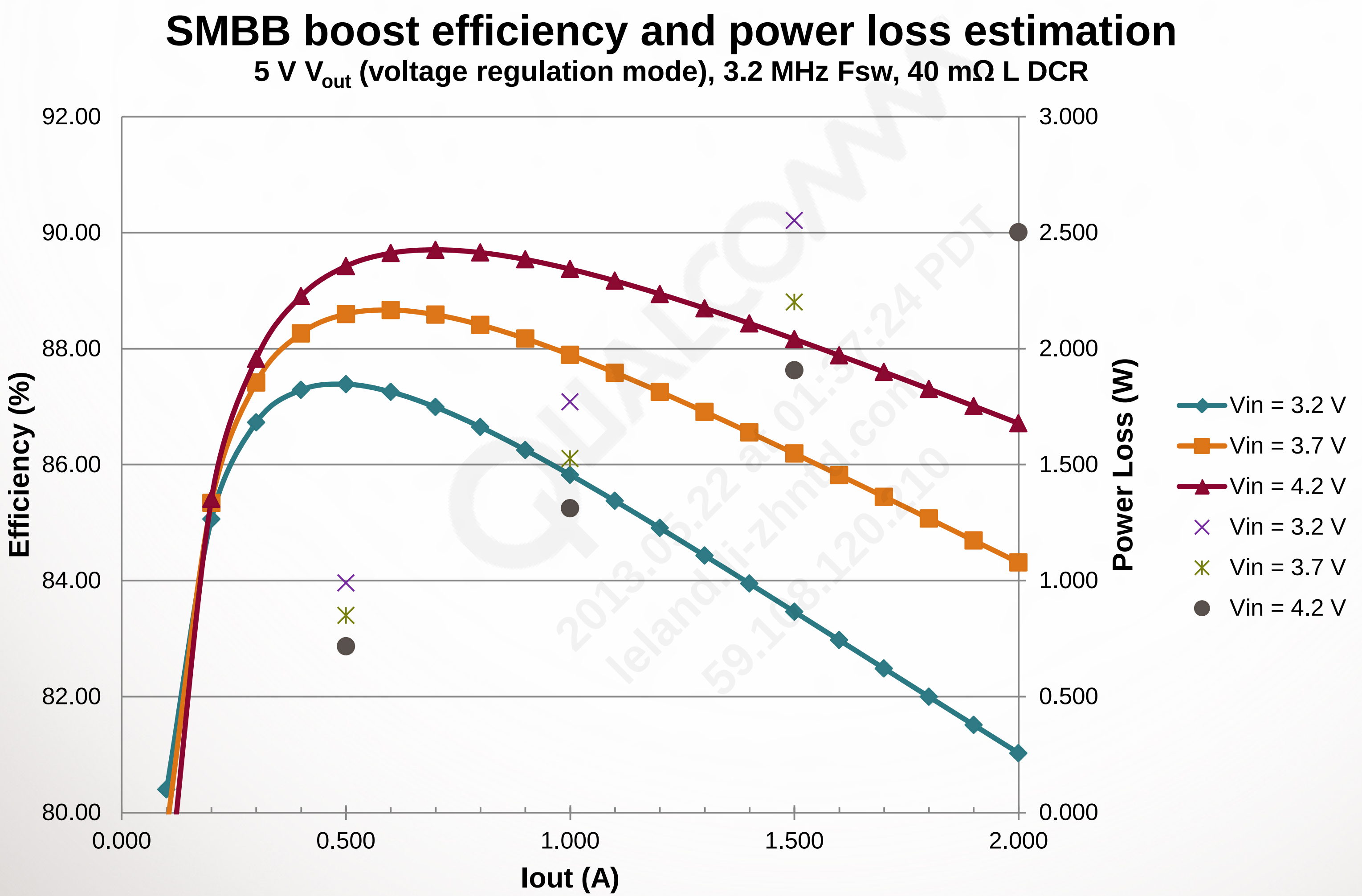


4 V output (adaptive mode)

Power loss includes the loss in the flash LED driver.

If 2 W heat dissipation is allowed, the maximum boost current is 2 A with 3.7 V V_{BAT}.

SMBB Reverse Boost Efficiency and Power Loss Estimation (2 of 2)

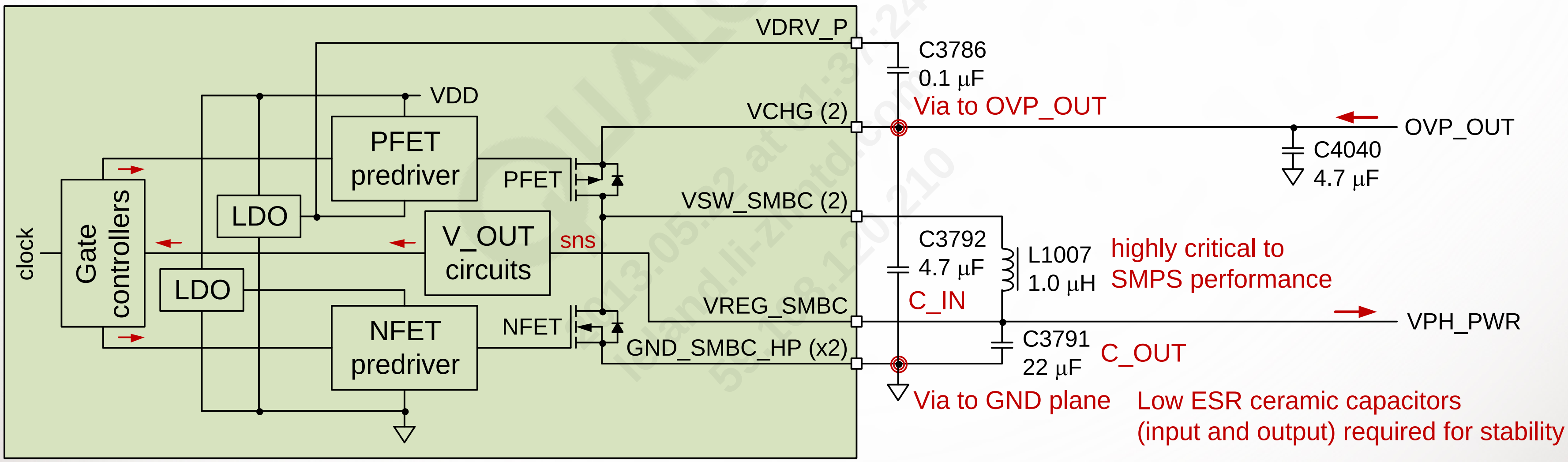


5 V output (voltage regulation mode)

Power loss include 1 W budgeted for the flash LED driver.

If 2 W heat dissipation is allowed, the maximum boost current is 1.5 A with 3.7 V V_{BAT}.

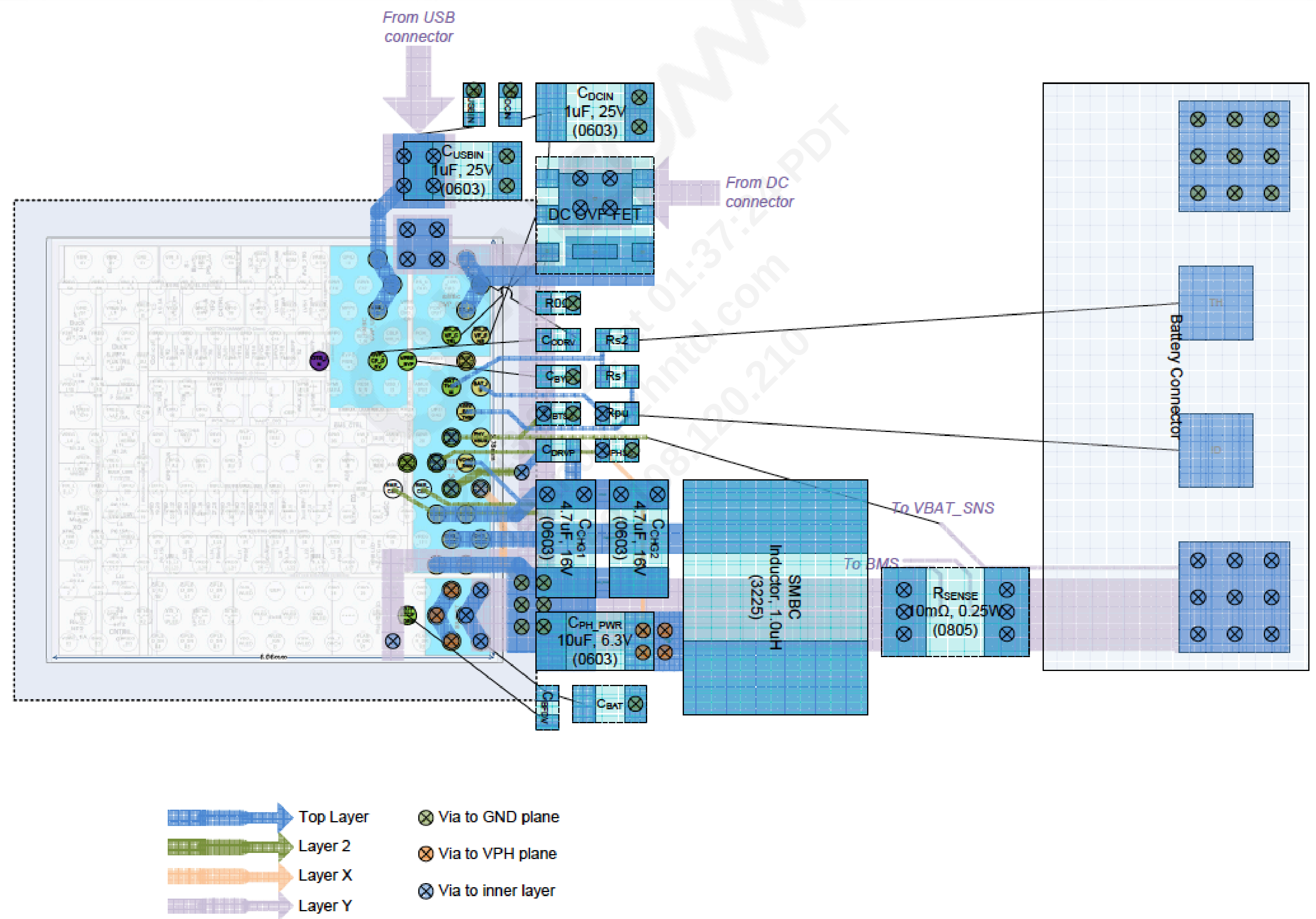
Example SMBB Schematic



Note: Refer to latest version of the *MSM8974 Preliminary Baseband Reference Schematic* (80-NA437-41) for the SMBB schematic.

SMBB Layout Guidelines (1 of 2)

Example SMBB Layout



SMBB Layout Guidelines (2 of 2)

Placement:

- Minimize switching loop. Place charger input capacitors, output capacitors, and inductor close to each other.
- Place the DRV_P capacitor close to the charger input capacitor.

Grounding:

- Connect GND of charger input capacitors, output capacitors, and GND_CHG_HP pins of PMIC together. Connect the common point directly to the main GND using multiple vias.

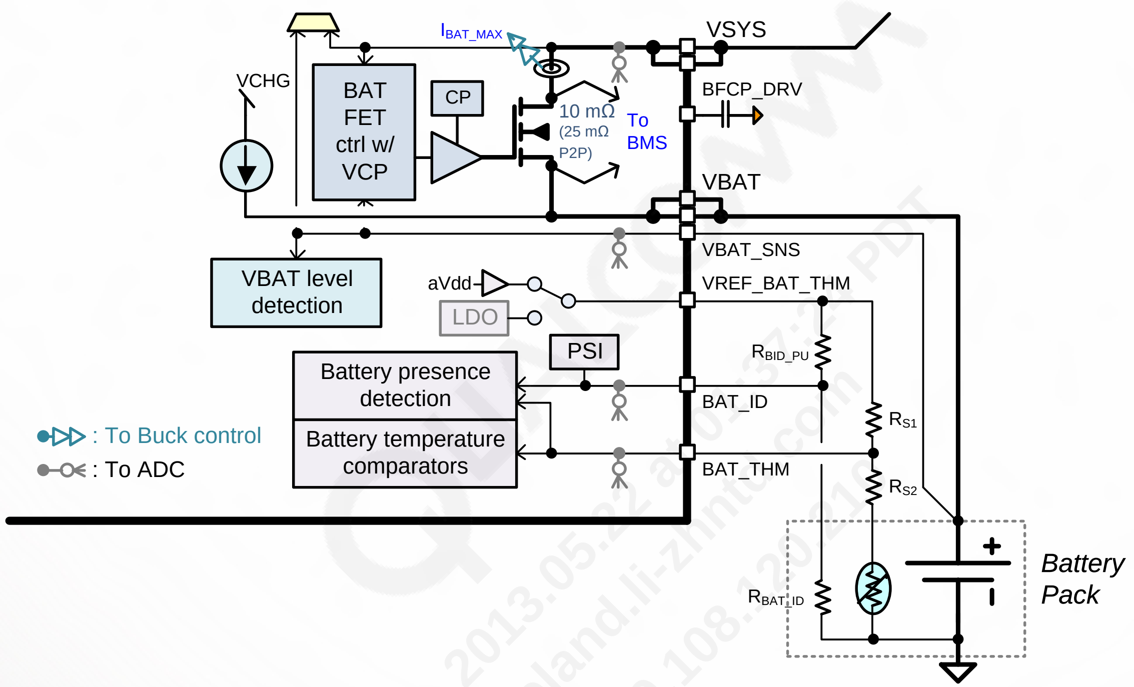
High current paths:

- Use a thick trace from USB connector to USB_IN pins and DC connector to DC_IN pins of the PMIC.
- Use a thick trace from OVP_OUT pin to VCHG pin of PMIC.
- Use a thick trace from VCHG to VDD_FLASH pin of PMIC.
- Use a thick and short trace from VSW_SMBC pin to inductor.
- Use a thick trace from battery connector to VBAT pin.

Sensing:

- Connect the VBAT_SNS pin to the battery connector using a thin trace.
- Connect the VCHG_SNS pin to VCHG using a thin trace.
- Connect VREG_SMBC to the output of SMBB using a thin trace.

Integrated Battery FET

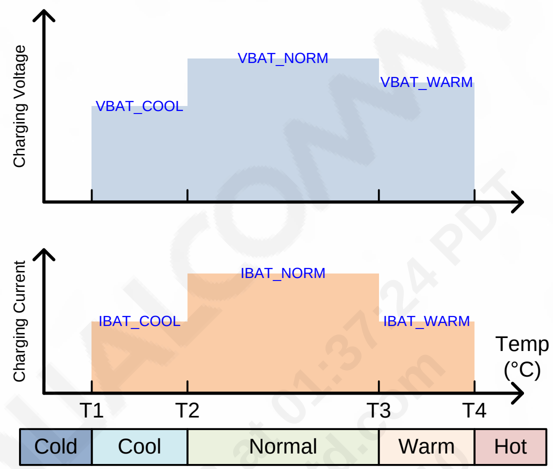


Integrated NMOS BAT FET

- Battery current sensed across BAT FET Rds(on) for SMBC IBAT_MAX limiting and BMS; eliminating the external I_{BAT} sensing resistor.
- BAT FET Rds(on) regulated at 10 mΩ ± 2% across temperature (-30°C to 125°C) and V_{BAT} range (2.5 V to 4.5 V) after trim; 25 mΩ max pin-to-pin.

Hardware battery presence detection and JEITA-compliant battery temperature comparators PMIC serial interface (PSI) for the digital battery interface.

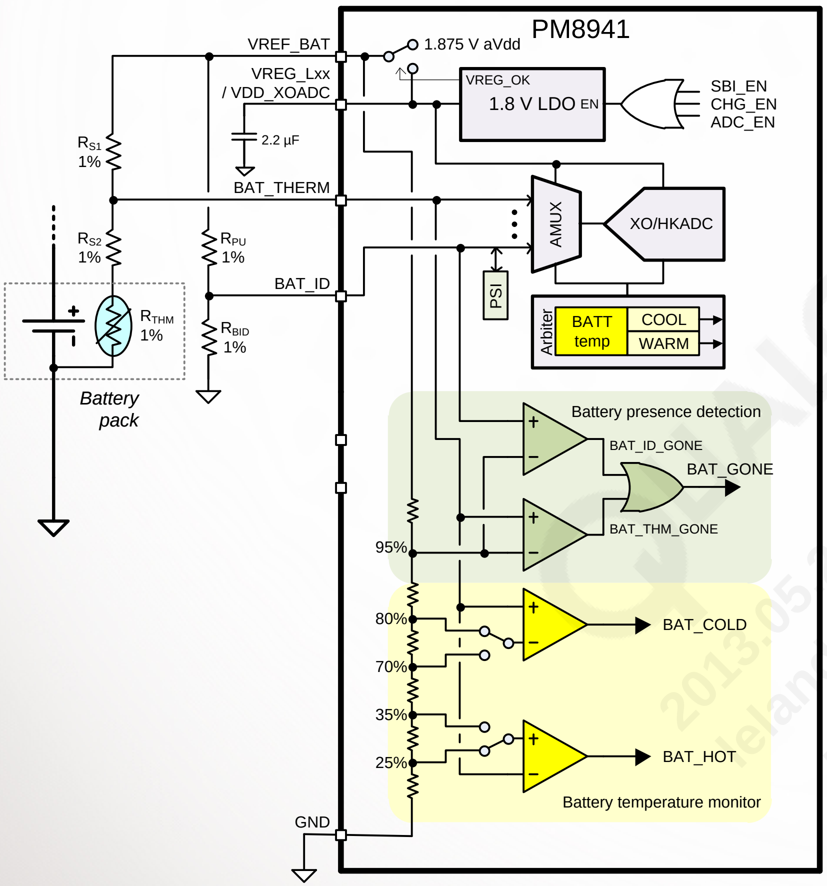
JEITA Specification – Battery Temperature Dependent Charging



JEITA: *A Guide to the Safe Use of Secondary Lithium Ion Batteries in Notebook-type Personal Computers*

- Reduced maximum battery charging voltage and current at extended battery temperature ranges
  - NORMAL region (T2 < TBAT < T3): optimal charging with VBAT_NORM and IBAT_NORM
  - COOL region (T1 < TBAT < T2): reduced charging with VBAT_COOL and IBAT_COOL
  - WARM region (T3 < TBAT < T4): reduced charging with VBAT_WARM and IBAT_WARM
  - COLD region (TBAT < T1) or HOT region (TBAT > T4): charging is prohibited
- Mandatory in Japan after November 2011
- Actual T1, T2, T3, and T4 values vary by battery manufacturer.
- JEITA: Japan Electronics and Information Technology Industries Association

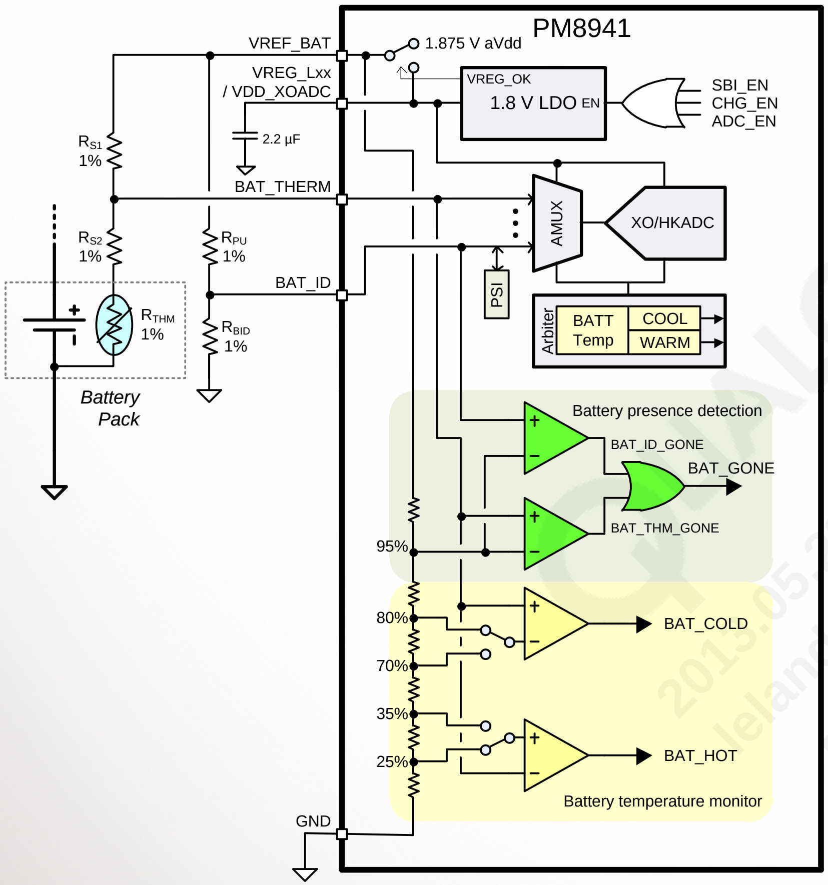
Battery Temperature Monitoring (BTM)



Enhanced BTM with JEITA compliance

- Two analog BTM comparators that monitor the cold and hot conditions
  - Four thresholds generated by internal resistor ladder
    - For charging with traditional battery temperature range, use 70% and 35% thresholds.
    - For charging with extended battery temperature range (JEITA), use 80% and 25% thresholds.
  - Using RS1 and RS2 pull-up resistors to tune the trip points
  - Battery charging is paused if either comparator asserts
- An automated digital BTM routine that monitors the cool and warm conditions
  - If enabled, battery temperature is automatically measured by the ADC Arbiter periodically (programmable up to 16 seconds).
  - The battery temperature measurement result compared with programmable cold and warm thresholds; interrupts are generated if either of the thresholds are exceeded.
  - Charging software adjusts the VBAT_MAX and IBAT_MAX accordingly.
- Battery thermistor/resistor biasing
  - VREF_BAT_THM: 1.875 V aVdd before power on; 1.8 V LDO after poweron

Battery Presence Detection (BPD)



Flexible BPD with battery thermistor or ID resistor inputs

- Battery presence is detected by sensing the presence of battery thermistor or ID resistor, whichever is inside the battery pack
  - If battery is absent, the pull-up resistors will pull BAT_THM and/or BAT_ID high.
- Two dedicated comparators for BPD
  - Battery is considered as gone, if BAT_THM or BAT_ID is above 95% of VREF_BAT_THM.
  - Interrupts are generated (after deglitching) when detecting battery insertion or removal.
  - Charging shall be stopped upon battery removal.

Battery Identification

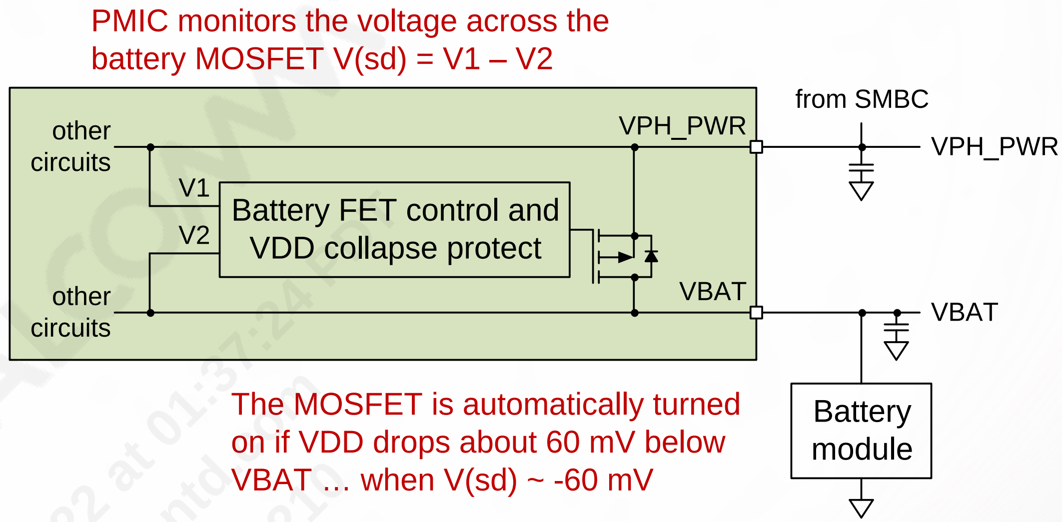
- BAT_ID is sent to PMIC AMUX/HKADC for battery ID resistor (RBID) measurement.

PMIC serial interface (PSI)

- A low-speed serial communication on the battery ID line, to transfer battery size/voltage/age information.
- BAT_ID line driven/listened by the PSI block when not measuring RBID.

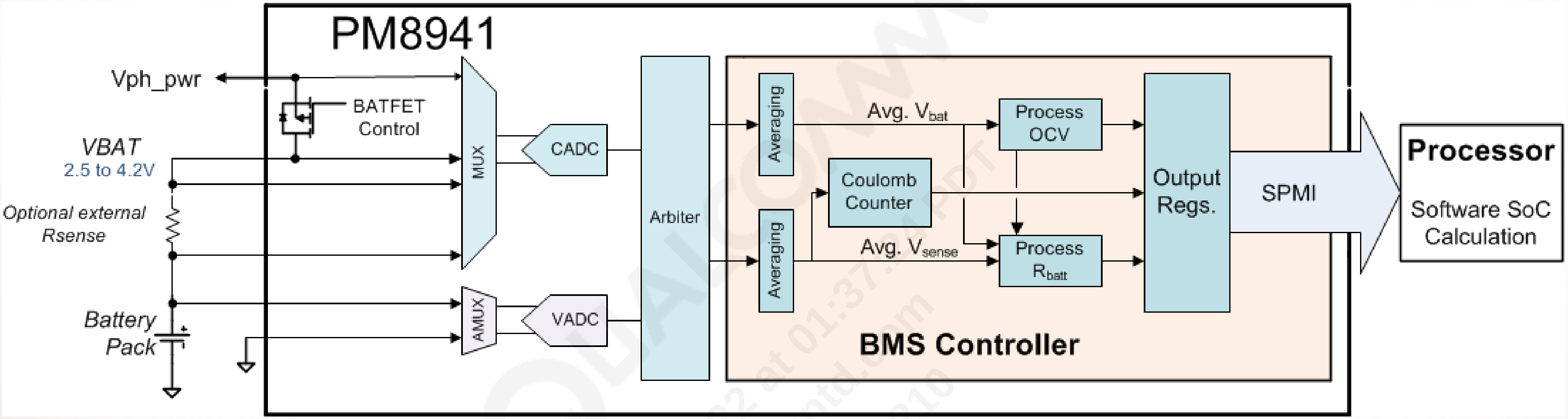
VDD Collapse Protection

The PMIC prevents a sudden load from inadvertently collapsing the VDD voltage as discussed here.



- When a valid external charger is connected, and the battery is either fully charged or too hot or cold to be charged, the battery FET is opened and the system runs off the external charger.
- If the external charger’s current limit is exceeded, voltage collapse protection (VCP) is executed.
  - If VPH_PWR drops 60 mV below VBAT, VCP is activated.
  - The battery FET is turned on, allowing the battery to supplement the external source.
    - Turn-on is a single-step, not a linearly regulated process.
  - With the added battery current, the system’s high current does not cause VDD to collapse.
  - The battery FET is turned off when the excessive current condition ends.
    - When > 100 mA flows into the battery, or
    - When 0 to 5 mA flows into the battery for at least 1 second
  - Battery FET turn-on time is fixed at 5 ms max; the turn-off time is 1 ms by default, but can be increased to 10 ms via SPMI.

Battery Monitoring System (BMS)



The CADC samples Vsense generated across BATFET (10 mΩ) → current measurement

The VADC samples Vbat → OCV measurement

- Shared use with other housekeeping functions

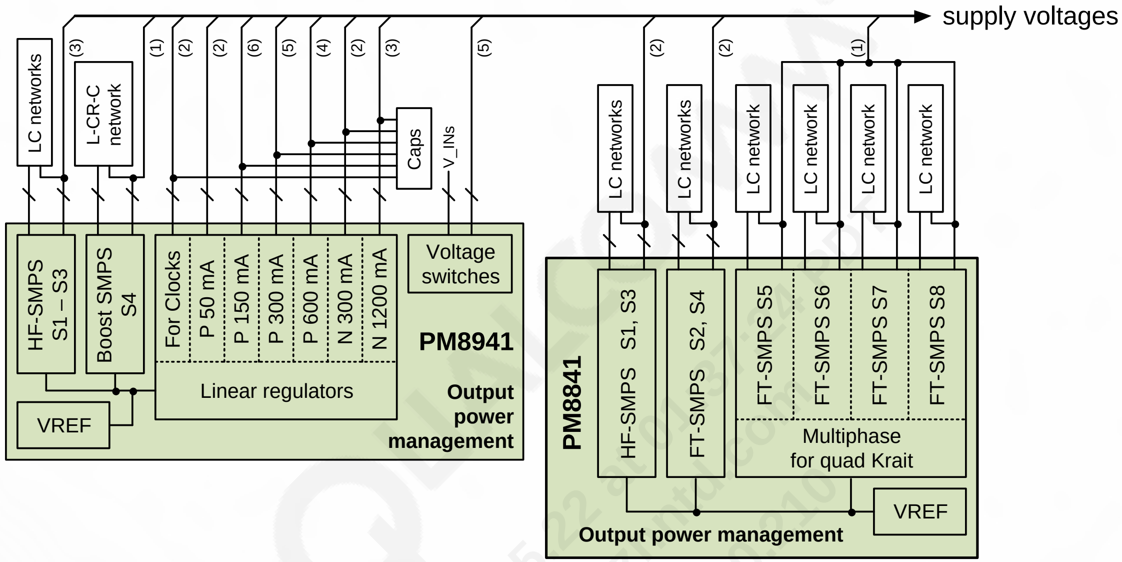
The BMS controller autonomously manages ADCs and key measurements

- Controls measurement frequency, averaging, coulomb counting, and CC resets
- All data for SoC calculations are stored, read as desired by software → no periodic software intervention
- The BMS controller utilizes a Qualcomm-proprietary algorithm.

The PMIC software reads stored data, executes software algorithms and calculates SoC.

Output Power Management

Output Power Management Content



Summary of OPM functions

MSM8974 power grid

Buck vs. buck/LDO

HF-SMPS circuits

- Operation
- Efficiency plot
- Schematic and layout

Multi-phase FT-SMPS circuits

- Krait power delivery
- Bimodal functional modes
- Schematic and layout

Boost SMPS circuits

- Operation
- Schematic and layout

SMPS switching loops and components

Low dropout (LDO) linear regulators

- Pseudo-capless LDOs

Regulator low-power modes

Internal regulator connections

External regulator connections and subregulation

Voltage switches

Need for external boost bypass

Output Power Management – Summary (1 of 3)

PM8941 page 1 of 2

Function	Circuit type	Default voltage (V)	Specified range (V)	Programmable range (V)	Rated current (mA)	Default on	Expected use
S1	HF-SMPS	1.400	1.200–1.500	0.375–3.050	2000	Y	Source for L1 and L3, L4 and L11; external connections
S2	HF-SMPS	2.150	1.800–2.250	0.375–3.050	1000	Y	WCD plus source for L5 and L7, L6 and L12 and L14 and L15; external connections
S3	HF-SMPS	1.800	1.750–1.850	0.375–3.050	2000	Y	Modem IC pad group 3, option 4 and 7; L2 and LVS; chipset and other I/Os
S4 or '5V'	Boost SMPS	5.000	4.000–5.500	4.000–5.500	1300	–	WCD spkr driver and source for 5VS1, 5VS2; option for kypd, RGB drivers
L1	NMOS LDO	1.225	1.200–1.250	0.750–1.5375	1200	Y	Modem IC pad group 1, option 4, and 7; DDR memory; eMMC
L2	NMOS LDO	1.200	1.100–1.450	0.750–1.5375	300	–	MIPI_DSI - analog
L3	NMOS LDO	1.200	1.100–1.450	0.750–1.5375	300	–	MIPI_CSI
L4	NMOS LDO	1.300	1.150–1.400	0.750–1.5375	1200	–	RFIC low -V; modem IC analog low -V
L5	Low noise LDO	1.800	1.700–2.200	–	On-chip only	–	PMIC low noise XO buffers
L6	PMOS LDO	1.800	1.700–1.900	1.500 - 4.900	150	Y	USB; WCN XO; PMIC low power XO output buffers
L7	Low noise LDO	1.800	1.700–2.200	–	On-chip only	–	PMIC XO circuits
L8	PMOS LDO	1.800	1.700–1.900	1.500 - 4.900	50	–	PMIC HKADC
L9	PMOS LDO	1.800	1.700–3.050	1.500 - 4.900	150	Y	Modem IC pad group 5, dual-voltage UIM1 (1.8 / 2.95 V)
L10	PMOS LDO	1.800	1.700–3.050	1.500 - 4.900	150	–	Modem IC pad group 6, dual-voltage UIM2 (1.8 / 2.95 V)
L11	NMOS LDO	1.300	1.200–1.400	0.750–1.5375	1200	–	WCN; modem IC ADC/DAC
L12	PMOS LDO	1.800	1.700–1.900	1.500 - 4.900	300	–	Modem IC PLLs, MIPI_DSI, MIPI_CSI, HDMI, EDP; MIPI_DSI I/Os
L13	PMOS LDO	2.950	2.750–3.000	1.500 - 4.900	150	Y	Modem IC pad group 2
L14	PMOS LDO	1.900	1.700–2.100	1.500 - 4.900	150	–	Modem IC analog - high V
L15	PMOS LDO	2.050	2.000–2.100	1.500 - 4.900	600	–	RFICs - low voltage
L16	PMOS LDO	2.750	2.600–3.000	1.500 - 4.900	150	–	Qualcomm front-end, RF switches, GPS LNA
L17	PMOS LDO	2.800	2.700–3.000	1.500 - 4.900	300	–	3D cameras - analog

PM8941 page 2 of 2

Function	Circuit type	Default voltage (V)	Specified range (V)	Programmable range (V)	Rated current (mA)	Default on	Expected use
L18	PMOS LDO	2.850	2.400–3.300	1.500–4.900	300	–	Sensors; touchscreen
L19	PMOS LDO	2.900	2.600–3.300	1.500–4.900	600	–	WCN
L20	PMOS LDO	2.950	2.750–3.000	1.500–4.900	600	Y	eMMC memory
L21	PMOS LDO	2.950	2.700–3.000	1.500–4.900	600	Y	SD/MMC card
L22	PMOS LDO	3.000	2.600–3.300	1.500–4.900	300	–	MIPI_DSI1
L23	PMOS LDO	3.000	2.600–3.300	1.500–4.900	300	–	MIPI_DSI2 or MIPI_CSI
L24	PMOS LDO	3.075	3.000–3.300	1.500–4.900	50	Y	HS-USB high-voltage
LVS1	Low V switch	1.800	–	–	300	–	Sensors; touchscreen
LVS2	Low V switch	1.800	–	–	300	–	Available
LVS3	Low V switch	1.800	–	–	300	–	3D cameras
5VS1	5 V switch	5.000	–	–	500	–	USB-OTG
5VS2	5 V switch	5.000	–	–	55	–	HDMI

1) Default voltages and power-on states may depend upon option pin (OPT_x) settings.

2) S1 and S3 current ratings assume V_{out} is less than or equal to 1.8 V. Duty-cycle limitations reduce the rated current to TBD mA for 1.8 V < V_{out} < 2.4 V.

3) S3 powers internal circuitry and must be kept at its default setting.

4) L6 and L8 power internal circuits that are limited to 1.8 V operation; they should not exceed the maximum stated in their programmable ranges. L6 is used as the internal dVdd source after powerup; its programmed voltage should not be changed, and it should not be turned off.

5) Rated current for S4, the 5 V boost circuit, depends upon the input voltage: 1.3 A for V_IN 3.6 to 4.2 V; 0.9 A for 3.0 to 3.6 V; 0.6 A for 2.5 to 3.0 V.

6) L24 is a conventional PMOS, 150 mA LDO that is powered off VPH_PWR and is used for USB. Its dropout voltage is reduced by a factor of three when its output current is limited to 50 mA.

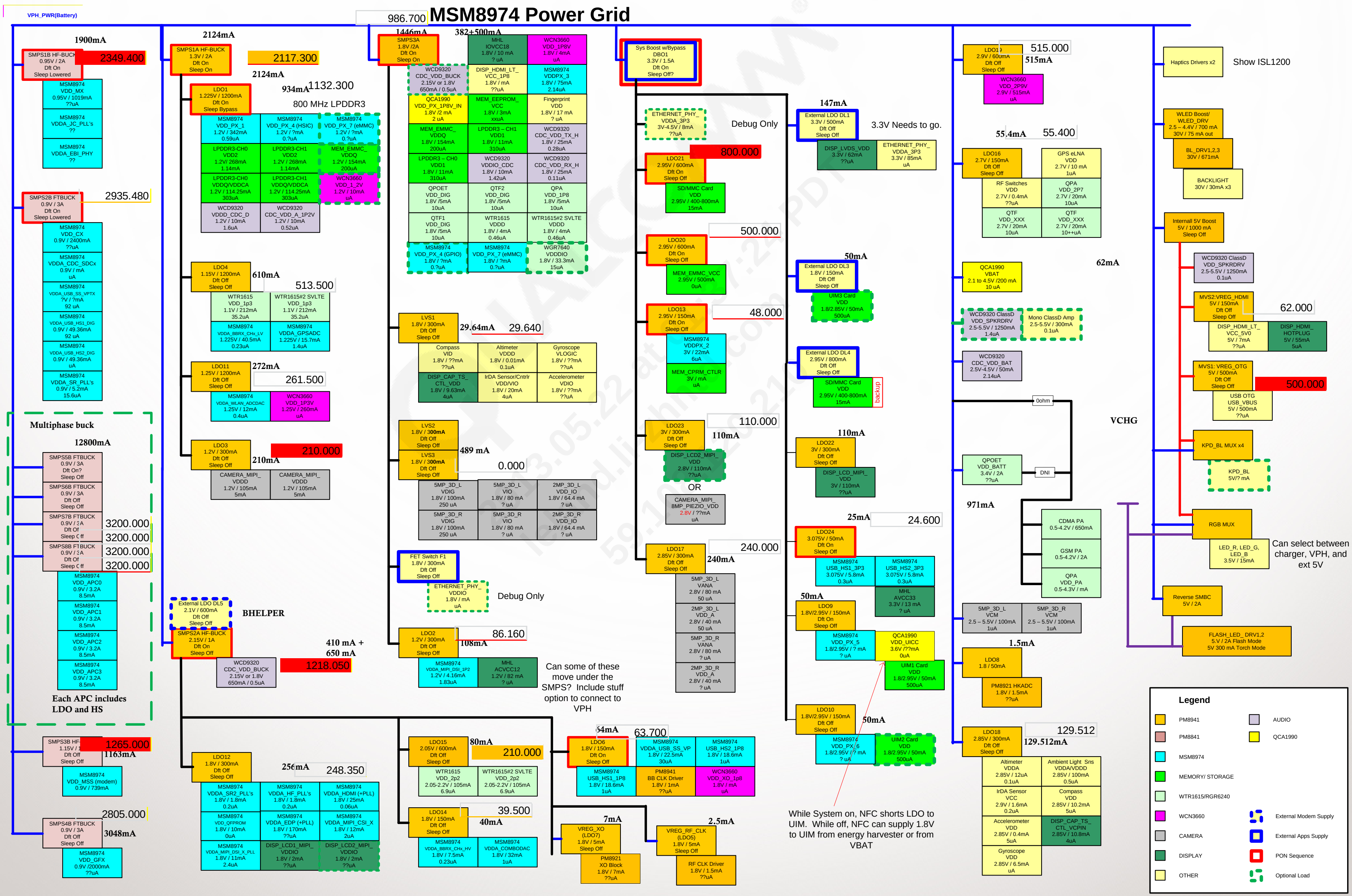
Output Power Management – Summary (3 of 3)

PM8841 page 1 of 1

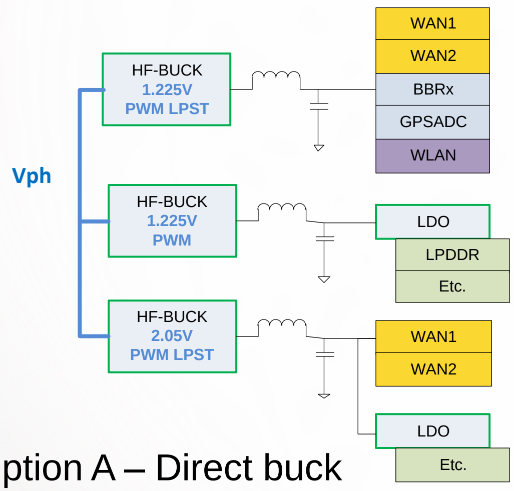
Function	Circuit type	Default voltage (V)	Specified range (V)	Programmable range (V)	Rated current (mA)	Default on	Expected use
S1	HF-SMPS	0.950	0.500–1.400	0.375–3.050	2000	Y	Modem IC memory and PLLs
S2	FT-SMPS	0.900	0.500–1.250	0.350–3.300	3000	Y	Modem IC core, SDC, and USB
S3	HF-SMPS	1.150	0.500–1.400	0.375–3.050	1000	–	Modem IC modem system
S4	FT-SMPS	0.900	0.500–1.250	0.350–3.300	3000	–	Modem IC graphics
S5	FT-SMPS	0.900	0.500–1.250	0.350–3.300	3000	–	Modem IC quad Krait microprocessors
S6	FT-SMPS	0.900	0.500–1.250	0.350–3.300	3000	–	
S7	FT-SMPS	0.900	0.500–1.250	0.350–3.300	3000	–	
S8	FT-SMPS	0.900	0.500–1.250	0.350–3.300	3000	–	

1) Default voltages and poweron states may depend upon option pin (OPT_x) settings.

MSM8974 Power Grid

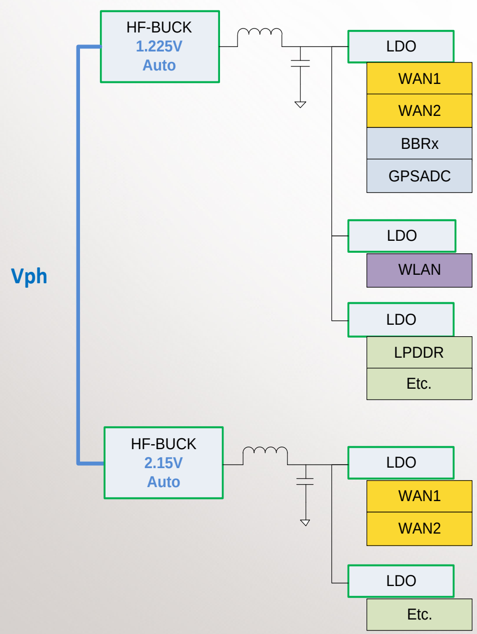


Bucks vs. Buck/LDO - Example Analysis



Option A – Direct buck

Option B – LDO subregulation



Item	Option A	Option B	Comment
Bucks	+1	+0	
BOM	+1 Ind +10 mm^2	+0	LC for additional Buck
I_{Bat_Wasted} – GSMTalk *(mA)*	4.9	2	I_{Load}=30mA
I_{Bat_Wasted} - CDMA Talk *(mA)*	7.5	6.5	I_{Load}=100mA
I_{Bat_Wasted} - LTE (CAT2) *(mA)*	10.3	12.3	I_{Load}=200mA
I_{Bat_Wasted} - SV-LTE *(mA)*	14	17.3	I_{Load}=300mA
I_{Bat_Wasted} – GPS *(mA)*	3.8	1.3	I_{Load}=20mA
I_{Bat_Wasted} – WLAN *(mA)*	3.2	1.1	I_{Load}=15mA
Noise – GSM *(mV_{RMS})*	0.25	0.35	BW: 0-100kHz, I_{Load}=30mA
Noise - CDMA Talk *(mV_{RMS})*	0.72	1.4	BW: 0-2MHz, I_{Load}=100mA
Noise - LTE (CAT2) *(mV_{RMS})*	3.1	2.1	BW: 0-10MHz, I_{Load}=200mA
Noise - SV-LTE *(mV_{RMS})*	3.2	2.4	BW: 0-10MHz, I_{Load}=300mA
Noise – GPS *(mV_{RMS})*			BW: 0-1MHz, I_{Load}=20mA
Noise – WLAN *(mV_{RMS})*	2.8	1	BW: 0-10MHz, I_{Load}=15mA

With a LDO subregulated RF, the system can work with a single 1.3 V buck instead of two. This results in reduction of die area, PWB area, and BOM cost.

The LDO subregulation provides sufficient suppression of buck noise and spurs to allow running buck in Auto mode. This results in significantly better buck efficiency below ~100–150 mA load current.

Improving RF noise sensitivity and buck/LDO output noise can now be turned into power savings by reducing LDO headroom.

Provides flexibility to tradeoff power and RF performance post silicon, reducing need for re-spin.

I_{bat} wasted based only on WAN loads

HF-SMPS – Operational Details

PM8941 and PM8841 have second-generation HF-SMPS (PM8921 had first-generation)

The second-generation HF-SMPS supports all features of the first-generation HF-SMPS

- Better transient response
- Slow start feature
- Current limiting
- Operating modes
  - Pulse width modulation (PWM)
    - Current-mode constant-frequency PWM control
    - Delivers the specified rated current to the load
    - Pulse skipping
  - Pulse frequency modulation (PFM)
    - The power switch is only turned on when the output voltage dips below a threshold.
    - Main advantage: maintains high efficiency even at light loads
  - Auto mode
    - Automatic switching between PFM and PWM modes, based upon load current
    - Programmable threshold

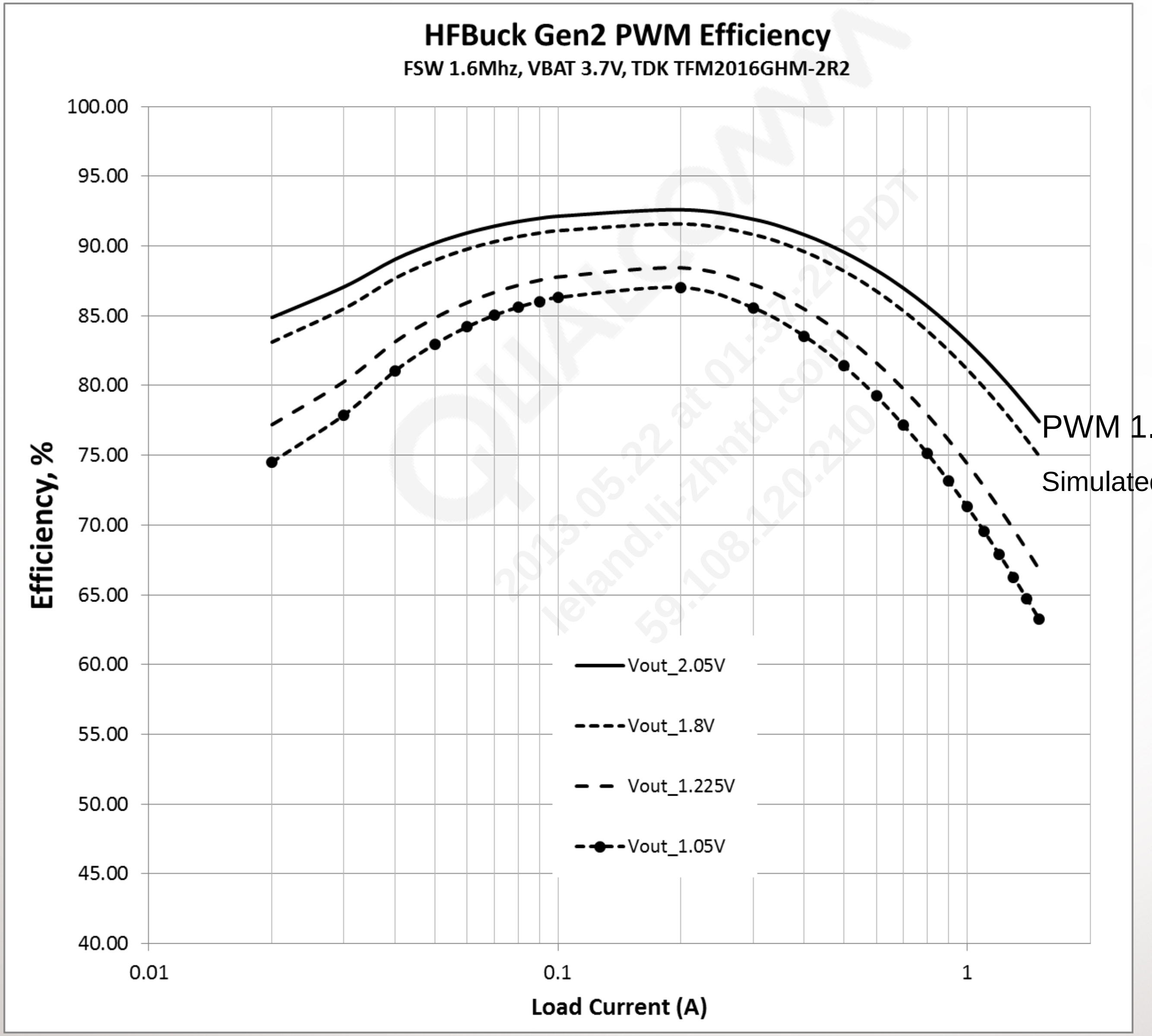
In addition, the second-generation HF-SMPS has improved auto-PFM/PWM operation

- Reduced PFM ripple
- Reduced PFM/PWM transients
- Improved output stages
- Improved isolation and biasing

RF rails use subregulated LDOs to improve noise and efficiency

- Allows RF bucks to use auto-mode
- LDOs set for minimal headroom clean up any ripple

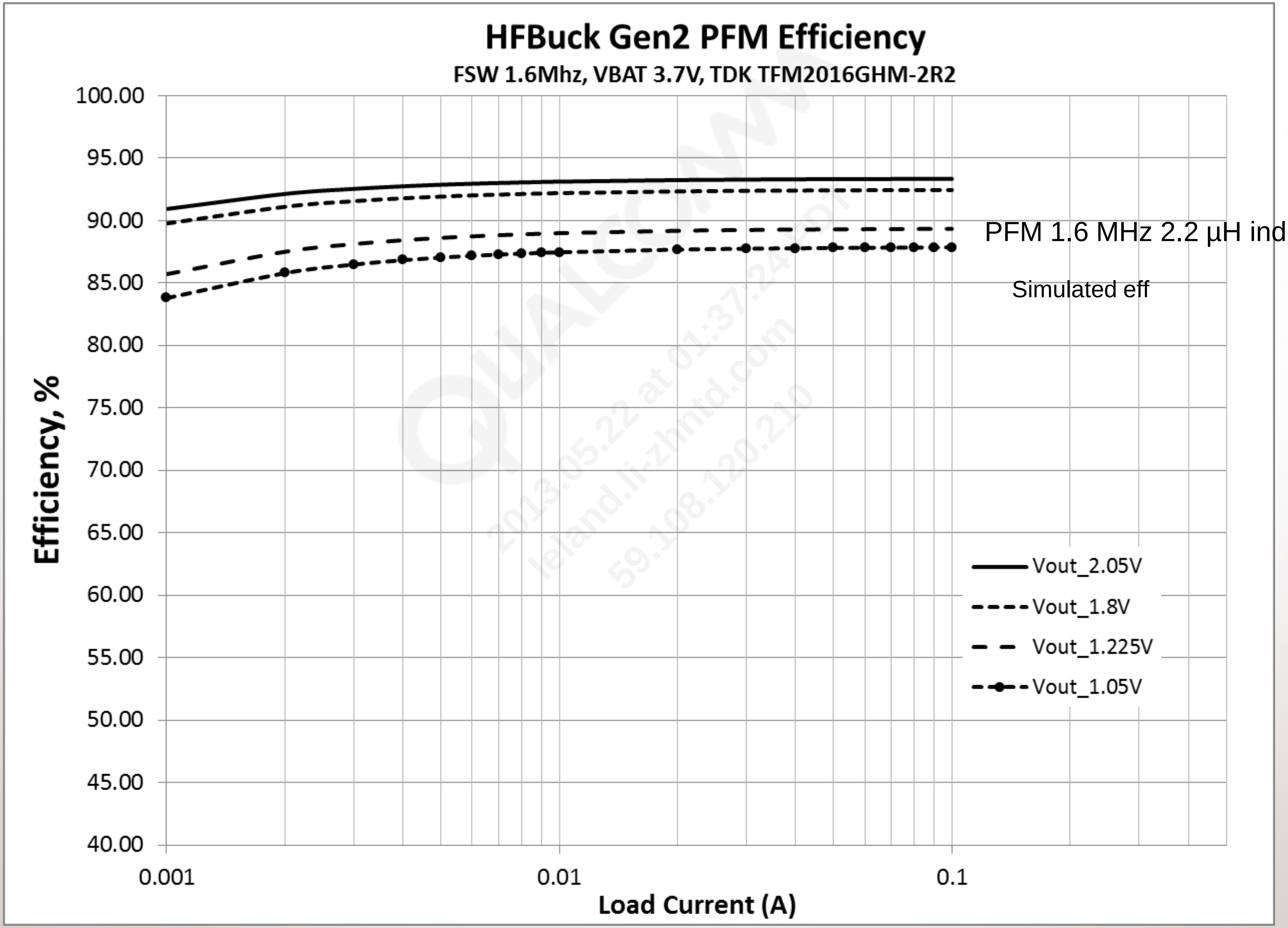
HF-SMPS Estimated Efficiency (1 of 4)



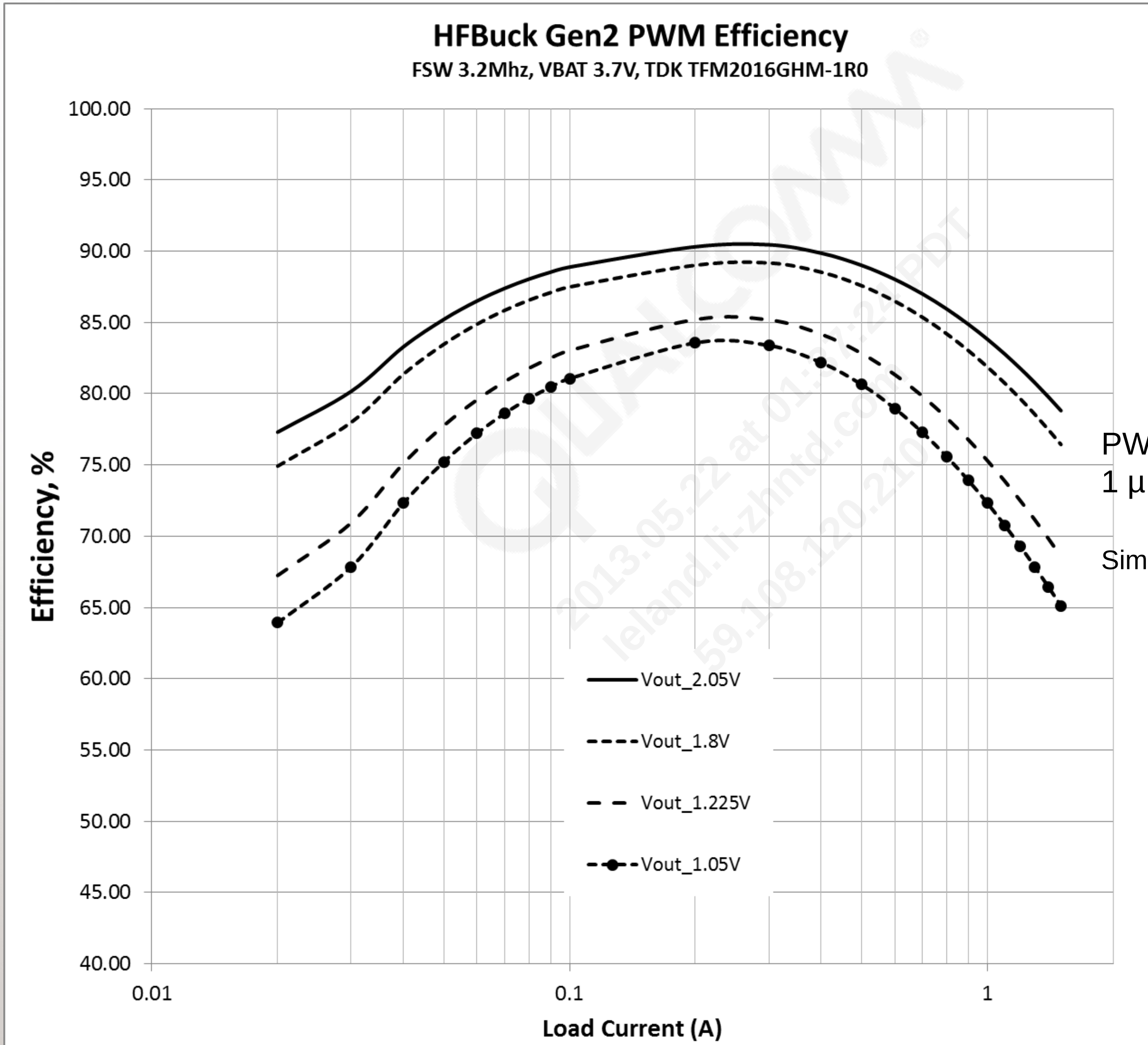
PWM 1.6 MHz 2.2 µH inductor

Simulated eff

HF-SMPS Estimated Efficiency (2 of 4)



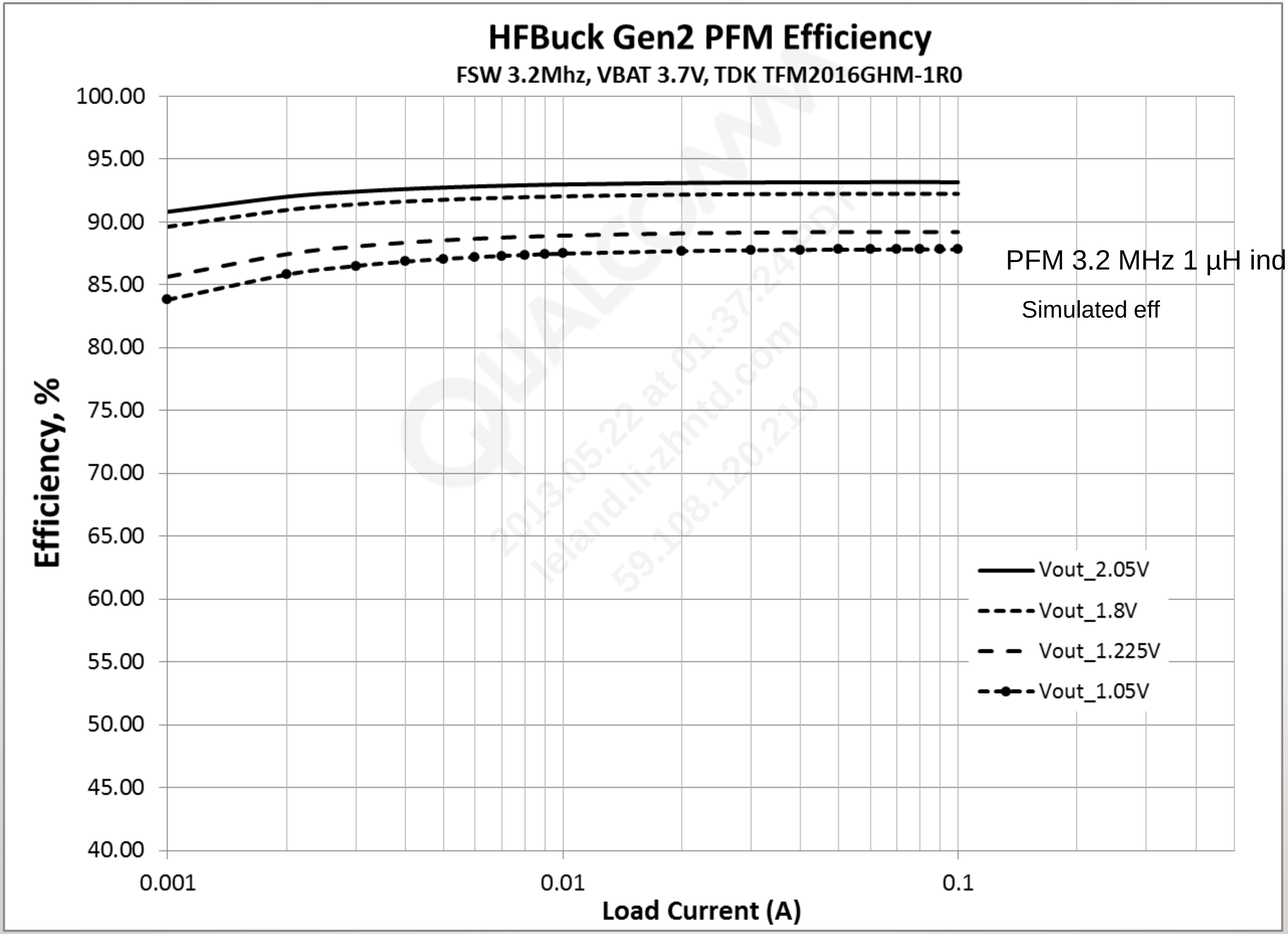
HF-SMPS Estimated Efficiency (3 of 4)



PWM 3.2 MHz
1 µH inductor

Simulated eff

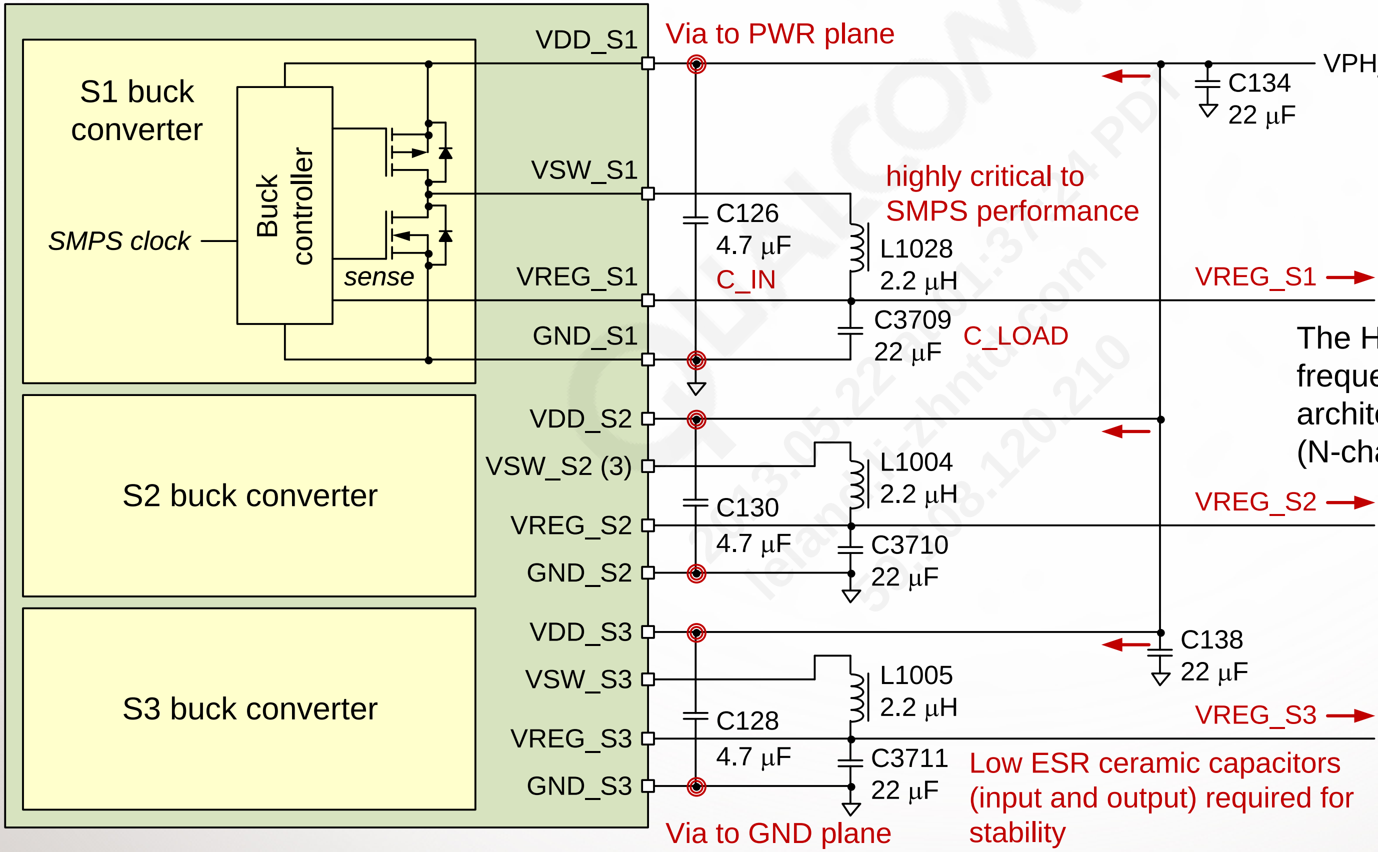
HF-SMPS Estimated Efficiency (4 of 4)



PFM 3.2 MHz 1 µH inductor

Simulated eff

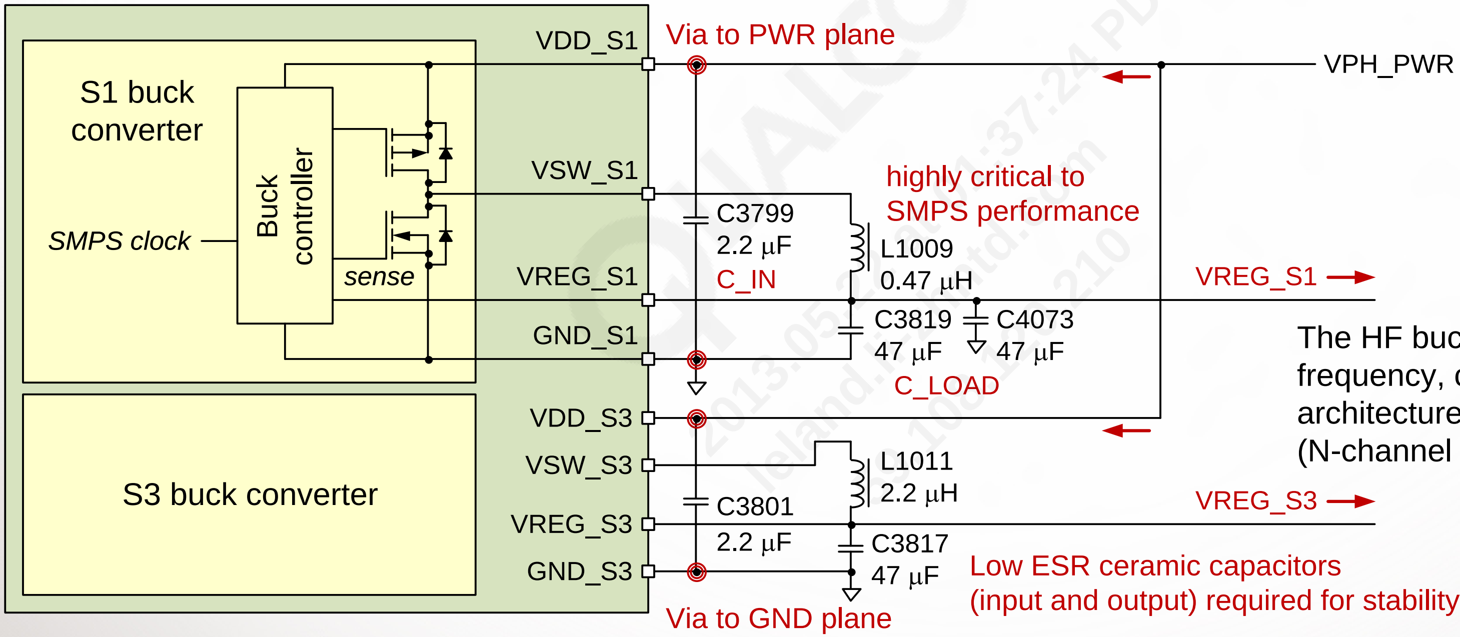
Example PM8941 HF-SMPS Schematic



The HF buck converters use a constant frequency, current mode control architecture with integrated switches (N-channel and P-channel MOSFETs).

Note: Refer to latest version of the *MSM8974 Preliminary Baseband Reference Schematic* (80-NA437-41) for the HF-SMPS schematic.

Example PM8841 HF-SMPS Schematic



The HF buck converters use a constant frequency, current mode control architecture with integrated switches (N-channel and P-channel MOSFETs)

Note: Refer to latest version of the *MSM8974 Preliminary Baseband Reference Schematic* (80-NA437-41) for the HF-SMPS schematic.

PM8941 and PM8841 HF-SMPS – Layout Guidelines

Placement:

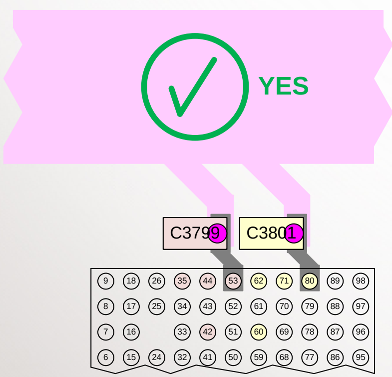
- Minimize switching loop. Place HF-SMPS input cap, output cap and inductor close to each other.

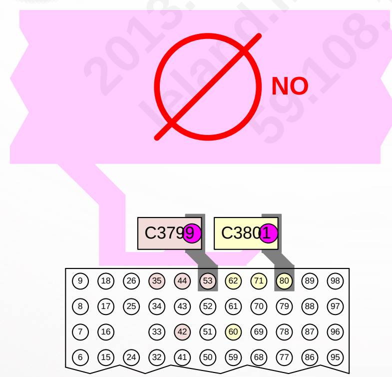
Grounding:

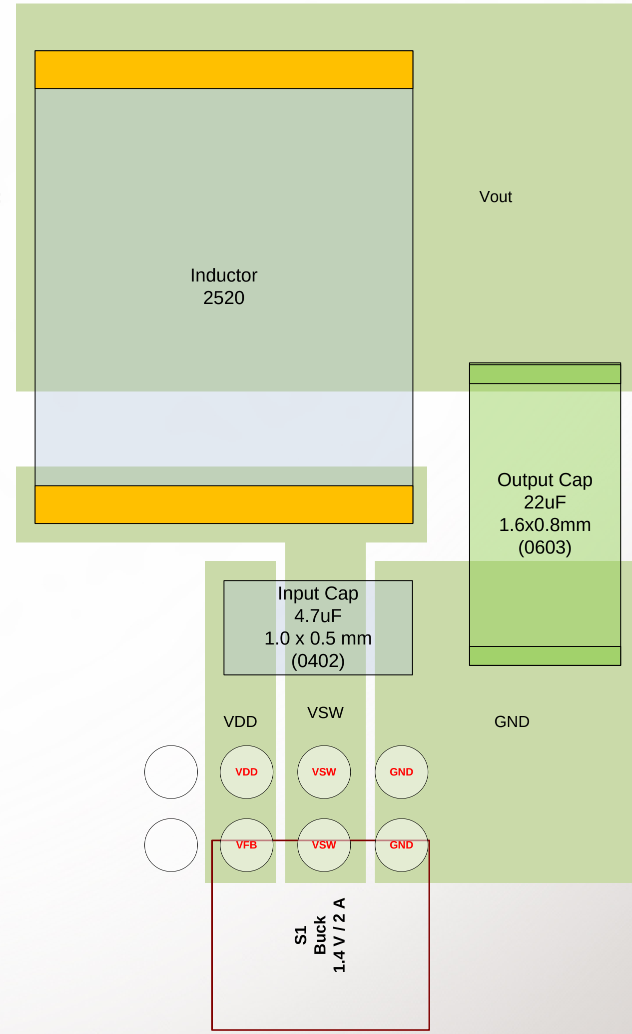
- Connect GND of HF-SMPS input caps, output cap and GND_Sx pins of PMIC together. Connect the common point directly to main GND.

High current paths:

- Use thick and short trace from VSW_Sx pin to inductor.
- Use thick and short trace from VSW_Sx pin to output capacitor.
- Use star routing from main power plane to VDD_Sx pins as shown below.







Sensing:

- Connect VREG_Sx pin to output of the SMPS using a thin trace.

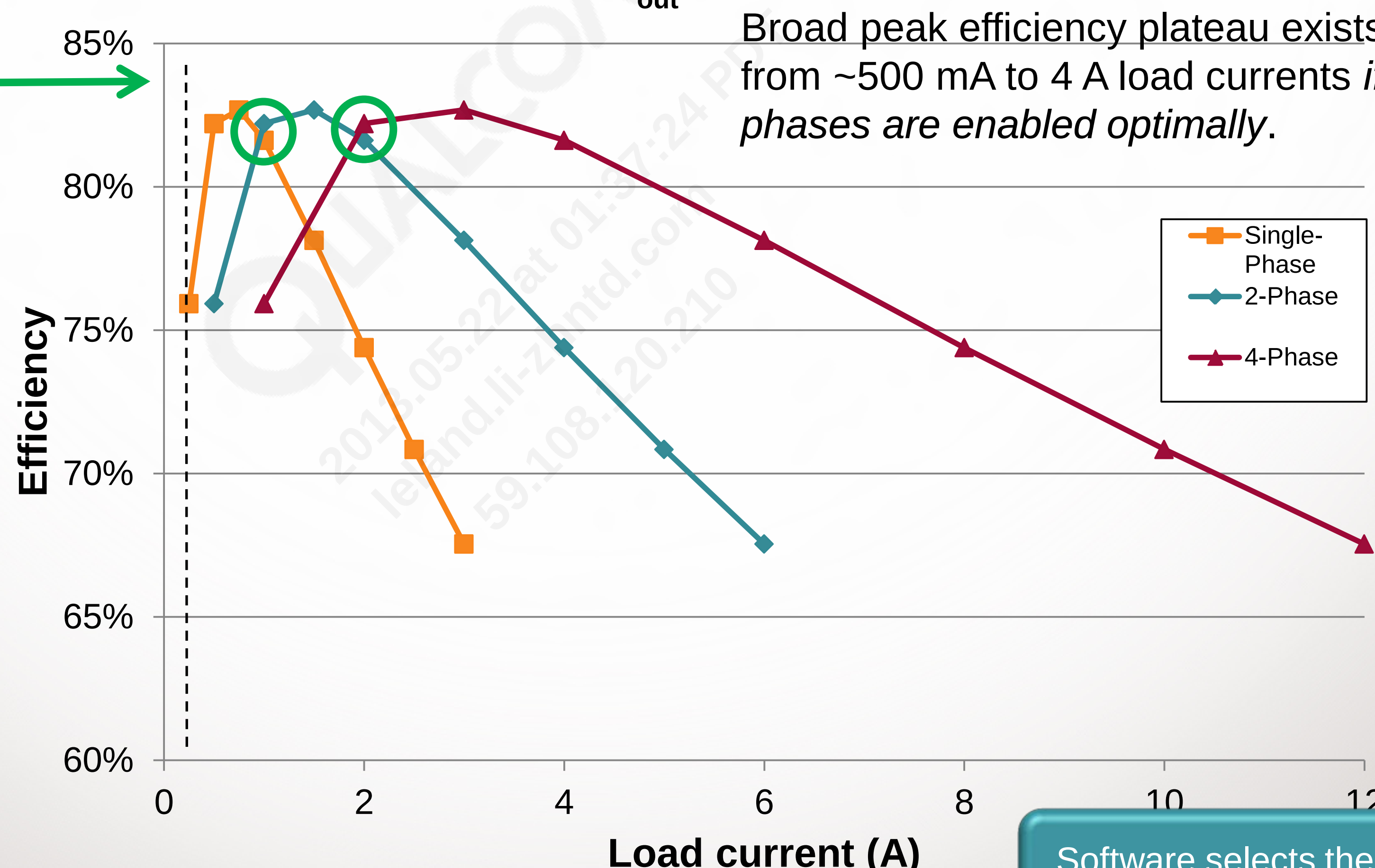
Multiphase FT-SMPS

PM8841 has a second-generation FT-SMPS that employs multiphase operation to extend efficiency on a wider load range

Optimum transition points are at 1 A from one to two phases and at 2 A from two to four phases.

High efficiency discontinuous operation required below 500 mA load current

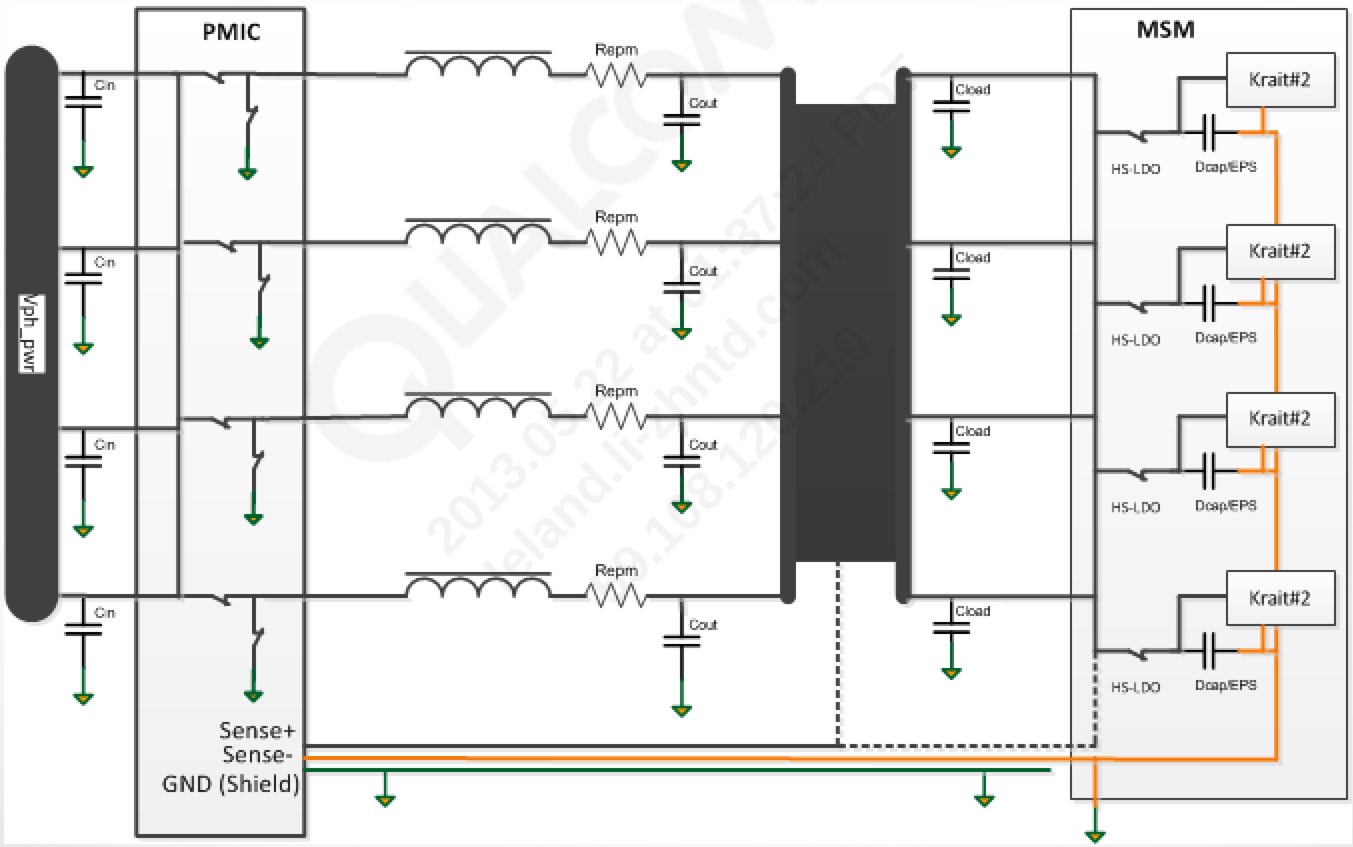
Efficiency vs. number of phases and load current for V_{out} = 0.93 V



Note: Note: PFM (low current mode) not shown

Software selects the number of phases

Quad Core Krait (Apps Processor) Power Delivery



Sense+ connection point on PWB instead vs. inside MSM is TBD.

Krait Bi-Modal Functional Modes Supported

Single core mode – full DCVS (1.1 V–0.5 V)

- Maximum power efficiency

Multicore symmetric mode – full DCVS (1.1 V–0.5 V)

- Good power efficiency, could support running higher PMIC setpoint for same performance

Multicore asymmetric mode – HS (1.1 V–0.85 V)
and LDO (0.75 V–0.5 V)

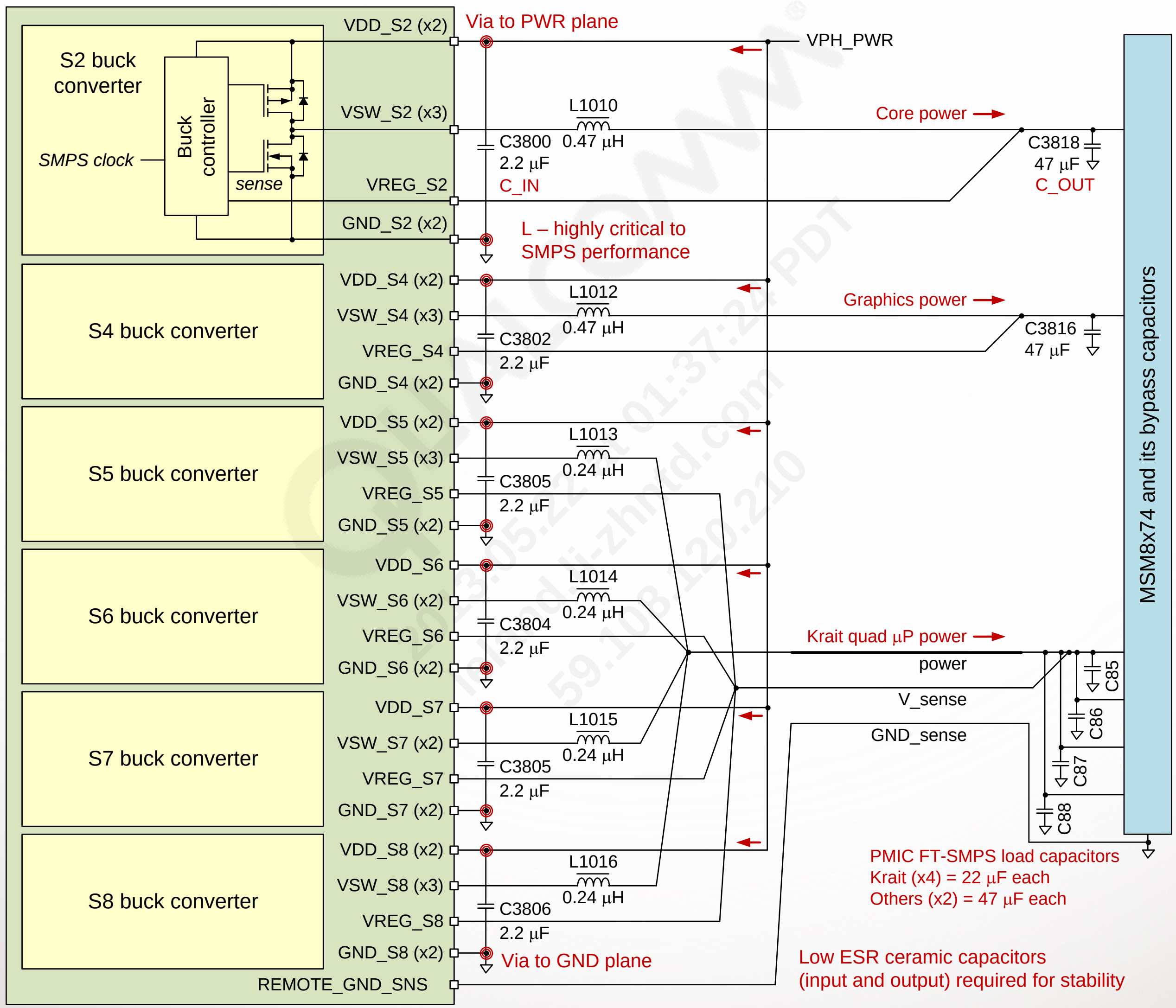
- PMIC DCVS through HS but limited to maximum setpoint of all core voltages
- Need SW/HW aggregation to maintain PMIC at the common mode max

Multicore asymmetric mode – HS+LDO Duty-cycling (1.1 V–0.5 V)

- PMIC at Hi and DCVS range by duty-cycling between HS and LDO modes
- Needs HW sequencing support (possibly future enhancement)

Note: All Modes can support AVS.

Example PM8841 FT-SMPS – Schematic



Note: Refer to latest version of the *MSM8974 Preliminary Baseband Reference Schematic* (80-NA437-41) for the FT-SMPS schematic.

PM8841 FT-SMPS – Layout Guidelines

Placement:

- Place the SMPS output capacitor closer to the MSM device. This is required for reduced IR drops and best transient performance.
- Place SMPS input capacitor and inductor close to the PMIC.
- Place the bulk input capacitor closer to the PMIC.

Grounding:

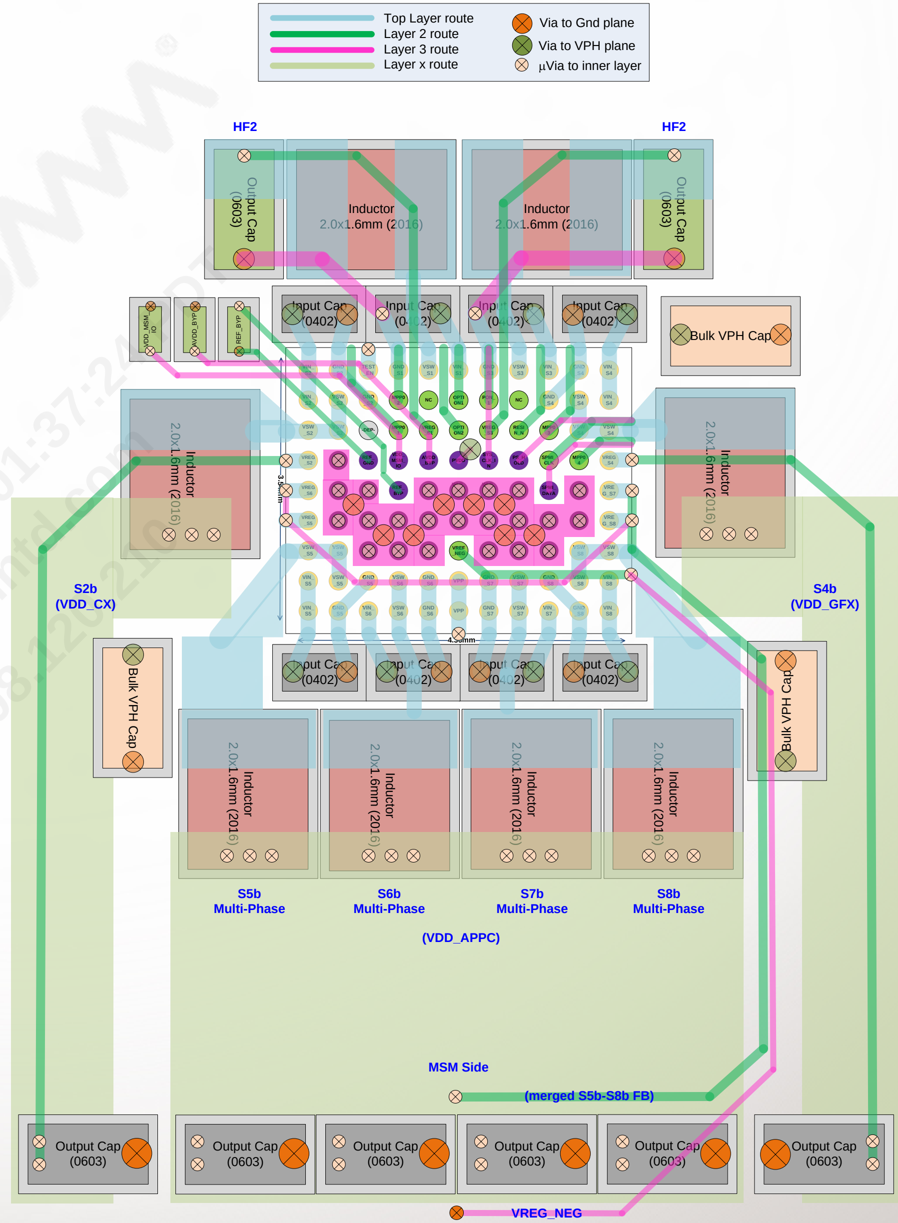
- Connect the GND of SMPS input capacitor and GND_Sx pins of PMIC together. Connect the common point directly to the main GND.
- Connect GND of SMPS output capacitor directly to the main GND.
- Connect GND of the bulk input capacitor directly to the main GND.

High current paths:

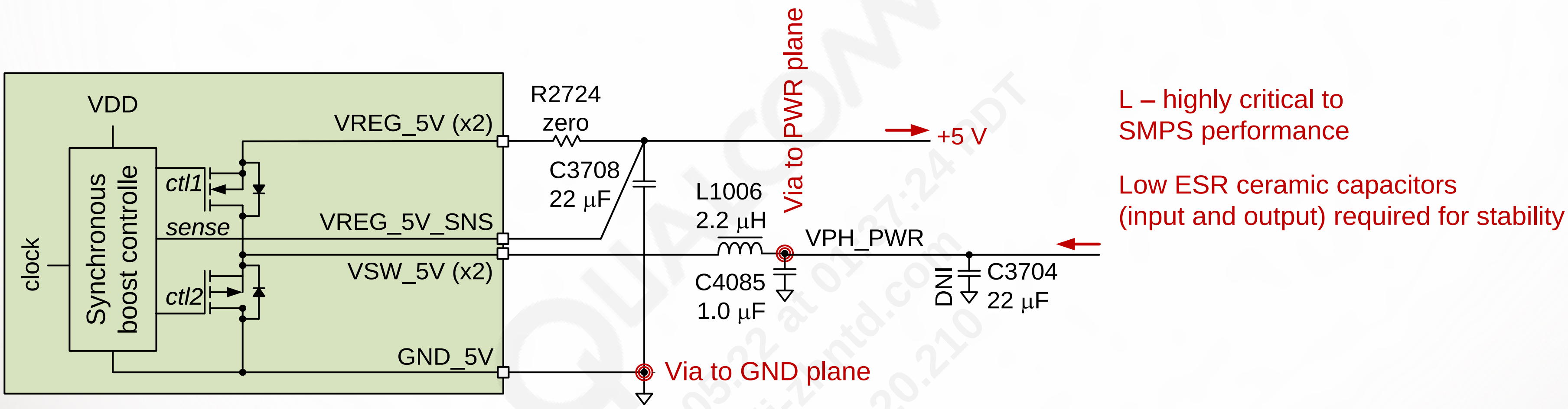
- For multiphase FT SMPS (S5-S8), ensure that all the inductors are connected together to the output capacitors via large area fill as shown in the adjacent figure.
- For S2, S4 FT SMPS, ensure that there is a thick trace from the inductor to output capacitor.

Sensing:

- Connect VREG_Sx directly to remote output capacitors, as shown in adjacent figure.



PM8941 Synchronous Boost SMPS – Schematic and Layout Guidelines



Earlier discussion of high-frequency switching loops also applies to the Boost SMPS.

Same placement and layout guidelines apply to the 5 V synchronous boost SMPS as HF SMPS. Example placement and layout can be seen in the Top-level design topics section later in the slides.

SMPS Switching Frequencies

SMPS*	Type	L (µH)	F_{sw} (MHz)
S1A	HF	2.2	1.6
S2A	HF	2.2	1.6
S3A	HF	2.2	1.6
S1B	HF	0.47	4.8
S2B	FT	0.47	3.2
S3B	HF	2.2	1.6
S4B	FT	0.47	3.2
S5B – S8B	FT	0.24	6.4

***** A = PM8941, B = PM8841

The SMPS inductors are especially critical to performance, and should be selected in accordance with the guidelines given in *Application Note: Switched-Mode Power Supply (SMPS) Inductor Selection* (80-VC603-9).

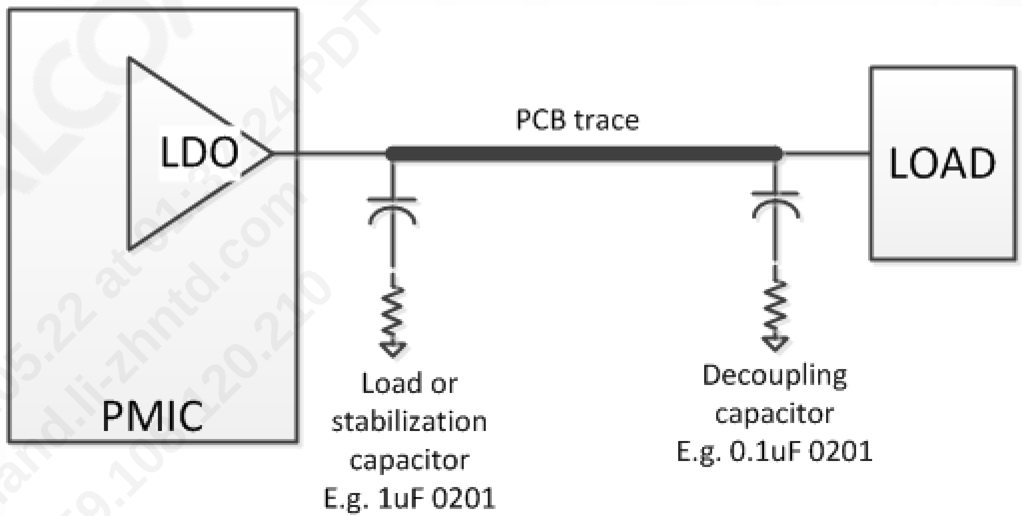
Designers should select inductors that have the same or better specifications as the inductors used in the QCT reference designs.

Low Dropout Linear Regulators – Pseudo-Capless PMOS LDOs (1 of 2)

PM8941 eliminates the need to have load capacitor for certain PMOS LDOs. These LDOs are called the Pseudo-capless LDOs. These LDOs have been identified in the *MSM8974 Preliminary Baseband Reference Schematic* (80-NA437-41), with DNI load capacitors.

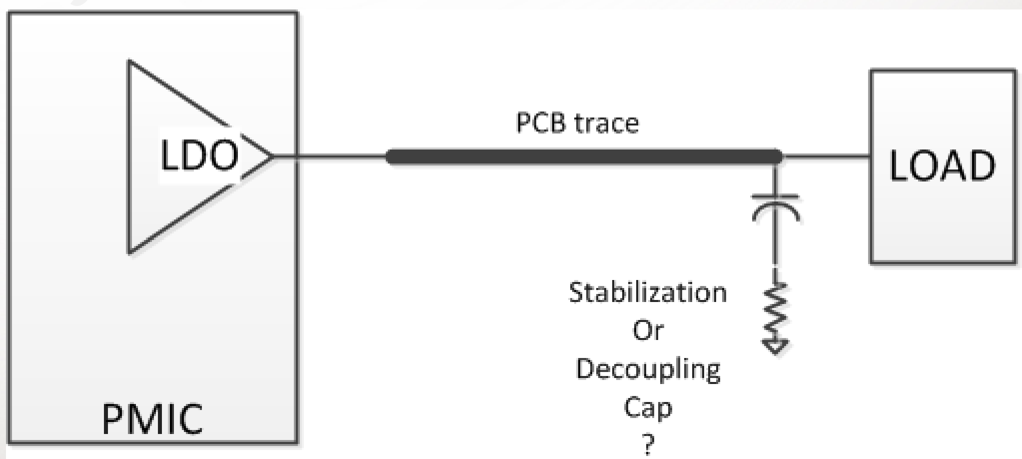
Present situation

- Load capacitor at LDO output
- Decoupling capacitor at load

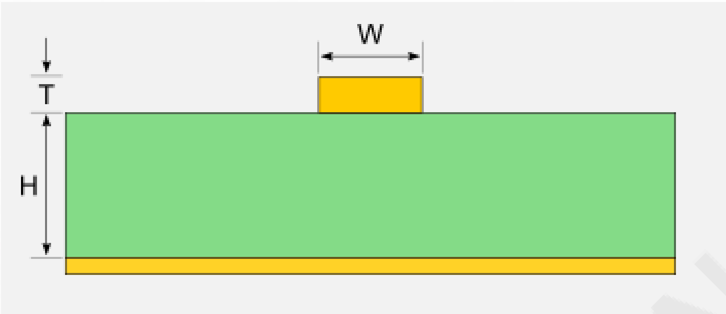


Want to eliminate the LDO load capacitor

- Reduce BOM cost
- Reduce board area



Low Dropout Linear Regulators – Pseudo-Capless PMOS LDOs (2 of 2)

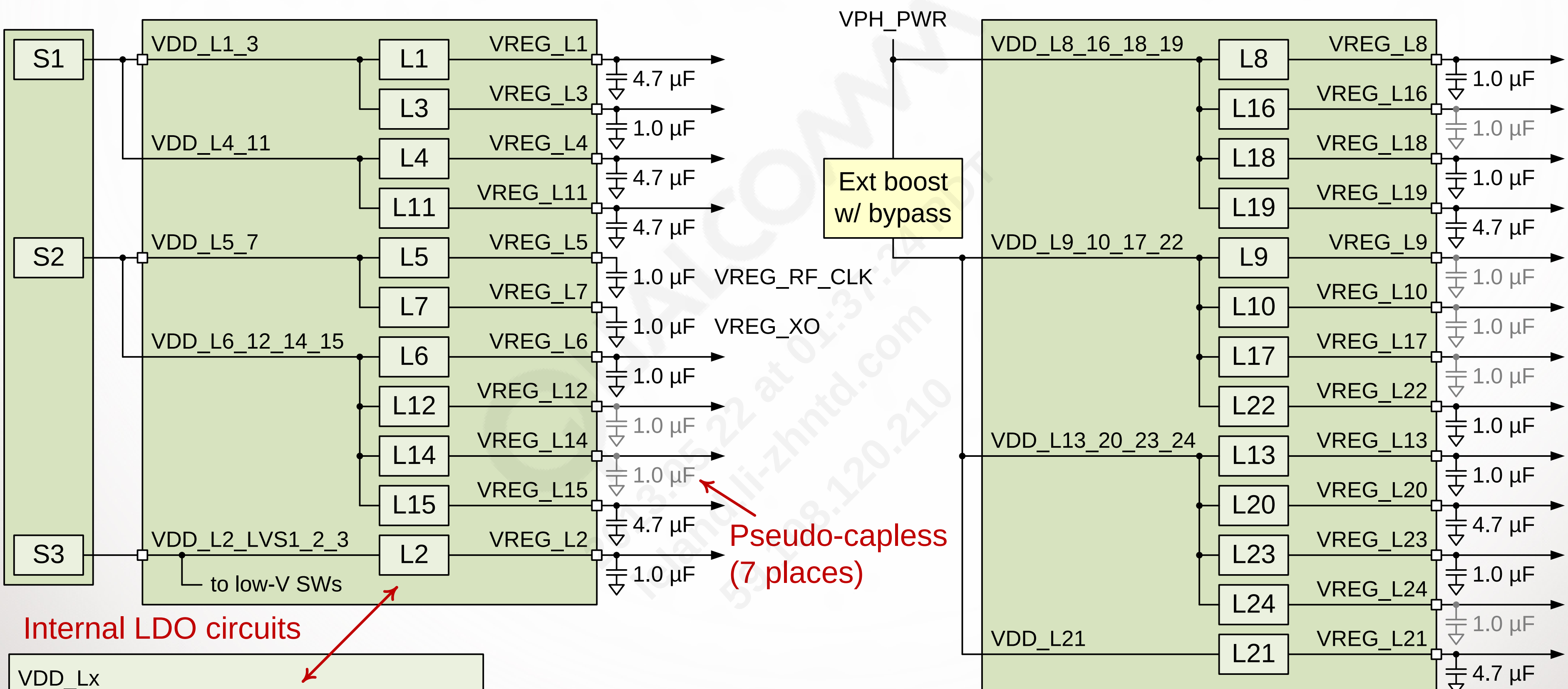


W = width of the trace
L = length of the trace
T = thickness of the trace
H = height of the substrate

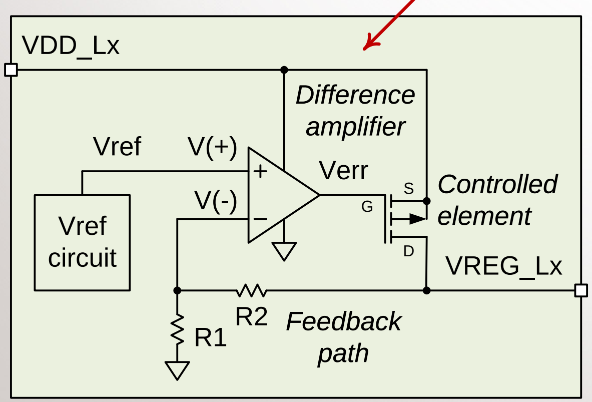
Rough guidelines – use worst case CAD extraction	W (µm)	H (µm)	T (µm)	L (cm)	Trace inductance (nH)	Trace resistance (mΩ)
Long trace carrying 600 mA	1600	90	17	5	4.6	< 30
Long trace carrying 300 mA	1000	90	17	5	5.7	40
Long trace carrying 200 mA	800	90	17	5	7.05	60
Long trace carrying 100 mA	400	90	17	5	14.1	120
Long trace carrying 25 mA	100	90	17	5	56.5	480

Recommendation:
For PMOS LDOs with load within 5 cm of the PMIC LDO pin, combine the PMIC load capacitor and load bypass capacitor, and place at the load.

Example Low Dropout Linear Regulators – Schematic



Internal LDO circuits



X5R or X7R ceramic capacitors are required to ensure stability

Note: The above schematic is an example. Pseudo-capless LDOs have been identified in the *MSM8974 Preliminary Baseband Reference Schematic* (80-NA437-41), with DNI load capacitors.

Low Dropout Linear Regulators – Layout Guidelines

Pseudo-capless LDO

- The trace from LDO output pin to the load capacitor must meet the inductance and resistance requirements quoted in the previous slides.

Other LDO

- The trace from LDO output pin to the output capacitor must have inductance and resistance less than 5 nH and 5 mΩ, respectively.

Regulator Low-Power Modes

All SMPS and linear regulators – except for the RF_CLK and XO LDOs (L5 and L7) – support low-power modes that reduce their quiescent currents. This is especially useful during the handset sleep mode, enabling maximum standby time. Different regulator types implement their low-power modes differently, as described below:

Linear regulator – implements its low-power mode by reducing the current of its feedback loop. During low-power operation, the regulator performance is degraded – lower PSRR, less output current capability, etc. If the load is greater than 10 mA, the output voltage is likely to be out of specification.

Buck SMPS – two control modes: pulse frequency modulation (PFM) control for low-power operation, and pulse width modulation (PWM) control for normal operation. For best efficiency, the buck regulator switches automatically between PFM and PWM, but it can be switched manually via software as well (depending upon sleep or active operation).

- In PFM mode, the controller shuts down, except for a comparator that monitors the output voltage. Starting with the pass device off, eventually the output dips below the programmed output voltage. The pass device is then turned on (a single pulse) until the output voltage slightly exceeds the programmed voltage, and then it is turned off. The on/off process repeats. If the buck SMPS is loaded too heavily in PFM mode, the output ripple is degraded
- During PFM operation, the pulse frequency varies with load current, while the ripple stays constant at about 30 to 50 mV peak-to-peak. Depending upon the load, the pulse frequency can drop into the audio range and could become audible if it couples into the audio system
- For normal (active) phone operation, the PWM mode should be used.

Boost SMPS – very similar to Buck modes, except low power operation uses pulse burst modulation (PBM).

Internal Regulator Connections

Some regulator input voltages and several regulated outputs are used to power internal PM8941 circuits. The regulators must be enabled and set to their default values for proper PMIC operation.

Regulator pin	Default voltage	Connected internal circuits
VDD_L2_LVS1_2_3 or VDD_MSM_IO	VREG_S3 (1.8 V)	Sleep clock pad, PON circuit I/Os, SPMI pads, various internal circuits, and miscellaneous I/Os
VREG_L1	1.225 V	Selectable GPIO supply Selectable MPP I/O supply
VREG_RF_CLK (L5)	1.8 V	RF clock circuits Low-noise XO outputs (XO_OUT_Ax)
VREG_L6	1.8 V	Selectable GPIO supply Selectable MPP I/O supply Low-power XO outputs (XO_OUT_Dx)
VREG_XO (L7)	1.8 V	XO core
VREG_L8	1.8 V	VREF_BAT supply HK/XO ADC
VREG_S3	1.8 V	Selectable GPIO supply Selectable MPP I/O supply
VREG_S4	5 V	Selectable GPIO supply

External Connection Options and Subregulation

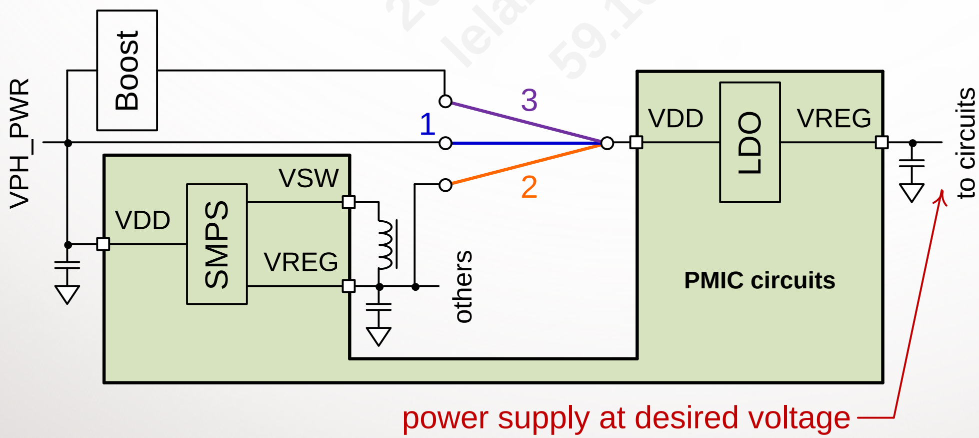
Linear regulators are powered by one of three sources (see below):

1. An SMPS output – this option implements subregulation (see the next slide)
2. The primary phone power supply node (VPH_PWR; see the LDO Regulator Supplies – Other than Subregulation slide)
3. An external boost SMPS with optional bypass mode (see the LDO Regulator Supplies – Other than Subregulation slide)

1) Select VPH_PWR for single-stage, direct regulation

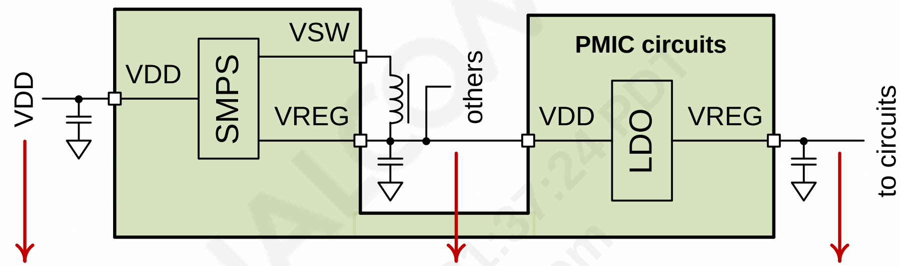
2) Select PMIC SMPS output for two-stage, subregulation

3) Select external boost SMPS output for two-stage, subregulation when higher final output voltages are needed; if the SMPS has a bypass option, it can be placed in its bypass mode if the primary voltage (VPH_PWR) is high enough (boost not required)



LDO Regulator Supplies – Those Using Subregulation

All of the MSM8x74 reference designs subregulation implementations are described below.



3.6 V	S1	1.30 V	L1	1.225 V
			L3	1.200 V
			L4	1.150 V
			L11	1.250 V
3.6 V	S2	2.15 V	L5	1.800 V
			L7	1.800 V
			L6	1.800 V
			L12	1.800 V
			L14	1.800 V
			L15	2.050 V
3.6 V	S3	1.80 V	L2	1.200 V

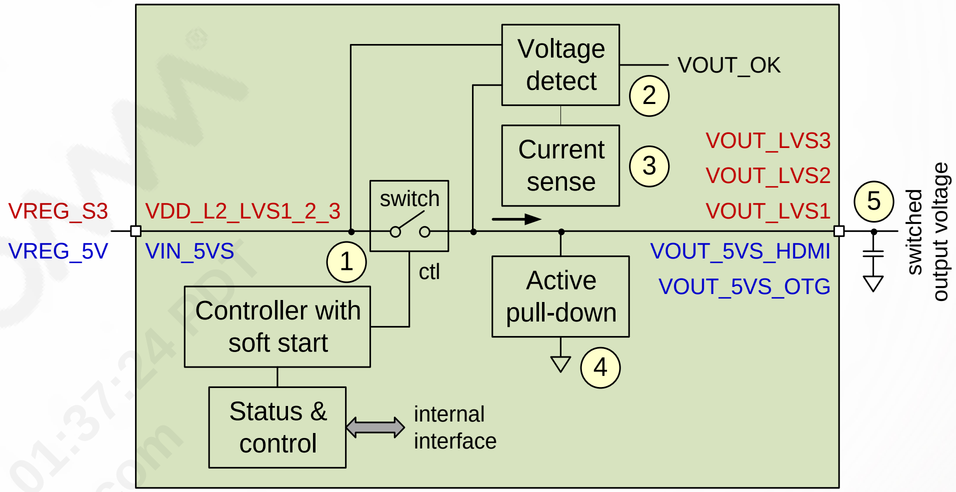
LDO Regulator Supplies – Other Than Subregulation

Regulator supply	Source
VDD_L9_10_17_22	External boost with bypass option (VPH_PWR)
VDD_L13_20_23_24	
VDD_21	
VDD_L8_16_18_19	VPH_PWR

Voltage Switches

A low-voltage switch (LVS) or 5 V switch (5VS) can be used to gate a supply voltage to functions that do not support phone operation, such as sensors and OTG. Switch features include:

- Soft start – prevents in-rush current from causing a voltage dip at the source regulator's output
- Output voltage verification
- Over-current protection – automatically turns off the switch and sends an interrupt
- Non-floating output – active pull-down during powerdown
- Low-power mode – switch remains closed but all control functions are turned off



1. The switch is turned on slowly (by ramping its gate voltage) to limit in-rush current.
2. The output voltage is deemed okay when it is about 10% less than the input voltage.
3. The current-protection threshold is 2 to 6 × I_rated current; switch is opened and an interrupt is generated if the current goes above 3 × I_rated value.
4. When opened, the output is pulled down to ground.
5. External components are not required. If an output capacitor is used, do not exceed 1.0 µF.

Need for External Boost Bypass

Battery impedance could be as high as 250 mΩ. For a 4 A transient current consumption:

- 4 A × 250 mΩ = 1 V drop

With 4 A of transient current drawn from the battery, a fully charged battery is on the verge of browning out the eMMC and SD card.

- 4.2 V → 3.2 V

Peripheral	Battery Cut-off Voltage
HS USB Phy 3.3 V	3.15 V
SD card	3.16 V
eMMC	3.16 V
LCD (typical)	3.01 V
Camera (typical)	3.0 V
UIM Card	2.99 V
Sensors (typical)	3.02 V (moving to 2.5 V)

The external boost bypass (FAN48630UC315X) boosts the system voltage and powers critical rails like eMMC, SD, etc., during high current events.

External Boost Bypass Operation

The mode of external boost bypass and its output voltage depends upon the input voltage and status of EN, BYP_N, VSEL pins as indicated in the table below.

EN	BYP_N	VSEL	Vout
0	x	x	Boost bypass disabled
1	1	0	For Vin < 3.15 V, Vout = 3.15 V (boost mode) For Vin > = 3.15 V, Vout = Vin (bypass mode)
1	1	1	For Vin < 3.3 V, Vout = 3.3 V (boost mode) For Vin > = 3.3 V, Vout = Vin (bypass mode)
1	0	x	Vout = Vin (forced bypass mode)

General Housekeeping

General Housekeeping Content

Analog multiplexer and scaling circuits

HK/XO ADC circuits

Clock architecture

System clocks – 19.2 MHz XO

- 19.2 MHz XO source
- XO buffers and controllers
- Low-noise, low-power, and differential outputs

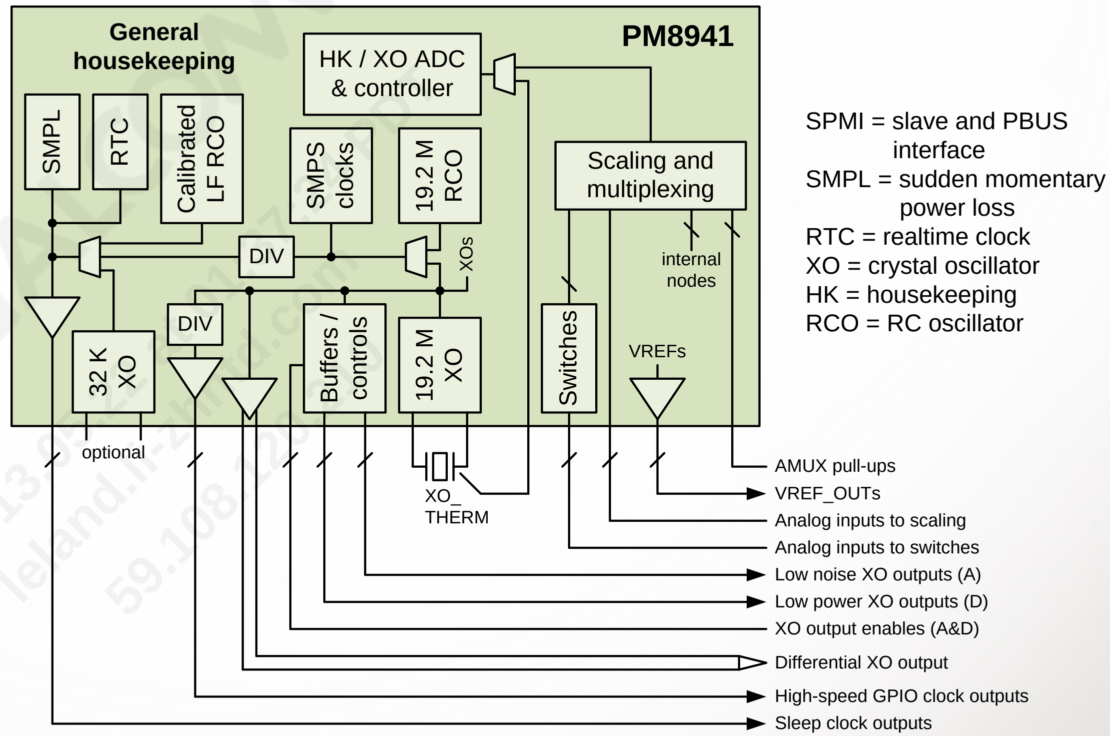
System clocks – sleep clock

Other clock topics

- MP3 and other alternate clocks
- SMPS clock circuits
- Realtime clock
- 19.2 MHz RC oscillator
- Calibrated low-frequency RC oscillator
- External components
- RTC accuracy

Over-temperature protection

Automatic fault protection (AFP)



Analog Multiplexer and Scaling Circuits (1 of 2)

Several analog switches and multiplexers select one signal for ADC conversion.

Nestled within the multiplexers are voltage scaling circuits that condition the signals to best use the ADC's dynamic range.

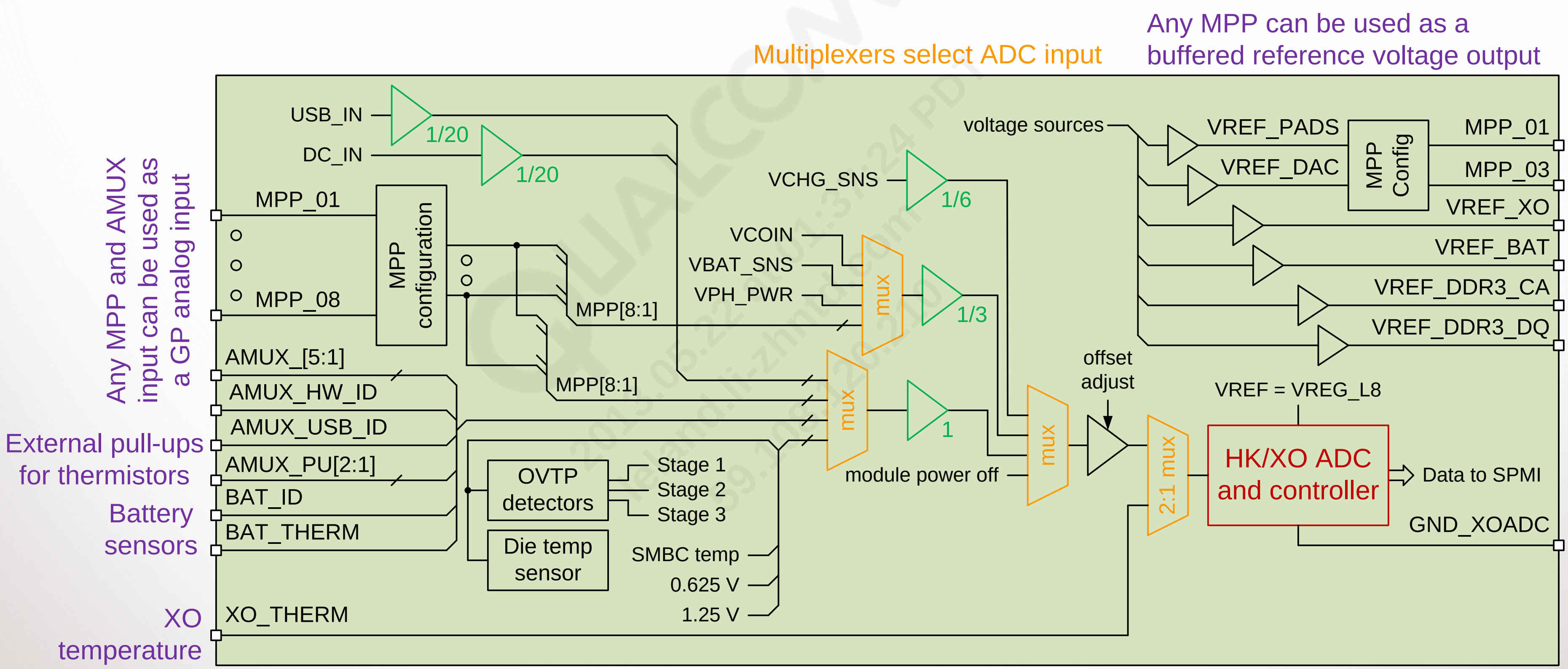
The selected signal allows handset software to monitor various voltage nodes, auxiliary inputs, and the die temperature using a single ADC.

The ADC input cannot reliably go below 0.05 V or above VREG_L8 + 0.05 V; do not exceed this range.

Gain and offset errors vary between multiplexer channels; calibration values apply to the specific channel being calibrated only. Calibrate each channel separately.

A functional block diagram is provided on the next slide.

Analog Multiplexer and Scaling Circuits (2 of 2)



Voltage scaling sets ADC input range

Analog Multiplexer Channel Assignments (1 of 2)

Ch #	Description	Typical input range (V)	Scaling	Typical output range (V)
0	USB_IN pin (divided by 20)	0.15 to 0.50	1	0.15 to 0.50
1	DC_IN pin (divided by 20)	0.15 to 0.50	1	0.15 to 0.50
2	VCHG_SNS	3 to 10	1/6	0.50 to 1.67
3, 4	–	–	–	–
5	VCOIN pin	2.0 to 3.25	1/3	0.67 to 1.08
6	VBAT_SNS pin	2.5 to 4.5	1/3	0.83 to 1.50
7	VPH_PWR pin	2.5 to 4.5	1/3	0.83 to 1.50
8	Die-temperature monitor	0.4 to 0.9	1	0.4 to 0.9
9	0.625 V reference voltage	0.625	1	0.625
10	1.25 V reference voltage	1.25	1	1.25
11	Charger temperature	0.05 to (VL8 - 0.05)	1	0.05 to (VL8 - 0.05)
12, 13	–	–	–	–
14, 15	GND_REF, VDD_ADC	–	–	–
16 to 23	MPP_01 to MPP_08 pin	0.05 to 1.5	1	0.05 to 1.5
24 to 31	–	–	–	–

Analog Multiplexer Channel Assignments (2 of 2)

Ch #	Description	Typical input range (V)	Scaling	Typical output range (V)
48	BAT_THERM pin	0.05 to (VL8 – 0.05)	1	0.05 to (VL8 – 0.05)
49	BAT_ID pin	0.05 to (VL8 – 0.05)	1	0.05 to (VL8 – 0.05)
50	XO_THERM pin direct	0.05 to (VL8 – 0.05)	1	0.05 to (VL8 – 0.05)
51 to 53	AMUX_1 to AMUX_3 pin	0.05 to (VL8 – 0.05)	1	0.05 to (VL8 – 0.05)
54	AMUX_HW_ID pin	0.05 to (VL8 – 0.05)	1	0.05 to (VL8 – 0.05)
55, 56	AMUX_4, AMUX_5 pin	0.05 to (VL8 – 0.05)	1	0.05 to (VL8 – 0.05)
57	AMUX_USB_ID pin	0.05 to (VL8 – 0.05)	1	0.05 to (VL8 – 0.05)
58, 59	AMUX_PU1, AMUX_PU2 pin	0.05 to (VL8 – 0.05)	1	0.05 to (VL8 – 0.05)
60	XO_THERM pin through amux	0.05 to (VL8 – 0.05)	1	0.05 to (VL8 – 0.05)
61, 62	–	–	–	–
63	Module power off	–	–	–

1) Amux circuits include switches that allow signals from off-chip thermistors to use one of two external pull-up resistors (at AMUX_PU1 or AMUX_PU2), thereby reducing the number of resistors in the thermistor networks.

2) Channel 63 should be selected when the amux is not being used; this prevents the scalers from loading the inputs.

3) Input voltages must not exceed the highest of the following supply voltages: VCOIN, VBAT, VCHG, or VPH_PWR. The term 'VL8' is the VREG_L8 output voltage (connected internally).

HK and XO ADC Circuits

As implied by its name, the HK/XO ADC circuit supports two modes:

- General HK operation, where the signal selected by the analog multiplexer is routed to the ADC
- A direct path for crystal oscillator (XO) thermal monitoring

ADC input from AMUX circuits (ADC in HK mode) or XO circuits (ADC in XO mode); XO details are shown

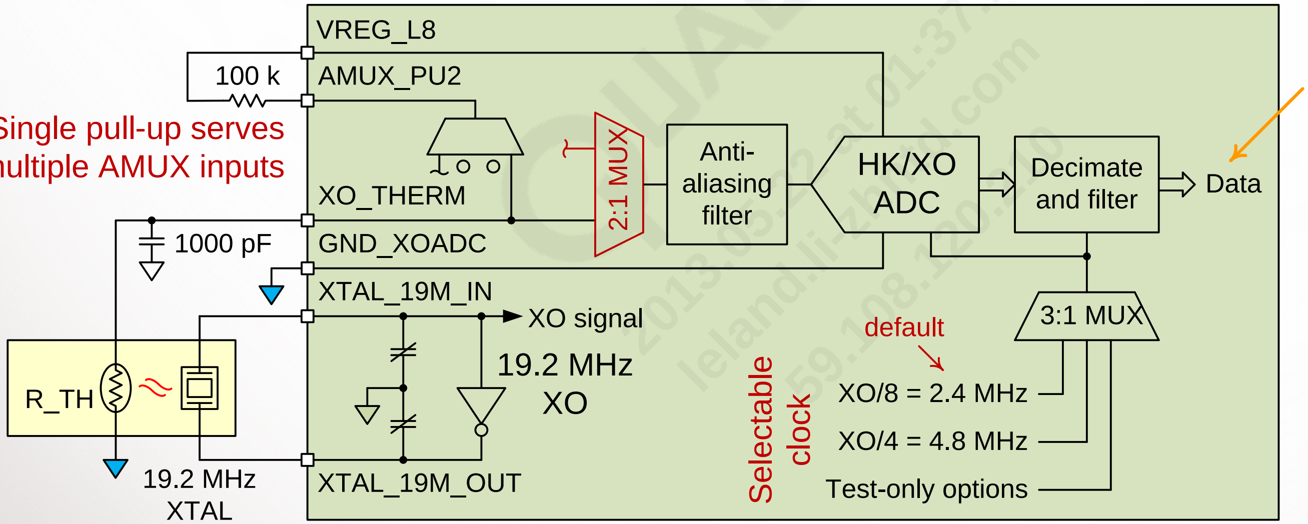
2) Analog voltage into PMIC is proportional to crystal temperature

3) Filter and convert to digital domain

- Sigma-Delta (ΣΔ) type ADC
- High accuracy
- Slow conversion and filtering

Programmable decimation rate and filtering (below)

Single pull-up serves multiple AMUX inputs



4) Data → SPMI → modem IC

5) Modem IC algorithms compensate for errors and drift versus cellular network timing

16 bits = sign + 15-bit data

Format = 2's compliment

1) Thermistor detects crystal temp

= Isolated (island) ground for XO circuits only

The decimation filter can be enabled (Sinc1 & Sinc2) or disabled; the examples given at right are with the filter enabled.

Clock rate, decimation rate, and conversion time

CLK	Decimation ratio	Update rate	Conversion time
2.4 MHz	512	2.26 kHz	442 µs
	1024	1.15 kHz	868 µs
	2048	580 Hz	1.722 ms
	4096	290 Hz	3.428 ms

CLK	Decimation ratio	Update rate	Conversion time
4.8 MHz	512	4.38 kHz	228 µs
	1024	2.26 kHz	442 µs
	2048	1.15 k Hz	868 µs
	4096	580 Hz	1.722 ms

Clock Architecture

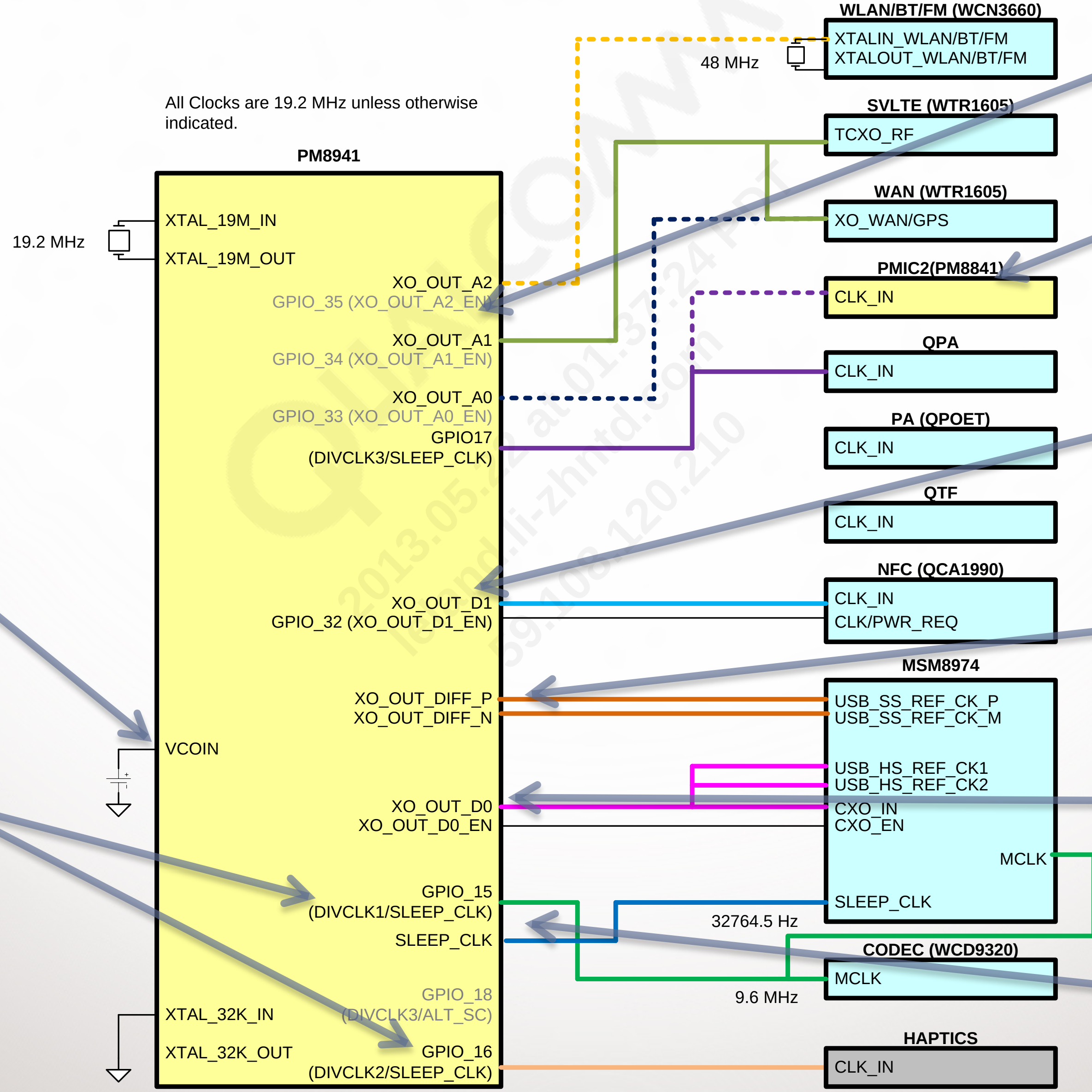
Clock drivers have 50 Ω output impedance

Single 19.2 MHz XTAL can act as the source for all clocks in the system

RTC backed up with a coincell/coincap even with no 32 kHz XTAL

Additional sleep clocks and DIVCLKs hidden behind GPIOs

32 kHz RTC/ sleep clock not required



High performance RF clocks

PM8841 requires no clock (other than for SPMI)

Clocks can be controlled via external hardware signal or via software

Differential clock for extra noise immunity for USB 3.0

Low power baseband clocks with tight duty cycle

DIVCLKs provide system clock /1, /2, /4, /8, /16

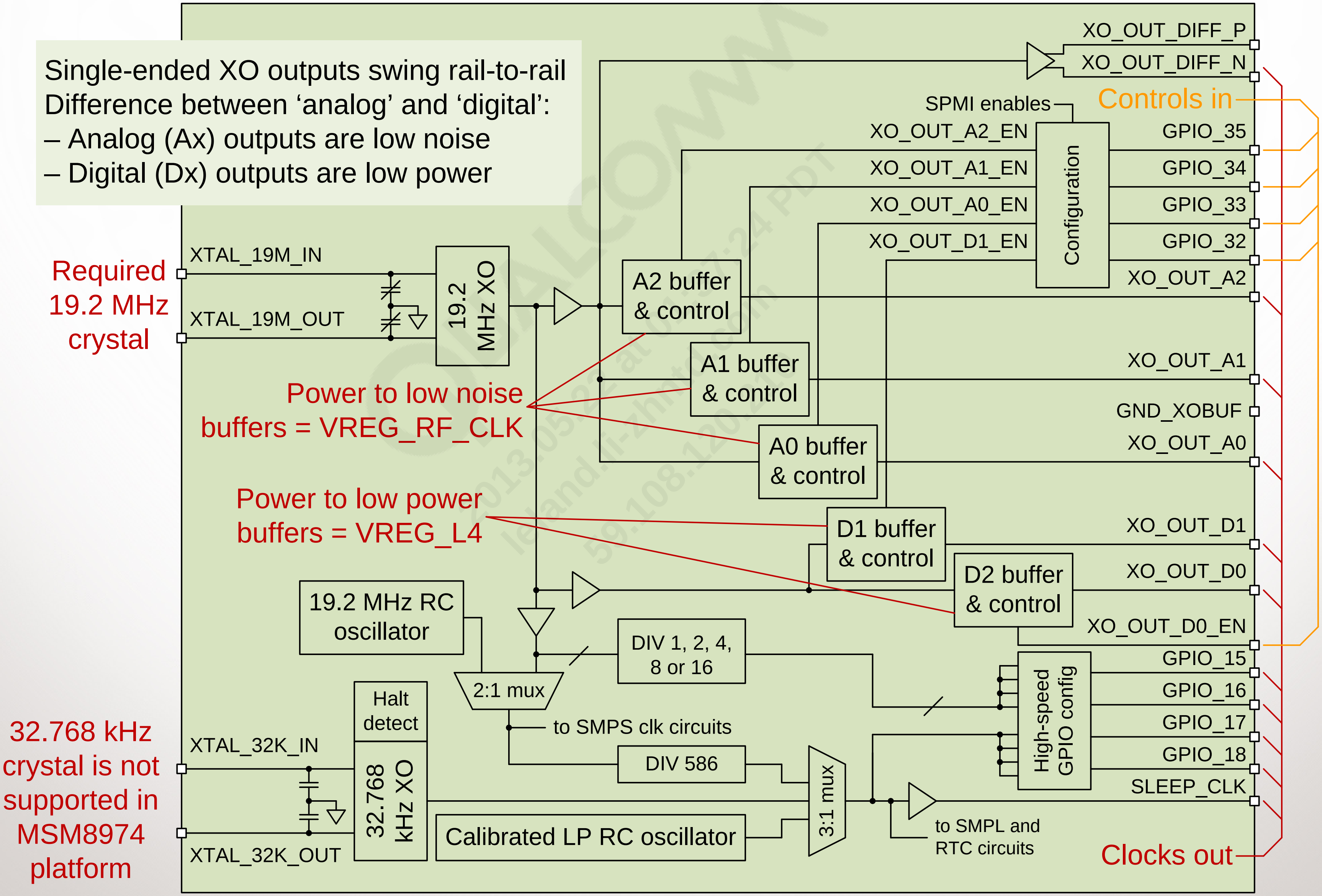
System Clocks (1 of 2)

Several clocks and clock outputs are used for general housekeeping functions and elsewhere throughout the system.

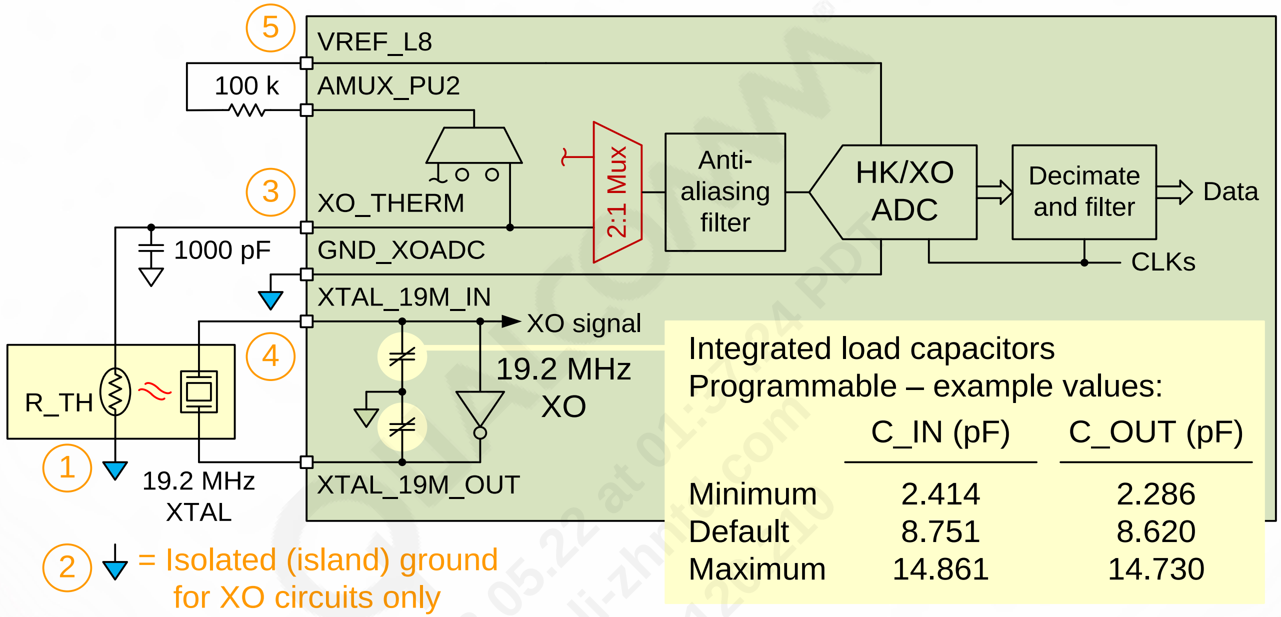
- 19.2 MHz crystal oscillator (XO) circuit – the system's master clock
- Five sets of XO controller and buffer circuits
- Differential XO output
- 19.2 MHz RC oscillator for power-up and emergency backup
- Divided and buffered clock for MP3 support
- 32.768 kHz XO – or calibrated low-frequency RC oscillator – for sleep and for the realtime clock (RTC)
- Multiple buffered SLEEP clock outputs
- SMPS clocks

System Clocks (2 of 2)

Single-ended XO outputs swing rail-to-rail
Difference between ‘analog’ and ‘digital’:
– Analog (Ax) outputs are low noise
– Digital (Dx) outputs are low power



19.2 MHz XO Source – Schematic



Integrated load capacitors
Programmable – example values:

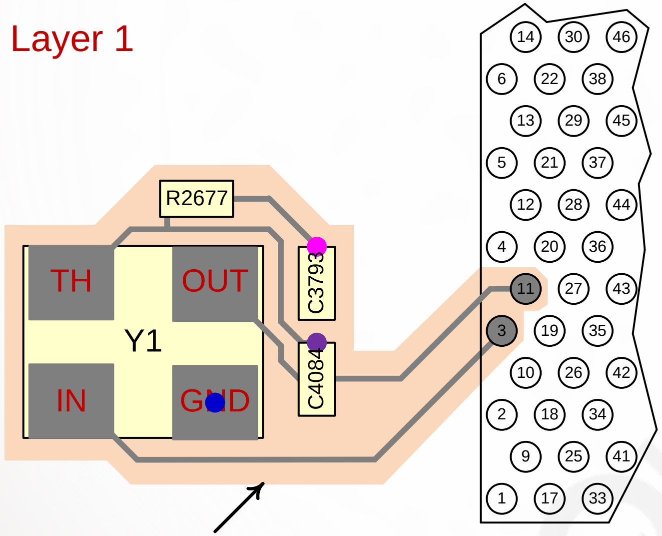
	C_IN (pF)	C_OUT (pF)
Minimum	2.414	2.286
Default	8.751	8.620
Maximum	14.861	14.730

1. The thermistor is normally integrated into the same package as the crystal.
2. Ground connections are critical to thermal management (more on the next slide).
   A. The XO ground is a surface-layer island that must be isolated from other ground fill areas. This island is also thermally isolated from the PMIC to prevent heating.
   B. Associated XO components are connected to this ground island: thermistor, GND_XOADC.
3. The output of the thermistor network is XO_THERM – the node between the resistor and the thermistor; this analog voltage is routed directly to the XO/HK ADC.
4. The XTAL_19M_IN and XTAL_19M_OUT nodes must not be loaded by external circuits. The PMIC provides other outputs for driving external loads (details later).
5. The thermistor network and ADC circuits use the same voltage (VREG_L8).

19.2 MHz XO Source – Layout Guidelines (1 of 3)

Also see comments on ‘Layout Guidelines (3)

Layer 1

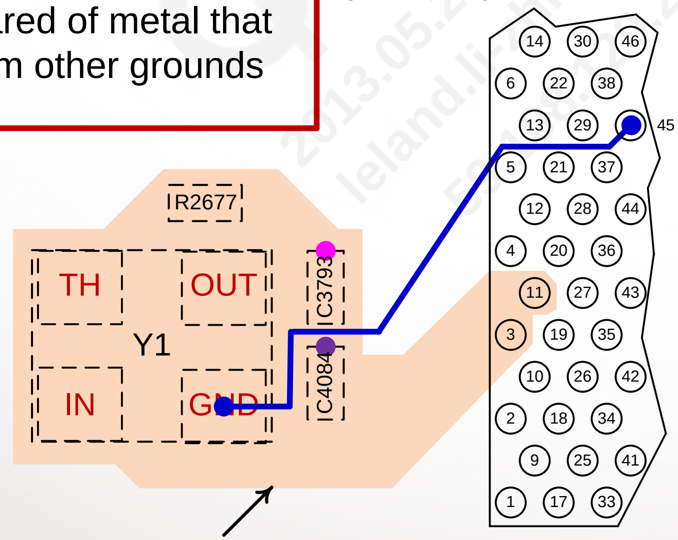


Orange is a ‘moat’ cleared of metal that isolates XO ground from other grounds

- = VREF_XO (magenta)
- = GND_XOADC (blue)
- = XO_THERM (purple)

Layer 2

XO ground points connect to GND_XOADC pin using thin traces

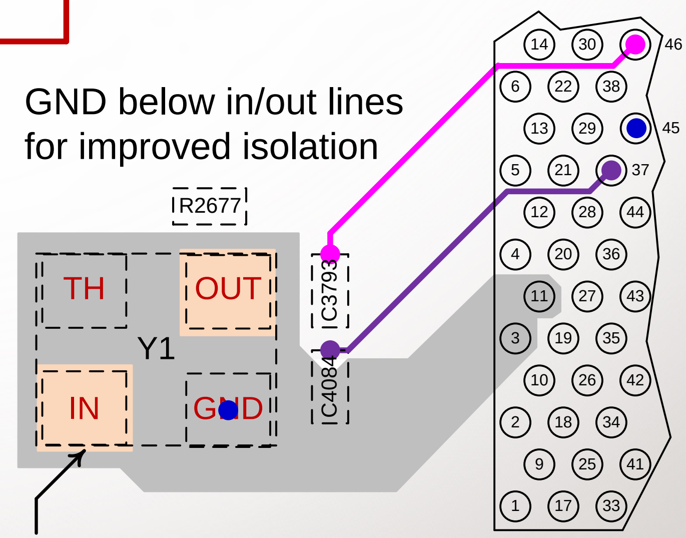


Maintain moat on layer 2 except for thin traces connecting ground points (blue)

Deeper layers

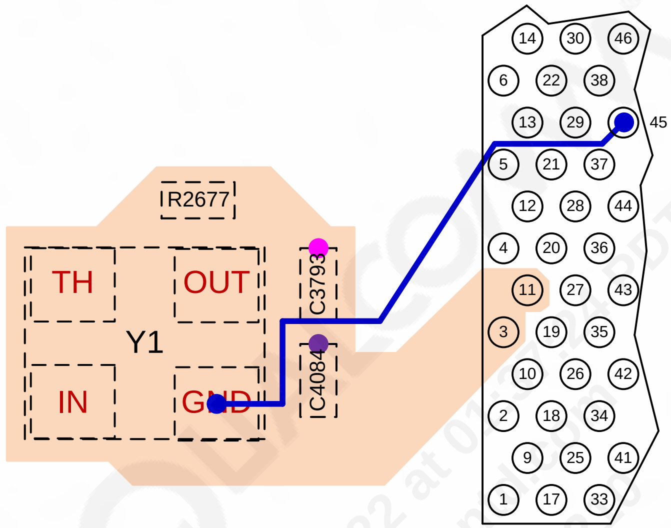
Connect GND_XOADC to main ground plane below pin 45

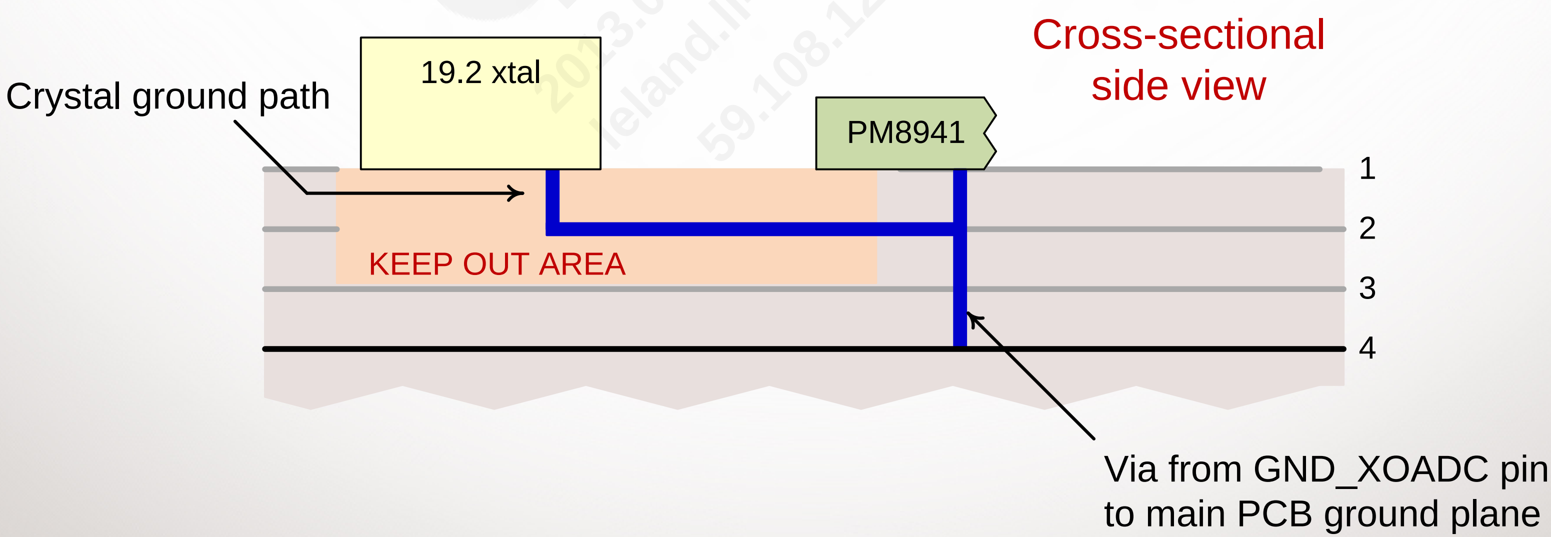
GND below in/out lines for improved isolation



Maintain clearance below in/out pads for reduced parasitic capacitance

19.2 MHz XO Source – Layout Guidelines (2 of 3)





See comments on the following Layout Guidelines slide for more information.

19.2 MHz XO Source – Layout Guidelines (3 of 3)

Crystal location and connections (thermal concerns)

- Locate the crystal 1 to 3 cm from the PMIC
- Provide keep out area as illustrated (no metal)
- Use thin traces for high thermal resistance

Signal connections

- XTAL_19M_IN and XTAL_19M_OUT should not be routed as a differential pair – isolate them
- Isolate from other signals (no parallel routing)
- Thermistor is integrated into the crystal package

R & C close to crystal

- Ground connections
- Connect crystal GND to PMIC GND_XOADC pin using a thin trace
- Connect GND_XOADC pin to main GND using a dedicated via

Note: For best GPS performance, refer to the *Enhanced Guidelines to Implement 19.2 MHz Crystal for Small PCB/High Thermal Layouts* (80-VP447-10) for more information.

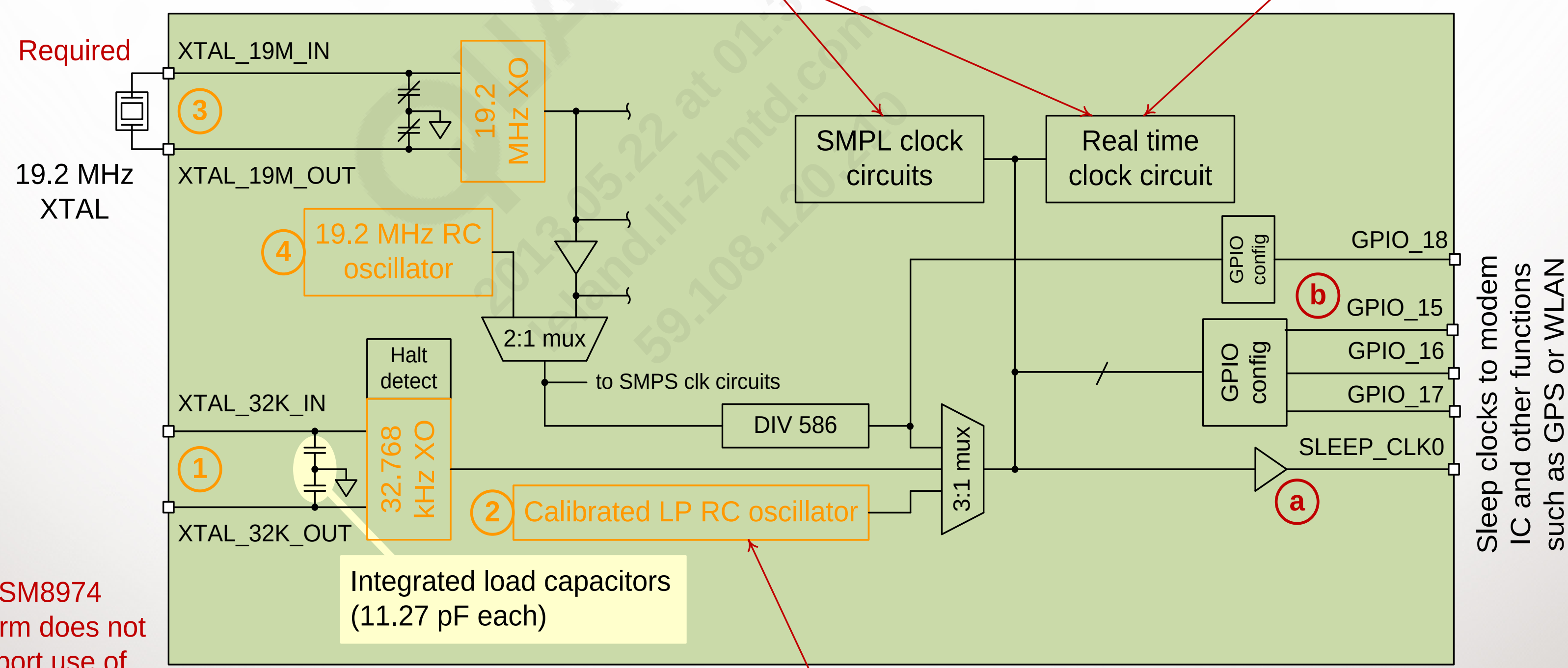
Sleep/RTC Clock Generation and Outputs (1 of 3)

Further discussion on the next slide:

- Source options (orange)
- Switchover
- Output options (red)

- SMPL is supported even if the only power source is a keep-alive capacitor at VCOIN.
- RTC is not supported by keep-alive capacitor; requires qualified coin cell/super capacitor when the main battery is missing.

RTC input clock source
- Uses XO/586 when the device is in active and sleep mode
- Uses calibrated low-frequency RC oscillator when the device is off



MSM8974 platform does not support use of 32.768 kHz XTAL

Cal RC is meant to be used as a RTC clock source and not as a sleep clock source when PMIC is off.

Sleep/RTC Clock Generation and Outputs (2 of 3)

Source options

1. A 32.768 kHz crystal source – This low-power source can have high accuracy and stability, depending upon the external crystal; the 32.768 kHz oscillator circuit is disabled by default in hardware and is not supported in MSM8974 platform.
2. Calibrated low-frequency RC oscillator
   - Used as a source of RTC clock when PMIC is off; requires a qualified coin cell or super capacitor to support RTC when the battery is removed.
   - Periodically uses the XO signal for calibration, achieving accuracy suitable for RTC without an external crystal.
   - Eliminates the external 32.768 kHz crystal, but increases the sleep mode current consumption; the 32.768 kHz oscillator consumes about 1 µA average current, while this solution consumes about 5.5 µA average current.
3. The 19.2 MHz XO divided by 586 (32.7645 kHz nominal) – This is the source of sleep clock and RTC clock when the device is in active and sleep mode.
4. The 19.2 MHz RC oscillator divided by 586 (32.7645 kHz nominal) – 19.2 MHz RC oscillator is a on-chip circuit with coarse frequency accuracy:
   - Used during PMIC powerup until software switches over to XO/586
   - Used in active or sleep mode only if other sources are unavailable

Note: For Cal RC operation details, see the *Use of Super Capacitor for Cal-RC Application Note* (80-N4420-11).

Sleep/RTC Clock Generation and Outputs (3 of 3)

Switchover

- The 32.768 kHz signal is monitored to ensure continuous oscillation. If the 19.2 MHz XO oscillator source stops oscillating, a multiplexer automatically switches to the 19.2 MHz RC signal, and an interrupt is generated. Narrow pulses at the SLEEP_CLK output may occur during this switchover.

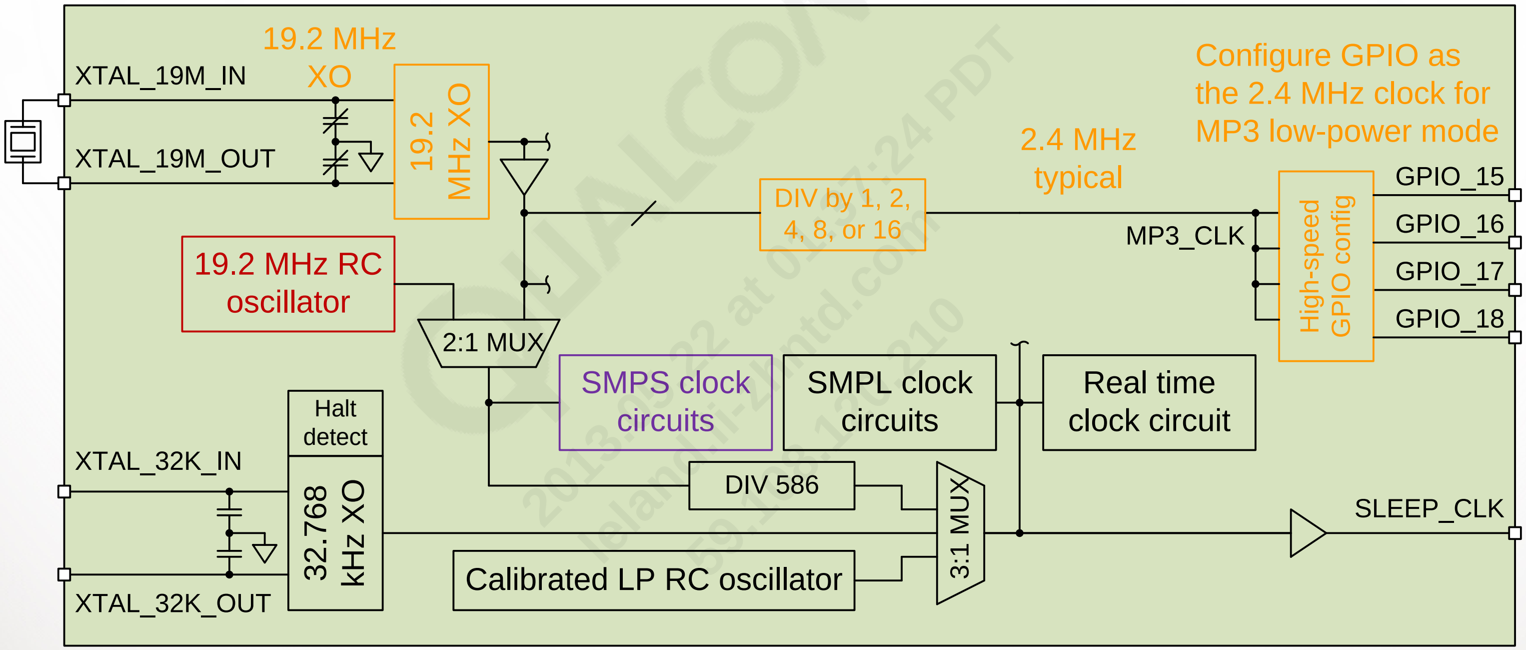
Output options

1. A dedicated output pin (SLEEP_CLK) for the modem IC and others; toggles only when the PMIC is on and stays low when the device is off, even though the crystal oscillator continues to run.
2. GPIO_15, GPIO_16, GPIO_17, GPIO_18 can be configured as sleep clock outputs to support other functions.

Other Clock Topics (1 of 2)

1) MP3 clock

- 19.2 MHz XO source
- Divide by 8 for 2.4 MHz
- Configure high-speed GPIO for external routing



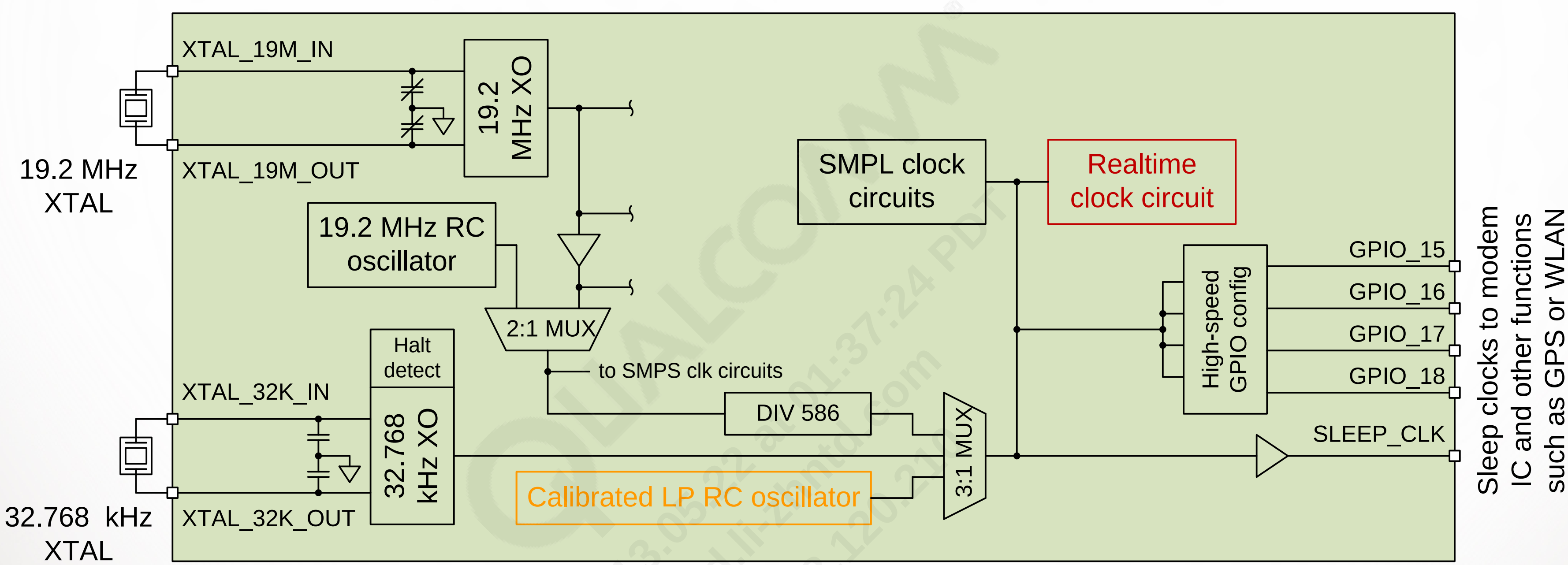
2) 19.2 MHz RC oscillator

- Default clock source during powerup
- Modem IC clears interrupts that allow switchovers to 32.768 kHz XTAL and 19.2 MHz XO sources
- Transitions synchronized, glitch-free
- RC oscillator powered down when not used to reduce power consumption; draws too much current for keep-alive battery – PMIC must be on
- Restarts if XTAL or XO halts

3) SMPS clocks

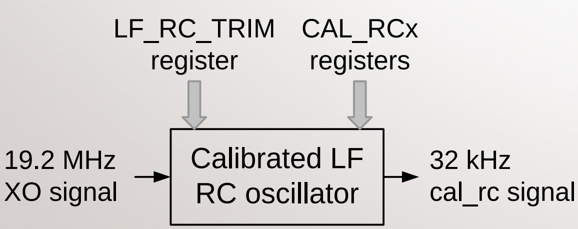
- The switched-mode power supplies are driven by one of two clock sources: 1) RC oscillator or 2) XO source (both 19.2 MHz nominal).
- Programmable and variable divide-by-3 creates 6.4 MHz
- Capable of skipping pulses; allows adjustments so that spectra due to transients can be shifted to minimize RFI

Other Clock Topics (2 of 2)



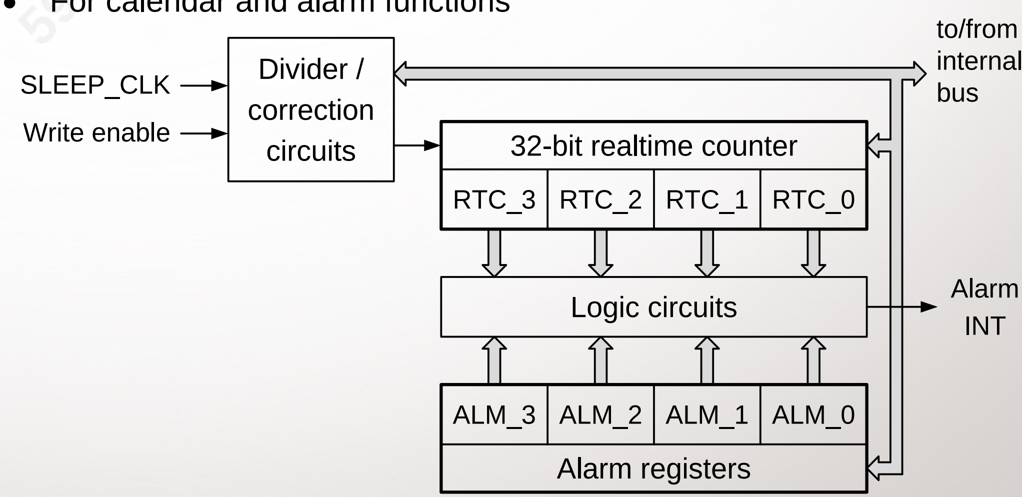
4) Calibrated low-frequency RC oscillator

- Periodically uses XO signal for calibration, achieving accuracy suitable for RTC without external crystal
- Eliminates the external 32.768 kHz crystal, but increases the sleep mode current consumption; the 32.768 kHz oscillator consumes about 1 µA average current, while this solution consumes about 5.5 µA average current



5) Realtime clock (RTC)

- For calendar and alarm functions



RTC Accuracy

The PM8941 supports RTC function without the requirement of a 32 kHz sleep crystal. When the phone is on, a low-power 19.2 MHz XO provides the RTC clock. When the phone is off, the Cal RC is used to maintain the RTC clock.

RTC source	Battery current (μA)	Typical use case accuracy	Coin cap RTC run time, without battery	Notes
19.2 M XO divided (phone on)	80	2 ppm	NA	XO frequency divided by 586 is used as the RTC source.
Cal RC (phone pff)	5.0	46 ppm (4 seconds per day)	1 hr	With default calibration frequency.
32K XO	2.5	30 ppm (2.6 seconds per day, error is determined by crystal tolerance)	2 hr	32 kHz XO is the traditional RTC source. Its performance is listed for comparison purpose only.

A typical case is defined as room temperature and typical battery voltage, 3.7 V or 3.2 V coincell voltage.
Note: Assuming a 33 mF super capacitor

External Clock Components

The reference designs use the Kyocera CT2016DB19200C0FLHA1 as the 19.2 MHz crystal with integrated thermistor.

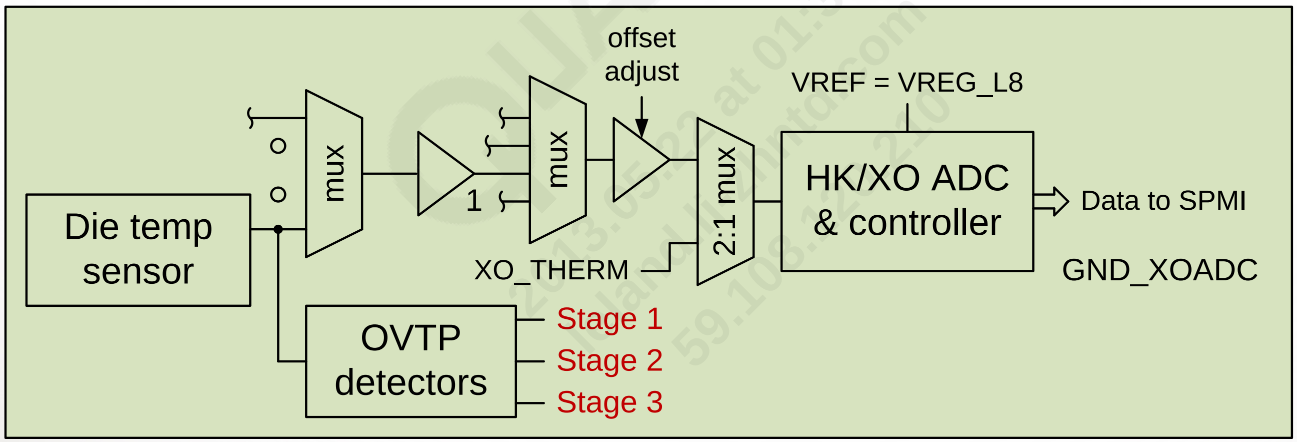
See the *19.2 MHz Modem Crystal Qualification Requirements and Approved Suppliers* document (80-V9690-19) for the following information:

- Data needed from crystal suppliers to demonstrate compliance
- Approved suppliers for different crystal configurations
  - 2.0 mm × 1.6 mm package with integrated thermistor
  - 2.5 mm × 2.0 mm package with integrated thermistor
  - 2.5 mm × 2.0 mm package with pin 2 GND, pin 4 floating
  - 2.5 mm × 2.0 mm package with pins 2 and 4 GND
  - 3.2 mm × 2.5 mm package
- Discussion of various schematic options

Over-Temperature Protection

The PMIC provides over-temperature protection in stages, depending upon the level of urgency as the die temperature rises.

- Stage 0 – Normal operating conditions (less than 110°C); no interrupt is generated.
- Stage 1 – 110°C to 130°C; interrupt sent to modem IC without shutting down any PM circuits.
- Stage 2 – 130°C to 150°C; an interrupt is sent to the modem IC, and high-current drivers (LED drivers, backlight drivers, etc.) are shut down.
- Stage 3 – Greater than 150°C; an interrupt is sent to the modem IC, and PM functions are completely shut down.



Temperature hysteresis is incorporated such that the die temperature must cool significantly before the device can be powered on again.

- If any start signals are present while at stage 3, they are ignored until stage 0 is reached.
- When the device cools enough to reach stage 0 and a start signal is present, the PM circuits will power up immediately.

Automatic Fault Protection (AFP)

The AFP feature of PM8941 is useful to protect the system from damage in the event of a catastrophe. Example catastrophic events include:

- Water damage caused to handset
- Overheating of the handset due to component failure

The PMIC can be put in AFP mode by software or hardware.

- Upon detection of a fault, software can force the PMIC to enter AFP mode.
- If software is non-operational, the PMIC can still enter AFP mode via a dedicated watchdog timer.

AFP Mode – Entry and Exit

Upon entry in AFP mode, the PMIC executes a poweroff sequence:

- High-current circuits, such as backlight drivers, are disabled.
- The FET controls the turn-off system DC distribution paths (battery FET, USB OVP FET, etc.).
- Clocks are turned off.
- Regulators are turned off.

A latch is set that blocks all the poweron triggers except KYPD_PWR_N.

Once the AFP poweroff sequence is completed and the latch is set, the off state is maintained until:

- KYPD_PWR_N goes low, regardless of the VBAT level or charger presence.
- All power sources except VCOIN – including VBAT and chargers – are off.

When one of these events occurs, the latch is cleared and the AFP watchdog timer is reset.

Once the latch is cleared, the poweron triggers are no longer blocked and a normal powerup is executed at the next triggering event. If CBL_PWRx_N is tied to ground, an immediate poweron sequence is started when a valid battery is inserted.

The pull-down on VBAT ensures its voltage changes fast enough to detect battery insertions/removals.

AFP Watchdog Timer and VREG_FAULT

AFP watchdog timer

- The PMIC also has a AFP watchdog timer that can put the device in AFP mode.
- Watchdog timer has programmable timeout settings of 30, 60, 90, and 120 seconds (default) .
- If the watchdog timer is enabled, it barks upon expiry.
- Software has to pet the watchdog timer before it bites (within 6 seconds after the bark) for normal operation to continue.
- If the watchdog bites, the PMIC enters AFP mode.

VREG_FAULT

- When the PMIC is in AFP mode, LDO VREG_FAULT is available to power fault related circuits.
- 1.2 or 1.8 V; 200 mA rating
- The AFP LDO is always off when the PMIC is in off mode.

Other AFP comments

- During AFP poweroff, the PMIC registers are not accessible, but the AFP trigger information is preserved for debugging purposes if a valid coin cell is connected to VCOIN. In this case, the RTC continues to run.
- The PMIC can be configured to perform a warm reset after an AFP event.

User Interfaces

User Interfaces Content

Lighting architecture

Light pulse generators

- Architecture
- Waveforms
- Programmable parameters and controls

RGB LED driver

2x 1A flash driver

- Feature summary
- VPH_PWR dip monitoring
- Mask behavior

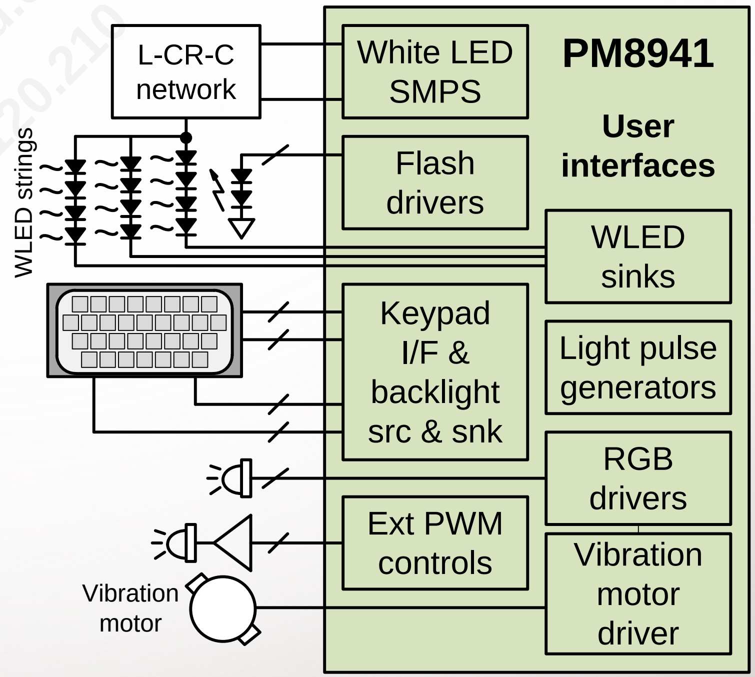
White LED support

- High-voltage SMPS
- Schematic and layout guidelines
- WLED string drivers

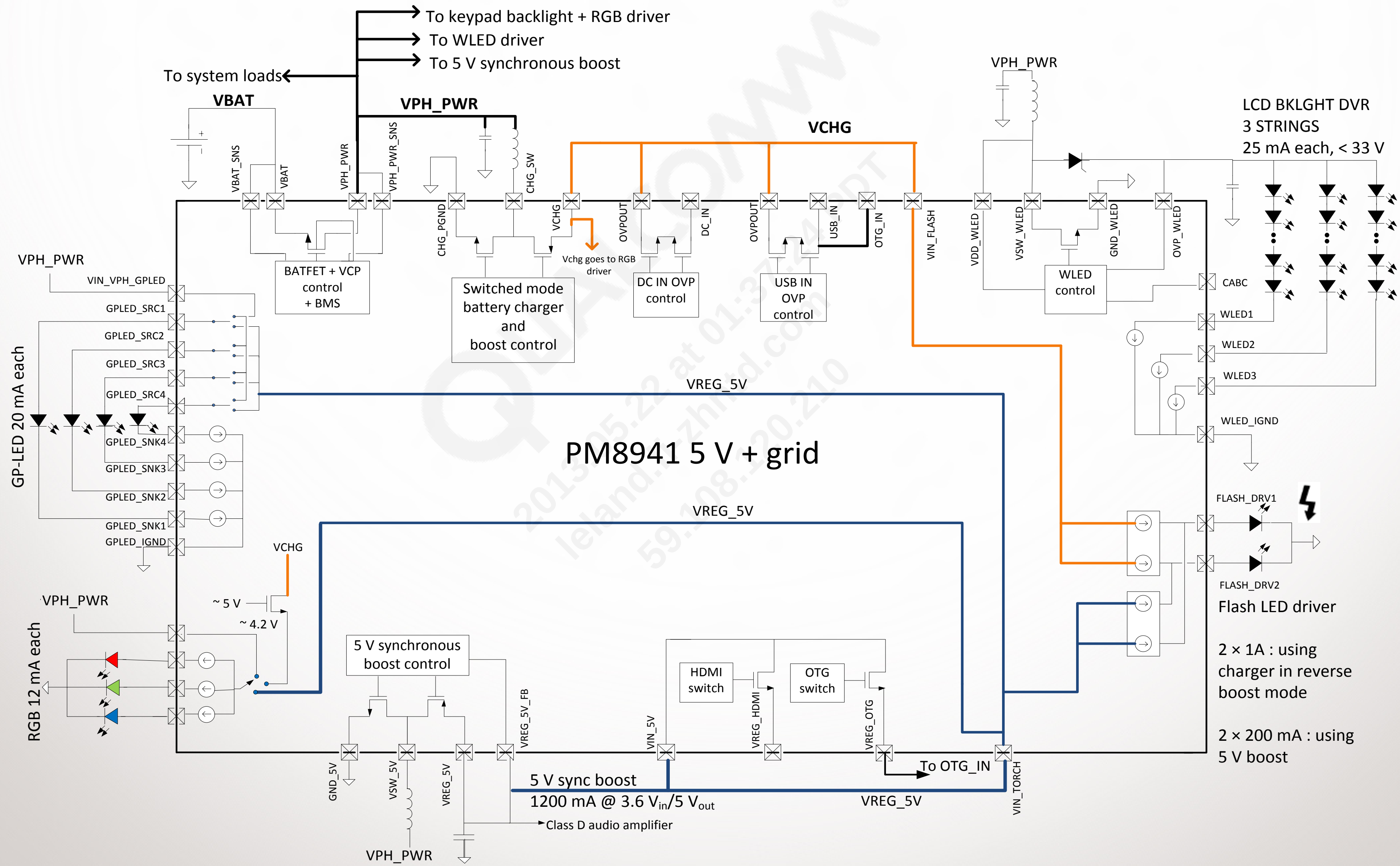
Home row lighting/key illumination

Keypad interface

Vibration motor driver

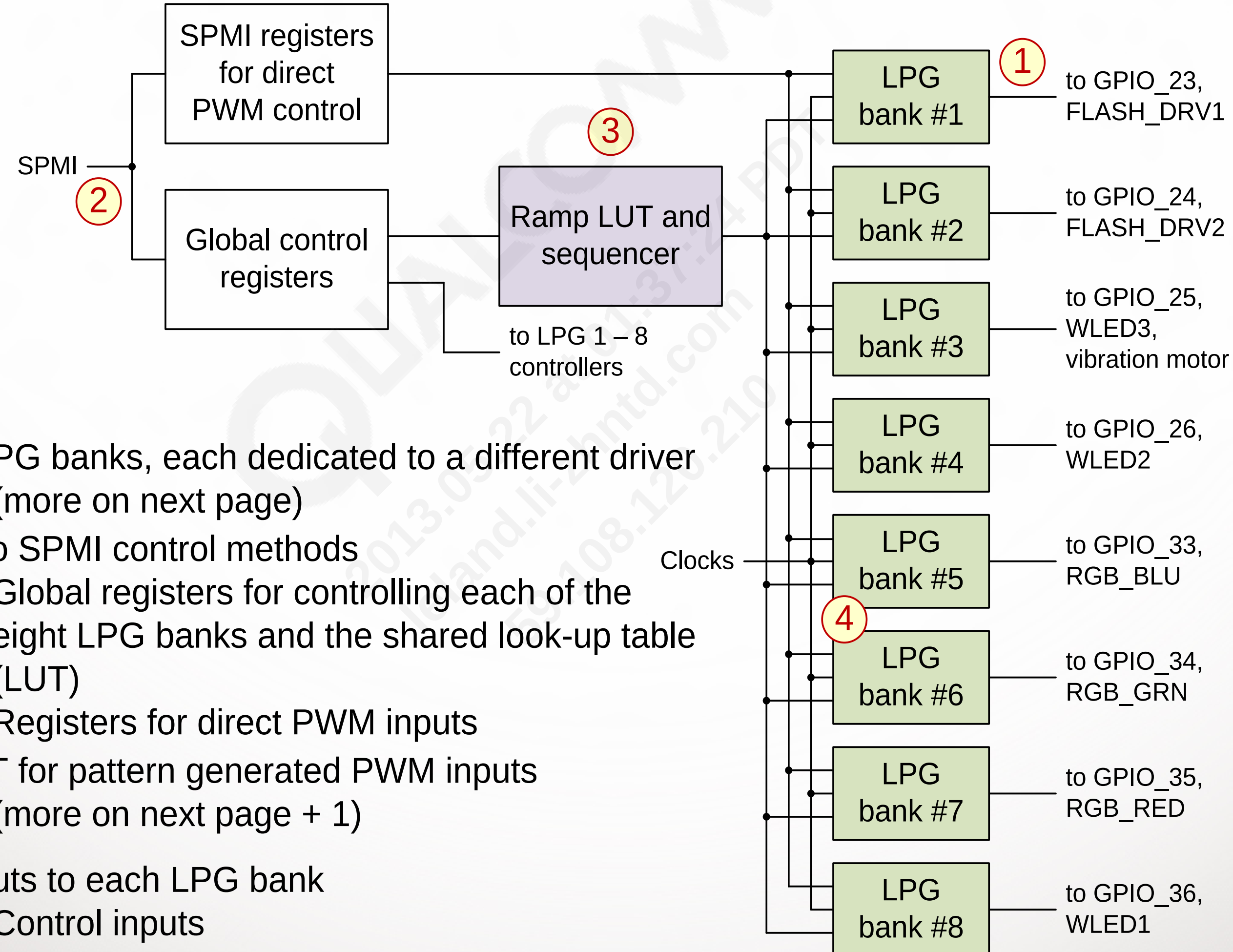


Lighting Architecture



Light Pulse Generators

Two light pulse generator (LPG) circuits – one eight-channel (shown below) and one four-channel that controls the keypad backlighting (GPLED sources and drivers)



1) 8 LPG banks, each dedicated to a different driver (more on next page)

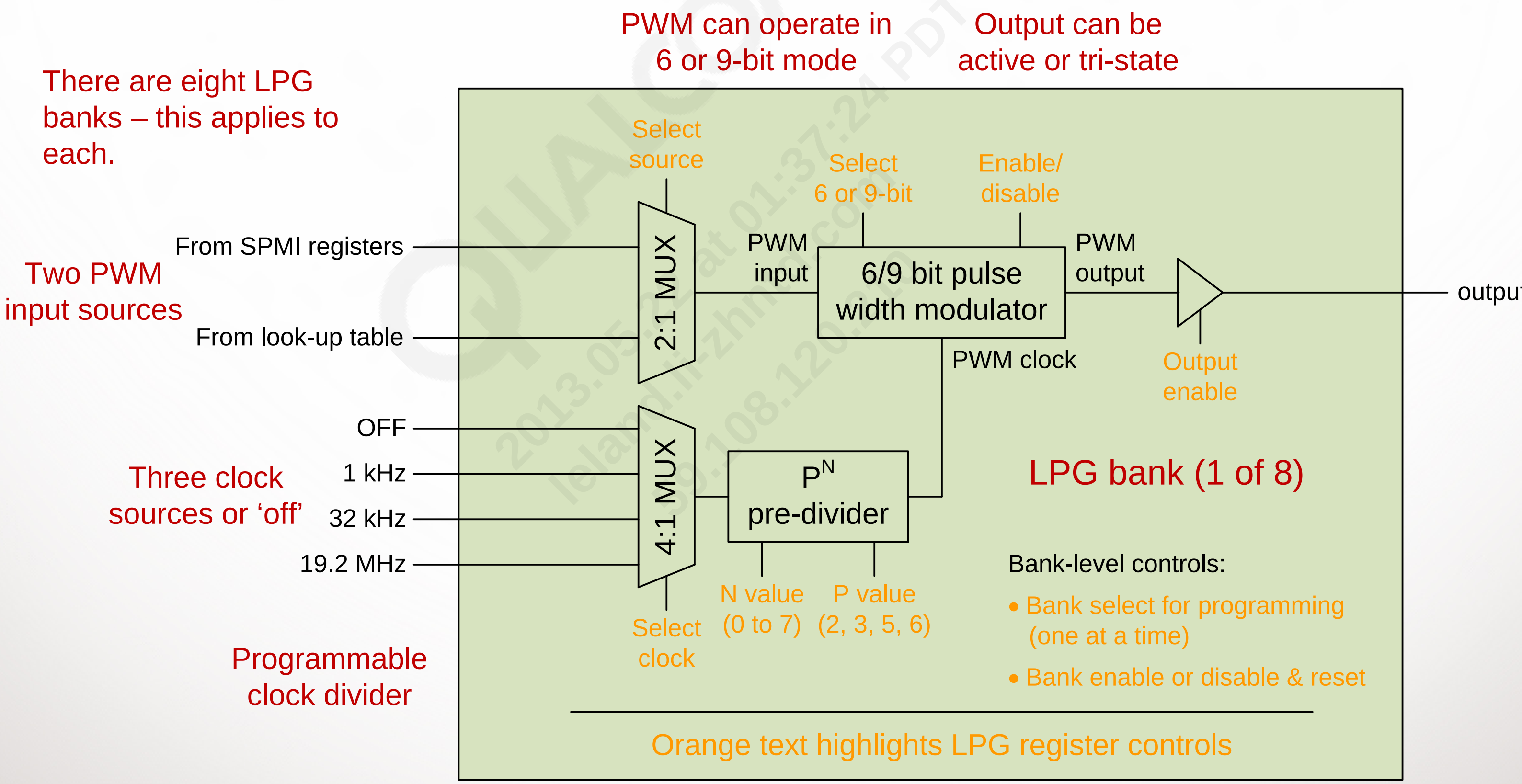
2) Two SPMI control methods
   - a) Global registers for controlling each of the eight LPG banks and the shared look-up table (LUT)
   - b) Registers for direct PWM inputs

3) LUT for pattern generated PWM inputs (more on next page + 1)

4) Inputs to each LPG bank
   - a) Control inputs
   - b) Three clock sources (plus ‘off’)
   - c) Direct SPMI register inputs to PWM
   - d) LUT pattern generated inputs to PWM

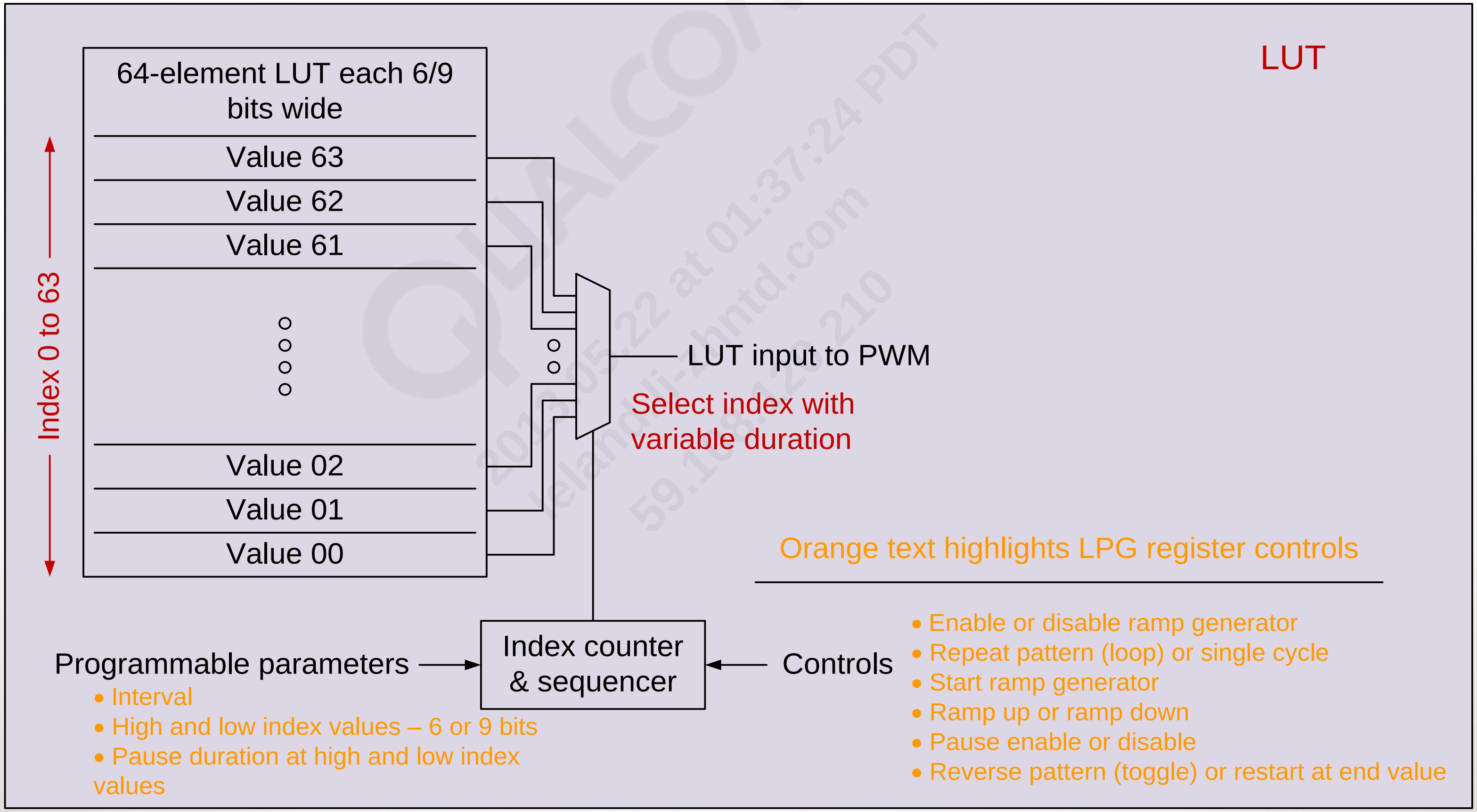
LPG Banks

Item 1 from the previous Light Pulse Generators slide – eight LPG banks, each dedicated to a different driver



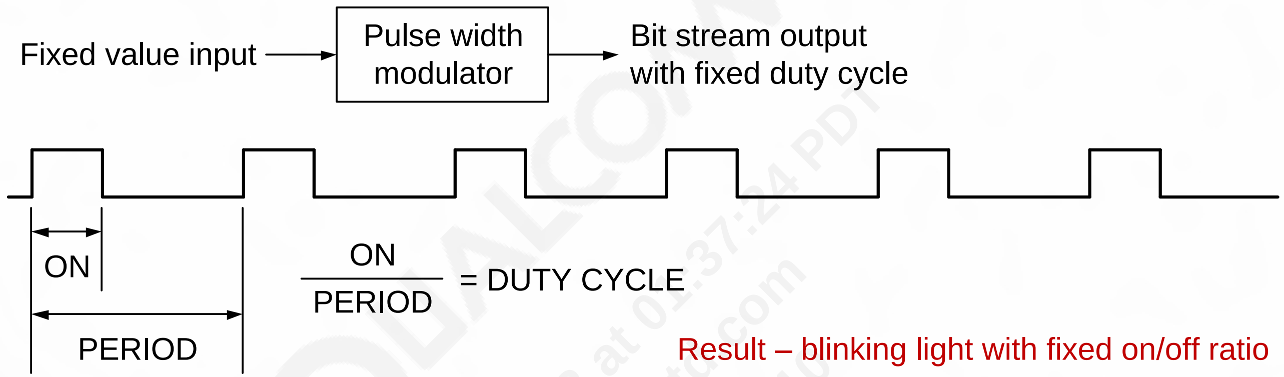
LPG LUT

Item 3 from the Light Pulse Generators slide – look-up table for pattern generated PWM inputs

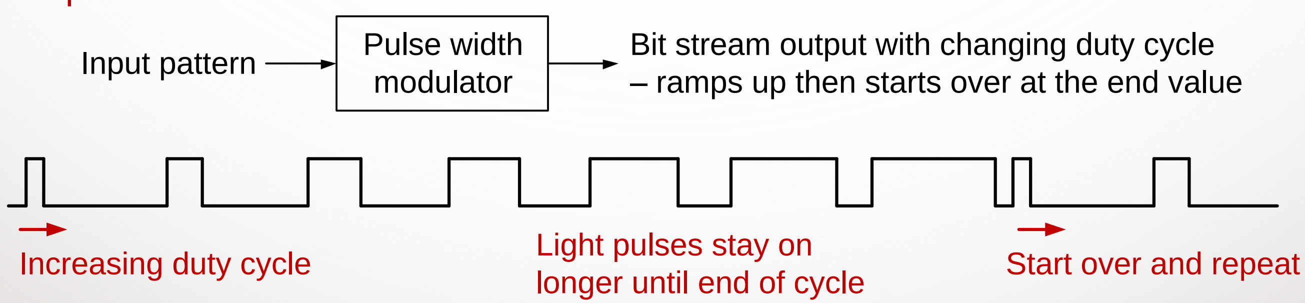


Example PWM Output Waveforms

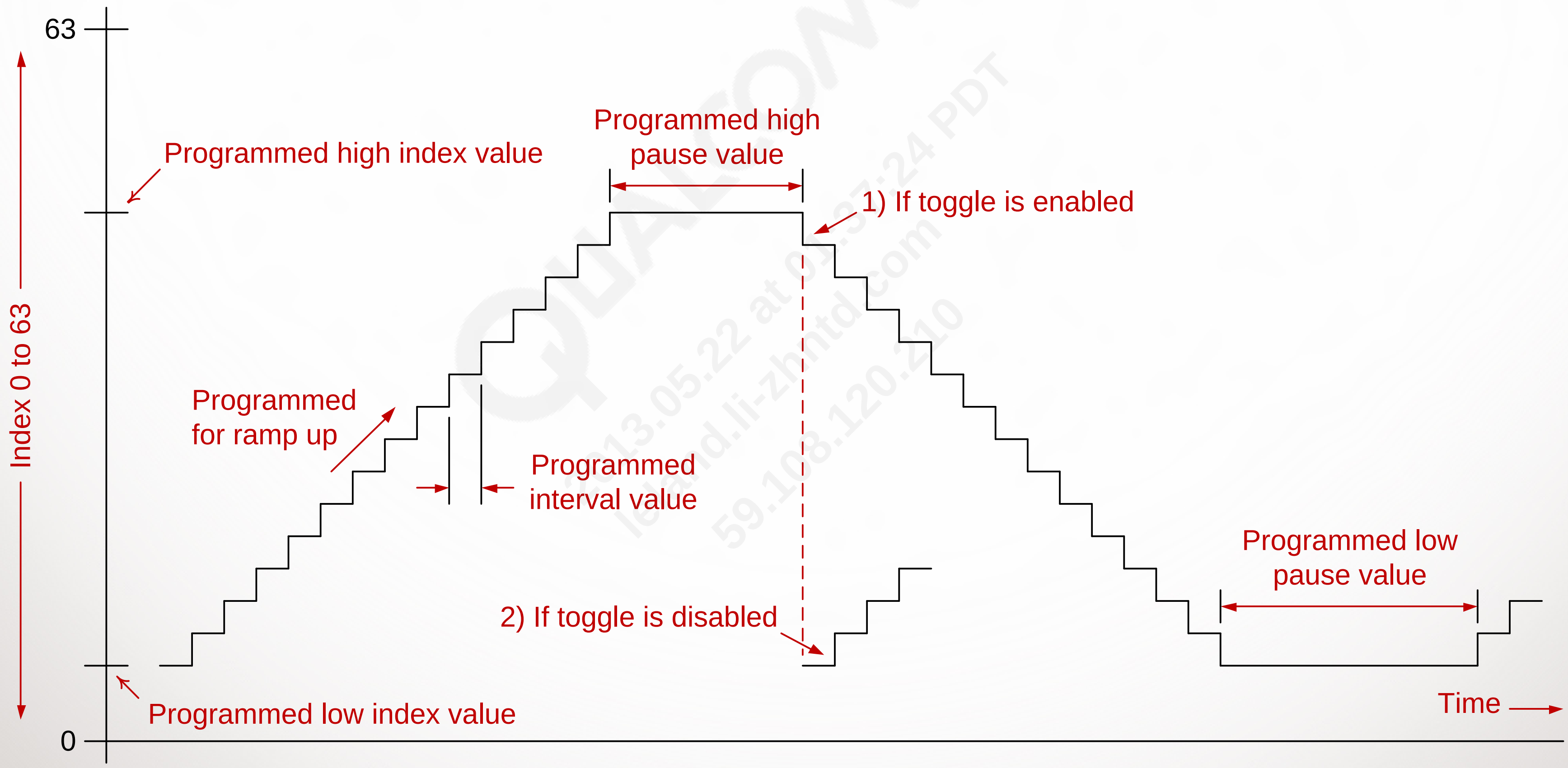
Example 1



Example 2



Example PWM Input Patterns Via LUT

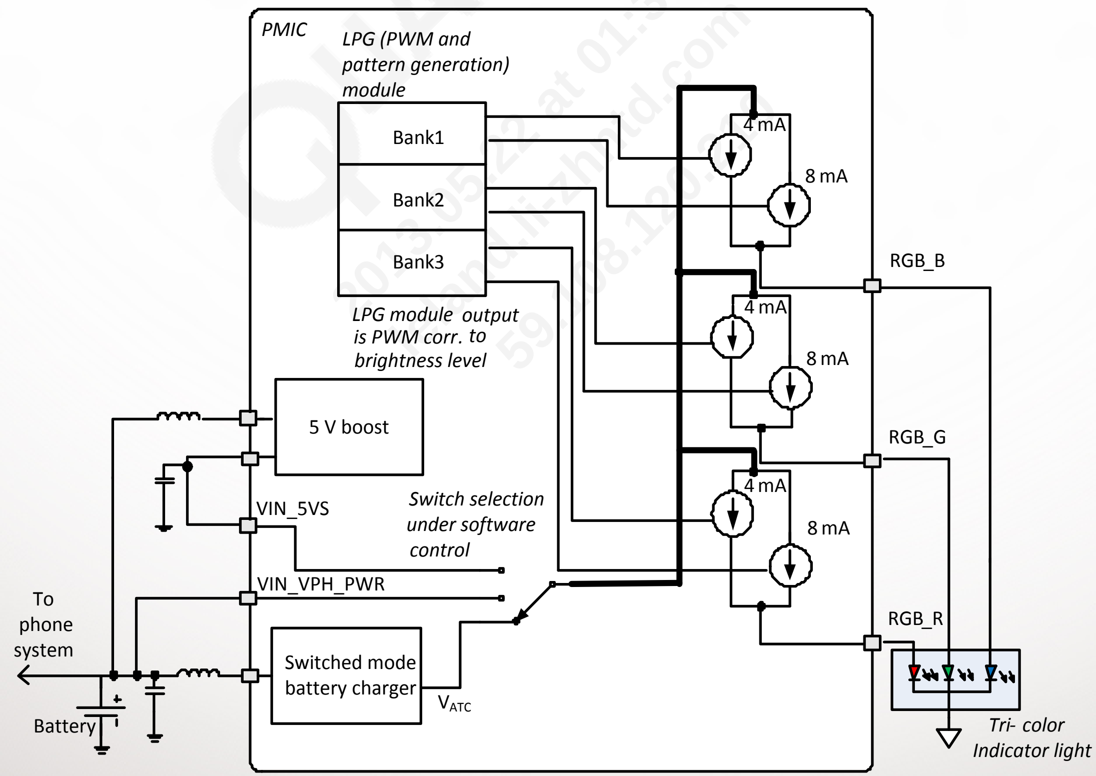


LPG Programmable Parameters and Controls

Parameter or control	Description
Interval	Time spent at each LUT value 1 ms to ~ 1/2 sec; divided down from 1 kHz
Loop	Repeat the pattern or a single cycle
Ramp direction	Up – start low index value, end high value Down – start high value, end low value
Enable ramp generator	Enable or disable
Start LPG ramp	Ramp starts when set; cleared at ramp starts
End value toggle or restart	Toggle – reverse direction at end value Restart – return to start when end reached
High index values	6-bit or 9-bit
Low index values	6-bit or 9-bit
Enable PWM	Enable or disable
PWM input source	Directly from SPMI registers or from LUT
PWM clock source	OFF (no clock), 1 kHz, 32 kHz, or 19.2 MHz
Clock pre-divide value (P)	2, 3, 5, or 6
Clock pre-divide exponent (N)	0 to 7
Pause at low index value duration	1 to 16 (all) then 23 to 7000 (select values) – 1 kHz clock
Pause at high index value duration	1 to 16 (all) then 23 to 7000 (select values) – 1 kHz clock
Enable pause at low index value	Enable or disable
Enable pause at high index value	Enable or disable
PWM output enable	Active or tri-state mode
PWM size	6-bit or 9-bit
LPG bank select	Only one can be programmed at a time.
LPG bank enable	Each can be enabled or disabled individually; when disabled, the LUT is set to its low index value and the interval is set to 0.

RGB LED driver

- Independent brightness control of R, G, and B channels
- Independently programmable duty cycle and period via 3 LPG channels
- 8-bit resolution, digital dimming
- Software control of power source switch from VPH_PWR to VIN_5VS when operating headroom is not met in mission mode
- Constant current (4 mA/channel) during auto-trickle charging. By default, the R and G LEDs are lit.



2x 1 A Flash Driver

Flash power source: the charger module runs in reverse as boost in closed loop with the flash module to minimize internal power dissipation

Concurrency:

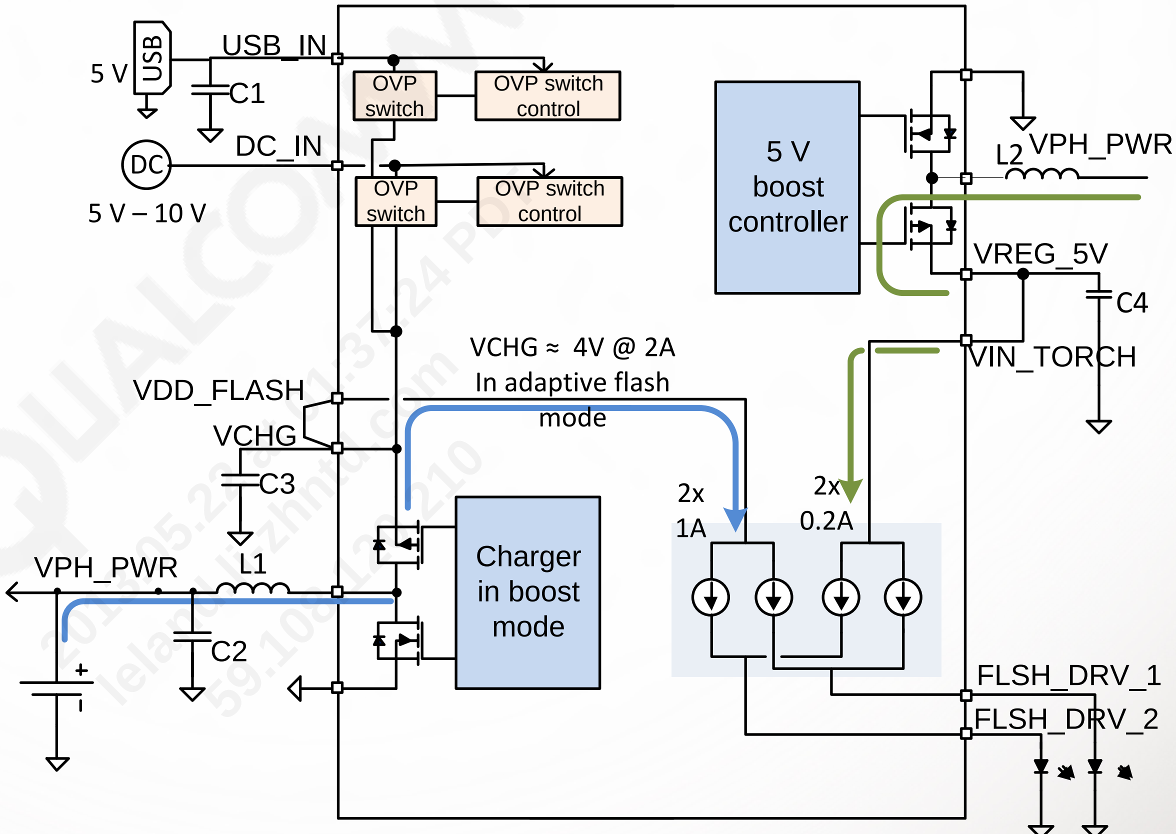
- With external DC_IN, charging is paused while the flash module and charger in reverse boost is used

Video power sources : Uses an internal 5 V boost regulator

Concurrency:

- With class D audio and USB OTG, video current is managed by SW

Flash	Video
2 × 1 A	2 × 0.2 A



Current path for flash mode : from Vph_pwr to charger in boost mode and then using the 2 × 1 A current driver

Current path for video : from Vph_pwr to internal boost (5 V, typ) and then using the 2 × 200 mA current driver

L1	Charger inductor	Toko DFE32251C, 1 µH, I_{sat} = 3.1 A
C3	VCHG cap	2 x Murata 4.7 µF/0603/16 V

Keep FLSH_DRV loop inductance below 100 nH

2x 1 A Flash Driver Feature Summary

Two LED channels, independent current control, 12.5 mA step size

2x 1 A high side current driver for flash

- Flash driver uses internal switched mode battery charger as a boost regulator
- Boost adaptively regulates supply rail (VCHG) to minimum headroom of 300 mV across the two current sources.

2x 200 mA high side current driver for video

- Torch driver uses internal 5 V boost regulator

Supports hardware-controlled (GPIO) or software-controlled flash triggering

Three mask inputs for current clipping during flash event

- GSM_PA_ON, direct video to flash support, spare

Low battery voltage monitoring

- Monitors VPH_PWR at PMIC pin and clips and/or freezes LED current if Vdip threshold is crossed

During flash pulse, the actual current set by software and hardware derating can be read out

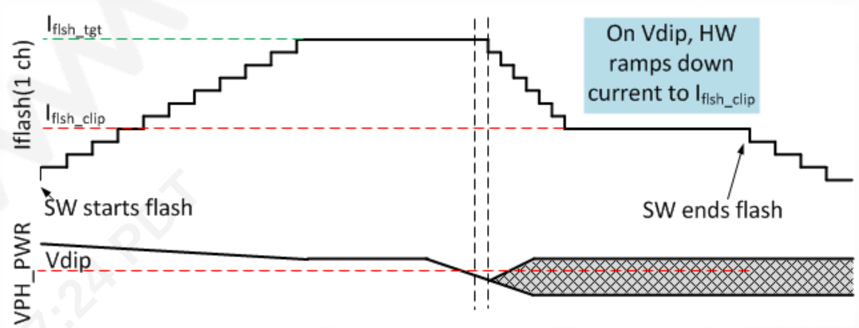
Safety features

- Flash timeout, video watchdog timer, Open LED/Short LED fault detection, thermal derating during flash, hot LED detection

Flash LED VPH_PWR Voltage Dip (V_{dip}) Monitoring and Response

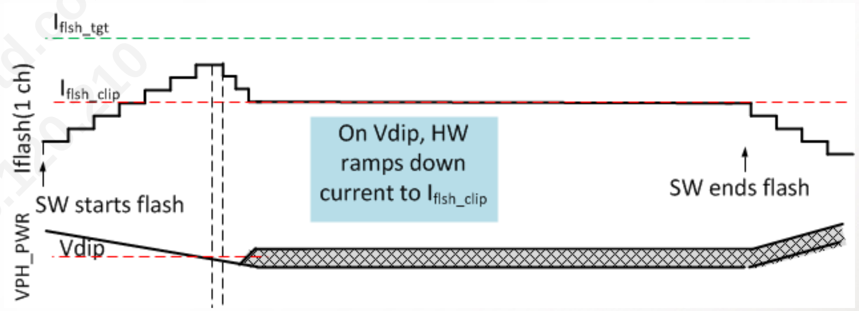
Use case 1

- Flash is at target current, when an additional load causes V_{dip}
- Hardware quickly ramps flash current down to I_{flsh_clip} until flash ends



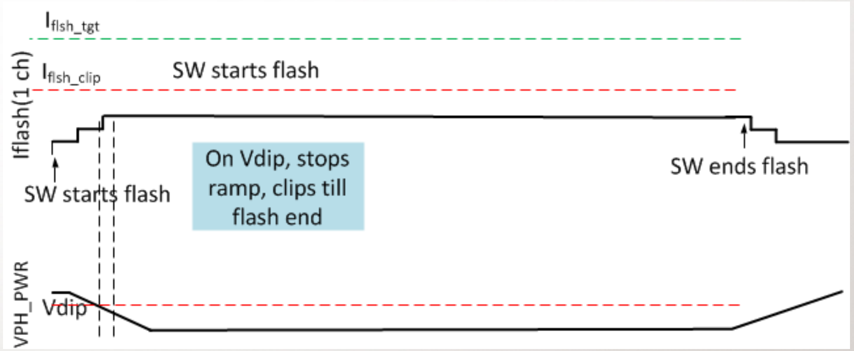
Use case 2

- Flash current is ramping up, when Battery V_{dip} threshold occurs
- Hardware will quickly ramp flash current down to I_{flsh_clip} and keep it there until the flash ends



Use case 3

- Weak battery, start of flash current causes V_{dip}
- Hardware stops ramp and clips immediately, never reaching I_{flsh_clip}
- Software reads out I_{actual} current



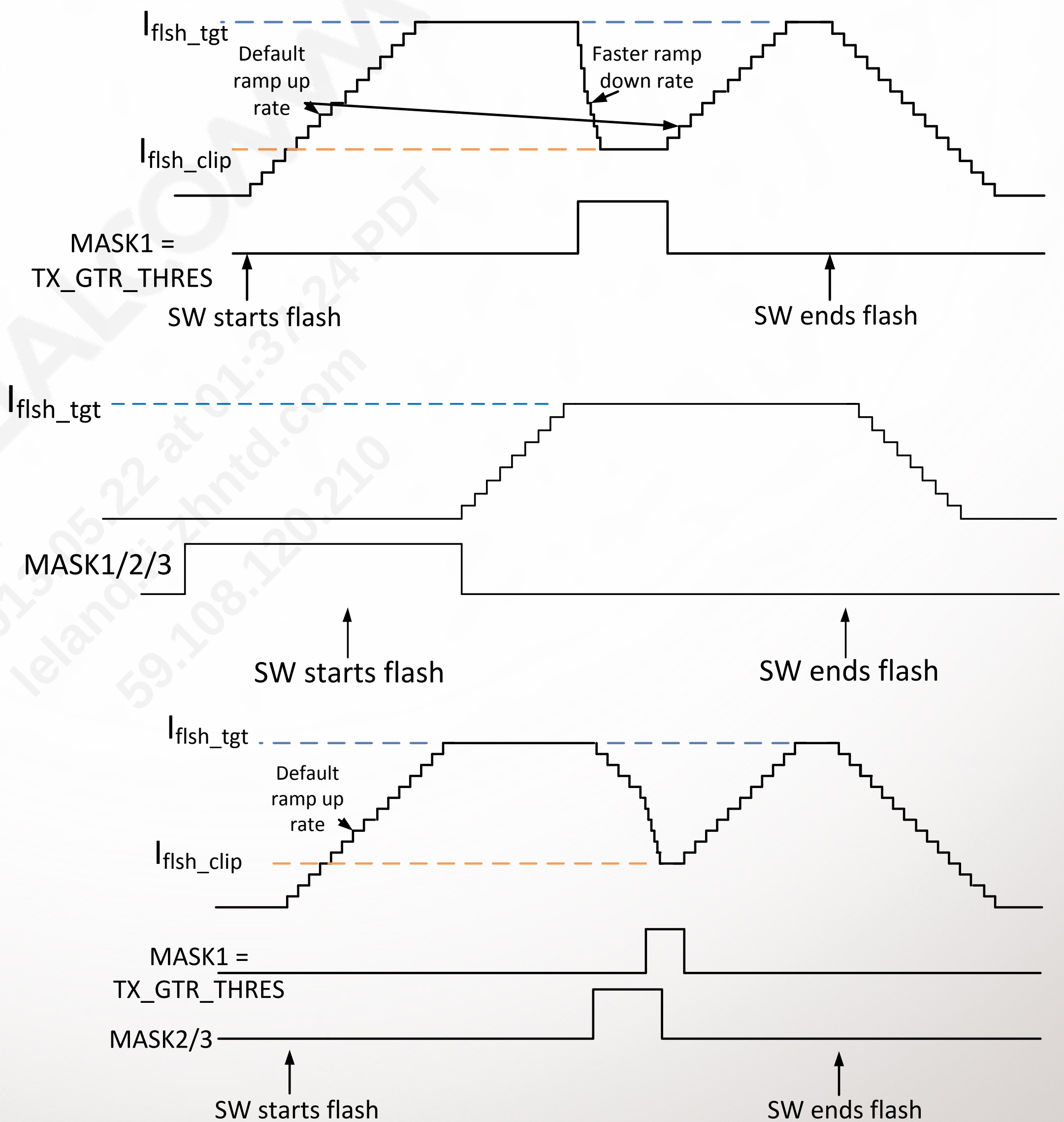
Flash LED Mask Behavior

Mask 1 is used current reduction from Iflsh_tgt to Iflsh_clip during high power GSM Tx. The MSM device sends Tx_GTR_THRES 130 µs before PA on ramp.

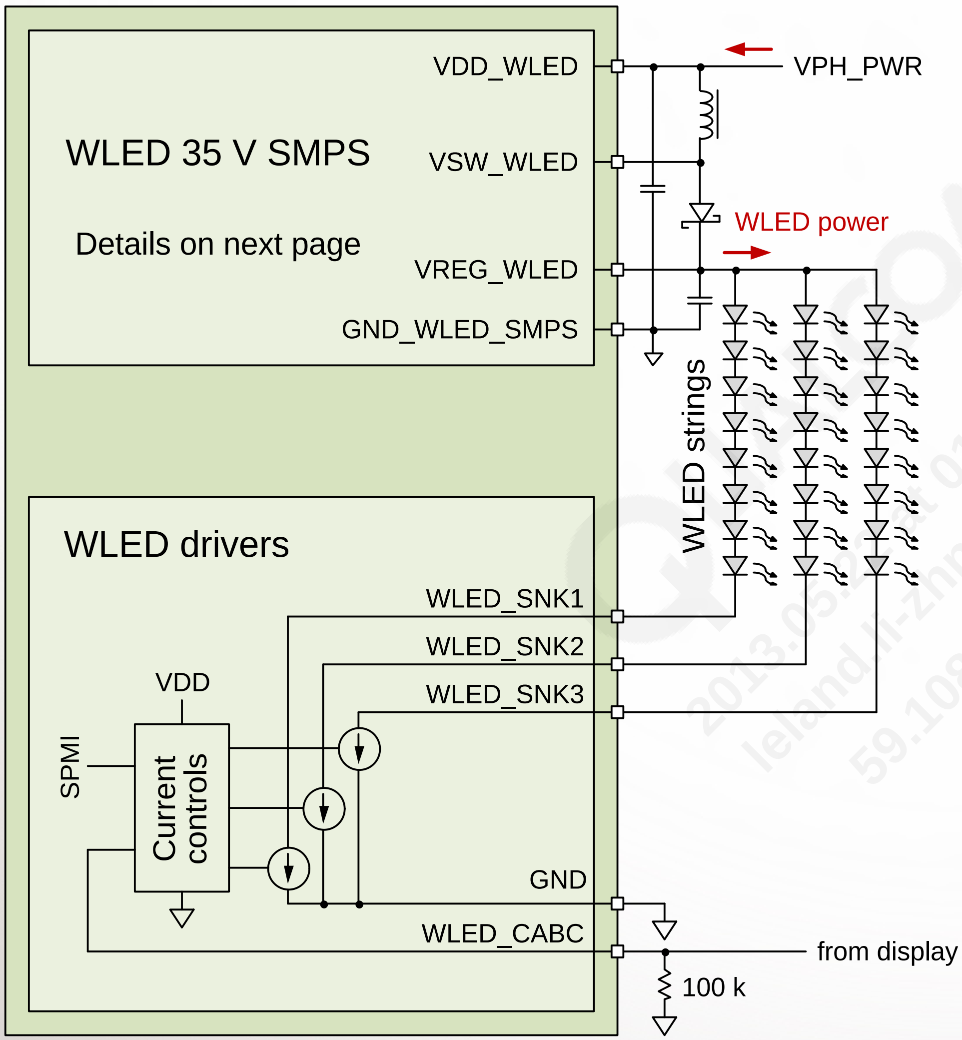
Mask before software trigger disables Iflsh_clip ramp until the mask is removed.

Mask 1 takes priority in ramp down rate over Mask 2/3.

All masks share setting (programmable) for Iflsh_clip.



White LED Support



Integrated boost SMPS generates the high voltage needed for white LEDs.

- SMPS details on next page

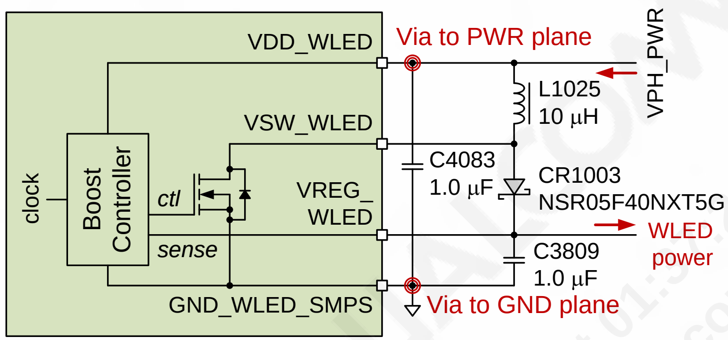
Three ground-referenced current sinks

- Each support a string of up to 8 LEDs
- 25 mA each
- Dedicated ground pin

White LED content adaptive backlight control (CABC) is supported.

- Connect the WLED_CABC pin to ground through a 10 k resistor if this feature is not used.

WLED SMPS Schematic and Layout Guidelines



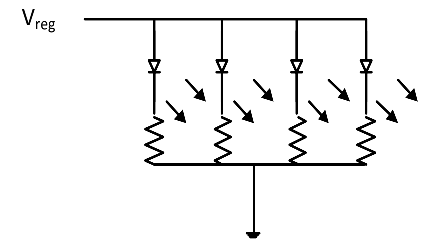
Same placement and layout guidelines apply to the WLED boost SMPS as HF SMPS. Example placement and layout can be seen in the top-level design topics section later in the slides.

Home Row Lighting/Key Illumination

2 to 4 WLEDs

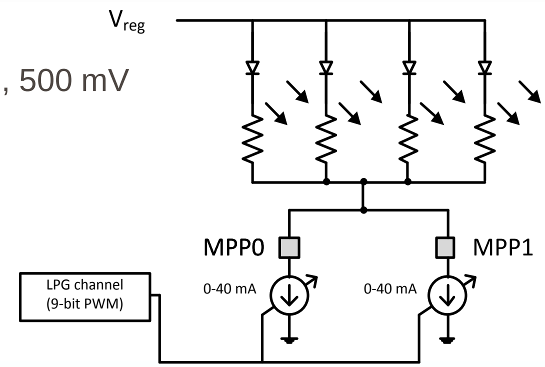
Option #1

- Four ballast resistors for matching and current limiting
- Power source can be Vsys or regulated supply rail (see diagram at right)
- Available in most PMICs



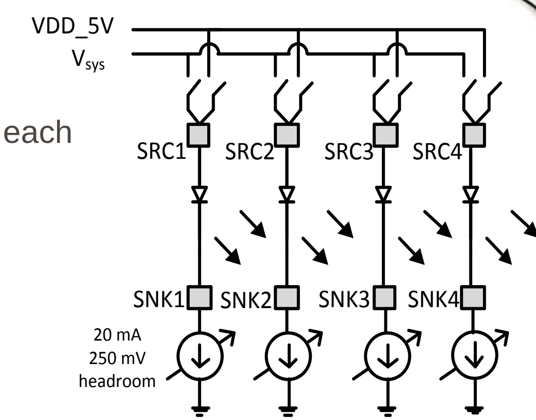
Option #2

- Use one to two MPPs as current sinks (80 mA total, 500 mV headroom)
- Uses Vsys or regulated rail as power source
- LED brightness is controlled via PWM (6-bit/9-bit LPG output)
- Available in most PMICs



Option #3

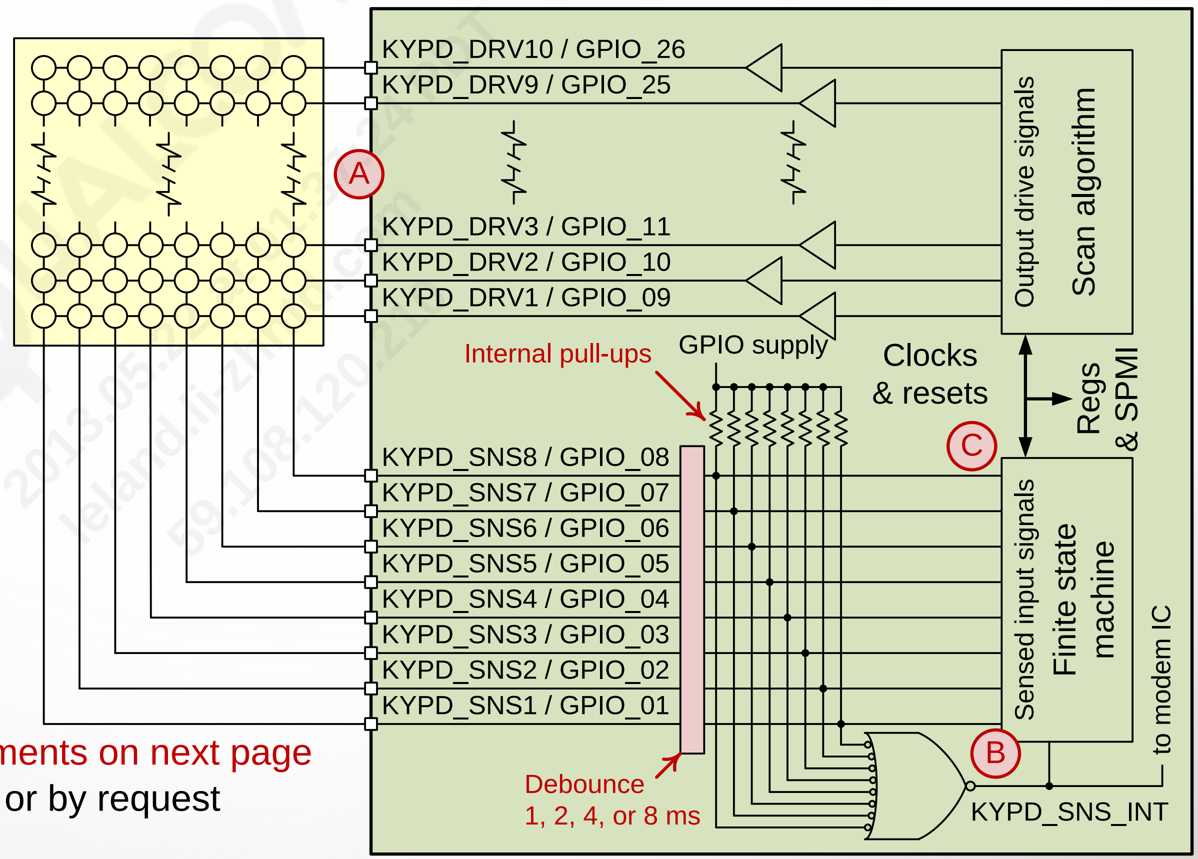
- Four individually programmable current sinks at 20 mA each
- Each current sink controlled via PWM (8-bit resolution)
- 250 mV headroom
- Software switch to Vbst (5 V) when Vsys drops below threshold
- 2% matching, 2% accuracy



Keypad Interface

A keypad button press is detected by ORing all column signals (KYPD_SNSx) together

- Before a keypad button is pressed, all rows are driven low. A
- When a button is pressed, its corresponding column is pulled low (since all rows are low).
- The interrupt is asserted when any keypad button, from any column, is pressed. B



When the interrupt signal is received, the FSM requests the next scan.

- During a scan, each row is sequentially driven low, one at a time. A
- As each row is driven low, the columns are sensed. C
- The pressed button is identified when that button's column reads low while its row is driven low.

Other operational details – plus enhancements on next page

- A scan can be initiated by a key press or by request from FSM to get next keypad entry.
- After a scan, the FSM compares current and last data; an interrupt is generated if there was a change.
- The modem IC must read the stored key presses via SPMI.
- The delay between scans is programmable (4, 8, 16, 32, 64, or 128 ms).

Keypad Scan Enhancements

Up to 16 keys can be programmed to wakeup the processor, while all others are masked out; masking is bypassed when the full keypad is enabled, ensuring that all keys can generate an interrupt for normal operation.

The wakeup can be executed in response to any of the following conditions:

- A software-defined single key is pressed, and no other keys are pressed.
- A software-defined two-key combination is pressed and no other keys are pressed.
- A software-defined three-key combination is pressed and not other keys are pressed.

The software-defined combinations are mutually exclusive – any key used for the one-key wakeup cannot be used in any other combination.

Three separate wakeup combinations can be programmed:

- One can be used to trigger a warm reset.
- One of the remaining two can be used to trigger a hard reset.
- The main purpose is to execute the poweron sequence.

Warm resets include a programmable debounce time of up to 3.5 seconds, in 0.5 second steps.

A hard reset can be debounced up to 15 seconds in 1 second steps.

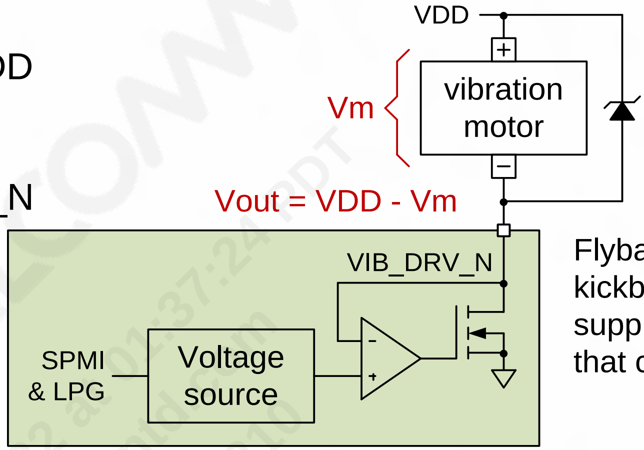
During debounce, the keypad continues to be scanned and sampled.

The entire key combination must be pressed during the reset debounce time to generate the intended warm or hard reset.

Vibration Motor Driver

The vibration motor driver supports silent incoming-call alarms with a dedicated output pin (VIB_DRV_N).

- Programmable voltage output referenced to VDD
- When off, the output voltage is VDD
- Motor connected between VDD and VIB_DRV_N
- Voltage across motor is V_m = VDD - V_{out}
- Vout is the voltage at the PMIC pin.



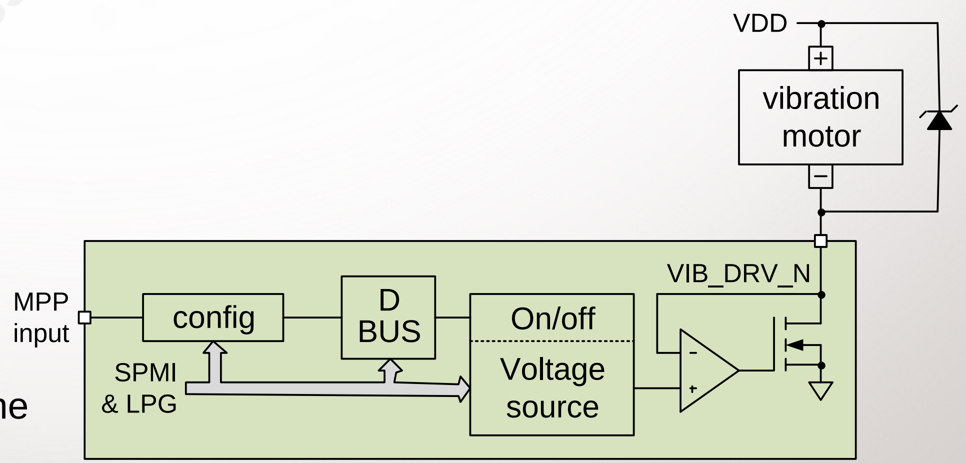
Flyback diode prevents inductive kickback during turn-off, thereby suppressing voltage transients that could damage the IC.

The driver is programmable for motor voltages from 1.2 to 3.1 V in 100-mV increments.

Short circuit current limiting protects the IC when the motor is stalled or shorted.

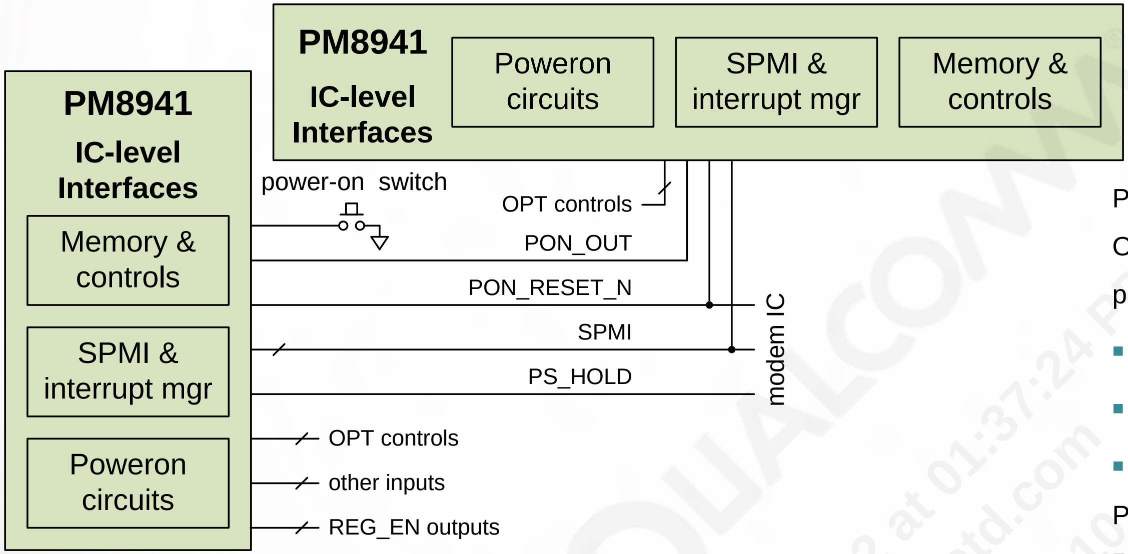
The PMIC provides the option to control the motor driver through an MPP, thereby providing greater flexibility in defining on and off vibration intervals. The following API software steps are required:

- Configure the MPP as a digital input
- Define that MPP to be one of three DBUS signals
- Define the polarity of the control signal
- Define the vibration motor driver on/off control to the same DBUS signal



IC-level Interfaces

IC-Level Interfaces Content



Poweron circuits and coordination between PMICs

OPT hardware configuration controls

programmable boot sequence (PBS)

- Use cases
- Triggers
- Programming

Poweron/poweroff sequence

Resets

- Nomenclature
- Reset sources
- 3-stage reset
- Reset timers

Under-voltage lockout

Sudden momentary power loss (SMPL)

SPMI and interrupt managers

Modem power management support

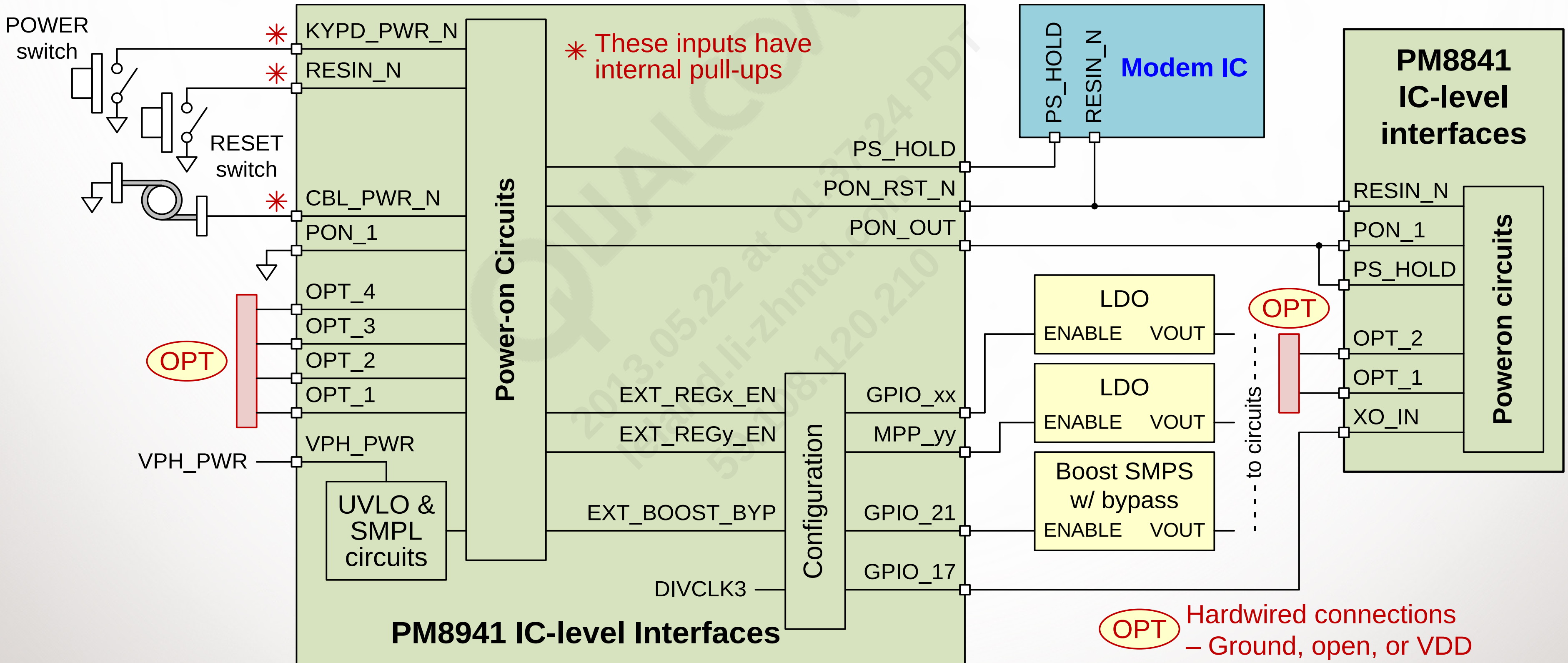
Battery UICC alarm (BUA) interface

- Introduction
- Overview
- Operation

Other IC-level interface uses for MPPs and GPIOs

Poweron Circuits

- Dedicated PM8941 circuits continuously monitor events that might trigger a poweron sequence
- If an event occurs, these circuits power on the IC, determine the handset's available power sources, enable the correct source, enable the PM8841, and take the modem IC out of reset



OPT Hardwired connections
- Ground, open, or VDD
- Sets some PMIC features
- See the following slides for more information

- To power up immediately upon battery insertion, tie KYPD_PWR_N or CBL_PWR_N to ground
- In this case, the PMIC is always on and the modem IC should clear the xxxPWR_PU bit to turn-off the internal pull-up resistor, thereby reducing the PMIC quiescent current.

PM8941 OPT Hardware Configuration Controls (1 of 2)

Four PM8941 pins – OPT_[4:1] – must be hardwired to ground or VDD, or be left open (in a high-impedance state or Hi-Z); the settings of these four pins defines or influences the following PM8941 parameters:

Each chipset that uses the PM8941 must set the OPT pins correctly for their particular application; the MSM8x74-based reference designs use these settings: OPT_[4:1] = GND, GND, GND, GND

OPT_1	External reset configuration
GND	KYPD_PWR_N + RESIN_N
Hi-Z	RESIN_N
VDD	KYPD_PWR_N

OPT_2	Chipset support
GND	MSM8974
Hi-Z	Reserved
VDD	Reserved

PM8941 OPT Hardware Configuration Controls (2 of 2)

OPT_3	PMIC watchdog
GND	Disabled
Hi-Z	Enabled
VDD	Reserved

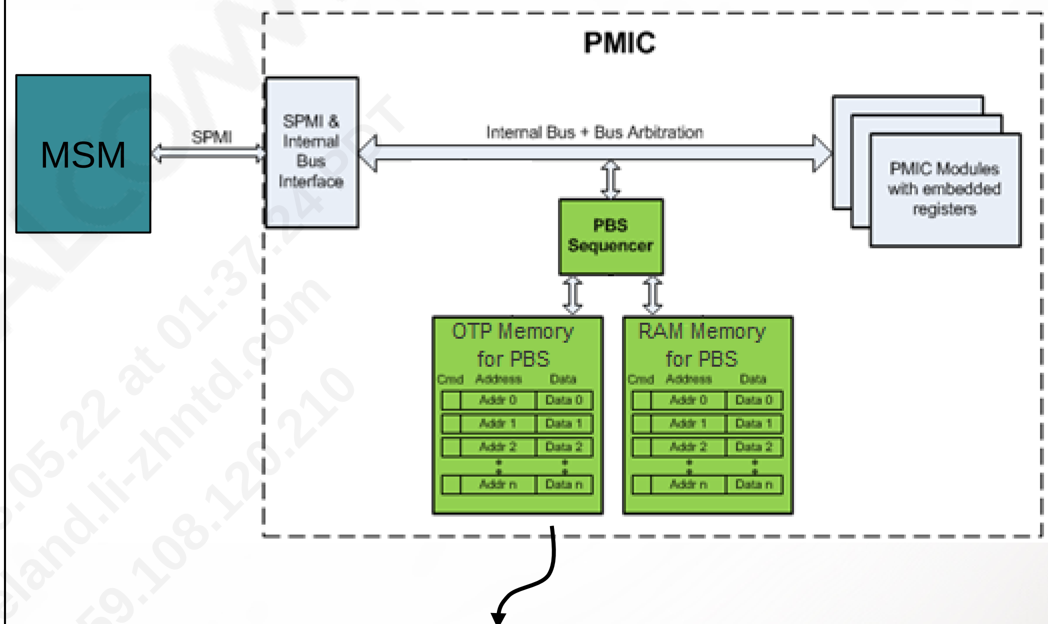
OPT_4	Chipset support
GND	MSM8974
Hi-Z	Reserved
VDD	Reserved

Programmable Boot Sequence (PBS)

Key features:

- Custom **programmable boot sequences** configured with OTP and RAM
- Implemented as a series of address + data transactions which mimic normal software control
- Programmable control of any PMIC resource in any order with any available programmable configuration
- Support for **API-like routines** are implemented with OTP-defined sequences. Initiate via SPMI write to address pointer or via hardware trigger
- Support for a **limited command set** of executable functions

PBS illustrative concept drawing



PBS command set

- Write/read
- Delay
- Compare
- End-of-sequence
- Up to 256 commands supported in RAM
- Up to ~232 commands supported in ROM (OTP) with some space reserved for PTE, version control

PBS Use Cases

Poweron sequence (OTP)

- Make decisions based on the state of option pins or other registers
- Enable regulators, change GPIO/MPP states
- Wait for event to occur (register to change state, timer to expire)
- Change register defaults (e.g., charger limits) prior to enabling module

Poweroff sequence (OTP)

Custom poweroff sequence (RAM)

- Blink LED, toggle vibrator motor, etc., as handset shuts down

Battery UICC alarm (RAM)

- Disables LDOs based on hardware triggers (battery removal, UICC card removal)

Sleep/wake batch sequence

- Several writes can done quickly when entering/exiting sleep to reduce software workload.
- Can vibrate the VIB motor before initiating shutdown operation

PBS Triggers

There are 16 different PBS clients in PM8941 and 8 in PM8841.

Each client can be programmed to point to any address within OTP or RAM.

Each client can trigger a sequence via software (e.g., register write) or a hardware trigger (see list below).

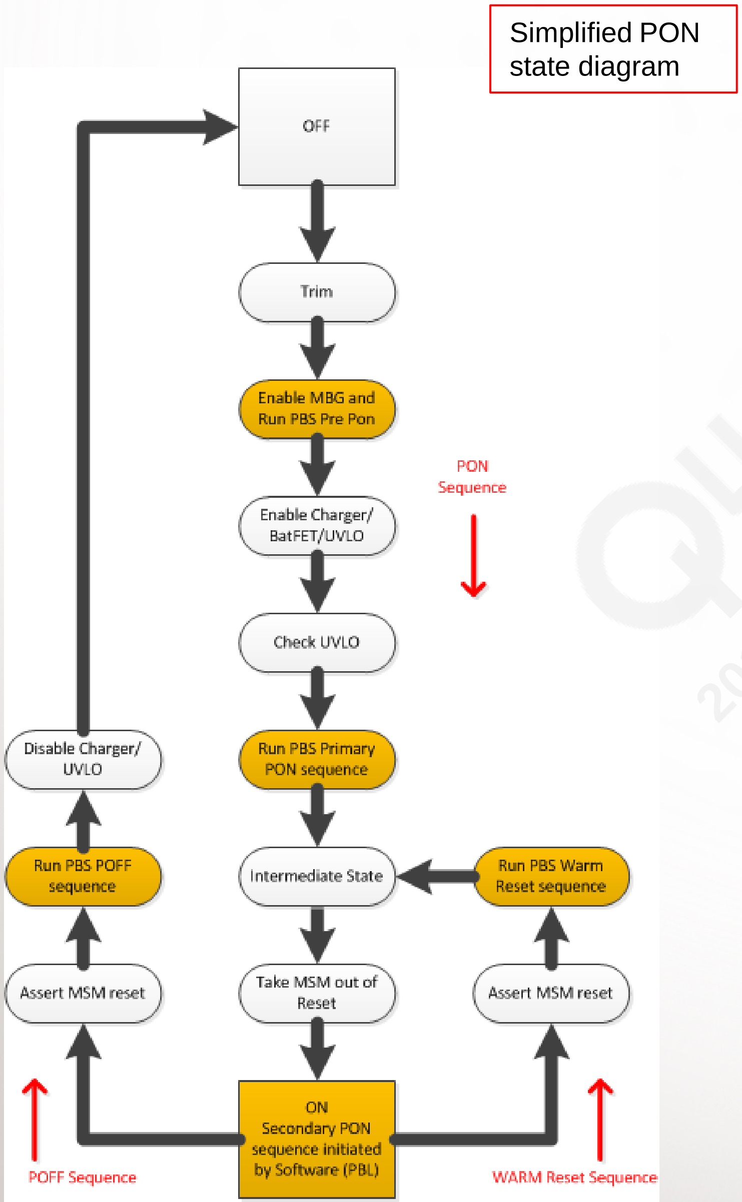
PM8941

- Trigger 1 – Secondary poweron
- Trigger 2 – Primary poweron
- Trigger 3 – Warm reset
- Trigger 4 – Shutdown
- Trigger 5 – XO_OUT_D0_EN
- Trigger 6 – XO_OUT_D1_EN
- Trigger 7 – Battery UICC alarm
- Trigger 8 – Reserved
- Trigger 9 – Pre-poweron
- Trigger 10 – Sleep
- Trigger 11 – RTC alarm
- Trigger 12 – RTC timer
- Trigger 13 – DTEST1
- Trigger 14 – DTEST2
- Trigger 15 – DTEST3
- Trigger 16 – DTEST4

PM8841

- Trigger 1 –Secondary poweron
- Trigger 2 – Primary poweron
- Trigger 3 – Warm reset
- Trigger 4 – Shutdown
- Trigger 5 – DTEST1
- Trigger 6 – DTEST2
- Trigger 7 – DTEST3
- Trigger 8 – DTEST4

Poweron/Poweroff/Warm Reset Sequence



PBS is run three times during poweron.

1. Configure features (i.e. charging) prior to enabling anything in the system
2. Enable the minimum infrastructure required to boot MSM and start fast low current boot image (FLCB)
3. Enable Krait, eMMC, etc., once it is established that the battery is sufficient, or a charger is available.

PBS runs once during shutdown for regulator sequencing.

- Can also support shutdown indication (e.g., flash LED)

PBS runs once during warm reset.

PBS Programming

PBS OTP

- Programmed during ATE by Qualcomm; customers cannot modify it.
- Option pins allow for adjustment of the sequences or to set certain features within the PMIC.
- Some area needs to be reserved for future enhancement or workarounds.

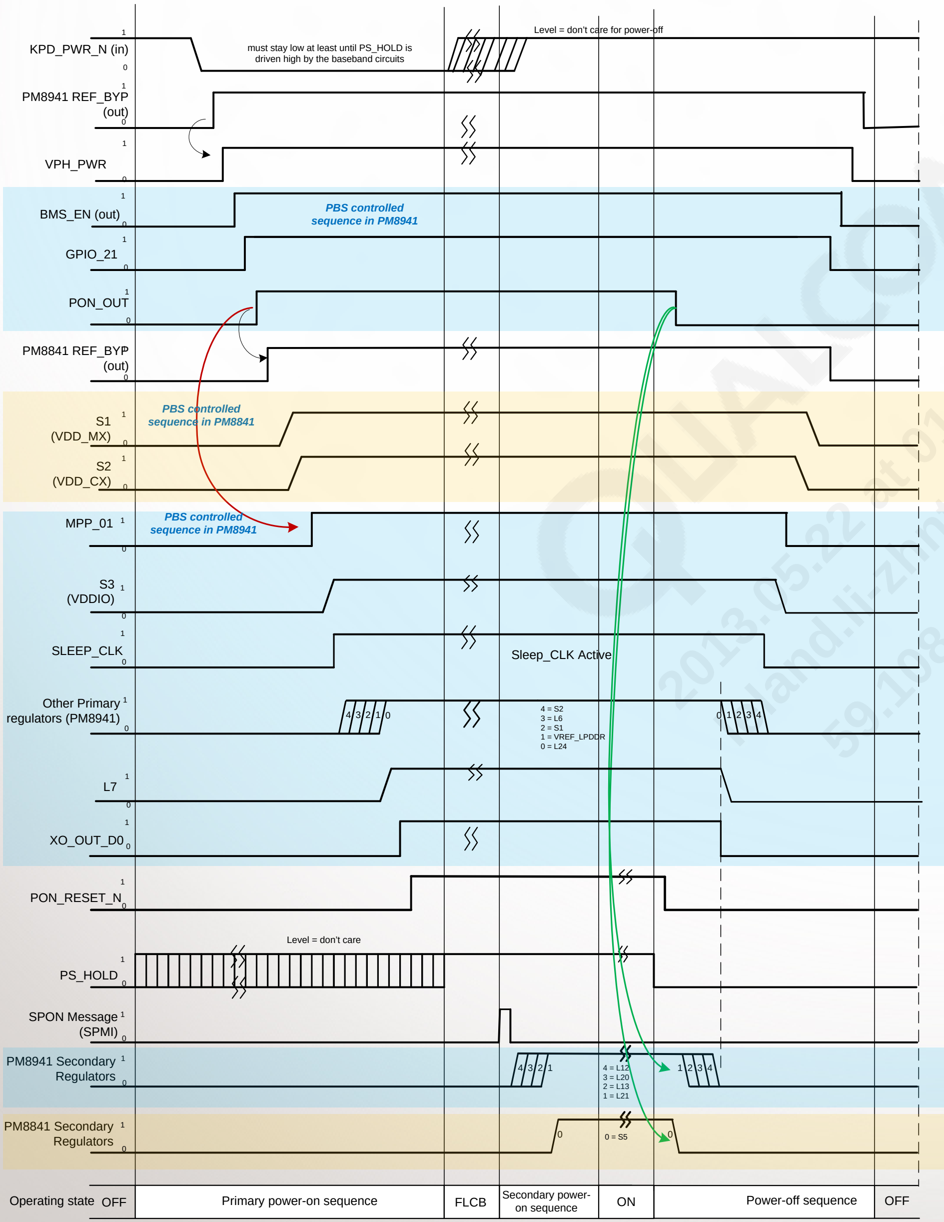
PBS RAM

- For bringup, programmed during SBL.
- Can be reprogrammed at anytime by software.
- PBS programming must be handled by trusted software.
- Some space will be reserved by Qualcomm during development, but these sequences can potentially be moved into OTP prior to CS.
- Note: RAM sequences can prepend some ROM sequence (e.g., during POFF sequence, customer specific POFF sequence is run and then calls the OTP POFF sequence.

Poweron/Poweroff Sequence (1 of 2)

1. PM8941 receives a poweron trigger (e.g. KPD_PWR_N press).
2. PM8941 poweron sequence begins (PBS sequence runs). The following take place:
   - BMS OCV measurement occurs.
   - EXT_REG_EN1 is asserted (VPH_PWR) to enable external supplies.
   - PON_OUT is asserted (1.8 V) to enable PM8841.
   - A timer starts to allow PM8841 to complete his sequence.
3. PM8841 receives poweron trigger (PON_1 and PS_HOLD are asserted).
4. PM8841 poweron sequence begins (PBS sequence runs). The following take place:
   - S1 is turned ON (memory supply).
   - S2 is turned ON (core supply).
5. PM8841 PBS sequence completes. Since PM8841 PS_HOLD is already high, the PM8841 sequence completes. PM8841 is on.
6. PBS sequence on PM8941 continues.
   - The timer on PM8841 expires.
   - The rest of the power sequence (regulators, clocks) are enabled in several steps.
7. The PM8941 PBS sequence completes. PM8941 PON module deasserts PON_RESET_N and sets PS_HOLD timer.
8. Once PON_RESET_N is deasserted, MSM comes out of reset. and PBL will assert PS_HOLD. PM8941 is on.
9. After FLCB, secondary poweron sequence takes place.

Poweron/Poweroff Sequence (2 of 2)



Poweron sequence spans PM8941 and PM8841

Split into two parts (both in OTP)

- Primary poweron sequence
- Secondary poweron sequence

Resets – Nomenclature

Reset triggers

- Internal and external triggers that are routed to the PMIC's poweron module. The poweron module decides what action should be taken, based on these triggers (e.g., over-temperature stage 3, KYPD_PWR_N, RESIN_N, PS_HOLD).

Reset types

- Describes the behavior of the PMIC during a reset or shutdown event (e.g., warm reset or hard reset event).
- The type of reset event is determined by configuration registers in the poweron module and broadcast throughout the PMIC using reset signals.

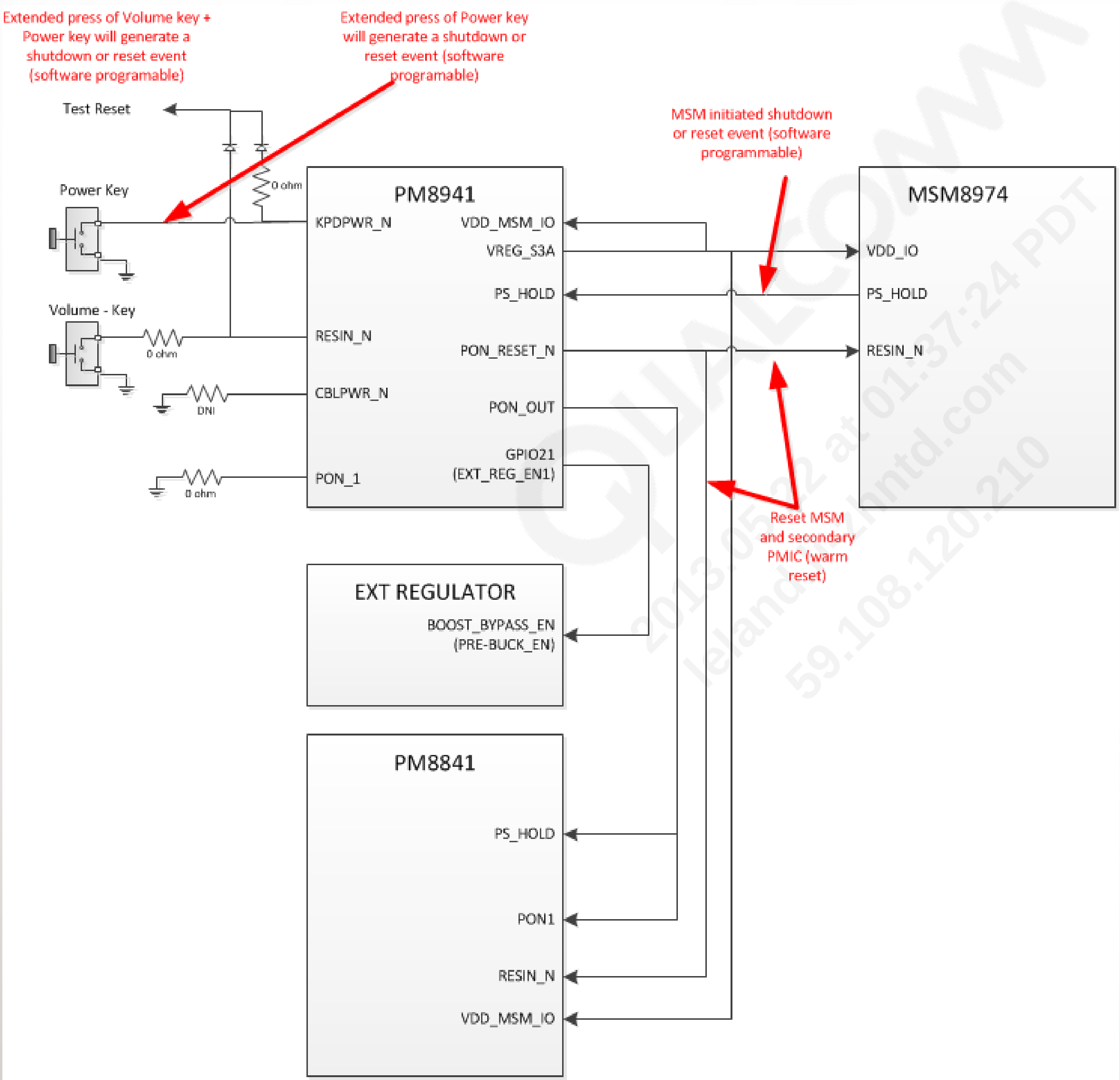
Reset signals

- Signals that are generated in the poweron module and broadcast throughout the PMIC (e.g., xVdd_rb, dVdd_rb, global_soft_rb, shutdown1_rb).
- (Register) reset domains.
- Several reset domains exist to allow some PMIC registers to maintain state throughout certain reset events.

Reset stages

- Three stages of resets: software configurable bark, software configurable reset, failsafe reset

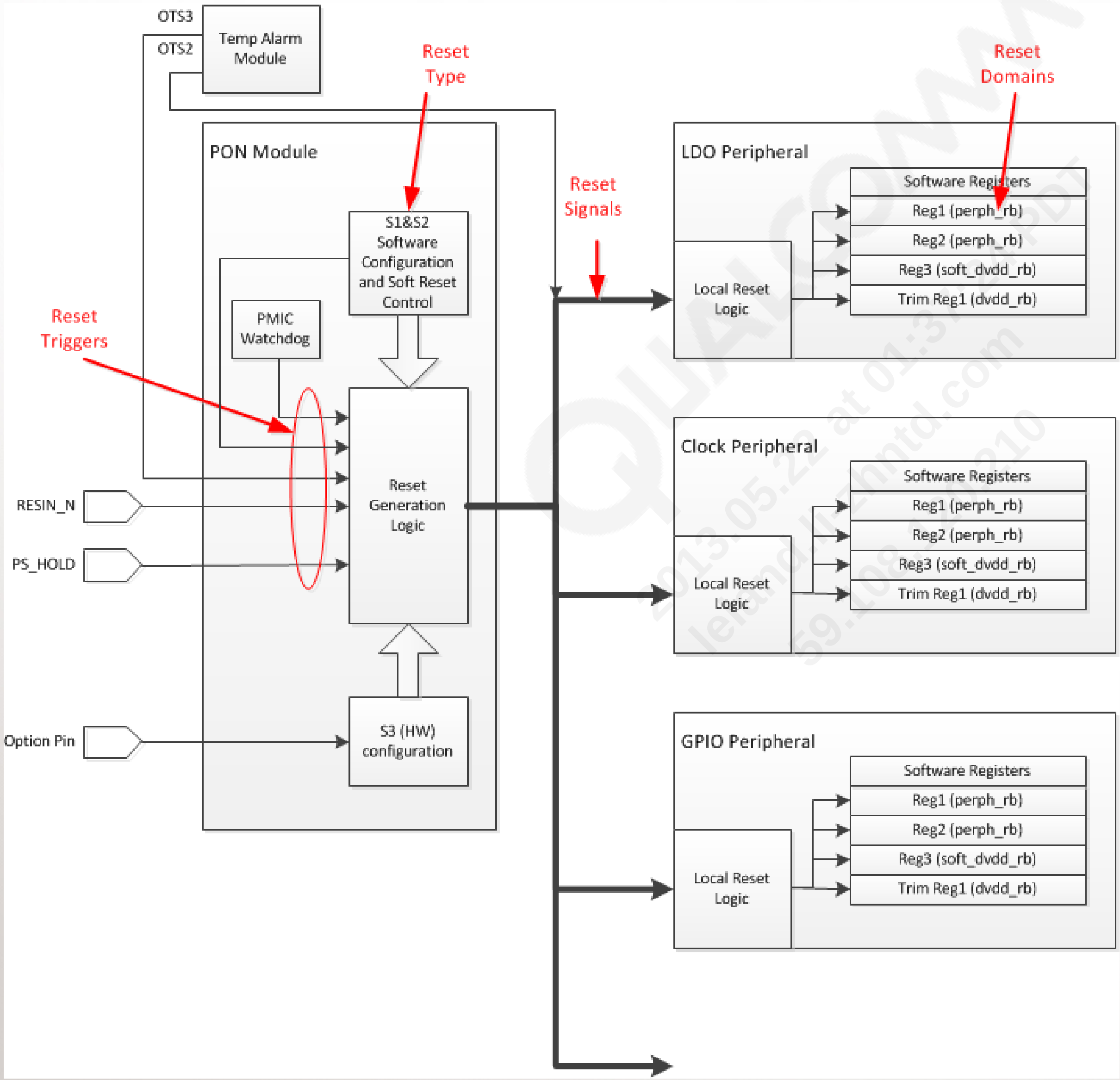
External Reset Block Diagram



Sources of reset (programmable)

- Power button (KYPD_PWR_N)
- Reset button (RESIN_N)
- Power button + reset button
- Apps processor (PS_HOLD)
- Keypad combination (up to three keys)
- Software write
- PMIC watchdog
- PMIC over-temperature sensor
- UVLO (mandatory immediate shutdown)

Peripheral/Module Resets and Internal Reset Block Diagram



PMIC supports multiple triggers for reset

- (i.e., poweron button, overtemp, PS_HOLD (apps processor), and dedicated reset button)
- By default, all peripherals will follow all resets.
- Software can individually configure each peripheral to ignore each reset trigger individually according to mask.
  - Maintain core rails during watchdog reset (for debug)
  - Maintain LCD backlight during reset (maintain LCD content through reset)

3-Stage Reset

Stage 1 (software-configurable bark)

- PMIC generates interrupt, giving the MSM device the opportunity to fix the problem or gracefully reset the system. Example events that can cause a bark:
  - Overtemperature indicates system is getting too hot.
  - PMIC watchdog indicates that it has not kicked.

Stage 2 (software-configurable bite)

- If reset is ignored, PMIC will force a reset event (selectable by software).

Stage 3 (hardware-mandatory bite)

- User can generate a mandatory reset by long key press of RESIN_N, KYPD_PWR_N or RESIN_N and KYPD_PWR_N in combination (selectable via OPT_1 pin setting as shown below).
  - Cannot be disabled by software
  - Resets PMIC back to factory default
  - Only intended as a backup option if stage 1 and stage 2 fail

OPT_1 pin connection

VDD → KYPD_PWR_N
Hi-Z → RESIN_N
GND → RESIN_N + KYPD_PWR_N

Reset Timers

<table>
<tr><th>#</th><th>Reset trigger</th><th>Stage 1 reset (debounce) timer</th><th>Stage 2 reset (delay) timer</th><th>Stage 3 reset timer</th></tr>
<tr><td>1</td><td>KYPD_PWR_N [a]</td><td>0–10.256 sec</td><td>0–2 sec</td><td rowspan="4">0 sec
2–128 sec</td></tr>
<tr><td>2</td><td>RESIN_N [a]</td><td>0–10.256 sec</td><td>0–2 sec</td></tr>
<tr><td>3</td><td>KYPD_PWR_N + RESIN_N [a]</td><td>0–10.256 sec</td><td>0–2 sec</td></tr>
<tr><td>4</td><td>Keypad press [a]</td><td>0–10.256 sec</td><td>0–2 sec</td></tr>
<tr><td>5</td><td>PMIC watchdog [b]</td><td>0–127 sec</td><td>0 -127 sec</td><td>N/A</td></tr>
<tr><td>6</td><td>PS_HOLD</td><td>N/A</td><td>N/A</td><td>N/A</td></tr>
<tr><td>7</td><td>Global reset</td><td>N/A</td><td>N/A</td><td>N/A</td></tr>
<tr><td>8</td><td>Over-temperature reset</td><td>N/A</td><td>N/A</td><td>N/A</td></tr>
</table>

a. Each reset trigger has individual debounce and delay timers. The default value of the debounce and delay timers are 10.256 sec and 2 sec, respectively. The reset triggers share the same stage 3 reset timer.
b. The default value of the debounce and the delay timers for the PMIC watchdog reset is 31 sec and 32 sec.

Under-Voltage Lockout (UVLO)

The UVLO circuit automatically turns off the PM8941 at severely low VDD conditions (2.475 V nom).

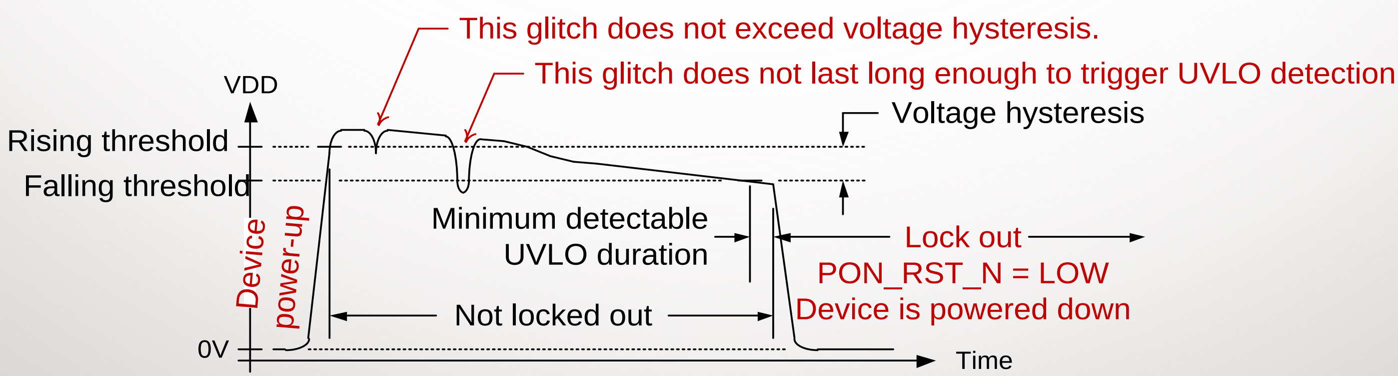
Although UVLO is a hardware feature, it allows for software interaction to realize additional features, such as SMPL recovery, poweron sequence abort, and watchdog timeout soft reset.

Operation

- As the IC powers up, VDD must exceed a rising threshold (2.775 V, default) to initiate the poweron sequence.
- Voltage hysteresis (300 mV, default) and delays prevent minor glitches from being detected as UVLO events.
- If VDD drops below the falling threshold (UVLO rising threshold minus voltage hysteresis) for sufficient duration, a valid UVLO event is detected.
  - PON_RST_N is cleared (LOW) and the device is powered down.

The UVLO rising threshold voltage is programmable.

- 1.675 V to 3.225 V in 50 mV increments (2.775 V, default)
- Other than this programmable threshold, software is not involved in UVLO detection.
- Hysteresis and time delays are not programmable, and UVLO events do not generate interrupts; they are reported to the modem IC via PON_RST_N as part of powerdown.



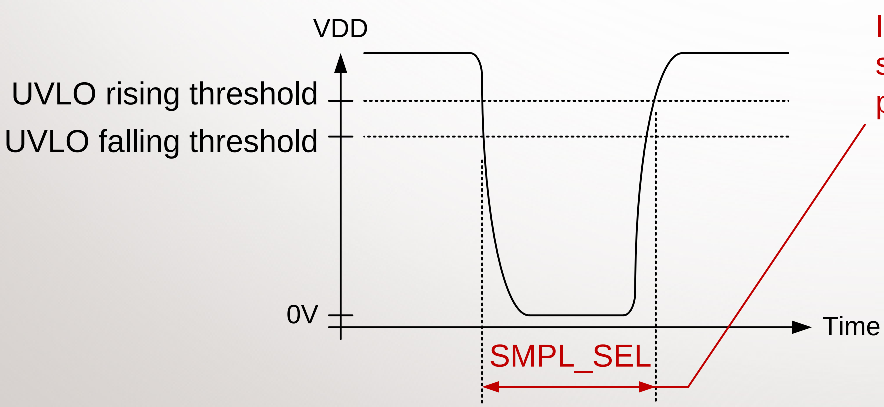
Sudden Momentary Power Loss (SMPL)

When enabled by software → immediate and automatic recovery from a momentary PM8941 power loss.

- If VDD drops out of range (< 2.475 V nominal), then it returns in-range within a programmable interval of between 0.5 and 2.0 seconds, and the recovery is executed.

Some operational details:

- UVLO event clears PON_RST_N; PMIC is powered down.
- Super capacitor or coin cell takes over as SMPL power source.
- If VDD returns to its valid range before timeout, a poweron sequence is initiated without software intervention, and an interrupt is sent to the modem IC indicating: 1) Power was momentarily lost, 2) RTC is corrupted due to insufficient voltage, and 3) Current PMIC actions are not a normal power sequence.
- If SMPL times out without VDD returning to its valid range – the handset must undergo normal poweron sequence whenever the next initializing event occurs.
- SMPL operation must be enabled by software and requires a coin cell or keep-alive capacitor (values listed below) at VCOIN.
- For a normal powerdown, SMPL must be disabled via software before de-asserting PS_HOLD to avoid an inadvertent SMPL override.



If VDD recovers within this programmed interval a poweron sequence is immediately and automatically initiated by power management circuits without software intervention.

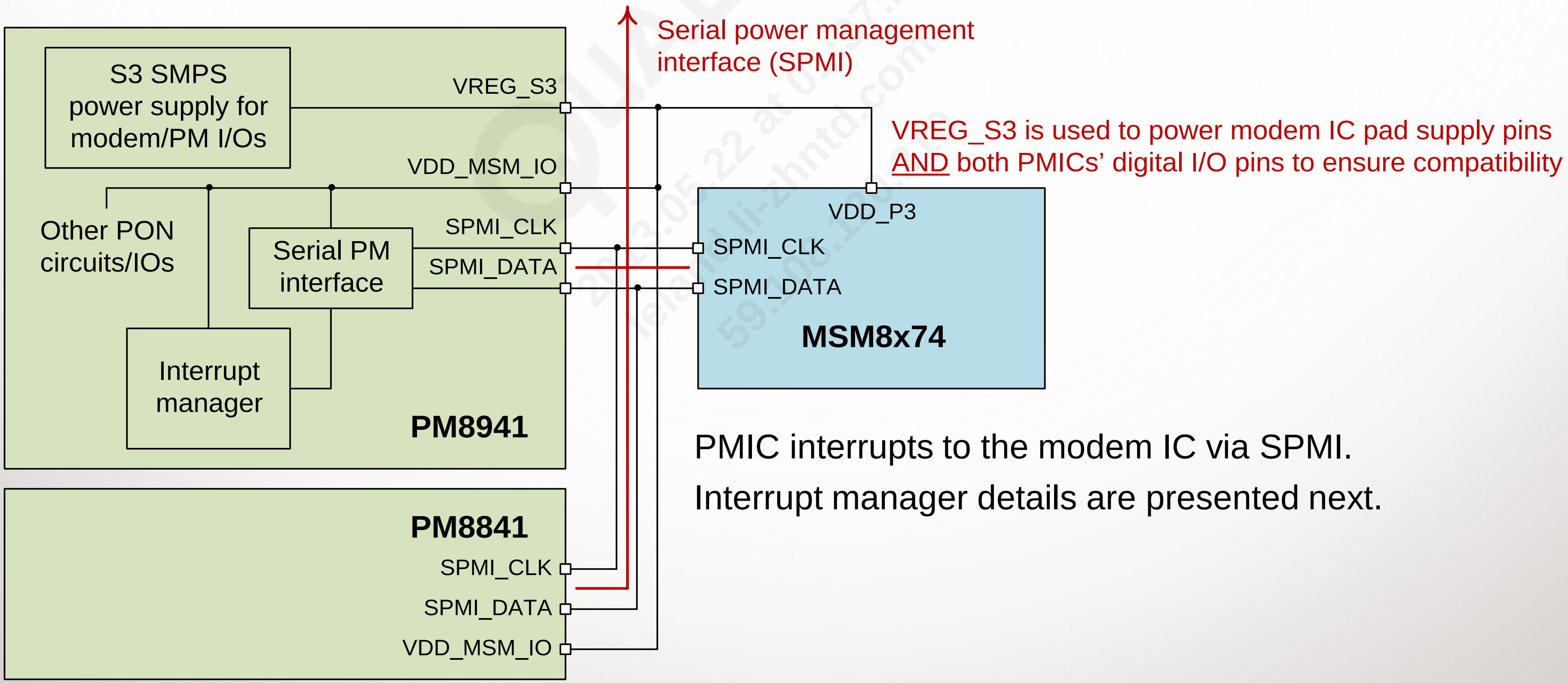
If RTC support is not needed when battery is removed, a backup capacitor can be used on VCOIN pin. A ceramic capacitor with an effective capacitance of 10 µF can support SMPL for up to 2 seconds.

SPMI and Interrupt Manager

SPMI – primary IC-level interface for efficient initialization, status, and control communications.

Application programming interface (API) is used to program PMICs, indirectly exercising SPMI.

The coin cell backs up several SPMI registers; at powerup, SPMI defaults are restored, except bits backed up by the coin cell – they are only restored to default values if the coin cell expired.



PMIC interrupts to the modem IC via SPMI.

Interrupt manager details are presented next.

Interrupt Manager Details

An interrupt manager receives internal reports on numerous functions and conveys status signals to the modem device, supporting its interrupt processing.

Each interrupt event has the following associated SPMI bits:

- Interrupt mask (read/write) – allows modem IC to ignore event; latched status hidden and interrupt is not asserted.
- Interrupt real-time status (read only) – follows realtime interrupt status (active or inactive) for standard configuration interrupts; special configuration interrupts are highlighted in red and defined further below.
- Interrupt latched status (read only) – set when event is active and interrupt mask bit is cleared; stays set until clear bit is set.
- Interrupt clear (read/write) – clears latched status automatically after latched status is read.

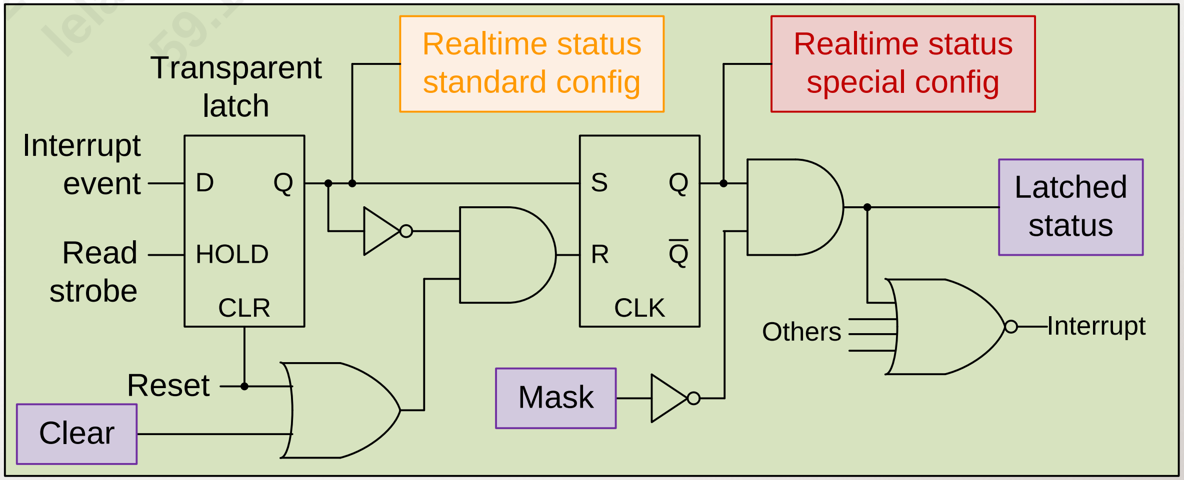
Unmasked interrupts notify the modem device that at least one interrupt has occurred.

Upon powerup, software should check the RTCRST interrupt – if set, the coin cell voltage is too low, and the RTC and SRAM contents and the SMPL and WDOG interrupts are unreliable.

Most interrupts are standard (orange), but four are special (red) interrupts:

- Real-time clock reset (RTCRST)
- Sudden momentary power loss (SMPL)
- MDM watchdog timeout (WDOG)
- Die over-temperature (OVERTEMP)

These are not realtime readable – they occur only when the PMIC is reset or when they cause a PMIC reset. They are latched and backed up via coin cell. Upon a PMIC restart, latched interrupts inform the modem device why they were triggered.

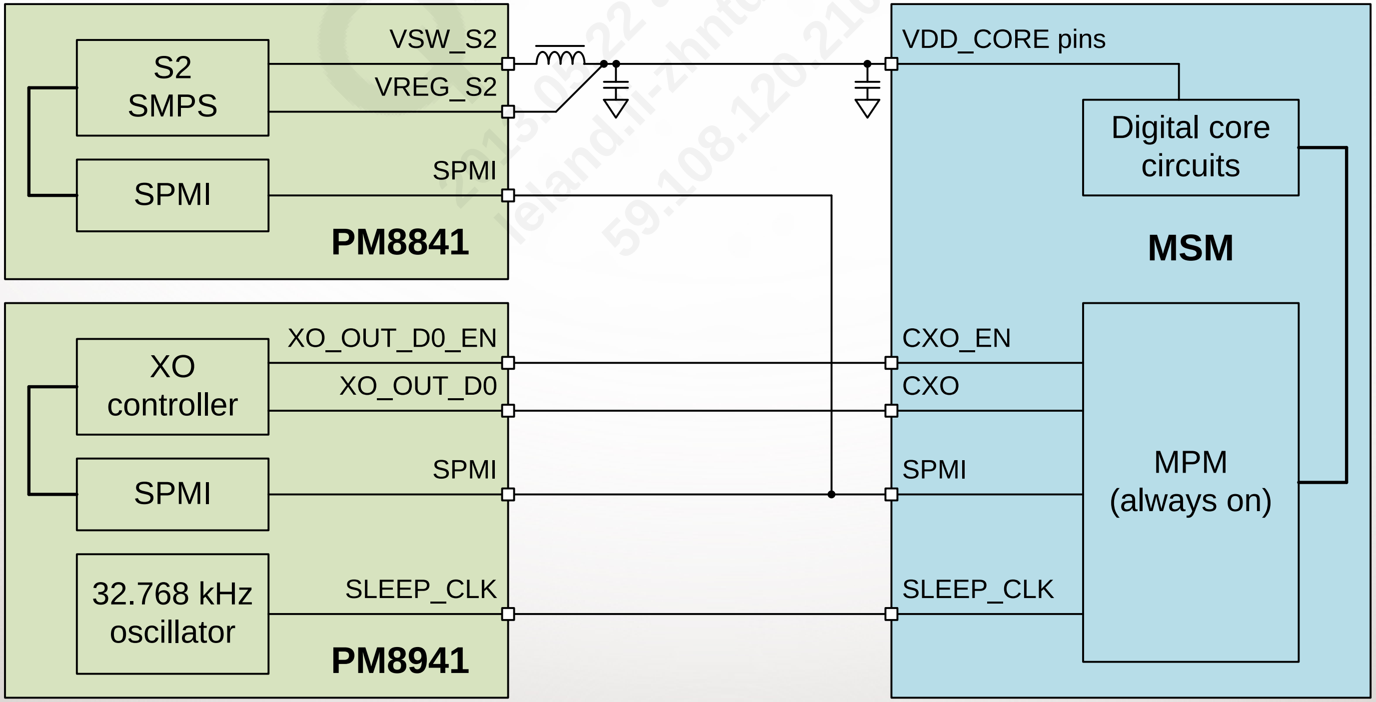


Modem Power Management Support (1 of 2)

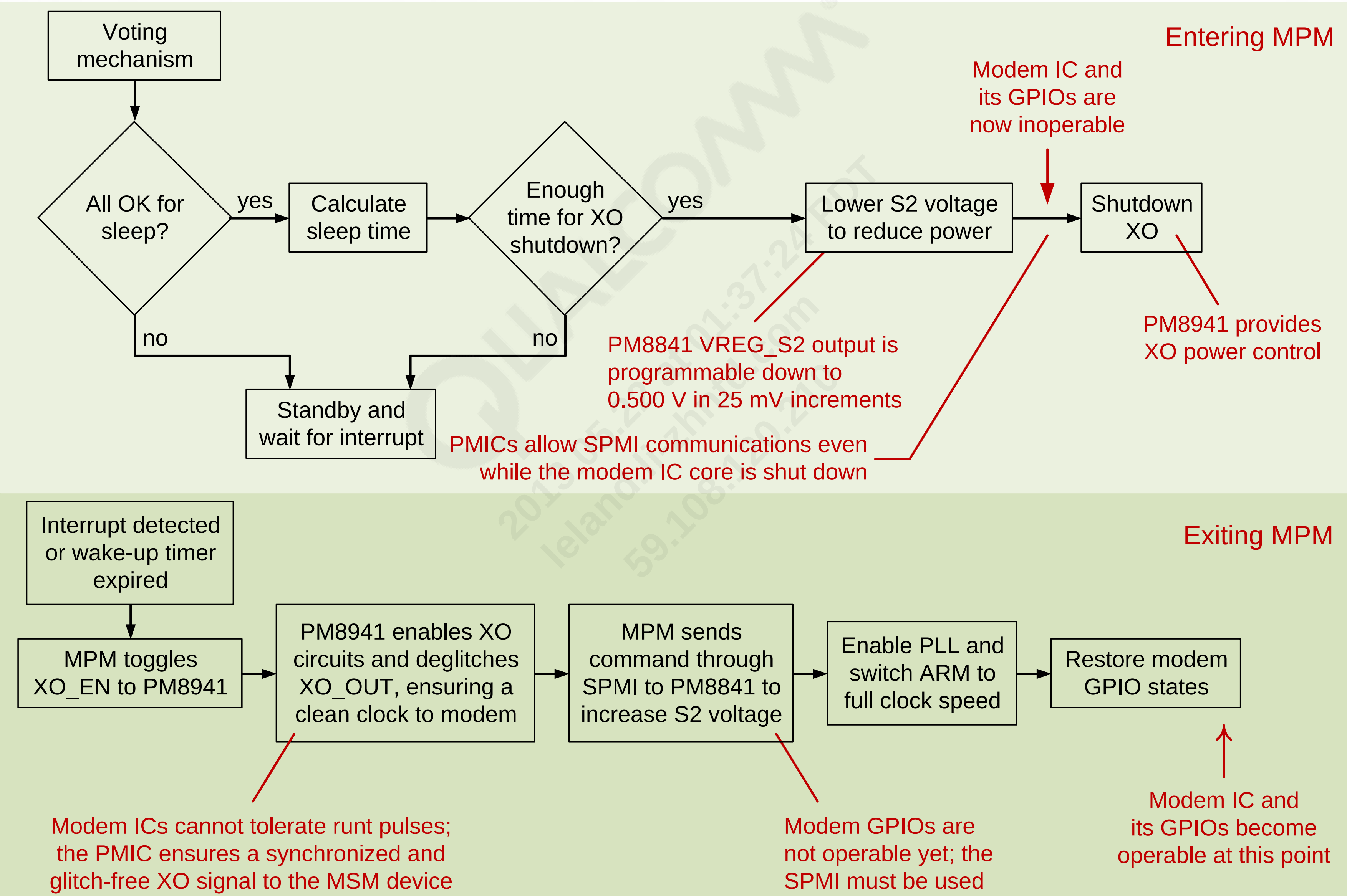
SPMI is able to communicate with the modem IC, even while its core circuits are powered down. PMIC features necessary to support MPM:

- Key regulator outputs programmable to 750 mV.
- SPMI continues modem communications, even while the modem IC core is powered down.
- The PMIC controls the XO power supply.
- The PMIC ensures a synchronized and glitch-free XO signal for the modem device.

Connections required for MPM support are illustrated below.



Modem Power Management Support (2 of 2)



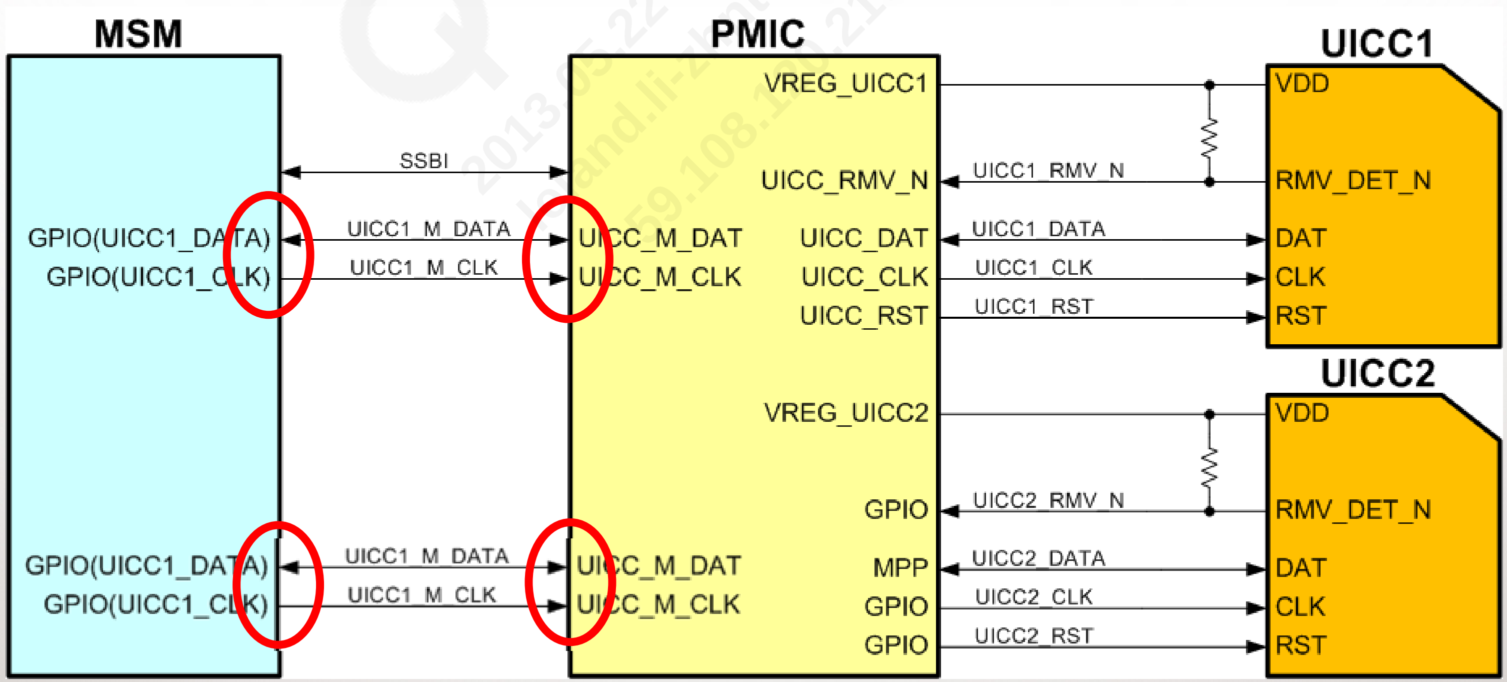
Battery UICC Alarm (BUA) Interface – Introduction

MSM8960 required PM8921 to level shift every UIM interface

- This costs an additional eight pins in the system (for two UIM interfaces).
- Reducing the number of pins on the PMIC allows the PMIC to fit into smaller WLP packages.

To support UIM card removal detection/battery removal detection, a new, low latency, bidirectional interface was created.

- Battery UICC alarm (BUA) interface



BUA Overview

ISO-7816-3 specifies that a smartcard (UICC/UIM) shall be powered down in a controlled and predefined manner.

Battery UICC alarm (BUA) is a bidirectional interface between the PMIC and the MSM that allows for a controlled power down of UICC when either the battery or the UICC is removed.

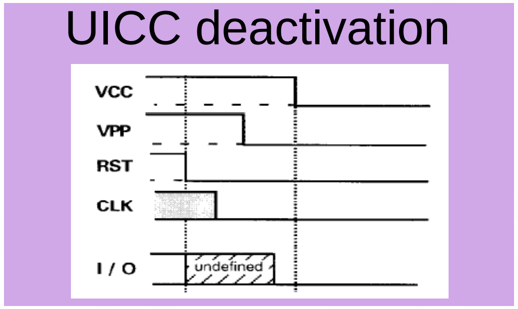
System interconnect

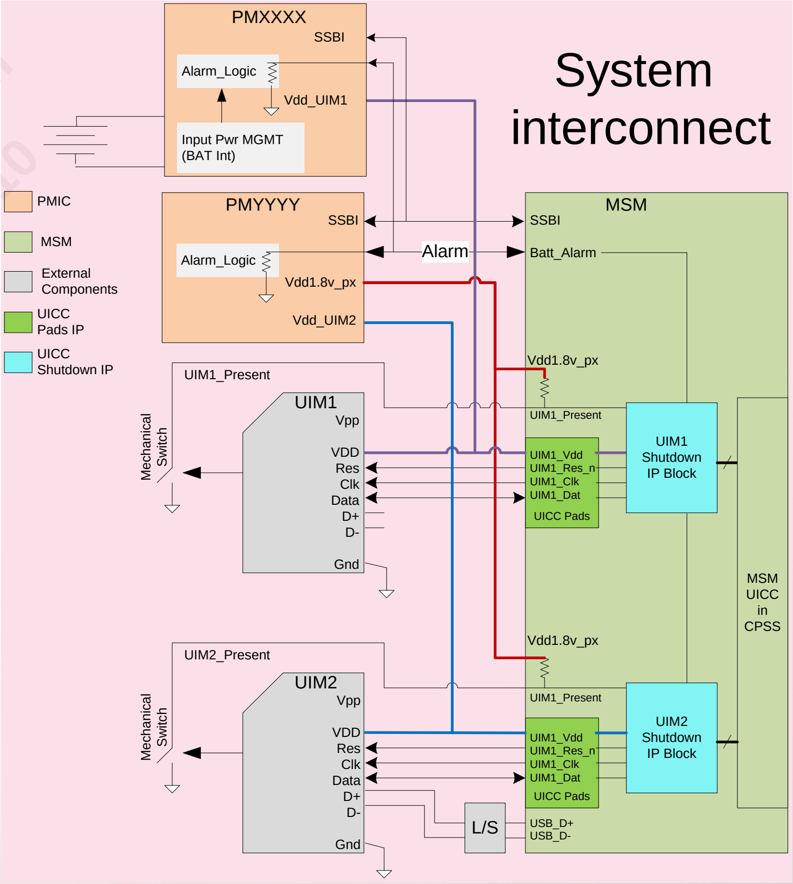
- UICC DATA/CLK/RST pins are connected directly to the MSM
- UICC supply is supplied from the PMIC

The PMIC alerts the MSM device over the bidirectional interface when a battery is removed so that the UICC can be deactivated while the system is still powered by capacitors.

The MSM device alerts the PMIC over the bidirectional interface when a UICC removal is initiated so that the UICC can be deactivated before it is completely removed.

Alarm and deactivation are based in hardware; no software intervention is required.





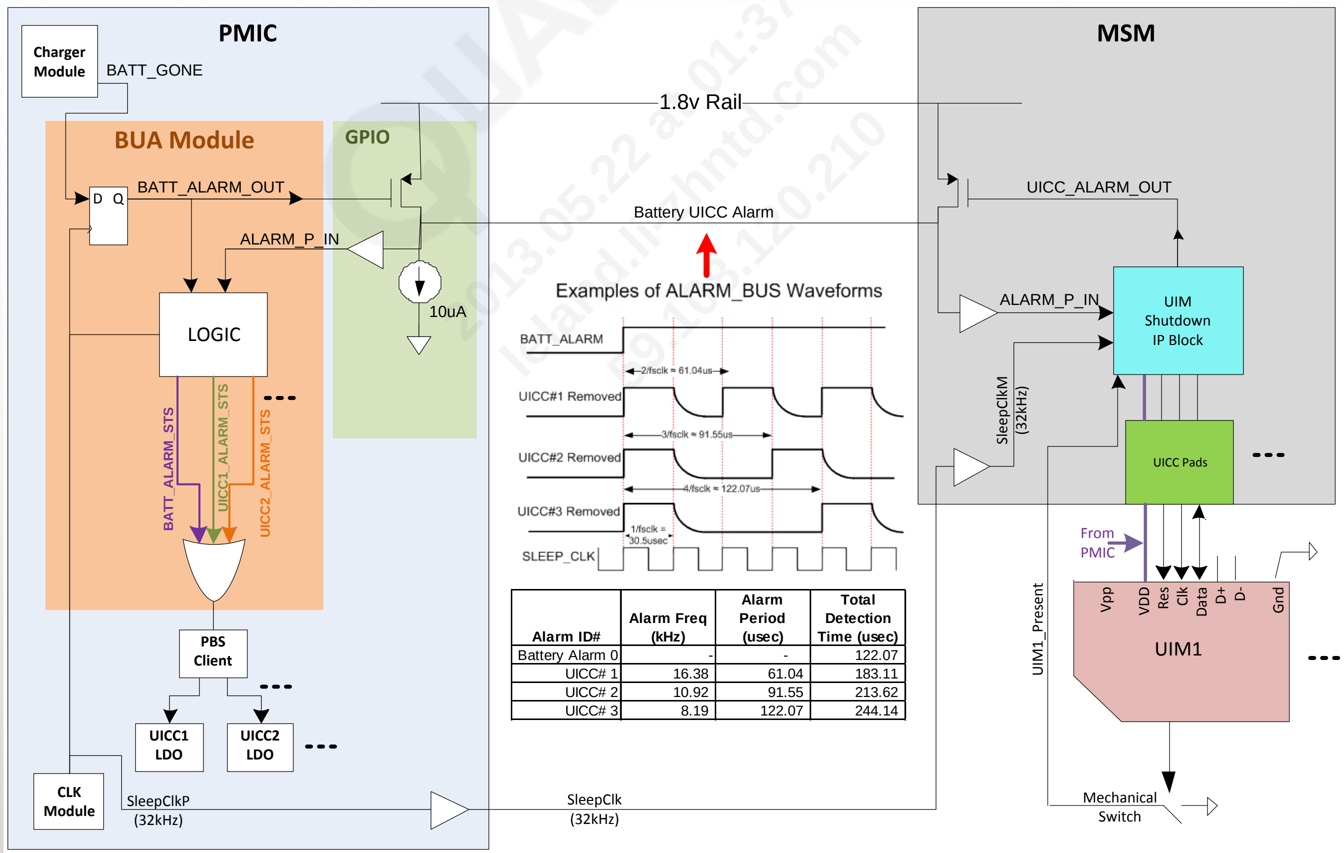
BUA Operation

Battery removal: PMIC detects battery removal and triggers the alarm by pulling it high. PMIC waits for a pre-determined time while MSM shuts down DATA/CLK/RST and then powers down all UICC LDOs.

- Battery removal to deactivation complete: ~884 µs (nominal)

UICCx removal: MSM detects UICCx removal via a mechanical switch. MSM shuts down DATA/CLK/RST and then triggers the alarm by pulsing a fSCLK/(x+1) signal. PMIC decodes the alarm and powers down UICCx LDO.

- UICC removal to deactivation complete: ~1565 µs (nominal)

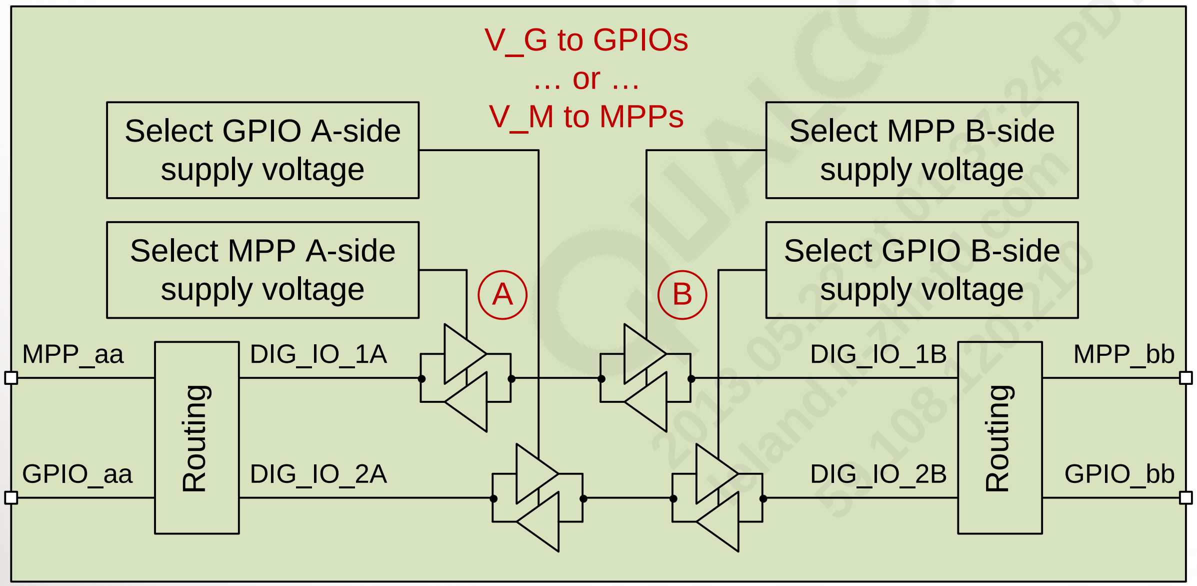


Alarm ID#	Alarm Freq (kHz)	Alarm Period (usec)	Total Detection Time (usec)
Battery Alarm 0	-	-	122.07
UICC# 1	16.38	61.04	183.11
UICC# 2	10.92	91.55	213.62
UICC# 3	8.19	122.07	244.14

Other IC-level Interface Uses for MPPs or GPIOs (1 of 2)

Level translators

Since the two sides (A and B) can run off different voltages, a level-translation is achieved.



V_M options for MPP_01 to _04
VDD_L8_16_18_19 = VPH_PWR
VREG_L1 = 1.225 V
VDD_L2_LVS1_2_3 = 1.8 V (VREG_S3)
VREG_L6 = 1.8 V

V_M options for MPP_05 to _08
VDD_GPLED = VPH_PWR
VREG_L1 = 1.225 V
VDD_L2_LVS1_2_3 = 1.8 V (VREG_S3)
VREG_L6 = 1.8 V

V_G options for GPIO_1 to _14
VDD_L8_16_18_19 = VPH_PWR
VREG_L1 = 1.225 V
VDD_L2_LVS1_2_3 = 1.8 V (VREG_S3)
VREG_L6 = 1.8 V

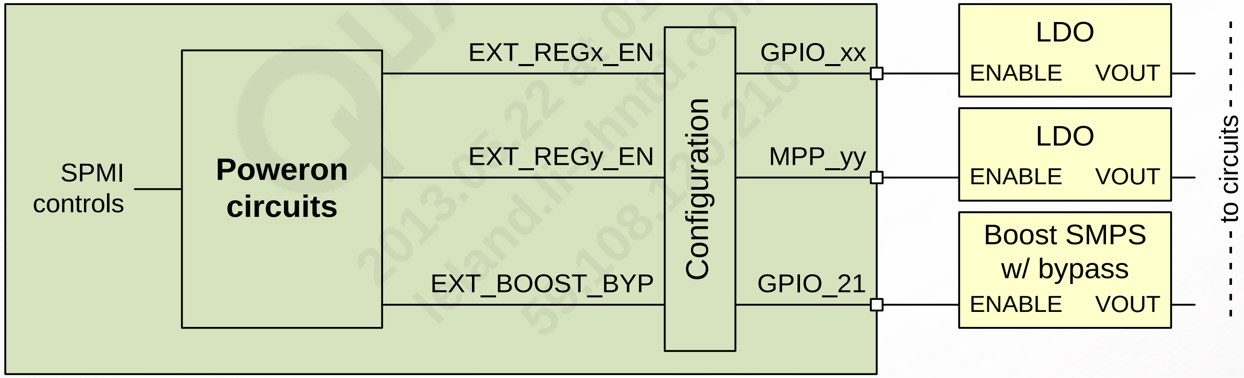
V_G options for GPIO_15 to _18
VDD_L2_LVS1_2_3 = 1.8 V (VREG_S3)
VREG_L6 = 1.8 V

V_G options for GPIO_19 to _36
VDD_RGB = VPH_PWR
VDD_TORCH = TBD
VDD_MSM_IO = 1.8 V (VREG_S3)
VREG_L4 = 1.8 V
VREG_L6 = 1.8 V

Other IC-level Interface Uses for MPPs or GPIOs (2 of 2)

External LDO or SMPS controls

GPIO and MPP outputs can control external LDOs, SMPS circuits, or power gating



Some GPIOs and MPPs can be included in the default-on poweron sequence, as discussed earlier.

PMIC Configurable I/Os

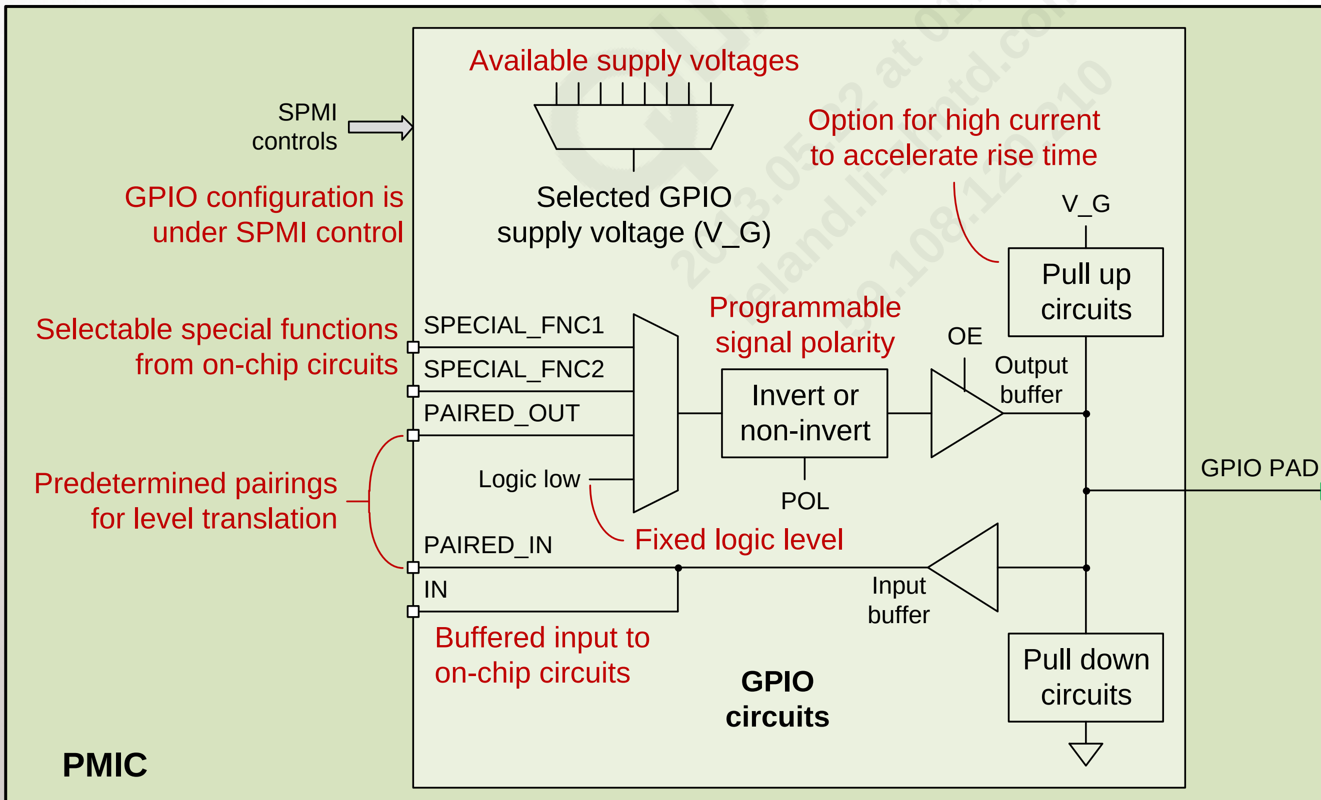
PMIC GPIO Pins

36 GPIOs are available, all on the PM8941 (none on PM8841)

Some likely GPIO applications, which are discussed elsewhere: clock outputs; external current driver control; external LDO, SMPS, or power gate controls; status bit; XO controller input; and level translator.

GPIO pairs

- Each GPIO pin is assigned as a member of a pair.
- Each pair is a combination of sequential odd and even GPIO pins (GPIO_1 is paired with GPIO_2, etc.).
- Each member can be assigned a different supply, so each pair can be used as a digital level translator.



Note:
All GPIOs hardware default to digital input with 10 μA pull-down. GPIO_21 is driven high at VPH_PWR level by PBS during PMIC poweron.

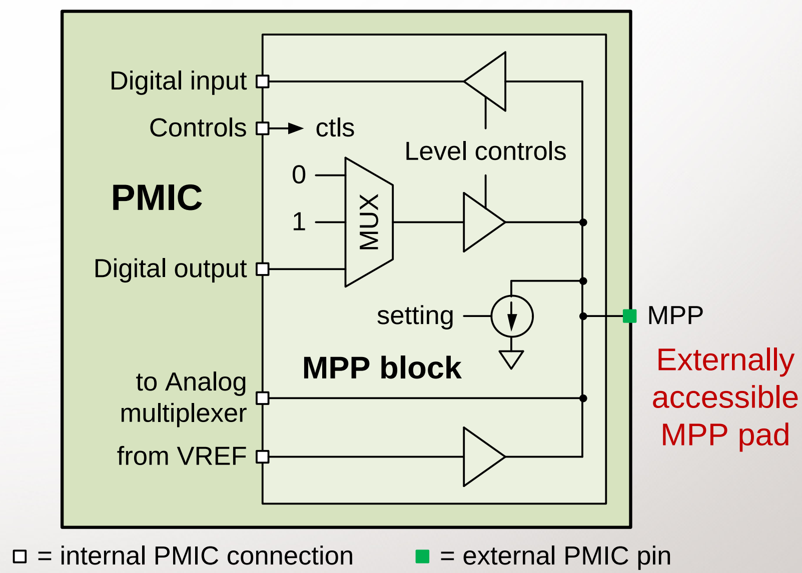
PMIC Multipurpose Pins

12 MPPs are available: Eight on the PM8941 and four on the PM8841. All can be programmed to any of the following configurations.

- Digital input – Digital inputs applied to the pin can be read via software, can trigger an interrupt, or can be routed to another MPP (making this pin the input side of a level translator or current sink controller). The logic level is programmable, providing compliance between I/Os running off different power supplies.
- Digital output – The output signal can be set via software to logic LOW or HIGH, can come from this pin's complementary MPP (making this pin the output side of a level translator), or can be tri-stated for use as a switch. The logic level is programmable, providing compliance between I/Os running off different supplies.
- Bidirectional I/O – The two MPPs making up a complementary pair can be jointly configured as a bidirectional, level-translating pair.
- Analog input – Inputs are routed to the analog multiplexer switch network; if selected, that analog voltage is routed to the HK/XO ADC for digitization.
- Analog output – Buffered version of on-chip voltage reference (VREF).
- Programmable current sink – for driving LEDs.

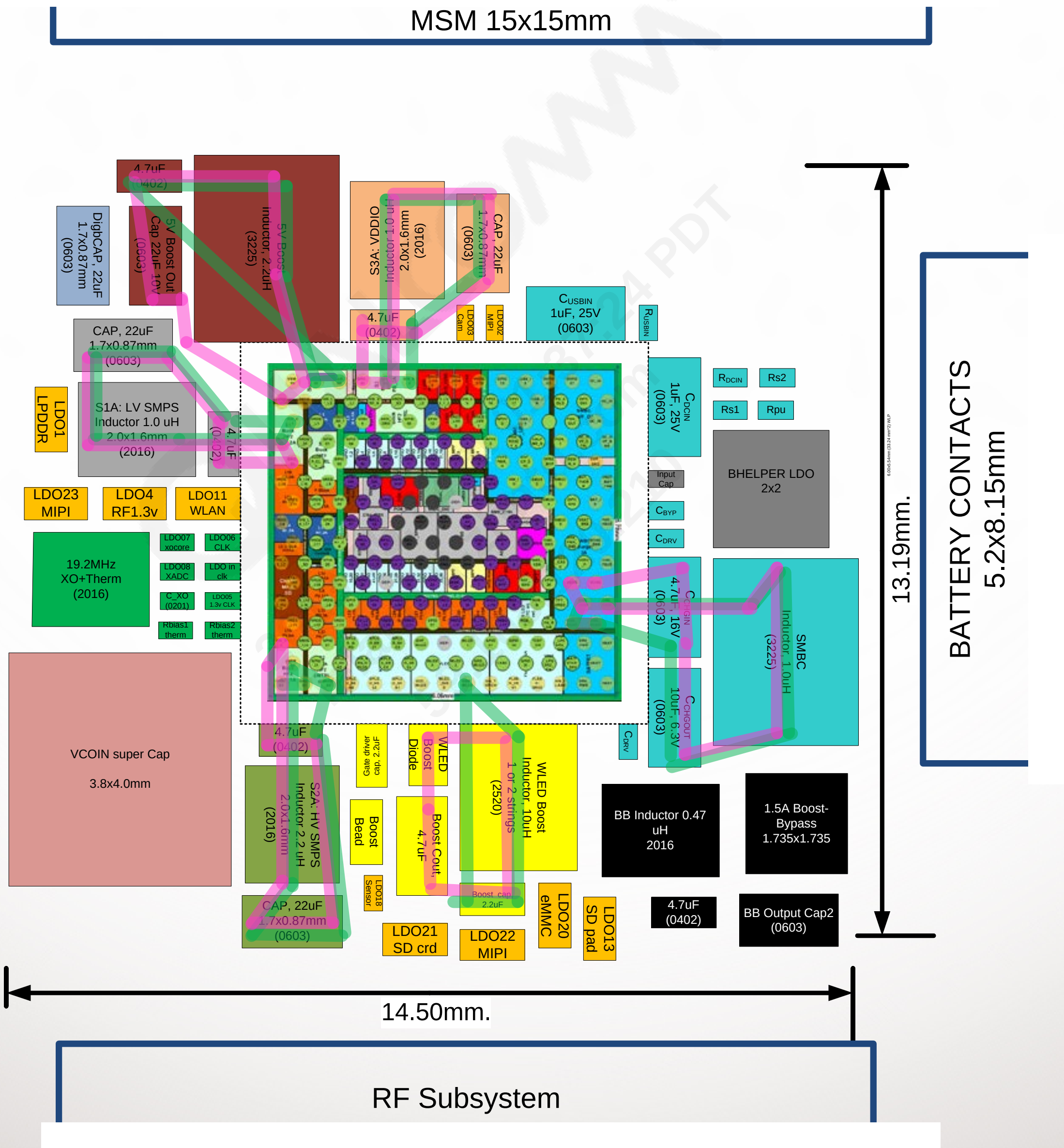
Notes:

1. PM8841 MPPs can be configured as analog inputs but with no AMUX present in the PMIC, the voltage cannot be read
2. Only odd PM8941 MPPs (MPP_01, MPP_03, MPP_05, MPP_07) can be configured as analog outputs.
3. Only even MPPs (MPP_02, MPP_04, MPP_06, MPP_08) have current sink capability.

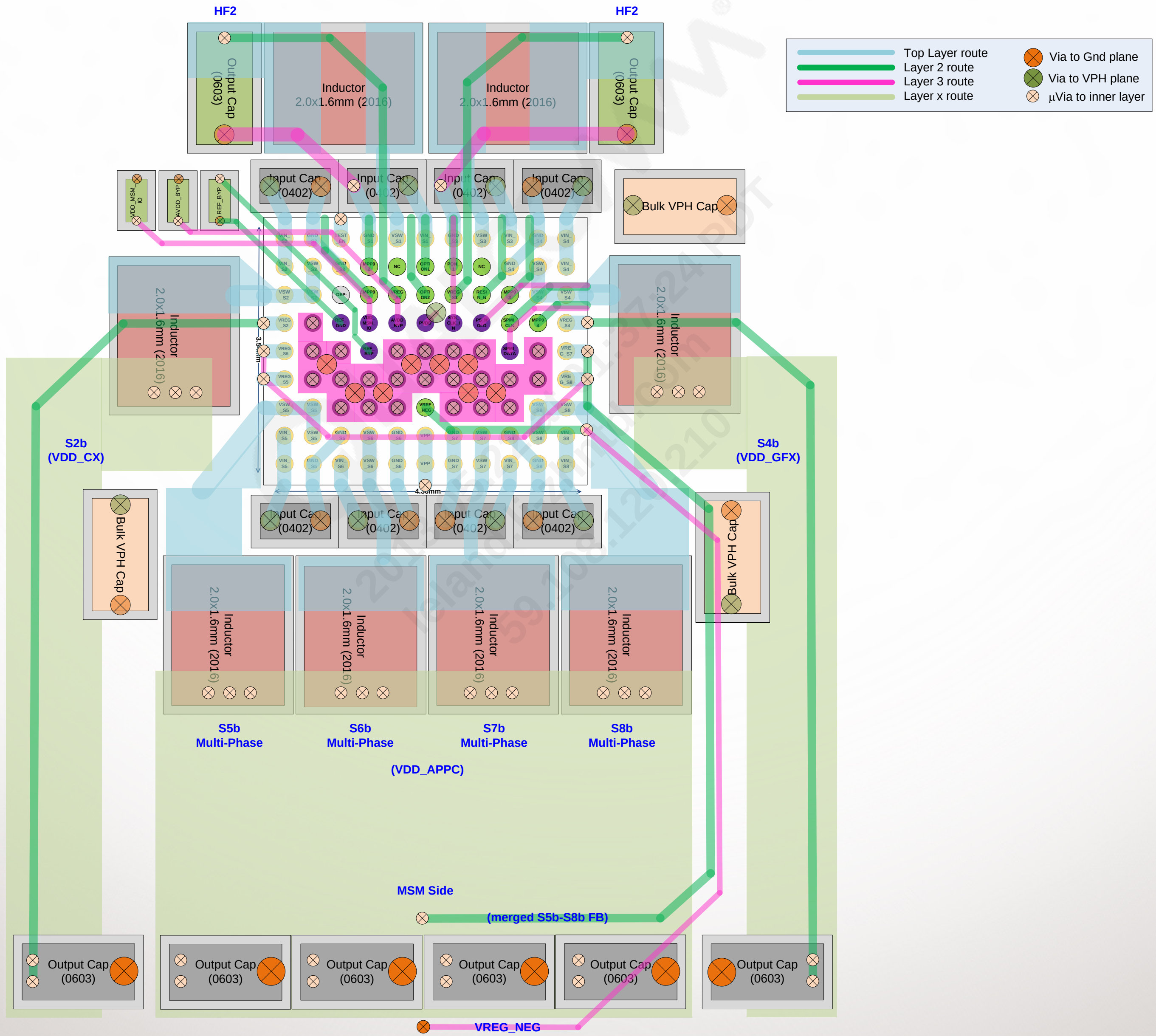


PMIC Top-level Design Topics

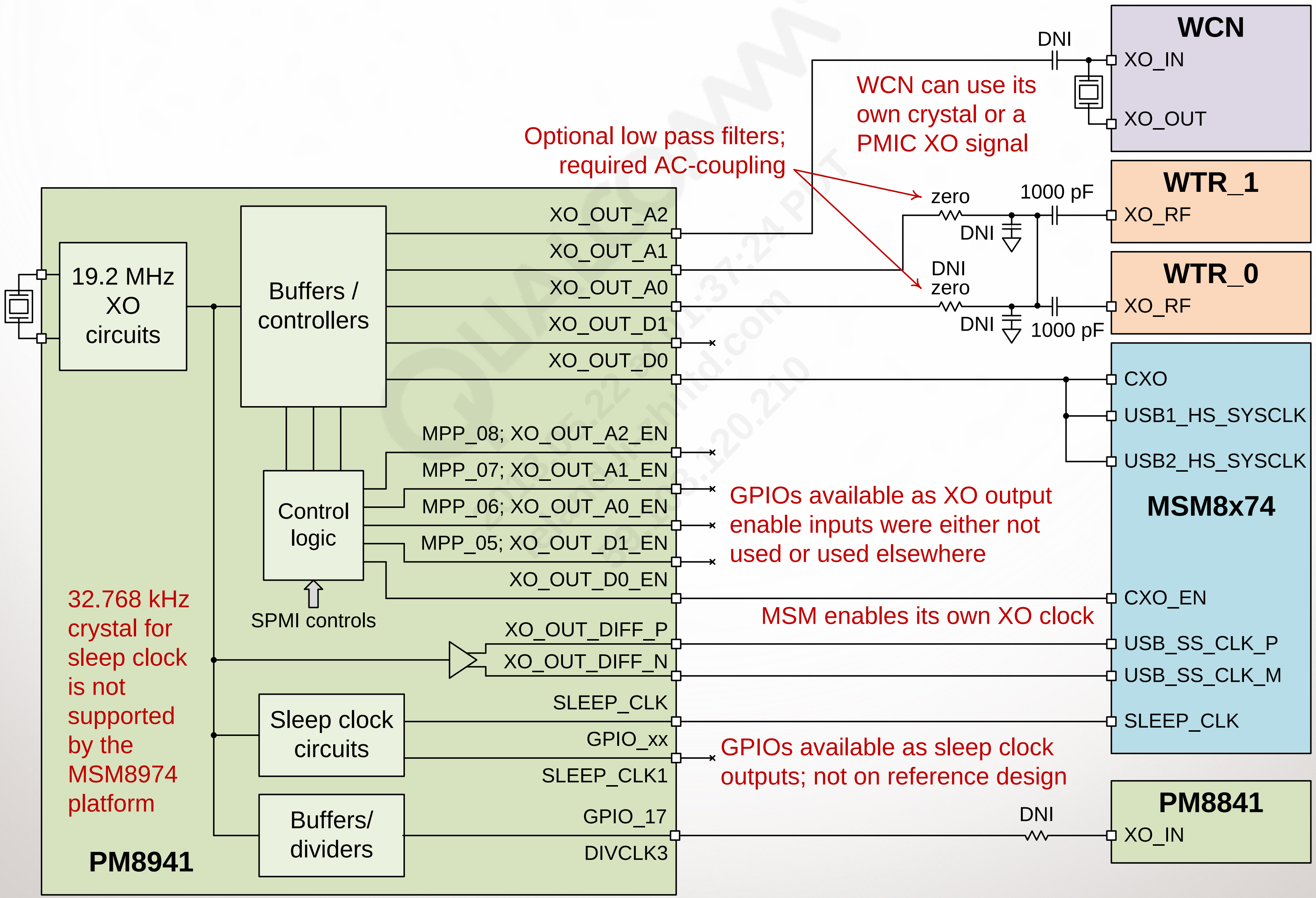
Example PM8941 Top-level Parts Placement



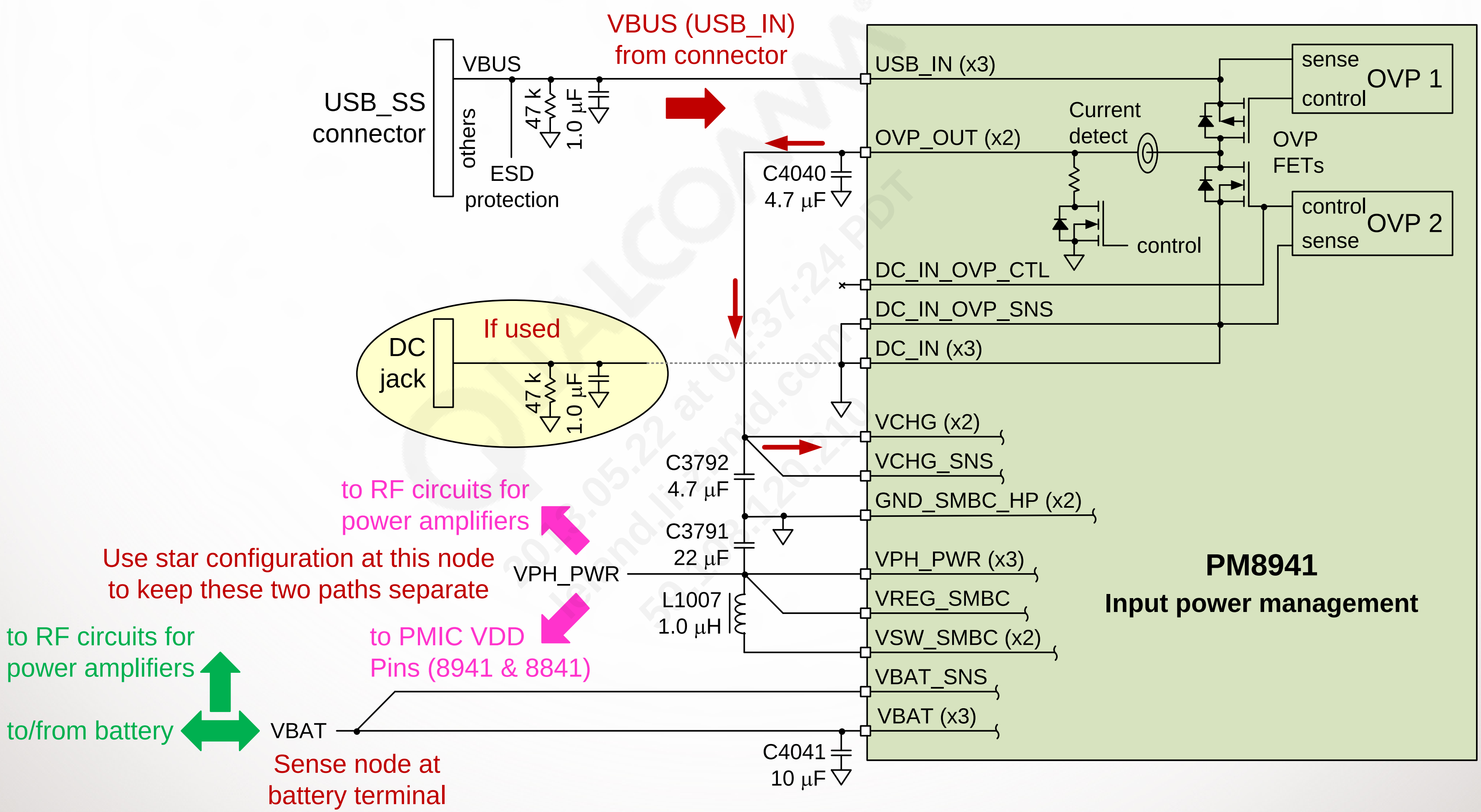
Example PM8841 Top-level Parts Placement



Example XO and Sleep Clock Distributions



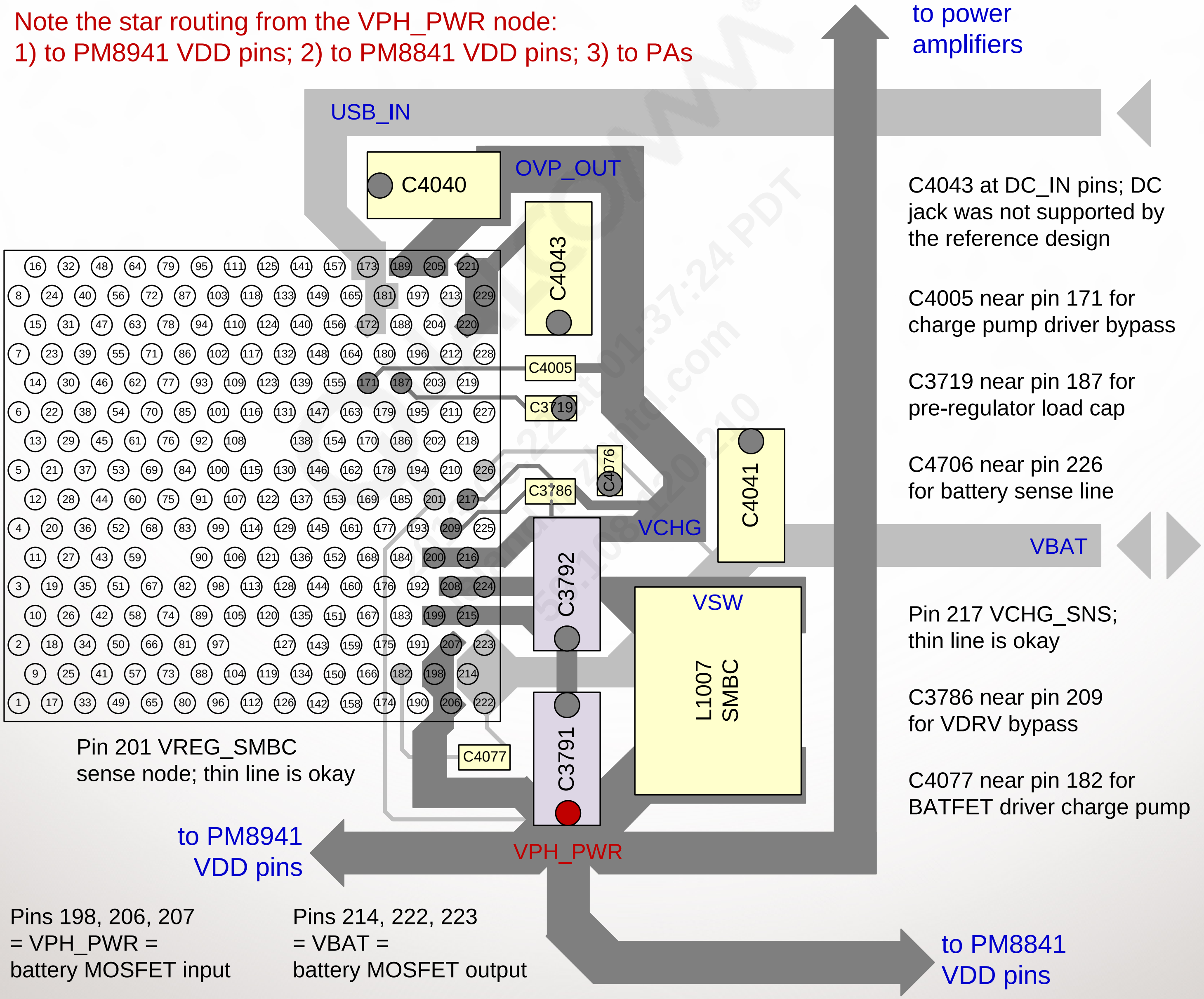
Example PM8941 Input DC Power – Schematic



Note: Refer to latest version of the *MSM8974 Preliminary Baseband Reference Schematic* (80-NA437-41) for the input DC power schematic.

PMIC High-level Input DC Power – Layout Guidelines

Note the star routing from the VPH_PWR node:
1) to PM8941 VDD pins; 2) to PM8841 VDD pins; 3) to PAs



C4043 at DC_IN pins; DC jack was not supported by the reference design

C4005 near pin 171 for charge pump driver bypass

C3719 near pin 187 for pre-regulator load cap

C4706 near pin 226 for battery sense line

Pin 217 VCHG_SNS; thin line is okay

C3786 near pin 209 for VDRV bypass

C4077 near pin 182 for BATFET driver charge pump

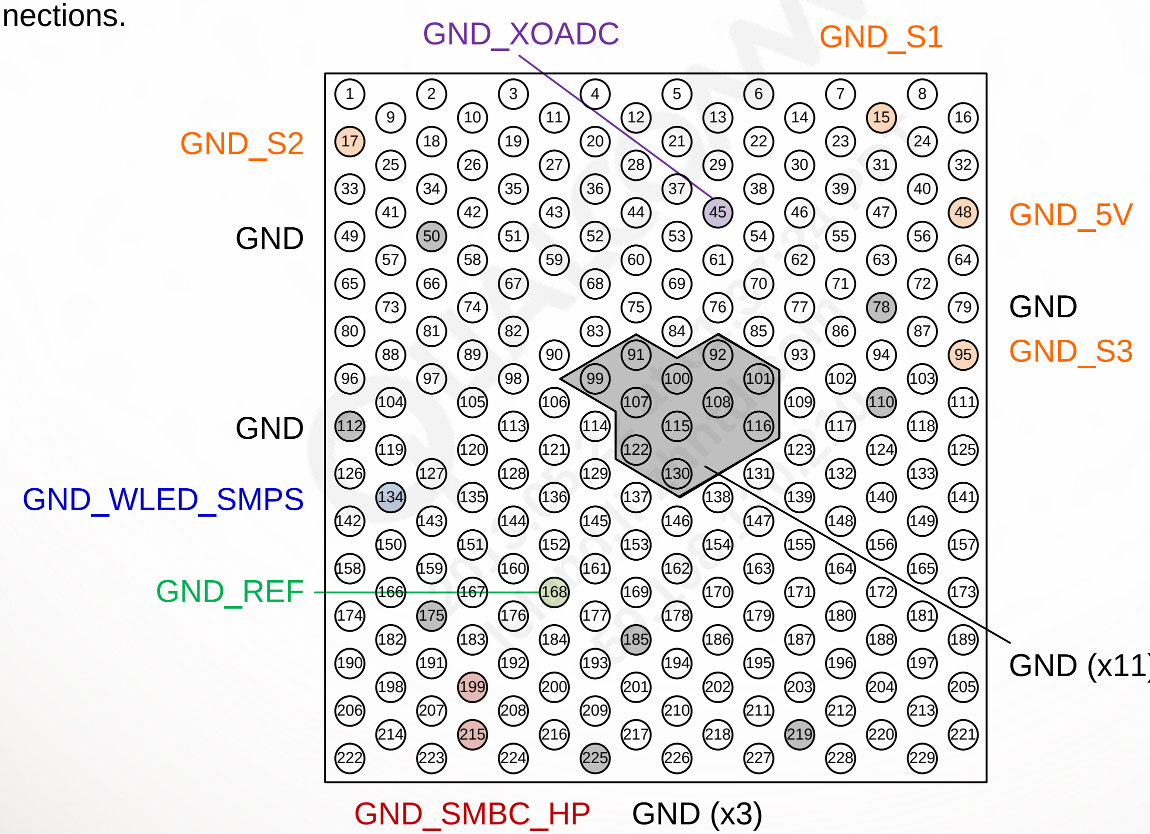
Pin 201 VREG_SMBC sense node; thin line is okay

Pins 198, 206, 207 = VPH_PWR = battery MOSFET input

Pins 214, 222, 223 = VBAT = battery MOSFET output

PM8941 Ground Connections

Common ground pins near the IC center improve electrical ground, mechanical strength, and thermal continuity. These pins are tied together internally and should be connected to PCB ground. Several other pins provide special-purpose ground connections.

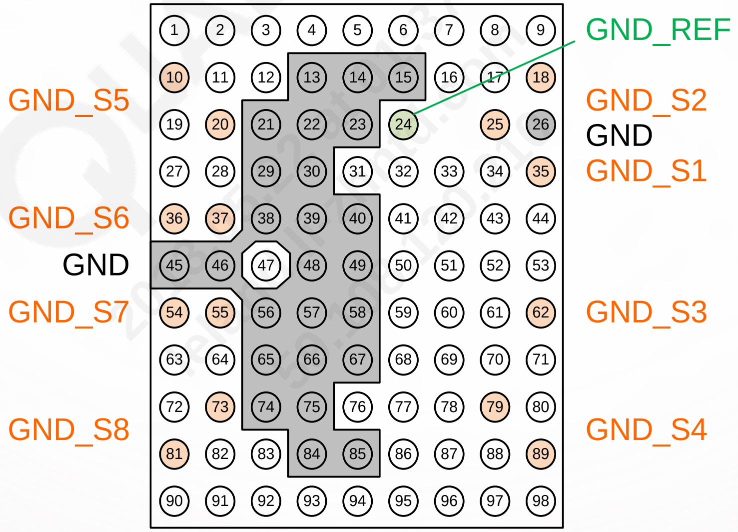


Common ground pins must be soldered to PCB pads located directly below the device, with many ground vias conducting PMIC heat directly to several inner layers. The inner layers should provide very large areas of ground fill and additional vias connected to outer layer ground fill areas. All these large ground surfaces minimize thermal resistance to the handset's ambient environment.

All others – shown in different colors – are special-purpose grounds that were discussed in the context of their assigned functionality within other sections of this document.

PM8841 Ground Connections

Notes from the PM8941 ground connection page apply for the PM8841 as well.



Power Management Troubleshooting Techniques

The recommended troubleshooting sequence for an initial dual-PMIC powerup is as follows:

1. Check the PM8941 charger input power supply voltage (USB_IN, OVP_OUT, DC_IN, and/or VCHG).
2. Check the PM8941 charger output voltage (VPH_PWR).
3. Check the other input power pins (VDD_xxx) at both PMICs.
4. Verify the logic levels at the external control pins:
   - PM8941 CBL_PWR_N
   - PM8941 KYPD_PWR_N
   - PM8941 OPT_[4:1] and PM8841 OPT_[2:1]
   - RESIN_N at both PMICs
4. Check the internal reference voltages by probing the REF_BYP pin on both PMICs.
5. Check the regulated voltages that default to their on state. Note that the sequence depends upon the hardwired connections at PM8941 OPT_[4:1] and PM8841 OPT_[2:1].
6. Each of these should settle to within 5 to 10% of their target voltage before the PMIC continues its poweron sequence by initiating the next regulator. The devices shut down if any of these default regulators do not turn on and settle properly.
7. If a device shuts down due to a failed regulator output, the start signal will have to be removed and reapplied to attempt another powerup.
8. Monitor PM8941 PON_RST_N; verify that it goes to logic high after all the default regulators power up correctly.
9. Monitor PM8941 PS_HOLD; verify that it is at logic high. It can transition between logic states throughout the poweron sequence but must be stable at logic high within hundreds of milliseconds after the PON_RST_N signal went high. Confirm that this signal is applied to the PM8841 PS_HOLD and PON_1 pins.

   If any of the first nine steps are not completed successfully, one of the installed PMICs has failed. If step 10 fails, there may be a problem with the modem device, one of the PMICs, or their interconnections.

Questions?

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