MSM8274/MSM8674/ MSM8974 Chipset Design Guidelines

System Topics

Qualcomm Technologies, Inc.

80-NA437-5C Rev. C

Qualcomm Technologies, Inc.
5775 Morehouse Drive
San Diego, CA 92121
U.S.A.

Revision History

Revision	Date	Description
A	July 2012	Initial release
B	September 28, 2012	• Removed explanation about design guidelines vs. training slides/documentation introduction (Slides 5-10) • Removed slides describing the pins. • Updated PDN specifications (Slide 6) • Updated subsystem name and added two acronyms (Slide 17) • Updated power features with new color legend, indicating enhanced and new features (Slide 18) • Updated the list of package thermal models (Slide 25) • Updated device name in the title (Slide 28)
C	April 2013	• Added a PDN specification for VDD_DDR_CORE_1P2/ VDD_P1/ VDD_P4 (Slide 6) • Updated diagram and note for the differential routing of VSENSE_KRAIT_0P9 and REMOTE_GND_SNS nets (Slide 9) • Added a new slide for the conditions and notes for Linux Android/Windows Phone 8 (LA/WP8) power targets (Slide 20) • Updated power targets (Slide 21) • Updated thermal power concurrency information (Slide 33) • Added new slides for thermal design considerations (Slides 44-57)

Contents

Power Distribution Network (PDN)

Power Distribution Network Requirements

- PDN requirements are listed below:

Power domain	Max impedance DC to 10 Hz	Max impedance 10 Hz to 25 MHz
VDD_CORE	10 mΩ	22 mΩ
VDD_GFX	10 mΩ	56 mΩ
VDD_KRAIT	2 mW	17 mW
VDD_MEM	10 mΩ	18 mΩ
VDD_MODEM	10 mΩ	57 mΩ
VDD_DDR_CORE_1P2/ VDD_P1/ VDD_P4	11 mΩ	14 mΩ

- Design guidelines are provided in *Power Delivery Network Design* (80-VT310-13).

Thermal vs. PDN

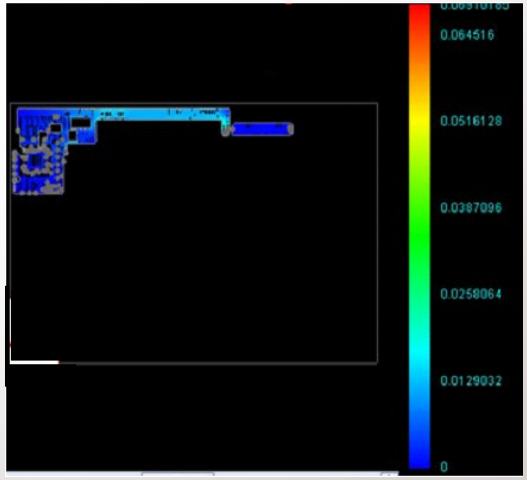
Question: What is the recommended distance between the PMIC and the processor (MSM8974) power supply pins?

Answer:

- The PCB placement distance between the PMIC and the processor must be determined from the results of phone level thermal simulations using commercially available thermal simulation software (e.g., Icepak or FloTHERM).
  - Placing the PMIC and the processor too close together on the PCB can greatly compromise the design from a thermal perspective.
- Once the placement of the PMIC and the processor has been defined by thermal simulation, PDN traces should be routed and verified by simulation in order to meet device specification requirements.
- Meeting PDN requirements will guarantee no functional failure due to PDN under worst-case temperature and process variations.

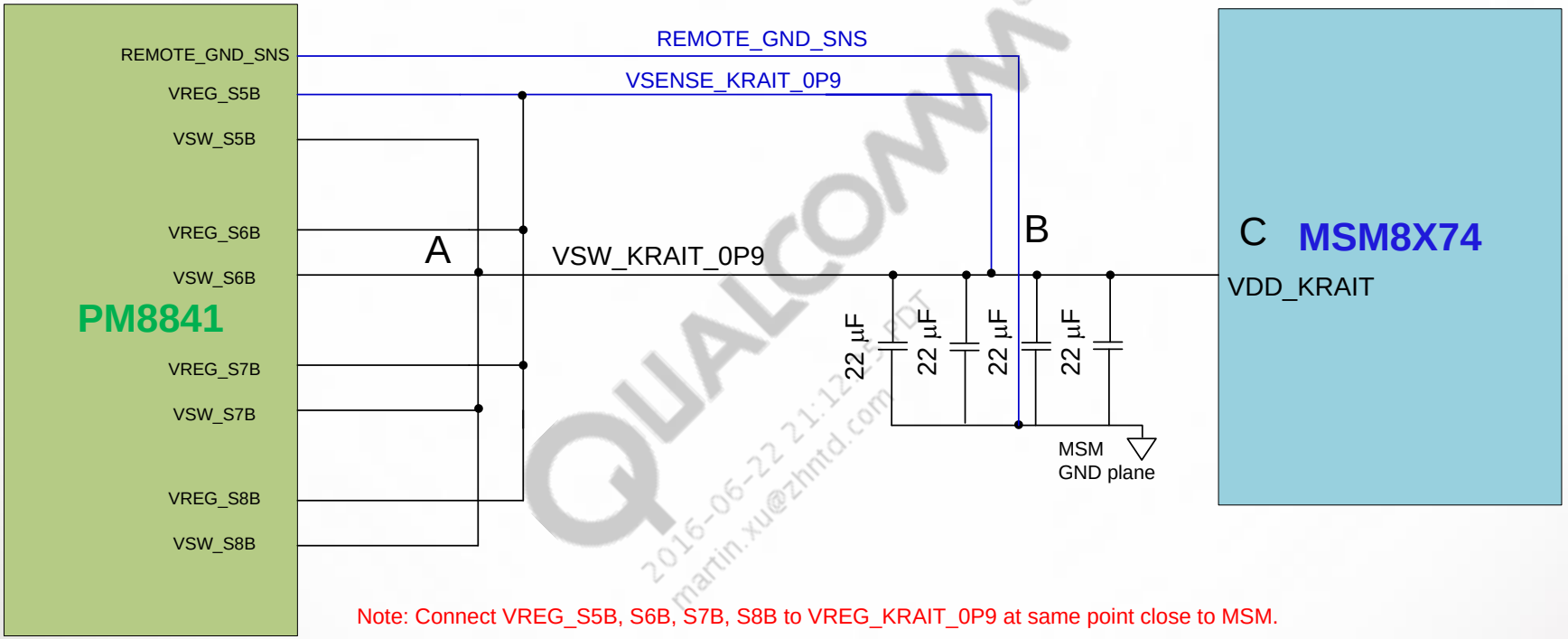
Static DC IR Drop

- Calculate the resistance of power trace between the PMIC and MSM™ device using:
  - R = ρ (L/A) where
  - ρ = Resistivity of copper
  - L = Length of trace
  - A = Cross-section area = width of trace × thickness of trace
- Calculate the minimum number of vias required to carry the current. Always use more vias than the minimum required.
  - Minimum vias ≥ Total current/Current carrying capacity of each via
  - Copper paste filled vias are used in certain PCBs. Copper paste is electrically and thermally less conductive than copper. More vias are required when using copper paste vias.
- Static IR drop analysis shows current densities at different locations in the layout.



Power Routing – VDD_KRAIT Power Supplies

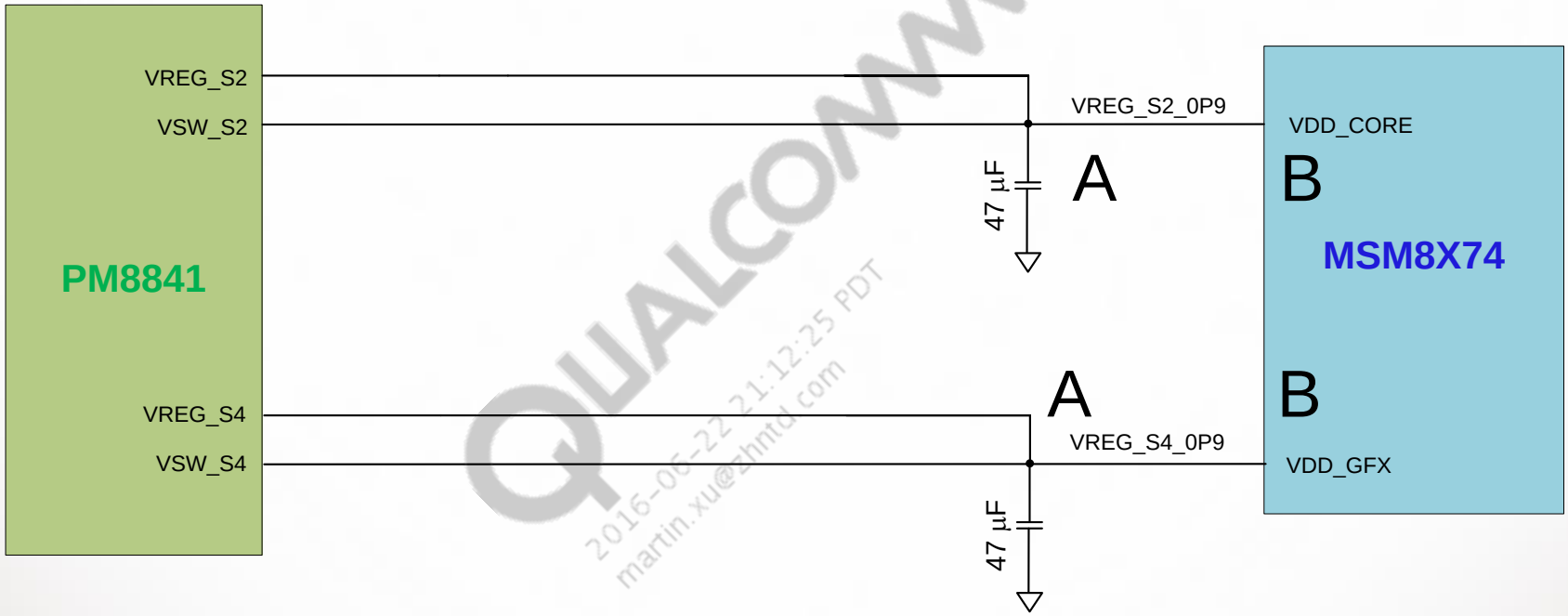
VSENSE_KRAIT_0P9 and REMOTE_GND_SNS need to be routed **differentially** as shown in below diagram



Note: Connect VREG_S5B, S6B, S7B, S8B to VREG_KRAIT_0P9 at same point close to MSM.

- The feedback pins for S5B-S8B should be shorted together (point A) close to the PMIC side and routed to a center point in the VDD_KRAIT fill area close to the MSM side.
- The REMOTE_GND_SNS pin of the PMIC should be routed to a center point in the GND fill area or plane close to the MSM side.
- The 2 mΩ PDN specification for VDD_KRAIT is from point B to C.

VDD_CORE and VDD_GFX Routing for MSM8974



- The 10 mΩ PDN specification for VDD_CORE/VDD_GFX is from point A to B.
- The bulk capacitors for VREG_S2 and VREG_S4 should be placed close to the MSM device.

Power Distribution – Power Traces Not Covered Under PDN Requirements

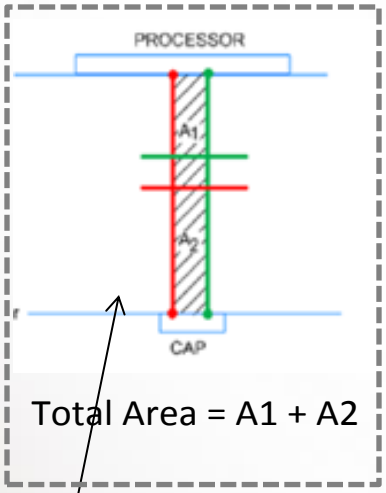
- Determine the minimum trace width for DC distribution using the following:
  1. Find the maximum current (I_{MAX}) conducted by the trace – the sum of maximum currents expected for all its loads.
  2. Define the regulator's operating output voltage (V_{REG}).
  3. Calculate the maximum tolerable trace resistance (R_{MAX}) assuming a 1% IR drop:

     $R_{MAX} = 0.01 \times V_{REG} / I_{MAX}$
  4. Estimate total trace length (L) based upon the preliminary layout.
  5. Determine the copper thickness (T): 1 ounce copper foil thickness is 1.34 mil – scale as needed for thicknesses other than 1 ounce.
  6. Calculate the minimum trace width (W_{MIN}) allowed.

     $W_{MIN} = \rho \times L / (R_{MAX} \times T)$ where ρ = copper resistivity (1.7×10^{-8} Ω-m)

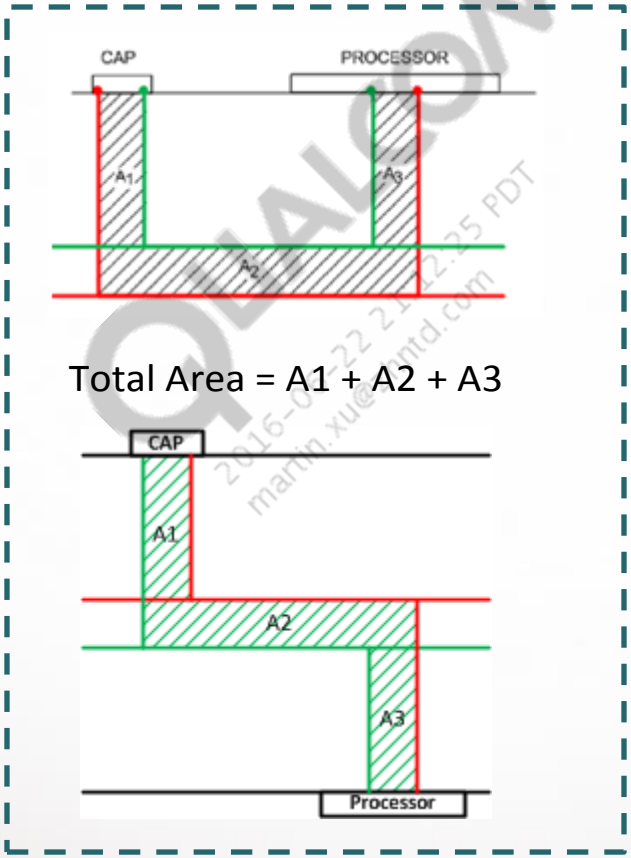
Capacitor Placements

- Lower power-ground loop area reduces loop inductance thereby improving the effectiveness of a capacitor at high frequencies.
- Local decoupling capacitors must be placed as close to the MSM pins as possible.

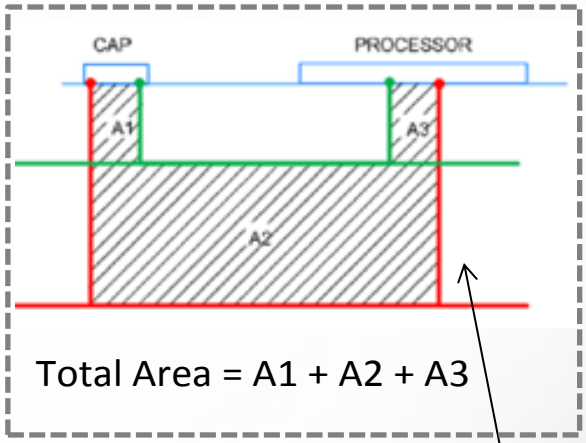


A

Least inductance



B



C

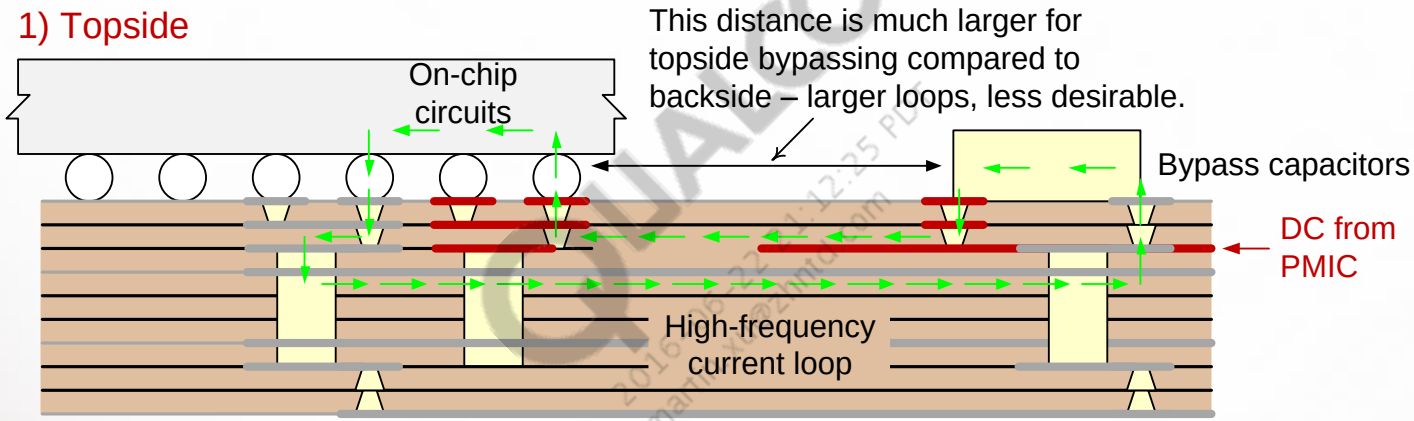
Largest inductance

Note: Geometries are not to scale.

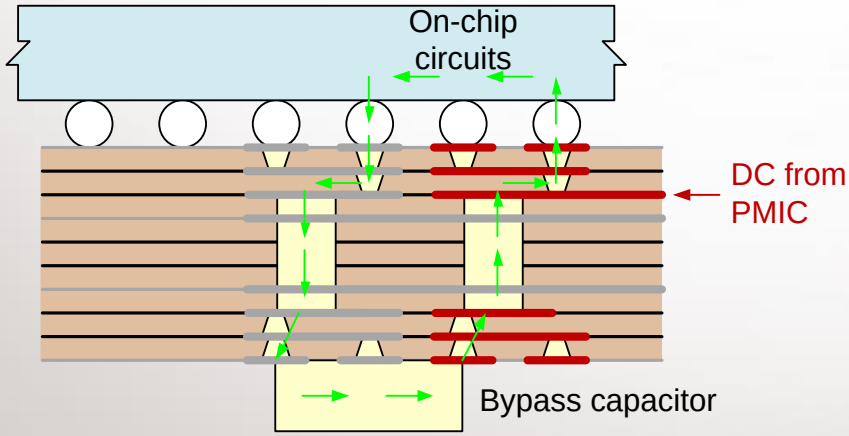
Topside Versus Backside Bypass Capacitors

- Bypass capacitors can be located on the same side as the MSM (topside) or on the opposite side (backside).
- Both are supported by the MSM IC.
- Backside is better, as illustrated, and easier to implement.
- Design examples are shown using topside (the more difficult routing).

1) Topside



2) Backside – smaller loop



Power

MSM8974 Power Architecture Concepts

(Note: The block diagram is an abstracted representation to show power features only and may not represent the actual chip.)

Low Power System and SoC techniques across the chipset:

- Activity driven clock gating
- DDR controller auto-self-refresh entry/exit
- PMIC auto switching between modes for better efficiency
- Distributed, fine grain energy management in HW
- Collapsible XPUs
- Optimized timeline operations including WAN standby, WLAN/BT Power
- Low leakage, voltage retention mode, with efficient switching in and out of retention

Improved Active power from 28HPm technology

Multiple voltage domains: CPU core0/1/2/3, GRP, modem, digital, memory

Collapsible logic domains & memories

Voltage scaling

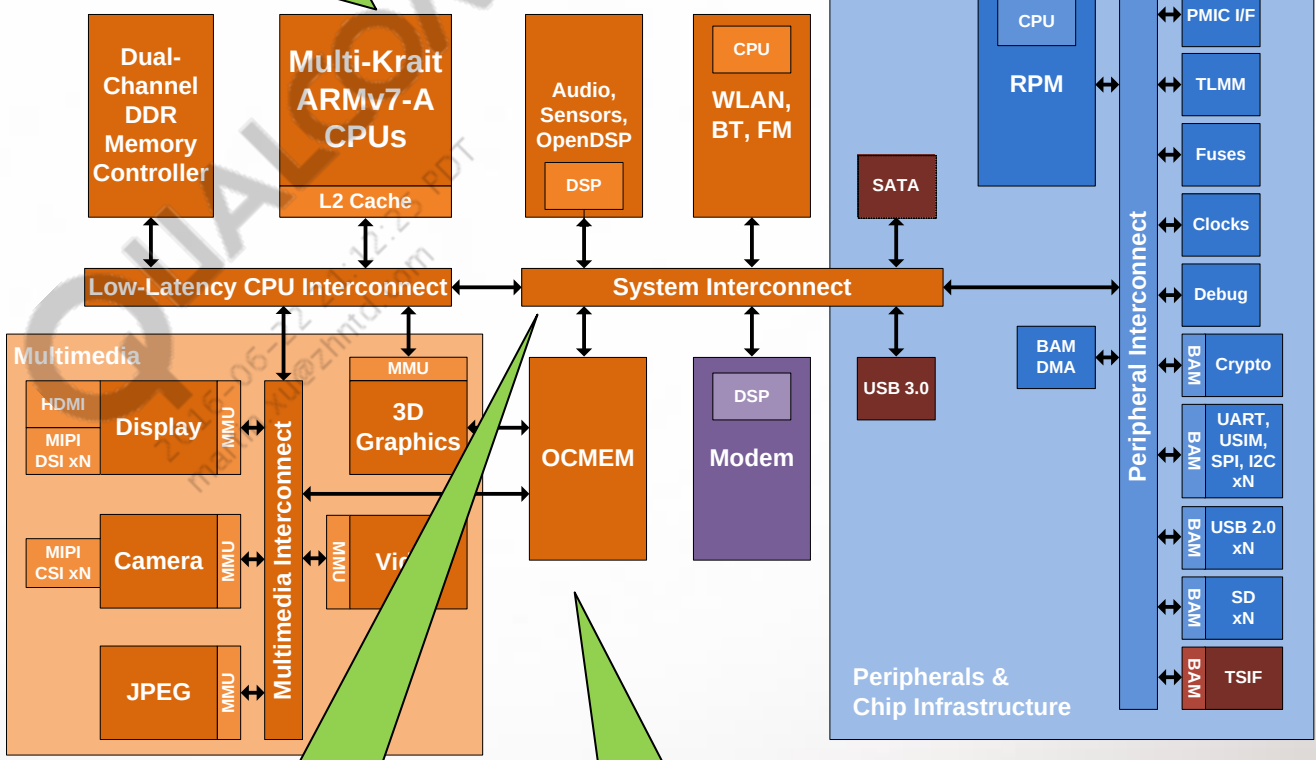
-Each CPU core scales in fine voltage steps

-Other core support Turbo, nominal, low and retention voltage levels.

Deep sleep modes to save leakage

-Low power/high performance proprietary design
-Improved/faster CPU power collapse
-Asynchronous clock frequencies for cores and L2

Coarse grain, use-case level energy management using RPM, with HW Acceleration for Resource control



Enhanced QoS based Interconnect for better performance and power

OCMEM to reduce traffic to external memory

Key Enhancements

Category	MSM8960	MSM8974
Resource management	Shared resource energy management using RPM (64 MHz ARM7), with HW acceleration for resource control	- RPM processor upgraded to 170/100 MHz Cortex M3, PMIC SPMI Interface - Changes to RPM-Core processor communication for improved timeline operations
Clocking	Split clocking (CXO+PXO)	Single crystal CXO
Voltage rails	Split-rail Cx/Mx, Q6 rails	Split-rail Cx/Mx, separate rails for MSS (modem subsystem), graphics
Multi-Krait	Individual switcher control	Unified PDN driven by multi-phase switchers, with eLDO for asymmetric operation
DCVS	Multi-processor-DCVS, GPU-DCVS	+ Bus-DCVS
OCMEM	-	Shared OCMEM for graphics, audio, sensors
Subsystem power managers	Gen 1 SAW (SPM AVS Wrapper), SPM (Subsystem Power Manager)	Enhanced for Quad-Kraits, connectivity, modem
Power grid	Auto-PFM operation of SMPS for improved efficiency at low-loads	Auto-mode applied to RF loads with subregulation (*) and isolation of WAN/LAN
Topology	Modem integration through Sys-NOC	Direct low-latency BIMC port for modem Q6

- Other changes
  - Sensors from ARM7 to LPASS
  - New Infrastructure blocks: DDR controller (BIMC) and interconnects (NOCs)

Enhancements for Low Power Integration

Category	MSM8974
WLAN DTIM	- Increase in WCSS (Wireless Connectivity Subsystem) internal memory (cMem) to allow all-local execution for WLAN-DTIM - SPM enhancements to increase SW offloading Overall, timeline reduction from 10+ ms down to ~6 ms, bringing down WLAN DTIM power contribution from 2+ mA to ~1.6 mA
WAN standby	MSM8974 platform enhancements, along with WAN improvements demonstrate potential to get standby numbers near best-in-class
WAN+ connectivity concurrency	Subregulated WAN+LAN RF loads allowing reduced power contribution with Voice-call + BT LPPS, WLAN DTIM

Note: DTIM means delivery traffic indication message and LPPS means low power page scan.

MSM8974 Power Features

Feature name	HW/SW	Feature description
Autonomous End-to-End QoS	HW/SW	Multi-priority, weight-based QoS and arbitration. Consistent solution through busses and memory controller.
Collapsible XPU and new MMU	SW	XPUs are collasible as part of VBIF for each MM (Multimedia) cores. System MMU for MM cores on 4 KB page boundary eliminate need for contiguous memory allocation (PMEM), reducing external memory copy operations.
OCMEM	HW/SW	Shared on-chip SRAM improves performance and power by reducing DRAM bandwidth.
MP-DCVS + GPU-DCVS	SW	Independent control of each CPU's and GPU voltage and MHz to optimize power and latencies.
Coarse grain freq scaling	SW	Adjusting the frequency of cores and infrastructure at the start of a use-case to save power.
SVS	HW/SW	Static voltage scaling of digital and memory rails.
System-DCVS	HW/SW	Bus frequency and voltage scaling.
Fine grain HW clock gating	HW	Helps reduce power by quickly turning clocks on and off based on activity without SW involvement.
DDR activity based auto self-refresh entry and exit	HW	Helps reduce power by putting DDR in self-refresh automatically when idle and improves transient response by bringing it out of self-refresh on activity, all without SW involvement.
Dynamic Memory Management (DMM)	SW	SW feature to move in-use memory to lower/contiguous region, to collapse other un-used resgion(s) or for single channel DDR operation.
PMIC auto mode switching	HW	Automatically switch mode between PFM, PWM and PS to save power.
Multiple voltage/power domains	HW/SW	Multiple voltage and power domains for independent voltage scaling and power collapse.
Split logic and memory rails	HW/SW	Separate voltage rails and regulators for logic and internal memories, allows lowering logic voltage while retaining the contents or collapse logic rail while retaining internal memories.
Dedicated PLLs	HW/SW	Dedicated PLL for each subsystem reduces inter-dependencies and allows each subsystem to achieve lowest power by lowering its MHz without affecting the performance of other subsystems.
VDD minimization	SW	VDD minimization for power saving.
Collapsible logic/memories	SW	Individually collapse internal memory blocks and architect additional collapsible domains.
Memory Controller (BIMC) power collapse	HW/SW	BIMC can be power collapsed to save leakage.
Modem power collapse	HW/SW	Modem + mDSP are all on a separate rail. The only way to collapse is by collapsing the rail.
SAW	HW	APSS and Q6SS have SAW to assist CPU power management.
Shared PLL HW managed on/off	HW	HW managed on/off based on executing environment votes.
Collapsible analog cores	HW/SW	Individually collapse unused analog cores (PHYs, DACs, ADCs, PLLs, Sensors).
XO shutdown	SW	All collapsible cores collapsed, VDD_DIG and VDD_MEM in retention; all other rails collapsed
PMDVS	HW	Process monitors based DVS: Scale voltage based on device characterization.
AVS	HW	Adaptive voltage scaling for power saving.

Technology | Dynamic pwr | Standby pwr | Archictecture

Supported previously; Enhancement; New

MSM8974 Power – Highlights (Projection-based)

- Significant (~10 to 15%) improvements in modem active power use cases
  - Digital-modem reductions
- Significant (~10 to 20%) improvements in multimedia graphics and video power use cases
  - Digital video and graphics core power improvements
- Low power use cases – process leakage increases mitigated through design changes

MSM8974 Chipset Power Targets

- Conditions:
  - System memory: 2 channels × (2 dies × 512 MB/die)/channel = 2 GB LPDDR3
  - Display: 720HD (1280 × 720)
  - 3.7 V battery
- Notes on Windows Phone 8 projection data:
  - *Projected numbers assuming a realizable CPU utilization and clock setting
  - Power contributions from Windows DCVS-driven operating points under analysis

MSM8974 Chipset Power Targets (2 GB LPDDR3, 720HD/1280 × 720)

Category	Use cases	LA	WP8
	Rock bottom sleep	**2.9-3.5**	**2.9-3.5**
	WCDMA standby 2.56 s	**3.2-3.8**	**3.2-3.8**
	WCDMA talk +0 dBm, IMT	**103-111**	**103-111**
	CDMA QPCH 5.12 s	**3.4-4.0**	**3.4-4.0**
	CDMA talk +0 dBm, CEL	**112-120**	**112-120**
	GSM standby 1.18 s	**3.5-4.2**	**3.5-4.2**
	GSM talk 5 dBm, no DTX, PGSM	**70-78**	**70-78**
	HSDPA DL 7.2 Mbps +0 dBm, IMT (RxD/No RxD)	**165-195/148-178**	**165-195/148-178 ***
	HSDPA DC 42 Mbps +0 dBm, IMT (RxD/No RxD)	**210-241/190-221**	**210-241/190-221***
	LTE standby 2.56 s	**3.5-4.1**	**3.5-4.1**
	LTE Cat 3 (68/23 Mbps, +0 dbm, B13)	**270-305**	**270-305 ***
	LTE Cat 3 (100/50 Mbps, +0 dBm, B7)	**390-440**	**390-440***
	LTE Cat 4 (150/50 Mbps, +0 dBm, B7)	**430-480**	**430-480 ***
	LTE Cat3 CA 10+10 (100/25 Mbps, +0 dBm, B4 + B17, Tx B17)	**425-475**	**425-475***
	TD-SCDMA standby 1.28 s	**3.4-4.0**	**3.4-4.0**
	TD-SCDMA talk 0 dBm, B34	**74-82**	**74-82**
	EV-DO DL 3.1 Mbps +0 dBm, CEL	**159-195**	**159 - 195***
Modem	SVLTE Cat2 (50 Mbps, +0 dBm, B13) & 1x voice	**375-430**	**375 – 430***
	GPS 1 Hz Trk (DPO)	**11-11.6**	**11-11.6**
GPS	GNSS 1 Hz Trk	**41-47**	**41-47**
	MP3 playback 128 kbps (TM)	**17.6-20.6**	**17.6-20.6**
	H.264 720p decode, 30 fps	**98-126**	**108-138***
	H.264 30 fps 1080P, 20 Mbps, decode	**127-155**	**137-172***
	H.264 30 fps 1080P, 20 Mbps, encode	–	–
	3D UI 30 fps (graphic, power lift)	**110-148**	**110-148***
	3D gaming (Egypt GLB2.1.1) 60 fps	**390-435**	**390-435***
Multimedia	Static image	**49-53**	**49-53**
	BT sniff/scan on W standby	**3.85-4.45 (.65)**	**3.85-4.45 (.65)**
Connectivity	WLAN DTIM1 on W standby	**4.8-5.5 (1.6-1.7)**	**4.8-5.5 (1.6-1.7)**
	Accel background processing @ 10 Hz (SNS5A)	**4.3-5.2 (1.4-1.7)**	**NA**
Sensors	Accel active use case @15 Hz (SNS4A)	**58-65 (8-12)**	**NA**
	Browser over Wi-Fi (WB1A)	**78-86**	**90-98***
Net apps	Video streaming over Wi-Fi (VS6A)	**146-177**	**146-177***

Thermal Design Considerations

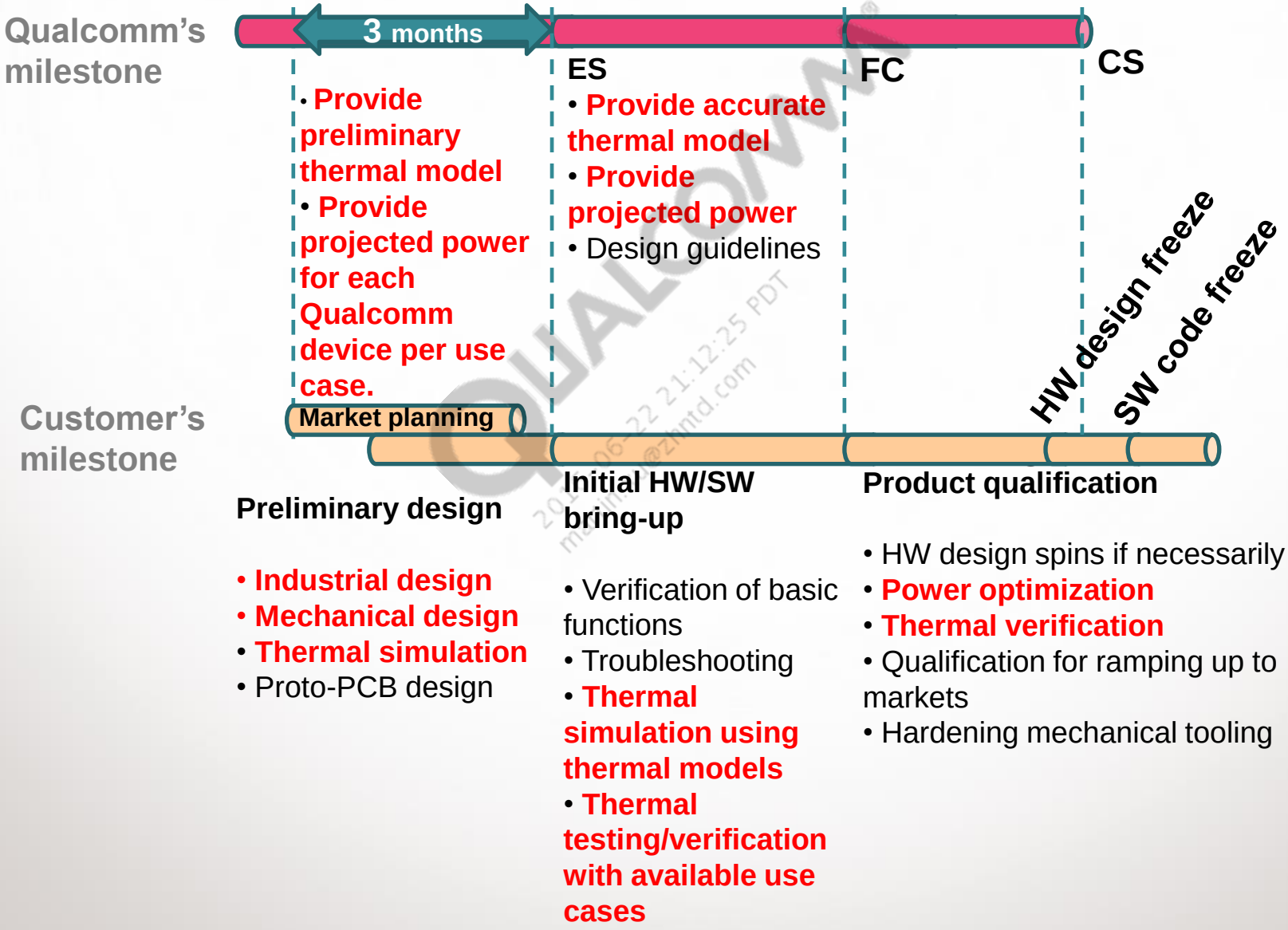
Agenda

- Introduction
- MSM8974 Thermal Topics
  - General key message
  - Thermal design milestone and typical chipset product development timeline
  - **Mobile Devices Thermal Design – Where to Start?**
  - MSM8x74 chipset packages thermal models
  - What to do with the thermal models?
  - Thermal simulation:
    - Packages thermal modeling and simulation
    - System thermal modeling and simulation
    - Transient vs. steady-state thermal analysis
- Projected power dissipation – thermal design power – TDP for MSM8x74 chipsets
- Thermal design considerations
- SW thermal mitigation
  - Definition and goals
    - Thermal testing – stress tests for mobile devices
  - Testing and bring-up with and with SW thermal mitigation

Introduction: What are MSM8x74 chipsets?

- MSM8x74 chipsets consist of the following supporting chips:
  - MSM8x74 (LPDDR3 POP, Quad Krait CPU cores)
  - PMICs: PM8841; PM8941
  - QFE1100; QFE2320; QFE1510
  - WCD9320
  - WCN36x0
  - WTR1605L
- The targeted platforms are high performance and rich graphics mobile devices.
- Higher performance means increased demand on the chipsets and increased heat.
- Qualcomm® **strongly** recommends that customers use these chipsets in their products to conduct thermal simulation for their overall systems under consideration.
- Thermal models for all packages are available in Icepak (filename.tzr – zipped form) and in FloTHERM (prb.pdml). The thermal models can be found on CDMATech Documents and Downloads.
- All thermal models have material properties; thermal resistance can be extracted, and there are validation procedures for the thermal models.
- Qualcomm also provides documents summarizing projected thermal power dissipation for certain use-case scenarios.

Thermal Design Milestones



MSM8974 Chipset Package Thermal Models

- Icepak models
  - WCN3680 Icepak Thermal Package Model (HS11-WL005-5HW)
  - WCD9320 84WLNSP Icepak Thermal Package Model (HS11-NA556-5HW)
  - QFE1100 28WLNSP Icepak Thermal Package Model (HS11-NA681-5HW)
  - QCA1990 30WLNSP Icepak Thermal Package Model (HS11-NB792-5HW)
  - MSM8974 Icepak Thermal Package Model (HS11-NA104-5HW)
  - PM8941 Icepak Thermal Package Model (HS11-NA445-5HW)
  - PM8841 Icepak Thermal Package Model (HS11-NA444-5HW)
  - WTR1605 Icepak Thermal Package Model (HS11-NA446-5HW)
- FloTHERM models
  - WCN3680 FloTHERM Thermal Package Model (HS11-WL005-6HW)
  - WCD9320 84WLNSP FloTHERM Thermal Package Model (HS11-NA556-6HW)
  - QFE1100 28WLNSP FloTHERM Thermal Package Model (HS11-NA681-6HW)
  - QCA1990 30WLNSP FloTHERM Thermal Package Model (HS11-NB792-6HW)
  - MSM8974 FloTHERM Thermal Package Model (HS11-NA437-6HW)
  - PM8941 FloTHERM Thermal Package Model (HS11-NA555-6HW)
  - PM8841 FloTHERM Thermal Package Model (HS11-NA554-6HW)
  - WTR1605 FloTHERM Thermal Package Model (HS11-NA446-6HW)

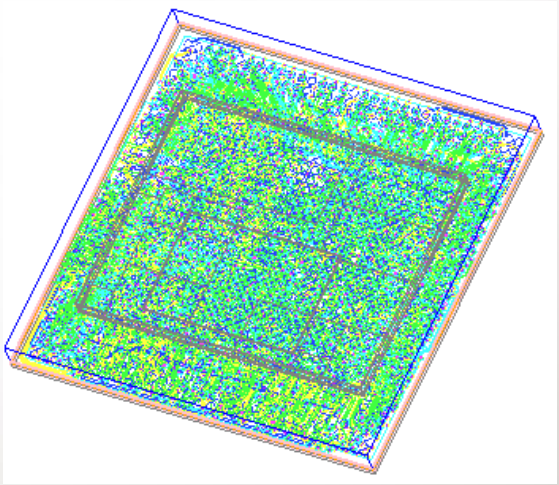
What to do with the Package Thermal Models from Qualcomm?

- Package thermal models provide:
  - Chipset components' overall packages form factor (dimensions)
  - Package thermal characteristics and physical properties
  - Information about how to obtain thermal resistance values
  - Validation with JEDEC standards that can be used to scale customers' PCB thermal performance; use such information for specific PCB designs
- Performing overall system thermal simulation:
  - Customers can download thermal models without recreating such models from scratch.
  - Uploading the packages' thermal models into customers' without re-meshing misalignment with the overall system thermal model
  - Customers are assured that these thermal models have been validated for power and temperature limits in a standard operating environment in standalone as well as in reference enclosure modes.
  - These models were created by professionals from the source with all pertinent information that customers will need to create their own overall enclosure form-factor thermal model and can drop in these packages' thermal models based on their layout requirements.
  - This represents tremendous time and resources savings for customers when performing a complex and successful thermal simulation.

Thermal Simulation – Building Blocks (Components Packages)

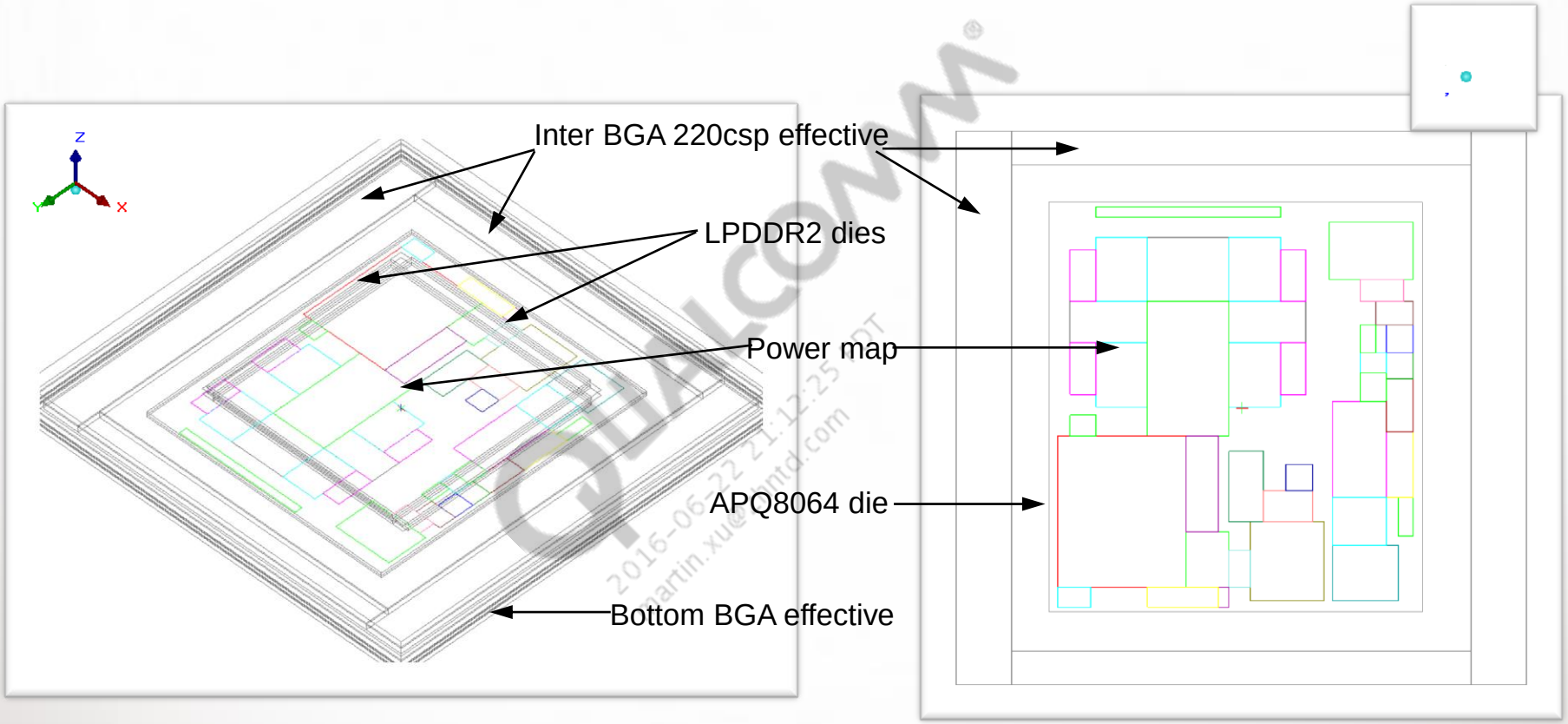
Package thermal model ISO and cross-sectional views

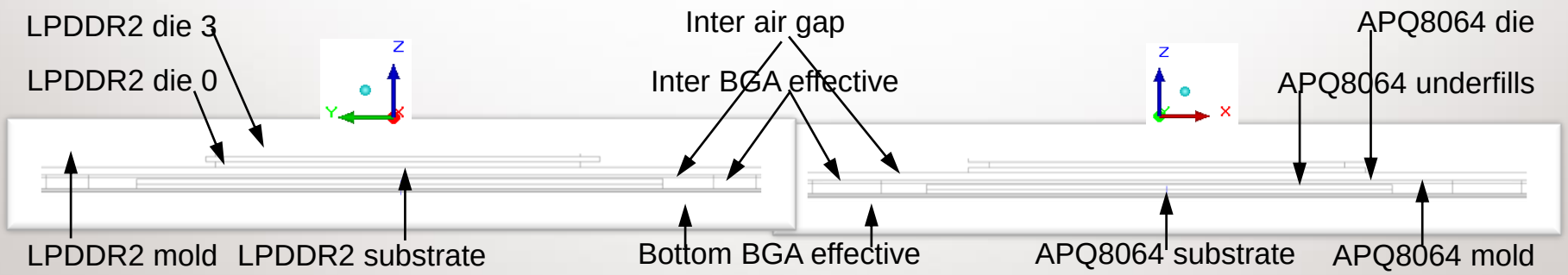
- Qualcomm provides package models for OEM customers
- Package thermal models are thoroughly validated.
- Models are picked and dropped in the overall system thermal model.
- Thermal properties are included in the thermal. models



Meshed package model for validation

An Example: APQ8064-839NSP – Package Thermal Model





Package Thermal Characteristics – Thermal Resistance Values for Packages

Tool: ANSYS Icepak 13.0

Solution domain

- Jedec JESD51-2A enclosure
  - 304 x 304 x 304 mm
  - Wall objects with zero thickness
- Jedec JESD51-9 test board
  - 114 x 76 x 1.6 mm
  - 4-layer, 1s2p (no thermal vias)
  - 2-1-1 Cu stackup (70u-35u-35u)
  - FR-4 dielectric
  - Top trace, K = 194 W/mK
  - Metal layers 2=3, K= 387 W/mK

Analysis type

- Steady-state conjugate heat transfer
- Natural convection air flow

Boundary conditions

- Heat trans coeff. applied to each cabinet wall
  - Heat Tr. Coeff. = 5.0 W/m^2-K
- Radiation
  - Surface-to-surface radiation model
  - Far-field temperature reference
  - Package mold and test board only
- Ambient air temperature = 70^{o}C

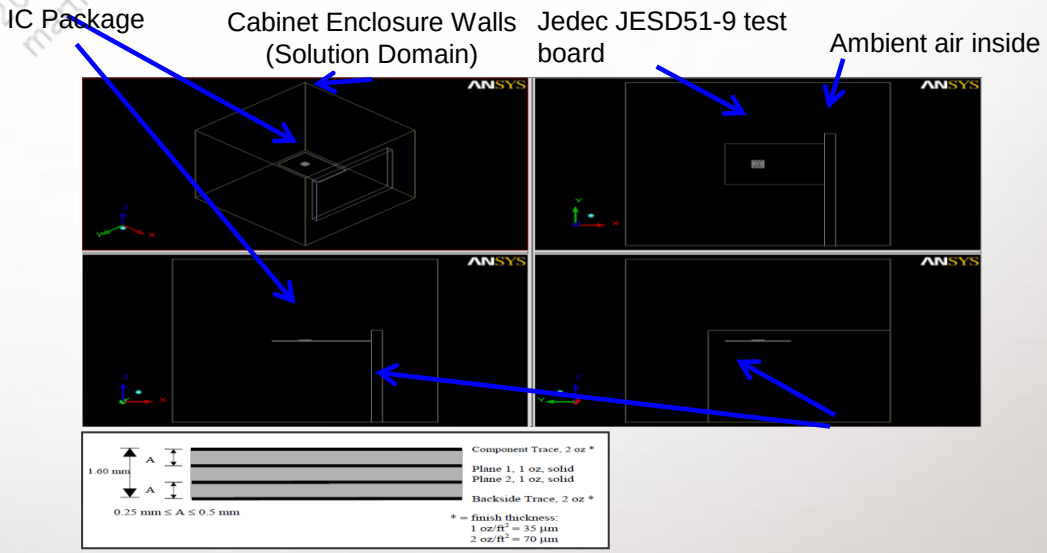
Mesh parameters

- Hexa unstructured
- 622,232 elements /681,149 nodes

Numerical precision = Double

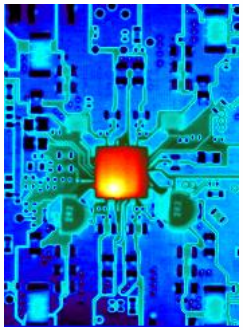
Component	Projected theoretical (through analysis) thermal resistance		Maximum junction temperature
	Θ_{ja} (C/W)	Θ_{jc} (C/W)	Degree C
MSM8x74	~22 C/W	~6 C/W	105; 85Tc
PM8841	~24 C/W	~5 C/W	Refer to device specs
PM8941	~24 C/W	~5 C/W	Refer to device specs
WTR1605L	~20 C/W	~4 C/W	105
WCN3660/80	~21 C/W	~6 C/W	105
QFE1100	~22 C/W	~4 C/W	105
QCA1990	~21 C/W	~5 C/W	105
WCD9320	~22 C/W	~6 C/W	105

Note: All packages thermal data were derived with simulation methods.

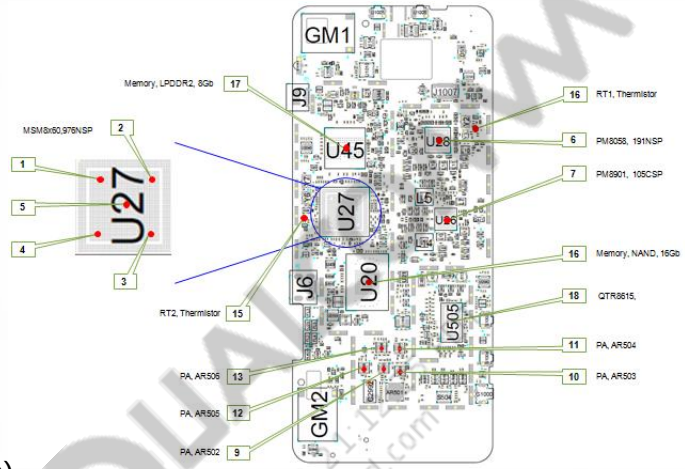


Overall System Thermal Simulation: An Example – FLUID Platform

Concurrency Power

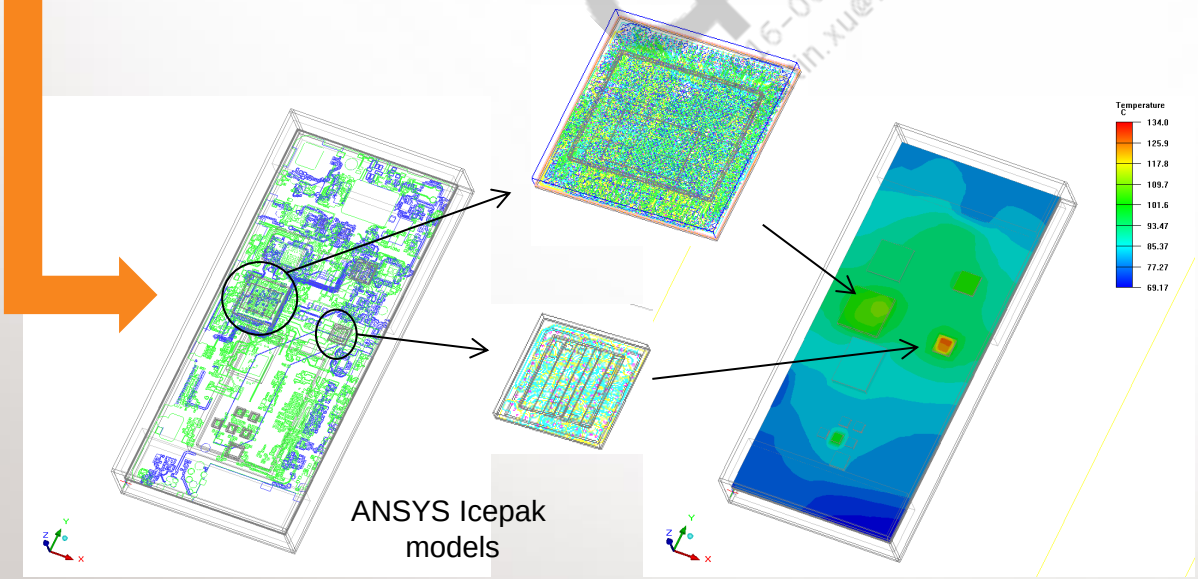


Infrared imaging
(FLIR SC4000 scientific camera)



Empirical data

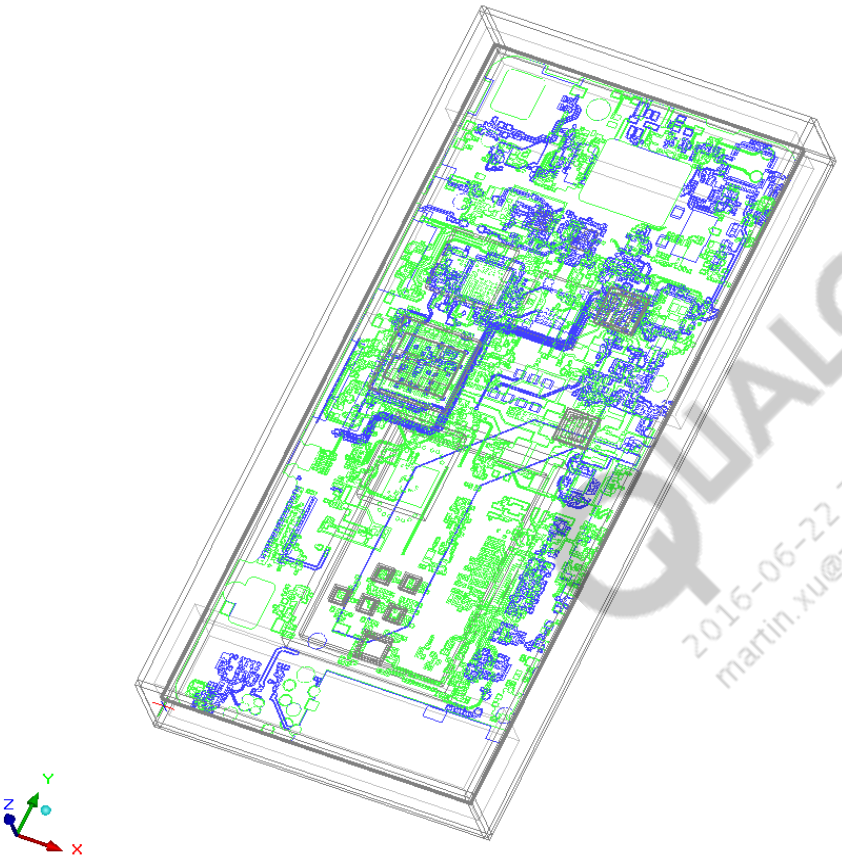
Benchmarking

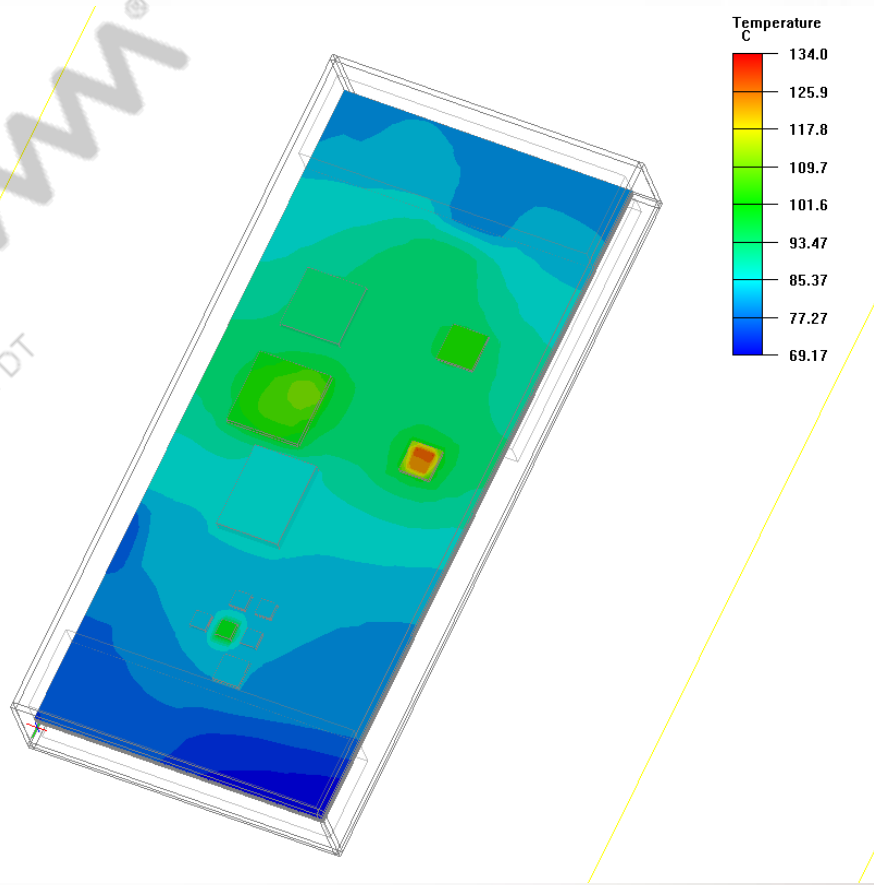


ANSYS Icepak
models

Thermal design kit

Overall System Thermal Simulation Output (Temperature Contours)





Overall system thermal model

Overall system thermal simulation results

- "What if?" scenarios (power use cases)
- Evaluate device skin and internal temperatures
- Early thermal prediction

Chipset Concurrency (Thermal) Power Breakout

Use case (Thermal power projections are evaluated at Ta (ambient temperature) of 25°C; however, the operating temperature of the respective devices while performing the task is as shown below.)	Unit: mW								
	MSM8974	POP -LPDDR3	WTR1605	PA1	WCD9320	WCN3660	PM8841	PM8941	Total
WCDMA voice call (24 dBm, -90 dBm Rx) at 55°C	227*	32	195	1276 (~250 mW radiated power)	8	0	44*	45	1830
LTE data call (CAT4, 150DL, 50 UL, B7 20 MHz, Tx = 22 dBm, Rx = -50 dBm) at 55°C	1505*	84	382	932 (~160 mW radiated power)	0	0	320*	95	3314
Graphics-intensive (Egypt 3D graphics, 60 fps) 1080 p display at 55°C	2761*	301	0	0	0	0	500*	70	3632
CPU-intensive (Quad Dhrystone, 2.3 GHz) at 85°C	5885**	10	0	0	0	0	1002**	13	6920

NOTES

1. **This is a thermal power projection, to be used for performing thermal analysis and simulation.**

2a. *** indicates the updated worst-case thermal power projection for this use case. Further updates are forthcoming.**

2b. ****Worst-case thermal power projection is still under investigation.**

3. **The preceding thermal power data has been estimated at room ambience of 25°C. However, the device operating temperature is as indicated while performing the stress task.**

4. **This thermal power projection is not intended to be used for PDN or power budgeting purposes.**

5. **PA thermal power = PA input power - PA output power (~Tx power).**
   - * Pending characterization
   - PA numbers include radiated power (250 mW for Wtalk, 160 mW for LTE which is not dissipated thermally)

4. **System key configuration: Android phone (2 GB LPDDR3, 1280 × 768 resolution, MIPI-DSI)**

5. **The power numbers listed are unmitigated, and will be lowered via thermal mitigation routines when the thermal limits are reached.**

6. **The PA and front-end power used are with envelope tracking.**

7. **LCD-related power is not included. The LCD power varies depending on the choice of LCD model/resolution/brightness.**

Note: This table contains preliminary information and is for illustration purposes only; an updated table will be available soon. The table was derived from *MSM8974 – Power Concurrency Values for Performing Device Thermal Analysis* (80-NA437-9, Rev. B, currently in work.)

Thermal Introduction and Reference Material

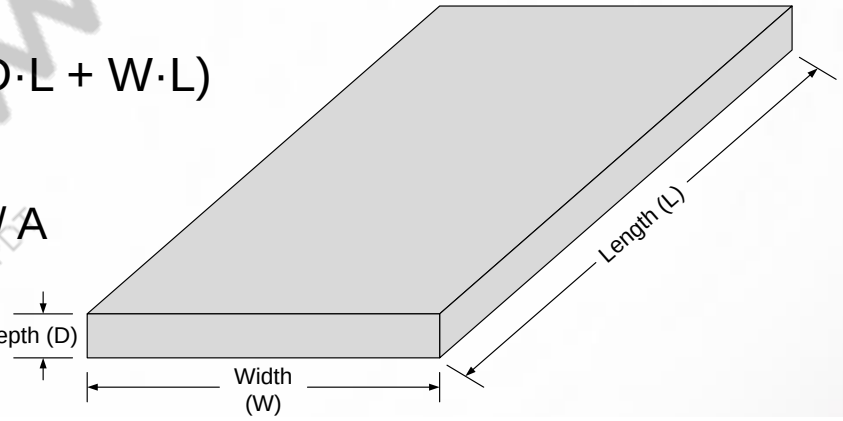
- Each generation of wireless handset devices adds more and more features, often into a smaller volume.
- Increasing power dissipation in small devices creates special mechanical/thermal design challenges.
- The thermal issues discussed on the following slides apply to all Qualcomm chipsets, regardless of the modem IC product-type (MSM, MDM, APQ, etc.).
- Each thermal issue needs to be evaluated at each stage of the development process.
  - Packaging and industrial design
  - Parts placements
  - PCB design — stack-up, via designs, ground planes, etc.
- In addition to the introductory presented on the following slides, download and study the related reference material:
  - *Thermal Design Considerations Application Note* (80-VU794-5)
  - *Thermal Protection Algorithm Overview* (80-VT344-1)
- Five thermal-related topics are discussed briefly within the following introduction:
  - Wireless product overall power density
  - PCB area
  - Distances between major heat sources
  - Package wall thickness and air flow
  - Heat conductivity below ICs

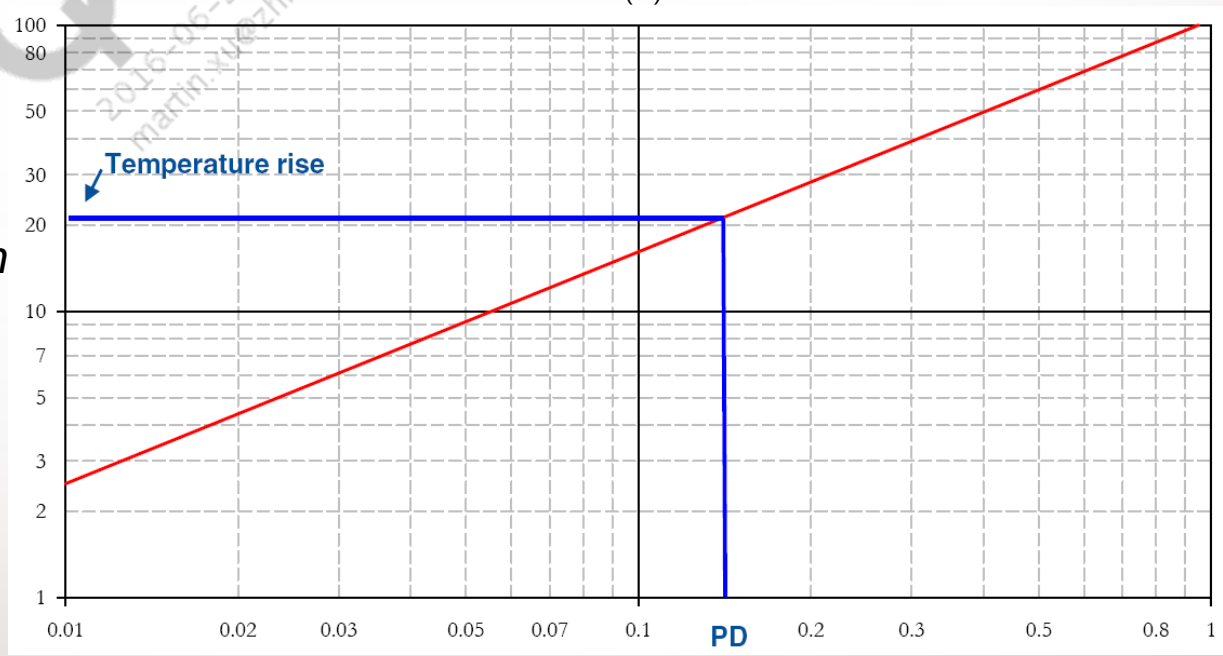
Wireless Product Overall Power Density

High power (or dissipation) in a small volume makes for a difficult thermal design.

A quick calculation and use of the plot at the lower right provides an estimate of a design's external surface temperature rise.

1. Calculate total surface area: $A = 2(D \cdot W + D \cdot L + W \cdot L)$
2. Calculate the total power dissipation (P)
3. Calculate the surface power density: $PD = P / A$
4. Estimate the temperature rise from the plot
   - In the example (blue lines)
     - PD ~ 1.5 W/in^2
     - ΔT ~ 21 °C

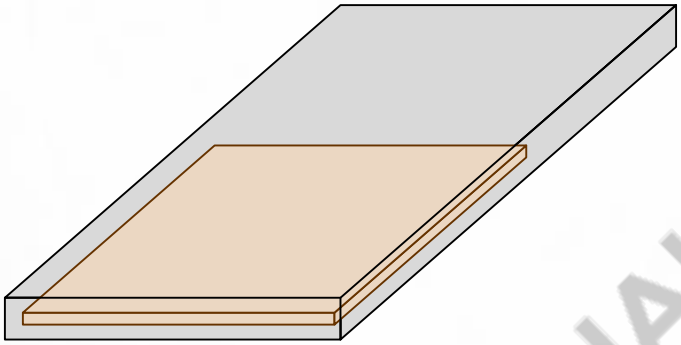


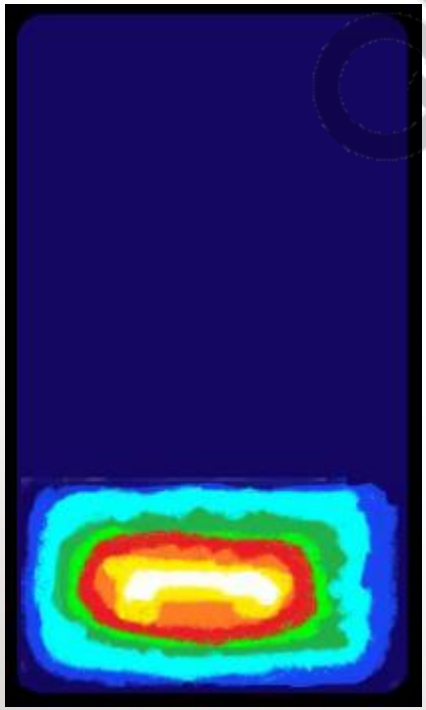


- See the *Thermal Design Considerations Application Note* (80-VU794-5) for additional details.

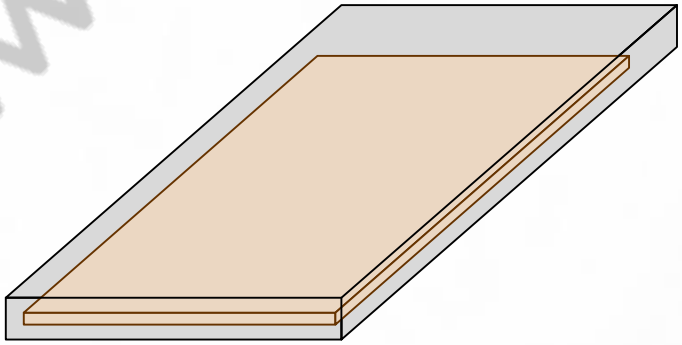
PCB Area and Heat Distribution

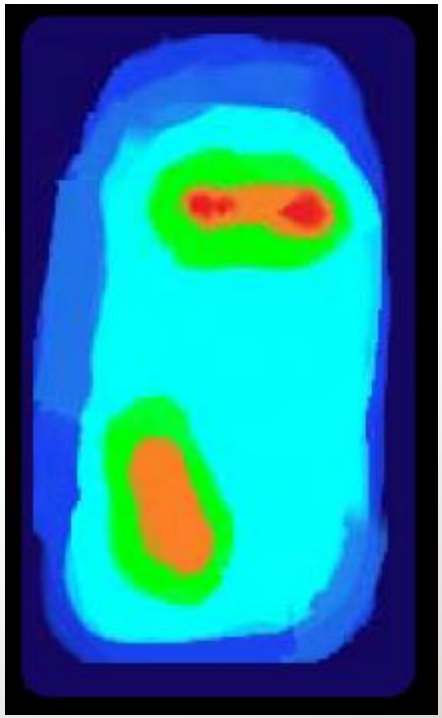
Spreading the heat across a large PCB surface area helps avoid hot spots within the handset.





Larger PCB area (and proper parts placements) results in better heat distribution.

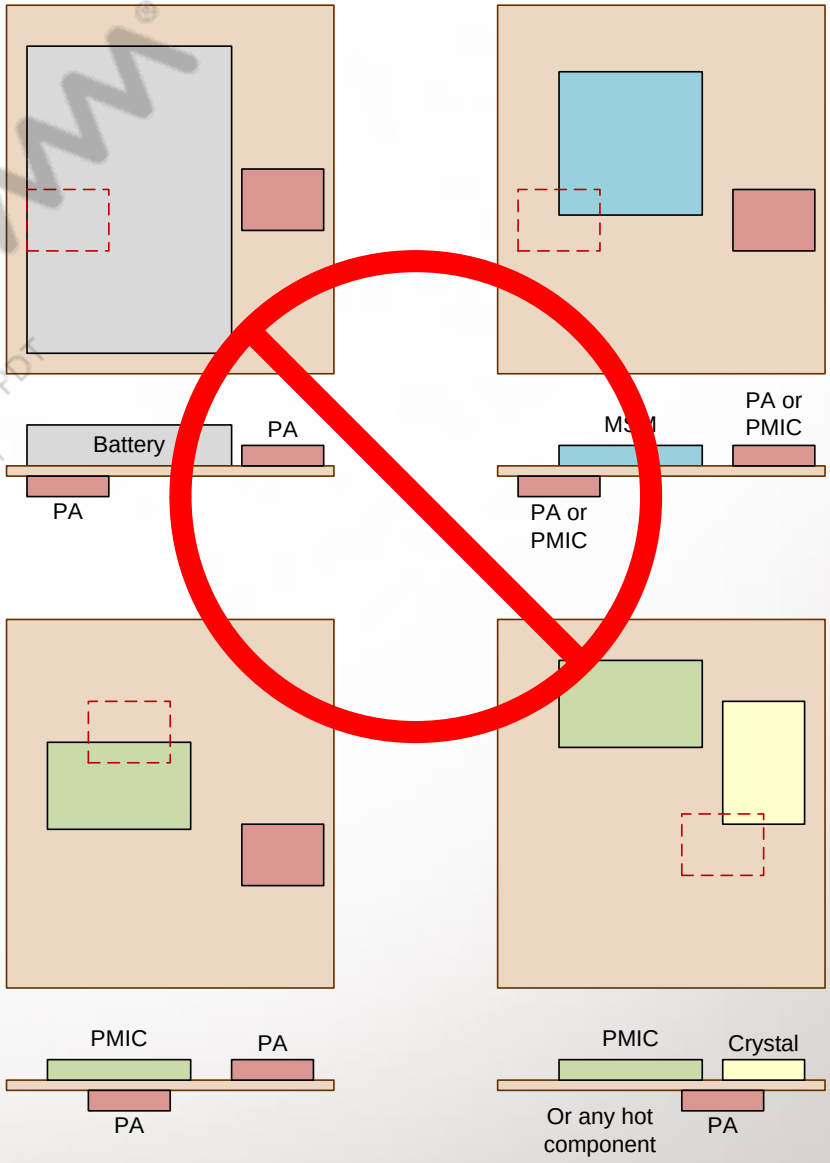




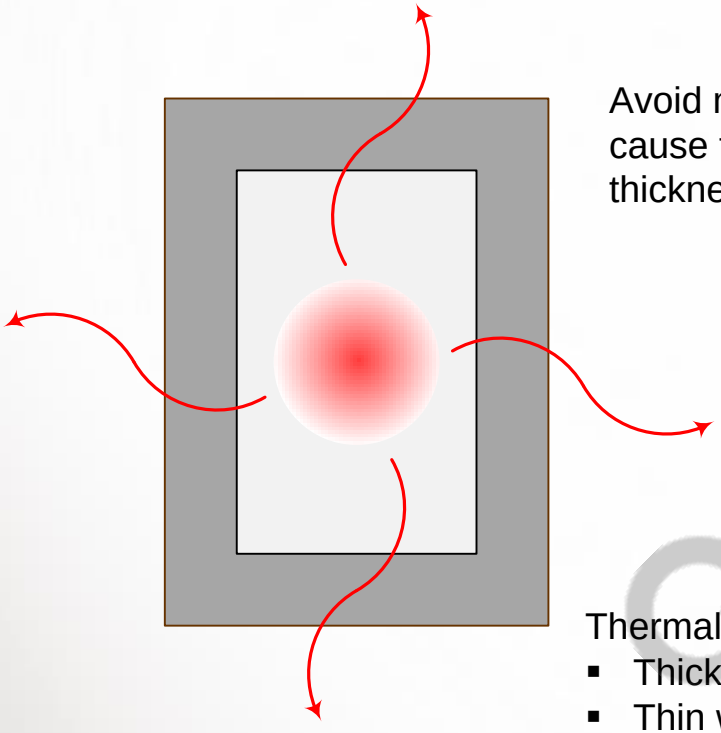
Distance Between Major Heat Source

Keep high power density parts away from each other – whether they are on the same side or opposite sides of the PCB.

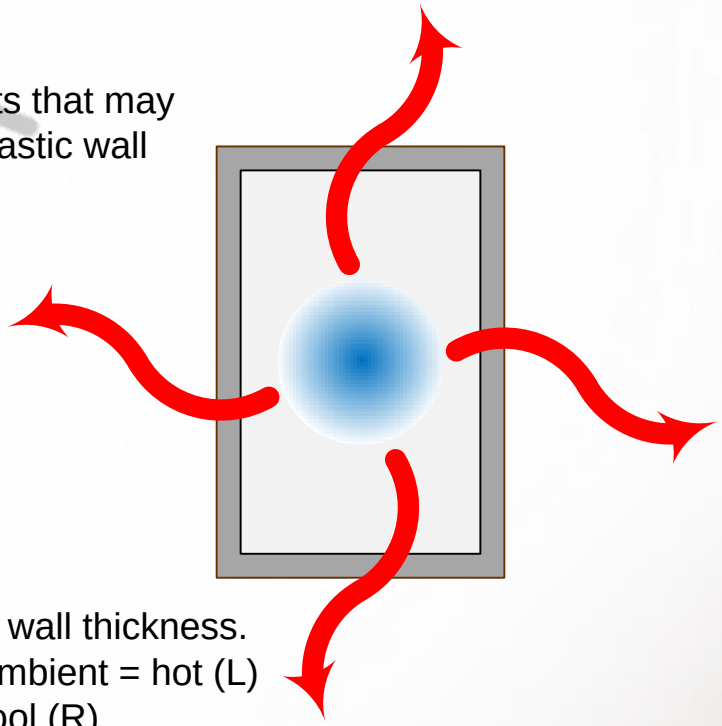
- Examples:
  - PA and other heat sources
  - Hot components and the battery
  - PMIC and modem IC
  - Oscillator crystals and heat sources that might cause harsh thermal gradients



Package Wall Thickness and Air Flow

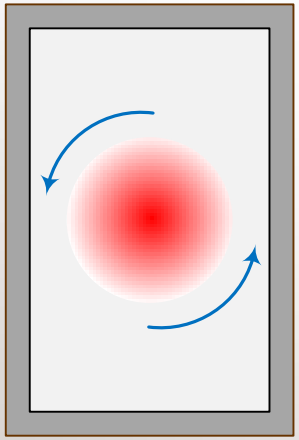


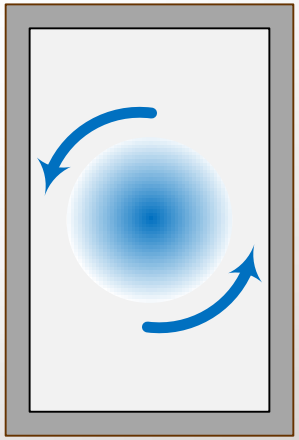
Avoid mechanical design constraints that may cause thermal issues – including plastic wall thickness and absence of air flow.



Thermal resistance is proportional to wall thickness.

- Thick walls = little conduction to ambient = hot (L)
- Thin walls = more conduction = cool (R)

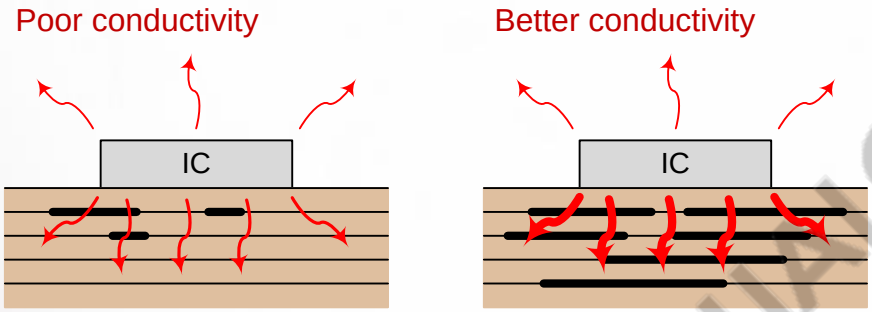




Air flow is very effective in reducing heat build-up.

- Little air flow (little convection) = hot (L)
- Adequate air flow = more convection = cool (R)

Heat Conductivity Below ICs

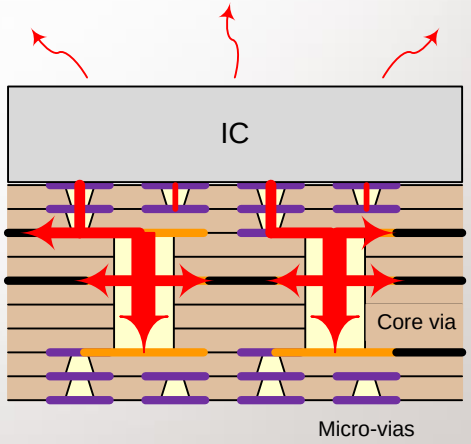


Include several layers with high copper density on each layer to increase thermal conductivity. Higher copper density provides better thermal relief and heat transfer.

- Do not rely on only air dissipation for RF power amplifiers; lots of copper is needed as a heat sink for these thermal loads.
- Fill empty board layers with copper wherever possible.
- It is very important that the heat source's mounting side is filled with copper.
- Use thick copper as much as possible; this is especially important for high current DC power supply distribution.

Include several vias under and around hot spots.

- Vias should go to large ground planes for better heat transfer.
- Via material is very important; solid copper is better than paste.
- Core vias are better than micro vias; stacked vias are better than staggered.
- Vias in the PA ground pad are very important; use as many as possible.



SW Thermal Mitigation (SW–TM)

- The MSM8x74 chipset family has thermal sensors on each chipset die.
- Thermal sensors detect maximum die active block temperature.
  - Sensors are calibrated and validated before releasing to customers.
  - Any correction factors will be implemented in the thermal mitigation SW.
- SW TM maintains the max die temperature at a preset value.
- SW-TM does not remove heat.
- If the die exceeds the preset value, the mobile device performance will be throttled.
  - The protocol of slowing or shutting down levels is predetermined based on the mobile device skin touch temperature requirements.
  - It is essential that customers download the latest thermal mitigation SW.
  - No bootup or testing should be attempted without SW thermal mitigation.

Why Do We Need SW Thermal Mitigation Algorithms?

The SW thermal mitigation algorithm is targeted to:

- Protect components from exceeding thermal design limits; if the limits are exceeded, the quality of service (QoS) can be degraded, and components can be damaged
- Ensure compliance with external case and touch temperature requirements from customers, carriers, and standard organizations (underwriters laboratory, PCI express, and user expectations)
- Minimize the risk of power-limit constraints
- Manage the thermal risk and tradeoffs during concurrent operations
- Allow limited customizable temperature thresholds and methods for power reduction

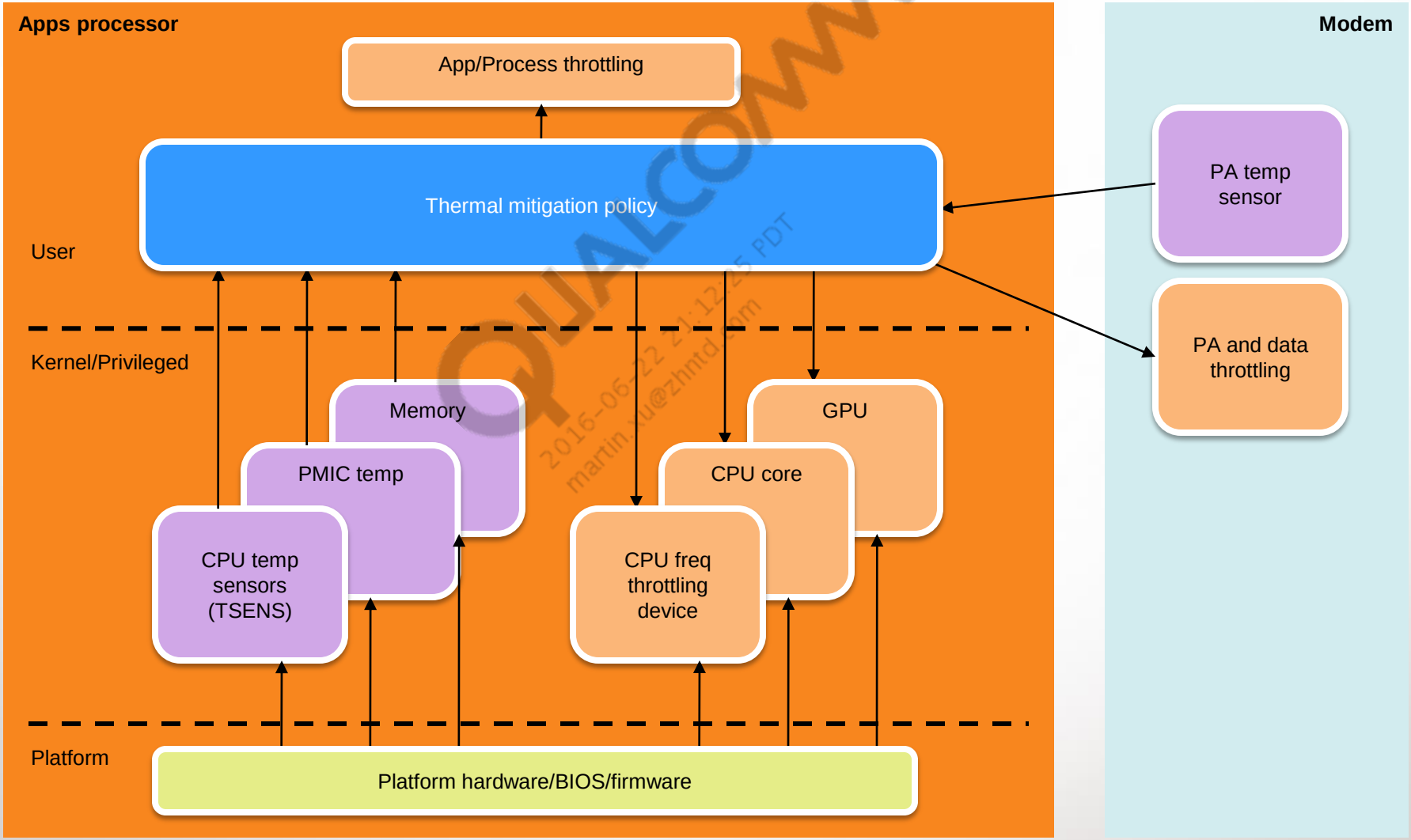
Thermal mitigation algorithm (TMA) allows:

- Protection against user harm or component damage for rare worst-case conditions
- Controlling/reducing temperature by trading off device performance

TMA does *not:*

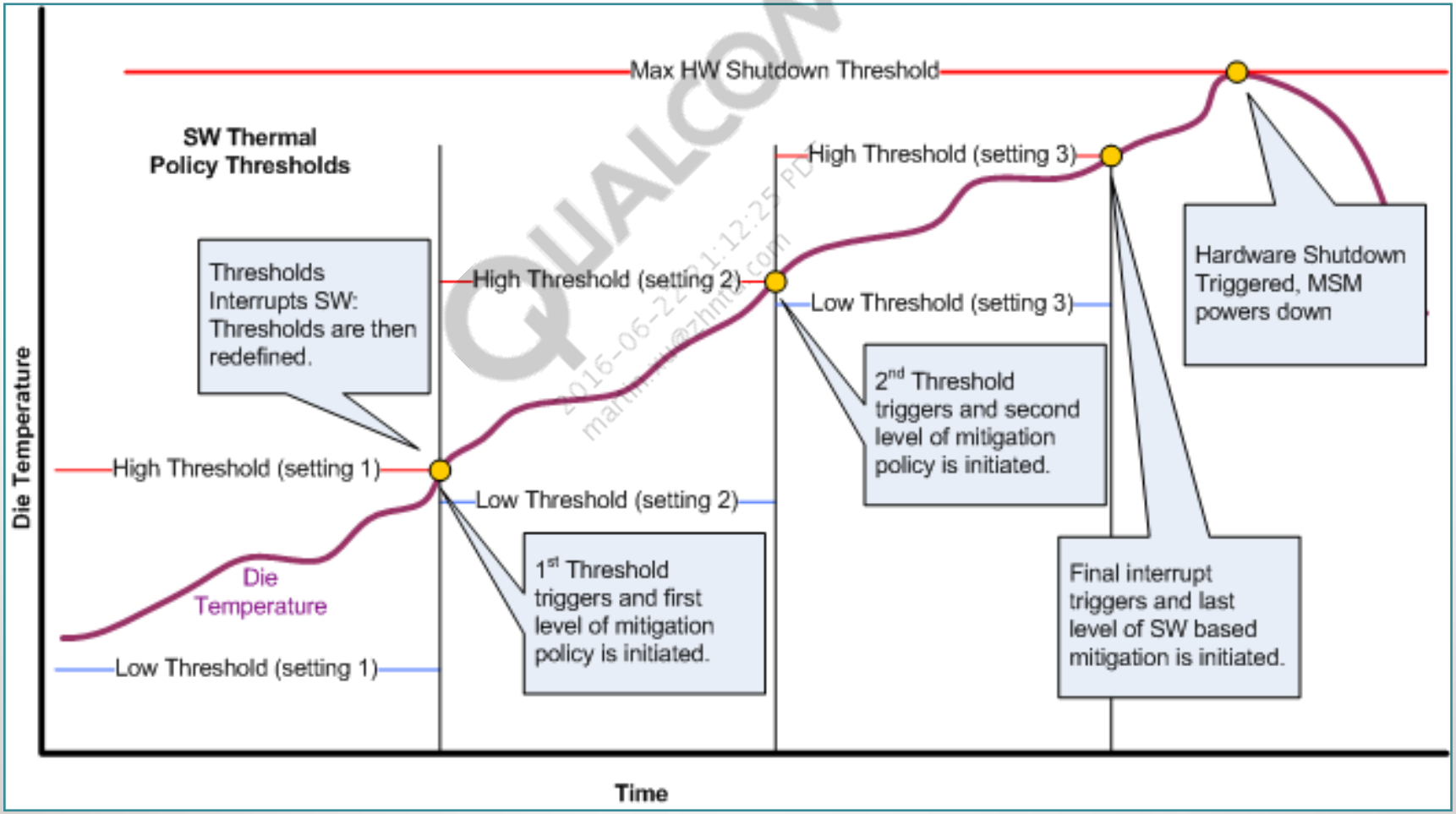
- Alter basic power efficiency or heat dissipation properties of the device
- Change mechanics of the device
- Fix the cause of heat
- Remove heat

SW Thermal Management Architecture Overview for MSM Systems



HW Response: TM vs. Temperature Plot (Example)

The MSM device has three to eight software temperature threshold/mitigation levels and one high hardware shutdown limit.



Design for Thermal: Key Requirements

Why, What, Where, and When

Definitions

- **CFD software:** Third-party computational fluid dynamics software used to design for thermal management. Solves energy, continuity, and momentum equations. (Examples are Icepak by ANSYS and FloTHERM from Mentor Graphics.)
- **Device:** Any type of wireless terminal, smartphone, or data card.
- **Device skin:** The outside material on a device that is typically in contact with a user.
- **Heat:** Thermal energy (J) typically transferred by conduction, convection, or radiation as a result of a temperature difference. The term “heat” can also be used interchangeably with thermal power (W).
- **Heat capacity:** Amount of heat required to increase the temperature of a device by one degree. (J/°C)
- **Heat density:** Heat (thermal power) per unit area (W/m^2)
- **Heat spreader:** Material with high thermal conductivity (k) used to reduce peak temperatures through heat dissipation. Effectively increases the overall heat capacity of a design. (e.g., PCB copper ground planes, metal shields, metal device skins, and thin graphite based sheets).
- **ID/MD:** Industrial design/mechanical design. The most significant factor in designing for thermal. Refers to the entire form factor of a device including total surface area, skin material type and finish, all dimensions and relative placement of ICs, shields, battery, sockets, peripherals, LCD panels, PCB stack-up, via type, amount of copper, etc.
- **Isotherms:** Temperature profiles of a device generated by thermal CFD software. Each line in an isotherm represents a constant temperature.
- **KPI:** Key performance indicators.
- **Thermal conductivity:** The measure of a materials ability to conduct heat. (W/m°K).
- **Thermal power:** The amount of heat energy per unit time. (W)
- **Thermal equilibrium:** A steady state where there is no longer any change in temperature over time.

Requirements to Design for Thermal (1 of 6)

Why is this needed?

- Heat generation is increasing and device form factors are shrinking.
  - **Higher performance** (more heat generated)
    - Increase in CPU, graphics, and memory clock frequencies
    - Product performance exceeding laptop performance of a few years ago.
    - Leakage current increases exponentially with temperature. (Leakage current also generates heat.)
  - **Smaller form factors** (less heat capacity)
    - The industrial & mechanical design (ID/MD) determine the overall heat capacity of a device.
    - Thinner form factors make it more difficult to incorporate heat spreader material.
  - **Smaller process nodes** (more heat generated)
    - Supply voltages no longer scale down linearly with process node
    - Increase in leakage currents.
- Increased heat creates potential issues:
  - Uncomfortable or unusable device skin temperatures
  - Increased probability of thermally induced failure in IC components
- Thermal mitigation algorithms decrease performance and user experience

Key message: *Proper thermal design greatly extends the time of operation at maximum performance levels without adversely affecting user experience or increasing the probability of device failure.*

Requirements to Design for Thermal (2 of 6)

What is needed?

- Thermal models for key components – supplied by Qualcomm
  - Theoretically validated through JEDEC standards
  - Includes material property characteristics and basic geometry
  - Includes relevant heat sources (Note: customers can modify the models to suite their use-case scenarios.)
- Thermal use-case examples – supplied by Qualcomm
  - Thermal power concurrency per device for the most challenging use cases
- Thermal CFD software – purchased by the customer
  - Icepak from ANSYS or FloTHERM from Mentor Graphics
  - Solves energy, continuity, and momentum equations
  - Provides temperature profiles for each component of the design including ICs and skin
  - Enables “What if?” scenarios allowing the designer to select the proper materials, components, geometries, and overall industrial/mechanical design to achieve goals in performance, user experience, and cost

Key message: *Thermal CFD software must be purchased by the customer and used with models from Qualcomm in order to properly design for thermal*

Requirements to Design for Thermal (3 of 6)

What is needed? (cont.)

- Chipset hardware requirements – supplied by Qualcomm
  - Design guidelines contain chipset thermal design information (e.g., thermistor placement)
  - The *Thermal Design Checklist* document (80-VU794-21) contains important thermal design information.
  - Device specifications contain chipset max case temperature and PDN specifications.
- Software to control thermal power in passively cooled devices – supplied by Qualcomm
- Key performance indicators (KPIs) must be defined by the customer.
  - Example: Download data at maximum data rates during video playback of 30 fps at 1080p for X minutes with no impact to user (no fps or data rate degradation or device skin/IC case temperature issue)
- Software parameters for each device or device subsystem to control overall thermal power must be tuned by the customer.
  - Examples: WLAN, LCD backlight, CPU, GPU, modem (WCDMA, 1X EV-DO, LTE, GSM,TDS CDMA), battery charging, kernel, camcorder, core control, threshold control, dynamic control algorithm, battery current limiting, speaker coil calibration (for speaker protection algorithm), SBL thermal management, low temperature voltage restriction

Key message: *The customer must define thermal KPIs, design ID/MD using CFD thermal SW, and edit thermal configuration files.*

Requirements to Design for Thermal (4 of 6)

Why thermal management software?

- Compensate for inadequate ID/MD design (not enough heat capacity)
- Manage IC case temperature limits 85–90°C logic/85°C PMIC, POP memory 85°C
- Manage device skin temperature limits (OEM/carrier typically 45°C – depends on material and finish)

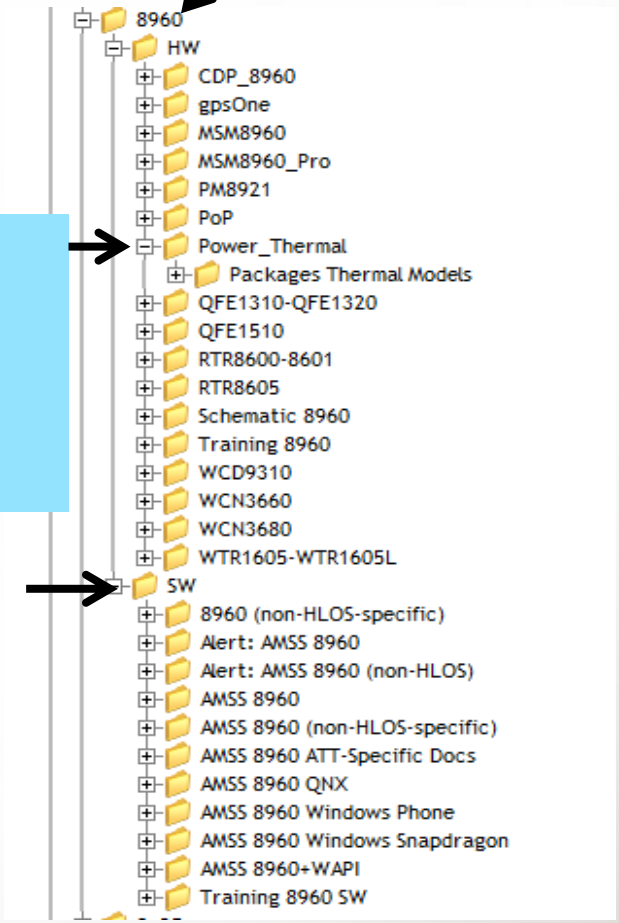
- Hardware sensors
  - Temperature sensors on the MSM die (MSM7x25A, MSM8x25, and MSM8x25Q are exceptions)
  - Board thermistors – PMIC, PA, and XO. (See chipset design guidelines for details)
- How it works
  - Passive cooling by reducing performance
  - The customer MUST configure thermal management devices and thresholds for each unique ID/MD. The goal is to optimize the tradeoff between maximum system performance and device temperature.
- Thermal SW architecture
  - A thermal daemon controls thermal management device performance levels.
  - Thermal management devices communicate with kernel space drivers, user space daemons, and other remote subsystems.
  - Provides coverage from boot up to power down

Key message: *Thermal mitigation software cools devices by limiting performance (e.g., reduces fps, data throughput, effective mips, clock rates, etc.).*

Requirements to Design for Thermal (5 of 6)

- Where to obtain the thermal models, use cases, training?

Chipset number



Power_Thermal folder:

- ❑ Package thermal models
- ❑ Thermal power concurrency use cases
- ❑ *Thermal Design Check List* (80-VU794-21)
- ❑ Thermal training docs

SW folder:

- ❑ Thermal mitigation docs
- ❑ OS specifics SW dos
- ❑ Training docs

Key message: *Qualcomm's customer portal, Docs & Downloads, contains thermal models, thermal use cases, and thermal training for each chipset.*

Requirements to Design for Thermal (6 of 6)

When are these items needed?

- Thermal KPIs – defined by the customer
  - At least two months before Qualcomm ES
- Thermal models for key components – supplied by Qualcomm
  - During ID & MD definition
  - Typically two months before Qualcomm ES
- Thermal use-case examples – supplied by Qualcomm
  - Two months before ES
- Thermal CFD software – purchased by customer
  - At least three months before ES (allow time for training by third-party SW vendor)

Key message: *Plan to start thermal simulations approximately two months before Qualcomm chipset engineering samples are available. See the next slides for details on thermal design timelines.*

Timeline to Design for Thermal (1 of 3)

~8 to 12 weeks before Qualcomm ES and/or customer's first SMT

- Qualcomm thermal models and use-case projections, current consumption documents are released for download.
- Customer to define power and thermal KPIs.
- Customer to define ID/MD, including battery size and chipset placement on PCB.
- Customer to start thermal simulations using CFD software (e.g., Icepak or FloTHERM).

~6 to 8 weeks before ES (and/or customer's first SMT)

- Qualcomm reference schematic and design guidelines are available for download.
- Customer to create schematic and submit for review (open a schematic design review case).

~4 to 6 weeks before ES (and/or customer's first SMT)

- Customer to submit parts placement, PDN, and critical signal routing for review (via PDN and routing review case).
- Customer to re-simulate any PDN or thermal-related KPIs affected by PDN and thermal final parts placement and/or critical routes.

Timeline to Design for Thermal (2 of 3)

~Qualcomm HW + SW ES (and/or customer's first SMT)

- Customer completes SMT. Initial board bring-up and debug.

~Two months after ES

- Qualcomm completes characterization and PVS fuses are blown on samples shipping from this timeframe.
- Customer to install shields and button up phones for initial thermal testing.
- Customer to run high power use cases (as SW available) to confirm assumptions about hot spots and power dissipation. Begin to validate KPIs on thermal.

Qualcomm feature-complete (FC) software

- Qualcomm includes auto voltage scaling (AVS) and thermal mitigation algorithms in the SW build.
- Customers to begin tuning SW to minimize power consumption.
- Customers to begin testing thermal mitigation algorithms.
  - Set thermal mitigation trigger points.
  - Calibrate thermal related items.

Timeline to Design for Thermal (3 of 3)

~Qualcomm CS (HW + SW)

- Qualcomm includes any final adjustments to PVS/AVS and thermal software.
- Customer to complete SMT and begins CS hardware bring-up.
- Customer to submit thermal management plan for review.
  - Joint review of thermal software and test-related items: config files, thermal KPIs, and test plan.
- Customer to verify that overall KPIs on performance, power, and thermal are acceptable.
  - Thermal mitigation algorithm tuning.
  - Final adjustments to ID/MD.
  - Use case performance vs. time and temperature KPIs.
  - Current consumption vs. use cases.

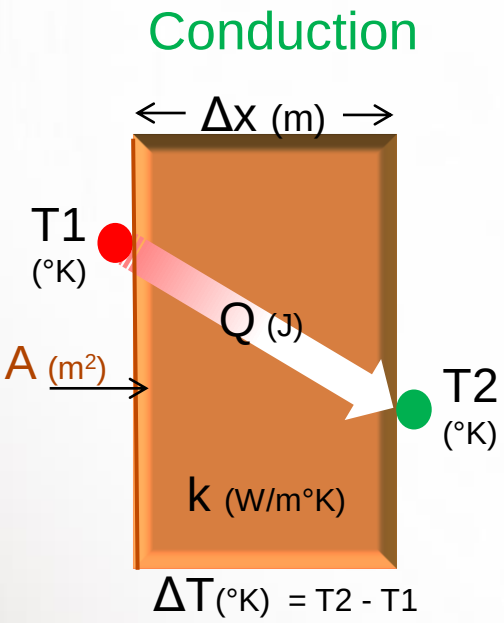
Customer lab entry

- Customer software including thermal config files should be frozen at this time.

Product launch!

Backup – Thermal Concepts

Thermal Concepts: Conductive Heat Transfer



Q' = heat transfer rate (W)

$$\frac{\Delta Q}{\Delta t} = -kA\frac{\Delta T}{\Delta x}$$

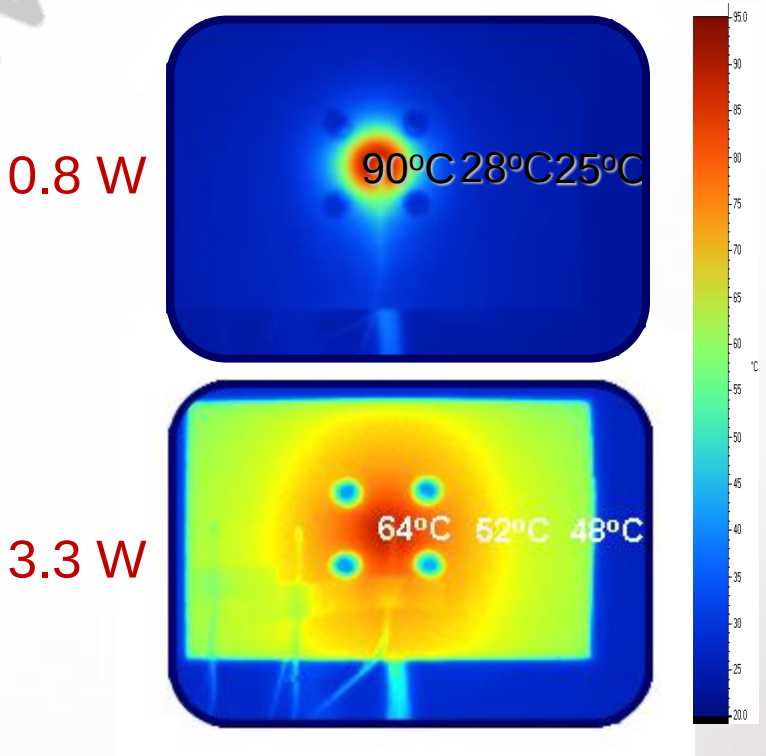
- A larger thermal conductivity (k) material conducts heat better.
  - Metal shields, PCB ground planes, graphite sheets, and device skins made of higher k materials help lower peak temperatures in devices by transferring larger amounts of heat energy away from hot spots (also known as heat spreaders).
    - Graphite (in-plane): k > 370 W/m°K
    - Copper: k = 360 W/m°K
    - Aluminum: k = 205 W/m°K
    - Magnesium: k = 156 W/m°K
    - Plastic: k = 0.2 W/m°K
    - Air: k = 0.024 W/m°K
- A larger heat transfer surface area (A) conducts heat better.
  - Heat spreaders extend heat-transfer surface area of ICs when attached to the IC through a high k material. (e.g., PCB GND plane connected to IC by solder balls).
  - A PCB ground plane's thickness and width (cross- sectional surface area), number of layers and vias are critical items in reducing IC peak temperatures by spreading heat energy.
- A larger temperature differential (ΔT) across a smaller distance (Δx) conducts heat better.
  - In the device skin, ΔT is constrained by the maximum allowed skin touch temperature (T2).

Key message: *Conduction is THE primary heat transfer mechanism in mobile devices. Material type and area are key variables to increase conductive heat transfer.*

Thermal Concepts: Heat Spreaders Using Conductive Heat Transfer

Graphite-based heat spreader example:

- A 0.8 W heat source generated a 90°C hot-spot within seconds in the top image.
- SPREADERSHIELD™ flexible graphite (SS400-0.127-P1GP1A1) was applied in bottom image.
- Peak temperature was reduced by 26°C (90°C to 64°C) while allowing a 400% increase in power (~3.3 W).



Thermal images from a bare 0.8 W heat source vs. a 3.3 W heat source with SPREADERSHIELD

Key message: *A graphite heat spreader material uses conductive heat transfer to improve the overall heat capacity of a device.*

Questions?

Submit technical questions to https://support.cdmatech.com.