Qualcomm
TECHNOLOGIES, INC

PM8841 Power Management IC

Software Interface

80-NA554-2 Rev. A

February 2013

Confidential and Proprietary - Qualcomm Technologies, Inc.

Qualcomm Technologies, Inc.
5775 Morehouse Drive
San Diego, CA 92121
U.S.A.

Preface

Technical assistance

For assistance or clarification on information in this document, submit a case to Qualcomm CDMA Technologies at https://support.cdmatech.com/. If you do not have access to the CDMATech Support Service website, register for access or send email to support.cdmatech@qualcomm.com.

Revision history

Revision A, February 2013, initial release

Contents

1 PMIC Register Mapping

1.1 Addressing structure

Each PMIC consists of two slave IDs. Each slave ID has 64 K addresses, which are subdivided into 256 groups of 256 addresses. Each group is known as a peripheral. The map can support up to 512 peripherals because each PMIC has two slave IDs, but the MSM can only support up to 256 peripherals.

Splitting the map into 256 peripherals with 256 addresses provides a convenient way of subdividing the 16-bit register addresses. The top eight bits are the peripheral address and the bottom eight bits are the register offset. If there are two identical peripherals (for example, LDOs), they will have different peripheral IDs, but their registers will be located at the same register offset. The unique slave ID (USID) allows the MSM to access more peripherals by effectively increasing the available register map.

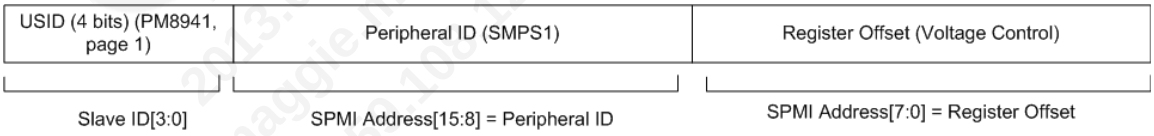


Figure 1-1 Addressing structure

Peripheral IDs are predefined and are specified.

1.2 Slave ID

Each PMIC has two unique slave IDs (USID).

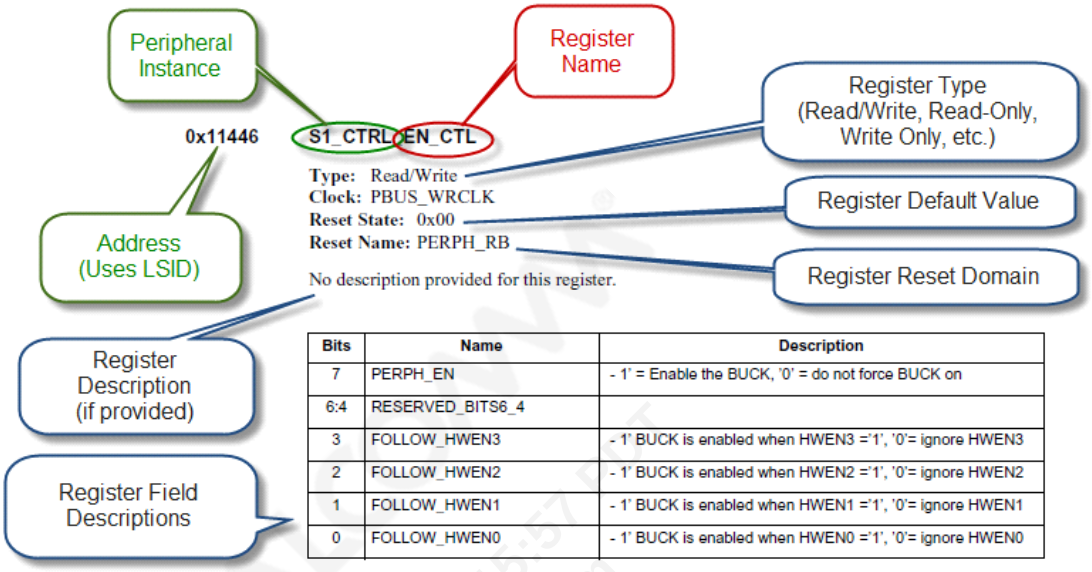
- USID 0 and 1 are reserved for the primary PMIC (i.e., the PM8941 device)
- USID 2 and 3 are reserved for a stand-alone Qualcomm PMIC charger
- USID 4 and 5 are reserved for the first slave PMIC (i.e., the PM8841 device)

Internally, the USID is translated into a local slave ID (LSID).

- The first USID maps to LSID 0
- The second USID maps to LSID 1

The PMIC can have up to four LSIDs, but the SPMI bus can address only the first two.

1.3 PMIC register maps



Bits	Name	Description
7	PERPH_EN	- 1' = Enable the BUCK, '0' = do not force BUCK on
6:4	RESERVED_BITS6_4	
3	FOLLOW_HWEN3	- 1' BUCK is enabled when HWEN3 ='1', '0'= ignore HWEN3
2	FOLLOW_HWEN2	- 1' BUCK is enabled when HWEN2 ='1', '0'= ignore HWEN2
1	FOLLOW_HWEN1	- 1' BUCK is enabled when HWEN1 ='1', '0'= ignore HWEN1
0	FOLLOW_HWEN0	- 1' BUCK is enabled when HWEN0 ='1', '0'= ignore HWEN0

Figure 1-2 PMIC register map

The address is broken down into LSID, PID, and register offset.

For example, in the address 0x11446:

- The unique slave ID is in red
- The peripheral ID is in green
- The register offset is in purple

The LSID is provided in all the register maps. In most applications, where the PMIC is accessed from the SPMI bus, the USID is used.

- For PM8941 add 0x00000 to the address (no change).
- For PM8841 add 0x40000 to the address.

1.4 Peripheral register map

Each peripheral has 256 registers that are subdivided into different sections.

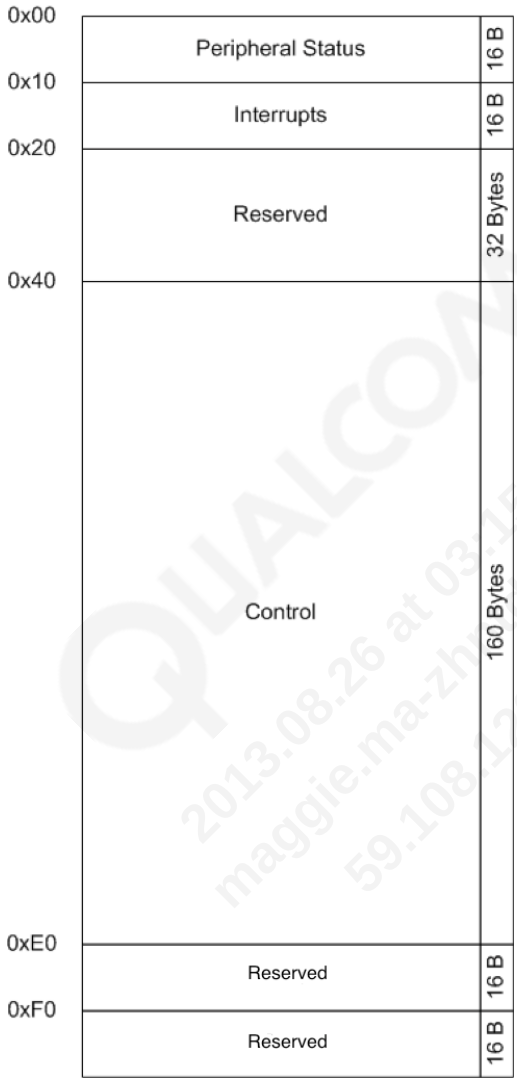


Figure 1-3 Peripheral register map

The subsections of the peripheral register map are

- Peripheral status
- Interrupts
- Control
- Reserved

1.5 Peripheral interrupts

The interrupts for each peripheral are in its peripheral register map. Each register is reserved for a different function. Each bit defines a different interrupt.

For example, bit 0 is reserved for the GPIO_IN interrupt:

- 0x10[0] holds the real-time status of the GPIO_IN interrupt
- 0x11[0] defines the type (level/edge) for GPIO_IN
- 0x12[0] defines the polarity for GPIO_IN

This setup reduces the number of transactions required to service interrupts. All real-time status bits for the interrupts in the module can be read with a single read of the INT_RT_STS register. Similarly, the latched interrupts status can be acquired with a single read of the INT_LATCHED_STS register.

Table 1-1 Sample interrupt register map

Addr_ offset	Register_name	Field_ MSB	Field_ LSB	Field_name	Default	Description
0x10	INT_RT_STS	1	1	GPIO_HI_RT_STS	0	Interrupt real time status bits
		0	0	GPIO_IN_RT_STS	0	
0x12	INT_POLARITY_HIGH	1	1	GPIO_HI_HIGH	0	1: Interrupt will trigger on a level high (rising edge) event 0: Level HIGH triggering is disabled
		0	0	GPIO_IN_HIGH	0	
0x13	INT_POLARITY_LOW	1	1	GPIO_HI_LOW	0	1: Interrupt will trigger on a level low (falling edge) event 0: Level low triggering is disabled
		0	0	GPIO_IN_LOW	0	
0x14	INT_LATCHED_CLR	1	1	GPIO_HI_LATCHED_CLR	0	Writing a 1 to this interrupt rearms the interrupt when an interrupt is pending. It clears the internal latched status.
		0	0	GPIO_IN_LATCHED_CLR	0	
0x15	INT_EN_SET	1	1	GPIO_HI_EN_SET	0	Writing 0 to this register has no effect. Writing a 1 enables the corresponding interrupt. Reading this register reads back enable status
		0	0	GPIO_IN_EN_SET	0	
0x16	INT_EN_CLR	1	1	GPIO_HI_EN_CLR	0	Writing 0 to this register has no effect. Writing a 1 disables the corresponding interrupt. Reading this register reads back enable status
		0	0	GPIO_IN_EN_CLR	0	
0x18	INT_LATCHED_STS	1	1	GPIO_HI_LATCHED_STS	0	Latched Interrupt. 1 indicates that the interrupt has triggered. When the latched bit is set it can only be cleared by writing the clear bit.
		0	0	GPIO_IN_LATCHED_STS	0	
0x19	INT_PENDING_STS	1	1	GPIO_HI_PENDING_STS	0	Pending is set if interrupt has been sent but not cleared.
		0	0	GPIO_IN_PENDING_STS	0	
0x1A	INT_MID_SEL	1	0	INT_MID_SEL	0	Selects the MID that will receive the interrupt
0x1B	INT_PRIORITY	0	0	INT_PRIORITY	0	SR = 0 A = 1

1.6 Interrupt configuration

1.6.1 Set and forget registers

- INT_MID_SEL – 0x00 for every peripheral because the MSM is the only master.
- INT_PRIORITY – The SPMI supports two levels of priority. Every interrupt uses low priority. No high priority use cases have been identified.

1.6.2 Enabling interrupts

Interrupts default to disabled. To enable an interrupt, set the TYPE, PRIORITY_HIGH, and PRORITY_LOW fields. Use read-modify-write to control these registers.

After the interrupts are configured, they can be enabled. INT_EN has two registers: INT_EN_SET and INT_EN_CLR. To set these registers:

- Enable the interrupt by setting the corresponding bit in INT_EN_SET.
- Disable the interrupt by setting the corresponding bit in INT_EN_CLR.

The INT_EN registers do not require read-modify-write. Writing 0 to these registers has no effect. Reading either register will read back the enable status.

1.6.3 Interrupt detection

Interrupts are sent to the master using the SPMI master write command. The interrupt message includes the peripheral ID and the interrupt that fired. All interrupt information is communicated to the MSM in one message.

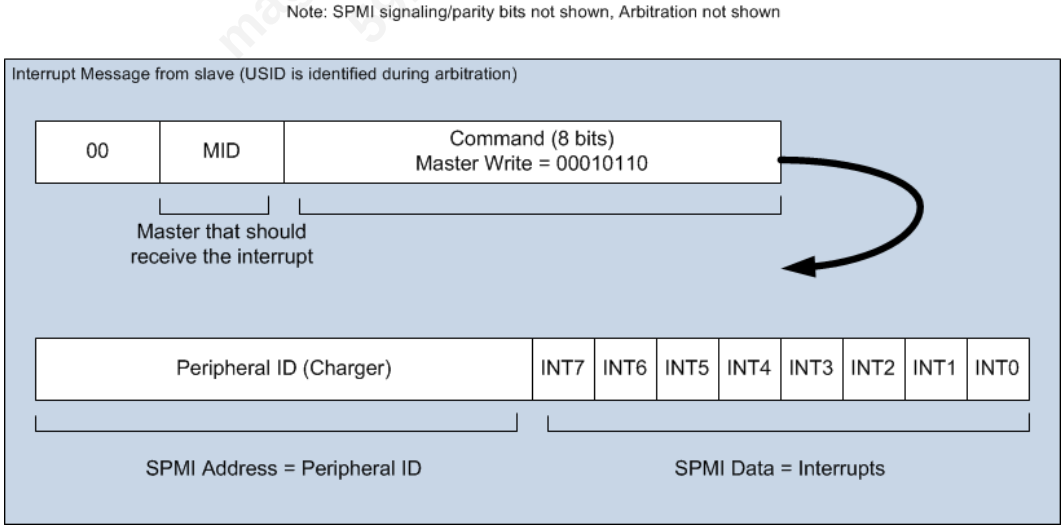


Figure 1-4 PMIC interrupt message

1.6.4 Clearing interrupts

Assume an interrupt is fired by GPIO_01 (peripheral id 0x25).

1. The interrupt is generated in the PMIC. The message is sent to the peripheral owner (i.e., RPM) via SPMI and the PMIC arbiter (in the MSM device). The message indicates that the interrupt came from GPIO_01 (PID = 0x25) and that the VREG_OK interrupt triggered.
2. Optional: The software does a 6-byte read starting at address 0x2510. The software can read status, type (level/edge), en_high, en_low, and enable state in a single read.
3. The software does a 1-byte write of 0x01 to register 0x2516 only to disable the interrupt.
4. The interrupt handler takes care of the interrupt.
5. When the software is ready, a 2-byte write of 0x0101 to 0x2514 clears the interrupt and then re-enables the interrupt.

2 REVID_REVID_PM8841

0x103 REVID_REVISION4

Type: read-only
Clock: PBUS_WRCLK
Reset State: 0x01
Reset Name: N/A

HW Version Register [31:24]

REVID_REVISION4

Bits	Name	Type	Description
7:0	ALL_LAYER	read-only	This number is incremented every time there is an all layer revision of the chip 0x01 = ES1 0x02 = ES2

0x104 REVID_PERPH_TYPE

Type: read-only
Clock: PBUS_WRCLK
Reset State: 0x51
Reset Name: N/A

Peripheral Type

REVID_PERPH_TYPE

Bits	Name	Type	Description
7:0	TYPE	read-only	REV_ID (This tells you that you are talking to a PMIC)

0x105 REVID_PERPH_SUBTYPE

Type: read-only
Clock: PBUS_WRCLK
Reset State: 0x02
Reset Name: N/A

Peripheral SubType

REVID_PERPH_SUBTYPE

Bits	Name	Type	Description
7:0	SUBTYPE	read-only	This is PM8841

0x108 REVID_STATUS1

Type: read-only
Clock: PBUS_WRCLK
Reset State: 0x00
Reset Name: N/A

Status Registers

REVID_STATUS1

Bits	Name	Type	Description
7:6	OP4	read-only	Option Pin State 11: VDD 10: HiZ 00: GND
5:4	OP3	read-only	Option Pin State 11: VDD 10: HiZ 00: GND
3:2	OP2	read-only	Option Pin State 11: VDD 10: HiZ 00: GND
1:0	OP1	read-only	Option Pin State 11: VDD 10: HiZ 00: GND

3 PON_PON

0x804 PON_PERPH_TYPE

Type: read-only
Clock: PBUS_WRCLK
Reset State: 0x01
Reset Name: N/A

Peripheral Type

PON_PERPH_TYPE

Bits	Name	Type	Description
7:0	TYPE	read-only	PON

0x805 PON_PERPH_SUBTYPE

Type: read-only
Clock: PBUS_WRCLK
Reset State: 0x01
Reset Name: N/A

Peripheral SubType

PON_PERPH_SUBTYPE

Bits	Name	Type	Description
7:0	SUBTYPE	read-only	PNP PON

0x807 PON_PON_PBL_STATUS

Type: read-only
Clock: PBUS_WRCLK
Reset State: Undefined
Reset Name: N/A

Stage 2 reset generation and register access error status.

PON_PON_PBL_STATUS

Bits	Name	Type	Description
7	DVDD_RB_OCCURRED	read-only	DVDD_RB was asserted during the last power cycle
6	XVDD_RB_OCCURRED	read-only	XVDD_RB was asserted during the last power cycle
5	REG_WRITE_ERROR	read-only	A register field write was attempted when a block was enabled. Writing to this address clears field.
4	REG_RESET_ERROR	read-only	A register field write was attempted when reset was asserted. Writing to this address clears field.
3	REG_SYNC_ERROR	read-only	Indicates a synchronized register field was over written before it's contents were latched by logic. Writing to this address clears field.,,,,'

0x808 PON_PON_REASON1

Type: read-only
Clock: PBUS_WRCLK
Reset State: Undefined
Reset Name: raw_xVdd_rb

Reasons that the PMIC left the off state. All zeros mean that no trigger received

PON_PON_REASON1

Bits	Name	Type	Description
7	KPDPWR_N	read-only	Triggered from new KPDPWR press
6	CBLPWR_N	read-only	Triggered from CBL_PWR1_N
5	PON1	read-only	Triggered from PON1
4	USB_CHG	read-only	Triggered from USB charger
3	DC_CHG	read-only	Triggered from DC charger

PON_PON_REASON1 (Continued)

Bits	Name	Type	Description
2	RTC	read-only	Triggered from RTC
1	SMPL	read-only	Triggered from SMPL
0	HARD_RESET	read-only	Triggered from a Hard Reset event (check POFF reason for the trigger)

0x80A PON_WARM_RESET_REASON1

Type: read-only
Clock: PBUS_WRCLK
Reset State: Undefined
Reset Name: raw_xVdd_rb

Reasons that PMIC entered the Warm Reset state (pst_13). This register is automatically reset when the PMIC turns on (i.e. PON_WARM_REASON_CLEAR register field 1) or by writing to this address.

PON_WARM_RESET_REASON1

Bits	Name	Type	Description
7	KPDPWR_N	read-only	Triggered by KPDPWR_N
6	RESIN_N	read-only	Triggered by RESIN_N
5	KPDPWR_AND_RESIN	read-only	Triggered by simultaneous KPDPWR_N + RESIN_N
4	GP2	read-only	Triggered by Keypad_Reset2
3	GP1	read-only	Triggered by Keypad_Reset1
2	PMIC_WD	read-only	Triggered by PMIC Watchdog
1	PS_HOLD	read-only	Triggered by PS_HOLD
0	SOFT	read-only	Triggered by Software

0x80B PON_WARM_RESET_REASON2

Type: read-only
Clock: PBUS_WRCLK
Reset State: Undefined
Reset Name: raw_xVdd_rb

Reasons that PMIC entered the Warm Reset state (pst_13). This register is automatically reset when the PMIC turns on (i.e. PON_WARM_REASON_CLEAR register field 1) or by writing to WARM_RESET_REASON1 register address.

PON_WARM_RESET_REASON2

Bits	Name	Type	Description
4	AFP	read-only	Triggered AFP

0x80C PON_POFF_REASON1

Type: read-only
Clock: PBUS_WRCLK
Reset State: Undefined
Reset Name: raw_xVdd_rb

Reasons that the PMIC left the on state and commenced a shutdown sequence. All zeros mean that no trigger received or a master bandgap or phone power fault occurred.

PON_POFF_REASON1

Bits	Name	Type	Description
7	KPDPWR_N	read-only	Triggered by KPDPWR_N
6	RESIN_N	read-only	Triggered by RESIN_N
5	KPDPWR_AND_RESIN	read-only	Triggered by simultaneous KPDPWR_N + RESIN_N
4	GP2	read-only	Triggered by Keypad_Reset2
3	GP1	read-only	Triggered by Keypad_Reset1
2	PMIC_WD	read-only	Triggered by PMIC Watchdog
1	PS_HOLD	read-only	Triggered by PS_HOLD
0	SOFT	read-only	Triggered by Software

0x80D PON_POFF_REASON2

Type: read-only
Clock: PBUS_WRCLK
Reset State: Undefined
Reset Name: raw_xVdd_rb

Reasons that the PMIC left the on state and commenced a shutdown sequence. All zeros mean that no trigger received or a master bandgap or phone power fault occurred.

PON_POFF_REASON2

Bits	Name	Type	Description
7	STAGE3	read-only	Triggered by stage3 reset
6	OTST3	read-only	Triggered by Overtemp
5	UVLO	read-only	Triggered by UVLO
4	AFP	read-only	Triggered AFP

0x80E PON_SOFT_RESET_REASON1

Type: read-only
Clock: PBUS_WRCLK
Reset State: Undefined
Reset Name: raw_xVdd_rb

Reasons that the PMIC registers were reset. All zeros mean that no trigger received. Clear the soft reason registers by writing to this register

PON_SOFT_RESET_REASON1

Bits	Name	Type	Description
7	KPDPWR_N	read-only	Triggered by KPDPWR_N
6	RESIN_N	read-only	Triggered by RESIN_N
5	KPDPWR_AND_RESIN	read-only	Triggered by simultaneous KPDPWR_N + RESIN_N
4	GP2	read-only	Triggered by Keypad_Reset2
3	GP1	read-only	Triggered by Keypad_Reset1

PON_SOFT_RESET_REASON1 (Continued)

Bits	Name	Type	Description
2	PMIC_WD	read-only	Triggered by PMIC Watchdog
1	PS_HOLD	read-only	Triggered by PS_HOLD
0	SOFT	read-only	Triggered by Software

0x80F PON_SOFT_RESET_REASON2

Type: read-only
Clock: PBUS_WRCLK
Reset State: Undefined
Reset Name: raw_xVdd_rb

Reasons that the PMIC registers were reset. All zeros mean that no trigger received. Clear the soft reason registers by writing to the SOFT_RESET_REASON1 register

PON_SOFT_RESET_REASON2

Bits	Name	Type	Description
4	AFP	read-only	Triggered AFP

0x810 PON_INT_RT_STS

Type: read-only
Clock: PBUS_WRCLK
Reset State: Undefined
Reset Name: N/A

Interrupt Real Time Status Bits

PON_INT_RT_STS

Bits	Name	Type	Description
6	PMIC_WD_BARK	read-only	warning that a reset event has been triggered by the PMIC Watchdog timer
5	K_R_BARK	read-only	warning that a reset event has been triggered by asserting RESIN_N and KPDPWR_N simultaneously
4	RESIN_BARK	read-only	warning that a reset event has been triggered by RESIN_N
3	KPDPWR_BARK	read-only	warning that a reset event has been triggered by KPDPWR_N

PON_INT_RT_STS (Continued)

Bits	Name	Type	Description
2	CBLPWR_ON	read-only	CBLPWR_N has changed states for longer than his debounce timer
1	RESIN_ON	read-only	RESIN_N has changed states for longer than his debounce timer
0	KPDPWR_ON	read-only	KPDPWR_N has changed states for longer than his debounce timer

0x811 PON_INT_SET_TYPE

Type: read-write
Clock: PBUS_WRCLK
Reset State: 0x00
Reset Name: perph_rb

0 = use level trigger interrupts, 1 = use edge trigger interrupts

PON_INT_SET_TYPE

Bits	Name	Type	Description
6	PMIC_WD_BARK	read-write	
5	K_R_BARK	read-write	
4	RESIN_BARK	read-write	
3	KPDPWR_BARK	read-write	
2	CBLPWR_ON	read-write	
1	RESIN_ON	read-write	
0	KPDPWR_ON	read-write	

0x812 PON_INT_POLARITY_HIGH

Type: read-write
Clock: PBUS_WRCLK
Reset State: 0x00
Reset Name: perph_rb

1= Interrupt will trigger on a level high (rising edge) event, 0 = level high triggering is disabled

PON_INT_POLARITY_HIGH

Bits	Name	Type	Description
6	PMIC_WD_BARK	read-write	
5	K_R_BARK	read-write	
4	RESIN_BARK	read-write	
3	KPDPWR_BARK	read-write	
2	CBLPWR_ON	read-write	
1	RESIN_ON	read-write	
0	KPDPWR_ON	read-write	

0x813 PON_INT_POLARITY_LOW

Type: read-write
Clock: PBUS_WRCLK
Reset State: 0x00
Reset Name: perph_rb

1' = Interrupt will trigger on a level low (falling edge) event, '0' = level low triggering is disabled

PON_INT_POLARITY_LOW

Bits	Name	Type	Description
6	PMIC_WD_BARK	read-write	
5	K_R_BARK	read-write	
4	RESIN_BARK	read-write	
3	KPDPWR_BARK	read-write	
2	CBLPWR_ON	read-write	
1	RESIN_ON	read-write	
0	KPDPWR_ON	read-write	

0x814 PON_INT_LATCHED_CLR

Type: write-only
Clock: PBUS_WRCLK
Reset State: 0x00
Reset Name: perph_rb

Writing a '1' to this interrupt will rearm the interrupt when an interrupt is pending. It clears the internal sticky and sent bits

PON_INT_LATCHED_CLR

Bits	Name	Type	Description
6	PMIC_WD_BARK	write-only	
5	K_R_BARK	write-only	
4	RESIN_BARK	write-only	
3	KPDPWR_BARK	write-only	
2	CBLPWR_ON	write-only	
1	RESIN_ON	write-only	
0	KPDPWR_ON	write-only	

0x815 PON_INT_EN_SET

Type: read-write
Clock: PBUS_WRCLK
Reset State: 0x00
Reset Name: perph_rb

Writing '0' to this register has no effect. Writing a '1' will enable the corresponding interrupt. Reading this register will readback enable status

PMIC_SET_MASK

PON_INT_EN_SET

Bits	Name	Type	Description
6	PMIC_WD_BARK	read-write	
5	K_R_BARK	read-write	

PON_INT_EN_SET (Continued)

Bits	Name	Type	Description
4	RESIN_BARK	read-write	
3	KPDPWR_BARK	read-write	
2	CBLPWR_ON	read-write	
1	RESIN_ON	read-write	
0	KPDPWR_ON	read-write	

0x816 PON_INT_EN_CLR

Type: read-write
Clock: PBUS_WRCLK
Reset State: 0x00
Reset Name: perph_rb

Writing '0' to this register has no effect. Writing a '1' will disable the corresponding interrupt. Reading this register will readback enable status

PMIC_CLR_MASK=INT_EN_SET

PON_INT_EN_CLR

Bits	Name	Type	Description
6	PMIC_WD_BARK	read-write	
5	K_R_BARK	read-write	
4	RESIN_BARK	read-write	
3	KPDPWR_BARK	read-write	
2	CBLPWR_ON	read-write	
1	RESIN_ON	read-write	
0	KPDPWR_ON	read-write	

0x818 PON_INT_LATCHED_STS

Type: read-only
Clock: PBUS_WRCLK
Reset State: Undefined
Reset Name: N/A

Debug: Latched (Sticky) Interrupt. '1' indicates that the interrupt has triggered. Once the latched bit is set it can only be cleared by writing the clear bit.

PON_INT_LATCHED_STS

Bits	Name	Type	Description
6	PMIC_WD_BARK	read-only	
5	K_R_BARK	read-only	
4	RESIN_BARK	read-only	
3	KPDPWR_BARK	read-only	
2	CBLPWR_ON	read-only	
1	RESIN_ON	read-only	
0	KPDPWR_ON	read-only	

0x819 PON_INT_PENDING_STS

Type: read-only
Clock: PBUS_WRCLK
Reset State: Undefined
Reset Name: N/A

Debug: Pending is set if interrupt has been sent but not cleared.

PON_INT_PENDING_STS

Bits	Name	Type	Description
6	PMIC_WD_BARK	read-only	
5	K_R_BARK	read-only	
4	RESIN_BARK	read-only	

PON_INT_PENDING_STS (Continued)

Bits	Name	Type	Description
3	KPDPWR_BARK	read-only	
2	CBLPWR_ON	read-only	
1	RESIN_ON	read-only	
0	KPDPWR_ON	read-only	

0x81A PON_INT_MID_SEL

Type: read-write
Clock: PBUS_WRCLK
Reset State: 0x00
Reset Name: perph_rb

Selects the MID that will receive the interrupt

PON_INT_MID_SEL

Bits	Name	Type	Description
1:0	INT_MID_SEL	read-write	

0x81B PON_INT_PRIORITY

Type: read-write
Clock: PBUS_WRCLK
Reset State: 0x00
Reset Name: perph_rb

SR=0 A=1

PON_INT_PRIORITY

Bits	Name	Type	Description
0	INT_PRIORITY	read-write	

0x840 PON_KPDPWR_N_RESET_S1_TIMER

Type: read-write
Clock: PBUS_WRCLK
Reset State: 0x0F
Reset Name: soft_dVdd_rb

Stage 1 (Bark) Timer. Bark cannot be disabled, but interrupt can be disabled if necessary

PON_KPDPWR_N_RESET_S1_TIMER

Bits	Name	Type	Description
3:0	S1_TIMER	read-write	Time that the debounced trigger must be held before bark is sent to MSM -- 0: 0 ms 1: 32 ms 2: 56 ms 3: 80 ms 4: 128 ms 5: 184 ms 6: 272 ms 7: 408 ms 8: 608 ms 9: 904 ms 10: 1352 ms 11: 2048 ms 12: 3072 ms 13: 4480 ms 14: 6720 ms 15: 10256 ms This field can only be updated when block is disabled (i.e. 10 sleep clock cycles after writing 0 to S2_RESET_EN and PON_TRIGGER_EN:KPDPWR_N fields).

0x841 PON_KPDPWR_N_RESET_S2_TIMER

Type: read-write
Clock: PBUS_WRCLK
Reset State: 0x07
Reset Name: soft_dVdd_rb

Stage 2 (bite) configuration

PON_KPDPWR_N_RESET_S2_TIMER

Bits	Name	Type	Description
2:0	S2_TIMER	read-write	Time that debounced trigger must be held before S2 reset occurs {0ms, 10ms, 50ms, 100ms, 250ms, 500ms, 1s, 2s} This field can only be updated when block is disabled (i.e. 10 sleep clock cycles after writing 0 to S2_RESET_EN field).

0x842 PON_KPDPWR_N_RESET_S2_CTL

Type: read-write
Clock: PBUS_WRCLK
Reset State: 0x04
Reset Name: soft_dVdd_rb

Stage 2 (bite) configuration

PON_KPDPWR_N_RESET_S2_CTL

Bits	Name	Type	Description
7	S2_RESET_EN	read-write	Enable Stage 2 reset
3:0	RESET_TYPE	read-write	0000 = Reserved for soft reset, 0001 = warm reset, 0010 = Reserved for immediate xVdd shutdown 0011 = Reserved (default to xVdd Shutdown) 0100 = Shutdown (Normal Shutdown) 0101 = dVdd Shutdown (Shutdown + dVdd_rb), 0110 = xVdd Shutdown (Shutdown + dVdd_rb + xVdd_rb), 0111 = Hard reset (Shutdown + Automatic power up) 1000 = Reserved for dVdd Hard reset (Shutdown + dVdd_rb + Automatic power up), 1001 = Reserved for xVdd Hard reset (Shutdown + dVdd_rb + xVdd_rb+ Automatic power up), 1010 = Reserved for warm reset + dvdd shutdown 1011 = Reserved for warm reset + xVdd shutdown 1100 = Reserved for warm reset + Shutdown 1101 = Reserved for warm reset then Hard reset 1110 = Reserved for warm reset then dVdd Hard reset 1111 = Reserved for warm reset then xVdd Hard reset This field can only be updated when block is disabled (i.e. 10 sleep clock cycles after writing 0 to S2_RESET_EN field).

0x844 PON_RESIN_N_RESET_S1_TIMER

Type: read-write
Clock: PBUS_WRCLK
Reset State: 0x0F
Reset Name: soft_dVdd_rb

Stage 1 (Bark) Timer. Bark cannot be disabled, but interrupt can be disabled if necessary

PON_RESIN_N_RESET_S1_TIMER

Bits	Name	Type	Description
3:0	S1_TIMER	read-write	Time that the debounced trigger must be held before bark is sent to MSM -- 0: 0 ms 1: 32 ms 2: 56 ms 3: 80 ms 4: 128 ms 5: 184 ms 6: 272 ms 7: 408 ms 8: 608 ms 9: 904 ms 10: 1352 ms 11: 2048 ms 12: 3072 ms 13: 4480 ms 14: 6720 ms 15: 10256 ms This field can only be updated when block is disabled (i.e. 10 sleep clock cycles after writing 0 to S2_RESET_EN field).

0x845 PON_RESIN_N_RESET_S2_TIMER

Type: read-write
Clock: PBUS_WRCLK
Reset State: 0x07
Reset Name: soft_dVdd_rb

Stage 2 (bite) configuration

PON_RESIN_N_RESET_S2_TIMER

Bits	Name	Type	Description
2:0	S2_TIMER	read-write	Time that debounced trigger must be held before S2 reset occurs {0ms, 10ms, 50ms, 100ms, 250ms, 500ms, 1s, 2s} This field can only be updated when block is disabled (i.e. 10 sleep clock cycles after writing 0 to S2_RESET_EN field).

0x846 PON_RESIN_N_RESET_S2_CTL

Type: read-write
Clock: PBUS_WRCLK
Reset State: 0x04
Reset Name: soft_dVdd_rb

Stage 2 (bite) configuration

PON_RESIN_N_RESET_S2_CTL

Bits	Name	Type	Description
7	S2_RESET_EN	read-write	Enable Stage 2 reset
3:0	RESET_TYPE	read-write	0000 = Reserved for soft reset, 0001 = warm reset, 0010 = Reserved for immediate xVdd shutdown 0011 = Reserved (default to xVdd Shutdown) 0100 = Shutdown (Normal Shutdown) 0101 = dVdd Shutdown (Shutdown + dVdd_rb), 0110 = xVdd Shutdown (Shutdown + dVdd_rb + xVdd_rb), 0111 = Hard reset (Shutdown + Automatic power up) 1000 = Reserved for dVdd Hard reset (Shutdown + dVdd_rb + Automatic power up), 1001 = Reserved for xVdd Hard reset (Shutdown + dVdd_rb + xVdd_rb+ Automatic power up), 1010 = Reserved for warm reset + dvdd shutdown 1011 = Reserved for warm reset + xVdd shutdown 1100 = Reserved for warm reset + Shutdown 1101 = Reserved for warm reset then Hard reset 1110 = Reserved for warm reset then dVdd Hard reset 1111 = Reserved for warm reset then xVdd Hard reset This field can only be updated when block is disabled (i.e. 10 sleep clock cycles after writing 0 to S2_RESET_EN field).

0x848 PON_RESIN_AND_KPDPWR_RESET_S1_TIMER

Type: read-write
Clock: PBUS_WRCLK
Reset State: 0x0F
Reset Name: soft_dVdd_rb

Stage 1 (Bark) Timer. Bark cannot be disabled, but interrupt can be disabled if necessary

PON_RESIN_AND_KPDPWR_RESET_S1_TIMER

Bits	Name	Type	Description
3:0	S1_TIMER	read-write	Time that the debounced trigger must be held before bark is sent to MSM -- 0: 0 ms 1: 32 ms 2: 56 ms 3: 80 ms 4: 128 ms 5: 184 ms 6: 272 ms 7: 408 ms 8: 608 ms 9: 904 ms 10: 1352 ms 11: 2048 ms 12: 3072 ms 13: 4480 ms 14: 6720 ms 15: 10256 ms This field can only be updated when block is disabled (i.e. 10 sleep clock cycles after writing 0 to S2_RESET_EN field).

0x849 PON_RESIN_AND_KPDPWR_RESET_S2_TIMER

Type: read-write
Clock: PBUS_WRCLK
Reset State: 0x07
Reset Name: soft_dVdd_rb

Stage 2 (bite) configuration

PON_RESIN_AND_KPDPWR_RESET_S2_TIMER

Bits	Name	Type	Description
2:0	S2_TIMER	read-write	Time that debounced trigger must be held before S2 reset occurs {0ms, 10ms, 50ms, 100ms, 250ms, 500ms, 1s, 2s} This field can only be updated when block is disabled (i.e. 10 sleep clock cycles after writing 0 to S2_RESET_EN field).

0x84A PON_RESIN_AND_KPDPWR_RESET_S2_CTL

Type: read-write
Clock: PBUS_WRCLK
Reset State: 0x04
Reset Name: soft_dVdd_rb

Stage 2 (bite) configuration

PON_RESIN_AND_KPDPWR_RESET_S2_CTL

Bits	Name	Type	Description
7	S2_RESET_EN	read-write	Enable Stage 2 reset
3:0	RESET_TYPE	read-write	0000 = Reserved for soft reset, 0001 = warm reset, 0010 = Reserved for immediate xVdd shutdown 0011 = Reserved (default to xVdd Shutdown) 0100 = Shutdown (Normal Shutdown) 0101 = dVdd Shutdown (Shutdown + dVdd_rb), 0110 = xVdd Shutdown (Shutdown + dVdd_rb + xVdd_rb), 0111 = Hard reset (Shutdown + Automatic power up) 1000 = Reserved for dVdd Hard reset (Shutdown + dVdd_rb + Automatic power up), 1001 = Reserved for xVdd Hard reset (Shutdown + dVdd_rb + xVdd_rb+ Automatic power up), 1010 = Reserved for warm reset + dvdd shutdown 1011 = Reserved for warm reset + xVdd shutdown 1100 = Reserved for warm reset + Shutdown 1101 = Reserved for warm reset then Hard reset 1110 = Reserved for warm reset then dVdd Hard reset 1111 = Reserved for warm reset then xVdd Hard reset This field can only be updated when block is disabled (i.e. 10 sleep clock cycles after writing 0 to S2_RESET_EN field).

0x84C PON_GP2_RESET_S1_TIMER

Type: read-write
Clock: PBUS_WRCLK
Reset State: 0x0F
Reset Name: soft_dVdd_rb

Stage 1 (Bark) Timer. Bark cannot be disabled, but interrupt can be disabled if necessary

PON_GP2_RESET_S1_TIMER

Bits	Name	Type	Description
3:0	S1_TIMER	read-write	Time that the debounced trigger must be held before bark is sent to MSM -- 0: 0 ms 1: 32 ms 2: 56 ms 3: 80 ms 4: 128 ms 5: 184 ms 6: 272 ms 7: 408 ms 8: 608 ms 9: 904 ms 10: 1352 ms 11: 2048 ms 12: 3072 ms 13: 4480 ms 14: 6720 ms 15: 10256 ms This field can only be updated when block is disabled (i.e. 10 sleep clock cycles after writing 0 to S2_RESET_EN field).

0x84D PON_GP2_RESET_S2_TIMER

Type: read-write
Clock: PBUS_WRCLK
Reset State: 0x07
Reset Name: soft_dVdd_rb

Stage 2 (bite) configuration

PON_GP2_RESET_S2_TIMER

Bits	Name	Type	Description
2:0	S2_TIMER	read-write	Time that debounced trigger must be held before S2 reset occurs {0ms, 10ms, 50ms, 100ms, 250ms, 500ms, 1s, 2s} This field can only be updated when block is disabled (i.e. 10 sleep clock cycles after writing 0 to S2_RESET_EN field).

0x84E PON_GP2_RESET_S2_CTL

Type: read-write
Clock: PBUS_WRCLK
Reset State: 0x04
Reset Name: soft_dVdd_rb

Stage 2 (bite) configuration

PON_GP2_RESET_S2_CTL

Bits	Name	Type	Description
7	S2_RESET_EN	read-write	Enable Stage 2 reset
3:0	RESET_TYPE	read-write	0000 = Reserved soft reset, 0001 = warm reset, 0010 = Reserved for immediate xVdd shutdown 0011 = Reserved (default to xVdd Shutdown) 0100 = Shutdown (Normal Shutdown) 0101 = dVdd Shutdown (Shutdown + dVdd_rb), 0110 = xVdd Shutdown (Shutdown + dVdd_rb + xVdd_rb), 0111 = Hard reset (Shutdown + Automatic power up) 1000 = Reserved for dVdd Hard reset (Shutdown + dVdd_rb + Automatic power up), 1001 = Reserved for xVdd Hard reset (Shutdown + dVdd_rb + xVdd_rb+ Automatic power up), 1010 = Reserved for warm reset + dvdd shutdown 1011 = Reserved for warm reset + xVdd shutdown 1100 = Reserved for warm reset + Shutdown 1101 = Reserved for warm reset then Hard reset 1110 = Reserved for warm reset then dVdd Hard reset 1111 = Reserved for warm reset then xVdd Hard reset This field can only be updated when block is disabled (i.e. 10 sleep clock cycles after writing 0 to S2_RESET_EN field).

0x850 PON_GP1_RESET_S1_TIMER

Type: read-write
Clock: PBUS_WRCLK
Reset State: 0x0F
Reset Name: soft_dVdd_rb

Stage 1 (Bark) Timer. Bark cannot be disabled, but interrupt can be disabled if necessary

PON_GP1_RESET_S1_TIMER

Bits	Name	Type	Description
3:0	S1_TIMER	read-write	Time that the debounced trigger must be held before bark is sent to MSM -- 0: 0 ms 1: 32 ms 2: 56 ms 3: 80 ms 4: 128 ms 5: 184 ms 6: 272 ms 7: 408 ms 8: 608 ms 9: 904 ms 10: 1352 ms 11: 2048 ms 12: 3072 ms 13: 4480 ms 14: 6720 ms 15: 10256 ms This field can only be updated when block is disabled (i.e. 10 sleep clock cycles after writing 0 to S2_RESET_EN field).

0x851 PON_GP1_RESET_S2_TIMER

Type: read-write
Clock: PBUS_WRCLK
Reset State: 0x07
Reset Name: soft_dVdd_rb

Stage 2 (bite) configuration

PON_GP1_RESET_S2_TIMER

Bits	Name	Type	Description
2:0	S2_TIMER	read-write	Time that debounced trigger must be held before S2 reset occurs {0ms, 10ms, 50ms, 100ms, 250ms, 500ms, 1s, 2s} This field can only be updated when block is disabled (i.e. 10 sleep clock cycles after writing 0 to S2_RESET_EN field).

0x852 PON_GP1_RESET_S2_CTL

Type: read-write
Clock: PBUS_WRCLK
Reset State: 0x04
Reset Name: soft_dVdd_rb

Stage 2 (bite) configuration

PON_GP1_RESET_S2_CTL

Bits	Name	Type	Description
7	S2_RESET_EN	read-write	Enable Stage 2 reset
3:0	RESET_TYPE	read-write	0000 = Reserved for soft reset, 0001 = warm reset, 0010 = Reserved for immediate xVdd shutdown 0011 = Reserved (default to xVdd Shutdown) 0100 = Shutdown (Normal Shutdown) 0101 = dVdd Shutdown (Shutdown + dVdd_rb), 0110 = xVdd Shutdown (Shutdown + dVdd_rb + xVdd_rb), 0111 = Hard reset (Shutdown + Automatic power up) 1000 = Reserved for dVdd Hard reset (Shutdown + dVdd_rb + Automatic power up), 1001 = Reserved for xVdd Hard reset (Shutdown + dVdd_rb + xVdd_rb+ Automatic power up), 1010 = Reserved for warm reset + dvdd shutdown 1011 = Reserved for warm reset + xVdd shutdown 1100 = Reserved for warm reset + Shutdown 1101 = Reserved for warm reset then Hard reset 1110 = Reserved for warm reset then dVdd Hard reset 1111 = Reserved for warm reset then xVdd Hard reset This field can only be updated when block is disabled (i.e. 10 sleep clock cycles after writing 0 to S2_RESET_EN field).

0x854 PON_PMIC_WD_RESET_S1_TIMER

Type: read-write
Clock: PBUS_WRCLK
Reset State: 0x1F
Reset Name: soft_dVdd_rb

Stage 1 (Bark) Timer. Bark cannot be disabled, but interrupt can be disabled if necessary

PON_PMIC_WD_RESET_S1_TIMER

Bits	Name	Type	Description
6:0	S1_TIMER	read-write	Time that the debounced trigger must be held before bark is sent to MSM (seconds) -- 0 ? 127 seconds, default 31 seconds. Program hex value of decimal count desired (not binary coded). This field can only be updated when block is disabled (i.e. 10 sleep clock cycles after writing 0 to S2_RESET_EN field).

0x855 PON_PMIC_WD_RESET_S2_TIMER

Type: read-write
Clock: PBUS_WRCLK
Reset State: 0x01
Reset Name: soft_dVdd_rb

Stage 2 (bite) configuration

PON_PMIC_WD_RESET_S2_TIMER

Bits	Name	Type	Description
6:0	S2_TIMER	read-write	Time that debounced trigger must be held before S2 reset occurs -- 0 ? 127 seconds (default = 32 seconds). Program hex value of decimal count desired (Not binary coded). Timer starts after WD bark expires This field can only be updated when block is disabled (i.e. 10 sleep clock cycles after writing 0 to S2_RESET_EN field).

0x856 PON_PMIC_WD_RESET_S2_CTL

Type: read-write
Clock: PBUS_WRCLK
Reset State: 0x86
Reset Name: soft_dVdd_rb

Stage 2 (bite) configuration

PON_PMIC_WD_RESET_S2_CTL

Bits	Name	Type	Description
7	S2_RESET_EN	read-write	Enable Stage 2 reset
3:0	RESET_TYPE	read-write	0000 = Reserved for soft reset, 0001 = warm reset, 0010 = Reserved for immediate xVdd shutdown 0011 = Reserved (default to xVdd Shutdown) 0100 = Shutdown (Normal Shutdown) 0101 = dVdd Shutdown (Shutdown + dVdd_rb), 0110 = xVdd Shutdown (Shutdown + dVdd_rb + xVdd_rb), 0111 = Hard reset (Shutdown + Automatic power up) 1000 = Reserved for dVdd Hard reset (Shutdown + dVdd_rb + Automatic power up), 1001 = Reserved for xVdd Hard reset (Shutdown + dVdd_rb + xVdd_rb+ Automatic power up), 1010 = Reserved for warm reset + dvdd shutdown 1011 = Reserved for warm reset + xVdd shutdown 1100 = Reserved for warm reset + Shutdown 1101 = Reserved for warm reset then Hard reset 1110 = Reserved for warm reset then dVdd Hard reset 1111 = Reserved for warm reset then xVdd Hard reset This field can only be updated when block is disabled (i.e. 10 sleep clock cycles after writing 0 to S2_RESET_EN field).

0x857 PON_PMIC_WD_RESET_PET

Type: write-only
Clock: PBUS_WRCLK
Reset State: 0x00
Reset Name: soft_dVdd_rb

Stage 2 (bite) configuration

PON_PMIC_WD_RESET_PET

Bits	Name	Type	Description
0	WATCHDOG_PET	write-only	Writing '1' to this bit will clear the PMIC WD timer. Writing '0' has no effect.

0x85A PON_PS_HOLD_RESET_CTL

Type: read-write
Clock: PBUS_WRCLK
Reset State: 0x84
Reset Name: soft_dVdd_rb

PON_PS_HOLD_RESET_CTL

Bits	Name	Type	Description
7	S2_RESET_EN	read-write	Enable reset
3:0	RESET_TYPE	read-write	0000 = Reserved for soft reset, 0001 = warm reset, 0010 = Reserved for immediate xVdd shutdown 0011 = Reserved (default to xVdd Shutdown) 0100 = Shutdown (Normal Shutdown) 0101 = dVdd Shutdown (Shutdown + dVdd_rb), 0110 = xVdd Shutdown (Shutdown + dVdd_rb + xVdd_rb), 0111 = Hard reset (Shutdown + Automatic power up) 1000 = Reserved for dVdd Hard reset (Shutdown + dVdd_rb + Automatic power up), 1001 = Reserved for xVdd Hard reset (Shutdown + dVdd_rb + xVdd_rb+ Automatic power up), 1010 = Reserved for warm reset + dvdd shutdown 1011 = Reserved for warm reset + xVdd shutdown 1100 = Reserved for warm reset + Shutdown 1101 = Reserved for warm reset then Hard reset 1110 = Reserved for warm reset then dVdd Hard reset 1111 = Reserved for warm reset then xVdd Hard reset This field can only be updated when block is disabled (i.e. 10 sleep clock cycles after writing 0 to S2_RESET_EN field).

0x862 PON_SW_RESET_S2_CTL

Type: read-write
Clock: PBUS_WRCLK
Reset State: 0x00
Reset Name: soft_dVdd_rb

Software initiated shutdown (AFP)

PON_SW_RESET_S2_CTL

Bits	Name	Type	Description
7	SW_RESET_EN	read-write	Enable SW reset

PON_SW_RESET_S2_CTL (Continued)

Bits	Name	Type	Description
3:0	RESET_TYPE	read-write	0000 = soft reset, 0001 = warm reset, 0010 = Reserved for immediate xVdd shutdown 0011 = Reserved (default to xVdd Shutdown) 0100 = Shutdown (Normal Shutdown) 0101 = dVdd Shutdown (Shutdown + dVdd_rb), 0110 = xVdd Shutdown (Shutdown + dVdd_rb + xVdd_rb), 0111 = Hard reset (Shutdown + Automatic power up) 1000 = Reserved for dVdd Hard reset (Shutdown + dVdd_rb + Automatic power up), 1001 = Reserved for xVdd Hard reset (Shutdown + dVdd_rb + xVdd_rb+ Automatic power up), 1010 = Reserved for warm reset + dvdd shutdown 1011 = Reserved for warm reset + xVdd shutdown 1100 = Reserved for warm reset + Shutdown 1101 = Reserved for warm reset then Hard reset 1110 = Reserved for warm reset then dVdd Hard reset 1111 = Reserved for warm reset then xVdd Hard reset This field can only be updated when block is disabled (i.e. 10 sleep clock cycles after writing 0 to SW_RESET_EN field).

0x863 PON_SW_RESET_GO

Type: write-only
Clock: PBUS_WRCLK
Reset State: 0x00
Reset Name: soft_dVdd_rb

Initiate SW Reset by writing 0xA5 to this register

PON_SW_RESET_GO

Bits	Name	Type	Description
7:0	SW_RESET_GO	write-only	Initiate SW Reset by writing 0xA5 to this register

0x866 PON_OVERTEMP_RESET_CTL

Type: read-write
Clock: PBUS_WRCLK
Reset State: 0x84
Reset Name: soft_dVdd_rb

PON_OVERTEMP_RESET_CTL

Bits	Name	Type	Description
7	S2_RESET_EN	read-write	Enable stage 2 reset
3:0	RESET_TYPE	read-write	0000 = Reserved for soft reset, 0001 = warm reset, 0010 = Reserved for immediate xVdd shutdown 0011 = Reserved (default to xVdd Shutdown) 0100 = Shutdown (Normal Shutdown) 0101 = dVdd Shutdown (Shutdown + dVdd_rb), 0110 = xVdd Shutdown (Shutdown + dVdd_rb + xVdd_rb), 0111 = Hard reset (Shutdown + Automatic power up) 1000 = Reserved for dVdd Hard reset (Shutdown + dVdd_rb + Automatic power up), 1001 = Reserved for xVdd Hard reset (Shutdown + dVdd_rb + xVdd_rb+ Automatic power up), 1010 = Reserved for warm reset + dvdd shutdown 1011 = Reserved for warm reset + xVdd shutdown 1100 = Reserved for warm reset + Shutdown 1101 = Reserved for warm reset then Hard reset 1110 = Reserved for warm reset then dVdd Hard reset 1111 = Reserved for warm reset then xVdd Hard reset This field can only be updated when block is disabled (i.e. 10 sleep clock cycles after writing 0 to S2_RESET_EN field).

0x86A PON_AFP_RESET_CTL

Type: read-write
Clock: PBUS_WRCLK
Reset State: 0x04
Reset Name: soft_dVdd_rb

PON_AFP_RESET_CTL

Bits	Name	Type	Description
7	S2_RESET_EN	read-write	Enable stage 2reset

PON_AFP_RESET_CTL (Continued)

Bits	Name	Type	Description
3:0	RESET_TYPE	read-write	0000 = Reserved for soft reset, 0001 = warm reset, 0010 = Reserved for immediate xVdd shutdown 0011 = Reserved (default to xVdd Shutdown) 0100 = Shutdown (Normal Shutdown) 0101 = dVdd Shutdown (Shutdown + dVdd_rb), 0110 = xVdd Shutdown (Shutdown + dVdd_rb + xVdd_rb), 0111 = Hard reset (Shutdown + Automatic power up) 1000 = Reserved for dVdd Hard reset (Shutdown + dVdd_rb + Automatic power up), 1001 = Reserved for xVdd Hard reset (Shutdown + dVdd_rb + xVdd_rb+ Automatic power up), 1010 = Reserved for warm reset + dvdd shutdown 1011 = Reserved for warm reset + xVdd shutdown 1100 = Reserved for warm reset + Shutdown 1101 = Reserved for warm reset then Hard reset 1110 = Reserved for warm reset then dVdd Hard reset 1111 = Reserved for warm reset then xVdd Hard reset This field can only be updated when block is disabled (i.e. 10 sleep clock cycles after writing 0 to S2_RESET_EN field).

0x870 PON_PULL_CTL

Type: read-write
Clock: PBUS_WRCLK
Reset State: 0x0F
Reset Name: soft_dVdd_rb

PON_PULL_CTL

Bits	Name	Type	Description
3	PON1_PD_EN	read-write	
2	CBLPWR_N_PU_EN	read-write	
1	KPDPWR_N_PU_EN	read-write	
0	RESIN_N_PU_EN	read-write	

0x871 PON_DEBOUNCE_CTL

Type: read-write
Clock: PBUS_WRCLK
Reset State: 0x00
Reset Name: soft_dVdd_rb

PON_DEBOUNCE_CTL

Bits	Name	Type	Description
2:0	DEBOUNCE	read-write	KPD/CBL/GP_DLY/RESIN/RESIN_AND_KPD/GP1/GP2: Time delay for KPD, CBL, General Purpose PON, RESIN, RESIN_AND_KPD, GP1 and GP2 state change interrupt and triggering. Delay = (1/1024)* 2^ (x+4) This is a synchronized field. For reliable hardware operation, the minimum time allowed between write accesses is 10 sleep clock cycles.

0x875 PON_RESET_S3_TIMER

Type: read-write
Clock: PBUS_WRCLK
Reset State: 0x06
Reset Name: raw_xVdd_rb

Time that debounced trigger must be held before S3 reset occurs (seconds)

PON_RESET_S3_TIMER

Bits	Name	Type	Description
2:0	S3_TIMER	read-write	Time that debounced trigger must be held before S3 reset occurs. 000 = Instant, else 2^(x) seconds (2 to 128) This is a synchronized field. For reliable hardware operation, the minimum time allowed between write accesses is 10 sleep clock cycles.

0x880 PON_PON_TRIGGER_EN

Type: read-write
Clock: PBUS_WRCLK
Reset State: 0xF8
Reset Name: soft_dVdd_rb

Power on trigger enables.

PON_PON_TRIGGER_EN

Bits	Name	Type	Description
7	KPDPWR_N	read-write	Enable PON trigger for new KPDPWR press
6	CBLPWR_N	read-write	Enable PON trigger for CBL_PWR_N
5	PON1	read-write	Enable PON trigger for PON1
4	USB_CHG	read-write	Enable PON trigger for USB CHG
3	DC_CHG	read-write	Enable PON trigger for DC CHG
2	RTC	read-write	Enable PON trigger for RTC
1	SMPL	read-write	Enable PON trigger for SMPL

0x888 PON_UVLO

Type: read-write
Clock: PBUS_WRCLK
Reset State: 0x05
Reset Name: soft_dVdd_rb

UVLO Delay

PON_UVLO

Bits	Name	Type	Description
2:0	UVLO_DLY	read-write	Time delay for UVLO detection. if X = 0 then delay = 0, else delay = (1/1024) seconds * 2 X-1 where X = value of bits <2:0> This is a synchronized field. For reliable hardware operation, the minimum time allowed between write accesses is 10 sleep clock cycles.

0x88C PON_PERPH_RB_SPARE

Type: read-write
Clock: PBUS_WRCLK
Reset State: 0x00
Reset Name: perph_rb

Extra registers for SW to keep information through resets

PON_PERPH_RB_SPARE

Bits	Name	Type	Description
7:0	SPARE	read-write	SPARE registers for SW

0x88D PON_DVDD_RB_SPARE

Type: read-write
Clock: PBUS_WRCLK
Reset State: 0x00
Reset Name: dVdd_rb

Extra registers for SW to keep information through resets

PON_DVDD_RB_SPARE

Bits	Name	Type	Description
7:0	SPARE	read-write	SPARE registers for SW

0x88E PON_XVDD_RB_SPARE

Type: read-write
Clock: PBUS_WRCLK
Reset State: 0x00
Reset Name: xVdd_rb

Extra registers for SW to keep information through resets

PON_XVDD_RB_SPARE

Bits	Name	Type	Description
7:0	SPARE	read-write	SPARE registers for SW

0x88F PON_SOFT_RB_SPARE

Type: read-write
Clock: PBUS_WRCLK
Reset State: 0x00
Reset Name: soft_dVdd_rb

Extra registers for SW to keep information through resets

PON_SOFT_RB_SPARE

Bits	Name	Type	Description
7:0	SPARE	read-write	SPARE registers for SW

0x890 PON_PON1_INTERFACE

Type: read-write
Clock: PBUS_WRCLK
Reset State: 0x00
Reset Name: shutdown2_rb

PON module interface signalling.

PON_PON1_INTERFACE

Bits	Name	Type	Description
7	PON_OUT	read-write	Field drives primary PMIC PON output buffer input.

4 TEMP_ALARM_TEMP_ALARM

0x2404 TEMP_ALARM_PERPH_TYPE

Type: read-only
Clock: PBUS_WRCLK
Reset State: 0x09
Reset Name: N/A

Peripheral Type

TEMP_ALARM_PERPH_TYPE

Bits	Name	Type	Description
7:0	TYPE	read-only	Alarm

0x2405 TEMP_ALARM_PERPH_SUBTYPE

Type: read-only
Clock: PBUS_WRCLK
Reset State: 0x08
Reset Name: N/A

Peripheral SubType

TEMP_ALARM_PERPH_SUBTYPE

Bits	Name	Type	Description
7:0	SUBTYPE	read-only	Temp Alarm

0x2408 TEMP_ALARM_STATUS1

Type: read-only
Clock: PBUS_WRCLK
Reset State: 0x00
Reset Name: N/A

Status Registers

TEMP_ALARM_STATUS1

Bits	Name	Type	Description
7	TEMP_ALARM_OK	read-only	1: TEMP ALARM enabled 0: TEMP ALARM disabled
3	ST3_SHUTDOWN_STS	read-only	Stage 3 shutdown occurred, writing 1 to ST3_SHUTDOWN_CLR clears this bit
2	ST2_SHUTDOWN_STS	read-only	Stage 2 shutdown occurred, writing 1 to ST2_SHUTDOWN_CLR clears this bit
1:0	TEMP_ALARM_FSM_STATE	read-only	TEMP_ALARM_FSM_STATE 00 = STAGE 0 01 = STAGE 1 10 = STAGE 2 11 = STAGE 3

0x2410 TEMP_ALARM_INT_RT_STS

Type: read-only
Clock: PBUS_WRCLK
Reset State: 0x00
Reset Name: N/A

Interrupt Real Time Status Bits

TEMP_ALARM_INT_RT_STS

Bits	Name	Type	Description
0	TEMP_ALARM_RT_STS	read-only	

0x2411 TEMP_ALARM_INT_SET_TYPE

Type: read-write
Clock: PBUS_WRCLK
Reset State: 0x00
Reset Name: PERPH_RB

0 = use level trigger interrupts, 1 = use edge trigger interrupts

TEMP_ALARM_INT_SET_TYPE

Bits	Name	Type	Description
0	TEMP_ALARM_TYPE	read-write	

0x2412 TEMP_ALARM_INT_POLARITY_HIGH

Type: read-write
Clock: PBUS_WRCLK
Reset State: 0x00
Reset Name: PERPH_RB

1= Interrupt will trigger on a level high (rising edge) event, 0 = level high triggering is disabled

TEMP_ALARM_INT_POLARITY_HIGH

Bits	Name	Type	Description
0	TEMP_ALARM_HIGH	read-write	

0x2413 TEMP_ALARM_INT_POLARITY_LOW

Type: read-write
Clock: PBUS_WRCLK
Reset State: 0x00
Reset Name: PERPH_RB

1' = Interrupt will trigger on a level low (falling edge) event, '0' = level low triggering is disabled

TEMP_ALARM_INT_POLARITY_LOW

Bits	Name	Type	Description
0	TEMP_ALARM_LOW	read-write	

0x2414 TEMP_ALARM_INT_LATCHED_CLR

Type: write-only
Clock: PBUS_WRCLK
Reset State: 0x00
Reset Name: PERPH_RB

Writing a '1' to this interrupt will rearm the interrupt when an interrupt is pending. It clears the internal sticky and sent bits

TEMP_ALARM_INT_LATCHED_CLR

Bits	Name	Type	Description
0	TEMP_ALARM_LATCHED_CLR	write-only	

0x2415 TEMP_ALARM_INT_EN_SET

Type: read-write
Clock: PBUS_WRCLK
Reset State: 0x00
Reset Name: PERPH_RB

Writing '0' to this register has no effect. Writing a '1' will enable the corresponding interrupt. Reading this register will readback enable status

PMIC_SET_MASK

TEMP_ALARM_INT_EN_SET

Bits	Name	Type	Description
0	TEMP_ALARM_EN_SET	read-write	

0x2416 TEMP_ALARM_INT_EN_CLR

Type: read-write
Clock: PBUS_WRCLK
Reset State: 0x00
Reset Name: PERPH_RB

Writing '0' to this register has no effect. Writing a '1' will disable the corresponding interrupt. Reading this register will readback enable status

PMIC_CLR_MASK=INT_EN_SET

TEMP_ALARM_INT_EN_CLR

Bits	Name	Type	Description
0	TEMP_ALARM_EN_CLR	read-write	

0x2418 TEMP_ALARM_INT_LATCHED_STS

Type: read-only
Clock: PBUS_WRCLK
Reset State: 0x00
Reset Name: N/A

Debug: Latched (Sticky) Interrupt. '1' indicates that the interrupt has triggered. Once the latched bit is set it can only be cleared by writing the clear bit.

TEMP_ALARM_INT_LATCHED_STS

Bits	Name	Type	Description
0	TEMP_ALARM_LATCHED_STS	read-only	

0x2419 TEMP_ALARM_INT_PENDING_STS

Type: read-only
Clock: PBUS_WRCLK
Reset State: 0x00
Reset Name: N/A

Debug: Pending is set if interrupt has been sent but not cleared.

TEMP_ALARM_INT_PENDING_STS

Bits	Name	Type	Description
0	TEMP_ALARM_PENDING_STS	read-only	

0x241A TEMP_ALARM_INT_MID_SEL

Type: read-write
Clock: PBUS_WRCLK
Reset State: 0x00
Reset Name: PERPH_RB

Selects the MID that will receive the interrupt

TEMP_ALARM_INT_MID_SEL

Bits	Name	Type	Description
1:0	INT_MID_SEL	read-write	

0x241B TEMP_ALARM_INT_PRIORITY

Type: read-write
Clock: PBUS_WRCLK
Reset State: 0x00
Reset Name: PERPH_RB

SR=0 A=1

TEMP_ALARM_INT_PRIORITY

Bits	Name	Type	Description
0	INT_PRIORITY	read-write	

0x2440 TEMP_ALARM_SHUTDOWN_CTL1

Type: read-write
Clock: PBUS_WRCLK
Reset State: 0x01
Reset Name: PERPH_RB

TEMP_ALARM_SHUTDOWN_CTL1

Bits	Name	Type	Description
7	OVRD_ST3_EN	read-write	OVRD_ST3_EN : Override automatic shutdown in stage 3
6	OVRD_ST2_EN	read-write	OVRD_ST2_EN : Override partial automatic shutdown in stage 2
1:0	TEMP_THRESH_CNTRL	read-write	TEMP_THRESH_CNTRL 0 = {105, 125, 145} 1 = {110, 130, 150} 2 = {115, 135, 155} 3 = {120, 140, 160}

0x2442 TEMP_ALARM_SHUTDOWN_CTL2

Type: write-only
Clock: PBUS_WRCLK
Reset State: 0x00
Reset Name: PERPH_RB

TEMP_ALARM_SHUTDOWN_CTL2

Bits	Name	Type	Description
7	ST3_SHUTDOWN_CLR	write-only	writing 1 clears ST3_SHUTDOWN_STS bit

TEMP_ALARM_SHUTDOWN_CTL2 (Continued)

Bits	Name	Type	Description
6	ST2_SHUTDOWN_CLR	write-only	writing 1 clears ST2_SHUTDOWN_STS bit

0x2446 TEMP_ALARM_EN_CTL1

Type: read-write
Clock: PBUS_WRCLK
Reset State: 0x01
Reset Name: PERPH_RB

TEMP_ALARM_EN_CTL1

Bits	Name	Type	Description
7	TEMP_ALARM_EN	read-write	1: force enable TEMP ALARM 0: don't force enable TEMP ALARM
0	FOLLOW_TEMP_ALARM_HW_EN	read-write	1: follow TEMP_ALARM_HW_EN 0: disable TEMP ALARM

5 CLK_DIST_CLK_DIST

0x5904 CLK_DIST_PERPH_TYPE

Type: read-only
Clock: PBUS_WRCLK
Reset State: 0x06
Reset Name: N/A

Peripheral Type

CLK_DIST_PERPH_TYPE

Bits	Name	Type	Description
7:0	TYPE	read-only	Clock

0x5905 CLK_DIST_PERPH_SUBTYPE

Type: read-only
Clock: PBUS_WRCLK
Reset State: 0x02
Reset Name: N/A

Peripheral SubType

CLK_DIST_PERPH_SUBTYPE

Bits	Name	Type	Description
7:0	SUBTYPE	read-only	Clock Dist

0x5908 CLK_DIST_STATUS1

Type: read-only
Clock: PBUS_WRCLK
Reset State: 0x00
Reset Name: N/A

Status Registers

CLK_DIST_STATUS1

Bits	Name	Type	Description
7	RC19M_OK	read-only	0 = 19M2 RC is off 1 =19M2 RC is on

0x5910 CLK_DIST_INT_RT_STS

Type: read-only
Clock: PBUS_WRCLK
Reset State: 0x00
Reset Name: N/A

Interrupt Real Time Status Bits

CLK_DIST_INT_RT_STS

Bits	Name	Type	Description
0	XO19M2_HALT_DET_RT_STS	read-only	19M2_XO HALT detected

0x5911 CLK_DIST_INT_SET_TYPE

Type: read-write
Clock: PBUS_WRCLK
Reset State: 0x00
Reset Name: PERPH_RB

0 = use level trigger interrupts, 1 = use edge trigger interrupts

CLK_DIST_INT_SET_TYPE

Bits	Name	Type	Description
0	XO19M2_HALT_DET_TYPE	read-write	

0x5912 CLK_DIST_INT_POLARITY_HIGH

Type: read-write
Clock: PBUS_WRCLK
Reset State: 0x00
Reset Name: PERPH_RB

1= Interrupt will trigger on a level high (rising edge) event, 0 = level high triggering is disabled

CLK_DIST_INT_POLARITY_HIGH

Bits	Name	Type	Description
0	XO19M2_HALT_DET_HIGH	read-write	

0x5913 CLK_DIST_INT_POLARITY_LOW

Type: read-write
Clock: PBUS_WRCLK
Reset State: 0x00
Reset Name: PERPH_RB

1' = Interrupt will trigger on a level low (falling edge) event, '0' = level low triggering is disabled

CLK_DIST_INT_POLARITY_LOW

Bits	Name	Type	Description
0	XO19M2_HALT_DET_LOW	read-write	

0x5914 CLK_DIST_INT_LATCHED_CLR

Type: write-only
Clock: PBUS_WRCLK
Reset State: 0x00
Reset Name: PERPH_RB

Writing a '1' to this interrupt will rearm the interrupt when an interrupt is pending. It clears the internal sticky and sent bits

CLK_DIST_INT_LATCHED_CLR

Bits	Name	Type	Description
0	XO19M2_HALT_DET_LATCHED_CLR	write-only	

0x5915 CLK_DIST_INT_EN_SET

Type: read-write
Clock: PBUS_WRCLK
Reset State: 0x00
Reset Name: PERPH_RB

0' = interrupt is disabled (or masked), 1 = interrupt is enabled

PMIC_SET_MASK

CLK_DIST_INT_EN_SET

Bits	Name	Type	Description
0	XO19M2_HALT_DET_EN_SET	read-write	

0x5916 CLK_DIST_INT_EN_CLR

Type: read-write
Clock: PBUS_WRCLK
Reset State: 0x00
Reset Name: PERPH_RB

0' = interrupt is disabled (or masked), 1 = interrupt is enabled

PMIC_CLR_MASK=INT_EN_SET

CLK_DIST_INT_EN_CLR

Bits	Name	Type	Description
0	XO19M2_HALT_DET_EN_CLR	read-write	

0x5918 CLK_DIST_INT_LATCHED_STS

Type: read-only
Clock: PBUS_WRCLK
Reset State: 0x00
Reset Name: N/A

Latched (Sticky) Interrupt. '1' indicates that the interrupt has triggered. Once the latched bit is set it can only be cleared by writing the clear bit.

CLK_DIST_INT_LATCHED_STS

Bits	Name	Type	Description
0	XO19M2_HALT_DET_LATCHED_STS	read-only	

0x5919 CLK_DIST_INT_PENDING_STS

Type: read-only
Clock: PBUS_WRCLK
Reset State: 0x00
Reset Name: N/A

Debug: Pending is set if interrupt has been sent but not cleared.

CLK_DIST_INT_PENDING_STS

Bits	Name	Type	Description
0	XO19M2_HALT_DET_PENDING_STS	read-only	

0x591A CLK_DIST_INT_MID_SEL

Type: read-write
Clock: PBUS_WRCLK
Reset State: 0x00
Reset Name: PERPH_RB

Selects the MID that will receive the interrupt

CLK_DIST_INT_MID_SEL

Bits	Name	Type	Description
1:0	INT_MID_SEL	read-write	

0x591B CLK_DIST_INT_PRIORITY

Type: read-write
Clock: PBUS_WRCLK
Reset State: 0x00
Reset Name: PERPH_RB

SR=0 A=1

CLK_DIST_INT_PRIORITY

Bits	Name	Type	Description
0	INT_PRIORITY	read-write	

0x5940 CLK_DIST_CLK_CTL1

Type: read-write
Clock: PBUS_WRCLK
Reset State: 0x15
Reset Name: PERPH_RB

CLK_DIST_CLK_CTL1

Bits	Name	Type	Description
5:4	SMPS_CLK_SEL	read-write	00: (XO_OUTBUFF_EN_DLY AND 19M2_HALT_b) 1=19.2 MHz XO, 0=19.2 MHz RC 01: Force 19.2 MHz RC osc as source 10: Force 19.2 MHz XO osc as source 11: Follow 19.2 MHz osc halt Halt = 1 : RC Halt = 0 : XO
3:2	GPCLK_19M2_SEL	read-write	00: (XO_OUTBUFF_EN_DLY AND 19M2_HALT_b) 1=19.2 MHz XO, 0=19.2 MHz RC 01: Force 19.2 MHz RC osc as source 10: Force 19.2 MHz XO osc as source 11: Follow 19.2 MHz osc halt Halt = 1 : RC Halt = 0 : XO
1:0	XORC19M2_CLK_SEL	read-write	00: (XO_OUTBUFF_EN_DLY AND 19M2_HALT_b) 1=19.2 MHz XO, 0=19.2 MHz RC 01: Force 19.2 MHz RC osc as source 10: Force 19.2 MHz XO osc as source 11: Follow 19.2 MHz osc halt Halt = 1 : RC Halt = 0 : XO

0x5941 CLK_DIST_CLK_CTL2

Type: read-write
Clock: PBUS_WRCLK
Reset State: 0x00
Reset Name: PERPH_RB

CLK_DIST_CLK_CTL2

Bits	Name	Type	Description
0	SEL_ALT_SC	read-write	When high, enables xo/586 clock & changes sleep clock source in the clocks module to xo/586. ORed with xxx bit This pRvides the low power sleep clock output. Enables the XO and sets sleep clock mux to output XO / 586 thRugh ripple divider.

0x5942 CLK_DIST_CLK_CTL3

Type: read-write
Clock: PBUS_WRCLK
Reset State: 0x00
Reset Name: dVdd_rb

CLK_DIST_CLK_CTL3

Bits	Name	Type	Description
0	SEL_ALT_RTC	read-write	

0x5943 CLK_DIST_CLK_CTL4

Type: read-write
Clock: PBUS_WRCLK
Reset State: 0x02
Reset Name: xVdd_rb

CLK_DIST_CLK_CTL4

Bits	Name	Type	Description
1	CLK_32K_RC	read-write	CLK_32K_RC: This bit along with SEL_ALT_SC abd SEL_ALT_RTC fRm CLK_CTRL2??? register sets the source of the sleep clock and RTC clock. 0 = The state of SEL_ALT_SC and SEL_ALT_RTC determines the source of 32K clock (either one of the 32K clock source or divided down clock source) 1 = Forces the divided down (XO or RC) / 586 as 32K clock source ** This bit also affects the 32K, 1K and 1 Hz clock outputs. See note 1 for more details.
0	XO32K_CLK_SEL	read-write	Selects between CalRC/LFRC and 32K XO/external 32K source

0x5945 CLK_DIST_HALT_CTL

Type: read-write
Clock: PBUS_WRCLK
Reset State: 0x00
Reset Name: PERPH_RB

CLK_DIST_HALT_CTL

Bits	Name	Type	Description
7	XO19M2_HALT_DET_EN	read-write	XO19M2_HALT_DET_EN 1=Enable the 19.2 MHz halt detector. 0=Disable the 19.2 MHz halt detector.
6	FORCE_XO19M2_OSC_HALT	read-write	FORCE_19M2_OSC_HALT Forces 19.2 MHz halt detect output = 1
0	HOLD_XO19M2_OSC_HALT	read-write	HOLD_19M2_OSC_HALT 1 = Hold the 19.2 MHz halt detector output once it goes high 0 = Clear the 19.2 MHz halt detector output if it is high.

0x5946 CLK_DIST_RC_CTL

Type: read-write
Clock: PBUS_WRCLK
Reset State: 0x01
Reset Name: PERPH_RB

RC_EN=FORCE_RC19M2_OSC_ON OR(RC19M2_OSC_HW_CTL AND HW_CTL).

Writing zero to this register will disable the RC osc

CLK_DIST_RC_CTL

Bits	Name	Type	Description
7	FORCE_RC19M2_OSC_ON	read-write	RC19M2RC_OSC_ON : Force relaxation oscillator ON (higher priority than FORCE_RC19M2_OSC_ON)
0	RC19M2_OSC_HW_CTL	read-write	RC oscillator state follows HW requests.

0x5948 CLK_DIST_PD_CTL

Type: read-write
Clock: PBUS_WRCLK
Reset State: 0x80
Reset Name: PERPH_RB

CLK_DIST_PD_CTL

Bits	Name	Type	Description
7	PD_EN	read-write	1' = Enable the pulldown on SYS_CLK pad (used only on the slave pmic)

6 PBS_CLIENTn

6.1 Overview

Table 6-1 Blocks

Name
PBS_CLIENT0
PBS_CLIENT1
PBS_CLIENT2
PBS_CLIENT3
PBS_CLIENT4
PBS_CLIENT5
PBS_CLIENT6
PBS_CLIENT7

6.2 PBS_CLIENT0_PBS_CLIENT

0x7104 PBS_CLIENT0_PERPH_TYPE

Type: read-only
Clock: PBUS_WRCLK
Reset State: 0x16
Reset Name: N/A

Peripheral Type

PBS_CLIENT0_PERPH_TYPE

Bits	Name	Type	Description
7:0	TYPE	read-only	PBS Reset State: 0x16

0x7105 PBS_CLIENT0_PERPH_SUBTYPE

Type: read-only
Clock: PBUS_WRCLK
Reset State: 0x08
Reset Name: N/A

Peripheral SubType

PBS_CLIENT0_PERPH_SUBTYPE

Bits	Name	Type	Description
7:0	SUBTYPE	read-only	Client 0 Reset State: 0x08

0x7108 PBS_CLIENT0_STATUS0

Type: read-only
Clock: PBUS_WRCLK
Reset State: 0bXXXXX000
Reset Name: N/A

Status Registers

PBS_CLIENT0_STATUS0

Bits	Name	Type	Description
7	TRIG_EN_STATUS	read-only	Overall trigger-sequence enable state

PBS_CLIENT0_STATUS0 (Continued)

Bits	Name	Type	Description
5:4	COMP_STATUS	read-only	These bits show the completion state of this client trigger-sequence pair. 00 = In execution. 01 = Normal completion 10 = Error completion. 11= Abort completion.
2:0	TRIG_FSM_STATUS	read-only	Show state of trigger slice FSM.

0x7110 PBS_CLIENT0_INT_RT_STS

Type: read-only
Clock: PBUS_WRCLK
Reset State: 0x00
Reset Name: PBS_CORE_PERPH_RB

Interrupt Real Time Status Bits

PBS_CLIENT0_INT_RT_STS

Bits	Name	Type	Description
1	SEQ_ENDED_RT_STS	read-only	
0	SEQ_ERROR_RT_STS	read-only	

0x7111 PBS_CLIENT0_INT_SET_TYPE

Type: read-write
Clock: PBUS_WRCLK
Reset State: 0x00
Reset Name: PBS_CORE_PERPH_RB

0 = use level trigger interrupts, 1 = use edge trigger interrupts

PBS_CLIENT0_INT_SET_TYPE

Bits	Name	Type	Description
1	SEQ_ENDED_TYPE	read-write	
0	SEQ_ERROR_TYPE	read-write	

0x7112 PBS_CLIENT0_INT_POLARITY_HIGH

Type: read-write
Clock: PBUS_WRCLK
Reset State: 0x00
Reset Name: PBS_CORE_PERPH_RB

1= Interrupt will trigger on a level high (rising edge) event, 0 = level high triggering is disabled

PBS_CLIENT0_INT_POLARITY_HIGH

Bits	Name	Type	Description
1	SEQ_ENDED_HIGH	read-write	
0	SEQ_ERROR_HIGH	read-write	

0x7113 PBS_CLIENT0_INT_POLARITY_LOW

Type: read-write
Clock: PBUS_WRCLK
Reset State: 0x00
Reset Name: PBS_CORE_PERPH_RB

1' = Interrupt will trigger on a level low (falling edge) event, '0' = level low triggering is disabled

PBS_CLIENT0_INT_POLARITY_LOW

Bits	Name	Type	Description
1	SEQ_ENDED_LOW	read-write	
0	SEQ_ERROR_LOW	read-write	

0x7114 PBS_CLIENT0_INT_LATCHED_CLR

Type: write-only
Clock: PBUS_WRCLK
Reset State: 0x00
Reset Name: PBS_CORE_PERPH_RB

Writing a '1' to this interrupt will rearm the interrupt when an interrupt is pending. It clears the internal sticky and sent bits

PBS_CLIENT0_INT_LATCHED_CLR

Bits	Name	Type	Description
1	SEQ_ENDED_LATCHED_CLR	write-only	
0	SEQ_ERROR_LATCHED_CLR	write-only	

0x7115 PBS_CLIENT0_INT_EN_SET

Type: read-write
Clock: PBUS_WRCLK
Reset State: 0x00
Reset Name: PBS_CORE_PERPH_RB

Writing '0' to this register has no effect. Writing a '1' will enable the corresponding interrupt. Reading this register will readback enable status

PMIC_SET_MASK

PBS_CLIENT0_INT_EN_SET

Bits	Name	Type	Description
1	SEQ_ENDED_EN_SET	read-write	
0	SEQ_ERROR_EN_SET	read-write	

0x7116 PBS_CLIENT0_INT_EN_CLR

Type: read-write
Clock: PBUS_WRCLK
Reset State: 0x00
Reset Name: PBS_CORE_PERPH_RB

Writing '0' to this register has no effect. Writing a '1' will disable the corresponding interrupt. Reading this register will readback enable status

PMIC_CLR_MASK=INT_EN_SET

PBS_CLIENT0_INT_EN_CLR

Bits	Name	Type	Description
1	SEQ_ENDED_EN_CLR	read-write	

PBS_CLIENT0_INT_EN_CLR (Continued)

Bits	Name	Type	Description
0	SEQ_ERROR_EN_CLR	read-write	

0x7118 PBS_CLIENT0_INT_LATCHED_STS

Type: read-only
Clock: PBUS_WRCLK
Reset State: 0x00
Reset Name: PBS_CORE_PERPH_RB

Debug: Latched (Sticky) Interrupt. '1' indicates that the interrupt has triggered. Once the latched bit is set it can only be cleared by writing the clear bit.

PBS_CLIENT0_INT_LATCHED_STS

Bits	Name	Type	Description
1	SEQ_ENDED_LATCHED_STS	read-only	
0	SEQ_ERROR_LATCHED_STS	read-only	

0x7119 PBS_CLIENT0_INT_PENDING_STS

Type: read-only
Clock: PBUS_WRCLK
Reset State: 0x00
Reset Name: PBS_CORE_PERPH_RB

Debug: Pending is set if interrupt has been sent but not cleared.

PBS_CLIENT0_INT_PENDING_STS

Bits	Name	Type	Description
1	SEQ_ENDED_PENDING_STS	read-only	
0	SEQ_ERROR_PENDING_STS	read-only	

0x711A PBS_CLIENT0_INT_MID_SEL

Type: read-write
Clock: PBUS_WRCLK
Reset State: 0x00
Reset Name: PBS_CORE_PERPH_RB

Selects the MID that will receive the interrupt

PBS_CLIENT0_INT_MID_SEL

Bits	Name	Type	Description
1:0	INT_MID_SEL	read-write	

0x711B PBS_CLIENT0_INT_PRIORITY

Type: read-write
Clock: PBUS_WRCLK
Reset State: 0x00
Reset Name: PBS_CORE_PERPH_RB

SR=0 A=1

PBS_CLIENT0_INT_PRIORITY

Bits	Name	Type	Description
0	INT_PRIORITY	read-write	

0x7140 PBS_CLIENT0_TRIG_CFG

Type: read-write
Clock: PBUS_WRCLK
Reset State: 0x80
Reset Name: PBS_CORE_PERPH_RB

Trigger Configuration

PMIC_SYNC=pbs_clk:pbs_rb

PBS_CLIENT0_TRIG_CFG

Bits	Name	Type	Description
7	TRIGGER_RE_EN	read-write	1 = Enable Rising Edge Trigger 0 = Disable Falling Edge Trigger

PBS_CLIENT0_TRIG_CFG (Continued)

Bits	Name	Type	Description
6	TRIGGER_FE_EN	read-write	1 = Enable Falling Edge Trigger 0 = Disable Falling Edge Trigger

0x7142 PBS_CLIENT0_TRIG_CTL

Type: write-only
Clock: PBUS_WRCLK
Reset State: 0x00
Reset Name: PBS_CORE_PERPH_RB

PBS_CLIENT0_TRIG_CTL

Bits	Name	Type	Description
0	SW_TRIGGER	write-only	Writing 0x01 to this register will immediately create a trigger pulse.

0x7146 PBS_CLIENT0_EN_CTL

Type: read-write
Clock: PBUS_WRCLK
Reset State: 0x80
Reset Name: PBS_CORE_PERPH_RB

PMIC_SYNC=pbs_clk:pbs_rb

PBS_CLIENT0_EN_CTL

Bits	Name	Type	Description
7	TRIGGER_EN	read-write	Must be set to 1 to enable all triggers in the peripheral

6.3 PBS_CLIENT1_PBS_CLIENT

0x7204 PBS_CLIENT1_PERPH_TYPE

Type: read-only
Clock: PBUS_WRCLK
Reset State: 0x16
Reset Name: N/A

Peripheral Type

PBS_CLIENT1_PERPH_TYPE

Bits	Name	Type	Description
7:0	TYPE	read-only	PBS Reset State: 0x16

0x7205 PBS_CLIENT1_PERPH_SUBTYPE

Type: read-only
Clock: PBUS_WRCLK
Reset State: 0x08
Reset Name: N/A

Peripheral SubType

PBS_CLIENT1_PERPH_SUBTYPE

Bits	Name	Type	Description
7:0	SUBTYPE	read-only	Client 1 Reset State: 0x08

0x7208 PBS_CLIENT1_STATUS0

Type: read-only
Clock: PBUS_WRCLK
Reset State: 0bXXXXX000
Reset Name: N/A

Status Registers

PBS_CLIENT1_STATUS0

Bits	Name	Type	Description
7	TRIG_EN_STATUS	read-only	Overall trigger-sequence enable state

PBS_CLIENT1_STATUS0 (Continued)

Bits	Name	Type	Description
5:4	COMP_STATUS	read-only	These bits show the completion state of this client trigger-sequence pair. 00 = In execution. 01 = Normal completion 10 = Error completion. 11= Abort completion.
2:0	TRIG_FSM_STATUS	read-only	Show state of trigger slice FSM.

0x7210 PBS_CLIENT1_INT_RT_STS

Type: read-only
Clock: PBUS_WRCLK
Reset State: 0x00
Reset Name: PBS_CORE_PERPH_RB

Interrupt Real Time Status Bits

PBS_CLIENT1_INT_RT_STS

Bits	Name	Type	Description
1	SEQ_ENDED_RT_STS	read-only	
0	SEQ_ERROR_RT_STS	read-only	

0x7211 PBS_CLIENT1_INT_SET_TYPE

Type: read-write
Clock: PBUS_WRCLK
Reset State: 0x00
Reset Name: PBS_CORE_PERPH_RB

0 = use level trigger interrupts, 1 = use edge trigger interrupts

PBS_CLIENT1_INT_SET_TYPE

Bits	Name	Type	Description
1	SEQ_ENDED_TYPE	read-write	
0	SEQ_ERROR_TYPE	read-write	

0x7212 PBS_CLIENT1_INT_POLARITY_HIGH

Type: read-write
Clock: PBUS_WRCLK
Reset State: 0x00
Reset Name: PBS_CORE_PERPH_RB

1= Interrupt will trigger on a level high (rising edge) event, 0 = level high triggering is disabled

PBS_CLIENT1_INT_POLARITY_HIGH

Bits	Name	Type	Description
1	SEQ_ENDED_HIGH	read-write	
0	SEQ_ERROR_HIGH	read-write	

0x7213 PBS_CLIENT1_INT_POLARITY_LOW

Type: read-write
Clock: PBUS_WRCLK
Reset State: 0x00
Reset Name: PBS_CORE_PERPH_RB

1' = Interrupt will trigger on a level low (falling edge) event, '0' = level low triggering is disabled

PBS_CLIENT1_INT_POLARITY_LOW

Bits	Name	Type	Description
1	SEQ_ENDED_LOW	read-write	
0	SEQ_ERROR_LOW	read-write	

0x7214 PBS_CLIENT1_INT_LATCHED_CLR

Type: write-only
Clock: PBUS_WRCLK
Reset State: 0x00
Reset Name: PBS_CORE_PERPH_RB

Writing a '1' to this interrupt will rearm the interrupt when an interrupt is pending. It clears the internal sticky and sent bits

PBS_CLIENT1_INT_LATCHED_CLR

Bits	Name	Type	Description
1	SEQ_ENDED_LATCHED_CLR	write-only	
0	SEQ_ERROR_LATCHED_CLR	write-only	

0x7215 PBS_CLIENT1_INT_EN_SET

Type: read-write
Clock: PBUS_WRCLK
Reset State: 0x00
Reset Name: PBS_CORE_PERPH_RB

Writing '0' to this register has no effect. Writing a '1' will enable the corresponding interrupt. Reading this register will readback enable status

PMIC_SET_MASK

PBS_CLIENT1_INT_EN_SET

Bits	Name	Type	Description
1	SEQ_ENDED_EN_SET	read-write	
0	SEQ_ERROR_EN_SET	read-write	

0x7216 PBS_CLIENT1_INT_EN_CLR

Type: read-write
Clock: PBUS_WRCLK
Reset State: 0x00
Reset Name: PBS_CORE_PERPH_RB

Writing '0' to this register has no effect. Writing a '1' will disable the corresponding interrupt. Reading this register will readback enable status

PMIC_CLR_MASK=INT_EN_SET

PBS_CLIENT1_INT_EN_CLR

Bits	Name	Type	Description
1	SEQ_ENDED_EN_CLR	read-write	

PBS_CLIENT1_INT_EN_CLR (Continued)

Bits	Name	Type	Description
0	SEQ_ERROR_EN_CLR	read-write	

0x7218 PBS_CLIENT1_INT_LATCHED_STS

Type: read-only
Clock: PBUS_WRCLK
Reset State: 0x00
Reset Name: PBS_CORE_PERPH_RB

Debug: Latched (Sticky) Interrupt. '1' indicates that the interrupt has triggered. Once the latched bit is set it can only be cleared by writing the clear bit.

PBS_CLIENT1_INT_LATCHED_STS

Bits	Name	Type	Description
1	SEQ_ENDED_LATCHED_STS	read-only	
0	SEQ_ERROR_LATCHED_STS	read-only	

0x7219 PBS_CLIENT1_INT_PENDING_STS

Type: read-only
Clock: PBUS_WRCLK
Reset State: 0x00
Reset Name: PBS_CORE_PERPH_RB

Debug: Pending is set if interrupt has been sent but not cleared.

PBS_CLIENT1_INT_PENDING_STS

Bits	Name	Type	Description
1	SEQ_ENDED_PENDING_STS	read-only	
0	SEQ_ERROR_PENDING_STS	read-only	

0x721A PBS_CLIENT1_INT_MID_SEL

Type: read-write
Clock: PBUS_WRCLK
Reset State: 0x00
Reset Name: PBS_CORE_PERPH_RB

Selects the MID that will receive the interrupt

PBS_CLIENT1_INT_MID_SEL

Bits	Name	Type	Description
1:0	INT_MID_SEL	read-write	

0x721B PBS_CLIENT1_INT_PRIORITY

Type: read-write
Clock: PBUS_WRCLK
Reset State: 0x00
Reset Name: PBS_CORE_PERPH_RB

SR=0 A=1

PBS_CLIENT1_INT_PRIORITY

Bits	Name	Type	Description
0	INT_PRIORITY	read-write	

0x7240 PBS_CLIENT1_TRIG_CFG

Type: read-write
Clock: PBUS_WRCLK
Reset State: 0x80
Reset Name: PBS_CORE_PERPH_RB

Trigger Configuration

PMIC_SYNC=pbs_clk:pbs_rb

PBS_CLIENT1_TRIG_CFG

Bits	Name	Type	Description
7	TRIGGER_RE_EN	read-write	1 = Enable Rising Edge Trigger 0 = Disable Falling Edge Trigger

PBS_CLIENT1_TRIG_CFG (Continued)

Bits	Name	Type	Description
6	TRIGGER_FE_EN	read-write	1 = Enable Falling Edge Trigger 0 = Disable Falling Edge Trigger

0x7242 PBS_CLIENT1_TRIG_CTL

Type: write-only
Clock: PBUS_WRCLK
Reset State: 0x00
Reset Name: PBS_CORE_PERPH_RB

PBS_CLIENT1_TRIG_CTL

Bits	Name	Type	Description
0	SW_TRIGGER	write-only	Writing 0x01 to this register will immediately create a trigger pulse.

0x7246 PBS_CLIENT1_EN_CTL

Type: read-write
Clock: PBUS_WRCLK
Reset State: 0x80
Reset Name: PBS_CORE_PERPH_RB

PMIC_SYNC=pbs_clk:pbs_rb

PBS_CLIENT1_EN_CTL

Bits	Name	Type	Description
7	TRIGGER_EN	read-write	Must be set to 1 to enable all triggers in the peripheral

6.4 PBS_CLIENT2_PBS_CLIENT

0x7304 PBS_CLIENT2_PERPH_TYPE

Type: read-only
Clock: PBUS_WRCLK
Reset State: 0x16
Reset Name: N/A

Peripheral Type

PBS_CLIENT2_PERPH_TYPE

Bits	Name	Type	Description
7:0	TYPE	read-only	PBS Reset State: 0x16

0x7305 PBS_CLIENT2_PERPH_SUBTYPE

Type: read-only
Clock: PBUS_WRCLK
Reset State: 0x08
Reset Name: N/A

Peripheral SubType

PBS_CLIENT2_PERPH_SUBTYPE

Bits	Name	Type	Description
7:0	SUBTYPE	read-only	Client 2 Reset State: 0x08

0x7308 PBS_CLIENT2_STATUS0

Type: read-only
Clock: PBUS_WRCLK
Reset State: 0bXXXXX000
Reset Name: N/A

Status Registers

PBS_CLIENT2_STATUS0

Bits	Name	Type	Description
7	TRIG_EN_STATUS	read-only	Overall trigger-sequence enable state

PBS_CLIENT2_STATUS0 (Continued)

Bits	Name	Type	Description
5:4	COMP_STATUS	read-only	These bits show the completion state of this client trigger-sequence pair. 00 = In execution. 01 = Normal completion 10 = Error completion. 11= Abort completion.
2:0	TRIG_FSM_STATUS	read-only	Show state of trigger slice FSM.

0x7310 PBS_CLIENT2_INT_RT_STS

Type: read-only
Clock: PBUS_WRCLK
Reset State: 0x00
Reset Name: PBS_CORE_PERPH_RB

Interrupt Real Time Status Bits

PBS_CLIENT2_INT_RT_STS

Bits	Name	Type	Description
1	SEQ_ENDED_RT_STS	read-only	
0	SEQ_ERROR_RT_STS	read-only	

0x7311 PBS_CLIENT2_INT_SET_TYPE

Type: read-write
Clock: PBUS_WRCLK
Reset State: 0x00
Reset Name: PBS_CORE_PERPH_RB

0 = use level trigger interrupts, 1 = use edge trigger interrupts

PBS_CLIENT2_INT_SET_TYPE

Bits	Name	Type	Description
1	SEQ_ENDED_TYPE	read-write	
0	SEQ_ERROR_TYPE	read-write	

0x7312 PBS_CLIENT2_INT_POLARITY_HIGH

Type: read-write
Clock: PBUS_WRCLK
Reset State: 0x00
Reset Name: PBS_CORE_PERPH_RB

1= Interrupt will trigger on a level high (rising edge) event, 0 = level high triggering is disabled

PBS_CLIENT2_INT_POLARITY_HIGH

Bits	Name	Type	Description
1	SEQ_ENDED_HIGH	read-write	
0	SEQ_ERROR_HIGH	read-write	

0x7313 PBS_CLIENT2_INT_POLARITY_LOW

Type: read-write
Clock: PBUS_WRCLK
Reset State: 0x00
Reset Name: PBS_CORE_PERPH_RB

1' = Interrupt will trigger on a level low (falling edge) event, '0' = level low triggering is disabled

PBS_CLIENT2_INT_POLARITY_LOW

Bits	Name	Type	Description
1	SEQ_ENDED_LOW	read-write	
0	SEQ_ERROR_LOW	read-write	

0x7314 PBS_CLIENT2_INT_LATCHED_CLR

Type: write-only
Clock: PBUS_WRCLK
Reset State: 0x00
Reset Name: PBS_CORE_PERPH_RB

Writing a '1' to this interrupt will rearm the interrupt when an interrupt is pending. It clears the internal sticky and sent bits

PBS_CLIENT2_INT_LATCHED_CLR

Bits	Name	Type	Description
1	SEQ_ENDED_LATCHED_CLR	write-only	
0	SEQ_ERROR_LATCHED_CLR	write-only	

0x7315 PBS_CLIENT2_INT_EN_SET

Type: read-write
Clock: PBUS_WRCLK
Reset State: 0x00
Reset Name: PBS_CORE_PERPH_RB

Writing '0' to this register has no effect. Writing a '1' will enable the corresponding interrupt. Reading this register will readback enable status

PMIC_SET_MASK

PBS_CLIENT2_INT_EN_SET

Bits	Name	Type	Description
1	SEQ_ENDED_EN_SET	read-write	
0	SEQ_ERROR_EN_SET	read-write	

0x7316 PBS_CLIENT2_INT_EN_CLR

Type: read-write
Clock: PBUS_WRCLK
Reset State: 0x00
Reset Name: PBS_CORE_PERPH_RB

Writing '0' to this register has no effect. Writing a '1' will disable the corresponding interrupt. Reading this register will readback enable status

PMIC_CLR_MASK=INT_EN_SET

PBS_CLIENT2_INT_EN_CLR

Bits	Name	Type	Description
1	SEQ_ENDED_EN_CLR	read-write	

PBS_CLIENT2_INT_EN_CLR (Continued)

Bits	Name	Type	Description
0	SEQ_ERROR_EN_CLR	read-write	

0x7318 PBS_CLIENT2_INT_LATCHED_STS

Type: read-only
Clock: PBUS_WRCLK
Reset State: 0x00
Reset Name: PBS_CORE_PERPH_RB

Debug: Latched (Sticky) Interrupt. '1' indicates that the interrupt has triggered. Once the latched bit is set it can only be cleared by writing the clear bit.

PBS_CLIENT2_INT_LATCHED_STS

Bits	Name	Type	Description
1	SEQ_ENDED_LATCHED_STS	read-only	
0	SEQ_ERROR_LATCHED_STS	read-only	

0x7319 PBS_CLIENT2_INT_PENDING_STS

Type: read-only
Clock: PBUS_WRCLK
Reset State: 0x00
Reset Name: PBS_CORE_PERPH_RB

Debug: Pending is set if interrupt has been sent but not cleared.

PBS_CLIENT2_INT_PENDING_STS

Bits	Name	Type	Description
1	SEQ_ENDED_PENDING_STS	read-only	
0	SEQ_ERROR_PENDING_STS	read-only	

0x731A PBS_CLIENT2_INT_MID_SEL

Type: read-write
Clock: PBUS_WRCLK
Reset State: 0x00
Reset Name: PBS_CORE_PERPH_RB

Selects the MID that will receive the interrupt

PBS_CLIENT2_INT_MID_SEL

Bits	Name	Type	Description
1:0	INT_MID_SEL	read-write	

0x731B PBS_CLIENT2_INT_PRIORITY

Type: read-write
Clock: PBUS_WRCLK
Reset State: 0x00
Reset Name: PBS_CORE_PERPH_RB

SR=0 A=1

PBS_CLIENT2_INT_PRIORITY

Bits	Name	Type	Description
0	INT_PRIORITY	read-write	

0x7340 PBS_CLIENT2_TRIG_CFG

Type: read-write
Clock: PBUS_WRCLK
Reset State: 0x80
Reset Name: PBS_CORE_PERPH_RB

Trigger Configuration

PMIC_SYNC=pbs_clk:pbs_rb

PBS_CLIENT2_TRIG_CFG

Bits	Name	Type	Description
7	TRIGGER_RE_EN	read-write	1 = Enable Rising Edge Trigger 0 = Disable Falling Edge Trigger

PBS_CLIENT2_TRIG_CFG (Continued)

Bits	Name	Type	Description
6	TRIGGER_FE_EN	read-write	1 = Enable Falling Edge Trigger 0 = Disable Falling Edge Trigger

0x7342 PBS_CLIENT2_TRIG_CTL

Type: write-only
Clock: PBUS_WRCLK
Reset State: 0x00
Reset Name: PBS_CORE_PERPH_RB

PBS_CLIENT2_TRIG_CTL

Bits	Name	Type	Description
0	SW_TRIGGER	write-only	Writing 0x01 to this register will immediately create a trigger pulse.

0x7346 PBS_CLIENT2_EN_CTL

Type: read-write
Clock: PBUS_WRCLK
Reset State: 0x80
Reset Name: PBS_CORE_PERPH_RB

PMIC_SYNC=pbs_clk:pbs_rb

PBS_CLIENT2_EN_CTL

Bits	Name	Type	Description
7	TRIGGER_EN	read-write	Must be set to 1 to enable all triggers in the peripheral

6.5 PBS_CLIENT3_PBS_CLIENT

0x7404 PBS_CLIENT3_PERPH_TYPE

Type: read-only
Clock: PBUS_WRCLK
Reset State: 0x16
Reset Name: N/A

Peripheral Type

PBS_CLIENT3_PERPH_TYPE

Bits	Name	Type	Description
7:0	TYPE	read-only	PBS Reset State: 0x16

0x7405 PBS_CLIENT3_PERPH_SUBTYPE

Type: read-only
Clock: PBUS_WRCLK
Reset State: 0x08
Reset Name: N/A

Peripheral SubType

PBS_CLIENT3_PERPH_SUBTYPE

Bits	Name	Type	Description
7:0	SUBTYPE	read-only	Client 3 Reset State: 0x08

0x7408 PBS_CLIENT3_STATUS0

Type: read-only
Clock: PBUS_WRCLK
Reset State: 0bXXXXX000
Reset Name: N/A

Status Registers

PBS_CLIENT3_STATUS0

Bits	Name	Type	Description
7	TRIG_EN_STATUS	read-only	Overall trigger-sequence enable state

PBS_CLIENT3_STATUS0 (Continued)

Bits	Name	Type	Description
5:4	COMP_STATUS	read-only	These bits show the completion state of this client trigger-sequence pair. 00 = In execution. 01 = Normal completion 10 = Error completion. 11= Abort completion.
2:0	TRIG_FSM_STATUS	read-only	Show state of trigger slice FSM.

0x7410 PBS_CLIENT3_INT_RT_STS

Type: read-only
Clock: PBUS_WRCLK
Reset State: 0x00
Reset Name: PBS_CORE_PERPH_RB

Interrupt Real Time Status Bits

PBS_CLIENT3_INT_RT_STS

Bits	Name	Type	Description
1	SEQ_ENDED_RT_STS	read-only	
0	SEQ_ERROR_RT_STS	read-only	

0x7411 PBS_CLIENT3_INT_SET_TYPE

Type: read-write
Clock: PBUS_WRCLK
Reset State: 0x00
Reset Name: PBS_CORE_PERPH_RB

0 = use level trigger interrupts, 1 = use edge trigger interrupts

PBS_CLIENT3_INT_SET_TYPE

Bits	Name	Type	Description
1	SEQ_ENDED_TYPE	read-write	
0	SEQ_ERROR_TYPE	read-write	

0x7412 PBS_CLIENT3_INT_POLARITY_HIGH

Type: read-write
Clock: PBUS_WRCLK
Reset State: 0x00
Reset Name: PBS_CORE_PERPH_RB

1= Interrupt will trigger on a level high (rising edge) event, 0 = level high triggering is disabled

PBS_CLIENT3_INT_POLARITY_HIGH

Bits	Name	Type	Description
1	SEQ_ENDED_HIGH	read-write	
0	SEQ_ERROR_HIGH	read-write	

0x7413 PBS_CLIENT3_INT_POLARITY_LOW

Type: read-write
Clock: PBUS_WRCLK
Reset State: 0x00
Reset Name: PBS_CORE_PERPH_RB

1' = Interrupt will trigger on a level low (falling edge) event, '0' = level low triggering is disabled

PBS_CLIENT3_INT_POLARITY_LOW

Bits	Name	Type	Description
1	SEQ_ENDED_LOW	read-write	
0	SEQ_ERROR_LOW	read-write	

0x7414 PBS_CLIENT3_INT_LATCHED_CLR

Type: write-only
Clock: PBUS_WRCLK
Reset State: 0x00
Reset Name: PBS_CORE_PERPH_RB

Writing a '1' to this interrupt will rearm the interrupt when an interrupt is pending. It clears the internal sticky and sent bits

PBS_CLIENT3_INT_LATCHED_CLR

Bits	Name	Type	Description
1	SEQ_ENDED_LATCHED_CLR	write-only	
0	SEQ_ERROR_LATCHED_CLR	write-only	

0x7415 PBS_CLIENT3_INT_EN_SET

Type: read-write
Clock: PBUS_WRCLK
Reset State: 0x00
Reset Name: PBS_CORE_PERPH_RB

Writing '0' to this register has no effect. Writing a '1' will enable the corresponding interrupt. Reading this register will readback enable status

PMIC_SET_MASK

PBS_CLIENT3_INT_EN_SET

Bits	Name	Type	Description
1	SEQ_ENDED_EN_SET	read-write	
0	SEQ_ERROR_EN_SET	read-write	

0x7416 PBS_CLIENT3_INT_EN_CLR

Type: read-write
Clock: PBUS_WRCLK
Reset State: 0x00
Reset Name: PBS_CORE_PERPH_RB

Writing '0' to this register has no effect. Writing a '1' will disable the corresponding interrupt. Reading this register will readback enable status

PMIC_CLR_MASK=INT_EN_SET

PBS_CLIENT3_INT_EN_CLR

Bits	Name	Type	Description
1	SEQ_ENDED_EN_CLR	read-write	

PBS_CLIENT3_INT_EN_CLR (Continued)

Bits	Name	Type	Description
0	SEQ_ERROR_EN_CLR	read-write	

0x7418 PBS_CLIENT3_INT_LATCHED_STS

Type: read-only
Clock: PBUS_WRCLK
Reset State: 0x00
Reset Name: PBS_CORE_PERPH_RB

Debug: Latched (Sticky) Interrupt. '1' indicates that the interrupt has triggered. Once the latched bit is set it can only be cleared by writing the clear bit.

PBS_CLIENT3_INT_LATCHED_STS

Bits	Name	Type	Description
1	SEQ_ENDED_LATCHED_STS	read-only	
0	SEQ_ERROR_LATCHED_STS	read-only	

0x7419 PBS_CLIENT3_INT_PENDING_STS

Type: read-only
Clock: PBUS_WRCLK
Reset State: 0x00
Reset Name: PBS_CORE_PERPH_RB

Debug: Pending is set if interrupt has been sent but not cleared.

PBS_CLIENT3_INT_PENDING_STS

Bits	Name	Type	Description
1	SEQ_ENDED_PENDING_STS	read-only	
0	SEQ_ERROR_PENDING_STS	read-only	

0x741A PBS_CLIENT3_INT_MID_SEL

Type: read-write
Clock: PBUS_WRCLK
Reset State: 0x00
Reset Name: PBS_CORE_PERPH_RB

Selects the MID that will receive the interrupt

PBS_CLIENT3_INT_MID_SEL

Bits	Name	Type	Description
1:0	INT_MID_SEL	read-write	

0x741B PBS_CLIENT3_INT_PRIORITY

Type: read-write
Clock: PBUS_WRCLK
Reset State: 0x00
Reset Name: PBS_CORE_PERPH_RB

SR=0 A=1

PBS_CLIENT3_INT_PRIORITY

Bits	Name	Type	Description
0	INT_PRIORITY	read-write	

0x7440 PBS_CLIENT3_TRIG_CFG

Type: read-write
Clock: PBUS_WRCLK
Reset State: 0x80
Reset Name: PBS_CORE_PERPH_RB

Trigger Configuration

PMIC_SYNC=pbs_clk:pbs_rb

PBS_CLIENT3_TRIG_CFG

Bits	Name	Type	Description
7	TRIGGER_RE_EN	read-write	1 = Enable Rising Edge Trigger 0 = Disable Falling Edge Trigger

PBS_CLIENT3_TRIG_CFG (Continued)

Bits	Name	Type	Description
6	TRIGGER_FE_EN	read-write	1 = Enable Falling Edge Trigger 0 = Disable Falling Edge Trigger

0x7442 PBS_CLIENT3_TRIG_CTL

Type: write-only
Clock: PBUS_WRCLK
Reset State: 0x00
Reset Name: PBS_CORE_PERPH_RB

PBS_CLIENT3_TRIG_CTL

Bits	Name	Type	Description
0	SW_TRIGGER	write-only	Writing 0x01 to this register will immediately create a trigger pulse.

0x7446 PBS_CLIENT3_EN_CTL

Type: read-write
Clock: PBUS_WRCLK
Reset State: 0x80
Reset Name: PBS_CORE_PERPH_RB

PMIC_SYNC=pbs_clk:pbs_rb

PBS_CLIENT3_EN_CTL

Bits	Name	Type	Description
7	TRIGGER_EN	read-write	Must be set to 1 to enable all triggers in the peripheral

6.6 PBS_CLIENT4_PBS_CLIENT

0x7504 PBS_CLIENT4_PERPH_TYPE

Type: read-only
Clock: PBUS_WRCLK
Reset State: 0x16
Reset Name: N/A

Peripheral Type

PBS_CLIENT4_PERPH_TYPE

Bits	Name	Type	Description
7:0	TYPE	read-only	PBS Reset State:0x16

0x7505 PBS_CLIENT4_PERPH_SUBTYPE

Type: read-only
Clock: PBUS_WRCLK
Reset State: 0x08
Reset Name: N/A

Peripheral SubType

PBS_CLIENT4_PERPH_SUBTYPE

Bits	Name	Type	Description
7:0	SUBTYPE	read-only	Client 4 Reset State: 0x08

0x7508 PBS_CLIENT4_STATUS0

Type: read-only
Clock: PBUS_WRCLK
Reset State: 0bXXXXX000
Reset Name: N/A

Status Registers

PBS_CLIENT4_STATUS0

Bits	Name	Type	Description
7	TRIG_EN_STATUS	read-only	Overall trigger-sequence enable state

PBS_CLIENT4_STATUS0 (Continued)

Bits	Name	Type	Description
5:4	COMP_STATUS	read-only	These bits show the completion state of this client trigger-sequence pair. 00 = In execution. 01 = Normal completion 10 = Error completion. 11= Abort completion.
2:0	TRIG_FSM_STATUS	read-only	Show state of trigger slice FSM.

0x7510 PBS_CLIENT4_INT_RT_STS

Type: read-only
Clock: PBUS_WRCLK
Reset State: 0x00
Reset Name: PBS_CORE_PERPH_RB

Interrupt Real Time Status Bits

PBS_CLIENT4_INT_RT_STS

Bits	Name	Type	Description
1	SEQ_ENDED_RT_STS	read-only	
0	SEQ_ERROR_RT_STS	read-only	

0x7511 PBS_CLIENT4_INT_SET_TYPE

Type: read-write
Clock: PBUS_WRCLK
Reset State: 0x00
Reset Name: PBS_CORE_PERPH_RB

0 = use level trigger interrupts, 1 = use edge trigger interrupts

PBS_CLIENT4_INT_SET_TYPE

Bits	Name	Type	Description
1	SEQ_ENDED_TYPE	read-write	
0	SEQ_ERROR_TYPE	read-write	

0x7512 PBS_CLIENT4_INT_POLARITY_HIGH

Type: read-write
Clock: PBUS_WRCLK
Reset State: 0x00
Reset Name: PBS_CORE_PERPH_RB

1= Interrupt will trigger on a level high (rising edge) event, 0 = level high triggering is disabled

PBS_CLIENT4_INT_POLARITY_HIGH

Bits	Name	Type	Description
1	SEQ_ENDED_HIGH	read-write	
0	SEQ_ERROR_HIGH	read-write	

0x7513 PBS_CLIENT4_INT_POLARITY_LOW

Type: read-write
Clock: PBUS_WRCLK
Reset State: 0x00
Reset Name: PBS_CORE_PERPH_RB

1' = Interrupt will trigger on a level low (falling edge) event, '0' = level low triggering is disabled

PBS_CLIENT4_INT_POLARITY_LOW

Bits	Name	Type	Description
1	SEQ_ENDED_LOW	read-write	
0	SEQ_ERROR_LOW	read-write	

0x7514 PBS_CLIENT4_INT_LATCHED_CLR

Type: write-only
Clock: PBUS_WRCLK
Reset State: 0x00
Reset Name: PBS_CORE_PERPH_RB

Writing a '1' to this interrupt will rearm the interrupt when an interrupt is pending. It clears the internal sticky and sent bits

PBS_CLIENT4_INT_LATCHED_CLR

Bits	Name	Type	Description
1	SEQ_ENDED_LATCHED_CLR	write-only	
0	SEQ_ERROR_LATCHED_CLR	write-only	

0x7515 PBS_CLIENT4_INT_EN_SET

Type: read-write
Clock: PBUS_WRCLK
Reset State: 0x00
Reset Name: PBS_CORE_PERPH_RB

Writing '0' to this register has no effect. Writing a '1' will enable the corresponding interrupt. Reading this register will readback enable status

PMIC_SET_MASK

PBS_CLIENT4_INT_EN_SET

Bits	Name	Type	Description
1	SEQ_ENDED_EN_SET	read-write	
0	SEQ_ERROR_EN_SET	read-write	

0x7516 PBS_CLIENT4_INT_EN_CLR

Type: read-write
Clock: PBUS_WRCLK
Reset State: 0x00
Reset Name: PBS_CORE_PERPH_RB

Writing '0' to this register has no effect. Writing a '1' will disable the corresponding interrupt. Reading this register will readback enable status

PMIC_CLR_MASK=INT_EN_SET

PBS_CLIENT4_INT_EN_CLR

Bits	Name	Type	Description
1	SEQ_ENDED_EN_CLR	read-write	

PBS_CLIENT4_INT_EN_CLR (Continued)

Bits	Name	Type	Description
0	SEQ_ERROR_EN_CLR	read-write	

0x7518 PBS_CLIENT4_INT_LATCHED_STS

Type: read-only
Clock: PBUS_WRCLK
Reset State: 0x00
Reset Name: PBS_CORE_PERPH_RB

Debug: Latched (Sticky) Interrupt. '1' indicates that the interrupt has triggered. Once the latched bit is set it can only be cleared by writing the clear bit.

PBS_CLIENT4_INT_LATCHED_STS

Bits	Name	Type	Description
1	SEQ_ENDED_LATCHED_STS	read-only	
0	SEQ_ERROR_LATCHED_STS	read-only	

0x7519 PBS_CLIENT4_INT_PENDING_STS

Type: read-only
Clock: PBUS_WRCLK
Reset State: 0x00
Reset Name: PBS_CORE_PERPH_RB

Debug: Pending is set if interrupt has been sent but not cleared.

PBS_CLIENT4_INT_PENDING_STS

Bits	Name	Type	Description
1	SEQ_ENDED_PENDING_STS	read-only	
0	SEQ_ERROR_PENDING_STS	read-only	

0x751A PBS_CLIENT4_INT_MID_SEL

Type: read-write
Clock: PBUS_WRCLK
Reset State: 0x00
Reset Name: PBS_CORE_PERPH_RB

Selects the MID that will receive the interrupt

PBS_CLIENT4_INT_MID_SEL

Bits	Name	Type	Description
1:0	INT_MID_SEL	read-write	

0x751B PBS_CLIENT4_INT_PRIORITY

Type: read-write
Clock: PBUS_WRCLK
Reset State: 0x00
Reset Name: PBS_CORE_PERPH_RB

SR=0 A=1

PBS_CLIENT4_INT_PRIORITY

Bits	Name	Type	Description
0	INT_PRIORITY	read-write	

0x7540 PBS_CLIENT4_TRIG_CFG

Type: read-write
Clock: PBUS_WRCLK
Reset State: 0x00
Reset Name: PBS_CORE_PERPH_RB

Trigger Configuration

PMIC_SYNC=pbs_clk:pbs_rb

PBS_CLIENT4_TRIG_CFG

Bits	Name	Type	Description
7	TRIGGER_RE_EN	read-write	1 = Enable Rising Edge Trigger 0 = Disable Falling Edge Trigger

PBS_CLIENT4_TRIG_CFG (Continued)

Bits	Name	Type	Description
6	TRIGGER_FE_EN	read-write	1 = Enable Falling Edge Trigger 0 = Disable Falling Edge Trigger

0x7542 PBS_CLIENT4_TRIG_CTL

Type: write-only
Clock: PBUS_WRCLK
Reset State: 0x00
Reset Name: PBS_CORE_PERPH_RB

PBS_CLIENT4_TRIG_CTL

Bits	Name	Type	Description
0	SW_TRIGGER	write-only	Writing 0x01 to this register will immediately create a trigger pulse.

0x7546 PBS_CLIENT4_EN_CTL

Type: read-write
Clock: PBUS_WRCLK
Reset State: 0x00
Reset Name: PBS_CORE_PERPH_RB

PMIC_SYNC=pbs_clk:pbs_rb

PBS_CLIENT4_EN_CTL

Bits	Name	Type	Description
7	TRIGGER_EN	read-write	Must be set to 1 to enable all triggers in the peripheral

6.7 PBS_CLIENT5_PBS_CLIENT

0x7604 PBS_CLIENT5_PERPH_TYPE

Type: read-only
Clock: PBUS_WRCLK
Reset State: 0x16
Reset Name: N/A

Peripheral Type

PBS_CLIENT5_PERPH_TYPE

Bits	Name	Type	Description
7:0	TYPE	read-only	PBS Reset State: 0x16

0x7605 PBS_CLIENT5_PERPH_SUBTYPE

Type: read-only
Clock: PBUS_WRCLK
Reset State: 0x08
Reset Name: N/A

Peripheral SubType

PBS_CLIENT5_PERPH_SUBTYPE

Bits	Name	Type	Description
7:0	SUBTYPE	read-only	Client 5 Reset State: 0x08

0x7608 PBS_CLIENT5_STATUS0

Type: read-only
Clock: PBUS_WRCLK
Reset State: 0bXXXXX000
Reset Name: N/A

Status Registers

PBS_CLIENT5_STATUS0

Bits	Name	Type	Description
7	TRIG_EN_STATUS	read-only	Overall trigger-sequence enable state

PBS_CLIENT5_STATUS0 (Continued)

Bits	Name	Type	Description
5:4	COMP_STATUS	read-only	These bits show the completion state of this client trigger-sequence pair. 00 = In execution. 01 = Normal completion 10 = Error completion. 11= Abort completion.
2:0	TRIG_FSM_STATUS	read-only	Show state of trigger slice FSM.

0x7610 PBS_CLIENT5_INT_RT_STS

Type: read-only
Clock: PBUS_WRCLK
Reset State: 0x00
Reset Name: PBS_CORE_PERPH_RB

Interrupt Real Time Status Bits

PBS_CLIENT5_INT_RT_STS

Bits	Name	Type	Description
1	SEQ_ENDED_RT_STS	read-only	
0	SEQ_ERROR_RT_STS	read-only	

0x7611 PBS_CLIENT5_INT_SET_TYPE

Type: read-write
Clock: PBUS_WRCLK
Reset State: 0x00
Reset Name: PBS_CORE_PERPH_RB

0 = use level trigger interrupts, 1 = use edge trigger interrupts

PBS_CLIENT5_INT_SET_TYPE

Bits	Name	Type	Description
1	SEQ_ENDED_TYPE	read-write	
0	SEQ_ERROR_TYPE	read-write	

0x7612 PBS_CLIENT5_INT_POLARITY_HIGH

Type: read-write
Clock: PBUS_WRCLK
Reset State: 0x00
Reset Name: PBS_CORE_PERPH_RB

1= Interrupt will trigger on a level high (rising edge) event, 0 = level high triggering is disabled

PBS_CLIENT5_INT_POLARITY_HIGH

Bits	Name	Type	Description
1	SEQ_ENDED_HIGH	read-write	
0	SEQ_ERROR_HIGH	read-write	

0x7613 PBS_CLIENT5_INT_POLARITY_LOW

Type: read-write
Clock: PBUS_WRCLK
Reset State: 0x00
Reset Name: PBS_CORE_PERPH_RB

1' = Interrupt will trigger on a level low (falling edge) event, '0' = level low triggering is disabled

PBS_CLIENT5_INT_POLARITY_LOW

Bits	Name	Type	Description
1	SEQ_ENDED_LOW	read-write	
0	SEQ_ERROR_LOW	read-write	

0x7614 PBS_CLIENT5_INT_LATCHED_CLR

Type: write-only
Clock: PBUS_WRCLK
Reset State: 0x00
Reset Name: PBS_CORE_PERPH_RB

Writing a '1' to this interrupt will rearm the interrupt when an interrupt is pending. It clears the internal sticky and sent bits

PBS_CLIENT5_INT_LATCHED_CLR

Bits	Name	Type	Description
1	SEQ_ENDED_LATCHED_CLR	write-only	
0	SEQ_ERROR_LATCHED_CLR	write-only	

0x7615 PBS_CLIENT5_INT_EN_SET

Type: read-write
Clock: PBUS_WRCLK
Reset State: 0x00
Reset Name: PBS_CORE_PERPH_RB

Writing '0' to this register has no effect. Writing a '1' will enable the corresponding interrupt. Reading this register will readback enable status

PMIC_SET_MASK

PBS_CLIENT5_INT_EN_SET

Bits	Name	Type	Description
1	SEQ_ENDED_EN_SET	read-write	
0	SEQ_ERROR_EN_SET	read-write	

0x7616 PBS_CLIENT5_INT_EN_CLR

Type: read-write
Clock: PBUS_WRCLK
Reset State: 0x00
Reset Name: PBS_CORE_PERPH_RB

Writing '0' to this register has no effect. Writing a '1' will disable the corresponding interrupt. Reading this register will readback enable status

PMIC_CLR_MASK=INT_EN_SET

PBS_CLIENT5_INT_EN_CLR

Bits	Name	Type	Description
1	SEQ_ENDED_EN_CLR	read-write	

PBS_CLIENT5_INT_EN_CLR (Continued)

Bits	Name	Type	Description
0	SEQ_ERROR_EN_CLR	read-write	

0x7618 PBS_CLIENT5_INT_LATCHED_STS

Type: read-only
Clock: PBUS_WRCLK
Reset State: 0x00
Reset Name: PBS_CORE_PERPH_RB

Debug: Latched (Sticky) Interrupt. '1' indicates that the interrupt has triggered. Once the latched bit is set it can only be cleared by writing the clear bit.

PBS_CLIENT5_INT_LATCHED_STS

Bits	Name	Type	Description
1	SEQ_ENDED_LATCHED_STS	read-only	
0	SEQ_ERROR_LATCHED_STS	read-only	

0x7619 PBS_CLIENT5_INT_PENDING_STS

Type: read-only
Clock: PBUS_WRCLK
Reset State: 0x00
Reset Name: PBS_CORE_PERPH_RB

Debug: Pending is set if interrupt has been sent but not cleared.

PBS_CLIENT5_INT_PENDING_STS

Bits	Name	Type	Description
1	SEQ_ENDED_PENDING_STS	read-only	
0	SEQ_ERROR_PENDING_STS	read-only	

0x761A PBS_CLIENT5_INT_MID_SEL

Type: read-write
Clock: PBUS_WRCLK
Reset State: 0x00
Reset Name: PBS_CORE_PERPH_RB

Selects the MID that will receive the interrupt

PBS_CLIENT5_INT_MID_SEL

Bits	Name	Type	Description
1:0	INT_MID_SEL	read-write	

0x761B PBS_CLIENT5_INT_PRIORITY

Type: read-write
Clock: PBUS_WRCLK
Reset State: 0x00
Reset Name: PBS_CORE_PERPH_RB

SR=0 A=1

PBS_CLIENT5_INT_PRIORITY

Bits	Name	Type	Description
0	INT_PRIORITY	read-write	

0x7640 PBS_CLIENT5_TRIG_CFG

Type: read-write
Clock: PBUS_WRCLK
Reset State: 0x00
Reset Name: PBS_CORE_PERPH_RB

Trigger Configuration

PMIC_SYNC=pbs_clk:pbs_rb

PBS_CLIENT5_TRIG_CFG

Bits	Name	Type	Description
7	TRIGGER_RE_EN	read-write	1 = Enable Rising Edge Trigger 0 = Disable Falling Edge Trigger

PBS_CLIENT5_TRIG_CFG (Continued)

Bits	Name	Type	Description
6	TRIGGER_FE_EN	read-write	1 = Enable Falling Edge Trigger 0 = Disable Falling Edge Trigger

0x7642 PBS_CLIENT5_TRIG_CTL

Type: write-only
Clock: PBUS_WRCLK
Reset State: 0x00
Reset Name: PBS_CORE_PERPH_RB

PBS_CLIENT5_TRIG_CTL

Bits	Name	Type	Description
0	SW_TRIGGER	write-only	Writing 0x01 to this register will immediately create a trigger pulse.

0x7646 PBS_CLIENT5_EN_CTL

Type: read-write
Clock: PBUS_WRCLK
Reset State: 0x00
Reset Name: PBS_CORE_PERPH_RB

PMIC_SYNC=pbs_clk:pbs_rb

PBS_CLIENT5_EN_CTL

Bits	Name	Type	Description
7	TRIGGER_EN	read-write	Must be set to 1 to enable all triggers in the peripheral

6.8 PBS_CLIENT6_PBS_CLIENT

0x7704 PBS_CLIENT6_PERPH_TYPE

Type: read-only
Clock: PBUS_WRCLK
Reset State: 0x16
Reset Name: N/A

Peripheral Type

PBS_CLIENT6_PERPH_TYPE

Bits	Name	Type	Description
7:0	TYPE	read-only	PBS Reset State: 0x16

0x7705 PBS_CLIENT6_PERPH_SUBTYPE

Type: read-only
Clock: PBUS_WRCLK
Reset State: 0x08
Reset Name: N/A

Peripheral SubType

PBS_CLIENT6_PERPH_SUBTYPE

Bits	Name	Type	Description
7:0	SUBTYPE	read-only	Client 6 Reset State: 0x08

0x7708 PBS_CLIENT6_STATUS0

Type: read-only
Clock: PBUS_WRCLK
Reset State: 0bXXXXX000
Reset Name: N/A

Status Registers

PBS_CLIENT6_STATUS0

Bits	Name	Type	Description
7	TRIG_EN_STATUS	read-only	Overall trigger-sequence enable state

PBS_CLIENT6_STATUS0 (Continued)

Bits	Name	Type	Description
5:4	COMP_STATUS	read-only	These bits show the completion state of this client trigger-sequence pair. 00 = In execution. 01 = Normal completion 10 = Error completion. 11= Abort completion.
2:0	TRIG_FSM_STATUS	read-only	Show state of trigger slice FSM.

0x7710 PBS_CLIENT6_INT_RT_STS

Type: read-only
Clock: PBUS_WRCLK
Reset State: 0x00
Reset Name: PBS_CORE_PERPH_RB

Interrupt Real Time Status Bits

PBS_CLIENT6_INT_RT_STS

Bits	Name	Type	Description
1	SEQ_ENDED_RT_STS	read-only	
0	SEQ_ERROR_RT_STS	read-only	

0x7711 PBS_CLIENT6_INT_SET_TYPE

Type: read-write
Clock: PBUS_WRCLK
Reset State: 0x00
Reset Name: PBS_CORE_PERPH_RB

0 = use level trigger interrupts, 1 = use edge trigger interrupts

PBS_CLIENT6_INT_SET_TYPE

Bits	Name	Type	Description
1	SEQ_ENDED_TYPE	read-write	
0	SEQ_ERROR_TYPE	read-write	

0x7712 PBS_CLIENT6_INT_POLARITY_HIGH

Type: read-write
Clock: PBUS_WRCLK
Reset State: 0x00
Reset Name: PBS_CORE_PERPH_RB

1= Interrupt will trigger on a level high (rising edge) event, 0 = level high triggering is disabled

PBS_CLIENT6_INT_POLARITY_HIGH

Bits	Name	Type	Description
1	SEQ_ENDED_HIGH	read-write	
0	SEQ_ERROR_HIGH	read-write	

0x7713 PBS_CLIENT6_INT_POLARITY_LOW

Type: read-write
Clock: PBUS_WRCLK
Reset State: 0x00
Reset Name: PBS_CORE_PERPH_RB

1' = Interrupt will trigger on a level low (falling edge) event, '0' = level low triggering is disabled

PBS_CLIENT6_INT_POLARITY_LOW

Bits	Name	Type	Description
1	SEQ_ENDED_LOW	read-write	
0	SEQ_ERROR_LOW	read-write	

0x7714 PBS_CLIENT6_INT_LATCHED_CLR

Type: write-only
Clock: PBUS_WRCLK
Reset State: 0x00
Reset Name: PBS_CORE_PERPH_RB

Writing a '1' to this interrupt will rearm the interrupt when an interrupt is pending. It clears the internal sticky and sent bits

PBS_CLIENT6_INT_LATCHED_CLR

Bits	Name	Type	Description
1	SEQ_ENDED_LATCHED_CLR	write-only	
0	SEQ_ERROR_LATCHED_CLR	write-only	

0x7715 PBS_CLIENT6_INT_EN_SET

Type: read-write
Clock: PBUS_WRCLK
Reset State: 0x00
Reset Name: PBS_CORE_PERPH_RB

Writing '0' to this register has no effect. Writing a '1' will enable the corresponding interrupt. Reading this register will readback enable status

PMIC_SET_MASK

PBS_CLIENT6_INT_EN_SET

Bits	Name	Type	Description
1	SEQ_ENDED_EN_SET	read-write	
0	SEQ_ERROR_EN_SET	read-write	

0x7716 PBS_CLIENT6_INT_EN_CLR

Type: read-write
Clock: PBUS_WRCLK
Reset State: 0x00
Reset Name: PBS_CORE_PERPH_RB

Writing '0' to this register has no effect. Writing a '1' will disable the corresponding interrupt. Reading this register will readback enable status

PMIC_CLR_MASK=INT_EN_SET

PBS_CLIENT6_INT_EN_CLR

Bits	Name	Type	Description
1	SEQ_ENDED_EN_CLR	read-write	

PBS_CLIENT6_INT_EN_CLR (Continued)

Bits	Name	Type	Description
0	SEQ_ERROR_EN_CLR	read-write	

0x7718 PBS_CLIENT6_INT_LATCHED_STS

Type: read-only
Clock: PBUS_WRCLK
Reset State: 0x00
Reset Name: PBS_CORE_PERPH_RB

Debug: Latched (Sticky) Interrupt. '1' indicates that the interrupt has triggered. Once the latched bit is set it can only be cleared by writing the clear bit.

PBS_CLIENT6_INT_LATCHED_STS

Bits	Name	Type	Description
1	SEQ_ENDED_LATCHED_STS	read-only	
0	SEQ_ERROR_LATCHED_STS	read-only	

0x7719 PBS_CLIENT6_INT_PENDING_STS

Type: read-only
Clock: PBUS_WRCLK
Reset State: 0x00
Reset Name: PBS_CORE_PERPH_RB

Debug: Pending is set if interrupt has been sent but not cleared.

PBS_CLIENT6_INT_PENDING_STS

Bits	Name	Type	Description
1	SEQ_ENDED_PENDING_STS	read-only	
0	SEQ_ERROR_PENDING_STS	read-only	

0x771A PBS_CLIENT6_INT_MID_SEL

Type: read-write
Clock: PBUS_WRCLK
Reset State: 0x00
Reset Name: PBS_CORE_PERPH_RB

Selects the MID that will receive the interrupt

PBS_CLIENT6_INT_MID_SEL

Bits	Name	Type	Description
1:0	INT_MID_SEL	read-write	

0x771B PBS_CLIENT6_INT_PRIORITY

Type: read-write
Clock: PBUS_WRCLK
Reset State: 0x00
Reset Name: PBS_CORE_PERPH_RB

SR=0 A=1

PBS_CLIENT6_INT_PRIORITY

Bits	Name	Type	Description
0	INT_PRIORITY	read-write	

0x7740 PBS_CLIENT6_TRIG_CFG

Type: read-write
Clock: PBUS_WRCLK
Reset State: 0x00
Reset Name: PBS_CORE_PERPH_RB

Trigger Configuration

PMIC_SYNC=pbs_clk:pbs_rb

PBS_CLIENT6_TRIG_CFG

Bits	Name	Type	Description
7	TRIGGER_RE_EN	read-write	1 = Enable Rising Edge Trigger 0 = Disable Falling Edge Trigger

PBS_CLIENT6_TRIG_CFG (Continued)

Bits	Name	Type	Description
6	TRIGGER_FE_EN	read-write	1 = Enable Falling Edge Trigger 0 = Disable Falling Edge Trigger

0x7742 PBS_CLIENT6_TRIG_CTL

Type: write-only
Clock: PBUS_WRCLK
Reset State: 0x00
Reset Name: PBS_CORE_PERPH_RB

PBS_CLIENT6_TRIG_CTL

Bits	Name	Type	Description
0	SW_TRIGGER	write-only	Writing 0x01 to this register will immediately create a trigger pulse.

0x7746 PBS_CLIENT6_EN_CTL

Type: read-write
Clock: PBUS_WRCLK
Reset State: 0x00
Reset Name: PBS_CORE_PERPH_RB

PMIC_SYNC=pbs_clk:pbs_rb

PBS_CLIENT6_EN_CTL

Bits	Name	Type	Description
7	TRIGGER_EN	read-write	Must be set to 1 to enable all triggers in the peripheral

6.9 PBS_CLIENT7_PBS_CLIENT

0x7804 PBS_CLIENT7_PERPH_TYPE

Type: read-only
Clock: PBUS_WRCLK
Reset State: 0x16
Reset Name: N/A

Peripheral Type

PBS_CLIENT7_PERPH_TYPE

Bits	Name	Type	Description
7:0	TYPE	read-only	PBS Reset State: 0x16

0x7805 PBS_CLIENT7_PERPH_SUBTYPE

Type: read-only
Clock: PBUS_WRCLK
Reset State: 0x08
Reset Name: N/A

Peripheral SubType

PBS_CLIENT7_PERPH_SUBTYPE

Bits	Name	Type	Description
7:0	SUBTYPE	read-only	Client 7 Reset State: 0x08

0x7808 PBS_CLIENT7_STATUS0

Type: read-only
Clock: PBUS_WRCLK
Reset State: 0bXXXXX000
Reset Name: N/A

Status Registers

PBS_CLIENT7_STATUS0

Bits	Name	Type	Description
7	TRIG_EN_STATUS	read-only	Overall trigger-sequence enable state

PBS_CLIENT7_STATUS0 (Continued)

Bits	Name	Type	Description
5:4	COMP_STATUS	read-only	These bits show the completion state of this client trigger-sequence pair. 00 = In execution. 01 = Normal completion 10 = Error completion. 11= Abort completion.
2:0	TRIG_FSM_STATUS	read-only	Show state of trigger slice FSM.

0x7810 PBS_CLIENT7_INT_RT_STS

Type: read-only
Clock: PBUS_WRCLK
Reset State: 0x00
Reset Name: PBS_CORE_PERPH_RB

Interrupt Real Time Status Bits

PBS_CLIENT7_INT_RT_STS

Bits	Name	Type	Description
1	SEQ_ENDED_RT_STS	read-only	
0	SEQ_ERROR_RT_STS	read-only	

0x7811 PBS_CLIENT7_INT_SET_TYPE

Type: read-write
Clock: PBUS_WRCLK
Reset State: 0x00
Reset Name: PBS_CORE_PERPH_RB

0 = use level trigger interrupts, 1 = use edge trigger interrupts

PBS_CLIENT7_INT_SET_TYPE

Bits	Name	Type	Description
1	SEQ_ENDED_TYPE	read-write	
0	SEQ_ERROR_TYPE	read-write	

0x7812 PBS_CLIENT7_INT_POLARITY_HIGH

Type: read-write
Clock: PBUS_WRCLK
Reset State: 0x00
Reset Name: PBS_CORE_PERPH_RB

1= Interrupt will trigger on a level high (rising edge) event, 0 = level high triggering is disabled

PBS_CLIENT7_INT_POLARITY_HIGH

Bits	Name	Type	Description
1	SEQ_ENDED_HIGH	read-write	
0	SEQ_ERROR_HIGH	read-write	

0x7813 PBS_CLIENT7_INT_POLARITY_LOW

Type: read-write
Clock: PBUS_WRCLK
Reset State: 0x00
Reset Name: PBS_CORE_PERPH_RB

1' = Interrupt will trigger on a level low (falling edge) event, '0' = level low triggering is disabled

PBS_CLIENT7_INT_POLARITY_LOW

Bits	Name	Type	Description
1	SEQ_ENDED_LOW	read-write	
0	SEQ_ERROR_LOW	read-write	

0x7814 PBS_CLIENT7_INT_LATCHED_CLR

Type: write-only
Clock: PBUS_WRCLK
Reset State: 0x00
Reset Name: PBS_CORE_PERPH_RB

Writing a '1' to this interrupt will rearm the interrupt when an interrupt is pending. It clears the internal sticky and sent bits

PBS_CLIENT7_INT_LATCHED_CLR

Bits	Name	Type	Description
1	SEQ_ENDED_LATCHED_CLR	write-only	
0	SEQ_ERROR_LATCHED_CLR	write-only	

0x7815 PBS_CLIENT7_INT_EN_SET

Type: read-write
Clock: PBUS_WRCLK
Reset State: 0x00
Reset Name: PBS_CORE_PERPH_RB

Writing '0' to this register has no effect. Writing a '1' will enable the corresponding interrupt. Reading this register will readback enable status

PMIC_SET_MASK

PBS_CLIENT7_INT_EN_SET

Bits	Name	Type	Description
1	SEQ_ENDED_EN_SET	read-write	
0	SEQ_ERROR_EN_SET	read-write	

0x7816 PBS_CLIENT7_INT_EN_CLR

Type: read-write
Clock: PBUS_WRCLK
Reset State: 0x00
Reset Name: PBS_CORE_PERPH_RB

Writing '0' to this register has no effect. Writing a '1' will disable the corresponding interrupt. Reading this register will readback enable status

PMIC_CLR_MASK=INT_EN_SET

PBS_CLIENT7_INT_EN_CLR

Bits	Name	Type	Description
1	SEQ_ENDED_EN_CLR	read-write	

PBS_CLIENT7_INT_EN_CLR (Continued)

Bits	Name	Type	Description
0	SEQ_ERROR_EN_CLR	read-write	

0x7818 PBS_CLIENT7_INT_LATCHED_STS

Type: read-only
Clock: PBUS_WRCLK
Reset State: 0x00
Reset Name: PBS_CORE_PERPH_RB

Debug: Latched (Sticky) Interrupt. '1' indicates that the interrupt has triggered. Once the latched bit is set it can only be cleared by writing the clear bit.

PBS_CLIENT7_INT_LATCHED_STS

Bits	Name	Type	Description
1	SEQ_ENDED_LATCHED_STS	read-only	
0	SEQ_ERROR_LATCHED_STS	read-only	

0x7819 PBS_CLIENT7_INT_PENDING_STS

Type: read-only
Clock: PBUS_WRCLK
Reset State: 0x00
Reset Name: PBS_CORE_PERPH_RB

Debug: Pending is set if interrupt has been sent but not cleared.

PBS_CLIENT7_INT_PENDING_STS

Bits	Name	Type	Description
1	SEQ_ENDED_PENDING_STS	read-only	
0	SEQ_ERROR_PENDING_STS	read-only	

0x781A PBS_CLIENT7_INT_MID_SEL

Type: read-write
Clock: PBUS_WRCLK
Reset State: 0x00
Reset Name: PBS_CORE_PERPH_RB

Selects the MID that will receive the interrupt

PBS_CLIENT7_INT_MID_SEL

Bits	Name	Type	Description
1:0	INT_MID_SEL	read-write	

0x781B PBS_CLIENT7_INT_PRIORITY

Type: read-write
Clock: PBUS_WRCLK
Reset State: 0x00
Reset Name: PBS_CORE_PERPH_RB

SR=0 A=1

PBS_CLIENT7_INT_PRIORITY

Bits	Name	Type	Description
0	INT_PRIORITY	read-write	

0x7840 PBS_CLIENT7_TRIG_CFG

Type: read-write
Clock: PBUS_WRCLK
Reset State: 0x00
Reset Name: PBS_CORE_PERPH_RB

Trigger Configuration

PMIC_SYNC=pbs_clk:pbs_rb

PBS_CLIENT7_TRIG_CFG

Bits	Name	Type	Description
7	TRIGGER_RE_EN	read-write	1 = Enable Rising Edge Trigger 0 = Disable Falling Edge Trigger

PBS_CLIENT7_TRIG_CFG (Continued)

Bits	Name	Type	Description
6	TRIGGER_FE_EN	read-write	1 = Enable Falling Edge Trigger 0 = Disable Falling Edge Trigger

0x7842 PBS_CLIENT7_TRIG_CTL

Type: write-only
Clock: PBUS_WRCLK
Reset State: 0x00
Reset Name: PBS_CORE_PERPH_RB

PBS_CLIENT7_TRIG_CTL

Bits	Name	Type	Description
0	SW_TRIGGER	write-only	Writing 0x01 to this register will immediately create a trigger pulse.

0x7846 PBS_CLIENT7_EN_CTL

Type: read-write
Clock: PBUS_WRCLK
Reset State: 0x00
Reset Name: PBS_CORE_PERPH_RB

PMIC_SYNC=pbs_clk:pbs_rb

PBS_CLIENT7_EN_CTL

Bits	Name	Type	Description
7	TRIGGER_EN	read-write	Must be set to 1 to enable all triggers in the peripheral

7 MPPn

7.1 Overview

Table 7-1 Blocks

Name
MPP1
MPP2
MPP3
MPP4

7.2 MPP1_MPP

0xA004 MPP1_PERPH_TYPE

Type: read-only
Clock: PBUS_WRCLK
Reset State: 0x11
Reset Name: N/A

Peripheral Type

MPP1_PERPH_TYPE

Bits	Name	Type	Description
7:0	TYPE	read-only	MPP

0xA005 MPP1_PERPH_SUBTYPE

Type: read-only
Clock: PBUS_WRCLK
Reset State: 0x05
Reset Name: N/A

Peripheral SubType

MPP1_PERPH_SUBTYPE

Bits	Name	Type	Description
7:0	SUBTYPE	read-only	MPP

0xA008 MPP1_STATUS1

Type: read-only
Clock: PBUS_WRCLK
Reset State: Undefined
Reset Name: N/A

Status Registers

MPP1_STATUS1

Bits	Name	Type	Description
7	MPP_OK	read-only	0 = GPIO is disabled 1 = GPIO is enabled

MPP1_STATUS1 (Continued)

Bits	Name	Type	Description
0	MPP_VAL	read-only	Value read by the input buffer, if enabled

0xA010 MPP1_INT_RT_STS

Type: read-only
Clock: PBUS_WRCLK
Reset State: 0x00
Reset Name: N/A

Interrupt Real Time Status Bits

MPP1_INT_RT_STS

Bits	Name	Type	Description
0	MPP_IN_STS	read-only	

0xA011 MPP1_INT_SET_TYPE

Type: read-write
Clock: PBUS_WRCLK
Reset State: 0x00
Reset Name: PERPH_RB

0 = use level trigger interrupts, 1 = use edge trigger interrupts

MPP1_INT_SET_TYPE

Bits	Name	Type	Description
0	MPP_IN_TYPE	read-write	

0xA012 MPP1_INT_POLARITY_HIGH

Type: read-write
Clock: PBUS_WRCLK
Reset State: 0x00
Reset Name: PERPH_RB

1= Interrupt will trigger on a level high (rising edge) event, 0 = level high triggering is disabled

MPP1_INT_POLARITY_HIGH

Bits	Name	Type	Description
0	MPP_IN_HIGH	read-write	

0xA013 MPP1_INT_POLARITY_LOW

Type: read-write
Clock: PBUS_WRCLK
Reset State: 0x00
Reset Name: PERPH_RB

1' = Interrupt will trigger on a level low (falling edge) event, '0' = level low triggering is disabled

MPP1_INT_POLARITY_LOW

Bits	Name	Type	Description
0	MPP_IN_LOW	read-write	

0xA014 MPP1_INT_LATCHED_CLR

Type: write-only
Clock: PBUS_WRCLK
Reset State: 0x00
Reset Name: PERPH_RB

Writing a '1' to this interrupt will rearm the interrupt when an interrupt is pending. It clears the internal sticky and sent bits

MPP1_INT_LATCHED_CLR

Bits	Name	Type	Description
0	MPP_IN_LATCHED_CLR	write-only	

0xA015 MPP1_INT_EN_SET

Type: read-write
Clock: PBUS_WRCLK
Reset State: 0x00
Reset Name: PERPH_RB

Writing '0' to this register has no effect. Writing a '1' will enable the corresponding interrupt. Reading this register will readback enable status

PMIC_SET_MASK

MPP1_INT_EN_SET

Bits	Name	Type	Description
0	MPP_IN_EN_SET	read-write	

0xA016 MPP1_INT_EN_CLR

Type: read-write
Clock: PBUS_WRCLK
Reset State: 0x00
Reset Name: PERPH_RB

Writing '0' to this register has no effect. Writing a '1' will disable the corresponding interrupt. Reading this register will readback enable status

PMIC_CLR_MASK=INT_EN_SET

MPP1_INT_EN_CLR

Bits	Name	Type	Description
0	MPP_IN_EN_CLR	read-write	

0xA018 MPP1_INT_LATCHED_STS

Type: read-only
Clock: PBUS_WRCLK
Reset State: 0x00
Reset Name: N/A

Latched (Sticky) Interrupt. '1' indicates that the interrupt has triggered. Once the latched bit is set it can only be cleared by writing the clear bit.

MPP1_INT_LATCHED_STS

Bits	Name	Type	Description
0	MPP_IN_LATCHED_STS	read-only	

0xA019 MPP1_INT_PENDING_STS

Type: read-only
Clock: PBUS_WRCLK
Reset State: 0x00
Reset Name: N/A

Debug: Pending is set if interrupt has been sent but not cleared.

MPP1_INT_PENDING_STS

Bits	Name	Type	Description
0	MPP_IN_PENDING_STS	read-only	

0xA01A MPP1_INT_MID_SEL

Type: read-write
Clock: PBUS_WRCLK
Reset State: 0x00
Reset Name: PERPH_RB

Selects the MID that will receive the interrupt

MPP1_INT_MID_SEL

Bits	Name	Type	Description
1:0	INT_MID_SEL	read-write	

0xA01B MPP1_INT_PRIORITY

Type: read-write
Clock: PBUS_WRCLK
Reset State: 0x00
Reset Name: PERPH_RB

SR=0 A=1

MPP1_INT_PRIORITY

Bits	Name	Type	Description
0	INT_PRIORITY	read-write	

0xA040 MPP1_MODE_CTL

Type: read-write
Clock: PBUS_WRCLK
Reset State: 0x00
Reset Name: PERPH_RB

MPP Mode allows you to switch from one mode to another mode in a single register write.

MPP1_MODE_CTL

Bits	Name	Type	Description
6:4	MODE	read-write	MPP Type: 0: Digital Input 1: Digital Output 2: Digital Input and Digital Output 3: Bidirectional Logic 4: Analog Input 5: Analog Output 6: Current Sink 7: Reserved

MPP1_MODE_CTL (Continued)

Bits	Name	Type	Description
3:0	EN_AND_SOURCE_SEL	read-write	When configured as a digital output Source select: 0000 = 0 0001 = 1 0010 = paired MPP 0011 = inverted paired MPP 0100 = Reserved 0101 = Reserved 0110 = Reserved 0111 = Reserved 1000 = DTEST1 1001 = inverted DTEST1 1010 = DTEST2 1011 = inverted DTEST2 1100 = DTEST3 1101 = inverted DTEST3 1110 = DTEST4 1111 = inverted DTEST4 Enable control when configured as Bidirectional, AIN, AOUT, or Current Sink. MPP is enable whenever the selected condition is true. 0000 = 0 (mpp is always disabled) 0001 = 1 (mpp is always Enabled) 0010 = paired MPP 0011 = inverted paired MPP 0100 = Reserved 0101 = Reserved 0110 = Reserved 0111 = Reserved 1000 = DTEST1 1001 = inverted DTEST1 1010 = DTEST2 1011 = inverted DTEST2 1100 = DTEST3 1101 = inverted DTEST3 1110 = DTEST4 1111 = inverted DTEST4

0xA041 MPP1_DIG_VIN_CTL

Type: read-write
Clock: PBUS_WRCLK
Reset State: 0x00
Reset Name: PERPH_RB

MPP1_DIG_VIN_CTL

Bits	Name	Type	Description
2:0	VOLTAGE_SEL	read-write	Digital I/O mode: 000 = VIN0 (refer to the objective spec.) 001 = VIN1 (refer to the objective spec.) 010 = VIN2 (refer to the objective spec.)* 011 = VIN3 (refer to the objective spec.) 100 = VIN4 (refer to the objective spec.)* 101 = VIN5 (refer to the objective spec.) 110 = VIN6 (refer to the objective spec.) 111 = VIN7 (refer to the objective spec.)

0xA042 MPP1_DIG_PULL_CTL

Type: read-write
Clock: PBUS_WRCLK
Reset State: 0x00
Reset Name: PERPH_RB

MPP1_DIG_PULL_CTL

Bits	Name	Type	Description
2:0	PULLUP_SEL	read-write	Pullup Resistor Control in bidirectional mode only. 00: 0.6k? ** 01: 10 k? 10: 30 k? 11: Open (infinite resistance) *

0xA046 MPP1_EN_CTL

Type: read-write
Clock: PBUS_WRCLK
Reset State: 0x00
Reset Name: PERPH_RB

MPP1_EN_CTL

Bits	Name	Type	Description
7	PERPH_EN	read-write	MPP Master enable 0 = puts MPP_PAD at high Z and disables the block 1 = MPP is enabled

0xA048 MPP1_ANA_OUT_CTL

Type: read-write
Clock: PBUS_WRCLK
Reset State: 0x00
Reset Name: PERPH_RB

MPP1_ANA_OUT_CTL

Bits	Name	Type	Description
2:0	REF_SEL	read-write	Analog Output Control 0: Output = vref_1V25 = REF_BYP pin, typically 1.25 Volts

0xA04A MPP1_ANA_IN_CTL

Type: read-write
Clock: PBUS_WRCLK
Reset State: 0x00
Reset Name: PERPH_RB

MPP1_ANA_IN_CTL

Bits	Name	Type	Description
2:0	ROUTE_SEL	read-write	AMUX Channel Control 0: Route to AMUX5 1: Route to AMUX6 2: Route to AMUX7 3: Route to AMUX8 4 to 7: Reserved

0xA04C MPP1_SINK_CTL

Type: read-write
Clock: PBUS_WRCLK
Reset State: 0x00
Reset Name: PERPH_RB

MPP1_SINK_CTL

Bits	Name	Type	Description
2:0	CURRENT_SEL	read-write	Current Sink Output Control 0: Output = 5 mA 1: Output = 10 mA 2: Output = 15 mA 3: Output = 20 mA 4: Output = 25 mA 5: Output = 30 mA 6: Output = 35 mA 7: Output = 40 mA

7.3 MPP2_MPP

0xA104 MPP2_PERPH_TYPE

Type: read-only
Clock: PBUS_WRCLK
Reset State: 0x11
Reset Name: N/A

Peripheral Type

MPP2_PERPH_TYPE

Bits	Name	Type	Description
7:0	TYPE	read-only	MPP

0xA105 MPP2_PERPH_SUBTYPE

Type: read-only
Clock: PBUS_WRCLK
Reset State: 0x03
Reset Name: N/A

Peripheral SubType

MPP2_PERPH_SUBTYPE

Bits	Name	Type	Description
7:0	SUBTYPE	read-only	MPP

0xA108 MPP2_STATUS1

Type: read-only
Clock: PBUS_WRCLK
Reset State: Undefined
Reset Name: N/A

Status Registers

MPP2_STATUS1

Bits	Name	Type	Description
7	MPP_OK	read-only	0 = GPIO is disabled 1 = GPIO is enabled

MPP2_STATUS1 (Continued)

Bits	Name	Type	Description
0	MPP_VAL	read-only	Value read by the input buffer, if enabled

0xA110 MPP2_INT_RT_STS

Type: read-only
Clock: PBUS_WRCLK
Reset State: 0x00
Reset Name: N/A

Interrupt Real Time Status Bits

MPP2_INT_RT_STS

Bits	Name	Type	Description
0	MPP_IN_STS	read-only	

0xA111 MPP2_INT_SET_TYPE

Type: read-write
Clock: PBUS_WRCLK
Reset State: 0x00
Reset Name: PERPH_RB

0 = use level trigger interrupts, 1 = use edge trigger interrupts

MPP2_INT_SET_TYPE

Bits	Name	Type	Description
0	MPP_IN_TYPE	read-write	

0xA112 MPP2_INT_POLARITY_HIGH

Type: read-write
Clock: PBUS_WRCLK
Reset State: 0x00
Reset Name: PERPH_RB

1= Interrupt will trigger on a level high (rising edge) event, 0 = level high triggering is disabled

MPP2_INT_POLARITY_HIGH

Bits	Name	Type	Description
0	MPP_IN_HIGH	read-write	

0xA113 MPP2_INT_POLARITY_LOW

Type: read-write
Clock: PBUS_WRCLK
Reset State: 0x00
Reset Name: PERPH_RB

1' = Interrupt will trigger on a level low (falling edge) event, '0' = level low triggering is disabled

MPP2_INT_POLARITY_LOW

Bits	Name	Type	Description
0	MPP_IN_LOW	read-write	

0xA114 MPP2_INT_LATCHED_CLR

Type: write-only
Clock: PBUS_WRCLK
Reset State: 0x00
Reset Name: PERPH_RB

Writing a '1' to this interrupt will rearm the interrupt when an interrupt is pending. It clears the internal sticky and sent bits

MPP2_INT_LATCHED_CLR

Bits	Name	Type	Description
0	MPP_IN_LATCHED_CLR	write-only	

0xA115 MPP2_INT_EN_SET

Type: read-write
Clock: PBUS_WRCLK
Reset State: 0x00
Reset Name: PERPH_RB

Writing '0' to this register has no effect. Writing a '1' will enable the corresponding interrupt. Reading this register will readback enable status

PMIC_SET_MASK

MPP2_INT_EN_SET

Bits	Name	Type	Description
0	MPP_IN_EN_SET	read-write	

0xA116 MPP2_INT_EN_CLR

Type: read-write
Clock: PBUS_WRCLK
Reset State: 0x00
Reset Name: PERPH_RB

Writing '0' to this register has no effect. Writing a '1' will disable the corresponding interrupt. Reading this register will readback enable status

PMIC_CLR_MASK=INT_EN_SET

MPP2_INT_EN_CLR

Bits	Name	Type	Description
0	MPP_IN_EN_CLR	read-write	

0xA118 MPP2_INT_LATCHED_STS

Type: read-only
Clock: PBUS_WRCLK
Reset State: 0x00
Reset Name: N/A

Latched (Sticky) Interrupt. '1' indicates that the interrupt has triggered. Once the latched bit is set it can only be cleared by writing the clear bit.

MPP2_INT_LATCHED_STS

Bits	Name	Type	Description
0	MPP_IN_LATCHED_STS	read-only	

0xA119 MPP2_INT_PENDING_STS

Type: read-only
Clock: PBUS_WRCLK
Reset State: 0x00
Reset Name: N/A

Debug: Pending is set if interrupt has been sent but not cleared.

MPP2_INT_PENDING_STS

Bits	Name	Type	Description
0	MPP_IN_PENDING_STS	read-only	

0xA11A MPP2_INT_MID_SEL

Type: read-write
Clock: PBUS_WRCLK
Reset State: 0x00
Reset Name: PERPH_RB

Selects the MID that will receive the interrupt

MPP2_INT_MID_SEL

Bits	Name	Type	Description
1:0	INT_MID_SEL	read-write	

0xA11B MPP2_INT_PRIORITY

Type: read-write
Clock: PBUS_WRCLK
Reset State: 0x00
Reset Name: PERPH_RB

SR=0 A=1

MPP2_INT_PRIORITY

Bits	Name	Type	Description
0	INT_PRIORITY	read-write	

0xA140 MPP2_MODE_CTL

Type: read-write
Clock: PBUS_WRCLK
Reset State: 0x00
Reset Name: PERPH_RB

MPP Mode allows you to switch from one mode to another mode in a single register write.

MPP2_MODE_CTL

Bits	Name	Type	Description
6:4	MODE	read-write	MPP Type: 0: Digital Input 1: Digital Output 2: Digital Input and Digital Output 3: Bidirectional Logic 4: Analog Input 5: Analog Output 6: Current Sink 7: Reserved

MPP2_MODE_CTL (Continued)

Bits	Name	Type	Description
3:0	EN_AND_SOURCE_SEL	read-write	When configured as a digital output Source select: 0000 = 0 0001 = 1 0010 = paired MPP 0011 = inverted paired MPP 0100 = Reserved 0101 = Reserved 0110 = Reserved 0111 = Reserved 1000 = DTEST1 1001 = inverted DTEST1 1010 = DTEST2 1011 = inverted DTEST2 1100 = DTEST3 1101 = inverted DTEST3 1110 = DTEST4 1111 = inverted DTEST4 Enable control when configured as Bidirectional, AIN, AOUT, or Current Sink. MPP is enable whenever the selected condition is true. 0000 = 0 (mpp is always disabled) 0001 = 1 (mpp is always Enabled) 0010 = paired MPP 0011 = inverted paired MPP 0100 = Reserved 0101 = Reserved 0110 = Reserved 0111 = Reserved 1000 = DTEST1 1001 = inverted DTEST1 1010 = DTEST2 1011 = inverted DTEST2 1100 = DTEST3 1101 = inverted DTEST3 1110 = DTEST4 1111 = inverted DTEST4

0xA141 MPP2_DIG_VIN_CTL

Type: read-write
Clock: PBUS_WRCLK
Reset State: 0x00
Reset Name: PERPH_RB

MPP2_DIG_VIN_CTL

Bits	Name	Type	Description
2:0	VOLTAGE_SEL	read-write	Digital I/O mode: 000 = VIN0 (refer to the objective spec.) 001 = VIN1 (refer to the objective spec.) 010 = VIN2 (refer to the objective spec.)* 011 = VIN3 (refer to the objective spec.) 100 = VIN4 (refer to the objective spec.)* 101 = VIN5 (refer to the objective spec.) 110 = VIN6 (refer to the objective spec.) 111 = VIN7 (refer to the objective spec.)

0xA142 MPP2_DIG_PULL_CTL

Type: read-write
Clock: PBUS_WRCLK
Reset State: 0x00
Reset Name: PERPH_RB

MPP2_DIG_PULL_CTL

Bits	Name	Type	Description
2:0	PULLUP_SEL	read-write	Pullup Resistor Control in bidirectional mode only. 00: 0.6k? ** 01: 10 k? 10: 30 k? 11: Open (infinite resistance) *

0xA146 MPP2_EN_CTL

Type: read-write
Clock: PBUS_WRCLK
Reset State: 0x00
Reset Name: PERPH_RB

MPP2_EN_CTL

Bits	Name	Type	Description
7	PERPH_EN	read-write	MPP Master enable 0 = puts MPP_PAD at high Z and disables the block 1 = MPP is enabled

0xA148 MPP2_ANA_OUT_CTL

Type: read-write
Clock: PBUS_WRCLK
Reset State: 0x00
Reset Name: PERPH_RB

MPP2_ANA_OUT_CTL

Bits	Name	Type	Description
2:0	REF_SEL	read-write	Analog Output Control 0: Output = vref_1V25 = REF_BYP pin, typically 1.25 Volts

0xA14A MPP2_ANA_IN_CTL

Type: read-write
Clock: PBUS_WRCLK
Reset State: 0x00
Reset Name: PERPH_RB

MPP2_ANA_IN_CTL

Bits	Name	Type	Description
2:0	ROUTE_SEL	read-write	AMUX Channel Control 0: Route to AMUX5 1: Route to AMUX6 2: Route to AMUX7 3: Route to AMUX8 4 to 7: Reserved

0xA14C MPP2_SINK_CTL

Type: read-write
Clock: PBUS_WRCLK
Reset State: 0x00
Reset Name: PERPH_RB

MPP2_SINK_CTL

Bits	Name	Type	Description
2:0	CURRENT_SEL	read-write	Current Sink Output Control 0: Output = 5 mA 1: Output = 10 mA 2: Output = 15 mA 3: Output = 20 mA 4: Output = 25 mA 5: Output = 30 mA 6: Output = 35 mA 7: Output = 40 mA

7.4 MPP3_MPP

0xA204 MPP3_PERPH_TYPE

Type: read-only
Clock: PBUS_WRCLK
Reset State: 0x11
Reset Name: N/A

Peripheral Type

MPP3_PERPH_TYPE

Bits	Name	Type	Description
7:0	TYPE	read-only	MPP

0xA205 MPP3_PERPH_SUBTYPE

Type: read-only
Clock: PBUS_WRCLK
Reset State: 0x05
Reset Name: N/A

Peripheral SubType

MPP3_PERPH_SUBTYPE

Bits	Name	Type	Description
7:0	SUBTYPE	read-only	MPP

0xA208 MPP3_STATUS1

Type: read-only
Clock: PBUS_WRCLK
Reset State: Undefined
Reset Name: N/A

Status Registers

MPP3_STATUS1

Bits	Name	Type	Description
7	MPP_OK	read-only	0 = GPIO is disabled 1 = GPIO is enabled

MPP3_STATUS1 (Continued)

Bits	Name	Type	Description
0	MPP_VAL	read-only	Value read by the input buffer, if enabled

0xA210 MPP3_INT_RT_STS

Type: read-only
Clock: PBUS_WRCLK
Reset State: 0x00
Reset Name: N/A

Interrupt Real Time Status Bits

MPP3_INT_RT_STS

Bits	Name	Type	Description
0	MPP_IN_STS	read-only	

0xA211 MPP3_INT_SET_TYPE

Type: read-write
Clock: PBUS_WRCLK
Reset State: 0x00
Reset Name: PERPH_RB

0 = use level trigger interrupts, 1 = use edge trigger interrupts

MPP3_INT_SET_TYPE

Bits	Name	Type	Description
0	MPP_IN_TYPE	read-write	

0xA212 MPP3_INT_POLARITY_HIGH

Type: read-write
Clock: PBUS_WRCLK
Reset State: 0x00
Reset Name: PERPH_RB

1= Interrupt will trigger on a level high (rising edge) event, 0 = level high triggering is disabled

MPP3_INT_POLARITY_HIGH

Bits	Name	Type	Description
0	MPP_IN_HIGH	read-write	

0xA213 MPP3_INT_POLARITY_LOW

Type: read-write
Clock: PBUS_WRCLK
Reset State: 0x00
Reset Name: PERPH_RB

1' = Interrupt will trigger on a level low (falling edge) event, '0' = level low triggering is disabled

MPP3_INT_POLARITY_LOW

Bits	Name	Type	Description
0	MPP_IN_LOW	read-write	

0xA214 MPP3_INT_LATCHED_CLR

Type: write-only
Clock: PBUS_WRCLK
Reset State: 0x00
Reset Name: PERPH_RB

Writing a '1' to this interrupt will rearm the interrupt when an interrupt is pending. It clears the internal sticky and sent bits

MPP3_INT_LATCHED_CLR

Bits	Name	Type	Description
0	MPP_IN_LATCHED_CLR	write-only	

0xA215 MPP3_INT_EN_SET

Type: read-write
Clock: PBUS_WRCLK
Reset State: 0x00
Reset Name: PERPH_RB

Writing '0' to this register has no effect. Writing a '1' will enable the corresponding interrupt. Reading this register will readback enable status

PMIC_SET_MASK

MPP3_INT_EN_SET

Bits	Name	Type	Description
0	MPP_IN_EN_SET	read-write	

0xA216 MPP3_INT_EN_CLR

Type: read-write
Clock: PBUS_WRCLK
Reset State: 0x00
Reset Name: PERPH_RB

Writing '0' to this register has no effect. Writing a '1' will disable the corresponding interrupt. Reading this register will readback enable status

PMIC_CLR_MASK=INT_EN_SET

MPP3_INT_EN_CLR

Bits	Name	Type	Description
0	MPP_IN_EN_CLR	read-write	

0xA218 MPP3_INT_LATCHED_STS

Type: read-only
Clock: PBUS_WRCLK
Reset State: 0x00
Reset Name: N/A

Latched (Sticky) Interrupt. '1' indicates that the interrupt has triggered. Once the latched bit is set it can only be cleared by writing the clear bit.

MPP3_INT_LATCHED_STS

Bits	Name	Type	Description
0	MPP_IN_LATCHED_STS	read-only	

0xA219 MPP3_INT_PENDING_STS

Type: read-only
Clock: PBUS_WRCLK
Reset State: 0x00
Reset Name: N/A

Debug: Pending is set if interrupt has been sent but not cleared.

MPP3_INT_PENDING_STS

Bits	Name	Type	Description
0	MPP_IN_PENDING_STS	read-only	

0xA21A MPP3_INT_MID_SEL

Type: read-write
Clock: PBUS_WRCLK
Reset State: 0x00
Reset Name: PERPH_RB

Selects the MID that will receive the interrupt

MPP3_INT_MID_SEL

Bits	Name	Type	Description
1:0	INT_MID_SEL	read-write	

0xA21B MPP3_INT_PRIORITY

Type: read-write
Clock: PBUS_WRCLK
Reset State: 0x00
Reset Name: PERPH_RB

SR=0 A=1

MPP3_INT_PRIORITY

Bits	Name	Type	Description
0	INT_PRIORITY	read-write	

0xA240 MPP3_MODE_CTL

Type: read-write
Clock: PBUS_WRCLK
Reset State: 0x00
Reset Name: PERPH_RB

MPP Mode allows you to switch from one mode to another mode in a single register write.

MPP3_MODE_CTL

Bits	Name	Type	Description
6:4	MODE	read-write	MPP Type: 0: Digital Input 1: Digital Output 2: Digital Input and Digital Output 3: Bidirectional Logic 4: Analog Input 5: Analog Output 6: Current Sink 7: Reserved

MPP3_MODE_CTL (Continued)

Bits	Name	Type	Description
3:0	EN_AND_SOURCE_SEL	read-write	When configured as a digital output Source select: 0000 = 0 0001 = 1 0010 = paired MPP 0011 = inverted paired MPP 0100 = Reserved 0101 = Reserved 0110 = Reserved 0111 = Reserved 1000 = DTEST1 1001 = inverted DTEST1 1010 = DTEST2 1011 = inverted DTEST2 1100 = DTEST3 1101 = inverted DTEST3 1110 = DTEST4 1111 = inverted DTEST4 Enable control when configured as Bidirectional, AIN, AOUT, or Current Sink. MPP is enable whenever the selected condition is true. 0000 = 0 (mpp is always disabled) 0001 = 1 (mpp is always Enabled) 0010 = paired MPP 0011 = inverted paired MPP 0100 = Reserved 0101 = Reserved 0110 = Reserved 0111 = Reserved 1000 = DTEST1 1001 = inverted DTEST1 1010 = DTEST2 1011 = inverted DTEST2 1100 = DTEST3 1101 = inverted DTEST3 1110 = DTEST4 1111 = inverted DTEST4

0xA241 MPP3_DIG_VIN_CTL

Type: read-write
Clock: PBUS_WRCLK
Reset State: 0x00
Reset Name: PERPH_RB

MPP3_DIG_VIN_CTL

Bits	Name	Type	Description
2:0	VOLTAGE_SEL	read-write	Digital I/O mode: 000 = VIN0 (refer to the objective spec.) 001 = VIN1 (refer to the objective spec.) 010 = VIN2 (refer to the objective spec.)* 011 = VIN3 (refer to the objective spec.) 100 = VIN4 (refer to the objective spec.)* 101 = VIN5 (refer to the objective spec.) 110 = VIN6 (refer to the objective spec.) 111 = VIN7 (refer to the objective spec.)

0xA242 MPP3_DIG_PULL_CTL

Type: read-write
Clock: PBUS_WRCLK
Reset State: 0x00
Reset Name: PERPH_RB

MPP3_DIG_PULL_CTL

Bits	Name	Type	Description
2:0	PULLUP_SEL	read-write	Pullup Resistor Control in bidirectional mode only. 00: 0.6k? ** 01: 10 k? 10: 30 k? 11: Open (infinite resistance) *

0xA246 MPP3_EN_CTL

Type: read-write
Clock: PBUS_WRCLK
Reset State: 0x00
Reset Name: PERPH_RB

MPP3_EN_CTL

Bits	Name	Type	Description
7	PERPH_EN	read-write	MPP Master enable 0 = puts MPP_PAD at high Z and disables the block 1 = MPP is enabled

0xA248 MPP3_ANA_OUT_CTL

Type: read-write
Clock: PBUS_WRCLK
Reset State: 0x00
Reset Name: PERPH_RB

MPP3_ANA_OUT_CTL

Bits	Name	Type	Description
2:0	REF_SEL	read-write	Analog Output Control 0: Output = vref_1V25 = REF_BYP pin, typically 1.25 Volts

0xA24A MPP3_ANA_IN_CTL

Type: read-write
Clock: PBUS_WRCLK
Reset State: 0x00
Reset Name: PERPH_RB

MPP3_ANA_IN_CTL

Bits	Name	Type	Description
2:0	ROUTE_SEL	read-write	AMUX Channel Control 0: Route to AMUX5 1: Route to AMUX6 2: Route to AMUX7 3: Route to AMUX8 4 to 7: Reserved

0xA24C MPP3_SINK_CTL

Type: read-write
Clock: PBUS_WRCLK
Reset State: 0x00
Reset Name: PERPH_RB

MPP3_SINK_CTL

Bits	Name	Type	Description
2:0	CURRENT_SEL	read-write	Current Sink Output Control 0: Output = 5 mA 1: Output = 10 mA 2: Output = 15 mA 3: Output = 20 mA 4: Output = 25 mA 5: Output = 30 mA 6: Output = 35 mA 7: Output = 40 mA

7.5 MPP4_MPP

0xA304 MPP4_PERPH_TYPE

Type: read-only
Clock: PBUS_WRCLK
Reset State: 0x11
Reset Name: N/A

Peripheral Type

MPP4_PERPH_TYPE

Bits	Name	Type	Description
7:0	TYPE	read-only	MPP

0xA305 MPP4_PERPH_SUBTYPE

Type: read-only
Clock: PBUS_WRCLK
Reset State: 0x03
Reset Name: N/A

Peripheral SubType

MPP4_PERPH_SUBTYPE

Bits	Name	Type	Description
7:0	SUBTYPE	read-only	MPP

0xA308 MPP4_STATUS1

Type: read-only
Clock: PBUS_WRCLK
Reset State: Undefined
Reset Name: N/A

Status Registers

MPP4_STATUS1

Bits	Name	Type	Description
7	MPP_OK	read-only	0 = GPIO is disabled 1 = GPIO is enabled

MPP4_STATUS1 (Continued)

Bits	Name	Type	Description
0	MPP_VAL	read-only	Value read by the input buffer, if enabled

0xA310 MPP4_INT_RT_STS

Type: read-only
Clock: PBUS_WRCLK
Reset State: 0x00
Reset Name: N/A

Interrupt Real Time Status Bits

MPP4_INT_RT_STS

Bits	Name	Type	Description
0	MPP_IN_STS	read-only	

0xA311 MPP4_INT_SET_TYPE

Type: read-write
Clock: PBUS_WRCLK
Reset State: 0x00
Reset Name: PERPH_RB

0 = use level trigger interrupts, 1 = use edge trigger interrupts

MPP4_INT_SET_TYPE

Bits	Name	Type	Description
0	MPP_IN_TYPE	read-write	

0xA312 MPP4_INT_POLARITY_HIGH

Type: read-write
Clock: PBUS_WRCLK
Reset State: 0x00
Reset Name: PERPH_RB

1= Interrupt will trigger on a level high (rising edge) event, 0 = level high triggering is disabled

MPP4_INT_POLARITY_HIGH

Bits	Name	Type	Description
0	MPP_IN_HIGH	read-write	

0xA313 MPP4_INT_POLARITY_LOW

Type: read-write
Clock: PBUS_WRCLK
Reset State: 0x00
Reset Name: PERPH_RB

1' = Interrupt will trigger on a level low (falling edge) event, '0' = level low triggering is disabled

MPP4_INT_POLARITY_LOW

Bits	Name	Type	Description
0	MPP_IN_LOW	read-write	

0xA314 MPP4_INT_LATCHED_CLR

Type: write-only
Clock: PBUS_WRCLK
Reset State: 0x00
Reset Name: PERPH_RB

Writing a '1' to this interrupt will rearm the interrupt when an interrupt is pending. It clears the internal sticky and sent bits

MPP4_INT_LATCHED_CLR

Bits	Name	Type	Description
0	MPP_IN_LATCHED_CLR	write-only	

0xA315 MPP4_INT_EN_SET

Type: read-write
Clock: PBUS_WRCLK
Reset State: 0x00
Reset Name: PERPH_RB

Writing '0' to this register has no effect. Writing a '1' will enable the corresponding interrupt. Reading this register will readback enable status

PMIC_SET_MASK

MPP4_INT_EN_SET

Bits	Name	Type	Description
0	MPP_IN_EN_SET	read-write	

0xA316 MPP4_INT_EN_CLR

Type: read-write
Clock: PBUS_WRCLK
Reset State: 0x00
Reset Name: PERPH_RB

Writing '0' to this register has no effect. Writing a '1' will disable the corresponding interrupt. Reading this register will readback enable status

PMIC_CLR_MASK=INT_EN_SET

MPP4_INT_EN_CLR

Bits	Name	Type	Description
0	MPP_IN_EN_CLR	read-write	

0xA318 MPP4_INT_LATCHED_STS

Type: read-only
Clock: PBUS_WRCLK
Reset State: 0x00
Reset Name: N/A

Latched (Sticky) Interrupt. '1' indicates that the interrupt has triggered. Once the latched bit is set it can only be cleared by writing the clear bit.

MPP4_INT_LATCHED_STS

Bits	Name	Type	Description
0	MPP_IN_LATCHED_STS	read-only	

0xA319 MPP4_INT_PENDING_STS

Type: read-only
Clock: PBUS_WRCLK
Reset State: 0x00
Reset Name: N/A

Debug: Pending is set if interrupt has been sent but not cleared.

MPP4_INT_PENDING_STS

Bits	Name	Type	Description
0	MPP_IN_PENDING_STS	read-only	

0xA31A MPP4_INT_MID_SEL

Type: read-write
Clock: PBUS_WRCLK
Reset State: 0x00
Reset Name: PERPH_RB

Selects the MID that will receive the interrupt

MPP4_INT_MID_SEL

Bits	Name	Type	Description
1:0	INT_MID_SEL	read-write	

0xA31B MPP4_INT_PRIORITY

Type: read-write
Clock: PBUS_WRCLK
Reset State: 0x00
Reset Name: PERPH_RB

SR=0 A=1

MPP4_INT_PRIORITY

Bits	Name	Type	Description
0	INT_PRIORITY	read-write	

0xA340 MPP4_MODE_CTL

Type: read-write
Clock: PBUS_WRCLK
Reset State: 0x00
Reset Name: PERPH_RB

MPP Mode allows you to switch from one mode to another mode in a single register write.

MPP4_MODE_CTL

Bits	Name	Type	Description
6:4	MODE	read-write	MPP Type: 0: Digital Input 1: Digital Output 2: Digital Input and Digital Output 3: Bidirectional Logic 4: Analog Input 5: Analog Output 6: Current Sink 7: Reserved

MPP4_MODE_CTL (Continued)

Bits	Name	Type	Description
3:0	EN_AND_SOURCE_SEL	read-write	When configured as a digital output Source select: 0000 = 0 0001 = 1 0010 = paired MPP 0011 = inverted paired MPP 0100 = Reserved 0101 = Reserved 0110 = Reserved 0111 = Reserved 1000 = DTEST1 1001 = inverted DTEST1 1010 = DTEST2 1011 = inverted DTEST2 1100 = DTEST3 1101 = inverted DTEST3 1110 = DTEST4 1111 = inverted DTEST4 Enable control when configured as Bidirectional, AIN, AOUT, or Current Sink. MPP is enable whenever the selected condition is true. 0000 = 0 (mpp is always disabled) 0001 = 1 (mpp is always Enabled) 0010 = paired MPP 0011 = inverted paired MPP 0100 = Reserved 0101 = Reserved 0110 = Reserved 0111 = Reserved 1000 = DTEST1 1001 = inverted DTEST1 1010 = DTEST2 1011 = inverted DTEST2 1100 = DTEST3 1101 = inverted DTEST3 1110 = DTEST4 1111 = inverted DTEST4

0xA341 MPP4_DIG_VIN_CTL

Type: read-write
Clock: PBUS_WRCLK
Reset State: 0x00
Reset Name: PERPH_RB

MPP4_DIG_VIN_CTL

Bits	Name	Type	Description
2:0	VOLTAGE_SEL	read-write	Digital I/O mode: 000 = VIN0 (refer to the objective spec.) 001 = VIN1 (refer to the objective spec.) 010 = VIN2 (refer to the objective spec.)* 011 = VIN3 (refer to the objective spec.) 100 = VIN4 (refer to the objective spec.)* 101 = VIN5 (refer to the objective spec.) 110 = VIN6 (refer to the objective spec.) 111 = VIN7 (refer to the objective spec.)

0xA342 MPP4_DIG_PULL_CTL

Type: read-write
Clock: PBUS_WRCLK
Reset State: 0x00
Reset Name: PERPH_RB

MPP4_DIG_PULL_CTL

Bits	Name	Type	Description
2:0	PULLUP_SEL	read-write	Pullup Resistor Control in bidirectional mode only. 00: 0.6k? ** 01: 10 k? 10: 30 k? 11: Open (infinite resistance) *

0xA346 MPP4_EN_CTL

Type: read-write
Clock: PBUS_WRCLK
Reset State: 0x00
Reset Name: PERPH_RB

MPP4_EN_CTL

Bits	Name	Type	Description
7	PERPH_EN	read-write	MPP Master enable 0 = puts MPP_PAD at high Z and disables the block 1 = MPP is enabled

0xA348 MPP4_ANA_OUT_CTL

Type: read-write
Clock: PBUS_WRCLK
Reset State: 0x00
Reset Name: PERPH_RB

MPP4_ANA_OUT_CTL

Bits	Name	Type	Description
2:0	REF_SEL	read-write	Analog Output Control 0: Output = vref_1V25 = REF_BYP pin, typically 1.25 Volts

0xA34A MPP4_ANA_IN_CTL

Type: read-write
Clock: PBUS_WRCLK
Reset State: 0x00
Reset Name: PERPH_RB

MPP4_ANA_IN_CTL

Bits	Name	Type	Description
2:0	ROUTE_SEL	read-write	AMUX Channel Control 0: Route to AMUX5 1: Route to AMUX6 2: Route to AMUX7 3: Route to AMUX8 4 to 7: Reserved

0xA34C MPP4_SINK_CTL

Type: read-write
Clock: PBUS_WRCLK
Reset State: 0x00
Reset Name: PERPH_RB

MPP4_SINK_CTL

Bits	Name	Type	Description
2:0	CURRENT_SEL	read-write	Current Sink Output Control 0: Output = 5 mA 1: Output = 10 mA 2: Output = 15 mA 3: Output = 20 mA 4: Output = 25 mA 5: Output = 30 mA 6: Output = 35 mA 7: Output = 40 mA

8 Sn

8.1 Overview

Table 8-1 Blocks

Name
S1_CTRL
S1_PS
S1_FREQ
S2_CTRL
S2_PS
S2_FREQ
S3_CTRL
S3_PS
S3_FREQ
S4_CTRL
S4_PS
S4_FREQ
S5_CTRL
S5_PS
S5_FREQ
S6_CTRL
S6_PS
S6_FREQ
S7_CTRL
S7_PS
S7_FREQ
S8_CTRL
S8_PS
S8_FREQ

8.2 S1_CTRL_HFBUCK2_CTRL

0x11404 S1_CTRL_PERPH_TYPE

Type: read-only
Clock: PBUS_WRCLK
Reset State: 0x03
Reset Name: N/A

Peripheral Type

S1_CTRL_PERPH_TYPE

Bits	Name	Type	Description
7:0	TYPE	read-only	SMPS

0x11405 S1_CTRL_PERPH_SUBTYPE

Type: read-only
Clock: PBUS_WRCLK
Reset State: 0x08
Reset Name: N/A

Peripheral SubType

S1_CTRL_PERPH_SUBTYPE

Bits	Name	Type	Description
7:0	SUBTYPE	read-only	2A HF BUCK

0x11408 S1_CTRL_STATUS

Type: read-only
Clock: PBUS_WRCLK
Reset State: Undefined
Reset Name: N/A

Status Registers

S1_CTRL_STATUS

Bits	Name	Type	Description
7	VREG_OK	read-only	0 = VREG output voltage is below VREG_OK threshold 1 = VREG output voltage is above VREG_OK threshold

S1_CTRL_STATUS (Continued)

Bits	Name	Type	Description
5	ILS	read-only	Illegal Limit Stop. This is triggered when UL_Voltage < LL_Voltage
4	UL_VOLTAGE	read-only	Last voltage set was above or equal to UL_Voltage
3	LL_VOLTAGE	read-only	Last voltage set was below or equal to LL_Voltage
2	PS_TRUE	read-only	0 = buck is not pulse skipping 1 = buck is pulse skipping
1	NPM_TRUE	read-only	1 = VREG_OK and BUCK is in NPM
0	STEPPER_DONE	read-only	1 = stepper is done

0x11410 S1_CTRL_INT_RT_STS

Type: read-only
Clock: PBUS_WRCLK
Reset State: 0x00
Reset Name: PERPH_RB

Interrupt Real Time Status Bits

S1_CTRL_INT_RT_STS

Bits	Name	Type	Description
1	LIMIT_ERR_INT	read-only	Last voltage set was above UL or below LL
0	VREG_OK_INT	read-only	Regulator has been successfully enabled

0x11411 S1_CTRL_INT_SET_TYPE

Type: read-write
Clock: PBUS_WRCLK
Reset State: 0x00
Reset Name: PERPH_RB

0 = use level trigger interrupts, 1 = use edge trigger interrupts

S1_CTRL_INT_SET_TYPE

Bits	Name	Type	Description
1	LIMIT_ERR_INT	read-write	
0	VREG_OK_INT	read-write	

0x11412 S1_CTRL_INT_POLARITY_HIGH

Type: read-write
Clock: PBUS_WRCLK
Reset State: 0x00
Reset Name: PERPH_RB

1= Interrupt will trigger on a level high (rising edge) event, 0 = level high triggering is disabled

S1_CTRL_INT_POLARITY_HIGH

Bits	Name	Type	Description
1	LIMIT_ERR_INT	read-write	
0	VREG_OK_INT	read-write	

0x11413 S1_CTRL_INT_POLARITY_LOW

Type: read-write
Clock: PBUS_WRCLK
Reset State: 0x00
Reset Name: PERPH_RB

1' = Interrupt will trigger on a level low (falling edge) event, '0' = level low triggering is disabled

S1_CTRL_INT_POLARITY_LOW

Bits	Name	Type	Description
1	LIMIT_ERR_INT	read-write	
0	VREG_OK_INT	read-write	

0x11414 S1_CTRL_INT_LATCHED_CLR

Type: write-only
Clock: PBUS_WRCLK
Reset State: 0x00
Reset Name: PERPH_RB

Writing a '1' to this interrupt will rearm the interrupt when an interrupt is pending. It clears the internal sticky and sent bits

S1_CTRL_INT_LATCHED_CLR

Bits	Name	Type	Description
1	LIMIT_ERR_INT	write-only	
0	VREG_OK_INT	write-only	

0x11415 S1_CTRL_INT_EN_SET

Type: read-write
Clock: PBUS_WRCLK
Reset State: 0x00
Reset Name: PERPH_RB

Writing '0' to this register has no effect. Writing a '1' will enable the corresponding interrupt. Reading this register will readback enable status

PMIC_SET_MASK

S1_CTRL_INT_EN_SET

Bits	Name	Type	Description
1	LIMIT_ERR_INT	read-write	
0	VREG_OK_INT	read-write	

0x11416 S1_CTRL_INT_EN_CLR

Type: read-write
Clock: PBUS_WRCLK
Reset State: 0x00
Reset Name: PERPH_RB

Writing '0' to this register has no effect. Writing a '1' will disable the corresponding interrupt. Reading this register will readback enable status

PMIC_CLR_MASK=INT_EN_SET

S1_CTRL_INT_EN_CLR

Bits	Name	Type	Description
1	LIMIT_ERR_INT	read-write	
0	VREG_OK_INT	read-write	

0x11418 S1_CTRL_INT_LATCHED_STS

Type: read-only
Clock: PBUS_WRCLK
Reset State: 0x00
Reset Name: PERPH_RB

Debug: Latched (Sticky) Interrupt. '1' indicates that the interrupt has triggered. Once the latched bit is set it can only be cleared by writing the clear bit.

S1_CTRL_INT_LATCHED_STS

Bits	Name	Type	Description
1	LIMIT_ERR_INT	read-only	
0	VREG_OK_INT	read-only	

0x11419 S1_CTRL_INT_PENDING_STS

Type: read-only
Clock: PBUS_WRCLK
Reset State: 0x00
Reset Name: PERPH_RB

Debug: Pending is set if interrupt has been sent but not cleared.

S1_CTRL_INT_PENDING_STS

Bits	Name	Type	Description
1	LIMIT_ERR_INT	read-only	
0	VREG_OK_INT	read-only	

0x1141A S1_CTRL_INT_MID_SEL

Type: read-write
Clock: PBUS_WRCLK
Reset State: 0x00
Reset Name: PERPH_RB

Selects the MID that will receive the interrupt

S1_CTRL_INT_MID_SEL

Bits	Name	Type	Description
1:0	INT_MID_SEL	read-write	

0x1141B S1_CTRL_INT_PRIORITY

Type: read-write
Clock: PBUS_WRCLK
Reset State: 0x00
Reset Name: PERPH_RB

S1_CTRL_INT_PRIORITY

Bits	Name	Type	Description
0	INT_PRIORITY	read-write	SR=0 A=1

0x11440 S1_CTRL_VOLTAGE_CTL1

Type: read-write
Clock: PBUS_WRCLK
Reset State: 0x00
Reset Name: PERPH_RB

PMIC_LATCHED_WRITE=VOLTAGE_CTL2

S1_CTRL_VOLTAGE_CTL1

Bits	Name	Type	Description
0	RANGE	read-write	0 : 0.375 to 1.5625 V at steps of 12.5 mV (Vmin = 0.375 V, Vstep = 12.5 mV) 1 : 1.550 to 3.1250 V at steps of 25.0 mV (Vmin = 1.550 V, Vstep = 25.0 mV)

0x11441 S1_CTRL_VOLTAGE_CTL2

Type: read-write
Clock: PBUS_WRCLK
Reset State: 0x2E
Reset Name: PERPH_RB

S1_CTRL_VOLTAGE_CTL2

Bits	Name	Type	Description
6:0	V_SET	read-write	Voltage = Vmin + VSET*(Vstep)

0x11445 S1_CTRL_MODE_CTL

Type: read-write
Clock: PBUS_WRCLK
Reset State: 0x80
Reset Name: PERPH_RB

Define Buck Mode Transitions

S1_CTRL_MODE_CTL

Bits	Name	Type	Description
7	PWM	read-write	Force PWM
6	AUTO_MODE	read-write	1=Automatically enter NPM based on current
4	FOLLOW_PMIC_AWAKE	read-write	NPM when PMIC_AWAKE (SLEEP_B) = '1'
3	FOLLOW_HWEN3	read-write	1' BUCK is in NPM when HWEN3 ='1', '0'= ignore HWEN3
2	FOLLOW_HWEN2	read-write	1' BUCK is in NPM when HWEN2 ='1', '0'= ignore HWEN2
1	FOLLOW_HWEN1	read-write	1' BUCK is in NPM when HWEN1 ='1', '0'= ignore HWEN1
0	FOLLOW_HWEN0	read-write	1' BUCK is in NPM when HWEN0 ='1', '0'= ignore HWEN0

0x11446 S1_CTRL_EN_CTL

Type: read-write
Clock: PBUS_WRCLK
Reset State: 0x00
Reset Name: PERPH_RB

S1_CTRL_EN_CTL

Bits	Name	Type	Description
7	PERPH_EN	read-write	1' = Enable the BUCK, '0' = do not force BUCK on
3	FOLLOW_HWEN3	read-write	1' BUCK is enabled when HWEN3 ='1', '0'= ignore HWEN3
2	FOLLOW_HWEN2	read-write	1' BUCK is enabled when HWEN2 ='1', '0'= ignore HWEN2
1	FOLLOW_HWEN1	read-write	1' BUCK is enabled when HWEN1 ='1', '0'= ignore HWEN1
0	FOLLOW_HWEN0	read-write	1' BUCK is enabled when HWEN0 ='1', '0'= ignore HWEN0

0x11448 S1_CTRL_PD_CTL

Type: read-write
Clock: PBUS_WRCLK
Reset State: 0x80
Reset Name: PERPH_RB

S1_CTRL_PD_CTL

Bits	Name	Type	Description
7	PD_EN	read-write	1' = Enable the pulldown when the regulator is disabled, '0' = pulldown is always disabled. Preset by trim register

8.3 S1_FREQ_BCLK_GEN_CLK

0x11604 S1_FREQ_PERPH_TYPE

Type: read-only
Clock: PBUS_WRCLK
Reset State: 0x1D
Reset Name: N/A

Peripheral Type

S1_FREQ_PERPH_TYPE

Bits	Name	Type	Description
7:0	TYPE	read-only	BCLK GEN

0x11605 S1_FREQ_PERPH_SUBTYPE

Type: read-only
Clock: PBUS_WRCLK
Reset State: 0x09
Reset Name: N/A

Peripheral SubType

S1_FREQ_PERPH_SUBTYPE

Bits	Name	Type	Description
7:0	SUBTYPE	read-only	BCLK GEN CLK

0x11646 S1_FREQ_CLK_ENABLE

Type: read-write
Clock: PBUS_WRCLK
Reset State: 0x01
Reset Name: PERPH_RB

S1_FREQ_CLK_ENABLE

Bits	Name	Type	Description
7	EN_CLK_INT	read-write	0 = do not force the clock on 1 = enable the clock
0	FOLLOW_CLK_SX_REQ	read-write	0 = ignore smps_clk_req<X> 1 = clock is enabled when the clocks request is high smps_clk_req<X>='1'

0x11650 S1_FREQ_CLK_DIV

Type: read-write
Clock: PBUS_WRCLK
Reset State: 0x05
Reset Name: PERPH_RB

PMIC_GANGED

S1_FREQ_CLK_DIV

Bits	Name	Type	Description
3:0	CLK_DIV	read-write	clock_ frequency = 19.2MHz / (CLK_DIV + 1) FTS2 Buck supports 3.2, 4.8, 6.4 and 9.6 MHz HF2 Buck supports 1.6, 2.4, 2.74, 3.2, 3.8, 4.8, and 6.4 MHz CLK_DIV = 0 is not supported, it will generate 9.6 MHz

0x11651 S1_FREQ_CLK_PHASE

Type: read-write
Clock: PBUS_WRCLK
Reset State: 0x05
Reset Name: PERPH_RB

S1_FREQ_CLK_PHASE

Bits	Name	Type	Description
3:0	CLK_PHASE	read-write	Distributed clock phase select: clock phase delay = clock period * (CLK_PHASE / 16)

0x116C0 S1_FREQ_GANG_CTL1

Type: read-write
Clock: PBUS_WRCLK
Reset State: 0x00
Reset Name: PERPH_RB

S1_FREQ_GANG_CTL1

Bits	Name	Type	Description
7:0	GANG_LEADER_PID	read-write	When GANG_EN (GANG_CTL2[7]) is set, this peripheral will write the same data that is written to the gang leader Peripheral ID. Reads to the gang leader Peripheral ID are ignored by this peripheral. Ganged peripherals must reside within the same Slave ID

0x116C1 S1_FREQ_GANG_CTL2

Type: read-write
Clock: PBUS_WRCLK
Reset State: 0x00
Reset Name: PERPH_RB

S1_FREQ_GANG_CTL2

Bits	Name	Type	Description
7	GANG_EN	read-write	0 = disable 1 = enable When enabled, this peripheral will write the same data that is written to the gang leader PID. Reads to the gang leader PID are ignored by this peripheral

8.4 S2_CTRL_FTS2_CTRL

0x11704 S2_CTRL_PERPH_TYPE

Type: read-only
Clock: PBUS_WRCLK
Reset State: 0x03
Reset Name: N/A

Peripheral Type

S2_CTRL_PERPH_TYPE

Bits	Name	Type	Description
7:0	TYPE	read-only	FTS2 Control Reset State: 0x03

0x11705 S2_CTRL_PERPH_SUBTYPE

Type: read-only
Clock: PBUS_WRCLK
Reset State: 0x08
Reset Name: N/A

Peripheral SubType

S2_CTRL_PERPH_SUBTYPE

Bits	Name	Type	Description
7:0	SUBTYPE	read-only	

0x11708 S2_CTRL_STATUS_1

Type: read-only
Clock: PBUS_WRCLK
Reset State: Undefined
Reset Name: N/A

Status Registers

S2_CTRL_STATUS_1

Bits	Name	Type	Description
7	VREG_OK_FLAG	read-only	Indicates that VREG_SNS has reached a value that is greater than or equal to the threshold of the comparator tasked for VREG_SNS monitoring

S2_CTRL_STATUS_1 (Continued)

Bits	Name	Type	Description
6	VREG_FAULT_FLAG	read-only	Indicates a probable short circuit condition at VREG_SNS since VREG_SNS is below the VREG fault voltage level and the softstart ramp is done. Current limit foldback is in use.
1	NPM_FLAG	read-only	Indicates normal power mode is in use
0	STEPPER_DONE_FLAG	read-only	Softstart stepper and voltage stepper done

0x11709 S2_CTRL_STATUS_2

Type: read-only
Clock: PBUS_WRCLK
Reset State: Undefined
Reset Name: N/A

Status Registers

S2_CTRL_STATUS_2

Bits	Name	Type	Description
4	ILS_FLAG	read-only	Either of the following: => Both limit stops have been enabled, but the upper limit stop VSET_ULS has been programmed to a value below the lower limit stop VSET_LLS => Both limit stops have been enabled, but the lower limit stop VSET_LLS has been programmed to a value above the upper limit stop VSET_ULS
3	ULS_FLAG	read-only	Indicates that the voltage setpoint has been programmed to a value that is greater than or equal to the upper limit stop VSET_ULS
2	LLS_FLAG	read-only	Indicates that the voltage setpoint has been programmed to a value that is less than or equal to the lower limit stop VSET_LLS
1	GPL_HI_FLAG	read-only	Indicates that the voltage setpoint has reached a value that is greater than or equal to the high general purpose limit VSET_GPL_HI
0	GPL_LO_FLAG	read-only	Indicates that the voltage setpoint has reached a value that is less than or equal to the low general purpose limit VSET_GPL_LO

0x11710 S2_CTRL_INT_RT_STS

Type: read-only
Clock: PBUS_WRCLK
Reset State: Undefined
Reset Name: PERPH_RB

Interrupt Real Time Status Bits

S2_CTRL_INT_RT_STS

Bits	Name	Type	Description
2	VREG_FAULT_INT	read-only	
1	LIMIT_ERR_INT	read-only	
0	VREG_OK_INT	read-only	

0x11711 S2_CTRL_INT_SET_TYPE

Type: read-write
Clock: PBUS_WRCLK
Reset State: 0x00
Reset Name: PERPH_RB

0 = use level trigger interrupts, 1 = use edge trigger interrupts

S2_CTRL_INT_SET_TYPE

Bits	Name	Type	Description
2	VREG_FAULT_INT	read-write	
1	LIMIT_ERR_INT	read-write	
0	VREG_OK_INT	read-write	

0x11712 S2_CTRL_INT_POLARITY_HIGH

Type: read-write
Clock: PBUS_WRCLK
Reset State: 0x00
Reset Name: PERPH_RB

1= Interrupt will trigger on a level high (rising edge) event, 0 = level high triggering is disabled

S2_CTRL_INT_POLARITY_HIGH

Bits	Name	Type	Description
2	VREG_FAULT_INT	read-write	
1	LIMIT_ERR_INT	read-write	
0	VREG_OK_INT	read-write	

0x11713 S2_CTRL_INT_POLARITY_LOW

Type: read-write
Clock: PBUS_WRCLK
Reset State: 0x00
Reset Name: PERPH_RB

1' = Interrupt will trigger on a level low (falling edge) event, '0' = level low triggering is disabled

S2_CTRL_INT_POLARITY_LOW

Bits	Name	Type	Description
2	VREG_FAULT_INT	read-write	
1	LIMIT_ERR_INT	read-write	
0	VREG_OK_INT	read-write	

0x11714 S2_CTRL_INT_LATCHED_CLR

Type: write-only
Clock: PBUS_WRCLK
Reset State: 0x00
Reset Name: PERPH_RB

Writing a '1' to this interrupt will rearm the interrupt when an interrupt is pending. It clears the internal sticky and sent bits

S2_CTRL_INT_LATCHED_CLR

Bits	Name	Type	Description
2	VREG_FAULT_INT	write-only	

S2_CTRL_INT_LATCHED_CLR (Continued)

Bits	Name	Type	Description
1	LIMIT_ERR_INT	write-only	
0	VREG_OK_INT	write-only	

0x11715 S2_CTRL_INT_EN_SET

Type: read-write
Clock: PBUS_WRCLK
Reset State: 0x00
Reset Name: PERPH_RB

Writing '0' to this register has no effect. Writing a '1' will enable the corresponding interrupt. Reading this register will readback enable status

PMIC_SET_MASK

S2_CTRL_INT_EN_SET

Bits	Name	Type	Description
2	VREG_FAULT_INT	read-write	
1	LIMIT_ERR_INT	read-write	
0	VREG_OK_INT	read-write	

0x11716 S2_CTRL_INT_EN_CLR

Type: read-write
Clock: PBUS_WRCLK
Reset State: 0x00
Reset Name: PERPH_RB

Writing '0' to this register has no effect. Writing a '1' will disable the corresponding interrupt. Reading this register will readback enable status

PMIC_CLR_MASK=INT_EN_SET

S2_CTRL_INT_EN_CLR

Bits	Name	Type	Description
2	VREG_FAULT_INT	read-write	

S2_CTRL_INT_EN_CLR (Continued)

Bits	Name	Type	Description
1	LIMIT_ERR_INT	read-write	
0	VREG_OK_INT	read-write	

0x11718 S2_CTRL_INT_LATCHED_STS

Type: read-only
Clock: PBUS_WRCLK
Reset State: 0x00
Reset Name: PERPH_RB

Debug: Latched (Sticky) Interrupt. '1' indicates that the interrupt has triggered. Once the latched bit is set it can only be cleared by writing the clear bit.

S2_CTRL_INT_LATCHED_STS

Bits	Name	Type	Description
2	VREG_FAULT_INT	read-only	
1	LIMIT_ERR_INT	read-only	
0	VREG_OK_INT	read-only	

0x11719 S2_CTRL_INT_PENDING_STS

Type: read-only
Clock: PBUS_WRCLK
Reset State: 0x00
Reset Name: PERPH_RB

Debug: Pending is set if interrupt has been sent but not cleared.

S2_CTRL_INT_PENDING_STS

Bits	Name	Type	Description
2	VREG_FAULT_INT	read-only	
1	LIMIT_ERR_INT	read-only	
0	VREG_OK_INT	read-only	

0x1171A S2_CTRL_INT_MID_SEL

Type: read-write
Clock: PBUS_WRCLK
Reset State: 0x00
Reset Name: PERPH_RB

Selects the MID that will receive the interrupt

S2_CTRL_INT_MID_SEL

Bits	Name	Type	Description
1:0	INT_MID_SEL	read-write	

0x1171B S2_CTRL_INT_PRIORITY

Type: read-write
Clock: PBUS_WRCLK
Reset State: 0x00
Reset Name: PERPH_RB

SR=0 A=1

S2_CTRL_INT_PRIORITY

Bits	Name	Type	Description
0	INT_PRIORITY	read-write	

0x11740 S2_CTRL_VOLTAGE_CTL1

Type: read-write
Clock: PBUS_WRCLK
Reset State: 0x00
Reset Name: PERPH_RB

PMIC_GANGED

S2_CTRL_VOLTAGE_CTL1

Bits	Name	Type	Description
0	MV_RANGE	read-write	0 = Use low voltage range as specified by VSET and PFM_VOFFSET 1 = Use medium voltage range as specified by VSET and PFM_VOFFSET

0x11741 S2_CTRL_VOLTAGE_CTL2

Type: read-write
Clock: PBUS_WRCLK
Reset State: 0xB4
Reset Name: PERPH_RB

PMIC_GANGED

S2_CTRL_VOLTAGE_CTL2

Bits	Name	Type	Description
7:0	VSET	read-write	Output voltage set point in PWM mode and in PFM mode if the PFM_VOFFSET_EN bit is not asserted For MV_RANGE = 0: VSET => 0.005V * m + 0.080V, where m = <7:0> For MV_RANGE = 1: VSET => 0.010V * m + 0.160V, where m = <7:0> If PFM_VOFFSET_EN is asserted and in PFM mode, add PFM_VOFFSET

0x11742 S2_CTRL_VSET_VALID

Type: read-only
Clock: PBUS_WRCLK
Reset State: Undefined
Reset Name: PERPH_RB

S2_CTRL_VSET_VALID

Bits	Name	Type	Description
7:0	VSET_VALID	read-only	Readback the valid output voltage setpoint value

0x11744 S2_CTRL_VOLTAGE_CTL3

Type: read-write
Clock: PBUS_WRCLK
Reset State: 0x00
Reset Name: PERPH_RB

S2_CTRL_VOLTAGE_CTL3

Bits	Name	Type	Description
7	PFM_VOFFSET_EN	read-write	When in PFM mode 0 = Use VSET for output voltage set point 1 = Use VSET + PFM_VOFFSET for output voltage set point
1:0	PFM_VOFFSET	read-write	When in PFM mode and PFM_VOFFSET_EN is asserted, add a positive output voltage offset For MV_RANGE = 0: VOFFSET = 0.005V * 2 * m, where m = <1:0> For MV_RANGE = 1: VOFFSET = 0.010V * 2 * m, where m = <1:0>

0x11745 S2_CTRL_MODE_CTL

Type: read-write
Clock: PBUS_WRCLK
Reset State: 0xC0
Reset Name: PERPH_RB

PMIC_GANGED

S2_CTRL_MODE_CTL

Bits	Name	Type	Description
7	NPM	read-write	FTS NON-AUTO mode control 0 = Low power mode (LPM) unless AUTO_MODE is asserted 1 = Normal power mode (PWM)
6	AUTO_MODE	read-write	When asserted, FTS automatically enters and exits low power mode (PFM) based on load current qualifying triggers 0 = AUTO mode is disabled 1 = AUTO mode is enabled

0x11746 S2_CTRL_EN_CTL

Type: read-write
Clock: PBUS_WRCLK
Reset State: 0x00
Reset Name: PERPH_RB

PMIC_GANGED

S2_CTRL_EN_CTL

Bits	Name	Type	Description
7	PERPH_EN	read-write	FTS enable control 0 = Off 1 = On

0x11748 S2_CTRL_PD_CTL

Type: read-write
Clock: PBUS_WRCLK
Reset State: 0x80
Reset Name: PERPH_RB

S2_CTRL_PD_CTL

Bits	Name	Type	Description
7	PD_EN	read-write	0 = Strong pulldown is always disabled 1 = Strong pulldown is enabled when the regulator is disabled
6	WEAK_PD_EN	read-write	0 = Weak pulldown is not enabled in OFF state 1 = Weak pulldown is enabled in OFF state
5	WEAK_PD_PFM	read-write	0 = Weak pulldown is not enabled in PFM mode 1 = Weak pulldown is enabled in PFM mode
4	WEAK_PD_PWM	read-write	0 = Weak pulldown is not enabled in PWM mode (and in HCPFM mode) 1 = Weak pulldown is enabled in PWM mode (and in HCPFM mode)

0x11754 S2_CTRL_PHASE_CNT

Type: read-write
Clock: PBUS_WRCLK
Reset State: 0x00
Reset Name: PERPH_RB

PMIC_GANGED

S2_CTRL_PHASE_CNT

Bits	Name	Type	Description
1:0	PHASE_CNT	read-write	When MULTIPHASE_EN is asserted, the number of operating phases is 00 = Number of operating phases is 1 01 = Number of operating phases is 2 10 = Number of operating phases is 4 11 = Number of operating phases is 4

0x11760 S2_CTRL_SS_CTL

Type: read-write
Clock: PBUS_WRCLK
Reset State: 0x08
Reset Name: PERPH_RB

PMIC_GANGED

S2_CTRL_SS_CTL

Bits	Name	Type	Description
4:3	SS_STEP	read-write	Softstart voltage step size 00 = SS voltage step of 1 * LSB of VPROG 01 = SS voltage step of 2 * LSB 10 = SS voltage step of 4 * LSB 11 = SS voltage step of 8 * LSB
2:0	SS_DELAY	read-write	Softstart delay between steps = 2 ^ (m + 3) / Fsys, where m = <2:0> (Fsys = 19.2 MHz): 000 = 8-clock cycles (417ns) 001 = 16-clock cycles 010 = 32-clock cycles 011 = 64-clock cycles 100 = 128-clock cycles (6.67us) 101 = 256-clock cycles 110 = 512-clock cycles 111 = 1024-clock cycles (53.3us)

0x11761 S2_CTRL_VS_CTL

Type: read-write
Clock: PBUS_WRCLK
Reset State: 0x00
Reset Name: PERPH_RB

PMIC_GANGED

S2_CTRL_VS_CTL

Bits	Name	Type	Description
7	VS_EN	read-write	Voltage stepping control 0 = VS is disabled 1 = VS is enabled
4:3	VS_STEP	read-write	Voltage stepping voltage step size 00 = VS voltage step of 1 * LSB of VPROG 01 = VS voltage step of 2 * LSB 10 = VS voltage step of 4 * LSB 11 = VS voltage step of 8 * LSB
2:0	VS_DELAY	read-write	Voltage stepping delay between steps = 2 ^ (m + 3) / Fsys, where m = <2:0> (Assuming Fsys = 19.2 MHz): Desired default is 1.67us 000 = 8-clock cycles (417ns) 001 = 16-clock cycles 010 = 32-clock cycles 011 = 64-clock cycles 100 = 128-clock cycles (6.67us) 101 = 256-clock cycles 110 = 512-clock cycles 111 = 1024-clock cycles (53.3us)

0x1176A S2_CTRL_ULS_VALID

Type: read-only
Clock: PBUS_WRCLK
Reset State: Undefined
Reset Name: PERPH_RB

S2_CTRL_ULS_VALID

Bits	Name	Type	Description
7:0	ULS_VALID	read-only	Readback the valid upper limit stop value

0x1176C S2_CTRL_LLS_VALID

Type: read-only
Clock: PBUS_WRCLK
Reset State: Undefined
Reset Name: PERPH_RB

S2_CTRL_LLS_VALID

Bits	Name	Type	Description
7:0	LLS_VALID	read-only	Readback the valid lower limit stop value

8.5 S2_PS_FTS2_PS

0x11804 S2_PS_PERPH_TYPE

Type: read-only
Clock: PBUS_WRCLK
Reset State: 0x1C
Reset Name: N/A

Peripheral Type

S2_PS_PERPH_TYPE

Bits	Name	Type	Description
7:0	TYPE	read-only	FTS2 Power Stage Reset State: 0x1C

0x11805 S2_PS_PERPH_SUBTYPE

Type: read-only
Clock: PBUS_WRCLK
Reset State: 0x08
Reset Name: N/A

Peripheral SubType

S2_PS_PERPH_SUBTYPE

Bits	Name	Type	Description
7:0	SUBTYPE	read-only	

0x11840 S2_PS_VOLTAGE_CTL1

Type: read-write
Clock: PBUS_WRCLK
Reset State: 0x00
Reset Name: PERPH_RB

PMIC_GANGED

S2_PS_VOLTAGE_CTL1

Bits	Name	Type	Description
0	MV_RANGE	read-write	0 = Use low voltage range as specified by VSET and PFM_VOFFSET 1 = Use medium voltage range as specified by VSET and PFM_VOFFSET

0x11841 S2_PS_VOLTAGE_CTL2

Type: read-write
Clock: PBUS_WRCLK
Reset State: 0xB4
Reset Name: PERPH_RB

PMIC_GANGED

S2_PS_VOLTAGE_CTL2

Bits	Name	Type	Description
7:0	VSET	read-write	Output voltage set point in PWM mode and in PFM mode if the PFM_VOFFSET_EN bit is not asserted For MV_RANGE = 0: VSET => 0.005V * m + 0.080V, where m = <7:0> For MV_RANGE = 1: VSET => 0.010V * m + 0.160V, where m = <7:0> If PFM_VOFFSET_EN is asserted and in PFM mode, add PFM_VOFFSET

0x11854 S2_PS_PHASE_CNT

Type: read-write
Clock: PBUS_WRCLK
Reset State: 0x00
Reset Name: PERPH_RB

PMIC_GANGED, PMIC_SYNC=clk_19p2:phase_cnt_rb

S2_PS_PHASE_CNT

Bits	Name	Type	Description
1:0	PHASE_CNT	read-write	When MULTIPHASE_EN is asserted, the number of operating phases is 00 = Number of operating phases is 1 01 = Number of operating phases is 2 10 = Number of operating phases is 4 11 = Number of operating phases is 4

8.6 S2_FREQ_BCLK_GEN_CLK

0x11904 S2_FREQ_PERPH_TYPE

Type: read-only
Clock: PBUS_WRCLK
Reset State: 0x1D
Reset Name: N/A

Peripheral Type

S2_FREQ_PERPH_TYPE

Bits	Name	Type	Description
7:0	TYPE	read-only	BCLK GEN

0x11905 S2_FREQ_PERPH_SUBTYPE

Type: read-only
Clock: PBUS_WRCLK
Reset State: 0x09
Reset Name: N/A

Peripheral SubType

S2_FREQ_PERPH_SUBTYPE

Bits	Name	Type	Description
7:0	SUBTYPE	read-only	BCLK GEN CLK

0x11946 S2_FREQ_CLK_ENABLE

Type: read-write
Clock: PBUS_WRCLK
Reset State: 0x01
Reset Name: PERPH_RB

S2_FREQ_CLK_ENABLE

Bits	Name	Type	Description
7	EN_CLK_INT	read-write	0 = do not force the clock on 1 = enable the clock
0	FOLLOW_CLK_SX_REQ	read-write	0 = ignore smps_clk_req<X> 1 = clock is enabled when the clocks request is high smps_clk_req<X>='1'

0x11950 S2_FREQ_CLK_DIV

Type: read-write
Clock: PBUS_WRCLK
Reset State: 0x05
Reset Name: PERPH_RB

PMIC_GANGED

S2_FREQ_CLK_DIV

Bits	Name	Type	Description
3:0	CLK_DIV	read-write	clock_ frequency = 19.2MHz / (CLK_DIV + 1) FTS2 Buck supports 3.2, 4.8, 6.4 and 9.6 MHz HF2 Buck supports 1.6, 2.4, 2.74, 3.2, 3.8, 4.8, and 6.4 MHz CLK_DIV = 0 is not supported, it will generate 9.6 MHz

0x11951 S2_FREQ_CLK_PHASE

Type: read-write
Clock: PBUS_WRCLK
Reset State: 0x01
Reset Name: PERPH_RB

S2_FREQ_CLK_PHASE

Bits	Name	Type	Description
3:0	CLK_PHASE	read-write	Distributed clock phase select: clock phase delay = clock period * (CLK_PHASE / 16)

0x119C0 S2_FREQ_GANG_CTL1

Type: read-write
Clock: PBUS_WRCLK
Reset State: 0x17
Reset Name: PERPH_RB

S2_FREQ_GANG_CTL1

Bits	Name	Type	Description
7:0	GANG_LEADER_PID	read-write	When GANG_EN (GANG_CTL2[7]) is set, this peripheral will write the same data that is written to the gang leader Peripheral ID. Reads to the gang leader Peripheral ID are ignored by this peripheral. Ganged peripherals must reside within the same Slave ID

0x119C1 S2_FREQ_GANG_CTL2

Type: read-write
Clock: PBUS_WRCLK
Reset State: 0x80
Reset Name: PERPH_RB

S2_FREQ_GANG_CTL2

Bits	Name	Type	Description
7	GANG_EN	read-write	0 = disable 1 = enable When enabled, this peripheral will write the same data that is written to the gang leader PID. Reads to the gang leader PID are ignored by this peripheral

8.7 S3_CTRL_HFBUCK2_CTRL

0x11A04 S3_CTRL_PERPH_TYPE

Type: read-only
Clock: PBUS_WRCLK
Reset State: 0x03
Reset Name: N/A

Peripheral Type

S3_CTRL_PERPH_TYPE

Bits	Name	Type	Description
7:0	TYPE	read-only	SMPS

0x11A05 S3_CTRL_PERPH_SUBTYPE

Type: read-only
Clock: PBUS_WRCLK
Reset State: 0x08
Reset Name: N/A

Peripheral SubType

S3_CTRL_PERPH_SUBTYPE

Bits	Name	Type	Description
7:0	SUBTYPE	read-only	2A HF BUCK

0x11A08 S3_CTRL_STATUS

Type: read-only
Clock: PBUS_WRCLK
Reset State: Undefined
Reset Name: N/A

Status Registers

S3_CTRL_STATUS

Bits	Name	Type	Description
7	VREG_OK	read-only	0 = VREG output voltage is below VREG_OK threshold 1 = VREG output voltage is above VREG_OK threshold

S3_CTRL_STATUS (Continued)

Bits	Name	Type	Description
5	ILS	read-only	Illegal Limit Stop. This is triggered when UL_Voltage < LL_Voltage
4	UL_VOLTAGE	read-only	Last voltage set was above or equal to UL_Voltage
3	LL_VOLTAGE	read-only	Last voltage set was below or equal to LL_Voltage
2	PS_TRUE	read-only	0 = buck is not pulse skipping 1 = buck is pulse skipping
1	NPM_TRUE	read-only	1 = VREG_OK and BUCK is in NPM
0	STEPPER_DONE	read-only	1 = stepper is done

0x11A10 S3_CTRL_INT_RT_STS

Type: read-only
Clock: PBUS_WRCLK
Reset State: 0x00
Reset Name: PERPH_RB

Interrupt Real Time Status Bits

S3_CTRL_INT_RT_STS

Bits	Name	Type	Description
1	LIMIT_ERR_INT	read-only	Last voltage set was above UL or below LL
0	VREG_OK_INT	read-only	Regulator has been successfully enabled

0x11A11 S3_CTRL_INT_SET_TYPE

Type: read-write
Clock: PBUS_WRCLK
Reset State: 0x00
Reset Name: PERPH_RB

0 = use level trigger interrupts, 1 = use edge trigger interrupts

S3_CTRL_INT_SET_TYPE

Bits	Name	Type	Description
1	LIMIT_ERR_INT	read-write	
0	VREG_OK_INT	read-write	

0x11A12 S3_CTRL_INT_POLARITY_HIGH

Type: read-write
Clock: PBUS_WRCLK
Reset State: 0x00
Reset Name: PERPH_RB

1= Interrupt will trigger on a level high (rising edge) event, 0 = level high triggering is disabled

S3_CTRL_INT_POLARITY_HIGH

Bits	Name	Type	Description
1	LIMIT_ERR_INT	read-write	
0	VREG_OK_INT	read-write	

0x11A13 S3_CTRL_INT_POLARITY_LOW

Type: read-write
Clock: PBUS_WRCLK
Reset State: 0x00
Reset Name: PERPH_RB

1' = Interrupt will trigger on a level low (falling edge) event, '0' = level low triggering is disabled

S3_CTRL_INT_POLARITY_LOW

Bits	Name	Type	Description
1	LIMIT_ERR_INT	read-write	
0	VREG_OK_INT	read-write	

0x11A14 S3_CTRL_INT_LATCHED_CLR

Type: write-only
Clock: PBUS_WRCLK
Reset State: 0x00
Reset Name: PERPH_RB

Writing a '1' to this interrupt will rearm the interrupt when an interrupt is pending. It clears the internal sticky and sent bits

S3_CTRL_INT_LATCHED_CLR

Bits	Name	Type	Description
1	LIMIT_ERR_INT	write-only	
0	VREG_OK_INT	write-only	

0x11A15 S3_CTRL_INT_EN_SET

Type: read-write
Clock: PBUS_WRCLK
Reset State: 0x00
Reset Name: PERPH_RB

Writing '0' to this register has no effect. Writing a '1' will enable the corresponding interrupt. Reading this register will readback enable status

PMIC_SET_MASK

S3_CTRL_INT_EN_SET

Bits	Name	Type	Description
1	LIMIT_ERR_INT	read-write	
0	VREG_OK_INT	read-write	

0x11A16 S3_CTRL_INT_EN_CLR

Type: read-write
Clock: PBUS_WRCLK
Reset State: 0x00
Reset Name: PERPH_RB

Writing '0' to this register has no effect. Writing a '1' will disable the corresponding interrupt. Reading this register will readback enable status

PMIC_CLR_MASK=INT_EN_SET

S3_CTRL_INT_EN_CLR

Bits	Name	Type	Description
1	LIMIT_ERR_INT	read-write	
0	VREG_OK_INT	read-write	

0x11A18 S3_CTRL_INT_LATCHED_STS

Type: read-only
Clock: PBUS_WRCLK
Reset State: 0x00
Reset Name: PERPH_RB

Debug: Latched (Sticky) Interrupt. '1' indicates that the interrupt has triggered. Once the latched bit is set it can only be cleared by writing the clear bit.

S3_CTRL_INT_LATCHED_STS

Bits	Name	Type	Description
1	LIMIT_ERR_INT	read-only	
0	VREG_OK_INT	read-only	

0x11A19 S3_CTRL_INT_PENDING_STS

Type: read-only
Clock: PBUS_WRCLK
Reset State: 0x00
Reset Name: PERPH_RB

Debug: Pending is set if interrupt has been sent but not cleared.

S3_CTRL_INT_PENDING_STS

Bits	Name	Type	Description
1	LIMIT_ERR_INT	read-only	
0	VREG_OK_INT	read-only	

0x11A1A S3_CTRL_INT_MID_SEL

Type: read-write
Clock: PBUS_WRCLK
Reset State: 0x00
Reset Name: PERPH_RB

Selects the MID that will receive the interrupt

S3_CTRL_INT_MID_SEL

Bits	Name	Type	Description
1:0	INT_MID_SEL	read-write	

0x11A1B S3_CTRL_INT_PRIORITY

Type: read-write
Clock: PBUS_WRCLK
Reset State: 0x00
Reset Name: PERPH_RB

S3_CTRL_INT_PRIORITY

Bits	Name	Type	Description
0	INT_PRIORITY	read-write	SR=0 A=1

0x11A40 S3_CTRL_VOLTAGE_CTL1

Type: read-write
Clock: PBUS_WRCLK
Reset State: 0x00
Reset Name: PERPH_RB

PMIC_LATCHED_WRITE=VOLTAGE_CTL2

S3_CTRL_VOLTAGE_CTL1

Bits	Name	Type	Description
0	RANGE	read-write	0 : 0.375 to 1.5625 V at steps of 12.5 mV (Vmin = 0.375 V, Vstep = 12.5 mV) 1 : 1.550 to 3.1250 V at steps of 25.0 mV (Vmin = 1.550 V, Vstep = 25.0 mV)

0x11A41 S3_CTRL_VOLTAGE_CTL2

Type: read-write
Clock: PBUS_WRCLK
Reset State: 0x3E
Reset Name: PERPH_RB

S3_CTRL_VOLTAGE_CTL2

Bits	Name	Type	Description
6:0	V_SET	read-write	Voltage = Vmin + VSET*(Vstep)

0x11A45 S3_CTRL_MODE_CTL

Type: read-write
Clock: PBUS_WRCLK
Reset State: 0x80
Reset Name: PERPH_RB

Define Buck Mode Transitions

S3_CTRL_MODE_CTL

Bits	Name	Type	Description
7	PWM	read-write	Force PWM
6	AUTO_MODE	read-write	1=Automatically enter NPM based on current
4	FOLLOW_PMIC_AWAKE	read-write	NPM when PMIC_AWAKE (SLEEP_B) = '1'
3	FOLLOW_HWEN3	read-write	1' BUCK is in NPM when HWEN3 ='1', '0'= ignore HWEN3
2	FOLLOW_HWEN2	read-write	1' BUCK is in NPM when HWEN2 ='1', '0'= ignore HWEN2
1	FOLLOW_HWEN1	read-write	1' BUCK is in NPM when HWEN1 ='1', '0'= ignore HWEN1
0	FOLLOW_HWEN0	read-write	1' BUCK is in NPM when HWEN0 ='1', '0'= ignore HWEN0

0x11A46 S3_CTRL_EN_CTL

Type: read-write
Clock: PBUS_WRCLK
Reset State: 0x00
Reset Name: PERPH_RB

S3_CTRL_EN_CTL

Bits	Name	Type	Description
7	PERPH_EN	read-write	1' = Enable the BUCK, '0' = do not force BUCK on
3	FOLLOW_HWEN3	read-write	1' BUCK is enabled when HWEN3 ='1', '0'= ignore HWEN3
2	FOLLOW_HWEN2	read-write	1' BUCK is enabled when HWEN2 ='1', '0'= ignore HWEN2
1	FOLLOW_HWEN1	read-write	1' BUCK is enabled when HWEN1 ='1', '0'= ignore HWEN1
0	FOLLOW_HWEN0	read-write	1' BUCK is enabled when HWEN0 ='1', '0'= ignore HWEN0

0x11A48 S3_CTRL_PD_CTL

Type: read-write
Clock: PBUS_WRCLK
Reset State: 0x80
Reset Name: PERPH_RB

S3_CTRL_PD_CTL

Bits	Name	Type	Description
7	PD_EN	read-write	1' = Enable the pulldown when the regulator is disabled, '0' = pulldown is always disabled. Preset by trim register

8.8 S3_FREQ_BCLK_GEN_CLK

0x11C04 S3_FREQ_PERPH_TYPE

Type: read-only
Clock: PBUS_WRCLK
Reset State: 0x1D
Reset Name: N/A

Peripheral Type

S3_FREQ_PERPH_TYPE

Bits	Name	Type	Description
7:0	TYPE	read-only	BCLK GEN

0x11C05 S3_FREQ_PERPH_SUBTYPE

Type: read-only
Clock: PBUS_WRCLK
Reset State: 0x09
Reset Name: N/A

Peripheral SubType

S3_FREQ_PERPH_SUBTYPE

Bits	Name	Type	Description
7:0	SUBTYPE	read-only	BCLK GEN CLK

0x11C46 S3_FREQ_CLK_ENABLE

Type: read-write
Clock: PBUS_WRCLK
Reset State: 0x01
Reset Name: PERPH_RB

S3_FREQ_CLK_ENABLE

Bits	Name	Type	Description
7	EN_CLK_INT	read-write	0 = do not force the clock on 1 = enable the clock
0	FOLLOW_CLK_SX_REQ	read-write	0 = ignore smps_clk_req<X> 1 = clock is enabled when the clocks request is high smps_clk_req<X>='1'

0x11C50 S3_FREQ_CLK_DIV

Type: read-write
Clock: PBUS_WRCLK
Reset State: 0x05
Reset Name: PERPH_RB

PMIC_GANGED

S3_FREQ_CLK_DIV

Bits	Name	Type	Description
3:0	CLK_DIV	read-write	clock_ frequency = 19.2MHz / (CLK_DIV + 1) FTS2 Buck supports 3.2, 4.8, 6.4 and 9.6 MHz HF2 Buck supports 1.6, 2.4, 2.74, 3.2, 3.8, 4.8, and 6.4 MHz CLK_DIV = 0 is not supported, it will generate 9.6 MHz

0x11C51 S3_FREQ_CLK_PHASE

Type: read-write
Clock: PBUS_WRCLK
Reset State: 0x07
Reset Name: PERPH_RB

S3_FREQ_CLK_PHASE

Bits	Name	Type	Description
3:0	CLK_PHASE	read-write	Distributed clock phase select: clock phase delay = clock period * (CLK_PHASE / 16)

0x11CC0 S3_FREQ_GANG_CTL1

Type: read-write
Clock: PBUS_WRCLK
Reset State: 0x00
Reset Name: PERPH_RB

S3_FREQ_GANG_CTL1

Bits	Name	Type	Description
7:0	GANG_LEADER_PID	read-write	When GANG_EN (GANG_CTL2[7]) is set, this peripheral will write the same data that is written to the gang leader Peripheral ID. Reads to the gang leader Peripheral ID are ignored by this peripheral. Ganged peripherals must reside within the same Slave ID

0x11CC1 S3_FREQ_GANG_CTL2

Type: read-write
Clock: PBUS_WRCLK
Reset State: 0x00
Reset Name: PERPH_RB

S3_FREQ_GANG_CTL2

Bits	Name	Type	Description
7	GANG_EN	read-write	0 = disable 1 = enable When enabled, this peripheral will write the same data that is written to the gang leader PID. Reads to the gang leader PID are ignored by this peripheral

8.9 S4_CTRL_FTS2_CTRL

0x11D04 S4_CTRL_PERPH_TYPE

Type: read-only
Clock: PBUS_WRCLK
Reset State: 0x03
Reset Name: N/A

Peripheral Type

S4_CTRL_PERPH_TYPE

Bits	Name	Type	Description
7:0	TYPE	read-only	FTS2 Control Reset State: 0x03

0x11D05 S4_CTRL_PERPH_SUBTYPE

Type: read-only
Clock: PBUS_WRCLK
Reset State: 0x08
Reset Name: N/A

Peripheral SubType

S4_CTRL_PERPH_SUBTYPE

Bits	Name	Type	Description
7:0	SUBTYPE	read-only	

0x11D08 S4_CTRL_STATUS_1

Type: read-only
Clock: PBUS_WRCLK
Reset State: Undefined
Reset Name: N/A

Status Registers

S4_CTRL_STATUS_1

Bits	Name	Type	Description
7	VREG_OK_FLAG	read-only	Indicates that VREG_SNS has reached a value that is greater than or equal to the threshold of the comparator tasked for VREG_SNS monitoring

S4_CTRL_STATUS_1 (Continued)

Bits	Name	Type	Description
6	VREG_FAULT_FLAG	read-only	Indicates a probable short circuit condition at VREG_SNS since VREG_SNS is below the VREG fault voltage level and the softstart ramp is done. Current limit foldback is in use.
1	NPM_FLAG	read-only	Indicates normal power mode is in use
0	STEPPER_DONE_FLAG	read-only	Softstart stepper and voltage stepper done

0x11D09 S4_CTRL_STATUS_2

Type: read-only
Clock: PBUS_WRCLK
Reset State: Undefined
Reset Name: N/A

Status Registers

S4_CTRL_STATUS_2

Bits	Name	Type	Description
4	ILS_FLAG	read-only	Either of the following: => Both limit stops have been enabled, but the upper limit stop VSET_ULS has been programmed to a value below the lower limit stop VSET_LLS => Both limit stops have been enabled, but the lower limit stop VSET_LLS has been programmed to a value above the upper limit stop VSET_ULS
3	ULS_FLAG	read-only	Indicates that the voltage setpoint has been programmed to a value that is greater than or equal to the upper limit stop VSET_ULS
2	LLS_FLAG	read-only	Indicates that the voltage setpoint has been programmed to a value that is less than or equal to the lower limit stop VSET_LLS
1	GPL_HI_FLAG	read-only	Indicates that the voltage setpoint has reached a value that is greater than or equal to the high general purpose limit VSET_GPL_HI
0	GPL_LO_FLAG	read-only	Indicates that the voltage setpoint has reached a value that is less than or equal to the low general purpose limit VSET_GPL_LO

0x11D10 S4_CTRL_INT_RT_STS

Type: read-only
Clock: PBUS_WRCLK
Reset State: Undefined
Reset Name: PERPH_RB

Interrupt Real Time Status Bits

S4_CTRL_INT_RT_STS

Bits	Name	Type	Description
2	VREG_FAULT_INT	read-only	
1	LIMIT_ERR_INT	read-only	
0	VREG_OK_INT	read-only	

0x11D11 S4_CTRL_INT_SET_TYPE

Type: read-write
Clock: PBUS_WRCLK
Reset State: 0x00
Reset Name: PERPH_RB

0 = use level trigger interrupts, 1 = use edge trigger interrupts

S4_CTRL_INT_SET_TYPE

Bits	Name	Type	Description
2	VREG_FAULT_INT	read-write	
1	LIMIT_ERR_INT	read-write	
0	VREG_OK_INT	read-write	

0x11D12 S4_CTRL_INT_POLARITY_HIGH

Type: read-write
Clock: PBUS_WRCLK
Reset State: 0x00
Reset Name: PERPH_RB

1= Interrupt will trigger on a level high (rising edge) event, 0 = level high triggering is disabled

S4_CTRL_INT_POLARITY_HIGH

Bits	Name	Type	Description
2	VREG_FAULT_INT	read-write	
1	LIMIT_ERR_INT	read-write	
0	VREG_OK_INT	read-write	

0x11D13 S4_CTRL_INT_POLARITY_LOW

Type: read-write
Clock: PBUS_WRCLK
Reset State: 0x00
Reset Name: PERPH_RB

1' = Interrupt will trigger on a level low (falling edge) event, '0' = level low triggering is disabled

S4_CTRL_INT_POLARITY_LOW

Bits	Name	Type	Description
2	VREG_FAULT_INT	read-write	
1	LIMIT_ERR_INT	read-write	
0	VREG_OK_INT	read-write	

0x11D14 S4_CTRL_INT_LATCHED_CLR

Type: write-only
Clock: PBUS_WRCLK
Reset State: 0x00
Reset Name: PERPH_RB

Writing a '1' to this interrupt will rearm the interrupt when an interrupt is pending. It clears the internal sticky and sent bits

S4_CTRL_INT_LATCHED_CLR

Bits	Name	Type	Description
2	VREG_FAULT_INT	write-only	

S4_CTRL_INT_LATCHED_CLR (Continued)

Bits	Name	Type	Description
1	LIMIT_ERR_INT	write-only	
0	VREG_OK_INT	write-only	

0x11D15 S4_CTRL_INT_EN_SET

Type: read-write
Clock: PBUS_WRCLK
Reset State: 0x00
Reset Name: PERPH_RB

Writing '0' to this register has no effect. Writing a '1' will enable the corresponding interrupt. Reading this register will readback enable status

PMIC_SET_MASK

S4_CTRL_INT_EN_SET

Bits	Name	Type	Description
2	VREG_FAULT_INT	read-write	
1	LIMIT_ERR_INT	read-write	
0	VREG_OK_INT	read-write	

0x11D16 S4_CTRL_INT_EN_CLR

Type: read-write
Clock: PBUS_WRCLK
Reset State: 0x00
Reset Name: PERPH_RB

Writing '0' to this register has no effect. Writing a '1' will disable the corresponding interrupt. Reading this register will readback enable status

PMIC_CLR_MASK=INT_EN_SET

S4_CTRL_INT_EN_CLR

Bits	Name	Type	Description
2	VREG_FAULT_INT	read-write	

S4_CTRL_INT_EN_CLR (Continued)

Bits	Name	Type	Description
1	LIMIT_ERR_INT	read-write	
0	VREG_OK_INT	read-write	

0x11D18 S4_CTRL_INT_LATCHED_STS

Type: read-only
Clock: PBUS_WRCLK
Reset State: 0x00
Reset Name: PERPH_RB

Debug: Latched (Sticky) Interrupt. '1' indicates that the interrupt has triggered. Once the latched bit is set it can only be cleared by writing the clear bit.

S4_CTRL_INT_LATCHED_STS

Bits	Name	Type	Description
2	VREG_FAULT_INT	read-only	
1	LIMIT_ERR_INT	read-only	
0	VREG_OK_INT	read-only	

0x11D19 S4_CTRL_INT_PENDING_STS

Type: read-only
Clock: PBUS_WRCLK
Reset State: 0x00
Reset Name: PERPH_RB

Debug: Pending is set if interrupt has been sent but not cleared.

S4_CTRL_INT_PENDING_STS

Bits	Name	Type	Description
2	VREG_FAULT_INT	read-only	
1	LIMIT_ERR_INT	read-only	
0	VREG_OK_INT	read-only	

0x11D1A S4_CTRL_INT_MID_SEL

Type: read-write
Clock: PBUS_WRCLK
Reset State: 0x00
Reset Name: PERPH_RB

Selects the MID that will receive the interrupt

S4_CTRL_INT_MID_SEL

Bits	Name	Type	Description
1:0	INT_MID_SEL	read-write	

0x11D1B S4_CTRL_INT_PRIORITY

Type: read-write
Clock: PBUS_WRCLK
Reset State: 0x00
Reset Name: PERPH_RB

SR=0 A=1

S4_CTRL_INT_PRIORITY

Bits	Name	Type	Description
0	INT_PRIORITY	read-write	

0x11D40 S4_CTRL_VOLTAGE_CTL1

Type: read-write
Clock: PBUS_WRCLK
Reset State: 0x00
Reset Name: PERPH_RB

PMIC_GANGED

S4_CTRL_VOLTAGE_CTL1

Bits	Name	Type	Description
0	MV_RANGE	read-write	0 = Use low voltage range as specified by VSET and PFM_VOFFSET 1 = Use medium voltage range as specified by VSET and PFM_VOFFSET

0x11D41 S4_CTRL_VOLTAGE_CTL2

Type: read-write
Clock: PBUS_WRCLK
Reset State: 0xB4
Reset Name: PERPH_RB

PMIC_GANGED

S4_CTRL_VOLTAGE_CTL2

Bits	Name	Type	Description
7:0	VSET	read-write	Output voltage set point in PWM mode and in PFM mode if the PFM_VOFFSET_EN bit is not asserted For MV_RANGE = 0: VSET => 0.005V * m + 0.080V, where m = <7:0> For MV_RANGE = 1: VSET => 0.010V * m + 0.160V, where m = <7:0> If PFM_VOFFSET_EN is asserted and in PFM mode, add PFM_VOFFSET

0x11D42 S4_CTRL_VSET_VALID

Type: read-only
Clock: PBUS_WRCLK
Reset State: Undefined
Reset Name: PERPH_RB

S4_CTRL_VSET_VALID

Bits	Name	Type	Description
7:0	VSET_VALID	read-only	Readback the valid output voltage setpoint value

0x11D44 S4_CTRL_VOLTAGE_CTL3

Type: read-write
Clock: PBUS_WRCLK
Reset State: 0x00
Reset Name: PERPH_RB

S4_CTRL_VOLTAGE_CTL3

Bits	Name	Type	Description
7	PFM_VOFFSET_EN	read-write	When in PFM mode 0 = Use VSET for output voltage set point 1 = Use VSET + PFM_VOFFSET for output voltage set point
1:0	PFM_VOFFSET	read-write	When in PFM mode and PFM_VOFFSET_EN is asserted, add a positive output voltage offset For MV_RANGE = 0: VOFFSET = 0.005V * 2 * m, where m = <1:0> For MV_RANGE = 1: VOFFSET = 0.010V * 2 * m, where m = <1:0>

0x11D45 S4_CTRL_MODE_CTL

Type: read-write
Clock: PBUS_WRCLK
Reset State: 0x80
Reset Name: PERPH_RB

PMIC_GANGED

S4_CTRL_MODE_CTL

Bits	Name	Type	Description
7	NPM	read-write	FTS NON-AUTO mode control 0 = Low power mode (LPM) unless AUTO_MODE is asserted 1 = Normal power mode (PWM)
6	AUTO_MODE	read-write	When asserted, FTS automatically enters and exits low power mode (PFM) based on load current qualifying triggers 0 = AUTO mode is disabled 1 = AUTO mode is enabled

0x11D46 S4_CTRL_EN_CTL

Type: read-write
Clock: PBUS_WRCLK
Reset State: 0x00
Reset Name: PERPH_RB

PMIC_GANGED

S4_CTRL_EN_CTL

Bits	Name	Type	Description
7	PERPH_EN	read-write	FTS enable control 0 = Off 1 = On

0x11D48 S4_CTRL_PD_CTL

Type: read-write
Clock: PBUS_WRCLK
Reset State: 0x80
Reset Name: PERPH_RB

S4_CTRL_PD_CTL

Bits	Name	Type	Description
7	PD_EN	read-write	0 = Strong pulldown is always disabled 1 = Strong pulldown is enabled when the regulator is disabled
6	WEAK_PD_EN	read-write	0 = Weak pulldown is not enabled in OFF state 1 = Weak pulldown is enabled in OFF state
5	WEAK_PD_PFM	read-write	0 = Weak pulldown is not enabled in PFM mode 1 = Weak pulldown is enabled in PFM mode
4	WEAK_PD_PWM	read-write	0 = Weak pulldown is not enabled in PWM mode (and in HCPFM mode) 1 = Weak pulldown is enabled in PWM mode (and in HCPFM mode)

0x11D54 S4_CTRL_PHASE_CNT

Type: read-write
Clock: PBUS_WRCLK
Reset State: 0x00
Reset Name: PERPH_RB

PMIC_GANGED

S4_CTRL_PHASE_CNT

Bits	Name	Type	Description
1:0	PHASE_CNT	read-write	When MULTIPHASE_EN is asserted, the number of operating phases is 00 = Number of operating phases is 1 01 = Number of operating phases is 2 10 = Number of operating phases is 4 11 = Number of operating phases is 4

0x11D60 S4_CTRL_SS_CTL

Type: read-write
Clock: PBUS_WRCLK
Reset State: 0x08
Reset Name: PERPH_RB

PMIC_GANGED

S4_CTRL_SS_CTL

Bits	Name	Type	Description
4:3	SS_STEP	read-write	Softstart voltage step size 00 = SS voltage step of 1 * LSB of VPROG 01 = SS voltage step of 2 * LSB 10 = SS voltage step of 4 * LSB 11 = SS voltage step of 8 * LSB
2:0	SS_DELAY	read-write	Softstart delay between steps = 2 ^ (m + 3) / Fsys, where m = <2:0> (Fsys = 19.2 MHz): 000 = 8-clock cycles (417ns) 001 = 16-clock cycles 010 = 32-clock cycles 011 = 64-clock cycles 100 = 128-clock cycles (6.67us) 101 = 256-clock cycles 110 = 512-clock cycles 111 = 1024-clock cycles (53.3us)

0x11D61 S4_CTRL_VS_CTL

Type: read-write
Clock: PBUS_WRCLK
Reset State: 0x00
Reset Name: PERPH_RB

PMIC_GANGED

S4_CTRL_VS_CTL

Bits	Name	Type	Description
7	VS_EN	read-write	Voltage stepping control 0 = VS is disabled 1 = VS is enabled
4:3	VS_STEP	read-write	Voltage stepping voltage step size 00 = VS voltage step of 1 * LSB of VPROG 01 = VS voltage step of 2 * LSB 10 = VS voltage step of 4 * LSB 11 = VS voltage step of 8 * LSB
2:0	VS_DELAY	read-write	Voltage stepping delay between steps = 2 ^ (m + 3) / Fsys, where m = <2:0> (Assuming Fsys = 19.2 MHz): Desired default is 1.67us 000 = 8-clock cycles (417ns) 001 = 16-clock cycles 010 = 32-clock cycles 011 = 64-clock cycles 100 = 128-clock cycles (6.67us) 101 = 256-clock cycles 110 = 512-clock cycles 111 = 1024-clock cycles (53.3us)

0x11D6A S4_CTRL_ULS_VALID

Type: read-only
Clock: PBUS_WRCLK
Reset State: Undefined
Reset Name: PERPH_RB

S4_CTRL_ULS_VALID

Bits	Name	Type	Description
7:0	ULS_VALID	read-only	Readback the valid upper limit stop value

0x11D6C S4_CTRL_LLS_VALID

Type: read-only
Clock: PBUS_WRCLK
Reset State: Undefined
Reset Name: PERPH_RB

S4_CTRL_LLS_VALID

Bits	Name	Type	Description
7:0	LLS_VALID	read-only	Readback the valid lower limit stop value

8.10 S4_PS_FTS2_PS

0x11E04 S4_PS_PERPH_TYPE

Type: read-only
Clock: PBUS_WRCLK
Reset State: 0x1C
Reset Name: N/A

Peripheral Type

S4_PS_PERPH_TYPE

Bits	Name	Type	Description
7:0	TYPE	read-only	FTS2 Power Stage Reset State: 0x1C

0x11E05 S4_PS_PERPH_SUBTYPE

Type: read-only
Clock: PBUS_WRCLK
Reset State: 0x08
Reset Name: N/A

Peripheral SubType

S4_PS_PERPH_SUBTYPE

Bits	Name	Type	Description
7:0	SUBTYPE	read-only	

0x11E40 S4_PS_VOLTAGE_CTL1

Type: read-write
Clock: PBUS_WRCLK
Reset State: 0x00
Reset Name: PERPH_RB

PMIC_GANGED

S4_PS_VOLTAGE_CTL1

Bits	Name	Type	Description
0	MV_RANGE	read-write	0 = Use low voltage range as specified by VSET and PFM_VOFFSET 1 = Use medium voltage range as specified by VSET and PFM_VOFFSET

0x11E41 S4_PS_VOLTAGE_CTL2

Type: read-write
Clock: PBUS_WRCLK
Reset State: 0xB4
Reset Name: PERPH_RB

PMIC_GANGED

S4_PS_VOLTAGE_CTL2

Bits	Name	Type	Description
7:0	VSET	read-write	Output voltage set point in PWM mode and in PFM mode if the PFM_VOFFSET_EN bit is not asserted For MV_RANGE = 0: VSET => 0.005V * m + 0.080V, where m = <7:0> For MV_RANGE = 1: VSET => 0.010V * m + 0.160V, where m = <7:0> If PFM_VOFFSET_EN is asserted and in PFM mode, add PFM_VOFFSET

0x11E54 S4_PS_PHASE_CNT

Type: read-write
Clock: PBUS_WRCLK
Reset State: 0x00
Reset Name: PERPH_RB

PMIC_GANGED, PMIC_SYNC=clk_19p2:phase_cnt_rb

S4_PS_PHASE_CNT

Bits	Name	Type	Description
1:0	PHASE_CNT	read-write	When MULTIPHASE_EN is asserted, the number of operating phases is 00 = Number of operating phases is 1 01 = Number of operating phases is 2 10 = Number of operating phases is 4 11 = Number of operating phases is 4

8.11 S4_FREQ_BCLK_GEN_CLK

0x11F04 S4_FREQ_PERPH_TYPE

Type: read-only
Clock: PBUS_WRCLK
Reset State: 0x1D
Reset Name: N/A

Peripheral Type

S4_FREQ_PERPH_TYPE

Bits	Name	Type	Description
7:0	TYPE	read-only	BCLK GEN

0x11F05 S4_FREQ_PERPH_SUBTYPE

Type: read-only
Clock: PBUS_WRCLK
Reset State: 0x09
Reset Name: N/A

Peripheral SubType

S4_FREQ_PERPH_SUBTYPE

Bits	Name	Type	Description
7:0	SUBTYPE	read-only	BCLK GEN CLK

0x11F46 S4_FREQ_CLK_ENABLE

Type: read-write
Clock: PBUS_WRCLK
Reset State: 0x01
Reset Name: PERPH_RB

S4_FREQ_CLK_ENABLE

Bits	Name	Type	Description
7	EN_CLK_INT	read-write	0 = do not force the clock on 1 = enable the clock
0	FOLLOW_CLK_SX_REQ	read-write	0 = ignore smps_clk_req<X> 1 = clock is enabled when the clocks request is high smps_clk_req<X>='1'

0x11F50 S4_FREQ_CLK_DIV

Type: read-write
Clock: PBUS_WRCLK
Reset State: 0x05
Reset Name: PERPH_RB

PMIC_GANGED

S4_FREQ_CLK_DIV

Bits	Name	Type	Description
3:0	CLK_DIV	read-write	clock_ frequency = 19.2MHz / (CLK_DIV + 1) FTS2 Buck supports 3.2, 4.8, 6.4 and 9.6 MHz HF2 Buck supports 1.6, 2.4, 2.74, 3.2, 3.8, 4.8, and 6.4 MHz CLK_DIV = 0 is not supported, it will generate 9.6 MHz

0x11F51 S4_FREQ_CLK_PHASE

Type: read-write
Clock: PBUS_WRCLK
Reset State: 0x03
Reset Name: PERPH_RB

S4_FREQ_CLK_PHASE

Bits	Name	Type	Description
3:0	CLK_PHASE	read-write	Distributed clock phase select: clock phase delay = clock period * (CLK_PHASE / 16)

0x11FC0 S4_FREQ_GANG_CTL1

Type: read-write
Clock: PBUS_WRCLK
Reset State: 0x1D
Reset Name: PERPH_RB

S4_FREQ_GANG_CTL1

Bits	Name	Type	Description
7:0	GANG_LEADER_PID	read-write	When GANG_EN (GANG_CTL2[7]) is set, this peripheral will write the same data that is written to the gang leader Peripheral ID. Reads to the gang leader Peripheral ID are ignored by this peripheral. Ganged peripherals must reside within the same Slave ID

0x11FC1 S4_FREQ_GANG_CTL2

Type: read-write
Clock: PBUS_WRCLK
Reset State: 0x80
Reset Name: PERPH_RB

S4_FREQ_GANG_CTL2

Bits	Name	Type	Description
7	GANG_EN	read-write	0 = disable 1 = enable When enabled, this peripheral will write the same data that is written to the gang leader PID. Reads to the gang leader PID are ignored by this peripheral

8.12 S5_CTRL_FTS2_CTRL

0x12004 S5_CTRL_PERPH_TYPE

Type: read-only
Clock: PBUS_WRCLK
Reset State: 0x03
Reset Name: N/A

Peripheral Type

S5_CTRL_PERPH_TYPE

Bits	Name	Type	Description
7:0	TYPE	read-only	FTS2 Control Reset State: 0x03

0x12005 S5_CTRL_PERPH_SUBTYPE

Type: read-only
Clock: PBUS_WRCLK
Reset State: 0x08
Reset Name: N/A

Peripheral SubType

S5_CTRL_PERPH_SUBTYPE

Bits	Name	Type	Description
7:0	SUBTYPE	read-only	

0x12008 S5_CTRL_STATUS_1

Type: read-only
Clock: PBUS_WRCLK
Reset State: Undefined
Reset Name: N/A

Status Registers

S5_CTRL_STATUS_1

Bits	Name	Type	Description
7	VREG_OK_FLAG	read-only	Indicates that VREG_SNS has reached a value that is greater than or equal to the threshold of the comparator tasked for VREG_SNS monitoring

S5_CTRL_STATUS_1 (Continued)

Bits	Name	Type	Description
6	VREG_FAULT_FLAG	read-only	Indicates a probable short circuit condition at VREG_SNS since VREG_SNS is below the VREG fault voltage level and the softstart ramp is done. Current limit foldback is in use.
1	NPM_FLAG	read-only	Indicates normal power mode is in use
0	STEPPER_DONE_FLAG	read-only	Softstart stepper and voltage stepper done

0x12009 S5_CTRL_STATUS_2

Type: read-only
Clock: PBUS_WRCLK
Reset State: Undefined
Reset Name: N/A

Status Registers

S5_CTRL_STATUS_2

Bits	Name	Type	Description
4	ILS_FLAG	read-only	Either of the following: => Both limit stops have been enabled, but the upper limit stop VSET_ULS has been programmed to a value below the lower limit stop VSET_LLS => Both limit stops have been enabled, but the lower limit stop VSET_LLS has been programmed to a value above the upper limit stop VSET_ULS
3	ULS_FLAG	read-only	Indicates that the voltage setpoint has been programmed to a value that is greater than or equal to the upper limit stop VSET_ULS
2	LLS_FLAG	read-only	Indicates that the voltage setpoint has been programmed to a value that is less than or equal to the lower limit stop VSET_LLS
1	GPL_HI_FLAG	read-only	Indicates that the voltage setpoint has reached a value that is greater than or equal to the high general purpose limit VSET_GPL_HI
0	GPL_LO_FLAG	read-only	Indicates that the voltage setpoint has reached a value that is less than or equal to the low general purpose limit VSET_GPL_LO

0x12010 S5_CTRL_INT_RT_STS

Type: read-only
Clock: PBUS_WRCLK
Reset State: Undefined
Reset Name: PERPH_RB

Interrupt Real Time Status Bits

S5_CTRL_INT_RT_STS

Bits	Name	Type	Description
2	VREG_FAULT_INT	read-only	
1	LIMIT_ERR_INT	read-only	
0	VREG_OK_INT	read-only	

0x12011 S5_CTRL_INT_SET_TYPE

Type: read-write
Clock: PBUS_WRCLK
Reset State: 0x00
Reset Name: PERPH_RB

0 = use level trigger interrupts, 1 = use edge trigger interrupts

S5_CTRL_INT_SET_TYPE

Bits	Name	Type	Description
2	VREG_FAULT_INT	read-write	
1	LIMIT_ERR_INT	read-write	
0	VREG_OK_INT	read-write	

0x12012 S5_CTRL_INT_POLARITY_HIGH

Type: read-write
Clock: PBUS_WRCLK
Reset State: 0x00
Reset Name: PERPH_RB

1= Interrupt will trigger on a level high (rising edge) event, 0 = level high triggering is disabled

S5_CTRL_INT_POLARITY_HIGH

Bits	Name	Type	Description
2	VREG_FAULT_INT	read-write	
1	LIMIT_ERR_INT	read-write	
0	VREG_OK_INT	read-write	

0x12013 S5_CTRL_INT_POLARITY_LOW

Type: read-write
Clock: PBUS_WRCLK
Reset State: 0x00
Reset Name: PERPH_RB

1' = Interrupt will trigger on a level low (falling edge) event, '0' = level low triggering is disabled

S5_CTRL_INT_POLARITY_LOW

Bits	Name	Type	Description
2	VREG_FAULT_INT	read-write	
1	LIMIT_ERR_INT	read-write	
0	VREG_OK_INT	read-write	

0x12014 S5_CTRL_INT_LATCHED_CLR

Type: write-only
Clock: PBUS_WRCLK
Reset State: 0x00
Reset Name: PERPH_RB

Writing a '1' to this interrupt will rearm the interrupt when an interrupt is pending. It clears the internal sticky and sent bits

S5_CTRL_INT_LATCHED_CLR

Bits	Name	Type	Description
2	VREG_FAULT_INT	write-only	

S5_CTRL_INT_LATCHED_CLR (Continued)

Bits	Name	Type	Description
1	LIMIT_ERR_INT	write-only	
0	VREG_OK_INT	write-only	

0x12015 S5_CTRL_INT_EN_SET

Type: read-write
Clock: PBUS_WRCLK
Reset State: 0x00
Reset Name: PERPH_RB

Writing '0' to this register has no effect. Writing a '1' will enable the corresponding interrupt. Reading this register will readback enable status

PMIC_SET_MASK

S5_CTRL_INT_EN_SET

Bits	Name	Type	Description
2	VREG_FAULT_INT	read-write	
1	LIMIT_ERR_INT	read-write	
0	VREG_OK_INT	read-write	

0x12016 S5_CTRL_INT_EN_CLR

Type: read-write
Clock: PBUS_WRCLK
Reset State: 0x00
Reset Name: PERPH_RB

Writing '0' to this register has no effect. Writing a '1' will disable the corresponding interrupt. Reading this register will readback enable status

PMIC_CLR_MASK=INT_EN_SET

S5_CTRL_INT_EN_CLR

Bits	Name	Type	Description
2	VREG_FAULT_INT	read-write	

S5_CTRL_INT_EN_CLR (Continued)

Bits	Name	Type	Description
1	LIMIT_ERR_INT	read-write	
0	VREG_OK_INT	read-write	

0x12018 S5_CTRL_INT_LATCHED_STS

Type: read-only
Clock: PBUS_WRCLK
Reset State: 0x00
Reset Name: PERPH_RB

Debug: Latched (Sticky) Interrupt. '1' indicates that the interrupt has triggered. Once the latched bit is set it can only be cleared by writing the clear bit.

S5_CTRL_INT_LATCHED_STS

Bits	Name	Type	Description
2	VREG_FAULT_INT	read-only	
1	LIMIT_ERR_INT	read-only	
0	VREG_OK_INT	read-only	

0x12019 S5_CTRL_INT_PENDING_STS

Type: read-only
Clock: PBUS_WRCLK
Reset State: 0x00
Reset Name: PERPH_RB

Debug: Pending is set if interrupt has been sent but not cleared.

S5_CTRL_INT_PENDING_STS

Bits	Name	Type	Description
2	VREG_FAULT_INT	read-only	
1	LIMIT_ERR_INT	read-only	
0	VREG_OK_INT	read-only	

0x1201A S5_CTRL_INT_MID_SEL

Type: read-write
Clock: PBUS_WRCLK
Reset State: 0x00
Reset Name: PERPH_RB

Selects the MID that will receive the interrupt

S5_CTRL_INT_MID_SEL

Bits	Name	Type	Description
1:0	INT_MID_SEL	read-write	

0x1201B S5_CTRL_INT_PRIORITY

Type: read-write
Clock: PBUS_WRCLK
Reset State: 0x00
Reset Name: PERPH_RB

SR=0 A=1

S5_CTRL_INT_PRIORITY

Bits	Name	Type	Description
0	INT_PRIORITY	read-write	

0x12040 S5_CTRL_VOLTAGE_CTL1

Type: read-write
Clock: PBUS_WRCLK
Reset State: 0x00
Reset Name: PERPH_RB

PMIC_GANGED

S5_CTRL_VOLTAGE_CTL1

Bits	Name	Type	Description
0	MV_RANGE	read-write	0 = Use low voltage range as specified by VSET and PFM_VOFFSET 1 = Use medium voltage range as specified by VSET and PFM_VOFFSET

0x12041 S5_CTRL_VOLTAGE_CTL2

Type: read-write
Clock: PBUS_WRCLK
Reset State: 0xB4
Reset Name: PERPH_RB

PMIC_GANGED

S5_CTRL_VOLTAGE_CTL2

Bits	Name	Type	Description
7:0	VSET	read-write	Output voltage set point in PWM mode and in PFM mode if the PFM_VOFFSET_EN bit is not asserted For MV_RANGE = 0: VSET => 0.005V * m + 0.080V, where m = <7:0> For MV_RANGE = 1: VSET => 0.010V * m + 0.160V, where m = <7:0> If PFM_VOFFSET_EN is asserted and in PFM mode, add PFM_VOFFSET

0x12042 S5_CTRL_VSET_VALID

Type: read-only
Clock: PBUS_WRCLK
Reset State: Undefined
Reset Name: PERPH_RB

S5_CTRL_VSET_VALID

Bits	Name	Type	Description
7:0	VSET_VALID	read-only	Readback the valid output voltage setpoint value

0x12044 S5_CTRL_VOLTAGE_CTL3

Type: read-write
Clock: PBUS_WRCLK
Reset State: 0x00
Reset Name: PERPH_RB

S5_CTRL_VOLTAGE_CTL3

Bits	Name	Type	Description
7	PFM_VOFFSET_EN	read-write	When in PFM mode 0 = Use VSET for output voltage set point 1 = Use VSET + PFM_VOFFSET for output voltage set point
1:0	PFM_VOFFSET	read-write	When in PFM mode and PFM_VOFFSET_EN is asserted, add a positive output voltage offset For MV_RANGE = 0: VOFFSET = 0.005V * 2 * m, where m = <1:0> For MV_RANGE = 1: VOFFSET = 0.010V * 2 * m, where m = <1:0>

0x12045 S5_CTRL_MODE_CTL

Type: read-write
Clock: PBUS_WRCLK
Reset State: 0x80
Reset Name: PERPH_RB

PMIC_GANGED

S5_CTRL_MODE_CTL

Bits	Name	Type	Description
7	NPM	read-write	FTS NON-AUTO mode control 0 = Low power mode (LPM) unless AUTO_MODE is asserted 1 = Normal power mode (PWM)
6	AUTO_MODE	read-write	When asserted, FTS automatically enters and exits low power mode (PFM) based on load current qualifying triggers 0 = AUTO mode is disabled 1 = AUTO mode is enabled

0x12046 S5_CTRL_EN_CTL

Type: read-write
Clock: PBUS_WRCLK
Reset State: 0x00
Reset Name: PERPH_RB

PMIC_GANGED

S5_CTRL_EN_CTL

Bits	Name	Type	Description
7	PERPH_EN	read-write	FTS enable control 0 = Off 1 = On

0x12048 S5_CTRL_PD_CTL

Type: read-write
Clock: PBUS_WRCLK
Reset State: 0x80
Reset Name: PERPH_RB

S5_CTRL_PD_CTL

Bits	Name	Type	Description
7	PD_EN	read-write	0 = Strong pulldown is always disabled 1 = Strong pulldown is enabled when the regulator is disabled
6	WEAK_PD_EN	read-write	0 = Weak pulldown is not enabled in OFF state 1 = Weak pulldown is enabled in OFF state
5	WEAK_PD_PFM	read-write	0 = Weak pulldown is not enabled in PFM mode 1 = Weak pulldown is enabled in PFM mode
4	WEAK_PD_PWM	read-write	0 = Weak pulldown is not enabled in PWM mode (and in HCPFM mode) 1 = Weak pulldown is enabled in PWM mode (and in HCPFM mode)

0x12054 S5_CTRL_PHASE_CNT

Type: read-write
Clock: PBUS_WRCLK
Reset State: 0x00
Reset Name: PERPH_RB

PMIC_GANGED

S5_CTRL_PHASE_CNT

Bits	Name	Type	Description
1:0	PHASE_CNT	read-write	When MULTIPHASE_EN is asserted, the number of operating phases is 00 = Number of operating phases is 1 01 = Number of operating phases is 2 10 = Number of operating phases is 4 11 = Number of operating phases is 4

0x12060 S5_CTRL_SS_CTL

Type: read-write
Clock: PBUS_WRCLK
Reset State: 0x00
Reset Name: PERPH_RB

PMIC_GANGED

S5_CTRL_SS_CTL

Bits	Name	Type	Description
4:3	SS_STEP	read-write	Softstart voltage step size 00 = SS voltage step of 1 * LSB of VPROG 01 = SS voltage step of 2 * LSB 10 = SS voltage step of 4 * LSB 11 = SS voltage step of 8 * LSB
2:0	SS_DELAY	read-write	Softstart delay between steps = 2 ^ (m + 3) / Fsys, where m = <2:0> (Fsys = 19.2 MHz): 000 = 8-clock cycles (417ns) 001 = 16-clock cycles 010 = 32-clock cycles 011 = 64-clock cycles 100 = 128-clock cycles (6.67us) 101 = 256-clock cycles 110 = 512-clock cycles 111 = 1024-clock cycles (53.3us)

0x12061 S5_CTRL_VS_CTL

Type: read-write
Clock: PBUS_WRCLK
Reset State: 0x00
Reset Name: PERPH_RB

PMIC_GANGED

S5_CTRL_VS_CTL

Bits	Name	Type	Description
7	VS_EN	read-write	Voltage stepping control 0 = VS is disabled 1 = VS is enabled
4:3	VS_STEP	read-write	Voltage stepping voltage step size 00 = VS voltage step of 1 * LSB of VPROG 01 = VS voltage step of 2 * LSB 10 = VS voltage step of 4 * LSB 11 = VS voltage step of 8 * LSB
2:0	VS_DELAY	read-write	Voltage stepping delay between steps = 2 ^ (m + 3) / Fsys, where m = <2:0> (Assuming Fsys = 19.2 MHz): Desired default is 1.67us 000 = 8-clock cycles (417ns) 001 = 16-clock cycles 010 = 32-clock cycles 011 = 64-clock cycles 100 = 128-clock cycles (6.67us) 101 = 256-clock cycles 110 = 512-clock cycles 111 = 1024-clock cycles (53.3us)

0x1206A S5_CTRL_ULS_VALID

Type: read-only
Clock: PBUS_WRCLK
Reset State: Undefined
Reset Name: PERPH_RB

S5_CTRL_ULS_VALID

Bits	Name	Type	Description
7:0	ULS_VALID	read-only	Readback the valid upper limit stop value

0x1206C S5_CTRL_LLS_VALID

Type: read-only
Clock: PBUS_WRCLK
Reset State: Undefined
Reset Name: PERPH_RB

S5_CTRL_LLS_VALID

Bits	Name	Type	Description
7:0	LLS_VALID	read-only	Readback the valid lower limit stop value

8.13 S5_PS_FTS2_PS

0x12104 S5_PS_PERPH_TYPE

Type: read-only
Clock: PBUS_WRCLK
Reset State: 0x1C
Reset Name: N/A

Peripheral Type

S5_PS_PERPH_TYPE

Bits	Name	Type	Description
7:0	TYPE	read-only	FTS2 Power Stage Reset State: 0x1C

0x12105 S5_PS_PERPH_SUBTYPE

Type: read-only
Clock: PBUS_WRCLK
Reset State: 0x08
Reset Name: N/A

Peripheral SubType

S5_PS_PERPH_SUBTYPE

Bits	Name	Type	Description
7:0	SUBTYPE	read-only	

0x12140 S5_PS_VOLTAGE_CTL1

Type: read-write
Clock: PBUS_WRCLK
Reset State: 0x00
Reset Name: PERPH_RB

PMIC_GANGED

S5_PS_VOLTAGE_CTL1

Bits	Name	Type	Description
0	MV_RANGE	read-write	0 = Use low voltage range as specified by VSET and PFM_VOFFSET 1 = Use medium voltage range as specified by VSET and PFM_VOFFSET

0x12141 S5_PS_VOLTAGE_CTL2

Type: read-write
Clock: PBUS_WRCLK
Reset State: 0xB4
Reset Name: PERPH_RB

PMIC_GANGED

S5_PS_VOLTAGE_CTL2

Bits	Name	Type	Description
7:0	VSET	read-write	Output voltage set point in PWM mode and in PFM mode if the PFM_VOFFSET_EN bit is not asserted For MV_RANGE = 0: VSET => 0.005V * m + 0.080V, where m = <7:0> For MV_RANGE = 1: VSET => 0.010V * m + 0.160V, where m = <7:0> If PFM_VOFFSET_EN is asserted and in PFM mode, add PFM_VOFFSET

0x12154 S5_PS_PHASE_CNT

Type: read-write
Clock: PBUS_WRCLK
Reset State: 0x00
Reset Name: PERPH_RB

PMIC_GANGED, PMIC_SYNC=clk_19p2:phase_cnt_rb

S5_PS_PHASE_CNT

Bits	Name	Type	Description
1:0	PHASE_CNT	read-write	When MULTIPHASE_EN is asserted, the number of operating phases is 00 = Number of operating phases is 1 01 = Number of operating phases is 2 10 = Number of operating phases is 4 11 = Number of operating phases is 4

8.14 S5_FREQ_BCLK_GEN_CLK

0x12204 S5_FREQ_PERPH_TYPE

Type: read-only
Clock: PBUS_WRCLK
Reset State: 0x1D
Reset Name: N/A

Peripheral Type

S5_FREQ_PERPH_TYPE

Bits	Name	Type	Description
7:0	TYPE	read-only	BCLK GEN

0x12205 S5_FREQ_PERPH_SUBTYPE

Type: read-only
Clock: PBUS_WRCLK
Reset State: 0x09
Reset Name: N/A

Peripheral SubType

S5_FREQ_PERPH_SUBTYPE

Bits	Name	Type	Description
7:0	SUBTYPE	read-only	BCLK GEN CLK

0x12246 S5_FREQ_CLK_ENABLE

Type: read-write
Clock: PBUS_WRCLK
Reset State: 0x01
Reset Name: PERPH_RB

S5_FREQ_CLK_ENABLE

Bits	Name	Type	Description
7	EN_CLK_INT	read-write	0 = do not force the clock on 1 = enable the clock
0	FOLLOW_CLK_SX_REQ	read-write	0 = ignore smps_clk_req<X> 1 = clock is enabled when the clocks request is high smps_clk_req<X>='1'

0x12250 S5_FREQ_CLK_DIV

Type: read-write
Clock: PBUS_WRCLK
Reset State: 0x02
Reset Name: PERPH_RB

PMIC_GANGED

S5_FREQ_CLK_DIV

Bits	Name	Type	Description
3:0	CLK_DIV	read-write	clock_ frequency = 19.2MHz / (CLK_DIV + 1) FTS2 Buck supports 3.2, 4.8, 6.4 and 9.6 MHz HF2 Buck supports 1.6, 2.4, 2.74, 3.2, 3.8, 4.8, and 6.4 MHz CLK_DIV = 0 is not supported, it will generate 9.6 MHz

0x12251 S5_FREQ_CLK_PHASE

Type: read-write
Clock: PBUS_WRCLK
Reset State: 0x00
Reset Name: PERPH_RB

S5_FREQ_CLK_PHASE

Bits	Name	Type	Description
3:0	CLK_PHASE	read-write	Distributed clock phase select: clock phase delay = clock period * (CLK_PHASE / 16)

0x122C0 S5_FREQ_GANG_CTL1

Type: read-write
Clock: PBUS_WRCLK
Reset State: 0x20
Reset Name: PERPH_RB

S5_FREQ_GANG_CTL1

Bits	Name	Type	Description
7:0	GANG_LEADER_PID	read-write	When GANG_EN (GANG_CTL2[7]) is set, this peripheral will write the same data that is written to the gang leader Peripheral ID. Reads to the gang leader Peripheral ID are ignored by this peripheral. Ganged peripherals must reside within the same Slave ID

0x122C1 S5_FREQ_GANG_CTL2

Type: read-write
Clock: PBUS_WRCLK
Reset State: 0x80
Reset Name: PERPH_RB

S5_FREQ_GANG_CTL2

Bits	Name	Type	Description
7	GANG_EN	read-write	0 = disable 1 = enable When enabled, this peripheral will write the same data that is written to the gang leader PID. Reads to the gang leader PID are ignored by this peripheral

8.15 S6_CTRL_FTS2_CTRL

0x12304 S6_CTRL_PERPH_TYPE

Type: read-only
Clock: PBUS_WRCLK
Reset State: 0x03
Reset Name: N/A

Peripheral Type

S6_CTRL_PERPH_TYPE

Bits	Name	Type	Description
7:0	TYPE	read-only	FTS2 Control Reset State: 0x03

0x12305 S6_CTRL_PERPH_SUBTYPE

Type: read-only
Clock: PBUS_WRCLK
Reset State: 0x08
Reset Name: N/A

Peripheral SubType

S6_CTRL_PERPH_SUBTYPE

Bits	Name	Type	Description
7:0	SUBTYPE	read-only	

0x12308 S6_CTRL_STATUS_1

Type: read-only
Clock: PBUS_WRCLK
Reset State: Undefined
Reset Name: N/A

Status Registers

S6_CTRL_STATUS_1

Bits	Name	Type	Description
7	VREG_OK_FLAG	read-only	Indicates that VREG_SNS has reached a value that is greater than or equal to the threshold of the comparator tasked for VREG_SNS monitoring

S6_CTRL_STATUS_1 (Continued)

Bits	Name	Type	Description
6	VREG_FAULT_FLAG	read-only	Indicates a probable short circuit condition at VREG_SNS since VREG_SNS is below the VREG fault voltage level and the softstart ramp is done. Current limit foldback is in use.
1	NPM_FLAG	read-only	Indicates normal power mode is in use
0	STEPPER_DONE_FLAG	read-only	Softstart stepper and voltage stepper done

0x12309 S6_CTRL_STATUS_2

Type: read-only
Clock: PBUS_WRCLK
Reset State: Undefined
Reset Name: N/A

Status Registers

S6_CTRL_STATUS_2

Bits	Name	Type	Description
4	ILS_FLAG	read-only	Either of the following: => Both limit stops have been enabled, but the upper limit stop VSET_ULS has been programmed to a value below the lower limit stop VSET_LLS => Both limit stops have been enabled, but the lower limit stop VSET_LLS has been programmed to a value above the upper limit stop VSET_ULS
3	ULS_FLAG	read-only	Indicates that the voltage setpoint has been programmed to a value that is greater than or equal to the upper limit stop VSET_ULS
2	LLS_FLAG	read-only	Indicates that the voltage setpoint has been programmed to a value that is less than or equal to the lower limit stop VSET_LLS
1	GPL_HI_FLAG	read-only	Indicates that the voltage setpoint has reached a value that is greater than or equal to the high general purpose limit VSET_GPL_HI
0	GPL_LO_FLAG	read-only	Indicates that the voltage setpoint has reached a value that is less than or equal to the low general purpose limit VSET_GPL_LO

0x12310 S6_CTRL_INT_RT_STS

Type: read-only
Clock: PBUS_WRCLK
Reset State: Undefined
Reset Name: PERPH_RB

Interrupt Real Time Status Bits

S6_CTRL_INT_RT_STS

Bits	Name	Type	Description
2	VREG_FAULT_INT	read-only	
1	LIMIT_ERR_INT	read-only	
0	VREG_OK_INT	read-only	

0x12311 S6_CTRL_INT_SET_TYPE

Type: read-write
Clock: PBUS_WRCLK
Reset State: 0x00
Reset Name: PERPH_RB

0 = use level trigger interrupts, 1 = use edge trigger interrupts

S6_CTRL_INT_SET_TYPE

Bits	Name	Type	Description
2	VREG_FAULT_INT	read-write	
1	LIMIT_ERR_INT	read-write	
0	VREG_OK_INT	read-write	

0x12312 S6_CTRL_INT_POLARITY_HIGH

Type: read-write
Clock: PBUS_WRCLK
Reset State: 0x00
Reset Name: PERPH_RB

1= Interrupt will trigger on a level high (rising edge) event, 0 = level high triggering is disabled

S6_CTRL_INT_POLARITY_HIGH

Bits	Name	Type	Description
2	VREG_FAULT_INT	read-write	
1	LIMIT_ERR_INT	read-write	
0	VREG_OK_INT	read-write	

0x12313 S6_CTRL_INT_POLARITY_LOW

Type: read-write
Clock: PBUS_WRCLK
Reset State: 0x00
Reset Name: PERPH_RB

1' = Interrupt will trigger on a level low (falling edge) event, '0' = level low triggering is disabled

S6_CTRL_INT_POLARITY_LOW

Bits	Name	Type	Description
2	VREG_FAULT_INT	read-write	
1	LIMIT_ERR_INT	read-write	
0	VREG_OK_INT	read-write	

0x12314 S6_CTRL_INT_LATCHED_CLR

Type: write-only
Clock: PBUS_WRCLK
Reset State: 0x00
Reset Name: PERPH_RB

Writing a '1' to this interrupt will rearm the interrupt when an interrupt is pending. It clears the internal sticky and sent bits

S6_CTRL_INT_LATCHED_CLR

Bits	Name	Type	Description
2	VREG_FAULT_INT	write-only	

S6_CTRL_INT_LATCHED_CLR (Continued)

Bits	Name	Type	Description
1	LIMIT_ERR_INT	write-only	
0	VREG_OK_INT	write-only	

0x12315 S6_CTRL_INT_EN_SET

Type: read-write
Clock: PBUS_WRCLK
Reset State: 0x00
Reset Name: PERPH_RB

Writing '0' to this register has no effect. Writing a '1' will enable the corresponding interrupt. Reading this register will readback enable status

PMIC_SET_MASK

S6_CTRL_INT_EN_SET

Bits	Name	Type	Description
2	VREG_FAULT_INT	read-write	
1	LIMIT_ERR_INT	read-write	
0	VREG_OK_INT	read-write	

0x12316 S6_CTRL_INT_EN_CLR

Type: read-write
Clock: PBUS_WRCLK
Reset State: 0x00
Reset Name: PERPH_RB

Writing '0' to this register has no effect. Writing a '1' will disable the corresponding interrupt. Reading this register will readback enable status

PMIC_CLR_MASK=INT_EN_SET

S6_CTRL_INT_EN_CLR

Bits	Name	Type	Description
2	VREG_FAULT_INT	read-write	

S6_CTRL_INT_EN_CLR (Continued)

Bits	Name	Type	Description
1	LIMIT_ERR_INT	read-write	
0	VREG_OK_INT	read-write	

0x12318 S6_CTRL_INT_LATCHED_STS

Type: read-only
Clock: PBUS_WRCLK
Reset State: 0x00
Reset Name: PERPH_RB

Debug: Latched (Sticky) Interrupt. '1' indicates that the interrupt has triggered. Once the latched bit is set it can only be cleared by writing the clear bit.

S6_CTRL_INT_LATCHED_STS

Bits	Name	Type	Description
2	VREG_FAULT_INT	read-only	
1	LIMIT_ERR_INT	read-only	
0	VREG_OK_INT	read-only	

0x12319 S6_CTRL_INT_PENDING_STS

Type: read-only
Clock: PBUS_WRCLK
Reset State: 0x00
Reset Name: PERPH_RB

Debug: Pending is set if interrupt has been sent but not cleared.

S6_CTRL_INT_PENDING_STS

Bits	Name	Type	Description
2	VREG_FAULT_INT	read-only	
1	LIMIT_ERR_INT	read-only	
0	VREG_OK_INT	read-only	

0x1231A S6_CTRL_INT_MID_SEL

Type: read-write
Clock: PBUS_WRCLK
Reset State: 0x00
Reset Name: PERPH_RB

Selects the MID that will receive the interrupt

S6_CTRL_INT_MID_SEL

Bits	Name	Type	Description
1:0	INT_MID_SEL	read-write	

0x1231B S6_CTRL_INT_PRIORITY

Type: read-write
Clock: PBUS_WRCLK
Reset State: 0x00
Reset Name: PERPH_RB

SR=0 A=1

S6_CTRL_INT_PRIORITY

Bits	Name	Type	Description
0	INT_PRIORITY	read-write	

0x12340 S6_CTRL_VOLTAGE_CTL1

Type: read-write
Clock: PBUS_WRCLK
Reset State: 0x00
Reset Name: PERPH_RB

PMIC_GANGED

S6_CTRL_VOLTAGE_CTL1

Bits	Name	Type	Description
0	MV_RANGE	read-write	0 = Use low voltage range as specified by VSET and PFM_VOFFSET 1 = Use medium voltage range as specified by VSET and PFM_VOFFSET

0x12341 S6_CTRL_VOLTAGE_CTL2

Type: read-write
Clock: PBUS_WRCLK
Reset State: 0xB4
Reset Name: PERPH_RB

PMIC_GANGED

S6_CTRL_VOLTAGE_CTL2

Bits	Name	Type	Description
7:0	VSET	read-write	Output voltage set point in PWM mode and in PFM mode if the PFM_VOFFSET_EN bit is not asserted For MV_RANGE = 0: VSET => 0.005V * m + 0.080V, where m = <7:0> For MV_RANGE = 1: VSET => 0.010V * m + 0.160V, where m = <7:0> If PFM_VOFFSET_EN is asserted and in PFM mode, add PFM_VOFFSET

0x12342 S6_CTRL_VSET_VALID

Type: read-only
Clock: PBUS_WRCLK
Reset State: Undefined
Reset Name: PERPH_RB

S6_CTRL_VSET_VALID

Bits	Name	Type	Description
7:0	VSET_VALID	read-only	Readback the valid output voltage setpoint value

0x12344 S6_CTRL_VOLTAGE_CTL3

Type: read-write
Clock: PBUS_WRCLK
Reset State: 0x00
Reset Name: PERPH_RB

S6_CTRL_VOLTAGE_CTL3

Bits	Name	Type	Description
7	PFM_VOFFSET_EN	read-write	When in PFM mode 0 = Use VSET for output voltage set point 1 = Use VSET + PFM_VOFFSET for output voltage set point
1:0	PFM_VOFFSET	read-write	When in PFM mode and PFM_VOFFSET_EN is asserted, add a positive output voltage offset For MV_RANGE = 0: VOFFSET = 0.005V * 2 * m, where m = <1:0> For MV_RANGE = 1: VOFFSET = 0.010V * 2 * m, where m = <1:0>

0x12345 S6_CTRL_MODE_CTL

Type: read-write
Clock: PBUS_WRCLK
Reset State: 0x80
Reset Name: PERPH_RB

PMIC_GANGED

S6_CTRL_MODE_CTL

Bits	Name	Type	Description
7	NPM	read-write	FTS NON-AUTO mode control 0 = Low power mode (LPM) unless AUTO_MODE is asserted 1 = Normal power mode (PWM)
6	AUTO_MODE	read-write	When asserted, FTS automatically enters and exits low power mode (PFM) based on load current qualifying triggers 0 = AUTO mode is disabled 1 = AUTO mode is enabled

0x12346 S6_CTRL_EN_CTL

Type: read-write
Clock: PBUS_WRCLK
Reset State: 0x00
Reset Name: PERPH_RB

PMIC_GANGED

S6_CTRL_EN_CTL

Bits	Name	Type	Description
7	PERPH_EN	read-write	FTS enable control 0 = Off 1 = On

0x12348 S6_CTRL_PD_CTL

Type: read-write
Clock: PBUS_WRCLK
Reset State: 0x00
Reset Name: PERPH_RB

S6_CTRL_PD_CTL

Bits	Name	Type	Description
7	PD_EN	read-write	0 = Strong pulldown is always disabled 1 = Strong pulldown is enabled when the regulator is disabled
6	WEAK_PD_EN	read-write	0 = Weak pulldown is not enabled in OFF state 1 = Weak pulldown is enabled in OFF state
5	WEAK_PD_PFM	read-write	0 = Weak pulldown is not enabled in PFM mode 1 = Weak pulldown is enabled in PFM mode
4	WEAK_PD_PWM	read-write	0 = Weak pulldown is not enabled in PWM mode (and in HCPFM mode) 1 = Weak pulldown is enabled in PWM mode (and in HCPFM mode)

0x12354 S6_CTRL_PHASE_CNT

Type: read-write
Clock: PBUS_WRCLK
Reset State: 0x00
Reset Name: PERPH_RB

PMIC_GANGED

S6_CTRL_PHASE_CNT

Bits	Name	Type	Description
1:0	PHASE_CNT	read-write	When MULTIPHASE_EN is asserted, the number of operating phases is 00 = Number of operating phases is 1 01 = Number of operating phases is 2 10 = Number of operating phases is 4 11 = Number of operating phases is 4

0x12360 S6_CTRL_SS_CTL

Type: read-write
Clock: PBUS_WRCLK
Reset State: 0x00
Reset Name: PERPH_RB

PMIC_GANGED

S6_CTRL_SS_CTL

Bits	Name	Type	Description
4:3	SS_STEP	read-write	Softstart voltage step size 00 = SS voltage step of 1 * LSB of VPROG 01 = SS voltage step of 2 * LSB 10 = SS voltage step of 4 * LSB 11 = SS voltage step of 8 * LSB
2:0	SS_DELAY	read-write	Softstart delay between steps = 2 ^ (m + 3) / Fsys, where m = <2:0> (Fsys = 19.2 MHz): 000 = 8-clock cycles (417ns) 001 = 16-clock cycles 010 = 32-clock cycles 011 = 64-clock cycles 100 = 128-clock cycles (6.67us) 101 = 256-clock cycles 110 = 512-clock cycles 111 = 1024-clock cycles (53.3us)

0x12361 S6_CTRL_VS_CTL

Type: read-write
Clock: PBUS_WRCLK
Reset State: 0x00
Reset Name: PERPH_RB

PMIC_GANGED

S6_CTRL_VS_CTL

Bits	Name	Type	Description
7	VS_EN	read-write	Voltage stepping control 0 = VS is disabled 1 = VS is enabled
4:3	VS_STEP	read-write	Voltage stepping voltage step size 00 = VS voltage step of 1 * LSB of VPROG 01 = VS voltage step of 2 * LSB 10 = VS voltage step of 4 * LSB 11 = VS voltage step of 8 * LSB
2:0	VS_DELAY	read-write	Voltage stepping delay between steps = 2 ^ (m + 3) / Fsys, where m = <2:0> (Assuming Fsys = 19.2 MHz): Desired default is 1.67us 000 = 8-clock cycles (417ns) 001 = 16-clock cycles 010 = 32-clock cycles 011 = 64-clock cycles 100 = 128-clock cycles (6.67us) 101 = 256-clock cycles 110 = 512-clock cycles 111 = 1024-clock cycles (53.3us)

0x1236A S6_CTRL_ULS_VALID

Type: read-only
Clock: PBUS_WRCLK
Reset State: Undefined
Reset Name: PERPH_RB

S6_CTRL_ULS_VALID

Bits	Name	Type	Description
7:0	ULS_VALID	read-only	Readback the valid upper limit stop value

0x1236C S6_CTRL_LLS_VALID

Type: read-only
Clock: PBUS_WRCLK
Reset State: Undefined
Reset Name: PERPH_RB

S6_CTRL_LLS_VALID

Bits	Name	Type	Description
7:0	LLS_VALID	read-only	Readback the valid lower limit stop value

8.16 S6_PS_FTS2_PS

0x12404 S6_PS_PERPH_TYPE

Type: read-only
Clock: PBUS_WRCLK
Reset State: 0x1C
Reset Name: N/A

Peripheral Type

S6_PS_PERPH_TYPE

Bits	Name	Type	Description
7:0	TYPE	read-only	FTS2 Power Stage Reset State: 0x1C

0x12405 S6_PS_PERPH_SUBTYPE

Type: read-only
Clock: PBUS_WRCLK
Reset State: 0x08
Reset Name: N/A

Peripheral SubType

S6_PS_PERPH_SUBTYPE

Bits	Name	Type	Description
7:0	SUBTYPE	read-only	

0x12440 S6_PS_VOLTAGE_CTL1

Type: read-write
Clock: PBUS_WRCLK
Reset State: 0x00
Reset Name: PERPH_RB

PMIC_GANGED

S6_PS_VOLTAGE_CTL1

Bits	Name	Type	Description
0	MV_RANGE	read-write	0 = Use low voltage range as specified by VSET and PFM_VOFFSET 1 = Use medium voltage range as specified by VSET and PFM_VOFFSET

0x12441 S6_PS_VOLTAGE_CTL2

Type: read-write
Clock: PBUS_WRCLK
Reset State: 0xB4
Reset Name: PERPH_RB

PMIC_GANGED

S6_PS_VOLTAGE_CTL2

Bits	Name	Type	Description
7:0	VSET	read-write	Output voltage set point in PWM mode and in PFM mode if the PFM_VOFFSET_EN bit is not asserted For MV_RANGE = 0: VSET => 0.005V * m + 0.080V, where m = <7:0> For MV_RANGE = 1: VSET => 0.010V * m + 0.160V, where m = <7:0> If PFM_VOFFSET_EN is asserted and in PFM mode, add PFM_VOFFSET

0x12454 S6_PS_PHASE_CNT

Type: read-write
Clock: PBUS_WRCLK
Reset State: 0x00
Reset Name: PERPH_RB

PMIC_GANGED, PMIC_SYNC=clk_19p2:phase_cnt_rb

S6_PS_PHASE_CNT

Bits	Name	Type	Description
1:0	PHASE_CNT	read-write	When MULTIPHASE_EN is asserted, the number of operating phases is 00 = Number of operating phases is 1 01 = Number of operating phases is 2 10 = Number of operating phases is 4 11 = Number of operating phases is 4

8.17 S6_FREQ_BCLK_GEN_CLK

0x12504 S6_FREQ_PERPH_TYPE

Type: read-only
Clock: PBUS_WRCLK
Reset State: 0x1D
Reset Name: N/A

Peripheral Type

S6_FREQ_PERPH_TYPE

Bits	Name	Type	Description
7:0	TYPE	read-only	BCLK GEN

0x12505 S6_FREQ_PERPH_SUBTYPE

Type: read-only
Clock: PBUS_WRCLK
Reset State: 0x09
Reset Name: N/A

Peripheral SubType

S6_FREQ_PERPH_SUBTYPE

Bits	Name	Type	Description
7:0	SUBTYPE	read-only	BCLK GEN CLK

0x12546 S6_FREQ_CLK_ENABLE

Type: read-write
Clock: PBUS_WRCLK
Reset State: 0x01
Reset Name: PERPH_RB

S6_FREQ_CLK_ENABLE

Bits	Name	Type	Description
7	EN_CLK_INT	read-write	0 = do not force the clock on 1 = enable the clock
0	FOLLOW_CLK_SX_REQ	read-write	0 = ignore smps_clk_req<X> 1 = clock is enabled when the clocks request is high smps_clk_req<X>='1'

0x12550 S6_FREQ_CLK_DIV

Type: read-write
Clock: PBUS_WRCLK
Reset State: 0x02
Reset Name: PERPH_RB

PMIC_GANGED

S6_FREQ_CLK_DIV

Bits	Name	Type	Description
3:0	CLK_DIV	read-write	clock_ frequency = 19.2MHz / (CLK_DIV + 1) FTS2 Buck supports 3.2, 4.8, 6.4 and 9.6 MHz HF2 Buck supports 1.6, 2.4, 2.74, 3.2, 3.8, 4.8, and 6.4 MHz CLK_DIV = 0 is not supported, it will generate 9.6 MHz

0x12551 S6_FREQ_CLK_PHASE

Type: read-write
Clock: PBUS_WRCLK
Reset State: 0x04
Reset Name: PERPH_RB

S6_FREQ_CLK_PHASE

Bits	Name	Type	Description
3:0	CLK_PHASE	read-write	Distributed clock phase select: clock phase delay = clock period * (CLK_PHASE / 16)

0x125C0 S6_FREQ_GANG_CTL1

Type: read-write
Clock: PBUS_WRCLK
Reset State: 0x20
Reset Name: PERPH_RB

S6_FREQ_GANG_CTL1

Bits	Name	Type	Description
7:0	GANG_LEADER_PID	read-write	When GANG_EN (GANG_CTL2[7]) is set, this peripheral will write the same data that is written to the gang leader Peripheral ID. Reads to the gang leader Peripheral ID are ignored by this peripheral. Ganged peripherals must reside within the same Slave ID

0x125C1 S6_FREQ_GANG_CTL2

Type: read-write
Clock: PBUS_WRCLK
Reset State: 0x80
Reset Name: PERPH_RB

S6_FREQ_GANG_CTL2

Bits	Name	Type	Description
7	GANG_EN	read-write	0 = disable 1 = enable When enabled, this peripheral will write the same data that is written to the gang leader PID. Reads to the gang leader PID are ignored by this peripheral

8.18 S7_CTRL_FTS2_CTRL

0x12604 S7_CTRL_PERPH_TYPE

Type: read-only
Clock: PBUS_WRCLK
Reset State: 0x03
Reset Name: N/A

Peripheral Type

S7_CTRL_PERPH_TYPE

Bits	Name	Type	Description
7:0	TYPE	read-only	FTS2 Control Reset State: 0x03

0x12605 S7_CTRL_PERPH_SUBTYPE

Type: read-only
Clock: PBUS_WRCLK
Reset State: 0x08
Reset Name: N/A

Peripheral SubType

S7_CTRL_PERPH_SUBTYPE

Bits	Name	Type	Description
7:0	SUBTYPE	read-only	

0x12608 S7_CTRL_STATUS_1

Type: read-only
Clock: PBUS_WRCLK
Reset State: Undefined
Reset Name: N/A

Status Registers

S7_CTRL_STATUS_1

Bits	Name	Type	Description
7	VREG_OK_FLAG	read-only	Indicates that VREG_SNS has reached a value that is greater than or equal to the threshold of the comparator tasked for VREG_SNS monitoring

S7_CTRL_STATUS_1 (Continued)

Bits	Name	Type	Description
6	VREG_FAULT_FLAG	read-only	Indicates a probable short circuit condition at VREG_SNS since VREG_SNS is below the VREG fault voltage level and the softstart ramp is done. Current limit foldback is in use.
1	NPM_FLAG	read-only	Indicates normal power mode is in use
0	STEPPER_DONE_FLAG	read-only	Softstart stepper and voltage stepper done

0x12609 S7_CTRL_STATUS_2

Type: read-only
Clock: PBUS_WRCLK
Reset State: Undefined
Reset Name: N/A

Status Registers

S7_CTRL_STATUS_2

Bits	Name	Type	Description
4	ILS_FLAG	read-only	Either of the following: => Both limit stops have been enabled, but the upper limit stop VSET_ULS has been programmed to a value below the lower limit stop VSET_LLS => Both limit stops have been enabled, but the lower limit stop VSET_LLS has been programmed to a value above the upper limit stop VSET_ULS
3	ULS_FLAG	read-only	Indicates that the voltage setpoint has been programmed to a value that is greater than or equal to the upper limit stop VSET_ULS
2	LLS_FLAG	read-only	Indicates that the voltage setpoint has been programmed to a value that is less than or equal to the lower limit stop VSET_LLS
1	GPL_HI_FLAG	read-only	Indicates that the voltage setpoint has reached a value that is greater than or equal to the high general purpose limit VSET_GPL_HI
0	GPL_LO_FLAG	read-only	Indicates that the voltage setpoint has reached a value that is less than or equal to the low general purpose limit VSET_GPL_LO

0x12610 S7_CTRL_INT_RT_STS

Type: read-only
Clock: PBUS_WRCLK
Reset State: Undefined
Reset Name: PERPH_RB

Interrupt Real Time Status Bits

S7_CTRL_INT_RT_STS

Bits	Name	Type	Description
2	VREG_FAULT_INT	read-only	
1	LIMIT_ERR_INT	read-only	
0	VREG_OK_INT	read-only	

0x12611 S7_CTRL_INT_SET_TYPE

Type: read-write
Clock: PBUS_WRCLK
Reset State: 0x00
Reset Name: PERPH_RB

0 = use level trigger interrupts, 1 = use edge trigger interrupts

S7_CTRL_INT_SET_TYPE

Bits	Name	Type	Description
2	VREG_FAULT_INT	read-write	
1	LIMIT_ERR_INT	read-write	
0	VREG_OK_INT	read-write	

0x12612 S7_CTRL_INT_POLARITY_HIGH

Type: read-write
Clock: PBUS_WRCLK
Reset State: 0x00
Reset Name: PERPH_RB

1= Interrupt will trigger on a level high (rising edge) event, 0 = level high triggering is disabled

S7_CTRL_INT_POLARITY_HIGH

Bits	Name	Type	Description
2	VREG_FAULT_INT	read-write	
1	LIMIT_ERR_INT	read-write	
0	VREG_OK_INT	read-write	

0x12613 S7_CTRL_INT_POLARITY_LOW

Type: read-write
Clock: PBUS_WRCLK
Reset State: 0x00
Reset Name: PERPH_RB

1' = Interrupt will trigger on a level low (falling edge) event, '0' = level low triggering is disabled

S7_CTRL_INT_POLARITY_LOW

Bits	Name	Type	Description
2	VREG_FAULT_INT	read-write	
1	LIMIT_ERR_INT	read-write	
0	VREG_OK_INT	read-write	

0x12614 S7_CTRL_INT_LATCHED_CLR

Type: write-only
Clock: PBUS_WRCLK
Reset State: 0x00
Reset Name: PERPH_RB

Writing a '1' to this interrupt will rearm the interrupt when an interrupt is pending. It clears the internal sticky and sent bits

S7_CTRL_INT_LATCHED_CLR

Bits	Name	Type	Description
2	VREG_FAULT_INT	write-only	

S7_CTRL_INT_LATCHED_CLR (Continued)

Bits	Name	Type	Description
1	LIMIT_ERR_INT	write-only	
0	VREG_OK_INT	write-only	

0x12615 S7_CTRL_INT_EN_SET

Type: read-write
Clock: PBUS_WRCLK
Reset State: 0x00
Reset Name: PERPH_RB

Writing '0' to this register has no effect. Writing a '1' will enable the corresponding interrupt. Reading this register will readback enable status

PMIC_SET_MASK

S7_CTRL_INT_EN_SET

Bits	Name	Type	Description
2	VREG_FAULT_INT	read-write	
1	LIMIT_ERR_INT	read-write	
0	VREG_OK_INT	read-write	

0x12616 S7_CTRL_INT_EN_CLR

Type: read-write
Clock: PBUS_WRCLK
Reset State: 0x00
Reset Name: PERPH_RB

Writing '0' to this register has no effect. Writing a '1' will disable the corresponding interrupt. Reading this register will readback enable status

PMIC_CLR_MASK=INT_EN_SET

S7_CTRL_INT_EN_CLR

Bits	Name	Type	Description
2	VREG_FAULT_INT	read-write	

S7_CTRL_INT_EN_CLR (Continued)

Bits	Name	Type	Description
1	LIMIT_ERR_INT	read-write	
0	VREG_OK_INT	read-write	

0x12618 S7_CTRL_INT_LATCHED_STS

Type: read-only
Clock: PBUS_WRCLK
Reset State: 0x00
Reset Name: PERPH_RB

Debug: Latched (Sticky) Interrupt. '1' indicates that the interrupt has triggered. Once the latched bit is set it can only be cleared by writing the clear bit.

S7_CTRL_INT_LATCHED_STS

Bits	Name	Type	Description
2	VREG_FAULT_INT	read-only	
1	LIMIT_ERR_INT	read-only	
0	VREG_OK_INT	read-only	

0x12619 S7_CTRL_INT_PENDING_STS

Type: read-only
Clock: PBUS_WRCLK
Reset State: 0x00
Reset Name: PERPH_RB

Debug: Pending is set if interrupt has been sent but not cleared.

S7_CTRL_INT_PENDING_STS

Bits	Name	Type	Description
2	VREG_FAULT_INT	read-only	
1	LIMIT_ERR_INT	read-only	
0	VREG_OK_INT	read-only	

0x1261A S7_CTRL_INT_MID_SEL

Type: read-write
Clock: PBUS_WRCLK
Reset State: 0x00
Reset Name: PERPH_RB

Selects the MID that will receive the interrupt

S7_CTRL_INT_MID_SEL

Bits	Name	Type	Description
1:0	INT_MID_SEL	read-write	

0x1261B S7_CTRL_INT_PRIORITY

Type: read-write
Clock: PBUS_WRCLK
Reset State: 0x00
Reset Name: PERPH_RB

SR=0 A=1

S7_CTRL_INT_PRIORITY

Bits	Name	Type	Description
0	INT_PRIORITY	read-write	

0x12640 S7_CTRL_VOLTAGE_CTL1

Type: read-write
Clock: PBUS_WRCLK
Reset State: 0x00
Reset Name: PERPH_RB

PMIC_GANGED

S7_CTRL_VOLTAGE_CTL1

Bits	Name	Type	Description
0	MV_RANGE	read-write	0 = Use low voltage range as specified by VSET and PFM_VOFFSET 1 = Use medium voltage range as specified by VSET and PFM_VOFFSET

0x12641 S7_CTRL_VOLTAGE_CTL2

Type: read-write
Clock: PBUS_WRCLK
Reset State: 0xB4
Reset Name: PERPH_RB

PMIC_GANGED

S7_CTRL_VOLTAGE_CTL2

Bits	Name	Type	Description
7:0	VSET	read-write	Output voltage set point in PWM mode and in PFM mode if the PFM_VOFFSET_EN bit is not asserted For MV_RANGE = 0: VSET => 0.005V * m + 0.080V, where m = <7:0> For MV_RANGE = 1: VSET => 0.010V * m + 0.160V, where m = <7:0> If PFM_VOFFSET_EN is asserted and in PFM mode, add PFM_VOFFSET

0x12642 S7_CTRL_VSET_VALID

Type: read-only
Clock: PBUS_WRCLK
Reset State: Undefined
Reset Name: PERPH_RB

S7_CTRL_VSET_VALID

Bits	Name	Type	Description
7:0	VSET_VALID	read-only	Readback the valid output voltage setpoint value

0x12644 S7_CTRL_VOLTAGE_CTL3

Type: read-write
Clock: PBUS_WRCLK
Reset State: 0x00
Reset Name: PERPH_RB

S7_CTRL_VOLTAGE_CTL3

Bits	Name	Type	Description
7	PFM_VOFFSET_EN	read-write	When in PFM mode 0 = Use VSET for output voltage set point 1 = Use VSET + PFM_VOFFSET for output voltage set point
1:0	PFM_VOFFSET	read-write	When in PFM mode and PFM_VOFFSET_EN is asserted, add a positive output voltage offset For MV_RANGE = 0: VOFFSET = 0.005V * 2 * m, where m = <1:0> For MV_RANGE = 1: VOFFSET = 0.010V * 2 * m, where m = <1:0>

0x12645 S7_CTRL_MODE_CTL

Type: read-write
Clock: PBUS_WRCLK
Reset State: 0x80
Reset Name: PERPH_RB

PMIC_GANGED

S7_CTRL_MODE_CTL

Bits	Name	Type	Description
7	NPM	read-write	FTS NON-AUTO mode control 0 = Low power mode (LPM) unless AUTO_MODE is asserted 1 = Normal power mode (PWM)
6	AUTO_MODE	read-write	When asserted, FTS automatically enters and exits low power mode (PFM) based on load current qualifying triggers 0 = AUTO mode is disabled 1 = AUTO mode is enabled

0x12646 S7_CTRL_EN_CTL

Type: read-write
Clock: PBUS_WRCLK
Reset State: 0x00
Reset Name: PERPH_RB

PMIC_GANGED

S7_CTRL_EN_CTL

Bits	Name	Type	Description
7	PERPH_EN	read-write	FTS enable control 0 = Off 1 = On

0x12648 S7_CTRL_PD_CTL

Type: read-write
Clock: PBUS_WRCLK
Reset State: 0x00
Reset Name: PERPH_RB

S7_CTRL_PD_CTL

Bits	Name	Type	Description
7	PD_EN	read-write	0 = Strong pulldown is always disabled 1 = Strong pulldown is enabled when the regulator is disabled
6	WEAK_PD_EN	read-write	0 = Weak pulldown is not enabled in OFF state 1 = Weak pulldown is enabled in OFF state
5	WEAK_PD_PFM	read-write	0 = Weak pulldown is not enabled in PFM mode 1 = Weak pulldown is enabled in PFM mode
4	WEAK_PD_PWM	read-write	0 = Weak pulldown is not enabled in PWM mode (and in HCPFM mode) 1 = Weak pulldown is enabled in PWM mode (and in HCPFM mode)

0x12654 S7_CTRL_PHASE_CNT

Type: read-write
Clock: PBUS_WRCLK
Reset State: 0x00
Reset Name: PERPH_RB

PMIC_GANGED

S7_CTRL_PHASE_CNT

Bits	Name	Type	Description
1:0	PHASE_CNT	read-write	When MULTIPHASE_EN is asserted, the number of operating phases is 00 = Number of operating phases is 1 01 = Number of operating phases is 2 10 = Number of operating phases is 4 11 = Number of operating phases is 4

0x12660 S7_CTRL_SS_CTL

Type: read-write
Clock: PBUS_WRCLK
Reset State: 0x00
Reset Name: PERPH_RB

PMIC_GANGED

S7_CTRL_SS_CTL

Bits	Name	Type	Description
4:3	SS_STEP	read-write	Softstart voltage step size 00 = SS voltage step of 1 * LSB of VPROG 01 = SS voltage step of 2 * LSB 10 = SS voltage step of 4 * LSB 11 = SS voltage step of 8 * LSB
2:0	SS_DELAY	read-write	Softstart delay between steps = 2 ^ (m + 3) / Fsys, where m = <2:0> (Fsys = 19.2 MHz): 000 = 8-clock cycles (417ns) 001 = 16-clock cycles 010 = 32-clock cycles 011 = 64-clock cycles 100 = 128-clock cycles (6.67us) 101 = 256-clock cycles 110 = 512-clock cycles 111 = 1024-clock cycles (53.3us)

0x12661 S7_CTRL_VS_CTL

Type: read-write
Clock: PBUS_WRCLK
Reset State: 0x00
Reset Name: PERPH_RB

PMIC_GANGED

S7_CTRL_VS_CTL

Bits	Name	Type	Description
7	VS_EN	read-write	Voltage stepping control 0 = VS is disabled 1 = VS is enabled
4:3	VS_STEP	read-write	Voltage stepping voltage step size 00 = VS voltage step of 1 * LSB of VPROG 01 = VS voltage step of 2 * LSB 10 = VS voltage step of 4 * LSB 11 = VS voltage step of 8 * LSB
2:0	VS_DELAY	read-write	Voltage stepping delay between steps = 2 ^ (m + 3) / Fsys, where m = <2:0> (Assuming Fsys = 19.2 MHz): Desired default is 1.67us 000 = 8-clock cycles (417ns) 001 = 16-clock cycles 010 = 32-clock cycles 011 = 64-clock cycles 100 = 128-clock cycles (6.67us) 101 = 256-clock cycles 110 = 512-clock cycles 111 = 1024-clock cycles (53.3us)

0x1266A S7_CTRL_ULS_VALID

Type: read-only
Clock: PBUS_WRCLK
Reset State: Undefined
Reset Name: PERPH_RB

S7_CTRL_ULS_VALID

Bits	Name	Type	Description
7:0	ULS_VALID	read-only	Readback the valid upper limit stop value

0x1266C S7_CTRL_LLS_VALID

Type: read-only
Clock: PBUS_WRCLK
Reset State: Undefined
Reset Name: PERPH_RB

S7_CTRL_LLS_VALID

Bits	Name	Type	Description
7:0	LLS_VALID	read-only	Readback the valid lower limit stop value

8.19 S7_PS_FTS2_PS

0x12704 S7_PS_PERPH_TYPE

Type: read-only
Clock: PBUS_WRCLK
Reset State: 0x1C
Reset Name: N/A

Peripheral Type

S7_PS_PERPH_TYPE

Bits	Name	Type	Description
7:0	TYPE	read-only	FTS2 Power Stage Reset State: 0x1C

0x12705 S7_PS_PERPH_SUBTYPE

Type: read-only
Clock: PBUS_WRCLK
Reset State: 0x08
Reset Name: N/A

Peripheral SubType

S7_PS_PERPH_SUBTYPE

Bits	Name	Type	Description
7:0	SUBTYPE	read-only	

0x12740 S7_PS_VOLTAGE_CTL1

Type: read-write
Clock: PBUS_WRCLK
Reset State: 0x00
Reset Name: PERPH_RB

PMIC_GANGED

S7_PS_VOLTAGE_CTL1

Bits	Name	Type	Description
0	MV_RANGE	read-write	0 = Use low voltage range as specified by VSET and PFM_VOFFSET 1 = Use medium voltage range as specified by VSET and PFM_VOFFSET

0x12741 S7_PS_VOLTAGE_CTL2

Type: read-write
Clock: PBUS_WRCLK
Reset State: 0xB4
Reset Name: PERPH_RB

PMIC_GANGED

S7_PS_VOLTAGE_CTL2

Bits	Name	Type	Description
7:0	VSET	read-write	Output voltage set point in PWM mode and in PFM mode if the PFM_VOFFSET_EN bit is not asserted For MV_RANGE = 0: VSET => 0.005V * m + 0.080V, where m = <7:0> For MV_RANGE = 1: VSET => 0.010V * m + 0.160V, where m = <7:0> If PFM_VOFFSET_EN is asserted and in PFM mode, add PFM_VOFFSET

0x12754 S7_PS_PHASE_CNT

Type: read-write
Clock: PBUS_WRCLK
Reset State: 0x00
Reset Name: PERPH_RB

PMIC_GANGED, PMIC_SYNC=clk_19p2:phase_cnt_rb

S7_PS_PHASE_CNT

Bits	Name	Type	Description
1:0	PHASE_CNT	read-write	When MULTIPHASE_EN is asserted, the number of operating phases is 00 = Number of operating phases is 1 01 = Number of operating phases is 2 10 = Number of operating phases is 4 11 = Number of operating phases is 4

8.20 S7_FREQ_BCLK_GEN_CLK

0x12804 S7_FREQ_PERPH_TYPE

Type: read-only
Clock: PBUS_WRCLK
Reset State: 0x1D
Reset Name: N/A

Peripheral Type

S7_FREQ_PERPH_TYPE

Bits	Name	Type	Description
7:0	TYPE	read-only	BCLK GEN

0x12805 S7_FREQ_PERPH_SUBTYPE

Type: read-only
Clock: PBUS_WRCLK
Reset State: 0x09
Reset Name: N/A

Peripheral SubType

S7_FREQ_PERPH_SUBTYPE

Bits	Name	Type	Description
7:0	SUBTYPE	read-only	BCLK GEN CLK

0x12846 S7_FREQ_CLK_ENABLE

Type: read-write
Clock: PBUS_WRCLK
Reset State: 0x01
Reset Name: PERPH_RB

S7_FREQ_CLK_ENABLE

Bits	Name	Type	Description
7	EN_CLK_INT	read-write	0 = do not force the clock on 1 = enable the clock
0	FOLLOW_CLK_SX_REQ	read-write	0 = ignore smps_clk_req<X> 1 = clock is enabled when the clocks request is high smps_clk_req<X>='1'

0x12850 S7_FREQ_CLK_DIV

Type: read-write
Clock: PBUS_WRCLK
Reset State: 0x02
Reset Name: PERPH_RB

PMIC_GANGED

S7_FREQ_CLK_DIV

Bits	Name	Type	Description
3:0	CLK_DIV	read-write	clock_ frequency = 19.2MHz / (CLK_DIV + 1) FTS2 Buck supports 3.2, 4.8, 6.4 and 9.6 MHz HF2 Buck supports 1.6, 2.4, 2.74, 3.2, 3.8, 4.8, and 6.4 MHz CLK_DIV = 0 is not supported, it will generate 9.6 MHz

0x12851 S7_FREQ_CLK_PHASE

Type: read-write
Clock: PBUS_WRCLK
Reset State: 0x08
Reset Name: PERPH_RB

S7_FREQ_CLK_PHASE

Bits	Name	Type	Description
3:0	CLK_PHASE	read-write	Distributed clock phase select: clock phase delay = clock period * (CLK_PHASE / 16)

0x128C0 S7_FREQ_GANG_CTL1

Type: read-write
Clock: PBUS_WRCLK
Reset State: 0x20
Reset Name: PERPH_RB

S7_FREQ_GANG_CTL1

Bits	Name	Type	Description
7:0	GANG_LEADER_PID	read-write	When GANG_EN (GANG_CTL2[7]) is set, this peripheral will write the same data that is written to the gang leader Peripheral ID. Reads to the gang leader Peripheral ID are ignored by this peripheral. Ganged peripherals must reside within the same Slave ID

0x128C1 S7_FREQ_GANG_CTL2

Type: read-write
Clock: PBUS_WRCLK
Reset State: 0x80
Reset Name: PERPH_RB

S7_FREQ_GANG_CTL2

Bits	Name	Type	Description
7	GANG_EN	read-write	0 = disable 1 = enable When enabled, this peripheral will write the same data that is written to the gang leader PID. Reads to the gang leader PID are ignored by this peripheral

8.21 S8_CTRL_FTS2_CTRL

0x12904 S8_CTRL_PERPH_TYPE

Type: read-only
Clock: PBUS_WRCLK
Reset State: 0x03
Reset Name: N/A

Peripheral Type

S8_CTRL_PERPH_TYPE

Bits	Name	Type	Description
7:0	TYPE	read-only	FTS2 Control Reset State: 0x03

0x12905 S8_CTRL_PERPH_SUBTYPE

Type: read-only
Clock: PBUS_WRCLK
Reset State: 0x08
Reset Name: N/A

Peripheral SubType

S8_CTRL_PERPH_SUBTYPE

Bits	Name	Type	Description
7:0	SUBTYPE	read-only	

0x12908 S8_CTRL_STATUS_1

Type: read-only
Clock: PBUS_WRCLK
Reset State: Undefined
Reset Name: N/A

Status Registers

S8_CTRL_STATUS_1

Bits	Name	Type	Description
7	VREG_OK_FLAG	read-only	Indicates that VREG_SNS has reached a value that is greater than or equal to the threshold of the comparator tasked for VREG_SNS monitoring

S8_CTRL_STATUS_1 (Continued)

Bits	Name	Type	Description
6	VREG_FAULT_FLAG	read-only	Indicates a probable short circuit condition at VREG_SNS since VREG_SNS is below the VREG fault voltage level and the softstart ramp is done. Current limit foldback is in use.
1	NPM_FLAG	read-only	Indicates normal power mode is in use
0	STEPPER_DONE_FLAG	read-only	Softstart stepper and voltage stepper done

0x12909 S8_CTRL_STATUS_2

Type: read-only
Clock: PBUS_WRCLK
Reset State: Undefined
Reset Name: N/A

Status Registers

S8_CTRL_STATUS_2

Bits	Name	Type	Description
4	ILS_FLAG	read-only	Either of the following: => Both limit stops have been enabled, but the upper limit stop VSET_ULS has been programmed to a value below the lower limit stop VSET_LLS => Both limit stops have been enabled, but the lower limit stop VSET_LLS has been programmed to a value above the upper limit stop VSET_ULS
3	ULS_FLAG	read-only	Indicates that the voltage setpoint has been programmed to a value that is greater than or equal to the upper limit stop VSET_ULS
2	LLS_FLAG	read-only	Indicates that the voltage setpoint has been programmed to a value that is less than or equal to the lower limit stop VSET_LLS
1	GPL_HI_FLAG	read-only	Indicates that the voltage setpoint has reached a value that is greater than or equal to the high general purpose limit VSET_GPL_HI
0	GPL_LO_FLAG	read-only	Indicates that the voltage setpoint has reached a value that is less than or equal to the low general purpose limit VSET_GPL_LO

0x12910 S8_CTRL_INT_RT_STS

Type: read-only
Clock: PBUS_WRCLK
Reset State: Undefined
Reset Name: PERPH_RB

Interrupt Real Time Status Bits

S8_CTRL_INT_RT_STS

Bits	Name	Type	Description
2	VREG_FAULT_INT	read-only	
1	LIMIT_ERR_INT	read-only	
0	VREG_OK_INT	read-only	

0x12911 S8_CTRL_INT_SET_TYPE

Type: read-write
Clock: PBUS_WRCLK
Reset State: 0x00
Reset Name: PERPH_RB

0 = use level trigger interrupts, 1 = use edge trigger interrupts

S8_CTRL_INT_SET_TYPE

Bits	Name	Type	Description
2	VREG_FAULT_INT	read-write	
1	LIMIT_ERR_INT	read-write	
0	VREG_OK_INT	read-write	

0x12912 S8_CTRL_INT_POLARITY_HIGH

Type: read-write
Clock: PBUS_WRCLK
Reset State: 0x00
Reset Name: PERPH_RB

1= Interrupt will trigger on a level high (rising edge) event, 0 = level high triggering is disabled

S8_CTRL_INT_POLARITY_HIGH

Bits	Name	Type	Description
2	VREG_FAULT_INT	read-write	
1	LIMIT_ERR_INT	read-write	
0	VREG_OK_INT	read-write	

0x12913 S8_CTRL_INT_POLARITY_LOW

Type: read-write
Clock: PBUS_WRCLK
Reset State: 0x00
Reset Name: PERPH_RB

1' = Interrupt will trigger on a level low (falling edge) event, '0' = level low triggering is disabled

S8_CTRL_INT_POLARITY_LOW

Bits	Name	Type	Description
2	VREG_FAULT_INT	read-write	
1	LIMIT_ERR_INT	read-write	
0	VREG_OK_INT	read-write	

0x12914 S8_CTRL_INT_LATCHED_CLR

Type: write-only
Clock: PBUS_WRCLK
Reset State: 0x00
Reset Name: PERPH_RB

Writing a '1' to this interrupt will rearm the interrupt when an interrupt is pending. It clears the internal sticky and sent bits

S8_CTRL_INT_LATCHED_CLR

Bits	Name	Type	Description
2	VREG_FAULT_INT	write-only	

S8_CTRL_INT_LATCHED_CLR (Continued)

Bits	Name	Type	Description
1	LIMIT_ERR_INT	write-only	
0	VREG_OK_INT	write-only	

0x12915 S8_CTRL_INT_EN_SET

Type: read-write
Clock: PBUS_WRCLK
Reset State: 0x00
Reset Name: PERPH_RB

Writing '0' to this register has no effect. Writing a '1' will enable the corresponding interrupt. Reading this register will readback enable status

PMIC_SET_MASK

S8_CTRL_INT_EN_SET

Bits	Name	Type	Description
2	VREG_FAULT_INT	read-write	
1	LIMIT_ERR_INT	read-write	
0	VREG_OK_INT	read-write	

0x12916 S8_CTRL_INT_EN_CLR

Type: read-write
Clock: PBUS_WRCLK
Reset State: 0x00
Reset Name: PERPH_RB

Writing '0' to this register has no effect. Writing a '1' will disable the corresponding interrupt. Reading this register will readback enable status

PMIC_CLR_MASK=INT_EN_SET

S8_CTRL_INT_EN_CLR

Bits	Name	Type	Description
2	VREG_FAULT_INT	read-write	

S8_CTRL_INT_EN_CLR (Continued)

Bits	Name	Type	Description
1	LIMIT_ERR_INT	read-write	
0	VREG_OK_INT	read-write	

0x12918 S8_CTRL_INT_LATCHED_STS

Type: read-only
Clock: PBUS_WRCLK
Reset State: 0x00
Reset Name: PERPH_RB

Debug: Latched (Sticky) Interrupt. '1' indicates that the interrupt has triggered. Once the latched bit is set it can only be cleared by writing the clear bit.

S8_CTRL_INT_LATCHED_STS

Bits	Name	Type	Description
2	VREG_FAULT_INT	read-only	
1	LIMIT_ERR_INT	read-only	
0	VREG_OK_INT	read-only	

0x12919 S8_CTRL_INT_PENDING_STS

Type: read-only
Clock: PBUS_WRCLK
Reset State: 0x00
Reset Name: PERPH_RB

Debug: Pending is set if interrupt has been sent but not cleared.

S8_CTRL_INT_PENDING_STS

Bits	Name	Type	Description
2	VREG_FAULT_INT	read-only	
1	LIMIT_ERR_INT	read-only	
0	VREG_OK_INT	read-only	

0x1291A S8_CTRL_INT_MID_SEL

Type: read-write
Clock: PBUS_WRCLK
Reset State: 0x00
Reset Name: PERPH_RB

Selects the MID that will receive the interrupt

S8_CTRL_INT_MID_SEL

Bits	Name	Type	Description
1:0	INT_MID_SEL	read-write	

0x1291B S8_CTRL_INT_PRIORITY

Type: read-write
Clock: PBUS_WRCLK
Reset State: 0x00
Reset Name: PERPH_RB

SR=0 A=1

S8_CTRL_INT_PRIORITY

Bits	Name	Type	Description
0	INT_PRIORITY	read-write	

0x12940 S8_CTRL_VOLTAGE_CTL1

Type: read-write
Clock: PBUS_WRCLK
Reset State: 0x00
Reset Name: PERPH_RB

PMIC_GANGED

S8_CTRL_VOLTAGE_CTL1

Bits	Name	Type	Description
0	MV_RANGE	read-write	0 = Use low voltage range as specified by VSET and PFM_VOFFSET 1 = Use medium voltage range as specified by VSET and PFM_VOFFSET

0x12941 S8_CTRL_VOLTAGE_CTL2

Type: read-write
Clock: PBUS_WRCLK
Reset State: 0xB4
Reset Name: PERPH_RB

PMIC_GANGED

S8_CTRL_VOLTAGE_CTL2

Bits	Name	Type	Description
7:0	VSET	read-write	Output voltage set point in PWM mode and in PFM mode if the PFM_VOFFSET_EN bit is not asserted For MV_RANGE = 0: VSET => 0.005V * m + 0.080V, where m = <7:0> For MV_RANGE = 1: VSET => 0.010V * m + 0.160V, where m = <7:0> If PFM_VOFFSET_EN is asserted and in PFM mode, add PFM_VOFFSET

0x12942 S8_CTRL_VSET_VALID

Type: read-only
Clock: PBUS_WRCLK
Reset State: Undefined
Reset Name: PERPH_RB

S8_CTRL_VSET_VALID

Bits	Name	Type	Description
7:0	VSET_VALID	read-only	Readback the valid output voltage setpoint value

0x12944 S8_CTRL_VOLTAGE_CTL3

Type: read-write
Clock: PBUS_WRCLK
Reset State: 0x00
Reset Name: PERPH_RB

S8_CTRL_VOLTAGE_CTL3

Bits	Name	Type	Description
7	PFM_VOFFSET_EN	read-write	When in PFM mode 0 = Use VSET for output voltage set point 1 = Use VSET + PFM_VOFFSET for output voltage set point
1:0	PFM_VOFFSET	read-write	When in PFM mode and PFM_VOFFSET_EN is asserted, add a positive output voltage offset For MV_RANGE = 0: VOFFSET = 0.005V * 2 * m, where m = <1:0> For MV_RANGE = 1: VOFFSET = 0.010V * 2 * m, where m = <1:0>

0x12945 S8_CTRL_MODE_CTL

Type: read-write
Clock: PBUS_WRCLK
Reset State: 0x80
Reset Name: PERPH_RB

PMIC_GANGED

S8_CTRL_MODE_CTL

Bits	Name	Type	Description
7	NPM	read-write	FTS NON-AUTO mode control 0 = Low power mode (LPM) unless AUTO_MODE is asserted 1 = Normal power mode (PWM)
6	AUTO_MODE	read-write	When asserted, FTS automatically enters and exits low power mode (PFM) based on load current qualifying triggers 0 = AUTO mode is disabled 1 = AUTO mode is enabled

0x12946 S8_CTRL_EN_CTL

Type: read-write
Clock: PBUS_WRCLK
Reset State: 0x00
Reset Name: PERPH_RB

PMIC_GANGED

S8_CTRL_EN_CTL

Bits	Name	Type	Description
7	PERPH_EN	read-write	FTS enable control 0 = Off 1 = On

0x12948 S8_CTRL_PD_CTL

Type: read-write
Clock: PBUS_WRCLK
Reset State: 0x00
Reset Name: PERPH_RB

S8_CTRL_PD_CTL

Bits	Name	Type	Description
7	PD_EN	read-write	0 = Strong pulldown is always disabled 1 = Strong pulldown is enabled when the regulator is disabled
6	WEAK_PD_EN	read-write	0 = Weak pulldown is not enabled in OFF state 1 = Weak pulldown is enabled in OFF state
5	WEAK_PD_PFM	read-write	0 = Weak pulldown is not enabled in PFM mode 1 = Weak pulldown is enabled in PFM mode
4	WEAK_PD_PWM	read-write	0 = Weak pulldown is not enabled in PWM mode (and in HCPFM mode) 1 = Weak pulldown is enabled in PWM mode (and in HCPFM mode)

0x12954 S8_CTRL_PHASE_CNT

Type: read-write
Clock: PBUS_WRCLK
Reset State: 0x00
Reset Name: PERPH_RB

PMIC_GANGED

S8_CTRL_PHASE_CNT

Bits	Name	Type	Description
1:0	PHASE_CNT	read-write	When MULTIPHASE_EN is asserted, the number of operating phases is 00 = Number of operating phases is 1 01 = Number of operating phases is 2 10 = Number of operating phases is 4 11 = Number of operating phases is 4

0x12960 S8_CTRL_SS_CTL

Type: read-write
Clock: PBUS_WRCLK
Reset State: 0x00
Reset Name: PERPH_RB

PMIC_GANGED

S8_CTRL_SS_CTL

Bits	Name	Type	Description
4:3	SS_STEP	read-write	Softstart voltage step size 00 = SS voltage step of 1 * LSB of VPROG 01 = SS voltage step of 2 * LSB 10 = SS voltage step of 4 * LSB 11 = SS voltage step of 8 * LSB
2:0	SS_DELAY	read-write	Softstart delay between steps = 2 ^ (m + 3) / Fsys, where m = <2:0> (Fsys = 19.2 MHz): 000 = 8-clock cycles (417ns) 001 = 16-clock cycles 010 = 32-clock cycles 011 = 64-clock cycles 100 = 128-clock cycles (6.67us) 101 = 256-clock cycles 110 = 512-clock cycles 111 = 1024-clock cycles (53.3us)

0x12961 S8_CTRL_VS_CTL

Type: read-write
Clock: PBUS_WRCLK
Reset State: 0x00
Reset Name: PERPH_RB

PMIC_GANGED

S8_CTRL_VS_CTL

Bits	Name	Type	Description
7	VS_EN	read-write	Voltage stepping control 0 = VS is disabled 1 = VS is enabled
4:3	VS_STEP	read-write	Voltage stepping voltage step size 00 = VS voltage step of 1 * LSB of VPROG 01 = VS voltage step of 2 * LSB 10 = VS voltage step of 4 * LSB 11 = VS voltage step of 8 * LSB
2:0	VS_DELAY	read-write	Voltage stepping delay between steps = 2 ^ (m + 3) / Fsys, where m = <2:0> (Assuming Fsys = 19.2 MHz): Desired default is 1.67us 000 = 8-clock cycles (417ns) 001 = 16-clock cycles 010 = 32-clock cycles 011 = 64-clock cycles 100 = 128-clock cycles (6.67us) 101 = 256-clock cycles 110 = 512-clock cycles 111 = 1024-clock cycles (53.3us)

0x1296A S8_CTRL_ULS_VALID

Type: read-only
Clock: PBUS_WRCLK
Reset State: Undefined
Reset Name: PERPH_RB

S8_CTRL_ULS_VALID

Bits	Name	Type	Description
7:0	ULS_VALID	read-only	Readback the valid upper limit stop value

0x1296C S8_CTRL_LLS_VALID

Type: read-only
Clock: PBUS_WRCLK
Reset State: Undefined
Reset Name: PERPH_RB

S8_CTRL_LLS_VALID

Bits	Name	Type	Description
7:0	LLS_VALID	read-only	Readback the valid lower limit stop value

8.22 S8_PS_FTS2_PS

0x12A04 S8_PS_PERPH_TYPE

Type: read-only
Clock: PBUS_WRCLK
Reset State: 0x1C
Reset Name: N/A

Peripheral Type

S8_PS_PERPH_TYPE

Bits	Name	Type	Description
7:0	TYPE	read-only	FTS2 Power Stage Reset State: 0x1C

0x12A05 S8_PS_PERPH_SUBTYPE

Type: read-only
Clock: PBUS_WRCLK
Reset State: 0x08
Reset Name: N/A

Peripheral SubType

S8_PS_PERPH_SUBTYPE

Bits	Name	Type	Description
7:0	SUBTYPE	read-only	

0x12A40 S8_PS_VOLTAGE_CTL1

Type: read-write
Clock: PBUS_WRCLK
Reset State: 0x00
Reset Name: PERPH_RB

PMIC_GANGED

S8_PS_VOLTAGE_CTL1

Bits	Name	Type	Description
0	MV_RANGE	read-write	0 = Use low voltage range as specified by VSET and PFM_VOFFSET 1 = Use medium voltage range as specified by VSET and PFM_VOFFSET

0x12A41 S8_PS_VOLTAGE_CTL2

Type: read-write
Clock: PBUS_WRCLK
Reset State: 0xB4
Reset Name: PERPH_RB

PMIC_GANGED

S8_PS_VOLTAGE_CTL2

Bits	Name	Type	Description
7:0	VSET	read-write	Output voltage set point in PWM mode and in PFM mode if the PFM_VOFFSET_EN bit is not asserted For MV_RANGE = 0: VSET => 0.005V * m + 0.080V, where m = <7:0> For MV_RANGE = 1: VSET => 0.010V * m + 0.160V, where m = <7:0> If PFM_VOFFSET_EN is asserted and in PFM mode, add PFM_VOFFSET

0x12A54 S8_PS_PHASE_CNT

Type: read-write
Clock: PBUS_WRCLK
Reset State: 0x00
Reset Name: PERPH_RB

PMIC_GANGED, PMIC_SYNC=clk_19p2:phase_cnt_rb

S8_PS_PHASE_CNT

Bits	Name	Type	Description
1:0	PHASE_CNT	read-write	When MULTIPHASE_EN is asserted, the number of operating phases is 00 = Number of operating phases is 1 01 = Number of operating phases is 2 10 = Number of operating phases is 4 11 = Number of operating phases is 4

8.23 S8_FREQ_BCLK_GEN_CLK

0x12B04 S8_FREQ_PERPH_TYPE

Type: read-only
Clock: PBUS_WRCLK
Reset State: 0x1D
Reset Name: N/A

Peripheral Type

S8_FREQ_PERPH_TYPE

Bits	Name	Type	Description
7:0	TYPE	read-only	BCLK GEN

0x12B05 S8_FREQ_PERPH_SUBTYPE

Type: read-only
Clock: PBUS_WRCLK
Reset State: 0x09
Reset Name: N/A

Peripheral SubType

S8_FREQ_PERPH_SUBTYPE

Bits	Name	Type	Description
7:0	SUBTYPE	read-only	BCLK GEN CLK

0x12B46 S8_FREQ_CLK_ENABLE

Type: read-write
Clock: PBUS_WRCLK
Reset State: 0x01
Reset Name: PERPH_RB

S8_FREQ_CLK_ENABLE

Bits	Name	Type	Description
7	EN_CLK_INT	read-write	0 = do not force the clock on 1 = enable the clock
0	FOLLOW_CLK_SX_REQ	read-write	0 = ignore smps_clk_req<X> 1 = clock is enabled when the clocks request is high smps_clk_req<X>='1'

0x12B50 S8_FREQ_CLK_DIV

Type: read-write
Clock: PBUS_WRCLK
Reset State: 0x02
Reset Name: PERPH_RB

PMIC_GANGED

S8_FREQ_CLK_DIV

Bits	Name	Type	Description
3:0	CLK_DIV	read-write	clock_ frequency = 19.2MHz / (CLK_DIV + 1) FTS2 Buck supports 3.2, 4.8, 6.4 and 9.6 MHz HF2 Buck supports 1.6, 2.4, 2.74, 3.2, 3.8, 4.8, and 6.4 MHz CLK_DIV = 0 is not supported, it will generate 9.6 MHz

0x12B51 S8_FREQ_CLK_PHASE

Type: read-write
Clock: PBUS_WRCLK
Reset State: 0x0C
Reset Name: PERPH_RB

S8_FREQ_CLK_PHASE

Bits	Name	Type	Description
3:0	CLK_PHASE	read-write	Distributed clock phase select: clock phase delay = clock period * (CLK_PHASE / 16)

0x12BC0 S8_FREQ_GANG_CTL1

Type: read-write
Clock: PBUS_WRCLK
Reset State: 0x20
Reset Name: PERPH_RB

S8_FREQ_GANG_CTL1

Bits	Name	Type	Description
7:0	GANG_LEADER_PID	read-write	When GANG_EN (GANG_CTL2[7]) is set, this peripheral will write the same data that is written to the gang leader Peripheral ID. Reads to the gang leader Peripheral ID are ignored by this peripheral. Ganged peripherals must reside within the same Slave ID

0x12BC1 S8_FREQ_GANG_CTL2

Type: read-write
Clock: PBUS_WRCLK
Reset State: 0x80
Reset Name: PERPH_RB

S8_FREQ_GANG_CTL2

Bits	Name	Type	Description
7	GANG_EN	read-write	0 = disable 1 = enable When enabled, this peripheral will write the same data that is written to the gang leader PID. Reads to the gang leader PID are ignored by this peripheral

Index of Registers