Qualcomm
TECHNOLOGIES, INC

# PM8841

## Device Specification

## 80-NA554-1 Rev. D

**May 13, 2013**

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**Qualcomm Technologies, Inc.**
**5775 Morehouse Drive**
**San Diego, CA 92121**
**U.S.A.**

## Revision history

Bars appearing in the margin (as shown here) indicate where technical changes have occurred for this revision. The following table lists the technical content changes for all revisions.

| Revision | Date | Description |
|---|---|---|
| A | April 2012 | Initial release |
| B | June 2012 | ■ Updated Table 2-2 (Expected maximum currents at PI and PO pad types)<br>■ Added content to Chapter 3 through Chapter 7. Since this is all new material, change bars are not used to identify changes on any of these pages. |
| C | October 2012 | ■ Changed BiCMOS to CMOS in Section 1.2 (PM8841 introduction)<br>■ Updated the V_MPP pad voltage grouping in Table 2-1 (I/O description (pad type) parameters)<br>■ Removed Table 2-2 (Expected maximum currents at PI and PO pad types)<br>■ Updated the OPT_2 and OPT_1 entries, and removed the final entry in Table 2-3 (Pin descriptions – IC-level interface functions)<br>■ Updated Table 2-4 (Pin descriptions – configurable input/output functions), and also updated the second note under this table<br>■ Removed the VDD_MSM_IO entry from Table 3-1 (Absolute maximum ratings)<br>■ Added the I_BAT3 entry to Table 3-3 (DC power-supply currents)<br>■ Updated the S3 default voltage to 0.950 V, and changed the S5 default-on status to “Y” in Table 3-5 (Regulator summary)<br>■ Updated multiple values in Table 3-7 (HF-SMPS performance specifications), including a new table footnote<br>■ Updated Figure 3-1 (Example power sequences)<br>■ Added the “MPPs configured as current drivers” section and note 3 to Table 3-10 (Multipurpose-pin performance specifications) |

| Revision | Date | Description |
|---|---|---|
| D | May 2013 | ■ Added V_INT row to Table 2-1<br>■ Updated Functional Description column and added third note under Table 2-4<br>■ Added Steady state parameter in Table 3-1<br>■ Removed the Tc row and replaced it with the TA and TJ rows in Table 3-2<br>■ Table 3-3:<br>□ Added a row for IBAT_2<br>□ Updated note 2, added note 4, and updated Typ and Max values<br>■ Table 3-5:<br>□ Updated all Specified range (V) value ranges<br>□ Updated Default value (V) and Expected use for HF-SMPS row<br>□ Added all notes following<br>■ Updated Note in Section 3.5.1<br>■ Table 3-7:<br>□ Updated comments in Efficiency, Output ripple voltage, and Response to load transitions rows<br>□ Made PWM <-> PFM Parameter, Min, Typ, and Max value changes as noted by change bars,<br>□ Added 100 KHz to 1 MHz sub-row to Power-supply ripple rejection parameter<br>□ Added Peak output impedance row<br>□ Updated Output voltage ranges Parameter<br>□ Added two sub-rows to Rated load current (I_rated)/Low-power PFM mode<br>□ Updated comments in first and third rows<br>□ Updated Comments in all rows except Temperature coefficient, Efficiency – PWM mode, Response to voltage setting, Output ripple, Constant load, and PSR rows<br>□ Added PWM and PFM sub-rows under Load regualation and Line regulation rows<br>□ Removed following note 3<br>■ Replaced Figure 3-1, Figure 3-2, Figure 3-3, and added Figure 3-5<br>■ Updated Min, Typ, and Max values as noted by change bars in Table 3-8<br>■ Added Table 3-9<br>■ Updated second paragraph in Table 3.6.1<br>■ Updated content in Section 3.6.2<br>■ Replaced Table 3-10, including following notes<br>■ Added Table 3-11<br>■ Added Table 3-6<br>■ Updated text in Section 3.7<br>■ Updated Table 3-12:<br>□ Changed Leakage current parameter to Power supply current<br>□ Updated Comments in Output current row<br>□ Added footnote 5 to MPP configured as analog output (buffered VREF output) row and added note 5,<br>□ Updated note 4 and Typ, Max, and Unit values as noted by change bars<br>■ Updated Line 4 row supplier information in Table 4-1<br>■ Added PM8841 ES3/CS row to Table 4-2<br>■ Added MPP configured as analog output (buffered VREF output) row to Table 4-2<br>■ Added Table 7-1 and following note<br>■ Updated Fab and Assembly sites in Section 7.2 |

# Contents

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# 1 Introduction

## 1.1 Documentation overview

Technical information for the PM8841 device is primarily covered by the documents listed in Table 1-1; all of these documents should be studied for a thorough understanding of the IC and its applications. Released PM8841 documents are posted on the CDMA Tech Support Website (https://support.cdmatech.com) and are available for download.

**Table 1-1 Primary PM8841 documentation**

| Document number | Title/description |
|---|---|
| 80-NA554-1<br>(this document) | *PM8841 Device Specification*<br>Provides all PM8841 electrical and mechanical specifications. Additional material includes pin assignment definitions; shipping, storage, and handling instructions; PCB mounting guidelines; and part reliability. This document can be used by company purchasing departments to facilitate procurement. |
| 80-NA554-4 | *PM8841 Device Revision Guide*<br>Provides a history of PM8841 revisions. This document explains how to identify the various IC revisions and discusses known issues (or bugs) for each revision, and how to work around them. |
| 80-NA555-5 | *PM8841 and PM8941 Design Guidelines*<br>■ Detailed functional and interface descriptions for both ICs<br>■ Key design guidelines are illustrated and explained, including:<br>□ Technology overviews<br>□ DC power distribution<br>□ Interface schematic details<br>□ PCB layout guidelines<br>□ External-component recommendations<br>□ Ground and shielding recommendations |

This PM8841 device specification is organized as follows:

| | |
|---|---|
| Chapter 1 | Provides an overview of PM8841 documentation, shows a high-level PM8841 functional block diagram, lists the device features, and lists terms and acronyms used throughout this document. |
| Chapter 2 | Defines the IC pin assignments. |
| Chapter 3 | Defines the IC electrical performance specifications, including absolute maximum ratings and recommended operating conditions. |
| Chapter 4 | Provides IC mechanical information, including dimensions, markings, ordering information, moisture sensitivity, and thermal characteristics. |
| Chapter 5 | Discusses shipping, storage, and handling of PM8841 devices. |
| Chapter 6 | Presents procedures and specifications for mounting the PM8841 onto printed circuit boards (PCBs). |
| Chapter 7 | Presents PM8841 reliability data, including definitions of the qualification samples and a summary of qualification test results. |

## 1.2 PM8841 introduction

The PM8841 device (Figure 1-1), plus its companion PM8941 device, integrates all wireless handset power management, general housekeeping, and user interface support functions into two mixed-signal ICs. Their versatile designs are suitable for multimode, multiband phones, and other wireless products such as data cards and PDAs.

The PM8841 mixed-signal CMOS device is available in the 98-pin wafer-level nanoscale package (98 WLNSP) that includes several ground pins for improved electrical ground, mechanical stability, and thermal continuity.

The PM8841 document set is organized by the following device functionality:

- Output power management
- IC interfaces
- Configurable pins (MPPs) that can be configured to function within these two categories, and perhaps as a user interface function

Most of the information contained in this device specification is organized accordingly – including the circuit groupings within the block diagram (Figure 1-1), pin descriptions (Chapter 2), and detailed electrical specifications (Chapter 3). Refer to the *PM8841 and PM8941 Design Guidelines* (80-NA555-5) for more detailed diagrams and descriptions of each PM8841 function and interface.

**Two major functional blocks:**

**1) Output power management**

**2) IC-level interfaces**

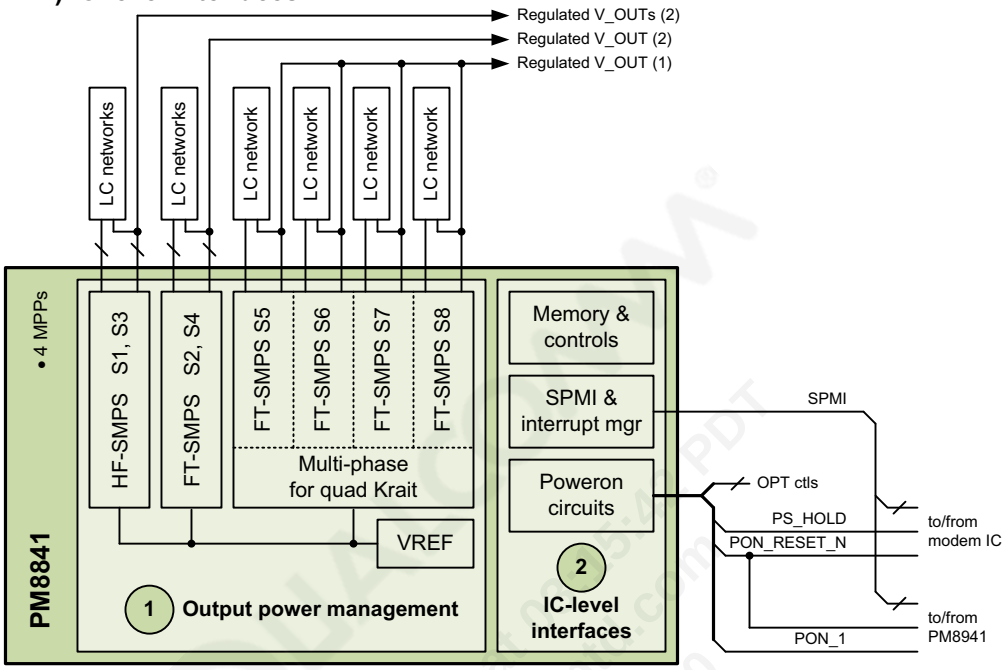



**Figure 1-1 High-level PM8841 functional block diagram**

# 1.3 PM8841 features

**NOTE** Some of the hardware features integrated within the PM8841 must be enabled through the modem IC software. See the latest version of the applicable software release notes to identify the enabled PMIC features.

## 1.3.1 New features integrated into the PM8841

- Supplemented by the PM8941 (the master device in the PM8941/PM8841 device combination)
- Multiphase FT-SMPS circuits (S5 – S8) provide power to the modem IC's quad-Krait applications processor system
- The slave and PBUS interface (SPMI) is shared with the PM8941 to provide modem IC communications, including interrupts
- Programmable boot sequencer and reset control
- Plug-and-play support

### 1.3.2 Summary of PM8841 features

The PM8841 features are listed in Table 1-2.

**Table 1-2 PM8841 feature summary**

| Feature | PM8841 capability |
|---|---|
| ***Output voltage regulation*** | |
| Switched-mode power supplies<br>HF-SMPS<br>Individual FT-SMPS<br>Multi-phase FT-SMPS | <br>Two; one at 2.0 A, one at 1.0 A<br>Two; each at 3.0 A<br>Four; each at 3.0 A |
| ***IC-level interfaces*** | |
| Primary status and control | 2-line SPMI |
| PM8941 interface | Power-on, resets, and shared SPMI |
| Interrupt managers | Supported by SPMI |
| Optional hardware configurations | OPT bits select hardware configuration |
| Power sequencing | Power-on, power-off, and soft resets |
| Extra features | Level translation; external regulator enables; detect inputs & interrupt outputs |
| ***Configurable I/Os*** | |
| MPPs | 4; configurable as digital inputs or outputs; level-translating bidirectional I/Os; analog multiplexer inputs; or VREF analog outputs |
| ***Package*** | |
| Size | 4.45 × 3.58 × 0.55 mm |
| Pin count and package type | 98-pin WLNSP |

## 1.4 Terms and acronyms

Table 1-3 defines terms and acronyms used throughout this document.

**Table 1-3 Terms and acronyms**

| Term or acronym | Definition |
|---|---|
| ADC | Analog-to-digital converter |
| API | Application programming interface |
| ATC | Auto-trickle charger |
| AVS | Adaptive voltage scaling |
| BMS | Battery monitoring system |
| BW | bandwidth |
| CDMA | Code division multiple access |
| DVS | Dynamic voltage scaling |
| FT-SMPS | Fast-transient SMPS |

**Table 1-3 Terms and acronyms** (cont.)

| Term or acronym | Definition |
|---|---|
| GPIO | General-purpose input/output |
| GSM | Global system for mobile communications |
| HF-SMPS | High-frequency SMPS |
| HK | Housekeeping |
| HSED | Headset send/end detect |
| HS-USB | High-speed USB |
| ID | Identification |
| LDO | Low dropout (linear regulator) |
| Li | Lithium |
| LPG | Light pulse generator |
| MPP | Multipurpose pin |
| MUX | Multiplexer |
| OTG | On-the-go |
| OVP | Over-voltage protection |
| PA | Power amplifier |
| PBM | Pulse burst modulation |
| PCB | Printed circuit board |
| PDA | Personal digital assistant |
| PFM | Pulse-frequency modulation |
| PLL | Phase-locked loop |
| PM | Power management |
| PWM | Pulse-width modulation |
| QCT | Qualcomm CDMA Technologies division |
| RCO | RC oscillator |
| RTC | Realtime clock |
| RUIM | Removable user identity module |
| SMBC | Switched-mode battery charger |
| SMPL | Sudden momentary power loss |
| SMPS | Switched-mode power supply (DC-to-DC converter) |
| SPMI | Slave and PBUS interface |
| SS-USB | Super-speed USB |
| SSC | SMPS step control |
| SVS | Static voltage scaline |
| TCXO | Temperature-compensated crystal oscillator |
| UART | Universal asynchronous receiver/transmitter |
| UICC | Universal integrated circuit card |

**Table 1-3 Terms and acronyms** (cont.)

| Term or acronym | Definition |
|---|---|
| UIM | User identity module |
| UMTS | Universal mobile telecommunications system |
| USB | Universal serial bus |
| UVLO | Under-voltage lockout |
| VCO | Voltage-controlled oscillator |
| VCTCXO | Voltage-controlled temperature-compensated crystal oscillator |
| WLNSP | Wafer-level NSP |
| WLED | White LED |
| XO | Crystal oscillator |
| Zero-IF or ZIF | Zero intermediate frequency |

## 1.5 Special marks

Special marks used in this document are defined in Table 1-4.

**Table 1-4 Special marks**

| Mark | Definition |
|---|---|
| [ ] | Brackets ([ ]) sometimes follow a pin, register, or bit name. These brackets enclose a range of numbers. For example, DATA [7:4] may indicate a range that is 4 bits in length, or DATA[7:0] may refer to eight DATA pins. |
| _N | A suffix of _N indicates an active low signal. For example, PON_RESET_N. |
| 0x0000 | Hexadecimal numbers are identified with an x in the number, (for example, 0x0000). All numbers are decimal (base 10) unless otherwise specified. Non-obvious binary numbers have the term binary enclosed in parentheses at the end of the number, [for example, 0011 (binary)]. |
| \| | A vertical bar in the outside margin of a page indicates that a change was made since the previous revision of this document. |

# 2 Pin Definitions

The PM8841 is available in the 98 WLNSP – see Chapter 4 for package details. A high-level view of the pin assignments is illustrated in Figure 2-1.

| | | | | | | | | |
|---|---|---|---|---|---|---|---|---|
| 1 VDD_S5 | 2 VDD_S5 | 3 VSW_S5 | 4 VREG_S5 | 5 VREG_S6 | 6 VREG_S2 | 7 VSW_S2 | 8 VDD_S2 | 9 VDD_S2 |
| 10 GND_S5 | 11 VSW_S5 | 12 VSW_S5 | 13 GND | 14 GND | 15 GND | 16 VSW_S2 | 17 VSW_S2 | 18 GND_S2 |
| 19 VDD_S6 | 20 GND_S5 | 21 GND | 22 GND | 23 GND | 24 GND_REF | | 25 GND_S2 | 26 GND |
| 27 VSW_S6 | 28 VSW_S6 | 29 GND | 30 GND | 31 REF_BYP | 32 VDD_MSM_IO | 33 MPP_01 | 34 MPP_02 | 35 GNDS1 |
| 36 GND_S6 | 37 GND_S6 | 38 GND | 39 GND | 40 GND | 41 VDD_INT_BYP | 42 VREG_S1 | 43 NC | 44 VSW_S1 |
| 45 GND | 46 GND | 47 REMOTE_GND_SNS | 48 GND | 49 GND | 50 VDD_PON | 51 OPT_2 | 52 OPT_1 | 53 VDD_S1 |
| 54 GND_S7 | 55 GND_S7 | 56 GND | 57 GND | 58 GND | 59 XO_IN | 60 VREG_S3 | 61 PON_1 | 62 GND_S3 |
| 63 VSW_S7 | 64 VSW_S7 | 65 GND | 66 GND | 67 GND | 68 PS_HOLD | 69 RESIN_N | 70 NC | 71 VSW_S3 |
| 72 VDD_S7 | 73 GND_S8 | 74 GND | 75 GND | 76 SPMI_DATA | 77 SPMI_CLK | 78 MPP_03 | 79 GND_S4 | 80 VDD_S3 |
| 81 GND_S8 | 82 VSW_S8 | 83 VSW_S8 | 84 GND | 85 GND | 86 MPP_04 | 87 VSW_S4 | 88 VSW_S4 | 89 GND_S4 |
| 90 VDD_S8 | 91 VDD_S8 | 92 VSW_S8 | 93 VREG_S8 | 94 VREG_S7 | 95 VREG_S4 | 96 VSW_S4 | 97 VDD_S4 | 98 VDD_S4 |

OUTPUT PWR MGT | IC I/F | MPPs and GPIOs | No Connection | Power | Ground

**Figure 2-1 PM8841 pin assignments (top view)**

## 2.1 I/O parameter definitions

**Table 2-1 I/O description (pad type) parameters**

| Symbol | Description |
|---|---|
| ***Pad attribute*** | |
| AI | Analog input |
| AO | Analog output |
| DI | Digital input (CMOS) |
| DO | Digital output (CMOS) |
| PI | Power input; a pin that handles 10 mA or more of current flow into the device |
| PO | Power output; a pin that handles 10 mA or more of current flow out of the device |
| Z | High-impedance (high-Z) output |
| ***Pad voltage groupings*** | |
| V_INT | Internally generated voltage supply voltage for some poweron circuits |
| V_PAD | Supply for modem IC interfaces; connected to VDD_MSM_IO |
| V_MPP | Selectable supply for MPP circuits; options include:<br>□ 0 = VPH_PWR (3.6 V)<br>□ 1 = VPH_PWR (3.6 V)<br>□ 2 = VDD_MSM_IO (1.8 V)<br>□ 3 = VDD_MSM_IO (1.8 V) |

## 2.2 Pin descriptions

Descriptions of all pins are presented in the following tables, organized by functional group:

Table 2-2 Output power management

Table 2-3 IC-level interfaces

Table 2-4 Configurable input/output – GPIO and MPPs

Table 2-5 No connect, do not connect, and reserved pins

Table 2-6 Power-supply pins

Table 2-7 Ground pins

**Table 2-2 Pin descriptions – output power management functions**

| Pad # | Pad name and/or function | Pad name or alt function | Pad characteristics [1] | | Functional description |
|---|---|---|---|---|---|
| | | | Voltage | Type | |
| ***Switched-mode power supply (SMPS) circuits*** | | | | | |
| 44 | VSW_S1 | | – | PO | S1 SMPS switching output |
| 42 | VREG_S1 | | – | AI | S1 SMPS sense point |
| 7, 16, 17 | VSW_S2 | | – | PO | S2 SMPS switching output |
| 6 | VREG_S2 | | – | AI | S2 SMPS sense point |
| 71 | VSW_S3 | | – | PO | S3 SMPS switching output |
| 60 | VREG_S3 | | – | AI | S3 SMPS sense point |
| 87, 88, 96 | VSW_S4 | | – | PO | S3 SMPS switching output |
| 95 | VREG_S4 | | – | AI | S3 SMPS sense point |
| 3, 11, 12 | VSW_S5 | | – | PO | S3 SMPS switching output |
| 4 | VREG_S5 | | – | AI | S3 SMPS sense point |
| 27, 28 | VSW_S6 | | – | PO | S3 SMPS switching output |
| 5 | VREG_S6 | | – | AI | S3 SMPS sense point |
| 63, 64 | VSW_S7 | | – | PO | S3 SMPS switching output |
| 94 | VREG_S7 | | – | AI | S3 SMPS sense point |
| 82, 83, 92 | VSW_S8 | | – | PO | S3 SMPS switching output |
| 93 | VREG_S8 | | – | AI | S3 SMPS sense point |
| 47 | REMOTE_GND_SNS | | – | AI | Remote ground sense for multi-phase SMPS (S5 – S8) |
| ***Bandgap voltage reference (VREF) circuits*** | | | | | |
| 31 | REF_BYP | | – | AO | Bandgap reference bypass cap |

1. Refer to Table 2-1 for parameter and acronym definitions.

**Table 2-3 Pin descriptions – IC-level interface functions**

| Pad # | Pad name and/or function | Pad name or alt function | Pad characteristics [1] | | Functional description |
|---|---|---|---|---|---|
| | | | Voltage | Type | |
| 51 | OPT_2 | | | DI | Option HW configuration control bit 2 |
| 52 | OPT_1 | | | DI | Option HW configuration control bit 1 |
| 59 | XO_IN | | V_PAD | DI | XO clock input |
| 69 | RESIN_N | | V_INT | DI | PMIC reset input |
| 68 | PS_HOLD | | V_PAD | DI | Power supply hold control input |
| 61 | PON_1 | | V_PAD | DI | Edge-triggered power-on input |
| 77 | SPMI_CLK | | V_PAD | DO | Slave and PBUS interface clock |
| 76 | SPMI_DATA | | V_PAD | DI, DO | Slave and PBUS interface data |

1. Refer to Table 2-1 for parameter and acronym definitions.

**Table 2-4 Pin descriptions – configurable input/output functions**

| Pad # | Pad name | Configurable function | Pad characteristics [2] | | Functional description |
|---|---|---|---|---|---|
| | | | Voltage | Type | |
| ***MPP functions*** [1] | | | | | |
| 33 | MPP_01 | | – | AO-Z | Configurable MPP; default Hi-Z out |
| 34 | MPP_02 | | – | AO-Z | Configurable MPP; default Hi-Z out |
| 78 | MPP_03 | | – | AO-Z | Configurable MPP; default Hi-Z out |
| 86 | MPP_04 | | – | AO-Z | Configurable MPP; default Hi-Z out |

1. Each MPP pair can be used as a level translator by using different rail voltages.
2. Refer to Table 2-1 for parameter and acronym definitions.

**NOTE** All MPPs default to their high-Z state at power-up, and must be configured after power-up for their intended purposes.

**NOTE** MPPs can be configured as analog inputs; however, with no AMUX present in the PMIC, the voltage cannot be read.

**NOTE** Only odd MPPs (MPP_1 and MPP_3) can be configured as analog outputs. Only even MPPs (MPP_02 and MPP_04) have current sink capability.

**Table 2-5 Pin descriptions – no connect, do not connect, and reserved**

| Pad # | Pad name | Functional description |
|---|---|---|
| 43, 70 | NC | No connect; not connected internally |

**Table 2-6 Pin descriptions – input DC power**

| Pad # | Pad name | Functional description |
|---|---|---|
| 41 | VDD_INT_BYP | Bypass capacitor for internal supply voltage |
| 32 | VDD_MSM_IO | Power supply for PMIC/modem IC I/Os |
| 50 | VDD_PON | Power supply for power-on circuits |
| 53 | VDD_S1 | Power supply for S1 buck converter |
| 8, 9 | VDD_S2 | Power supply for S2 buck converter |
| 80 | VDD_S3 | Power supply for S3 buck converter |
| 97, 98 | VDD_S4 | Power supply for S4 buck converter |
| 1, 2 | VDD_S5 | Power supply for S5 buck converter |
| 19 | VDD_S6 | Power supply for S6 buck converter |
| 72 | VDD_S7 | Power supply for S7 buck converter |
| 90, 91 | VDD_S8 | Power supply for S8 buck converter |

**Table 2-7 Pin descriptions – grounds**

| Pad # | Pad name | Functional description |
|---|---|---|
| 13, 14, 15, 21, 22, 23, 26, 29, 30, 38, 39, 40, 45, 46, 48, 49, 56, 57, 58, 65, 66, 67, 74, 75, 84, 85 | GND | Ground for all non-specialized circuits |
| 24 | GND_REF | Ground for bandgap reference circuit |
| 35 | GND_S1 | Ground for S1 buck converter circuits |
| 18, 25 | GND_S2 | Ground for S2 buck converter circuits |
| 62 | GND_S3 | Ground for S3 buck converter circuits |
| 79, 89 | GND_S4 | Ground for S4 buck converter circuits |
| 10, 20 | GND_S5 | Ground for S5 buck converter circuits |
| 36, 37 | GND_S6 | Ground for S6 buck converter circuits |
| 54, 55 | GND_S7 | Ground for S7 buck converter circuits |
| 73, 81 | GND_S8 | Ground for S8 buck converter circuits |

# 3 Electrical Specifications

## 3.1 Absolute maximum ratings

Operating the PM8841 under conditions beyond its absolute maximum ratings (Table 3-1) may damage the device. Absolute maximum ratings are limiting values to be considered individually, when all other parameters are within their specified operating ranges. Functional operation and specification compliance under any absolute maximum condition, or after exposure to any of these conditions, is not guaranteed or implied. Exposure may affect device reliability.

**Table 3-1 Absolute maximum ratings**

| Parameter | | Min | Max | Units |
|---|---|---|---|---|
| ***Power-supply voltages*** | | | | |
| VDD_PON | Poweron-circuits supply voltage | -0.5 | +6.0 | V |
| VDD_Sx | Steady state | -0.5 | +6.0 | V |
| | Transient (<10 ms) | -0.5 | +7.0 | V |
| ***Signal pins*** | | | | |
| V_IN | Voltage on any non-power-supply pin 1 | -0.5 | $V_{XX}$ + 0.5 | V |
| ***ESD protection and thermal conditions*** – see Section 7.1. | | | | |

1. $V_{XX}$ is the supply voltage associated with the input or output pin to which the test voltage is applied.

## 3.2 Recommended operating conditions

Operating conditions include parameters that are under the control of the user: power-supply voltage and ambient temperature (Table 3-2). The PM8841 meets all performance specifications listed in Section 3.3 through Section 3.7 when used within the recommended operating conditions, unless otherwise noted in those sections (provided the absolute maximum ratings have never been exceeded).

**Table 3-2 Recommended operating conditions**

| Parameter | | Min | Typ | Max | Units |
|---|---|---|---|---|---|
| ***Power-supply and related sense voltages*** | | | | | |
| VDD_MSM_IO | Pad voltage for digital I/Os to/from the IC | 1.75 | – | 1.85 | V |
| VDD_PON | Poweron-circuits supply voltage 1 | 2.5 | 3.6 | 4.5 | V |
| VDD_Sx | SMPS supply voltages 1 | 2.5 | 3.6 | 4.5 | V |
| ***Signal pins*** | | | | | |
| V_IN | Voltage on any non-power-supply pin 2 | 0 | – | $V_{XX}$ + 0.5 | V |
| ***Thermal conditions*** | | | | | |
| TA | Ambient temperature | -30 | +25 | +85 | C |
| TJ | Junction temperature | -30 | +25 | +125 | C |

1. Specified range accommodates *low-voltage* lithium batteries on the low end, and *high-voltage* lithium batteries on the high end.
2. $V_{XX}$ is the supply voltage associated with the input or output pin to which the test voltage is applied.

## 3.3 DC power consumption

This section specifies DC power-supply currents for the various IC operating modes (Table 3-3). Typical currents are based on IC operation at room temperature (+25°C) using default parameter settings.

**Table 3-3 DC power-supply currents**

| Parameter | | Comments | Min | Typ | Max | Units |
|---|---|---|---|---|---|---|
| I_BAT1 | Supply current, active mode 1 [1] | | – | 2.9 | 3.0 | mA |
| I_BAT2 | Supply current, active mode 2 [2] | | – | 1.9 | 3 | mA |
| I_BAT3 | Supply current, sleep mode [3] | | – | 110 | 120 | µA |
| I_BAT4 | Supply current, off mode [4] | | – | 3 | 10 | µA |

1. I_BAT1 is the total supply current from the main battery with the PMIC on, crystal oscillators on, and the following outputs enabled but without loading: VREG_S1 = 0.95 V, VREG_S2 = 0.9 V, VREG_S5 = 0.9 V.
2. I_BAT2 is the total supply current from the main battery with the PMIC on, crystal oscillators on, and the following outputs enabled but without loading: VREG_S1 = 0.95 V, VREG_S2 = 0.9 V, and VREG_S3 = 0.9 V.
3. I_BAT3 is the total supply current from the main battery with the PMIC on, the master bandgap reference in its low-power mode, and the following outputs enabled in their low-power modes but without loading: VREG_S1 = 0.67 V, VREG_S2 = 0.5 V.
4. I_BAT4 is the total supply current from the main battery with the PMIC off. This only applies when the temperature is between -30°C and 60°C.

## 3.4 Digital logic characteristics

PM8841 digital I/O characteristics such as voltage levels, current levels, and capacitance are specified in Table 3-4.

**Table 3-4 Digital I/O characteristics**

| Parameter | | Comments [4] | Min | Typ | Max | Units |
|---|---|---|---|---|---|---|
| $V_{IH}$ | High-level input voltage | | 0.65 · $V_{IO}$ | – | $V_{IO}$ + 0.3 | V |
| $V_{IL}$ | Low-level input voltage | | -0.3 | – | 0.35 · $V_{IO}$ | V |
| $V_{SHYS}$ | Schmitt hysteresis voltage | | 15 | – | – | mV |
| $I_L$ | Input leakage current [1] | $V_{IO}$ = max, $V_{IN}$ = 0 V to $V_{IO}$ | -0.20 | – | +0.20 | µA |
| $V_{OH}$ | High-level output voltage | $I_{out}$ = $I_{OH}$ | $V_{IO}$ - 0.45 | – | $V_{IO}$ | V |
| $V_{OL}$ | Low-level output voltage | $I_{out}$ = $I_{OL}$ | 0 | – | 0.45 | V |
| $I_{OH}$ | High-level output current [2] | $V_{out}$ = $V_{OH}$ | 3 | – | – | mA |
| $I_{OL}$ | Low-level output current 2 | $V_{out}$ = $V_{OL}$ | – | – | -3 | mA |
| $C_{IN}$ | Input capacitance [3] | | – | – | 5 | pF |

1. MPP pins comply with the input leakage specification only when configured as a digital input, or set to its tri-state mode.
2. Output current specifications apply to all digital outputs unless specified otherwise, and are superseded by specifications for specific pins (such as MPP pins).
3. Input capacitance is guaranteed by design, but is not 100% tested.
4. $V_{IO}$ is the supply voltage for the MSM/PM IC interface (most PMIC digital I/Os).

## 3.5 Output power management

Output power management circuits include:

- Bandgap voltage reference circuit
- HF-SMPS circuits
- FT-SMPS circuits

The PM8841 is supplemented by the PM8941 to provide all the regulated voltages needed for most wireless handset applications. Independent regulated power sources are required for various electronic functions to avoid signal corruption between diverse circuits, support power-management sequencing, and to meet different voltage-level requirements.

A total of eight programmable voltage regulators are provided by the PM8841, with all outputs derived from a common bandgap reference circuit. Each regulator can be set to a low-power mode for power savings.

A high-level summary of the regulators and their intended uses is presented in Table 3-5.

**Table 3-5 Regulator summary**

| Function | Circuit type | Default voltage (V) [1] | Specified range (V) [2] | Programmable range (V) | Rated current (mA) [3] | Default on | Expected use |
|---|---|---|---|---|---|---|---|
| S1 | HF-SMPS | 0.950 | 0.675 – 1.050 | 0.375 – 3.050 | 2000 | Y | Modem IC memory and PLLs |
| S2 | FT-SMPS | 0.900 | 0.500 – 1.050 | 0.350 – 2.250 | 3000 | Y | Modem IC core, SDC, and USB |
| S3 | HF-SMPS | 0.900 | 0.500 – 1.050 | 0.375 – 3.050 | 1000 | – | Modem IC modem subsystem |
| S4 | FT-SMPS | 0.900 | 0.500 – 1.050 | 0.350 – 2.250 | 3000 | – | Modem IC graphics |
| S5 | FT-SMPS | 0.900 | 0.500 – 1.050 | 0.350 – 2.250 | 3000 | Y | Modem IC quad-Krait microprocessors |
| S6 | FT-SMPS | 0.900 | 0.500 – 1.050 | 0.350 – 2.250 | 3000 | – | |
| S7 | FT-SMPS | 0.900 | 0.500 – 1.050 | 0.350 – 2.250 | 3000 | – | |
| S8 | FT-SMPS | 0.900 | 0.500 – 1.050 | 0.350 – 2.250 | 3000 | – | |

1. All regulators have output voltage default settings. The default voltage and poweron state depends on the PBS configurations.
2. The specified range corresponds to the range where performance is tested
3. Rated current is the maximum current for which specification compliance is guaranteed unless otherwise stated.

### 3.5.1 Reference circuit

All PMIC regulator circuits, and some other internal circuits, are driven by a common, on-chip voltage-reference circuit. An on-chip series resistor supplements an off-chip 0.1 µF bypass capacitor at the REF_BYP pin to create a lowpass function, which filters the reference voltage distributed throughout the device.

**NOTE** Do not load the REF_BYP pin and do not share the REF_GND pin with any other block. Use an MPP configured as an analog output if the reference voltage is needed off-chip.

Applicable voltage-reference performance specifications are given in Table 3-6.

**Table 3-6 Voltage-reference performance specifications**

| Parameter | Comments | Min | Typ | Max | Units |
|---|---|---|---|---|---|
| Nominal internal VREF | At REF_BYP pin | – | 1.250 | – | V |
| Output voltage deviations | | | | | |
| Normal operation | Over temperature only, -20 to +120ºC | -0.32 | – | +0.32 | % |
| Normal operation | All operating conditions | -0.50 | – | +0.50 | % |
| Sleep mode | All operating conditions | -1.00 | – | +1.00 | % |

### 3.5.2 HF-SMPS

The PM8841 includes two high-frequency switched-mode power supply (HF-SMPS) circuits. They support PWM and PFM modes, and automatically transition between PWM and PFM modes depending on the load current. Pertinent performance specifications are given in Table 3-7.

**Table 3-7 HF-SMPS performance specifications**

| Parameter | Comments [2, 3] | Min | Typ | Max | Units |
|---|---|---|---|---|---|
| Output voltage ranges | | | | | |
| Programmable range | 12.5 mV steps | 0.375 | – | 1.5625 | V |
| | 25 mV steps | 1.550 | – | 3.1250 | V |
| Rated load current (I_rated) | Continuous current delivery | | | | |
| PWM mode | | | | | |
| S1 | | – | 2000 | – | mA |
| S3 | | – | 1000 | – | mA |
| PFM mode | | | | | |
| S1 | | – | – | 200 | mA |
| S3 | | – | – | 200 | mA |
| Short circuit/peak current (through inductor) | VREG pin shorted; current limit is set via SPMI programming. | 0.7 * I_limit | I_limit | 1.3 *I_limit | mA |

**Table 3-7 HF-SMPS performance specifications** (cont.)

| Parameter | Comments [2, 3] | Min | Typ | Max | Units |
|---|---|---|---|---|---|
| Voltage error | | | | | |
| PWM mode | V_out > 1.0 V, I_rated/2 | -1 | – | +1 | % |
| | V_out < 1.0 V, I_rated/2 | -10 | – | +10 | mV |
| PFM mode | V_out > 1.0 V, I_rated/2 | -1 | – | +1 | % |
| | V_out < 1.0 V, I_rated/2 | -10 | – | +10 | mV |
| Overall error [1] | | | | | |
| PWM mode | V_out > 1.0 V, I_rated/2 | -2 | – | +2 | % |
| | V_out < 1.0 V, I_rated/2 | -20 | – | +20 | mV |
| PFM mode | V_out > 1.0 V, I_rated/2 | -2 | – | +4 | % |
| | V_out < 1.0 V, I_rated/2 | -20 | – | +40 | mV |
| Temperature coefficient | | -100 | – | +100 | ppm/C |
| Efficiency | VBAT 3.6 V | | | | |
| PWM mode | V_out = 1.8 V, I_load = 300 mA | – | 90 | – | % |
| | V_out = 1.8 V, I_load = 10 and 600 mA | – | 85 | – | % |
| PFM mode | V_out = 1.8 V, I_load = 800 mA | – | 80 | – | % |
| | V_out = 1.2 V, I_load = 5 mA | – | 80 | – | % |
| Enable settling time | From enable to within 1% of final value | | | | |
| Slow start | | – | – | 500 | µs |
| Fast start | | – | – | 100 | µs |
| Enable overshoot | | | | | |
| Slow start | V_out > 1.0 V, no load | – | – | 3 | % |
| | V_out < 1.0 V, no load | – | – | 30 | mV |
| Fast start | V_out > 1.0 V, no load | – | – | 6 | % |
| | V_out < 1.0 V, no load | – | – | 60 | mV |
| Voltage-step settling time, per least significant bit (LSB) | To within 1% of final value | – | – | 10 | µs |
| Response to load transitions | PWM mode | | | | |
| Dip due to low-to-high load | 400 mA load change in 0.05*I_rated to I_rated range | – | – | 40 | mV |
| Spike due to high-to-low load | T400 mA load change in 0.05*I_rated to I_rated range | – | – | 70 | mV |
| Output ripple voltage | Tested at the switching frequency and 20 MHz measurement BW | | | | |
| PWM pulse-skipping mode | 40 mA load | – | 20 | 40 | mVpp |
| PWM non-pulse-skipping mode | I_rated | – | 10 | 20 | mVpp |
| PFM mode | 50 mA load | – | 30 | 50 | mVpp |
| Load regulation | V_in ≥ V_out + 1 V; I_load = 0.01 · I_rated to I_rated | – | – | 0.25 | % |

**Table 3-7 HF-SMPS performance specifications** (cont.)

| Parameter | Comments [2, 3] | Min | Typ | Max | Units |
|---|---|---|---|---|---|
| Line regulation | V_in = 3.2 V to 4.2 V; I_load = 100 mA | – | – | 0.25 | %/V |
| Power-supply ripple rejection (PSRR) | | | | | |
| 50 Hz to 1 kHz | | – | 40 | – | dB |
| 1 kHz to 100 kHz | | – | 20 | – | dB |
| 100 kHz to 1 MHz | | – | 30 | – | dB |
| Output noise | | | | | |
| F < 5 kHz | | – | -101 | – | dBm/Hz |
| F = 5 kHz to 10 kHz | | – | -106 | – | dBm/Hz |
| F = 10 kHz to 500 kHz | | – | -106 | – | dBm/Hz |
| F = 500 kHz to 1 MHz | | – | -116 | – | dBm/Hz |
| F > 1 MHz | | – | -116 | – | dBm/Hz |
| Peak output impedance | 1 kHz to 1 MHz | – | 150 | – | mΩ |
| Ground current | | | | | |
| PWM mode, no load | | – | 550 | 750 | µA |
| PFM mode, no load | | – | 20 | 30 | µA |

1. Overall error includes voltage error, load and line regulation, and errors due to temperature and process.
2. All specifications apply over the device's recommended operating conditions, load current range, and capacitor ESR range, unless noted otherwise.
3. Performance characteristics that may degrade if the rated output current is exceeded:
   • Voltage error • Efficiency • Output ripple

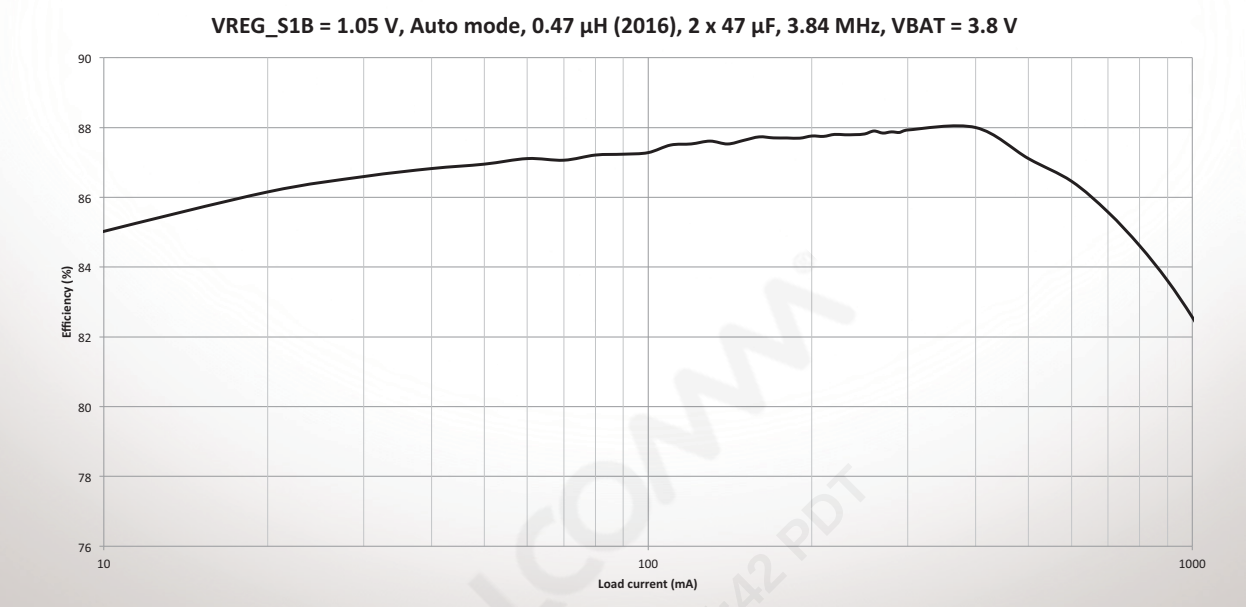



**Figure 3-1 S1 efficiency plot (measured) on a PM8841 device**

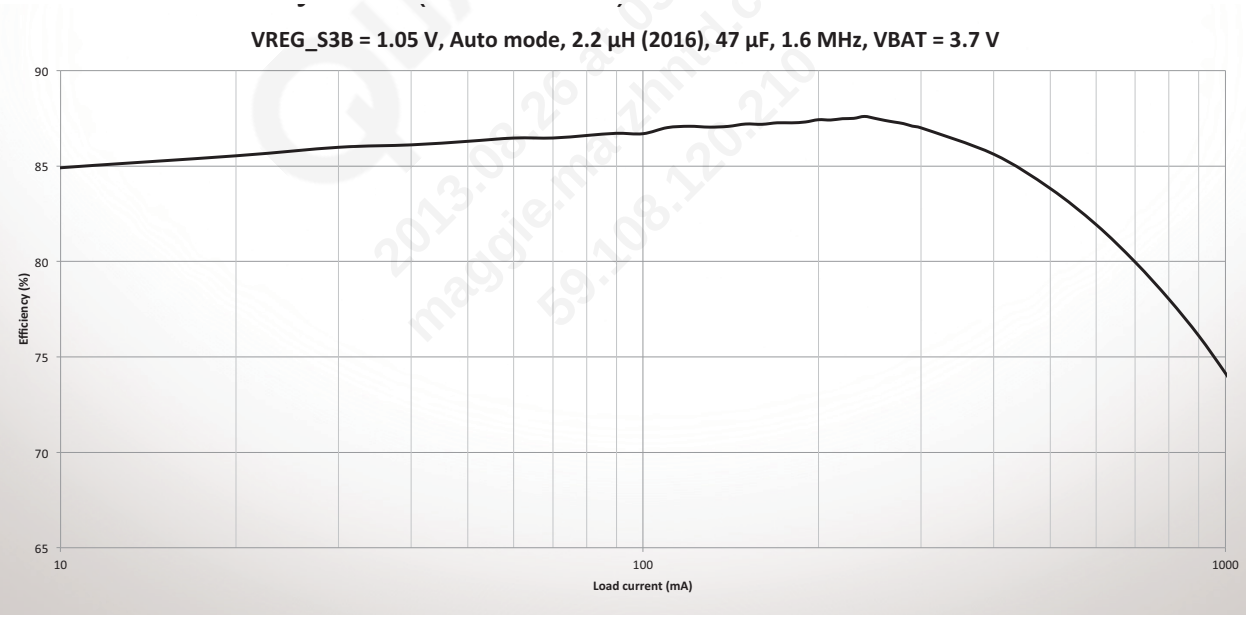



**Figure 3-2 S3 efficiency plot (measured) on a PM8841**

## 3.5.3 FT-SMPS

The PM8841 includes six fast-transient switched-mode power supply (FT-SMPS) circuits; four are combined in a multi-phase scheme to create the quad-Krait microprocessor power rail. All FT-SMPS circuits support PWM and PFM modes, and automatically transition between PWM and PFM modes depending on the load current. Pertinent performance specifications are given in Table 3-8 and Table 3-9.

### Table 3-8 3000 mA FT-SMPS performance specifications (single phase)

| Parameter | Comments [1, 2] | Min | Typ | Max | Unit |
|---|---|---|---|---|---|
| Output voltage ranges | Selected in SW | | | | |
| LV range | 5 mV increments | 0.350 | – | 1.275 | V |
| MV range | 10 mV increments | 0.700 | – | 2.250 | V |
| Rated load current (I_rated) | | | | | |
| Normal PWM mode | | – | – | 3000 | mA |
| Low-power PFM mode | LPM_CL = 1.0 A | – | – | 500 | mA |
| | LPM_CL = 0.5 A | – | – | 250 | mA |
| Voltage error | | | | | |
| PWM mode | V_out > 0.8 V | -1 | – | +1 | % |
| | V_out < 0.8 V | -8 | – | +8 | mV |
| PFM mode | V_out > 0.8 V | -2 | – | +2 | % |
| | V_out < 0.8 V | -16 | – | +16 | mV |
| Temperature coefficient | | -100 | 0 | +100 | ppm/C |
| Efficiency – PWM mode | VBAT = 3.6 V; V_out = 0.9 V | | | | |
| I_load = TBD mA | | – | TBD | – | % |
| I_load = TBD mA | | – | TBD | – | % |
| Enable responses | From enable to within 1% of final value, 100 µs with Cload = 10 µF, no load | | | | |
| Settling time | | – | – | 100 | µs |
| Overshoot | | – | – | +3 | % |
| Response to load transitions | PWM mode | | | | |
| Dip due to low-to-high load | 500 to 2500 mA load change | – | – | 40 | mV |
| Overshoot due to high-to-low load | 2500 to 500 mA load change | – | – | 70 | mV |
| Response to voltage setting | | | | | |
| Settling time | | – | – | 1 | µs |
| Overshoot | | – | – | TBD | % |
| Output ripple, constant load | | | | | |
| PWM mode | | – | 5 | 10 | mVpp |
| PFM mode | | – | 20 | 25 | mVpp |
| Load regulation | | | | | |
| PWM mode | | – | – | 0.25 | % |
| PFM mode | | – | – | 0.50 | % |
| Line regulation | V_in = 3.0 V to 4.4 V | | | | |
| PWM mode | | – | – | 0.10 | %/V |
| PFM mode | | – | – | 0.25 | %/V |

**Table 3-8 3000 mA FT-SMPS performance specifications (single phase)** (cont.)

| Parameter | Comments [1, 2] | Min | Typ | Max | Unit |
|---|---|---|---|---|---|
| PSRR | Power-supply ripple rejection ratio | | | | |
| 50 to 1000 Hz | | – | 50 | – | dB |
| 1 to 100 kHz | | – | 30 | – | dB |
| Ground current | | | | | |
| No load, PFM mode | | – | 65 | 100 | µA |
| No load, PWM mode | | – | 350 | 600 | µA |

1. All specifications apply over the device's recommended operating conditions, load current range, and capacitor ESR range, unless noted otherwise.
2. Performance characteristics that may degrade if the rated output current is exceeded:
   • Voltage error • Efficiency • Output ripple

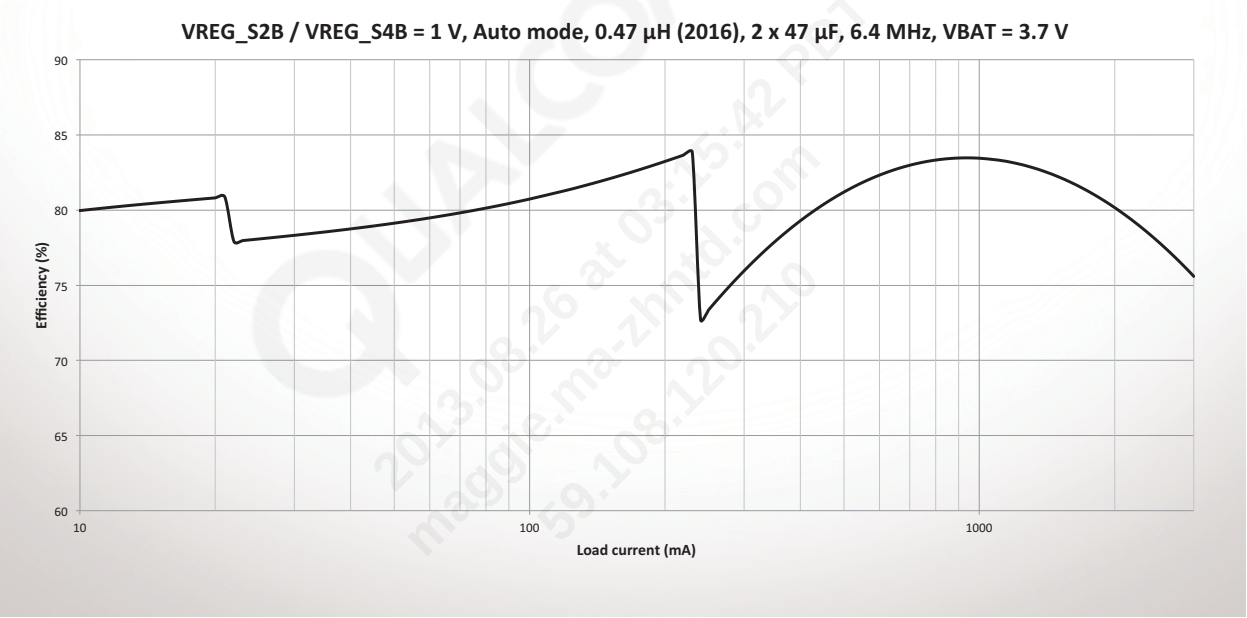



**Figure 3-3 S2/S4 efficiency plot (measured) on a PM8841 device**

**Table 3-9 Multiphase FT-SMPS performance specifications**

| Parameter | Comments [1, 2] | Min | Typ | Max | Unit |
|---|---|---|---|---|---|
| Output voltage ranges | Selected in SW | | | | |
| LV range | 5 mV increments | 0.350 | – | 1.275 | V |
| MV range | 10 mV increments | 0.700 | – | 2.250 | V |
| Rated load current (I_rated) | | | | | |
| Normal PWM mode | | – | – | 12 | A |
| Low-power PFM mode | | – | – | 0.5 | A |

**Table 3-9 Multiphase FT-SMPS performance specifications** (cont.)

| | | | | | |
|---|---|---|---|---|---|
| Voltage error | | | | | |
| PWM mode | V_out > 0.8 V | -1 | – | 1 | % |
| | V_out > 0.8 V | -8 | – | 8 | mV |
| PFM mode | V_out > 0.8 V | -1 | – | 3 | % |
| | V_out > 0.8 V | -8 | – | 24 | mV |
| Enable responses | From enable to within 1% of final value 100 µs with Cload = 10 µF, no load | – | - | 100 | µs |
| Responses to load transitions | | – | – | 40 | mV |
| Dip due to low-to-high | 2 A to 10 A load change | – | – | 70 | mV |
| Overshoot due to high-to-low | 10 A to 2 A load change | | | | |
| Output ripple, constant load | | | | | |
| PWM mode | | – | 5 | 10 | mVpp |
| PFM mode | | – | 12 | 20 | mVpp |
| Ground current | | | | | |
| No load, PFM mode | | – | 65 | 100 | µA |
| No load, PWM mode | | – | 1.85 | 2.85 | mA |

1. All specifications apply over the device's recommended operating conditions, load current range, and capacitor ESR range, unless noted otherwise.
2. Performance characteristics that may degrade if the rated output current is exceeded:
   • Voltage error • Efficiency • Output ripple

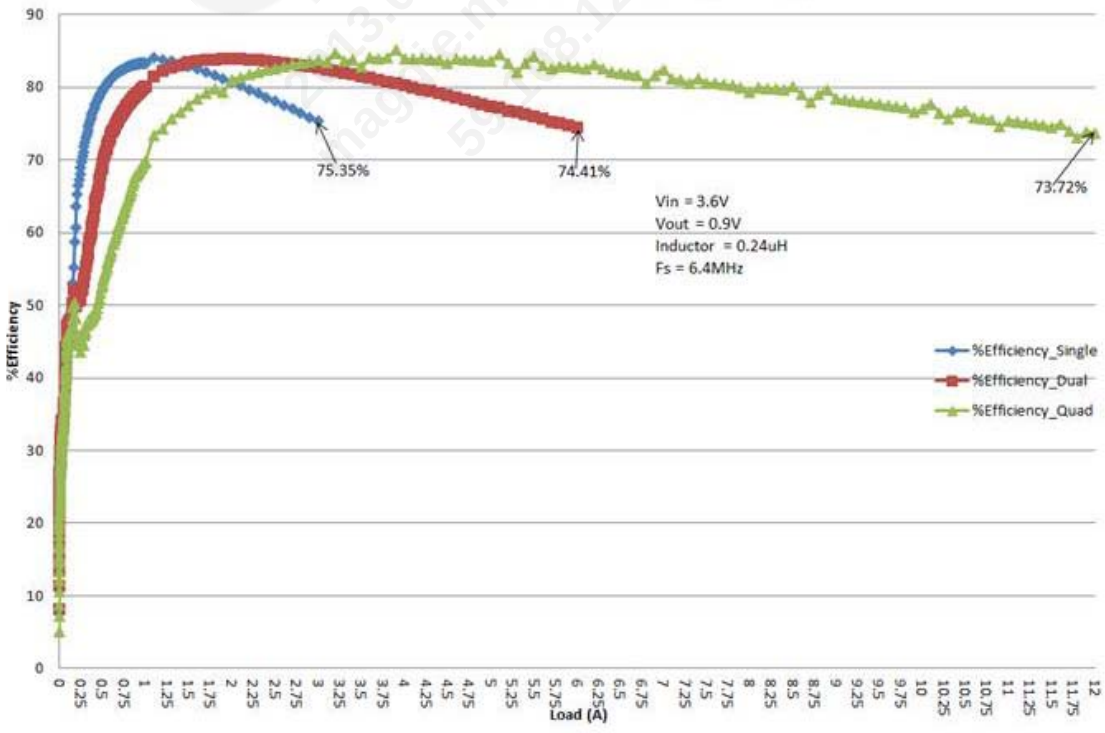



**Figure 3-4 S5-8 efficiency plots (measured) on a PM8841 device**

## 3.6 IC-level interfaces

The IC-level interfaces include poweron circuits; the SPMI; and interrupt managers. Parameters associated with these IC-level interface functions are specified in the following subsections. MPP functions are also considered part of the IC-level interface functional block, but they are specified in their own section (Section 3.7).

### 3.6.1 Poweron circuits and the power sequences

Dedicated input pins continuously monitor PM8941 output signals that might trigger a poweron sequence. When triggered, the PM8841 circuits are powered on, and then its regulators are enabled.

PM8841 ES1 devices exhibit a single poweron sequence as shown in Figure 3-5. ES2 devices and onwards exhibit the dual poweron sequence as shown in Figure 3-6.

The I/Os to/from the poweron circuits are basic digital control signals that must meet the voltage-level requirements stated in Section 3.4. Additional poweron-circuit performance specifications are listed in Table 3-9. More complete definitions for time intervals included in the table are provided in the *PM8841 and PM8941 Design Guidelines* (80-NA555-5).

**Table 3-10 Specifications for single poweron sequence**

| Parameter | Comments | Min | Typ | Max | Units |
|---|---|---|---|---|---|
| Internal pullup resistor | At KYPD_PWR_N and CBL_PWR_N pins | 150 | 200 | 250 | kΩ |
| tmbg | Poweron trigger to MBG_EN/pre-pon PBS sequence (includes debounce time of the poweron trigger) | 12.01 | 15.99 | 20.02 | msec |
| tBMS | Time for BMS to make an open circuit voltage measurement | 48.00 | 64.00 | 80.00 | msec |
| tprepon1 | Time from MBG_EN to start of first regulator event | 64.95 | 86.60 | 108.25 | msec |
| tgpio21 | Time from MBG going HIGH until GPIO21 begins to go HIGH | 16.95 | 22.60 | 28.25 | msec |
| tprebuck | Hardcoded delay in PBS OTP to allow external boost bypass or prebuck to settle | 7.50 | 10.00 | 12.50 | msec |
| tMBG_slave | Poweron event for slave PMIC to MBG_EN/pre-pon PBS sequence (includes debounce time of the poweron trigger) | 12.01 | 15.99 | 20.02 | msec |
| tprepon_slave | Time from MBG_EN to start of first regulator event | 11.70 | 15.60 | 19.50 | msec |
| tpbs_dly1 | Hardcoded delay to allow the slave PMIC to boot core supplies before continuing PON sequence | 36.62 | 48.80 | 61.00 | msec |
| tsettle | Regulator settling time | – | – | 500.00 | µsec |
| treg [1] | Time between regulator enables | 73.24 | – | 622.07 | µsec |
| tBBCLK_1 | Time from the XO_OUT_D0 clock enable to the first clock edge | 14.25 | 19.00 | 23.75 | msec |

**Table 3-10 Specifications for single poweron sequence** (cont.)

| Parameter | Comments | Min | Typ | Max | Units |
|---|---|---|---|---|---|
| tsec_reg | Time from LDO24 enable to the next regulator in the sequence (LDO12) | 18.75 | 25 | 31.25 | msec |
| tpbs_dly2 | Time between first clock edge and PON_RESET_N being set high | – | 30 | – | msec |
| tpshold | Time for MSM to assert PS_HOLD (PS_HOLD timeout) | 150 | 200 | 250 | msec |
| tpbs_dly3 | Time delay between PON_OUT dropping low and the beginning of the LDO21 turn-off event (PBS controlled) | 0.34 | 0.46 | 0.57 | msec |
| tpbs_dly4 | Wait time (hardcoded in the PBS) for the Krait rail to go low and turn-off event start for S2B. The assumption is that the entire Poff sequence in PM8941 will finish by this time. | 5.26 | 7.02 | 8.77 | msec |
| tpbs_dly5 | Wait time (hardcoded in PBS) between the instant the MPP1 goes low and the beginning of the GPIO21 turn-off event. | 2.27 | 3.02 | 3.78 | msec |
| Debounce timer [2] | | 16 | – | 10256 | msec |

1. $t_{reg}$ for LDO24 to LDO7 is about 200 µsec; VREF_LPDDR is derived from LDO1 and turns on about 250 µsec after LDO1.
2. Delay between triggering event (such as keypad press) and corresponding interrupt; a programmable value.

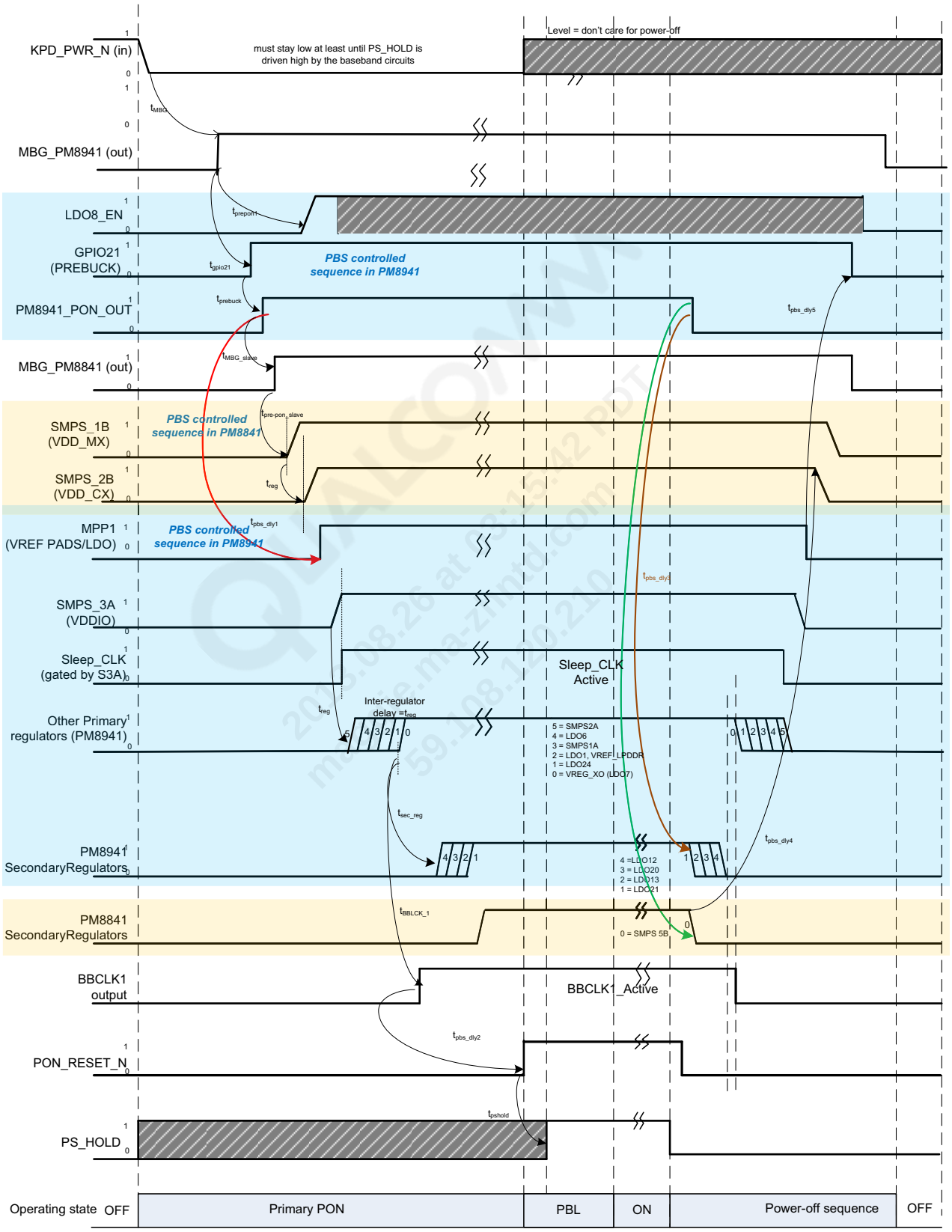



**Figure 3-5 Example PM8x41 single poweron sequence**

### Table 3-11 Poweron circuit performance specifications with dual poweron sequence

| Parameter | Comments | Min | Typ | Max | Units |
|---|---|---|---|---|---|
| Internal pullup resistor | At KYPD_PWR_N and CBL_PWR_N pins | 150 | 200 | 250 | kΩ |
| tmbg | Poweron trigger to MBG_EN/pre-pon PBS sequence (includes debounce time of the power-on trigger) | 12.01 | 15.99 | 20.02 | msec |
| tBMS | Time for BMS to make an open circuit voltage measurement | 48.00 | 64.00 | 80.00 | msec |
| tprepon1 | Time from MBG_EN to start of first regulator event | 64.95 | 86.60 | 108.25 | msec |
| tgpio21 | Time from MBG going HIGH till GPIO21 begins to go HIGH | 16.95 | 22.60 | 28.25 | msec |
| tprebuck | Hardcoded delay in PBS OTP to allow external boost bypass or prebuck to settle | 7.50 | 10.00 | 12.50 | msec |
| tMBG_slave | Poweron event for slave PMIC to MBG_EN/pre-pon PBS sequence (includes debounce time of the power-on trigger) | 12.01 | 15.99 | 20.02 | msec |
| tprepon_slave | Time from MBG_EN to start of first regulator event | 11.70 | 15.60 | 19.50 | msec |
| tpbs_dly1 | Hardcoded delay to allow slave PMIC to boot core supplies before continuing PON sequence | 36.62 | 48.80 | 61.00 | msec |
| tsettle | Regulator settling time | – | – | 500.00 | µsec |
| treg [1] | Time between regulator enables | 73.24 | – | 622.07 | µsec |
| tBBCLK_1 | Time from the enable of the XO_OUT_D0 clock to the first clock edge | 14.25 | 19.00 | 23.75 | msec |
| treset1 | Time between first clock edge and PON_RESET_N being set high | TBD | TBD | TBD | msec |
| tpshold | Time for MSM to assert PS_HOLD (PS_HOLD timeout) | 150 | 200.00 | 250 | msec |
| tpbs_dly2 | Time between SPON message from MSM to S5B turning ON | 2.44 | 3.20 | 4.06 | msec |
| tpbs_dly3 | Time delay between PON_OUT dropping low and the beginning of turn-off event of LDO21 (PBS controlled) | 0.34 | 0.46 | .057 | msec |
| tpbs_dly4 | Wait Time (hardcoded in PBS) for the Krait rail to go low, and the beginning of turn-off event for S2B. We assume that the entire Poff sequence in PM8941 shall finish by this time | 5.26 | 7.02 | 8.77 | msec |
| tpbs_dly5 | Wait time (hardcoded in PBS) between the instant the MPP1 goes low, and the beginning of the GPIO21 turn-off event | 2.27 | 3.02 | 3.78 | msec |
| Debounce timer [2] | | 16 | – | 10256 | msec |

1. $t_{reg}$ for LDO24 to LDO7 is about 200 µsec; VREF_LPDDR is derived from LDO1 and turns on about 250 µsec after LDO1.
2. Delay between triggering event (such as keypad press) and corresponding interrupt; a programmable value.

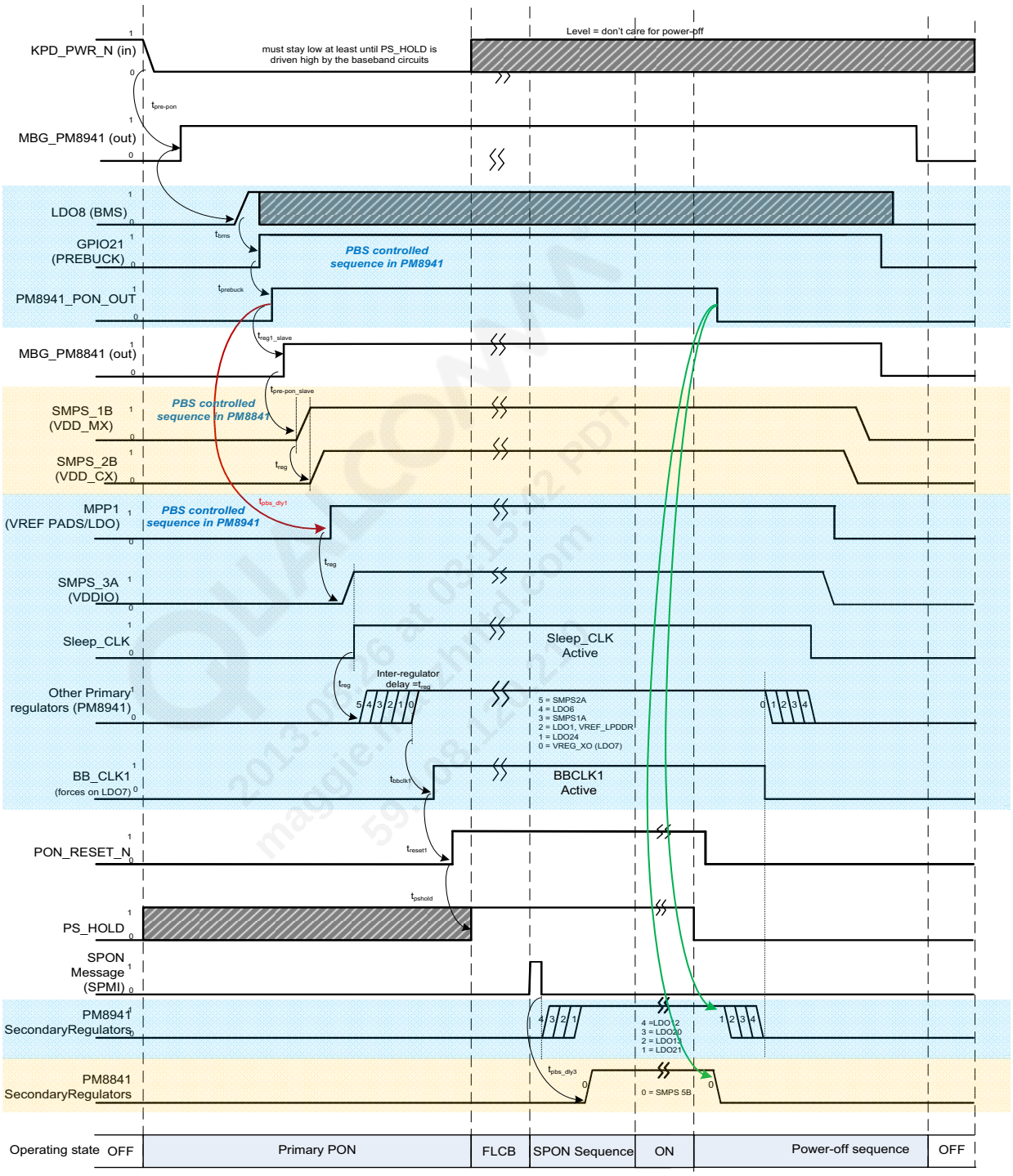



**Figure 3-6 Example PM8x41 dual poweron sequence**

### 3.6.2 OPT[2:1] hardwired controls

Two pins (OPT_2 and OPT_1) must be hardwired to ground or VDD, or be left open (high-impedance state or Hi-z); this yields nine possible combinations. At the time of this document's release, one combination has been assigned for the MSM8x74 chipset:

- OPT[2:1] = GND, GND

### 3.6.3 SPMI and the interrupt managers

The SPMI is a bidirectional, two-line digital interface that meets the voltage-level and current-level requirements stated in Section 3.4.

PMIC interrupt managers support the chipset modem and its processors, and communicates with the modem IC via SPMI. Since the interrupt managers are entirely embedded functions, additional performance specifications are not required.

## 3.7 Multipurpose pin specifications

The PM8841 includes four multipurpose pins (MPPs), and they can be configured for any of the functions specified within Table 3-12. All MPPs are high-Z at power on (set as disabled current sinks). All MPPs can be setup as interrupt trigger sources.

**Table 3-12 Multipurpose-pin performance specifications**

| Parameter | Comments | Min | Typ | Max | Units |
|---|---|---|---|---|---|
| ***MPP configured as digital input*** [1] | | | | | |
| Logic high input voltage | | 0.65 · V_M | – | – | V |
| Logic low input voltage | | – | – | 0.35 · V_M | V |
| ***MPP configured as digital output*** [1] | | | | | |
| Logic high output voltage | $I_{out} = I_{OH}$ | V_M - 0.45 | – | V_M | V |
| Logic low output voltage | $I_{out} = I_{OL}$ | 0 | – | 0.45 | V |
| ***MPP configured as bidirectional I/O*** [2] | | | | | |
| Nominal pullup resistance | Programmable range [4] | 0.6 | – | 30 | kΩ |
| Maximum frequency | | 200 | – | – | kHz |
| Switch on resistance | | – | 20 | 50 | Ω |
| Power-supply current | | – | 6 | 7 | µA |

**Table 3-12 Multipurpose-pin performance specifications** (cont.)

| Parameter | Comments | Min | Typ | Max | Units |
|---|---|---|---|---|---|
| ***MPP configured as analog input (analog multiplexer input)*** | | | | | |
| Input current | | – | – | 100 | µA |
| Input capacitance | | – | – | 10 | pF |
| ***MPP configured as analog output (buffered VREF output)*** [3, 5] | | | | | |
| Output voltage error | -50 µA to +50 µA | – | – | 30 | mV |
| Temperature variation | Due to buffer only; does not include VREF variation (see Table 3-6) | -0.03 | – | +0.03 | % |
| Load capacitance | | – | – | 25 | pF |
| Power-supply current | | – | 0.17 | 0.20 | mA |
| ***MPP configured as level translator*** | | | | | |
| Maximum frequency | | 4 | – | – | MHz |
| ***MPPs configured as current drivers*** [5] | | | | | |
| Power-supply voltage | | – | $V_{DD}$ | – | V |
| Output current | Programmable in 5 mA increments | 0 | – | 40 | mA |
| Output current accuracy | Any programmed current value | -20 | – | +20 | % |
| Dropout voltage | V_IN – V_OUT, with I_OUT within the accuracy limits of its current setting | – | – | 1000 | mV |
| Power supply current | Driver disabled | – | 105 | 115 | µA |

1. Input and output stages can use different power supplies, thereby implementing a level translator. See Table 2-1 for V_M supply options. Other specifications are included in Section 3.4.
2. MPP pairs are listed in Table 3-13.
3. MPPs can be configured as analog inputs; however, with no AMUX present in the PMIC, the voltage cannot be read.
4. Pullup resistance is programmable to values of 0.6 kΩ, 10 kΩ, 30 kΩ, or open.
5. Only odd MPPs (MPP_1 and MPP_3) can be configured as analog outputs. Only even MPPs (MPP_02 and MPP_04) have current sink capability.

**Table 3-13 MPP pairs**

| MPP # | | MPP # |
|---|---|---|
| 1 | <–> | 2 |
| 3 | <–> | 4 |

# 4 Mechanical Information

## 4.1 Device physical dimensions

The PM8841 is available in the 98-pin wafer-level nanoscale package (98 WLNSP) that includes dedicated ground pins for improved grounding, mechanical strength, and thermal continuity. The 98 WLNSP package has a 4.45 × 3.58 mm body with a maximum height of 0.55 mm. Pin 1 is located by an indicator mark on the top of the package, and by the ball pattern when viewed from below. A simplified version of the 98 WLNSP outline drawing is shown in Figure 4-1.

**NOTE** Click the link below to download the 98 WLNSP outline drawing (NT90-NA035-1) from the CDMA Tech Support website.

https://downloads.cdmatech.com/qdc/drl/objectId/0901001481aa6ab3

If you have permission to view the document, a prompt will be presented for initiating the download.

**NOTE** Subscribe to the package drawing to be notified of any changes.

Click the **Help** button to download the latest revision of *Using CDMA Tech Support Documents and Downloads User Guide* (80-V7273-1). This document includes subscription instructions.

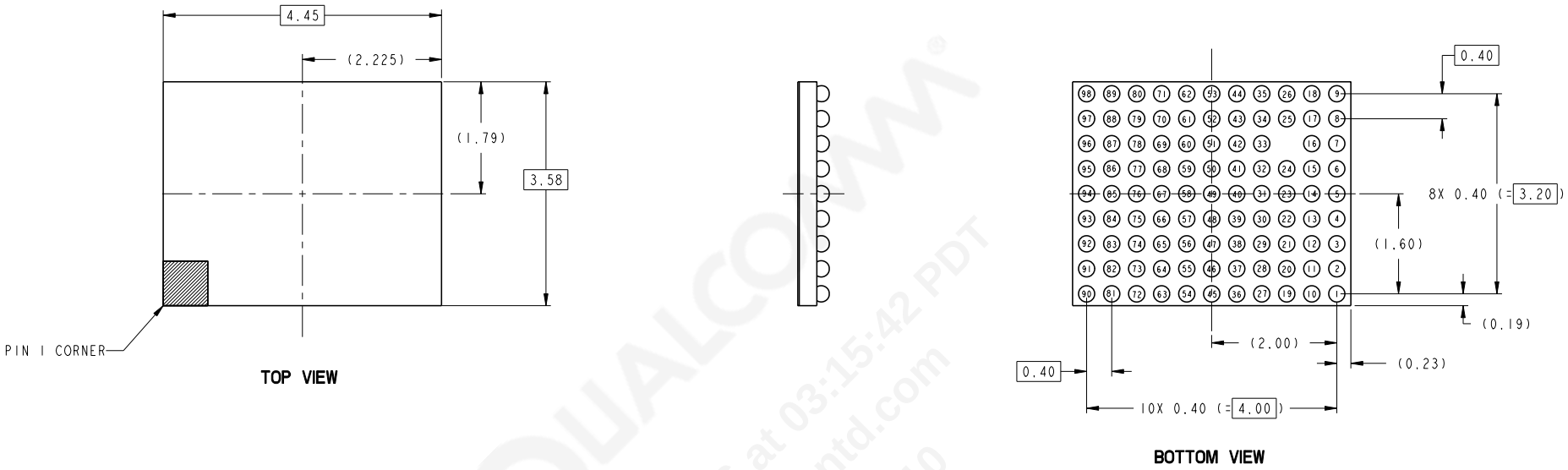



**Figure 4-1 98 WLNSP (4.45 × 3.58 × 0.55 mm) package outline drawing**

**NOTE** This is a simplified outline drawing. Click the link below to download the complete, up-to-date package outline drawing:

https://downloads.cdmatech.com/qdc/drl/objectId/0901001481aa6ab3

# 4.2 Part marking

## 4.2.1 Specification-compliant devices

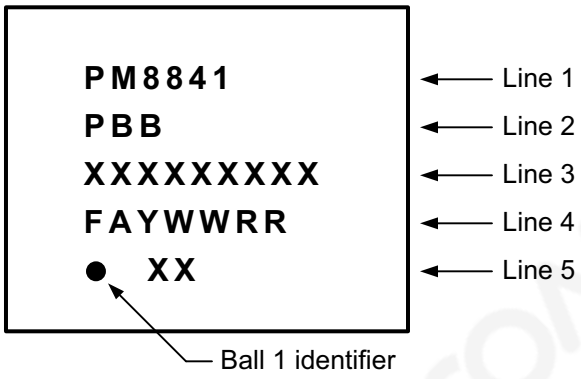



**Figure 4-2 PM8841 device marking (top view, not to scale)**

**Table 4-1 PM8841 marking line definitions**

| Line | Marking | Description |
|---|---|---|
| 1 | PM8841 | Qualcomm product name |
| 2 | PBB | P = product configuration code<br>■ See Table 4-2 for assigned values.<br>BB = feature code<br>■ See Table 4-2 for assigned values. |
| 3 | XXXXXXXXX | XXXXXXXXX = traceability information |
| 4 | FAYWWRR | F = supply source code<br>■ F = A for Global Foundries, Fab3, Singapore<br>A = assembly site code<br>■ A =<br>□ A for STATSChipPAC, SCS, Singapore<br>□ B for Amkor, ATC, China<br>Y = single-digit year<br>WW = work week (based on calendar year)<br>RR = product revision<br>■ See Table 4-2 for assigned values. |
| 5 | • XX | • = dot identifying pin 1<br>XX = traceability information |

**NOTE** For complete marking definitions of all PM8841 variants and revisions, refer to the *PM8841 Device Revision Guide* (80-NA554-4).

### 4.2.2 Daisy chain devices

This information will be included in future revisions of this document.

## 4.3 Device ordering information

### 4.3.1 Specification-compliant devices

This device can be ordered using the identification code shown in Figure 4-3 and explained below.

| Device ID code ► | AA-AAAA | — P | — CCC | DDDDD | — EE | — RR | — S | — BB |
|---|---|---|---|---|---|---|---|---|
| Symbol definition ► | Product name | Config code | Number of pins | Package type | Shipping package | Product version | Source code | Feature code |
| Example ► | PM-8841 | — 0 | — 98 | WLNSP | — TR | — 00 | — 0 | — VV |
| Feature code (BB) may not be included when identifying older devices. ↗ | | | | | | | | |

**Figure 4-3 Device identification code**

Ordering information details for all samples available to date are summarized in Table 4-2.

**Table 4-2 Device identification code/ordering information details**

| PMIC variant | P value | RR value | HW ID # | S value [1] | BB value [2] |
|---|---|---|---|---|---|
| ***ES sample type*** | | | | | |
| PM8841 ES1 | 0 | 00 | v1.0 | 0 | VV |
| PM8841 ES2 | 0 | 01 | v2.0 | 0 | VV |
| PM8841 ES3/CS | 0 | 02 | v2.1 | 0 | VV |
| Other sample types will be included in future revisions of this document. | | | | | |
| | | | | | |

1. 'S' is the source configuration code that identifies all the qualified die fabrication-source combinations available at the time a particular sample type was shipped. S values are defined in Table 4-3.
2. 'BB' is the feature code that identifies an IC's specific feature set, which distinguishes it from other versions or variants. Defined feature sets available at the time of this document's release are:
   VV = null set; all devices available at this time have the same feature set.

**Table 4-3 Source configuration code**

| S value | Die | F value = TBD | F value = TBD | F value = TBD | F value = TBD |
|---|---|---|---|---|---|
| 0 | CMOS | TBD | – | – | – |
| Other columns and rows will be added in future revisions of this document, if needed. | | | | | |
| | | | | | |

### 4.3.2 Daisy-chain devices

This information will be included in future revisions of this document.

## 4.4 Device moisture-sensitivity level

Plastic-encapsulated surface mount packages are susceptible to damage induced by absorbed moisture and high temperature. A package's moisture-sensitivity level (MSL) indicates its ability to withstand exposure after it is removed from its shipment bag, while it is on the factory floor awaiting PCB installation. A low MSL rating is better than a high rating; a low MSL device can be exposed on the factory floor longer than a high MSL device. All pertinent MSL ratings are summarized in Table 4-4.

**Table 4-4 MSL ratings summary**

| MSL | Out-of-bag floor life | Comments |
|---|---|---|
| 1 | Unlimited | ≤ 30°C/85% RH |
| 2 | 1 year | ≤ 30°C/60% RH; **PM8841 rating** |
| 2a | 4 weeks | ≤ 30°C/60% RH |
| 3 | 168 hours | ≤ 30°C/60% RH |
| 4 | 72 hours | ≤ 30°C/60% RH |
| 5 | 48 hours | ≤ 30°C/60% RH |
| 5a | 24 hours | ≤ 30°C/60% RH |
| 6 | Mandatory bake before use. After bake, must be reflowed within the time limit specified on the label. | ≤ 30°C/60% RH |

Qualcomm follows the latest IPC/JEDEC J-STD-020 standard revision for moisture-sensitivity qualification. ***The PM8841 devices are classified as MSL2; the qualification temperature was 250ºC.*** This qualification temperature (250°C) should not be confused with the peak temperature within the recommended solder reflow profile (see Section 6.2.3 for more details).

## 4.5 Thermal characteristics

Rather than provide thermal resistance values $\theta_{JC}$ and $\theta_{JA}$, validated thermal package models are provided through the CDMA Tech Support website. A thermal model for each device is provided within the *Power_Thermal* subfolder for each chipset family. Designers can extract thermal resistance values by conducting their own thermal simulations.

**NOTE** Click the link below to download the PM8841 thermal package model from the CDMA Tech Support website.

This link will be included in future revisions of this document.

If you have permission to view the document, a prompt will be presented for initiating the download.

**NOTE** Subscribe to the PM8841 thermal package model to be notified of any changes.

Click the **Help** button to download the latest revision of *Using CDMA Tech Support Documents and Downloads User Guide* (80-V7273-1). This document includes subscription instructions.

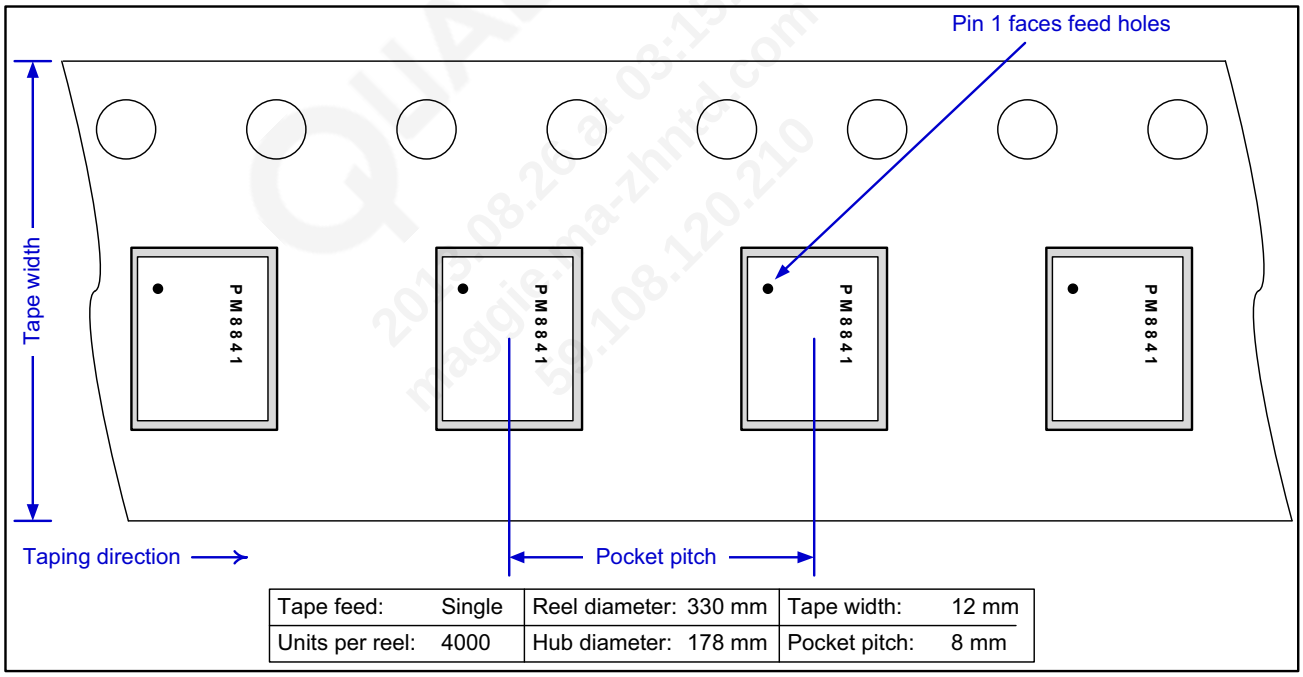
# 5 Carrier, Storage, & Handling Information

## 5.1 Carrier

### 5.1.1 Tape and reel information

All Qualcomm carrier tape systems conform to EIA-481 standards.

A simplified sketch of the PM8841 tape carrier is shown in Figure 5-1, including the proper part orientation, maximum number of devices per reel, and key dimensions.




| | | | | | |
|---|---|---|---|---|---|
| Tape feed: | Single | Reel diameter: | 330 mm | Tape width: | 12 mm |
| Units per reel: | 4000 | Hub diameter: | 178 mm | Pocket pitch: | 8 mm |

**Figure 5-1 Carrier tape drawing with part orientation**

Tape-handling recommendations are shown in Figure 5-2.

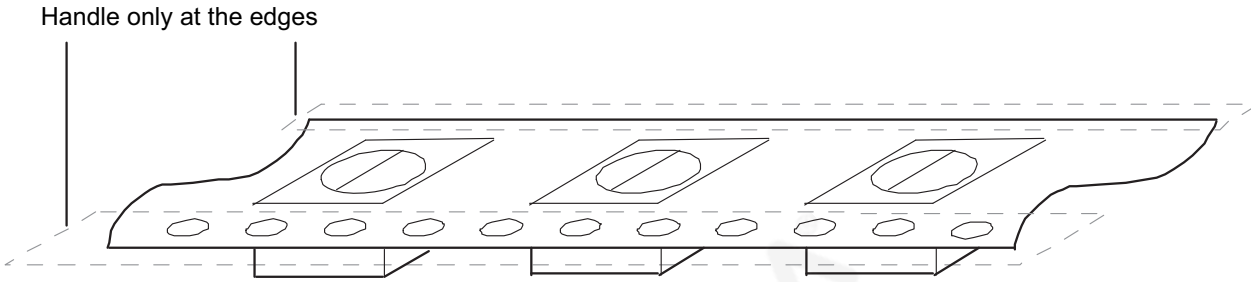



**Figure 5-2 Tape handling**

# 5.2 Storage

## 5.2.1 Bagged storage conditions

PM8841 devices delivered in tape and reel carriers must be stored in sealed, moisture barrier, anti-static bags. Refer to the *IC Packing Methods and Materials Specification* (80-VK055-1) for the expected shelf life.

## 5.2.2 Out-of-bag duration

The out-of-bag duration is the time a device can be on the factory floor before being installed onto a PCB. It is defined by the device MSL rating, as described in Section 4.4.

# 5.3 Handling

Tape handling was described in Section 5.1.1. Other (IC-specific) handling guidelines are presented below.

## 5.3.1 Baking

Wafer-level packages such as the 98 WLNSP should not be baked.

### 5.3.2 Electrostatic discharge

Electrostatic discharge (ESD) occurs naturally in laboratory and factory environments. An established high-voltage potential is always at risk of discharging to a lower potential. If this discharge path is through a semiconductor device, destructive damage may occur.

ESD countermeasures and handling methods must be developed and used to control the factory environment at each manufacturing site.

Qualcomm products must be handled according to the ESD Association standard: ANSI/ESD S20.20-1999, *Protection of Electrical and Electronic Parts, Assemblies, and Equipment*.

Refer to Section 7.1 for the PM8841 ESD ratings.

## 5.4 Barcode label and packing for shipment

Refer to the *IC Packing Methods and Materials Specification* (80-VK055-1) for all packing-related information, including barcode-label details.

# 6 PCB Mounting Guidelines

## 6.1 RoHS compliance

The device is lead-free and RoHS-compliant. Its SnAgCu solder balls use TBD composition. Qualcomm defines its lead-free (or Pb-free) semiconductor products as having a maximum lead concentration of 1000 ppm (0.1% by weight) in raw (homogeneous) materials and end products. Qualcomm package environmental programs, RoHS compliance details, and tables defining pertinent characteristics of all Qualcomm IC products are described in the *IC Package Environmental Roadmap* (80-V6921-1).

## 6.2 SMT parameters

This section describes Qualcomm board-level characterization process parameters. It is included to assist customers with their SMT process development; it is not intended to be a specification for their SMT processes.

### 6.2.1 Land pad and stencil design

The land pattern and stencil recommendations presented in this section are based on Qualcomm internal characterizations for lead-free solder pastes on an eight-layer PCB built primarily to the specifications described in JEDEC JESD22-B111.

Qualcomm recommends characterizing the land patterns according to each customer's processes, materials, equipment, stencil design, and reflow profile prior to PCB production. Optimizing the solder stencil pattern design and print process is critical to ensure print uniformity, decrease voiding, and increase board-level reliability.

General land-pattern guidelines:

- Non-solder-mask-defined (NSMD) pads provide the best reliability.
- Keep the solder-able area consistent for each pad, especially when mixing via-in-pad and non-via-in-pad in the same array.
- Avoid large solder-mask openings over ground planes.
- Traces for external routing are recommended to be less than or equal to half the pad diameter to ensure consistent solder-joint shapes.

One key parameter that should be evaluated is the ratio of aperture area to sidewall area, known as the area ratio (AR). Qualcomm recommends square apertures for optimal solder-paste release. In this case, a simple equation can be used relating the side length of the aperture to the stencil thickness (as shown and explained in Figure 6-1). Larger area ratios enable better transfer of solder paste to the PCB, minimize defects, and ensure a more stable printing process. Inter-aperture spacing should be at least as thick as the stencil; otherwise, paste deposits may bridge.

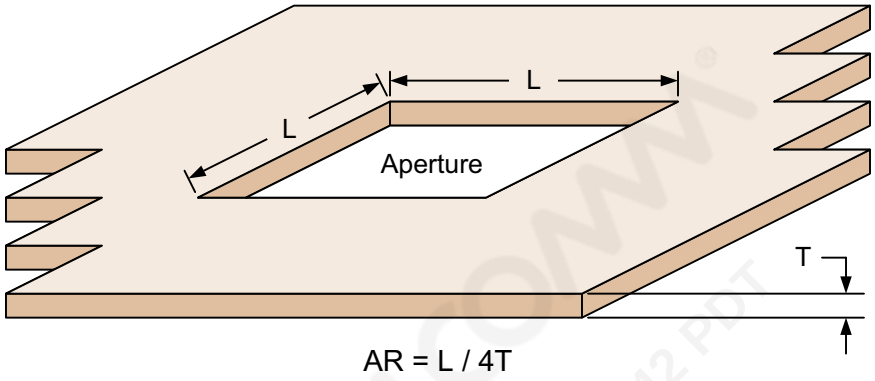



**Figure 6-1 Stencil printing aperture area ratio (AR)**

Guidelines for an acceptable relationship between L and T are listed below, and are shown in Figure 6-2:

- R = L/4T > 0.65 – best
- 0.60 ≤ R ≤ 0.65 – acceptable
- R < 0.60 – not acceptable

| Stencil Aperture L (µm) | Stencil thickness, T (µm) | | | | | | | |
|---|---|---|---|---|---|---|---|---|
| | 75 | 80 | 85 | 90 | 95 | 100 | 105 | 110 |
| 210 | 0.70 | 0.66 | 0.62 | 0.58 | 0.55 | 0.53 | 0.50 | 0.48 |
| 220 | 0.73 | 0.69 | 0.65 | 0.61 | 0.58 | 0.55 | 0.52 | 0.50 |
| 230 | 0.77 | 0.72 | 0.68 | 0.64 | 0.61 | 0.58 | 0.55 | 0.52 |
| 240 | 0.80 | 0.75 | 0.71 | 0.67 | 0.63 | 0.60 | 0.57 | 0.55 |
| 250 | 0.83 | 0.78 | 0.74 | 0.69 | 0.66 | 0.63 | 0..60 | 0.57 |
| 260 | 0.87 | 0.81 | 0.76 | 0.72 | 0.68 | 0.65 | 0.62 | 0.59 |

**Figure 6-2 Acceptable solder paste geometries**

Qualcomm provides an example PCB land pattern and stencil design for the 98 WLNSP package.

**NOTE** Click the link below to download the 98 WLNSP land/stencil drawing (LS90-NA035-1) from the CDMA Tech Support Website.

https://downloads.cdmatech.com/qdc/drl/objectId/0901001481a266be

If you have permission to view the document, a prompt will be presented for initiating the download.

**NOTE** Subscribe to the land/stencil drawing to be notified of any changes.

Click the **Help** button to download the latest revision of *Using CDMA Tech Support Documents and Downloads User Guide* (80-V7273-1). This document includes subscription instructions.

## 6.2.2 Reflow profile

Reflow profile conditions typically used by Qualcomm for lead-free systems are listed in Table 6-1 and shown in Figure 6-3.

**Table 6-1 Qualcomm typical SMT reflow-profile conditions (for reference only)**

| Profile stage | Description | Temp range | Condition |
|---|---|---|---|
| Preheat | Initial ramp | < 150°C | 3°C/sec max |
| Soak | Flux activation | 150 to 190°C | 60 to 75 sec |
| Ramp | Transition to liquids (solder-paste melting point) | 190 to 220°C | < 30 sec |
| Reflow | Time above liquidus | 220 to 245°C [1] | 50 to 70 sec |
| Cool down | Cool rate – ramp to ambient | < 220°C | 6°C/sec max |

1. During the reflow process, the recommended peak temperature is 245°C (minimum). This temperature should not be confused with the peak temperature reached during MSL testing, as described in Section 6.2.3.

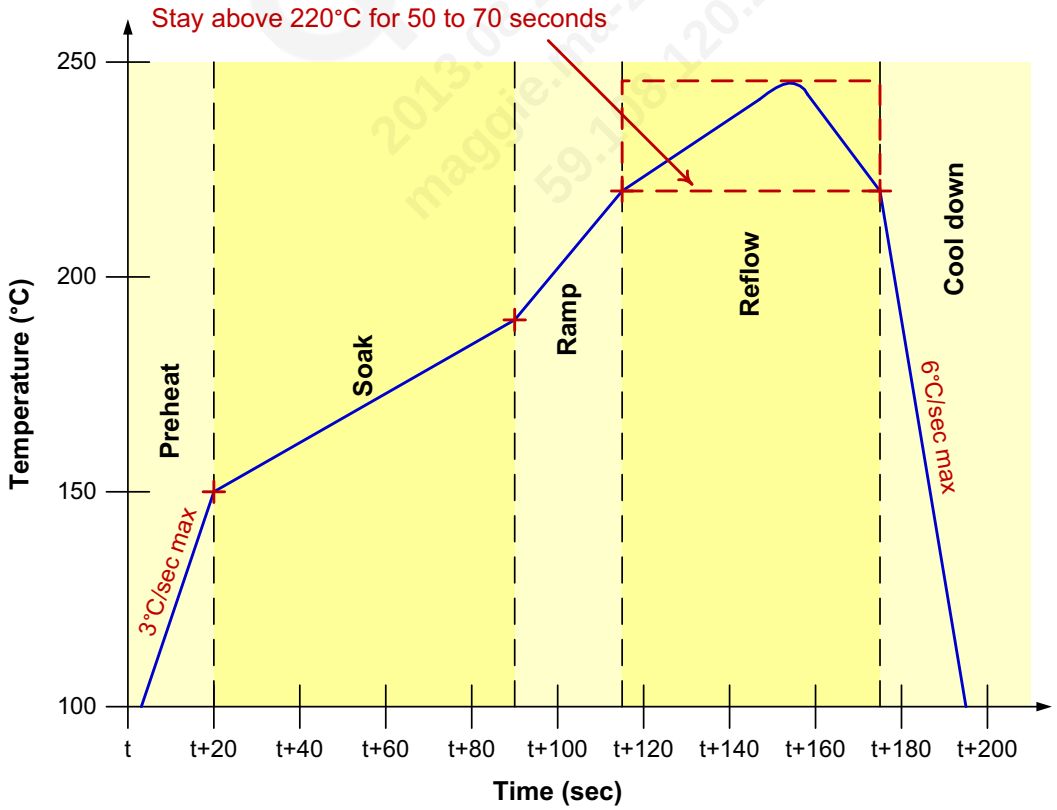



**Figure 6-3 Qualcomm typical SMT reflow profile**

### 6.2.3 SMT peak package-body temperature

This document states a peak package-body temperature in three other places within this document, and without explanation, they may appear to conflict. The three places are listed below, along with an explanation of the stated value and its meaning within that section's context.

1. Section 4.4 – *Device moisture-sensitivity level*

   PM8841 devices are classified as MSL2@250°C. The temperature (250°C) included in this designation is the lower limit of the range stated for moisture resistance testing during the device qualification process, as explained in #2 below.

2. Section 7.1 – *Reliability qualifications summary*

   One of the tests conducted for device qualification is the moisture resistance test. Qualcomm follows J-STD-020-C, and hits a peak reflow temperature that falls within the range of 260°C +0/-5°C (255°C to 260°C).

3. Section 6.2.2 – *Reflow profile*

   During a production board's reflow process, the temperature seen by the package must be controlled. Obviously, the temperature must be high enough to melt the solder and provide reliable connections, but it must not go so high that the device might be damaged. The recommended peak temperature during production assembly is 245°C. This is comfortably above the solder melting point (220°C), yet well below the proven temperature reached during qualification (250°C or more).

### 6.2.4 SMT process verification

Qualcomm recommends verification of the SMT process prior to high-volume board assembly, including:

- In-line solder-paste deposition monitoring
- Reflow profile measurement and verification
- Visual and x-ray inspection after soldering to confirm adequate alignment, solder voids, solder-ball shape, and solder bridging
- Cross-section inspection of solder joints for wetting, solder-ball shape, and voiding

## 6.3 Daisy-chain components

Daisy-chain packages use the same processes and materials as actual products; they are recommended for SMT characterization and board-level reliability testing. In fact, all SMT process recommendations discussed above can be performed using daisy-chain components.

Ordering information is given in Section 4.3.2.

Daisy-chain PCB routing recommendations are available for download.

**NOTE** Click the link below to download the 98 WLNSP daisy-chain interconnect drawing (DS90-NA035-1) from the CDMA Tech Support Website.

https://downloads.cdmatech.com/qdc/drl/objectId/0901001481a22846

If you have permission to view the document, a prompt will be presented for initiating the download.

**NOTE** Subscribe to the daisy-chain interconnect drawing to be notified of any changes.

Click the **Help** button to download the latest revision of *Using CDMA Tech Support Documents and Downloads User Guide* (80-V7273-1). This document includes subscription instructions.

## 6.4 Board-level reliability

Qualcomm conducts characterization tests to assess the device's board-level reliability, including the following physical tests on evaluation boards:

- Drop shock (JESD22-B111)
- Temperature cycling (JESD22-A104)
- Cyclic bend testing – optional (JESD22-B113)

Board-level reliability data is available for download.

**NOTE** Click the link below to download the 98 WLNSP board-level reliability data (BR80-TBD) from the CDMA Tech Support Website.

This link will be included in future revisions of this document.

If you have permission to view the document, a prompt will be presented for initiating the download.

**NOTE** Subscribe to the board-level reliability document to be notified of any changes.

Click the **Help** button to download the latest revision of *Using CDMA Tech Support Documents and Downloads User Guide* (80-V7273-1). This document includes subscription instructions.

## 6.5 High-temperature warpage

Qualcomm measures high-temperature warpage using a shadow moire system; the measured data is available for download.

**NOTE** Click the link below to download the 98 WLNSP high-temperature warpage data (WP80-TBD) from the CDMA Tech Support Website.

This link will be included in future revisions of this document.

If you have permission to view the document, a prompt will be presented for initiating the download.

**NOTE** Subscribe to the high-temperature warpage document to be notified of any changes.

Click the **Help** button to download the latest revision of *Using CDMA Tech Support Documents and Downloads User Guide* (80-V7273-1). This document includes subscription instructions.

# 7 Part Reliability

## 7.1 Reliability qualifications summary

**Table 7-1 PM8841 IC reliability evaluation**

| Tests, standards, and conditions | Sample Size | Result |
|---|---|---|
| **Average failure rate (AFR) in FIT (λ) failure in billion device-hours**<br>**HTOL:** JESD22-A108-D | 48 | 0F/48<br>ELFR = 727 DPPM<br>AFR = 16 FITs |
| **Mean time to failure (MTTF) t = 1/λ in million hours** | | 64 Mhours |
| **ESD – Human-body model (HBM) rating**<br>JESD22-A114-F | 3 | ±2000 V |
| **ESD – Charge-device model (CDM) rating**<br>JESD22-C101-D | 3 | ±500 V |
| **Latch-up (I-test):** EIA/JESD78C<br>Trigger current: ±100 mA; temperature: 85°C | 6 | ±100 mA |
| **Latch-up (Vsupply overvoltage):** EIA/JESD78<br>Trigger voltage: stress at 1.5 × Vdd max per device specification; temperature: 85°C | 6 | 6.6 V |
| **Moisture resistance test (MRT):** J-STD-020C<br>Reflow @ 260 +0/-5°C | 462 | MSL1 pass |
| **Temperature cycle:** JESD22-A104-D<br>Temperature: -55°C to 125°C; number of cycles: 1000<br>Soak time at minimum/maximum temperature: 8-10 minutes<br>Cycle rate: 2 cycles per hour (cph)<br>**Preconditioning:** JESD22-A113-F<br>MSL1, reflow @ 260 +0/-5°C | 231 | Pass |
| Unbiased highly accelerated stress test (HAST)<br>JESD22-A118; 130° C / 85% RH and 96 hrs<br>**Preconditioning:** JESD22-A113-F<br>MSL1, reflow @ 260 +0/-5°C | 231 | Pass |
| **High-temperature storage life:** JESD22-A103-C<br>Temperature = 150°C; time= 1000 hours | 231 | Pass |
| **Physical dimensions:** JESD22-B100-A | 75 | |
| **Solder ball shear**<br>JESD22-B117 | 30 | |

**Table 7-1 PM8841 IC reliability evaluation** (cont.)

| Tests, standards, and conditions | Sample Size | Result |
|---|---|---|
| **Internal/external visual**<br>Ball diameter, height & x-ray | 30 | |
| **Flammability**<br>UL-STD-94<br>Flammability test – not required | | See note. |

**Note:** Qualcomm ICs are exempt from the flammability requirements due to their sizes per UL/EN 60950-1, as long as they are mounted on materials rated V-1 or better. Most PWBs onto which our ICs mounted are rated V-0 (better than V-1).

## 7.2 Qualification sample description

### Device characteristics

Device name:PM8841

Package type:98 WLNSP

Package body size:4.45 mm × 3.58 mm × 0.55 mm

Lead count:98

Lead composition:TBD

Fab process:0.18 µm CMOS

Fab sites:GF, Fab3, Singapore;

Assembly sites:STATSChipPAC, SCS, Singapore; Amkor, ATC, China; ASE, ASE-kh, Taiwan

Solder ball pitch:0.4 mm