Qualcomm
TECHNOLOGIES, INC

PM8841 Power Management IC

Device Revision Guide

80-NA554-4 Rev. H

June 20, 2013

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Revision history

Bars appearing in the left margin (as shown here) indicate where technical changes have occurred for this revision. The following table lists the technical content changes for all revisions.

Revision	Date	Description
A	September 2012	Initial release
B	October 2012	Updated the part marking figure and description in Section 2.1 Device marking Added the feature code (BB) definition to Table 3 PM8841 device identification details Added the following issues: ■ Issue 3 Certain PMIC modules not trimmed correctly ■ Issue 4 Internal pull-down on PON_1 pin of PM8841 enabled by default
C	December 2012	Updated Issue 1 PMIC off current (IBAT_3) not meeting specification Added Issue 5 PMIC does not meet absolute maximum VPH_PWR specification and Issue 6 Multiphase FT SMPS show abnormal current balancing during phase transition
D	March 2013	Added new sample type and corresponding identification details to Table 3 Updated Table 4 to include listing of new sample type and new issues Added the following issues: ■ Issue 7 FT SMPS PFM efficiency does not meet specifications ■ Issue 8 FT SMPS can exhibit multiple switching pulses within a single switching period
E	April 22, 2013	Added a footnote in Table 3 Added the following issue: ■ Issue 9 Failure to poweron due to dVdd dip
F	April 29, 2013	Updated Table 3 and Table 4 with a new sample type
G	May 2013	Updated Table 3 with CS3/ES2 Added the following issues and updated Table 4: ■ Issue 10 Maximum off current (I_BAT3) of the PMIC out of specification at high temperature ■ Issue 11 FT SMPS stepper voltage ramp blanked during certain voltage transitions ■ Issue 12 FT SMPS voltage collapse
H	June 2013	Updated the lot number for ES3/CS parts in Table 3 footnote.

1 Introduction

Technical information for the PM8841 IC is primarily covered by the documents listed in Table 1. All documents are available from the CDMATech Support Website at https://support.cdmatech.com.

Table 1 Primary PM8841 documents

Document number	Document title
80-NA554-1	*PM8841 Device Specification (Advance Information)*
80-NA554-4 (this document)	*PM8841 Power Management IC Device Revision Guide*

1.1 Scope and intended audience

This device revision guide identifies issues with all released PM8841 samples. The following information is included:

- Introduction to this document and its topic (this chapter)
- Device identification (Chapter 2)
  - Device marking
  - Hardware revision number
  - Identification details for each sample type
  - Sample testing – engineering samples (ES) and commercial samples (CS) explanations
  - Identification of compatible software releases
- Known issues (Chapter 3)
  - Issue description
  - Impact to system performance
  - Possible workarounds (what designers should do to minimize the issue's impact)

This device revision guide is intended for new product developers who are designing, testing, or evaluating phones or terminals that include the PM8841 device.

2 Device Identification

The PM8841 device can be identified by markings on its top surface and by the contents of an identification register; these identification techniques are described in Section 2.1 and Section 2.3. Further details about each sample type are presented in Section 2.3 and Chapter 3.

2.1 Device marking

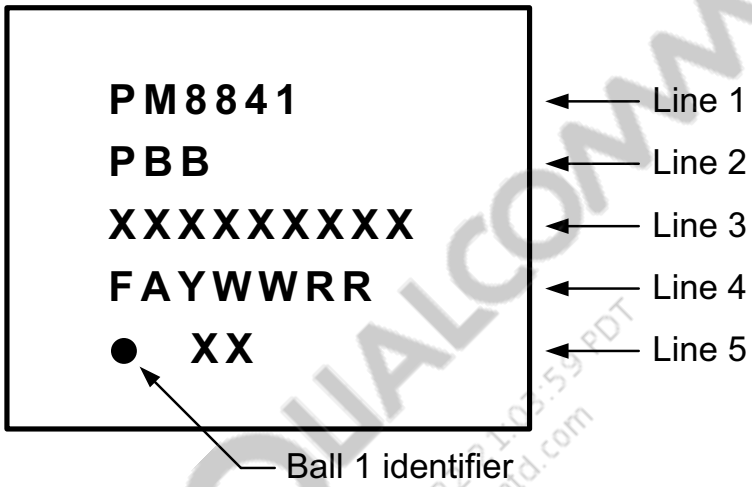

Figure 1 PM8841 device marking (top view – not to scale)

Table 2 Part marking line descriptions

Line	Marking	Description
1	PM8841	Qualcomm product name
2	PBB	P = product configuration code ■ See Table 3 for assigned values. BB = feature code ■ See Table 3 for assigned values.
3	XXXXXXXXX	XXXXXXXXX = traceability information
4	FAYWWRR	F = supply source code ■ F = A for Global Foundries, Fab3, Singapore A = assembly site code ■ A = A for StatsChipPac, SCS, Singapore ■ A = B for Amkor, ATC, China Y = single-digit year WW = work week (based on calendar year) RR = product revision ■ See Table 3 for assigned values.
5	• XX	• = dot identifying pin 1 XX = traceability information

2.2 Device identification for each sample type

This section provides details for identifying each sample type.

Table 3 PM8841 device identification details

PM8841 variant		Product configuration code (*P*)	Product revision (*RR*)	Feature code (*BB*)	Hardware revision	Known issues
PM8841	ES1	0	00	VV	v1.0	Chapter 3
PM8841	ES2	0	01	VV	v2.0[1]	Chapter 3
PM8841	ES3/CS[2]	0	02	VV	v2.1	Chapter 3

1. PM8841 v2.0 must be used with MSM8974 v2.x and PM8941 v3.0. FC or a later software build must be used with this combination of the hardware.
2. ES3/CS parts have the same PRR code. All devices with lot prefix L or WW = 19 (and later) are CS quality material.

2.3 Sample testing

2.3.1 Engineering samples (ES)

These devices have undergone limited testing and may have significant feature limitations. They are suitable to assist with printed circuit board (PCB) development, to conduct board-level electrical evaluation tests, and to explore manufacturing considerations. Engineering samples are not to be used for phone-level qualification.

2.3.2 Commercial samples (CS)

These devices have undergone full production-level testing and meet the specifications and features described in the device specification, except as otherwise noted in this document. They have passed device-level qualification. Commercial samples are suitable to be used for performance testing and phone-level production and qualification.

3 Known Issues

3.1 Summary of known issues

All known issues for each revision of the PM8841 device are summarized in Table 4. The text within the *Issue* column provides links to the sections of this document that explain the issues, regardless of the sample type (or types) on which they occur. An *X* in any of the other columns indicates that the issue occurs on the corresponding sample type.

Table 4 Known issues – all sample types and revisions [1]

#	Issue	Functional area	PM8841 P = 0 RR = 00	PM8841 P = 0 RR = 01	PM8841 P = 0 RR = 02
1	PMIC off current (IBAT_3) not meeting specification	–	X		
2	Default voltage of S3 SMPS incorrect set	HF SMPS	X		
3	Certain PMIC modules not trimmed correctly	–	X		
4	Internal pull-down on PON_1 pin of PM8841 enabled by default	Poweron	X		
5	PMIC does not meet absolute maximum VPH_PWR specification	–	X	X	
6	Multiphase FT SMPS show abnormal current balancing during phase transition	FT SMPS	X		
7	FT SMPS PFM efficiency does not meet specifications	FT SMPS	X		
8	FT SMPS can exhibit multiple switching pulses within a single switching period	FT SMPS	X	X	X
9	Failure to poweron due to dVdd dip	Poweron		X	
10	Maximum off current (I_BAT3) of the PMIC out of specification at high temperature	–			X
11	FT SMPS stepper voltage ramp blanked during certain voltage transitions	FT SMPS			X
12	FT SMPS voltage collapse	FT SMPS		X	X

1. Table 3 details *P* and *RR* values.

3.2 Issues – description, impact, and workaround

Issue 1 PMIC off current (IBAT_3) not meeting specification

Description	The off current of the PM8841 device does not meet the maximum specification of 10 µA. The measured current is about 500 µA.
Impact	The off current of the system will increase due to this issue.
Workaround	There is no workaround available for this issue. It will be fixed in a future version of the device.

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Issue 2 Default voltage of S3 SMPS incorrect set

Description	The default voltage of S3 is set to 1.15 V. Instead it should be set to 0.9 V.
Impact	There is no impact, since S3 is a default off regulator.
Workaround	Software can set the SMPS voltage to 0.9 V before enabling the SMPS. This issue will be fixed in the next version of the device.

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Issue 3 Certain PMIC modules not trimmed correctly

Description	Certain PMIC modules are not trim-optimized in the ES1 devices.
Impact	Performance specifications of the affected modules may not entirely be met.
Workaround	The optimization of the trimming test program is in progress, and will be improved in increments. Table 5 identifies the revision of the test program, the work week that the test program was implemented, and performance limitations of the devices trimmed with the test program.

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Table 5 ATE test program – performance limitations[1]

ATE test program	Work week (WW)	Performance limitation
Rev 1	35 and later	HF SMPS: ■ Auto-mode support ■ Accuracy in specification FT SMPS: ■ No auto-mode support ■ FTS voltage accuracy slightly out of specification (±2% vs. ±1% for the specification)

1. Refer to the *PM8x41 Status Update* (80-NA555-11) for more information.

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Issue 4 Internal pull-down on PON_1 pin of PM8841 enabled by default

Description	In platforms using PM8941 and PM8841, the PON_OUT pin of PM8941 is connected to the PON_1 and PS_HOLD pins of PM8841. The PON_OUT pin of PM8941 has an internal 50 kΩ series resistor. The PON_1 pin of PM8841 has an internal pull-down resistor of 200 kΩ enabled by default. During poweron, when PON_RESET_N is driven high by PM8941, PON_1 is at about 1.4 V due to this internal pull-down.
Impact	There is no system impact, except that PON_1 and PS_HOLD will be held at about 1.4 V (instead of 1.8 V) during PM8941 powerup.
Workaround	The software workaround for this issue is to disable the internal pull-down on PON_1. The PMIC will remember this value as long as a valid supply is available.

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Issue 5 PMIC does not meet absolute maximum VPH_PWR specification

Description	The absolute maximum VPH_PWR specification for PM8841 is 6 V (steady state) and 7 V (transient less than 10 ms). The current version of the device does not meet this specification. The root cause of the issue is a design-level bug that causes the device to become damaged if more than 5.8 V is applied to VDD_PON and VDD_Sx.
Impact	The impact of this issue is minimal.
Workaround	There is no workaround for this issue. This issue will be fixed in the next version of the device.

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Issue 6 Multiphase FT SMPS show abnormal current balancing during phase transition

Description	The S5, S6, S7 and S8 SMPS of the PM8841 device are multiphase FT SMPS. Depending upon the load current, either one SMPS (S5), two SMPS (S5, S6) or four SMPS (S5, S6, S7, S8) are turned on. During the phase transition, abnormal current balancing between the SMPS has been observed.
Impact	Multiphase FT SMPS cannot have certain phase transitions.
Workaround	The workaround for this issue is to turn on all of the multiphase FT SMPS and not allow phase transitions. This issue will be fixed in the next version of the device.

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Issue 7 FT SMPS PFM efficiency does not meet specifications

Description	In the current version of the device, the efficiency of the FT SMPS in the PFM mode does not meet specifications. The root cause of the issue is a design bug that needs to be fixed.
Impact	Other than additional current consumption, impact due to this issue is minimal.
Workaround	There is no workaround for this issue. This issue will be fixed in the next version of the device.

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Issue 8 FT SMPS can exhibit multiple switching pulses within a single switching period

Description	In the current version of the device, multiple switching pulses can be observed within a single switching period of the FT SMPS. The root cause of the issue is a design bug that causes the FT SMPS to exhibit multiple switching pulses within a single switching period.
Impact	System impact due to this issue is minimal, since the additional pulses do not affect the output voltage.
Workaround	There is no workaround for this issue.

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Issue 9 Failure to poweron due to dVdd dip

Description	dVdd is an internal 1.8 V infrastructure supply that is generated by the PMIC before turning on the master bandgap reference (REF_BYP) and regulators in the poweron sequence. dVdd is used to power the internal digital logic within the PMIC. It is observed that occasionally during PMIC poweron, dVdd supply dips. This causes the PMIC to fail powerup. The root cause of the issue is a design bug that will be fixed in the metal on the next version of the device (v2.1).
Impact	PMIC may fail to powerup. Empirical tests indicate that the failure rate is about 8 failures in 5000 tries.
Workaround	There is no workaround for this issue. This issue will be fixed in next version of the device (v2.1).

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Issue 10 Maximum off current (I_BAT3) of the PMIC out of specification at high temperature

Description	In PM8841 ES3/CS devices, the maximum off current (IBAT_3) does not meet the specification of 10 µA at high temperature (60°C). At cold (-30°C) and room temperature (25°C), the 10 µA specification is met.
Impact	The maximum off current (IBAT_3) of ES3/CS devices may be as high as 20 µA at high temperature (60°C). There is no impact at cold (-30°C) and room temperature (25°C).
Workaround	There is no workaround for this issue.

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Issue 11 FT SMPS stepper voltage ramp blanked during certain voltage transitions

Description	FT SMPS in PM8841 has a voltage stepper that is used to transition from one voltage to another. It is observed that the stepper may be blanked for a certain duration under the following conditions: 1. Voltage transition when FT SMPS is in HC-PFM mode (stepper is blanked for 40 µsec) 2. Voltage transition when FT SMPS is in auto mode (stepper is blanked for 80 µsec) As a result, the FT SMPS may take a longer time to reach its target voltage.
Impact	The total time taken for voltage transitions will depend upon the stepper blanking time and the actual stepping time.
Workaround	A software workaround for this issue is to do the following for voltage transitions in the above modes: 1. Change from current mode to PWM mode in the above modes. 2. Perform voltage transition. 3. Change back from PWM mode to previous mode. This workaround is implemented in software CR #490325.

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Issue 12 FT SMPS voltage collapse

Description	Certain ES2/ES3 samples can exhibit a process related defect that could cause the FT SMPS to voltage collapse as explained below. For FT SMPS, the expected response to a current limit event is to turn the PFET off and turn the NFET on for a minimum OFF time dictated by a current limit timer. In faulty devices, the current limit timer can fail to expire upon a current limit event. As a result, the SMPS will be locked in a current limit state. The switching node will be pulled to ground indefinitely, hence collapsing the output voltage. Estimated failure rate in ES3 samples is about 1800 dpm
Impact	FT SMPS may fail to power-on or may voltage collapse during load transients if current limit is hit.
Workaround	Qualcomm has implemented an ATE screen that will screen faulty devices. CS quality devices will not exhibit this issue. Please refer to note 2 of Table 3.

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