Qualcomm
TECHNOLOGIES, INC

MSM8274/MSM8674/MSM8974

Device Revision Guide

80-NA437-4 Rev. K

May 13, 2013

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Revision history

Revision	Date	Description
A	September 2012	Initial release
B	October 2012	■ Table 4: added MSM8974 ES1.1 sample ■ Table 5: added MSM8974 ES1.1 sample ■ Table 6: added MSM8974 ES1.1 sample ■ Table 8: added MSM8974 ES1.1 sample ■ Boot failure after system startup with JTAG connection: modified workaround ■ Secure boot is not fully supported: added new issue
C	December 2012	■ Table 8: added issues 11 to 15. ■ Section 3.2: added issues 11 to 15.
D	January 2013	■ Table 4: added another row on MSM8974 device identification ■ Table 7: added Peripheral SS, a new functional area ■ Table 8: added Issue 16 ■ Section 3.2 □ Updated issue 12 information □ Added issue 16
E	February 1, 2013	■ Table 8: added Issue 17: Krait L1 instruction cache error ■ Section 3.2: added Issue 17
F	March 1, 2013	■ Table 4: Added MSM8974 sample type ES2.0 and MSM8974/MSM8274/MSM8674 sample type ES2.0.1 information. Updated ES1.1 information. ■ Table 5: Added device sample type ES2.0 information ■ Table 6: Added sample type ES2.0 and ES2.0.1 information ■ Table 8: □ Added new columns for ES2.0 and ES2.0.1 □ Updated issue 7 information □ Updated issue 12 with a table footnote □ Added issues 18,19, 20, 21, and 22 ■ Section 3.2 □ Added issue 18: Display pixel corruption issue ■ Added issue 19: RFFE $V_{VIO-RST}$ specification incompliance due to VDD_P3 leakage ■ Added issue 20: Video 4K x 2K support limitation ■ Added issue 21: DDR FIFO buffer overflow ■ Added issue 22: Modem QDSP6 peak speed limitation
G	March 14, 2013	■ Updated Table 4 and Table 5: ■ Table 8: Added issue 23 ■ Added issue 23: WCN_XO clock coupling

Revision	Date	Description
H	April 10, 2013	■ Updated Table 4 with ES2.1 device variants ■ Updated Table 8 with new issues for ES2.1 devices ■ Added Krait generation information to Table 6 ■ Updated Issue 7 in Section 3.2 ■ Added Issues 24 through 27 in Section 3.2 ■ Added Section 4
J	May 2, 2013	■ Updated sample information in Table 4 (*MSM device identification details*) ■ Added ES2.1 compatible SW in Table 5 [*Software compatibility for each sample type (PRR value)*] ■ Removed Issue 22 from ES2.0/ES2.0.1 in Table 8 (*Known issues – all sample types and revisions*) ■ Updated impact/workaround for Issue 22 (*Modem QDSP6 peak speed limitation*) ■ Updated Chapter 4 (*Enhancements in Rev2.2*)
K	May 13, 2013	■ Global: added Rev2.2 sample descriptions throughout this document ■ Added the *Feature_ID* code to Table 4 (MSM device identification details) ■ Updated the Linux Android software release info for ES2.1 in Table 5 (Software compatibility for each sample type (PRR value)) ■ Changed the functional area of Issue 27 to MSS in Table 8 (*Known issues – all sample types and revisions*)

Rev. I omitted, according to Qualcomm documentation conventions

1 Introduction

Technical information for the MSM™ devices listed on the cover is contained in documents listed in Table 1 and are available for download from the CDMA Tech Support Website at https://support.cdmatech.com.

Table 1 MSM primary documents

Document number	Document title
80-NA437-1	*MSM8274/MSM8674/MSM8974 Device Specification*
80-NA437-2	*MSM8274/MSM8674/MSM8974 Software Interface*
80-NA437-4 (this document)	*MSM8274/MSM8674/MSM8974 Device Revision Guide*
80-NA437-5A	*MSM8274/MSM8674/MSM8974 Chipset Design Guidelines - Introduction*
80-NA437-5B	*MSM8274/MSM8674/MSM8974 Chipset Design Guidelines - Digital Baseband*
80-NA437-5C	*MSM8274/MSM8674/MSM8974 Chipset Design Guidelines - System Level*

1.1 Scope and intended audience

This device revision guide identifies issues with all the MSM samples released to date. The following information is included:

- Introduction to this document and its topic (Chapter 1)
- Device identification (Chapter 2)
  - Device marking
  - Hardware revision number
  - Identification details for each sample type
  - Sample testing (engineering sample (ES))
  - Identification of compatible software releases
- Known issues (Chapter 3)
  - Issue description
  - Impact to system performance
  - Possible workarounds (what designers should do to minimize the issue's impact)

This device revision guide is intended for new product developers who are designing, testing, and/or evaluating phones or terminals that include one of the MSM devices listed on the cover of this document.

2 Device Identification

MSM devices can be identified by markings on the top surface and by the contents of an identification register; these identification techniques are described in Section 2.1 and Section 2.2, respectively. Further details about each sample type are presented in Section 2.3 through Section 2.5.

2.1 Device marking

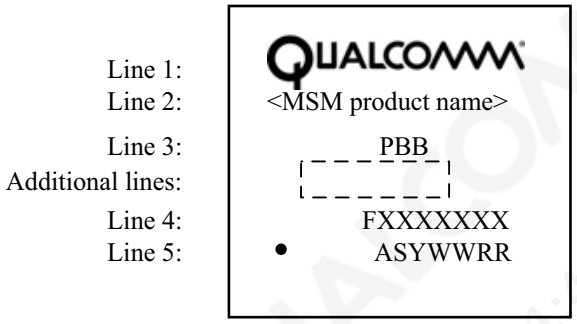

Figure 1 Device marking (top view, not to scale)

Table 2 Device marking line definitions

Line	Marking	Description
1	QUALCOMM	Qualcomm® name or logo
2	MSM8XXX	Qualcomm product name XXX = 274, 674, 974
3	PBB	P = product configuration code (see Table 4) BB = VV
4	FXXXXXXX	F = supply source code ■ F = A (for TSMC) XXXXXXX = traceability number
5	ASYWWRR	A = assembly site code ■ A = C (for Amkor K4) ■ A = K (for SPIL) ■ A = H (for SCK) S = traceability number Y = single-digit year code WW = work week (based on calendar year) RR = product revision (see Table 4)
Additional lines may appear on the part marking for some samples; this is manufacturing information that is only relevant to Qualcomm and Qualcomm suppliers.		

2.2 Hardware revision number – general format

The device identification register allows the user to determine the device's manufacturer, part number, and version via the test access port (TAP). The 32-bit device identification register is read through the JTAG interface and is summarized in Table 3.

Table 3 Device identification register

Bit location	Description	Value
bits [31:28]	Version data (may change with sample type)	0x0
bits [27:12]	Product ID/ Part number (changes with sample type)	07B0
bits [11:1]	Manufacturer identity code (administered by JEDEC)	0x070 (Qualcomm's code)
bit [0]	Device identification register start bit	Always = 1

2.3 Device identification for each sample type

Table 4 MSM device identification details

Device	Product config. code (P)	Product revision (RR)	Hardware revision number	Sample type	BB value	Feature_ID	Comments
MSM8974	0	01	0x1 07B0 0E1	ES1.0	VV	00	2 GHz Quad Krait, LTE CAT4, DC-HSPA, DOrB, TD-SCDMA, without HDCP
	0	02	0x2 07B0 0E1	ES1.1	VV	00	2 GHz Quad Krait, MLP, LTE CAT4, DC-HSPA+, DOrB, TD-SCDMA, without HDCP
	1	02	0x2 07B0 0E1	ES1.1	VV	01	2 GHz Quad Krait, MLP, LTE CAT4, DC-HSPA+, DOrB, TD-SCDMA, with HDCP
	0	02	0x2 07B0 0E1	ES1.1	VV	00	2 GHz Quad Krait, BDP, LTE CAT4, DC-HSPA+, DOrB, TD-SCDMA, without HDCP
	1	02	0x2 07B0 0E1	ES1.1	VV	01	2 GHz Quad Krait, BDP, LTE CAT4, DC-HSPA+, DOrB, TD-SCDMA, with HDCP
	0	03	0x4 07B0 0E1	ES2.0	VV	00	2 GHz Quad Krait, MLP, LTE CAT4 CA / DC-HSPA+ 42 Mbps / DOrB/ TD-SCDMA, without HDCP
	1	03	0x4 07B0 0E1	ES2.0	VV	02	2 GHz Quad Krait, MLP, LTE CAT4 CA / DC-HSPA+ 42 Mbps / DOrB / TD-SCDMA, with HDCP
	0	03	0x4 07B0 0E1	ES2.0	VV	00	2 GHz Quad Krait, BDP, LTE CAT4 CA / DC-HSPA+ 42 Mbps / DOrB / TD-SCDMA, without HDCP
	1	03	0x4 07B0 0E1	ES2.0	VV	02	2 GHz Quad Krait, BDP, LTE CAT4 CA / DC-HSPA+ 42 Mbps / DOrB / TD-SCDMA, with HDCP

Table 4 MSM device identification details (cont.)

Device	Product config. code (P)	Product revision (RR)	Hardware revision number	Sample type	BB value	Feature_ID	Comments
MSM8274	0	04	0x5 07B2 0E1	ES2.0.1	VV	00	2 GHz Quad Krait, MLP, DC-HSPA+ 42 Mbps/TD-SCDMA, without HDCP
	1	04	0x5 07B2 0E1	ES2.0.1	VV	01	2 GHz Quad Krait, MLP, DC-HSPA+ 42 Mbps/TD-SCDMA, with HDCP
	2	04	0x5 07B2 0E1	ES2.0.1	VV	02	2 GHz Quad Krait, MLP, HSPA+ 21 Mbps / TD-SCDMA, without HDCP
	3	04	0x5 07B2 0E1	ES2.0.1	VV	03	2 GHz Quad Krait, MLP, HSPA+ 21 Mbps / TD-SCDMA, with HDCP
	0	04	0x5 07B2 0E1	ES2.0.1	VV	00	2 GHz Quad Krait, BDP, DC-HSPA+ 42 Mbps / TD-SCDMA, without HDCP
	1	04	0x5 07B2 0E1	ES2.0.1	VV	01	2 GHz Quad Krait, BDP, DC-HSPA+ 42 Mbps / TD-SCDMA, with HDCP
	2	04	0x5 07B2 0E1	ES2.0.1	VV	02	2 GHz Quad Krait, BDP, DC-HSPA+ 21 Mbps / TD-SCDMA, without HDCP
	3	04	0x5 07B2 0E1	ES2.0.1	VV	03	2 GHz Quad Krait, BDP, DC-HSPA+ 21 Mbps/TD-SCDMA, with HDCP
MSM8674	0	04	0x5 07B1 0E1	ES2.0.1	VV	00	2 GHz Quad Krait, MLP, HSPA+ 21 Mbps / DOrB, without HDCP
	1	04	0x5 07B1 0E1	ES2.0.1	VV	01	2 GHz Quad Krait, MLP, HSPA+ 21 Mbps / DOrB, with HDCP
	0	04	0x5 07B1 0E1	ES2.0.1	VV	00	2 GHz Quad Krait, BDP, HSPA+ 21 Mbps / DOrB, without HDCP
	1	04	0x5 07B1 0E1	ES2.0.1	VV	01	2 GHz Quad Krait, BDP, HSPA+ 21 Mbps / DOrB, with HDCP

Table 4 MSM device identification details (cont.)

Device	Product config. code (P)	Product revision (RR)	Hardware revision number	Sample type	BB value	Feature_ID	Comments
MSM8974	0	04	0x5 07B0 0E1	ES2.0.1	VV	00	2 GHz Quad Krait, MLP, LTE CAT4 CA/DC-HSPA+ 42 Mbps / DOrB / TD-SCDMA, without HDCP
	1	04	0x5 07B0 0E1	ES2.0.1	VV	02	2 GHz Quad Krait, MLP, LTE CAT4 CA / DC-HSPA+ 42 Mbps / DOrB / TD-SCDMA, with HDCP
	6	04	0x5 07B0 0E1	ES2.0.1	VV	05	2 GHz Quad Krait, MLP, LTE CAT4 CA / DC-HSPA+ 42 Mbps / TD-SCDMA, without HDCP
	7	04	0x5 07B0 0E1	ES2.0.1	VV	06	2 GHz Quad Krait, MLP, LTE CAT4 CA / DC-HSPA+ 42 Mbps / TD-SCDMA, with HDCP
	4	04	0x5 07B0 0E1	ES2.0.1	VV	09	2 GHz Quad Krait, MLP, LTE CAT4 Non CA / DC-HSPA+ 42 Mbps / DOrB / TD-SCDMA, without HDCP
	0	04	0x5 07B0 0E1	ES2.0.1	VV	00	2 GHz Quad Krait, BDP, LTE CAT4 CA / DC-HSPA+ 42 Mbps / DOrB / TD-SCDMA, without HDCP
	1	04	0x5 07B0 0E1	ES2.0.1	VV	02	2 GHz Quad Krait, BDP, LTE CAT4 CA / DC-HSPA+ 42 Mbps / DOrB / TD-SCDMA, with HDCP
	6	04	0x5 07B0 0E1	ES2.0.1	VV	05	2 GHz Quad Krait, BDP, LTE CAT4, CA / DC-HSPA+ 42 Mbps / TD-SCDMA, without HDCP
	7	04	0x5 07B0 0E1	ES2.0.1	VV	06	2 GHz Quad Krait, BDP, LTE CAT4, CA / DC-HSPA+ 42 Mbps / TD-SCDMA, with HDCP
	4	04	0x5 07B0 0E1	ES2.0.1	VV	09	2 GHz Quad Krait, BDP, LTE CAT4 Non CA / DC-HSPA+ 42 Mbps / DOrB / TD-SCDMA, without HDCP
MSM8974	5	04	0x5 07B0 0E1	ES2.0.1	VV	0A	2 GHz Quad Krait, BDP, LTE CAT4 Non CA / DC-HSPA+ 42 Mbps / DOrB / TD-SCDMA, without HDCP
	8	04	0x5 07B0 0E1	ES2.0.1	VV	0C	2 GHz Quad Krait, BDP, LTE CAT4 Non CA / DC-HSPA+ 42 Mbps / TD-SCDMA, without HDCP
	9	04	0x5 07B0 0E1	ES2.0.1	VV	0B	2 GHz Quad Krait, BDP, LTE CAT4 Non CA / DC-HSPA+ 42 Mbps / TD-SCDMA, with HDCP

Table 4 MSM device identification details (cont.)

Device	Product config. code (P)	Product revision (RR)	Hardware revision number	Sample type	BB value	Feature_ID	Comments
MSM8274	0	05	0x6 07B2 0E1	ES2.1	VV	00	2.2 GHz Quad Krait, BDP, DC-HSPA+ 42 Mbps / TD-SCDMA without HDCP
	1	05	0x6 07B2 0E1	ES2.1	VV	01	2.2 GHz Quad Krait, BDP, DC-HSPA+ 42 Mbps / TD-SCDMA with HDCP
	2	05	0x6 07B2 0E1	ES2.1	VV	02	2.2 GHz Quad Krait, BDP, HSPA+ 21 Mbps / TD-SCDMA without HDCP
	3	05	0x6 07B2 0E1	ES2.1	VV	03	2.2 GHz Quad Krait, BDP, HSPA+ 21 Mbps / TD-SCDMA with HDCP
MSM8674	0	05	0x6 07B1 0E1	ES2.1	VV	00	2.2 GHz Quad Krait, BDP, HSPA+ 21 Mbps / DOrB without HDCP
	1	05	0x6 07B1 0E1	ES2.1	VV	01	2.2 GHz Quad Krait, BDP, HSPA+ 21 Mbps / DOrB with HDCP
MSM8974	0	05	0x6 07B0 0E1	ES2.1	VV	00	2.2 GHz Quad Krait, MLP, LTE CAT4 CA / DC-HSPA+ 42 Mbps / DOrB / TD-SCDMA without HDCP
	4	05	0x6 07B0 0E1	ES2.1	VV	09	2.2 GHz Quad Krait, MLP, LTE CAT4 Non CA/DC-HSPA+ 42 Mbps / DOrB / TD-SCDMA without HDCP
	8	05	0x6 07B0 0E1	ES2.1	VV	0C	2.2 GHz Quad Krait, MLP, LTE CAT4 Non-CA / DC-HSPA+ 42 Mbps / TD-SCDMA without HDCP
	9	05	0x6 07B0 0E1	ES2.1	VV	0B	2.2 GHz Quad Krait, MLP, LTE CAT4 Non-CA / DC-HSPA+ 42 Mbps / TD-SCDMA with HDCP
	0	05	0x6 07B0 0E1	ES2.1	VV	00	2.2 GHz Quad Krait, BDP, LTE CAT4 CA / DC-HSPA+ 42 Mbps / DOrB / TD-SCDMA without HDCP
	1	05	0x6 07B0 0E1	ES2.1	VV	02	2.2 GHz Quad Krait, BDP, LTE CAT4 CA / DC-HSPA+ 42 Mbps / DOrB / TD-SCDMA with HDCP
	4	05	0x6 07B0 0E1	ES2.1	VV	09	2.2 GHz Quad Krait, BDP, LTE CAT4 Non CA / DC-HSPA+ 42 Mbps / DOrB / TD-SCDMA without HDCP
	5	05	0x6 07B0 0E1	ES2.1	VV	0A	2.2 GHz Quad Krait, BDP, LTE CAT4 Non CA / DC-HSPA+ 42 Mbps / DOrB / TD-SCDMA with HDCP
	6	05	0x6 07B0 0E1	ES2.1	VV	05	2.2 GHz Quad Krait, BDP, LTE CAT4 CA / DC-HSPA+ 42 Mbps / TD-SCDMA without HDCP
	7	05	0x6 07B0 0E1	ES2.1	VV	06	2.2 GHz Quad Krait, BDP, LTE CAT4 CA / DC-HSPA+ 42 Mbps / TD-SCDMA with HDCP

Table 4 MSM device identification details (cont.)

Device	Product config. code (P)	Product revision (RR)	Hardware revision number	Sample type	BB value	Feature_ID	Comments
MSM8974	8	05	0x6 07B0 0E1	ES2.1	VV	0C	2.2 GHz Quad Krait, BDP, LTE CAT4 Non-CA / DC-HSPA+ 42 Mbps / TD-SCDMA without HDCP
	9	05	0x6 07B0 0E1	ES2.1	VV	0B	2.2 GHz Quad Krait, BDP, LTE CAT4 Non-CA / DC-HSPA+ 42 Mbps / TD-SCDMA with HDCP
MSM8274	0	06	0x7 07B2 0E1	Rev2.2	VV	00	2.2 GHz Quad Krait, BDP, DC-HSPA+ 42 Mbps / TD-SCDMA without HDCP
	1	06	0x7 07B2 0E1	Rev2.2	VV	01	2.2 GHz Quad Krait, BDP, DC-HSPA+ 42 Mbps / TD-SCDMA with HDCP
	2	06	0x7 07B2 0E1	Rev2.2	VV	02	2.2 GHz Quad Krait, BDP, HSPA+ 21 Mbps / TD-SCDMA without HDCP
	3	06	0x7 07B2 0E1	Rev2.2	VV	03	2.2 GHz Quad Krait, BDP, HSPA+ 21 Mbps / TD-SCDMA with HDCP
MSM8674	0	06	0x7 07B1 0E1	Rev2.2	VV	00	2.2 GHz Quad Krait, BDP, HSPA+ 21 Mbps / DOrB without HDCP
	1	06	0x7 07B1 0E1	Rev2.2	VV	01	2.2 GHz Quad Krait, BDP, HSPA+ 21 Mbps / DOrB with HDCP

Table 4 MSM device identification details (cont.)

Device	Product config. code (P)	Product revision (RR)	Hardware revision number	Sample type	BB value	Feature_ID	Comments
MSM8974	0	06	0x7 07B0 0E1	Rev2.2	VV	00	2.2 GHz Quad Krait, MLP, LTE CAT4 CA / DC-HSPA+ 42 Mbps / DOrB / TD-SCDMA without HDCP
	4	06	0x7 07B0 0E1	Rev2.2	VV	09	2.2 GHz Quad Krait, MLP, LTE CAT4 Non CA / DC-HSPA+ 42 Mbps / DOrB / TD-SCDMA without HDCP
	8	06	0x7 07B0 0E1	Rev2.2	VV	0C	2.2 GHz Quad Krait, MLP, LTE CAT4 Non CA / DC-HSPA+ 42 Mbps / TD-SCDMA without HDCP
	9	06	0x7 07B0 0E1	Rev2.2	VV	0B	2.2 GHz Quad Krait, MLP, LTE CAT4 Non CA / DC-HSPA+ 42 Mbps / TD-SCDMA with HDCP
	0	06	0x7 07B0 0E1	Rev2.2	VV	00	2.2 GHz Quad Krait, BDP, LTE CAT4 CA / DC-HSPA+ 42 Mbps / DOrB / TD-SCDMA without HDCP
	1	06	0x7 07B0 0E1	Rev2.2	VV	02	2.2 GHz Quad Krait, BDP, LTE CAT4 CA / DC-HSPA+ 42 Mbps / DOrB / TD-SCDMA with HDCP
	4	06	0x7 07B0 0E1	Rev2.2	VV	09	2.2 GHz Quad Krait, BDP, LTE CAT4 Non CA / DC-HSPA+ 42 Mbps / DOrB / TD-SCDMA without HDCP
	5	06	0x7 07B0 0E1	Rev2.2	VV	0A	2.2 GHz Quad Krait, BDP, LTE CAT4 Non CA / DC-HSPA+ 42 Mbps / DOrB / TD-SCDMA with HDCP
	6	06	0x7 07B0 0E1	Rev2.2	VV	05	2.2 GHz Quad Krait, BDP, LTE CAT4 CA / DC-HSPA+ 42 Mbps / TD-SCDMA without HDCP
	7	06	0x7 07B0 0E1	Rev2.2	VV	06	2.2 GHz Quad Krait, BDP, LTE CAT4 CA / DC-HSPA+ 42 Mbps / TD-SCDMA with HDCP
	8	06	0x7 07B0 0E1	Rev2.2	VV	0C	2.2 GHz Quad Krait, BDP, LTE CAT4 Non-CA / DC-HSPA+ 42 Mbps / TD-SCDMA without HDCP
	9	06	0x7 07B0 0E1	Rev2.2	VV	0B	2.2 GHz Quad Krait, BDP, LTE CAT4 Non CA / DC-HSPA+ 42 Mbps / TD-SCDMA with HDCP

2.4 Sample testing

2.4.1 Engineering samples (ES)

These devices have undergone limited testing and sometimes have significant feature limitations. They are suitable to assist with PCB development, to conduct board-level electrical evaluation tests, and to explore manufacturing considerations. Engineering samples are not to be used for phone-level qualification.

2.5 Compatible software releases

Each sample type is for use with a particular AMSS 8974 software version (or later). They are not expected to be compatible with AMSS software releases that occurred earlier than that particular version. Table 5 identifies the software compatibility of each sample type.

Table 5 Software compatibility for each sample type (PRR value)

MSM device sample	PRR[1]	Compatible software			Comments
		Windows Phone 8	QNX	Linux Android	
ES1.0	001	M8974AAAAANWAD1011 or later	M8974AAAAANQZD1010.4 or later	M8974AAAAANLYD1010 or later	–
ES1.1	002	M8974AAAAANWZD1013.2 or later	M8974AAAAANQZD1010.4 or later	M8974AAAAANLYD1011 or later	–
ES2.0	003	M8974AAAAANWZD1021 or later	M8974AAAAANQAD1014 or later	M8974AAAAANLYD1020 or later	MSM8974 ES2.0 sample should be used **only** with PM8941 ES3 and PM8841 ES2
ES2.0.1	004	M8974AAAAANWZD1021 or later	M8974AAAAANQAD1014 or later	M8974AAAAANLYD1020 or later	MSM8974 ES2.0.1 sample should be used **only** with PM8941 ES3 and PM8841 ES2
ES2.1	005	M8974AAAAANWZD1023.3 or later	M8974AAAAANQAD1016 or later	M8974AAAAANLYD1022 or later	
Rev2.2	006	TBD	TBD	TBD	

1. Only one PRR variant is shown per sample as example. Refer to Table 4 for the full list of available PRR codes.

3 Known Issues

3.1 Summary of known issues

All known issues for each revision of the MSM8974 device and its variants are summarized in Table 8. The text within the *Issue* column provides links to the sections of this document that explain the issues, regardless of the sample type (or types) on which they occur. An *X* in any of the other columns indicates that the issue occurs on the corresponding sample type. Absence of an X indicates the issue does not apply to the corresponding sample type. For Krait processor errata, see the *Krait Processor Family Errata Document* (80-N6565-1) for more information. Table 6 lists the sample type version and Krait processor version.

Table 6 Sample type vs. Krait processor

Sample type	Krait processor	Generation
ES1.0; ES1.1	KR28M4B10	Pass 3
ES2.0; ES2.0.1; ES2.1; Rev2.2	KR28M4B20	Pass 4

Table 7 Functional area description

Functional area	Description
MSS	Modem subsystem
WCSS	Wireless connectivity subsystem
MMSS	Multimedia subsystem
KPSS	Krait processor subsystem
QDSS	Qualcomm debug subsystem
LPASS	Low power audio subsystem
Peripheral SS	Peripheral subsystem
General	General area

Table 8 Known issues – all sample types and revisions [1]

#	Issue	Functional area See Table 7	ES					
			MSM8974 ES1.0	MSM8974 ES1.1	MSM8974 ES2.0	MSM8974 ES2.0.1	MSM8974 ES2.1	MSM8974 Rev2.2
			P = 0	P = 0	P = 0,1	P = 0,1	P = x	P = x
			RR = 01	RR = 02	RR = 03	RR = 04	RR = 05	RR = 06
1	Modem Digital-to-Analog Converter (DAC) performance degradation	MSS	X		–	–	–	–
2	Camera MCLK frequency limitation	MMSS	X	X	–	–	–	–
3	DAP clock frequency limitation for ATB funnel in KPSS	QDSS	X	X	–	–	–	–
4	USB trace bandwidth limitation	QDSS	X	X	–	–	–	–
5	Debug feature disablement issue	Security	X	X	–	–	–	–
6	Boot failure after sys.up with JTAG connection	QDSS	X	X	–	–	–	–
7	Krait CPU core speed limitation	KPSS	X	X	X	X	X	X
8	Video core decode performance limitation	MMSS	X	X	–	–	–	–
9	LPDDR3 operation at lower voltages are not verified	General	X	X	–	–	–	–
10	Secure boot is not fully supported	General	X	X	–	–	–	–
11	Krait level 2 cache issue	KPSS	X	X	–	–	–	–
12	Process voltage setting (PVS) not enabled[2]	KPSS	X	X	–	–	–	–
13	GPU hangs during boot up	MMSS	X	X	–	–	–	–
14	OCIMEM retention issue	General	X	X	–	–	–	–
15	MIPI DSI maximum rate issue	MMSS	X	X	–	–	–	–
16	Low throughput for USB 2.0 and HSIC transactions while using USB 2.0 controller	Peripheral SS	X	X	–	–	–	–
17	Krait L1 instruction cache error	KPSS	X	X	–	–	–	–
18	Display pixel corruption issue	MMSS	X	X	X	–	–	–
19	RFFE $V_{VIO-RST}$ specification incompliance due to VDD_P3 leakage	General	X	X	X	X	X	X
20	Video 4K x 2K support limitation	MMSS	X	X	X	X	X	X

Table 8 Known issues – all sample types and revisions [1] (cont.)

#	Issue	Functional area See Table 7	ES					
			MSM8974 ES1.0	MSM8974 ES1.1	MSM8974 ES2.0	MSM8974 ES2.0.1	MSM8974 ES2.1	MSM8974 Rev2.2
			P = 0	P = 0	P = 0,1	P = 0,1	P = x	P = x
			RR = 01	RR = 02	RR = 03	RR = 04	RR = 05	RR = 06
21	DDR FIFO buffer overflow	General	–	–	X	X	–	–
22	Modem QDSP6 peak speed limitation	MSS	–	–	–	–	–	–
23	WCN_XO clock coupling	WCNSS	–	–	X	X	X	–
24	QDSP6 security	Security	–	–	–	–	X	–
25	PDN optimization	General	X	X	X	X	X	–
26	GPU enhancement	GFX	X	X	X	X	X	–
27	TDD-LTE 15 MHz 4x2 MIMO not supported	MSS	X	X	X	X	X	–

1. *P* and *RR* values are detailed in Table 4.
2. PVS is enabled for the ES1.1 devices with date code YWW = 304 and later. YWW code is shown in Section 2.1.

3.2 Issues – description, impact, and workaround

Issue 1 Modem Digital-to-Analog Converter (DAC) performance degradation

Description	Layout error in modem DAC produces a short in the capacitor and results in a small jump in the DAC output.
Impact	RF performance will be degraded with the following projection: ■ Rx noise goes up by 10 – 15 dB. ■ RF desense of the receiver by 3 dB.
Workaround	No workaround at this time but the hardware fix will be available in the next revision of the MSM device with ES1.1.

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Issue 2 Camera MCLK frequency limitation

Description	Due to the incorrect clock divider cell used, the MSM may not generate right clock frequencies for the MCLK for camera sensors.
Impact	Only certain specific MCLK frequency will be generated and intended frequency may not be generated.
Workaround	Board level reworks of adding test points for the GP_CLK GPIOs (26, 27, 57, 58, 59) for MCLKs to get appropriate MCLK frequencies. The hardware fix will be available in the future revision of the MSM device with ES2.0.

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Issue 3 DAP clock frequency limitation for ATB funnel in KPSS

Description	The ATB funnel in KPSS uses the DAP clock (150 MHz) instead of the expected ATB clock (240 MHz).
Impact	Cannot trace four Krait cores in cycle accurate mode or in non-cycle accurate mode at 2.3 GHz, but can trace four Krait cores in non-cycle accurate mode at 1.8 GHz.
Workaround	No workaround at this time, but plan to fix on future hardware revision with ES2.0.

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Issue 4 USB trace bandwidth limitation

Description	USB trace bandwidth cut to 1.5 Gbps under host burst-to-burst delay as demonstrated by the NEC host, 2 Gbps might not be met.
Impact	The best settings in SW for this scenario are to be shared later. This is burst size of 3 for the DBM end point.
Workaround	No workaround at this time, but plan to fix on future hardware revision with ES2.0.

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Issue 5 Debug feature disablement issue

Description	A limitation in the debug features disable mechanism might unintentionally expose information contained in these disabled features.
Impact	In very rare instances, debug information that has been disabled properly could still be available to the user.
Workaround	No workaround at this time, but plan to fix on future hardware revision with ES2.0.

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Issue 6 Boot failure after sys.up with JTAG connection

Description	Security controller AHB2AHB bridge does not get full reset when SRST_N or QDSS_SRST_N fire.
Impact	Potential boot up failure might be observed with JTAG connection but not a normal boot up issue.
Workaround	The workaround is to disable the Security Control XPU in the TrustZone.

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Issue 7 Krait CPU core speed limitation

Description	Krait CPU core will not run up to 2.3 GHz in the ES1.x and ES2.x sample MSM8974 device.
Impact	The Krait CPU core will run up to 1.7 GHz on the ES1.x sample, up to 2.0 GHz on the ES2.0/2.0.1 samples and up to 2.2 GHz on ES2.1 and later samples of the MSM8974 device.
Workaround	Not applicable with the 2.2 GHz plan.

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Issue 8 Video core decode performance limitation

Description	Video core will not provide 120 fps at 1080p for decoding.
Impact	Video core will provide 96 fps at 1080p for decoding with the ES1.0 sample MSM8974 device.
Workaround	120 fps at 1080p for decoding on future hardware revision of the MSM device with ES2.0.

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Issue 9 LPDDR3 operation at lower voltages are not verified

Description	LPDDR3 verification at lower voltages are yet to be completed.
Impact	None.
Workaround	VDD_EBI will be set at 0.945 V at this early stage in software until verification and validation are completed in the lower voltage conditions.

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Issue 10 Secure boot is not fully supported

Description	Modem boot authenticator (MBA) image cannot be authenticated by modem BootROM as part of secure boot in the MSM device with ES1.x.
Impact	Secure boot cannot be fully verified without BootROM patch.
Workaround	The BootROM patch is planned to be in the future revision of the MSM device with ES2.0.

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Issue 11 Krait level 2 cache issue

Description	On some devices, during Android boot, the operating system panics due to a double bit – an incorrigible data error in the Krait level 2 cache.
Impact	The temporary software workaround will increase power consumption (due to the increased voltage and frequency) ■ With the current ES software, the power impact of the workaround will vary with the specific use-case. ■ With fully optimized CS software: □ Low power use-cases (standby, voice, audio playback etc.) will not see any power increases. □ Medium power use-cases (HSDPA, LTE Cat 3/Cat 4, SVLTE Cat 2, 3D gaming) will see up to 8% power increases.
Workaround	The MSM8974 chipset ES1.1 samples are robust if the software avoids intermediate L2 frequency ranges and sets the Vdd_Mx to 1.05 V. The software workaround is available in the software ES3 release with these changes: ■ Avoid lowering Vdd_Mx below 1.05 VPMIC setting at any time. ■ Avoid a range of L2 clock frequencies between 300 MHz and 1500 MHz.

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Issue 12 Process voltage setting (PVS) not enabled

Description	The process voltage scaling (PVS) has not been fully enabled in the ES devices. A fully enabled PVS ensures optimum supply voltage settings based on device characteristics. However these ES devices are all programmed with PVS = 0b000.
Impact	The devices without PVS fully enabled may have a range of performance issues caused by excessive power consumption and thermal issues including but not limited to “failure to boot properly”; therefore, these devices should not be used for thermal testing, current consumption analysis, or high load (benchmark) testing.
Workaround	The devices without PVS fully enabled can be used for board bring up and software development but may require external thermal mitigation methods including heat spreader, to ensure the maximum case temperature is not exceeded. The thermal mitigation algorithm must also be enabled, but this alone may not be sufficient if the thermal issues occur during boot. Note: This document will be updated with the corresponding date code of devices once PVS is fully enabled.

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Issue 13 GPU hangs during boot up

Description	The GPU may hang during boot up. Turning the clocks on and off causes glitches in the GPU command processor and the command stream reads invalid data resulting in a GPU hang.
Impact	Potential boot up or operational failure due to the GPU hang
Workaround	The fix is to turn off the dynamic debug clock (CP_DEBUG=DYNAMIC_CLK_OFF) that is available in the software ES3.0 release onwards.

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Issue 14 OCIMEM retention issue

Description	OCIMEM on the MSM8974 chipset could be corrupted after reset.
Impact	If the software sets the OCIMEM to the SBL download mode, ram dump may not be guaranteed as expected due to the OCIMEM retention issue.
Workaround	Some memory from the RPM MsgRAM for shared IMEM contents must be retained through resets. This issue will be fixed on the future hardware revision of the MSM device with the ES2.0 chipset.

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Issue 15 MIPI DSI maximum rate issue

Description	The DSI maximum rate could be limited.
Impact	The DSI maximum rate cannot meet 1.5 Gbps/lane due to the insufficient size of the Tclk_pre counter in the DSI controller.
Workaround	There is no workaround at this time; however, the risk level is considered to be low arising due to this limitation since most of the panels do not support greater than 1 Gbps/lane. This issue will be fixed on the future hardware revision of the MSM device with the ES2.0 chipset.

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Issue 16 Low throughput for USB 2.0 and HSIC transactions while using USB 2.0 controller

Description	The peripheral NOC for USB 2.0 treats any bus transaction as single while writing to DDR3; there is a bus turn around delay per 32 bit. This causes potential throughput issue on USB 2.0 transactions.
Impact	There is a minor impairment for USB HS throughput only when using the USB 2.0 controller.
Workaround	A software workaround is available for LA in the ES1.0 and ES1.1 devices. There is no impact on the USB 3.0 controller throughput. Enable bufferable writes on the AHB master interface of USB 2.0 with system delay adjustment. This issue will be fixed in the chipset ES2.0 sample device.

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Issue 17 Krait L1 instruction cache error

Description	There is a feature in the prefetch engine that permits a demand fetch miss to “take over” an L1 I-cache line fill buffer that may already be busy processing a speculatively-generated next sequential line fill prefetch operation. Under certain obscure circumstances, the Krait core program execution may become corrupted. This corruption may include L1 instruction cache parity errors and/or a hang condition, as well as generalized corruption of the instruction stream. Refer to *Errata 42* in *Krait Processor Family Errata Document* (80-N6565-1 Rev. H or later) for details.
Impact	The most common symptom of this error is a software-controlled crash with the message **L1 i-cache parity error**. Other symptoms, such as APSS related watchdog timeout due to inter-CPU interaction and DALVIK crash, were also observed. The reproducibility of the problem occurred approximately one instance in every 48 to 72 hours while testing eight devices during regular product testing, such as MTBF. A special back-to-back reboot test was able to accelerate the occurrence of the failure to approximately one instance within 10 hours while testing eight devices.
Workaround	The software workaround (CR#447709) partially disables the L1 I-cache prefetching engine such that the ability for a demand fetch miss to “take over” a prefetch's L1 I-cache line fill buffer is disabled. This simple workaround minimizes the performance impact as it allows the L1 I-cache prefetching engine to remain enabled, while only disabling the “take over” mechanism. The number of scenarios where the “take over” mechanism increases performance is very limited.

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Issue 18 Display pixel corruption issue

Description	The multicycle timing constraint impacts the read and write timing in the shared memory pool in MDP. This requires a minor silicon change on the MSM8974.
Impact	When the MDP operates at maximum frequency, it can result in some display resolution issues (corrupt pixels). However, there is no hang issue or crash expected.
Workaround	This will be fixed in the new MSM8974 ES2.0.1 sample release that recovers frequency drop. There is no impact on CS silicon or timing due to this issue.

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Issue 19 RFFE $V_{VIO-RST}$ specification incompliance due to VDD_P3 leakage

Description	The MIPI RFFE specification requires VIO supply reset voltage level < 0.2 V when the RFFE device is in the reset mode. Due to the MSM chipset’s internal leakages, the voltage on the VREG_S3A rail that powers VIO of the RFFE devices could see approximately 450 mV before it is turned on.
Impact	There are no failures or performance impacts observed on the Qualcomm test platforms because of this specification violation. However, note that not all RFFE parts are tested by Qualcomm.
Workaround	The *RFFE Vendor Specification* (80-N7876-1) has been updated with recommendation to the vendors to tolerate up to 450 mV when the device is in the reset mode. If an RFFE device that is not tolerant to 450mV is used while in the reset mode, it is recommended to add a stuff option for a load switch controlled by the MSM_RESOUT_N on VREG_S3A to gate the power supply to the RFFE devices until VREG_S3A is turned on.

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Issue 20 Video 4K x 2K support limitation

Description	The MSM8974 chipset will not support a frame width of 4096 x 2160.
Impact	The MSM8974 chipset CS sample will only support 3840 x 2160 maximum resolution across all operating systems (most common 4k format).
Workaround	There is no workaround planned for the CS sample for this issue. Only a frame width of 3840 x 2160 will be supported.

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Issue 21 DDR FIFO buffer overflow

Description	A combination of the worst case MSM (slow part + low voltage) and worst case memory may encounter buffer overflows causing DDR corruption for certain read patterns.
Impact	A DDR corruption is expected for certain read patterns.
Workaround	A temporary software workaround will be added for ES2.0/2.0.1 that adds extra cycles between bursts of reads so FIFO will not overrun ensuring specification compliance. This issue will be fixed in the hardware on the ES2.1 chipset sample.

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Issue 22 Modem QDSP6 peak speed limitation

Description	QDSP6 of the modem subsystem does not achieve full projected speed at all voltages on the ES2.0 and ES2.0.1 samples.
Impact	This issue has no impact.
Workaround	Not applicable. This issue is obsolete; there is no limitation.

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Issue 23 WCN_XO clock coupling

Description	There is significant substrate coupling between WCN_XO (24 MHz) and the WLAN_BB_I/Q output lines of the MSM8x74 device. This causes 24 MHz spurs on the WCN3680 WLAN Tx.
Impact	The spurs can cause degradation in the WLAN performance resulting in failure to meet IEEE spectral mask and Tx EVM specifications.
Workaround	A board level workaround is to reduce the voltage swing of the WCN_XO clock from 1.8 V to 400 mV which can result in significant reduction of the Tx spur, to a point where the performance impact is negligible. The circuit has been added in the *MSM8274/MSM8274AB, MSM8674/MSM8674AB, and MSM8974/MSM8974AB Baseband Reference Schematic* (80-NA437-41 Revision H and later). This has been fully verified. *MSM8974 24 MHz Clock Coupling Application Note* (80-NA437-11) provides the assessment for the reduced swing on the WCN_XO pin. Rev2.2 MSM devices will have improved EVM through its substrate level fix. With Rev2.2 MSM devices, the board level workaround is recommended to be removed.

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Issue 24 QDSP6 security

Description	Limitation in debug disable mechanism prevents OEM from disabling QDSP6 debug access via JTAG. Qualcomm is required to disable QDSP6 debug access as part of Qualcomm manufacture process.
Impact	OEMs will not have JTAG debug access to the modem or Apps (LPASS) QDSP6 on the CS2.1. For special OEM QDSP6 development needs, OEMs will need to allocate HW for debug with special ES2.1 parts where Q6 JTAG debugging is not disabled by Qualcomm. These special ES2.1 parts should not be used as commercial devices as QDSP6 debugging cannot be disabled by the OEM.
Workaround	Qualcomm to blow fuse to disable all Q6 ISDB port for all CS parts to make sure QDSP6 debug is disabled. No limitations on Rev2.2 HW as the debug limitation is fixed and OEM can disable QDSP6 debug access.

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Issue 25 PDN optimization

VDD_CORE	
Description	On-die voltage variation due to high board inductance near sensitive circuits.
Impact	On MSM8974 version ES2.1, it is possible for a non-ideal board to cause on-die voltage droop and functional failures.
Workaround	MSM8974 Rev2.2 device modifies the power distribution circuits to greatly reduce on-die droop on a non-ideal board. Refer to the *MSM8974 PDN Specification Updates Application Note* (80-NA437-17) for our latest PDN specification updates for ES2.1 to avoid any risk, as well as all recommendations for PCB routing in *Training: Power Delivery Network Design* (80-VT310-13).
VDD_MEM	
Description	Excess variation on internal voltage used to power internal memories and the DDR system.
Impact	Increase in power in rock bottom and cellular standby modes (up to 10%). Increase in low power active use cases (up to 2 mA). The power impact will be eliminated on Rev2.2 by disabling the power management workarounds
Workaround	By modifying the SOC power management, Qualcomm will eliminate risk of failures due to voltage variation in ES2.1. The issue will be resolved in HW on Rev2.2 samples.

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Issue 26 GPU enhancement

Description	Optimization for instancing features in Open GLES3.0
Impact	No functionality impacts for all use cases of GPU, Open CL, Open GLES 1.x, 2.0. Only for instancing use cases in Open GLES 3.0, for certain frames with heavy instancing load.
Workaround	Rev2.2 HW will have hardware optimization for higher instancing count.

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Issue 27 TDD-LTE 15 MHz 4x2 MIMO not supported

Description	LTE TDD 15 MHz 4x2 MIMO mode is not supported on MSM8974 version ES2.1.
Impact	Currently there are no networks with immediate plans to deploy this, but Qualcomm anticipates operators to mandate this capability for forward compatibility. There is a possibility that CMCC mandates 15 MHz BW for B39. All LTE TDD projects will need to be aligned with Rev2.2 hardware to avoid any future compatibility or roaming concerns.
Workaround	No immediate plans for an ES2.1 software workaround and thus Rev2.2 HW will resolve this issue and all LTE TDD projects on MSM8974 will need Rev2.2 HW.

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4 Enhancements in Rev2.2

4.1 Multiple root certificates (MRC)

- Support 16 root certificates (keys) on device
  - Previous versions of MSM8974 support 1 root
- Certificates are stored in flash memory
  - Hash of certificates is protected in eFuses
- Enables OEM to switch to another root of trust on device
  - Example: From an OEM root certificate to a Government root certificate
  - To prevent tampering, only one switch operation is permitted
- Mechanism provided to select root certificate to use
  - Selection is secured using eFuses

4.2 Emergency download over SDIO

- Current MSM8974 (up to ES2.0/ES2.0.1/ES2.1 and CS2.1 in plan) supports emergency download (EDL) via the HS-USB port and the SDC2 port.
- MSM8974 Rev2.2 supports flexibility to choose and configure EDL on the SDC2 or SDC3 ports, depending on the fuse configuration.
- EDL remains on the SDC2 port by default and customers will need to blow the fuse bit (ALT_SD_PORT_FOR_BOOT) in the customer supply chain to enable the SDC3 port for EDL.