Qualcomm
TECHNOLOGIES, INC

MSM8216/MSM8616/MSM8916

Device Specification

80-NK807-1 Rev. J

October 29, 2014

Submit technical questions at:
https://support.cdmatech.com

Confidential and Proprietary – Qualcomm Technologies, Inc.

Qualcomm Technologies, Inc.
5775 Morehouse Drive
San Diego, CA 92121
U.S.A.

Revision history

Bars appearing in the margin (as shown at left) indicate where technical changes have occurred for this revision. The following table lists the technical content changes for all revisions.

Revision	Date	Description
A	November 2013	Initial release
B	December 2013	■ Global change: Updated package dimension ■ Updated the feature support information in Section 1.3.2 and Table 1-9 ■ Updated pin map information in Chapter 2 ■ Updated mechanical, part marking and identification details in Chapter 4
C	March 2014	■ Global change: □ Format changes throughout the doc □ Added WTR4905 and WCN3660B support □ Changed the clock frequencies of A53 CPU □ Changed display resolution FPS rate to TBD ■ Updated Figure 1-1 with new block diagram, replaces QFE1101 with QFE2101 ■ Format changes for Table 1-9 ■ Updated Figure 2-2 with new pin map with correct color coding and sizing of cells ■ Table 2-2 - Table 2-14: format changes and correct alignment of pad numbers with pin names ■ Added PDN information in Chapter 3, Electrical Specification ■ Figure 4-1: Updated part making information; cleaned up figure and remove some dimensions
D	June 2014	■ Global change: Replaced MSM8916 with MSM8x16 across the document ■ Updated Table 1-1 with updated document titles ■ Updated Table 1-3 with QFE1520/1550/2550/2322 ■ Updated Figure 1-1 with WCN3660B and QFE1520/1550/2550/2322 ■ Updated Section 1.1, Table 1-2, Table 4-1 and Table 4-2 to include device variant infomation ■ Updated Figure 2-2 with NC and DNC pins ■ Updated Table 2-3 with MIPI CSI pad numbers ■ Updated Table 2-4; Removed USB_HS_ID pin as it is an NC pin ■ Updated Table 2-6 on BLSP with appropriate UART and GPIO functionalities ■ Updated Table 2-7 with pad characteristics of JTAG signals ■ Updated Table 2-10 with WDOG_DISABLE for GPIO_80 and USB_HS_ID for GPIO_110 ■ Updated Table 2-12 with NC and DNC pins ■ Added Section 3.2 on operating conditions ■ Added Section 3.5 on power sequencing information ■ Added Section 3.6 on digital logic sequencing informtion ■ Added Section 4.4 on device moisture-sensitivity level ■ Added information in Chapter 5 and Chapter 6

Revision	Date	Description
E	July 2014	■ Global: Updated TBDs in various tables across the document ■ Updated Section 1.3.3 on air interfaces ■ Updated Table 1-9 with RF operating band information ■ Updated the device variants in Table 4-2 ■ Added Section 3.1, Section 3.2, Section 3.4, Section 3.7 to Section 3.12 ■ Added information into Chapter 7
F	August 13, 2014	■ Updated all MIPI CSI and DSI signal names in Figure 2-2 to match Table 2-3; For example: MIPI_CSI0_LANE0_N has been renamed to MIPI_CSI0_LN0_N ■ Updated the display resolution for variant 3 and 4; and removed variant 2 in Table 1-2 and Table 4-2 ■ Updated clock frequency for A53 CPU in Table 3-2 ■ Updated operating voltage values for the following in Table 3-3: □ VDD_P1 □ VDD_MIPI □ VDD_A1 □ VDD_WLAN □ VDD_PLL1 □ VDD_HS_USB_CORE □ VDD_PLL2 □ VDD_A2 □ VDD_USBPHY_1P8 ■ Combined a few parameters that have same power supply sources and hence left a few rows empty in Table 3-3.
G	August 14, 2014	■ Updated the following signal names in Figure 2-2: □ Changed pin T1 from MIPI_CSI0_LN2_P to MIPI_CSI0_LN1_P □ Changed pin U2 from MIPI_CSI0_LN2_N to MIPI_CSI0_LN1_N □ Changed pin V1 from MIPI_CSI0_LN3_P to MIPI_CSI0_LN2_P □ Changed pin V5 from MIPI_CSI0_LN1_P to MIPI_CSI0_CLK_P □ Changed pin W2 from MIPI_CSI0_LN3_N to MIPI_CSI0_LN2_N □ Changed pin W6 from MIPI_CSI0_LN1_N to MIPI_CSI0_CLK_N □ Changed pin Y5 from MIPI_CSI0_LN4_P to MIPI_CSI0_LN3_P □ Changed pin AA6 from MIPI_CSI0_LN4_N to MIPI_CSI0_LN3_N □ Changed pin AB1 from MIPI_CSI1_LN2_P to MIPI_CSI1_LN1_P □ Changed pin AB3 from MIPI_CSI1_LN1_P to MIPI_CSI1_CLK_P □ Changed pin AB5 from MIPI_CSI1_LN1_N to MIPI_CSI1_CLK_N □ Changed pin AB7 from MIPI_DSI_DCDC to MIPI_DSI_LDO □ Changed pin AC2 from MIPI_CSI1_LN2_N to MIPI_CSI1_LN1_N □ Changed pin BD11 from GNSS_BB_IP2 to GNSS_BB_IM ■ Updated VDD_HS_USB_CORE to VDD_USB_HS in Table 3-3

Revision	Date	Description
H	September 2014	■ Table 3-1, Absolute maximum ratings: □ Updated absolute voltage values for the following: – VDD_A1 – VDD_A2 – VDD_APC – VDD_CORE – VDD_MEM – VDD_PLL1 □ Added VDD_USB_HS ■ Updated sample sizes for the following in Table 7-1, Silicon reliability results and Table 7-3, Silicon reliability results: □ DPPM rate (ELFR) and average failure rate (AFR) in FIT (I) failure in billion device-hours □ Mean time to failure (MTTF) t = 1/I in million hours ■ Updated sample sizes for the biased highly accelerated stress test in Table 7-2, Package reliability results and Table 7-4, Package reliability results ■ Updated Section 7.1.3, MSM8916 reliability evaluation report for device from Samsung with Table 7-5, Section A: Silicon reliability results and Table 7-6, Section B: Package reliability results ■ Removed countries from fab sites in Section 7.2, Qualification sample description
These letters are not used to designate document revisions as per Qualcomm documentation standards: I, O, Q, S, X, and Z.		
J	October 2014	■ Table 2-4 Pin descriptions – connectivity functions: □ Moved audio MI2S interface #1 under a new sub-heading audio clock □ Updated the functional descriptions of audio MI2S interface #2 ■ Table 2-8 MSM8x16 wakeup pins for modem power management (MPM) and Table 2-10 Pin descriptions – general-purpose input/output ports: Updated C40 pad type to B-PU:nppukp ■ Table 3-1 Absolute maximum ratings and Table 3-3 Operating conditions: Changed VDD_MIPI_DSI_1P8 to VDD_MIPI_DSI_PLL and updated the description ■ Section 3.5 Power sequencing: Removed VDD_PLL2 ■ Section 3.10.2 UIM interface: Added a new section ■ Section 4.1 Device physical dimensions: Corrected the DnD links for the 760 NSP outline diagram (NT90-NK468-1) ■ Section 6.2.1 Land pad and stencil design: Corrected the DnD link for 760 NSP land/stencil drawing (LS90-NG134-1) ■ Section 6.5 High-temperature warpage: Corrected the DnD link for 760 NSP high-temperature warpage data (WR80-NK468-1)

Contents

Tables

Figures

1 Introduction

1.1 Documentation overview

This device specification defines three MSM™ devices: MSM8216, MSM8616, and MSM8916. Throughout this document, the devices are referred to as the MSM8x16 when material being presented applies to all of them. The main difference between the MSM variants is the air interface standards that are supported; variant details are listed in Table 4-2.

Technical information for the MSM8x16 device is primarily covered by the documents listed in Table 1-1. All documents should be studied for a thorough understanding of the device and its applications. Released MSM8x16 documents will be available for download at the CDMATech Support website (https://support.cdmatech.com).

NOTE This current revision is an early release to support initial product developers. The content is subject to change without advance notice.

Table 1-1 Primary MSM8x16 documentation

Document number	Title/description
80-NK807-1 (this document)	*MSM8216/MSM8616/MSM8916 Device Specification* Provides all MSM8x16 electrical specifications and mechanical information. Additional material includes pin assignments; shipping, storage, and handling instructions; PCB mounting guidelines; and part reliability. This document can be used by company purchasing departments to facilitate procurement.
80-NK807-1A	*MSM8x16 Pin Assignment Spreadsheet* A Microsoft Excel spreadsheet listing all MSM8x16 pad numbers (in alphanumeric order), pad names, pad voltages, pad types, and functional descriptions. This can be used to help build the IC's CAD library symbol, or for quick reference for a particular pad's functional assignment.
80-NK807-1B	*MSM8x16 GPIO Configuration Spreadsheet* A Microsoft Excel spreadsheet listing all MSM8x16 GPIOs (in numeric order), pad numbers, pad voltages, pull states, and available configurations. This can be used to help designers define their products' GPIO assignments.
80-NK807-2	*MSM8x16 Software Interface Manual for OEMs* Provides detailed information about the MSM8x16 software interface and its clocks, security, user interface, and registers.
80-NK807-4	*MSM8216/MSM8616/MSM8916 Device Revision Guide* Provides a history of MSM8x16 revisions, explains how to identify the various device revisions, and discusses known issues (or bugs) for each revision and how to work around them.

Table 1-1 Primary MSM8x16 documentation (cont.)

Document number	Title/description
80-NK807-21	*MSM8216/MSM8616/MSM8916 Chipset Introduction Training Slides* ■ Introductions to the MSM8x16 chipsets and all ICs within the chipsets: □ Required RFICs are WTR4905, WTR1605L, and WTR2605 □ Required power management IC is the PM8916 □ WCN3620, WCN3660B wireless connectivity IC □ NFC1990 NFC connectivity IC ■ Introduction to chipset evaluation platforms
80-NK807-22	*MSM8216/MSM8616/MSM8916 – Digital Baseband* ■ Detailed descriptions of MSM8x16 functions ■ Detailed interface descriptions for the MSM in various applications ■ Key design guidelines for the chipset are illustrated and explained, including: □ Technology overviews □ DC power distribution □ Interface schematic details □ PCB layout guidelines □ External-component recommendations □ Ground and shielding recommendations

This document is organized as follows:

Chapter 1 Provides an overview of the MSM8x16 documentation, gives a high-level functional description of the device, lists the device features, and defines marking conventions, terms, and acronyms used throughout this document.

Chapter 2 Defines the device pin assignments.

Chapter 3 Defines the device electrical performance specifications, including absolute maximum ratings and operating conditions.

Chapter 4 Provides IC mechanical information, including dimensions, markings, ordering information, moisture sensitivity, and thermal characteristics.

Chapter 5 Discusses shipping, storage, and handling of the MSM8x16.

Chapter 6 Presents procedures and specifications for mounting the MSM8x16 onto printed circuit boards (PCBs).

Chapter 7 Presents MSM8x16 reliability data, including a definition of the qualification samples and a summary of qualification test results.

1.2 MSM8x16 introduction

Mobile devices continue to integrate more and increasingly complex functions, and support more operating bands while maintaining performance, board space, and cost.

These demands are met by the MSM8x16 (Figure 1-1) — with its ARM Cortex-A53 application processors – which further expand mass-market chipset capabilities by making 3G and 4G high-speed data and rich multimedia features accessible to more consumers worldwide. This multimode solution supports the latest air interface standards including 1xEV-DOrA, 1x Advanced, HSPA+ and TD-SCDMA, LTE as well as single SIM, dual SIM dual standby (DSDS) and dual SIM dual active (DSDA) enable simultaneous voice and data operation for user multitasking. The new MSM8x16 leverages Qualcomm Technologies, Inc. (QTI) airlink and multimedia technology leadership to significantly lower the cost of high-performance mobile devices.

The MSM8x16 has a high level of integration that reduces the bill-of-material (BOM), which delivers board-area savings. The cost and time-to-market advantages of this IC will help drive wireless broadband adoption in mass markets around the world.

Wireless products based on the MSM8x16 may include:

- Voice and data phones, smartphones
- Support for the latest, most-popular operating systems
- Music player-enabled devices and applications
- Camera phones
- Multimedia phones with gaming, streaming video, and video conferencing features
- GPS, GLONASS, and BeiDou for global location-based service. Supports three band only.
- Wireless connectivity – NFC (QCA1990), Bluetooth, WLAN, and FM receiver (with the WCN3620/WCN3660B)

The MSM8x16 benefits are applied to each of these product types and include:

- Higher integration to reduce PCB surface area, time-to-market, and BOM costs while adding capabilities and processing power
- Integrated application processors and hardware cores eliminate multimedia coprocessors, providing superior image quality and resolution for mobile devices while extending application times
  - Higher computing power for high-end applications, and DC power savings for longer run times
- Position location and navigation systems are supported via the WTR’s global navigation satellite system (GNSS) receiver
  - The MSM8x16 supports Gen 8C operation
- Single platform that provides dedicated support for all market-leading codecs and other multimedia formats to support carrier deployments around the world
- DC power reduction using innovative techniques

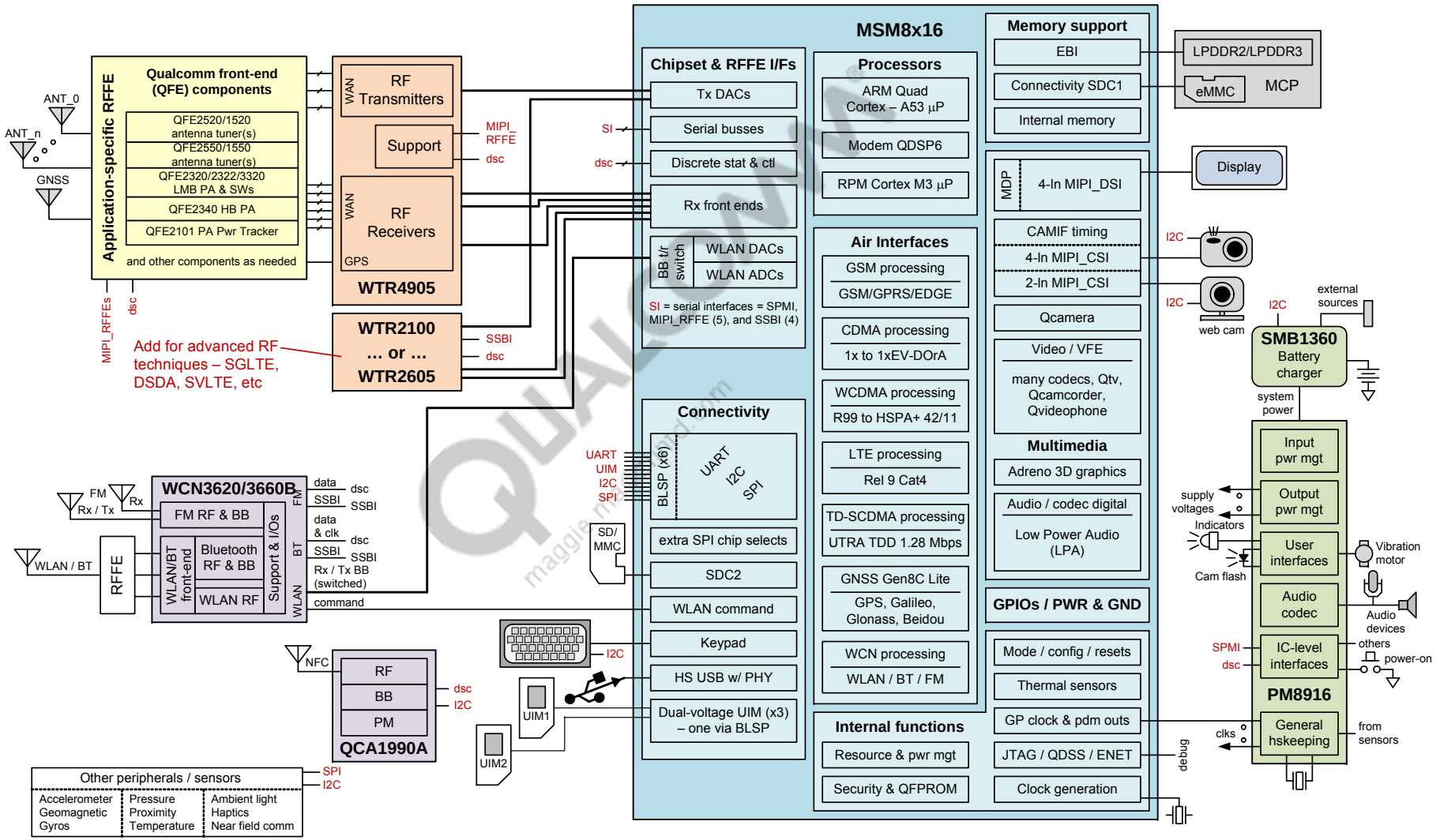

Figure 1-1 MSM8x16 functional block diagram and example application

The MSM8x16 is fabricated using the advanced 28 nm LP CMOS process, and is available in the 760 NSP; a 14.0 × 12.0 × 0.96 mm package with many ground pins for improved electrical grounding, mechanical strength, and thermal continuity. See Chapter 2 for pin assignment details and Chapter 4 for mechanical information.

The MSM8x16 supports high-performance applications worldwide using a variety of wireless networks:

- GSM/GPRS/EDGE
- CDMA2000 1x, 1x Advanced, and 1xEV-DOrA
- WCDMA R99, Rel 5 HSDPA, Rel 6 HSUPA, and Rel 7 HSPA+ (42 Mbps)
- TD-SCDMA with 4.2 Mbps DL and 2.2 Mbps UL option
- LTE Cat 4
- GPS, GNSS, and BeiDou

Complementary ICs within the MSM8x16 chipset include:

- Wafer-level RFICs: WTR4905 (80-NL713-x), WTR1605L (80-N5420-x) and WTR2605 (80-N9978-x documents)
- Power management: PM8916 (80-NK808-x documents)
- Wireless connectivity: WCN3620/WCN3660B for WLAN, Bluetooth, and FM (80-WL006-x and 80-WL007-x documents)
- NFC Connectivity: QCA1990 (80-Y0597-x)

The MSM8x16 chipset and system software solution supports the Convergence Platform for mobile applications by leveraging the years of systems expertise and field experience with CDMA, WCDMA, GSM, TD-SCMDA, LTE, and GNSS technologies that QTI brings. QTI works with its partners to develop products that meet the exact needs of the growing wireless market, providing its customers with complete, verifiable solutions, including fully segmented product families, systems software, testing, and support.

Since the MSM8x16 includes so many diverse functions, its operation is more easily understood by considering major functional blocks individually. Therefore, the MSM8x16 document set is organized according to the following block partitioning:

- Architecture and baseband processors
- Memory support
- Air interfaces
- Multimedia
- Connectivity
- Internal functions
- Interfaces to other functions (including the other ICs within the chipset)
- Configurable general-purpose input/output (GPIO) ports

Most of the information contained in this device specification is organized accordingly — including the circuit groupings within its functional block diagram (Figure 1-1), pin descriptions

(Chapter 2), and detailed electrical specifications (Chapter 3).

1.2.1 Device variants

The only difference between the MSM variants is the combination of air interfaces and display. The camera resolution remains the same for all variants. All variants are summarized in Table 1-2.

Table 1-2 Device information details

Device	Variant	LTE	UMTS	CDMA	TDS	GSM	Display resolution	Camera resolution
MSM8916	3	X	X	X	X	X	1920 x 1080	8 MP/13 MP
	4	X	X		X	X	1920 x 1080	8 MP/13 MP
	5	X	X	X	X	X	1280 x 720	8 MP/13 MP
	6	X	X		X	X	1280 x 720	8 MP/13 MP
	7	X			X	X	1280 x 720	8 MP/13 MP
	0	X	X	X	X	X	qHD	8 MP/13 MP
	1	X	X		X	X	qHD	8 MP/13 MP
	8	X			X	X	qHD	8 MP/13 MP
MSM8616	1		X	X	X	X	1280 x 720	8 MP/13 MP
MSM8216	1		X		X	X	1280 x 720	8 MP/13 MP

1.3 MSM8x16 features

NOTE Some of the hardware features integrated within the MSM8x16 must be enabled by software. Refer to the latest version of the applicable software release notes to identify the enabled MSM8x16 features.

1.3.1 MSM8x16 CS schedules

Table 1-3 MSM8x16 chipset and CS timelines

July-14	MSM8x16	PM8916	WTR 1605L 2605 2100	QFE 2320 2322	QFE 2340	QFE 2101	QFE 1520	QFE 1550	SMB 1360	QCA 1990	WCN 3620 3660B
Oct-14	MSM8x16	PM8916	WTR 4905 2605	QFE 3320	QFE 2340	QFE 2101	QFE 2520	QFE 2550	SMB 1360	QCA 1990	WCN 3620 3660B

1.3.2 New features integrated into MSM8x16

Features integrated into MSM8x16 are as follows:

- Quad 1.2 GHz ARM Cortex-A53 64-bit application processors with 512 kB L2 cache
- 28 nm LP process for lower active power dissipation, and faster peak CPU performance
- Single-channel, non-PoP high-speed memory – LPDDR2/LPDDR3 SDRAM up to 533 MHz clock rate
- QDSP6 v5 processor (modem) up to 691 MHz
- LTE Cat 4
- DSDA support
- Three dual-voltage UIM ports
- Adreno™ A306 3D graphics core

1.3.3 Air interface features

1.3.3.1 Network voice and data

Air interface support depends on the MSM variant, as listed in Table 1-2. Operation of the hardware features are dependent on software implementation. Refer to the most recent software release notes for details.

Table 1-4 3GPP GSM support

Standard	Feature descriptions
GSM	
GPRS	■ Packet-switched data: □ DTM (simple class A) operation □ Multislot class 12 and 33 data services □ CS schemes – CS1, CS2, CS3, and CS4 □ GEA1, GEA2, and GEA3 ciphering □ Maximum of four Rx timeslots per frame
EDGE	■ E2 power class for 8 PSK ■ DTM (simple class A), multislot class 12 and class 33 ■ Downlink coding schemes – CS 1-4, MCS 1-9 ■ Uplink coding schemes – CS 1-4, MCS 1-9 ■ BEP reporting ■ SRB loopback and test mode B ■ 8-bit and 11-bit RACH ■ One-phase/two-phase access procedures ■ Link adaptation and IR ■ NACC, extended UL TBF

Table 1-5 3GPP2 CDMA support

Standard	Feature descriptions
1x	■ 153.6 kbps forward link, 153.6 kbps reverse link ■ Quasi-linear interference cancellation (QLIC) ■ Supported 1x features include: fast 800 Hz forward power control, quasi-orthogonal functions, supplemental channel (SCH) support, forward quick-paging channel (F-QPCH), convolutional and turbo codes on SCH, radio-link protocol 3 (RLP3)
1xEV-DOr0	■ High-speed peak data rates – 2.4 Mbps forward link; 153 kbps reverse link ■ Handoffs between IS-2000 and IS-856 systems ■ Slotted mode operation for reduced power consumption
1xEV-DOrA	■ High-speed peak data rates – 3.1 Mbps forward link; 1.8 Mbps reverse link ■ Platinum broadcast up to 1.5 Mbps multicast services on the forward link via OFDM overlay ■ VoIP, IMs, and IPv6 ■ Plus the r0 features listed above
1x Advanced	■ TIA-2000-E compliant ■ Enhanced quasi-linear interference cancellation (eQLIC) ■ New radio configurations (RC11 on FL, RC8 on RL) ■ New RC's support frame early termination (FET), lower rate power control, and smart blanking of 1/8 rate frames ■ Plus the 1x features listed above

Table 1-6 3GPP WCDMA support

Standard	Feature descriptions
R99	■ All modes and data rates for WCDMA FDD, with the following restrictions: □ The downlink supports the following specifications: – Up to four physical channels, including the broadcast channel (BCH), if present – Up to three dedicated physical channels (DPCHs) – Spreading factor (SF) range support from 4 to 256 – Support for the following transmit diversity modes: space-time transmit diversity (STTD); time-switched transmit diversity (TSTD); closed-loop feedback transmit diversity (CLTD) □ The uplink supports the following specifications: – One physical channel, eight TrCH, and 16 TrBks starting at any frame boundary – A maximum data rate of 384 kbps □ Full SF range support from 4 to 256 ■ PS data rates of 384 kbps DL and 384 kbps UL; CS data rates of 64 kbps DL and 64 kbps UL
R5 HSDPA	■ HS-DSCH (HS-SCCH, HS-PDSCH, and HS-DPCCH) ■ Maximum of 15 HS-PDSCH channels, both QPSK and 16 QAM modulation ■ Support for 3GPP-defined features: □ R99 transport channels □ Maximum of four simultaneous HS-SCCH channels □ CQI and ACK/NACK on HS-DPCCH channel □ All incremental redundancy versions for HARQ □ Configurable support for power classes 3 or 4 per TS 25.101 □ TFC selection limitation on UL factoring in transmissions on the HS-DPCCH per TS 25.133 ■ Switching between HS-PDSCH and DPCH channel resources as directed by the network ■ Network activation of compressed mode by SF/2 or HLS on the DPCH for conducting inter-frequency or inter-radio access technology (RAT) measurements when the HS-DSCH is active ■ STTD on both associated DPCH and HS-DSCH simultaneously ■ CLTD mode 1 on the DPCH when the HS-PDSCH is active ■ STTD on HS-SCCH when STTD or CLTD mode 1 are configured on the associated DPCH

Table 1-6 3GPP WCDMA support (cont.)

Standard	Feature descriptions
R6 HSUPA	■ E-DCH data rates of up to 5.76 Mbps for 2 ms TTI (UE category 6) uplink ■ Support for 3GPP-defined features: □ E-AGCH, E-RGCH and E-HICH channels for downlink; E-RGCH and E-HICH supports serving and non-serving radio links, with up to four radio links in the E-DCH active set □ All HARQ incremental redundancy versions and maximum number of HARQ retransmissions □ Uplink E-DCH channel with support for up to four E-DPDCH channels □ HSUPA channels run simultaneously with R99 and HSDPA channels ■ STTD on all HSUPA downlink channels ■ CLTD mode 1 on HS-PDSCH and DPCH along with HSUPA channels ■ Switch between HSUPA channels and DPCH channel resources as directed by the network ■ Handover using compressed mode with simultaneous E-DCH and HS-DSCH interactive, background, and streaming QoS classes
R7 HSPA+	■ Downlink 64 QAM; up to 21 Mbps ■ Uplink 16 QAM; up to 11 Mbps ■ DTX (discontinuous transmission) and DRX (discontinuous reception) ■ Enhanced F-DPCH ■ Layer 2 optimizations ■ Enhanced cell forward access channel (FACH)
R8 DC-HSPA+	■ Downlink dual carrier with 64 QAM; up to 42 Mbps ■ Enhanced serving cell change ■ Plus the R7 features listed above

Table 1-7 3GPP TD-SCDMA support

Standard	Feature descriptions
R99	■ L1 PHY □ DPCH downlink data processing □ DPCH Uplink data processing □ Cell searcher □ Random access procedure □ Uplink synchronization □ Power Control □ Idle Mode DRX and Paging □ Measurement □ Cell reselection □ Hard handover □ Baton handover □ N-Frequency (primary frequency and working frequency) ■ L2 MAC □ Transport channels support - FACH, RACH, BCH, PCH, DCH □ Logical channels support - BCCH, PCCH, DCCH, CCCH, DTCH, CTCH □ Mapping between logical channels and transport channels □ TFC selection □ Traffic volume measurement □ Access Service Class selection for RACH transmission □ Priority handling between data flows □ Multiplexing/demultiplexing of upper layer PDUs into/from transport blocks (sets) □ Control of RACH transmissions □ Multiple CCTrCH ■ L2 RLC □ Transparent Mode (TM) data transmitting and receiving □ Unacknowledged Mode (UM) data transmitting and receiving □ Acknowledged Mode (AM) data transmitting and receiving ■ L3 RRC □ RRC states: Idle, CELL_DCH, CELL_FACH, CELL_PCH, URA_PCH □ RRC procedures – Connection management procedures • Broadcast of system information • Paging • RRC connection • UE capability • Direct transfer • Security mode control • Signaling connection □ Inter-RAT handover information transfer

Table 1-7 3GPP TD-SCDMA support

	– Radio bearer procedures • Radio bearer establishment/reconfiguration • Transport channel reconfiguration • Physical channel reconfiguration • Uplink Physical Channel Control (TDD only) – Mobility procedures • Cell and URA update procedures • Hard handover • Inter-RAT handover/cell reselection/cell change order – Measurement procedures • Intra-frequency, Inter-frequency, Inter-RAT measurements □ General procedures – Open Loop Power Control – FACH measurement occasion – Access Service Classes – RRC message IE handling - UE Capability IE, Radio Bearer IE, Transport Channel IE, Physical Channel IE, Measurement IE, etc. – Cell Selection/Reselection – Timers – Measurement events – ANS.1

Table 1-8 3GPP GSM support

Standard	Feature descriptions
R8	□ FDD: up to 100 Mbps downlink, 50 Mbps uplink (Cat3) □ FDD: up to 150 Mbps downlink, 50 Mbps uplink (Cat4) □ TDD: up to 68 Mbps downlink, 17 Mbps uplink (Cat3) □ TDD: up to 117 Mbps downlink, 30 Mbps uplink (Cat4) □ 1.4 to 20 MHz RF bandwidth □ 2 × 2 downlink SU-MIMO; 4 × 2 downlink SU-MIMO □ IPv6, QoS □ Inter-RAT capabilities with 1x, 1xEV-DO Rev B, DC-HSPA+, EDGE, and TD-SCDMA modes
Note: For TDD mode uplink/downlink peak throughputs are configuration dependent.	

1.3.4 Summary of MSM8x16 features

MSM8x16 features are summarized in Table 1-9.

Table 1-9 Summary of MSM8x16 features

Feature	MSM8x16 capability
Processors	
Applications	ARM Cortex-A53 microprocessor cores up to 1.2 GHz ■ 64-bit processor ■ Quad core, 512 kB L2 cache ■ Primary boot processor
Modem system	QDSP6 v5 core at up to 691 Hz 768 kB L2 caches ■ MSM8x16: DSDS and DSDA
RPM system	Cortex M3: Modem power manager (MPM) MPM coordinates shutdown/wakeup, clock rates, and VDDs
Memory support	
System memory via EBI	Non PoP LPDDR2, LPDDR3 SDRAM; 32-bit wide; up to 533 MHz
Graphics internal memory	128 kB unified SRAM pool on-chip memory (GMEM)
External memory via SDC1	eMMC v4.5/SD flash devices
RF support	
RF operating bands	Defined by WTR device
Air interfaces ■ GSM ■ CDMA ■ WCDMA ■ TD-SCDMA ■ LTE ■ WLAN/BT/FM ■ NFC	See summary in Table 1-9 and details in Section 1.3.3 ■ Yes ■ Yes ■ Yes ■ Yes ■ Yes ■ Yes – all (with WCN3620/WCN3660B) ■ Yes – With QCA1990
GNSS – Qualcomm® IZat™ engine	Gen 8C; Support for three bands ***concurrently***: ■ GPS, BeiDou, and **Glonass** or ■ GPS, BeiDou, and **Galileo**
Multimedia	
Display interfaces MIPI_DSI General display features	HD (1280 x 720) 60 fps; 16/18/24 bpp RGB MIPI DSI 4-lane Wi-fi display – 720p30/1080p30 FHD + 720p external wireless display
Camera interfaces Number of CSIs Primary (CSI0) Secondary (CSI1) Configurations supported General camera features	Qcamera Two; 1.5 Gbps per lane 4-lane; supports CMOS and CCD sensors Up to 13 MP sensors 2-lane MIPI_CSI – webcam support up to 8 MP sensors Pixel manipulations, camera modes, image effects, and post-processing techniques, including defective pixel correction I2C controls

Table 1-9 Summary of MSM8x16 features (cont.)

Feature	MSM8x16 capability
Mobile display processor	MDP for display processing
Video applications performance	
Encode	720p 30 fps (H.264 Baseline/MPEG-4)
	30 fps 1080p (MPEG-4/H.264/VP8/H.263)
	WFD 720p @ 30 fps
Decode	30 fps 1080p (MPEG- 4/H.264/H.263/DivX/MPEG2/VC1/Soreson/VP8)
	WFD 1080p @ 30 fps
Graphics	Adreno 306; up to 400 MHz 3D graphics accelerator
Audio	
Low-power audio	Low power audio for mp3 and AAC playback; surround sound;
Voice codec support	Versatile – many audio playback and voice modes; encoders for audio and FM
Audio codec support	recording; many concurrency modes
	G711; Raw PCM; QCELP; EVRC, -B, -WB; AMR-NB, -WB; GSM-EFR, -FR, -HR
Enhanced audio	
Synthesizer	MP3; AAC+, eAAC; AMR-NB, -WB, G.711, WMA 9/10 Pro
	Dolby Digital Plus and DTS-HD surround sound
	Fluence™ Noise Cancellation
	QAudioFX/Qconcert/QEnsemble
	128-voice polyphony wavetable
Web technologies	V8 JavaScript Engine optimizations
	Webkit browser JPEG hardware decode acceleration
	Networking Stack IP and HTTP tuning
	Flash 10.x and video processor decode optimization
Messaging	Text messages; text encoding for SMS
	Multimedia messaging services – combined video (MPEG4), still image (JPEG), voice tag (AMR), text sent as message
Connectivity	
BLSP ports	six, 4 bits each; multiplexed serial interface functions
UART	Yes – up to 4 Mbps
I2C	Yes – cameras, sensors, near field communicator (NFC), SMB etc.
SPI (master only)	Yes – cameras, sensors, etc.
UIM	Three ports – dual voltage (1.8 V/2.85 V)
USB	One USB 2.0 high-speed
Secure digital interfaces	Up to two ports, both dual-voltage
	One 8-bit and one 4-bit
	SD 3.0; SD/MMC card; eMMC v4.5
Wireless connectivity	With WCN3620 and WCN3660B
WLAN	802.11 a/b/g/n
Bluetooth	BT 4.0 LE and earlier
FM radio	Rx
NFC	QCA1990

Table 1-9 Summary of MSM8x16 features (cont.)

Feature	MSM8x16 capability
Touch screen support	Capacitive panels via ext IC (I^2C, SPI, and interrupts)
Audio interfaces	
DMIC	One port for digital mic application
MI2S	Up to two ports (primary and secondary ports)
CDC PDM port	Interface between PM8916 and MSM8x16 for audio application
Configurable GPIOs	
Number of GPIO ports	122 GPIOs – GPIO_0 to GPIO_121
Input configurations	Pull-up, pull-down, keeper, or no pull
Output configurations	Programmable drive current
Top-level mode multiplexer	Provides a convenient way to program groups of GPIOs
Internal functions	
Security	Secure boot, SFS, ARM TrustZone, SEE, secure debug, and Microsoft WM DRM10
Crypto engine	Increased throughput via increased frequencies and a new internal AXI-based data master; support for multiple execution environments per Crypto; algorithm accelerate file system encryption (AES-XTS), IPSec and SSL (HMAC-SHA, CCM, CMAC)
QFPROM	Large fuse array, replaces previous-generation Qfuse chains; non-volatile memory with faster and simpler programming
Security controller	Chip-wide configuration for security, feature enable, and debug; persistent storage of ID numbers and sensitive key data; secure HDCP key provisioning and secure debug facility; primary and secondary hardware key blocking for SFS
PLLs and clocks	Multiple clock regimes; watchdog and sleep timers 19.2 MHz CXO master clock input General-purpose outputs: M/N counter, PDM
Resource and power manager	Fundamental to power management Key blocks: RPM core, Cortex M3, security controller, MPM Improved efficiency via clock control, split-rail power collapse and voltage scaling; several low-power sleep modes
Debug	JTAG, QDSS
Others	Thermal sensors; modes and resets; peripheral subsystem
Chipset and RF front-end (RFFE) interface features	
WTR RFICs	WTR4905, WTR1605L, and WTR2605
WLAN baseband data	One Rx and one Tx analog interface
GNSS baseband data	Rx analog interface
Status and control	SSBIs and discrete signals as needed via GPIOs
Power management	PM8916 2-line SPMI; dedicated clock and reset lines; plus other GPIOs as needed

Table 1-9 Summary of MSM8x16 features (cont.)

Feature	MSM8x16 capability
WCN wireless connectivity WLAN baseband data WLAN status and control Bluetooth FM radio	WCN3620/WCN3660B Multiplexed Rx/Tx analog interface Proprietary 5-line interface 2-line data interface plus SSBI 1-line data interface plus SSBI
QCA near field communicator	I2C plus other GPIOs as needed
QFE PA power management	RFFE clock and data ports via GPIOs
Power amplifiers and RF switches	Discrete control lines
Fabrication technology and package	
Digital die	28 nm LP CMOS
Small, thermally efficient package	760 NSP: 14.0 × 12.0 × 0.96 mm; 0.4-mm pitch

1.4 Terms and acronyms

Table 1-10 defines terms and acronyms commonly used throughout this document.

Table 1-10 Terms and acronyms

Term	Definition
ADC	Analog-to-digital converter
AGC	Automatic gain control
BER	Bit error rate
bps	Bits per second
BT	Bluetooth
CDMA	Code division multiple access
CRC	Cyclic redundancy code
CSI	Camera serial interface
DAC	Digital-to-analog converter
DDR	Double data rate
DRM	Digital Rights Management
DSDA	Dual SIM dual active
DSDS	Dual SIM dual standby
DSI	Display serial interface
DSP	Digital signal processor
EBI	External bus interface
EDGE	Enhanced data rates for GSM evolution
ETB	Embedded trace buffer
EV-DO	Evolution data optimized

Table 1-10 Terms and acronyms (cont.)

Term	Definition
FDD	Frequency division duplex
GLONASS	Global orbiting navigation satellite system
GNSS	Global navigation satellite system
GPIO	General-purpose input/output
GPRS	General packet radio services
GPS	Global positioning system
GPU	Graphics processing unit
GRFC	General RF control
GSM	Global system for mobile communications
HSPA+	High-speed packet access
I^2C	Inter-integrated circuit
ISP	Image signal processing
JPEG	Joint Photographic Experts Group
JTAG	Joint Test Action Group (ANSI/ICEEE Std. 1149.1-1760)
kbps	kilobits per second
LCD	Liquid crystal display
LPA	Low-power audio
LPASS	Low-power audio subsystem
LPDDR	Low-power DDR
LPM	LPASS memory
LSB	Defines whether the LSB is the least significant bit or least significant byte. All instances of LSB used in this manual are assumed to be LSByte, unless otherwise specified.
MDP	Mobile display processor
MIPI	Mobile industry processor interface
MMC	Multimedia card
MPM	Modem power management
MSB	Defines whether the MSB is the most significant bit or most significant byte. All instances of MSB used in this manual are assumed to be MSByte, unless otherwise specified.
NSP	Nanoscale package
OMA	Open Mobile Alliance
PA	Power amplifier
PDM	Pulse-density modulation
PM	Power management
QDSS	Qualcomm debug subsystem
QFPROM	Qualcomm fuse programmable read-only memory
QLIC	Quasi-linear interference cancellation

Table 1-10 Terms and acronyms (cont.)

Term	Definition
QTI	Qualcomm Technologies, Inc.
QUP	Qualcomm Unified Peripheral
RBDS	Radio broadcast data system
RDS	Radio data system
RLP	Radio link protocol
RPM	Resource power manager
SBI	Serial bus interface
SD	Secure digital
SDC	Secure digital controller
SEE	Secure Execution Environment
SFS	Secure file system
SIM	Subscriber identity module
SMT	Surface mount technology
SPI	Serial peripheral interface
sps	Symbols per second (or samples per second)
SPSS	Smart peripheral subsystem
SSBI	Single-wire SBI
TAP	Test access port
TCXO	Temperature-compensated crystal oscillator
TDD	Time division duplexing
TSTS	Triple SIM Triple Standby
UART	Universal asynchronous receiver transmitter
UIM	User identity module
UMTS	Universal mobile telecommunications system
USB	Universal serial bus
USIM	UMTS subscriber identity module
WCDMA	Wideband code division multiple access
WCN	Wireless connectivity network
WLAN	Wireless local area network
WTR	Wafer-scale RF transceiver
XO	Crystal oscillator
ZIF	Zero intermediate frequency

1.5 Special marks

Table 1-11 defines special marks used in this document.

Table 1-11 Special marks

Mark	Definition
[ ]	Brackets ([ ]) sometimes follow a pin, register, or bit name. These brackets enclose a range of numbers. For example, DATA[7:4] may indicate a range that is 4 bits in length, or DATA[7:0] may refer to all eight DATA pins.
_N	A suffix of _N indicates an active low signal. For example, RESIN_N.
0x0000	Hexadecimal numbers are identified with an x in the number (for example, 0x0000). All numbers are decimal (base 10) unless otherwise specified. Non-obvious binary numbers have the term binary enclosed in parentheses at the end of the number; for example, 0011 (binary).
|	A blue vertical bar in the outside margin of a page indicates that a change was made since the previous revision of this document.

2 Pin Definitions

The MSM8x16 is available in the 760 NSP – see Chapter 4 for package details. A high-level view of all pin assignments is shown in Figure 2-3. The pins are colored to indicate which function type they support, as defined in Figure 2-1.

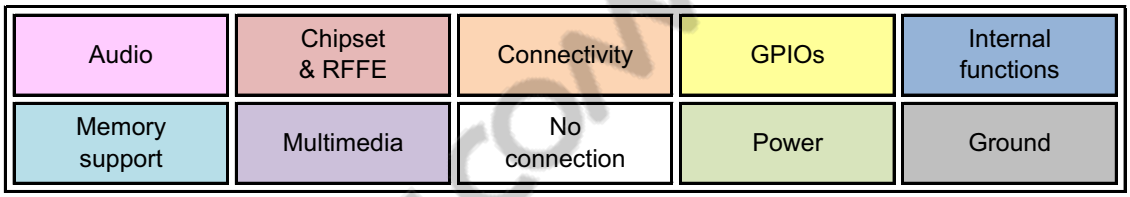

Figure 2-1 MSM8x16 pin assignments – legend

The text within Figure 2-3 is difficult to read when viewing an 8½" by 11" hard copy. Other viewing options are available:

- Print that one page on an 11" by 17" sheet.
- View the graphic soft copy and zoom in – the resolution is sufficient for comfortable reading.
- Download the *MSM8916 Pin Assignment Spreadsheet* (80-NK807-1A) – this Microsoft® Excel spreadsheet lists all MSM8x16 pad numbers (in alphanumeric order), pad names, pad voltages, pad types, and functional descriptions.

NOTE Click the link below to download the pin assignment spreadsheet (80-NK807-1A) from the CDMA Tech Support website.

https://downloads.cdmatech.com/qdc/drl/objectId/09010014824cc7b4

If you have permission to view the document, a prompt will be presented for initiating the download.

NOTE Subscribe to the pin assignment spreadsheet to be notified of any changes.

Click the **Help** button to download the latest revision of *Using CDMATech Support Documents and Downloads User Guide* (80-V7273-1). This document includes subscription instructions.

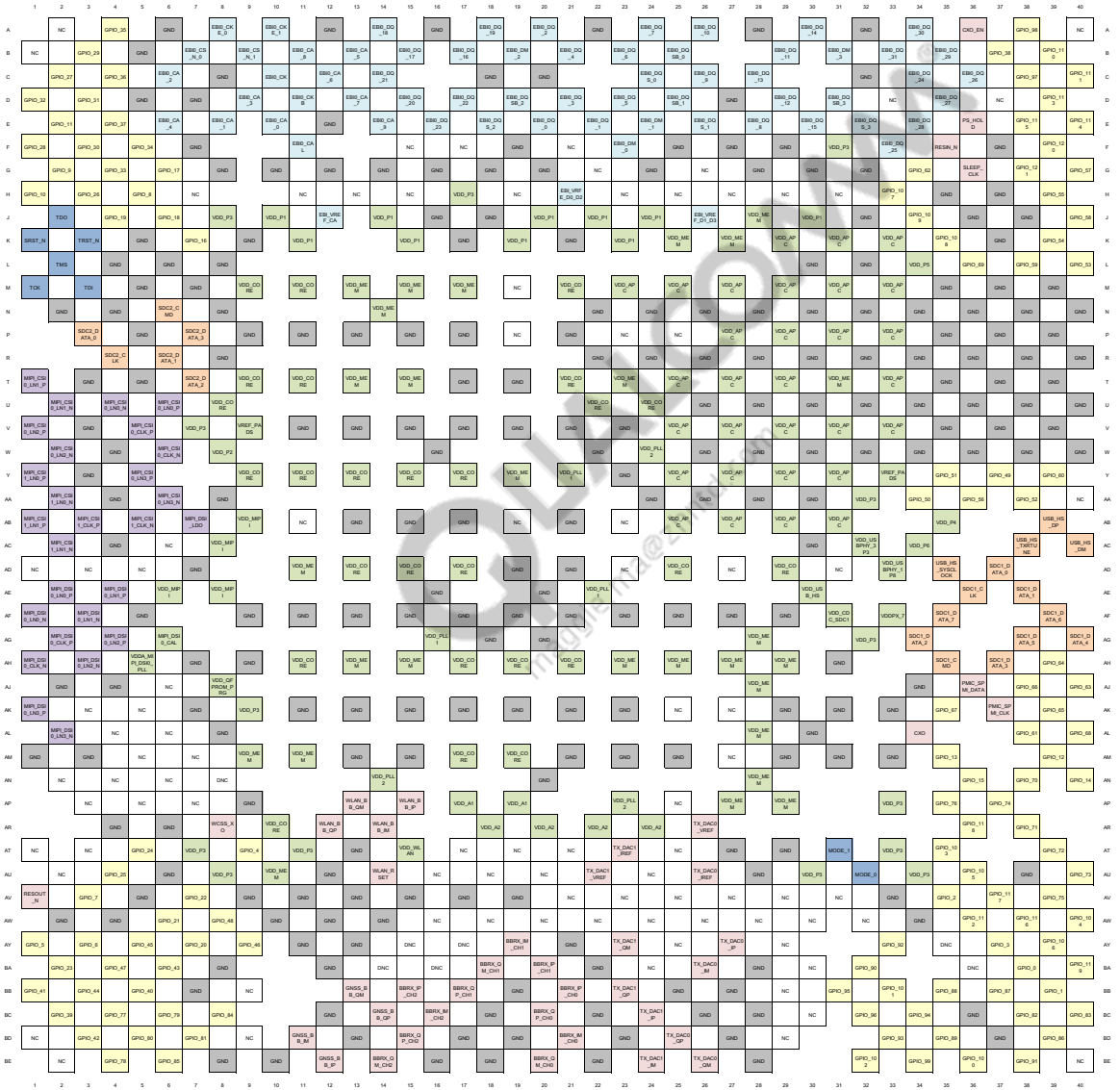

Figure 2-2 High-level view of MSM8x16 pin assignments (top view)

2.1 I/O parameter definitions

Table 2-1 I/O description (pad type) parameters

Symbol	Description
Pad attribute	
AI	Analog input (does not include pad circuitry)
AO	Analog output (does not include pad circuitry)
B	Bidirectional digital with CMOS input
DI	Digital input (CMOS)
DO	Digital output (CMOS)
H	High-voltage tolerant
S	Schmitt trigger input
Z	High-impedance (high-Z) output
Pad pull details for digital I/Os	
nppdpukp	Programmable pull resistor. The default pull direction is indicated using capital letters and is a prefix to other programmable options: ■ NP: pdpukp = default no-pull with programmable options following the colon (:) ■ PD: nppukp = default pulldown with programmable options following the colon (:) ■ PU: nppdkp = default pullup with programmable options following the colon (:) ■ KP: nppdpu = default keeper with programmable options following the colon (:)
KP	Contains an internal weak keeper device (keepers cannot drive external buses)
NP	Contains no internal pull
PU	Contains an internal pullup device
PD	Contains an internal pulldown device
Pad voltage groupings for baseband circuits	
P1	EBI Pad group 1 (EBI for LPDDR2/LPDDR3 memory); tied to VDD_P1 pins (1.2 V only)
P2	Pad group 2 (SDC2); tied to VDD_P2 pins (1.8 V or 2.85 V)
P3	Pad group 3 (most peripherals); tied to VDD_P3 pins (1.8 V only)
P4	Pad group 4 (UIM3); tied to VDD_P4 pins (1.8 V or 2.85 V)
P5	Pad group 5 (UIM1); tied to VDD_P5 pins (1.8 V or 2.85 V)
P6	Pad group 6 (UIM2); tied to VDD_P6 pins (1.8 V or 2.85 V)
P7	Pad group 7 (SDC1); tied to VDD_P7 pins (1.2 V or 1.8 V)
MIPI	Supply voltage for MIPI_CSI, MIPI_DSI circuits, and I/Os; tied VDD_MIPI (1.8 V only)

Table 2-1 I/O description (pad type) parameters (cont.)

Symbol	Description
Output current drive strength	
EBI pads	Pads for EBI are tailored for 1.2 V interfaces and are source terminated; additional details will be given in future revisions of this document.
3.0 V (H) pads	Programmable drive strength, 2–8 mA in 2 mA steps
Others [1]	Programmable drive strength, 2–16 mA in 2 mA steps

1. Digital pads other than EBI pads or high-voltage tolerant pads.

2.1.1 Pin descriptions

Descriptions of all pins are presented in the following tables, organized by functional group:

Table 2-2: Memory support functions

Table 2-3: Multimedia functions

Table 2-4: Connectivity functions

Table 2-7: Internal functions

Table 2-9: Chipset interface functions

Table 2-10: General-purpose input/output ports

Table 2-11: RF front-end interface functions

Table 2-12: No connection, do not connect, and reserved pins

Table 2-13: Power supply pins

Table 2-14: Ground pins

Table 2-2 Pin descriptions – memory support functions

Pad #	Pad name and/or function	Pad name or alt function	Pad characteristics		Functional description
			Voltage	Type	
E10	EBI_CA_0		P1	DO	LPDDR2/LPDDR3 command/address bit 0
E8	EBI_CA_1		P1	DO	LPDDR2/LPDDR3 command/address bit 1
C6	EBI_CA_2		P1	DO	LPDDR2/LPDDR3 command/address bit 2
D9	EBI_CA_3		P1	DO	LPDDR2/LPDDR3 command/address bit 3
E6	EBI_CA_4		P1	DO	LPDDR2/LPDDR3 command/address bit 4
B13	EBI_CA_5		P1	DO	LPDDR2/LPDDR3 command/address bit 5
C12	EBI_CA_6		P1	DO	LPDDR2/LPDDR3 command/address bit 6
D13	EBI_CA_7		P1	DO	LPDDR2/LPDDR3 command/address bit 7
B11	EBI_CA_8		P1	DO	LPDDR2/LPDDR3 command/address bit 8
E14	EBI_CA_9		P1	DO	LPDDR2/LPDDR3 command/address bit 9

Table 2-2 Pin descriptions – memory support functions (cont.)

Pad #	Pad name and/or function	Pad name or alt function	Pad characteristics		Functional description
			Voltage	Type	
F11	EBI_CAL_REXT		-	AI	LPDDR2/LPDDR3 calibration resistor
C10	EBI_CK		P1	DO	LPDDR2/LPDDR3 differential clock (+)
D11	EBI_CKB		P1	DO	LPDDR2/LPDDR3 differential clock (-)
A8	EBI_CKE_0		P1	DO	LPDDR2/LPDDR3 clock enable 0
A10	EBI_CKE_1		P1	DO	LPDDR2/LPDDR3 clock enable 1
B7	EBI_CS0_N		P1	DO	LPDDR2/LPDDR3 chip select 0
B9	EBI_CS1_N		P1	DO	LPDDR2/LPDDR3 chip select 1
F23	EBI_DM_0		P1	DO	LPDDR2/LPDDR3 data mask for byte 0
E24	EBI_DM_1		P1	DO	LPDDR2/LPDDR3 data mask for byte 1
B19	EBI_DM_2		P1	DO	LPDDR2/LPDDR3 data mask for byte 2
B31	EBI_DM_3		P1	DO	LPDDR2/LPDDR3 data mask for byte 3
E20	EBI_DQ_0		P1	B	LPDDR2/LPDDR3 data bit 0
E22	EBI_DQ_1		P1	B	LPDDR2/LPDDR3 data bit 1
A20	EBI_DQ_2		P1	B	LPDDR2/LPDDR3 data bit 2
D21	EBI_DQ_3		P1	B	LPDDR2/LPDDR3 data bit 3
B21	EBI_DQ_4		P1	B	LPDDR2/LPDDR3 data bit 4
D23	EBI_DQ_5		P1	B	LPDDR2/LPDDR3 data bit 5
B23	EBI_DQ_6		P1	B	LPDDR2/LPDDR3 data bit 6
A24	EBI_DQ_7		P1	B	LPDDR2/LPDDR3 data bit 7
E28	EBI_DQ_8		P1	B	LPDDR2/LPDDR3 data bit 8
C26	EBI_DQ_9		P1	B	LPDDR2/LPDDR3 data bit 9
A26	EBI_DQ_10		P1	B	LPDDR2/LPDDR3 data bit 10
B29	EBI_DQ_11		P1	B	LPDDR2/LPDDR3 data bit 11
D29	EBI_DQ_12		P1	B	LPDDR2/LPDDR3 data bit 12
C28	EBI_DQ_13		P1	B	LPDDR2/LPDDR3 data bit 13
A30	EBI_DQ_14		P1	B	LPDDR2/LPDDR3 data bit 14
E30	EBI_DQ_15		P1	B	LPDDR2/LPDDR3 data bit 15
B17	EBI_DQ_16		P1	B	LPDDR2/LPDDR3 data bit 16
B15	EBI_DQ_17		P1	B	LPDDR2/LPDDR3 data bit 17
A14	EBI_DQ_18		P1	B	LPDDR2/LPDDR3 data bit 18
A18	EBI_DQ_19		P1	B	LPDDR2/LPDDR3 data bit 19
D15	EBI_DQ_20		P1	B	LPDDR2/LPDDR3 data bit 20
C14	EBI_DQ_21		P1	B	LPDDR2/LPDDR3 data bit 21
D17	EBI_DQ_22		P1	B	LPDDR2/LPDDR3 data bit 22
E16	EBI_DQ_23		P1	B	LPDDR2/LPDDR3 data bit 23
C34	EBI_DQ_24		P1	B	LPDDR2/LPDDR3 data bit 24
F33	EBI_DQ_25		P1	B	LPDDR2/LPDDR3 data bit 25

Table 2-2 Pin descriptions – memory support functions (cont.)

Pad #	Pad name and/or function	Pad name or alt function	Pad characteristics		Functional description
			Voltage	Type	
C36	EBI_DQ_26		P1	B	LPDDR2/LPDDR3 data bit 26
D35	EBI_DQ_27		P1	B	LPDDR2/LPDDR3 data bit 27
E34	EBI_DQ_28		P1	B	LPDDR2/LPDDR3 data bit 28
B35	EBI_DQ_29		P1	B	LPDDR2/LPDDR3 data bit 29
A34	EBI_DQ_30		P1	B	LPDDR2/LPDDR3 data bit 30
B33	EBI_DQ_31		P1	B	LPDDR2/LPDDR3 data bit 31
C24	EBI_DQS_0		P1	B	LPDDR2/LPDDR3 differential data strobe for byte 0 (+)
E26	EBI_DQS_1		P1	B	LPDDR2/LPDDR3 differential data strobe for byte 1 (+)
E18	EBI_DQS_2		P1	B	LPDDR2/LPDDR3 differential data strobe for byte 2 (+)
E32	EBI_DQS_3		P1	B	LPDDR2/LPDDR3 differential data strobe for byte 3 (+)
B25	EBI_DQS_0B		P1	B	LPDDR2/LPDDR3 differential data strobe for byte 0 (-)
D25	EBI_DQS_1B		P1	B	LPDDR2/LPDDR3 differential data strobe for byte 1 (-)
D19	EBI_DQS_2B		P1	B	LPDDR2/LPDDR3 differential data strobe for byte 2 (-)
D31	EBI_DQS_3B		P1	B	LPDDR2/LPDDR3 differential data strobe for byte 3 (-)
J12	EBI_VREF_CA		-	AI	LPDDR2/LPDDR3 CA reference voltage
H21	EBI_VREF_D0_D2		-	AI	LPDDR2/LPDDR3 D0 and D2 reference voltage
J26	EBI_VREF_D1_D3		-	AI	LPDDR2/LPDDR3 D1 and D3 reference voltage

Table 2-3 Pin descriptions – multimedia functions

Pad #	Pad name and/or function	Pad name or alt function	Pad characteristics		Functional description
			Voltage	Type	
Primary camera serial interface – 4-lane MIPI_CSI0					
U4	MIPI_CSI0_LN0_N		MIPI	AI, AO	MIPI camera serial interface 0 lane 0 – negative
U6	MIPI_CSI0_LN0_P		MIPI	AI, AO	MIPI camera serial interface 0 lane 0 – positive
W6	MIPI_CSI0_CLK_N		MIPI	AI	MIPI camera serial interface 0 clock – negative
V5	MIPI_CSI0_CLK_P		MIPI	AI	MIPI camera serial interface 0 clock – positive
U2	MIPI_CSI0_LN1_N		MIPI	AI, AO	MIPI camera serial interface 0 lane 1 – negative
T1	MIPI_CSI0_LN1_P		MIPI	AI, AO	MIPI camera serial interface 0 lane 1 – positive
W2	MIPI_CSI0_LN2_N		MIPI	AI, AO	MIPI camera serial interface 0 lane 2 – negative
V1	MIPI_CSI0_LN2_P		MIPI	AI, AO	MIPI camera serial interface 0 lane 2 – positive
AA6	MIPI_CSI0_LN3_N		MIPI	AI, AO	MIPI camera serial interface 0 lane 3 – negative
Y5	MIPI_CSI0_LN3_P		MIPI	AI, AO	MIPI camera serial interface 0 lane 3 – positive
Secondary camera serial interface – 2-lane MIPI_CSI1					
AA2	MIPI_CSI1_LN0_N		MIPI	AI, AO	MIPI camera serial interface 1 lane 0 – negative
Y1	MIPI_CSI1_LN0_P		MIPI	AI, AO	MIPI camera serial interface 1 lane 0 – positive
AB5	MIPI_CSI1_CLK_N		MIPI	AI	MIPI camera serial interface 1 clock – negative
AB3	MIPI_CSI1_CLK_P		MIPI	AI	MIPI camera serial interface 1 clock – positive
AC2	MIPI_CSI1_LN1_N		MIPI	AI, AO	MIPI camera serial interface 1 lane 1 – negative
AB1	MIPI_CSI1_LN1_P		MIPI	AI, AO	MIPI camera serial interface 1 lane 1 – positive
H3	CAM_MCLK0	GPIO_26	P3	DO B-PD:nppukp	Camera master clock 0 Configurable I/O
C2	CAM_MCLK1	GPIO_27	P3	DO B-PD:nppukp	Camera master clock 1 Configurable I/O
B3	CAM_I2C_SDA	GPIO_29	P3	B B-PD:nppukp	Camera I2C serial data Configurable I/O
F3	CAM_I2C_SCL	GPIO_30	P3	B B-PD:nppukp	Camera I2C serial clock Configurable I/O
D3	CCI_TIMER0	GPIO_31	P3	DO B-PD:nppukp	Camera control interface timer 0 Configurable I/O
D1	CCI_TIMER1	GPIO_32	P3	DO B-PD:nppukp	Camera control interface timer 1 Configurable I/O
B37	CCI_TIMER2	GPIO_38	P3	DO B-PD:nppukp	Camera control interface timer 2 Configurable I/O
G4	CCI_ASYNC0	GPIO_33	P3	DI B-PD:nppukp	Camera control interface async 0 Configurable I/O
F1	CAM1_RST_N	GPIO_28	P3	DO B-PD:nppukp	Camera 1 (front camera) reset Configurable I/O
F5	CAM0_STANDBY_N	GPIO_34	P3	DO B-PD:nppukp	Camera 0 (rear camera) standby Configurable I/O
A4	CAM0_RSTN_N	GPIO_35	P3	DO B-PD:nppukp	Camera 0 (rear camera) reset Configurable I/O

Table 2-3 Pin descriptions – multimedia functions (cont.)

Pad #	Pad name and/or function	Pad name or alt function	Pad characteristics		Functional description
			Voltage	Type	
Display serial interface – 4-lane MIPI_DSI0					
AH1	MIPI_DSI0_CLK_N		MIPI	AO	MIPI display serial interface 0 clock – negative
AG2	MIPI_DSI0_CLK_P		MIPI	AO	MIPI display serial interface 0 clock – positive
AF1	MIPI_DSI0_LN0_N		MIPI	AI, AO	MIPI display serial interface 0 lane 0 – negative
AE2	MIPI_DSI0_LN0_P		MIPI	AI, AO	MIPI display serial interface 0 lane 0 – positive
AF3	MIPI_DSI0_LN1_N		MIPI	AI, AO	MIPI display serial interface 0 lane 1 – negative
AE4	MIPI_DSI0_LN1_P		MIPI	AI, AO	MIPI display serial interface 0 lane 1 – positive
AH3	MIPI_DSI0_LN2_N		MIPI	AI, AO	MIPI display serial interface 0 lane 2 – negative
AG4	MIPI_DSI0_LN2_P		MIPI	AI, AO	MIPI display serial interface 0 lane 2 – positive
AL2	MIPI_DSI0_LN3_N		MIPI	AI, AO	MIPI display serial interface 0 lane 3 – negative
AK1	MIPI_DSI0_LN3_P		MIPI	AI, AO	MIPI display serial interface 0 lane 3 – positive
AB7	MIPI_DSI_LDO		MIPI	AI, AO	MIPI display serial interface 0 low-dropout regulator
AT5	MDP_VSYNC_P	GPIO_24	P3	DO B-PD:nppukp	MDP VSYNC Signal Configurable I/O
AG6	MIPI_DSI0_CAL		MIPI	AI, AO	MIPI display serial interface 0 calibration

Table 2-4 Pin descriptions – connectivity functions

Pad #	Pad name and/or function	Pad name or alt function	Pad characteristics		Functional description
			Voltage	Type	
High-speed USB 2.0					
AC40	USB_HS_DM			AI, AO	USB HS data minus
AB39	USB_HS_DP			AI, AO	USB HS data plus
AD35	USB_HS_SYSCLOCK			DI	USB HS system clock (19.2 MHz)
AC38	USB_HS_REXT			AI	USB HS external resistor
Secure digital controller 1 (SDC1) interface – supports dual-voltage eMMC NAND					
AE36	SDC1_CLK		P7	B-NP:pdpukp	Secure digital controller 1 clock
AH35	SDC1_CMD		P7	B-PD:nppukp	Secure digital controller 1 command
AD37	SDC1_DATA_0		P7	B-PD:nppukp	Secure digital controller 1 data bit 0
AE38	SDC1_DATA_1		P7	B-PD:nppukp	Secure digital controller 1 data bit 1
AG34	SDC1_DATA_2		P7	B-PD:nppukp	Secure digital controller 1 data bit 2
AH37	SDC1_DATA_3		P7	B-PD:nppukp	Secure digital controller 1 data bit 3
AG40	SDC1_DATA_4		P7	B-PD:nppukp	Secure digital controller 1 data bit 4
AG38	SDC1_DATA_5		P7	B-PD:nppukp	Secure digital controller 1 data bit 5
AF39	SDC1_DATA_6		P7	B-PD:nppukp	Secure digital controller 1 data bit 6
AF35	SDC1_DATA_7		P7	B-PD:nppukp	Secure digital controller 1 data bit 7

Table 2-4 Pin descriptions – connectivity functions (cont.)

Pad #	Pad name and/or function	Pad name or alt function	Pad characteristics		Functional description
			Voltage	Type	
Secure digital controller 2 (SDC2) interface – supports dual-voltage SD 3.0					
R4	SDC2_CLK		P2	BH-NP:pdpukp	Secure digital controller 2 clock
N6	SDC2_CMD		P2	BH-PD:nppukp	Secure digital controller 2 command
P3	SDC2_DATA_0		P2	BH-PD:nppukp	Secure digital controller 2 data bit 0
R6	SDC2_DATA_1		P2	BH-PD:nppukp	Secure digital controller 2 data bit 1
T7	SDC2_DATA_2		P2	BH-PD:nppukp	Secure digital controller 2 data bit 2
P7	SDC2_DATA_3		P2	BH-PD:nppukp	Secure digital controller 2 data bit 3
B37	SD_CARD_DET_N	GPIO_38	P3	DI PD:nppukp	Secure digital card detection Configurable I/O
G38	SD_WRITE_PROTECT	GPIO_121	P3	DI PD:nppukp	Secure digital card write protection Configurable I/O
Secure digital controller interfaces – common to all SDCs					
V9	VREF_PADS			AI	Reference for secure digital I/O pads
Dual-voltage UIM interfaces					
G40	UIM1_DATA	GPIO_57	P5	B PD:nppukp	UIM1 data Configurable I/O
J40	UIM1_CLK	GPIO_58	P5	DO PD:nppukp	UIM1 clock Configurable I/O
L38	UIM1_RESET	GPIO_59	P5	DO PD:nppukp	UIM1 reset Configurable I/O
Y39	UIM1_PRESENT	GPIO_60	P3	DI PD:nppukp	UIM1 removal detection Configurable I/O
L40	UIM2_DATA	GPIO_53	P6	B PD:nppukp	UIM2 data Configurable I/O
K39	UIM2_CLK	GPIO_54	P6	DO PD:nppukp	UIM2 clock Configurable I/O
H39	UIM2_RESET	GPIO_55	P6	DO PD:nppukp	UIM2 reset Configurable I/O
AA36	UIM2_PRESENT	GPIO_56	P3	DI PD:nppukp	UIM2 removal detection Configurable I/O
Y37	UIM3_DATA	GPIO_49	P4	B PD:nppukp	UIM3 data Configurable I/O
AA34	UIM3_CLK	GPIO_50	P4	DO PD:nppukp	UIM3 clock Configurable I/O
Y35	UIM3_RESET	GPIO_51	P4	DO PD:nppukp	UIM3 reset Configurable I/O
AA38	UIM3_PRESENT	GPIO_52	P3	DI PD:nppukp	UIM3 removal detection Configurable I/O
AL38	UIM_BATT_ALARM	GPIO_61	P3	DI PD:nppukp	UIM battery alarm Configurable I/O
Y33	VREF_PADS			AI	Reference for UIM I/O pads

Table 2-4 Pin descriptions – connectivity functions (cont.)

Pad #	Pad name and/or function	Pad name or alt function	Pad characteristics		Functional description
			Voltage	Type	
Sensors and keypad buttons					
G34	SMB_INT	GPIO_62	P3	DI B-PD:nppukp	SMB interrupt Configurable I/O
L36	MAG_INT	GPIO_69	P3	DI B-PD:nppukp	magnetometer interrupt Configurable I/O
E38	GYRO_ACCEL_INT_N	GPIO_115	P3	DI B-PD:nppukp	Gyro interrupt Configurable I/O
H33	KYPD_SNS0	GPIO_107	P3	DI B-PD:nppukp	Keypad sense bit 0 Configurable I/O
K35	KYPD_SNS1	GPIO_108	P3	DI B-PD:nppukp	Keypad sense bit 1 Configurable I/O
J34	KYPD_SNS2	GPIO_109	P3	DI B-PD:nppukp	Keypad sense bit 2 Configurable I/O
BAM-based low-speed peripheral interface 1 – see Table 2-6 for application-specific pin assignments					
BA38	BLSP1_3	GPIO_0	P3	B PD:nppukp	BLSP 1 bit 3; UART or SPI Configurable I/O
BB39	BLSP1_2	GPIO_1	P3	B PD:nppukp	BLSP 1 bit 2; UART or SPI Configurable I/O
AV35	BLSP1_1	GPIO_2	P3	B PD:nppukp	BLSP 1 bit 1; UART, SPI, or I2C Configurable I/O
AY37	BLSP1_0	GPIO_3	P3	B PD:nppukp	BLSP 1 bit 0; UART, SPI, or I2C Configurable I/O
BAM-based low-speed peripheral interface 2 – see Table 2-6 for application-specific pin assignments					
AT9	BLSP2_3	GPIO_4	P3	B PD:nppukp	BLSP 2 bit 3; UART or SPI Configurable I/O
AY1	BLSP2_2	GPIO_5	P3	B PD:nppukp	BLSP 2 bit 2; UART or SPI Configurable I/O
AY3	BLSP2_1	GPIO_6	P3	B PD:nppukp	BLSP 2 bit 1; UART, SPI, or I2C Configurable I/O
AV3	BLSP2_0	GPIO_7	P3	B PD:nppukp	BLSP 2 bit 0; UART, SPI, or I2C Configurable I/O
BAM-based low-speed peripheral interface 3 – see Table 2-6 for application-specific pin assignments					
H5	BLSP3_3	GPIO_8	P3	B PD:nppukp	BLSP 3 bit 3; SPI Configurable I/O
G2	BLSP3_2	GPIO_9	P3	B PD:nppukp	BLSP 3 bit 2; SPI Configurable I/O
H1	BLSP3_1	GPIO_10	P3	B PD:nppukp	BLSP 3 bit 1; SPI, or I2C Configurable I/O
E2	BLSP3_0	GPIO_11	P3	B PD:nppukp	BLSP 3 bit 0; SPI, or I2C Configurable I/O

Table 2-4 Pin descriptions – connectivity functions (cont.)

Pad #	Pad name and/or function	Pad name or alt function	Pad characteristics		Functional description
			Voltage	Type	
BAM-based low-speed peripheral interface 4 – see Table 2-6 for application-specific pin assignments					
AM39	BLSP4_3	GPIO_12	P3	B PD:nppukp	BLSP 4 bit 3; SPI Configurable I/O
AM35	BLSP4_2	GPIO_13	P3	B PD:nppukp	BLSP 4 bit 2; SPI Configurable I/O
AN40	BLSP4_1	GPIO_14	P3	B PD:nppukp	BLSP 4 bit 1; SPI, or I2C Configurable I/O
AN36	BLSP4_0	GPIO_15	P3	B PD:nppukp	BLSP 4 bit 0; SPI, or I2C Configurable I/O
BAM-based low-speed peripheral interface 5 – see Table 2-6 for application-specific pin assignments					
K7	BLSP5_3	GPIO_16	P3	B PD:nppukp	BLSP 5 bit 3; SPI Configurable I/O
G6	BLSP5_2	GPIO_17	P3	B PD:nppukp	BLSP 5 bit 2; SPI Configurable I/O
J6	BLSP5_1	GPIO_18	P3	B PD:nppukp	BLSP 5 bit 1; SPI, or I2C Configurable I/O
J4	BLSP5_0	GPIO_19	P3	B PD:nppukp	BLSP 5 bit 0; SPI, or I2C Configurable I/O
BAM-based low-speed peripheral interface 6 – see Table 2-6 for application-specific pin assignments					
AY7	BLSP6_3	GPIO_20	P3	B PD:nppukp	BLSP 6 bit 3; SPI Configurable I/O
AW6	BLSP6_3	GPIO_21	P3	B PD:nppukp	BLSP 6 bit 2; SPI Configurable I/O
AV7	BLSP6_3	GPIO_22	P3	B PD:nppukp	BLSP 6 bit 1; SPI, or I2C Configurable I/O
BA2	BLSP6_3	GPIO_23	P3	B PD:nppukp	BLSP 3 bit 0; SPI, or I2C Configurable I/O
Serial peripheral interface (SPI) extra chip selects (supplements BLSP ports configured for SPI protocol) signals					
AT9	BLSP1_SPI_CS3_N	GPIO_4	P3	B PD:nppukp	BLSP 1 Chip select 3 Configurable I/O
AY1	BLSP2_SPI_CS3_N	GPIO_5	P3	B PD:nppukp	BLSP 2Chip select 3 Configurable I/O
K7	BLSP1_SPI_CS2_N	GPIO_16	P3	B PD:nppukp	BLSP 1 Chip select 2 Configurable I/O
G6	BLSP2_SPI_CS2_N	GPIO_17	P3	B PD:nppukp	BLSP 2 Chip select 2 Configurable I/O
E4	BLSP3_SPI_CS2_N	GPIO_37	P3	B PD:nppukp	BLSP 3 Chip select 2 Configurable I/O
L36	BLSP3_SPI_CS3_N	GPIO_69	P3	B PD:nppukp	BLSP 3 Chip select 3 Configurable I/O
B39	BLSP1_SPI_CS1_N	GPIO_110	P3	B PD:nppukp	BLSP 1 Chip select 1 Configurable I/O

Table 2-4 Pin descriptions – connectivity functions (cont.)

Pad #	Pad name and/or function	Pad name or alt function	Pad characteristics		Functional description
			Voltage	Type	
F39	BLSP3_SPI_CS1_N	GPIO_120	P3	B PD:nppukp	BLSP 3 Chip select 1 Configurable I/O
G38	BLSP2_SPI_CS1_N	GPIO_121	P3	B PD:nppukp	BLSP 2 Chip select 1 Configurable I/O
Audio clock					
AW38	MI2S_MCLK	GPIO_116	P3	B PD:nppukp	MI2S Master CLK signal Configurable I/O
Audio MI2S interface #1					
D39	MI2S_1_SCLK	GPIO_113	P3	B PD:nppukp	MI2S SCLK signal Configurable I/O
B39	MI2S_1_WS	GPIO_110	P3	B PD:nppukp	MI2S Word Select signal Configurable I/O
E40	MI2S_1_D0	GPIO_114	P3	B PD:nppukp	MI2S Data0 signal Configurable I/O
E38	MI2S_1_D1	GPIO_115	P3	B PD:nppukp	MI2S Data1 signal Configurable I/O
Audio MI2S interface #2					
AR36	MI2S_2_SCLK	GPIO_118	P3	B PD:nppukp	MI2S SCLK signal Configurable I/O
AV37	MI2S_2_WS	GPIO_117	P3	B PD:nppukp	MI2S Word Select signal Configurable I/O
BA40	MI2S_2_D0	GPIO_119	P3	B PD:nppukp	MI2S Data0 signal Configurable I/O
AW36	MI2S_2_D1	GPIO_112	P3	B PD:nppukp	MI2S Data1 signal Configurable I/O
Digital MIC interface					
BA38	DMIC0_CLK	GPIO_0	P3	DO PD:nppukp	Digital MIC0 clock Configurable I/O
BB39	DMIC0_DATA	GPIO_1	P3	B PD:nppukp	Digital MIC0 data Configurable I/O

BAM-enabled low-speed peripheral (BLSP)

The BAM integrates three serial bus cores: UART DM, SPI, and I2C. The SPI and I^2C cores are, in turn, integrated into a single core called the Qualcomm Unified Peripheral (QUP) where both the subcores share the same FIFO. The UARTDM is integrated separately with its own FIFO. All the cores share the same bus interface.

The external I/O ports of these cores are shared and only one of the cores can be used at any given time. However, in the mode where UARTDM is used as a two-pin UART interface, the I2C, which is also a two-pin interface, can be used simultaneously with UART functionality.

The BLSP supports the following serial protocols:

- UART_DM
- I2C (master only), driven by QUP
- SPI, driven by QUP

Detailed pin assignments are presented in Table 2-5 and Table 2-6.

Table 2-5 BLSP alternate function configurations

Pad name	Alternate function			
GPIO[0]	BLSP1_SPI_MOSI	BLSP1_UART_TX		
GPIO[1]	BLSP1_SPI_MISO	BLSP1_UART_RX		
GPIO[2]	BLSP1_SPI_CS_N	BLSP1_UART_CTS_N	BLSP1_I2C_SDA_A	
GPIO[3]	BLSP1_SPI_CLK	BLSP1_UART_RFR_N	BLSP1_I2C_SCL_A	
GPIO[4]	BLSP2_SPI_MOSI	BLSP2_UART_TX		
GPIO[5]	BLSP2_SPI_MISO	BLSP2_UART_RX		
GPIO[6]	BLSP2_SPI_CS_N	BLSP2_UART_CTS_N	BLSP2_I2C_SDA_A	
GPIO[7]	BLSP2_SPI_CLK	BLSP2_UART_RFR_N	BLSP2_I2C_SCL_A	
GPIO[8]	BLSP3_SPI_MOSI			
GPIO[9]	BLSP3_SPI_MISO			
GPIO[10]	BLSP3_SPI_CS_N		BLSP3_I2C_SDA_A	
GPIO[11]	BLSP3_SPI_CLK		BLSP2_I2C_SCL_A	
GPIO[12]	BLSP4_SPI_MOSI			
GPIO[13	BLSP4_SPI_MISO			
GPIO[14]	BLSP4_SPI_CS_N		BLSP4_I2C_SDA_A	
GPIO[15]	BLSP4_SPI_CLK		BLSP4_I2C_SCL_A	
GPIO[16]	BLSP5_SPI_MOSI			
GPIO[17]	BLSP5_SPI_MISO			
GPIO[18]	BLSP5_SPI_CS_N		BLSP5_I2C_SDA_B	
GPIO[19]	BLSP5_SPI_CLK		BLSP5_I2C_SCL_B	
GPIO[20]	BLSP6_SPI_MOSI			
GPIO[21]	BLSP6_SPI_MISO			
GPIO[22]	BLSP6_SPI_CS_N		BLSP6_I2C_SDA_A	
GPIO[23]	BLSP6_SPI_CLK		BLSP6_I2C_SCL_A	

Table 2-6 BLSP internal pin mapping

Pin	4-pin UART	I2C + GPIOs	I2C + 2-pin UART	4-pin SPI	4 GPIOs
3	UART_TX_DATA	GPIO_XX	UART_TX_DATA	SPI_MOSI_DATA	GPIO_XX
2	UART_RX_DATA	GPIO_XX	UART_RX_DATA	SPI_MISO_DATA	GPIO_XX
1	UART_CTS_N	I2C_DATA	I2C_DATA	SPI_CS_N	GPIO_XX
0	UART_RFR_N	I2C_CLK	I2C_CLK	SPI_CLK	GPIO_XX

Table 2-7 Pin descriptions – internal functions

Pad #	Pad name and/or function	Pad name or alt function	Pad characteristics		Functional description
			Voltage	Type	
JTAG interface					
K1	SRST_N		P3	PU	JTAG reset for debug
M1	TCK		P3	PU	JTAG clock input
M3	TDI		P3	PU:nppdkp	JTAG data input
J2	TDO		P3	-	JTAG data output
L2	TMS		P3	PU:nppdkp	JTAG mode-select input
K3	TRST_N		P3	PD	JTAG reset
General Purpose Clocks, PDM, and related signals					
AY7	GP_PDM_0A	GPIO_20	P3	DO B-PD:nppukp	General-purpose PDM output 0A, 12-bit, XO/4 clock Configurable I/O
AA38	GP_PDM_1A	GPIO_52	P3	DO B-PD:nppukp	General-purpose PDM output 1A, 12-bit, XO/4 clock Configurable I/O
AU4	GP_PDM_0B	GPIO_25	P3	DO B-PD:nppukp	General-purpose PDM output 0B, 12-bit, XO/4 clock Configurable I/O
AW6	GP_PDM_1B	GPIO_21	P3	DO B-PD:nppukp	General-purpose PDM output 1B, 12-bit, XO/4 clock Configurable I/O
A38	GP_PDM_2A	GPIO_98	P3	DO B-PD:nppukp	General-purpose PDM output 2A, 12-bit, XO/4 clock Configurable I/O
D39	GP_PDM_2B	GPIO_113	P3	DO B-PD:nppukp	General-purpose PDM output 2B, 12-bit, XO/4 clock Configurable I/O
D3	GP_CLK0	GPIO_31	P3	DO B-PD:nppukp	General-purpose clock 0 Configurable I/O
D1	GP_CLK1	GPIO_32	P3	DO B-PD:nppukp	General-purpose clock 1 Configurable I/O
Y37	GP_CLK_1A	GPIO_49	P4	DO B-PD:nppukp	General-purpose clock 1A Configurable I/O
AA34	GP_CLK_2A	GPIO_50	P4	DO B-PD:nppukp	General-purpose clock 2A Configurable I/O
Y35	GP_CLK_3A	GPIO_51	P4	DO B-PD:nppukp	General-purpose clock 3A Configurable I/O
C38	GP_CLK_1B	GPIO_97	P3	DO B-PD:nppukp	General-purpose clock 1B Configurable I/O
AM39	GP_CLK_2B	GPIO_12	P3	DO B-PD:nppukp	General-purpose clock 2B Configurable I/O

Table 2-7 Pin descriptions – internal functions (cont.)

Pad #	Pad name and/or function	Pad name or alt function	Pad characteristics		Functional description
			Voltage	Type	
AM35	GP_CLK_3B	GPIO_13	P3	DO B-PD:nppukp	General-purpose clock 3B Configurable I/O
B39	GP_MN	GPIO_110	P3	DO B-PD:nppukp	General-purpose M/N:D counter output Configurable I/O
Resets and mode controls					
AU32	MODE_0		P3	DIS-PD	Mode control bit 0, unconnected for native mode
AT31	MODE_1		P3	DIS-PD	Mode control bit 1, unconnected for native mode
AV1	RESOUT_N		P3	DO	Reset output
E4	FORCED_USB_BOOT	GPIO[37]	P3	DI B-PD:nppukp	Force USB boot control Configurable I/O
C38	BOOT_CONFIG[14]	GPIO[97]	P3	DI B-PD:nppukp	Boot configuration control bit 14 Configurable I/O
BC34	BOOT_CONFIG[13]	GPIO[94]	P3	DI B-PD:nppukp	Boot configuration control bit 13 Configurable I/O
BD33	BOOT_CONFIG[12]	GPIO[93]	P3	DI B-PD:nppukp	Boot configuration control bit 12 Configurable I/O
AY33	BOOT_CONFIG[11]	GPIO[92]	P3	DI B-PD:nppukp	Boot configuration control bit 11 Configurable I/O
BE38	BOOT_CONFIG[10]	GPIO[91]	P3	DI B-PD:nppukp	Boot configuration control bit 10 Configurable I/O
BA32	BOOT_CONFIG[9]	GPIO[90]	P3	DI B-PD:nppukp	Boot configuration control bit 9 Configurable I/O
BD35	BOOT_CONFIG[8]	GPIO[89]	P3	DI B-PD:nppukp	Boot configuration control bit 8 Configurable I/O
BB35	BOOT_CONFIG[7]	GPIO[88]	P3	DI B-PD:nppukp	Boot configuration control bit 7 Configurable I/O
BB37	BOOT_CONFIG[6]	GPIO[87]	P3	DI B-PD:nppukp	Boot configuration control bit 6 Configurable I/O
BD39	BOOT_CONFIG[5]	GPIO[86]	P3	DI B-PD:nppukp	Boot configuration control bit 5 Configurable I/O
BC8	BOOT_CONFIG[4]	GPIO[84]	P3	DI B-PD:nppukp	Boot configuration control bit 4 Configurable I/O
BC40	BOOT_CONFIG[3]	GPIO[83]	P3	DI B-PD:nppukp	Boot configuration control bit 3 Configurable I/O
BC38	BOOT_CONFIG[2]	GPIO[82]	P3	DI B-PD:nppukp	Boot configuration control bit 2 Configurable I/O
BD7	BOOT_CONFIG[1]	GPIO[81]	P3	DI B-PD:nppukp	Boot configuration control bit 1 Configurable I/O
BD5	BOOT_CONFIG[0]	GPIO[80]	P3	DI B-PD:nppukp	Boot configuration control bit 0 Configurable I/O

GPIO functions with output options like ‘A’, ‘B’, etc use the same core circuits

These options are created by output multiplexing

Software must select just one output (such as the ‘A’ output or the ‘B’ output); multiple outputs for the same function are not available simultaneously

Multiple options are provided to increase GPIO assignment flexibility

Multiple output options are available for the following functions:

GP_PDM_2
GP_PDM_1
GP_PDM_0

GP_PDM signals are an example

GP_CLK_3
GP_CLK_2
GP_CLK_1

QDSS trace (16 bits, clock, control, trigger in, and trigger out)

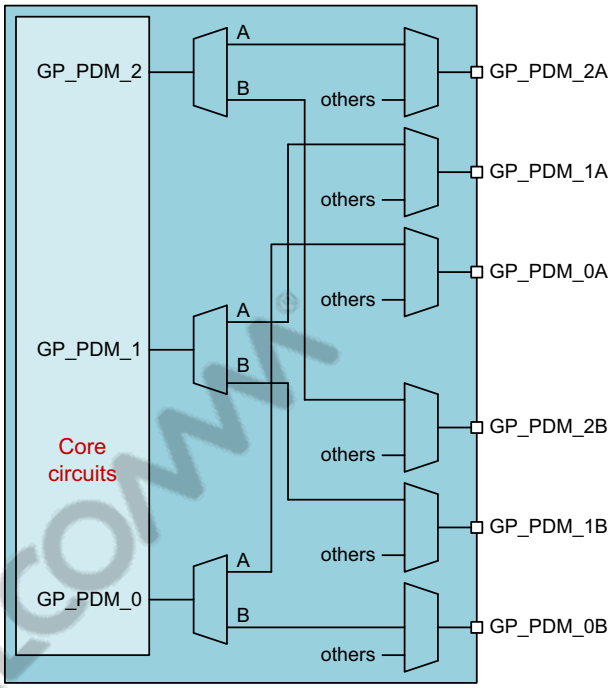

Figure 2-3 GPIO ‘A/B’ multiplexing

Table 2-8 MSM8x16 wakeup pins for modem power management (MPM)

Pad #	Pad name	Pad characteristics [1]		Wakeup functional description
		Voltage	Type	
BB39	GPIO_1	P3	B-PD:nppukp	General purpose wakeup
AY1	GPIO_5	P3	B-PD:nppukp	General purpose wakeup
G2	GPIO_9	P3	B-PD:nppukp	General purpose wakeup
E2	GPIO_11	P3	B-PD:nppukp	General-purpose wakeup
AM39	GPIO_12	P3	B-PD:nppukp	General-purpose wakeup
AM35	GPIO_13	P3	B-PD:nppukp	General-purpose wakeup
AY7	GPIO_20	P3	B-PD:nppukp	General-purpose wakeup
AW6	GPIO_21	P3	B-PD:nppukp	General-purpose wakeup
AU4	GPIO_25	P3	B-PD:nppukp	General-purpose wakeup
F1	GPIO_28	P3	B-PD:nppukp	General-purpose wakeup
D3	GPIO_31	P3	B-PD:nppukp	General-purpose wakeup
F5	GPIO_34	P3	B-PD:nppukp	General-purpose wakeup
A4	GPIO_35	P3	B-PD:nppukp	General-purpose wakeup
C4	GPIO_36	P3	B-PD:nppukp	General-purpose wakeup

Table 2-8 MSM8x16 wakeup pins for modem power management (MPM) (cont.)

Pad #	Pad name	Pad characteristics [1]		Wakeup functional description
		Voltage	Type	
E4	GPIO_37	P3	B-PD:nppukp	General-purpose wakeup
B37	GPIO_38	P3	B-PD:nppukp	General-purpose wakeup
Y37	GPIO_49	P4	B-PD:nppukp	General-purpose wakeup
AA34	GPIO_50	P4	B-PD:nppukp	General-purpose wakeup
Y35	GPIO_51	P4	B-PD:nppukp	General-purpose wakeup
AA38	GPIO_52	P3	B-PD:nppukp	General-purpose wakeup
K39	GPIO_54	P3	B-PD:nppukp	General-purpose wakeup
G34	GPIO_62	P3	B-PD:nppukp	General-purpose wakeup
AJ38	GPIO_66	P3	B-PD:nppukp	General-purpose wakeup
AL40	GPIO_68	P3	B-PD:nppukp	General-purpose wakeup
L36	GPIO_69	P3	B-PD:nppukp	General-purpose wakeup
C38	GPIO_97	P3	B-PD:nppukp	General-purpose wakeup
A38	GPIO_98	P3	B-PD:nppukp	General-purpose wakeup
H33	GPIO_107	P3	B-PD:nppukp	General-purpose wakeup
K35	GPIO_108	P3	B-PD:nppukp	General-purpose wakeup
J34	GPIO_109	P3	B-PD:nppukp	General-purpose wakeup
B39	GPIO_110	P3	B-PD:nppukp	General-purpose wakeup
C40	GPIO_111	P3	B-PU:nppukp	General-purpose wakeup
AW36	GPIO_112	P3	B-PD:nppukp	General-purpose wakeup
D39	GPIO_113	P3	B-PD:nppukp	General-purpose wakeup
E40	GPIO_114	P3	B-PD:nppukp	General-purpose wakeup
E38	GPIO_115	P3	B-PD:nppukp	General-purpose wakeup
AV37	GPIO_117	P3	B-PD:nppukp	General-purpose wakeup
AR36	GPIO_118	P3	B-PD:nppukp	General-purpose wakeup
F39	GPIO_120	P3	B-PD:nppukp	General-purpose wakeup
G38	GPIO_121	P3	B-PD:nppukp	General-purpose wakeup
AE38	SDC1_DATA_1	P7	BH-PD:nppukp	SDIO wakeup
AH37	SDC1_DATA_3	P7	BH-PD:nppukp	SD card detect
R6	SDC2_DATA_1	P2	BH-PD:nppukp	SDIO wakeup
P7	SDC2_DATA_3	P2	BH-PD:nppukp	SD card detect
K1	SRST_N	P3	DI	JTAG

1. Refer to Table 2-1 for parameter and acronym definitions.

Table 2-9 Pin descriptions – chipset interface functions

Pad #	Pad name and/or function	Pad name or alt function	Pad characteristics		Functional description
			Voltage	Type	
RFIC – Rx baseband interfaces					
BD21	BBRX_IM_CH0		-	AI	Baseband receiver input, in-phase minus, channel 0
AY19	BBRX_IM_CH1		-	AI	Baseband receiver input, in-phase minus, channel 1
BC16	BBRX_IM_CH2		-	AI	Baseband receiver input, in-phase minus, channel 2
BB21	BBRX_IP_CH0		-	AI	Baseband receiver input, in-phase plus, channel 0
BA20	BBRX_IP_CH1		-	AI	Baseband receiver input, in-phase plus, channel 1
BB15	BBRX_IP_CH2		-	AI	Baseband receiver input, in-phase plus, channel 2
BE20	BBRX_QM_CH0		-	AI	Baseband receiver input, quadrature minus, channel 0
BA18	BBRX_QM_CH1		-	AI	Baseband receiver input, quadrature minus, channel 1
BE14	BBRX_QM_CH2		-	AI	Baseband receiver input, quadrature minus, channel 2
BC20	BBRX_QP_CH0		-	AI	Baseband receiver input, quadrature plus, channel 0
BB17	BBRX_QP_CH1		-	AI	Baseband receiver input, quadrature plus, channel 1
BD15	BBRX_QP_CH2		-	AI	Baseband receiver input, quadrature plus, channel 2
RFIC – GNSS Rx baseband interface					
BE12	GNSS_BB_IP		-	AI	GNSS receiver baseband input, in-phase plus
BD11	GNSS_BB_IM		-	AI	GNSS receiver baseband input, in-phase minus
BC14	GNSS_BB_QP		-	AI	GNSS receiver baseband input, quadrature plus
BB13	GNSS_BB_QM		-	AI	GNSS receiver baseband input, quadrature minus
RFIC – Tx baseband interfaces					
BA26	TX_DAC0_IM		-	AO	Transmitter DAC 0 output, in-phase minus
AY27	TX_DAC0_IP		-	AO	Transmitter DAC 0 output, in-phase plus
AU26	TX_DAC0_IREF		-	AI	Transmitter DAC 0 current reference
BE26	TX_DAC0_QM		-	AO	Transmitter DAC 0 output, quadrature minus
BD25	TX_DAC0_QP		-	AO	Transmitter DAC 0 output, quadrature plus
AR26	TX_DAC0_VREF		-	AI	Transmitter DAC 0 voltage reference
BE24	TX_DAC1_IM		-	AO	Transmitter DAC 1 output, in-phase minus
BC24	TX_DAC1_IP		-	AO	Transmitter DAC 1 output, in-phase plus
AT23	TX_DAC1_IREF		-	AI	Transmitter DAC 1 current reference
AY23	TX_DAC1_QM		-	AO	Transmitter DAC 1 output, quadrature minus
BB23	TX_DAC1_QP		-	AO	Transmitter DAC 1 output, quadrature plus
AU22	TX_DAC1_VREF		-	AI	Transmitter DAC 1 voltage reference
RFIC – GSM transmit phase adjust signals					
BE34	GSM0_TX_PHASE_D0	GPIO_99	P3	DO-Z B-PD:nppukp	GSM0 transmit phase adjust data bit 0 Configurable I/O
BE36	GSM0_TX_PHASE_D1	GPIO_100	P3	DO-Z B-PD:nppukp	GSM0 transmit phase adjust data bit 1 Configurable I/O
BB33	GSM1_TX_PHASE_D0	GPIO_101	P3	DO-Z B-PD:nppukp	GSM1 transmit phase adjust data bit 0 Configurable I/O

Table 2-9 Pin descriptions – chipset interface functions (cont.)

Pad #	Pad name and/or function	Pad name or alt function	Pad characteristics		Functional description
			Voltage	Type	
BE32	GSM1_TX_PHASE_D1	GPIO_102	P3	DO-Z B-PD:nppukp	GSM1 transmit phase adjust data bit 1 Configurable I/O
RFIC – status and control signals					
AT35	SSBI_WTR0_RX	GPIO_103	P3	B B-PD:nppukp	WTR0 receivers single-wire serial bus interface Configurable I/O
AW40	SSBI_WTR0_TX	GPIO_104	P3	B B-PD:nppukp	WTR0 transmitters single-wire serial bus interface Configurable I/O
AU36	SSBI_WTR1_RX	GPIO_105	P3	B B-PD:nppukp	WTR1 receivers single-wire serial bus interface Configurable I/O
AY39	SSBI_WTR1_TX	GPIO_106	P3	B B-PD:nppukp	WTR1 transmitters single-wire serial bus interface Configurable I/O
WCN – WLAN signals					
BD3	WLAN_DATA0	GPIO_42	P3	B B-PD:nppukp	WLAN data bit 0 Configurable I/O
BB1	WLAN_DATA1	GPIO_41	P3	B B-PD:nppukp	WLAN data bit 1 Configurable I/O
BB5	WLAN_DATA2	GPIO_40	P3	B B-PD:nppukp	WLAN data bit 2 Configurable I/O
BB3	WLAN_CLK	GPIO_44	P3	DO-Z B-PD:nppukp	WLAN Clock Configurable I/O
BA6	WLAN_SET	GPIO_43	P3	DO-Z B-PD:nppukp	WLAN Set Configurable I/O
AR14	WLAN_BB_IM		-	AI, AO	WLAN baseband Rx/Tx switched, in-phase minus
AP15	WLAN_BB_IP		-	AI, AO	WLAN baseband Rx/Tx switched, in-phase plus
AP13	WLAN_BB_QM		-	AI, AO	WLAN baseband Rx/Tx switched, quadrature minus
AR12	WLAN_BB_QP		-	AI, AO	WLAN baseband Rx/Tx switched, quadrature plus
AU14	WLAN_REXT		-	AI	WLAN external resistor
AR8	WLAN_XO		-	DI	WLAN clock
WCN – Bluetooth signals					
AW8	BT_DATA	GPIO_48	P3	B B-PD:nppukp	Bluetooth dual-function signal – serial data and strobe Configurable I/O
BA4	BT_CTL	GPIO_47	P3	DO B-PD:nppukp	Bluetooth control Configurable I/O
BC2	BT_SSBI	GPIO_39	P3	B B-PD:nppukp	Bluetooth single-wire serial bus interface Configurable I/O
WCN – FM signals					
AY9	FM_DATA	GPIO_46	P3	B B-PD:nppukp	FM radio serial data interface Configurable I/O
AY5	FM_SSBI	GPIO_45	P3	B B-PD:nppukp	FM radio single-wire serial bus interface Configurable I/O

Table 2-9 Pin descriptions – chipset interface functions (cont.)

Pad #	Pad name and/or function	Pad name or alt function	Pad characteristics		Functional description
			Voltage	Type	
PMIC interfaces					
AK37	PMIC_SPMI_CLK		P3	DO	Slave and PBUS interface for PMICs – clock
AJ36	PMIC_SPMI_DATA		P3	B	Slave and PBUS interface for PMICs – data
E36	PS_HOLD		P3	DO	Power-supply hold signal to PMIC
F35	RESIN_N		P3	DI	Reset input
G36	SLEEP_CLK		P3	DI	Sleep clock
AL34	CXO		P3	DI	Core crystal oscillator (system clock at 19.2 MHz
A36	CXO_EN		P3	DO	Core crystal oscillator enable
General RF control (GRFC) signals					
AP37	GRFC_0	GPIO_74	P3	B PD:nppukp	Generic RF controller bit 0 Configurable I/O
AV39	GRFC_1	GPIO_75	P3	B PD:nppukp	Generic RF controller bit 1 Configurable I/O
AP35	GRFC_2	GPIO_76	P3	B PD:nppukp	Generic RF controller bit 2 Configurable I/O
BC4	GRFC_3	GPIO_77	P3	B PD:nppukp	Generic RF controller bit 3 Configurable I/O
BE4	GRFC_4	GPIO_78	P3	B PD:nppukp	Generic RF controller bit 4 Configurable I/O
BC6	GRFC_5	GPIO_79	P3	B PD:nppukp	Generic RF controller bit 5 Configurable I/O
BD5	GRFC_6	GPIO_80	P3	B PD:nppukp	Generic RF controller bit 6 Configurable I/O
BD7	GRFC_7	GPIO_81	P3	B PD:nppukp	Generic RF controller bit 7 Configurable I/O
BC38	GRFC_8	GPIO_82	P3	B PD:nppukp	Generic RF controller bit 8 Configurable I/O
BC40	GRFC_9	GPIO_83	P3	B PD:nppukp	Generic RF controller bit 9 Configurable I/O
BC8	GRFC_10	GPIO_84	P3	B PD:nppukp	Generic RF controller bit 10 Configurable I/O
BE6	GRFC_11	GPIO_85	P3	B PD:nppukp	Generic RF controller bit 11 Configurable I/O
BD39	GRFC_12	GPIO_86	P3	B PD:nppukp	Generic RF controller bit 12 Configurable I/O
BB37	GRFC_13	GPIO_87	P3	B PD:nppukp	Generic RF controller bit 13 Configurable I/O
BB35	GRFC_14	GPIO_88	P3	B PD:nppukp	Generic RF controller bit 14 Configurable I/O
BD35	GRFC_15	GPIO_89	P3	B PD:nppukp	Generic RF controller bit 15 Configurable I/O

Table 2-9 Pin descriptions – chipset interface functions (cont.)

Pad #	Pad name and/or function	Pad name or alt function	Pad characteristics		Functional description
			Voltage	Type	
BA32	GRFC_16	GPIO_90	P3	B PD:nppukp	Generic RF controller bit 16 Configurable I/O
BE38	GRFC_17	GPIO_91	P3	B PD:nppukp	Generic RF controller bit 17 Configurable I/O
AY33	GRFC_18	GPIO_92	P3	B PD:nppukp	Generic RF controller bit 18 Configurable I/O
BD33	GRFC_19	GPIO_93	P3	B PD:nppukp	Generic RF controller bit 19 Configurable I/O
BC34	GRFC_20	GPIO_94	P3	B PD:nppukp	Generic RF controller bit 20 Configurable I/O
BB31	GRFC_21	GPIO_95	P3	B PD:nppukp	Generic RF controller bit 21 Configurable I/O
Qualcomm RFFE interfaces					
AN38	RFFE1_CLK	GPIO_70	P3	DO PD:nppukp	RF front end clock 1 Configurable I/O
AR38	RFFE1_DATA	GPIO_71	P3	B PD:nppukp	RF front end data 1 Configurable I/O
AT39	RFFE2_CLK	GPIO_72	P3	DO PD:nppukp	RF front end clock 2 Configurable I/O
AU40	RFFE2_DATA	GPIO_73	P3	B PD:nppukp	RF front end data 2 Configurable I/O
AP37	RFFE3_CLK	GPIO_74	P3	DO PD:nppukp	RF front end clock 3 Configurable I/O
AP35	RFFE3_DATA	GPIO_76	P3	B PD:nppukp	RF front end data 3 Configurable I/O
AU36	RFFE4_CLK	GPIO_105	P3	DO PD:nppukp	RF front end clock 4 Configurable I/O
AY39	RFFE4_DATA	GPIO_106	P3	B PD:nppukp	RF front end data 4 Configurable I/O
AT35	RFFE5_CLK	GPIO_103	P3	DO PD:nppukp	RF front end clock 5 Configurable I/O
AW40	RFFE5_DATA	GPIO_104	P3	B PD:nppukp	RF front end data 5 Configurable I/O
GPS Control					
BC32	EXT_GPS_LNA_EN	GPIO_96	P3	DO PD:nppukp	EXT_GPS_LNA_EN Configurable I/O

Table 2-10 Pin descriptions – general-purpose input/output ports

Pad #	Pad name	Configurable function	Pad characteristics		Functional description
			Voltage	Type	
BA38	GPIO_0		P3	B-PD:nppukp	Configurable I/O
		BLSP1_3		B	BLSP #1, bit 3; UART or SPI
		DMIC0_CLK		DO	Digital MIC0 clock
BB39	GPIO_1		P3	B-PD:nppukp	Configurable I/O
		BLSP1_2		B	BLSP #1, bit 2; UART or SPI
		DMIC0_DATA		DI	Digital MIC0 data
AV35	GPIO_2		P3	B-PD:nppukp	Configurable I/O
		BLSP1_1		B	BLSP #1, bit 1; UART, SPI or I2C
AY37	GPIO_3		P3	B-PD:nppukp	Configurable I/O
		BLSP1_0		B	BLSP #1, bit 0; UART, SPI or I2C
AT9	GPIO_4		P3	B-PD:nppukp	Configurable I/O
		BLSP2_3		B	BLSP #2, bit 3; UART or SPI
		BLSP1_SPI_CS3_N		DO	Chip select 3 for SPI on BLSP1
AY1	GPIO_5		P3	B-PD:nppukp	Configurable I/O
		BLSP2_2		B	BLSP #2, bit 2; UART or SPI
		BLSP2_SPI_CS3_N		DO	Chip select 3 for SPI on BLSP2
AY3	GPIO_6		P3	B-PD:nppukp	Configurable I/O
		BLSP2_1		B	BLSP #2, bit 1; UART, SPI, or I2C
AV3	GPIO_7		P3	B-PD:nppukp	Configurable I/O
		BLSP2_0		B	BLSP #2, bit 0; UART, SPI, or I2C
H5	GPIO_8		P3	B-PD:nppukp	Configurable I/O
		BLSP3_3		B	BLSP #3, bit 3; SPI, or I2C
G2	GPIO_9		P3	B-PD:nppukp	Configurable I/O
		BLSP3_2		B	BLSP #3, bit 2; SPI, or I2C
H1	GPIO_10		P3	B-PD:nppukp	Configurable I/O
		BLSP3_1		B	BLSP #3, bit 1; SPI, or I2C
E2	GPIO_11		P3	B-PD:nppukp	Configurable I/O
		BLSP3_0		B	BLSP #3, bit 0; SPI, or I2C
AM39	GPIO_12		P3	B-PD:nppukp	Configurable I/O
		BLSP4_3		B	BLSP #4, bit 3; SPI, or I2C
		GP_CLK_2B		DO	General-purpose clock output 2B
AM35	GPIO_13		P3	B-PD:nppukp	Configurable I/O
		BLSP4_2		B	BLSP #4, bit 2; SPI, or I2C
		GP_CLK_3B		DO	General-purpose clock output 3B
AN40	GPIO_14		P3	B-PD:nppukp	Configurable I/O
		BLSP4_1		B	BLSP #4, bit 1; SPI, or I2C
AN36	GPIO_15		P3	B-PD:nppukp	Configurable I/O
		BLSP4_0		B	BLSP #4, bit 0; SPI, or I2C
K7	GPIO_16		P3	B-PD:nppukp	Configurable I/O
		BLSP5_3		B	BLSP #5, bit 3; SPI, or I2C
		BLSP1_SPI_CS2_N		DO	Chip select 2 for SPI on BLSP1
G6	GPIO_17		P3	B-PD:nppukp	Configurable I/O
		BLSP5_2		B	BLSP #5, bit 2; SPI, or I2C
		BLSP2_SPI_CS2_N		DO	Chip select 2 for SPI on BLSP1

Table 2-10 Pin descriptions – general-purpose input/output ports (cont.)

Pad #	Pad name	Configurable function	Pad characteristics		Functional description
			Voltage	Type	
J6	GPIO_18	BLSP5_1	P3	B-PD:nppukp B	Configurable I/O BLSP #5, bit 1; SPI, or I2C
J4	GPIO_19	BLSP5_0	P3	B-PD:nppukp B	Configurable I/O BLSP #5, bit 0; SPI, or I2C
AY7	GPIO_20	BLSP6_3 GP_PDM_0A	P3	B-PD:nppukp B DO	Configurable I/O BLSP #6, bit 3; SPI, or I2C General-purpose PDM output 0A, 12-bit, XO/4 clock
AW6	GPIO_21	BLSP6_2 GP_PDM_1B	P3	B-PD:nppukp B DO	Configurable I/O BLSP #6, bit 2; SPI, or I2C General-purpose PDM output 1B, 12-bit, XO/4 clock
AV7	GPIO_22	BLSP6_1	P3	B-PD:nppukp B	Configurable I/O BLSP #6, bit 1; SPI, or I2C
BA2	GPIO_23	BLSP6_0	P3	B-PD:nppukp B	Configurable I/O BLSP #6, bit 0; SPI, or I2C
AT5	GPIO_24	MDP_VSYNC_P	P3	B-PD:nppukp DI	Configurable I/O MDP vertical sync – primary
AU4	GPIO_25	DSI_RST_N GP_PDM_0B	P3	B-PD:nppukp DO DO	Configurable I/O Display reset General-purpose PDM output 0B, 12-bit, XO/4 clock
H3	GPIO_26	CAM_MCLK0	P3	B-PD:nppukp DO	Configurable I/O Camera master clock 0
C2	GPIO_27	CAM_MCLK1	P3	B-PD:nppukp DO	Configurable I/O Camera master clock 1
F1	GPIO_28	CAM1_RST_N	P3	B-PD:nppukp DO	Configurable I/O Camera 1 (front camera) reset
B3	GPIO_29	CAM_I2C_SDA	P3	B-PD:nppukp B	Configurable I/O Camera control interface I2C 0 serial data
F3	GPIO_30	CAM_I2C_SCL	P3	B-PD:nppukp B	Configurable I/O Camera control interface I2C 0 serial Clock
D3	GPIO_31	CCI_TIMER0 GP_CLK0	P3	B-PD:nppukp DO DO	Configurable I/O Camera control interface timer 0 General-purpose clock 0
D1	GPIO_32	CCI_TIMER1 GP_CLK1	P3	B-PD:nppukp DO DO	Configurable I/O Camera control interface timer 1 General-purpose clock 1
G4	GPIO_33	CCI_ASYNC0	P3	B-PD:nppukp DI	Configurable I/O Camera control interface async 0
F5	GPIO_34	CAM0_STANDBY_N	P3	B-PD:nppukp DO	Configurable I/O Camera 0 (rear camera) standby
A4	GPIO_35	CAM0_RST_N	P3	B-PD:nppukp DO	Configurable I/O Camera 0 (rear camera) reset

Table 2-10 Pin descriptions – general-purpose input/output ports (cont.)

Pad #	Pad name	Configurable function	Pad characteristics		Functional description
			Voltage	Type	
C4	GPIO_36	FLASH_LED_RESET	P3	B-PD:nppukp DO	Configurable I/O LED Flash reset
E4	GPIO_37	BLSP3_SPI_CS2_N FORCED_USB_BOOT	P3	B-PD:nppukp DO DI	Configurable I/O Chip select 2 for SPI on BLSP3 Force USB boot control
B37	GPIO_38	SD_CARD_DET_N CCI_TIMER2	P3	B-PD:nppukp DI DO	Configurable I/O Secure digital card detection Camera control interface timer 2
BC2	GPIO_39	BT_SSBI	P3	B-PD:nppukp B	Configurable I/O Bluetooth single-wire serial bus interface
BB5	GPIO_40	WLAN_DATA2	P3	B-PD:nppukp B	Configurable I/O WLAN data bit 2
BB1	GPIO_41	WLAN_DATA1	P3	B-PD:nppukp B	Configurable I/O WLAN data bit 1
BD3	GPIO_42	WLAN_DATA0	P3	B-PD:nppukp B	Configurable I/O WLAN data bit 0
BA6	GPIO_43	WLAN_SET	P3	B-PD:nppukp DO-Z	Configurable I/O WLAN set
BB3	GPIO_44	WLAN_CLK	P3	B-PD:nppukp DO-Z	Configurable I/O WLAN clock
AY5	GPIO_45	FM_SSBI	P3	B-PD:nppukp B	Configurable I/O FM-radio SSBI
AY9	GPIO_46	FM_DATA	P3	B-PD:nppukp B	Configurable I/O FM radio serial data interface
BA4	GPIO_47	BT_CTL	P3	B-PD:nppukp DO	Configurable I/O Bluetooth control
AW8	GPIO_48	BT_DATA	P3	B-PD:nppukp B	Configurable I/O Bluetooth dual function: data and strobe
Y37	GPIO_49	UIM3_DATA GP_CLK_1A	P4	B-PD:nppukp B DO	Configurable I/O UIM3 data General-purpose clock output 1A
AA34	GPIO_50	UIM3_CLK GP_CLK_2A	P4	B-PD:nppukp DO DO	Configurable I/O UIM3 clock General-purpose clock output 2A
Y35	GPIO_51	UIM3_RST GP_CLK_3A	P4	B-PD:nppukp DO DO	Configurable I/O UIM3 reset General-purpose clock output 3A
AA38	GPIO_52	UIM3_PRESENT GP_PDM_1A	P3	B-PD:nppukp DI DO	Configurable I/O UIM3 removal detection General-purpose PDM output 1A, 12-bit, XO/4 clock
L40	GPIO_53	UIM2_DATA	P6	B-PD:nppukp B	Configurable I/O UIM2 data
K39	GPIO_54	UIM2_CLK	P6	B-PD:nppukp DO	Configurable I/O UIM2 clock

Table 2-10 Pin descriptions – general-purpose input/output ports (cont.)

Pad #	Pad name	Configurable function	Pad characteristics		Functional description
			Voltage	Type	
H39	GPIO_55	UIM2_RST	P6	B-PD:nppukp DO	Configurable I/O UIM2 reset
AA36	GPIO_56	UIM2_PRESENT	P3	B-PD:nppukp DI	Configurable I/O UIM2 removal detection
G40	GPIO_57	UIM1_DATA	P5	B-PD:nppukp B	Configurable I/O UIM1 data
J40	GPIO_58	UIM1_CLK	P5	B-PD:nppukp DO	Configurable I/O UIM1 clock
L38	GPIO_59	UIM1_RST	P5	B-PD:nppukp DO	Configurable I/O UIM1 reset
Y39	GPIO_60	UIM1_PRESENT	P3	B-PD:nppukp DI	Configurable I/O UIM1 removal detection
AL38	GPIO_61	UIM_BATT_ALARM	P3	B-PD:nppukp DI	Configurable I/O UIM battery alarm
G34	GPIO_62	SMB_INT	P3	B-PD:nppukp DI	Configurable I/O SMB interrupt
AJ40	GPIO_63	CDC_PDM0_CLK	P3	B-PD:nppukp DO	Configurable I/O PDM0 Clock
AH39	GPIO_64	CDC_PDM0_SYNC	P3	B-PD:nppukp DO	Configurable I/O PDM0 sync signal
AK39	GPIO_65	CDC_PDM0_TX0	P3	B-PD:nppukp DI	Configurable I/O PDM0 Transmit signal 0
AJ38	GPIO_66	CDC_PDM0_RX0	P3	B-PD:nppukp DO	Configurable I/O PDM0 Receive signal 0
AK35	GPIO_67	CDC_PDM0_RX1	P3	B-PD:nppukp DO	Configurable I/O PDM0 Receive signal 1
AL40	GPIO_68	CDC_PDM0_RX2	P3	B-PD:nppukp DO	Configurable I/O PDM0 Receive signal 2
L36	GPIO_69	MAG_INT BLSP3_SPI_CS3_N	P3	B-PD:nppukp DI DO	Configurable I/O magnetometer interrupt Chip select 3 for SPI on BLSP3
AN38	GPIO_70	RFFE1_CLK	P3	B-PD:nppukp DO	Configurable I/O RF front end clock 1
AR38	GPIO_71	RFFE1_DATA	P3	B-PD:nppukp B	Configurable I/O RF front end data 1
AT39	GPIO_72	RFFE2_CLK	P3	B-PD:nppukp DO	Configurable I/O RF front end clock 2
AU40	GPIO_73	RFFE2_DATA	P3	B-PD:nppukp B	Configurable I/O RF front end data 2
AP37	GPIO_74	GRFC_0 PA_ON0 RFFE3_CLK	P3	B-PD:nppukp DO DO DO	Configurable I/O Generic RF controller bit 0 Power amplifier enable 0; only high for Tx RF front end clock 3

Table 2-10 Pin descriptions – general-purpose input/output ports (cont.)

Pad #	Pad name	Configurable function	Pad characteristics		Functional description
			Voltage	Type	
AV39	GPIO_75		P3	B-PD:nppukp	Configurable I/O
		GRFC_1		DO	Generic RF controller bit 1
		PA_ON1		DO	Power amplifier enable 1; only high for Tx
AP35	GPIO_76		P3	B-PD:nppukp	Configurable I/O
		GRFC_2		DO	Generic RF controller bit 2
		PA_ON2		DO	Power amplifier enable 2; only high for Tx
		RFFE3_DATA		B	RF front end data 3
BC4	GPIO_77		P3	B-PD:nppukp	Configurable I/O
		GRFC_3		DO	Generic RF controller bit 3
		PA_ON3		DO	Power amplifier enable 3; only high for Tx
BE4	GPIO_78		P3	B-PD:nppukp	Configurable I/O
		GRFC_4		DO	Generic RF controller bit 4
		PA_ON4		DO	Power amplifier enable 4; only high for Tx
BC6	GPIO_79		P3	B-PD:nppukp	Configurable I/O
		GRFC_5		DO	Generic RF controller bit 5
		PA_ON5		DO	Power amplifier enable 5; only high for Tx
BD5	GPIO_80		P3	B-PD:nppukp	Configurable I/O
		GRFC_6		DO	Generic RF controller bit 6
		BOOT_CONFIG_0 (WDOG_ DISABLE)		DI	Boot configuration control bit 0
BD7	GPIO_81		P3	B-PD:nppukp	Configurable I/O
		GRFC_7		DO	Generic RF controller bit 7
		BOOT_CONFIG_1		DI	Boot configuration control bit 1
BC38	GPIO_82		P3	B-PD:nppukp	Configurable I/O
		GRFC_8		DO	Generic RF controller bit 8
		BOOT_CONFIG_2		DI	Boot configuration control bit 2
		PA0_RANGE0		DO	PA set 0 range control bit 0
BC40	GPIO_83		P3	B-PD:nppukp	Configurable I/O
		GRFC_9		DO	Generic RF controller bit 9
		BOOT_CONFIG_3		DI	Boot configuration control bit 3
		PA0_RANGE1		DO	PA set 0 range control bit 1
BC8	GPIO_84		P3	B-PD:nppukp	Configurable I/O
		GRFC_10		DO	Generic RF controller bit 10
		BOOT_CONFIG_4		DI	Boot configuration control bit 4
BE6	GPIO_85		P3	B-PD:nppukp	Configurable I/O
		GRFC_11		DO	Generic RF controller bit 11
		SDC1_EMMC_1P2_EN		DI	Enables 1.2 V I/O for eMMC on SDC1
BD39	GPIO_86		P3	B-PD:nppukp	Configurable I/O
		GRFC_12		DO	Generic RF controller bit 12
		BOOT_CONFIG_5		DI	Boot configuration control bit 5
BB37	GPIO_87		P3	B-PD:nppukp	Configurable I/O
		GRFC_13		DO	Generic RF controller bit 13
		BOOT_CONFIG_6		DI	Boot configuration control bit 6
BB35	GPIO_88		P3	B-PD:nppukp	Configurable I/O
		GRFC_14		DO	Generic RF controller bit 14
		PA1_RANGE0		DO	PA set 1 range control bit 0
		BOOT_CONFIG_7		DI	Boot configuration control bit 7

Table 2-10 Pin descriptions – general-purpose input/output ports (cont.)

Pad #	Pad name	Configurable function	Pad characteristics		Functional description
			Voltage	Type	
BD35	GPIO_89		P3	B-PD:nppukp	Configurable I/O
		GRFC_15		DO	Generic RF controller bit 15
		PA1_RANGE1		DO	PA set 1 range control bit 1
		BOOT_CONFIG_8		DI	Boot configuration control bit 8
BA32	GPIO_90		P3	B-PD:nppukp	Configurable I/O
		GRFC_16		DO	Generic RF controller bit 16
		BOOT_CONFIG_9		DI	Boot configuration control bit 9
BE38	GPIO_91		P3	B-PD:nppukp	Configurable I/O
		GRFC_17		DO	Generic RF controller bit 17
		BOOT_CONFIG_10		DI	Boot configuration control bit 10
AY33	GPIO_92		P3	B-PD:nppukp	Configurable I/O
		GRFC_18		DO	Generic RF controller bit 18
		BOOT_CONFIG_11		DI	Boot configuration control bit 11
BD33	GPIO_93		P3	B-PD:nppukp	Configurable I/O
		GRFC_19		DO	Generic RF controller bit 19
		BOOT_CONFIG_12		DI	Boot configuration control bit 12
BC34	GPIO_94		P3	B-PD:nppukp	Configurable I/O
		GRFC_20		DO	Generic RF controller bit 20
		BOOT_CONFIG_13		DI	Boot configuration control bit 13
BB31	GPIO_95		P3	B-PD:nppukp	Configurable I/O
		GRFC_21		DO	Generic RF controller bit 21
BC32	GPIO_96		P3	B-PD:nppukp	Configurable I/O
		EXT_GNSS_LNA_EN		DO	External GNSS LNA enable
		GRFC_24		DO	Generic RF controller bit 24
C38	GPIO_97		P3	B-PD:nppukp	Configurable I/O
		LCD_DRIVER_5V_EN		DO	5 V display driver enable
		GP_CLK_1B		DO	General-purpose clock output 1B
		BOOT_CONFIG_14		DI	Boot configuration control bit 14
A38	GPIO_98		P3	B-PD:nppukp	Configurable I/O
		LCD_BL_EN		DO	Display backlight enable
		GP_PDM_2A		DO	General-purpose PDM 2A output
BE34	GPIO_99		P3	B-PD:nppukp	Configurable I/O
		GSM0_TX_PHASE_D0		DO-Z	GSM0 transmit phase adjust data bit 0
BE36	GPIO_100		P3	B-PD:nppukp	Configurable I/O
		GSM0_TX_PHASE_D1		DO-Z	GSM0 transmit phase adjust data bit 1
BB33	GPIO_101		P3	B-PD:nppukp	Configurable I/O
		GSM1_TX_PHASE_D0		DO-Z	GSM1 transmit phase adjust data bit 0
BE32	GPIO_102		P3	B-PD:nppukp	Configurable I/O
		GSM1_TX_PHASE_D1		DO-Z	GSM1 transmit phase adjust data bit 1
AT35	GPIO_103		P3	B-PD:nppukp	Configurable I/O
		SSBI_WTR0_RX		B	WTR0 receivers single-wire serial bus IF
		RFFE5_CLK		DO	RF front end clock 5
AW40	GPIO_104		P3	B-PD:nppukp	Configurable I/O
		SSBI_WTR0_TX		B	WTR0 transmitters single-wire serial bus IF
		RFFE5_DATA		DO	RF front end DATA 5

Table 2-10 Pin descriptions – general-purpose input/output ports (cont.)

Pad #	Pad name	Configurable function	Pad characteristics		Functional description
			Voltage	Type	
AU36	GPIO_105		P3	B-PD:nppukp	Configurable I/O
		SSBI_WTR1_RX		B	WTR1 receivers single-wire serial bus IF
		RFFE4_CLK		DO	RF front end clock 4
AY39	GPIO_106		P3	B-PD:nppukp	Configurable I/O
		SSBI_WTR1_TX		B	WTR1 transmitters single-wire serial bus IF
		RFFE4_DATA		DO	RF front end DATA 4
H33	GPIO_107		P3	B-PD:nppukp	Configurable I/O
		KYPD_SNS0		DI	Keypad sense bit 0
K35	GPIO_108		P3	B-PD:nppukp	Configurable I/O
		KYPD_SNS1		DI	Keypad sense bit 1
J34	GPIO_109		P3	B-PD:nppukp	Configurable I/O
		KYPD_SNS2		DI	Keypad sense bit 2
B39	GPIO_110		P3	B-PD:nppukp	Configurable I/O
		BLSP1_SPI_CS1_N		DO	Chip select 1 for SPI on BLSP1
		MI2S_1_WS		B	MI2S #1 word select (L/R)
		GP_MN		DO	General-purpose M/N:D counter output
		USB_HS_ID		AI	USB ID pin for host mode detection
C40	GPIO_111		P3	B-PU:nppukp	Configurable I/O
AW36	GPIO_112		P3	B-PD:nppukp	Configurable I/O
		MI2S_2_D1		B	MI2S #2 serial data channel 1
D39	GPIO_113		P3	B-PD:nppukp	Configurable I/O
		MI2S_1_SCLK		B	MI2S #1 bit clock
		GP_PDM_2B		DO	General-purpose PDM 2B output
E40	GPIO_114		P3	B-PD:nppukp	Configurable I/O
		MI2S_1_D0		B	MI2S #1 serial data channel 0
E38	GPIO_115		P3	B-PD:nppukp	Configurable I/O
		GYRO_ACCEL_INT_N		DI	Gyro interrupt
		MI2S_1_D1		B	MI2S #1 serial data channel 1
AW38	GPIO_116		P3	B-PD:nppukp	Configurable I/O
		MI2S_1_MCLK		DO	MI2S #1 master clock
AV37	GPIO_117		P3	B-PD:nppukp	Configurable I/O
		MI2S_2_WS		B	MI2S #2 word select (L/R)
AR36	GPIO_118		P3	B-PD:nppukp	Configurable I/O
		MI2S_2_SCLK		B	MI2S #2 bit clock
BA40	GPIO_119		P3	B-PD:nppukp	Configurable I/O
		MI2S_2_D0		B	MI2S #2 serial data channel 0
F39	GPIO_120		P3	B-PD:nppukp	Configurable I/O
		BLSP3_SPI_CS1_N		DO	Chip select 1 for SPI on BLSP3
G38	GPIO_121		P3	B-PD:nppukp	Configurable I/O
		BLSP2_SPI_CS1_N		DO	Chip select 2 for SPI on BLSP2

Table 2-11 Pin descriptions – RF front-end functions

Pad #	Pad name and/or function	Pad name or alt function	Pad characteristics [1]		Functional description
			Voltage	Type	
GPS control signal					
BC32	EXT_GPS_LNA_EN	GPIO_96	P3	DO B-PD:nppukp	External GPS LNA enable Configurable I/O
General RF control (GRFC) signals					
BB31	GRFC_21	GPIO_95	P3	DO B-PD:nppukp	Generic RF controller bit 21 Configurable I/O
BC34	GRFC_20	GPIO_94	P3	DO B-PD:nppukp	Generic RF controller bit 20 Configurable I/O
BD33	GRFC_19	GPIO_93	P3	DO B-PD:nppukp	Generic RF controller bit 19 Configurable I/O
AY33	GRFC_18	GPIO_92	P3	DO B-PD:nppukp	Generic RF controller bit 18 Configurable I/O
BE38	GRFC_17	GPIO_91	P3	DO B-PD:nppukp	Generic RF controller bit 17 Configurable I/O
BA32	GRFC_16	GPIO_90	P3	DO B-PD:nppukp	Generic RF controller bit 16 Configurable I/O
BD35	GRFC_15	GPIO_89	P3	DO B-PD:nppukp	Generic RF controller bit 15 Configurable I/O
BB35	GRFC_14	GPIO_88	P3	DO B-PD:nppukp	Generic RF controller bit 14 Configurable I/O
BB37	GRFC_13	GPIO_87	P3	DO B-PD:nppukp	Generic RF controller bit 13 Configurable I/O
BD39	GRFC_12	GPIO_86	P3	DO B-PD:nppukp	Generic RF controller bit 12 Configurable I/O
BE6	GRFC_11	GPIO_85	P3	DO B-PD:nppukp	Generic RF controller bit 11 Configurable I/O
BC8	GRFC_10	GPIO_84	P3	DO B-PD:nppukp	Generic RF controller bit 10 Configurable I/O
BC40	GRFC_9	GPIO_83	P3	DO B-PD:nppukp	Generic RF controller bit 9 Configurable I/O
BC38	GRFC_8	GPIO_82	P3	DO B-PD:nppukp	Generic RF controller bit 8 Configurable I/O
BD7	GRFC_7	GPIO_81	P3	DO B-PD:nppukp	Generic RF controller bit 7 Configurable I/O
BD5	GRFC_6	GPIO_80	P3	DO B-PD:nppukp	Generic RF controller bit 6 Configurable I/O
BZC6	GRFC_5	GPIO_79	P3	DO B-PD:nppukp	Generic RF controller bit 5 Configurable I/O
BE4	GRFC_4	GPIO_78	P3	DO B-PD:nppukp	Generic RF controller bit 4 Configurable I/O
BC4	GRFC_3	GPIO_77	P3	DO B-PD:nppukp	Generic RF controller bit 3 Configurable I/O

Table 2-11 Pin descriptions – RF front-end functions (cont.)

Pad #	Pad name and/or function	Pad name or alt function	Pad characteristics [1]		Functional description
			Voltage	Type	
AP35	GRFC_2	GPIO_76	P3	DO B-PD:nppukp	Generic RF controller bit 2 Configurable I/O
AV39	GRFC_1	GPIO_75	P3	DO B-PD:nppukp	Generic RF controller bit 1 Configurable I/O
AP37	GRFC_0	GPIO_74	P3	DO B-PD:nppukp	Generic RF controller bit 0 Configurable I/O

1. Refer to Table 2-1 for parameter and acronym definitions.

NOTE GPIO pins can support multiple functions. To assign GPIOs to particular functions (such as the options listed in the table above), designers must identify all their application's requirements and map each GPIO to its function – carefully avoiding conflicts in GPIO assignments. Refer to Table 2-10 for a list of all supported functions for each GPIO.

NOTE Handset designers must examine each GPIO's external connection and programmed configuration, and take necessary steps to avoid excessive leakage current. Combinations of the following factors must be controlled properly:

- GPIO configuration
  - Input versus output
  - Pullup or pulldown
- External connections
  - Unused inputs
  - Connections to high-impedance (tri-state) outputs
  - Connections to external devices that may not be attached

To help designers define their products' GPIO assignments, QTI provides an Excel spreadsheet that lists all MSM8x16 GPIOs (in numeric order), pad numbers, pad voltages, pull states, and available configurations.

NOTE Click the link below to download the *MSM8916 GPIO Configuration Spreadsheet* (80-NK807-1B) from the CDMA Tech Support website.

https://downloads.cdmatech.com/qdc/drl/objectId/09010014825db1e2

If you have permission to view the document, a prompt will be presented for initiating the download.

NOTE Subscribe to the pin assignment spreadsheet to be notified of any changes.

Click the **Help** button to download the latest revision of *Using CDMA Tech Support Documents and Downloads User Guide* (80-V7273-1). This document includes subscription instructions.

Table 2-12 Pin descriptions – No connection, do not connect, and reserved pins

Pad #	Pad name	Functional description
A2, A40, AB11, AB19, AB23, AC6, AD1, AD23, AD27, AD3, AD31, AD5, AJ6, AK25, AK27, AK3, AK5, AL4, AL6, AM27, AM5, AM7, AN2, AN4, AN6, AP25, AP3, AP5, AP7, AT1, AT17, AT19, AT21, AT25, AT3, AU16, AU18, AU2, AU20, AU24, AV21, AV23, AV25, AV27, AV29, AV31, AW16, AW18, AW20,AW22, AW24, AW26, AW28, AW30, AW32, AY25, AY29, B1, BA24, BA30, BB29, BB9, BC30, BD1, BD29, BD9, BE2, BE40, D33, D37, F15, F17, F21, G22, G26, H11, H13, H15, H19, H23, H25, H27, H29, H31, H7, M19, P19, P23, P25, AA40	NC	No connect; not connected internally
BA36, AY35, AN8, AY15, AY17, BA14, BA16	DNC	Do not connect; connected internally, do not connect externally

Table 2-13 Pin descriptions – power supply pins

Pad #	Pad name	Functional description
AP17, AP19	VDD_A1	Power for analog circuits – low voltage
AR24, AR22, AR18, AR20	VDD_A2	Power for analog circuits – high voltage
AB25, AB27, AB29, AB31, K29, K31, K33, M23, M25, M27, M29, M31, M33, P27, P29, P31, P33, T25, T27, T29, T33, V25, V27, V29, V31, V33, Y25, Y27, Y29, Y31	VDD_APC	Power for applications microprocessors
AF31, U8, AD13, AD15, AD17, AD25, AD29, AH11, AH17, AH19, AH21, AM17, AM19, AR10, M11, M21, M9, T11, T21, T9, U22, U24, Y11, Y13, Y15, Y17, Y9	VDD_CORE	Power for digital core circuits
AD11, AG28, AH13, AH15, AH23, AH25, AH27, AH29, AJ28, AL28, AM11, AM9, AN28, AP29, AU10, K25, M15, N14, T13, T15, T23, T31, Y19, J28, K27, M13, M17, AP27	VDD_MEM	Power for on-chip memory
AE6, AE8, AB9, AC8	VDD_MIPI	Power for MIPI circuits (CSI and DSI)
AH5	VDD_MIPI_DSI_PLL	Power for MIPI _DSI PHY PLL
J10, J14, J20, J22, J24, J30, K11, K15, K19, K23	VDD_P1	Power for pad group 1 – EBI pads
W8	VDD_P2	Power for pad group 2 – SDC2 pads
AA32, AG32, AK9, AP33, AT11, AT33, AT7, AU30, AU34, AU8, F31, H17, J8, V7	VDD_P3	Power for pad group 3 – most I/O pads
AB35	VDD_P4	Power for pad group 4 – UIM3 pads
L34	VDD_P5	Power for pad group 5 – UIM1 pads
AC34	VDD_P6	Power for pad group 6 – UIM2 pads
AF33	VDD_P7	Power for pad group 7 – SDC1 pads
Y21, AG16, AE22	VDD_PLL1	Power for PLL circuits – low voltage

Table 2-13 Pin descriptions – power supply pins (cont.)

W24, AP23, AN14	VDD_PLL2	Power for PLL circuits – high voltage
AJ8	VDD_QFPROM_PRG	Power for programming the QFPROM; otherwise GND
AE30	VDD_USB_HS	Power for USB PHY interface – digital voltage
AD33	VDD_USBPHY_1P8	Power for USB PHY interface – low voltage
AC32	VDD_USBPHY_3P3	Power for USB PHY interface – high voltage
AT15	VDD_WLAN	Power for WLAN ADC circuits

Table 2-14 Pin descriptions – ground pins

Pad #	Pad name	Functional description
AV15, AW14, AY13, BA12, BC12, BD13, AC30, W22, Y23, AN20, AE16, AG18, AE20, AD21, V23, V21, AM23, AM21, AM15, AM13, AY21, BD19, BE18, AV19, BB19, BC18, AV17, BD17, BE16, BB25, BE22, AA4, AA8, AC4, AD7, T3, T5, V3, W4, Y3, AF5, AH7, AJ2, AK7, AL8, AM1, AM3, AJ4, AT27, AU28, BA28, BB27, BC26, BC28, BD27, BE28, BA22, BC22, BD23, AT13, AV13, AW12, A12, A16, A22, A28, A32, A6, AA24, AA26, AA28, AA30, AB13, AB15, AB17, AB21, AD19, AF11, AF13, AF15, AF17, AF19, AF21, AF23, AF25, AF27, AF29, AF9, AG20, AH31, AH9, AJ34, AK11, AK13, AK15, AK17, AK19, AK21, AK23, AK29, AK31, AK33, AL30, AM25, AM29, AM31, AM33, AP9, AR4, AR6, AT29, AU12, AU38, AU6, AV11, AV33, AV5, AV9, AW10, AW2, AW34, AW4, AY11, B5, BA8, BB7, BC36, BD37, BE10, BE8, C18, C20, C32, C8, D27, D5, D7, E12, F19, F25, F27, F29, F37, F7, G10, G12, G14, G16, G18, G20, G24, G28, G30, G32, G8, H35, H37, J16, J18, J32, J36, J38, K17, K21, K37, K5, K9, L30, L32, L4, L6, L8, M35, M37, M39, M5, M7, N2, N22, N24, N26, N28, N30, N32, N34, N36, N38, N4, N40, N8, P11, P13, P15, P17, P21, P35, P37, P39, P5, P9, R22, R24, R26, R28, R30, R32, R34, R36, R38, R40, R8, T17, T19, T35, T37, T39, U26, U28, U30, U32, U34, U36, U38, U40, V11, V13, V15, V17, V19, V35, V37, V39, W16, W26, W28, W30, W32, W34, W36, W38, W40	GND	Ground

3 Electrical Specifications

3.1 Absolute maximum ratings

Absolute maximum ratings (Table 3-1) reflect conditions that the MSM8x16 device may be exposed to beyond the operating limits, without experiencing immediate functional failure. They are limiting values, to be considered individually when all other parameters are within their specified operating ranges. Functionality and long-term reliability can only be expected within the operating conditions, as described in Section 3.2.

Table 3-1 Absolute maximum ratings

Parameter		Min	Max	Unit
Power-supply voltages				
VDD_A1	Analog circuits	-0.30	1.56	V
VDD_A2	Analog circuits	-0.30	2.16	V
VDD_APC	Application microprocessors	-0.30	1.62	V
VDD_CORE	Digital core circuits	-0.30	1.55	V
VDD_MEM	On-chip memory	-0.30	1.55	V
VDD_MIPI_DSI_PLL	Power for MIPI _DSI PHY PLL	-0.30	2.16	V
VDD_P1	Digital pad circuits	-0.30	1.44	V
VDD_P2	Digital pad circuits – 2.95 V Digital pad circuits – 1.80 V	-0.30 -0.30	3.25 2.16	V
VDD_P3	Digital pad circuits	-0.30	2.16	V
VDD_P4	Digital pad circuits – 2.95 V Digital pad circuits – 1.80 V	-0.30 -0.30	3.25 2.16	V
VDD_P5	Digital pad circuits – 2.95 V Digital pad circuits – 1.80 V	-0.30 -0.30	3.25 2.16	V
VDD_P6	Digital pad circuits – 2.95 V Digital pad circuits – 1.80 V	-0.30 -0.30	3.25 2.16	V
VDD_P7	Digital pad circuits	-0.30	2.45	V
VDD_PLL1	PLL circuits	-0.30	1.55	V
VDD_PLL2	PLL circuits	-0.30	2.16	V
VDD_QFPROM_ PRG	QFPROM programming voltage	-0.30	2.16	V
VDD_USBPHY_1P8	USB PHY low-voltage circuit	-0.30	2.16	V
VDD_USBPHY_3P3	USB PHY high-voltage circuit	-0.30	3.63	V

Table 3-1 Absolute maximum ratings (cont.)

Parameter		Min	Max	Unit
VDD_USB_HS	Core circuits for USB	-0.30	1.55	V
VDD_WLAN	WLAN ADC circuits	-0.30	1.56	V
Signal pins				
V_IN	Voltage on any non-power input pin	-0.3	V_{xx} + 20% [1]	V
VIN_P7	Voltage on any eMMC input pin	-0.30	2.45	V
I_IN	Latch-up current	-100	100	mA
ESD protection – see Section 7.1				
Thermal conditions – see Section 4.3				

1. V_{XX} is the supply voltage associated with the input or output pin to which the test voltage is applied.

3.2 Operating conditions

Operating conditions include parameters that are under the control of the design team: power-supply voltage, power-distribution impedances, and thermal conditions (Table 3-3). The MSM8x16 meets all performance specifications listed in Section 3.3 through Section 3.12, when used within the operating conditions, unless otherwise noted in those sections (provided the absolute maximum ratings have never been exceeded).

Table 3-2 Operating conditions for APC and CORE rails

Parameter		Min	Typ	Max	Unit
VDD_APC	Quad Cortex A53 [operating at a maximum frequency of 1.15+ GHz]				
	Turbo mode	1.07	–	1.42	V
	Nominal mode	0.97	–	1.22	V
	SVS* mode	0.97	1.05	1.12	V
VDD_CORE	Turbo mode	1.05	–	1.36	V
	Nominal mode	0.93	–	1.22	V
	SVS mode	0.84	–	1.12	V

NOTE Parts with voltages outside the specified ranges are not guaranteed to operate properly

* AVS Type I is not enabled on APC rail in SVS mode.

Table 3-3 Operating conditions

Parameter		Min	Typ [2]	Max	Unit
Power-supply voltages					
VDD_A1 VDD_WLAN	Power for analog circuits – low voltage for PA DAC and Tx DAC circuits Power for WLAN ADC circuits	1.25	1.3	1.35	V
VDD_MEM VDD_PLL1 VDD_USB_HS	Power supply for internal memory cores Power for PLL circuits – low voltage Power for core circuits of USB				
	Turbo mode	1.22	1.2875	1.33	V
	Nominal mode	1.10	1.15	1.19	V
	SVS mode	1.00	1.05	1.09	V
VDD_PLL2 VDD_A2 VDD_USBPHY_1P8	Power for PLL circuits – high voltage Power for analog circuits – high voltage for analog baseband receiver and SVideo circuits Power for USB PHY interface – low voltage	1.75	1.80	1.93	V
VDD_P1 VDD_MIPI	Power for pad group 1 – EBI pads Power for MIPI circuits (CSI and DSI)	1.15	1.20	1.25	V
VDD_P2	Power for pad group 2				
	SDC2 pads low voltage	1.67	1.8	1.93	V
	SDC2 pads high voltage	2.75	2.95	3.04	V
VDD_P3	Power for pad group 3 – most I/O pads	1.67	1.8	1.93	V
VDD_P4	Power for pad group 4				
	UIM3 pads low voltage	1.67	1.8	1.93	V
	UIM3 pads high voltage	2.75	2.95	3.04	V
VDD_P5	Power for pad group 5				
	UIM1 pads low voltage	1.67	1.8	1.93	V
	UIM1 pads high voltage	2.75	2.95	3.04	V
VDD_P6	Power for pad group 6				
	UIM2 pads low voltage	1.67	1.8	1.93	V
	UIM2 pads high voltage	2.75	2.95	3.04	V
VDD_P7	Power for pad group 7 – SDC1 pads	1.67	1.8	1.93	V
VDD_MIPI_DSI_PLL	Power for MIPI _DSI PHY PLL	1.72	1.8	1.95	V
VDD_QFPROM_PRG	Power for programming the QFPROM; otherwise ground	1.67	1.8	1.93	V
VDD_USBPHY_3P3	Power for USB PHY interface – high voltage	2.97	3.08	3.50	V
Thermal conditions					
T_C	Device operating temperature (case)	-30	+25	+85	°C
T_A [1]	3GPP2-mode operating temperature (ambient)	-30	+25	+60	°C
	3GPP-mode operating temperature (ambient)	-20	+25	+60	°C

1. These temperature ranges are defined by the 3GPP and 3GPP2 system specifications.
2. Typical voltages represent the recommended output settings of the companion PMIC device

3.2.1 Core voltage minimization (retention mode)

The MPM supports VDD minimization, also known as VDD_CORE retention mode. This technique reduces the leakage of the digital logic by reducing VDD to the minimum required to maintain the register and memory state.

The V(MIN) for state retention is found through characterization. As in any normal distribution, retention voltages vary across devices. Three fuses are blown to set the core voltage in retention mode. These fuses are used by software.

The fuse locations in Table 3-4 refer to register 0x0005C00C SECURITY_CONTROL_CORE_QFPROM_CORR_PTE2.

Table 3-4 Core voltage in retention mode

VDD_CORE [1]	Bit 7 (MSB)	Bit 6	Bit 5 (LSB)
0.65 V	0	0	0
0.5 V	0	0	1
0.65 V	0	1	1

1. The specified VDD_CORE voltages are PMIC settings.

3.3 Power delivery network specification

This is the power delivery network (PDN) maximum impedance specification.

NOTE Design guidelines for the PDN are listed in *Training: Power Delivery Network Design* (80-VT310-13). If PCB designers have difficulty meeting these impedances, please contact QTI for assistance.

3.3.1 PDN system specification (PCB + baseband IC)

Table 3-5 lists the PCB + baseband IC PDN requirements. Meeting this specification requires the use of a commercial circuit simulator program (e.g., ADS) and the MSM8x16 S-parameter model *(Power Distribution Network Package Model* (HS11-NK807-10HW).

Table 3-5 PCB + baseband IC PDN impedance vs. frequency

Power domain	Required PCB routing inductance (caps shorted) [1]	Max impedance		
		DC to 10 Hz	10 Hz to 10 MHz	10 MHz–500 MHz
VDD_MEM	500 pH	11 mΩ	104 mΩ	250 mΩ
VDD_CORE	250 pH	5 mΩ	79 mΩ	160 mΩ
VDD_APC	200 pH	4 mΩ	45 mΩ	140 mΩ

1. Meeting the PCB routing inductance is the required starting point to reap maximum benefits from the PDN capacitor optimization process described in *PDN Capacitor Optimization Guidelines* (80-VT310-15).

3.3.2 PDN specification (PCB-only)

Table 3-6 lists the PCB-only PDN requirements. Refer to this specification **only** if a commercial circuit simulator program (e.g., ADS) is not available.

Table 3-6 PCB-only PDN impedance vs. frequency

Power domain	Max impedance		Pin number of positive ports	Pin number of negative ports
	DC to 10 Hz	10 Hz to 25 MHz		
VDD_MEM	11 mΩ	78 mΩ	All VDD_MEM pins	All GND pins
VDD_CORE	5 mΩ	78 mΩ	All VDD_CORE pins	All GND pins
VDD_APC	4 mΩ	45 mΩ	All VDD_APC pins	All GND pins
VDD_P1	35 mΩ	141 mΩ	J10, J14, K11	G10, G12, G14, G16, K9, J16
		141 mΩ	J20, J22	G18, G20, G24, J18, K21
		141 mΩ	J24, K23	G24, K21
		141 mΩ	K15, K19	K17, K21
		141 mΩ	J30	G28, G30, G32, J32

NOTE Design guidelines for the PDN are listed in *Training: Power Delivery Network Design* (80-VT310-13). If PCB designers have difficulty meeting these impedances, contact QTI for assistance.

NOTE The PDN DC specification for VDD_P1 applies for both MSM and external memory domains powered by VREG_L2_1P2 under the assumption that the maximum current drawn by memory device is 250 mA. The PDN AC specification for VDD_P1 applies only for MSM domain powered by VREG_L2_1P2.

3.4 DC power characteristics

3.4.1 Average operating current

Detailed current-consumption information and details about the operating modes tested are available in the *MSM8916 Linux Android Current Consumption Data* (80-NK807-7).

3.4.2 Dhrystone and rock bottom maximum power

Table 3-7 lists values for Dhrystone and rock bottom power specifications.

Table 3-7 Dhrystone and rock bottom power specifications

MSM version	Dhrystone (W) at 85°C (T_j) [1] [2]	Rock bottom (mW) at 25°C (T_j) [3]
MSM8x16 (1.2 GHz)	3.78	11.8

1. Dhrystone should be measured using the QTI custom Dhrystone script that will be provided upon request.
2. The Dhrystone specification applies only to MSM8x16 CS devices. Dhrystone should be run and measured on all four APC together.
3. Rock bottom (VDD_CORE and VDD_MEM) should be measured at VDD_CORE and VDD_MEM rails when VDD_CORE and VDD_MEM are at retention voltage. Refer to AIR1, Table 3-1 in *MSM8916 Linux Android Current Consumption Data* (80-NK807-7) for the test setup.

3.5 Power sequencing

The PM8916 includes poweron circuits that provide the proper power sequencing for the entire MSM8x16 chipset. The supplies are turned on as groups of regulators that are selected by the hardware configuration of some PMIC pins. Refer to the *PM8916 Power Management IC Device Specification* (80-NK808-1) for details.

A high-level summary of the required poweron sequence is as follows:

- VDD_MEM (on-chip memory), VDD_PLL1
- VDD_CORE (digital core circuits)
- VDD_APC (Cortex A53 microprocessor)
- VREF_SDC (SDC reference voltage)
- VDD_P3 (SDC3 and I/Os), VDD_P7 (SDC1), VDD_DDR_1P8
- VDD_P1 (EBI and DDR I/Os), VDD_DDR_1P2
- VREG_XO
- VDD_USBPHY_1P8, VDD_PLL2
- EBI0_VREF_XX (LPDDR2/3 reference voltage)
- VDD_USB_3P3
- VDD_QFPROM_PRG, VDD_P2 (SDC2)

Comments regarding this sequence:

- The core voltage (VDD_CORE) needs to power up before the pad circuits (VDD_Px), so that internal circuits can take control of the I/Os and pads.
- If pad voltages power up first, the output drivers might be stuck in unknown states, and might cause large leakage currents until VDD_CORE powers on.
- The general-purpose pad voltage (VDD_P3) needs to precede the analog voltages (VDD_Ax), since the SSBIs are initialized to their default states before VDD_Ax powers up (analog circuits are controlled by SSBI).
- Other noncritical supplies are included within the poweron sequence. Any other desired supplies can be powered on by software after the sequence is completed.

- Each domain needs to reach its 90% value before the next domain starts ramping up. For example, when VDD_MEM reaches 90% of its value, then the VDD_CORE supply can start ramping up.

3.6 Digital logic characteristics

A digital I/O's performance specification depends upon its pad type, its usage, and/or its supply voltage:

- Some are dedicated for interconnections between the MSM8x16 chipset and other ICs within the QTI chipset, and therefore do not require specification.
- Some are defined by existing standards (such as I^2C, SPI, etc). QTI devices comply with those standards and additional specifications are not required.
- All other digital I/Os require performance specifications, and are organized within this section as described in Table 3-8.

Table 3-8 Digital I/Os specified in this section

Pad voltage	Usage	Table
1.2 V	EBI0 (P1)	Table 3-9
1.8 V	GPIO (P3)	Table 3-10
Dual- V (1.8 V/2.95 V)	SDC2 (P2), GPIO (P5, P6, P4), UIM1 (P5), UIM2 (P6), UIM3 (P4)	Table 3-11
Dual- V (1.2 V/1.8 V)	SDC1 (P7)	Table 3-12

Table 3-9 1.2 V digital I/O characteristics

Parameter		Comments	Min	Max	Unit
EBI0 pads only (as identified in Table 3-8)					
V_{REF}	Reference voltage		0.49 * V_{DD_Px}	0.51 * V_{DD_Px}	V
V_{IH}	High-level input voltage	CMOS/Schmitt	V_{REF} + 0.13	–	V
V_{IL}	Low-level input voltage	CMOS/Schmitt	–	V_{REF} - 0.13	V
I_{IH}	Input high leakage current	No pulldown	–	2	µA
I_{IL}	Input low leakage current	No pullup	-2	–	µA
I_{IHPD}	Input high leakage current with pulldown		40	200	µA
I_{ILPU}	Input low leakage current with pullup		-200	-40	µA
I_{OZHKP}	High-level, tri-state leakage current with keeper		-120	-10	µA
I_{OZLKP}	Low-level, tri-state leakage current with keeper		10	120	µA
V_{OH}	High-level output voltage	CMOS, at rated drive strength [1]	0.9 * V_{DD_Px}	–	V

Table 3-9 1.2 V digital I/O characteristics (cont.)

Parameter		Comments	Min	Max	Unit
V_{OL}	Low-level output voltage	CMOS, at rated drive strength [1]	–	0.1 * V_{DD_Px}	V
$C_{I/O}$	I/O capacitance [2]		1.25	2.50	pF

1. Refer to Table 2-1 for each output pin's drive strength (IOH and IOL); the drive strengths of many output pins are programmable, and depend on the associated supply voltage.
2. Input capacitance and I/O capacitance values are guaranteed by design, but not 100% tested.

Table 3-10 1.8 V digital I/O characteristics

Parameter		Comments	Min	Max	Unit
GPIO (P3) (as identified in Table 3-8)					
V_{IH}	High-level input voltage	CMOS/Schmitt	0.65 * V_{DD_Px}	–	V
V_{IL}	Low-level input voltage	CMOS/Schmitt	–	0.35 * V_{DD_Px}	V
V_{OH}	High-level output voltage	CMOS, at rated drive strength [1]	V_{DD_Px} - 0.45		V
V_{OL}	Low-level output voltage	CMOS, at rated drive strength [3]	–	0.45	V
R_P	Pull resistance [2]	Pullup and pulldown	55	390	kΩ
R_K	Keeper resistance [2]		30	150	kΩ
I_{IH}	Input high leakage current [3]	No pulldown	–	1	µA
I_{IL}	Input low leakage current [4]	No pullup	-1	–	µA
V_{SHYS}	Schmitt hysteresis voltage		100	–	mV
$C_{I/O}$	I/O capacitance		–	5	pF
RFFE and SPMI pins					
V_{IH}	High-level input voltage	CMOS/Schmitt	0.65 * V_{DD_PX}	–	V
V_{IL}	Low-level input voltage	CMOS/Schmitt	–	0.35 * V_{DD_Px}	V
V_{OH}	High-level output voltage	CMOS, at rated drive strength	0.8 * V_{DD_PX}		V
V_{OL}	Low-level output voltage	CMOS, at rated drive strength	–	0.2 * V_{DD_Px}	V
R_P	Pull resistance	Pullup and pulldown	10	50	kΩ
R_K	Keeper resistance		10	50	kΩ
I_{IH}	Input high leakage current	No pulldown	–	1	µA
I_{IL}	Input low leakage current	No pullup	-1	–	µA
V_{SHYS}	Schmitt hysteresis voltage		165	–	mV

1. Refer to Table 2-1 for each output pin's drive strength (I_{OH} and I_{OL}); the drive strengths of many output pins are programmable, and depend on the associated supply voltage.
2. Refer to Table 2-1 for pullup, pulldown, and keeper options for each pad (where appropriate).
3. Pad voltage = V_{DD_Px} max.
4. Over all valid pad voltages.

Table 3-11 Dual-voltage 1.8 V/2.95 V digital I/O characteristics

Parameter		Comments	Min	Max	Unit
Common to dual-voltage pads 1.8 V/2.95 V (as identified in Table 3-8)					
R_P	Pull resistance [1]	Pullup and pulldown	10	100	kΩ
R_K	Keeper resistance [1]		10	100	kΩ
V_{SHYS}	Schmitt hysteresis voltage		100	–	mV
$C_{I/O}$	IO capacitance		–	5	pF
Common to SDC2 pad and UIM pad at 2.95 V only (as identified in Table 3-8)					
I_{IH}	Input high leakage current	No pulldown	–	10	µA
I_{IL}	Input low leakage current	No pullup	-10	–	µA
Common to UIM pads, either voltage (as identified in Table 3-8)					
V_{IH}	High-level input voltage	CMOS/Schmitt	0.7 * V_{DD_Px}	V_{DD_Px} + 0.3	V
V_{IL}	Low-level input voltage	CMOS/Schmitt	-0.3	0.2 * V_{DD_Px}	V
V_{OH}	High-level output voltage	CMOS, at rated drive strength [2]	0.8 * V_{DD_Px}	V_{DD_Px}	V
V_{OL}	Low-level output voltage	CMOS, at rated drive strength [2]	0	0.4	V
SDC2 pads at 2.95 V only (as identified in Table 3-8)					
V_{IH}	High-level input voltage	CMOS/Schmitt	0.625 * V_{DD_Px}	V_{DD_Px} + 0.3	V
V_{IL}	Low-level input voltage	CMOS/Schmitt	-0.3	0.25 * V_{DD_Px}	V
V_{OH}	High-level output voltage	CMOS, at rated drive strength [2]	0.75 * V_{DD_Px}	V_{DD_Px}	V
V_{OL}	Low-level output voltage	CMOS, at rated drive strength [2]	0	0.125 * V_{DD_Px}	V
Common to SDC2 pad and UIM pad at 1.8 V only (as identified in Table 3-8)					
I_{IH}	Input high leakage current	No pulldown	–	2	µA
I_{IL}	Input low leakage current	No pullup	-2	–	µA
SDC2 pads at 1.8 V only (as identified in Table 3-8)					
V_{IH}	High-level input voltage	CMOS/Schmitt	1.27	2	V
V_{IL}	Low-level input voltage	CMOS/Schmitt	-0.3	0.58	V
V_{OH}	High-level output voltage	CMOS, at rated drive strength	1.4		V
V_{OL}	Low-level output voltage	CMOS, at rated drive strength	0	0.45	V

1. Refer to Table 2-1 for pullup, pulldown, and keeper options for each pad (where appropriate).
2. Refer to Table 2-1 for each output pin's drive strength (I_{OH} and I_{OL}); the drive strengths of many output pins are programmable, and depend on the associated supply voltage.

Table 3-12 Dual-voltage 1.2 V/1.8 V digital I/O characteristics

Parameter		Comments	Min	Max	Unit
Common to all dual-voltage pads 1.2 V / 1.8 V(as identified in Table 3-8)					
V_{IH}	High-level input voltage	CMOS/Schmitt	0.625 * V_{DD_Px}	–	V

Table 3-12 Dual-voltage 1.2 V/1.8 V digital I/O characteristics (cont.)

Parameter		Comments	Min	Max	Unit
V_{IL}	Low-level input voltage	CMOS/Schmitt	–	0.35 * V_{DD_Px}	V
I_{IH}	Input high leakage current	No pulldown	–	2	µA
I_{IL}	Input low leakage current	No pullup	-2	–	µA
R_P	Pull resistance [1]	Pullup and pulldown	10	100	kΩ
R_K	Keeper resistance [1]		10	100	kΩ
C_{IN}	Input capacitance		–	5	pF
SDC1 (P7) pad at 1.2 V only (as identified in Table 3-8)					
V_{OH}	High-level output voltage	CMOS, at rated drive strength	0.75 * V_{DD_Px}	–	V
V_{OL}	Low-level output voltage	CMOS, at rated drive strength	–	0.25 * V_{DD_Px}	V
SDC1 (P7) pad at 1.8 V only (as identified in Table 3-8)					
V_{OH}	High-level output voltage	CMOS, at rated drive strength	V_{DD_Px} - 0.45	–	V
V_{OL}	Low-level output voltage	CMOS, at rated drive strength	–	0.45	V

1. Refer to Table 2-1 for pullup, pulldown, and keeper options for each pad (where appropriate).

In all digital I/O cases, V_{OL} and V_{OH} are linear functions (Figure 3-1) with respect to the drive current (drive currents are given in Table 2-1). They can be calculated using these relationships:

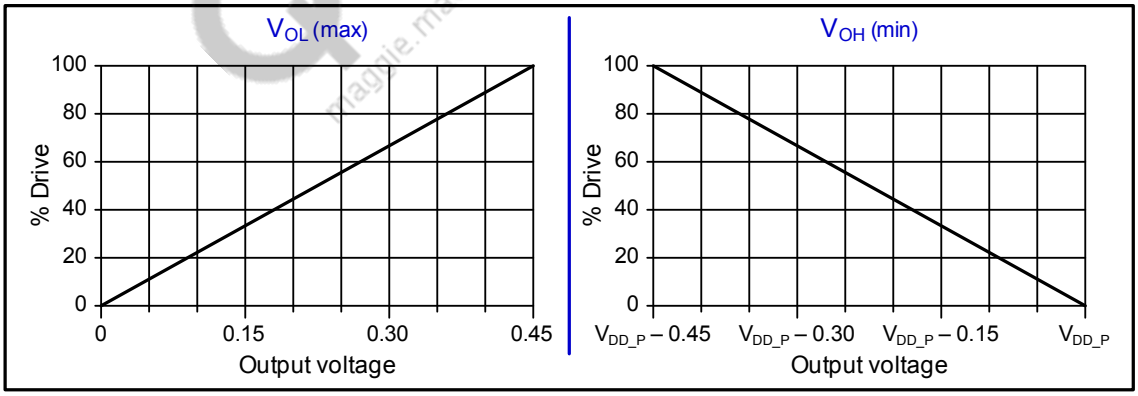

Figure 3-1 IV curve for V_{OL} and V_{OH} (valid for all V_{DD_Px})

3.7 Timing characteristics

Specifications for the device timing characteristics are included (where appropriate) under each function's section, along with all its other performance specifications. Some general comments about timing characteristics and pertinent pad-design methodologies are included here.

NOTE All MSM8x16 devices are characterized with actively terminated loads, so all baseband timing parameters in this document assume no bus loading. This is described further in Section 3.7.2.

3.7.1 Timing-diagram conventions

The conventions used within timing diagrams throughout this document are shown in Figure 3-2.

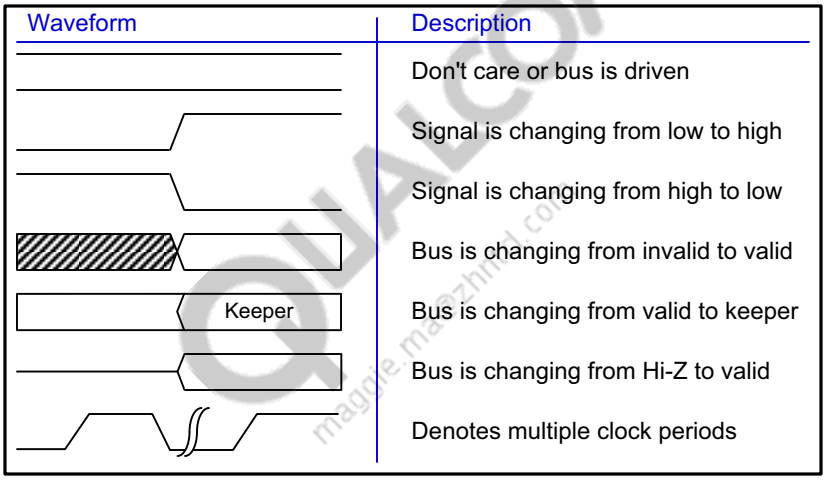

Figure 3-2 Timing-diagram conventions

For each signal in the diagram:

- One clock period (T) extends from one rising clock edge to the next rising clock edge.
- The high level represents 1, the low level represents 0, and the middle level represents the floating (high-impedance) state.
- When both the high and low levels are shown over the same time interval, the meaning depends on the signal type:
  - For a bus-type signal (multiple bits) – the processor or external interface is driving a value, but that value may or may not be valid.
  - For a single signal – indicates *don't care*.

3.7.2 Rise and fall time specifications

The testers that characterize MSM8x16 devices have actively terminated loads, making the rise and fall times quicker (mimicking a no-load condition). The impact that different external load conditions have on rise and fall times is shown in Figure 3-3.

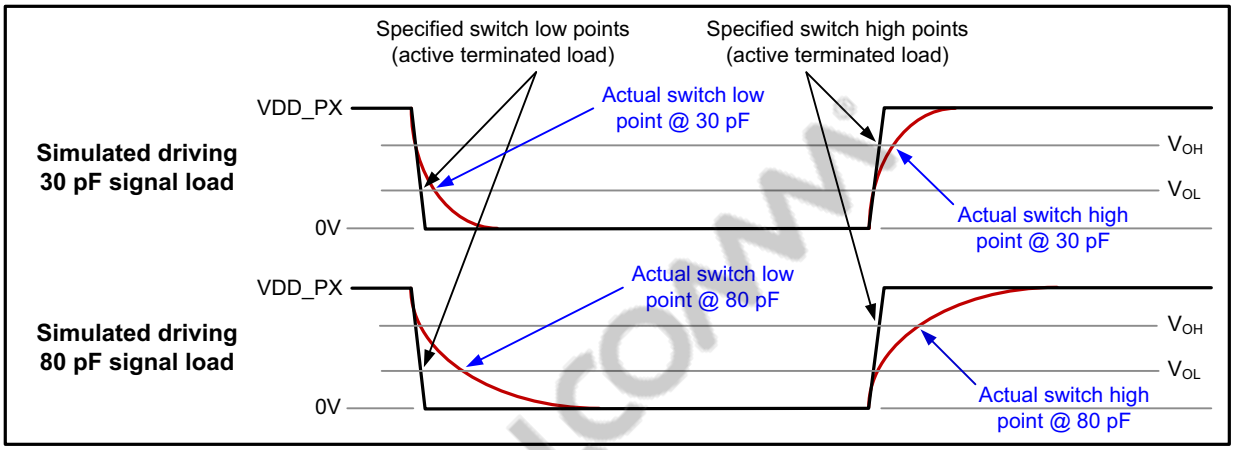

Figure 3-3 Rise and fall times under different load conditions

To account for external load conditions, rise or fall times must be added to parameters that start timing at the MSM device and terminate at an external device (or vice versa). Adding these rise and fall times is equivalent to applying capacitive load derating factors.

3.7.3 Pad design methodology

The MSM8x16 device uses a generic CMOS pad driver design. The intent of the pad design is to create pin response and behavior that is symmetric with respect to the associated V_{DD_Px} supply (Figure 3-4). The input switch point for pure input-only pads is designed to be $V_{DD\_Px}/2$ (or 50% of V_{DD_Px}). The documented switch points (guaranteed over worst-case combinations of process, voltage, and temperature by both design and characterization) are 35% of V_{DD_Px} for V_{IL} and 65% of V_{DD_Px} for V_{IH}.

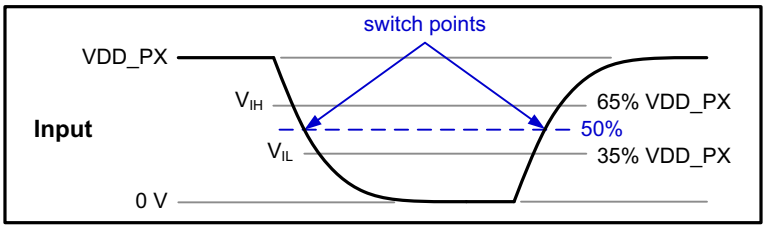

Figure 3-4 Digital input signal switch points

Outputs (address, chip selects, clocks, etc.) are designed and characterized to source or sink a large DC output current (several mA) at the documented V_{OH} (min) and V_{OL}(max) levels over worst-case process/voltage/temperature. Because the pad output structures (Figure 3-5) are

essentially CMOS drivers that possibly have a small amount of IR loss (estimated at less than 50 mV under worst-case conditions), the expected *zero DC load* outputs are *estimated* to be:

- V_{OH} ~ V_{DD_Px} - 50 mV or more
- V_{OL} ~ 50 mV or less

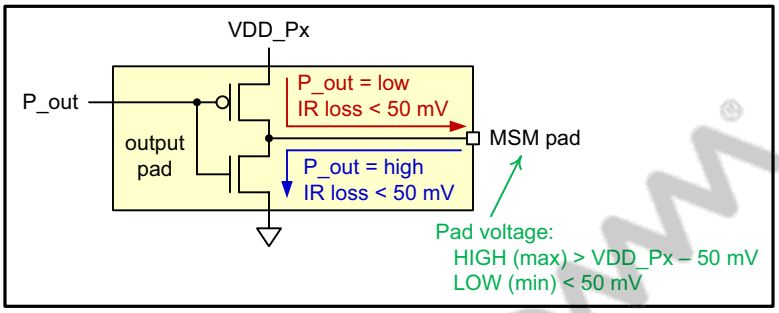

Figure 3-5 Output-pad equivalent circuit

The DC output drive strength can be *approximated* by linear interpolations between V_{OH} (min) and V_{DD_Px} - 50 mV, and between V_{OL} (max) and 50 mV. For example, an output pad driving low that guarantees 4.5 mA at V_{OL} (max) will provide approximately 3.0 mA or more at 2/3 × [V_{OL} (max) - 50 mV], and 1.5 mA or more at 1/3 × [V_{OL} (max) - 50 mV]. Likewise, an output pad driving high that guarantees 2.5 mA at V_{OH} (min) will provide approximately 1.25 mA or more at ½ × [V_{DD_Px} - 50 mV + V_{OH} (min)].

The output pads are essentially CMOS outputs with a corresponding FET-type output voltage/current transfer function. When an output pad is shorted to the opposite power rail, the pad is capable of sourcing or sinking I_{SC} (SC = short-circuit) of current, where the magnitude of I_{SC} is larger than the current capability at the intended output logic levels.

Since the target application includes a radio, output pads are designed to *minimize* output slew rates. Decreased slew rates limit high-frequency spectral components that tend to desensitize the companion radio.

Output drivers' rise time (**t**(r)) and fall time (**t**(f)) values are functions of board loading. Bidirectional pins include both input and output pad structures, and behave accordingly when used as inputs or outputs within the system. Both input and output behaviors were described above.

3.8 Memory support

All timing parameters in this document assume no bus loading. Rise/fall time numbers must be factored into the numbers in this document. For example, setup-time numbers will get worse and hold-time numbers may get better.

3.8.1 EBI0 memory support

The EBI0 port is dedicated to the LPDDR2/3 SDRAM memory that is attached to the top of the MSM8x16 device.

3.8.1.1 EBI0 pad drive strength

Pads for EBI0 are tailored for its 1.2 V interface and are source-terminated. Before the source termination, the pad drive strength is 15 mA to 60 mA. But at the pads, after the source termination, the drive strength at $I_{OL,}$ I_{OH} is equivalent to 0.90 mA to 3.35 mA in nonlinear steps when the JEDEC standard range (90% – 10%) is followed.

3.8.1.2 LPDDR2/3 SDRAM clock

For any timing analysis, the measurement point for all signals is at 50% of VDD_Px. All output timing parameters represent the point of the output signal transition; additional accounting for signal rise and fall times for specific bus loading is required.

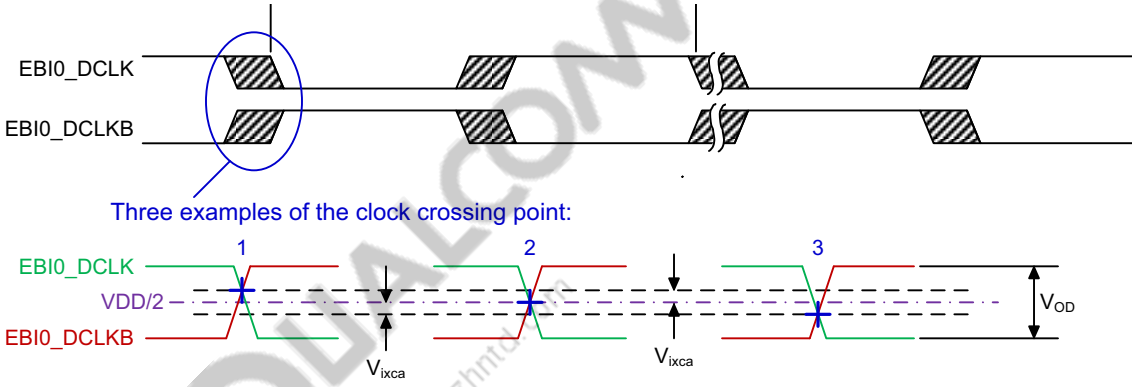

Figure 3-6 DDR SDRAM DCLK and DCLKB

Table 3-13 DDR SDRAM clock-timing parameters

Parameter		Comments	Min	Typ	Max	Unit
$1/t_{CK}$	DDR clock frequency		10	–	533 (LPDDR2) 533 (LPDDR3)	MHz
	Duty cycle		45	–	55	%
V_{ixca} [1]	Clock crossover-point	± offset from VDD/2	–	–	120	mV
V_{OD}	Differential output voltage		0.44	–	–	V

1. Crosstalk due to high CA activity might cause parameters to exceed the VIXCA limit

3.8.1.3 LPDDR2/3 SDRAM strobe

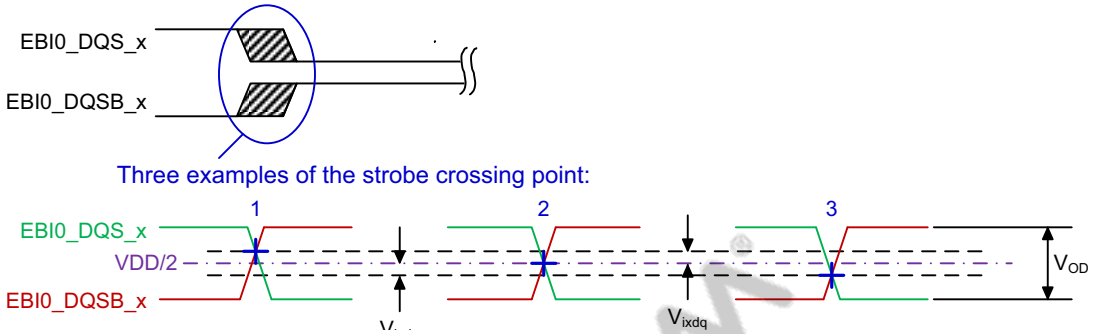

Figure 3-7 DDR SDRAM DQS_x and DQSB_x

Table 3-14 DDR SDRAM strobe timing parameters

Parameter		Comments	Min	Typ	Max	Unit
V_{IXDQ}	Clock cross-over point	± offset from VDDQ/2	–	–	120	mV
V_{OD}	Differential output voltage		0.44	–	–	V

3.8.1.4 LPDDR2 SDRAM read and write timing

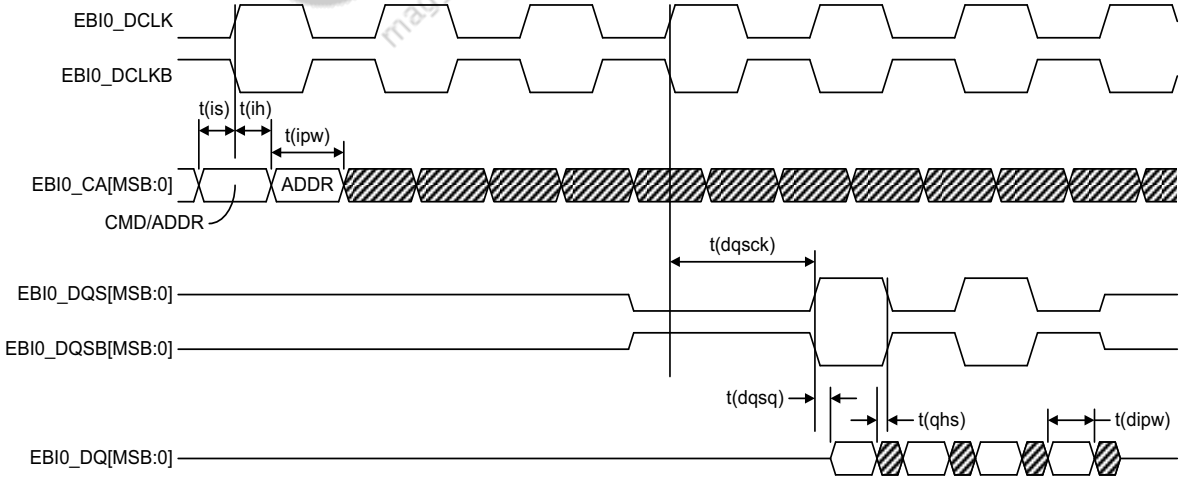

Figure 3-8 DDR SDRAM read timing

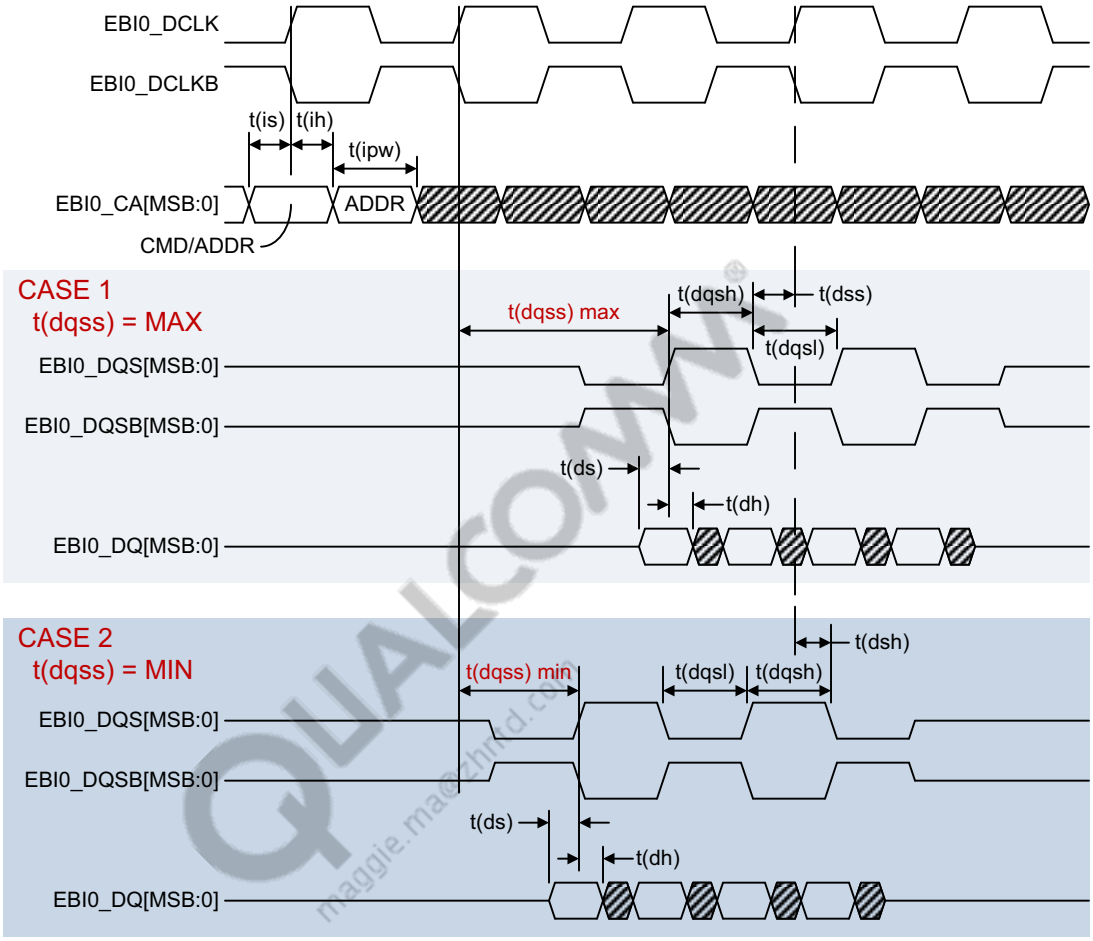

Figure 3-9 DDR SDRAM write timing

Table 3-15 DDR SDRAM read and write timing specifications

Parameter		Comments	Min	Typ	Max	Unit
LPDDR2 (533 MHz) – common to read and write						
t(is)	Address and control in setup time before CK		0.22	–	–	ns
t(ih)	Address and control input hold time after CK		0.22	–	–	ns
t(dipw)	DQ and DM pulse width		0.35	–	–	tCK
t(ipw)	Address and control input pulse width		0.40	–	–	tCK
t(tdiff)	Input transition slew rate from VIL to VIH	Differential clock	2.0	–	–	V/ns
t(t)	Input transition time from VIL to VIH	Other than diff clock	1.0	–	–	V/ns
LPDDR2 (533 MHz) – read cycle						
t(dqsck)	DQS access time from clock		2.50	–	5.50	ns
t(dqsq)	DQS to DQ skew limit		–	–	0.2	ns

Table 3-15 DDR SDRAM read and write timing specifications (cont.)

Parameter		Comments	Min	Typ	Max	Unit
t(rpre)	Read preamble		0.90	–	–	t(ck)
t(qhs)	Data hold skew factor		–	–	0.23	ns
LPDDR2 (533 MHz) – write cycle						
t(ds)	DQ and DM input setup time before DQS		0.21	–	–	ns
t(dh)	DQ and DM input hold time after DQS		0.21	–	–	ns
t(dqsh)	DQS input high-level width		0.40	–	–	t(ck)
t(dqsl)	DQS input low-level width		0.40	–	–	t(ck)
t(dqss)	First DQS latching transition		0.75	–	1.25	t(ck)
t(dss)	DQS falling edge to CK setup time		0.20	–	–	t(ck)
t(dsh)	DQS falling edge hold time after CK		0.20	–	–	t(ck)

3.8.1.5 LPDDR3 SDRAM read and write timing

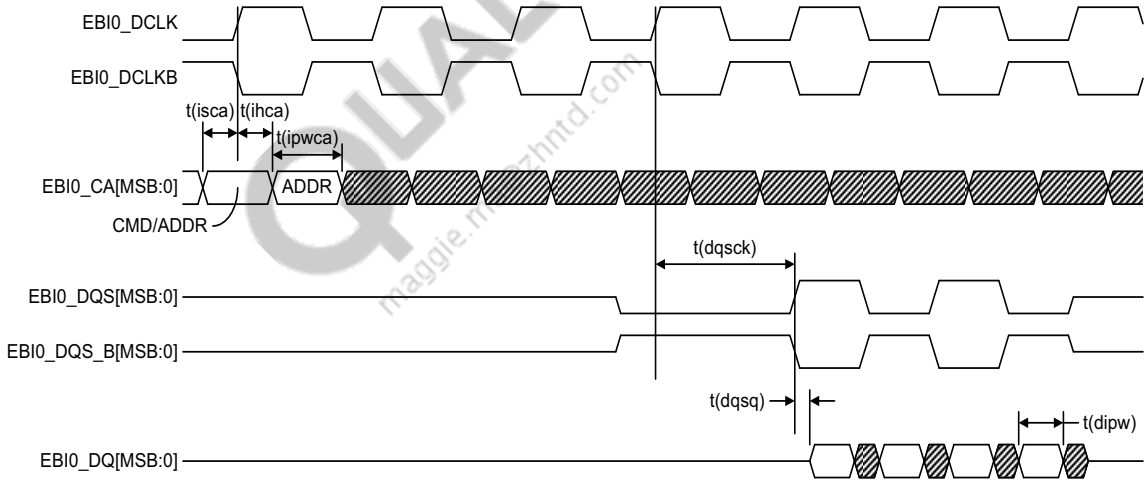

Figure 3-10 DDR SDRAM read timing

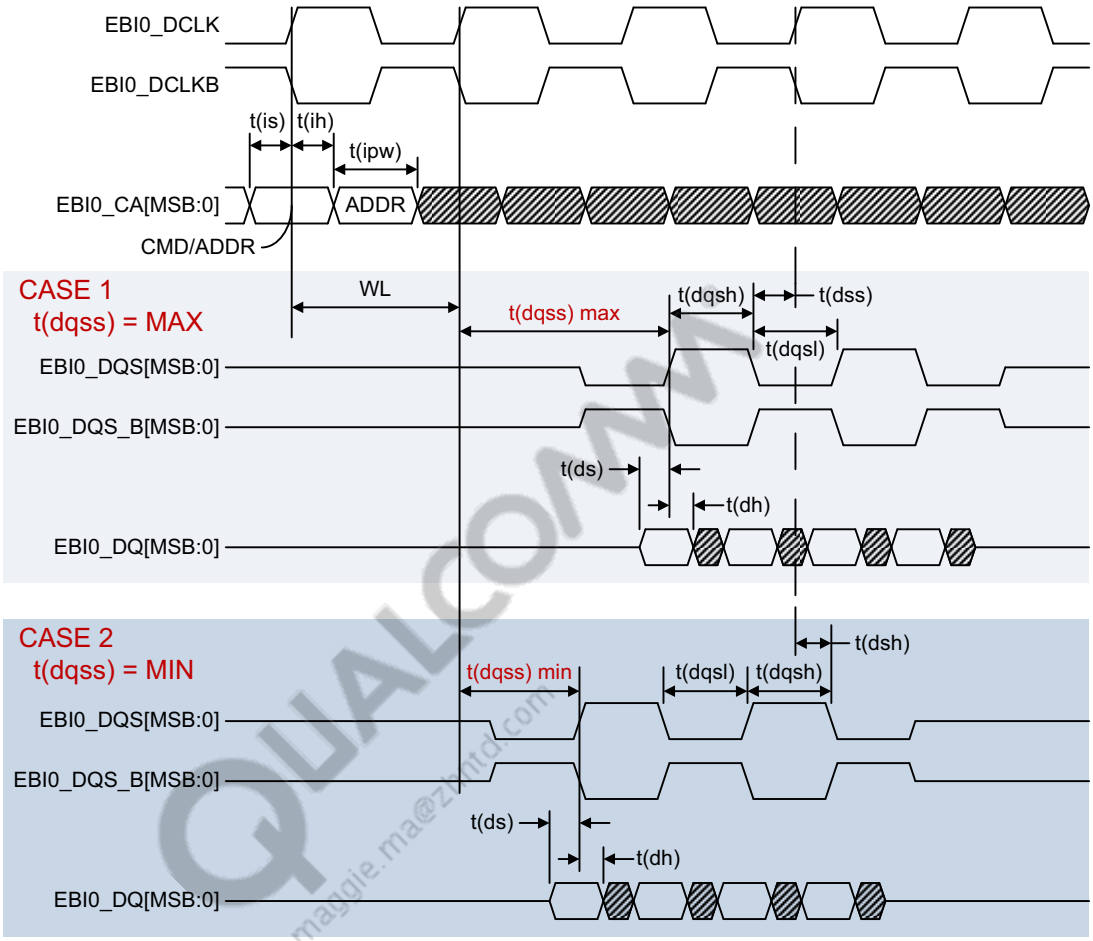

Figure 3-11 DDR SDRAM write timing

Table 3-16 DDR SDRAM read and write timing specifications

Parameter		Comments	Min	Typ	Max	Unit
LPDDR3 (533 MHz) – common to read and write						
t(isca)	Address and control in setup time before CK		0.175	–	–	ns
t(ihca)	Address and control input hold time after CK		0.175	–	–	ns
t(dipw)	DQ and DM pulse width		0.35	–	–	tCK
t(iscs)	CS_n input setup time		0.29	–	–	ns
t(ihcs)	CS_n input hold time		0.29	–	–	ns
t(ipwcs)	CS_n input pulse width		0.7	–	–	t(ck)
t(ipw)	Address and control input pulse width		0.35	–	–	tCK
t(tdiff)	Input transition slew rate from VIL to VIH	Differential clock	2.0	–	–	V/ns
t(t)	Input transition time from VIL to VIH	Other than diff clock	1.0	–	–	V/ns
LPDDR3 (533 MHz) – read cycle						

Table 3-16 DDR SDRAM read and write timing specifications (cont.)

Parameter		Comments	Min	Typ	Max	Unit
t(dqsck)	DQS access time from clock		2.50	–	5.50	ns
t(dqsq)	DQS to DQ skew limit		–	–	0.165	ns
t(qhs)	Data hold skew factor		–	–	0.713	ns
t(rpre)	Read preamble		0.9	–	–	t(ck)
LPDDR3 (533 MHz) – write cycle						
t(ds)	DQ and DM input setup time before DQS		0.175	–	–	ns
t(dh)	DQ and DM input hold time after DQS		0.175	–	–	ns
t(dqsh)	DQS input high-level width		0.40	–	–	t(ck)
t(dqsl)	DQS input low-level width		0.40	–	–	t(ck)
t(dqss)	First DQS latching transition		0.75	–	1.25	t(ck)
t(dss)	DQS falling edge to CK setup time		0.2	–	–	t(ck)
t(dsh)	DQS falling edge hold time after CK		0.2	–	–	t(ck)

3.8.2 eMMC on SDC1

See Section 3.10.1 for secure digital interface details.

3.9 Multimedia

Multimedia parameters requiring performance specification are addressed in this section.

3.9.1 Camera interfaces

The MSM8x16 supports two MIPI_CSIs.

- CSI0 is a single 4-lane CSI
- CSI1 is a 2-lane CSI

Table 3-17 Supported MIPI_CSI standards and exceptions

Applicable standard	Feature exceptions	MSM variations
MIPI Alliance Specification for D-PHY, v0.65 and v0.9/v1.0, October 8, 2007 http://www.mipi.org/specifications/physical-layer (Complete specifications are available to MIPI members only.)	Supports only unidirectional data receiving.	None

3.9.2 Audio support

The MSM8x16 device provides the system's audio functions with the analog audio codec integrated into PM8916 device. A proprietary audio PDM interface through GPIO[63:68] was used for transmission of audio data with PM8916 integrated analog codec. Refer to *PM8916 Device Specification* (80-NK808-1) for its performance characteristics.

MSM audio-related audio interface that support other audio devices included:

- I2S – Section 3.10.4
- I2C – Section 3.10.5

3.9.3 Display support

The MSM8x16 supports a 4-lane MIPI_DSI.

Table 3-18 Supported MIPI_DSI standards and exceptions

Applicable standard	Feature exceptions	MSM variations
MIPI Alliance Specification v1.01 for Display Serial Interface http://www.mipi.org/specifications/display-interface (Specifications are available to MIPI members only.)	None	None
MIPI D-PHY Specification v0.65, v0.81, v0.90 http://www.mipi.org/specifications/physical-layer (Complete specifications are available to MIPI members only.)	None	None

3.10 Connectivity

The connectivity functions supported by the MSM8x16 device that require electrical specifications include:

- Secure digital (SD), including SD cards and multimedia cards (MMC)
- High-speed universal serial bus/on-the-go (host mode only) with built-in physical layer (PHY)
- Inter-IC sound (I2S) interfaces
- Touch screen connections
- Through proper configuration of the six BLSP ports:
  - Universal asynchronous receiver/transmitter (UART) ports
  - User identity module (UIM) ports, including dual-voltage options
  - Inter-integrated circuit (I2C) interfaces
  - Serial peripheral interface (SPI) ports

Pertinent specifications for these functions are included in the following subsections:

NOTE In addition to reviewing the following hardware specifications, also be sure to review the latest software release notes for software-based performance features or limitations.

3.10.1 Secure digital interfaces

Table 3-19 Supported SD standards and exceptions

Applicable standard	Feature exceptions	Device variations
Multi Media Card Host Specification, version 4.4.1 http://www.jedec.org/ (Available for free download.)	None	Timing specifications – see Figure 3-12 and Table 3-20
Secure Digital: Physical Layer Specification, version 3.0 https://www.sdcard.org/downloads/pls/ (Simplified version of the Physical Layer Specification is available for free download.)	None	
SDIO Card Specification, version 2.0 https://www.sdcard.org/downloads/pls/simplified_specs/archive/partE1_200.pdf (Simplified specification version 3.00 is available for free download.)	None	

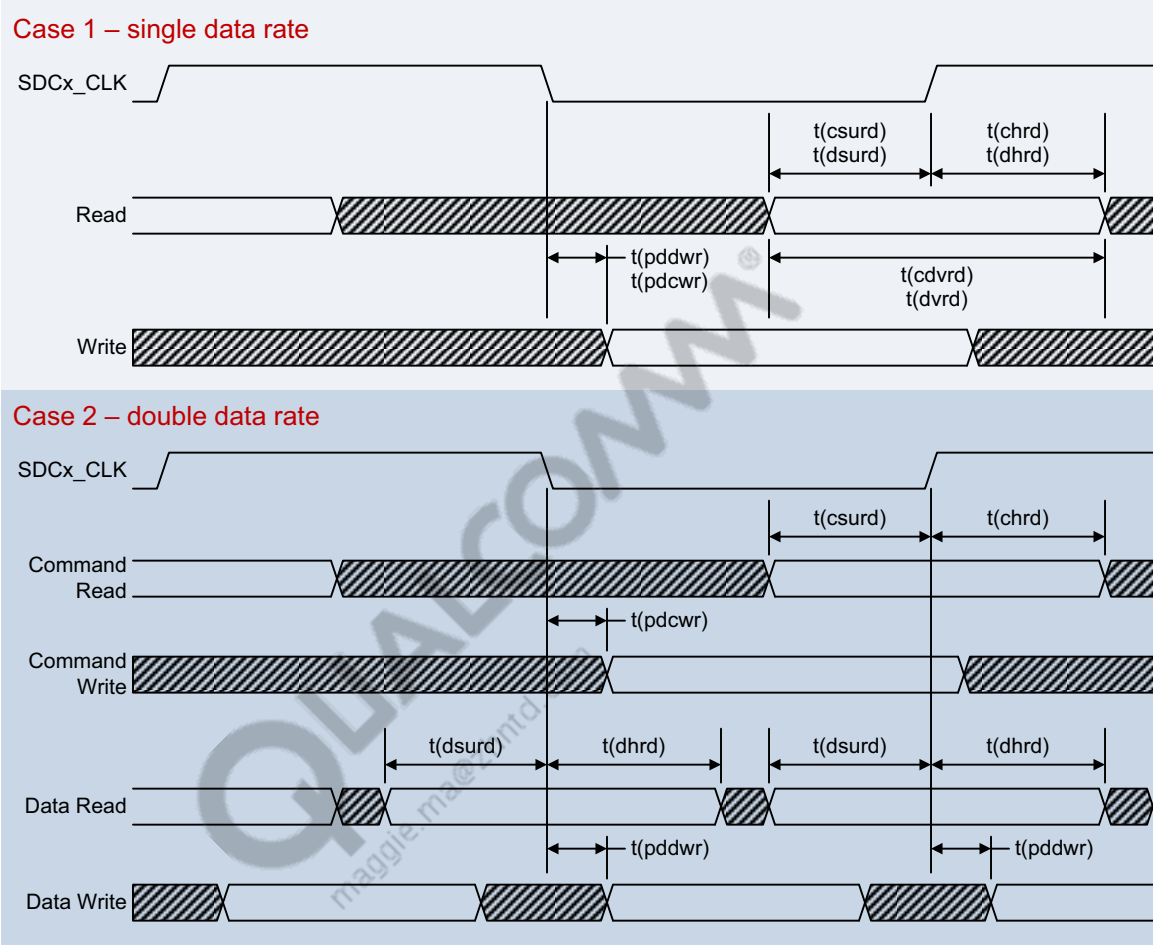

Figure 3-12 Secure digital interface timing

Table 3-20 Secure digital interface timing

Parameter		Min	Typ	Max	Unit
Single data rate (SDR) mode – SDC1 up to 200 MHz					
t(cvdrd)	Command valid	2.4	–	–	ns
t(dvdrd)	Data valid	2.4	–	–	ns
t(pddwr)	Propagation delay on data write	-1.45	–	0.85	ns
t(pdcwr)	Propagation delay on command write	-1.45	–	0.85	ns
Double data rate (DDR) mode – SDC1 up to 52 MHz					
t(chrd)	Command hold	1.5	–	–	ns
t(csurd)	Command setup	5.53	–	–	ns
t(dhrd)	Data hold	1.5	–	–	ns
t(dsurd)	Data setup	1.65	–	–	ns

Table 3-20 Secure digital interface timing (cont.)

Parameter		Min	Typ	Max	Unit
t(pddwr)	Propagation delay on data write	2.5	–	6.15	ns
t(pdcwr)	Propagation delay on command write	-7.85	–	2.65	ns
SDR mode – SDC2 up to 208 MHz					
t(cvdrd)	Command valid	2.4	–	–	ns
t(dvdrd)	Data valid	2.4	–	–	ns
t(pddwr)	Propagation delay on data write	-1.36	–	0.76	ns
t(pdcwr)	Propagation delay on command write	-1.36	–	0.76	ns
DDR mode – SDC2 up to 50 MHz					
t(chrd)	Command hold	1.5	–	–	ns
t(csurd)	Command setup	6.3	–	–	ns
t(dhrd)	Data hold	1.5	–	–	ns
t(dsurd)	Data setup	2	–	–	ns
t(pddwr)	Propagation delay on data write	0.8	–	6	ns
t(pdcwr)	Propagation delay on command write	-8.2	–	3	ns
SDR mode – SDC2 up to 100 MHz					
t(chrd)	Command hold	1.5	–	–	ns
t(csurd)	Command setup	2.5	–	–	ns
t(dhrd)	Data hold	1.5	–	–	ns
t(dsurd)	Data setup	2.5	–	–	ns
t(pddwr)	Propagation delay on data write	-3.7	–	1.5	ns
t(pdcwr)	Propagation delay on command write	-3.7	–	1.5	ns

3.10.2 UIM interface

Table 3-21 Supported UIM standards and exceptions

Applicable standard	Feature exceptions	MSM variations
ISO/IEC 7816-3 http://webstore.ansi.org/ (Available to ANSI Site Licensees or for a fee).	None	None

3.10.3 USB interfaces

Table 3-22 Supported USB standards and exceptions

Applicable standard	Feature exceptions	Device variations
Universal Serial Bus Specification, Revision 2.0 (April 27, 2000 or later) http://www.usb.org/developers/docs/ (Available for free download.)	None	Operating voltages, system clock, and VBUS – see Table 3-23
On-The-Go Supplement to the USB 2.0 Specification (June 24, 2003, Revision 1.0A or later) http://www.usb.org/developers/docs/ (Available for free download as part of the USB 2.0	Supports host mode aspect of OTG only	None

Table 3-23 Device-specific USBPHY specifications

Parameter	Comments	Min	Typ	Max	Unit
Supply voltages					
Dual-supply (see Table 3-3 for specifications)					
VDD_USB_1P8		–	1.80	–	V
VDD_USB_3P3		–	3.075	–	V
USB_SYSCLK					
Frequency	19.2 MHz clock is required.	–	19.2	–	MHz
Clock deviation		-400	–	400	ppm
Jitter (peak-to-peak)	0.5 to 1.75 MHz	0	–	60	ps
Duty cycle		40	–	60	%
Low-level input voltage (V_{IL})		–	–	0.85	V
High-level input voltage (V_{IH})		1.27	–	–	V
USB_VBUS					
Valid USB_HS_VBUS detection voltage		2.00	–	5.25	V

3.10.4 I2S interface

The MI2S (multiple I2S) interface for microphone and speaker functions is supported by the MSM8x16.

The following information applies to MI2S.

Table 3-24 Supported I2S standards and exceptions

Applicable standards	Feature exceptions	MSM variations
Phillips I2S Bus Specifications revised June 5, 1996 http://www.classic.nxp.com/acrobat_download2/various/I2SBUS.pdf (Available for free download.)	None	When an external SCK clock is used, a duty cycle between 45% to 55% is required.

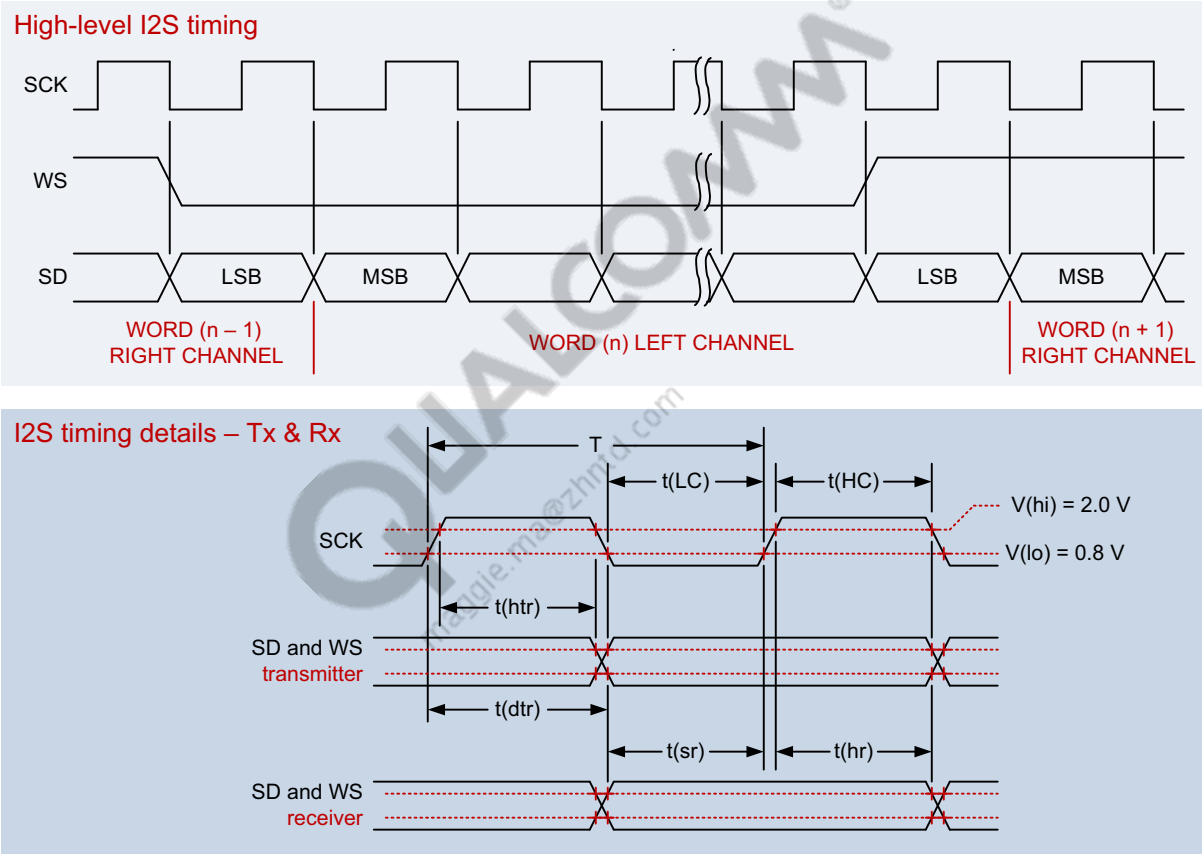

Figure 3-13 I2S timing diagram

Table 3-25 I2S interface timing

Parameter		Comments [1]	Min	Typ	Max	Unit
Using internal SCK						
	Frequency		–	–	12.288	MHz
T	Clock period		81.380	–	–	ns
t(HC)	Clock high		0.45 · T	–	0.55 · T	ns
t(LC)	Clock low		0.45 · T	–	0.55 · T	ns
t(sr)	SD and WS input setup time		16.276	–	–	ns
t(hr)	SD and WS input hold time		0	–	–	ns

Table 3-25 I2S interface timing (cont.)

Parameter		Comments [1]	Min	Typ	Max	Unit
t(dtr)	SD and WS output delay		–	–	65.100	ns
t(htr)	SD and WS output hold time		0	–	–	ns
Using external SCK						
	Frequency		–	–	12.288	MHz
T	Clock period		81.380	–	–	ns
t(HC)	Clock high		0.45 · T	–	0.55 · T	ns
t(LC)	Clock low		0.45 · T	–	0.55 · T	ns
t(sr)	SD and WS input setup time		16.276	–	–	ns
t(hr)	SD and WS input hold time		0	–	–	ns
t(dtr)	SD and WS output delay		–	–	65.100	ns
t(htr)	SD and WS output hold time		0	–	–	ns

1. Load capacitance is between 10 and 40 pF.

3.10.5 I2C interface

Table 3-26 Supported I2C standards and exceptions

Applicable standard	Feature exceptions	MSM variations
I2C Specification, version 5.0, October 2012	None	Multimaster is not supported

3.10.6 Serial peripheral interface

The MSM8x16 supports SPI as a master only. Any one of the six BLSP ports can be configured as an SPI master:

- BLSP @ 52 MHz (see Table 3-27)
- BLSP @ 26 MHz (see Table 3-28)

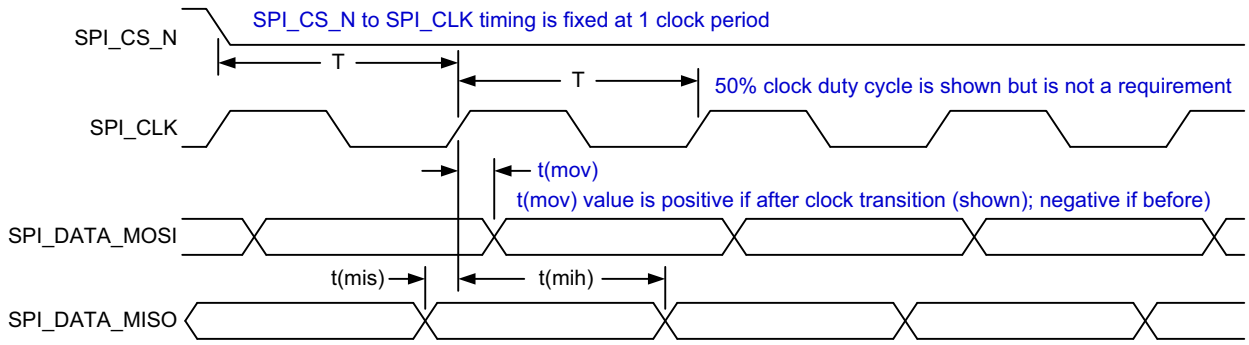

Figure 3-14 SPI master timing diagram

Table 3-27 SPI master timing characteristics at 48 MHz

Parameter	Comments	Min	Typ	Max	Unit
T [1]	SPI clock period: 48 MHz max	20.0	–	–	ns
t(ch)	Clock high	9.0	–	–	ns
t(cl)	Clock low	9.0	–	–	ns
t(mov)	Master output valid	-5.0	–	5.0	ns
t(mis)	Master input setup	5.0	–	–	ns
t(mih)	Master input hold	1.0	–	–	ns

1. The minimum clock period includes 1% jitter of the maximum frequency.

Table 3-28 SPI master timing characteristics at 26 MHz

Parameter	Comments	Min	Typ	Max	Unit
T	SPI clock period: 26 MHz max	38	–	–	ns
t(ch)	Clock high	17	–	–	ns
t(cl)	Clock low	17	–	–	ns
t(mov)	Master output valid	-5	–	5	ns
t(mis)	Master input setup	3	–	–	ns
t(mih)	Master input hold	1	–	–	ns

3.11 Internal functions

Some internal functions require external interfaces to enable their operation. These include clock generation, modes and resets, and JTAG functions – as specified in the following subsections.

3.11.1 Clocks

Clocks that are specific to particular functions are addressed in the corresponding sections of this document. Others are specified here.

3.11.1.1 19.2 MHz XO input

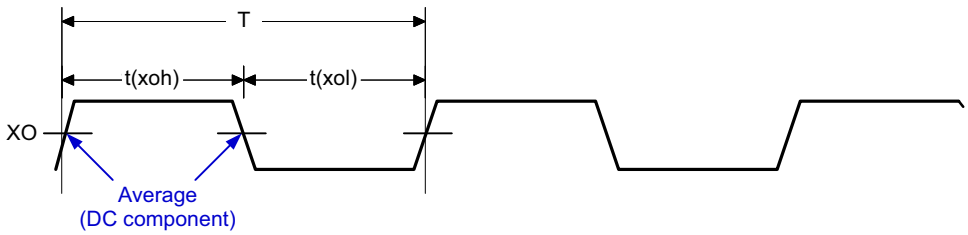

Figure 3-15 XO timing parameters

Table 3-29 XO timing parameters

Parameter		Comments [1]	Min	Typ	Max	Unit
t(xoh)	XO logic high		22.6	–	29.5	ns
t(xol)	XO logic low		22.6	–	29.5	ns
T	XO clock period		–	52.083	–	ns
1/T	Frequency	19.2 MHz must be used.	–	19.2	–	MHz

1. See *GPS Quality, 19.2 MHz 2520 Package Size, Crystal and TH + Xtal Mini-Specification* (80-V9690-24) for more details.

3.11.1.2 Sleep clock

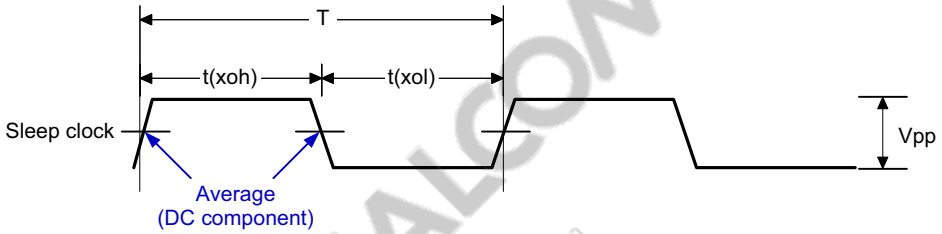

Figure 3-16 Sleep-clock timing parameters

Table 3-30 Sleep-clock timing parameters

Parameter		Comments	Min	Typ	Max	Unit
t(xoh)	Sleep-clock logic high		4.58	–	25.94	µs
t(xol)	Sleep-clock logic low		4.58	–	25.94	µs
T	Sleep-clock period		–	30.518	–	µs
F	Sleep-clock frequency	F = 1/T	–	32.768	–	kHz
Vpp	Peak-to-peak voltage		–	1.8	–	V

3.11.2 Modes and resets

Mode and reset functions are basic digital I/Os that meet the performance specifications presented in Section 3.6.

3.11.3 JTAG

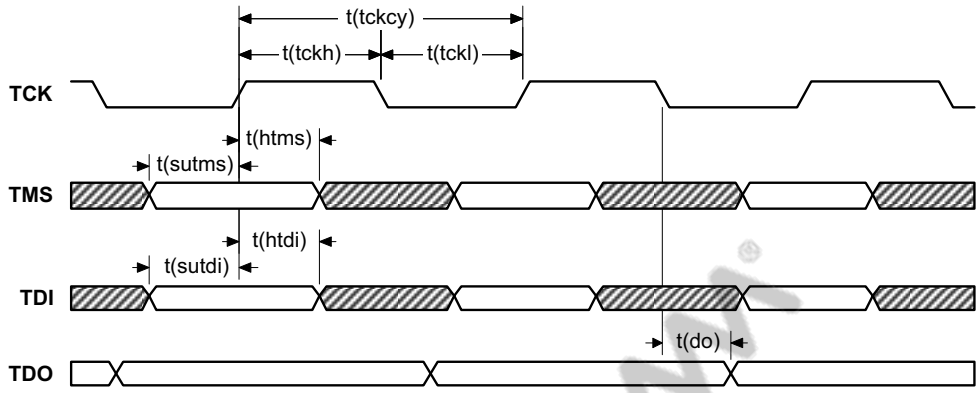

Figure 3-17 JTAG-interface timing diagram

Table 3-31 JTAG-interface timing characteristics

Parameter		Comments	Min	Typ	Max	Unit
t(tckcy)	TCK period		50	–	–	ns
t(tckh)	TCK pulse width high		20	–	–	ns
t(tckl)	TCK pulse width low		20	–	–	ns
t(sutms)	TMS input setup time		5	–	–	ns
t(htms)	TMS input hold time		20	–	–	ns
t(sutdi)	TDI input setup time		5	–	–	ns
t(htdi)	TDI input hold time		20	–	–	ns
t(do)	TDO data-output delay		–	–	15	ns

3.12 RF and power management interfaces

The supported chipset and RF front-end (RFFE) interfaces are listed in Table 3-32 and Table 3-33, respectively. The digital I/Os must meet the logic-level requirements specified in Section 3.6. The Rx and Tx baseband interfaces are proprietary, and therefore are not specified.

3.12.1 RF front-end (RFFE)

Table 3-32 Supported RFFE standards and exceptions

Applicable standard	Feature exceptions	MSM variations
MIPI Alliance Specification for RF Front-End Control Interface version 1.0	None	None

The maximum operation frequency of SCLK is 26 MHz, although lower rates may be utilized. A Slave might not be able to support a 26 MHz clock frequency during a read operation. In this case, known as Half Speed operation, a 13 MHz clock frequency may be implemented for only the read back.

Table 3-33 RFFE data

Symbol	Description	Half speed device		Full speed device		Units
		Min	Max	Min	Max	
Tsclkoh	Clock output high time	24		11.25		ns
Tsclkol	Clock output low time	24		11.25		ns
Tsclkotr	Clock output transition (rise/fall) time1	3.5	10	3.5	6.5	ns
Tsclkdch	Clock output duty cycle high time2,3	45	55	45	55	ns
Tsclkdcl	Clock output duty cycle low time2,3	45	55	45	55	ns

Table 3-34 Rx/Tx data

Parameter	Description	LSL	USL	units
Tsu	Rx Data setup time w.r.t falling edge of clock	15.75	N/A	ns
Thd	Rx Data hold time w.r.t falling edge of clock	0	N/A	ns
Tpd	Tx data output delay w.r.t rising edge of clock	NA	10.25	ns
TclHigh	Tx clock duty cycle	0.45*Tck	0.55*Tck	ns

3.12.2 System power management interface (SPMI)

Table 3-35 Supported SPMI standards and exceptions

Applicable standard	Feature exceptions	MSM variations
MIPI Alliance Specification for System Power Management Interface (SPMI) version 1.0	None	None

Table 3-36 Supported SPMI standards and exceptions

Interface	Parameter	Description	Target frequency	Spec min	Spec max	Units
SPMI	tsu	Input data set up time	19.2 MHz	1	1	ns
	thd	Input data hold time		5	5	ns
	tdataZ	data release time		-	11	ns
	tpd	Output data delay		-	11	ns

4 Mechanical Information

4.1 Device physical dimensions

The MSM8x16 is available in the 760-pin nanoscale package (NSP) that includes dedicated ground pins for improved grounding, mechanical strength, and thermal continuity. The 760 NSP has a 14.0 mm × 12.0 mm body with a maximum height of 0.96 mm. Pin A1 is located by an indicator mark on the top of the package, and by the ball pattern when viewed from below. A simplified version of the 760NSP outline drawing is shown in Figure 4-1.

NOTE Click the link below to download the 760 NSP outline drawing (NT90-NK468-1) from the CDMA Tech Support website.

https://downloads.cdmatech.com/qdc/drl/objectId/090100148263475c

https://downloads.cdmatech.com/qdc/drl/objectId/09010014826f4811

If you have permission to view the document, a prompt will be presented for initiating the download.

NOTE Subscribe to the package drawing to be notified of any changes.

Click the **Help** button to download the latest revision of *Using CDMATech Support Documents and Downloads User Guide* (80-V7273-1). This document includes subscription instructions.

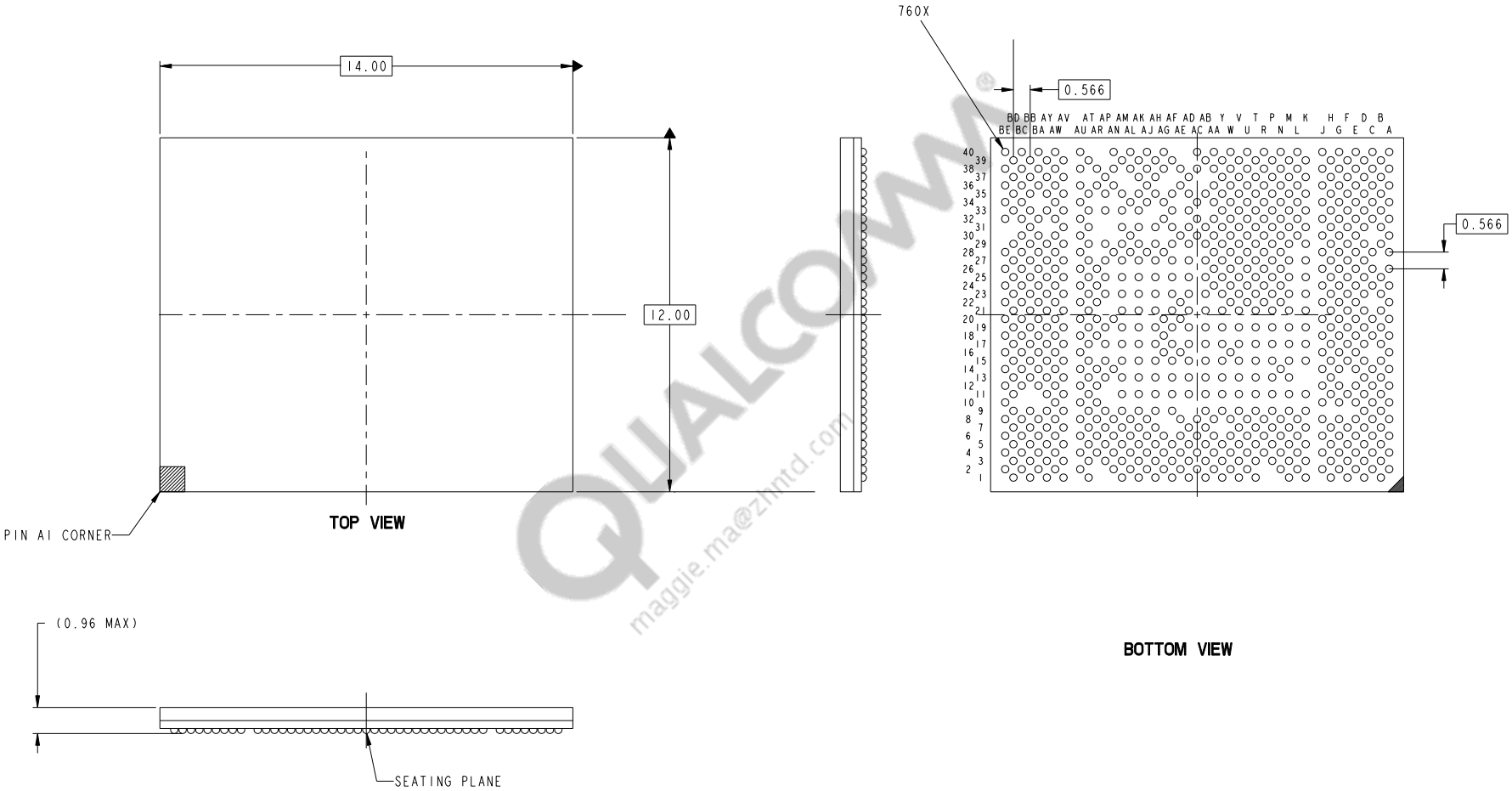

Figure 4-1 760 NSP (14.0 × 12.0 × 0.96 mm) outline drawing

NOTE This is a simplified outline drawing. Click the link below to download the complete, up-to-date package outline drawing:

https://downloads.cdmatech.com/qdc/drl/objectId/090100148263475c

https://downloads.cdmatech.com/qdc/drl/objectId/09010014826f4811

4.2 Part marking

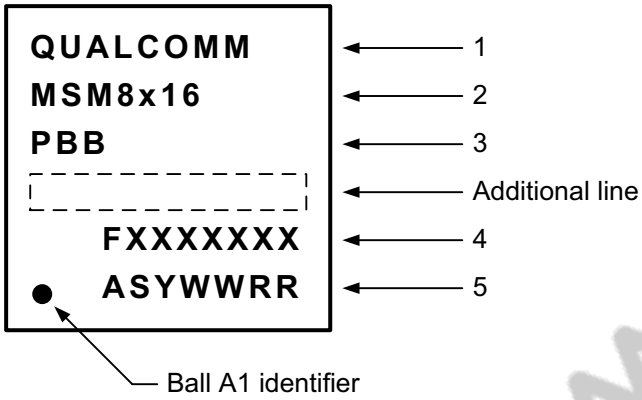

Figure 4-2 MSM8x16 device marking (top view, not to scale)

4.2.1 Specification-compliant devices

Table 4-1 MSM8x16 device marking line definitions

Line	Marking	Description
1	QUALCOMM	Qualcomm® name or logo
2	MSM8x16	QTI product name x = 2, 6, 9 (see Table 4-2 for differences)
3	PBB	P = product configuration code (see Table 4-2) BB = feature code (see Table 4-2)
An additional line may appear on the part marking for some samples; this is manufacturing information that is only relevant to QTI and QTI suppliers.		
4	FXXXXXXX	F = supply source code ■ F = A (for GF) ■ F = B (for TSMC) ■ F = C (for Samsung) XXXXXXX = traceability number
5	ASYWWRR	A = assembly site code ■ A = U (Amkor, Shanghai) ■ A = K (SPIL Taiwan) ■ A = V (STATSChipPAC, China) ■ A = E (ASE, Kaohsiung, Taiwan) S = assembly sequence number Y = single-digit year code WW = work week (based on calendar year) RR = product revision (see Table 4-2)

NOTE For complete marking definitions of all MSM8x16 variants and revisions, refer to the *MSM8216/MSM8616/MSM8916 Device Revision Guide* (80-NK807-4).

4.2.2 Daisy-chain devices

This information will be included in future revisions of this document.

4.3 Device ordering information

4.3.1 Specification-compliant devices

This device can be ordered using the identification code shown in Figure 4-3 and explained below.

Device ID code ►	AAA-AAAA	— P	— CCC	DDD	— EE	— RR	— S	— BB
Symbol definition ►	Product name	Config code	Number of pins	Package type	Shipping package	Product version	Source code	Feature code
Example ►	MSM-8916	— 0	— 760	NSP	— TR	— 00	— 0	— VV

Figure 4-3 MSM8x16 device identification code

Device ordering information details for all samples available to date are summarized in Table 4-2.

Table 4-2 Device identification code/ordering information details

Device	Product configuration code (P)	Product revision (RR)	HW revision number	FEATURE_ID	Sample type	HW revision	S value	BB value [2]	Comments
MSM8916	3	00	0x0 0705 0E1	03	ES/CS	v 1.0	0	VV	LTE/UMTS/CDMA/TDS/GSM, 1.2 GHz A53, 1920 x 1080, 8 MP/13 MP
	4	00	0x0 0705 0E1	04	ES/CS	v 1.0	0	VV	LTE/UMTS/TDS/GSM, 1.2 GHz A53, 1920 x 1080, 8 MP/13 MP
	5	00	0x0 0705 0E1	05	ES/CS	v 1.0	0	VV	LTE/UMTS/CDMA/TDS/GSM, 1.2 GHz A53, 1280 x 720, 8 MP/13 MP
	6	00	0x0 0705 0E1	06	ES/CS	v 1.0	0	VV	LTE/UMTS/TDS/GSM, 1.2 GHz A53, 1280 x 720, 8 MP/13 MP
	7	00	0x0 0705 0E1	07	ES/CS	v 1.0	0	VV	LTE/TDS/GSM, 1.2 GHz A53, 1280 x 720, 8 MP/13 MP
	0	00	0x0 0705 0E1	00	ES/CS	v 1.0	0	VV	LTE/UMTS/CDMA/TDS/GSM, 1.2 GHz A53, qHD, 8 MP/13 MP
	1	00	0x0 0705 0E1	01	ES/CS	v 1.0	0	VV	LTE/UMTS/TDS/GSM, 1.2 GHz A53, qHD, 8 MP/13 MP
	8	00	0x0 0705 0E1	08	ES/CS	v 1.0	0	VV	LTE/TDS/GSM, 1.2 GHz A53, qHD, 8 MP/13 MP
MSM8216	1	00	0x0 0707 0E1	01	ES/CS	v 1.0	0	VV	UMTS/TDS/GSM, 1.2 GHz A53, 1280 x 720, 8 MP/13 MP
MSM8616	1	00	0x0 0709 0E1	01	ES/CS	v 1.0	0	VV	CDMA/UMTS/TDS/GSM, 1.2 GHz A53, 1280 x 720 8 MP/13 MP

1. “S” is the source configuration code that identifies all of the qualified die fabrication-source combinations available at the time a particular sample type was shipped. S values are defined in Table 4-3.
2. “BB” is the feature code that identifies an IC’s specific feature set, which distinguishes it from other versions or variants. All feature sets available at the time of this document’s release are defined in Table 4-2.

NOTE Devices with date code (YWW) = 1423 or later are CS devices

Table 4-3 Source configuration code

S value	Die	F value = A	F value = B	F value = C
0	Digital	GF	TSMC	Samsung
Other columns and rows will be added in future revisions of this document, if needed.				

4.3.2 Daisy-chain devices

This information will be included in future revisions of this document.

4.4 Device moisture-sensitivity level

Plastic-encapsulated surface mount packages are susceptible to damage induced by absorbed moisture and high temperature. A package's moisture-sensitivity level (MSL) indicates its ability to withstand exposure after it is removed from its shipment bag, while it is on the factory floor awaiting PCB installation. A low MSL rating is better than a high rating; a low MSL device can be exposed on the factory floor longer than a high MSL device. All pertinent MSL ratings are summarized in Table 4-4.

Table 4-4 MSL ratings summary

MSL	Out-of-bag floor life	Comments
1	Unlimited	≤ 30°C / 85% RH
2	1 year	≤ 30°C / 60% RH
2a	4 weeks	≤ 30°C / 60% RH
3	168 hours	≤ 30°C / 60% RH
4	72 hours	≤ 30°C / 60% RH
5	48 hours	≤ 30°C / 60% RH
5a	24 hours	≤ 30°C / 60% RH
6	Mandatory bake before use. After bake, must be re-flowed within the time limit specified on the label.	≤ 30°C / 60% RH

QTI follows the latest IPC/JEDEC J-STD-020 standard revision for moisture-sensitivity qualification. ***The MSM8x16 device samples are currently classified as MSL3 at 255 (+5, -0)°C.*** This qualification temperature (255 (+5, -0)°C) should not be confused with the peak temperature within the recommended solder reflow profile (see Section 6.2.3 for more details).

4.5 Thermal characteristics

Rather than provide thermal resistance values Θ_{JC} and Θ_{JA}, validated thermal-package models are provided through the CDMA Tech Support website. A thermal model for each device is provided within the *Power_Thermal* subfolder for each chipset family. Designers can obtain thermal resistance values by conducting their own thermal simulations.

NOTE Click the link below to download the MSM8x16 thermal-package model from the CDMA Tech Support website.

The thermal package models can be found in downloads.cdma.tech.com under the folder:

library/8916/HW/Power_Thermal/Packages Thermal Models

If you have permission to view the document, a prompt will be presented for initiating the download.

NOTE Subscribe to the MSM8x16 thermal-package model to be notified of any changes.

Click the **Help** button to download the latest revision of *Using CDMA Tech Support Documents and Downloads User Guide* (80-V7273-1). This document includes subscription instructions

5 Carrier, Storage, & Handling Information

5.1 Carrier

5.1.1 Tape and reel information

All QTI carrier tape systems conform to EIA-481 standards.

A simplified sketch of the MSM8x16 tape carrier is shown in Figure 5-1, including the proper part orientation, maximum number of devices per reel, and key dimensions.

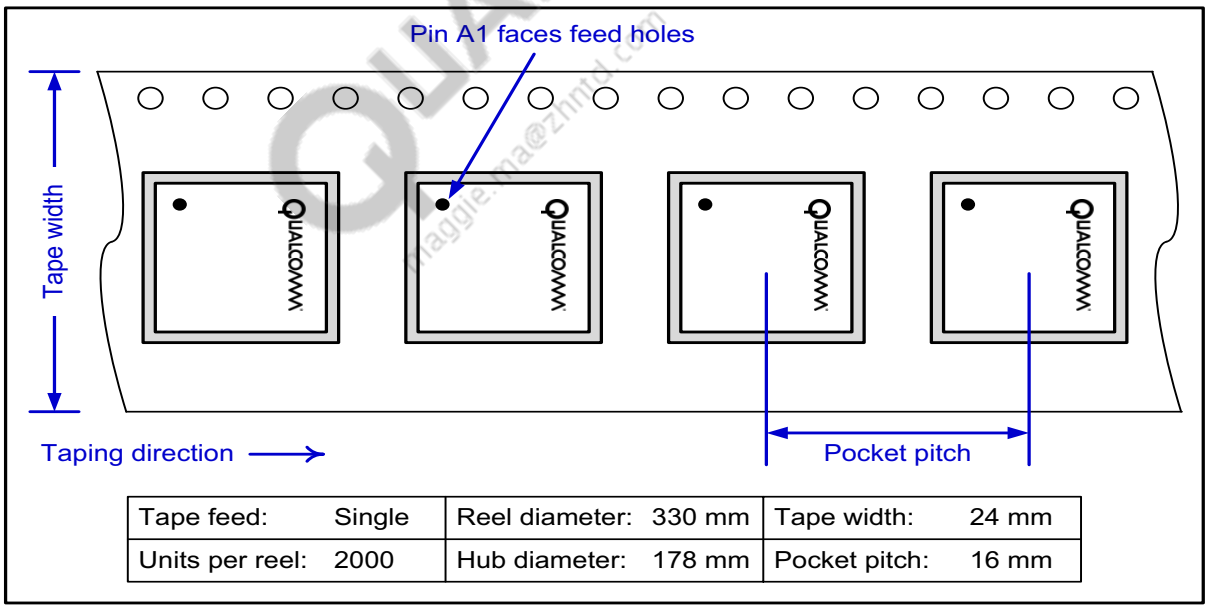

Figure 5-1 Carrier tape drawing with part orientation

Tape-handling recommendations are shown in Figure 5-2.

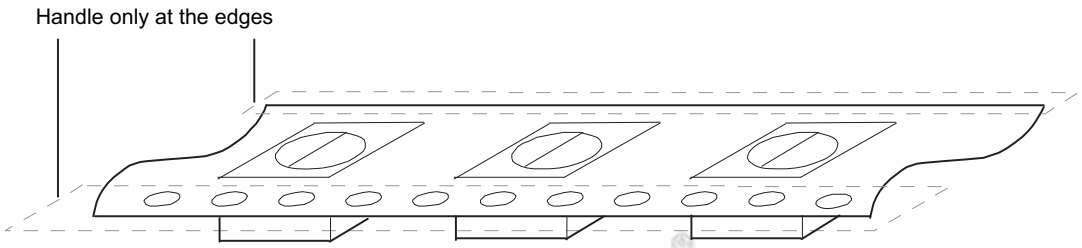

Figure 5-2 Tape handling

5.2 Storage

5.2.1 Bagged storage conditions

MSM8x16 devices delivered in tape and reel carriers must be stored in sealed, moisture barrier, anti-static bags. If the storage environment maintains an ambient temperature lower than 40°C and relative humidity less than 90%, the expected shelf life is at least 24 months.

5.2.2 Out-of-bag duration

The out-of-bag duration is the time a device can be on the factory floor before being installed onto a PCB. It is defined by the device MSL rating, as described in Section 4.4.

5.3 Handling

Tape handling was discussed in Section 5.1.1. Other (IC-specific) handling guidelines are presented below.

5.3.1 Baking

It is **not necessary** to bake the MSM8x16 if the conditions specified in Section 5.2.1 and Section 5.2.2 have **not been exceeded**.

It is **necessary** to bake the MSM8x16 if any condition specified in Section 5.2.1 or Section 5.2.2 has **been exceeded**. The baking conditions are specified on the moisture-sensitive caution label attached to each bag; see *ASIC Packing Methods and Materials Specification* (80-VK055-1) for details.

CAUTION If baking is required, the devices must be transferred into trays that can be baked to at least 125°C. Devices should not be baked in tape and reel carriers at any temperature.

5.3.2 Electrostatic discharge

Electrostatic discharge (ESD) occurs naturally in laboratory and factory environments. An established high-voltage potential is always at risk of discharging to a lower potential. If this discharge path is through a semiconductor device, it may result in destructive damage.

ESD countermeasures and handling methods must be developed and used to control the factory environment at each manufacturing site.

QTI products must be handled according to the ESD Association standard: ANSI/ESD S20.20-1999, *Protection of Electrical and Electronic Parts, Assemblies, and Equipment*.

Refer to Chapter 7 for the MSM8x16 device ESD ratings.

5.4 Barcode label and packing for shipment

Refer to the *ASIC Packing Methods and Materials Specification* (80-VK055-1) for all packing-related information, including barcode-label details.

6 PCB Mounting Guidelines

6.1 RoHS compliance

The device is lead-free and RoHS-compliant. Its SnAgCu solder balls use SAC305 composition on the top and SAC125/Ni on the bottom. QTI defines its lead-free (or Pb-free) semiconductor products as having a maximum lead concentration of 1000 ppm (0.1% by weight) in raw (homogeneous) materials and end products. QTI package environmental programs, RoHS compliance details, and tables defining pertinent characteristics of all QTI ASIC products are described in the *IC Package Environmental Roadmap* (80-V6921-1).

6.2 SMT parameters

This section describes QTI board-level characterization process parameters. It is included to assist customers with their SMT process development; it is not intended to be a specification for their SMT processes.

6.2.1 Land pad and stencil design

The land pattern and stencil recommendations presented in this section are based on QTI internal characterizations for lead-free solder pastes on an eight-layer PCB, built primarily to the specifications described in JEDEC JESD22-B111.

QTI recommends characterizing the land patterns according to each customer's processes, materials, equipment, stencil design, and reflow profile prior to PCB production. Optimizing the solder stencil pattern design and print process is critical to ensure print uniformity, decrease voiding, and increase board-level reliability.

General land pattern guidelines:

- Non-solder-mask-defined (NSMD) pads provide the best reliability.
- Keep the solderable area consistent for each pad, especially when mixing via-in-pad and non-via-in-pad in the same array.
- Avoid large solder mask openings over ground planes.
- Traces for external routing are recommended to be less than or equal to half the pad diameter, to ensure consistent solder-joint shapes.

One key parameter that should be evaluated is the ratio of aperture area to sidewall area, known as the area ratio (AR). QTI recommends square apertures for optimal solder-paste release. In this case, a simple equation can be used relating the side length of the aperture to the stencil thickness (as shown and explained in Figure 6-1). Larger area ratios enable better transfer of solder paste to the PCB, minimize defects, and ensure a more stable printing process. Inter-aperture spacing should be at least as thick as the stencil; otherwise, paste deposits may bridge.

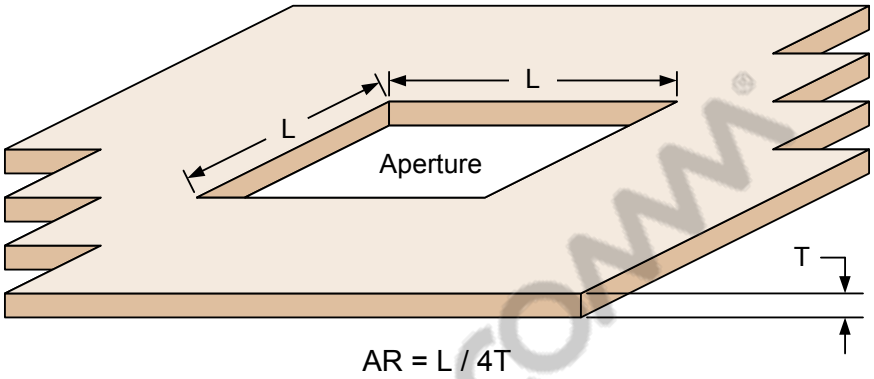

Figure 6-1 Area ratio (AR)

QTI provides an example PCB land pattern and stencil design for the 760 NSP.

NOTE Click the link below to download the 760 NSP land/stencil drawing (LS90-NG134-1) from the CDMA Tech Support website.

https://downloads.cdmatech.com/qdc/drl/objectId/09010014820ce73e

If you have permission to view the document, a prompt will be presented for initiating the download.

NOTE Subscribe to the land/stencil drawing to be notified of any changes.

Click the **Help** button to download the latest revision of *Using CDMA Tech Support Documents and Downloads User Guide* (80-V7273-1). This document includes subscription instructions.

6.2.2 Reflow profile

Reflow profile conditions typically used by QTI for lead-free systems are listed in Table 6-1, and are shown in Figure 6-2.

Table 6-1 QTI typical SMT reflow profile conditions (for reference only)

Profile stage	Description	Temp range	Condition
Preheat	Initial ramp	< 150°C	3°C/sec max
Soak	Flux activation	150 to 190°C	60 to 75 sec
Ramp	Transition to liquidus (solder-paste melting point)	190 to 220°C	< 30 sec

Table 6-1 QTI typical SMT reflow profile conditions (for reference only) (cont.)

Profile stage	Description	Temp range	Condition
Reflow	Time above liquidus	220 to 245°C [1]	50 to 70 sec
Cool down	Cool rate – ramp to ambient	< 220°C	6°C/sec max

1. During the reflow process, the recommended peak temperature is 245°C (minimum). This temperature should not be confused with the peak temperature reached during MSL testing, as described in Section 6.2.3.

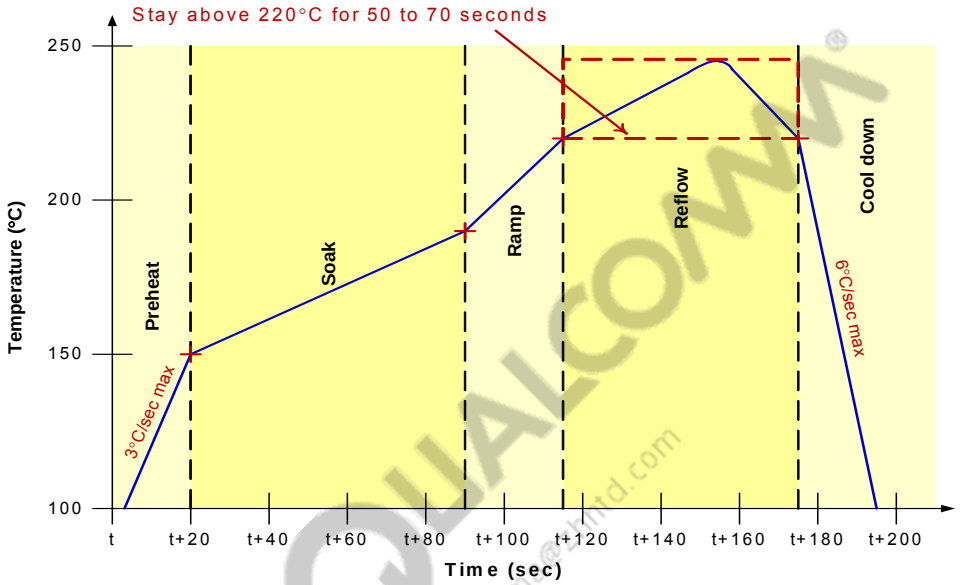

Figure 6-2 QTI typical SMT reflow profile

6.2.3 SMT peak package-body temperature

This document states a peak package-body temperature in three other places within this document; without explanation, they may appear to conflict. The three places are listed below, along with an explanation of the stated value and its meaning within that section's context.

- Section 4.4 – *Device moisture-sensitivity level*

  MSM8x16 devices are classified as MSL3@255°C. The temperature (255°C) included in this designation is the lower limit of the range stated for moisture resistance testing during the device qualification process, as explained immediately below.

- Section 7.1 – *Reliability qualifications summary*

  One of the tests conducted for device qualification is the moisture resistance test. QTI follows J-STD-020-C, and hits a peak reflow temperature that falls within the range of 260°C +0/-5°C (255°C to 260°C).

- Section 6.2.2 – *Reflow profile*

  During a production board's reflow process, the temperature experienced by the package must be controlled. Obviously, the temperature must be high enough to melt the solder and provide reliable connections, but it must not go so high that the device can be damaged. The recommended peak temperature during production assembly is 245°C. This is comfortably

above the solder melting point (220°C), yet well below the proven temperature reached during qualification (255°C or more).

6.2.4 SMT process verification

QTI recommends verification of the SMT process prior to high-volume board assembly, including:

- In-line solder-paste deposition monitoring
- Reflow profile measurement and verification
- Visual and x-ray inspection after soldering to confirm adequate alignment, solder voids, solder-ball shape, and solder bridging
- Cross-section inspection of solder joints for wetting, solder-ball shape, and voiding

6.3 Daisy-chain components

Daisy-chain packages use the same processes and materials as actual products; they are recommended for SMT characterization and board-level reliability testing. In fact, all SMT process recommendations described above can be performed using daisy-chain components.

Ordering information is given in Section 4.3.2.

Daisy-chain PCB routing recommendations are available for download.

NOTE Click the link below to download the 760 NSP daisy-chain interconnect drawing (DS90-NK468-1) from the CDMA Tech Support website.

https://downloads.cdmatech.com/qdc/drl/objectId/09010014824e2c61

If you have permission to view the document, a prompt will be presented for initiating the download.

NOTE Subscribe to the daisy-chain interconnect drawing to be notified of any changes.

Click the **Help** button to download the latest revision of *Using CDMA Tech Support Documents and Downloads User Guide* (80-V7273-1). This document includes subscription instructions.

6.4 Board-level reliability

QTI conducts characterization tests to assess the device's board-level reliability, including the following physical tests on evaluation boards:

- Drop shock (JESD22-B111)
- Temperature cycling (JESD22-A104)
- Cyclic bend testing – optional (JESD22-B113)

Board-level reliability data is available for download.

NOTE Click the link below to download the 760 NSP board-level reliability data (BR80-NK468-1) from the CDMA Tech Support website.

This link will be included in future revisions of this document.

If you have permission to view the document, a prompt will be presented for initiating the download.

NOTE Subscribe to the board-level reliability document to be notified of any changes.

Click the **Help** button to download the latest revision of *Using CDMA Tech Support Documents and Downloads User Guide* (80-V7273-1). This document includes subscription instructions.

6.5 High-temperature warpage

QTI measures high-temperature warpage using a shadow moire system; the measured data is available for download.

NOTE Click the link below to download the 760 NSP high-temperature warpage data (WR80-NK468-1) from the CDMA Tech Support website.

https://downloads.cdmatech.com/qdc/drl/objectId/09010014827d9ec5

If you have permission to view the document, a prompt will be presented for initiating the download.

NOTE Subscribe to the high-temperature warpage document to be notified of any changes.

Click the **Help** button to download the latest revision of *Using CDMA Tech Support Documents and Downloads User Guide* (80-V7273-1). This document includes subscription instructions.

7 Part Reliability

7.1 Reliability evaluation summary

7.1.1 MSM8x16 reliability evaluation report for device from GF-F8

Table 7-1 Silicon reliability results

Tests, standards, and conditions	Sample size	Result
DPPM rate (ELFR) and average failure rate (AFR) in FIT (λ) failure in billion device-hours HTOL: JESD22-A108-D Total samples from three different wafer lots	356	DPPM < 1000 Cum FITs < 25 FITs
Mean time to failure (MTTF) t = 1/λ in million hours Total samples from three different wafer lots	356	> 40
ESD – human-body model (HBM) rating: JESD22-A114-F Total samples from one wafer lot	3	2000 V
ESD – charge-device model (CDM) rating: JESD22-C101-D Target: 500 V Total samples from one wafer lot	3	500 V
Latch-up (I-test): EIA/JESD78C Trigger current: ±100 mA; temperature: 85°C Total samples from one wafer lot	6	Pass
Latch-up (V supply overvoltage): EIA/JESD78A Trigger voltage: each VDD pin, stress at 1.5 × V_{dd} max per device specification; temperature: 85°C Total samples from one wafer lot	6	Pass

NOTE Cum FITs from multiple products under GF F8, 28 nm LP process.

Table 7-2 Package reliability results

Tests, standards, and conditions	ATC assembly source sample size	SPIL assembly source sample size	ASE assembly source sample size	SCC assembly source sample size	Result
Moisture resistance test (MRT): J-STD-020 Reflow at 260°C +0/-5°C Total samples from three different assembly lots at each SAT	480	480	480	480	Pass
Temperature cycle: JESD22-A104-D Temperature: -55°C to 125C; number of cycles: 1000 Soak time at minimum/maximum temperature: 8–10 mins. Cycle rate: 2 cycles per hour (CPH) **Preconditioning:** JESD22-A113 MSL 1, reflow temperature: 260°C +0/-5°C Total samples from three different assembly lots at each SAT	240	240	240	240	Pass
Unbiased highly accelerated stress test: JESD22-A118 130°C/85% RH and 96 hrs duration Preconditioning: JESD22-A113-F MSL 1, reflow temperature: 260°C +0/-5°C Total samples from three different assembly lots at each SAT	240	240	240	240	Pass
Biased highly accelerated stress test: JESD22-A110 130°C/85% RH and 264 hrs duration Preconditioning: JESD22-A113-F MSL 1, reflow temperature: 260°C +0/-5°C Total samples from three different assembly lots at each SAT **Data is bridged from the 488 NSP 12 × 12 mm package. **Data is bridged from the 745 PNSP 12 × 12 mm package.	135*	135*	135**	135*	Pass
High-temperature storage life: JESD22-A103-C Temperature 150°C, 500, 1000 hrs. Total samples from three different assembly lots at each SAT	240	240	240	240	Pass

Table 7-2 Package reliability results (cont.)

Tests, standards, and conditions	ATC assembly source sample size	SPIL assembly source sample size	ASE assembly source sample size	SCC assembly source sample size	Result
Flammability UL-STD-94 UL-STD-94 **Note**: flammability test – not required UL-STD-94 QTI ICs are exempt from the flammability requirements due to their sizes per UL/EN 60950-1, as long as they are mounted on materials rated V-1 or better. Most PWBs onto which our ICs mounted are rated V-0 (better than V-1).	N/A	N/A	N/A	N/A	
Physical dimensions: JESD22-B100-A Case outline drawing: QTI internal document Total samples from three different assembly lots at each SAT	75	75	75	75	Pass
Solder ball shear: JESD22-B117 Total samples from three different assembly lots at each SAT	30	30	30	30	Pass
Internal/external visual Total samples from three different assembly lots at each SAT	75	75	75	75	Pass

7.1.2 MSM8x16 reliability evaluation report for device from TSMC-F15

Table 7-3 Silicon reliability results

Tests, standards, and conditions	Sample size	Result
DPPM rate (ELFR) and average failure rate (AFR) in FIT (λ) failure in billion device-hours HTOL: JESD22-A108-D Total samples from three different wafer lots	360	DPPM < 1000 Cum FITs < 25 FITs
Mean time to failure (MTTF) t = 1/λ in million hours Total samples from three different wafer lots	360	> 40
ESD – human-body model (HBM) rating: JESD22-A114-F Total samples from one wafer lot	3	2000 V

Table 7-3 Silicon reliability results (cont.)

Tests, standards, and conditions	Sample size	Result
ESD – charge-device model (CDM) rating: JESD22-C101-D Target: 500 V Total samples from one wafer lot	3	500 V
Latch-up (I-test): EIA/JESD78C Trigger current: ±100 mA; temperature: 85°C Total samples from one wafer lot	6	Pass
Latch-up (V supply overvoltage): EIA/JESD78A Trigger voltage: each VDD pin, stress at 1.5 × V_{dd} max per device specification; temperature: 85°C Total samples from one wafer lot	6	Pass

NOTE Cum FITs from multiple products under TSMC-F15, 28 nm LP process.

Table 7-4 Package reliability results

Tests, standards, and conditions	ATC assembly source sample size	SPIL assembly source sample size	ASE assembly source sample size	SCC assembly source sample size	Result
Moisture resistance test (MRT): J-STD-020 Reflow at 260°C +0/-5°C Total samples from three different assembly lots at each SAT	480	480	480	480	Pass
Temperature cycle: JESD22-A104-D Temperature: -55°C to 125°C; number of cycles: 1000 Soak time at minimum/maximum temperature: 8–10 mins. Cycle rate: 2 cycles per hour (CPH) **Preconditioning:** JESD22-A113 MSL 1, reflow temperature: 260°C +0/-5°C Total samples from three different assembly lots at each SAT	240	240	240	240	Pass

Table 7-4 Package reliability results (cont.)

Tests, standards, and conditions	ATC assembly source sample size	SPIL assembly source sample size	ASE assembly source sample size	SCC assembly source sample size	Result
Unbiased highly accelerated stress test: JESD22-A118 130°C/85% RH and 96 hrs. duration Preconditioning: JESD22-A113-F MSL 1, reflow temperature: 260°C +0/-5°C Total samples from three different assembly lots at each SAT	240	240	240	240	Pass
Biased highly accelerated stress test: JESD22-A110 130°C/85% RH and 264 hrs duration Preconditioning: JESD22-A113-F MSL 1, reflow temperature: 260°C +0/-5°C Total samples from three different assembly lots at each SAT *Data is bridged from the 488 NSP 12 × 12 mm package. **Data is bridged from the 745 PNSP 12 × 12 mm package.	135*	135*	135**	135*	Pass
High-temperature storage life: JESD22-A103-C Temperature 150°C, 500, 1000 hrs. Total samples from three different assembly lots at each SAT	240	240	240	240	Pass
Flammability UL-STD-94 UL-STD-94 **Note**: Flammability test – not required UL-STD-94 QTI ICs are exempt from the flammability requirements due to their sizes per UL/EN 60950-1, as long as they are mounted on materials rated V-1 or better. Most PWBs onto which our ICs mounted are rated V-0 (better than V-1).	N/A	N/A	N/A	N/A	
Physical dimensions: JESD22-B100-A Case outline drawing: QTI internal document Total samples from three different assembly lots at each SAT	75	75	75	75	Pass

Table 7-4 Package reliability results (cont.)

Tests, standards, and conditions	ATC assembly source sample size	SPIL assembly source sample size	ASE assembly source sample size	SCC assembly source sample size	Result
Solder ball shear: JESD22-B117 Total samples from three different assembly lots at each SAT	30	30	30	30	Pass
Internal/external visual Total samples from three different assembly lots at each SAT	75	75	75	75	Pass

7.1.3 MSM8916 reliability evaluation report for device from Samsung

Table 7-5 Section A: Silicon reliability results

Tests, standards, and conditions	Sample size	Result
DPPM rate (ELFR) and average failure rate (AFR) in FIT (λ) failure in billion device-hours HTOL: JESD22-A108-D Total samples from three different wafer lots	456	DPPM < 1000 Cum FITs < 25 FITs
Mean time to failure (MTTF) t = 1/λ in million hours Total samples from three different wafer lots	456	> 40
ESD – human-body model (HBM) rating: JESD22-A114-F Total samples from one wafer lot	3	2000 V
ESD – charge-device model (CDM) rating: JESD22-C101-D Target: 500 V Total samples from one wafer lot	3	500 V
Latch-up (I-test): EIA/JESD78C Trigger current: ±100 mA; temperature: 85C Total samples from one wafer lot	6	Pass
Latch-up (V supply overvoltage): EIA/JESD78A Trigger voltage: each VDD pin, stress at 1.5 × Vdd max per device specification; temperature: 85°C Total samples from one wafer lot	6	Pass

NOTE Cum FITs from multiple products under the Samsung-F15, 28 nm LP process.

Table 7-6 Section B: Package reliability results

Tests, standards, and conditions	ATC assembly source sample size	SPIL assembly source sample size	ASE assembly source sample size	SCC assembly source sample size	Result
Moisture resistance test (MRT): J-STD-020 Reflow at 260°C +0/-5°C Total samples from three different assembly lots at each SAT	480	480	480	480	Pass
Temperature cycle: JESD22-A104-D Temperature: -55°C to 125C; number of cycles: 1000 Soak time at minimum/maximum temperature: 8–10 mins. Cycle rate: 2 cycles per hour (CPH) **Preconditioning:** JESD22-A113 MSL 3, reflow temperature: 260°C +0/-5°C Total samples from three different assembly lots at each SAT	240	240	240	240	Pass
Unbiased highly accelerated stress test: JESD22-A118 130°C/85% RH and 96 hrs. duration Preconditioning: JESD22-A113-F MSL 3, reflow temperature: 260°C +0/-5°C Total samples from three different assembly lots at each SAT	240	240	240	240	Pass
Biased highly accelerated stress test: JESD22-A110 130°C/85% RH and 264 hrs. duration Preconditioning: JESD22-A113-F MSL 3, reflow temperature: 260°C +0/-5°C Total samples from three different assembly lots at each SAT *Data is bridged from the 488 NSP 12 × 12 mm PKG. **Data is bridged from the 745 PNSP 12 × 12 mm PKG	135*	135*	135**	135*	Pass

Table 7-6 Section B: Package reliability results (cont.)

Tests, standards, and conditions	ATC assembly source sample size	SPIL assembly source sample size	ASE assembly source sample size	SCC assembly source sample size	Result
High-temperature storage life: JESD22-A103-C Temperature 150°C, 500, 1000 hrs. Total samples from three different assembly lots at each SAT	240	240	240	240	Pass
Flammability UL-STD-94 UL-STD-94 **Note**: Flammability test – not required UL-STD-94 QTI ICs are exempt from the flammability requirements due to their sizes per UL/EN 60950-1, as long as they are mounted on materials rated V-1 or better. Most PWBs onto which our ICs mounted are rated V-0 (better than V-1).	N/A	N/A	N/A	N/A	
Physical dimensions: JESD22-B100-A Case outline drawing: QTI internal document Total samples from three different assembly lots at each SAT	75	75	75	75	Pass
Solder ball shear: JESD22-B117 Total samples from three different assembly lots at each SAT	30	30	30	30	Pass
Internal/external visual Total samples from three different assembly lots at each SAT	75	75	75	75	Pass

7.2 Qualification sample description

Device characteristics

Device name:	MSM8x16
Package type:	760 NSP
Package body size:	14 mm × 12 mm × 0.96 mm
Fab process:	28 nm CMOS
Fab sites:	GF TSMC Samsung
Assembly sites:	Amkor, Shangai SPIL, Taiwan (SPT) STATSChipPAC, China (SCC) ASE, Kaohsiung, Taiwan
Solder ball pitch:	0.4 mm