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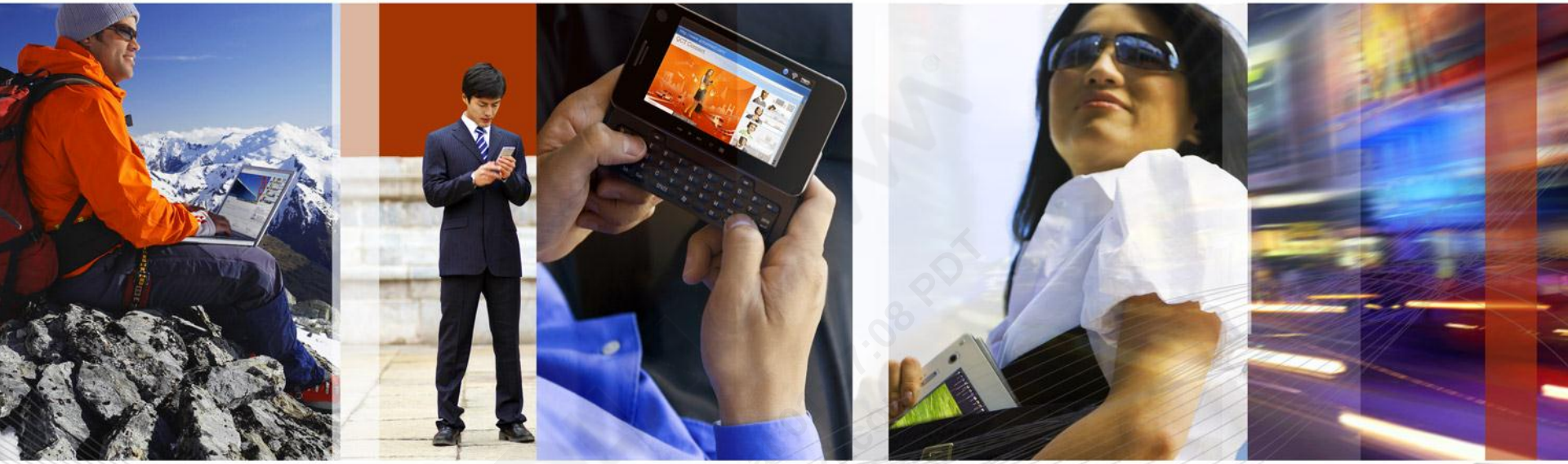

QUALCOMM CDMA Technologies

REDEFINING MOBILITY

MSM8274/MSM8674/MSM8974 Chipset Training Slides

System Topic

80-NA437-23 Rev. B

QUALCOMM Incorporated
5775 Morehouse Drive
San Diego, CA 92121-1714
U.S.A.

Revision History

Revision	Date	Description
A	August 2, 2012	Initial release
B	August 28, 2012	Removed slides describing the pins. Updated subsystem name and added two acronyms (Slide 17) Updated power features with new color legend, indicating enhanced and new features (Slide 18) Updated the list of package thermal models (Slide 25) Updated device name in the title (Slide 28)

Contents

Power Distribution Network (PDN)

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Power Distribution Network Requirements

- PDN requirements are listed below:

Power domain	Max impedance DC to 10 Hz	Max impedance 10 Hz to 25 MHz
VDD_CORE	10 mΩ	22 mΩ
VDD_GFX	10 mΩ	56 mΩ
VDD_KRAIT	2 mΩ	17 mΩ
VDD_MEM	10 mΩ	18 mΩ
VDD_MODEM	10 mΩ	57 mΩ

- Design guidelines are provided in *Power Delivery Network Design* (80-VT310-13).

Thermal vs. PDN

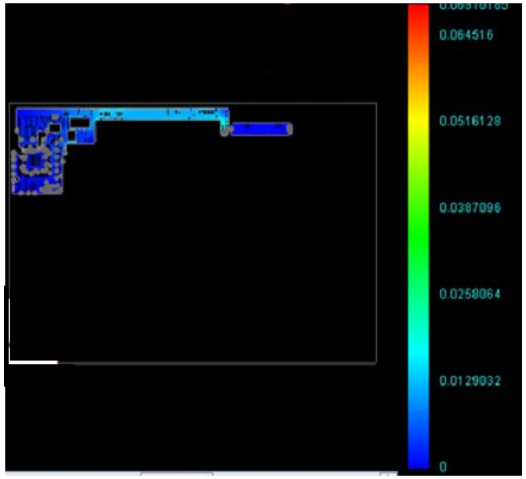
Question: What is the recommended distance between the PMIC and the processor (MSM8974) power supply pins?

Answer:

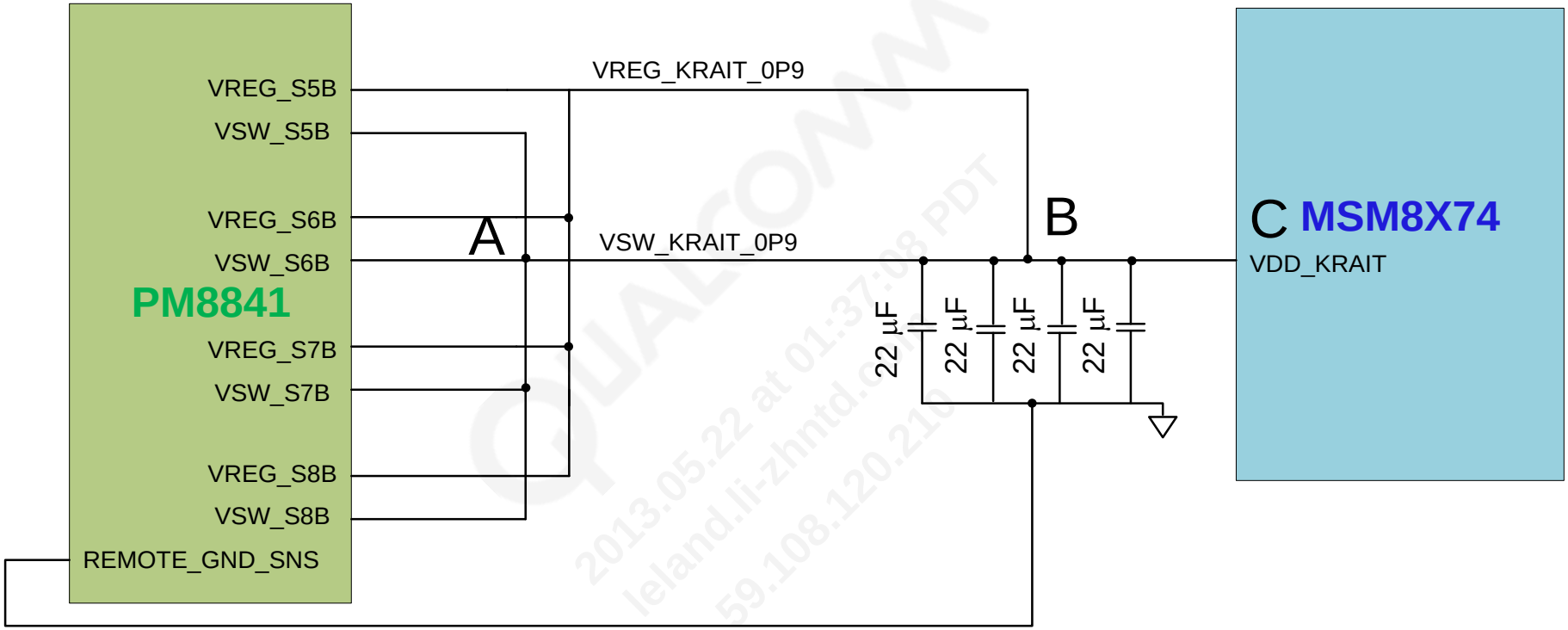
- The PCB placement distance between the PMIC and the processor must be determined from the results of phone level thermal simulations using commercial available thermal simulation software (e.g., Icepak or FloTHERM®).
  - Placing the PMIC and the processor too close together on the PCB can greatly compromise the design from a thermal perspective.
- Once the placement of the PMIC and the processor has been defined by thermal simulation, PDN traces should be routed and verified by simulation in order to meet device specification requirements.
- Meeting PDN requirements will guarantee no functional failure due to PDN under worst case temperature and process variations.

Static DC IR Drop

- Calculate the resistance of power trace between PMIC and MSM™ using:
  - R = ρ (L/A) where
  - ρ = Resistivity of copper
  - L = Length of trace
  - A = Cross-section area = width of trace × thickness of trace
- Calculate the minimum number of vias required to carry the current. Always use more vias than the minimum required.
  - Minimum vias ≥ Total current/Current carrying capacity of each via
  - Copper paste filled vias are used in certain PCBs. Copper paste is electrically and thermally less conductive than copper. More vias are required when using copper paste vias.
- Static IR drop analysis shows current densities at different locations in the layout



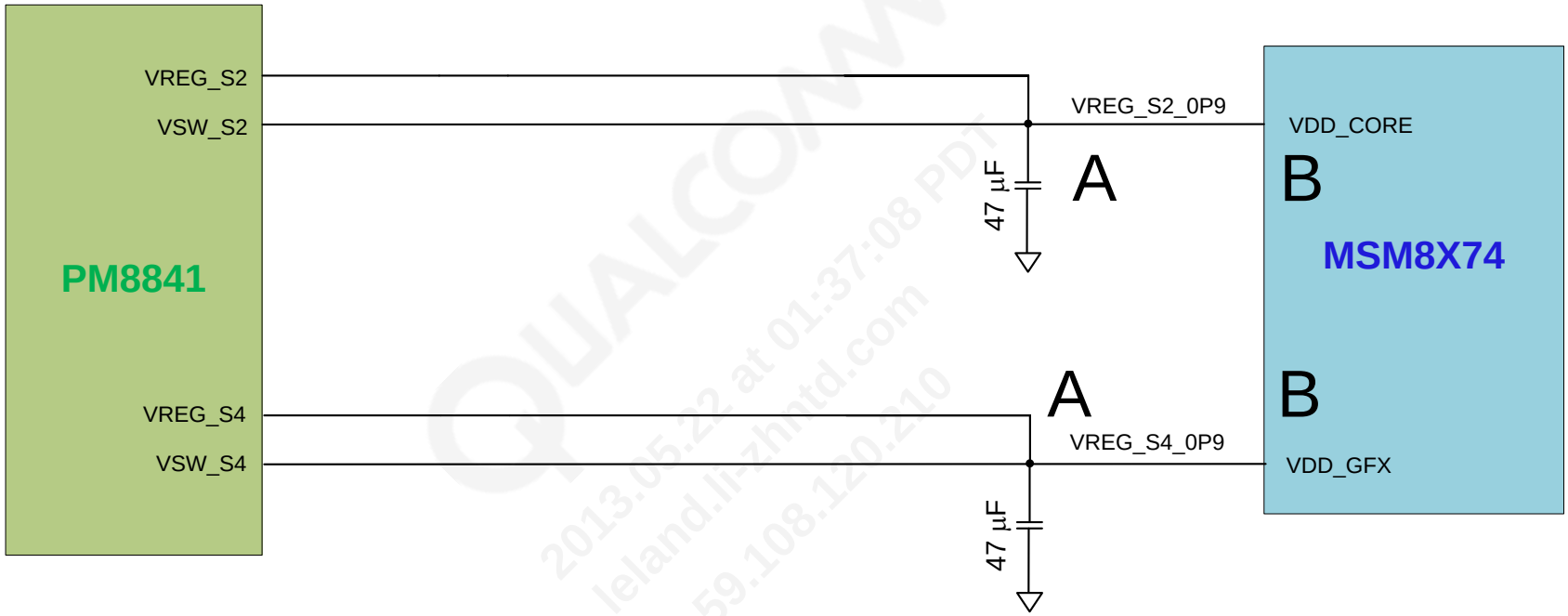
Power Routing – VDD_KRAIT Power Supplies



Note: Connect VREG_S5B, S6B, S7B, S8B to VREG_KRAIT_0P9 at same point close to the MSM device

- The feedback pins for S5b-S8b should be shorted together (point A) close to the PMIC side and routed to a center point in the VDD_KRAIT area fill close to the MSM side.
- The REMOTE_GND_SNS pin of the PMIC should be routed to a center point in the GND area fill or plane close to the MSM side.
- The 2 mΩ PDN spec for VDD_KRAIT is from point B to C.

VDD_CORE and VDD_GFX Routing for MSM8974



- The 10 mΩ PDN specification for VDD_CORE/VDD_GFX is from point A to B.
- The bulk capacitors for VREG_S2 and VREG_S4 should be placed close to the MSM.

Power Distribution – Power Traces Not Covered Under PDN Requirements

- Determine the minimum trace width for DC distribution using the following:

1. Find the maximum current (I_{MAX}) conducted by the trace – the sum of maximum currents expected for all its loads.
2. Define the regulator's operating output voltage (V_{REG}).
3. Calculate the maximum tolerable trace resistance (R_{MAX}) assuming a 1% IR drop:

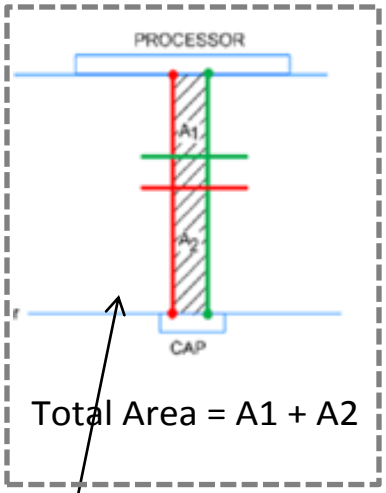
   $$R_{MAX} = 0.01 \times V_{REG} / I_{MAX}$$

4. Estimate total trace length (L) based upon the preliminary layout.
5. Determine the copper thickness (T): 1 ounce copper foil thickness is 1.34 mil – scale as needed for thicknesses other than 1 ounce.
6. Calculate the minimum trace width (W_{MIN}) allowed.

   $W_{MIN} = \rho \times L / (R_{MAX} \times T)$ where ρ = copper resistivity (1.7×10^{-8} Ω-m)

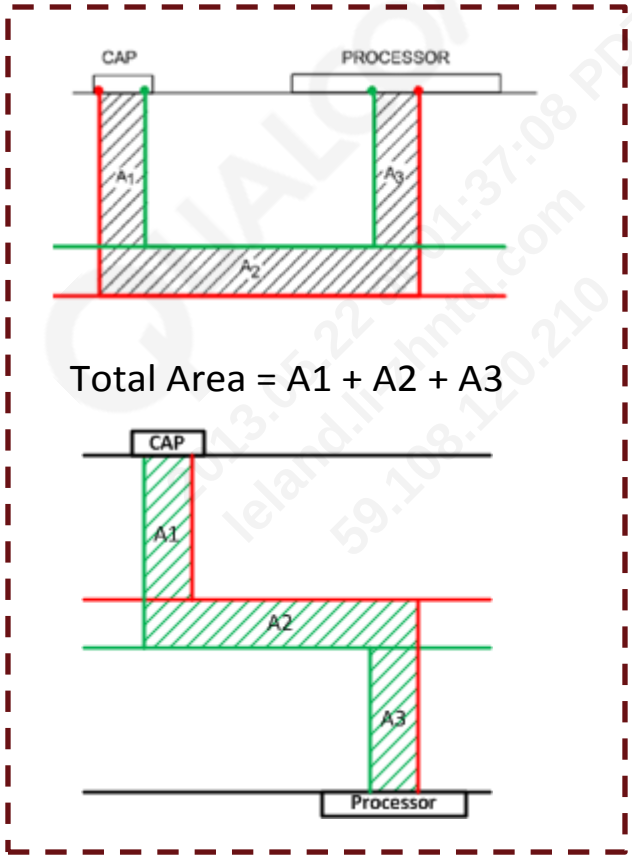
Capacitor Placements

- Lower power-ground loop area reduces loop inductance thereby improving the effectiveness of a capacitor at high frequencies.
- Local decoupling capacitors must be placed as close to the MSM pins as possible.

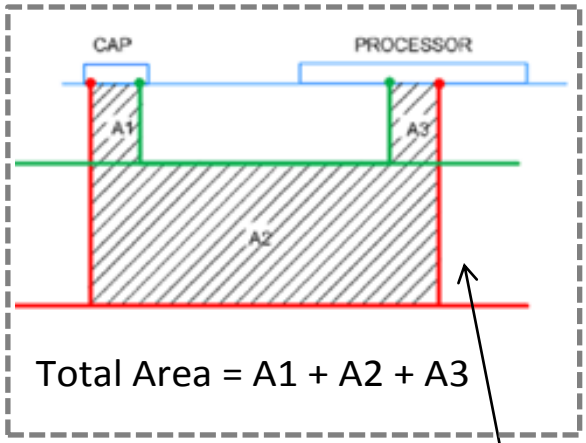


A

Least inductance



B



C

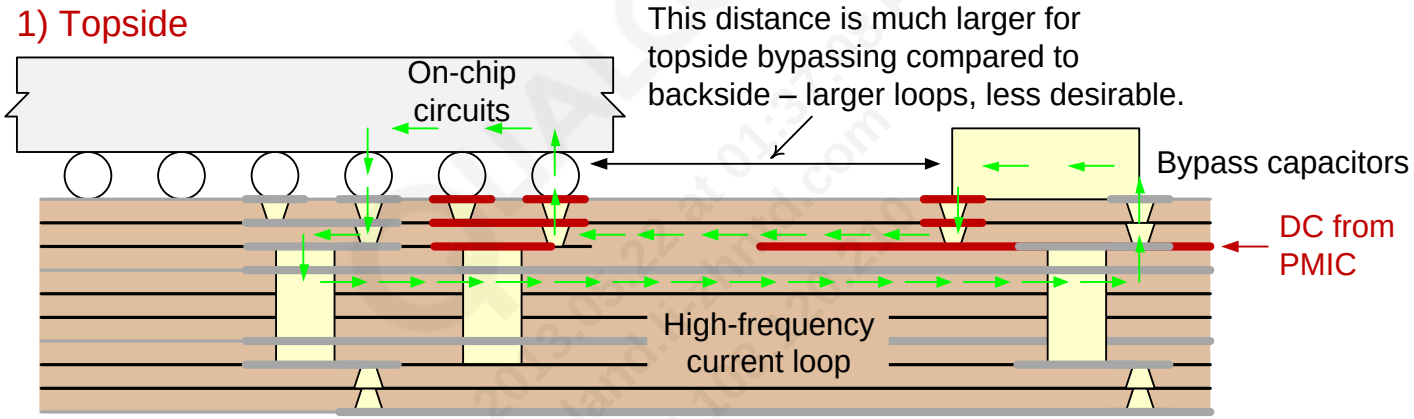
Largest inductance

Note: Geometries are not to scale.

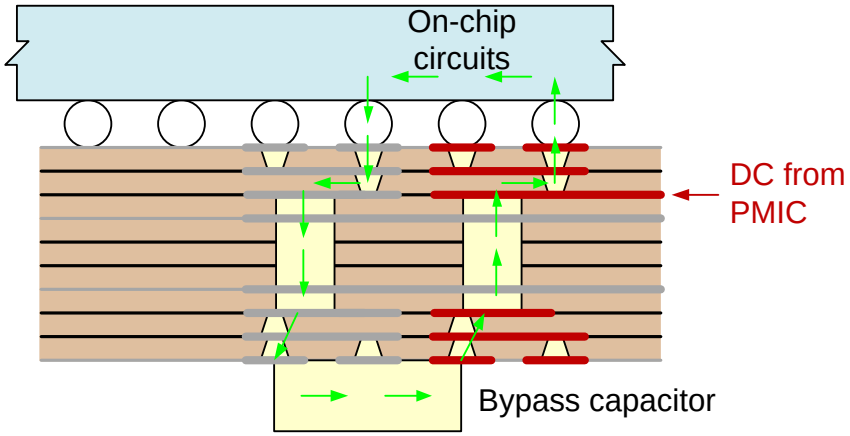
Topside Versus Backside Bypass Capacitors

- Bypass capacitors can be located on the same side as the MSM (topside) or on the opposite side (backside).
- Both are supported by the MSM IC.
- Backside is better, as illustrated, and easier to implement.
- Design examples are shown using topside (the more difficult routing).

1) Topside



2) Backside – smaller loop



Power

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MSM8974 Power Architecture Concepts

(Note: The block diagram is an abstracted representation to show power features only and may not represent the actual chip)

Low Power System and SoC techniques across the chipset:

- Activity driven clock gating
- DDR controller auto-self-refresh entry/exit
- PMIC auto switching between modes for better efficiency
- Distributed, fine grain energy management in HW
- Collapsible XPUs
- Optimized timeline operations including WAN standby, WLAN/BT Power
- Low leakage, voltage retention mode, with efficient switching in and out of retention

Improved Active power from 28HPm technology

Multiple voltage domains: CPU core0/1/2/3, GRP, modem, digital, memory

Collapsible logic domains & memories

Voltage scaling

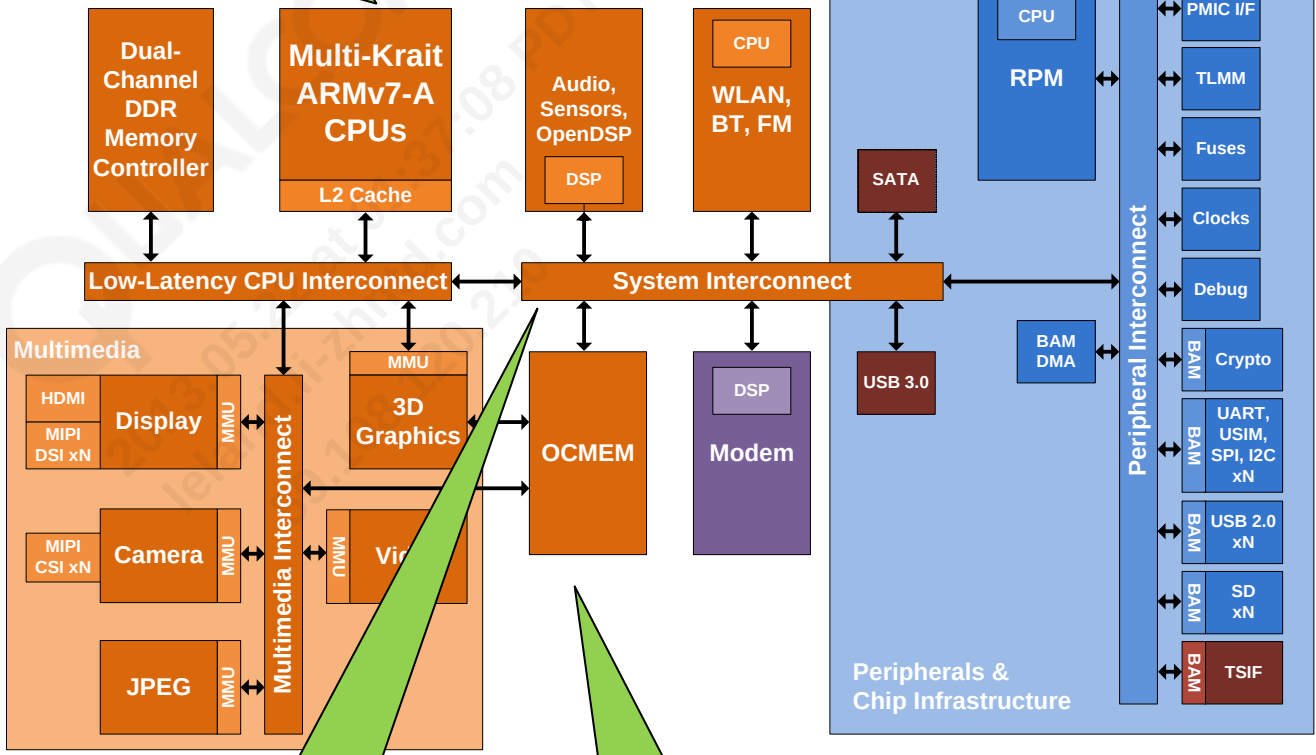
-Each CPU core scales in fine voltage steps

-Other core support Turbo, nominal, low and retention voltage levels.

Deep sleep modes to save leakage

-Low power/high performance proprietary design
-Improved/faster CPU power collapse
-Asynchronous clock frequencies for cores and L2

Coarse grain, use-case level energy management using RPM, with HW Acceleration for Resource control



Enhanced QoS based Interconnect for better performance and power

OCMEM to reduce traffic to external memory

Key Enhancements

Category	MSM8960	MSM8974
Resource management	Shared resource energy management using RPM (64 MHz ARM7), with HW acceleration for resource control	- RPM processor upgraded to 170/100 MHz Cortex M3, PMIC SPMI Interface - Changes to RPM-Core processor communication for improved timeline operations
Clocking	Split clocking (CXO+PXO)	Single Crystal CXO
Voltage rails	Split-Rail Cx/Mx, Q6 rails	Split-rail Cx/Mx, separate rails for MSS (Modem Subsystem), graphics
Multi-Krait	Individual switcher control	Unified PDN driven by multi-phase switchers, with eLDO for asymmetric operation
DCVS	Multi-processor-DCVS, GPU-DCVS	+ Bus-DCVS
OCMEM	-	Shared OCMEM for graphics, audio, sensors
Subsystem power managers	Gen 1 SAW (SPM AVS Wrapper), SPM (Subsystem Power Manager)	Enhanced for Quad-Kraits, connectivity, modem
Power grid	Auto-PFM operation of SMPS for improved efficiency at low-loads	Auto-mode applied to RF loads with sub-regulation (*) and isolation of WAN/LAN
Topology	Modem integration through Sys-NOC	Direct low-latency BIMC port for modem Q6

- Other changes
  - Sensors from ARM7 to LPASS
  - New Infrastructure blocks: DDR controller (BIMC) and interconnects (NOCs)

Enhancements for Low Power Integration

Category	MSM8974
WLAN DTIM	- Increase in WCSS (Wireless Connectivity Sub-system) Internal memory (cMem) to allow all-local execution for WLAN-DTIM - SPM enhancements to increase SW offloading Overall, timeline reduction from 10+ ms down to ~6 ms, bringing down WLAN DTIM adder from 2+ mA to ~1.6 mA
WAN standby	MSM8974 platform enhancements, along with WAN improvements demonstrate potential to get standby numbers near best-in-class
WAN+ connectivity concurrency	Sub-regulated WAN+LAN RF loads allowing reduced power adder with Voice-call + BT LPPS, WLAN DTIM

Note: DTIM means Delivery Traffic Indication Message and LPPS means Low Power Page Scan.

MSM8974 Power Features

Feature name	HW/SW	Feature description
Autonomous End-to-End QoS	HW/SW	Multi-priority, weight-based QoS and arbitration. Consistent solution through busses and memory controller.
Collapsible XPU and new MMU	SW	XPUs are collasible as part of VBIF for each MM (Multimedia) cores. System MMU for MM cores on 4 KB page boundary eliminate need for contiguous memory allocation (PMEM), reducing external memory copy operations.
OCMEM	HW/SW	Shared on-chip SRAM improves performance and power by reducing DRAM bandwidth.
MP-DCVS + GPU-DCVS	SW	Independent control of each CPU's and GPU voltage and MHz to optimize power and latencies.
Coarse grain freq scaling	SW	Adjusting the frequency of cores and infrastructure at the start of a use-case to save power.
SVS	HW/SW	Static voltage scaling of digital and memory rails.
System-DCVS	HW/SW	Bus frequency and voltage scaling.
Fine grain HW clock gating	HW	Helps reduce power by quickly turning clocks on and off based on activity without SW involvement.
DDR activity based auto self-refresh entry and exit	HW	Helps reduce power by putting DDR in self-refresh automatically when idle and improves transient response by bringing it out of self-refresh on activity, all without SW involvement.
Dynamic Memory Management (DMM)	SW	SW feature to move in-use memory to lower/contiguous region, to collapse other un-used resgion(s) or for single channel DDR operation.
PMIC auto mode switching	HW	Automatically switch mode between PFM, PWM and PS to save power.
Multiple voltage/power domains	HW/SW	Multiple voltage and power domains for independent voltage scaling and power collapse.
Split logic and memory rails	HW/SW	Separate voltage rails and regulators for logic and internal memories, allows lowering logic voltage while retaining the contents or collapse logic rail while retaining internal memories.
Dedicated PLLs	HW/SW	Dedicated PLL for each subsystem reduces inter-dependencies and allows each subsystem to achieve lowest power by lowering its MHz without affecting the performance of other subsystems.
VDD minimization	SW	VDD minimization for power saving.
Collapsible logic/memories	SW	Individually collapse internal memory blocks and architect additional collapsible domains.
Memory Controller (BIMC) power collapse	HW/SW	BIMC can be power collapsed to save leakage.
Modem power collapse	HW/SW	Modem + mDSP are all on a separate rail. The only way to collapse is by collapsing the rail.
SAW	HW	APSS and Q6SS have SAW to assist CPU power management.
Shared PLL HW managed on/off	HW	HW managed on/off based on executing environment votes.
Collapsible analog cores	HW/SW	Individually collapse unused analog cores (PHYs, DACs, ADCs, PLLs, Sensors).
XO shutdown	SW	All collapsible cores collapsed, VDD_DIG and VDD_MEM in retention; all other rails collapsed
PMDVS	HW	Process monitors based DVS: Scale voltage based on device characterization.
AVS	HW	Adaptive voltage scaling for power saving.

Technology | Dynamic pwr | Standby pwr | Archictecture

Supported previously; Enhancement; New

MSM8974 Power – Highlights (Projection based)

- Significant (~10-15%) improvements in modem active power use-cases
  - Digital-modem reductions
- Significant (~10-20%) improvements in multimedia graphics and video power use-cases
  - Digital video and graphics core power improvements
- Low power use-cases – process leakage increases mitigated through design changes

MSM8974 Chipset Power Targets

User cases	MSM8974 WTR1605 2x512MB LPDDR3 720HD DSI (1280x768)	MSM8960 WTR1605 2x512MB LPDDR2 WSVGA DSI (1024x600)
Rock bottom sleep	1.9	1.8
WCDMA Standby 2.56 s	2.2	2.6
WCDMA Talk +0 dBm, IMT	103	109
CDMA QPCH 5.12 s	2.4	2.4
CDMA Talk +0 dBm, CEL	112	115
GSM Standby 1.18s	2.5	2.7
GSM Talk 5 dBm, no DTX, PGSM	69	70
HSDPA DL 7.2 Mbps +0dBm, IMT (RxD/No RxD)	158/141	158
HSDPA DC 42 Mbps +0dBm, IMT (RxD/No RxD)	210/190	213
LTE Standby 2.56s	2.5	2.8
LTE Cat 3 (68/23 Mbps, +0 dbm, B13)	290	338
EVDO DL 3.1 Mbps +0 dBm	159	165
SVLTE Cat2 (50 Mbps, +0 dBm, B13) & 1x Voice	350	375
GPS 1Hz Trk (DPO)	10	12.2
GNSS 1Hz Trk	38	40
MP3 playback 128kbps – TM	16	18
H.264 720p decode, 30 fps	91	109
H.264 30 fps 1080P, 20 Mbps, decode	127	162
H.264 30 fps 1080P, 20 Mbps, encode	189	194
3D UI 30 fps (Graphic, power lift)	137	118
Static Image	38	33
BT SNIFF/Scan on W standby	2.75	3.3
WLAN DTIM1 on W standby	3.8	4.5

Target: mA@Battery - 3.7 V, 25°C, typical process

Thermal Design Considerations

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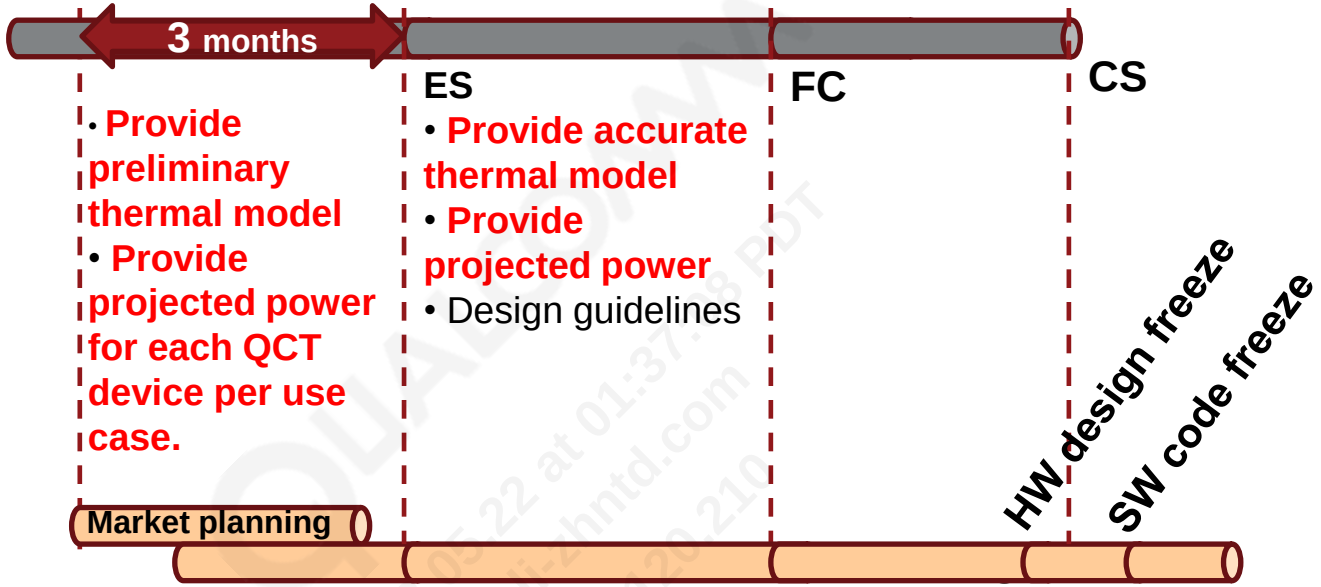
Agenda

- Introduction
- MSM8974 Thermal Topics
  - General key message
  - Thermal design milestone and typical chipset product development timeline
  - **Mobile Devices Thermal Design – Where to Start?**
  - MSM8x74 chipset packages thermal models
  - What to do with the thermal models?
  - Thermal simulation:
    - Packages thermal modeling and simulation
    - System thermal modeling and simulation
    - Transient vs. steady state thermal analysis
- Projected power dissipation – Thermal Design Power – TDP for MSM8x74 chipsets
- Thermal design considerations
- SW thermal mitigation
  - Definition and goals
    - Thermal testing – stress tests for mobile devices
  - Testing and bring up with and with SW thermal mitigation

Introduction: What are MSM8x74 chipsets?

- MSM8x74 chipsets consist of the following supporting chips:
  - MSM8x74 (LPDDR3 POP, Quad Krait CPU cores)
  - PMICs: PM8841; PM8941
  - QFE1100; QFE2320; QFE1510
  - WCD9320
  - WCN36x0
  - WTR1605L
- The targeted platforms are high performance and rich graphics mobile devices.
- Higher performance means increased demand on the chipsets and increased heat.
- Qualcomm **strongly** recommends that customers use these chipsets in their products to conduct thermal simulation for their overall systems under consideration.
- All packages thermal models are available in Icepak (filename.tzr - zipped form)- and in FloTHERM (prb.pdml). The thermal models can be found on CDMATech Documents and Downloads.
- All thermal models have material properties; thermal resistance can be extracted, and there are validation procedures for the thermal models.
- Qualcomm also provides documents summarizing projected thermal power dissipation for certain use-case scenarios.

Thermal Design Milestones



Preliminary design

- **Industrial design**
- **Mechanical design**
- **Thermal simulation**
- Proto-PCB design

Initial HW/SW bring-up

- Verification of basic functions
- Troubleshooting
- **Thermal simulation using thermal models**
- **Thermal testing/verification with available user cases**

Product qualification

- HW design spins if necessarily
- **Power optimization**
- **Thermal verification**
- Qualification for ramping up to markets
- Hardening mechanical tooling

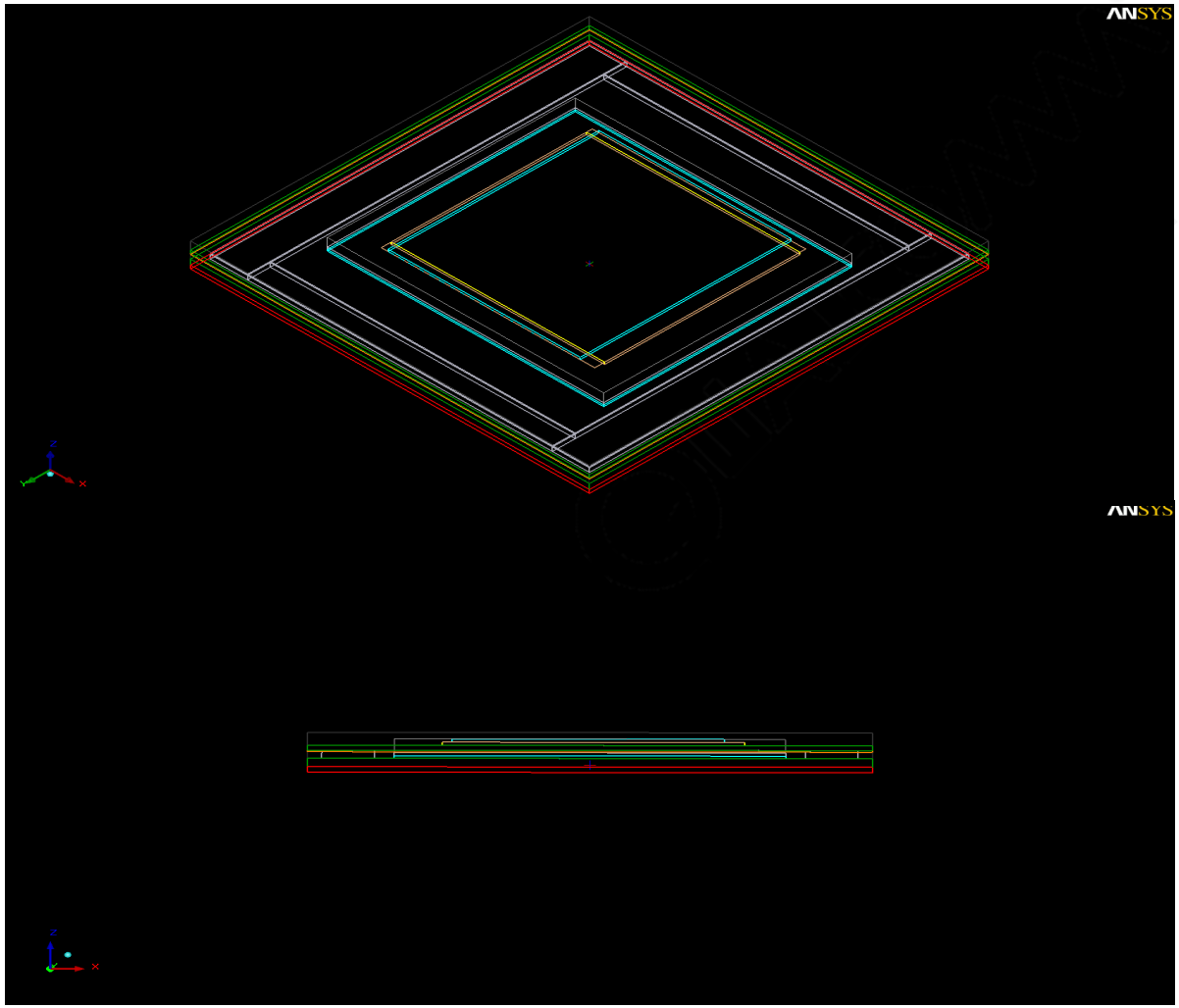
MSM8974 Chipset Package Thermal Models

- Icepak models
  - WCN3680 ICEPAK THERMAL PACKAGE MODEL (HS11-WL005-5HW)
  - WCD9320 84WLNSP ICEPAK THERMAL PACKAGE MODEL (HS11-NA556-5HW)
  - QFE1100 28WLNSP ICEPAK THERMAL PACKAGE MODEL (HS11-NA681-5HW)
  - QCA1990 30WLNSP ICEPAK THERMAL PACKAGE MODEL (HS11-NB792-5HW)
  - MSM8974 ICEPAK THERMAL PACKAGE MODEL (HS11-NA104-5HW)
  - PM8941 ICEPAK THERMAL PACKAGE MODEL (HS11-NA445-5HW)
  - PM8841 ICEPAK THERMAL PACKAGE MODEL (HS11-NA444-5HW)
  - WTR1605 ICEPAK THERMAL PACKAGE MODEL (HS11-NA446-5HW)
- FloTHERM models
  - WCN3680 FLOTHERM THERMAL PACKAGE MODEL (HS11-WL005-6HW)
  - WCD9320 84WLNSP FLOTHERM THERMAL PACKAGE MODEL (HS11-NA556-6HW)
  - QFE1100 28WLNSP FLOTHERM THERMAL PACKAGE MODEL (HS11-NA681-6HW)
  - QCA1990 30WLNSP FLOTHERM THERMAL PACKAGE MODEL (HS11-NB792-6HW)
  - MSM8974 FLOTHERM THERMAL PACKAGE MODEL (HS11-NA437-6HW)
  - PM8941 FLOTHERM THERMAL PACKAGE MODEL (HS11-NA555-6HW)
  - PM8841 FLOTHERM THERMAL PACKAGE MODEL (HS11-NA554-6HW)
  - WTR1605 FLOTHERM THERMAL PACKAGE MODEL (HS11-NA446-6HW)

What to do with the Package Thermal Models from Qualcomm?

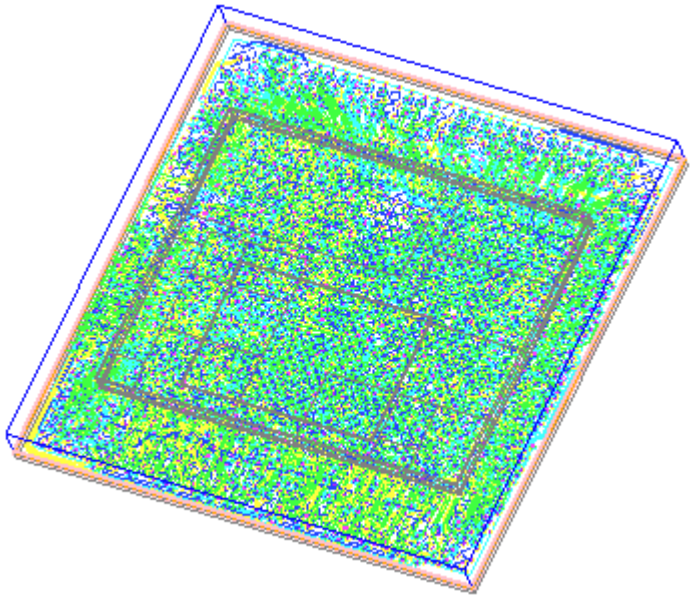
- Package thermal models provide:
  - Chipset components' overall packages form factor (dimensions)
  - Package thermal characteristics and physical properties
  - Information about how to obtain thermal resistance values
  - Validation with JEDEC standards that can be used to scale customer's PCB thermal performance. Use such information for specific PCB designs
- Performing overall system thermal simulation:
  - Customers can download thermal models without recreating such models from scratch
  - Uploading the packages thermal models into customers without re-meshing misalignment with the overall system thermal model
  - Customers are assured that these thermal models have been validated for power and temperature limits in standard operating environment in standalone as well as in reference enclosure modes
  - These models were created by professionals from the source with all pertinent information that customers will need to create their own overall enclosure form factor thermal model and drop in these packages thermal models based on their layout requirements
  - This represents tremendous time and resources savings for customers when performing a complex and successful thermal simulation.

Thermal Simulation – Building Blocks (Components Packages)



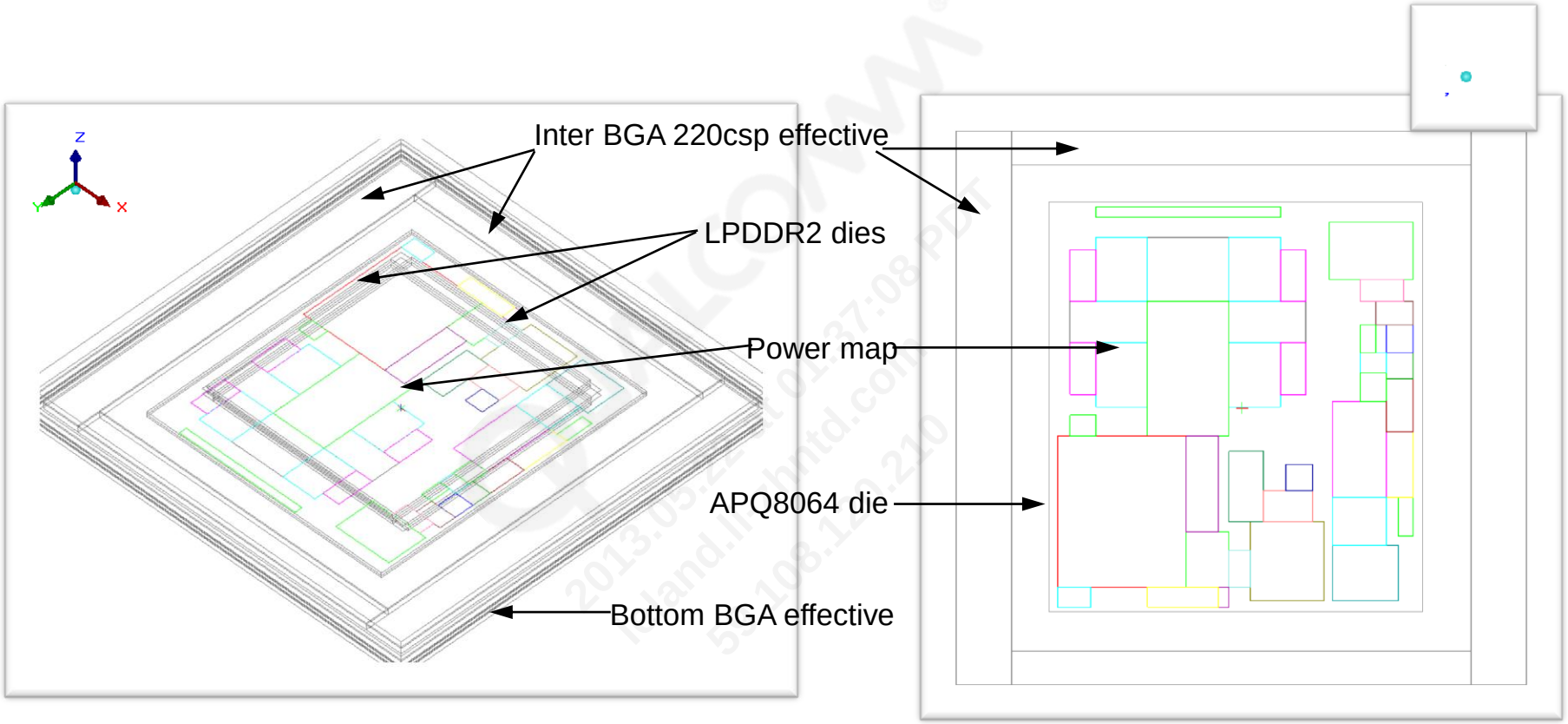
Package thermal model ISO and cross-sectional views

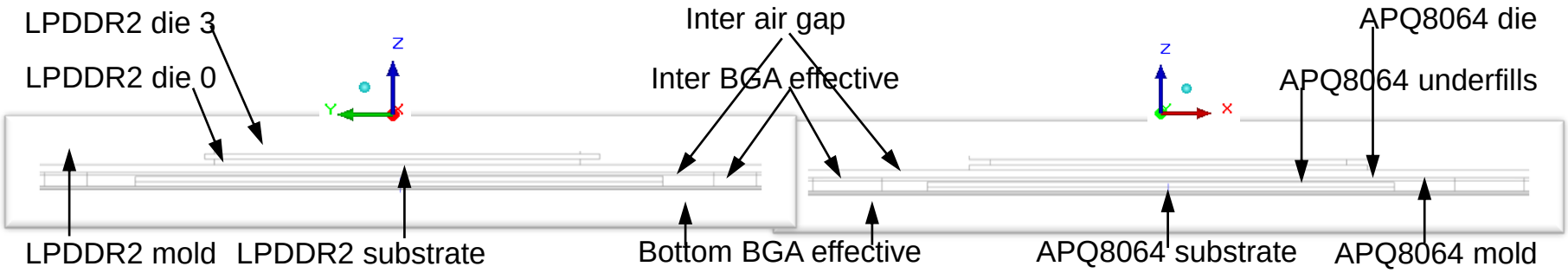
- Qualcomm provides package models for OEM customers
- Package thermal models are thoroughly validated.
- Models are picked and dropped in the overall system thermal model.
- Thermal properties are included in the thermal.



Meshed package model for validation

An Example: APQ8064-839NSP – Package Thermal Model



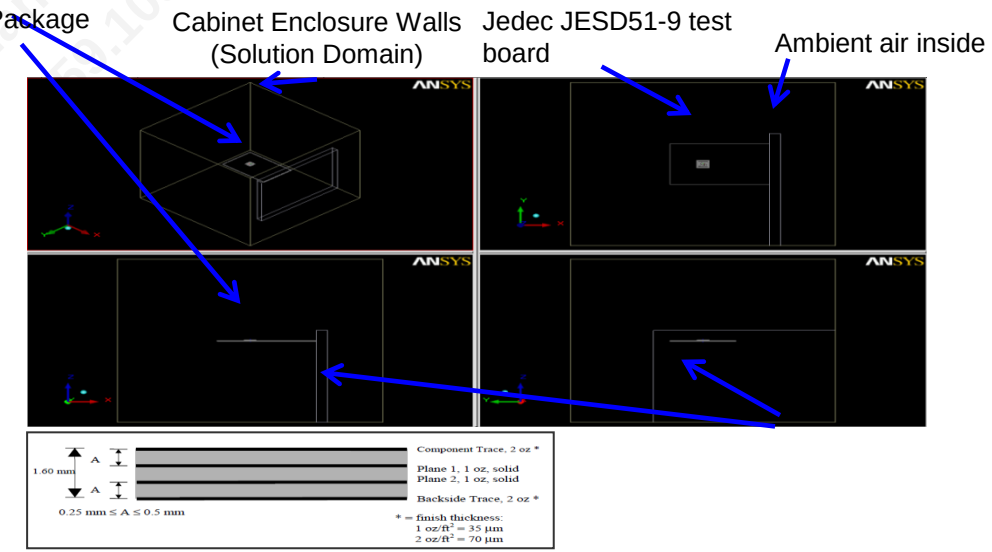


Package Thermal Characteristics – Thermal Resistance Values for Packages

- Tool: ANSYS Icepak 13.0
- Solution domain
  - Jedec JESD51-2A enclosure
    - 304 x 304 x 304 mm
    - Wall objects with zero thickness
  - Jedec JESD51-9 test board
    - 114 x 76 x 1.6 mm
    - 4-layer, 1s2p (no thermal vias)
    - 2-1-1 Cu stackup (70u-35u-35u)
    - FR-4 dielectric
    - Top trace, K = 194 W/mK
    - Metal layers 2=3, K= 387 W/mK
- Analysis type
  - Steady-state conjugate heat transfer
  - Natural convection air flow
- Boundary conditions
  - Heat trans coeff. applied to each cabinet wall
    - Heat Tr. Coeff. = 5.0 W/m^2-K
  - Radiation
    - Surface-to-surface radiation model
    - Far-field temperature reference
    - Package mold and test board only
  - Ambient air temperature = 70ºC
- Mesh parameters
  - Hexa unstructured
  - 622,232 elements /681,149 nodes
- Numerical precision = Double

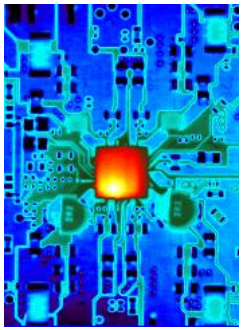
Component	Projected theoretical (through analysis) thermal resistance		Maximum junction temperature
	Θ_{ja} (C/W)	Θ_{jc} (C/W)	Degree C
MSM8x74	~22 C/W	~6 C/W	105; 85Tc
PM8841	~24 C/W	~5 C/W	Refer to device specs
PM8941	~24 C/W	~5 C/W	Refer to device specs
WTR1605L	~20 C/W	~4 C/W	105
WCN3660/80	~21 C/W	~6 C/W	105
QFE1100	~22 C/W	~4 C/W	105
QCA1990	~21 C/W	~5 C/W	105
WCD9320	~22 C/W	~6 C/W	105

Note: All packages thermal data were derived with simulation methods.

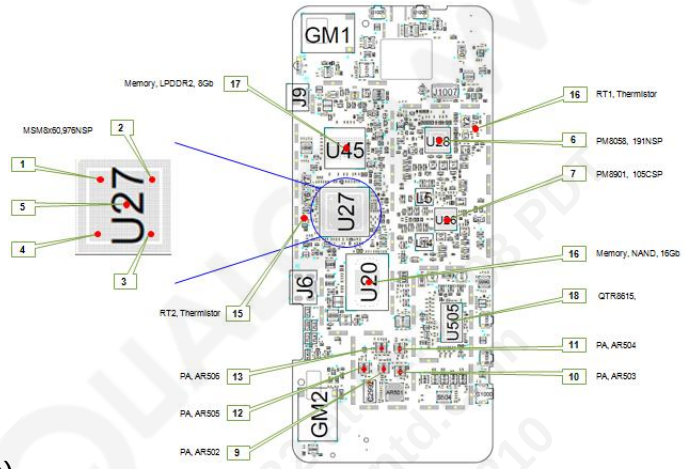


Overall System Thermal Simulation: An Example – FLUID Platform

Concurrency Power

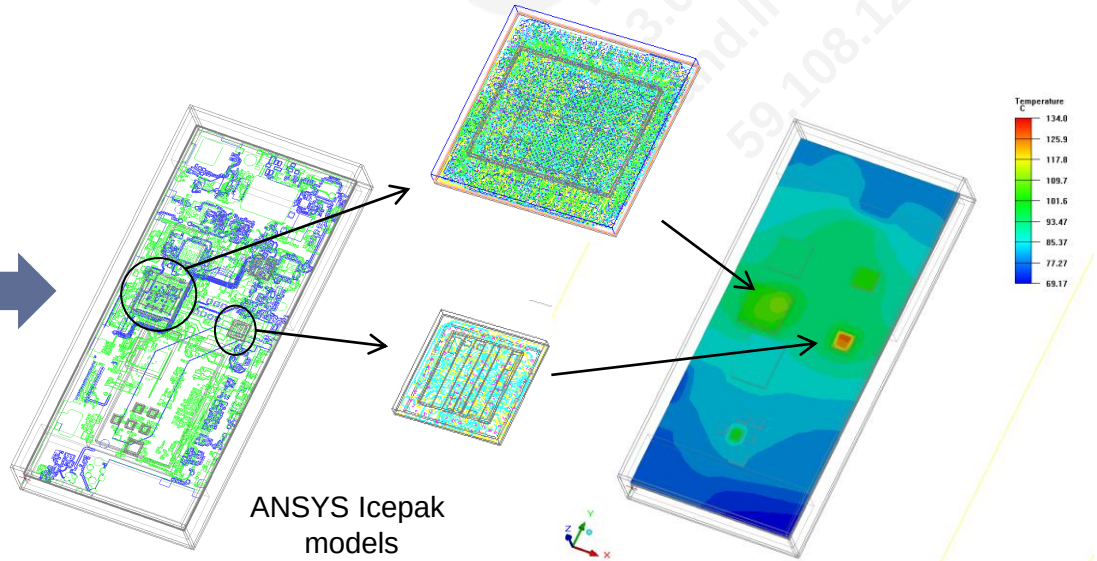


Infrared imaging
(FLIR SC4000 scientific camera)



Empirical data

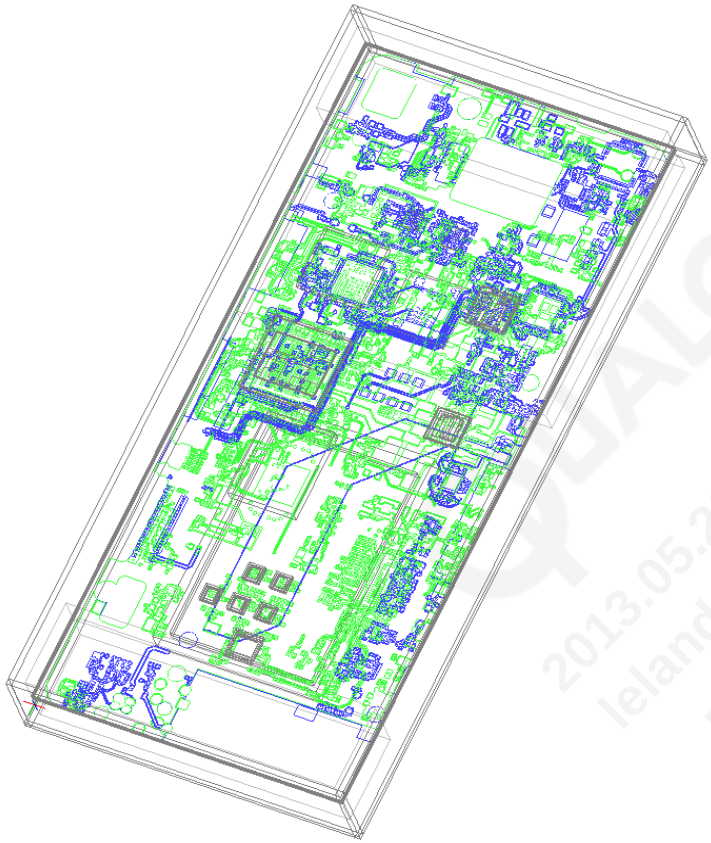
Benchmarking

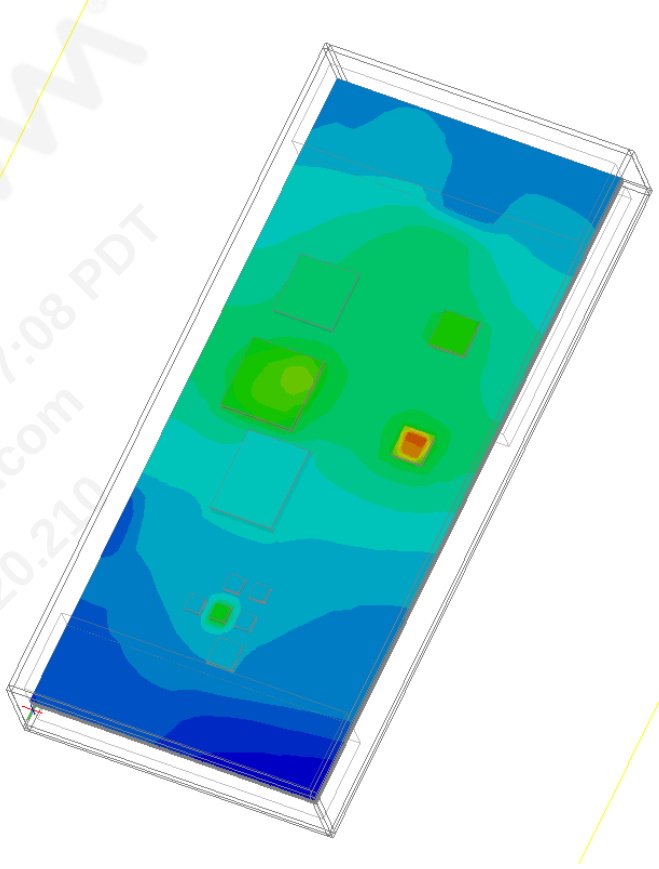


ANSYS Icepak
models

Thermal design kit

Overall System Thermal Simulation Output (Temperature Contours)





Overall system thermal model

Overall system thermal simulation results

- **What if scenarios (power use-cases)**
- **Evaluate device skin and internal temperatures**
- **Early thermal prediction**

Chipset Concurrency (Thermal) Power Breakout

Use-case (@ 25°C unless noted)	Unit: mΩ						
	MSM8974	POP -LPDDR3	WTR1605	PA1	WCD9320	PM8941 + PM8841	Total
Camcorder video encode (H.264, 1080 p, 30 fps)	339	167	0	0	7	185	698
WCDMA voice call (24 dBm, -90 dBm Rx)	78	20	192	1702**	7	91	2090
LTE data call (cat3, 68 DL and 23 UL, B13, Tx: 0 dBm; Rx:-50 dBm)	507	82	245	24	0	209	1067
GFX intensive (Egypt 3D graphics, 60 fps)	750	384	0	0	0	327	1461
CPU intensive (Quad-Dhrystone, 2 GHz)	3100	20	0	0	0	550	3670

NOTES

1. This is a thermal power projection to be used for performing thermal analysis and simulation.
2. This thermal power projection is not intended to be used for PDN or power-budgeting purposes.
3. PA thermal power = PA input power - PA output power (~Tx power).
4. System key configuration: Android phone (2 GB LPDDR3, 1280 × 768 resolution, MIPI-DSI).
5. The PMIC and SMBC conversion efficiency varies depending on workload current (Multiphase buck ~81% efficiency).
6. The power numbers listed are unmitigated, and will be lowered via thermal mitigation routines when the thermal limits are reached.
7. The PA power used is in standard operation mode (not APT- or EPT-optimized).
8. LCD-related power is not included. The LCD power varies, depending on the choice of LCD model/resolution/brightness.
9. The SMBC output (battery charging) voltage varies, depending on the battery charge level. (3.0~4.2 V); this does not critically impact on SMBC efficiency.
10. ** Less 250 mΩ for thermal dissipation (radiated power); ~ 1 Ω on PA, rest on distribution (switchers, etc.).
11. All uses assume Ta = 25°C.

Note: This table contains preliminary information and is for illustration purposes only; an updated table will be available soon. The table was derived from *MSM8974 – Power Concurrency Values for Performing Device Thermal Analysis* (80-NA437-0 Rev. A)

Thermal Introduction and Reference Material

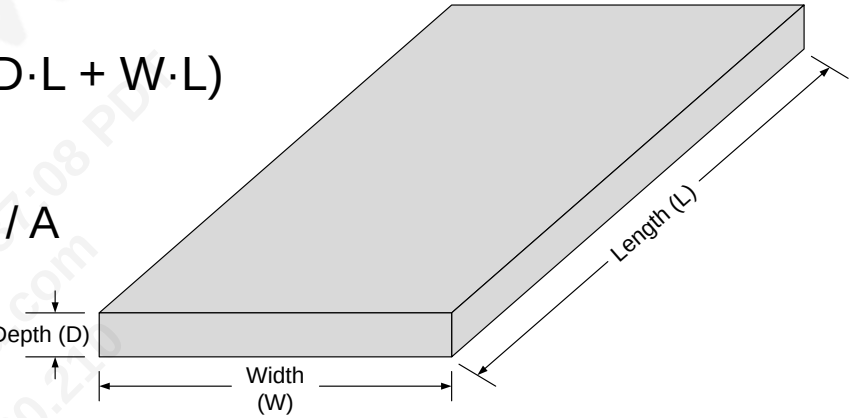
- Each generation of wireless handset devices adds more and more features, often into a smaller volume.
- Increasing power dissipation in small devices creates special mechanical/thermal design challenges.
- The thermal issues discussed on the following pages apply to all Qualcomm chipsets, regardless of the modem IC product-type (MSM, MDM, APQ, etc.).
- Each thermal issue needs to be evaluated at each stage of the development process.
  - Packaging and industrial design
  - Parts placements
  - PCB design — stack-up, via designs, ground planes, etc.
- In addition to the introductory presented on the following pages, download and study the related reference material:
  - *Thermal Design Considerations Application Note* (80-VU794-5)
  - *Thermal Protection Algorithm Overview* (80-VT344-1)
- Five thermal-related topics are discussed briefly within the following introduction:
  - Wireless product overall power density
  - PCB area
  - Distances between major heat sources
  - Package wall thickness and air flow
  - Heat conductivity below ICs

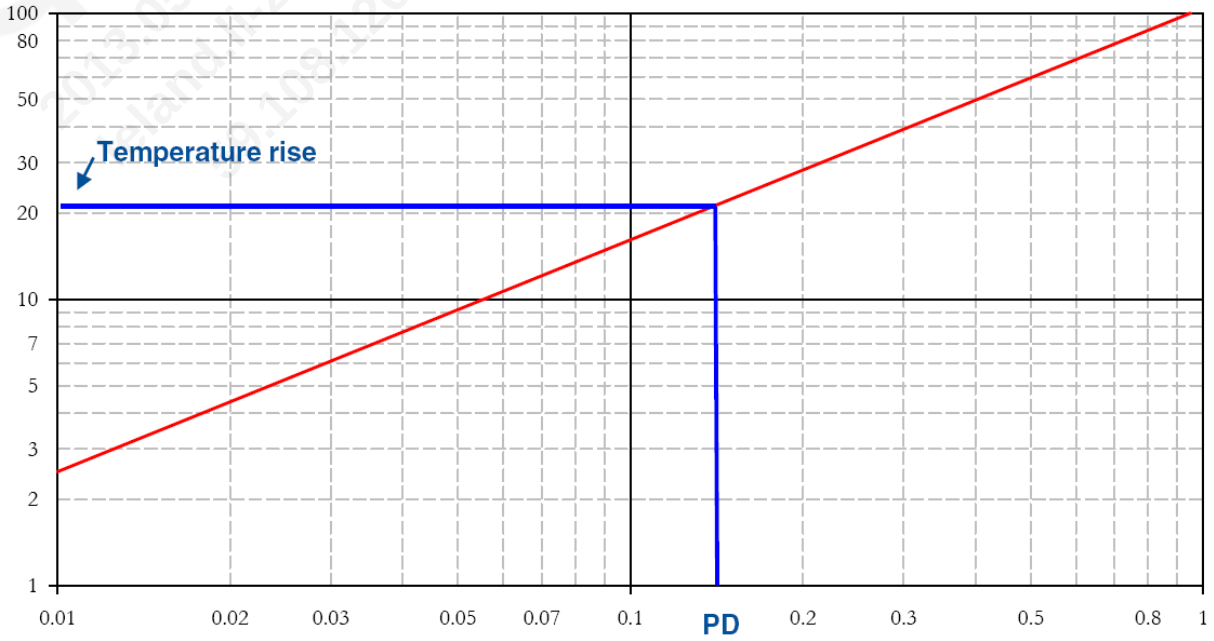
Wireless Product Overall Power Density

High power (or dissipation) in a small volume makes for a difficult thermal design.

A quick calculation and use of the plot at the lower right provides an estimate of a design's external surface temperature rise.

1. Calculate total surface area: $A = 2(D \cdot W + D \cdot L + W \cdot L)$
2. Calculate the total power dissipation (P)
3. Calculate the surface power density: PD = P / A
4. Estimate the temperature rise from the plot
   - In the example (blue lines)
     - PD ~ 1.5 W/in^2
     - ΔT ~ 21 °C

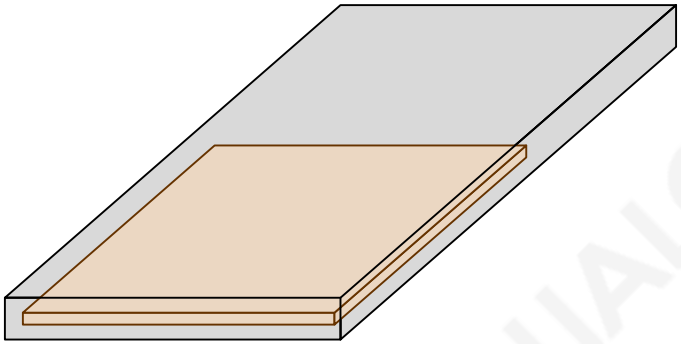


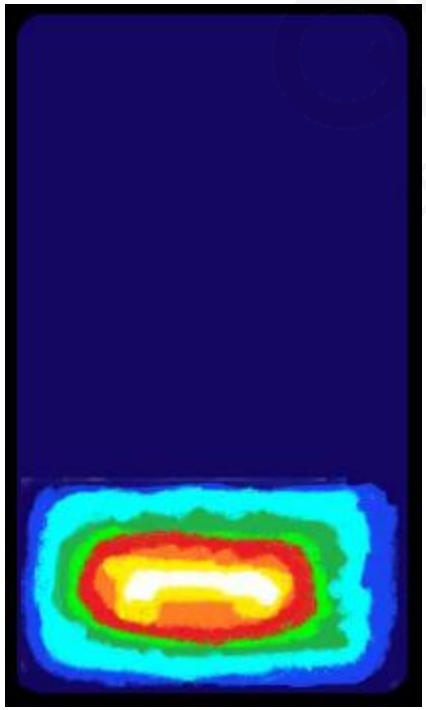


- See the *Thermal Design Considerations Application Note* (80-VU794-5) for additional details.

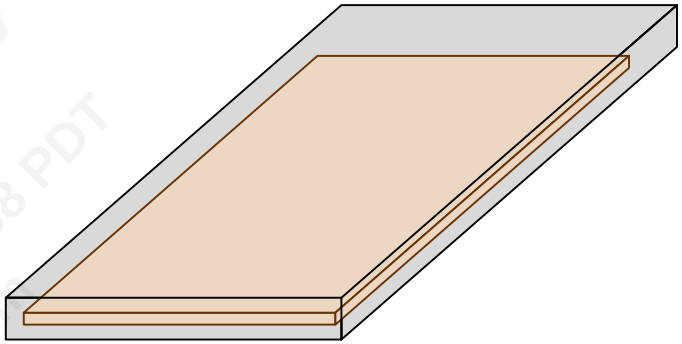
PCB Area and Heat Distribution

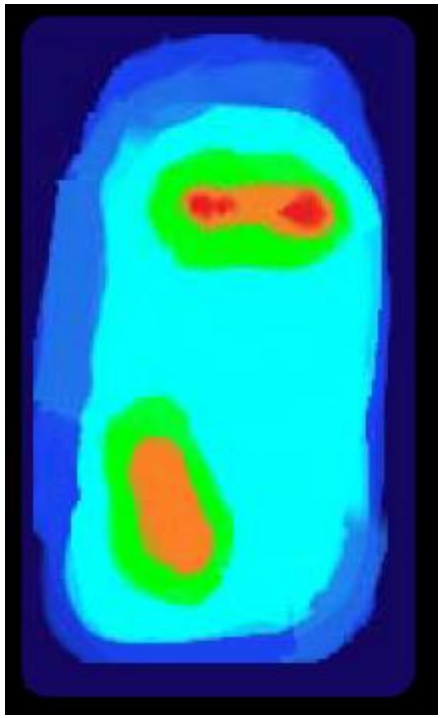
Spreading the heat across a large PCB surface area helps avoid hot spots within the handset.





Larger PCB area (and proper parts placements) results in better heat distribution.

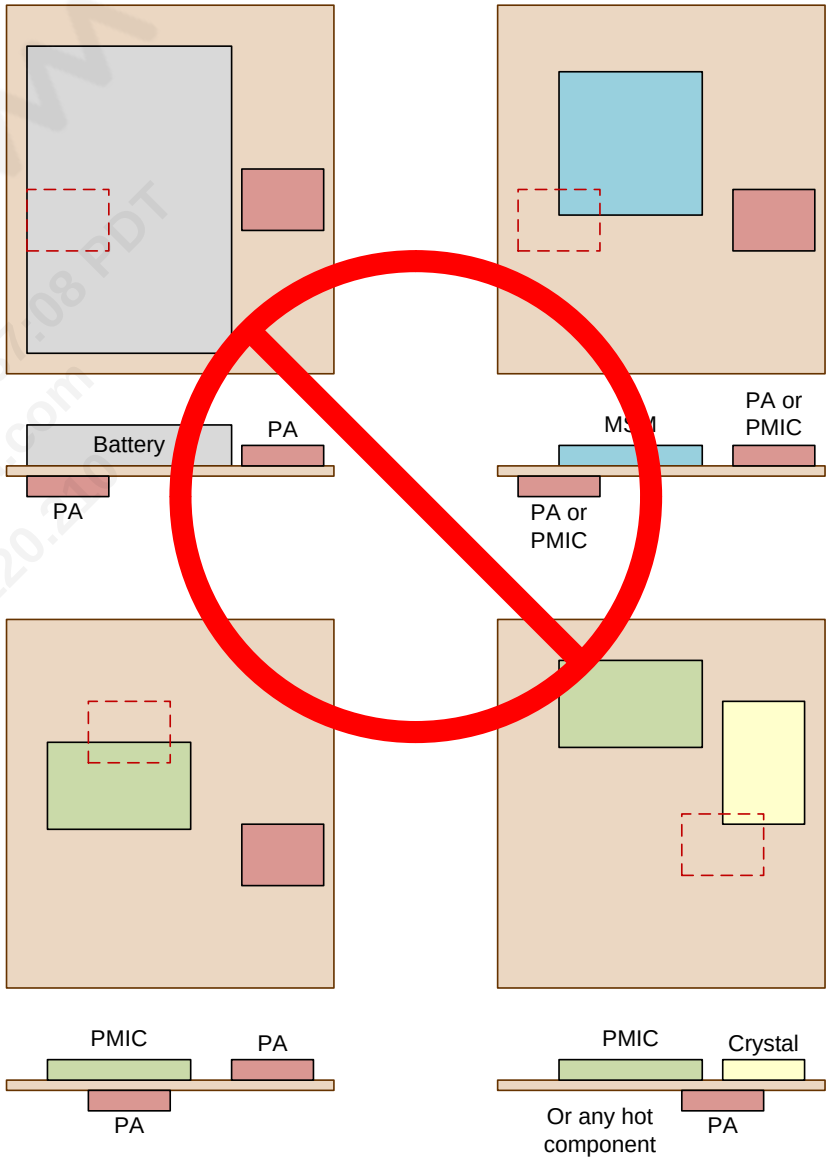




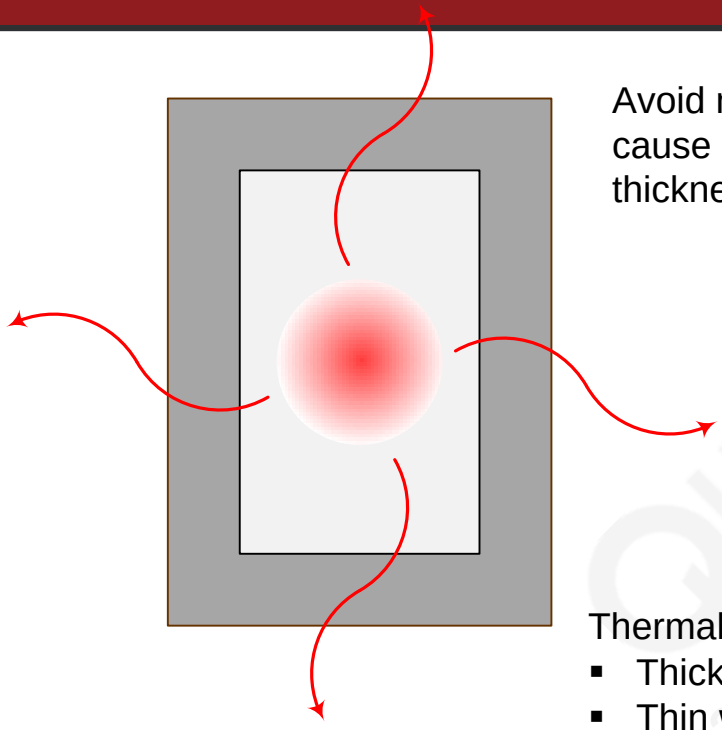
Distance Between Major Heat Source

Keep high power density parts away from each other – whether they are on the same side or opposite sides of the PCB.

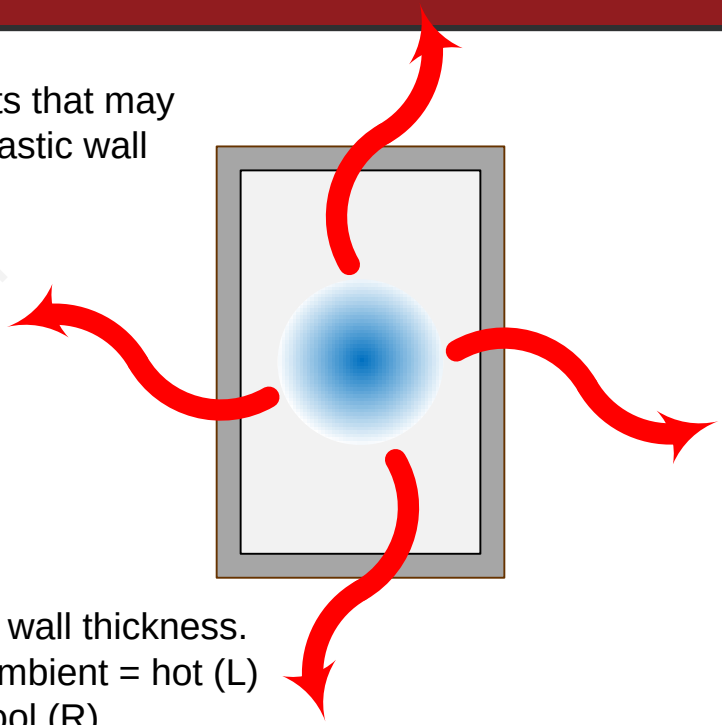
- Examples:
  - PA and other heat sources
  - Hot components and the battery
  - PMIC and modem IC
  - Oscillator crystals and heat sources that might cause harsh thermal gradients



Package Wall Thickness and Air Flow

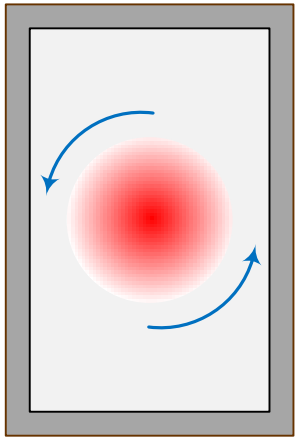


Avoid mechanical design constraints that may cause thermal issues – including plastic wall thickness and absence of air flow.



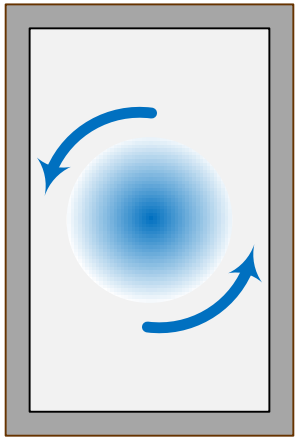
Thermal resistance is proportional to wall thickness.

- Thick walls = little conduction to ambient = hot (L)
- Thin walls = more conduction = cool (R)

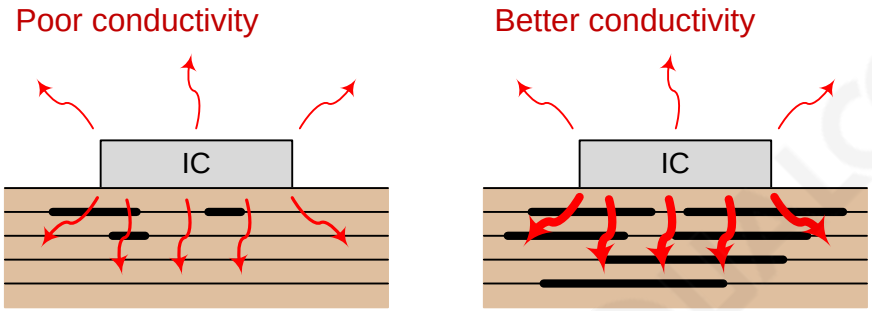


Air flow is very effective in reducing heat build-up.

- Little air flow (little convection) = hot (L)
- Adequate air flow = more convection = cool (R)



Heat Conductivity Below ICs

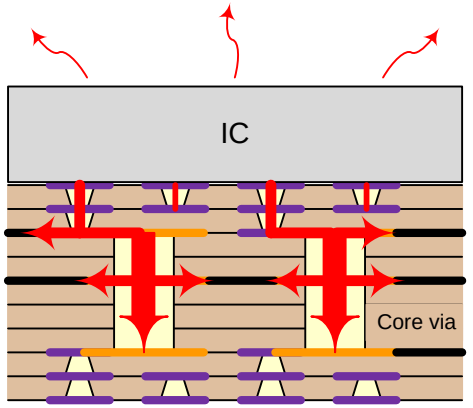


Include several layers with high copper density on each layer to increase thermal conductivity. Higher copper density provides better thermal relief and heat transfer.

- Do not rely on only air dissipation for RF power amplifiers; lots of copper is needed as a heat sink for these thermal loads.
- Fill empty board layers with copper wherever possible.
- It is very important that the heat source's mounting side is filled with copper.
- Use thick copper as much as possible; this is especially important for high current DC power supply distribution.

Include several vias under and around hot spots.

- Vias should go to large ground planes for better heat transfer.
- Via material is very important; solid copper is better than paste.
- Core vias are better than micro vias; stacked vias are better than staggered.
- Vias in the PA ground pad are very important; use as many as possible.



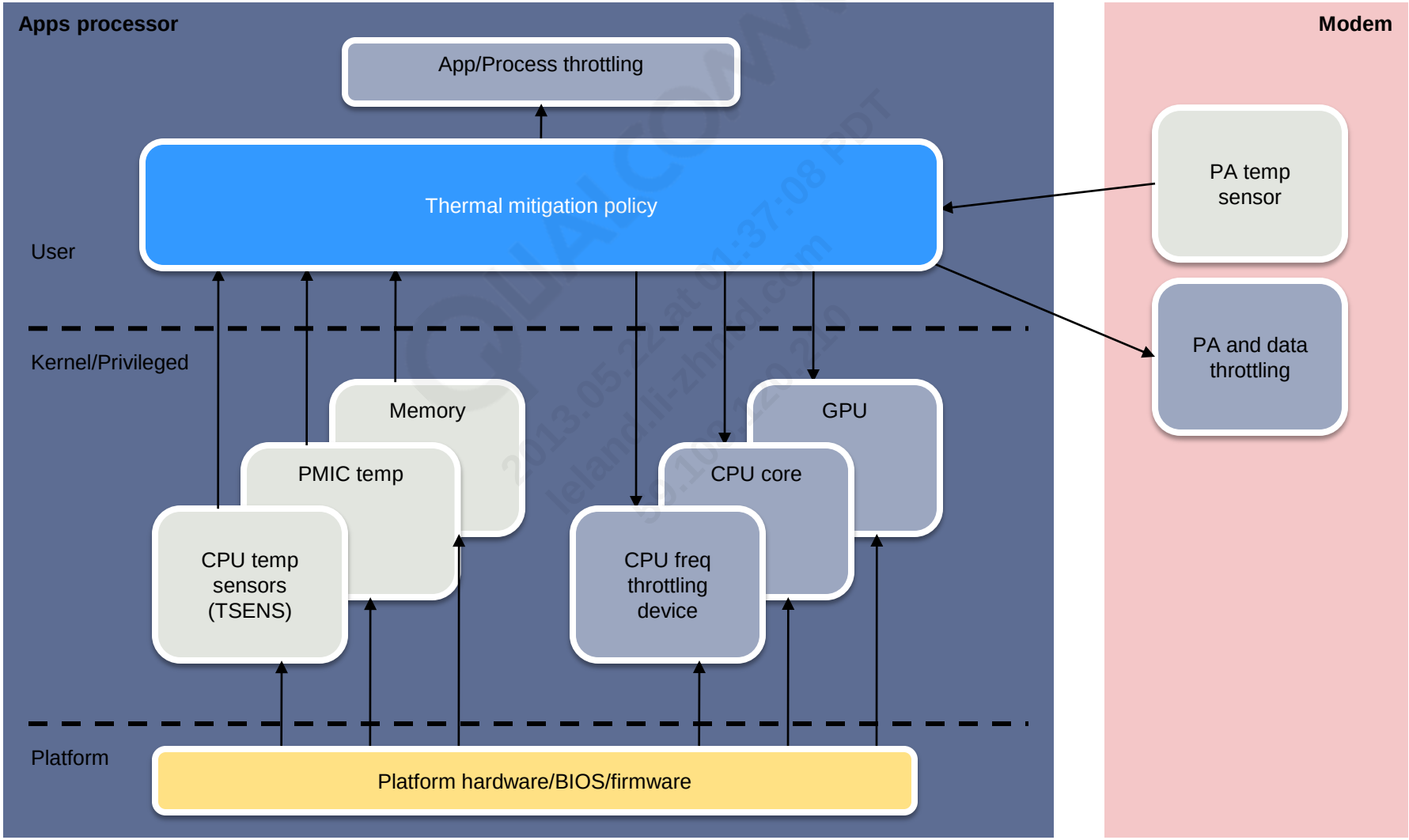
SW Thermal Mitigation (SW–TM)

- The MSM8x74 chipset family has thermal sensors on each chipset die.
- Thermal sensors detect maximum die active block temperature.
  - Sensors are calibrated and validated before releasing to customers.
  - Any correction factors will be implemented in the thermal mitigation SW.
- SW TM maintains the max die temperature at a preset value.
- SW-TM does not remove heat.
- If the die surpasses such preset value, the mobile device performance will be throttled.
  - The protocol of slowing or shutting down levels is predetermined based on the mobile device skin touch temperature requirements.
  - It is essential that customers download the latest thermal mitigation SW.
  - No boot up or testing should be tried without SW thermal mitigation.

Why Do We Need SW Thermal Mitigation Algorithms?

- The SW Thermal Mitigation Algorithm is targeted to:
  - Protect components from exceeding thermal design limits; if the limits are exceeded, the Quality of Service (QoS) can be degraded, and components can be damaged
  - Ensure compliance with external case and touch temperature requirements from customers, carriers, and standard organizations (underwriters laboratory, PCI express, and user expectations)
  - Minimize the risk of power-limit constraints
  - Manage the thermal risk and tradeoffs during concurrent operations
  - Allow limited customizable temperature thresholds and methods for power reduction
- Thermal Mitigation Algorithm (TMA) allows:
  - Protection against user harm or component damage for rare worst-case conditions
  - Controlling/reducing temperature by trading off device performance
- TMA does *not:*
  - Alter basic power efficiency or heat dissipation properties of the device
  - Change mechanics of the device
  - Fix the cause of heat
  - Remove heat

SW Thermal Management Architecture Overview for MSM Systems



HW Response: TM vs. Temperature Plot (Example)

- The MSM has three to eight software temperature threshold/mitigation levels and one high hardware shutdown limit.