Qualcomm
TECHNOLOGIES, INC

PM8941

Device Specification (Advance Information)

80-NA555-1 Rev. G

August 9, 2013

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Revision history

Bars appearing in the margin (as shown here) indicate where technical changes have occurred for this revision. The following table lists the technical content changes for all revisions.

Revision	Date	Description
A	April 2012	Initial release
B	June 2012	■ Updated Table 2-2 (Expected maximum currents at PI and PO pad types) ■ Added content to Chapter 3 through Chapter 7. Since this is all new material, change bars are not used to identify changes on any of these pages.
C	October 2012	■ Updated Figure 2-1 to correct pin name for pin 201. ■ Removed foot note from Table 2-1. ■ Update pin descriptions in Table 2-4, Table 2-5, Table 2-6 and Table 2-7. ■ Updated specifications in Table 3-1, Table 3-2, Table 3-5, Table 3-6, Table 3-7, Table 3-10, Table 3-11, Table 3-12,Table 3-13, Table 3-14, Table 3-15, Table 3-17, Table 3-20, Table 3-21, Table 3-22, Table 3-23, Table 3-24, Table 3-25, Table 3-27, Table 3-28, Table 3-31, Table 3-36, Table 3-37, Table 3-42, and Table 4-1 ■ Added battery FET and charge pump specifications in Table 3-8. ■ Added sleep clock jitter specifications in Table 3-30. ■ Added qualified coin cell / super cap specifications in Table 3-32. ■ Added RGB driver performance specifications in Table 3-33. ■ Added keypad backlight performance specifications in Table 3-34. ■ Added Flash LED driver performance specifications in Table 3-35. ■ Updated Figure 3-1, and Figure 4-2. ■ Updated pages 46 and 47

Revision	Date	Description
D	December 2012	■ Updated VCOIN maximum voltage in Table 3-2 ■ Updated VMAX value in Section 3.5.1 ■ Updated R(ovp_fet_on) typical resistance in Table 3-5 ■ Added Figure 3-2 Battery temperature monitoring ■ Added Table 3-16 BTM calculations ■ Updated minimum and maximum voltage for output voltage range in full specification compliance in Table 3-25 ■ Updated Table 3-39 ■ Updated Figure 3-5 ■ Updated Pad characteristics type in Table 2-7 ■ Updated Section 3.5.4.1 ■ Updated Section 3.6 ■ Updated Table 3-36 ■ Updated Table 3-39

Revision	Date	Description
E	May 2013	■ Table 2-7: □ Change the configurable function of Pad 117 □ Change the pad characteritics voltage for Pads 34, 105, 51, and 67 to V_G2 □ Updated functional descriptions ■ Table 3-2: Change the minimum voltages for DC_IN and DC_IN_OVP_SNS ■ Table 3-3: □ Updated typical and maximum values for the 19.2 MHz XO clock □ Updated table note 1 ■ Table 3-5: □ Added a new row to the OVD subsection □ Updated the R(ds_on_usb_ovp) row ■ Table 3-6: Numerous updates ■ Table 3-7: Updated min, typ, and max values for trickle voltage - threshold hysteresis ■ Table 3-8: Replaced the table entirely ■ Table 3-12: Replaced the table entirely ■ Table 3-13: Added a subsection about IADC accuracy ■ Table 3-14: Changed column heading to “BMS SoC Accuracy” ■ Table 3-18: □ Added a table title and footnote □ Changed several voltage ranges ■ Added Figure 3-4 ■ Table 3-20: □ Added a footnote □ Updated transient response values □ Updated the ground current comment ■ Table 3-21: □ Added data for load transients and for peak output impedance vs frequency □ Updated ground current values □ Added two footnotes ■ Added Figure 3-5, Figure 3-6, and Figure 3-7 ■ Table 3-22: □ Added new (and updated existing) N1200 data □ Added entries for bypass mode on-resistance □ Added a footnote ■ Table 3-25: Updated several typical input and output ranges

Revision		Date
E (*cont.*)	May 2013	■ Table 3-29: □ Added rows for low-noise output start-up time and output buffer shift □ Changed the sub-section title to “Low-noise outputs: XO_OUT_Ax (RFCLKx)” □ Changed the sub-section title to “Low-power outputs: XO_OUT_Dx (BBCLKx)” □ Added a row for low-power output start-up timeUpdated the “Low-noise outputs” subheading and voltage swing min and max values □ Added a “Low-noise outputs: XO_OUT_Ax (RFCLKx)” subsection and three rows with values ■ Table 3-30: Updated the start-up time unit of measure and the operating voltage values ■ Table 3-32: Added entries for duty cycle and tolerance ■ Table 3-35: Updated table parameters, comments, and values ■ Table 3-36: Replaced the entire table ■ Table 3-37: Updated the dropout voltage and table note 2 ■ Table 3-38: □ Updated numerous vales in the table □ Removed the “Average efficiency” row □ Added a footnote ■ Table 3-41: Updated numerous values in the table ■ Figure 3-11: Replaced the entire graphic ■ Table 3-42 : Added the entire table ■ Section 3.9.2: □ Removed the combination assigned to the chipset □ Updated OPT setting information ■ Removed the “VOL and VOH for different driver strengths” table (formerly Table 3-41) ■ Table 4-2: Added rows for the PM8941 ES3 and PM8941 ES4/CS

Revision		Date
F	June 2013	■ Table 2-1: Changed V_INT to dVdd, added VDD_TORCH voltage ■ Table 2-6: Clarified voltage domains of OPT_x and other pins ■ Table 3-3: Updated DC current specifications ■ Table 3-6: □ Updated USB_IN / DC_IN input current limit and accuracy specifications □ Updated SMBB efficiency □ Updated SMMB reverse boost current and efficiency specifications ■ Table 3-12: □ Updated charger to battery switchover time □ Added VPH_PWR voltage dip specification during charger to battery switchover ■ Table 3-13: Specified IADC accuracy temperature and voltage range ■ Table 3-15: Updated battery interface specification ■ Table 3-18: Updated boost SMPS specified range ■ Table 3-20: Updated boost SMPS rated current, programmable and specified voltage range ■ Table 3-21 :Updated the HF SMPS PFM mode rated current and the short circuit current limit ■ Table 3-29: Updated Output duty cycle values ■ Added Table 3-27, which shows AMUX input to ADC output end-to-end accuracy ■ Table 3-38: □ Added table notes 1 and 3 □ Updated WLED boost and driver performance specification ■ Table 3-42: □ Added table notes 1 and 3 □ Updated poweron circuit performance specifications for the dual power-on sequence ■ Updated Figure 3-12 ■ Added Table 7-1 to show reliability data of PM8941

Revision		Date
G	August 2013	■ Table 3-6: Updated VPH_PWR to 3.6 V ■ Table 3-13: □ Added OCV measurement information □ Updated IADC accuracy information ■ Section 3.5.5.1: Updated to contain State of Charge (SoC) specifications information ■ Table 3-21: Updated PFM mode information and added a table footnote ■ Section 3.6.7: Added a new section on input connection options ■ Table 3-33: Updated typical and maximum values of duty cycle ■ Table 3-37: Updated minimum input voltage ■ Section 3.9.2: Updated OPT[4:1] hardwired controls information ■ Table 3-42: Updated the debounce timer maximum value ■ Table 3-43: □ Updated the tprebuck parameter values □ Updated the debounce timer maximum value ■ Section 6.1: Updated TBD composition to SAC405 ■ Chapter 6: Deleted *High temperature warpage* section ■ Section 7.2: Updated lead composition TBD to SAC405

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1 Introduction

1.1 Documentation overview

Technical information for the PM8941 device is primarily covered by the documents listed in Table 1-1 These documents should be studied for a thorough understanding of the IC and its applications. PM8941 documents are available from the CDMA Tech Support Website at https://support.cdmatech.com.

Table 1-1 Primary PM8941 device documentation

Document number	Title/description
80-NA555-1 (this document)	*PM8941 Device Specification* Provides all PM8941 electrical and mechanical specifications. Additional material includes pin assignment definitions; shipping, storage, and handling instructions; PCB mounting guidelines; and part reliability. This document can be used by company purchasing departments to facilitate procurement.
80-NA555-4	*PM8941 Device Revision Guide* Provides a history of PM8941 revisions. This document explains how to identify the various IC revisions and discusses known issues (or bugs) for each revision, and how to work around them.
80-NA555-5	*PM8841 and PM8941 Design Guidelines* ■ Detailed functional and interface descriptions for both ICs ■ Key design guidelines are illustrated and explained, including: □ Technology overviews □ DC power distribution □ Interface schematic details □ PCB layout guidelines □ External-component recommendations □ Ground and shielding recommendations

This PM8941 device specification is organized as follows:

Chapter 1 Provides an overview of PM8941 documentation, shows a high-level PM8941 functional block diagram, lists the device features, and lists terms and acronyms used throughout this document.

Chapter 2 Defines the IC pin assignments.

Chapter 3 Defines the IC electrical performance specifications, including absolute maximum ratings and recommended operating conditions.

Chapter 4 Provides IC mechanical information, including dimensions, markings, ordering information, moisture sensitivity, and thermal characteristics.

Chapter 5 Discusses shipping, storage, and handling of PM8941 devices.

Chapter 6 Presents procedures and specifications for mounting the PM8941 onto printed circuit boards (PCBs).

Chapter 7 Presents PM8941 reliability data, including definitions of the qualification samples and a summary of qualification test results.

1.2 PM8941 introduction

The PM8941 device (Figure 1-1), plus its companion PM8841 (80-NA554-x), integrates all wireless handset power management, general housekeeping, and user interface support functions into two mixed-signal ICs. Their versatile designs are suitable for multimode, multiband phones, and other wireless products such as data cards and PDAs.

The PM8941 mixed-signal CMOS device is available in the 229-pin wafer-level nanoscale package (229 WLNSP) that includes several ground pins for improved electrical ground, mechanical stability, and thermal continuity.

Since the PM8941 includes so many diverse functions, its operation is more easily understood by considering major functional blocks individually. Therefore, the PM8941 document set is organized by the following device functionality:

- Input power management
- Output power management
- General housekeeping
- User interfaces
- IC interfaces
- Configurable pins – either MPPs or GPIOs – that can be configured to function within some of the other categories

Most of the information contained in this device specification is organized accordingly – including the circuit groupings within the block diagram (Figure 1-1), pin descriptions (Chapter 2), and detailed electrical specifications (Chapter 3). Refer to the *PM8841 and PM8941 Design Guidelines* (80-NA555-5) for more detailed diagrams and descriptions of each PM8941 function and interface.

Five major functional blocks:

1) Input power management
2) Output power management
3) General housekeeping
4) User interfaces
5) IC-level interfaces

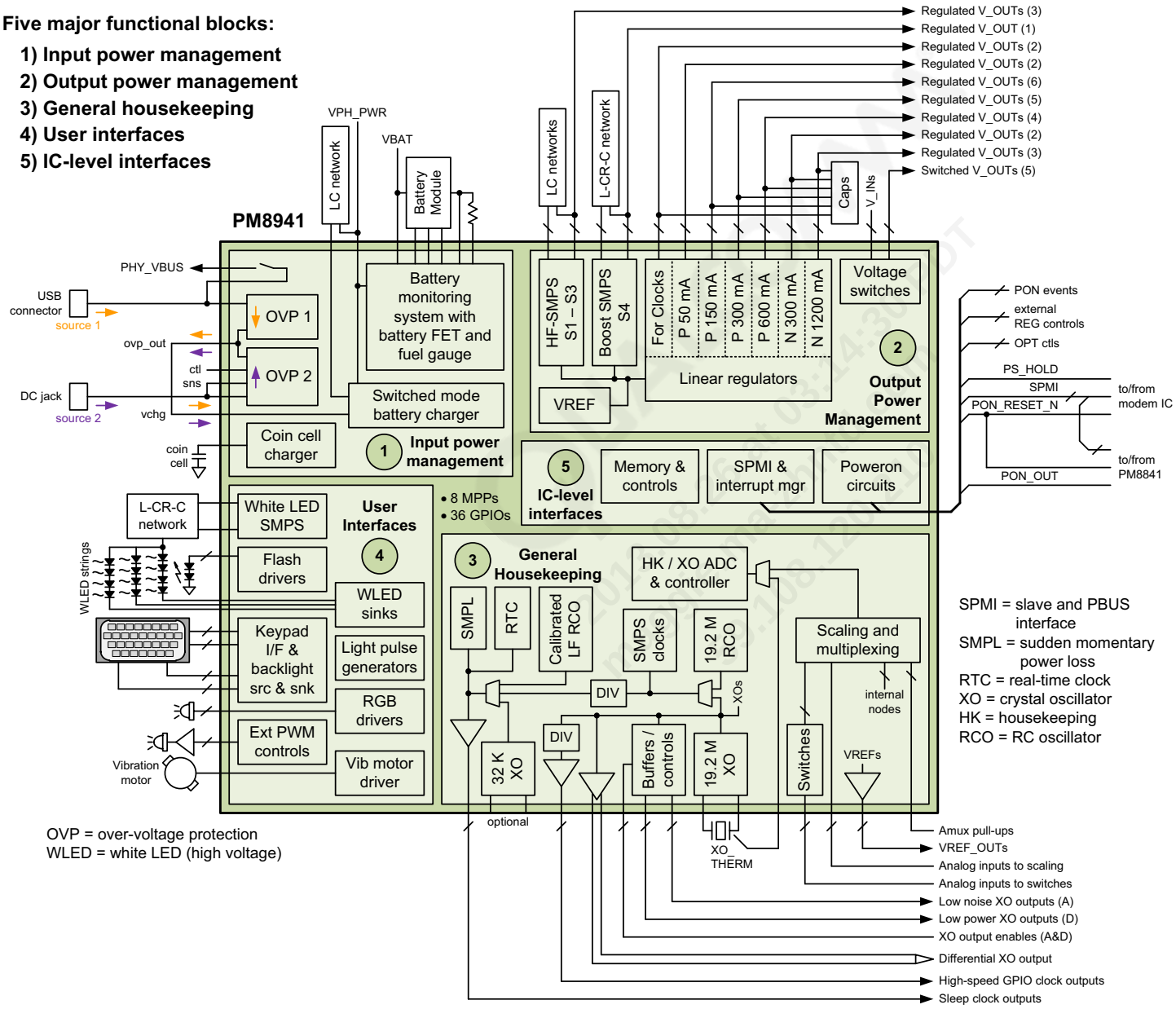


Figure 1-1 High-level PM8941 functional block diagram

1.3 PM8941 features

NOTE Some of the hardware features integrated within the PM8941 must be enabled through the modem IC software. See the latest version of the applicable software release notes to identify the enabled PMIC features.

1.3.1 New features integrated into the PM8941

- Dual-port switched mode battery charger (SMBC)
  - USB source with built-in 28 V over-voltage protection (OVP)
  - Wall charger source with built-in 15 V OVP, and the option for an external OVP pass device for higher protection voltages
- Integrated battery MOSFET
- 5 V boost SMPS
- Reverse boost mode
- Supplemented by the PM8841 (primarily for microprocessor FT-SMPS and other SMPS voltage sources)
- Many more analog multiplexer inputs for driving the HK/XO ADC
- Differential XO output port
- High-speed GPIOs suitable for clock outputs
- Four general-purpose LED sources and sinks – can be used for keypad backlighting
- Camera flash driver (two drivers at 1 A)
- The slave and PBUS interface (SPMI) is shared with the PM8841 to provide modem IC communications, including interrupts
- Programmable boot sequencer and reset control
- Plug-and-play support

1.3.2 Summary of PM8941 features

Features are listed on the next two pages.

Table 1-2 Summary of PM8941 features

Input power management	
Supported external power sources	USB and/or wall charger
Over-voltage protection USB Wall charger	 Fully integrated up to +28 V (integrated OVP FET) Fully integrated up to +15 V (integrated OVP FET); external pass device is supported for higher voltage
Supported battery technologies	Lithium-ion, lithium-ion polymer
Charger regulation method	Efficient switched-mode battery charger; four control loops: USB input current, VCHG input voltage, VPH_PWR output voltage, and battery current
Supported charging modes	Trickle, constant current, and constant voltage modes More automated for less software interaction
ATC indicator supply	Voltage options for when the RGB_RED driver is used for ATC indication
Battery MOSFET	Integrated
Voltage, current, & thermal sensors	Internal and external nodes; reported to on-chip state-machine
Battery monitoring system	Including battery fuel gauge for better accuracy
Coin cell or capacitor backup	Keep-alive power source; orchestrated charging
Output voltage regulation	
Switched-mode power supplies HF-SMPS Boost (5V)	 Three; two at 2.0 A each, one at 1.0 A One at 1.0 A
Low-dropout linear regulators	24 total: NMOS at 1.2 A (3), 300 mA (2); PMOS at 600 mA (4), 300 mA (5), 150 mA (6), 50 mA (2) and 2 for clocks
Pseudo-capless LDO designs	7 of 24 LDOs
Voltage switches	Suitable for power gating external circuitry: Three at 1.8 V, two at 5 V
General housekeeping	
On-chip ADC	Shared housekeeping (HK) and XO support
Analog multiplexing for ADC HK inputs XO input	 Many internal nodes and external inputs, including configurable MPPs Dedicated pin (XO_THERM)
Over-temperature protection	Multistage smart thermal control
Automatic fault protection	At fault: PMIC powers off, ignores all power-on triggers except KPD_PWR_N, and turns VREG_FAULT on
19.2 MHz oscillator support	XO (with on-chip ADC)
XO controller and XO outputs	Five sets: three low-noise outputs (A) and two low-power outputs (D)
Differential XO clock output	One
Special purpose clock outputs	Extra sleep clock; 19.2, 9.6, 4.8, 2.4, and 1.2 MHz, including low-power mode 2.4 MHz for MP3; four high-speed GPIOs for fast clocks
32 kHz clock source (optional)	XO source eliminates 32.768 kHz crystal if desired
Realtime clock	RTC clock circuits and alarms

User interfaces	
30 V WLED boost converter	Generates supply voltage for white LEDs
WLED sinks	Three (matched); supports strings of up to 8 white LEDs each
Keypad backlighting	General-purpose sources/sinks that can be used for backlighting
Camera flash drivers	Two; flash and torch modes
RGB drivers	Three – one for each color, 12 mA each
Other current drivers	MPPs can be configured to sink up to 40 mA ATC indicator (shared with red RGB driver)
Light pulse generators	8-channels for WLEDs, RGBs, vibration motor, and GPIOs 4-channels for general-purpose sources/sinks
Controls for external current drivers	Four PWM outputs (GPIOs)
Vibration motor driver	1.2 to 3.1 V in 100 mV increments
IC-level interfaces	
Primary status and control	2-line SPMI
PM8841 control	Power-on, resets, and shared SPMI
Interrupt managers	Supported by SPMI
Optional hardware configurations	OPT bits select hardware configuration
Power sequencing	Power-on, power-off, and soft resets
Extra features	Level translation; ext regulator enables; detect inputs & interrupt outputs
Configurable I/Os	
MPPs	8; configurable as digital inputs or outputs; level-translating bidirectional I/Os; analog multiplexer inputs; or VREF analog outputs
GPIO pins	36; configurable as digital inputs or outputs or level-translating I/Os; all are much faster than MPPs; four special high-speed GPIOs for clock outputs
Package	
Size	5.82 × 6.15 × 0.55 mm
Pin count and package type	229-pin WLNSP

1.4 Terms and acronyms

Table 1-3 defines terms and acronyms used throughout this document.

Table 1-3 Terms and acronyms

Term or acronym	Definition
ADC	Analog-to-digital converter
API	Application programming interface
ATC	Auto-trickle charger
AVS	Adaptive voltage scaling
BMS	Battery monitoring system
CDMA	Code Division Multiple Access
DVS	Dynamic voltage scaling
FT-SMPS	Fast transient SMPS
GPIO	General-purpose input/output
GSM	Global system for mobile communications
HF-SMPS	High frequency SMPS
HK	Housekeeping
HSED	Headset send/end detect
HS-USB	High-speed USB
ID	Identification
LDO	Low dropout (linear regulator)
Li	Lithium
LPG	Light pulse generator
MPP	Multipurpose pin
MUX	Multiplexer
OTG	On-the-go
OVP	Over-voltage protection
PA	Power amplifier
PBM	Pulse burst modulation
PCB	Printed circuit board
PDA	Personal digital assistant
PFM	Pulse frequency modulation
PLL	Phase-locked loop
PM	Power management
PWM	Pulse width modulation
QTI	Qualcomm Technologies, Incorporated
RCO	RC oscillator
RTC	Realtime clock

Table 1-3 Terms and acronyms (cont.)

Term or acronym	Definition
RUIM	Removable user identity module
SMBC	Switched-mode battery charger
SMPL	Sudden momentary power loss
SMPS	Switched-mode power supply (DC-to-DC converter)
SPMI	Slave and PBUS interface
SS-USB	Super-speed USB
SSC	SMPS step control
SVS	Static voltage scaline
TCXO	Temperature-compensated crystal oscillator
UART	Universal asynchronous receiver/transmitter
UICC	Universal integrated circuit card
UIM	User identity module
UMTS	Universal mobile telecommunications system
USB	Universal serial bus
UVLO	Under-voltage lockout
VCO	Voltage-controlled oscillator
VCTCXO	Voltage-controlled temperature-compensated crystal oscillator
WLNSP	Wafer-level NSP
WLED	White LED
XO	Crystal oscillator
Zero-IF or ZIF	Zero intermediate frequency

1.5 Special marks

Special marks used in this document are defined below.

Table 1-4 Special marks

Mark	Definition
[ ]	Brackets ([ ]) sometimes follow a pin, register, or bit name. These brackets enclose a range of numbers. For example, DATA [7:4] may indicate a range that is 4 bits in length, or DATA[7:0] may refer to eight DATA pins.
_N	A suffix of _N indicates an active low signal. For example, PON_RESET_N.
0x0000	Hexadecimal numbers are identified with an x in the number, (for example, 0x0000). All numbers are decimal (base 10) unless otherwise specified. Non-obvious binary numbers have the term binary enclosed in parentheses at the end of the number, [for example, 0011 (binary)].
|	A vertical bar in the outside margin of a page indicates that a change was made since the previous revision of this document.

2 Pin Definitions

The PM8941 is available in the 229 WLNSP – see Chapter 4 for package details. A high-level view of the pin assignments is illustrated in Figure 2-1.

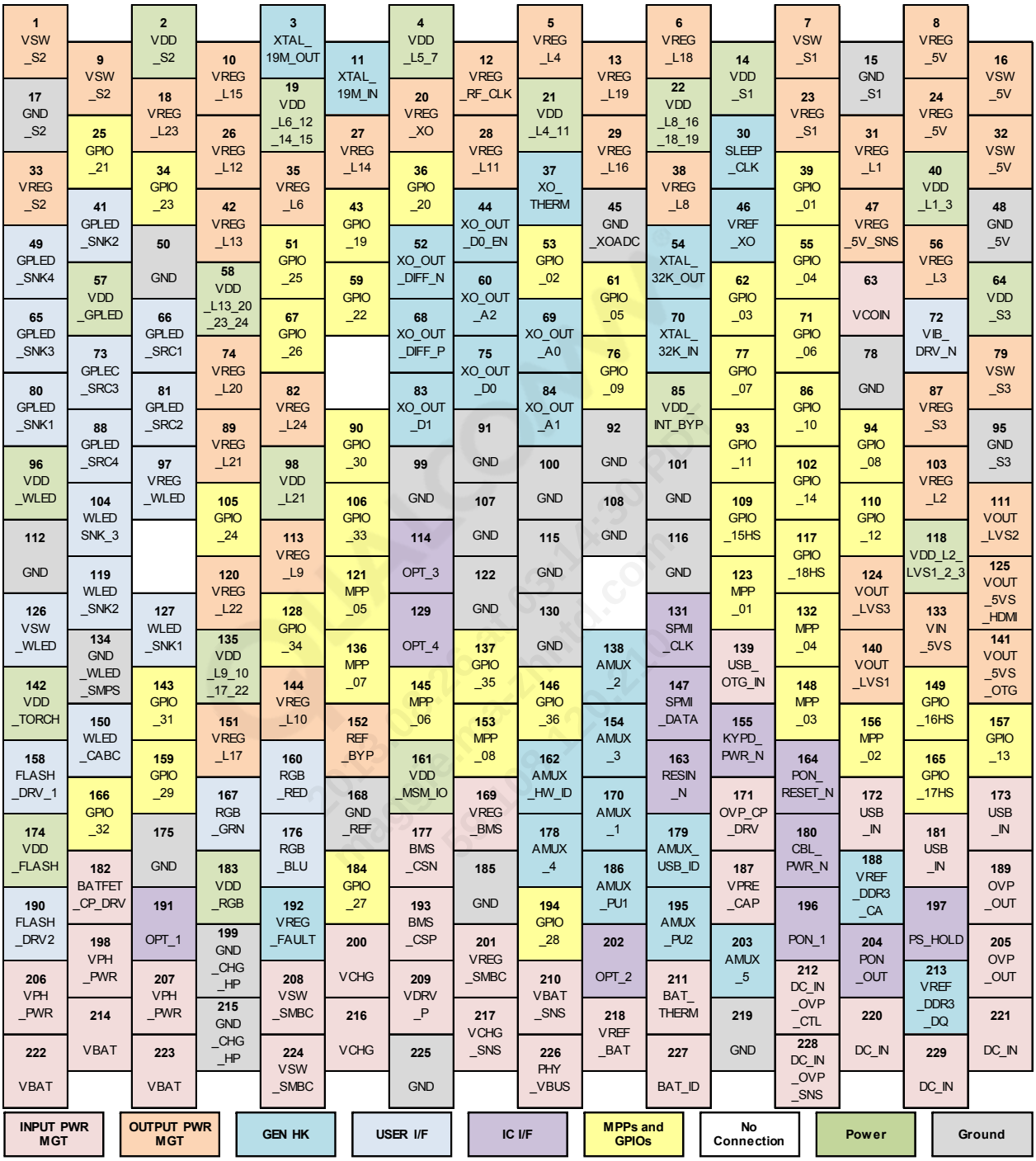


Figure 2-1 PM8941 pin assignments (top view)

2.1 I/O parameter definitions

Table 2-1 I/O description (pad type) parameters

Symbol	Description
Pad attribute	
AI	Analog input
AO	Analog output
DI	Digital input (CMOS)
DO	Digital output (CMOS)
PI	Power input; a pin that handles 10 mA or more of current flow into the device
PO	Power output; a pin that handles 10 mA or more of current flow out of the device
Z	High-impedance (high-Z) output
Pad voltage groupings	
dVdd	Internally generated 1.8 V supply voltage for some power-on circuits
V_PAD	Supply for modem IC interfaces; connected to VDD_MSM_IO
V_XLP	Supply for XO low-power (D) output buffers; connected internally to VREG_L6
V_XLN	Supply for XO low-noise (A) output buffers; connected internally to VREG_RF_CLK
V_G1	Selectable supply for GPIO circuits 1 – 14; options include: □ 0 = VPH_PWR (3.6 V); connected to VDD_L8_16_18_19 □ 1 = LDO1 (1.225 V); connected internally □ 2 = SMPS3 (1.8 V); connected to VDD_L2_LVS1_2_3 □ 3 = LDO6 (1.8 V); connected internally
V_G2	Selectable supply for GPIO circuits 19 – 36; options include: □ 0 = VPH_PWR (3.6 V); connected to VDD_RGB □ 1 = VDD_TORCH (5.1 V typical) □ 2 = SMPS3 (1.8 V); connected to VDD_MSM_IO □ 3 = LDO6 (1.8 V); connected internally
V_G3	Selectable supply for GPIO circuits 15 – 18; options include: □ 2 = SMPS3 (1.8 V); connected to VDD_L2_LVS1_2_3 □ 3 = LDO6 (1.8 V); connected internally
V_M1	Selectable supply for MPP circuits 1 – 4; options include: □ 0 = VPH_PWR (3.6 V); connected to VDD_L8_16_18_19 □ 1 = LDO1 (1.225 V); connected internally □ 2 = SMPS3 (1.8 V); connected to VDD_L2_LVS1_2_3 □ 3 = LDO6 (1.8 V); connected internally
V_M2	Selectable supply for MPP circuits 5 – 8; options include: □ 0 = VPH_PWR (3.6 V); connected to VDD_GPLED □ 1 = LDO1 (1.225 V); connected internally □ 2 = SMPS3 (1.8 V); connected to VDD_MSM_IO □ 3 = LDO6 (1.8 V); connected internally

Table 2-1 I/O description (pad type) parameters (cont.)

Symbol	Description
GPIO pin configurations	
GPIO pins, when configured as inputs, have configurable pull settings	
NP	No internal pull enabled
PU	Internal pullup enabled
PD	Internal pulldown enabled
GPIO pins, when configured as outputs, have configurable drive strengths	
H	High: ~ 0.9 mA at 1.8 V; ~ 1.9 mA at 2.6 V
M	Medium: ~ 0.6 mA at 1.8 V; ~ 1.25 mA at 2.6 V
L	Low: ~ 0.15 mA at 1.8 V; ~ 0.3 mA at 2.6 V

2.2 Pin descriptions

Descriptions of all pins are presented in the following tables, organized by functional group:

Table 2-2 Input power management

Table 2-3 Output power management

Table 2-4 General housekeeping

Table 2-5 User interfaces

Table 2-6 IC-level interfaces

Table 2-7 Configurable input/output – GPIO and MPPs

Table 2-8 Power-supply pins

Table 2-9 Ground pins

Table 2-2 Pin descriptions – input power management functions

Pad #	Pad name and/or function	Pad name or alt function	Pad characteristics [1]		Functional description
			Voltage	Type	
Dual-port SMBC (USB and wall charger sources)					
139	OTG_IN		–	PI	OTG switch input
226	PHY_VBUS		–	PO	Gated (protected) supply to USB_PHY
172, 173, 181	USB_IN		–	PI	Input power from USB source
220, 221, 229	DC_IN		–	PI	Input power from wall charger
189, 205	OVP_OUT		–	PO	Protected output via USB or wall charger
228	DC_IN_OVP_SNS		–	AI	Wall charger sense (external FET option)
212	DC_IN_OVP_CTL		–	AO	Control voltage to optional external FET
171	OVP_CP_DRV		–	AI	OVP charge pump driver bypass cap
187	VPRE_CAP		–	AO	VPRE regulator load capacitor
200, 216	VCHG		–	PI	Charger input voltage from OVP_OUT
217	VCHG_SNS		–	AI	Charger input voltage sense point
208, 224	VSW_SMBC		–	PO	Charger SMPS switching output
201	VREG_SMBC		–	AI	Charger SMPS sense point (VPH_PWR)
209	VDRV_P		–	AI	Buck driver high-side bypass capacitor
198, 206, 207	VPH_PWR		–	PI, PO	Phone power node; input during charging, output during battery operation
BMS circuits					
182	BATFET_CP_DRV		–	AI	BATFET charge pump driver bypass cap
214, 222, 223	VBAT		–	PI, PO	Battery node; input during battery operation, output during charging
210	VBAT_SNS		–	AI	Battery voltage sense point
169	VREG_BMS		–	AO	Load cap for LDO that powers BMS ADC
193	BMS_CSP		–	AI	Battery current sense – plus
177	BMS_CSM		–	AI	Battery current sense – minus
218	VREF_BAT		–	AO	Reference voltage for battery sensors
211	BAT_THERM		–	AI	Battery thermistor input
227	BAT_ID		–	AI	Battery identification input
Coin cell or keep-alive battery					
63	VCOIN		–	AI, AO	Sense input or charge output

1. Refer to Table 2-1 for parameter and acronym definitions.

Table 2-3 Pin descriptions – output power management functions

Pad #	Pad name and/or function	Pad name or alt function	Pad characteristics [1]		Functional description
			Voltage	Type	
Switched-mode power supply (SMPS) circuits					
7	VSW_S1		–	PO	S1 SMPS switching output
23	VREG_S1		–	AI	S1 SMPS sense point
1, 9	VSW_S2		–	PO	S2 SMPS switching output
33	VREG_S2		–	AI	S2 SMPS sense point
79	VSW_S3		–	PO	S3 SMPS switching output
87	VREG_S3		–	AI	S3 SMPS sense point
16, 32	VSW_5V		–	PO	S4 5 V SMPS switching output
8, 24	VREG_5V		–	AI, PO	S4 5 V SMPS regulated output
47	VREG_5V_SNS		–	AI	S4 5 V SMPS sense point
LDO linear regulators					
31	VREG_L1		–	PO	Linear regulator L1 output
103	VREG_L2		–	PO	Linear regulator L2 output
56	VREG_L3		–	PO	Linear regulator L3 output
5	VREG_L4		–	PO	Linear regulator L4 output
12	VREG_RF_CLK	VREG_L5	–	PO	Linear regulator RF clocks output
35	VREG_L6		–	PO	Linear regulator L6 output
20	VREG_XO	VREG_L7	–	PO	Linear regulator XO block load cap
38	VREG_L8		–	PO	Linear regulator L8 output
113	VREG_L9		–	PO	Linear regulator L9 output
144	VREG_L10		–	PO	Linear regulator L10 output
28	VREG_L11		–	PO	Linear regulator L11 output
26	VREG_L12		–	PO	Linear regulator L12 output
42	VREG_L13		–	PO	Linear regulator L13 output
27	VREG_L14		–	PO	Linear regulator L14 output
10	VREG_L15		–	PO	Linear regulator L15 output
29	VREG_L16		–	PO	Linear regulator L16 output
151	VREG_L17		–	PO	Linear regulator L17 output
6	VREG_L18		–	PO	Linear regulator L18 output
13	VREG_L19		–	PO	Linear regulator L19 output
74	VREG_L20		–	PO	Linear regulator L20 output
89	VREG_L21		–	PO	Linear regulator L21 output
120	VREG_L22		–	PO	Linear regulator L22 output
18	VREG_L23		–	PO	Linear regulator L23 output

Table 2-3 Pin descriptions – output power management functions (cont.)

Pad #	Pad name and/or function	Pad name or alt function	Pad characteristics [1]		Functional description
			Voltage	Type	
82	VREG_L24		–	PO	Linear regulator L24 output
192	VREG_FAULT		–	PO	Fault protection LDO output
Bandgap voltage reference (VREF) circuits					
152	REF_BYP		–	AO	Bandgap reference bypass cap
Voltage switches					
118	VDD_L2_LVS1_2_3		–	PI	Input to low voltage switches
140	VOUT_LVS1		–	PO	Low voltage switch 1 output (1.8 V)
111	VOUT_LVS2		–	PO	Low voltage switch 2 output (1.8 V)
124	VOUT_LVS3		–	PO	Low voltage switch 3 output (1.8 V)
133	VIN_5VS		–	PI	Input to 5 V switches
125	VOUT_5VS_HDMI		–	PO	5 V switch 1 output (HDMI)
141	VOUT_5VS_OTG		–	PO	5 V switch 2 output (OTG)

1. Refer to Table 2-1 for parameter and acronym definitions.

Table 2-4 Pin descriptions – general housekeeping functions

Pad #	Pad name and/or function	Pad name or alt function	Pad characteristics [3]		Functional description
			Voltage	Type	
GPIO assignments for general housekeeping functions [1]					
MPP assignments for general housekeeping functions [2]					
Analog multiplexer and HK/XO ADC circuits					
37	XO_THERM		–	AI	ADC input – XO thermistor
162	AMUX_HW_ID		–	AI	AMUX input for hardware ID
179	AMUX_USB_ID		–	AI	AMUX input for USB ID
170	AMUX_1		–	AI	AMUX input 1
138	AMUX_2		–	AI	AMUX input 2
154	AMUX_3		–	AI	AMUX input 3
178	AMUX_4		–	AI	AMUX input 4
203	AMUX_5		–	AI	AMUX input 5
186	AMUX_PU1		–	AI	AMUX pullup resistor 1
195	AMUX_PU2		–	AI	AMUX pullup resistor 2

Table 2-4 Pin descriptions – general housekeeping functions (cont.)

Pad #	Pad name and/or function	Pad name or alt function	Pad characteristics [3]		Functional description
			Voltage	Type	
19.2 MHz XO circuits					
11	XTAL_19M_IN		–	AI	19.2 MHz crystal input
3	XTAL_19M_OUT		–	AO	19.2 MHz crystal output
69	XO_OUT_A0		V_XLN	DO	Low noise XO output 0
84	XO_OUT_A1		V_XLN	DO	Low noise XO output 1
60	XO_OUT_A2		V_XLN	DO	Low noise XO output 2
75	XO_OUT_D0		V_XLP	DO	Low power XO output 0
83	XO_OUT_D1		V_XLP	DO	Low power XO output 1
68	XO_OUT_DIFF_P		–	AO	Differential XO output – positive
52	XO_OUT_DIFF_N		–	AO	Differential XO output – negative
44	XO_OUT_D0_EN		V_PAD	DI	Low power XO output 0 enable
32.768 kHz XTAL, sleep clock, and MP3 clock circuits					
70	XTAL_32K_IN		–	AI	32.768 kHz crystal input
54	XTAL_32K_OUT		–	AO	32.768 kHz crystal output
30	SLEEP_CLK		V_PAD	DO	Sleep clock to modem IC and others
VREF outputs					
46	VREF_XO		–	AO	Reference voltage for XO thermistor
188	VREF_DDR3_CA		–	AO	Reference voltage for DDR3 memory CA
213	VREF_DDR3_DQ		–	AO	Reference voltage for DDR3 memory DQ

1. GPIOs are used for other general housekeeping functions not listed here; those details will be included in future revisions of this document. To assign a GPIO a particular function, identify all of your application's requirements and map each GPIO to its function – carefully avoiding assignment conflicts. All GPIOs are listed in Table 2-7.
2. MPPs are used for other general housekeeping functions not listed here; those details will be included in future revisions of this document. To assign an MPP a particular function, identify all of your application's requirements and map each MPP to its function – carefully avoiding assignment conflicts. All MPPs are listed in Table 2-7.
3. Refer to Table 2-1 for parameter and acronym definitions.

Table 2-5 Pin descriptions – user interface functions

Pad #	Pad name and/or function	Pad name or alt function	Pad characteristics [1]		Functional description
			Voltage	Type	
White LED (high-voltage) current drivers					
126	VSW_WLED		–	PO	White LED boost SMPS switching output
97	VREG_WLED		–	AI	White LED boost SMPS sense point
127	WLED_SNK1		–	AI	White LED sink 1
119	WLED_SNK2		–	AI	White LED sink 2
104	WLED_SNK3		–	AI	White LED sink 3

Table 2-5 Pin descriptions – user interface functions (cont.)

Pad #	Pad name and/or function	Pad name or alt function	Pad characteristics [1]		Functional description
			Voltage	Type	
150	WLED_CABC		V_PAD	DI	WLED content adaptive backlight control
General-purpose current sources and sinks (can be used for backlighting)					
66	GPLED_SRC1		–	AO	General-purpose LED source 1
81	GPLED_SRC2		–	AO	General-purpose LED source 2
73	GPLED_SRC3		–	AO	General-purpose LED source 3
88	GPLED_SRC4		–	AO	General-purpose LED source 4
80	GPLED_SNK1		–	AI	General-purpose LED sink 1
41	GPLED_SNK2		–	AI	General-purpose LED sink 2
65	GPLED_SNK3		–	AI	General-purpose LED sink 3
49	GPLED_SNK4		–	AI	General-purpose LED sink 4
Camera flash or torch					
158	FLASH_DRV_1		–	AO	Flash/torch driver 1 output
190	FLASH_DRV_2		–	AO	Flash/torch driver 2 output
Low-voltage current drivers					
160	RGB_RED		–	AO	Red LED driver output
167	RGB_GRN		–	AO, PI	Green LED driver output
176	RGB_BLU		–	AO, PI	Blue LED driver output
Vibration motor driver					
72	VIB_DRV_N		–	PO	Vibration motor driver output control

1. Refer to Table 2-1 for parameter and acronym definitions.

Table 2-6 Pin descriptions – IC-level interface functions

Pad #	Pad name and/or function	Pad name or alt function	Pad characteristics [1]		Functional description
			Voltage	Type	
Poweron circuit inputs					
180	CBL_PWR_N		dVdd	DI	Cable poweron detect input
155	KYPD_PWR_N		dVdd	DI	Keypad poweron detect input
129	OPT_4		VDD	DI	Option HW configuration control bit 4
114	OPT_3		VDD	DI	Option HW configuration control bit 3
202	OPT_2		VDD	DI	Option HW configuration control bit 2
191	OPT_1		VDD	DI	Option HW configuration control bit 1

Table 2-6 Pin descriptions – IC-level interface functions (cont.)

Pad #	Pad name and/or function	Pad name or alt function	Pad characteristics [1]		Functional description
			Voltage	Type	
197	PS_HOLD		V_PAD	DI	Power supply hold control input
163	RESIN_N		dVdd	DI	PMIC reset input
196	PON_1		dVdd	DI	Edge-triggered poweron input
Poweron circuit outputs and primary PM / modem IC interface signals					
131	SPMI_CLK		V_PAD	DO	Slave and PBUS interface clock
147	SPMI_DATA		V_PAD	DI, DO	Slave and PBUS interface data
164	PON_RESET_N		V_PAD	DO	Poweron reset output control
204	PON_OUT		V_PAD	DO	Poweron control to PM8841

1. Refer to Table 2-1 for parameter and acronym definitions.

Table 2-7 Pin descriptions – configurable input/output functions

Pad #	Pad name	Configurable function	Pad characteristics [1]		Functional description
			Voltage	Type	
MPP functions					
123	MPP_01		–	DI-Z	Configurable MPP; default analog output at 1.25 V
		VREF_PADS	–	AO	Reference for modem IC 3 V I/Os
156	MPP_02		–	DI-Z	Configurable MPP; default Hi-Z out
148	MPP_03		–	DI-Z	Configurable MPP; default Hi-Z out
		VREF_DAC	–	AO	Reference for modem IC combo DAC
132	MPP_04		–	DI-Z	Configurable MPP; default Hi-Z out
121	MPP_05		–	DI-Z	Configurable MPP; default Hi-Z out
145	MPP_06		–	DI-Z	Configurable MPP; default Hi-Z out
136	MPP_07		–	DI-Z	Configurable MPP; default Hi-Z out
153	MPP_08		–	DI-Z	Configurable MPP; default Hi-Z out
GPIO functions					
39	GPIO_01		V_G1	DO-Z	Configurable GPIO; default digital input with 10 µA pull-down
		KYPD_SNS1	V_G1	DI	Keypad sense bit 1
53	GPIO_02		V_G1	DO-Z	Configurable GPIO, default digital input with 10 µA pull-down
		KYPD_SNS2	V_G1	DI	Keypad sense bit 2
62	GPIO_03		V_G1	DO-Z	Configurable GPIO; default digital input with 10 µA pull-down
		KYPD_SNS3	V_G1	DI	Keypad sense bit 3
55	GPIO_04		V_G1	DO-Z	Configurable GPIO; default digital input with 10 µA pull-down
		KYPD_SNS4	V_G1	DI	Keypad sense bit 4
61	GPIO_05		V_G1	DO-Z	Configurable GPIO; default digital input with 10 µA pull-down
		KYPD_SNS5	V_G1	DI	Keypad sense bit 5

Table 2-7 Pin descriptions – configurable input/output functions (cont.)

Pad #	Pad name	Configurable function	Pad characteristics [1]		Functional description
			Voltage	Type	
71	GPIO_06		V_G1	DO-Z	Configurable GPIO; default digital input with 10 µA pull-down
		KYPD_SNS6	V_G1	DI	Keypad sense bit 6
77	GPIO_07		V_G1	DO-Z	Configurable GPIO; default digital input with 10 µA pull-down
		KYPD_SNS7	V_G1	DI	Keypad sense bit 7
94	GPIO_08		V_G1	DO-Z	Configurable GPIO; default digital input with 10 µA pull-down
		KYPD_SNS8	V_G1	DI	Keypad sense bit 8
76	GPIO_09		V_G1	DO-Z	Configurable GPIO; default digital input with 10 µA pull-down
		KYPD_DRV1	V_G1	DO	Keypad driver bit 1
86	GPIO_10		V_G1	DO-Z	Configurable GPIO; default digital input with 10 µA pull-down
		KYPD_DRV2	V_G1	DO	Keypad driver bit 2
93	GPIO_11		V_G1	DO-Z	Configurable GPIO; default digital input with 10 µA pull-down
		KYPD_DRV3	V_G1	DO	Keypad driver bit 3
110	GPIO_12		V_G1	DO-Z	Configurable GPIO; default digital input with 10 µA pull-down
		KYPD_DRV4	V_G1	DO	Keypad driver bit 4
157	GPIO_13		V_G1	DO-Z	Configurable GPIO; default digital input with 10 µA pull-down
		KYPD_DRV5	V_G1	DO	Keypad driver bit 5
102	GPIO_14		V_G1	DO-Z	Configurable GPIO; default digital input with 10 µA pull-down
		KYPD_DRV6	V_G1	DO	Keypad driver bit 6
109	GPIO_15		V_G3	DO-Z	Configurable GPIO; default digital input with 10 µA pull-down
		DIVCLK1	V_G3	DO	Divided down XO clock output; used for codec
		SLEEP_CLK1	V_G3	DO	Extra sleep clock 1 output
149	GPIO_16		V_G3	DO-Z	Configurable GPIO ; default digital input with 10 µA pull-down
		DIVCLK2	V_G3	DO	Divided down XO clock output; used for haptics
		SLEEP_CLK2	V_G3	DO	Extra sleep clock 2 output
165	GPIO_17		V_G3	DO-Z	Configurable GPIO; default digital input with 10 µA pull-down
		DIVCLK3	V_G3	DO	Divided down XO clock output; used for QPA
		SLEEP_CLK3	V_G3	DO	Extra sleep clock 3 output
117	GPIO_18		V_G3	DO-Z	Configurable GPIO; default digital input with 10 µA pull-down
		DIVCLK3	V_G3	DO	Divided down XO clock output
		ALT_SLEEP_CLK	V_G3	DO	Internal RC or XO/586 output
43	GPIO_19		V_G2	DO-Z	Configurable GPIO; default digital input with 10 µA pull-down
36	GPIO_20		V_G2	DO-Z	Configurable GPIO; default digital input with 10 µA pull-down
25	GPIO_21		V_G2	DO-Z	Configurable GPIO; default digital output at VPH_PWR level
		EXT_REG_EN1	V_G2	DO	External regulator enable 1
59	GPIO_22		V_G2	DO-Z	Configurable GPIO; default digital input with 10 µA pull-down
34	GPIO_23		V_G2	DO-Z	Configurable GPIO
		KYPD_DRV7	V_G2	DO	Keypad driver bit 7
		LPG_CH1	V_G2	DO	LPG channel 1 output

Table 2-7 Pin descriptions – configurable input/output functions (cont.)

Pad #	Pad name	Configurable function	Pad characteristics [1]		Functional description
			Voltage	Type	
105	GPIO_24		V_G2	DO-Z	Configurable GPIO
		KYPD_DRV8	V_G2	DO	Keypad driver bit 8
		LPG_CH2	V_G2	DO	LPG channel 2 output
51	GPIO_25		V_G2	DO-Z	Configurable GPIO
		KYPD_DRV9	V_G2	DO	Keypad driver bit 9
		LPG_CH3	V_G2	DO	LPG channel 3 output
67	GPIO_26		V_G2	DO-Z	Configurable GPIO
		KYPD_DRV10	V_G2	DO	Keypad driver bit 10
		LPG_CH4	V_G2	DO	LPG channel 4 output
184	GPIO_27		V_G2	DO-Z	Configurable GPIO; default digital input with 10 µA pull-down
		FLASH_STROBE	V_G2	DI	Flash now strobe
194	GPIO_28		V_G2	DO-Z	Configurable GPIO; default digital input with 10 µA pull-down
		FLASH_MASK1	V_G2	DI	Mask 1 for FLASH LED driver
159	GPIO_29		V_G2	DO-Z	Configurable GPIO; default digital input with 10 µA pull-down
		FLASH_MASK2	V_G2	DI	Mask 2 for FLASH LED driver
90	GPIO_30		V_G2	DO-Z	Configurable GPIO; default digital input with 10 µA pull-down
		FLASH_MASK3	V_G2	DI	Mask 3 for FLASH LED driver
143	GPIO_31		V_G2	DO-Z	Configurable GPIO; default digital input with 10 µA pull-down
		BAT_ALARM_OUT	V_G2	DO	Battery removal detection output
166	GPIO_32		V_G2	DO-Z	Configurable GPIO; default digital input with 10 µA pull-down
		XO_OUT_D1_EN	V_G2	DI	Enable signal for low power D1 buffer
106	GPIO_33		V_G2	DO-Z	Configurable GPIO; default digital input with 10 µA pull-down
		PWM_LED_CTL1	V_G2	DO	PWM output for LED control 1
		LPG_CH5	V_G2	DO	LPG channel 5 output
		XO_OUT_A0_EN	V_G2	DI	Enable signal for low noise A0 buffer
128	GPIO_34		V_G2	DO-Z	Configurable GPIO; default digital input with 10 µA pull-down
		PWM_LED_CTL2	V_G2	DO	PWM output for LED control 2
		LPG_CH6	V_G2	DO	LPG channel 6 output
		XO_OUT_A1_EN	V_G2	DI	Enable signal for low noise A1 buffer
137	GPIO_35		V_G2	DO-Z	Configurable GPIO; default digital input with 10 µA pull-down
		PWM_LED_CTL3	V_G2	DO	PWM output for LED control 3
		LPG_CH7	V_G2	DO	LPG channel 7 output
		XO_OUT_A2_EN	V_G2	DI	Enable signal for low noise A2 buffer
146	GPIO_36		V_G2	DO-Z	Configurable GPIO; default digital input with 10 µA pull-down
		PWM_LED_CTL4	V_G2	DO	PWM output for LED control 4
		LPG_CH8	V_G2	DO	LPG channel 8 output

1. Refer to Table 2-1 for parameter and acronym definitions.

All GPIOs default to digital input with 10 µA pull-down at poweron. During power-on, PBS programs GPIO_21 as digital output high at VPH_PWR level to enable the external boost-bypass.

All MPPs are high-Z at power-on. During power-on, PBS programs MPP_01 as analog output which is used as a reference for modem IC 3 V I/Os.

Only odd MPPs (MPP_01, MPP_03, MPP_05, MPP_07) can be configured as analog outputs. Only even MPPs (MPP_02, MPP_04, MPP_06, MPP_08) have current sink capability.

Table 2-8 Pin descriptions – input DC power

Pad #	Pad name	Functional description
174	VDD_FLASH	Power supply for camera flash driver
57	VDD_GPLED	Power supply for general-purpose LED source/sinks
85	VDD_INT_BYP	Bypass capacitor for internal supply voltage
40	VDD_L1_3	Power supply for L1 and L3 LDO circuits
118	VDD_L2_LVS1_2_3	Power supply for L2 LDO and low V switch circuits
21	VDD_L4_11	Power supply for L4 and L11 LDO circuits
4	VDD_L5_7	Power supply for L5 and L7 LDO circuits
19	VDD_L6_12_14_15	Power supply for L6, L12, L14, and L15 LDO circuits
22	VDD_L8_16_18_19	Power supply for L8, L16, L18, and L19 LDO circuits
135	VDD_L9_10_17_22	Power supply for L9, L10, L17, and L22 LDO circuits
58	VDD_L13_20_23_24	Power supply for L13, L20, L23, and L24 LDO circuits
98	VDD_L21	Power supply for L21 LDO circuit
161	VDD_MSM_IO	Power supply for PMIC/modem IC I/Os
183	VDD_RGB	Power for red, green, blue LED drivers
14	VDD_S1	Power supply for S1 buck converter
2	VDD_S2	Power supply for S2 buck converter
64	VDD_S3	Power supply for S3 buck converter
142	VDD_TORCH	Power supply for camera torch drivers
96	VDD_WLED	Power supply for white LED boost SMPS circuits

Table 2-9 Pin descriptions – grounds

Pad #	Pad name	Functional description
50, 78, 91, 92, 99, 100, 101, 107, 108, 112, 115, 116, 122, 130, 175, 185, 219, 225	GND	Ground for all non-specialized circuits
199, 215	GND_CHG_HP	Ground for charger's buck high power circuits
168	GND_REF	Ground for bandgap reference circuit
15	GND_S1	Ground for S1 buck converter circuits
17	GND_S2	Ground for S2 buck converter circuits
95	GND_S3	Ground for S3 buck converter circuits
48	GND_5V	Ground for 5 V boost converter circuits

Table 2-9 Pin descriptions – grounds (cont.)

Pad #	Pad name	Functional description
134	GND_WLED_SMPS	Ground for white LED boost SMPS circuits
45	GND_XOADC	Ground for XO ADC circuits

3 Electrical Specifications

3.1 Absolute maximum ratings

Operating the PM8941 under conditions beyond its absolute maximum ratings (Table 3-1) may damage the device. Absolute maximum ratings are limiting values to be considered individually when all other parameters are within their specified operating ranges. Functional operation and specification compliance under any absolute maximum condition, or after exposure to any of these conditions, is not guaranteed or implied. Exposure may affect device reliability.

Table 3-1 Absolute maximum ratings

Parameter		Min	Max	Units
Power supply and related sense voltages				
USB_IN	Input power from USB source	-2.0	30	V
DC_IN_OVP_SNS	Input power from wall charger, sense pin	-2.0	30	V
DC_IN	Input power from wall charger	-2.0	15	V
VCHG, VCHG_SNS, VDD_FLASH	Charger input voltage, sense pin, flash driver supply in flash mode	-2.0	15	V
VREG_5V, VDD_TORCH, VIN_5VS, OTG_IN	5 V synchronous boost supply, flash driver supply in torch mode, MVS switches input, OTG switch input	-0.5	6	V
VPH_PWR	Handset power-supply voltage	-0.5	+6.0	V
VDD_xx	PMIC power-supply voltages not listed elsewhere	-0.5	+6.0	V
VBAT, VBAT_SNS	Main-battery voltage Steady state Transient (< 10 ms)	 -0.5 -0.5	 +6.0 +7.0	 V V
Signal pins				
V_IN	Voltage on any non-power-supply pin [1]	-0.5	V_{XX} + 0.5	V
ESD protection and thermal conditions – see Section 7.1.				

1. V_{XX} is the supply voltage associated with the input or output pin to which the test voltage is applied.

3.2 Recommended operating conditions

Operating conditions include parameters that are under the control of the user: power-supply voltage and ambient temperature (Table 3-2). The PM8941 meets all performance specifications listed in Section 3.3 through Section 3.11 when used within the recommended operating conditions, unless otherwise noted in those sections (provided the absolute maximum ratings have never been exceeded).

Table 3-2 Recommended operating conditions

Parameter		Min	Typ	Max	Units
Power-supply and related sense voltages					
USB_IN	Input power from USB source	4.35	–	28	V
DC_IN	Input power from wall charger	4.35	–	10	V
DC_IN_OVP_SNS	Input power sense pin for wall charger	4.35	–	28	V
VCHG, VCHG_SNS, VDD_FLASH	Charger input voltage, sense pin, flash driver supply in flash mode	4.35	–	10	V
VREG_5V, VDD_TORCH, VIN_5VS, OTG_IN	5 V synchronous boost supply, flash driver supply in torch mode, MVS switches input, OTG switch input.	–	5.0	–	V
VPH_PWR	Handset power-supply voltage [1]	2.5	3.6	4.5	V
VDD_MSM_IO	Pad voltage for digital I/Os to/from the IC	1.75	–	1.85	V
VDD_xx	PMIC power-supply voltages not listed elsewhere [1]	2.5	3.6	4.5	V
VBAT, VBAT_SNS	Main-battery voltage [1]	2.5	3.6	4.5	V
VCOIN	Coin-cell voltage	2.0	3.0	3.3	V
Signal pins					
V_IN	Voltage on any non-power-supply pin [2]	0	–	V_{XX} + 0.5	V
Thermal conditions					
T_A	Ambient temperature	-30	+25	+85	°C
T_J	Junction temperature	-30	+25	+125	°C

1. Specified range accommodates *low-voltage* lithium batteries on the low end, and *high-voltage* lithium batteries on the high end.
2. V_{XX} is the supply voltage associated with the input or output pin to which the test voltage is applied.

3.3 DC power consumption

This section specifies DC power-supply currents for the various IC operating modes (Table 3-3). Typical currents are based on IC operation at room temperature (+25°C) using default parameter settings.

Table 3-3 DC power-supply currents

Parameter		Comments	Min	Typ	Max	Units
I_BAT1	Supply current, active mode [1]		–	3.7	6.0	mA
I_BAT2	Supply current, sleep mode [2]					
	32 kHz XTAL clock		–	110	220	µA
	19.2 MHz XO clock		–	235	320	µA
I_BAT3	Supply current, off mode [3]		–	7	24	µA
I_SHIP	Ship mode current [4]		–	7	24	µA
I_COIN	Coin-cell supply current, off mode [5]					
	XTAL on		–	6	12	µA
	XTAL off		–	5	11	µA
	RC calibration	Average current	–	7	14	µA
I_CHG	External supply current [6]	Sleep mode	–	13.3	15.0	mA
I_USB	USB charger current in suspend [7]	Good battery, not charging	–	–	1.65	mA

1. I_BAT1 is the total supply current from the main battery with the PMIC on, crystal oscillators on, XO_OUT_D0 on at 19.2 MHz, driving no load, XO_OUT_A0 on at 19.2 MHz, driving no load, and these voltage regulators on with no load at the following: VREG_S1 = 1.25V, VREG_S2 = 2.1 V, VREG_S3 = 1.8 V, VREG_L1 = 1.225 V, VREG_L4 = 1.225 V, VREG_L5 = 1.74 V, VREG_L6 = 1.8 V, VREG_L7 = 1.74 V, VREG_L8 = 1.8 V, VREG_L9 = 2.85 V, VREG_LDO12 = 1.8 V, VREG_14 = 1.8 V, VREG_LDO15 = 2.05 V, VREG_L16 = 2.7 V, MPP1 = 1.25 V (Analog Out), MPP3 = 1.25 V (Analog (Out), VREF_LPDDR_CA = 0.5 * (VREG_L1), VREG_LPDDR_DQ = 0.5 * (VREG_L1).
2. I_BAT2 is the total supply current from the main battery with the PMIC on, either the 32 kHz XTAL oscillator or the XO oscillator on, these voltage regulators on with no load and low-power mode enabled: VREG_S1 = 1.225 V, VREG_S3 = 1.8 V, VREG_L1 = 1.225 V (bypass mode), MPP1 = 1.225 V (Digital Out). All other regulators are off, XO buffer off, and all XO_EN signals are low. MBG in low-power mode
3. I_BAT3 is the total supply current from the main battery with the PMIC off and the 32 kHz crystal oscillator on. This only applies from -30°C to +60°C.
4. I_SHIP is the total supply current from the main battery with the PMIC off, the 32 kHz crystal oscillator off and PMIC configured to ship mode. In ship mode VPH_PWR is isolated from VBAT. This specification only applies from -30°C to +60°C.
5. I_COIN is the total supply current from a 3.0 V coin cell with the PMIC off and the following conditions:
   – 32 kHz crystal oscillator on (only applies from -30°C to +60°C).
   – 32 kHz crystal oscillator off (only applies from -30°C to +60°C).
   – 32 kHz crystal oscillator off and RC calibration enabled with nominal settings (only applies from -30°C to +60°C, and does not include the peak currents when RC calibration is performed).
6. I_CHG is the total supply current from the charger with the PMIC in its sleep mode (see note 2), VCHG at 7 V, and CHG_VDD_MAX setting at 4.2 V.
7. I_USB is the total supply current from a USB charger when the phone has a good battery (>3.2 V, not being charged). During USB suspend, current from a PC is limited to 2.5 mA. The specified I_USB value allows 850 µA for external components connected to VBUS during suspend.

3.4 Digital logic characteristics

PM8941 digital I/O characteristics such as voltage levels, current levels, and capacitance are specified in Table 3-4.

Table 3-4 Digital I/O characteristics

Parameter		Comments [4]	Min	Typ	Max	Units
V_{IH}	High-level input voltage		0.65 · V_{IO}	–	V_{IO} + 0.3	V
V_{IL}	Low-level input voltage		-0.3	–	0.35 · V_{IO}	V
V_{SHYS}	Schmitt hysteresis voltage		15	–	–	mV
I_L	Input leakage current [1]	V_{IO} = max, V_{IN} = 0 V to V_{IO}	-0.20	–	+0.20	µA
V_{OH}	High-level output voltage	I_{out} = I_{OH}	V_{IO} - 0.45	–	V_{IO}	V
V_{OL}	Low-level output voltage	I_{out} = I_{OL}	0	–	0.45	V
I_{OH}	High-level output current [2]	V_{out} = V_{OH}	3	–	–	mA
I_{OL}	Low-level output current [2]	V_{out} = V_{OL}	–	–	-3	mA
I_{OH_XO}	High-level output current [2]	XO digital clock outputs only	6	–	–	mA
I_{OL_XO}	Low-level output current [2]	XO digital clock outputs only	–	–	-6	mA
C_{IN}	Input capacitance [3]		–	–	5	pF

1. MPP and GPIO pins comply with the input leakage specification only when configured as a digital input or set to the tri-state mode.
2. Output current specifications apply to all digital outputs unless specified otherwise, and are superseded by specifications for specific pins (such as MPP and GPIO pins).
3. Input capacitance is guaranteed by design, but is not 100% tested.
4. V_{IO} is the supply voltage for the MSM™/PM IC interface (most PMIC digital I/Os).

3.5 Input power management

All parameters associated with input power management functions are specified.

3.5.1 Over-voltage protection

The two external voltage sources (USB_IN and DC_IN) are continuously monitored; the following functional description applies to both. If the sensed voltage is more than about 2 V, the OVP circuits are automatically enabled. Once the circuits are enabled, if the sensed voltage is less than VMAX (10.5 V nominal), the OVP FET driver causes the *switch* to close, thereby connecting the external supply voltage to the OVP_OUT node. If the voltage exceeds VMAX, the OVP FET driver immediately opens the *switch* to protect the OVP_OUT node. OVP_OUT is connected to the switched-mode battery charger supply voltage (VCHG), so the charger is protected as well.

3.5.2 External supply detection

The PMIC continually monitors the external supply voltages such as USB_IN, DC_IN, and VCHG, and the handset supply voltage (at VPH_PWR). Internal detector circuits measure these voltages to recognize when an external supply is connected or removed, and verify that it is within its valid range when connected. Hysteresis prevents undesired switching near the thresholds, and status is reported to the on-chip state machine and to the modem IC via interrupts.

Performance specifications related to detecting external supply voltages and protecting the PMIC are presented in Table 3-5.

Table 3-5 External source interface performance specifications

Parameter		Comments	Min	Typ	Max	Units
Negative voltage protection						
V_NEG	Negative input voltage	USB_IN, DC_IN_OVP_SNS	–	–	-0.3	V
Undervoltage detection (UVD)						
V(thr_coarse)	Coarse detect threshold	USB_IN, DC_IN_OVP_SNS – rising	1.4	1.7	2.0	V
V(thr_uvd_r) [1]	UVD threshold	USB_IN, DC_IN_OVP_SNS – rising	4.25	–	4.55	V
V(thr_uvd_f) [2]	UVD threshold	USB_IN, DC_IN_OVP_SNS – falling	4.05	–	4.35	V
V(acc_uvd)	UVD threshold accuracy	USB_IN, DC_IN_OVP_SNS	100	–	100	mV
V(hyst_uvd)	UVD threshold hysteresis	USB_IN, DC_IN_OVP_SNS	150	200	250	mV
Overvoltage detection (OVD)						
V(thr_ovd_r)	OVD programmable setting [3]	USB_IN, DC_IN_OVP_SNS – rising	9.5	10.5	11	V
V(acc_ovd)	OVD threshold accuracy [4]	USB_IN, DC_IN_OVP_SNS	-2	–	+2	%
V(hyst_ovd)	OVD threshold hysteresis	USB_IN, DC_IN_OVP_SNS – falling	150	200	250	mV
t(db_ovd_r)	OVD debounce	USB_IN, DC_IN_OVP_SNS – rising	–	0.4	1	µs
t(db_ovd_f)	OVD debounce	USB_IN, DC_IN_OVP_SNS – falling	–	40	–	ms
t(fet_off)	OVP FET turnoff time		–	1	3	µs
R(ds_on_usb_ovp)	UBS OVP FET Rds(on)	USB_IN = 5 V	–	190	270	mΩ
R(ds_on_dc_ovp)	DC OVP FET Rds(on)	DC_IN = 5 V	–	130	180	mΩ
Recommended OVP output (SMBC input)						
VCHG	Charger input voltage [5]		4.35	–	6.5	V

1. Meets the 4.4 V VBUS minimum from an unloaded bus-powered hub, as specified in the USB 2.0 specification. Default value is 4.25 V. Programmable in 0.1 V steps.
2. Meets the 4.1 V VBUS minimum undershoot, as specified in the USB BC 1.1 specification. Default value is 4.05 V. Programmable in 0.1 V steps. Default value is 10.5 V.
3. Programmable in 0.5 V steps.
4. After the PMIC poweron sequence is completed.
5. This is the recommended operating range. The acceptable operating range is defined by the UVD and OVD thresholds specified earlier in this table.

3.5.3 Switched-mode battery charger

3.5.3.1 SMBC specifications that are not charging-specific

Table 3-6 SMBC specifications (not charging-specific)

Parameter	Comments	Min	Typ	Max	Units
Battery/VDD voltage programmable range	10 mA steps, 3.6 V default	3.24	4.2	4.5	V
Battery/VDD voltage accuracy	Including line and load regulation	-0.5	–	0.5	%
	Including line/load regulation and temp variation	-1	–	1	%
Battery charge-current programmable range	50 mA steps, 300 mA default	200	1000	3000	mA
Battery charge-current accuracy		-5% - 50 mA	–	+5% + 50 mA	
Input voltage-limit programmable range	50 mV steps, low range	4.2	4.3	5.5	V
	200 mv steps, high range	5.6	–	9.6	V
Input voltage-limit accuracy		-2	–	2	%
USB_IN / DC_IN input current Programmable range [1] (USB_IN default = 100 mA, DC_IN default = 500 mA)	100 mA steps	100	–	2500	mA
DC_IN, USB_IN input current limit accuracy	Iin = setting				
Current limit < 1500 mA [1]		0.9 * Iin	0.95 * In	Iin	mA
Current limit > 1500		0.93 * Iin	0.98 * Iin	1.03 * Iin	mA
Rated output (VDD) current	Continuous	–	3	–	A
Switching frequency (F_{SW})	3.2 MHz default	1.6	–	3.2	MHz
SMPS efficiency [2]					
USB_IN = 5 V, VPH_PWR = 3.6 V	100 mA output current	–	80	–	%
	500 mA output current	–	90	–	%
	1 A output current	–	88	–	%
	2.5 A output current	–	90	–	%
DC_IN = 5 V, VPH_PWR = 3.6 V	100 mA output current	–	78	–	%
(includes external DC OVP FET loss)	500 mA output current	–	90	–	%
	1 A output current	–	89	–	%
	2.5 A output current	–	80	–	%
USB_IN in parallel with DC_IN at 5 V	100 mA output current	–	82	–	%
VPH_PWR = 4.2 V	500 mA output current	–	91	–	%
	1 A output current	–	90	–	%
	2.5 A output current	–	82	–	%
PFET Rds(on)		–	95	135	mΩ
NFET Rds(on)		–	110	155	mΩ
VBAT_DET low comparator threshold programmable range	20 mV steps, 4.1 V default	3.3	4.1	4.7	V

Table 3-6 SMBC specifications (not charging-specific) (cont.)

Parameter	Comments	Min	Typ	Max	Units
VBAT_DET low comparator threshold accuracy		-30	–	30	mV
VBAT_DET low comparator debounce	For battery recharge	–	1	–	s
	For battery overvoltage	–	1	–	µs
VBAT_DET high comparator		–	VBAT_DET low + 5%	–	V
Battery charge termination	17.28 mA steps, 207 mA default, end of charge done by BMS	35	–	276	mA
Reverse boost mode voltage	50 mV steps	4.2	5	5.5	V
Reverse boost mode current	Rbat = 150 mΩ, Vout = 4 V Vbat > 3.55 V (adaptive mode)	–	–	2	A
	Rbat = 150 mΩ, Vout = 4 V Vbat > 3.55 V (fixed mode)	–	–	1	A
Efficiency in reverse boost mode					
VBAT = 3.6 V, Vout = 4 V	500 mA output current	–	92	–	%
(adaptive mode)	1 A output current	–	89	–	%
	2 A output current	–	90	–	%
VBAT = 3.6 V, Vout = 5 V	500 mA output current	–	92	–	%
(fixed output)	1 A output current	–	89	–	%
	2 A output current	–	90	–	%
Overvoltage protection in reverse boost mode	200 mV step, 5.6 V default	5.6	–	7	V

1. The 100 mA current input limit on the USB path is applicable during FLCB. Once this current limit is changed to a higher value during USB enumeration, it may not be changed back to 100 mA.
2. Figure 3-1 shows the SMBB efficiency plot at VBAT = 3.6 V and USB_IN = 5 V.

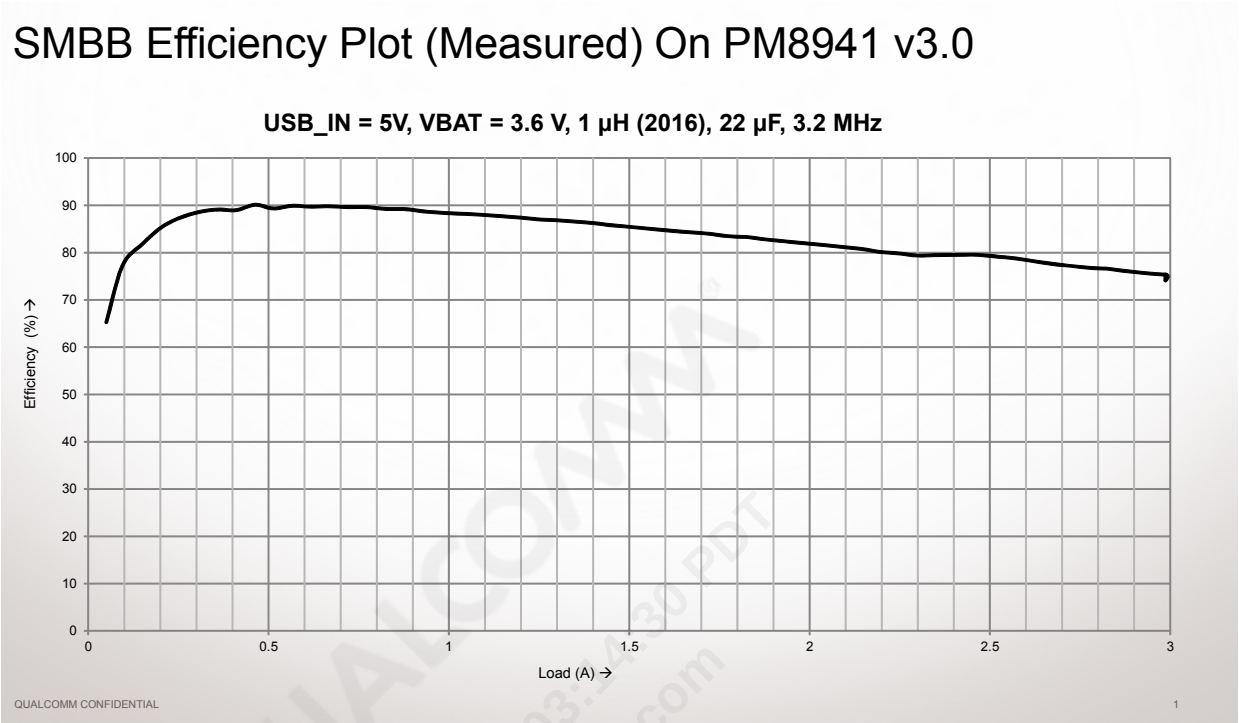


Figure 3-1 SMBB efficiency plot on the PM8941 device

3.5.3.2 Charging-specific SMBC specifications

Battery charging is controlled by a PMIC state-machine. The first step in the automated charging process determines if trickle charging is needed. Charging of a *severely* depleted battery must begin with trickle charging (Table 3-7) to limit the current, to avoid pulling VDD down, and to protect the battery from more charging current than it can handle. Once a minimum battery voltage is established using trickle charging, constant-current charging is enabled to charge the battery quickly – this mode is sometimes called fast charging. Once the battery approaches its target voltage, the charge is completed using constant-voltage charging.

Table 3-7 Trickle charging performance specifications

Parameter	Comments	Min	Typ	Max	Units
Trickle charge-current programmable range	10 mA steps, 50 mA default	50	–	200	mA
Trickle charge-current accuracy		-10% - 5 mA	–	10% + 5 mA	
Trickle voltage-threshold programmable range	50 mV steps, 2.8 V default	2.05	–	2.80	V
Trickle voltage-threshold accuracy		-50	–	50	mV
Trickle voltage - threshold hysteresis	VBAT falling	175	200	225	mV
Trickle voltage - threshold debounce		–	1	–	sec
System weak threshold programmable range (programmable in 100 mV steps; 3.2 V default)	Detect depleted battery	2.1	3.2	3.6	V
System weak threshold accuracy		-50	–	50	mV
System weak threshold falling hysteresis	VBAT falling	15	20	25	mV

Table 3-7 Trickle charging performance specifications

Parameter	Comments	Min	Typ	Max	Units
System weak threshold debounce		–	1	–	sec
Trickle fault voltage	Fixed threshold	3.65	3.7	3.75	V
Trickle fault voltage hysteresis	VBAT falling	15	20	25	V
Trickle fault voltage debounce		–	3	–	µs

Table 3-8 Battery FET and charge pump specifications

Parameter	Comments	Min	Typ	Max	Units
Battery FET					
Battery FET Rds,on (pin-to-pin)	VBAT = 2.5 V to 4.5 V, TJ = -30°C to 125°C	–	15	25	mΩ
Intrinsic battery FET Rds,on [1]	VBAT = 2.5V to 4.5V, TJ = -30°C to 125°C	9.35	10	10.65	mΩ
Intrinsic battery FET Rds,on variation [2] (VBAT = 2.5 V to 4.5 V, TJ = -30°C to 125°C)	IBAT = -2A to 2A IBAT = -3 A to 3A	-2 -3	– –	+2 +3	% %
PFET pull-up Rds,on [3]	BF_PDRV = 1, default BF_PDRV = 0	– –	8.5 30	– –	Ω Ω
Battery FET current	Continuous Peak (10% duty cycle)	– –	– –	4 6	A A
Battery FET leakage current [4]	BAT FET off, VPH_PWR = 4.2 V, VBAT = 0 V **Or** BAT FET off, VPH_PWR = 0 V, VBAT = 4.2 V	–	0.1	80	µA
Battery FET charge pump					
Charge pump output voltage (VBFCP_DRV) [5]	BATFET on, Rds(on) regulation loop on	VBAT+ 2.0	–	VBAT+ 6.0	V
	Battery FET OFF	–	VBAT	–	V
Charge pump quiescent Current [6]	NPM	–	110	135	µA
	LPM	–	50	65	µA
	Ultra LPM	–	0.1	–	µA

1. This initial Rds(on) error can be calibrated out by BMS.
2. This is the Rds(on) variation over temperature, supply voltage, and current with the Rds(on) regulation loop on.
3. The battery FET does not have a body diode from VBAT to VPH_PWR. Instead, in parallel with the battery FET is an integrated PFET that acts a pull-up between VBAT and VPH_PWR when the PMIC is off and in ultra LPM mode. PFET Rds(on) measured with 10 mA load on VPH_PWR.
4. Worst case measured at TJ = 60°C.
5. If Rds(on) regulation loop is off, VBFCP_DRV = 4.5 V - 6.0 V programmable, 0.5 V steps.
6. BAT FET power modes:
   NPM: NFET on, 600 kHz CP clock, CNST_RDS loop on, BAT FET Rds(on) = 10 mΩ
   LPM: NFET on, 600 kHz CP clock, CNST_RDS loop off, BAT FET Rds(on) = 6~20 mΩ
   Ultra LPM: NFET off, PFET on, BAT FET Rds(on) = 8.5 Ω

Constant-current charging

The PMIC parameters associated with constant-current charging are specified in the following subsections:

- External supply voltages Section 3.5.2
- Battery voltage detector Section 3.5.4

Additional performance specifications for constant-current charging are not required.

Constant-voltage charging

The PMIC parameters associated with constant-voltage charging are specified in the following subsections:

- External supply voltages Section 3.5.2
- Battery voltage detector Section 3.5.4

Additional performance specifications for constant-voltage charging are not required.

3.5.3.3 Charging flow diagram

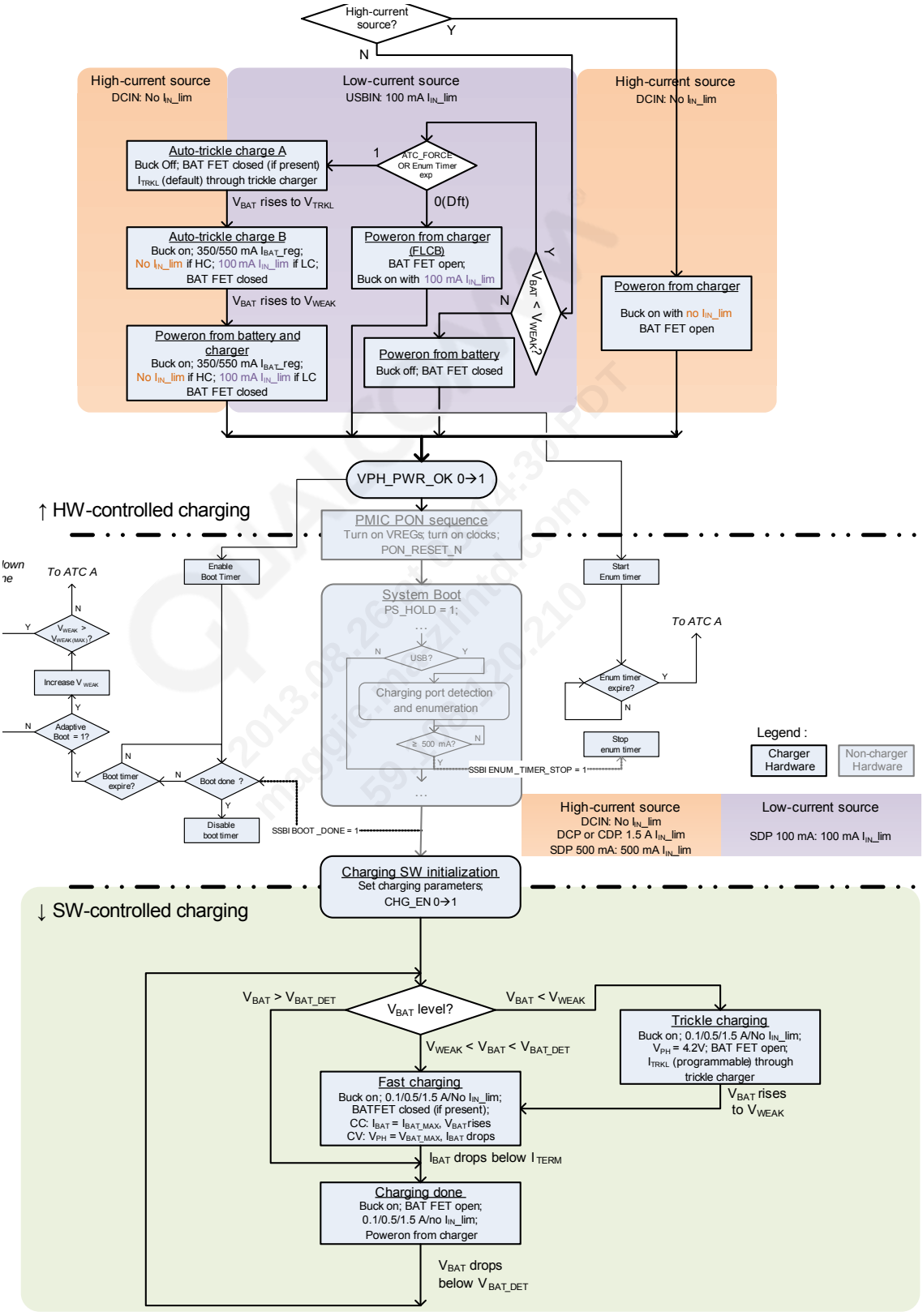


Figure 3-2 SMBC main-battery charging operation

3.5.3.4 SMBC exception handling

Table 3-9 SMBC exception handling

Exception event	Description	Condition	Battery charging	VPH_PWR source	Buck	Trickle charger	BAT FET	T_{TRKL} and T_{CHG}	T_{CHG_WD}
No exception (baseline)	Everything OK, actively charging		Run	Charger	B or T		On/closed	Run	Run
Charging complete			Stop	Charger	On	Off	Off/open	Stop	Stop
Adapter interface									
Charger not OK	No valid charging source – VCHG is unattached or out-of-range.		Stop	Battery	Off	Off	On/closed	Stop	Stop
USB suspended	USB port suspended by host; no more than 2.5 mA can be drawn (from PC).		Stop	Battery	Off	Off	On/closed	Stop	Stop
Battery interface									
Battery unattached	Battery presence detection circuit indicates that the battery is missing.		Stop	Charger	On	Off	Off/open	Rest	Stop
Battery temp not OK	Battery temperature monitoring circuit indicates that the battery is hot or cold.		Stop	Charger	On	Off	Off/open	Stop	Run
		In HW-Ctrl ATC	Stop	N/A	Off	Off	On/closed	Run	Stop

Table 3-9 SMBC exception handling (cont.)

Exception event	Description	Condition	Battery charging	VPH_PWR source	Buck	Trickle charger	BAT FET	T_{TRKL} and T_{CHG}	T_{CHG_WD}
Switch-mode charging control									
Charger temp too high	The SMBC buck or trickle charger temperature exceeds the limit.	In HW-Ctrl ATC	Stop	None	Off	Off	On/closed	Run	Stop
		In SW-Ctrl trickle chg	Stop	Charger	On	Off	Off/open	Stop	Run
		In SW-Ctrl fast chg	Stop	Battery	Off	Off	On/closed	Stop	Run
Charging disabled	SW disables charger via SPMI.		Stop	Charger	Off	Off	Off/open	Stop & rest	Stop
Charging paused	SW pauses battery charging via SPMI.		Stop	Charger	On	Off	Off/open	Stop	Run
T_{TRKL} expired	Trickle-charging timer expires.		Stop	Charger	On		Off/open	Stop	Stop
T_{CHG} expired	Maximum-charging timer expires.		Stop	Charger	On		Off/open	Stop	Stop
T_{CHG_WD} expired	Charging SW not responding, causing charger WD timer to expire.		Stop	Charger	On		Off/open	Stop	Stop
VTRKL_FAULT	VBAT rises above V_{TRKL_FAULT} during trickle charging.		Stop	Charger	On		Off/open	Stop	Stop
PMIC infrastructure									
VPH_PWR_EN goes low	PON module requests the charger **not** to bring up VDD.		Stop	Off	Off		Off/open	Stop & rest	Stop
PON not OK	PON module gets stuck in the powerup sequence, or the modem IC fails to raise PS_HOLD.		Stop	Charger	On		Off/open	Stop	Stop
CRIT_SHTDWN	MBG not OK, or PMIC over-temperature stage 2 occurred.	In HW-Ctrl ATC	Stop	Off			Off/open	Stop & rest	Stop
		Not in ATC	Stop						Stop

3.5.4 Battery voltage monitoring system

3.5.4.1 Under-voltage lockout

The handset supply voltage (VDD) is monitored continuously by a circuit that automatically turns off the device at severely low VDD conditions. This programmable UVLO threshold is even lower than the low-battery alarm threshold defined in Section 3.5.4.1.

UVLO events do not generate interrupts. They are reported to the modem IC via the PON_RESET_N signal. UVLO-related voltage and timing specifications are listed in Table 3-10.

Table 3-10 UVLO performance specifications

Parameter	Comments	Min	Typ	Max	Units
Rising threshold voltage [1]	Programmable value, 50 mV steps	1.675	2.725	3.225	V
Hysteresis [1]	175 mV setting	125	175	225	mV
	300 mV setting	250	300	350	mV
Falling threshold voltage [2]	175 mV hysteresis setting	1.500	2.550	3050	V
	300 mV hysteresis setting	1.375	2.425	2.925	V
UVLO detection interval		-	1	-	µsec

1. Default UVLO rising threshold is 2.725 V and hysteresis is 175 mV. For handset application, the UVLO rising threshold and hysteresis are reconfigured in SBL to 2. 775 V and 300 mV respectively
2. The UVLO rising threshold is programmable. UVLO falling threshold = UVLO rising threshold - UVLO hysteresis. For a default UVLO rising threshold setting of 2.725 V and hysteresis setting of 175 mV, the UVLO falling threshold is 2.550 V.

3.5.4.2 SMPL

The PMIC SMPL feature initiates a poweron sequence if the monitored VDD drops out of range, and then returns in-range within a programmable interval. When enabled by software, SMPL achieves immediate and automatic recovery from momentary power loss (such as a brief battery disconnect when the phone is jarred).

SMPL performance specifications are given in Table 3-11.

Table 3-11 SMPL performance specifications

Parameter	Comments	Min	Typ	Max	Units
Minimum SMPL interval [1]	Programmable range	0.5	–	2.0	s

1. SMPL interval assumes that SMPL timer is triggered by pon_rb as defined in SLEEP_CLK1_SMPL_CTL1 register of 80-NA555-2. Valid SMPL time settings are: 0.5, 1.0, 1.5, and 2.0 seconds. A capacitor with effective capacitance of at least 10 µF is required to support SMPL interval of 2 sec.

3.5.4.3 Voltage collapse protection (VCP)

To prevent a sudden load from inadvertently collapsing VDD when a low-current charger is used, the PMIC monitors the voltage across the battery MOSFET and automatically turns it on if VDD drops about 60 mV below VBAT.

Performance specifications related to voltage collapse protection are given in Table 3-12.

Table 3-12 Voltage collapse protection (VCP) performance specification

Parameter	Comments	Min	Typ	Max	Units
VCP detection comparator offset (VBAT - VPH_PWR)	PMIC enters VCP, protection interrupt triggers	20	60	100	mV
VCP activation time [1]	VBAT > VWEAK (3.2 V)	–	–	5	µs
VPH_PWR voltage dip below VBAT upon VCP [2]		–	–	200	mV
Charger to battery switch-over time [3]	VBAT > VWEAK (3.2 V), 2 A system load	–	–	10	µs
VPH_PWR voltage dip below VBAT upon charger to battery switchover	VBAT > VWEAK (3.2 V), 2 A system load	–	–	200	mV

1. VCP Activation Time is defined as the time from VCP_DET comparator output rising to V_{BFCP_DRV} rises to VBAT + 0.75 V.
2. USB_IN = 5 V, IUSB_MAX = 500 mA, VPH_PWR = 3.6 V, VBAT = 3.4 V, BATFET open; system current rises from 100 mA to 2.0 A in 20 µs; C_{BAT} = 10 µF, C_{VPH_PWR} = 200 µF (100 µF at PMIC, 100 µF at GSM PA).
3. Charger to battery switch-over time is defined as the time from charger removal (as detected by PMIC) to VBFCP_DRV rising to VBAT + 0.75 V.

3.5.5 Battery monitoring system (BMS)

Table 3-13 Battery fuel gauge specifications

Parameter	Comments	Min	Typ	Max	Units
Resolution on battery current measurement	Battery peak current = 2 A; sense resistor = 25 mΩ	–	16	–	bits
Resolution on battery voltage measurement		–	15	–	bits
Battery current range		-4	–	4	A
Input referred offset		–	–	50	µV
OCV measurement [1]					
Accuracy		-15	–	15	mV
Repeatability	With charger attached	-8	–	8	mV

Table 3-13 Battery fuel gauge specifications

Parameter	Comments	Min	Typ	Max	Units
IADC accuracy [1]					
Using internal battery FET					
0.1 A discharge	Average and instantaneous current, no charger attached	-5	–	5	%
1 A discharge	Average and instantaneous current, no charger attached	-3	–	3	%
0.1 A charge	Average current	-5	–	5	%
	Instantaneous current (charger switching causes short-term errors up to 30 mA)	-30	–	30	%
1A charge	Average current	-3	–	3	%
	Instantaneous current (charger switching causes short-term errors up to 30 mA)	-6	–	6	%
	Instantaneous and average current near charger CC-CV transition	-20	–	20	%
End of Charge (EoC)	When BATFET is open, current should be 0 mA, but IADC readings up to 30 mA can occur	-30	–	30	mA
Using external Rsense					
0.1 A discharge	Instantaneous and average current, no charger attached	-4	–	4	%
1 A discharge	Instantaneous and average current, no charger attached	-2	–	2	%
0.1 A charge	Average current	-4	–	4	%
	Instantaneous current (charger switching causes short-term errors up to 30 mA)	-30	–	30	%
1 A charge					
	Average current	-2	–	2	%
	Instantaneous current (charger switching causes short-term errors up to 30 mA)	-5	–	5	%
End of Charge (EoC)	When BATFET is open, current should be 0 mA, but IADC readings up to 30 mA can occur	-30	–	30	mA

1. Valid over a temperature range of -20°C to 70°C and a voltage range of 3.2 V to 4.35 V.

3.5.5.1 State of Charge (SoC) specifications

Table 3-14 State of Charge specifications

Parameter	Comments	Typ[1]	Max[2]	Units
SOC accuracy at power on				
Battery capacity > 80% or < 20%)	SOC accuracy immediately after powering on with settled battery with capacity > 80% or < 20%	±0.5	±3	%
Battery capacity between 20% and 80%	SOC accuracy immediately after powering on with settled battery with capacity between 20% and 80%	±3	±15	%
SOC accuracy after power on				
Battery capacity > 80% or < 20%)	SOC accuracy at any time during a charge or discharge cycle after powering on with settled battery with capacity > 80% or < 20%	±4	±9	%
Battery capacity between 20% and 80%	SOC accuracy at any time during a charge or discharge cycle after powering on with settled battery with capacity between 20% and 80%	±7	±20	%

1. Valid at 25°C.
2. Valid over a temperature range of -20°C to 70°C.

3.5.6 Battery temperature monitoring (BTM) and battery presence detection (BPD) specifications

If BAT_ID is not used, that pin can be grounded. If BAT_THERM is not used, it too can be grounded, and the software's battery temperature feature ***must be*** disabled.

Battery interface specifications are given in Table 3-15.

Table 3-15 Battery interface specifications

Parameter	Comments	Min	Typ	Max	Units
Battery-temperature monitoring					
Cold-comparator threshold programmable settings	Fraction of VREF_BAT, selectable as 70% or 80%	70	–	80	%
Cold-comparator offset		-20	–	20	mV
Cold-comparator voltage hysteresis	VREF_BAT falling (battery warming)				
70% setting		-100	–	-50	mV
80% setting		-90	–	-54	mV
Cold-comparator debounce	VREF_BAT rising or falling	1	–	2	s
Hot-comparator threshold programmable settings	Fraction of VREF_BAT	25	–	35	%
Hot-comparator offset		-20	–	20	mV

Table 3-15 Battery interface specifications (cont.)

Parameter	Comments	Min	Typ	Max	Units
Hot-comparator voltage hysteresis	VREF_BAT failing (battery cooling)				
35% setting		25	–	50	mV
25% setting		15	–	35	mV
Hot-comparator debounce	VREF_BAT rising or falling	1	–	2	s
Battery presence detection (BPD)					
BPD-comparator threshold	Fraction of VREF_BAT	–	95	–	%
BPD-comparator offset		-50	–	50	mV
BPD-comparator debounce					
VREF_BAT rising (battery removal)		1	–	3	µs
VREF_BAT falling (battery insertion)		–	1	–	s

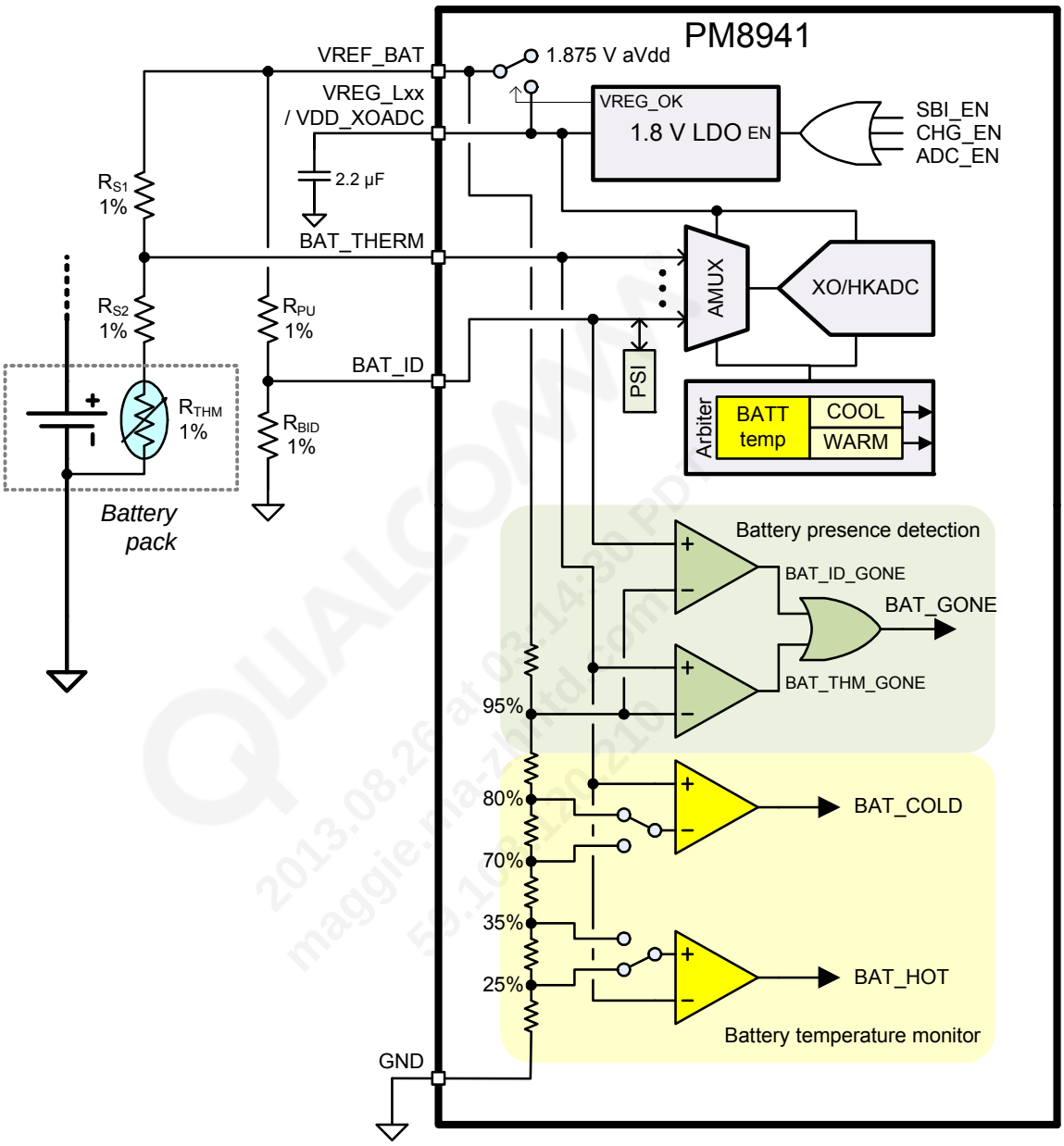


Figure 3-3 Battery temperature monitoring

Table 3-16 BTM calculations

Battery charging window	BTM comparator thresholds	Min
0ºC to 40/45ºC	70%/35%	Rs1 = 39(Rcold - Rhot)/70 Rs2 = (3Rcold -13Rhot)/10
-10ºC to 60ºC	80%/25%	Rs1 = 3(Rcold - Rhot)/11 Rs2 = (Rcold -12Rhot)/11

3.5.7 Coin-cell charging

Coin-cell charging is enabled through software control and powered from VBAT. The on-chip charger is implemented using a programmable voltage source and a programmable series resistor. The modem IC reads the coin-cell voltage through the PMIC's analog multiplexer to monitor charging. Coin-cell charging performance is specified in Table 3-17.

Table 3-17 Coin-cell charging performance specifications

Parameter	Comments	Min	Typ	Max	Units
Target regulator voltage [1]	V_{IN} > 3.3 V, I_{CHG} = 100 µA	2.50	3.10	3.20	V
Target series resistance [2]		800	–	2100	Ω
Coin-cell charger voltage error	I_{CHG} = 0 µA	-5	–	+5	%
Coin-cell charger resistor error		-20	–	+20	%
Dropout voltage [3]	I_{CHG} = 2 mA	–	–	200	mV
Ground current, charger enabled	PMIC = off; VCOIN = open				
VBAT = 3.6 V, T = 27ºC		–	4.5	–	µA
VBAT = 2.5 to 5.5 V		–	–	8	µA

1. Valid regulator voltage settings are 2.5, 3.0, 3.1, and 3.2 V.
2. Valid series resistor settings are 800, 1200, 1700, and 2100 Ω.
3. Set the input voltage (VBAT) to 3.5 V. Note the charger output voltage; call this value V_0. Decrease the input voltage until the regulated output voltage (V_1) drops 100 mV ($V_1 = V_0 – 0.1$ V). The voltage drop across the regulator under this condition is the dropout voltage ($V_{dropout} = VBAT – V_1$).

3.6 Output power management

Output power management circuits include:

- Bandgap voltage reference circuit
- 5 V boost SMPS circuit
- Buck SMPS circuits
- LDO linear regulators
- Voltage switches

The PM8941 is supplemented by the PM8841 to provide all the regulated voltages needed for most wireless handset applications. Independent regulated power sources are required for various electronic functions to avoid signal corruption between diverse circuits, to support power-management sequencing, and to meet different voltage-level requirements.

A total of 28 programmable voltage regulators are provided by the PM8941, with all outputs derived from a common bandgap reference circuit. Each regulator can be set to a low-power mode for power savings.

A high-level summary of all regulators and their intended uses is presented on the next two pages.

Table 3-18 Regulators and their intended uses

Function	Circuit type	Default voltage (V)[7]	Specified range (V)	Programmable range (V)	Rated current (mA)	Default on[7]	Expected use
S1	HF-SMPS	1.300	1.200 – 1.500	0.375 – 3.050	2000	Y	Source for L1 & L3, L4 & L11; external connections
S2	HF-SMPS	2.150	1.800 – 2.300	0.375 – 3.050	1000	Y	WCD plus source for L5 & L7, L6 & L12 & L14 & L15; external connections
S3 [1]	HF-SMPS	1.800	1.750 – 1.850	0.375 – 3.050	2000	Y	Modem IC pad group 3, option 4 & 7; L2 and LVS; chipset and other I/Os
S4 or '5V' [2]	Boost SMPS	5.000	4.500 – 5.200	4.000 – 5.500	1300	–	WCD speaker driver & source for 5VS1, 5VS2; option for keypad, RGB drivers
L1	NMOS LDO	1.225	1.200 – 1.250	0.750 – 1.525	1200	Y	Modem IC pad group 1, option 4, & 7; DDR memory; eMMC
L2	NMOS LDO	1.200	1.100 – 1.450	0.750 – 1.525	300	–	MIPI_DSI - analog
L3	NMOS LDO	1.200	1.100 – 1.450	0.750 – 1.525	300	–	MIPI_CSI
L4	NMOS LDO	1.200	1.150 – 1.400	0.750 – 1.525	1200	–	RFIC low-V; modem IC analog low-V
L5 [3]	Low noise LDO	1.740	1.700 – 2.200	–	On-chip only	–	PMIC low noise XO buffers
L6 [4]	PMOS LDO	1.800	1.700 – 1.900	1.500 - 4.900	150	Y	USB; WCN XO; PMIC low power XO output buffers
L7 [3]	Low noise LDO	1.740	1.700 – 2.200	–	On-chip only	Y	PMIC XO circuits
L8 [4, 5]	PMOS LDO	1.800	1.700 – 1.900	1.500 – 4.900	50	Y	PMIC HKADC
L9	PMOS LDO	1.800	1.700 – 3.050	1.500 – 4.900	150	–	Modem IC pad group 5, dual-voltage UIM1 (1.8 / 2.95 V)
L10	PMOS LDO	1.800	1.700 – 3.050	1.500 – 4.900	150	–	Modem IC pad group 6, dual-voltage UIM2 (1.8 / 2.95 V)
L11	NMOS LDO	1.225	1.200 – 1.400	0.750 - 1.525	1200	–	WCN; modem IC ADC/DAC
L12	PMOS LDO	1.800	1.700 – 1.900	1.500 – 4.900	300	Y	Modem IC PLLs, MIPI_DSI, MIPI_CSI, HDMI, EDP; MIPI_DSI I/Os
L13	PMOS LDO	2.950	2.750 – 3.000	1.500 – 4.900	150	Y	Modem IC pad group 2

Table 3-18 Regulators and their intended uses (cont.)

Function	Circuit type	Default voltage (V)[7]	Specified range (V)	Programmable range (V)	Rated current (mA)	Default on[7]	Expected use
L14	PMOS LDO	1.900	1.700 – 2.100	1.500 – 4.900	150	–	Modem IC analog - high V
L15	PMOS LDO	2.050	2.000 – 2.100	1.500 – 4.900	600	–	RFICs - low voltage
L16	PMOS LDO	2.750	2.600 – 3.000	1.500 – 4.900	150	–	Qualcomm front-end, RF switches, GPS LNA
L17	PMOS LDO	2.800	2.700 – 3.000	1.500 – 4.900	300	–	3D cameras - analog
L18	PMOS LDO	2.850	2.400 – 3.300	1.500 – 4.900	300	–	Sensors; touchscreen
L19	PMOS LDO	2.900	2.600 – 3.300	1.500 – 4.900	600	–	WCN
L20 [6]	PMOS LDO	2.950	2.750 – 3.000	1.500 – 4.900	600	Y	eMMC memory
L21 [6]	PMOS LDO	2.950	2.750 – 3.000	1.500 – 4.900	600	Y	SD/MMC card
L22	PMOS LDO	3.000	2.600 – 3.300	1.500 – 4.900	300	–	MIPI_DSI1
L23	PMOS LDO	3.000	2.600 – 3.300	1.500 – 4.900	300	–	MIPI_DSI2 or MIPI_CSI
L24	PMOS LDO	3.075	3.000 – 3.300	1.500 – 4.900	50	Y	HS-USB high-voltage
LVS1	Low V switch	1.800	–	–	300	–	Sensors; touchscreen
LVS2	Low V switch	1.800	–	–	300	–	Available
LVS3	Low V switch	1.800	–	–	300	–	3D cameras
5VS1	5 V switch	5.000	–	–	500	–	USB-OTG
5VS2	5 V switch	5.000	–	–	55	–	HDMI

1. S3 powers internal circuitry, and must be kept at its default setting.
2. Rated current for S4, the 5V boost circuit, depends on the input voltage: 1.3 A for VDD = 3 V to 4.5 V and 600 mA for VDD = 2.5 V to 3 V.
3. VREG_L5 (VREG_RF_CLK) and VREG_L7 (VREG_XO) power RF buffers and XO circuits respectively and must be kept at their default settings.
4. L6 and L8 power internal circuits that are limited to 1.8 V operation; they should not exceed the maximum stated in their programmable ranges. L6 is used as the internal dVdd source after power-up; its programmed voltage should not be changed, and it should not be turned off.
5. L8 is controlled by BMS during power-on
6. L20 and L21 have been characterized for 800 mA peak current capability. These regulators meet all the specifications at 800 mA except a) Overshoot due to load transients (100 mV overshoot observed) b) Load regulation at high temperature, low voltage (at VBAT = 3 V and 90°C, load regulation is about 0.68 % for normal power mode).
7. All regulators have output voltage default settings. Default voltage and power-on state depends on PBS configurations.

3.6.1 Reference circuit

All PMIC regulator circuits, and some other internal circuits, are driven by a common, on-chip voltage reference circuit. An on-chip series resistor supplements an off-chip 0.1 µF bypass capacitor at the REF_BYP pin to create a lowpass function that filters the reference voltage distributed throughout the device.

NOTE Do not load the REF_BYP pin. Use an MPP configured as an analog output if the reference voltage is needed off-chip.

Applicable voltage reference performance specifications are given in Table 3-19.

Table 3-19 Voltage reference performance specifications

Parameter	Comments	Min	Typ	Max	Units
Nominal internal VREF	At REF_BYP pin	–	1.250	–	V
Output voltage deviations					
Normal operation	Over temperature only, -20 to +120ºC	-0.32	–	+0.32	%
Normal operation	All operating conditions	-0.50	–	+0.50	%
Sleep mode	All operating conditions	-1.00	–	+1.00	%

3.6.2 Boost SMPS

The boost switched-mode power supply (SMPS) is rated for 1300 mA output current, and is intended for generating +5 V to power circuits such as USB-OTG and HDMI (through the 5 V switches), speaker drivers, LED indicators, and lighting. Although rated for 1300 mA, higher currents are allowed; however, higher input voltages may be required, and some performance characteristics may become degraded, as indicated below.

The boost converter offers a low power mode to reduce its quiescent current during the phone's sleep mode. This mode uses pulse burst modulation (PBM). This mode should only be used when the phone is in its sleep mode. Pertinent performance specifications are listed in Table 3-20.

Table 3-20 Boost regulator performance specifications

Parameter	Comments [4, 5]	Min	Typ	Max	Units
Rated current (I_rated)					
VDD = 4.2 V to 4.5 V		–	–	1300	mA
VDD = 3.6 V to 4.2 V		–	–	1200	mA
VDD = 3.0 V to 3.6 V		–	–	900	mA
VDD = 2.5 V to 3.0 V		–	–	600	mA
Output voltage ranges					
Programmable range	100 mV steps	4.0	5.0	5.5	V
Specified performance range		4.5	5.0	5.2	V
Voltage error	0 to 1300 mA load	-3	0	+3	%
Temperature coefficient		-100	0	+100	ppm/C

Table 3-20 Boost regulator performance specifications (cont.)

Parameter	Comments [4, 5]	Min	Typ	Max	Units
Transient response [1]					
Settling time	To within 90% of final value	–	–	200	µs
Overshoot	Regulator turn on / off, voltage step, load off	-5	–	+5	%
Voltage dip due to load transient	6 mA to 600 mA	–	–	500	mV
Voltage spike due to load transient	600 mA to 6 mA	–	–	500	mV
Output ripple [2]	1300 mA load, 10 µF X5R capacitor	–	–	80	mVpp
Efficiency [3]	VDD = +3.6 V				
I_{load} = 1300 mA		–	88	–	%
I_{load} = 600 mA		–	93	–	%
Ground current					
No load	VDD = +3.6 V, Vout = 5.1 V, fsw = 1.6 MHz	2	–	–	mA
Load regulation	I_load = 0.01·I_rated to I_rated	–	–	3	%
Line regulation	VDD = 3V to 4.5V at I_load=1200mA	–	–	2	%/V

1. The stated transient response performance is achieved regardless of the transitory mode – turning the regulator on and off, changing load conditions, changing input voltage, or reprogramming the output voltage setting.
2. Ripple voltage is measured within a 20 MHz bandwidth, and does not include glitches (such as those caused by coupling across the external Schottky diode's parasitic capacitance).
3. Figure 3-4 shows the boost efficiency plot under various load conditions.
4. All specifications apply over the device's recommended operating conditions, load current range, and capacitor ESR range, unless noted otherwise.
5. Performance characteristics that may degrade if the rated output current is exceeded:
   • Voltage error • Output ripple • Efficiency

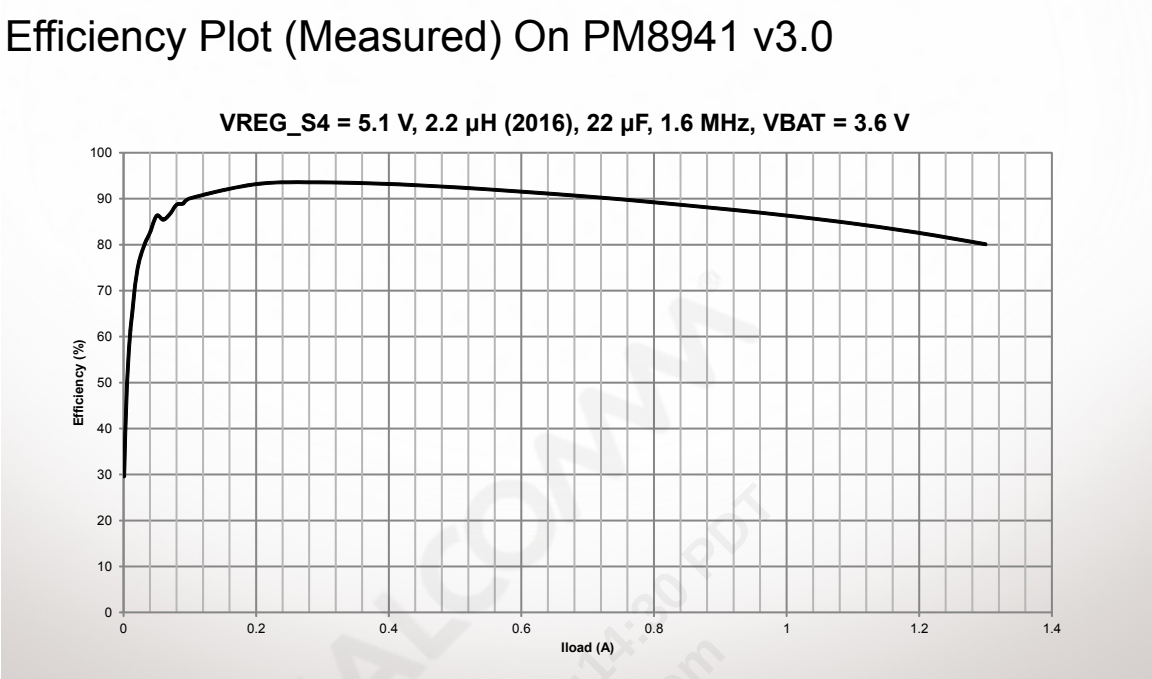


Figure 3-4 Boost SMPS efficiency

3.6.3 Buck SMPS

The PM8941 includes three high-frequency switched-mode power supply (HF-SMPS) circuits. They support PWM and PFM modes, and the automatic transition between PWM and PFM modes, depending on the load current. Pertinent performance specifications are given in Table 3-21.

Table 3-21 HF-SMPS performance specifications

Parameter	Comments [4, 5]	Min	Typ	Max	Units
Input voltage range [1]		2.500	3.600	5.500	V
Output voltage ranges					
Programmable range	25 mV steps	1.550	–	3.1250	V
	12.5 mV steps	0.375	–	1.5625	V
Rated load current (I_rated)	Continuous current delivery				
PWM mode					
S1, S3		2000	–	–	mA
S2		1000	–	–	mA
PFM mode [2]					
S1, S2, S3	Advanced PFM mode	–	–	200	mA
S2	Advanced PFM mode	–	–	200	mA
Short circuit/peak current limit (through inductor)	VREG pin shorted; Current limit (I_limit) is set via SPMI programming.	0.7 * I_limit	I_limit	1.3 * I_limit	mA

Table 3-21 HF-SMPS performance specifications (cont.)

Parameter	Comments [4, 5]	Min	Typ	Max	Units
Voltage error					
PWM mode	V_out > 1.0 V, I_rated / 2	-1	–	+1	%
	V_out < 1.0 V, I_rated / 2	-10	–	+10	mV
PFM mode	V_out > 1.0 V, I_rated / 2	-1	–	+1	%
	V_out < 1.0 V, I_rated / 2	-10	–	+10	mV
Overall error (includes voltage error, load and line regulation and errors due to temperature and process)					
PWM mode	V_out > 1.0 V, I_rated /2	-2	–	2	%
	V_out < 1.0 V, I_rated /2	-20	–	20	mV
PFM mode	V_out > 1.0 V, I_rated /2	-2	–	4	%
	V_out < 1.0 V, I_rated /2	-20	–	40	mV
Temperature coefficient		-100	–	+100	ppm/C
Efficiency [3]	VBAT 3.6 V				
PWM mode	V_out = 1.8 V, I_load = 300 mA	–	90	–	%
	V_out = 1.8 V, I_load = 10 to 600 mA	–	85	–	%
	V_out = 1.8 V, I_load = 800 mA	–	80	–	%
PFM mode	V_out = 1.2 V, I_load = 5 mA	–	80	–	%
Enable settling time	From enable to within 1% of final value				
Slow start		–	–	500	µs
Fast start		–	–	100	µs
Enable overshoot					
Slow start	V_out > 1.0 V, no load	–	–	3	%
	V_out < 1.0 V, no load	–	–	30	mV
Fast start	V_out > 1.0 V, no load	–	–	6	%
	V_out < 1.0 V, no load	–	–	60	mV
Voltage step settling time per LSB	To within 1% of final value	–	–	10	µs
Response to load transitions	PWM mode				
Dip due to low-to-high load	400 mA load change in 0.2*I_rated to I_rated range	–	–	40	mV
Spike due to high-to-low load	400 mA load change in 0.2*I_rated to I_rated range	–	–	70	mV
Load transient + ripple measured relative to PWM mode	For 1 A load step, 47 µF load cap	-40	–	70	mV
Output ripple voltage	Tested at the switching frequency				
PWM pulse-skipping mode	40 mA load; 20 MHz measurement bw	–	20	40	mVpp
PWM non-pulse-skipping mode	I_rated; 20 MHz measurement bw	–	10	20	mVpp
PFM mode	50 mA load; 20 MHz measurement bw	–	30	50	mVpp
Load regulation	V_in ≥ V_out + 1 V; I_load = 0.01·I_rated to I_rated	–	–	0.25	%
Line regulation	V_in = 3.2 V to 4.2 V; I_load = 100 mA	–	–	0.25	%/V

Table 3-21 HF-SMPS performance specifications (cont.)

Parameter	Comments [4, 5]	Min	Typ	Max	Units
Power-supply ripple rejection (PSRR)					
50 Hz to 1 kHz		40	–	–	dB
1 kHz to 100 kHz		20	–	–	dB
100 kHz to 1 MHz		30	–	–	dB
Output noise					
F < 5 kHz		–	-101	–	dBm/Hz
F = 5 kHz to 10 kHz		–	-106	–	dBm/Hz
F = 10 kHz to 500 kHz		–	-106	–	dBm/Hz
F = 500 kHz to 1 MHz		–	-116	–	dBm/Hz
F > 1 MHz		–	-116	–	dBm/Hz
Peak output impedance vs frequency	1 kHz – 1 MHz	–	150	–	mΩ
Ground current					
PWM mode, no load		–	550	750	µA
PFM mode, no load		–	20	30	µA

1. At 2.5 V input voltage, S2 SMPS can provide about 800 mA current. Bhelper LDO is required to supplement the additional current if the system demands it.
2. HF bucks have two low-power modes - legacy PFM and advanced PFM. In legacy PFM mode, the rated current is 100 mA maximum.
3. Figure 3-5, Figure 3-6, and Figure 3-7 show efficiency of S1, S2, S3 SMPS in auto mode.
4. All specifications apply over the device's recommended operating conditions, load current range, and capacitor ESR range, unless noted otherwise.
5. Performance characteristics that may degrade if the rated output current is exceeded:
   • Voltage error • Efficiency • Output ripple voltage

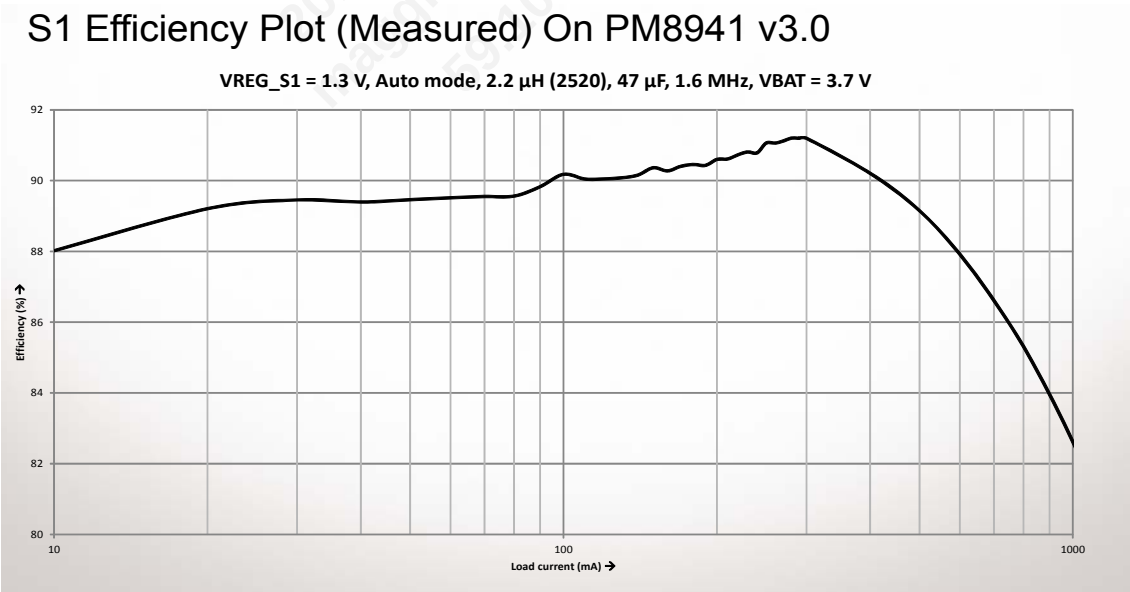


Figure 3-5 S1 efficiency plot (measured) on a PM8941

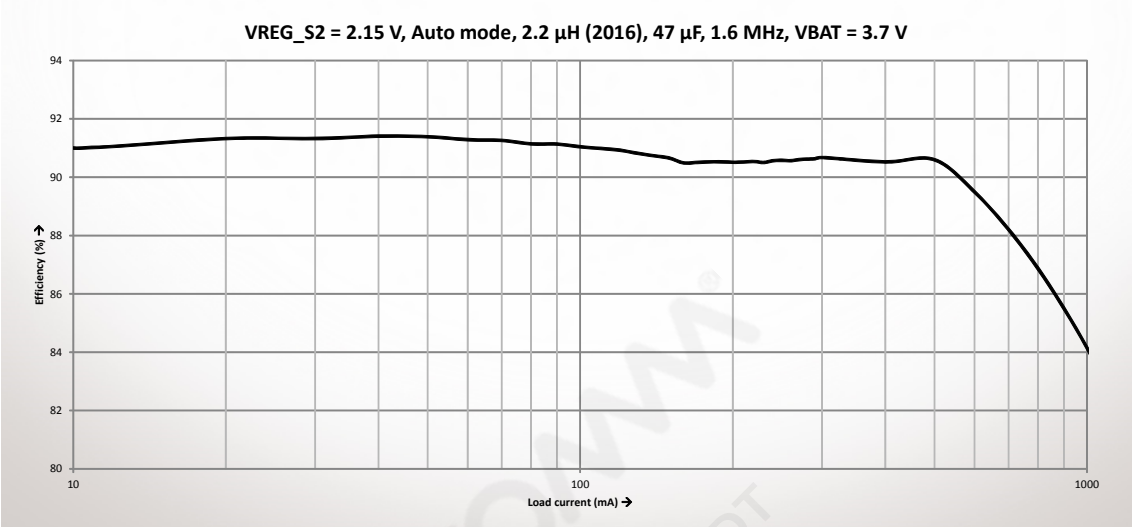


Figure 3-6 S2 efficiency plot (measured) on a PM8941

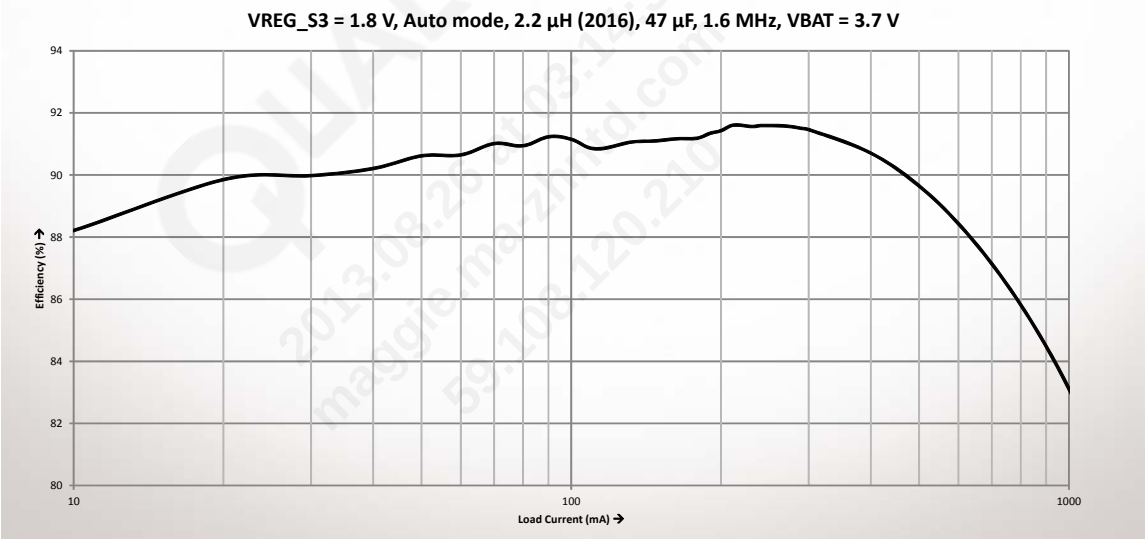


Figure 3-7 S3 efficiency plot (measured) on a PM8941

3.6.4 Linear regulators

Seven low dropout linear regulator designs are implemented within the PMIC:

- NMOS rated for 1200 mA (N1200)
- PMOS rated for 600 mA (P600)
- NMOS rated for 300 mA (N300)
- PMOS rated for 300 mA (P300)
- PMOS rated for 150 mA (P150)
- PMOS rated for 50 mA (P50)

- PMOS for on-chip clock circuits (VREG_L5 for low-noise XO buffers and VREG_L7 for the XO block)
  - Since these two LDOs are not used off-chip, most of their performance specifications are not published.
  - Each has a no-load ground current of 80 µA max.

All other LDO performance specifications are presented in Table 3-22.

Table 3-22 LDO performance specifications

Parameter	Comments [8]	Min	Typ	Max	Units
Output voltage ranges					
Programmable range					
All NMOS	12.5 mV steps	0.750	–	1.5375	V
All PMOS	25 mV steps from 0.75 to 1.525 V; 50 mV steps from 1.50 to 4.90 V	1.500	–	4.900	V
Rated load current (I_rated), normal [1]	Continuous current delivery				
N1200		–	–	1200	mA
P600 [2]		–	–	600	mA
N300		–	–	300	mA
P300		–	–	300	mA
P150		–	–	150	mA
P50		–	–	50	mA
Rated load current, low-power mode [1]	Continuous current delivery				
All LDOs except N1200 and P50 types		–	–	10	mA
N1200		–	–	100	mA
P50		–	–	5	mA
Pass FET power dissipation		–	–	600	mW
Overall error at default voltage (includes dc voltage error, load and line regulations and errors due to temperature and process)					
Normal mode	NMOS and PMOS	-2	–	+2	%
Low-power mode (NMOS)	NMOS	-4	–	+4	%
Low-power mode (PMOS)	PMOS	-5	–	5	%
Overall error at non-default voltages (includes dc voltage error, load and line regulations and errors due to temperature and process)					
Normal mode		-3	–	+3	%
Temperature coefficient		-100	–	+100	ppm/C
Transient settling time [3]	To within 1% of final value	20	100	200	µs

Table 3-22 LDO performance specifications (cont.)

Parameter	Comments [8]	Min	Typ	Max	Units
Transient overshoot / undershoot [3]					
Normal mode					
N1200	0.25·I_rated to 0.75·I_rated load step	-4	–	+4	%
All PMOS LDOs	0.01·I_rated to I_rated load step	-50	–	+70	mV
N300	0.01·I_rated to I_rated load step	-3	–	+3	%
Low-power mode (all LDOs)	Same load steps as listed above	-3	–	+3	%
Dropout voltage [4, 5]	Both operating modes				
N1200		–	–	60	mV
All other LDOs		–	–	300	mV
Load regulation	V_in > V_out + 0.5 V; 0.01·I_rated to I_rated				
Normal mode		–	–	0.3	%
Low-power mode		–	–	1.5	%
Line regulation [6]					
Normal mode		–	–	0.1	%/V
Low-power mode		–	–	0.5	%/V
Power-supply ripple rejection [7]	PSRR				
Normal mode					
50 Hz to 1 kHz		60	70	–	dB
1 kHz to 10 kHz		50	60	–	dB
10 kHz to 100 kHz		40	50	–	dB
100 kHz to 1 MHz	All LDOs except N1200	35	45	–	dB
	N1200	25	30	–	dB
Low-power mode					
50 Hz to 1 kHz		40	50	–	dB
1 kHz to 100 kHz	All LDOs except N1200	30	40	–	dB
	N1200	25	40	–	dB
Short-circuit current limiting	Normal mode				
N1200		1300	1800	2600	mA
All PMOS LDOs	Limit = I_rated x factor listed	1.5	2.5	3.5	–
N300	Limit = I_rated x factor listed	2.0	3.0	4.0	–

Table 3-22 LDO performance specifications (cont.)

Parameter	Comments [8]	Min	Typ	Max	Units
Soft current limit during startup	Current above I_rated	–	–	100	mA
Ground current					
Normal mode, no load					
N1200		–	200	220	µA
P600		–	90	300	µA
P300		–	65	150	µA
N300		–	100	150	µA
P150		–	55	100	µA
P50		–	45	100	µA
Low-power mode, no load					
N1200		–	26	30	µA
All PMOS LDOs		–	5	6	µA
N300		–	12	15	µA
With load, either mode					
All PMOS and NMOS LDOs		–	–	0.5	%
Bypass mode					
All NMOS LDOs		–	8	10	µA
All PMOS LDOs		–	–	1	µA
Bypass mode on-resistance					
N1200		–	12	20	mΩ
N300		–	–	1	Ω
P50		–	4.4	8	Ω
P150		–	1.5	2.7	Ω
P300		–	0.55	0.83	Ω
P600		–	0.28	0.42	Ω

1. Rated current is the current at which all specifications are met. Higher currents are allowed during normal operation, but more headroom will be needed to maintain performance. The low-power mode's current rating should not be exceeded; if so, switch to the normal mode.
2. L20 and L21 have been characterized for 800 mA peak current capability. These regulators meet all the specifications at 800 mA except a) Overshoot due to load transients (100 mV overshoot observed) b) Load regulation at high temperature, low voltage (at VBAT = 3 V and 90°C, load regulation is about 0.68% for normal power mode).
3. The stated transient response performance is achieved regardless of the transitory mode – turning the regulator on and off, changing load conditions, changing input voltage, or reprogramming the output voltage setting.
4. LDO voltage dropout measurement:
   –Program the LDO for its desired operating voltage (V_set_d).
   –Measure the output voltage; call this value V_set_m.
   –Adjust the load such that the LDO delivers its rated output current (I_rated).
   –Adjust the input voltage until V_in = V_set_m + 0.5 V.
   –Decrease V_in until V_out drops 100 mV (until V_out = V_set_m – 0.1 V); call the resulting input value V_in_do and call this output value V_out_do.
   –The voltage drop across the regulator under this condition is the dropout voltage (V_do = V_in_do – V_out_do).
5. The dropout voltage is specified at full rated current of the LDO. The voltage headroom required to maintain the LDO in regulation depends on the load current of the LDO. The current that an LDO can provide needs to be derated based on the headroom. For example, the 600 mA PMOS LDO has a dropout voltage of 300 mV. When headroom is 150 mV, the PMOS LDO can provide 600* (150/300) = 300 mA current without going out of regulation.

6. Line regulation is the output variation due to a changing input voltage, calculated as the output voltage change in percent divided by the input voltage change. The input voltage changes are:
   –From 1.10 to 1.80 V for N1200 LDOs
   –From 3.35 to 4.35 V for PMOS LDOs other than the USB LDO (L3)
   –From 3.80 to 4.80 V for USB LDO when powered off VDD
   –From 4.50 to 5.50 V for USB LDO when powered off +5 V or VBUS
   –From 1.80 to 2.80 V for N300 LDOs
7. The input voltage requirements for PSRR measurements depends on the LDO usage:
   –For the USB LDO when powered off +5 V or VBUS, the input voltage is adjusted to V_out + 1.0 V.
   –The input voltage for all other LDOs and for the USB LDO when powered off VDD is adjusted to V_out + 0.5 V.
8. All specifications apply over the device's recommended operating conditions, load current range, and capacitor ESR range, unless noted otherwise.

3.6.5 Voltage switches

The PM8941 has three low-voltage switches and two 5 V switches. All switch performance specifications are listed in Table 3-23, where they are partitioned into functional groups:

- Low-voltage switches – common input voltage is switched independently to three output pins.
- 5 V switches – a common input voltage is switched independently to two output pins:
  - HDMI
  - OTG

Table 3-23 Voltage switch performance specifications

Parameter	Comments	Min	Typ	Max	Units
Low-voltage switches (LVS)					
Input voltage range		1.200	–	1.875	V
Rated current (I_rated)		–	300	–	mA
Slew rate (switch output node)		–	–	100	mV/µs
Switch output ready	Soft start plus gate full enhancement	100	300	1200	µs
Over-current threshold	Threshold = I_rated x factor listed	1.3	1.5	2.6	–
On resistance		–	–	0.15	Ω
Ground current Sleep mode Normal mode, no load	Switch on, support functions disabled	 – –	 – –	 1 40	 µA µA
Pulldown discharge time	Switch turned off	–	0.5	2	ms
5 V HDMI switch					
Input voltage range		4.0	–	5.5	V
Rated current (I_rated)		–	55	–	mA
Switch output ready	Soft start plus gate full enhancement	0.1	0.35	1.4	ms
Over-current threshold	Threshold = I_rated x factor listed	6	8	10	–
On resistance		–	–	2.0	Ω

Table 3-23 Voltage switch performance specifications (cont.)

Parameter	Comments	Min	Typ	Max	Units
Ground current Off Normal mode, no load	 Module is disabled	 – –	 – 60	 1 –	 µA µA
Pulldown discharge time	Switch turned off	–	0.5	2	ms
5 V OTG switch					
Input voltage range		4.0	–	5.5	V
Rated current (I_rated)		–	500	–	mA
Switch output ready	Soft start plus gate full enhancement	–	–	1.4	ms
Over-current threshold	Threshold = I_rated x factor listed	1.3	1.5	2.0	–
On resistance		–	–	0.2	Ω
Ground current Off Normal mode, no load	 Module is disabled	 – –	 – 50	 1 –	 µA µA
Pulldown discharge time		–	0.5	2	ms

3.6.6 Internal voltage-regulator connections

Some regulator supply voltages and/or outputs are connected internally to power other PMIC circuits. These circuits will not operate properly unless their supplies are correct; this requires:

1. Certain regulator supply voltages must be delivered at the right value.
2. Corresponding regulator sources must be enabled and set to the proper voltages.

These requirements are summarized in Table 3-24.

Table 3-24 Internal voltage-regulator connections

Feature	Regulator / Connection	Default	Notes
GPIO_01-14 supplies	VREG_L6	1.8 V	
	VDD_L2_LVS1_2_3	1.8 V	Same as VREG_S3
	VREG_L1	1.225 V	
	VDD_L8_16_18_19	3.6 V	Same as VPH_PWR
GPIO_15-18 supplies	VREG_L6	1.8 V	
	VDD_L2_LVS1_2_3	1.8 V	Same as VREG_S3
GPIO_19-36 supplies	VREG_L6	1.8 V	
	VDD_MSM_IO	1.8 V	Same as VREG_S3
	VDD_TORCH	5.0 V	Same as VREG_5V
	VDD_GPLED	3.6 V	Same as VPH_PWR

Table 3-24 Internal voltage-regulator connections (cont.)

Feature	Regulator / Connection	Default	Notes
MPP_01-04	VREG_L6	1.8 V	
	VDD_L2_LVS1_2_3	1.8 V	Same as VREG_S3
	VREG_L1	1.225 V	
	VDD_L8_16_18_19	3.6 V	Same as VPH_PWR
MPP_05-08	VREG_L6	1.8 V	
	VDD_MSM_IO	1.8 V	Same as VREG_S3
	VREG_L1	1.225 V	
	VDD_GPLED	3.6 V	Same as VPH_PWR
Clocks	VDD_MSM_IO	1.8 V	Sleep clock pad (Vio)
	VREG_XO	1.8 V	XO core
	VREG_RF_CLK	1.8 V	Low noise output buffers (XO_OUT_Ax)
	VREG_L6	1.8 V	Low power output buffers (XO_OUT_Dx) The XO_OUT_Dx buffer supply VREG_L6 is forced on by XO_OUT_Dx EN
Power-on	VDD_MSM_IO	1.8 V	PAD IO (Vio)
	VREG_SMBC	3.6 V	UVLO detect
SPMI	VDD_MSM_IO	1.8 V	SPMI pad (Vio)
AMUX, XO/HKADC supply	VREG_L8	1.8 V	
BMS	VREG_L8	1.8 V	BMS IADC supply VREG_L8 is forced on by BMS for OCV measurement
SMBB	VREG_L8	1.8 V	VREF_BAT supply
RGB supply	VDD_RGB	3.6 V	Same as VPH_PWR
	VDD_TORCH	5.0 V	Same as VREG_5V
GPLED supply	VDD_GPLED	3.6 V	Same as VPH_PWR
	VDD_TORCH	5.0 V	Same as VREG_5V
Flash supply	VCHG	5.0 V	Flash mode
	VDD_TORCH	5.0 V	Torch mode
WLED supply	VDD_GPLED	3.6 V	Same as VPH_PWR
Vibrator driver supply	VDD_L8_16_18_19		Same as VPH_PWR
dVdd regulator	VDD_L2_LVS1_2_3	1.8 V	Same as VREG_S3
	VREG_L6	1.8 V	

3.6.7 Input connection options

Some voltage regulators have the option to be connected to different power sources. Table 3-25 lists the input connection options for each voltage regulator.

Table 3-25 Voltage regulator input options

Voltage regulator input	Input connection options
VDD_L1_3	VREG_S1
VDD_L4_11	VREG_S1
VDD_L5_7	VREG_S2 or VPH_PWR
VDD_L6_12_14_15	VREG_S2
VDD_L8_16_18_19	VPH_PWR
VDD_L9_10_17_22	Boost bypass output (VREG_BOOST_BYPASS)
VDD_L13_20_23_24	Boost bypass output (VREG_BOOST_BYPASS)
VDD_L21	Boost bypass output (VREG_BOOST_BYPASS)
VDD_L2_LVS1_2_3	VREG_S3
VIN_5VS	VREG_5V

3.7 General housekeeping

The PMIC includes many circuits that support handset-level housekeeping functions – various tasks that must be performed to keep the handset in order. Integration of these functions reduces the external parts count and the associated size and cost. Housekeeping functions include an analog switch matrix, multiplexers, and voltage scaling; an HK/XO ADC circuit; system clock circuits; a real-time clock for time and alarm functions; and over-temperature protection.

3.7.1 Analog multiplexer and scaling circuits

A set of analog switches, analog multiplexers, and voltage-scaling circuits select and condition a single analog signal for routing to the on-chip HK/XO ADC. The multiplexer and scaling functions are summarized in Table 3-26.

Table 3-26 Analog multiplexer and scaling functions

Ch #	Description	Typical input range (V) [3]	Scaling	Typical output range (V)
0	USB_IN pin (divided by 20)	0.15 to 0.50	1	0.15 to 0.50
1	DC_IN pin (divided by 20)	0.15 to 0.50	1	0.15 to 0.50
2	VCHG_SNS	3 to 10	1/6	0.50 to 1.67
3	–	–	–	–
4	AMUX_USB_ID pin (MV)	0.3 to 3 * (VL8 - 0.10)	1/3	0.10 to (VL8 - 0.10)
5	VCOIN pin	2.0 to 3.25	1/3	0.67 to 1.08
6	VBAT_SNS pin	2.5 to 4.5	1/3	0.83 to 1.50
7	VPH_PWR pin	2.5 to 4.5	1/3	0.83 to 1.50
8	Die-temperature monitor	0.4 to 0.9	1	0.4 to 0.9
9	0.625 V reference voltage	0.625	1	0.625
10	1.25 V reference voltage	1.25	1	1.25
11	Charger temperature	0.10 to (VL8 - 0.10)	1	0.10 to (VL8 - 0.10)
12, 13	–	–	–	–
14, 15	GND_REF, VDD_ADC	Direct connections to ADC for calibration		
16 to 23	MPP_01 to MPP_08 pin	0.05 to 1.5	1	0.05 to 1.5
24 to 31	–	–	–	–
32 to 39	MPP_01 to MPP_08 pin	0.05 to 4.5	1/3	0.05 to 1.5
40 to 47	–	–	–	–
48	BAT_THERM pin [1]	0.10 to (VL8 - 0.10)	1	0.05 to (VL8 – 0.05)
49	BAT_ID pin [1]	0.10 to (VL8 - 0.10)	1	0.05 to (VL8 – 0.05)
50	XO_THERM pin direct [1]	0.10 to (VL8 - 0.10)	1	0.10 to (VL8 - 0.10)
51 to 53	AMUX_1 to AMUX_3 pin [1]	0.10 to (VL8 - 0.10)	1	0.10 to (VL8 - 0.10)
54	AMUX_HW_ID pin [1]	0.10 to (VL8 - 0.10)	1	0.10 to (VL8 - 0.10)
55, 56	AMUX_4, AMUX_5 pin [1]	0.10 to (VL8 - 0.10)	1	0.10 to (VL8 - 0.10)
57	AMUX_USB_ID pin (LV)[1]	0.10 to (VL8 - 0.10)	1	0.10 to (VL8 - 0.10)

Table 3-26 Analog multiplexer and scaling functions (cont.)

Ch #	Description	Typical input range (V) [3]	Scaling	Typical output range (V)
58, 59	AMUX_PU1, AMUX_PU2 pin [1]	0.10 to (VL8 - 0.10)	1	0.10 to (VL8 - 0.10)
60	XO_THERM pin through amux [1]	0.10 to (VL8 - 0.10)	1	0.10 to (VL8 - 0.10)
61, 62	–	–	–	–
63	Module power off [2]	–	–	–

1. These AMUX inputs come from off-chip thermistor circuits. The AMUX circuits include switches that allow these inputs to use one of two external pullup resistors (at AMUX_PU1 or AMUX_PU2), thereby reducing the number of resistors in the thermistor networks.
2. Channel 63 should be selected when the analog multiplexer is not being used; this prevents the scalers from loading the inputs.
3. Input voltage must not exceed the highest of the following supply voltages: VCOIN, VBAT, VCHG, or VPH_PWR. The term *VL8* is the VREG_L8 output voltage (connected internally).

NOTE Gain and offset errors are different through each analog multiplexer channel. Each path should be calibrated individually over its valid gain and offset settings for best accuracy.

Performance specifications pertaining to the analog multiplexer and its associated circuits are listed in Table 3-27.

Table 3-27 Analog multiplexer performance specifications

Parameter	Comments [2]	Min	Typ	Max	Units
Supply voltage (VL8)	Connected internally to VREG_L8	–	1.8	–	V
Output voltage range					
Full specification compliance		0.10	–	VL8 – 0.10	V
Degraded accuracy at edges		0.05	–	VL8 – 0.05	V
Input referred offset errors					
Channels with x1 scaling		-2.0	–	+2.0	mV
Channels with 1/3 scaling		-1.5	–	+1.5	mV
Channels with 1/6 scaling		-3.0	–	+3.0	mV
Gain errors, including scaling	Excludes VREG_L8 output error				
Channels with x1 scaling		-0.20	–	+0.20	%
Channels with 1/3 scaling		-0.15	–	+0.15	%
Channels with 1/6 scaling		-0.30	–	+0.30	%
Integrated nonlinearity (INL)	Input referred to account for scaling	-3	–	+3	mV
Input resistance	Input referred to account for scaling				
Channels with x1 scaling		10	–	–	MΩ
Channels with 1/3 scaling		1	–	–	MΩ
Channels with 1/6 scaling		0.5	–	–	MΩ
Channel-to-channel isolation	1 V AC input at 1 kHz	50	–	–	dB

Table 3-27 Analog multiplexer performance specifications (cont.)

Parameter	Comments [2]	Min	Typ	Max	Units
Output settling time [1]	C_{load} = 28 pF	–	–	25	µs
Output noise level	f = 1 kHz	–	–	2	$\mu V/Hz^{1/2}$

1. The AMUX output and a typical load is modeled in Figure 3-9. After S1 closes, the voltage across C2 settles within the specified settling time.
2. Multiplexer offset error, gain error, and INL are measured as shown in Figure 3-8. Supporting comments:
   - The non-linearity curve is exaggerated for illustrative purposes.
   - Input and output voltages must stay within the ranges stated in Table 3-26; voltages beyond these ranges result in nonlinearity, and are beyond specification.
   - Offset is determined by measuring the slope of the endpoint line (m) and calculating its Y-intercept value (b):
     Offset = b = $y_1 - m \cdot x_1$
   - Gain error is calculated from the ideal response and the endpoint line as the ratio of their two slopes (in percentage):
     Gain_error = [(slope of endpoint line)/(slope of ideal response) - 1]·100%
   - INL is the worst-case deviation from the endpoint line. The endpoint line removes the gain and offset errors to isolate nonlinearity:
     INL(min) = min[V_{out}(actual at V_x input) - V_{out}(endpoint line at V_x input)]
     INL(max) = max[V_{out}(actual at V_x input) - V_{out}(endpoint line at V_x input)]

Table 3-28 AMUX input to ADC output end-to-end accuracy

AMUX ch #	Function	Typical input range		Automatic scaling	Typical output range		AMUX input to ADC output end-to-end accuracy, RSS [1, 2] (%)				AMUX input to ADC output end-to		
		Min (V)	Max (V)		Min	Max	Without calibration		Internal Calibration		Without calibration		
							Accuracy corresponding to min input voltage	Accuracy corresponding to max input voltage	Accuracy corresponding to min input voltage	Accuracy corresponding to max input voltage	Accuracy corresponding to min input voltage	Accuracy corresponding to max input voltage	co t
0	VCOIN	2	3.25	1/3	0.67	1.08	3.1	2.2	0.7	0.52	5.7	4.37	
1	VBAT	2.5	4.5	1/3	0.83	1.5	2.64	1.89	0.6	0.47	5	3.76	
2	OVP_SNS (protected)	4.5	9.5	1/6	0.75	1.58	2.84	1.84	0.62		5.33	3.68	
3	NC	-	-	-	-	-	-	-	-	-	-	-	
4	VPH_PWR	2.5	4.5	1/3	0.83	1.5	2.64	1.89	0.6	0.47	5	3.76	
5	IBAT: Battery charge current	0.3	1.5	1	0.3	1.5	6.3	1.87	1.33	0.47	10	3.73	
6	Selected input from pre-mux	0.1	1.7	1	0.1	1.7	18	1.76	4	0.47	26	3.59	
7	Selected input from pre-mux	0.3	5.1	1/3	0.1	1.7	18.33	1.78	3.67	0.45	25.67	3.59	
8	BATT_THERM	0.1	1.7	1	0.1	1.7	18	1.76	4	0.47	26	3.59	
9	BATT_ID	0.1	1.7	1	0.1	1.7	18	1.76	4	0.47	26	3.59	
10	USB_IN (protected)	4.35	6.5	1/4	1.09	1.63	2.21	1.82	0.53	0.46	4.34	3.68	
11	Die-temperature monitor	0.4	0.9	1	0.4	0.9	4.75	2.4	1	1.22	8	4.7	
12	0.625V reference voltage	0.625	0.625	1	0.625	0.625	3.27	3.27	0	0	5.95	5.95	
13	1.25V reference voltage	1.25	1.25	1	1.25	1.25	2.05	2.05	0	0	4.08	4.08	
14	NC	-	-	-	-	-	-	-	-	-	-	-	
15	Power off	-	-	-	-	-	-	-	-	-	-	-	
-	XO_THERM[5]	0.1	1.7	1	0.1	1.7	18.1	1.76	0.6	0.35	20.4	3.08	

1) The min and max accuracy values correspond to min and max input voltage to the AMUX channel
2) Accuracy based on Root Sum Square (RSS) of the individual errors
3) Accuracy is based on Worst Case sraighst Sum (WCS) of all errors
4) Absolute uses 0.625V and 1.25V MBG voltage reference as calibration points. Ratiometric uses the GND_XO and VREF_XO_THM as the calibration points
5) XO_THERM to ADC output end-to-end accuracy

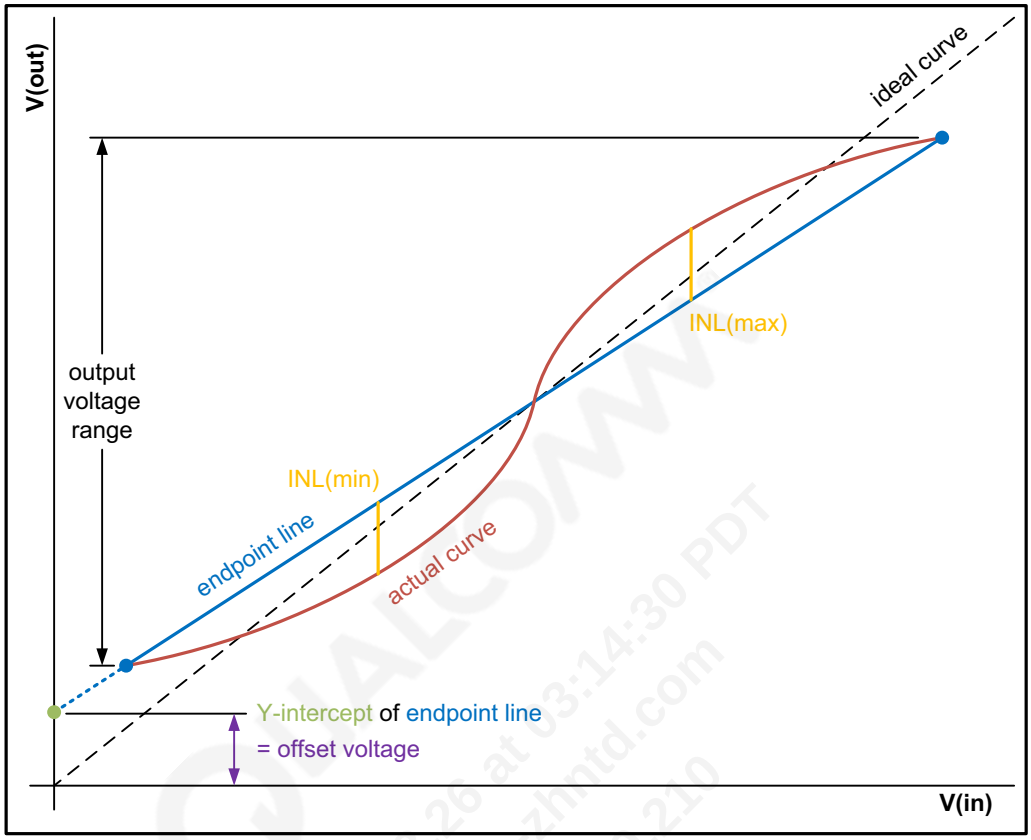


Figure 3-8 Multiplexer offset and gain errors

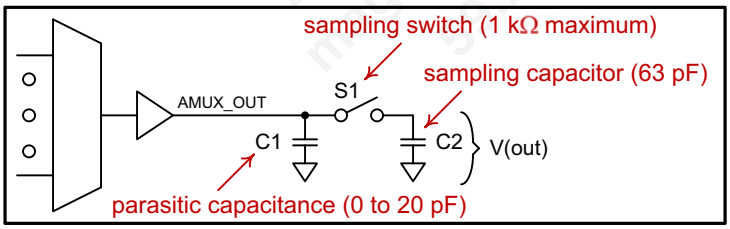


Figure 3-9 Analog multiplexer load condition for settling time specification

3.7.2 HK/XO ADC circuit

The analog-to-digital converter circuit is shared by the housekeeping (HK) and 19.2 MHz crystal oscillator (XO) functions. A 2:1 analog multiplexer selects which source is applied to the ADC:

- The HK source – the analog multiplexer output discussed in Section 3.7.1; or
- The XO source – the thermistor network output that estimates the 19.2 MHz crystal temperature.

HK/XO ADC performance specifications are listed in Table 3-29.

Table 3-29 HK/XO ADC performance specifications

Parameter	Comments	Min	Typ	Max	Units
Supply voltage	Connected internally to VREG_L14	–	1.8	–	V
Resolution		–	–	15	bits
Analog-input bandwidth		–	100	–	kHz
Sample rate	XO/8	–	2.4	–	MHz
Offset error	Relative to full-scale	-1	–	+1	%
Gain error	Relative to full-scale	-1	–	+1	%
INL	15-bit output	-8	–	+8	LSB
DNL	15-bit output	-4	–	+4	LSB

3.7.3 System clocks

The PMIC includes several clock circuits whose outputs are used for general housekeeping functions, and elsewhere within the handset system. These circuits include a 19.2 MHz XO with multiple controllers and buffers, an MP3 clock output, 32.768 kHz crystal support, an RC oscillator, and sleep-clock outputs. Performance specifications for these functions are presented in the following subsections.

3.7.3.1 19.2 MHz XO circuits

An external crystal is supplemented by on-chip circuits to generate the desired 19.2 MHz reference signal. Using an external thermistor network, the on-chip ADC, and advanced temperature compensation software, the PMIC eliminates the large and expensive VCTCXO module required by previous-generation chipsets. The XO circuits initialize and maintain valid pulse waveforms, and measure time intervals for higher-level handset functions. Multiple controllers manage the XO warmup and signal buffering, and generate the desired clock outputs (all derived from one source):

- Low-noise outputs XO_OUT_A0, XO_OUT_A1, and XO_OUT_A2 – enabled internally or can be enabled via properly configured GPIOs.
- Low-power output XO_OUT_D0 – enabled by the dedicated control pin XO_OUT_D0_EN; this output is used as the modem IC's clock signal.
- Low-power output XO_OUT_D1 – enabled internally or can be enabled via a properly configured GPIO.

Since the different controllers and outputs are independent, circuits other than those needed for the WAN can operate even while the modem IC is asleep and its RF circuits are powered down.

The XTAL_19M_IN and XTAL_19M_OUT pins are incapable of driving a load – the oscillator will be significantly disrupted if either pin is externally loaded.

As described in Section 3.7.3.5, an RC oscillator is used to drive some clock circuits until the XO source is established.

The 19.2 MHz XO circuit and related performance specifications are listed in Table 3-30.

Table 3-30 XO controller, buffer, and circuit performance specifications

Parameter	Comments	Min	Typ	Max	Units
XO circuits					
Operating frequency	Set by external crystal	–	19.2	–	MHz
Load conditions					
Capacitance		–	–	15	pF
Resistance		2.5	–	–	kΩ
Startup time					
Normal		–	–	6.0	ms
Enhanced	Warmup time enhancement feature	–	–	3.5	ms
Supply voltage = VREG_XO	Input buffer and core XO circuits	–	1.8	–	V
Low-noise outputs: XO_OUT_Ax (RFCLKx)					
Voltage swing		–	1.8	–	Vpp
Duty cycle		48	50	52	%
Start-up time	Oscillator enabled, clock output buffer regulator on	–	80	–	µs
	Oscillator enabled, clock output buffer regulator off	–	280	–	µs
Output buffer shift		–	–	0.1	°
Buffer output impedance					
at 1x drive strength		54	80	122	Ω
at 2x drive strength		30	42	64	Ω
at 3x drive strength		21	30	44	Ω
at 4x drive strength		17	22	35	Ω
Phase noise in low-power mode					
at 10 Hz		–	–	-86	dBc/Hz
at 100 Hz		–	–	-110	dBc/Hz
at 1 kHz		–	–	-124	dBc/Hz
at 10 kHz		–	–	-134	dBc/Hz
at 100 kHz		–	–	-140	dBc/Hz
at 1 MHz		–	–	-137	dBc/Hz
Phase noise in normal-power mode					
at 10 Hz		–	–	-86	dBc/Hz
at 100 Hz		–	–	-116	dBc/Hz
at 1 kHz		–	–	-134	dBc/Hz
at 10 kHz		–	–	-144	dBc/Hz
at 100 kHz		–	–	-144	dBc/Hz
at 1 MHz		–	–	-144	dBc/Hz

Table 3-30 XO controller, buffer, and circuit performance specifications (cont.)

Parameter	Comments	Min	Typ	Max	Units
Phase noise in high-power mode					
at 10 Hz		–	–	-86	dBc/Hz
at 100 Hz		–	–	-116	dBc/Hz
at 1 kHz		–	–	-134	dBc/Hz
at 10 kHz		–	–	-144	dBc/Hz
at 100 kHz		–	–	-148	dBc/Hz
at 1 MHz		–	–	-150	dBc/Hz
Supply = VREG_RF_CLK	Output buffers	–	1.30	–	V
Power-supply current					
High-power mode		–	1.39	1.74	mA
Normal-power mode		–	1.23	1.52	mA
Low-power mode		–	1.14	1.38	mA
Low-power outputs: XO_OUT_Dx (BBCLKx)					
Output levels					
Logic high (V_{OH})		0.65·VDD	–	–	V
Logic low (V_{OL})		–	–	0.35·VDD	V
Output duty cycle		44	50	56	%
Start-up time	Crystal oscillator is enabled	–	250	–	µs
USB jitter	Specified values are peak-to-peak period jitter.				
0.5 MHz to 2 MHz		–	–	50	ps
> 2 MHz		–	–	100	ps
Buffer output impedance	Current drive capabilities meet the output levels specified above.				
at 1x drive strength		54	80	122	Ω
at 2x drive strength		30	42	64	Ω
at 3x drive strength		21	30	44	Ω
at 4x drive strength		17	22	35	Ω
Supply voltage = VREG_L4	Output buffers	–	1.80	–	V
Power-supply current		–	0.98	1.0	mA
Low-power differential clock: XO_OUT_DIFF_x					
Frequency accuracy		-300	–	300	ppm
Duty cycle		40	–	60	%
Differential output swing		600	–	–	mVp-p
Output impedance	Differential	–	–	100	Ω
Capacitive load		–	–	10	pF
Deterministic jitter	At all frequencies	–	–	150	ps
Random jitter	RMS, 1.5 MHz to Nyquist frequency	–	–	3	ps

Table 3-30 XO controller, buffer, and circuit performance specifications (cont.)

Parameter	Comments	Min	Typ	Max	Units
Divided down XO clock: DIV_CLKx					
Buffer output impedance					
at low GPIO drive strength		30	42	64	Ω
at medium GPIO drive strength		21	30	44	Ω
at high GPIO drive strength		17	22	35	Ω

3.7.3.2 19.2 MHz XO crystal requirements

Crystal performance is critical to a wireless product's overall performance. Guidance is available within *19.2 MHz Modem Crystal Qualification Requirements and Approved Suppliers* (80-V9690-19). This document includes:

- Data needed from crystal suppliers to demonstrate compliance
- Approved suppliers for different crystal configurations
- Description of various schematic options

3.7.3.3 MP3 clock

GPIOs can be configured as a 2.4 MHz clock output to support MP3 in a low-power mode. This clock is a divided-down version of the 19.2 MHz XO signal, so its most critical performance features are defined within the XO table (Table 3-30). Output characteristics (voltage levels, drive strength, etc.) are defined in Section 3.4.

3.7.3.4 32.768 kHz XTAL oscillator

As described in Section 3.7.3.6, this oscillator is one of the sleep-clock options. Two pins are affiliated with this oscillator (XTAL_32K_IN and XTAL_32K_OUT), and neither is capable of driving a load; the oscillator will be significantly disrupted if either pin is loaded. Instead, the dedicated SLEEP_CLK pin or properly configured GPIOs must be used.

If a crystal is not used, the XTAL_32K_IN pin must be connected to GND and XTAL_32K_OUT pin must be left floating.

The PMIC includes a circuit that continually monitors this oscillation, when enabled. If the circuit is enabled but stops oscillating, the device automatically switches to the internal RC oscillator and generates an interrupt.

Performance specifications pertaining to the 32.768 kHz oscillator are listed in Table 3-31.

Table 3-31 Typical 32.768 kHz XTAL oscillator specifications

Parameter	Comments	Min	Typ	Max	Units
Nominal oscillation frequency		–	32.768	–	kHz
Duty cycle		30	50	70	%

Table 3-31 Typical 32.768 kHz XTAL oscillator specifications (cont.)

Parameter	Comments	Min	Typ	Max	Units
Cycle-to-cycle jitter	As defined in JDSE6	–	–	100	ns
Period jitter	As defined in JDSE6	–	–	150	ns
Start-up time	Specified with crystal having an ESR of 60 kΩ	–	–	3	s
Halt detection time	Oscillations stopped	–	–	200	µs
Operating voltage		1.5	–	3	V

3.7.3.5 RC oscillator

The PMIC includes an on-chip RC oscillator that is used during startup, and as a backup to other oscillators. Pertinent performance specifications are listed in Table 3-32.

Table 3-32 RC oscillator performance specifications

Parameter	Comments	Min	Typ	Max	Units
Oscillation frequency		14	19.2	24	MHz
Duty cycle		30	50	70	%
Divider in SLEEP_CLK path		–	586	–	–
Power-supply current		–	–	80	µA

3.7.3.6 Sleep clock

The sleep clock is generated one of three ways:

- Using the 32.768 kHz crystal and supporting PMIC circuits. This is a low-power source that can have high accuracy and stability, depending on the external crystal used.
- Using the 19.2 MHz XO circuit and dividing its output by 586 to create a 32.7645 kHz signal. This signal is used as the startup sleep clock, and as a backup if source 1 or 2 fails.
- Using the on-chip 19.2 MHz RC oscillator instead of the XO signal. This results in a much less accurate and less stable 32.7645 kHz signal that is used for backup only; it is never used in normal modes.

The PMIC sleep-clock output is routed to the modem IC via SLEEP_CLK. It is also available for other applications using properly configured GPIOs. Table 3-33 shows the sleep clock performance specifications.

Table 3-33 Sleep clock performance specifications

Parameter	Comments	Min	Typ	Max	Units
Cycle-to-cycle jitter	32 kHz XO source; as defined in JDSE6	-	-	250	ns
Period jitter	32 kHz XO source; as defined in JDSE6	-	-	350	ns
Period jitter (RMS)	XO/586 source; as defined in JDSE6	-	-	10	ns
Duty cycle	XO/586 source	–	50	–	%
Tolerance	XO/586 source	-12	–	+12	ppm

Related specifications presented elsewhere include:

- 19.2 MHz XO circuits (Section 3.7.3.1)
- 32.768 kHz XTAL oscillator (Section 3.7.3.4)
- 19.2 MHz RC oscillator (Section 3.7.3.5)
- Output characteristics (voltage levels, drive strength, etc.), as defined in Section 3.4

3.7.4 Real-time clock

The real-time clock (RTC) functions are implemented by a 32-bit real-time counter and one 32-bit alarm; both are configurable in one-second increments. The primary input to the RTC circuits is the selected sleep-clock source (32.768 kHz crystal, calibrated low-frequency oscillator, or divided-down 19.2 MHz XO). Even when the phone is off, the selected oscillator and RTC continue to run off the main battery.

If the main battery is present, and an SMPL event occurs, RTC contents are corrupted. As power is restored, the RTC pauses and skips a few seconds. The phone must reacquire system time from the network to resume the usual RTC accuracy. Similarly, if the main battery is not present and the voltage at VCOIN drops too much, RTC contents are again corrupted. In either case, the RTC reset interrupt is generated. A different interrupt is generated if the oscillator stops, also causing RTC errors.

If RTC support is needed when battery is removed, a qualified coin-cell or super capacitor is required on VCOIN pin of the PMIC. If only SMPL support is needed when battery is removed, a capacitor with effective capacitance of at least 10 µF is required on VCOIN pin of the PMIC.

Pertinent RTC specifications are listed in Table 3-34.

Table 3-34 RTC performance specifications

Parameter	Comments	Min	Typ	Max	Units
Tuning resolution	With known calibrated source	–	3.05	–	ppm
Tuning range		-192	–	+192	ppm
Accuracy					
32 kHz XTAL as RTC source	Phone on, phone off	–	–	100	ppm
XO/586 as RTC source	Phone on	–	–	24	ppm
CalRC as RTC source	Phone off, valid battery present	–	–	50	ppm
	Phone off, valid coin cell present			200	ppm

Table 3-35 Qualified coincell / super capacitor specifications

Parameter	Comments	Min	Typ	Max	Units
Operating temperature		-30	25	60	°C
Storage range		-30	-	85	°C
Rated voltage		3.1	3.2	3.3	V

Table 3-35 Qualified coincell / super capacitor specifications

Parameter	Comments	Min	Typ	Max	Units
Effective series resistance (ESR) [1]		-	-	2000	Ω
Effective capacitance of super capacitor [2]	0.5 hr runtime	12	-	-	mF
	1 hr runtime	24	-	-	mF

1. Effective series resistance (ESR) is the worst-case ESR of the unit tested at worst case temperate after 4 years of typical usage. A typical use case is a unit biased constantly with 3.2 V DC voltage at 25°C.
2. With shorter run time expectancy, the effective capacitance requirement can be scaled.

3.7.5 Over-temperature protection (smart thermal control)

The PMIC includes over-temperature protection in stages, depending on the level of urgency as the die temperature rises:

- Stage 0 – normal operating conditions (less than 105°C).
- Stage 1 – 105°C to 120°C; an interrupt is sent to the modem IC without shutting down any PMIC circuits.
- Stage 2 – 120°C to 140°C; an interrupt is sent to the modem IC, and unnecessary high-current circuits are shut down.
- Stage 3 – greater than 140°C; an interrupt is sent to the modem IC, and the PMIC is completely shut down.

Temperature hysteresis is incorporated, such that the die temperature must cool significantly before the device can be powered on again. If any start signals are present while at Stage 3, they are ignored until Stage 0 is reached. When the device cools enough to reach Stage 0 and a start signal is present, the PMIC will power up immediately.

3.8 User interfaces

In addition to housekeeping functions, the PMIC also includes these circuits in support of common handset-level user interfaces: two light pulse generators; LED current drivers (and control signals for external current drivers); white LED drivers for backlighting (including the integrated high-voltage SMPS source); keypad interface; and vibration motor driver.

3.8.1 Light pulse generators

The PMIC includes two light pulse generator (LPG) circuits:

- 8-channel LPG – for controlling RGB LEDs (*fun* lights); the white LEDs for display backlighting; and the vibration motor driver
- 4-channel LPG – for controlling the keypad backlight (via GPLED_xxxx pins)

Since the LPG function is entirely embedded within the PMIC, performance specifications are not appropriate. Instead, the *PM8841 and PM8941 Design Guidelines* (80-NA555-5) provides descriptions of the available features: the number of independent patterns, the types of patterns

available, PWM clock rates and resolutions, pattern synchronization, looping, and so on. That document also defines the LPG channel assignments and programmable parameters.

The LPG outputs can be used to control the on-chip current drivers, or to control external current drivers through up to eight GPIOs (discussed in Section 3.8.2).

3.8.2 LPG controllers (digital driver outputs)

Up to eight GPIOs can be configured as LPG controllers: GPIO[36:33] and GPIO[26:23]. Output characteristics (voltage levels, drive strength, etc.) are defined in Section 3.4.

3.8.3 Current drivers

This section discusses the PMIC's *low* voltage drivers: current drivers other than the white LED drivers. White LED drivers are covered in Section 3.8.4.

Several types of low-voltage LED current drivers are available:

- Red, green, and blue (RGB) drivers that can operate off VPH_PWR, +5 V, or VCHG.
- The red and green RGB drivers are turned ON during ATC.
- Four keypad backlight drivers can operate off VPH_PWR or +5 V.
- Two flash drivers that operate off VCHG in flash mode, and +5 V in torch mode.
- MPPs can be configured as current sinks that operate off VPH_PWR.

Table 3-36 RGB driver performance specifications

Parameter	Comments	Min	Typ	Max	Units
Input voltage		3.5	-	5.0	V
Current per channel (I_{out})		-	-	12	mA
Accuracy	Isink = 100 uA - 500 uA	-4	-	4	%
VIN-VLED = 0.3 V, fPWM = 18.75 kHz	Isink = 500 uA - 12 mA	-2	–	2	%
Matching accuracy between any two LEDs	Isink = 100 uA - 500 uA	-	-	5	%
VIN-VLED = 0.3 V, fPWM = 18.75 kHz	Isink = 500 uA - 12 mA	–	–	2	%
Current per channel when trickle charging	RGB_R and RGB_G channels turned-on in ATC	-	-	4	mA
Dropout voltage	VIN – V_{LED}; I_{out} = 12mA	-	-	250	mV
Dimming					
PWM frequency		0.1	-	18.75	kHz
Resolution		-	8	-	bit
Blinking					
Period	Programmable in 0.5 s steps	0	-	12	s
ON time	Programmable in 0.05 s steps	0	-	1	s

Table 3-37 Keypad-backlighting drivers performance specifications

Parameter	Comments			Min	Typ	Max	Units
Input voltage				3.0	-	5.5	V
Current sink capability (I_{OUT})	Dimming ratio = 50% Dimming ratio = 100%			–	420	–	mA
Absolute current accuracy with PWM dimming (VIN - VLED = 0.3 V, fPWM = 18.75 kHz)	***Typical current***	***PWMH duty cycle***	***PWML duty cycle***				
	20 mA	1	1	-2	–	2	%
	12 mA	0.5	1	-2	–	2	%
	4 mA	0	1	-2	–	2	%
	2 mA	0	0.5	-2	–	2	%
	93.75 µA	0	3/128	-2	–	2	%
Relative current accuracy between LEDs with PWM dimming (VIN - VLED = 0.3 V, fPWM = 18.75 kHz)	***Typical current***	***PWMH duty cycle***	***PWML duty cycle***				
	20 mA	1	1	–	–	2	%
	12 mA	0.5	1	–	–	2	%
	4 mA	0	1	–	–	2	%
	2 mA	0	0.5	–	–	2	%
	93.75 µA	0	3/128	–	–	2	%
PWM frequency				0.4	–	18.75	kHz
PWM resolution				–	8	–	bit
Source driver impedance	Powered by VPH_PWR			–	–	1	Ω
	Powered by VREG_5V			–	–	4	Ω
Short circuit threshold				–	300	–	mA
Current sink headroom	IOUT = 20 mA			–	–	250	mV

Table 3-38 Flash LED driver performance specifications

Parameter	Comments	Min	Typ	Max	Units
Flash driver input voltage					
VDD_FLASH	Flash disabled	2.5	-	10	V
VDD_TORCH	Flash enabled [1]	4.1	-	-	V
	Internal 5 V boost enabled	4.5	-	5.5	V
Output current per LED (I_{LED1}, I_{LED2})	Flash mode (power by VDD_FLASH)	0	-	1000	mA
	Torch mode (powered by VDD_TORCH)	0	-	200	mA
Output current steps	Both flash and torch modes	-	12.5	-	mA
Absolute current accuracy	$I_{LED1} = I_{LED2} > 100$ mA [2]	-7	-	7	%
	$I_{LED1} = I_{LED2} <= 100$ mA [2]	-12.5	-	+12.5	%

Table 3-38 Flash LED driver performance specifications

Parameter	Comments	Min	Typ	Max	Units
Matching current accuracy	$I_{LED1} = I_{LED2} = 1A$; $I_{LED1} = I_{LED2} = 100$ mA [2]	-5	-	5	%
Dropout voltage	VDD_FLASH - V_{LED}	-	500	-	mV
LED short circuit detection threshold	Current output enabled	-	1	-	V
LED open circuit detection threshold	Current output enabled	-	100	-	mV
VPH_PWR droop detection	Programmable in 100 mV steps	2.5	-	3.2	V
Flash safety timer	Programmable in 10 ms steps	10	-	1028	ms
Torch watchdog timer	Programmable in 1 s steps	2	-	33	s
Deglitch timer	FLASH_STROBE, FLASH_MASK1/2/3, VPH_PWR droop, fault	0	-	128	µs
Current ramp steps (up / down)	LED current from 0 to 200 mA LED current from 200 mA to 1 A	- -	12.5 50	- -	mA mA
Current ramp step duration		0.2	6.7	27	us
Thermal derating threshold	Programmable in 10 °C; Junction temperature	80	-	120	°C
Thermal derating slope	Programmable values: 2, 2.5, 4, 5, 10	2	-	10	%/°C

1. VLED1, VLED2 = 3.8 V, ILED1 = ILED2 = 1 A; charger in reverse boost, adaptive mode.
2. Headroom = 0.5 V for Flash or torch mode.

3.8.4 White LED SMPS and current drivers

White LEDs generate backlighting for the handset's LCD. The PMIC supports WLEDs with a boost converter that generates the high voltage needed for powering a string of WLEDs, plus three output drivers for sinking the current from WLED strings. Brightness can be controlled via SPMI, the on-chip LPG, and externally via content adaptive backlight control (CABC). Other useful features include over-voltage protection, over-current protection, soft-start, and adaptive output voltage (as the WLED forward-voltage drop changes with temperature, the boost output voltage changes appropriately. Current driver performance specifications are listed in Table 3-39.

Table 3-39 WLED boost and driver performance specification

Parameter	Comments		Min	Typ	Max	Units
Input voltage	25 mA/string, 8s1p or 8s2p, Vout ~ 27 V 25 mA/string, 8s3p, Vout ~ 27 V		3 3.3	– –	5.5 5.5	V
Output voltage			6	–	33	V
Over voltage protection (OVP)	Includes 0.5 V headroom for current sink; programmable in four steps		27	–	35	V
OVP hysteresis			–	2	–	V
Current sink headroom	Accuracy specs are met with this headroom		–	500	–	mV
Current limit	Programmable in 8 steps		100	–	1680	mA
Current limit accuracy	Current limit setting = 525 mA		-15	–	15	%

Table 3-39 WLED boost and driver performance specification (cont.)

Parameter	Comments		Min	Typ	Max	Units
Output current per string	100% brightness register setting, no CABC		–	25	–	mA
Absolute accuracy	Combined CABC duty cycle and internal dimming control; TA = 0ºC to 85ºC, VHEADROOM=0.5 V	100%	-2	–	2	%
		50%	-3	–	3	%
		25%	-5	–	5	%
		10%	-12	–	12	%
		5%	-25	–	25	%
		1%	-100	–	100	%
		0.4%	-100	–	220	%
Relative accuracy	Combined CABC; TA = 0 C to 85 C, VHEADROOM=0.5 V	100%	–	–	2	%
		50%	–	–	2.5	%
		25%	–	–	5	%
		10%	–	–	12.5	%
		5%	–	–	25	%
		1%	–	–	125	%
		0.4%	–	–	250	%
CABC frequency			20	40	60	kHz
CABC duty cycle [1]	Usable range		0	–	100	%
Efficiency [2]	VDD = 3.6 V, Iout = 15 mA/string, 8s1p or 8s2p, fSW = 0.8 MHz		–	83	–	%
Switching frequency			0.6	0.8	1.6	MHz
Ground current	Boost switching, no load		–	2	2.5	mA
Output capacitor [3] Up to 5s1p, 5s2p, 5s3p	Nominal capacitance		4.7	–	10	µF
	Derated at 30 V for bias and aging		0.2	–	–	µF
Power inductor [3]	Nominal inductance		4.7	10	22	µH

1. Recommended CABC duty cycle range is 4% to 100%. Under 4% CABC duty cycle, flickering is observed.
2. Figure 3-10 shows the efficiency plot for 8s1p and 8s2p configurations of the WLED boost and driver.
3. 7s3p, 8s3p may require use of two 4.7 µF output caps and a larger sized inductor.

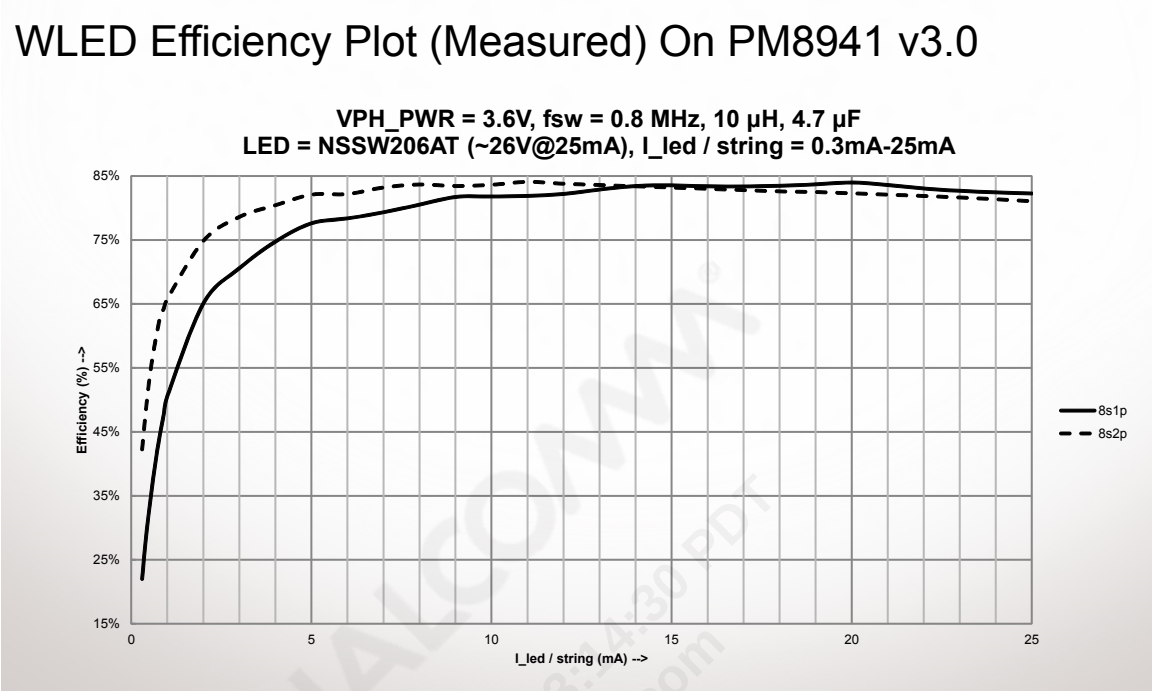


Figure 3-10 WLED efficiency plot on the PM8941 device

3.8.5 Keypad interface

GPIOs can be configured to implement a keypad interface supporting a matrix of up to 10 rows by 8 columns. Performance specifications that are specific to the keypad interface are listed in Table 3-40.

Table 3-40 Keypad interface performance specifications

Parameter	Comments	Min	Typ	Max	Units
Supply voltage		–	1.8	–	V
Load capacitance		–	–	100	pF
Sense lines					
Pullup current		20.8	31.5	42.2	µA
Pulldown current		400	600	800	µA
Key-stuck delay	Number of 32 kHz cycles = 325,000	7.94	9.92	13.60	sec
Drive lines					
Drive strength	Open-drain outputs	–	0.6	–	mA

3.8.6 Vibration motor driver

The PMIC supports silent incoming call alarms with its vibration motor driver. The vibration driver is a programmable voltage output that is referenced to VDD; when off, its output voltage is VDD. The motor is connected between VDD and the VIB_DRV_N pin.

Performance specifications for the vibration motor driver circuit are listed in Table 3-41.

Table 3-41 Vibration motor driver performance specifications

Parameter	Comments	Min	Typ	Max	Units
Output voltage (V_m) error [1] Relative error Absolute error	VDD > 3.2 V; I_m = 0 to 175 mA; V_m setting = 1.2 to 3.1 V Total error = relative + absolute	 -6 -60	 – –	 +6 +60	 % mV
Headroom [2]	I_m = 175 mA	–	–	200	mV
Short circuit current	VIB_DRV_N = VDD	225	–	600	mA

1. The vibration motor driver circuit is a low-side driver. The motor is connected directly to VDD, and the voltage across the motor is $V_m = V_{DD} - V_{out}$, where V_{out} is the PMIC voltage at VIB_DRV_N.
2. Adjust the programmed voltage until the lowest motor voltage occurs while still meeting the voltage accuracy specification. This *lowest* motor voltage ($V_m = V_{DD} - V_{out}$) is the *headroom*.

3.9 IC-level interfaces

The IC-level interfaces include poweron circuits; the SPMI; interrupt managers; and miscellaneous digital I/O functions like level translators, detectors, and controllers. Parameters associated with these IC-level interface functions are specified in the following subsections. GPIO and MPP functions are also considered part of the IC-level interface functional block, but they are specified in their own sections (Section 3.10 and Section 3.11, respectively).

3.9.1 Poweron circuits and the power sequences

Dedicated circuits continuously monitor several events that might trigger a poweron sequence. If any of these events occur, the PMIC circuits are powered on, the handset's available power sources are determined, the correct source is enabled, and the modem IC is taken out of reset.

PM8941 ES1, ES2 devices exhibit single power on sequence as shown in Figure 3-11. ES3 devices onwards exhibit dual power on sequence as shows in Figure 3-12.

The I/Os to/from the poweron circuits are basic digital control signals that must meet the voltage-level requirements stated in Section 3.4. The KYPD_PWR_N and CBL_PWR_N inputs are pulled up to an internal voltage (dVdd). Additional poweron-circuit performance specifications are listed in Table 3-42 and Table 3-44. More complete definitions for time intervals included in the table are provided in the *PM8841 and PM8941 Design Guidelines* (80-NA555-5).

Table 3-42 Poweron circuit performance specifications for single power-on sequence

Parameter	Comments	Min	Typ	Max	Units
Internal pullup resistor	At KYPD_PWR_N and CBL_PWR_N pins	150	200	250	kΩ
tmbg	Poweron trigger to MBG_EN/pre-pon PBS sequence (includes debounce time of the power-on trigger)	12.01	15.99	20.02	ms
tBMS	Time for BMS to make an open circuit voltage measurement	48.00	64.00	80.00	ms

Table 3-42 Poweron circuit performance specifications for single power-on sequence (cont.)

Parameter	Comments	Min	Typ	Max	Units
tprepon1	Time from MBG_EN to start of first regulator event	64.95	86.60	108.25	ms
tgpio21	Time from MBG going HIGH till GPIO21 begins to go HIGH	16.95	22.60	28.25	ms
tprebuck	Hardcoded delay in PBS OTP to allow external boost bypass or prebuck to settle	7.50	10.00	12.50	ms
tMBG_slave	Poweron event for slave PMIC to MBG_EN/pre-pon PBS sequence (includes debounce time of the power-on trigger)	12.01	15.99	20.02	ms
tprepon_slave	Time from MBG_EN to start of first regulator event	11.70	15.60	19.50	ms
tpbs_dly1	Hardcoded delay to allow slave PMIC to boot core supplies before continuing PON sequence	36.62	48.80	61.00	ms
tsettle	Regulator settling time	-	-	500.00	µsec
treg [1]	Time between regulator enables	73.24	-	622.07	µsec
tBBCLK_1	Time from the enable of the XO_OUT_D0 clock to the first clock edge	14.25	19.00	23.75	ms
tsec_reg	Time from LDO24 enable to next regulator in the sequence (LDO12)	18.75	25	31.25	ms
tpbs_dly2	Time between first clock edge and PON_RESET_N being set high	–	30	–	ms
tpshold	Time for MSM to assert PS_HOLD (PS_HOLD timeout)	150	200.00	250	ms
tpbs_dly3	Time delay between PON_OUT dropping low and the beginning of turn-off event of LDO21 (PBS controlled)	0.34	0.46	0.57	ms
tpbs_dly4	Wait Time (hardcoded in PBS) for the Krait rail to go low, and the beginning of turn-off event for S2B. We assume that the entire Poff sequence in PM8941 shall finish by this time	5.26	7.02	8.77	ms
tpbs_dly5	Wait time (hardcoded in PBS) between the instant the MPP1 goes low, and the beginning of the GPIO21 turn-off event	2.27	3.02	3.78	ms
Debounce timer [2]		16	–	2000	ms

1. treg for LDO24 to LDO7 is about 200 µsec; VREF_LPDRR is derived from LDO1 and turns on about 250 µsec after LDO1.
2. Delay between triggering event (such as keypad press) and corresponding interrupt; a programmable value.

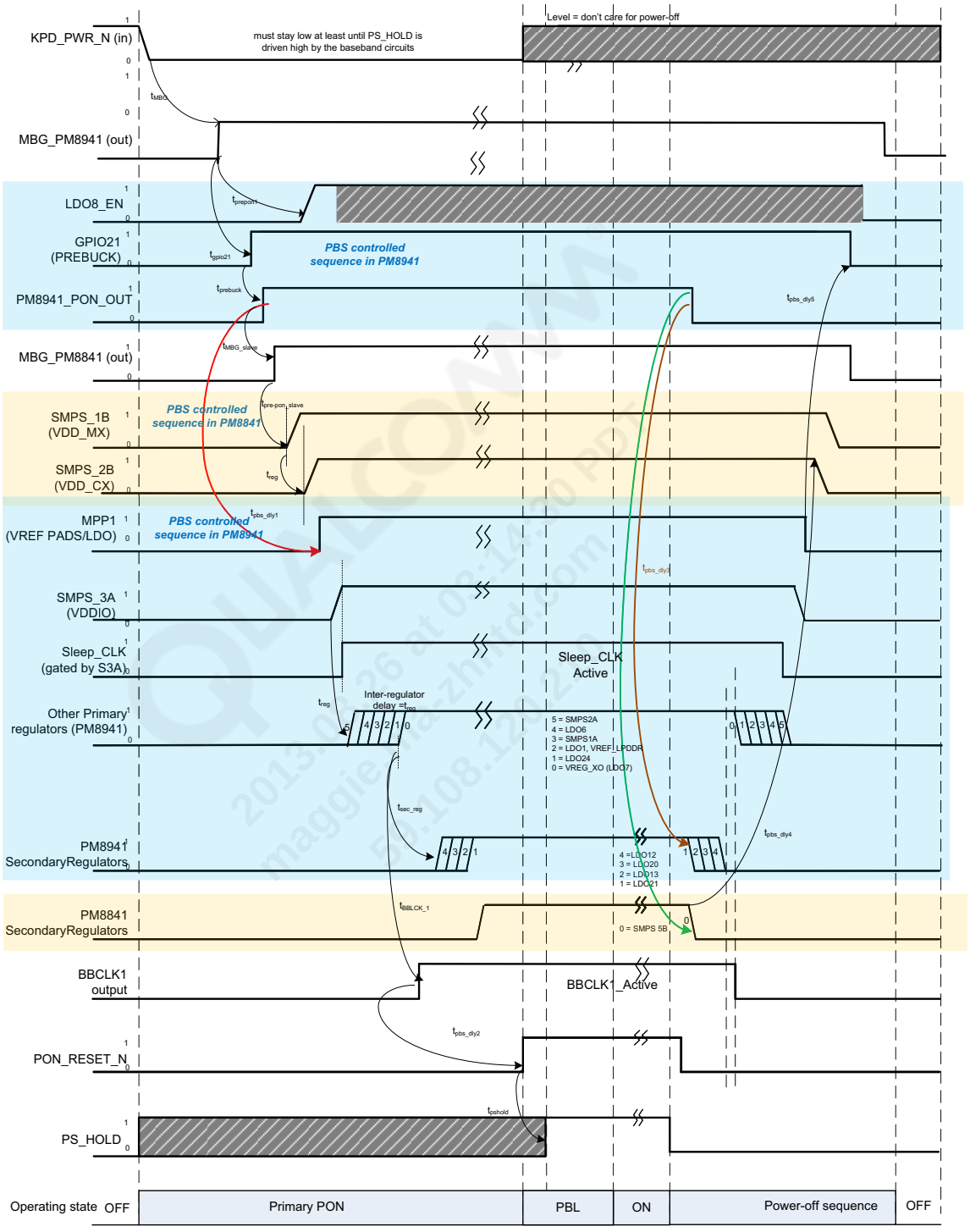


Figure 3-11 Example PM8x41 single power-on sequence

Table 3-43 Poweron circuit performance specifications with dual poweron sequence [1]

Parameter	Comments	Min	Typ	Max	Units
Internal pullup resistor	At KYPD_PWR_N and CBL_PWR_N pins	150	200	250	kΩ
tmbg	Poweron trigger to MBG_EN/pre-pon PBS sequence (includes debounce time of the power-on trigger)	14.63	19.50	24.38	ms
tBMS	Time for BMS to make an open circuit voltage measurement	96	128	160	ms
tprepon1	Time from MBG_EN to start of first regulator event	64.95	86.60	108.25	ms
tgpio21	Time from MBG going HIGH till GPIO21 begins to go HIGH	112.95	150.6	188.25	ms
tprebuck	Hardcoded delay in PBS OTP to allow external boost bypass or prebuck to settle	3.75	5.00	6.25	ms
tMBG_slave	Poweron event for slave PMIC to MBG_EN/pre-pon PBS sequence (includes debounce time of the poweron trigger)	14.40	19.2	24	ms
tprepon_slave	Time from MBG_EN to start of first regulator event	7.50	10	12.5	ms
tpbs_dly1	Hardcoded delay to allow slave PMIC to boot core supplies before continuing PON sequence	36.62	48.80	61.00	ms
tsettle	Regulator settling time	–	–	500.00	µs
treg [2, 3]	Time between regulator enables	73.24	–	622.07	µs
tBBCLK_1	Time from the enable of the XO_OUT_D0 clock to the first clock edge	14.25	19.00	23.75	ms
treset1	Time between first clock edge and PON_RESET_N being set high	3.8	5.06	6.33	ms
tpshold	Time for MSM to assert PS_HOLD (PS_HOLD timeout)	150	200.00	250	ms
tpbs_dly2	Time between SPON message from MSM to S5B turning ON	2.44	3.20	4.06	ms
tpbs_dly3	Time delay between PON_OUT dropping low and the beginning of turn-off event of LDO21 (PBS controlled)	0.34	0.46	0.57	ms
tpbs_dly4	Wait time (hardcoded in PBS) for the Krait rail to go low, and the beginning of turn-off event for S2B. We assume that the entire Poff sequence in PM8941 shall finish by this time	5.26	7.02	8.77	ms

Table 3-43 Poweron circuit performance specifications with dual poweron sequence [1]

Parameter	Comments	Min	Typ	Max	Units
tpbs_dly5	Wait time (hardcoded in PBS) between the instant the MPP1 goes low, and the beginning of the GPIO21 turn-off event	2.27	3.02	3.78	ms
Debounce timer [4]		16	–	2000	ms

1. The power-on sequence measured is on a standalone PM8x41 daughtercard without the bhelper LDO and MSM interaction. With the bhelper LDO and MSM present, the following differences will be seen:
   a) S2A will have a voltage as soon as GPIO_21 is driven high. This is because the bhelper LDO is enabled by GPIO_21.
   b) L6 and L7 will turn ON when S3A turns completely ON. This is because BBCLK enable (XO_OUT_DO_EN) is driven high by the MSM when S3A is turned ON.
2. treg for LDO24 to LDO7 is about 200 µsec; VREF_LPDDR is derived from LDO1 and turns on about 250 µsec after LDO1.
3. treg for HF SMPS (S1A, S2A, and S3A) in PM8941 ES3 device is about 3 msec. In ES4/CS devices it is 622 µsec for HF SMPS.
4. Delay between triggering event (such as a keypad press) and a corresponding interrupt; a programmable value.

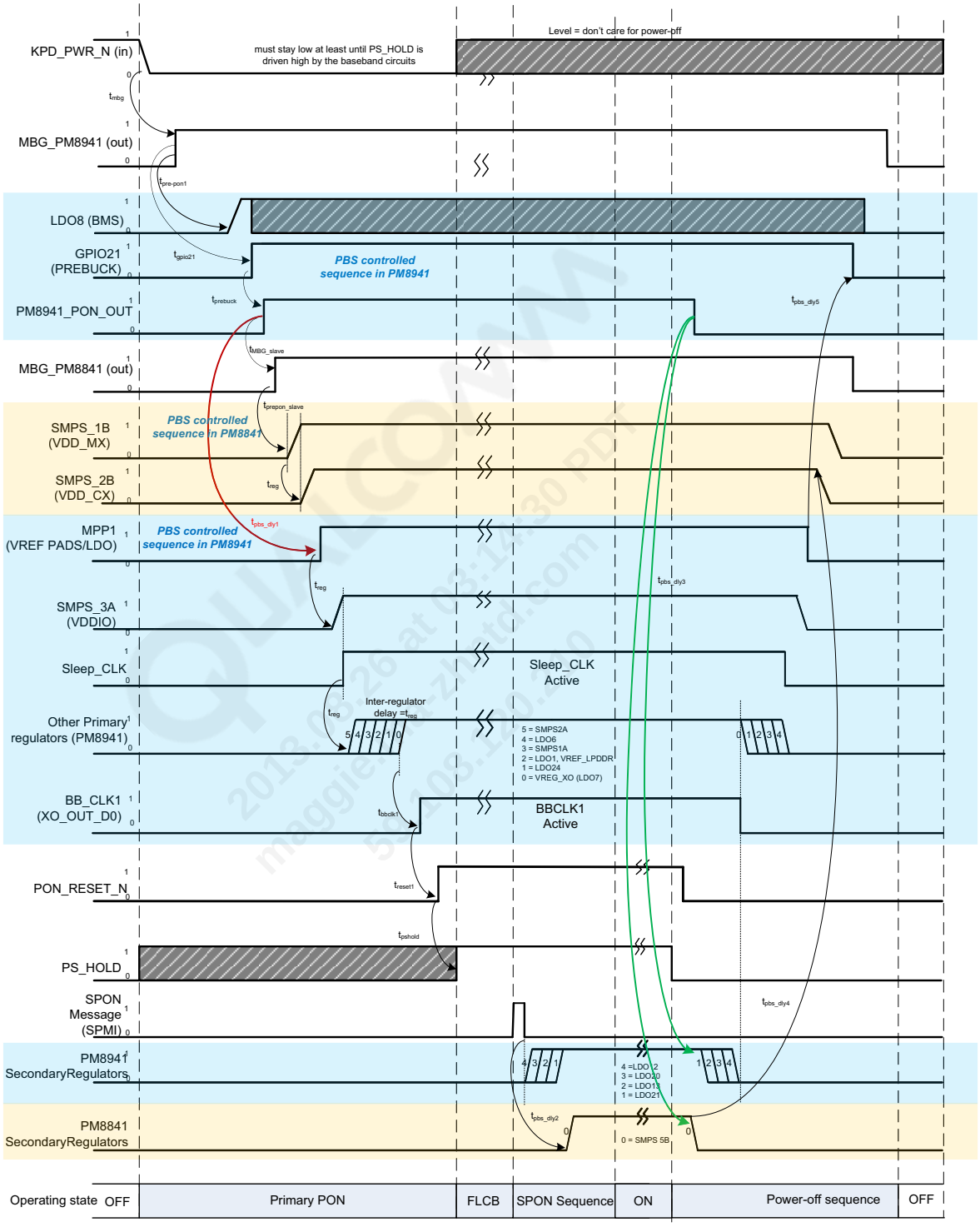


Figure 3-12 Example PM8x41 dual power-on sequence

3.9.2 OPT[4:1] hardwired controls

Four pins (OPT_4, OPT_3, OPT_2, and OPT_1) must be hardwired to ground or VDD, or be left open (high-impedance state or Hi-z); this yields 81 possible combinations.

MSM8x74-based reference designs use these settings: OPT_[4:1] = GND, GND, GND, GND.

3.9.3 SPMI and the interrupt managers

The SPMI is a bidirectional, two-line digital interface that meets the voltage and current level requirements stated in Section 3.4.

PMIC interrupt managers support the chipset modem and its processors, and communicate with the modem IC via SPMI. Since the interrupt managers are entirely embedded functions, additional performance specifications are not required.

3.10 General-purpose input/output specifications

The 36 general-purpose input/output (GPIO) ports are digital I/Os that can be programmed for a variety of configurations (Table 3-44). Performance specifications for the different configurations are included in Section 3.4.

NOTE Unused GPIO pins should be configured as inputs with 10 µA pulldown.

Table 3-44 Programmable GPIO configurations

Configuration type	Configuration description
Input	1. No pullup 2. Pullup (1.5, 30, or 31.5 µA) 3. Pulldown (10 µA) 4. Keeper
Output	Open-drain or CMOS Inverted or non-inverted Programmable drive current; see Table 3-45 for options.
Input/output pair	Requires two GPIOs. Input and output stages can use different power supplies, thereby implementing a level translator. See Table 2-1 for supply options.

GPIOs default to digital input with 10 µA pull-down at poweron. During poweron, PBS programs GPIO_21 as digital output high at VPH_PWR level to enable the external boost-bypass. Before they can be used for their desired purposes, they need to be configured for use.

GPIOs are designed to run at a 4 MHz rate to support high-speed applications. The supported rate depends on the load capacitance and IR drop requirements. If the application specifies load capacitance, then the maximum rate is determined by the IR drop. If the application does not require a specific IR drop, then the maximum rate can be increased by increasing the supply voltage, and adjusting the drive strength according to the actual load capacitance.

3.11 Multipurpose pin specifications

The PM8941 includes eight multipurpose pins (MPPs), and they can be configured for any of the functions specified within Table 3-45. All MPPs are high-Z at power-on. During poweron, PBS programs MPP_01 as analog output which is used as a reference for modem IC 3 V I/Os.

Table 3-45 Multipurpose pin performance specifications

Parameter	Comments	Min	Typ	Max	Units
MPP configured as digital input [1]					
Logic high input voltage		0.65·V_M	–	–	V
Logic low input voltage		–	–	0.35·V_M	V
MPP configured as digital output [1]					
Logic high output voltage	$I_{out} = I_{OH}$	V_M- 0.45	–	V_M	V
Logic low output voltage	$I_{out} = I_{OL}$	0	–	0.45	V
MPP configured as bidirectional I/O [2]					
Nominal pullup resistance	Programmable range [3]	1	–	30	kΩ
Maximum frequency		200	–	–	kHz
Switch on resistance		–	20	50	Ω
Power-supply current		–	6	7	µA

Table 3-45 Multipurpose pin performance specifications (cont.)

Parameter	Comments	Min	Typ	Max	Units
MPP configured as analog input (analog multiplexer input)					
Input current		–	–	100	nA
Input capacitance		–	–	10	pF
MPP configured as analog output (buffered VREF output)					
Output voltage error	-50 µA to +50 µA	–	–	12.5	mV
Temperature variation	Due to buffer only; does not include VREF variation (see Table 3-19)	-0.03	–	+0.03	%
Load capacitance		–	–	25	pF
Power-supply current		–	0.17	0.20	mA
MPP configured as level translator					
Maximum frequency		4	–	–	MHz
MPPs configured as current drivers					
Power supply voltage		–	VDD	–	V
Output current	Programmable in 2 mA increments	0	–	40	mA
Output current accuracy	Any programmed current value	-20	–	+20	%
Dropout voltage	V_IN - V_OUT with I_OUT within the accuracy limits of its current setting	–	–	500	mV
Leakage current	Driver disabled	–	20	100	nA

1. Input and output stages can use different power supplies, thereby implementing a level translator. See Table 2-1 for V_M supply options. Other specifications are included in Section 3.4.
2. MPP pairs are listed in Table 3-46.
3. Pullup resistance is programmable to values of 1 k, 10 k, 30 k, or open.

NOTE Only odd MPPs (MPP_01, MPP_03, MPP_05, MPP_07) can be configured as analog outputs. Only even MPPs (MPP_02, MPP_04, MPP_06, MPP_08) have current sink capability.

Table 3-46 MPP pairs

MPP #		MPP #
1	<–>	2
3	<–>	4
5	<–>	6
7	<–>	8

4 Mechanical Information

4.1 Device physical dimensions

The PM8941 is available in the 229-pin wafer-level nanoscale package (229 WLNSP) that includes dedicated ground pins for improved grounding, mechanical strength, and thermal continuity. The 229 WLNSP package has a 5.82 × 6.15 mm body with a maximum height of 0.55 mm. Pin 1 is located by an indicator mark on the top of the package, and by the ball pattern when viewed from below. A simplified version of the 229 WLNSP outline drawing is shown in Figure 4-1.

NOTE Click the link below to download the 229 WLNSP outline drawing (NT90-NA220-1) from the CDMA Tech Support website.

https://downloads.cdmatech.com/qdc/drl/objectId/09010014819d57ce

If you have permission to view the document, a prompt will be presented for initiating the download.

NOTE Subscribe to the package drawing to be notified of any changes.

Click the **Help** button to download the latest revision of *Using CDMA Tech Support Documents and Downloads User Guide* (80-V7273-1). This document includes subscription instructions.

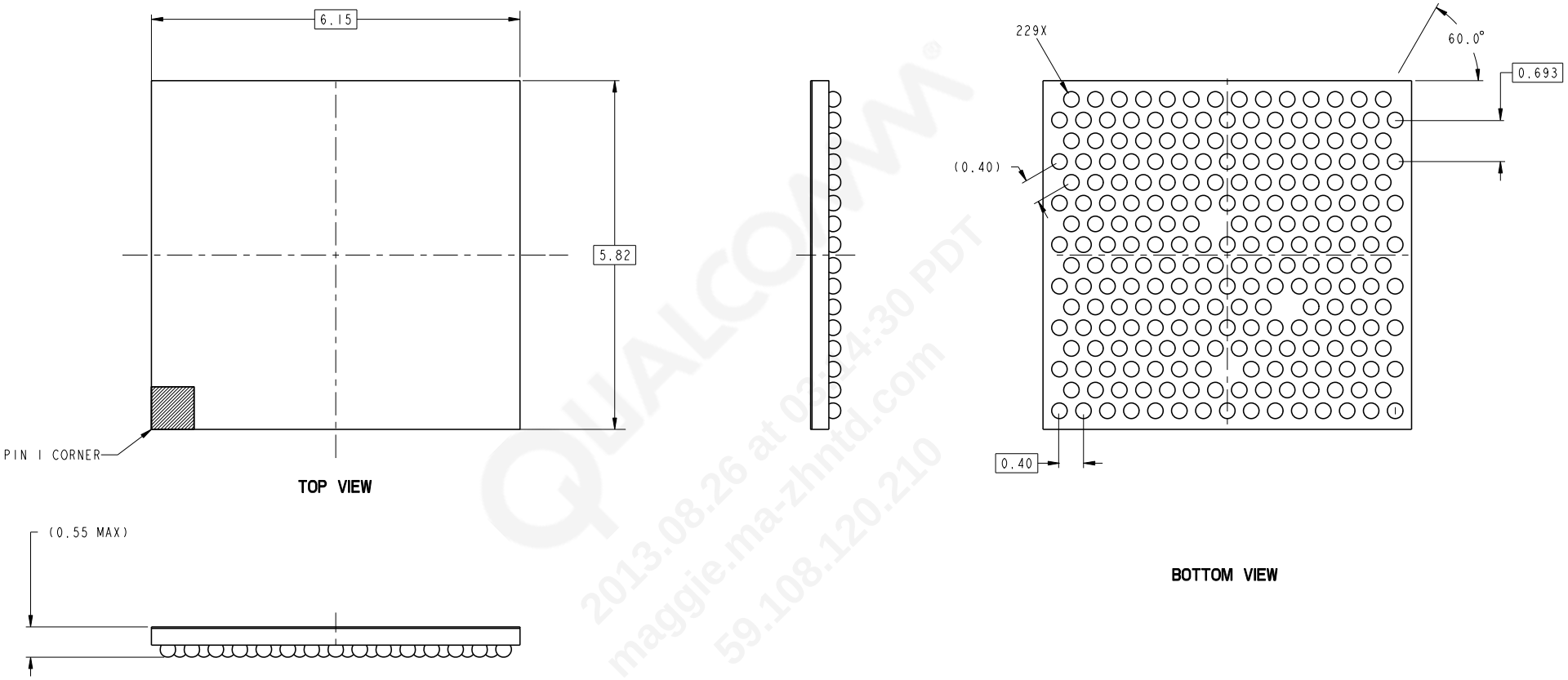


Figure 4-1 229 WLNSP (5.82 × 6.15 × 0.55 mm) package outline drawing

NOTE This is a simplified outline drawing. Click the link below to download the complete, up-to-date package outline drawing:

https://downloads.cdmatech.com/qdc/drl/objectId/09010014819d57ce

4.2 Part marking

4.2.1 Specification-compliant devices

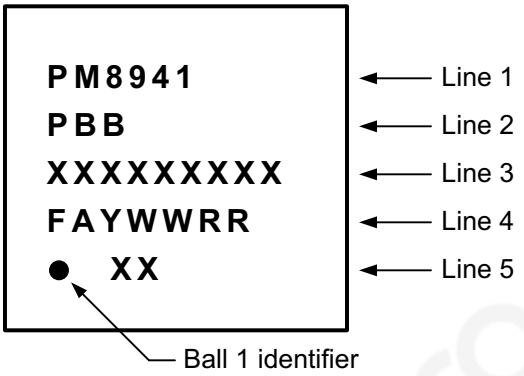


Figure 4-2 PM8941 device marking (top view, not to scale)

Table 4-1 PM8941 marking line definitions

Line	Marking	Description
1	PM8941	Qualcomm product name
2	PBB	P = product configuration code ■ See Table 4-2 for assigned values. BB = feature code ■ See Table 4-2 for assigned values.
3	XXXXXXXXX	XXXXXXXXX = traceability information
4	FAYWWRR	F = supply source code ■ F = A (GF, Fab3, Singapore) ■ F = B (TSMC, Fab5, Taiwan) A = assembly site code ■ A = A (StatsChipPac, SCS, Singapore) ■ A = B (Amkor, ATC, China) ■ A = C (ASE, ASE-kh, Taiwan) Y = single-digit year WW = work week (based on calendar year) RR = product revision ■ See Table 4-2 for assigned values.
5	• XX	• = dot identifying pin 1 XX = traceability information

NOTE For complete marking definitions of all PM8941 variants and revisions, refer to the *PM8941 Device Revision Guide* (80-NA555-4).

4.2.2 Daisy chain devices

This information will be included in future revisions of this document.

4.3 Device ordering information

4.3.1 Specification-compliant devices

This device can be ordered using the identification code shown in Figure 4-3 and explained below.

Device ID code ►	AA-AAAA	— P	— CCC	DDDDD	— EE	— RR	— S	— BB
Symbol definition ►	Product name	Config code	Number of pins	Package type	Shipping package	Product version	Source code	Feature code
Example ►	PM-8941	— 0	— 229	WLNSP	— TR	— 00	— 0	— VV
Feature code (BB) may not be included when identifying older devices. ↗								

Figure 4-3 Device identification code

Device ordering information details for all samples available to date are summarized in Table 4-2.

Table 4-2 Device identification code / ordering information details

PMIC variant	P value	RR value	HW ID #	S value [1]	BB value [2]
ES sample type					
PM8941 ES1	0	01	v2.0	0	VV
PM8941 ES2	0	02	v2.0.1	0	VV
PM8941 ES3	0	03	v3.0	0	VV
PM8941 ES4/CS	0	04	v3.1	0	VV
Other sample types will be included in future revisions of this document.					

1. 'S' is the source configuration code that identifies all the qualified die fabrication-source combinations available at the time a particular sample type was shipped.
2. 'BB' is the feature code that identifies an IC's specific feature set, which distinguishes it from other versions or variants. Defined feature sets available at the time of this document's release are:
   – VV = null set; all devices available at this time have the same feature set.

4.3.2 Daisy-chain devices

This information will be included in future revisions of this document.

4.4 Device moisture-sensitivity level

Plastic-encapsulated surface mount packages are susceptible to damage induced by absorbed moisture and high temperature. A package's moisture-sensitivity level (MSL) indicates its ability to withstand exposure after it is removed from its shipment bag, while it is on the factory floor awaiting PCB installation. A low MSL rating is better than a high rating; a low MSL device can be exposed on the factory floor longer than a high MSL device. All pertinent MSL ratings are summarized in Table 4-3.

Table 4-3 MSL ratings summary

MSL	Out-of-bag floor life	Comments
1	Unlimited	≤ 30°C / 85% RH
2	1 year	≤ 30°C / 60% RH; **PM8941 rating**
2a	4 weeks	≤ 30°C / 60% RH
3	168 hours	≤ 30°C / 60% RH
4	72 hours	≤ 30°C / 60% RH
5	48 hours	≤ 30°C / 60% RH
5a	24 hours	≤ 30°C / 60% RH
6	Mandatory bake before use. After bake, must be reflowed within the time limit specified on the label.	≤ 30°C / 60% RH

Qualcomm follows the latest IPC/JEDEC J-STD-020 standard revision for moisture-sensitivity qualification. ***The PM8941 devices are classified as MSL2; the qualification temperature was 250ºC.*** This qualification temperature (250°C) should not be confused with the peak temperature within the recommended solder reflow profile (see Section 6.2.3 for more details).

4.5 Thermal characteristics

Rather than provide thermal resistance values θ_{JC} and θ_{JA}, validated thermal package models are provided through the CDMA Tech Support website. A thermal model for each device is provided within the *Power_Thermal* subfolder for each chipset family. Designers can extract thermal resistance values by conducting their own thermal simulations.

NOTE Click the link below to download the PM8941 thermal package model from the CDMA Tech Support website.

This link will be included in future revisions of this document.

If you have permission to view the document, a prompt will be presented for initiating the download.

NOTE Subscribe to the PM8941 thermal package model to be notified of any changes.

Click the **Help** button to download the latest revision of *Using CDMA Tech Support Documents and Downloads User Guide* (80-V7273-1). This document includes subscription instructions.

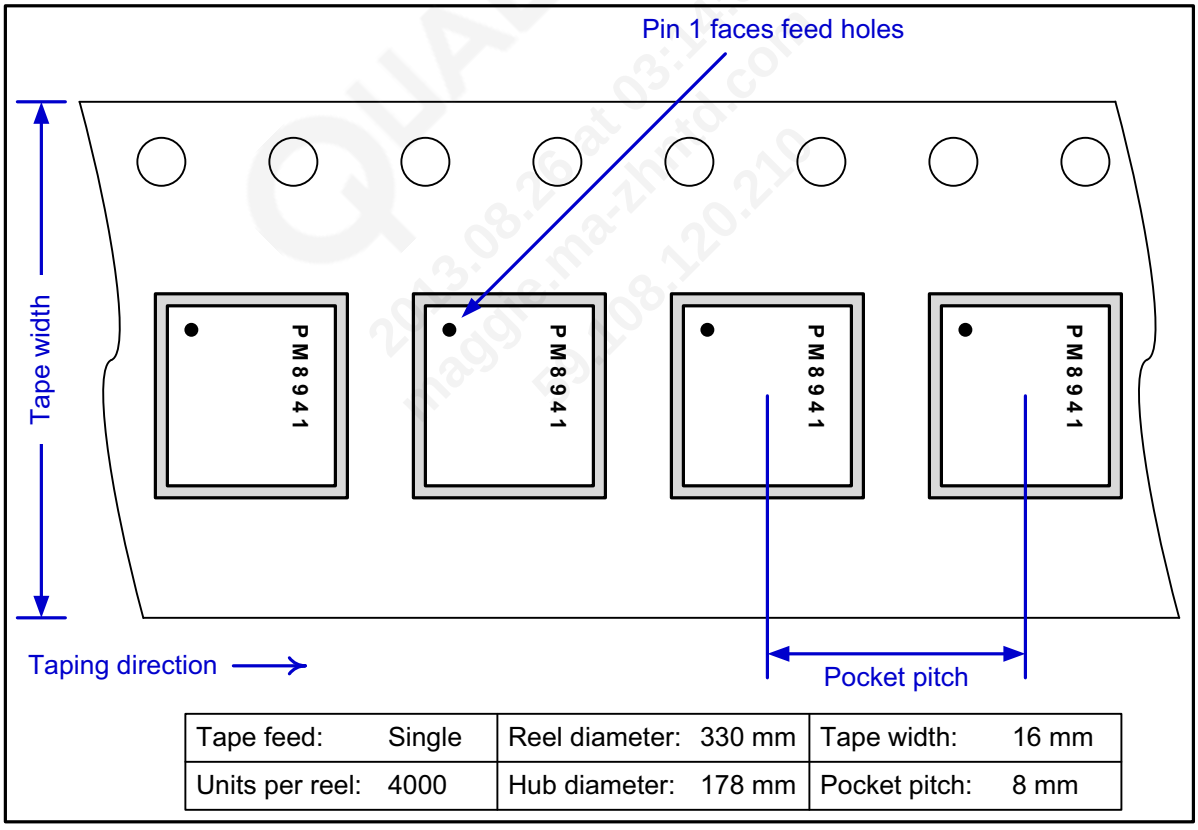
5 Carrier, Storage, & Handling Information

5.1 Carrier

5.1.1 Tape and reel information

All Qualcomm carrier tape systems conform to EIA-481 standards.

A simplified sketch of the PM8941 tape carrier is shown in Figure 5-1, including the proper part orientation, maximum number of devices per reel, and key dimensions.



Tape feed:	Single	Reel diameter:	330 mm	Tape width:	16 mm
Units per reel:	4000	Hub diameter:	178 mm	Pocket pitch:	8 mm

Figure 5-1 Carrier tape drawing with part orientation

Tape-handling recommendations are shown in Figure 5-2.

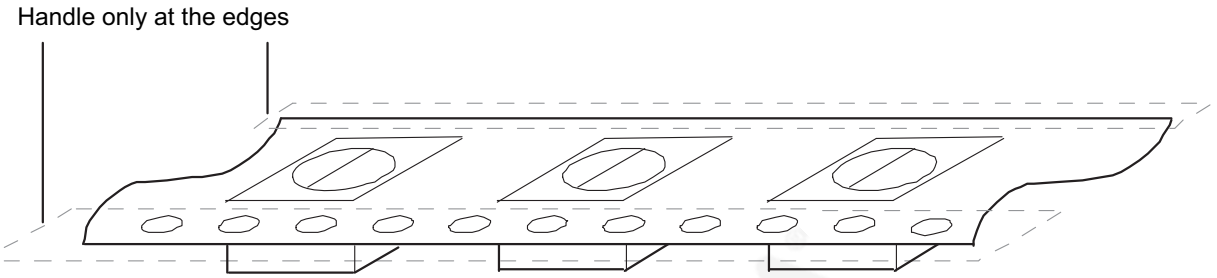


Figure 5-2 Tape handling

5.2 Storage

5.2.1 Bagged storage conditions

PM8941 devices delivered in tape and reel carriers must be stored in sealed, moisture barrier, antistatic bags. Refer to the *IC Packing Methods and Materials Specification* (80-VK055-1) for the expected shelf life.

5.2.2 Out-of-bag duration

The out-of-bag duration is the time a device can be on the factory floor before being installed onto a PCB. It is defined by the device MSL rating, as described in Section 4.4.

5.3 Handling

Tape handling was described in Section 5.1.1. Other (IC-specific) handling guidelines are presented below.

5.3.1 Baking

Wafer-level packages such as the 229 WLNSP should not be baked.

5.3.2 Electrostatic discharge

Electrostatic discharge (ESD) occurs naturally in laboratory and factory environments. An established high-voltage potential is always at risk of discharging to a lower potential. If this discharge path is through a semiconductor device, destructive damage may result.

ESD countermeasures and handling methods must be developed and used to control the factory environment at each manufacturing site.

Qualcomm products must be handled according to the ESD Association standard: ANSI/ESD S20.20-1999, *Protection of Electrical and Electronic Parts, Assemblies, and Equipment*.

Refer to Section 7.1 for the PM8941 ESD ratings.

5.4 Barcode label and packing for shipment

Refer to the *IC Packing Methods and Materials Specification* (80-VK055-1) for all packing-related information, including barcode-label details.

6 PCB Mounting Guidelines

6.1 RoHS compliance

The device is lead-free and RoHS-compliant. Its SnAgCu solder balls use SAC405 composition. QTI defines its lead-free (or Pb-free) semiconductor products as having a maximum lead concentration of 1000 ppm (0.1% by weight) in raw (homogeneous) materials and end products. Qualcomm package environmental programs, RoHS compliance details, and tables defining pertinent characteristics of all Qualcomm IC products are described in the *IC Package Environmental Roadmap* (80-V6921-1).

6.2 SMT parameters

This section describes Qualcomm board-level characterization process parameters. It is included to assist customers with their SMT process development; it is not intended to be a specification for their SMT processes.

6.2.1 Land pad and stencil design

The land-pattern and stencil recommendations presented in this section are based on Qualcomm internal characterizations for lead-free solder pastes on an eight-layer PCB, built primarily to the specifications described in JEDEC JESD22-B111.

Qualcomm recommends characterizing the land patterns according to each customer's processes, materials, equipment, stencil design, and reflow profile prior to PCB production. Optimizing the solder stencil pattern design and print process is critical to ensure print uniformity, decrease voiding, and increase board-level reliability.

General land-pattern guidelines:

- Non-solder-mask-defined (NSMD) pads provide the best reliability.
- Keep the solder-able area consistent for each pad, especially when mixing via-in-pad and non-via-in-pad in the same array.
- Avoid large solder mask openings over ground planes.
- Traces for external routing are recommended to be less than or equal to half the pad diameter, to ensure consistent solder-joint shapes.

One key parameter that should be evaluated is the ratio of aperture area to sidewall area, known as the area ratio (AR). Qualcomm recommends square apertures for optimal solder-paste release. In this case, a simple equation can be used relating the side length of the aperture to the stencil thickness (as shown and explained in Figure 6-1). Larger area ratios enable better transfer of solder paste to the PCB, minimize defects, and ensure a more stable printing process. Inter-aperture spacing should be at least as thick as the stencil; otherwise, paste deposits may bridge.

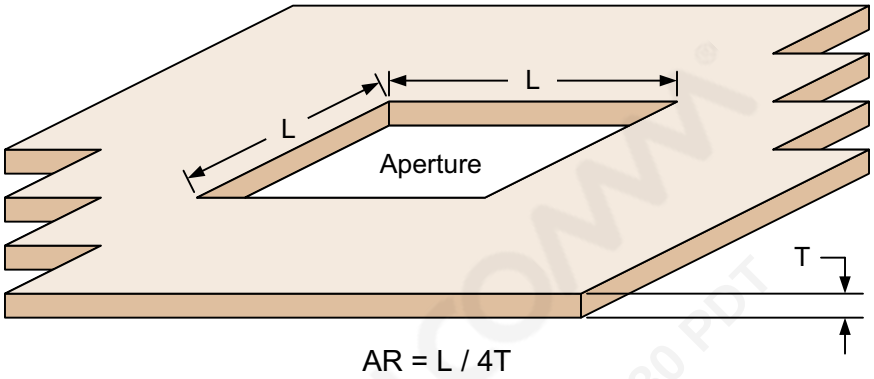


Figure 6-1 Stencil printing aperture area ratio (AR)

Guidelines for an acceptable relationship between L and T are listed below, and are shown in Figure 6-2:

- R = L/4T > 0.65 – best
- 0.60 ≤ R ≤ 0.65 – acceptable
- R < 0.60 – not acceptable

Stencil Aperture L (µm)	Stencil thickness, T (µm)							
	75	80	85	90	95	100	105	110
210	0.70	0.66	0.62	0.58	0.55	0.53	0.50	0.48
220	0.73	0.69	0.65	0.61	0.58	0.55	0.52	0.50
230	0.77	0.72	0.68	0.64	0.61	0.58	0.55	0.52
240	0.80	0.75	0.71	0.67	0.63	0.60	0.57	0.55
250	0.83	0.78	0.74	0.69	0.66	0.63	0..60	0.57
260	0.87	0.81	0.76	0.72	0.68	0.65	0.62	0.59

Figure 6-2 Acceptable solder-paste geometries

Qualcomm provides an example PCB land pattern and stencil design for the 229 WLNSP package.

NOTE Click the link below to download the 229 WLNSP land/stencil drawing (LS90-NA220-1) from the CDMA Tech Support Website.

https://downloads.cdmatech.com/qdc/drl/objectId/0901001481a1b0fd

If you have permission to view the document, a prompt will be presented for initiating the download.

NOTE Subscribe to the land/stencil drawing to be notified of any changes.

Click the **Help** button to download the latest revision of *Using CDMA Tech Support Documents and Downloads User Guide* (80-V7273-1). This document includes subscription instructions.

6.2.2 Reflow profile

Reflow profile conditions typically used by Qualcomm for lead-free systems are listed in Table 6-1, and are shown in Figure 6-3.

Table 6-1 Qualcomm typical SMT reflow profile conditions (for reference only)

Profile stage	Description	Temp range	Condition
Preheat	Initial ramp	< 150°C	3°C/sec max
Soak	Flux activation	150 to 190°C	60 to 75 sec
Ramp	Transition to liquidus (solder-paste melting point)	190 to 220°C	< 30 sec
Reflow	Time above liquidus	220 to 245°C [1]	50 to 70 sec
Cool down	Cool rate – ramp to ambient	< 220°C	6°C/sec max

1. During the reflow process, the recommended peak temperature is 245°C (minimum). This temperature should not be confused with the peak temperature reached during MSL testing, as described in Section 6.2.3.

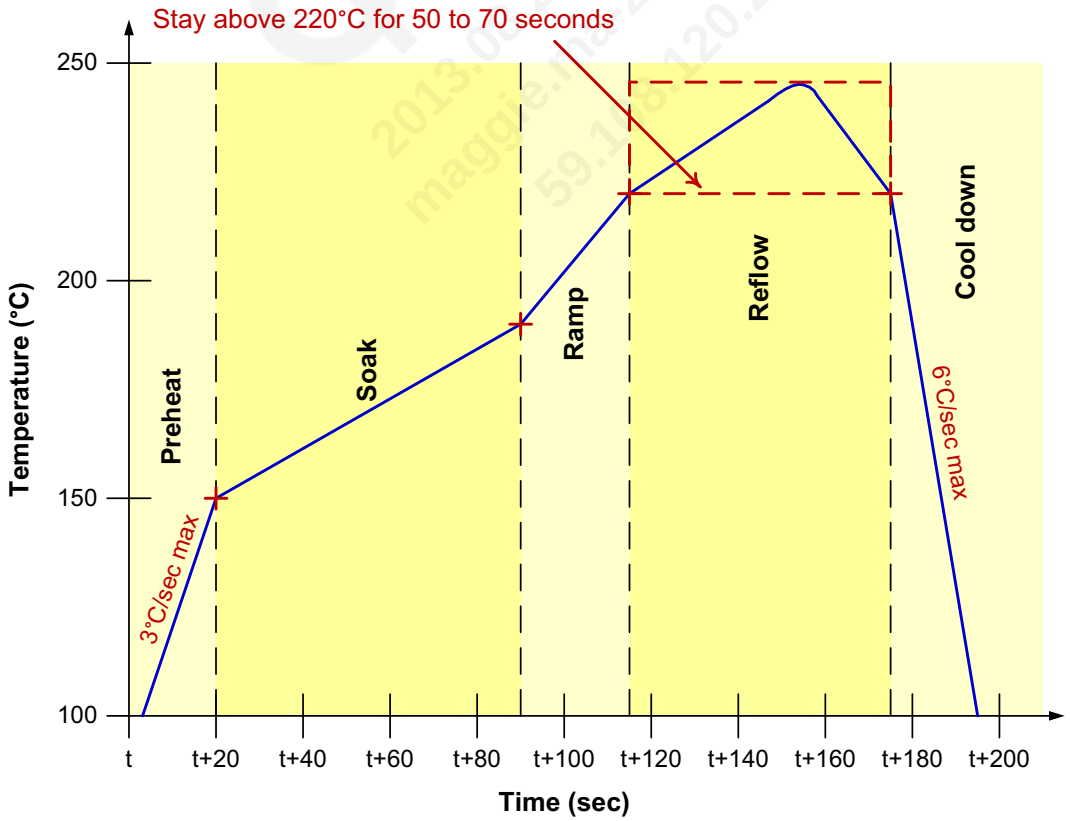


Figure 6-3 Qualcomm typical SMT reflow profile

6.2.3 SMT peak package-body temperature

This document states a peak package-body temperature in three other places within this document, and without explanation, they may appear to conflict. The three places are listed below, along with an explanation of the stated value and its meaning within that section's context.

1. Section 4.4 – *Device moisture-sensitivity level*

   PM8941 devices are classified as MSL2@250°C. The temperature (250°C) included in this designation is the lower limit of the range stated for moisture resistance testing during the device qualification process, as explained in #2 below.

2. Section 7.1 – *Reliability qualifications summary*

   One of the tests conducted for device qualification is the moisture resistance test. Qualcomm follows J-STD-020-C, and hits a peak reflow temperature that falls within the range of 260°C +0/-5 °C (255°C to 260 °C).

3. Section 6.2.2 – *Reflow profile*

   During a production board's reflow process, the temperature seen by the package must be controlled. Obviously, the temperature must be high enough to melt the solder and provide reliable connections. However, it must not go so high that the device might be damaged. The recommended peak temperature during production assembly is 245°C. This is comfortably above the solder melting point (220°C), yet well below the proven temperature reached during qualification (250°C or more).

6.2.4 SMT process verification

Qualcomm recommends verification of the SMT process prior to high-volume board assembly, including:

- In-line solder-paste deposition monitoring
- Reflow-profile measurement and verification
- Visual and x-ray inspection after soldering to confirm adequate alignment, solder voids, solder-ball shape, and solder bridging
- Cross-section inspection of solder joints for wetting, solder-ball shape, and voiding

6.3 Daisy-chain components

Daisy-chain packages use the same processes and materials as actual products; they are recommended for SMT characterization and board-level reliability testing. In fact, all SMT process recommendations discussed above can be performed using daisy-chain components.

Ordering information is given in Section 4.3.2.

Daisy-chain PCB routing recommendations are available for download.

NOTE Click the link below to download the 229 WLNSP daisy-chain interconnect drawing (DS90-NA220-1) from the CDMA Tech Support Website.

https://downloads.cdmatech.com/qdc/drl/objectId/0901001481a1b54e

If you have permission to view the document, a prompt will be presented for initiating the download.

NOTE Subscribe to the daisy-chain interconnect drawing to be notified of any changes.

Click the **Help** button to download the latest revision of *Using CDMA Tech Support Documents and Downloads User Guide* (80-V7273-1). This document includes subscription instructions.

6.4 Board-level reliability

Qualcomm conducts characterization tests to assess the device's board-level reliability, including the following physical tests on evaluation boards:

- Drop shock (JESD22-B111)
- Temperature cycling (JESD22-A104)
- Cyclic bend testing – optional (JESD22-B113)

Board-level reliability data is available for download.

NOTE Click the link below to download the 229 WLNSP board-level reliability data (BR80-TBD) from the CDMA Tech Support Website.

This link will be included in future revisions of this document.

If you have permission to view the document, a prompt will be presented for initiating the download.

NOTE Subscribe to the board-level reliability document to be notified of any changes.

Click the **Help** button to download the latest revision of *Using CDMA Tech Support Documents and Downloads User Guide* (80-V7273-1). This document includes subscription instructions.

7 Part Reliability

7.1 Reliability qualifications summary

Table 7-1 PM8941 IC reliability evaluation

Tests, standards, and conditions	Sample size	Result
Average failure rate (AFR) in FIT (λ) failure in billion device-hours **HTOL**: JESD22-A108-D	231	0F/48 ELFR = 727DPPM AFR=16 FITs
Mean time to failure (MTTF) t = 1/λ in million hours	231	64 MHrs
ESD - human-body model (HBM) rating JESD22-A114-F	3	±1500 V [1]
ESD - charge-device model (CDM) rating JESD22-C101-D	3	±500 V
Latch-up (I-test): EIA/JESD78C Trigger current: ±100 mA; temperature: 85ºC	6	±100 mA
Latch-up (Vsupply overvoltage): EIA/JESD78C Trigger voltage: stress at 1.5 × Vdd max per device specification; temperature: 85ºC	6	6.6 V
Moisture resistance test (MRT): J-STD-020C Reflow @ 260 +0/-5ºC	462	MSL1 pass
Temperature cycle: JESD22-A104-D Temperature: -55ºC to 125ºC; number of cycles: 1000 Soak time at minimum/maximum temperature: 8-10 minutes Cycle rate: 2 cycles per hour (cph) **Preconditioning**: JESD22-A113-F MSL1, reflow @ 260 +0/-5ºC	231	Pass
Unbiased highly accelerated stress test (HAST) JESD22-A118; 130ºC / 85% RH and 96 hrs **Preconditioning**: JESD22-A113-F MSL1, reflow @ 260 +0/-5ºC	231	Pass
High-temperature storage life: JESD22-A103-C Temperature = 150ºC; time= 1000 hours	231	Pass
Physical dimensions: JESD22-B100-A	75	Pass
Solder ball shear JESD22-B117	30	Pass

Table 7-1 PM8941 IC reliability evaluation (cont.)

Tests, standards, and conditions	Sample size	Result
Internal/external visual Ball diameter, height & x-ray	30	Pass
Flammability UL-STD-94 Flammability test - not required		See Note.
Note: QTI ICs are exempt from the flammability requirements due to their sizes per UL/EN 60950-1, as long as they are mounted on materials rated V-1 or better. Most PWBs onto which Qualcomm ICs mounted are rated V-0 (which is better than V-1).		

1. HBM ESD rating is 1500 V with the following minor exceptions:
   a) VIB_DRV_N to GND ⟶ 500 V HBM rating
   b) VREG_XO to VREG_RF_CLK ⟶ 1 kV HBM rating

   All other pins meet 1500 V HBM ESD rating.

7.2 Qualification sample description

Device characteristics

Device name: PM8941

Package type: 229 WLNSP

Package body size: 6.15 mm × 5.82 mm × 0.55 mm

Lead count: 229

Lead composition: SAC405

Fab process: 0.18 µm CMOS

Fab sites: GF, Fab3, Singapore; TSMC, Fab5, Taiwan

Assembly sites: StatsChipPac, SCS, Singapore; Amkor, ATC, China; ASE, ASE-kh, Taiwan

Solder ball pitch: 0.4 mm