Qualcomm TECHNOLOGIES, INC



# MSM8974 Power Management Overview

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# Revision History

| Rev | Date | Description |
|---|---|---|
| A | Aug 2012 | Initial release |
| B | Jan 2013 | Numerous changes were made to this document; it should be read in its entirety. |

# Contents

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- Power-Aware Chipset Architecture
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# Power

# Power

- Power = active power + static leakage
  - $P_{LOSS} = \alpha C V_{DD}^2 f + V_{DD} I_{LEAK}$

    Where α = factor related to effective percent of gates switching,
    C = circuit capacitance, f = clock frequency, $I_{LEAK}$ = leakage current.
  - Static leakage loss increases as process geometry decreases.
  - The dynamic power increases quadratically with the operating voltage $V_{DD.}$
  - The leakage is due primarily to gate and channel leakage in each transistor that is left “on” but idle.
  - Leakage power manifests itself in both Active and Standby modes of operation and can dominate dynamic power, especially as the process technology scales down.
  - While the process scaling improves transistor density, functionality, and higher performance on-chip, it also results in leakage power increase.
  - Leakage is critically dependent upon the operating temperature (exponentially) and $V_{DD}$ and is not dependent on the software application that is running.

# Power (cont.)

- Fundamental ways to reduce power consumption
  - Reduce power supply voltage $V_{DD}$ when appropriate
  - Run at a lower clock frequency when appropriate
  - Disable functional units with control signals when not in use
  - Disconnect parts from power supply when not in use
- Power management in mobile devices requires a comprehensive effort across:
  - Processor design
  - Chipset architecture
  - System and software design



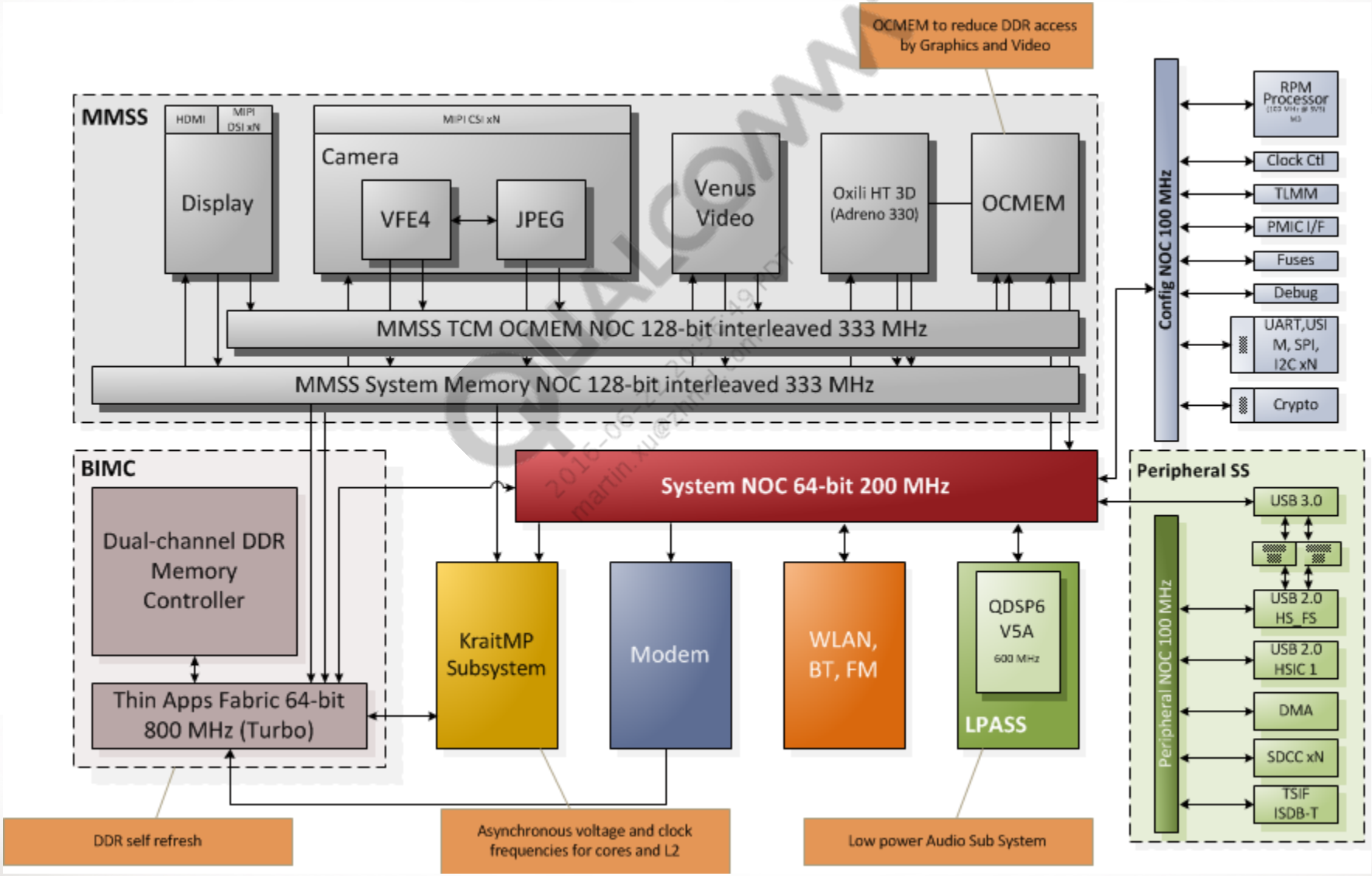
 

# Power-Aware Chipset Architecture

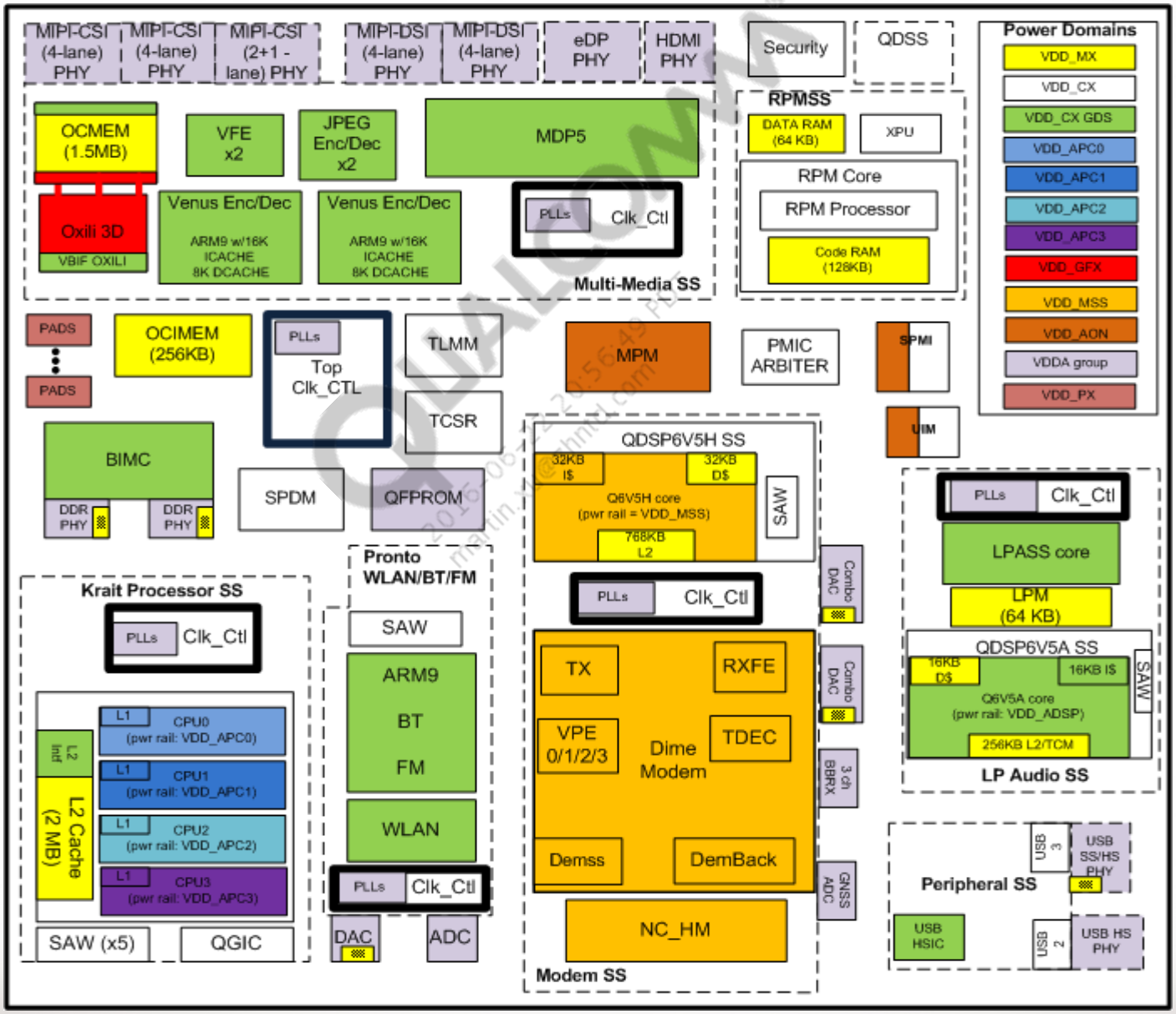
# MSM8974 Overview

- CPU – Quad 2.0+ GHz Krait apps processors
- Processor technology – HPM process, better active power, faster peak CPU
- Memory – Dual channel (2 x 800 MHz) LPDDR3 POP, eMMC 4.5
- GPU – Adreno™ 330, 500 MHz GPU
- Video – 1080p @ 120 fps HD video decode; 2x1080p @ 60 fps encode/decode; Venus ARM9™ video core processor
- Camera – Dual ISP; 32 MP, 15 fps; 16 MP, 30 fps
- Display – 2560x2048 display, HDMI interface
- Audio – Hexagon™ processor V5A, 600 MHz; WCD9320 codec; SLIMbus
- RF – WTR1605(L)
- Modem – LTE Cat 4, DC-HSPA+ Cat 28, DO Rev A/B, UMTS/EGPRS, TD-SCDMA
- PMIC – PM8941/PM8841
- Connectivity – WCN3660/WCN3680 WLAN (a/b/g/n/ac), Bluetooth (BT) 4.0, FM Rx/Tx
- NFC – QCA1990
- aSMP hardware design – Independent core voltage and clocks for each CPU
- Asynchronous L2 independent of core frequency
- Adaptive Voltage Scaling (AVS) on Krait, graphics, modem, and digital core

# MSM8974 Chip Architecture



# Voltage Domains in MSM8974



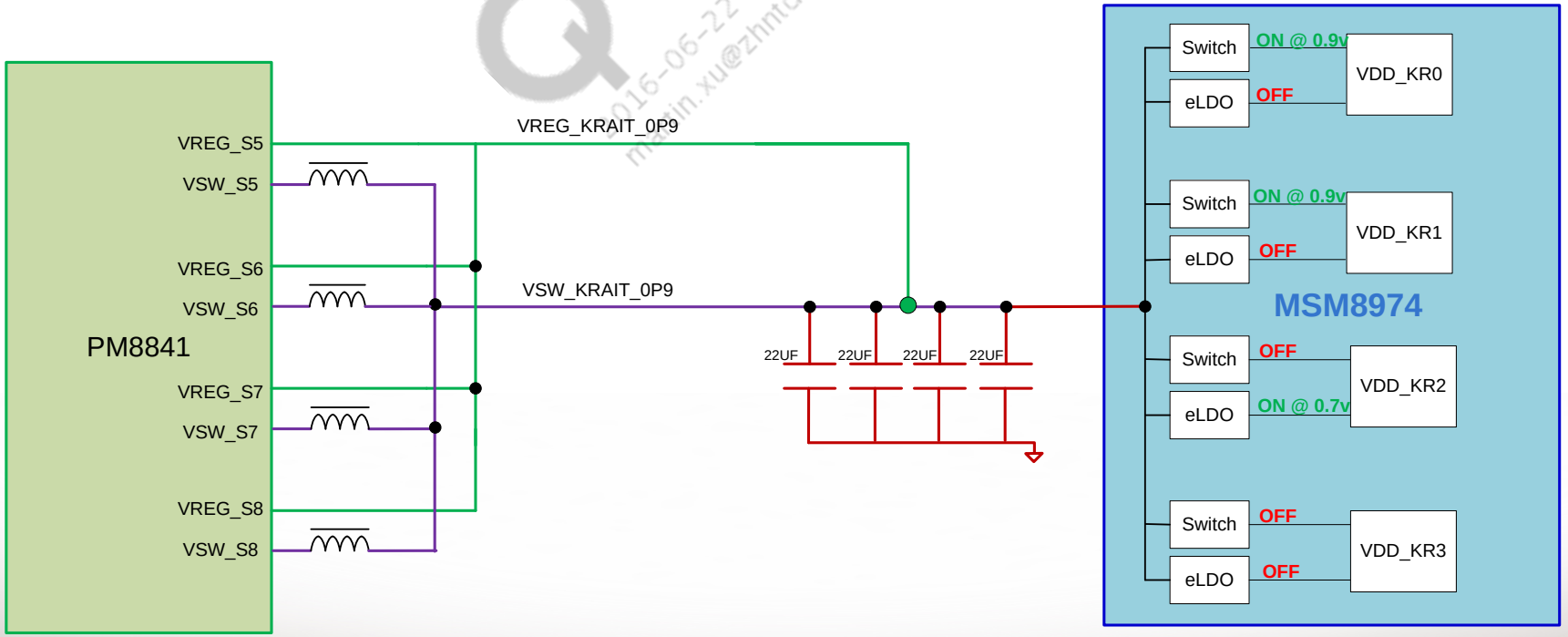
# Power-Aware Chipset Architecture

- Power domains
  - Individual control on power domains makes it possible to power-collapse blocks that are not needed to reduce leakage power
  - Split power rails for CX, modem, and graphics; active power reduction by controlling voltage levels for individual domains
  - Separate memory and CX rails to allow VDDcx to be lowered below VDDmx retention to reduce leakage
  - Multiphase buck for Krait cores
    - Each core subregulated (asynchronously) with on-die LDO for lower performance operating point per core
    - AVS voltage is applied while aggregating MAX request from all Kraits

| Subsystem | Block | Power domain |
|---|---|---|
| MPM | — | VDDaod |
| Memories | — | VDDmx |
| Multimedia SS | MDP5 | VDDcx |
| | VFE | VDDcx |
| | JPEG | VDDcx |
| | Venus 1080P | VDDcx |
| | Oxili | VDDgfx |
| | OCMEM_Int | VDDcx |
| Modem | Q6V5H | VDDmss |
| | NAV | VDDmss |
| Dime | Tx | VDDmss |
| | Rx | VDDmss |
| | Demback/Decob | VDDmss |
| | Demfront/mpif | VDDmss |
| | VPE | VDDmss |
| LPASS/Sensor | Q6V5A | VDDcx |
| | LPASS core | VDDcx |
| Pronto | ARM9 SS | VDDcx |
| | WLAN | VDDcx |
| | BT & FM | VDDcx |
| Krait SS | CPU0 | VDDapc0 |
| | CPU1 | VDDapc1 |
| | CPU2 | VDDapc2 |
| | CPU3 | VDDapc3 |
| | L2INTF | VDDcx |
| BIMC | BIMC | VDDcx |
| Peripherals SS | USB HSIC | VDDcx |

# Krait Power Supply – Example Use Case

- In certain use cases, assume that the following voltages are required by the four Kraits:
  - Krait 0 – 0.9 V
  - Krait 1 – 0.9 V
  - Krait 2 – 0.7 V
  - Krait 3 – OFF
- The above voltages are implemented as shown in the diagram.
- By default, only VREG_S5 is turned On. Based on the current requirement, the MSM will turn On other SMPSs using SPMI commands.



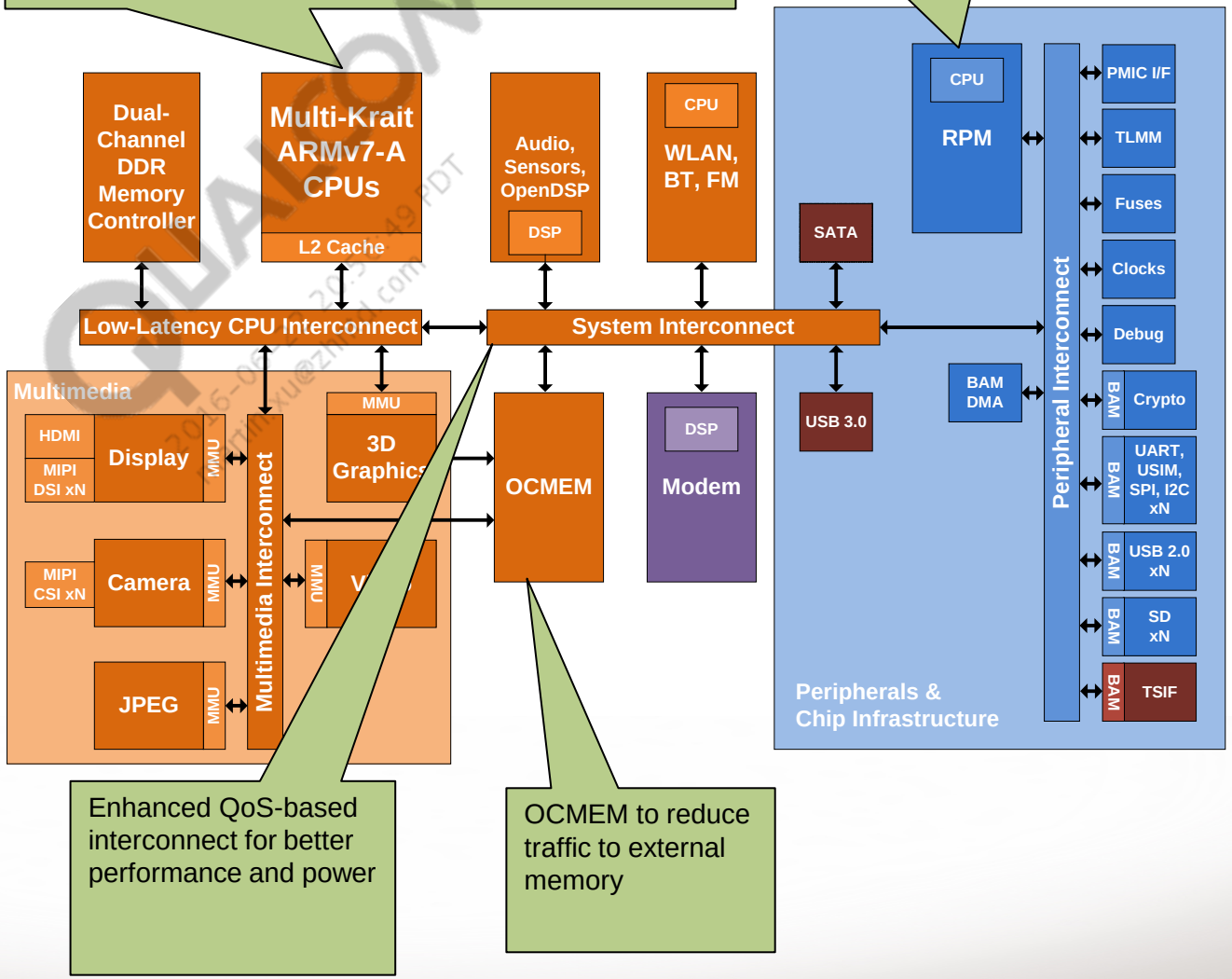
# MSM8974 Power Architecture Concepts

- Low Power System and SoC techniques across the chipset
  - Activity-driven clock gating
  - DDR Controller auto self-refresh entry/exit
  - PMIC auto switching between modes for better efficiency
  - Distributed, fine-grain energy management in hardware
  - Collapsible XPUs
  - Optimized timeline operations including WAN Standby, WLAN/BT power
  - Low leakage, voltage retention mode, with efficient switching in and out of retention

- Improved Active power from 28 HPM technology
- Multiple voltage domains – CPU core0/1/2/3, GRP, modem, digital, memory
- Collapsible logic domains and memories
- Voltage scaling
  - Each CPU core scales in fine voltage steps
  - Other core support – Turbo, nominal, low, and retention voltage levels
- Deep sleep modes to save leakage

- Low power/high performance proprietary design
- Improved/faster CPU power collapse
- Asynchronous clock frequencies for cores and L2

Coarse grain, use-case level-energy management using RPM, with hardware acceleration for resource control

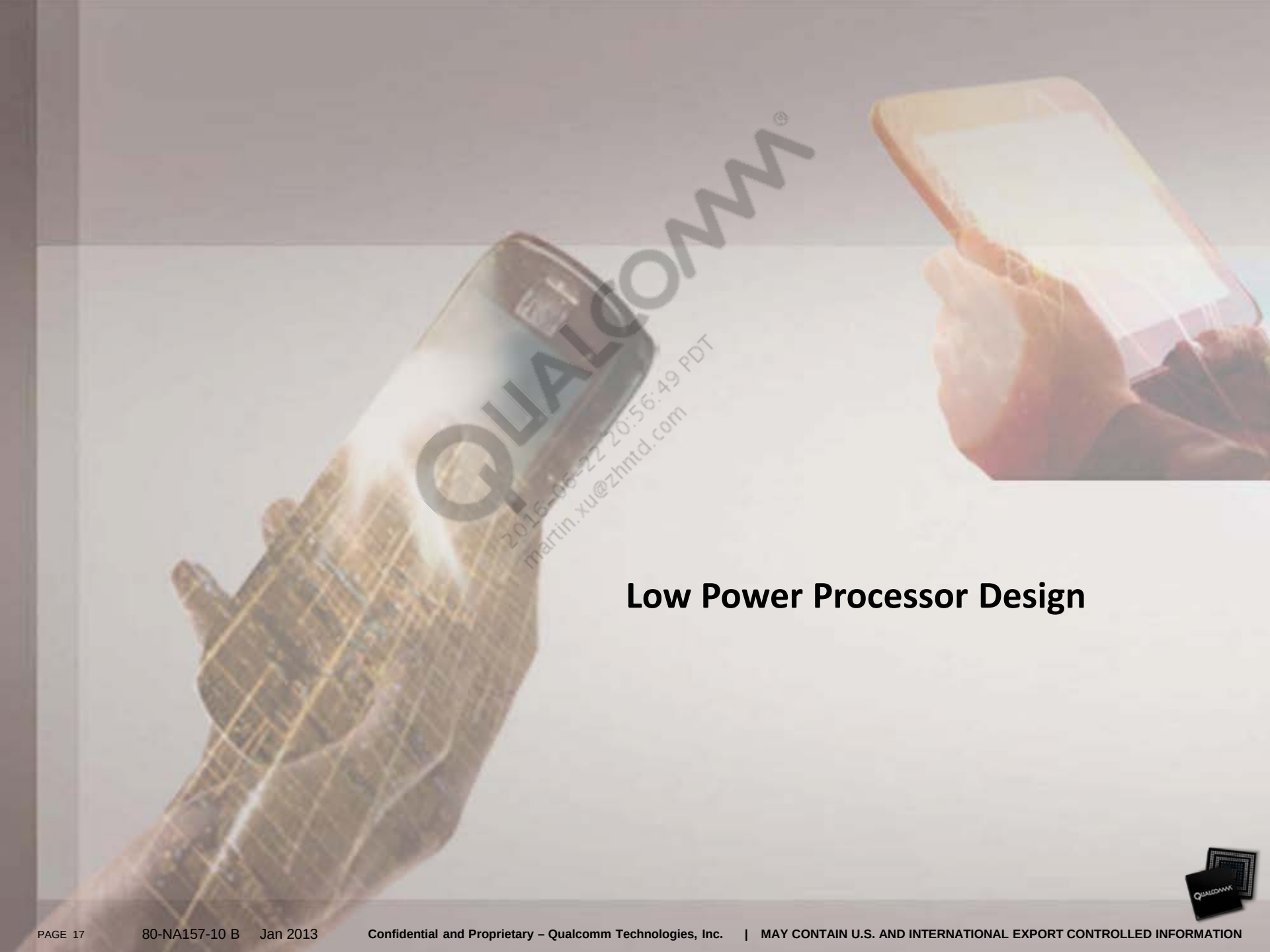


# Power-Aware Architecture

- Single XO
  - CXO (19.2 MHz) sources all clocks. CXO is always on; only its buffers are turned off when XO shutdown is exercised. The sleep clock (32 kHz) used by the MSM™ chipset when in XO Shutdown mode is derived from CXO; it is used to clock always-on domains such as the MSM Power Manager (MPM), parts of the modem core, and certain timer circuits.
  - There is no PXO warm-up time penalty as was the case in MSM8960.
- Improved active power from 28 HPM technology
  - 28 HPM is the high performance for mobile applications (HPM) technology that provides better speed than 28 High Performance (HP) and similar leakage power as 28 Low Power (LP). This gives better power for active use cases.
- Multiple voltage domains – CPU core0/1/2/3, GRP, modem, digital, memory
  - On-die compiler memory voltage, $V_{DD}$ MX, domain is split from the logic domains to allow the logic domains an extended operating range and lower retention voltage (memory voltage does not scale in low power modes with the logic domains).
  - Processor voltage domains are also independent for autonomous voltage and frequency scaling.

# Power-Aware Architecture (cont.)

- Collapsible logic domains, memories, and XPU
  - There are individually collapsible internal memory blocks that can help in power saving when the memory is not in use.
  - Collapsible logic domains are architected that can be power-collapsed through GDS and BHS.
  - VBIF and XPU (security core) are included inside core hard macros and collapsed along with the core to save leakage.
- On-Chip Memory (OCMEM) to reduce traffic to external memory
  - OCMEM is a large chunk of on-chip memory shared between several different cores including Oxili graphics, Venus video codec, LPASS audio, and sensors. It helps save power by reducing traffic to external DDR memory.



# Low Power Processor Design



# Low Power Processor Design

- Process Voltage Setting (PVS)
  - Some SoCs from a wafer or a wafer lot (at a given operating voltage) are capable of achieving higher switching speeds (fast parts) but have higher leakage currents, while others could have a lower maximum achievable speed but dissipate less power through leakage currents (slow or nominal parts).
  - PVS is a technique of identifying minimum operating voltage for each SoC (to meet the required performance) at the production line.
  - Fuses are programmed in individual SoCs with the information about the type of part (fast, nominal, or slow) it is.
  - Software reads the fuses to set the operating voltage for the SoC.
  - Without PVS, all SoCs would use the same higher voltage required for slow parts, causing higher leakage for fast and nominal parts. By adjusting the voltage for the fast and nominal parts, the overall power is normalized among different types of a part.
  - Applicable to Krait only.

# Low Power Processor Design (cont.)

- AVS
  - AVS utilizes the sensors embedded in the SoC that provide real-time feedback on silicon performance based on process and temperature; this closed loop feedback is processed by the software to make granular level $V_{DD}$ adjustments.
  - For example, AVS for digital core (CX) allows for finer voltage adjustment after the part has been determined to be slow, typical, or fast using PVS characterization.
  - AVS helps reduce power deviation by reducing voltage margins that are determined using PVS, thereby further normalizing power and reducing part-to-part variation.
  - In MSM8974, AVS applies to Krait, $V_{DD}$ CX, $V_{DD}$ GFX, and $V_{DD}$ MSS.

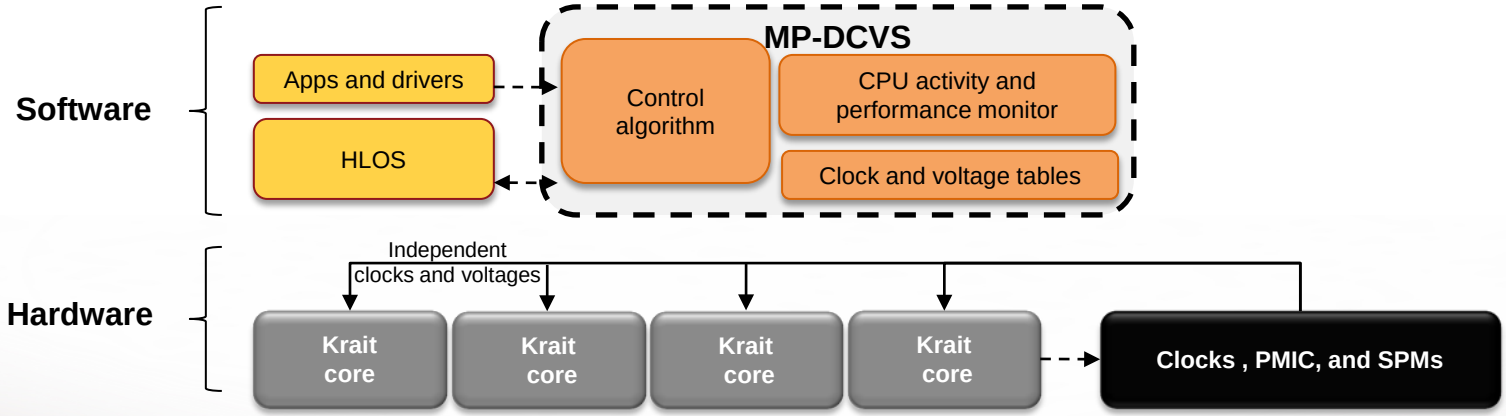
# Low Power Processor Design (cont.)

- Clock gating
  - Dynamic (hardware) clock gating provides the most amount of active power reduction for any design.
  - Shutting off the clock for a circuit prevents any switching activity of the clocks or registers in a design.
  - When not being switched, the switching power consumption goes to zero, and only leakage currents are incurred because the $V_{DD}$ supply is still on.
  - MSM8974 provides the ability to gate video, GFX, MDP, VFE, VPE, and JPEG/ rotator core clocks.
  - There is better clock gating efficiency in NOC.
- Power gating (power-collapse)
  - Power gating provides the most amount of leakage power savings for a device in Standby mode. Since leakage current is a significant factor in terms of power consumption, the chip is designed so that certain blocks can be temporarily shut down when they are not in use.
  - However, there is a higher recovery penalty to resume the Active state.
- DDR Auto Self-Refresh
  - Hardware-based DDR Self-Refresh mode automatically reduces power when idle and improves transient response by bringing it out of self-refresh on activity.

# Low Power System Design

# Low Power System Design

- Krait MP-Dynamic Clock and Voltage Scaling (DCVS) with MP-decision
  - DCVS in general utilizes the asynchronous clocking and independent voltage power domains
  - MP-DCVS (CPU governor) – Algorithm scales the clock the minimum frequency (for individual core) that meets the required QoS and adjusts the corresponding (statically determined) voltage
  - MP-decision – Monitors the load on CPUs to determine if additional cores should be powered up or a core needs to be power-collapsed
  - Uses per CPU thermal inputs
  - Reduces active and leakage current



# Low Power System Design (cont.)

- GPU DCVS
  - A low overhead algorithm that runs whenever GPU fires an interrupt to CPU; this turns itself off when the GPU is heavily loaded. It essentially dynamically scales the GPU frequency based on the load and, hence, reduces system power consumption for the active GPU use cases without negatively impacting performance. It has been tested across a variety of benchmarks and applications with no significant performance issues and power savings of up to approximately 20% observed on low usage applications.
- MSS DCVS
  - MSS DCVS is also referred to as CPU dynamics; it scales the CPU clock based on measured CPU utilization and MIPS request from clients. As a consequence of a CPU clock change, CPU dynamics would make implicitly instantaneous bus bandwidth requests to the bus arbiter for CPU data and instruction access from CPU to DDR.
- ADSP frequency scaling
  - ADSP CPU frequency scaling is done statically based on a client's MIPS request, e.g., audio driver, sensor driver. Due to a power grid change on MSM8974, there is no dedicated power rail for ADSP. As a result, ADSP frequency scaling would incur a $V_{DD}$ CX vote to the Resource Power Manager (RPM), as necessary.

# Low Power System Design (cont.)

- Static Voltage Scaling (SVS)
  - SVS refers to software-based setting the voltage of a core to a predetermined value to meet the system performance requirements
  - Applicable to digital core, Hexagon modem, GPU, DDR configuration, etc.
  - AVS on Krait, $V_{DD}$ CX, $V_{DD}$ GFX, VDD MSS further tunes voltage settings
  - MSM8974 has the modes SVS (Low), Nominal, Turbo, and Super Turbo
  - Table 1 shows the $V_{DD}$ CX and $V_{DD}$ MX voltage settings for different modes
  - Table 2 shows mode settings for different DDR frequencies

**Table 1**

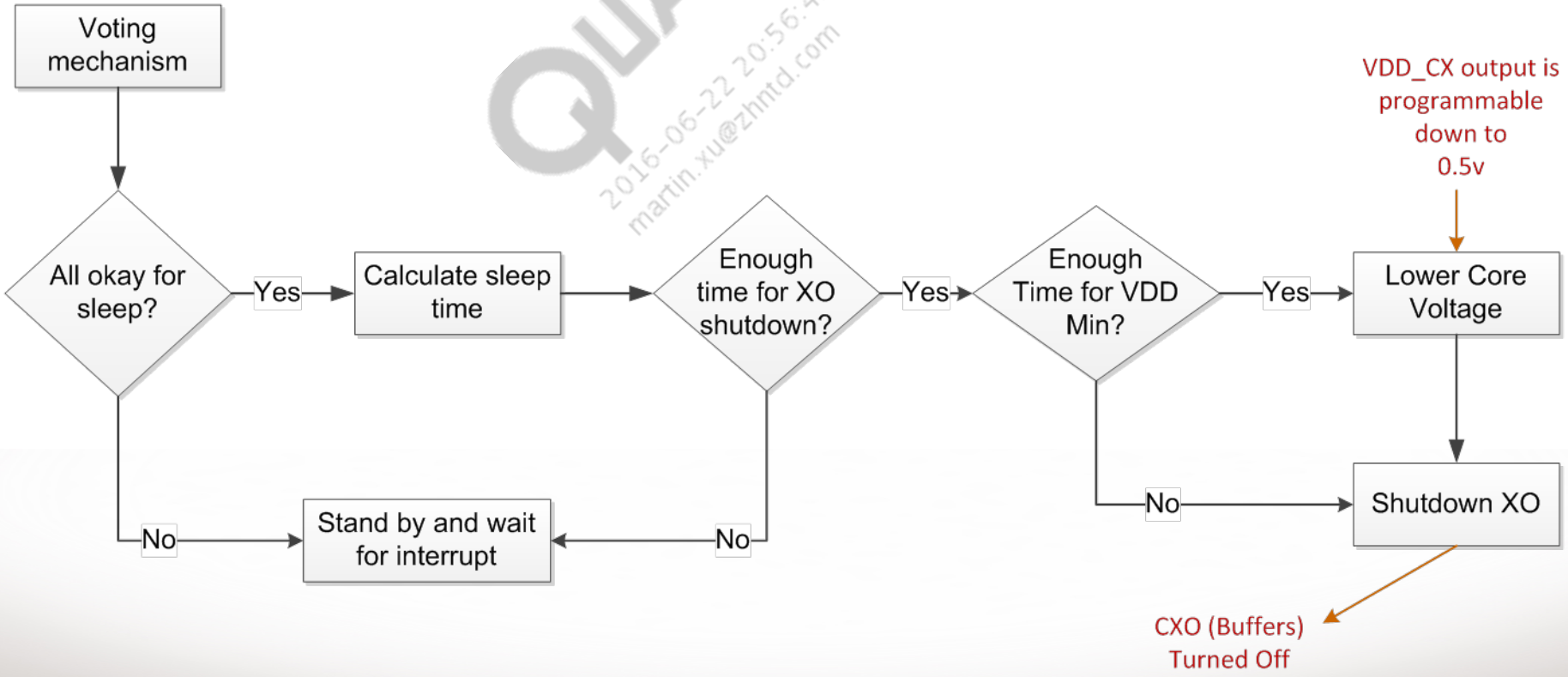
| Mode | Digital core voltage CX (V) | Memory voltage MX (V) |
|---|---|---|
| SVS (Low) | 0.81 | 0.95 |
| Nominal | 0.9 | 0.95 |
| Turbo | 0.99 | 1.05 |
| Super Turbo | 1.05 | 1.05 |

**Table 2**

| Performance level | Frequency (MHz) | Mode |
|---|---|---|
| 0 | 19.2 | SVS (Low) |
| 1 | 37.5 | SVS (Low) |
| 2 | 50 | SVS (Low) |
| 3 | 75 | SVS (Low) |
| 4 | 100 | SVS (Low) |
| 5 | 150 | SVS (Low) |
| 6 | 200 | SVS (Low) |
| 7 | 278.4 | SVS (Low) |
| 8 | 375 | Nominal |
| 9 | 556.8 | Nominal |
| 10 | 750 | Turbo |

# Low Power System Design (cont.)

- XO shutdown
  - XO shutdown disables the clock supply to MSM (apps/modem/ADSP/ W-Connect) for power-saving purposes; shutting down XOs is possible only when the MSM is completely unoccupied and is going to be so for at least some specific amount of time.





# Low Power System Design (cont.)

- XO shutdown (cont.)
  - CXO is always on; only its buffer is turned off when XO shutdown is exercised.
  - All master processors must be in Power-Collapse mode, dedicated clocks should be off, and shared clocks should have “off” vote from their clients.
  - Clock generation of CXO is still kept on at the PMIC and is used to generate the 32 kHz sleep clock.
  - No clock is fed to the MSM except for the 32 kHz sleep clock, which is required for the always-on parts like the MPM block.



# Low Power System Design (cont.)

- $V_{DD}$ minimization
  - $V_{DD}$ minimization is the deepest low power mode that can be achieved for $V_{DD}$ CX and $V_{DD}$ MX.
  - When $V_{DD}$ minimization is achieved, the chip is not operational, except for detecting wakeup interrupt/timer expiration for $V_{DD}$ min; however, all hardware (supplied by $V_{DD}$ CX/MX) states are still maintained. These two power domains cannot be power-collapsed, so they are put to a lower voltage that can sustain the contents in memories, etc.
  - Lowering the voltage still saves some leakage current, and therefore power.
  - XO shutdown conditions must be met before $V_{DD}$ minimization, as XO shutdown must happen after $V_{DD}$ minimization.
  - Retention voltages are $V_{DD}$ CX = 0.5 V and $V_{DD}$ MX = 0.675 V.

# Low Power System Design (cont.)

- Krait low power modes
  - Low power mode when Krait is idle; depending on the duration of idle time for Krait, it can enter SWFI (clock gating), retention (clock gated and retention voltage SVS), standalone power-collapse (clock and power gating), or (IDLE) power-collapse (RPM assisted).
- Modem low power modes
  - MSS supports various low power modes, such as MSS PC, WFI, XO shutdown, $V_{DD}$ minimization, L2 nonretention, etc.; the decision to enter these various LPRMs comes from dynamic sleep, based on latency and power penalty to enter/exit these modes.
- LPASS (Hexagon) power modes
  - Hexagon supports SVS mode (setting of minimum required voltage to support the requested frequency); voting for ADSP power-collapse depends upon its aggregated client requests. ADSP power-collapse and resumption from power-collapse is triggered by notifications from the Sleep task.
- Memory controller (BIMC) power-collapse
  - The Thin-Apps FABRIC and memory controller, which is referred to as Bus Interface Memory Controller (BIMC), can be collapsed in MSM8974 using a GDHS domain to remove leakage of the BIMC. Once BIMC is collapsed, DDR is not accessible.
  - This could be done while portions of the chip are operational; those portions must ensure that DDR will not be accessed.

# Low Power System Design (cont.)

- PMIC Auto mode
  - SMPS operates in Pulse Width Modulation (PWM) mode during active operation (higher voltages) because SMPS efficiency is better when operated in PWM mode at higher voltages.
  - Instead, SMPS should operate in Pulse Frequency Modulation (PFM) mode during low power modes (lower voltages), as the SMPS efficiency is better when operated in PFM mode at lower loads.
  - The PMIC Auto mode feature makes sure that SMPS shifts its mode of operation between PFM and PWM automatically, based on operating conditions to maximize efficiency.
    - RF circuits are powered by LDOs that are subregulated from SMPS; these SMPS can be put in Auto mode (PWM/PFM) for better efficiency.



# Modem Use Cases

# Modem Use Cases and Power Feature Impact

- Power features and impact on modem use cases

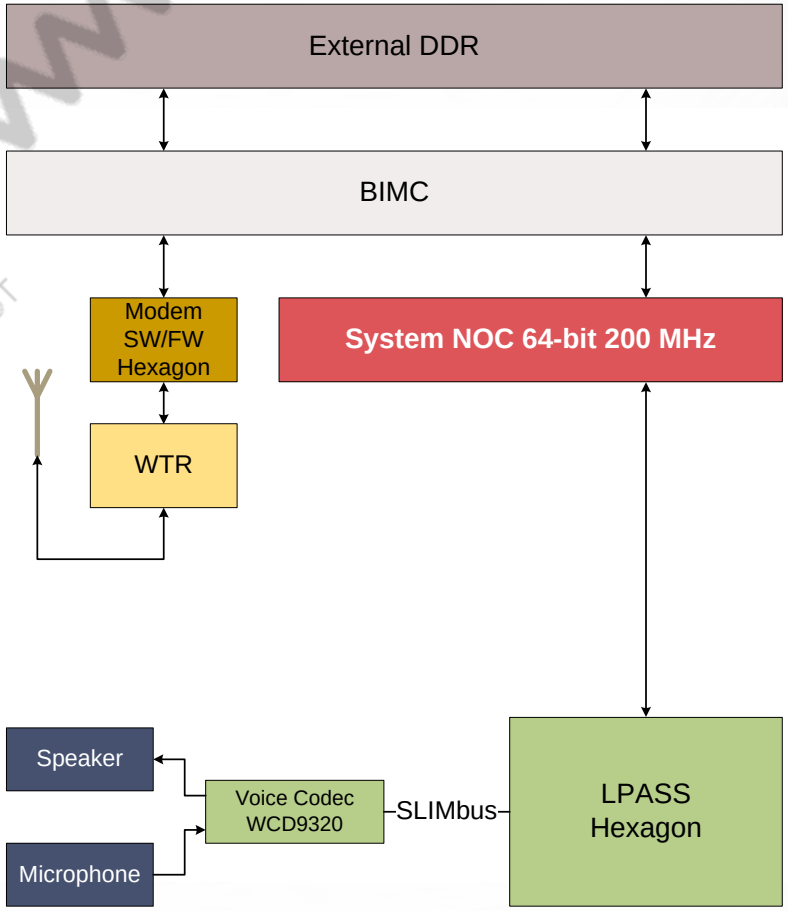
| Power features | Sleep | Awake | Talk | Data |
|---|---|---|---|---|
| XO shutdown | ✓ | | | |
| $V_{DD}$ minimization | ✓ | | | |
| SVS | | ✓ | ✓ | ✓ |
| CX AVS | | ✓ | ✓ | ✓ |
| Modem power collapse | ✓ | | | |
| Krait power collapse | ✓ | ✓ | ✓ | |
| MP-DCVS + MP-decision | | | | ✓ |
| MODEM-DCVS | | ✓ | ✓ | ✓ |
| PMIC Auto mode | | ✓ | ✓ | ✓ |
| DDR Auto self-refresh | ✓ | | | |
| BMIC power-collapse | ✓ | | | |



# Modem Use Cases – W-Talk Data Flow Diagram

- Rx
  1. Antenna receives the signal, which gets processed by the modem hardware for algorithmic processing and Hexagon modem software for protocol stack; the modem demodulates the received signal and produces digital data.
  2. Digital data is stored in DDR; LPASS takes this digital data and processes it; convolutional decoding (speech decoding) is done by LPASS, and the data is converted into raw digital data.
  3. Raw digital data is converted to analog signals in the analog codec.
  4. The analog codec feeds the analog signal to the speaker.
- Tx
  1. Analog voice signals are received through the microphone and sent to the analog codec.
  2. The analog codec does the sampling/ quantization and converts it into digital raw data.
  3. Digital raw data is processed by LPASS; voice/speech encoding is done in LPASS; encoded packets are stored in DDR.
  4. Modem hardware and modem software modulate the data from DDR and add the protocol headers before feeding it to the Tx antenna.



# Modem Use Cases – W-Talk Clock Plan

- W-Talk clock settings

| Clocks | Speed (MHz) | Remarks |
|---|---|---|
| Krait0 | 0 | Power-collapsed |
| Krait1-3 | — | N/A |
| BIMC/DDR-PHY | 100 | |
| DDR | 100 | |
| LPASS Hexagon | 196.6 | |
| Sys-NOC | 50 | |
| MMSS NOC | 0 | Power-collapsed |
| OCMEM | 0 | Power-collapsed |
| GPU, Venus | 0 | Power-collapsed |
| Modem Hexagon | 144 | |
| Peripheral NOC | 19.2 | |
| Config NOC | 37.5 | |

# Modem Use Cases – W-Talk Component Breakdown Projection

- W-Talk component power breakdown

| Components | W-Talk (mA) | Remarks |
|---|---|---|
| MSM digital | 31 | Includes digital current from CX, MSS, and MX |
| Analog | 9 | BBRX, DAC, PLL, and WCD codec |
| DDR | 6 | DDR current |
| PA | 8.5 | Power amplifier |
| RF | 43 | RF portion |
| PMIC, rest | 5 | PMIC internal consumption |
| Total | 103 | |



# Multimedia Use Cases

# Multimedia Use Cases and Power Feature Impact

- Power features and impact on multimedia use cases

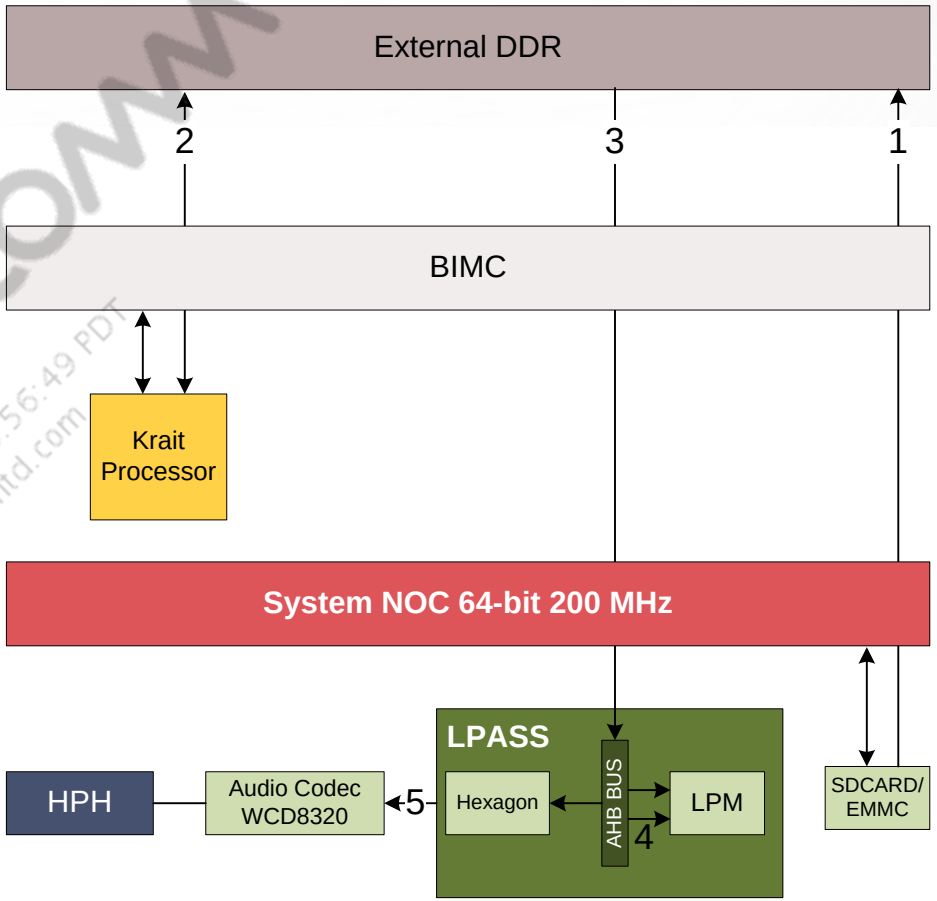
| Power features | Audio | Video |
|---|---|---|
| XO shutdown | | |
| $V_{DD}$ minimization | | |
| SVS | ✓ | ✓ |
| CX AVS | ✓ | ✓ |
| Modem power collapse | ✓ | ✓ |
| Krait power collapse | ✓ | ✓ |
| MP-DCVS + MP-decision | ✓ | ✓ |
| GPU-DCVS | | |
| Modem-DCVS | | |
| SMPS Auto mode | ✓ | ✓ |
| DDR auto self-refresh | ✓ | ✓ |
| Memory controller power collapse (BIMC) | | |



# Multimedia Use Cases – MP3 Data Flow Diagram

1. Krait reads 1 MB of data from SDCARD/EMMC to the DDR.
2. Krait parses the data and puts it in the DDR.
3. LPASS sets up DM-Lite to transfer 32 Kb of bitstream from DDR to LPM.
4. LPASS performs decoding and postprocessing and puts a PCM sample into LPM.
5. LPASS sets up the DMA to render PCM sample to the audio codec.



# Multimedia Use Cases – MP3 Clock Plan

- Audio – MP3 (44.1 kHz, 128 kbps) clock settings and power breakdown

| Clocks | Speed (MHz) | Remark |
|---|---|---|
| MMSS NOC | 0 | MMSS NOC not used |
| System NOC | 19.20 | Always runs to facilitate the data transfer between DDR and subsystems (LPASS/peripheral) |
| OCMEM | 0 | OCMEM not used (subject to change) |
| LPASS Hexagon | 81 | Hexagon never power-collapses during audio playback |
| Periph_NOC_SPSS | 19.2 | SD card data is sent via peripheral; NOC |
| Config NOC | 37.5 | RPM uses the config NOC to interconnect with system NOC |
| Krait0 | 0 (PC)/300 (wakeup) | Krait remains in power-collapsed state except for the short duration when it wakes up to read/parse data from storage |
| SPSS_SDCC | 5.2 | SDCC used by storage (eMMC/SD card) always runs |
| DDR | 19.2 | DDR needs to always run as all SS involved use this memory to store the intermediate data |
| BIMC | 19.2 | BIMC needs to run as DDR is always used and facilitates the data access by Krait/other SSs from DDR |

# Multimedia Use Cases – MP3 Component Breakdown Projection

- MP3 (44.1 kHz, 128 kbps) clock settings and power breakdown

| Components | MP3 Tunnel mode (mA) | Remark |
|---|---|---|
| MSM digital – CX | 9.3 | Digital core – CX always operates in SVS mode |
| MSM digital – MX | 1 | MX operates in Nominal mode |
| Analog | 0.6 | Contributed by BBRX, DAC, PLLs |
| Audio | 2 | Contributed by codec WCD9320 and power amp (Class H) |
| AP | 0.5 | Krait operates in Krait-SVS mode whenever it is active for very short duration while reading/parsing the data read from storage (SD card/ eMMC) |
| DDR | 0.8 | DDR power consumption |
| PMIC, SLIMbus, rest | 1.8 | Rest of the system power contribution |
| Total | 16 | |

# Multimedia Use Cases – Configurable Software and Hardware Factors Impact on Power

- Consolidated software and hardware factors that can impact the power for multimedia use cases

| Factors | MP3 (Tunnel mode) |
|---|---|
| Display resolution | |
| DDR size/DDR part number | ✓ |
| Audio codec/power amplifier | ✓ |
| Smart/dumb panel | |
| Panel type (LCD, AMOLED) | |
| RGB/MIPI display interface | |
| WLAN solution – WCNSS/custom | |
| Camera output resolution | |
| Sensor type – Bayer/YUV | |
| Frame rate/bit rate of content | |
| Rendering (full screen/partial screen) | |
| Composition types (Dyn/GPU/MDP) | |
| Non-tunnel mode (LPA/Non-LPA) | ✓ |
| Tunnel mode/Non-tunnel mode | ✓ |
| Page refresh rate, download, and caching | |

# References

| Ref. | Document | |
|---|---|---|
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| Q2 | *Presentation: Introduction to Graphics DCVS* | 80-N6621-1 |
| Q3 | *AMSS 8974 Current Consumption Data for Linux Android™* | 80-NA437-7 |



# Questions?

**https://support.cdmatech.com**