PM8941 Switch-Mode Battery Charger and Boost (SMBB)

Hardware/Software Application Note

Qualcomm Technologies, Inc.

80-NA555-12 Rev. A

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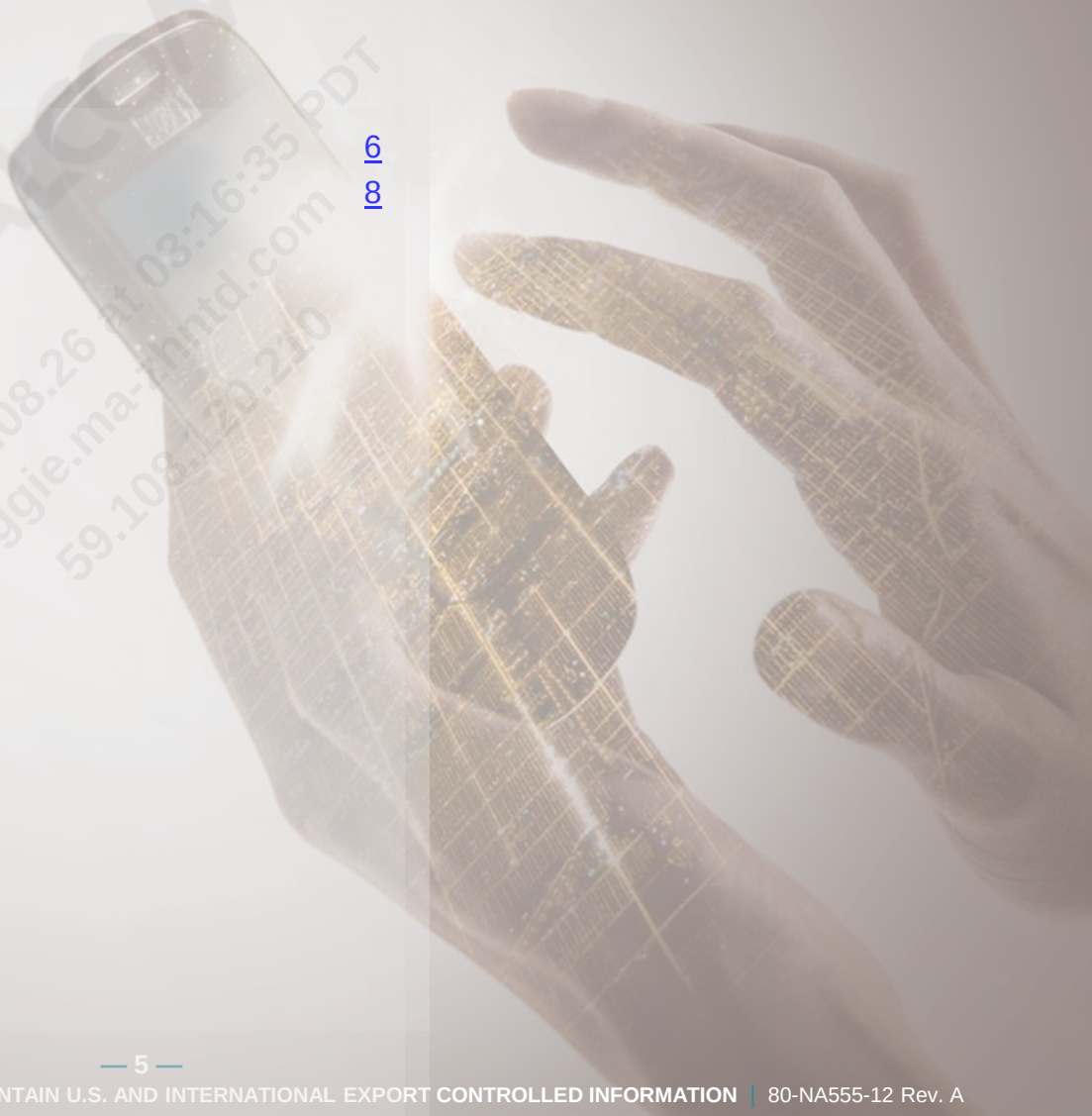
Revision History

Revision	Date	Description
A	December 2012	Initial release

Contents

Introduction



Reference Material

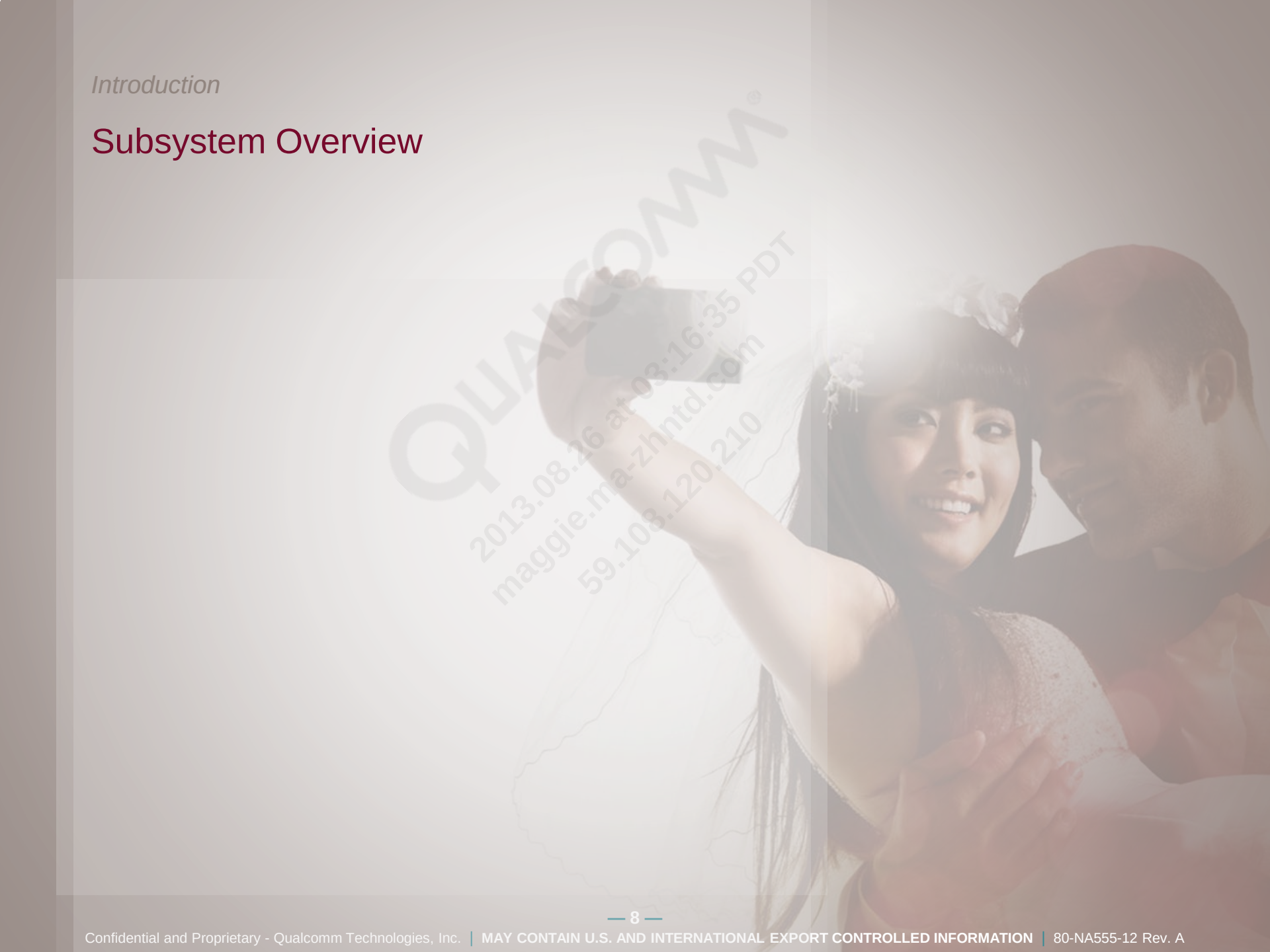
Reference Material

Primary device-specific documents					
PMIC	**Chipset**	**Device specification**	**Software interface**	**Device revision guide**	**Reference schematic**
PM8941	MSM8x74	80-NA555-1		80-NA555-4	80-NA437-41

This document is specific to PM8941.

PMIC hardware/software documents		
Topic	**Document number**	**Document title**
Lighting subsystem	80-NE399-11	*PM8941 Lighting Subsystem Hardware/Software Document*
Battery management subsystem	80-NE399-12	*PM8941 Battery Monitoring System (BMS) Hardware/Software Document*
Switched-mode battery charger	80-NA555-12 (this document)	*PM8941 Switch-Mode Battery Charger and Boost (SMBB) Hardware/Software Application Note*

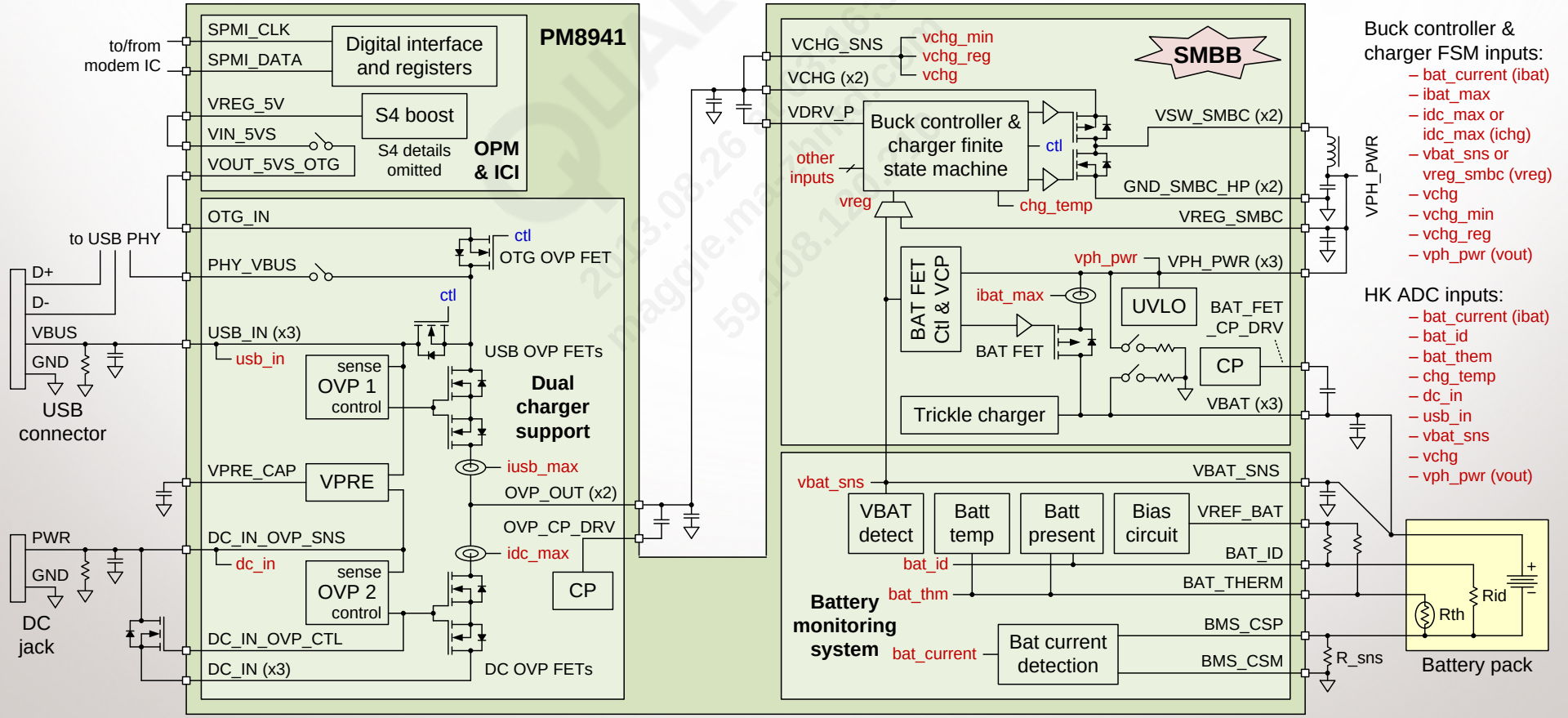
Subsystem Overview



Switch-Mode Battery Charger and Boost Subsystem

The switch-mode battery charger and boost (SMBB) is highlighted (upper right within this figure).
Other major blocks used in SMBB operation are also shown in this figure:

- SPMI digital interface and control registers
- Output power management (+5 V boost converter and voltage switch for universal serial bus on the go [USB-OTG])
- Dual charger support (USB connector or DC jack with over-voltage protection [OVP])
- BMS
- Plus inputs to the HK ADC for monitoring key nodes throughout



Top-level SMBB Subsystem Features

- The switch-mode battery charger (SMBC) was the first generation; its key advantage over a linear regulator is its higher efficiency (and therefore less heat is generated).
- The second generation adds the reverse boosting mode (SMBB).

SMBB features include:

- Top-level functionality
  - Regulate the phone's supply voltage
  - Monitor the main battery current in support of constant current and constant voltage charging modes
  - Limit the input current for USB compliance
  - Programmable minimum input voltage, thereby achieving the maximum power transfer
- 2 A charging current
- 85% efficiency
- 1.6 MHz switching frequency (3.2 MHz is also available)
- Input current sensing
- Semi-autonomous charger control

Four control loops with programmable thresholds:

- Output voltage – 3.5 V to 5.0 V, in 20 mV steps
- Battery current – 0.2 A to 1.5 A, in 50 mA steps and 1.5 A to 2.0 A, in 100 mA steps
- Input voltage limiting – 4.4 V to 5.5 V, in 100 mV steps and 5.5 V to 6.5 V, in 250 mV steps
- USB input current limiting – 0.1 A to 1.8 A
  - 0.1 A and 0.5 A for USB 2.0; 0.15 and 0.9 A for USB 3.0; plus 1.8 A

Trickle charger

Reverse boosting mode provides +5 V at up to 2 A

- Uses: Flash LED driver with adaptive mode; USB-OTG, HDMI, and other LED drivers
- Reliably detects and stops unintended reverse boosting

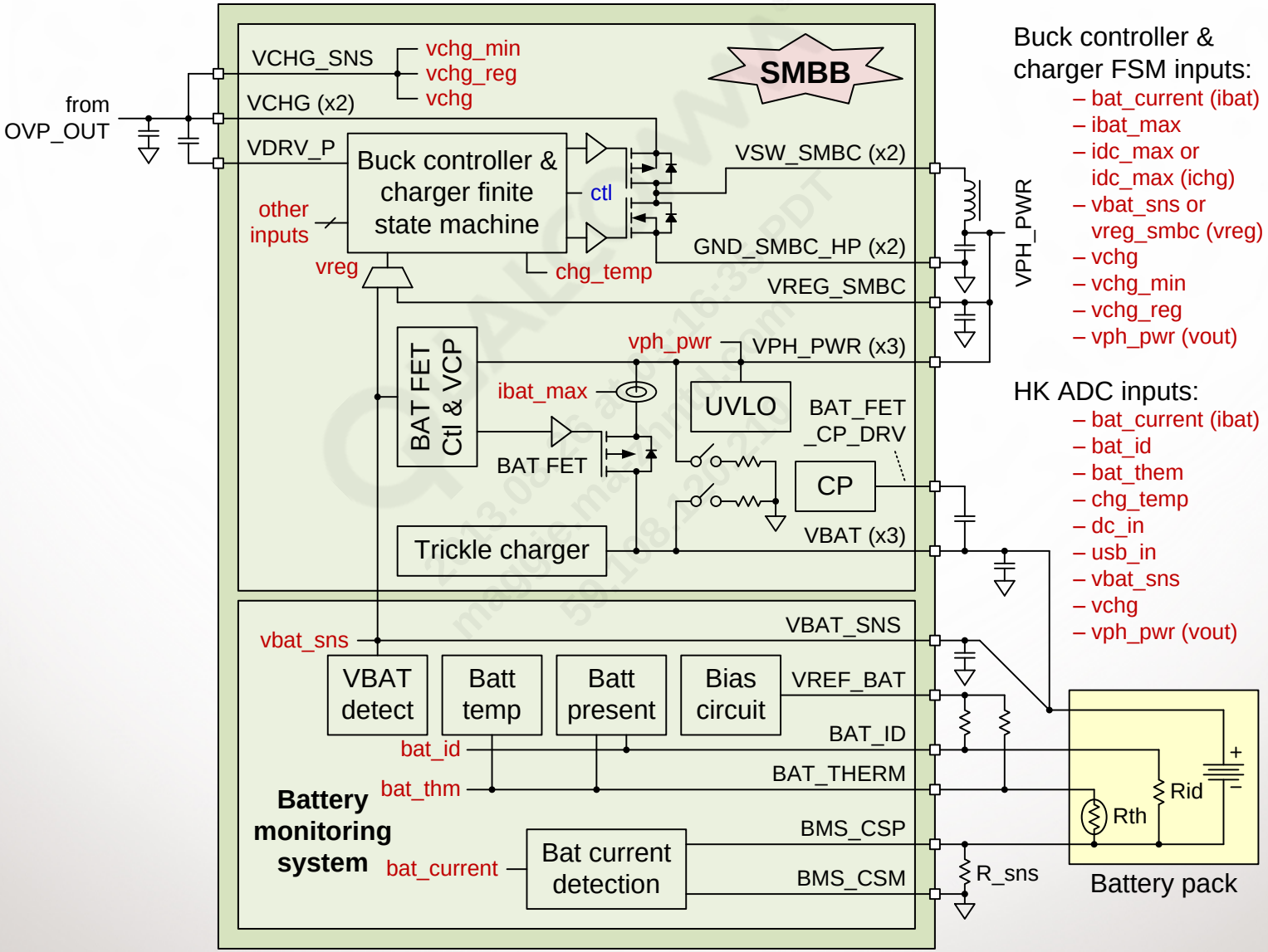
SMBB vs. SMBC

- Higher current rating and higher efficiency
  - Up to 3.0 A current to system and battery
  - Efficiency: 90% at 1.0 A ICHG_OUT; 85% at 2.5 A ICHG_OUT
  - High-current charging IR drop compensation
- Reverse boosting mode provide +5 V rail at up to 2 A
  - Mainly used for the flash LED driver in an adaptive mode to minimize heat
  - Can also be used for USB OTG, HDMI switch, and LED drivers (torch, keypad backlight, and RGB)
  - Reliably detects and stops unintended reverse boosting
- OVP
  - Integrated +15 V OVP FET for DC charging path; input current sensing (for wireless charger) and reverse current blocking; allows an optional external OVP FET to support +30 V OVP tolerance
  - Valid input range expanded to +10 V for both USB and DC charging paths
  - Integrated USB-OTG OVP FET
  - Automatic input current limit (AICL)
- Integrated BAT FET
  - Regulated BAT FET Rds(on) for BMS battery current sensing; makes the external sense resistor optional
- SMBB digital
  - Replaced SSBI with the serial power management interface (SPMI) and restructured the register map
- BMS-assisted charging
  - Uses IBAT measured by precise BMS/CCADC for end-of-charge (EoC) termination, voltage collapse protection (VCP) termination, and high-current charging IR drop compensation

Subsystem Hardware

Subsystem Hardware Overview

Subsystem Hardware Overview (1 of 3)



Subsystem Hardware Overview (2 of 3)

The SMBB block is shown at top of previous slide; its primary hardware functions and/or operating modes that are described in this section include:

- Buck converter and its controller
- Charger finite state machine (FSM™)
- Reverse boosting operation
- Automated trickle charging (ATC)

Other hardware blocks (shown on previous or next slide) are critical to SMBB operation and are also discussed:

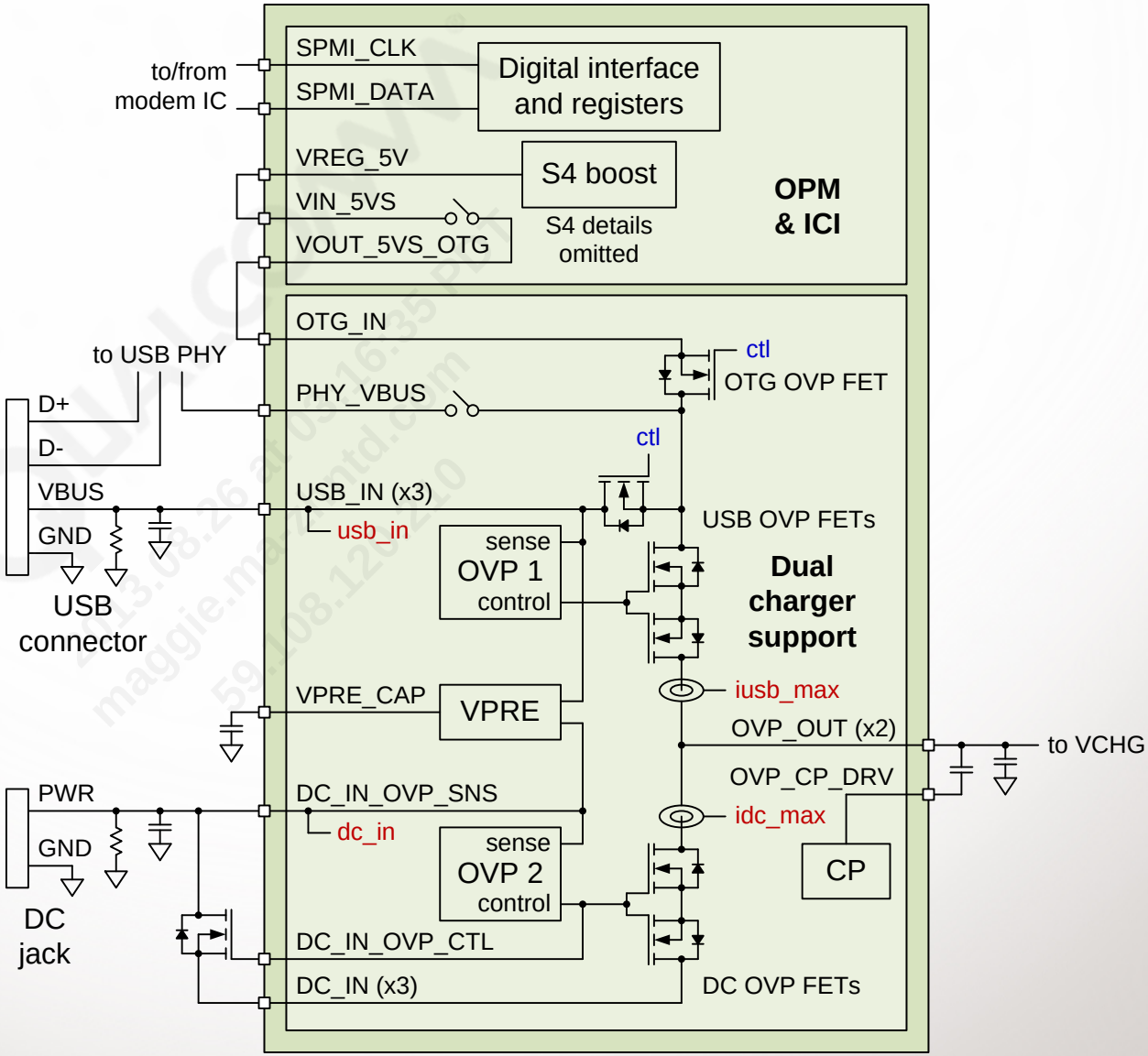
- OVP circuits within the dual-charger support block
- Portions of the BMS
- SPMI and the control registers
- +5 V SMPS

Also note the buck controller and FSM inputs, and the HK ADC inputs, listed on the previous slide and highlighted in red on the previous and next slides.

- These signals are key parameters used by software as described in later sections of this document.

Subsystem Hardware Overview (3 of 3)

- BMS (slide 14)
  - Voltage and current detectors
  - Supplements battery pack to determine ID and temperature
  - Plus more not shown
- SPMI digital interface and control registers
- Output power management
  - +5 V boost converter
  - +5 V switch for USB-OTG
- Dual charger support
  - Protected and gated +5 V OTG_IN
  - PHY_VBUS switch
  - USB input voltage monitoring
  - USB OVP
  - USB current monitoring
  - DC input voltage monitoring
  - DC OVP
  - DC current monitoring
  - Protected supply to charger
  - Preregulator (VPRE) for powering input power management circuits



Key External Components

Refer to reference schematics for the latest external devices being used by Qualcomm®. The following components warrant special emphasis:

DC OVP FET

- PM8941 SMBB integrates DC OVP FETs that offers +15 V tolerance. The external DC OVP FET is optional, and is only needed if higher OVP tolerance is required.

DC_OVP_CTRL

- DC_IN_OVP_CTL pin serves a dual-purpose
  - It is the gate drive signal if an external OVP FET is used.
  - It is also the charger option pin that indicates whether the system is using an external charger (CR-0000161116). The recommended connections are:
    - Floating if only the internal OVP FET is used
    - Connect to NFET gate if an external OVP FET is used
    - Ground if a DC jack (wall charger) is not used

VCHG capacitor

- Two 4.7 μF/16 V/0603 capacitors are recommended to accommodate derating.

Buck inductor

- A 1.0 μH/3225 inductor is recommended to support 3 A charging.
- Lower charging current allows for smaller package sizes.

Battery thermistor pull-ups

- Pull-up resistor values (BAT_ID and BAT_THERM) must be calculated to match the battery pack being used.

Additional Hardware Design Guidance

For additional hardware design guidance, see the *PM8841 and PM8941 Power Management Design Guidelines* document (80-NA555-5). It includes:

- Architectural diagrams and operational descriptions of its major functional blocks – input power management, output power management, general housekeeping, user interfaces, and IC-level interfaces – plus its configurable I/Os
- Explanations of all its external interfaces with supporting schematic diagram details
- Printed circuit board (PCB) layout guidelines
- PMIC input DC power and ground guidelines
- Hardware design suggestions not available elsewhere
- System-level information specific to the PMIC, such as the chipset's power grid and clock distribution
- Troubleshooting suggestions

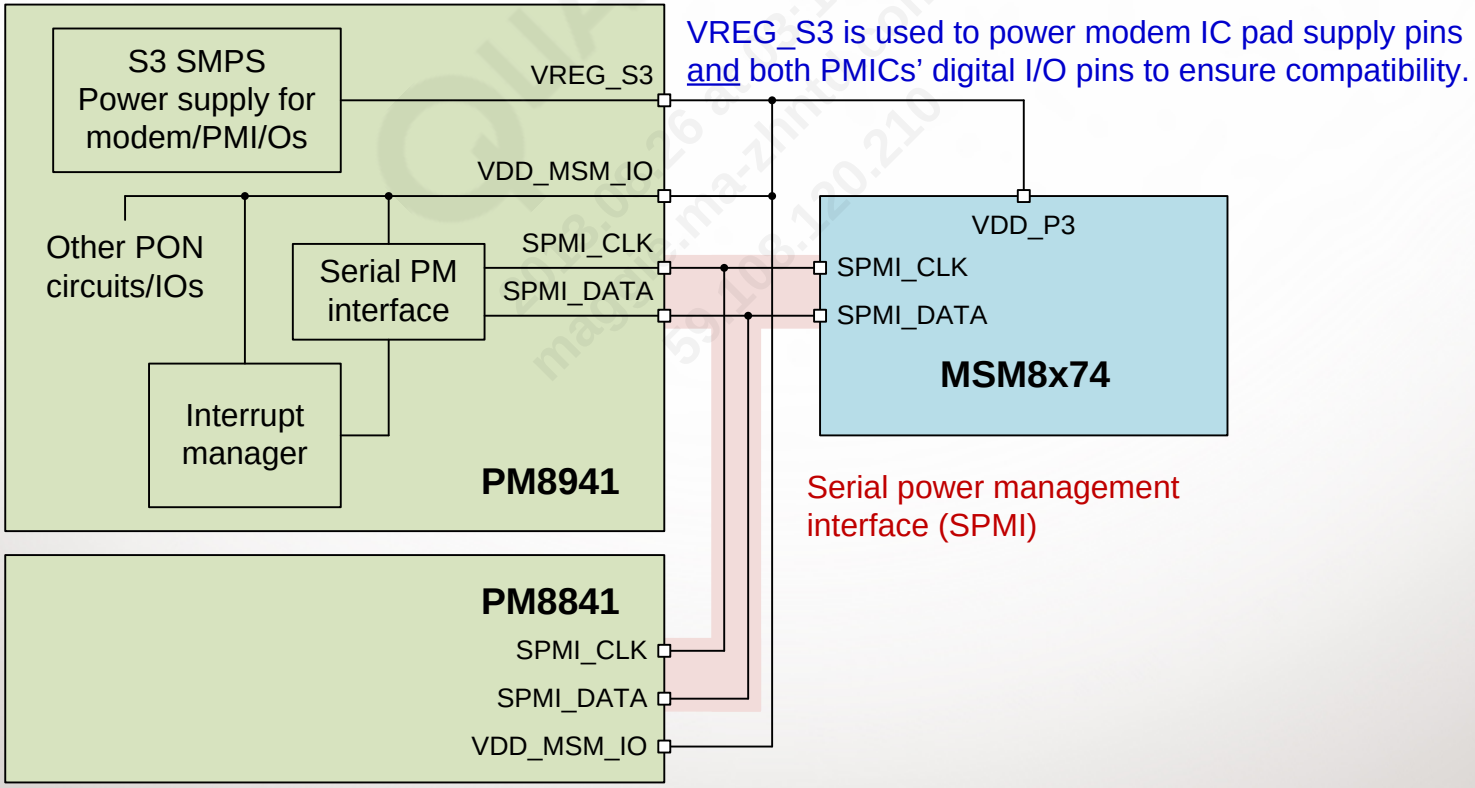
Feature trim options

- Compared to the first generation SMBC, the second generation SMBB requires fewer trim options.
- In fact, only one remains: BUCK_CTRL_TRIM6 should be trimmed to 0x05 on PM8941 versions 1.0 and 2.0.

SPMI and Control Registers

SPMI

- SPMI – This is the primary IC-level interface for efficient initialization, status, and control communications.
- The application programming interface (API) is used to program PMICs, indirectly exercising SPMI.
- The coin cell backs up several SPMI registers; at powerup, SPMI defaults are restored except bits backed up by the coin cell – they are only restored to default values if the coin cell expires.
- PMIC interrupts to the modem IC via SPMI.



SMBB Registers

The SMBB module consists of eight peripherals (see the table here); each peripheral has 256 registers.

Each peripheral has two registers:

1. The first register describes the peripheral type (0x02 for SMBB).
2. The second register describes the subtype (0x01–0x08 for the PM8941 SMBB peripherals).

Peripheral	Base address	PERPH_TYPE (0x4)	PERPH_SUBTYPE (0x5)	Description
SMBB_CHGR	0x1000	0x02	0x01	Main charging control
SMBB_BUCK	0x1100	0x02	0x02	Parameters and settings for buck
SMBB_BAT_IF	0x1200	0x02	0x03	Battery interfaces (BTM, BPD, VCP, PSI, etc.)
SMBB_USB_CHGPTH	0x1300	0x02	0x04	USB charging path: OVP, UVD, and AICL
SMBB_DC_CHGPTH	0x1400	0x02	0x05	DC charging path: OVP, UVD, and AICL
SMBB_BOOST	0x1500	0x02	0x06	Parameters and settings for boost
SMBB_MISC	0x1600	0x02	0x07	Miscellaneous (TFT, adaptive boot, revision, etc.)
SMBB_FREQ	0x1700	0x02	0x08	Sets the charger buck/boost switching frequency

Peripheral Types and Revisions

The SMBB_MISC peripheral tracks the SMBB revision:

- Two registers describe the analog revisions (major and minor).
- Two registers describe the digital revisions (major and minor).

PMIC	SMBB peripheral registers		SMBB revision registers	
	MISC_PERPH_TYPE	MISC_PERPH_SUBTYPE	ANA_MAJOR	ANA_MINOR
PM8941 v1.0	0x02	0x07	0x00	0x00
PM8941 v2.0	0x02	0x07	0x01	0x00
PM8941 v3.0	0x02	0x07	0x02	0x00

Other Hardware Used by the SMBB Software

Other Hardware Used by the SMBB Software

The other hardware blocks exercised by SMBB software are shown and discussed as needed within the software sections.

- SMBB FSM
- Poweron circuits
- Trickle charger
- Fast charger
- Charger timers
- Buck converter
- Reverse boosting
- Adapter interfaces and OVP (USB and DC)
- Battery interface and BMS

Performance Enhancements

Performance Enhancements (1 of 7)

VDD_MAX and IBAT_MAX steppers

- SMBB steppers mitigate transients when the software increases or decreases VDD_MAX and IBAT_MAX.
- The step size and delay time can be controlled in the corresponding VDD_MAX_STEP and IBAT_MAX_STEP registers.
- This feature is enabled by default since PM8941 version 1.0.

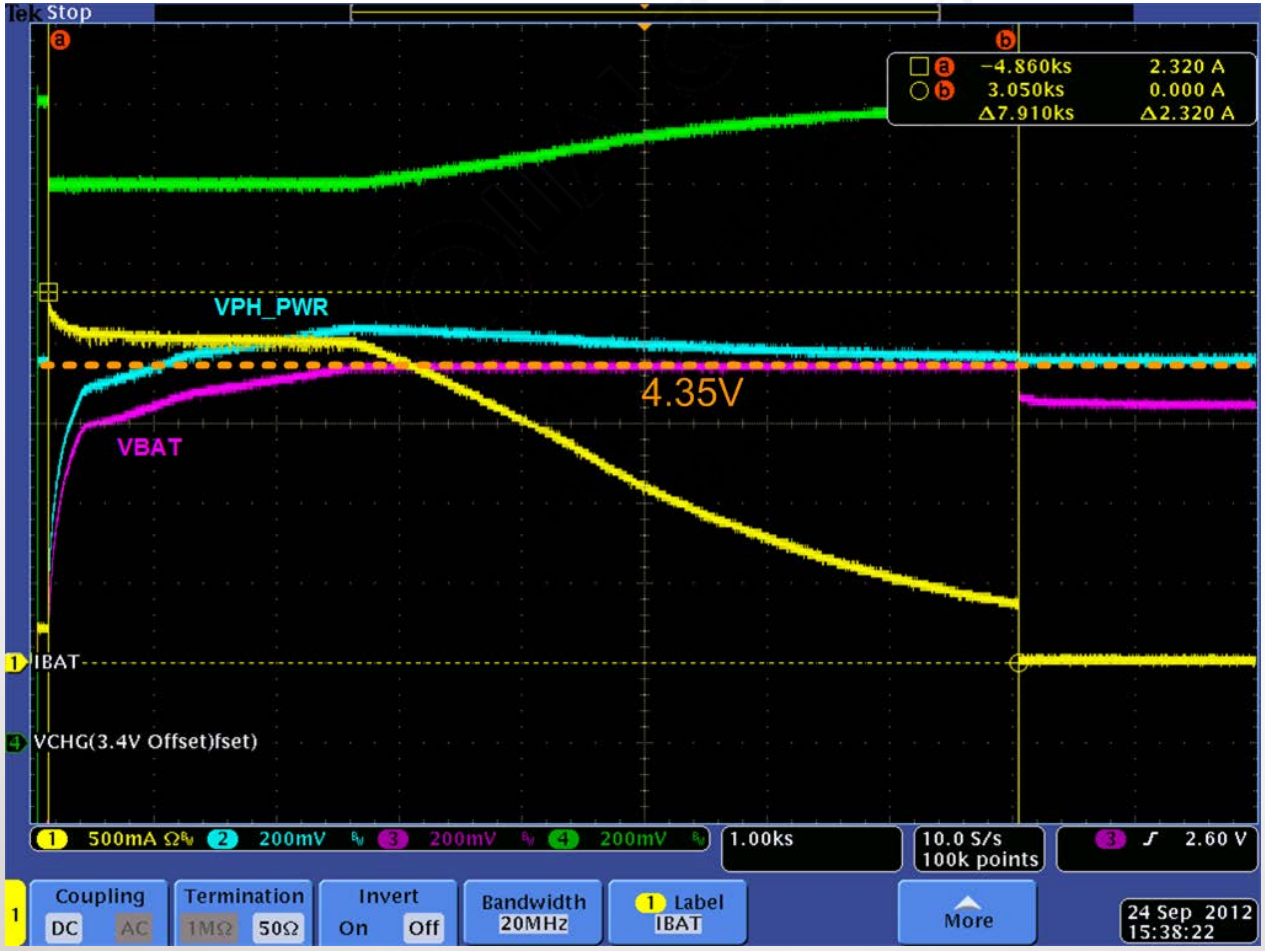
High-current charging IR drop compensation

- SMBB supports 3 A charging; higher current makes IR drops more critical.
  - VPH-to-VBAT charging path resistance includes the BAT FET, R_SNS, and PWB traces, and can easily add up to 100 mΩ.
  - The resulting IR drop causes the charger to leave constant current (CC) charging prematurely, thereby causing a longer charge time.
- Analog VPH-to-VBAT IR drop compensation
  - The VBAT_SNS pin enables Kelvin-sensing at the battery pack's VBAT during fast charging, and the SMBB control loop automatically switches its regulation point to VBAT_SNS during fast charging.
  - This method is the first option for IR drop compensation, and has been supported since PM8941 version 2.0.
  - To use this feature:
    `SMBB_BUCK_BCK_VBAT_REG_MODE = 0x01; //` Buck regulates VBAT (analog IR drop compensation enabled)

Performance Enhancements (2 of 7)

High-current charging IR drop compensation (continued)

- The effect of analog IR drop compensation when charging a 4.35 V battery is shown here.
  - VPH_PWR rises above 4.35 V to prolong CC charging.
  - VPH_PWR gradually decreases back to 4.35 V during constant voltage (CV) charging.
  - During the entire charging process, VBAT never exceeds 4.35 V.



Performance Enhancements (3 of 7)

High-current charging IR drop compensation (continued)

- Digital VPH-to-VBAT IR drop compensation
  - The VPH-to-VBAT charging path resistance is characterized and stored at SMBB_CHGR_IR_DROP_COMPEN: RES.
  - During CC charging, the SMBB hardware automatically elevates VDD_MAX to VDD_SAFE + IBAT_BMS * RES.
  - During CV charging, the SMBB hardware automatically reduces VDD_MAX to VDD_SAFE as IBAT_BMS drops.
  - This method is the second option for IR drop compensation and has been supported since PM8941 version 2.0
  - To use this feature:

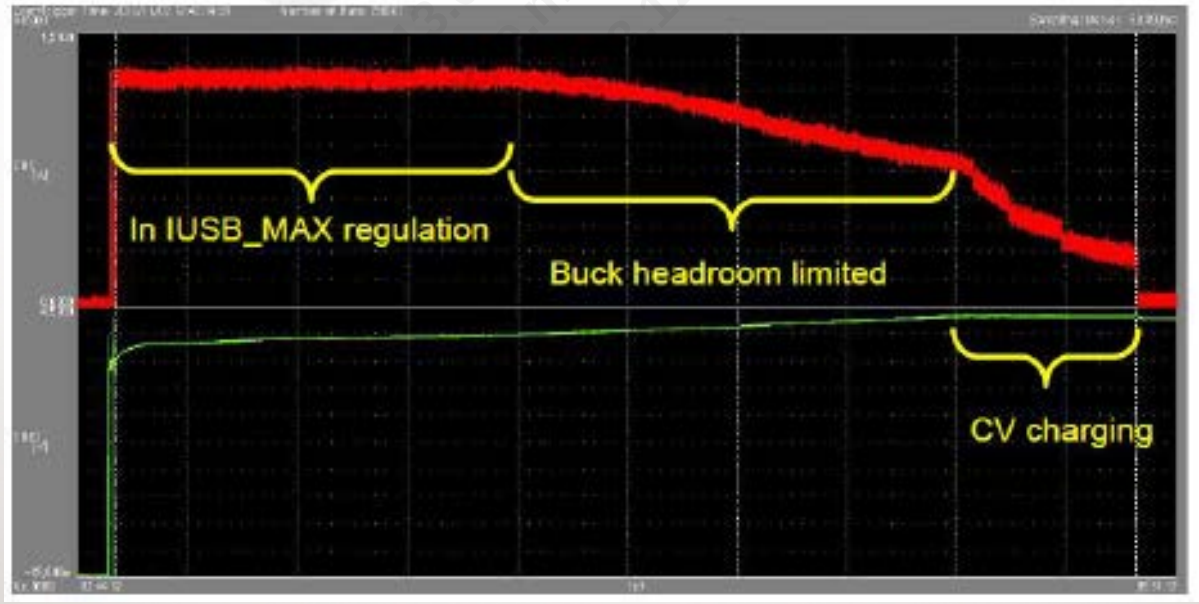
    `SMBB_BUCK_BCK_VBAT_REG_MODE = 0x00; //` Buck regulates to VPH (analog IR drop compensation disabled)

    `SMBB_CHGR_IR_DROP_COMPEN = 0x8X; //` Digital IR drop compensation enabled, RES = X
- Recommendation: Since the analog method is proven and does not require measuring the VPH-to-VBAT charging path resistance, it is the recommended IR drop compensation method.

Performance Enhancements (4 of 7)

Charger buck converter 100% duty-cycle operation

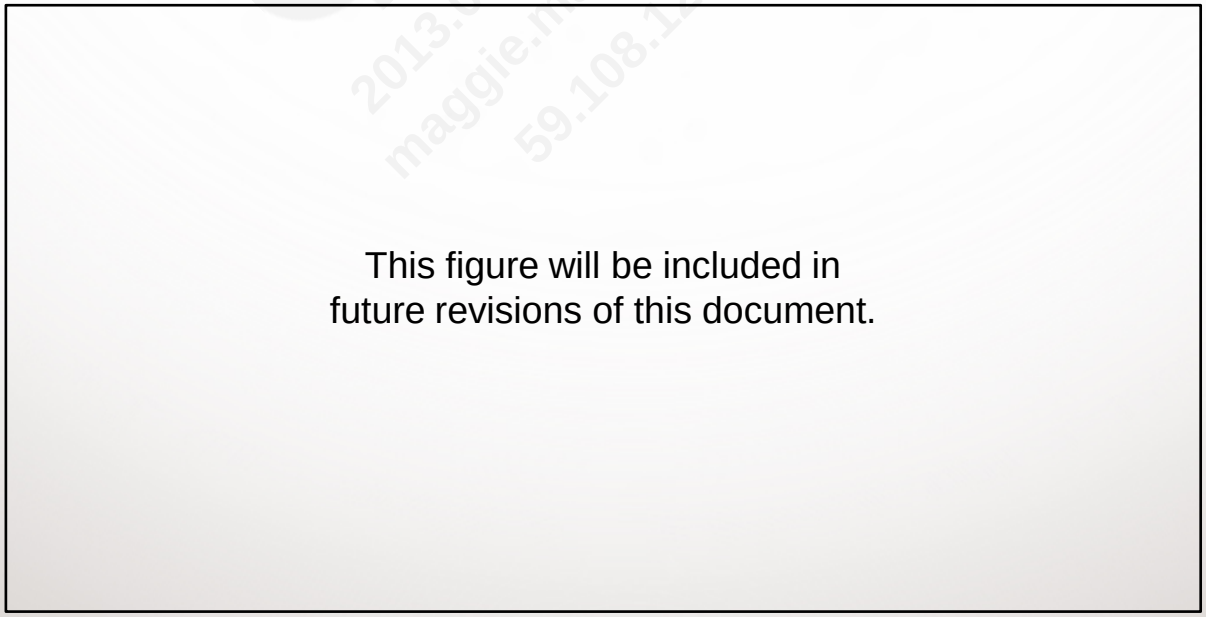
- Buck input – USB chargers output 5 V typical; during high-current charging, the IR drop due to the USB cable and OVP FET Rds(on) can easily bring the charger buck converter input voltage (VCHG) below 4.5 V.
- Buck output – 4.35 V batteries are popular due to their high capacity; with the VPH-to-VBAT IR drop compensation, an even higher charger buck output voltage (VPH) is required.
- Combining the low input voltage (VCHG) and high output voltage (VPH) requirements pushes the buck converter to an extremely high duty cycle.
- Buck regulators are normally limited to some maximum duty cycle (DMAX) to ensure stability, thereby limiting its output current and reducing its voltage headroom.
- A typical charging curve is shown here – when the charger current is headroom-limited, the battery current drops before CV charging starts.



Performance Enhancements (5 of 7)

Charger buck converter 100% duty-cycle operation (continued)

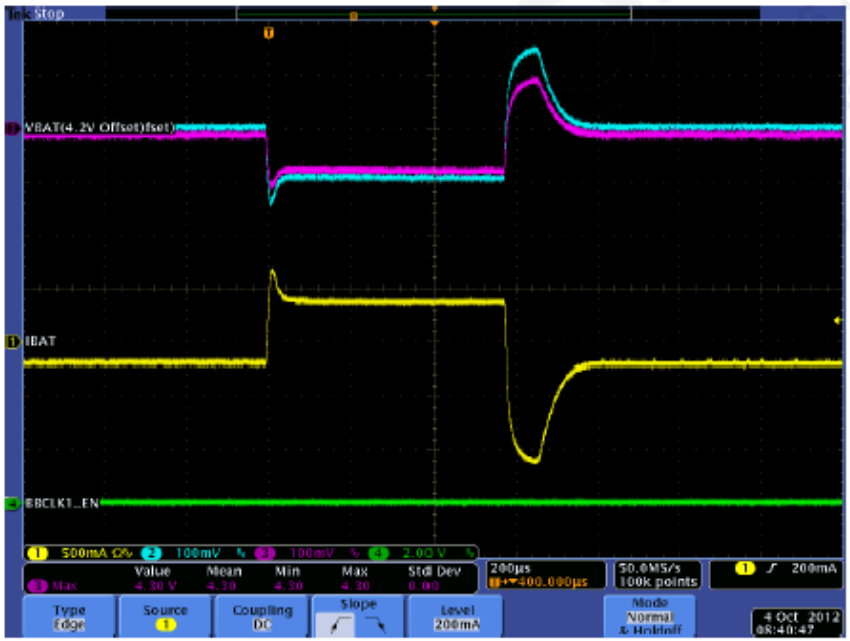
- To overcome the charging current drop when headroom-limited due to DMAX, thereby improving battery charging time, the SMBB supports 100% duty cycle operation.
- This allows the charger buck PFET to be fully ON when headroom-limited.
- This feature has been supported since PM8941 version 1.0; to enable this feature:
  `SMBB_BUCK_SEC_ACCESS = 0xA5; //` Unblock SEC_ACCESS
  `SMBB_BUCK_TEST_SMBC_MODES = 0x00; //` BUCK_MAX_DUTY = 0 ns (100% duty-cycle enabled)
- This figure shows the charging curve when a 100% duty cycle is enabled.
- Caution: Due to a charger removal detection issue with a fully charged battery, it is recommended that this 100% duty-cycle feature be disabled in PM8941 version 2.0 implementations by keeping SMBB_BUCK_TEST_SMBC_MODES at its default value. Other implementations can enable this feature.



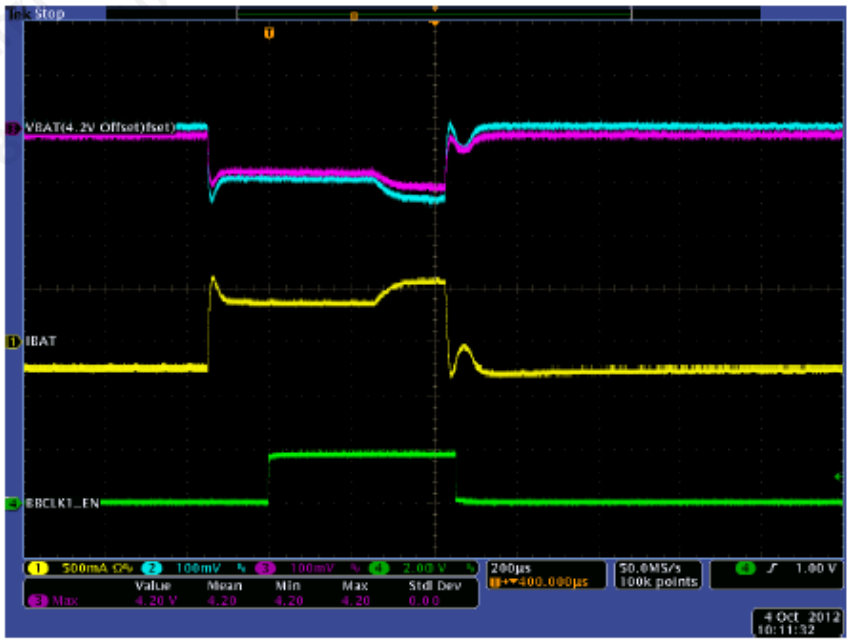
Performance Enhancements (6 of 7)

Automatic VDD_MAX adjustment upon GSM_PA_ON

- SMBB monitors a GSM_PA_ON signal (BBCLK1_EN) and reduces VDD_MAX set point (using a stepper) when GSM PA turns on; this reduces buck converter output voltage spike when GSM PA current burst ends.
  - The number of VDD_MAX reducing steps is programmable.
- This feature has been supported since PM8941 version 2.0; its effectiveness is shown in the figures here.
- Caution: PM8941 version 2.0 adjustment is based upon BBCLK1_EN, but without proper software it is not the same as GSM_PA_ON; instead, BBCLK1_EN is high whenever the modem IC is running, and VDD_MAX is 100 mV lower than intended. The VDDMAX_GSM_ADJ feature in PM8941 version 2.0 must be disabled by `SMBB_CHGR_VDDMAX_GSM_ADJ = 0x00; // VDDMAX_GSM_ADJ disabled`
- PM8941 version 3.0 fixes this issue by allowing the selection of GSM_PA_ON or TX_GTR_THRES (default) for triggering the VDD_MAX adjustment.



(a) VDDMAX_GSM_ADJ disabled: 100mV VBAT overshoot when GSM load releases

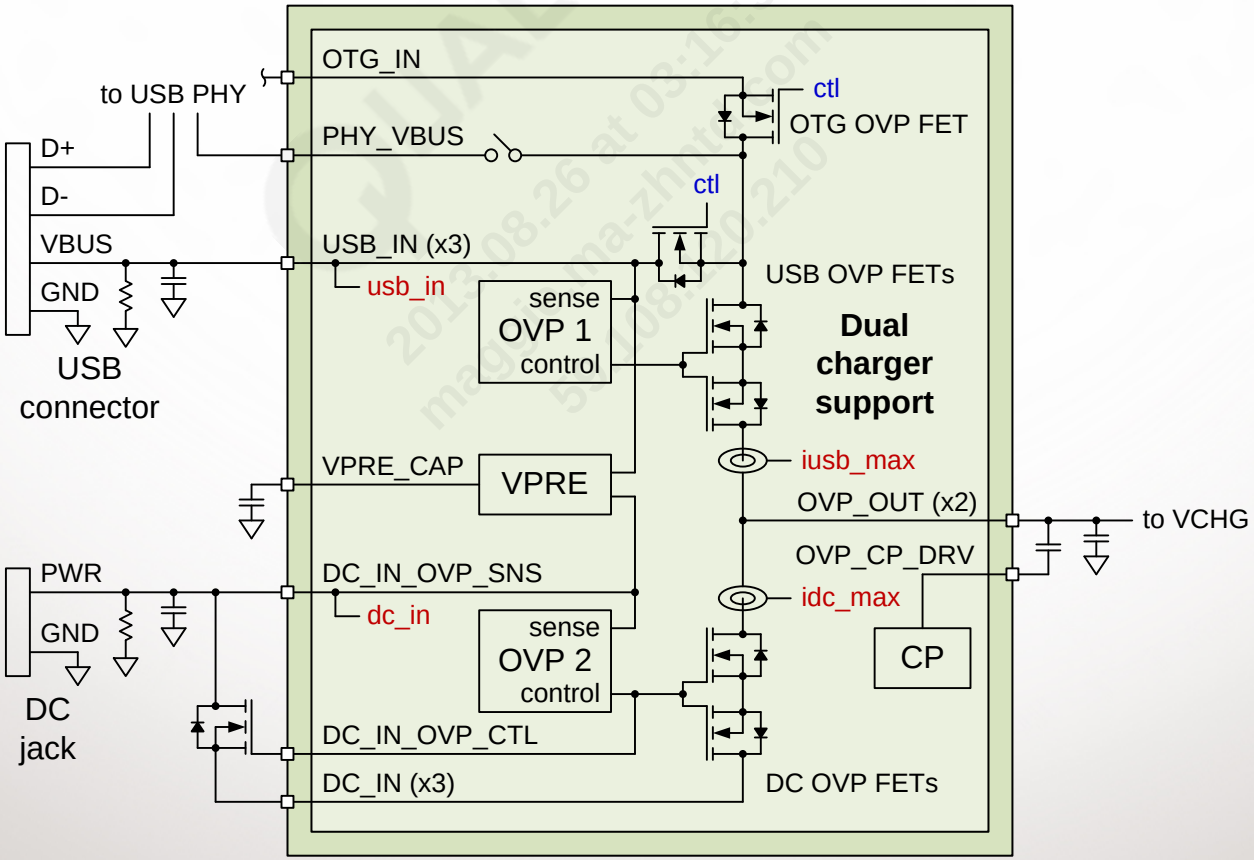


(b) VDDMAX_GSM_ADJ enabled: no VBAT overshoot

Performance Enhancements (7 of 7)

Adapter interfaces and OVP enhancements

- The OVP threshold has been extended to 11 V maximum for both the USB and DC paths.
- Programmable UVD thresholds have been added for both USB and DC paths.
- The DC charging path also supports input current limiting (IDC_MAX).
- An enable/disable bit has been added to both IUSB_MAX and IDC_MAX.
- The fast charging path switching is supported.



Top-level Operational Software

Top-level Operational Software Overview

Top-level Operational Software Overview

Top-level operational software

- Poweron and system boot
- Initializing subsystem and enabling charging
- Monitoring charging and EoC termination

Other key hardware/software blocks (presented in later sections)

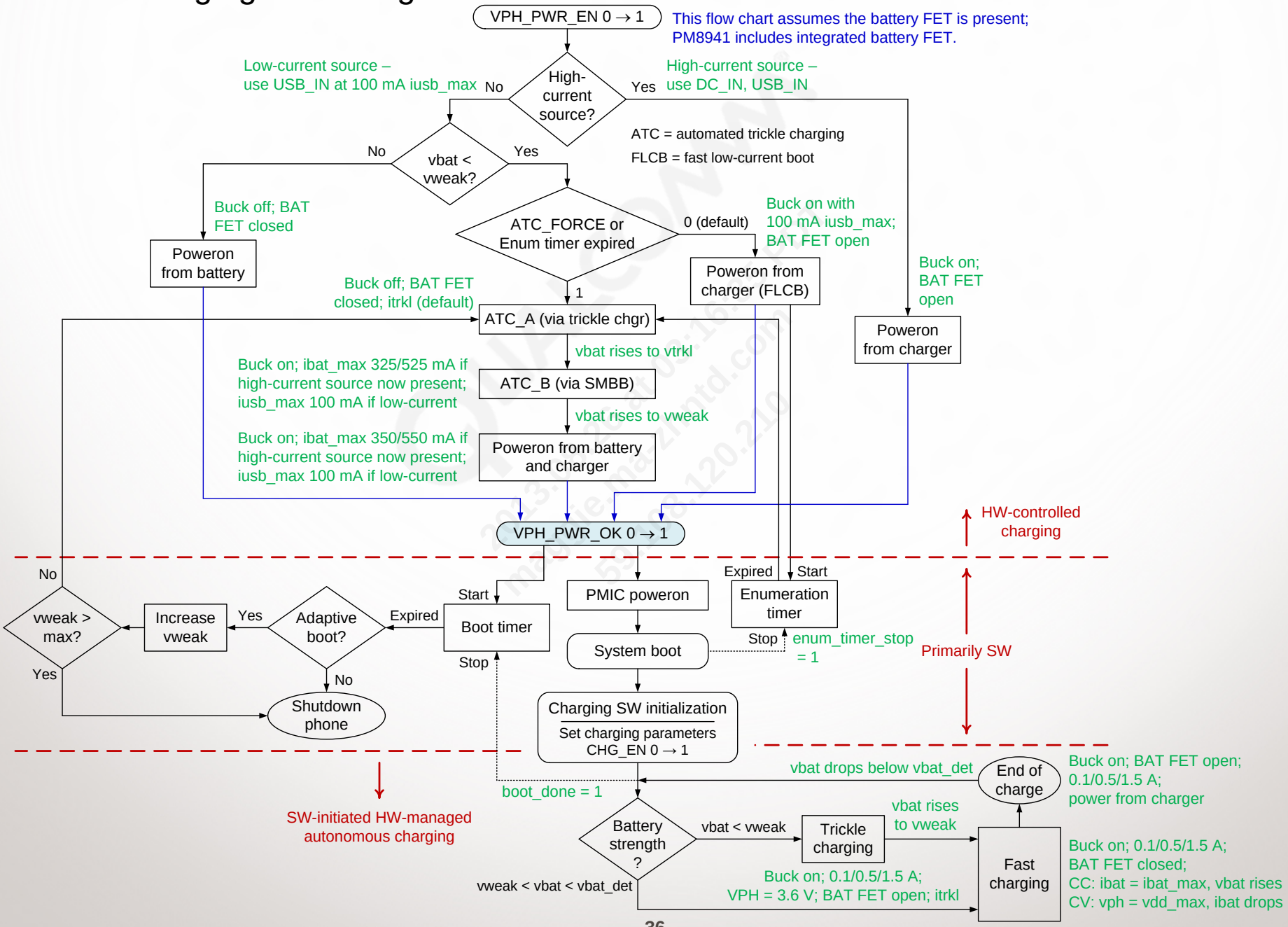
- SMBB-specific blocks
- Adapter interface blocks
- Battery interface blocks

A detailed flow diagram for SMBB charging is shown on the next slide and referred to throughout subsequent sections.

Operational software topics

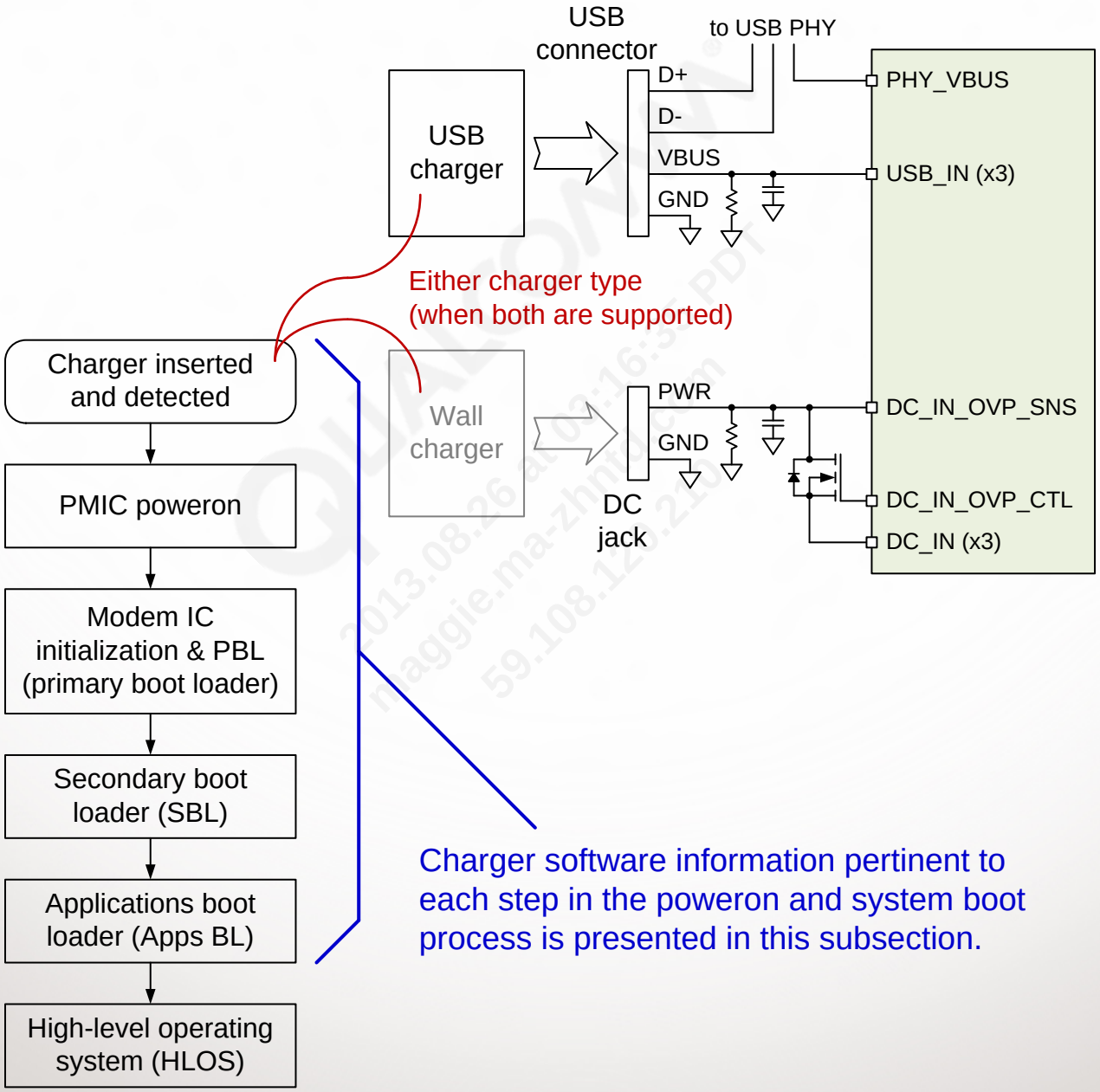
- Top-level operational software
  - Poweron and system boot
  - Initializing subsystem and enabling charging
  - Monitoring charging and EoC termination
- Other key hardware/software blocks
  - SMBB-specific blocks
  - Adapter interfaces blocks
  - Battery interface blocks

SMBB Charging Flow Diagram

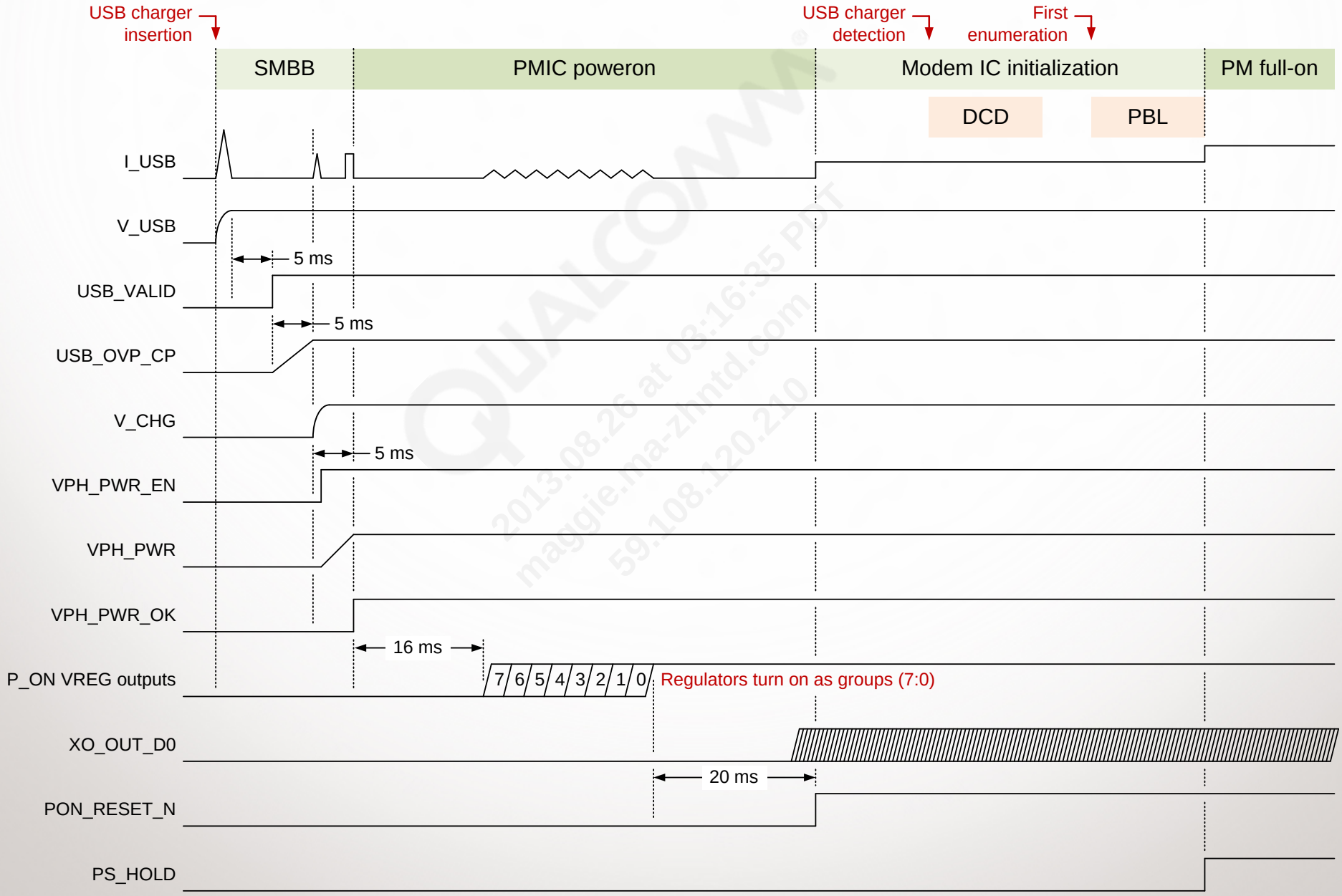


Poweron and System Boot

Poweron and System Boot



PMIC Poweron from Charger Insertion to Primary Boot Loader (1 of 2)



PMIC Poweron from Charger Insertion to Primary Boot Loader (2 of 2)

The typical PMIC hardware poweron sequence upon charger insertion, using USB charging path as example (DC path is similar), is:

1. USB charger insertion – As the USB_IN voltage rises above the coarse detect threshold (1.7 ± 0.3 V), the coarse_det comparator output goes high, which requests MBG and 19.2 MHz clock.
2. The USB under and over-voltage comparators qualify the USB_IN voltage against the corresponding thresholds. If the USB_IN voltage stays within the thresholds for longer than the debounce time, the usbin_valid signal goes high, thereby turning on the USB OVP FET and providing a poweron trigger.
3. PON circuits starts trim copy (state 2), enables MBG (state 3), and requests VPH_PWR (state 4) by sending a VPH_PWR_EN signal to the charger.
4. Depending upon the USB/DC charging path and VBAT level, the charger brings up VPH_PWR by turning on the charger buck, by closing the BAT FET, or by ATC. The charger then sends the VPH_PWR_OK signal back to PON circuits as an acknowledgement.
5. PON circuits measure VPH_PWR against the UVLO threshold (state 5); if it passes, it starts turning on the primary boot VREGs using the PMIC boot sequencer (PBS, state 6). If all these VREGs turns correctly, the PBS sends a pbs_ack signal back, which moves PON to the next step.
6. PON circuits enable the XO (state 7) and release PON_RESET_N (state 8), allowing the modem IC to boot, and waits for modem IC to assert the PS_HOLD signal.
7. The modem IC primary boot loader (PBL) asserts PS_HOLD, which puts PON circuits into their ON state (state 9).

PBS

The PBS allows the PMIC to execute preprogrammable software-like register read/write sequences upon powerup, powerdown, and certain other events. There are two possible PBS sequences during poweron:

- A pre-PON sequence triggered when entering state 3 (MBG_EN), mainly used by the charger to change its defaults and options
- A primary PON sequence triggered in state 6 (REG_ON) to turn on the primary boot regulators

Two example PBS commands that might be included in the Pre-PON sequence by the charger are:

- `WR Reg 0x10ED = 0x02; // Override CHG_OPTION_PIN = 0` (to indicate the system is using a third-party charger)
- `WR Reg 0x104A = 0x80; // SMBB_CHGR_ATC_CTRL: ATC_FORCE = 1;` to force ATC

The PBS commands to be used depend upon the supported use cases.

PBL (1 of 2)

The PBL is hard-coded in the modem IC and is used for the system initial bring-up. A few PBL notes specific to the charger are listed here:

- The PBL asserts PS_HOLD at its very beginning.
- The PBL reads the CHG_OPTION_PIN bit from SMBB_CHGR peripheral (Reg 0x1008 bit 7) to determine whether the system is using the PMIC charger or an external charger.
- When the following conditions are met, the PBL performs USB charger-type detection and enumeration (if SDP), and sets the proper IUSB_MAX and ENUM_TIMER_STOP values.
  - CHG_OPTION_PIN = 1: The system is using an internal charger.
  - POWER_PATH = 10: USB charger.
  - BAT_PRES = 1: The battery is present.
  - ABOVE_VBAT_WEAK = 0: The battery is weak (below VBAT_WEAK threshold).
- If the PMIC detects a weak battery (VBAT < VBAT_WEAK) and detects a USB power source, it attempts fast low-current boot (FLCB) with the USB dictated 100 mA input current limit.
- The firmware enables USB PHY to detect the USB port type (SDP/CDP/DCP/ACA), and enumerates if it is SDP (attempting to get more current from the USB port to assist FLCB).
- During FLCB, the SMBC FSM ticks an enumeration timer (90 sec default); at expiration, if the PBL still cannot draw 100 mA current from the USB port:
  - The system recognizes that FLCB cannot succeed.
  - SMBB turns off VPH_PWR and initiates ATC to charge the battery to the weak threshold before attempting another boot.
- Thus, it is necessary for the PBL to:
  - Configure CHG_IUSB_MAX (PBL_ACCESS2 [4:2]) based upon the USB port-type detection and enumeration result
  - And then write `ENUM_TIMER_STOP (PBL_ACCESS2 bit 1) = 1`
- SMBB registers used by the PBL are listed on the next slide.

PBL (2 of 2)

SMBB registers used by PBL					
Register name	**SID/GID**	**Address**	**Variable**	**Bits**	**Values**
CHG_OPTION	SID = 0 or 2	0x1008	CHG_OPTION_PIN	7	0 = External charger 1 = Internal charger
BAT_PRES_STATUS	SID = 0 or 2	0x1208	BAT_PRES	7	0 = Battery absent 1 = Battery present
VBAT_STATUS	SID = 0 or 2	0x100B	ABOVE_VBAT_WEAK	1	0 = Below threshold 1 = Above threshold
PWR_PTH_STS	SID = 0 or 2	0x1308	POWER_PATH	1:0	00 = Not used 01 = Battery 10 = USB charger 11 = DC charger
ENUM_TIMER_CTL	SID = 0 or 2	0x134E	ENUM_TIMER_STOP	0	Write 1 to stop timer
IUSB_MAX	SID = 0 or 2	0x1344	IUSB_MAX	4:0	0x00 = 100 mA 0x01 = 150 mA 0x02 = 200 mA | | 100 mA steps to 0x19 | | 0x19 = 2.5 A

Charger Software During the Secondary Boot Loader

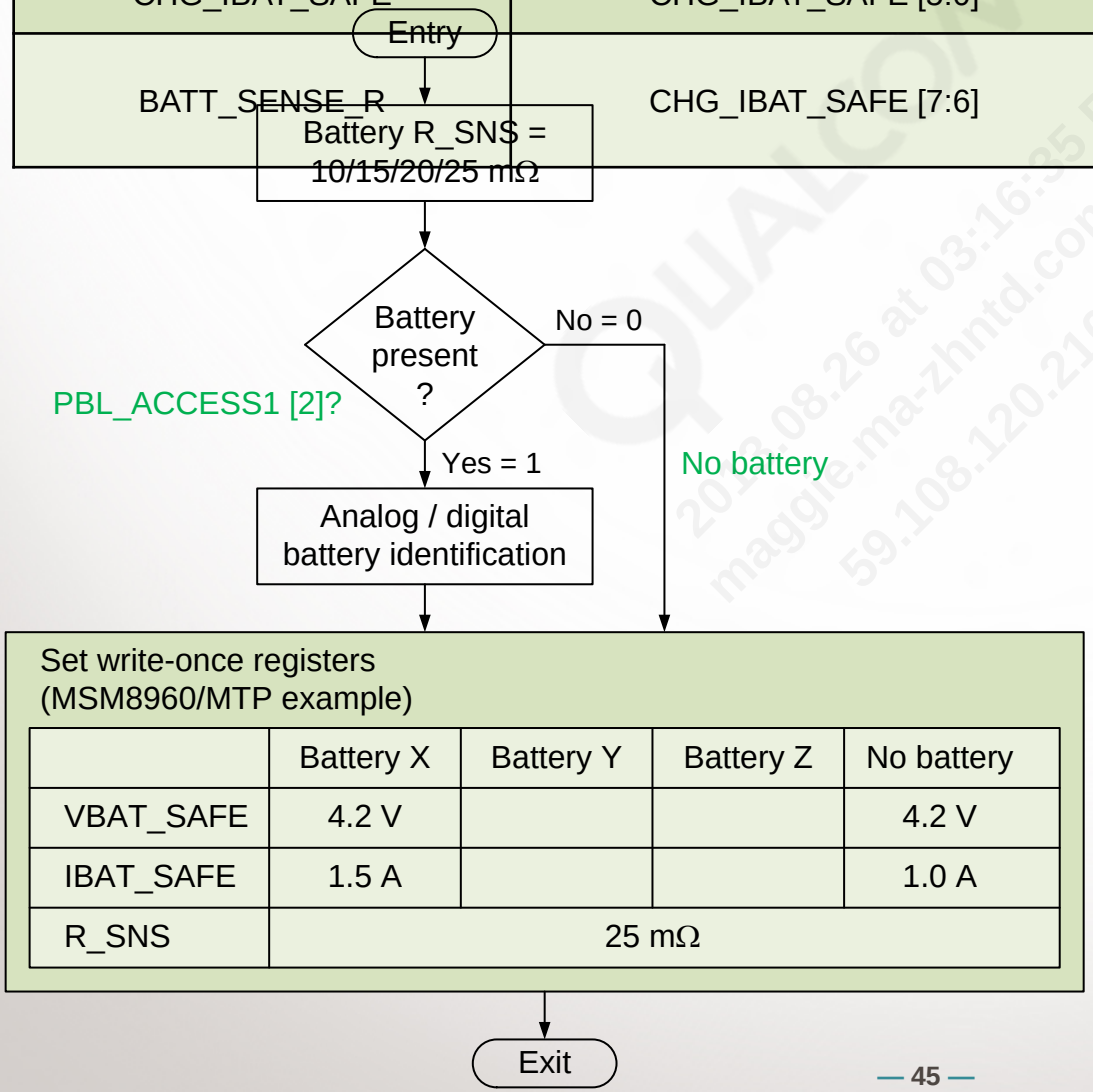
- General PMIC initialization is done in SBL – workarounds and optimization settings are applied.
- Even though the PBL supports FLCB, it can be stopped after PBL and ATC can be started:
  - Set the ATC_FORCE bit (CHG_CNTRL_2 bit 7) to 1
  - Reboot the phone

Write-once registers and analog/digital battery identification

- The SMBB includes two write-once registers (CHG_VDD_SAFE and CHG_IBAT_SAFE) that limit the maximum voltage and current that can be applied to the battery.
  - Any VDD_MAX or IBAT_MAX value larger than VDD_SAFE or IBAT_SAFE is ignored.
- To prevent third-party malware from changing the values in VBAT_SAFE and IBAT_SAFE, these registers can be written to only once after the PMIC poweron reset.
  - Any further write access to these registers is ignored.
- These registers should only be written to in a secure and OEM-configurable domain, such as SBL.
- If multiple battery types with different sizes and/or chemistries (such as 4.2 V normal voltage and 4.35 V high voltage) are supported, it is necessary to identify the battery type before configuring the write-once registers.
- When writing to the CHG_IBAT_SAFE register, it is also necessary to configure the BATT_SENSE_R field in the register, depending upon the battery current sensing resistor value (fixed for each phone model).
- If a battery is not present during boot, conservative values should be written to the write-once registers
  - For example: 4.2 V and 1.0 A
- Write-once registers (MSM8960 and MTP example) and the recommended flow chart for configuring them are shown on the next slide.

Write-once Registers

Parameter	Register	Software control instructions
CHG_VDD_SAFE	CHG_VDD_SAFE [6:0]	Set in SBL3, depending upon battery type
CHG_IBAT_SAFE	CHG_IBAT_SAFE [5:0]	
BATT_SENSE_R	CHG_IBAT_SAFE [7:6]	Set in SBL3, depending upon battery sense resistor value



	Battery X	Battery Y	Battery Z	No battery
VBAT_SAFE	4.2 V			4.2 V
IBAT_SAFE	1.5 A			1.0 A
R_SNS	25 mΩ			

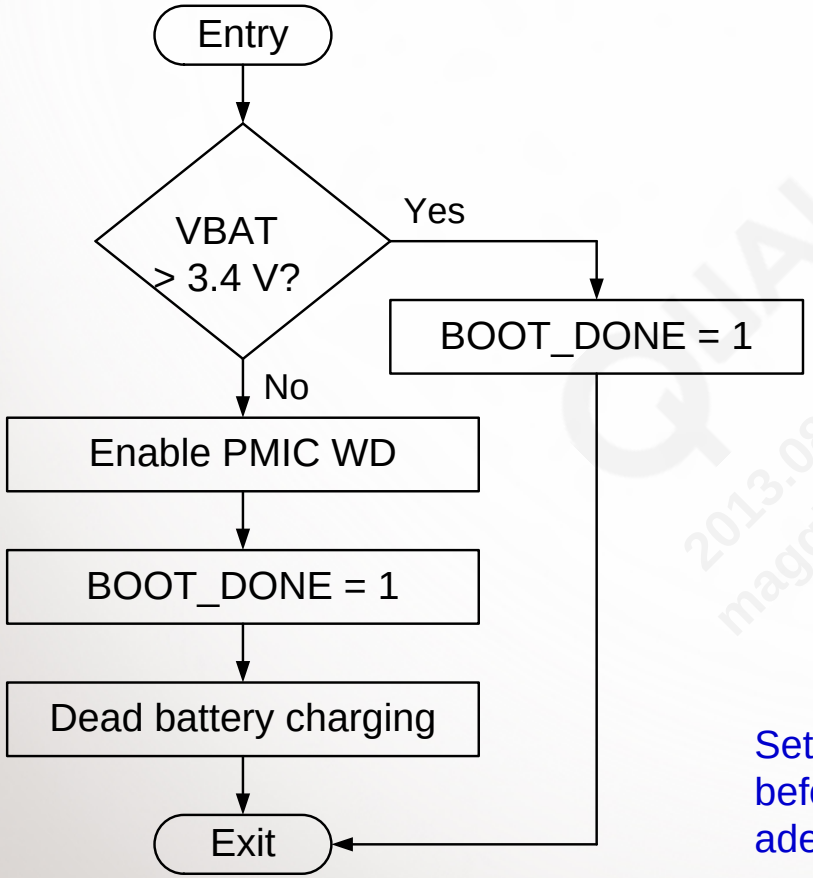
Charger Software During the Applications Boot Loader

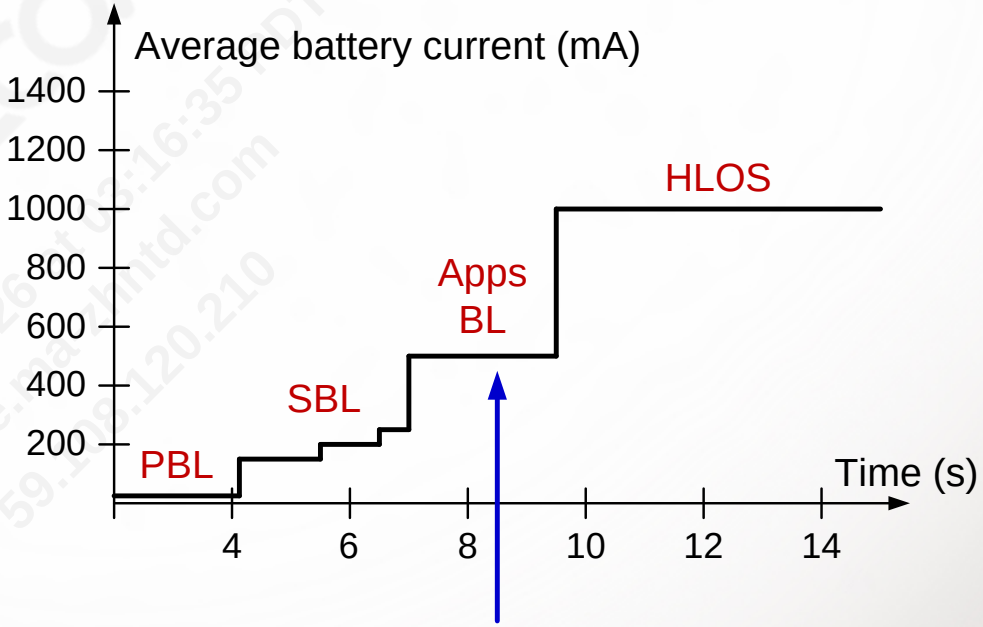
- When the battery is dead and the attached charger has limited current capability (such as USB 500 mA):
  - The HLOS cannot be launched successfully since it usually takes more than 1 A.
  - If HLOS launch is attempted, the software may hang-up, causing the phone to appear to be stuck in the boot process.
  - The dead battery needs to be charged to ~ 3.4 V before launching the HLOS; this is done within the applications boot loader.
- The SMBB FSM's boot timer prevents launching HLOS without a sufficient battery charge.
  - The boot timer is enabled when phone starts to boot.
  - If it is not stopped by the modem IC before it expires (2 minute default), the SMBC FSM assumes that the boot failed and automatically starts an adaptive boot.
- An adaptive boot shuts down VPH_PWR, increases the battery weak threshold (CHG_VBAT_WEAK), and begins automatic trickle charging (ATC) if a valid charging source is present.
  - See the SMBB Charging Flow Diagram slide for more details.
- Requirement: write

  `SYS_CONFIG_2 <6> = 0b1; // BOOT_DONE = '1'`

  to stop the boot timer before its 2 minute timeout, and after the system verifies that the boot was successful
- By default, the boot timer and adaptive boot are disabled.
  - This prevents affecting the initial system bring-up and debugging.
  - These features can be enabled after the software development is finished and stabilize.
- If the boot timer is enabled, software needs to properly set the BOOT_DONE bit during Apps BL (before launching HLOS) – see more details on the next slide.

Setting BOOT_DONE



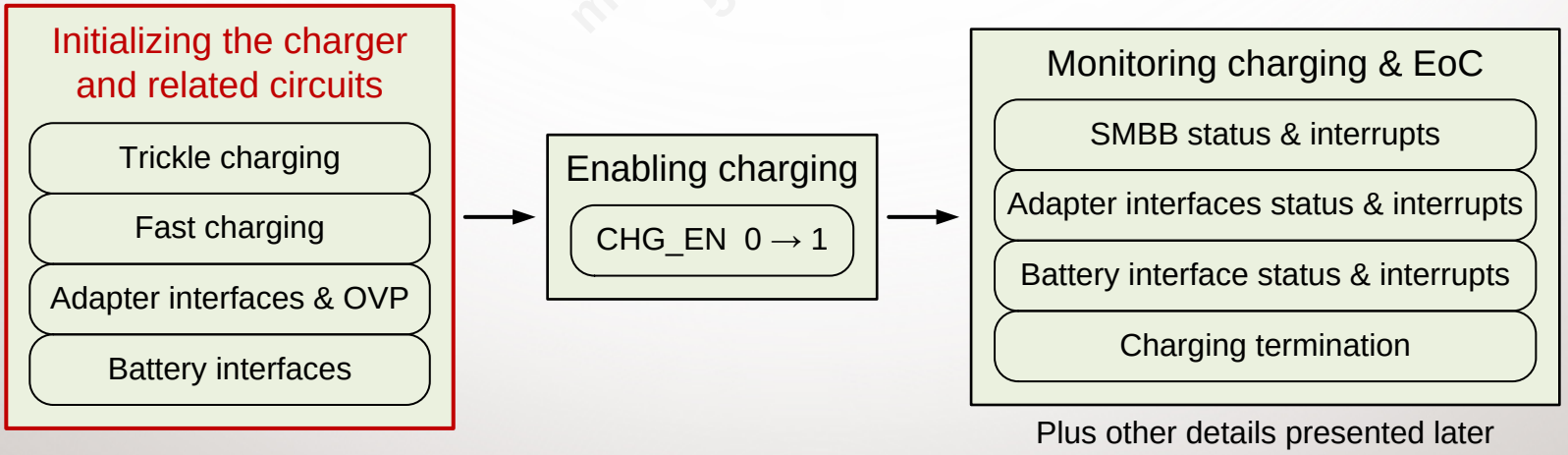


Set BOOT_DONE during the applications boot loader before dead battery charging to ensure the battery is adequately charged before HLOS is launched.

Initializing Subsystem and Enabling Charging

Subsystem Initialization in HLOS

- From the SMBB perspective, a boot begins with charger insertion and ends when BOOT_DONE is set by the software.
- After the boot, charging does not start automatically by default, so that the applications boot loader or HLOS can properly initialize the charging parameters before it starts the hardware-managed autonomous charging.
- Four areas of charging parameters need to be initialized:
  - Trickle charging
  - Fast charging
  - Adapter interface initialization
  - Battery interface initialization
- As shown below, the three main HLOS software stages are initializing the charger, enabling charging, and monitoring charging.



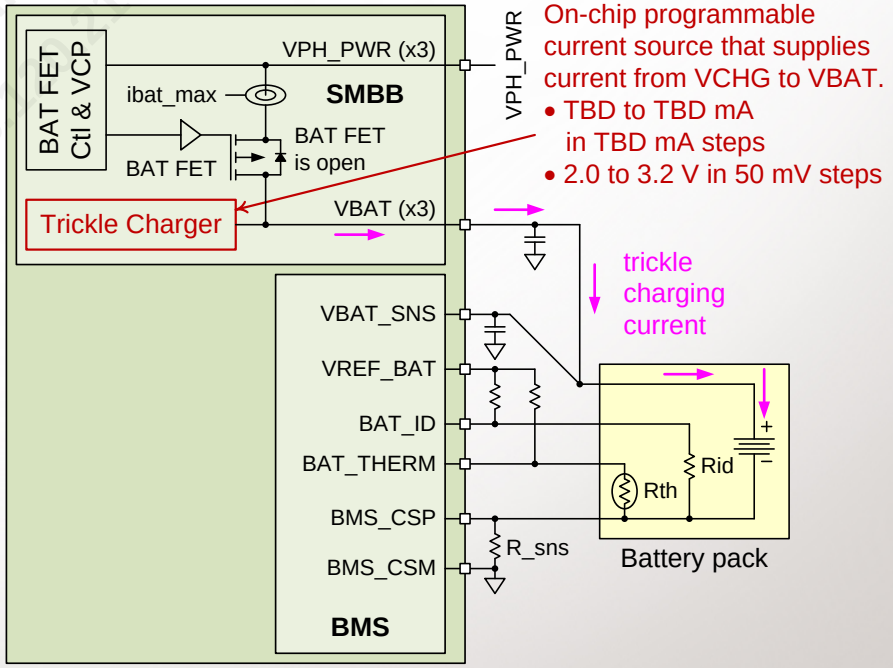
Initializing ATC (1 of 2)

- ATC is hardware-controlled charging that is necessary when the battery voltage is below the weak threshold (VBAT_WEAK), and when FLCB is not successful (e.g., due to USB enumeration failure).
- SMBB ATC has two phases: ATC_A and ATC_B (see the SMBB Charging Flow Diagram slide).
- During ATC, the modem IC has not been initialized and its software is not running.
- The parameters that affect ATC behavior are all backed up by an internal voltage (xVdd), so their values are retained from a previous successful boot as long as the coin cell voltage VCOIN is above 2 V, even if the battery is removed or deeply discharged.
- The table on the next slide summarizes the parameters that affect ATC behavior and their software control instructions.

In addition to the SSBI-to-SPMI register mapping, some SMBB ATC controls have been updated:

- Charging current during the ATC_B phase (IBAT_ATC_B) is now programmable up to 3.25 A (was 325 or 525 mA programmable).
- TTRKL_MAX now has an enable bit.
- An improved battery protection circuit recovery scheme allows the trickle charger output voltage to be clamped and the VTRKL_FAULT comparator to be disabled.

Additional SMBB ATC control details will be included in future revisions of this document.

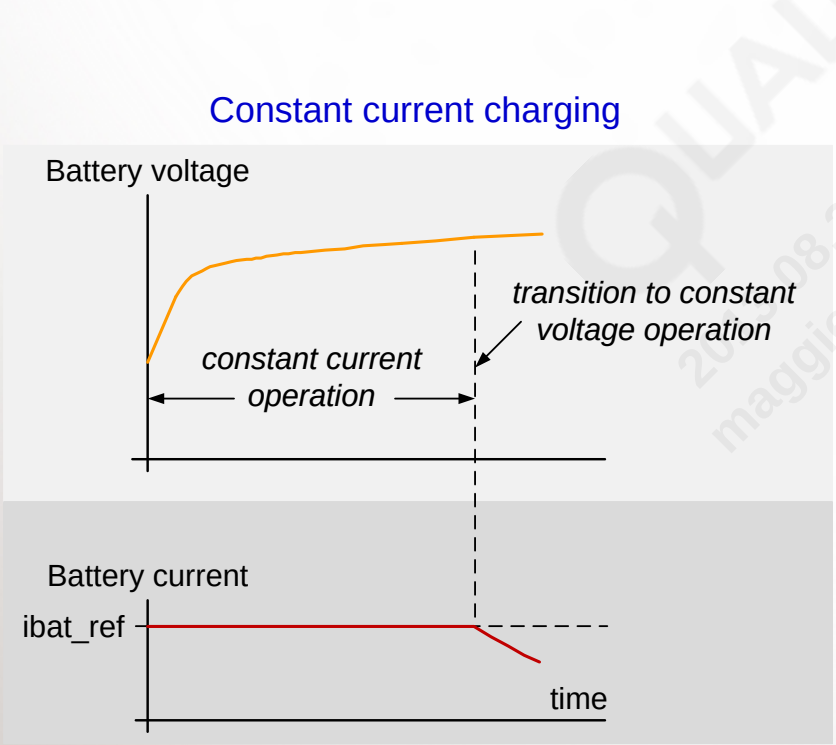


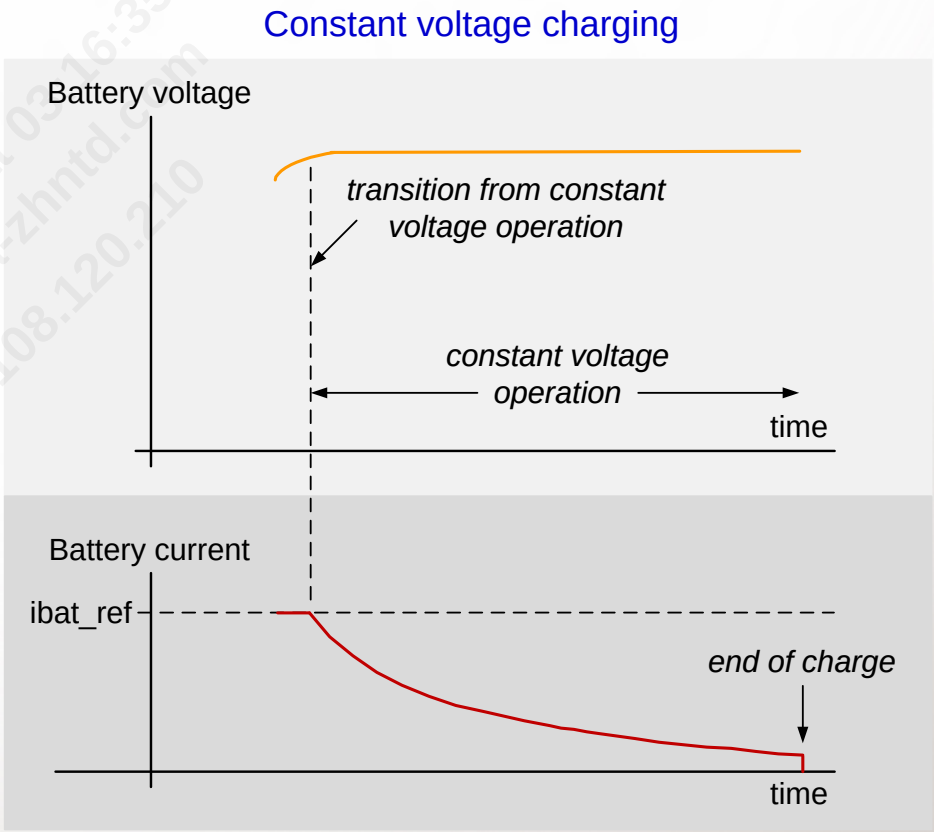
Initializing ATC (2 of 2)

Register	Address	Software control instructions	MSM8974/ MTP example
ATC_CTRL: ATC_FORCE	SMBB_CHGR: ATC_CTRL	Setting this bit will force the charger to skip FLCB and go to ATC_A even if FLCB conditions are met. Set to 1 if the system is not able to FLCB.	0
IBAT_ATC_A (CHG_ITRKL_LOW)	SMBB_CHGR: IBAT_ATC_A	Charge current during ATC_A or software-initiated trickle charge. This parameter is battery dependent.	0x04 (90 mA)
VBAT_TRKL (CHG_VTRKL_LOW)		VBAT threshold between ATC_A and ATC_B. This parameter is battery dependent.	0x0F (2.8 V)
IBAT_ATC_B (CHG_ATC_B_ISEL)		Charge current during ATC_B. This parameter is battery dependent.	0x14 (1.0 A)
VBAT_WEAK		VBAT threshold for end of ATC_B. This parameter is determined by the system; may be modified by an adaptive boot.	0x0B (3.2 V)
TTRKL_MAX_EN		Enable for maximum trickle charge timer	0x80
TTRKL_MAX		Maximum time allowed in ATC.	0x0E (15 min)

Initializing Fast Charging (1 of 2)

- Fast charging is available once VBAT is greater than VBAT_WEAK.
- The charger hardware autonomously manages fast (CC/CV) charging.

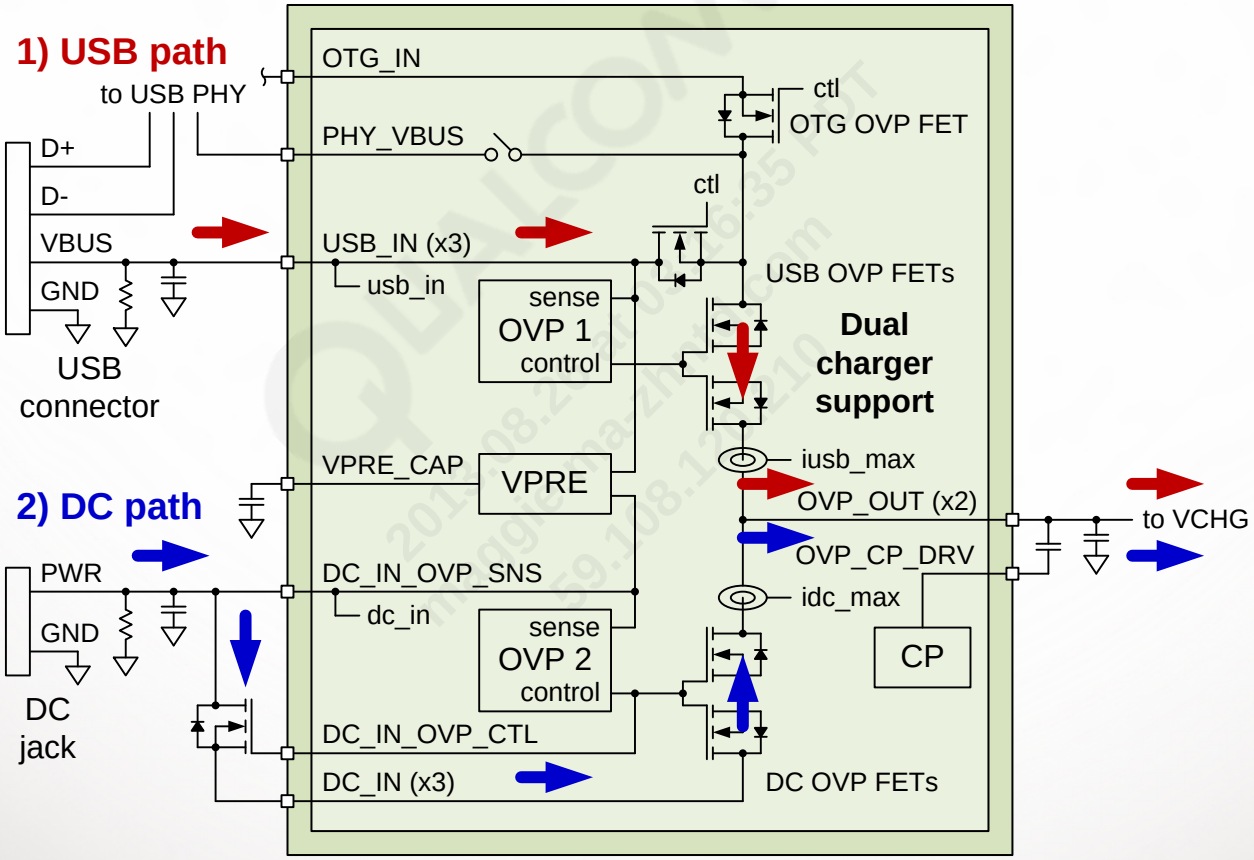




Initializing Fast Charging (2 of 2)

Register	Address	Software control instructions	MSM8974/ MTP example
VDD_MAX		These parameters are battery dependent and must be set during charging initialization if the battery is connected, or when the battery is inserted.	4.2 V
VDD_SAFE			4.2 V
IBAT_MAX			1.5 A
IBAT_SAFE			1.5 A
IBAT_TERM			100 mA
IBAT_TERM_BMS			100 mA
VIN_MIN		Optimal value per charging source V-I curve; 4.3 V allows more high-current IR drop in charger path.	4.3 V
IUSB_MAX		Set based upon USB port-type and enumeration result from USB driver, or relies upon AICL	N/A
IDC_MAX		Set based upon DC charger information or AICL	N/A
TCHG_MAX_EN		Enable for maximum charge timer	
TCHG_MAX		Battery and charging source dependent; increase to 240 minutes if connected to USB SDP (500 mA).	120 min
CHG_TEMP_STOP			120°C (def)
CHG_TEMP_RESUME			95°C (def)

Initializing the Adapter Interfaces and OVP (1 of 3)



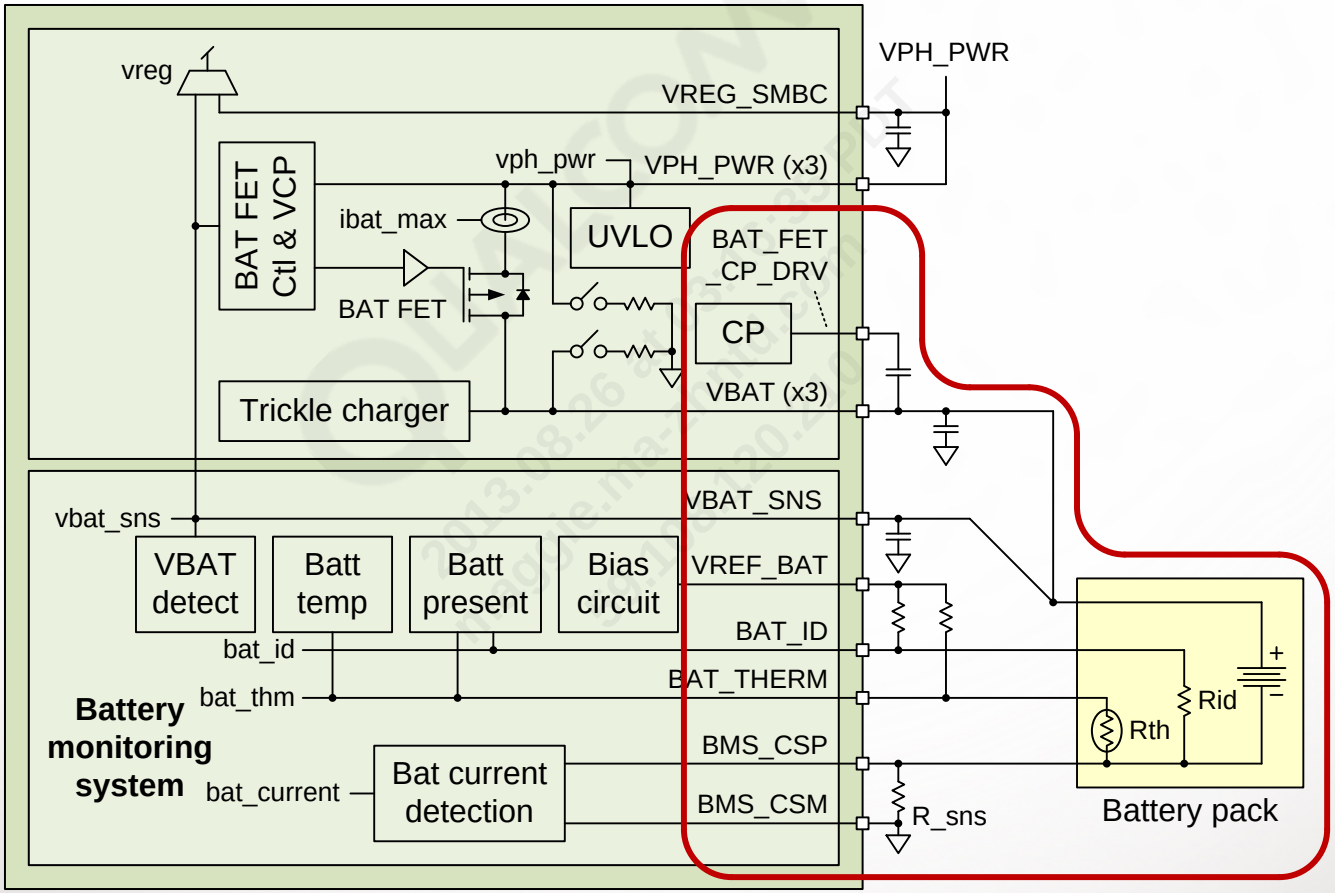
Initializing the Adapter Interfaces and OVP (2 of 3)

USB path			
Register: Bits	**Address**	**Software control instructions**	**MSM8974/ MTP example**
CHG_PTH_CTL: CHG_PTH_PRIORITY_SEL		0 = USB path; no charging through DC path, or to support USB || DC OVP mode. 1 = DC path wired for DC charging port	0b1 = DC (default)
CHG_PTH_CTL: CHG_PTH_SWITCH_TIME		Keeps the default value	0b00 = 60 ms (default)
USB_OVP_CTL: USB_OVP_THR		Keeps default value	0b11 = 11 V (default)
USB_OVP_CTL: USB_UVD_THR		Keeps the default value, although it may be raised due to OVP FET stuck-on issue that causes charger removal detection failure	0b00 = 4.05 V falling, 4.25 V rising (default)
USB_OVP_CTL: USB_VALID_DEB		Keeps the default value	0b01 = 5 ms (default)
IUSB_MAX_EN: EN		Enables/disables IUSB_MAX current limit	0b1 = Enable (default)
IUSB_MAX: IUSB_MAX		Set according to USB charger type; also see the AICL slide.	

Initializing the Adapter Interfaces and OVP (3 of 3)

DC path			
Register: Bits	**Address**	**Software control instructions**	**MSM8974/ MTP example**
DC_OVP_CTL: DC_OVP_THR		Keeps the default value	0b11 = 11 V (default)
DC_OVP_CTL: DC_UVD_THR		Keeps the default value, although it may be raised due to OVP FET stuck-on issue that causes charger removal detection failure.	0b00 = 4.05 V falling, 4.25 V rising (default)
DC_OVP_CTL: DC_VALID_DEB		Keeps the default value	0b01 = 5 ms (default)
IDC_MAX_EN: EN		Enables/disables IDC_MAX current limit	0b1 = Enable (default)
IDC_MAX: IDC_MAX		Set according to DC charger type; also see the AICL slide	

Initializing the Battery Interface (1 of 2)



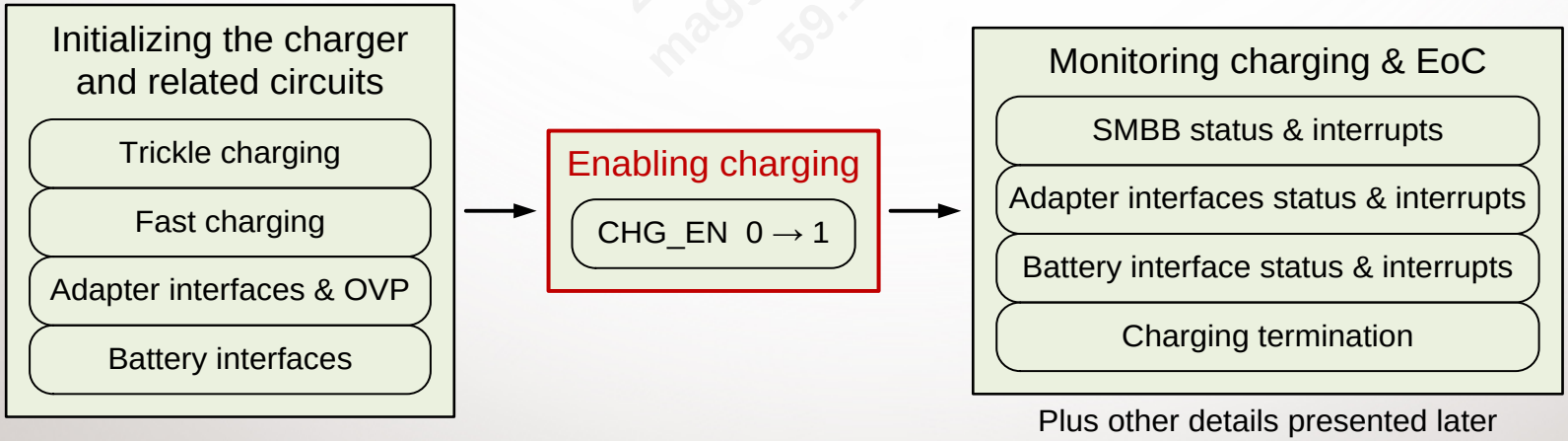
Initializing the Battery Interface (2 of 2)

Register: Bit(s)	Address	Software control instructions	MSM8974/ MTP example
VCP: EN (bit 7)	0x1247		0b1 (default)
BPD_CTRL: BAT_THM_EN (bit 1) BAT_ID_EN (bit 0)	0x1248		0b10 (default)
BTC_CTRL: BAT_TEMP_COMP_EN (bit 7)	0x1249		Default
BTC_CTRL: BAT_TEMP_COLD_THD (bit 1) BAT_TEMP_HOT_THD (bit 0)	0x1249		Default
VREF_BAT_THM_CTRL: EN (bits 7:6)	0x124A		Default
BATFET_CTRL1	0x1290		Default
BATFET_CTRL2	0x1291		Default
BATFET_CTRL3	0x1292		Default
BFCP_CLK_CTRL1	0x1294		Default
BFCP_CLK_CTRL2	0x1295		Default

Enabling Charging in HLOS

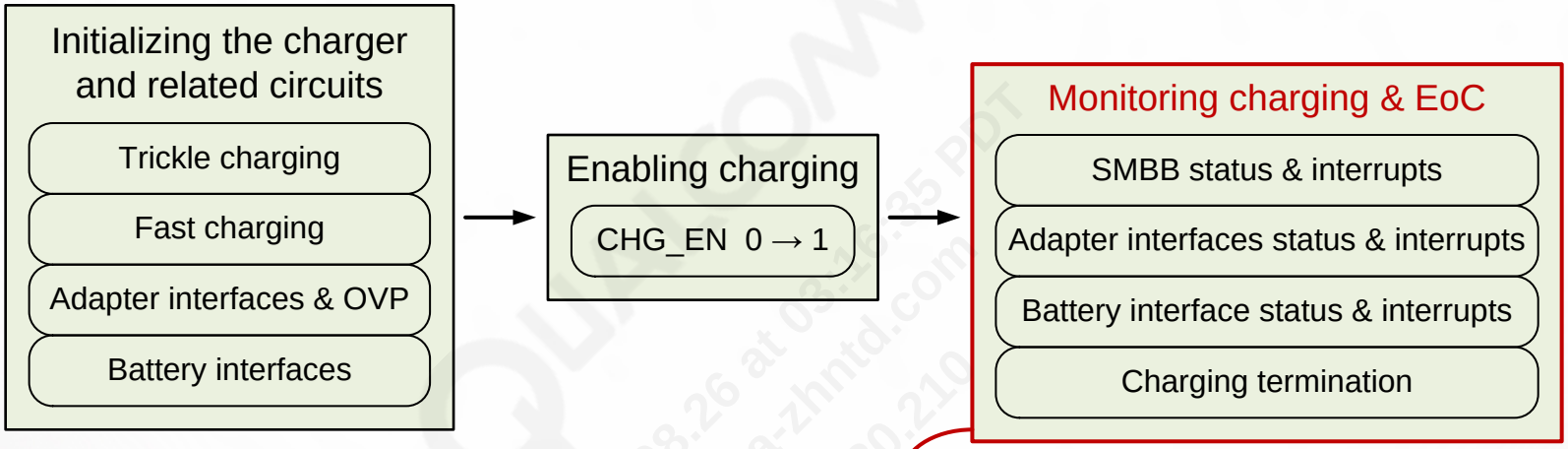
Charging is initiated by the software, but managed by the hardware.

- After charging parameters are properly initialized, the charger software enables hardware-managed autonomous charging by writing:
  `SMBB_CHGR_CHG_CTRL:CHG_EN = 0b1; //` Enable FSM-controlled autonomous charging
- Software-initiated trickle charging
  - If VBAT < VBAT_WEAK, the charger FSM enters this mode after the CHG_EN bit is set to 1.
  - The charger buck converter is on and generates VPH_PWR.
  - The BAT FET is open and the trickle charger charges the battery with IBAT_ATC_A until VBAT reaches VBAT_WEAK.
  - Note that the ATC_B phase is not used hardware-controlled ATC.
- CC/CV fast charging
  - If VBAT > VBAT_WEAK, the charger FSM enters this mode after the CHG_EN bit is set to 1.
  - The charger hardware autonomously manages CC/CV charging.
  - Charging termination is based upon IBAT.
  - Recharge is enabled as needed.



Monitoring Charging and EoC Termination

Monitoring Charging and EoC Termination



Plus other details presented later

- Charger timers
- Buck converter
- Reverse boosting mode
- Battery interface reference voltage
- Battery presence detection
- Battery temperature monitor
- Battery ID
- Battery MOSFET
- Voltage collapse protection

SMBB Status Registers

SMBB_CHGR status registers			
Address	**Register name**	**Indications**	**Expected software usage**
0x1008	CHG_OPTION		Used by PBL
0x1009	Reserved		
0x100A	ATC_STATUS	ATC_DONE ATC_FAILED	Informational; write to ATC_FAILED:CLR if ATC_FAILED flag is 1 to allow future trickle charging.
0x100B	VBAT_STATUS		Informational
0x100C	IBAT_BMS		Informational; used by hardware for charge termination, charging IR drop digital compensation
0x100D	IBAT_STS	BMS_SIGN IBAT_TERM_COMP	Informational; used by hardware for voltage collapse protection termination
0x100E	Reserved		
0x100F	Reserved		

SMBB Interrupts

SMBB_CHGR interrupts			
Bit	**Interrupt**	**Type**	**Expected software usage**
7	CHG_DONE	Rising edge	Informational
6	CHG_FAILED	Rising edge	Write 1 to the SMBB_CHGR_CHG_FAILED: CLR bit to clear the CHG_FAILED flag
5	FAST_CHG_ON	Rising edge	Informational
4	TRKL_CHG_ON	Rising edge	Informational
3	STATE_CHANGE	Rising edge	Informational
2	CHGWDOG	Rising edge	Check charger software condition; restart the charger software if necessary
1	VBAT_DET_HI	Both edges	To be added; replacing BATT_ALARM
0	VBAT_DET_LO	Both edges	To be added; replacing BATT_ALARM

Adapter Interfaces Status Registers and Interrupts

SMBB_USB status registers			
Address	**Register name**	**Indications**	**Expected software usage**
0x1308	PWR_PTH_STS		PBL branch, etc.
0x1309	USB_CHG_PTH_STS		Check USB OV or UV
0x130A	CHG_DONE_INT		Informational
SMBB_USB interrupts			
Bit	**Interrupt**	**Type**	**Expected software usage**
7:3	Reserved		
2	CHG_GONE		Informational
1	USBIN_VALID		Informational
0	COARSE_DET_USB		Informational
SMBB_DC status registers			
Address	**Register name**	**Indications**	**Expected software usage**
0x140A	DC_CHG_PTH_STS		Check DC OV or UV
SMBB_USB interrupts			
Bit	**Interrupt**	**Type**	**Expected software usage**
7:2	Reserved		
1	DCIN_VALID		Informational
0	COARSE_DET_DC		Informational

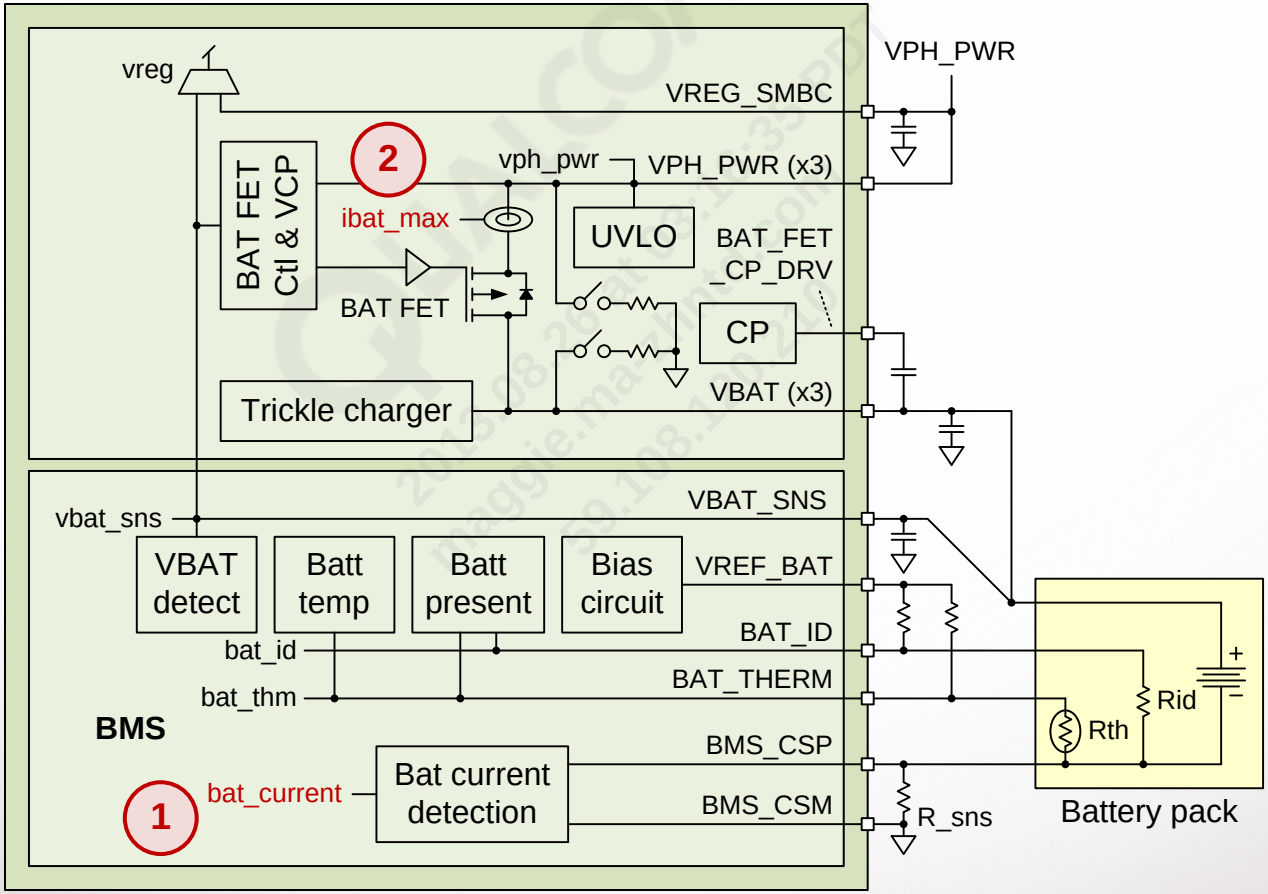
Battery Interface Status Registers and Interrupts

SMBB_BATT_IF status registers			
Address	**Register name**	**Indications**	**Expected software usage**
0x1208	BAT_PRES_STATUS		
0x1209	BAT_TEMP_STATUS		
0x120A	VREF_BAT_THM_STATUS		
0x120B	BAT_FET_STATUS		
0x120C	VCP_STATUS		
SMBB_BATT_IF interrupts			
Bit	**Interrupt**	**Type**	**Expected software usage**
7:5	Reserved		
4	PSI		
3	VCP_ON		
2	BAT_FET_ON		
1	BAT_TEMP_OK		
0	BAT_PRES		

Charging Termination (1 of 2)

Two charging termination methods are supported:

1. Digital end-of-charge (DEoC) – uses IBAT measurement from the BMS
2. Analog end-of-charge (AEoC) – uses IBAT sensed through the BAT FET



Charging Termination (2 of 2)

DEoC uses IBAT measurement from the BMS.

- The BMS periodically measures IBAT and sends a 9-bit report to the SMBB (1-bit sign, 8-bit magnitude).
- During fast charging, SMBB compares the IBAT_BMS value with a programmable threshold (IBAT_TERM_BMS; 8-bit unsigned, 1 LSB = 17.28 mA), and terminates charging when eight consecutive valid IBAT_BMS measurements are lower than IBAT_TERM_BMS.
- This feature has been supported since PM8941 version 2.0; benefits compared with the AEoC scheme:
  - BMS-grade EoC current accuracy (better than ±5 mA)
  - Much finer EoC granularity (17.28 mA steps)
- DEoC is recommended for PM8941 version 2.0 and newer implementations.
- To use DEoC:

```
SMBB_CHGR_IBAT_TERM_CHGR = 0x8X; // IEOC_SEL = 1 (select DEoC)
SMBB_CHGR_IBAT_TERM_BMS = 0x0B; // DEoC threshold; 1 LSB = 17.28 mA
```

- NOTE: For DEoC to work properly, the BMS IADC offset has to be calibrated; if not, IADC1_USR: CADC_OFFSET1 and CADC_OFFSET0 is 0xC000 (default). After calibration, CADC_OFFSET1 (MSB) usually reads 0xBX.

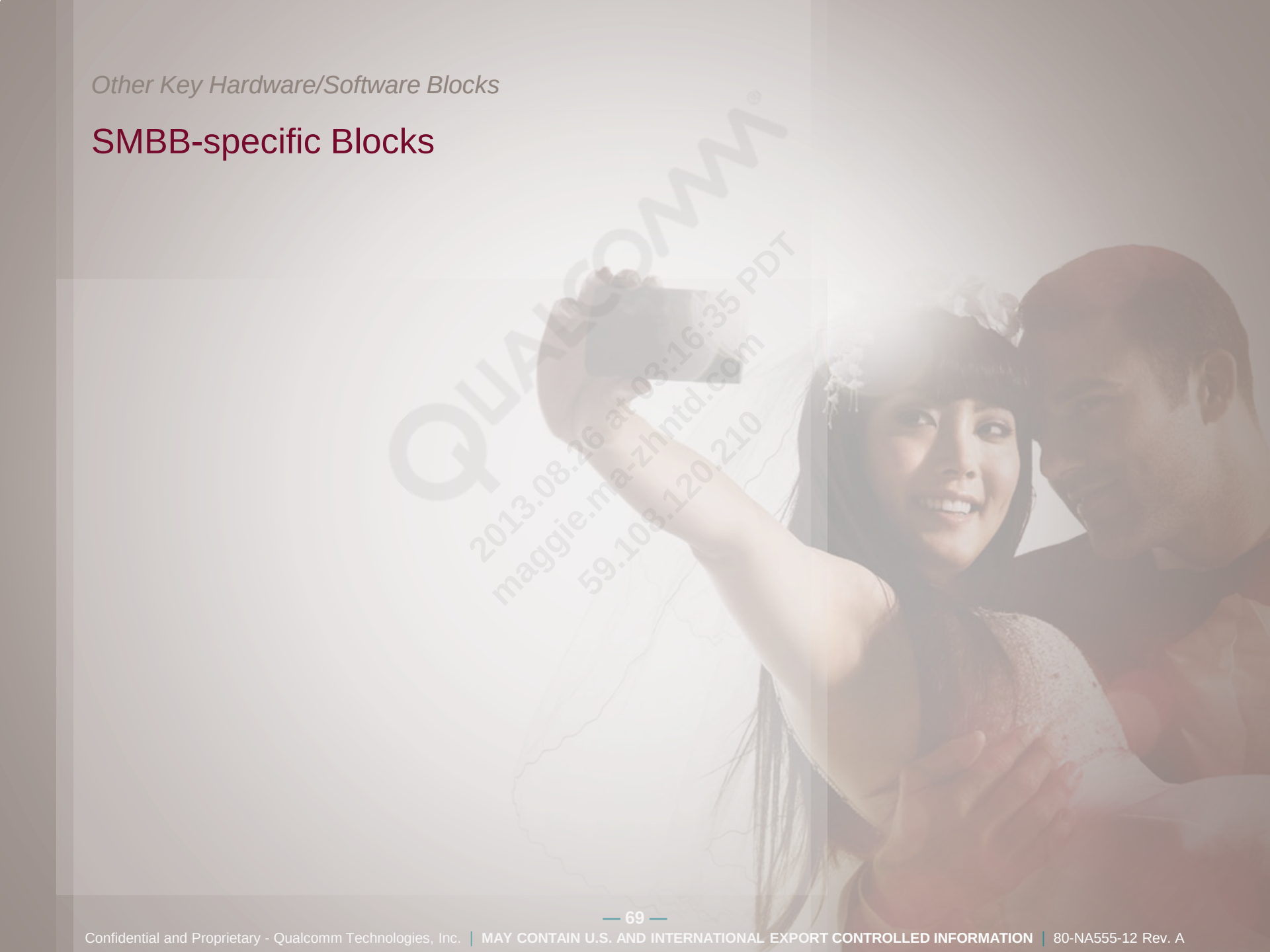
AEoC uses IBAT sensed through the BAT FET.

- This feature has been supported since PM8941 version 1.0.
- Do not use this EoC method except for PM8941 version 1.0 implementations.
- To use AEoC:

```
SMBB_CHGR_IBAT_TERM_CHGR = 0x0B; // IEOC_SEL = 0 (select AEoC), COMP_EN = 1,
THR_SEL = 11(200 mA)
```

Other Key Hardware/Software Blocks

SMBB-specific Blocks



Charger Timers

TTRKL_MAX – maximum trickle charging timer with enable/disable bit.

TCHG_MAX – maximum total charging timer with enable/disable bit.

- When TTRKL_MAX or TCHG_MAX expires, the FSM moves through the CHG_FAIL_9 state and sets a CHG_FAILED bit, which also generates CHG_FAILED_IRQ.
- The CHG_FAILED bit remembers that charging has failed, barring future entry to fast or trickle charge states until software sets the SMBB_CHGR_CHG_FAILED:CLR bit.

Charger watchdog (CHG_WDOG)

- Charger software can enable a dedicated hardware watchdog timer to ensure that the charging control software remains alive.
- Once enabled, charger software needs to periodically 'pet the dog' during any FSM-controlled charging (trickle, CC/CV, and even when charging is paused due to battery temperature moving out of range, etc.).
- If not petted, the watchdog will 'bark' (generate an interrupt) and eventually 'bite' (stop charging) after a programmable delay (5 sec default).
- Charger watchdog registers are listed below.

Register	Address	Software control instructions	MSM8974/MTP example
CHG_WDOG_TIME	0x1062		
CHG_WDOG_DLY	0x1063		
CHG_WDOG_PET	0x1064		
CHG_WDOG_EN	0x1065		

Charger Buck Converter (1 of 2)

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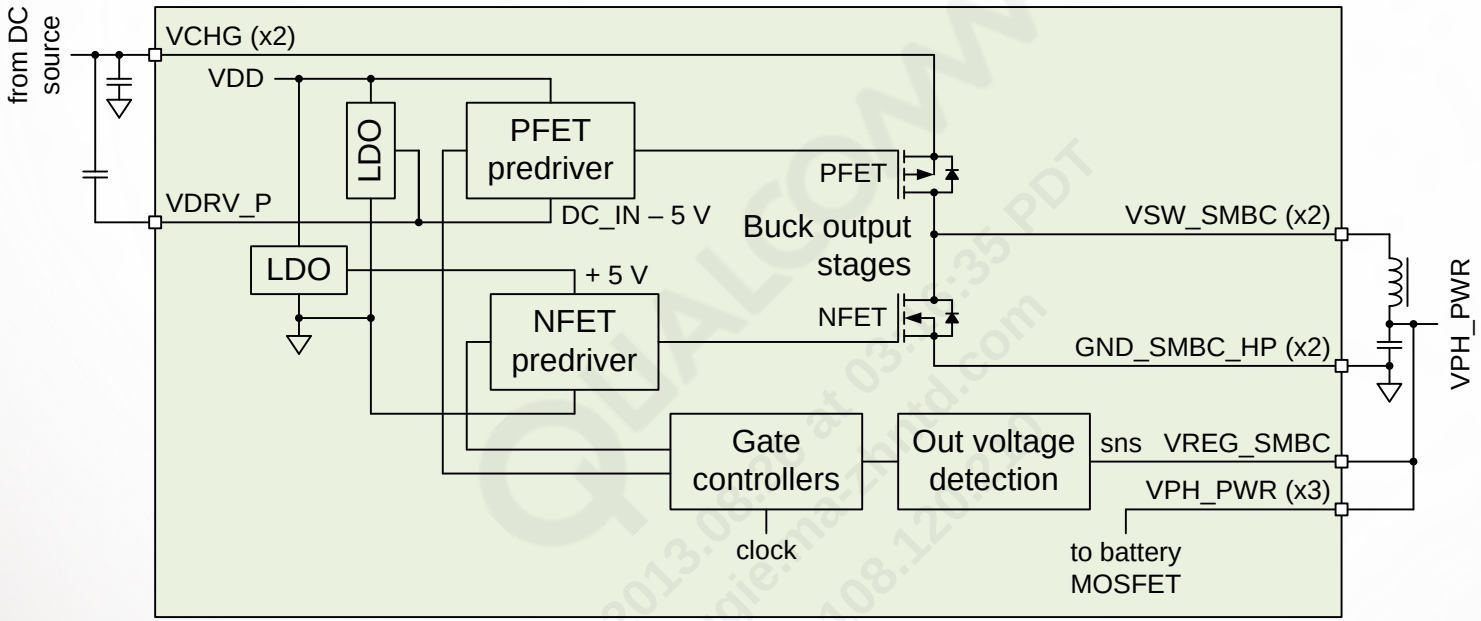


Controls

- ENABLE_CONTROL:
  - Bit 7 (BUCK_EN) forces SMBB buck converter on; used during test and in stack-cell application where the buck can be used as a general 5 V supply for flash, OTG, and HDMI.
  - Bit 0 (FOLLOW_HW_EN) is used by the SMBB FSM.
- Voltage setting control: use VDD_MAX () in SMBB_CHGR.

Charger Buck Converter (2 of 2)

Analog parameter configurations

- Analog parameters should be kept in their default states (VDD, VCHG, IBAT, ICHG_GM_CTRL, XX_LOOP_COMP_RES, etc.).

SMBB_BUCK status registers			
Address	**Register name**	**Indications**	**Expected software usage**
0x1108	BUCK_OK		Informational
SMBB_BUCK interrupts			
Bit	**Interrupt**	**Type**	**Expected software usage**
7	Reserved		
6	VDD_LOOP		Informational
5	IBAT_LOOP		Informational
4	ICHG_LOOP		Informational
3	VCHG_LOOP		Informational
2	OVERTEMP		Reduce charging current
1	VREG_OV		Informational
0	VBAT_OV		Informational

Reverse Boosting Mode (1 of 3)

The SMBB supports two boosting modes:

1. Flash supply – For camera flash lighting; typical flow:

- When flash is enabled, it sends a flash_en signal to SMBB to request VCHG.
- SMBB checks its conditions, exits charging if that's its current mode, and begins reverse boost operation to generate VCHG from VBAT; there are two reverse boost charger sub-modes:
  - Voltage mode: Bharger™ regulates VCHG voltage
  - Adaptive mode: Bharger regulates flash driver headroom
- SMBB signals power_good back to flash
- Flash module then draws current and flashes; at the end, it lowers the flash_en signal, allowing the SMBB to return to its original state.
- For additional details, see the *PM8941 Lighting Subsystem Hardware/Software Document* (80-NE399-11).

2. General 5 V supply – For applications, such as USB-OTG and HDMI

Reverse Boosting Mode (2 of 3)

Controls

- BOOST_VSET (0x1541): Sets the boost output voltage
  - BOOST_VSET_UL (0x1569)
  - BOOST_VSET_LL (0x156B)
- ADAPTIVE_BOOST_MODE (0x1544): Selects adaptive mode to be software forced or to follow hardware signals (default)
- BOOST_PASS_MODE (0x1545): Enables/disables boost pass mode for high-voltage battery
- ENABLE_CONTROL (0x1546): Software forces the boost on or it follows hardware signal (flash_en)
- BOOST_SOFT_START (0x154C): Enables/disables boost soft start feature
- BOOST_OVP_SEL (0x1570): Selects boost OVP threshold
- Others kept at their default states: BOOST_GM_CTRL (0x1572), _RZERO_CTRL (0x1573), _CZERO_CTRL (0x1574), _HIPOLE_CTRL (0x1575), _MAX_DUTY (0x1576), _SLOPE_COMP (0x1577), BOOST_ILIM (0x1578), and IPZ_EN (0x1579)

Interrupts

- BOOST_PWR_OK
- LIMIT_ERROR: When VSET is outside UL or LL

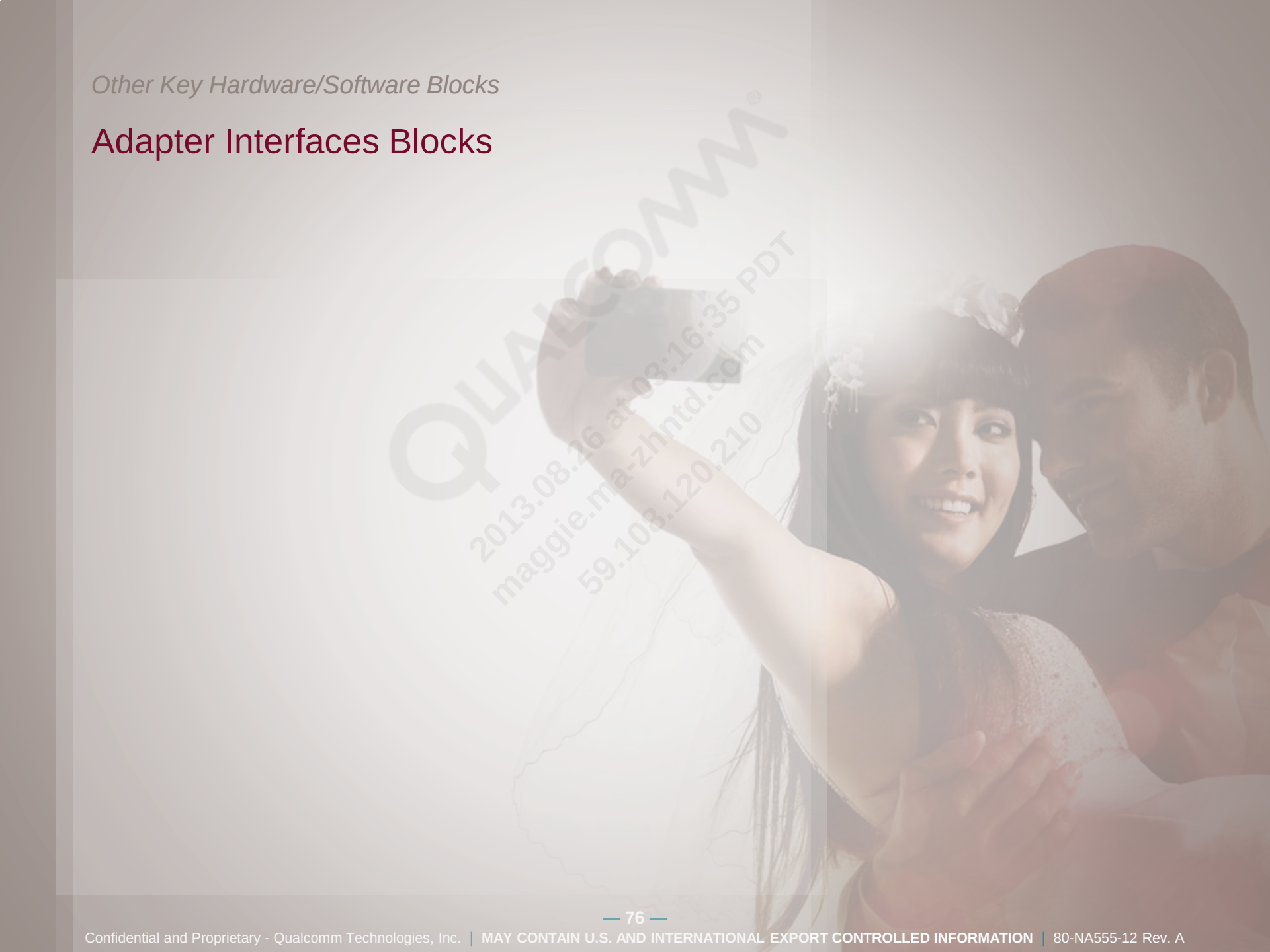
Status

- BOOST_STATUS: indicates BOOST_PWR_OK, and whether VSET is outside UL or LL.

Reverse Boosting Mode (3 of 3)

SMBB_BUCK status registers			
Address	**Register name**	**Indications**	**Expected software usage**
0x1508		Status	Informational
SMBB_BUCK interrupts			
Bit	**Interrupt**	**Type**	**Expected software usage**
7	Reserved		
6	Reserved		
5	Reserved		
4	Reserved		
3	Reserved		
2	Reserved		
1	LIMIT_ERROR		TBD
0	BOOST_PWR_OK		TBD

Adapter Interfaces Blocks

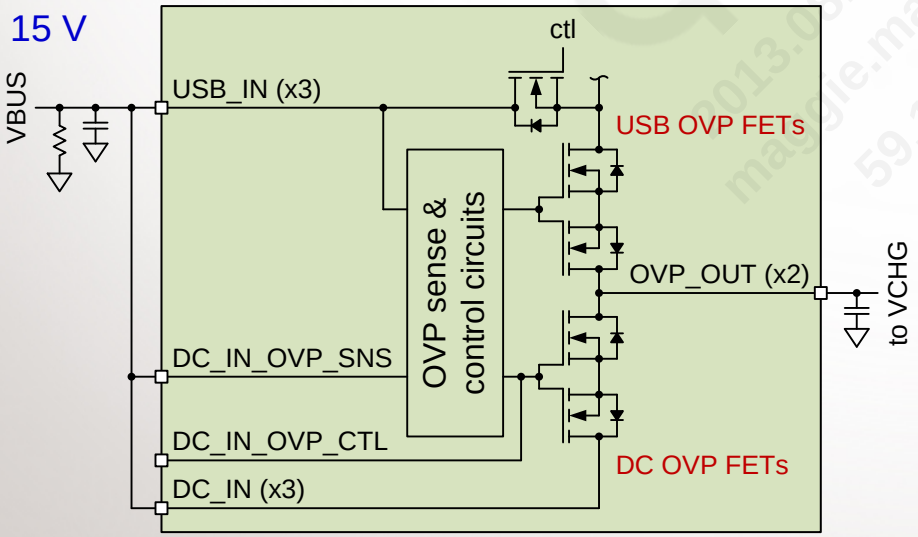


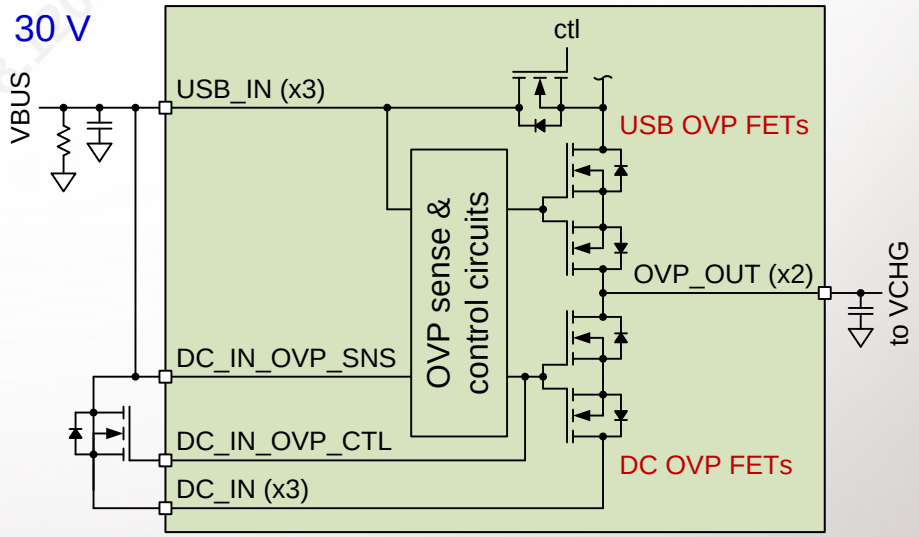
Parallel USB and DC (USB || DC) OVP Mode (1 of 2)

The SMBB integrates both USB and DC OVP FETs; when a design has a single charging port (most likely the USB port), the internal USB and DC OVP FETs can be operated in parallel to reduce Rds(on) and improve battery charging time. To use this USB || DC OVP mode:

Hardware (see diagrams below)

- If only 15 V OVP tolerance is required, short USB_IN, DC_IN, and DC_OVP_SNS pins together.
- If 30 V OVP tolerance is required, install an external DC OVP FET between DC_OVP_SNS and DC_IN, and then short USB_IN to DC_OVP_SNS.





Parallel USB and DC (USB || DC) OVP Mode (2 of 2)

Software

- USB_IN path is given priority during charger initialization; when both charging paths are valid, SMBB selects USB_IN and initiates the USB charger type detection and enumeration.

  ```
  SMBB_USB_CHG_PTH_CTL:CHG_PTH_PRIORITY_SEL = 0b0; //
  ```

- When a charger is connected, USB OVP FET turns on automatically and software forces DC OVP FET on

  ```
  SMBB_DC_SEC_ACCESS = 0xA5
  SMBB_DC_COMP_OVR1 = 0x0F; // for PM8941 version 2.0 only: override DCIN_UL and LL comps to 1
  SMBB_DC_SEC_ACCESS = 0xA5
  SMBB_DC_DC_OVP_FORCE = 0xC0; // force DC OVP FET on
  ```

- When the SMBB is in the USB || DC OVP mode, IUSB_MAX is effective in limiting the input current, even though the current splits between the USB and DC OVP FETs.

AICL

- SMBB features hardware AICL for both USB and DC charging paths.
- Full support is available in PM8941 versions 3.0.
- Software instructions will be included in future revisions of this document.

USB-specific Topics

USB-OTG

To enter USB-OTG host mode:

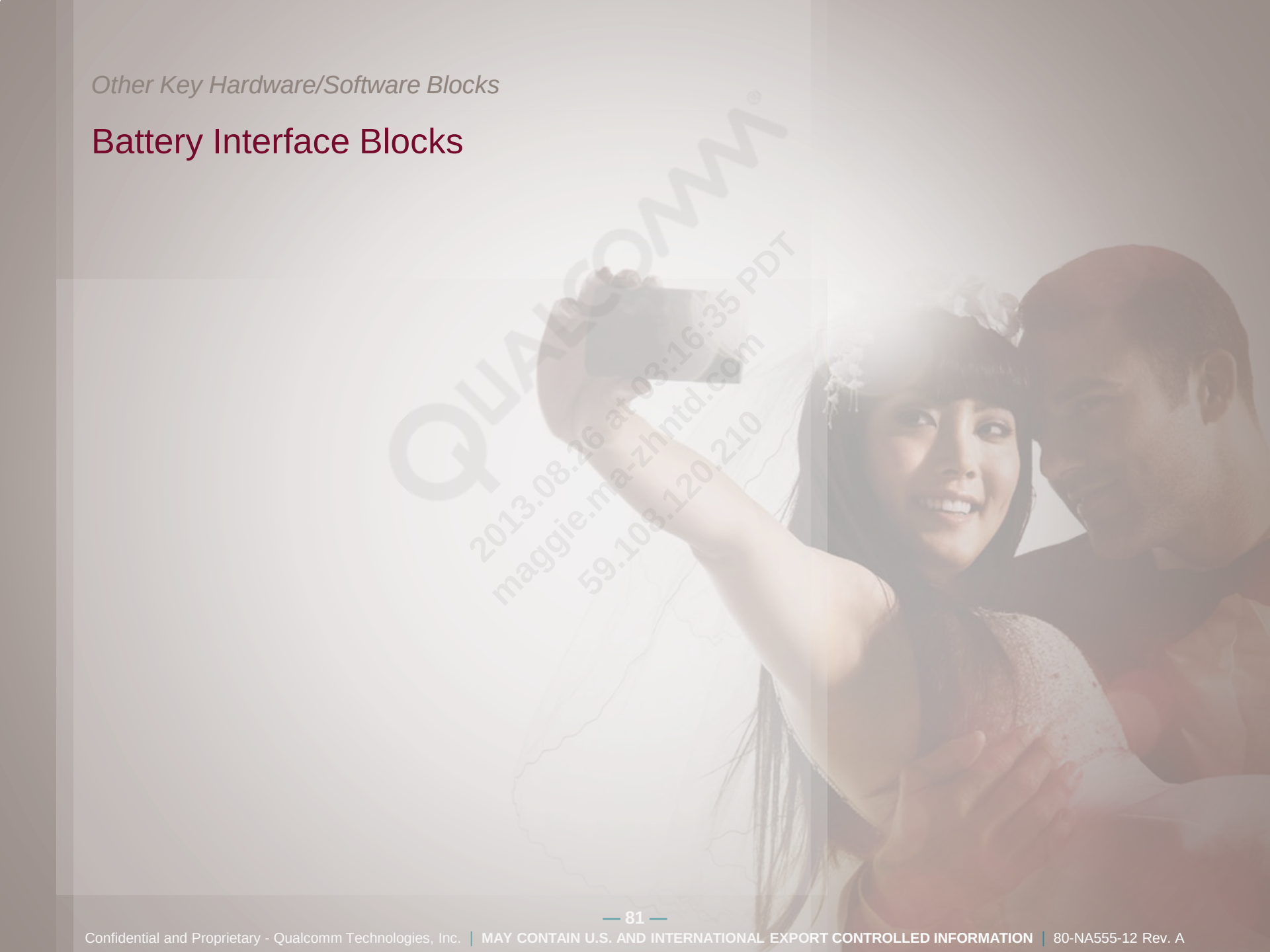
- Vote to turn on the PMIC 5V boost
- Set the USB_OTG_CTL: USB_OTG_EN bit (0x1348 bit0)
- Use USB_OTG_EN bit to turn on both the USB-OTG OVP FET and the top USB OVP FET, thereby connecting OTG_IN to USB_IN
- The USB_OTG_EN bit also forces the SMBB to ignore the USBIN_VALID state and to run off the battery (same effect as USB_SUSP: USB_SUSPEND), unless a DC charger is connected (in which case the SMBB runs off the DC charger).
- Turn on the OTG MVS (allows use of the MVS soft-start feature).

USB suspend

When the USB_SUSP: USB_SUSPEND bit is set:

- The SMBB is forced to ignore the USBIN_VALID state and to run off the battery, unless a DC charger is connected (in which case the SMBB runs off the DC charger).
- SMBB draws less than IDD_USB (1.5 mA) from the USB_IN pin.

Battery Interface Blocks



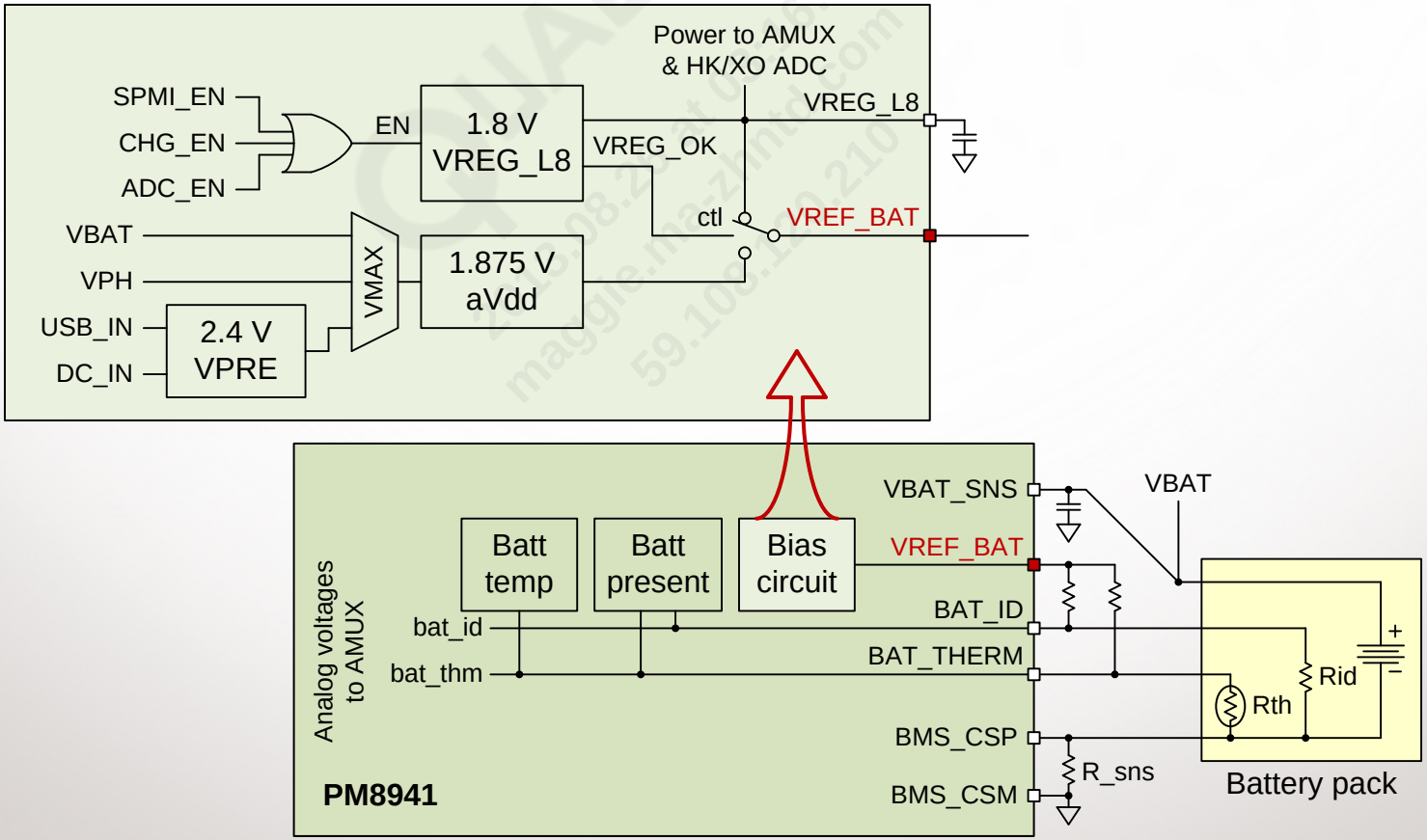
Battery Interface Reference Voltage (VREF_BAT)

Control

- VREF_BAT_THM_CTRL (0x124A) enables software to force VREF_BAT on or off (via SPMI_EN), or lets it be controlled by the SMBB FSM (via CHG_EN).

Status

VREF_BAT_THM_STATUS (0x120A) indicates the VREF_BAT state (on or off), and whether its supply voltage is sourced from the 1.875 V aVdd or the 1.8 V LDO.



Battery Presence Detection

SMBB battery presence detection (BPD) is based upon monitored voltages at BAT_THM and BAT_ID pins.

- When a battery is not present, pull-up resistors force BAT_THM and BAT_ID to the PMIC's internally generated VREF_BAT reference voltage.
- When a battery is present, the battery pack's thermistor and ID resistor provide current paths that reduce the voltages at BAT_THM and BAT_ID to less than 95% of VREF_BAT.

Control

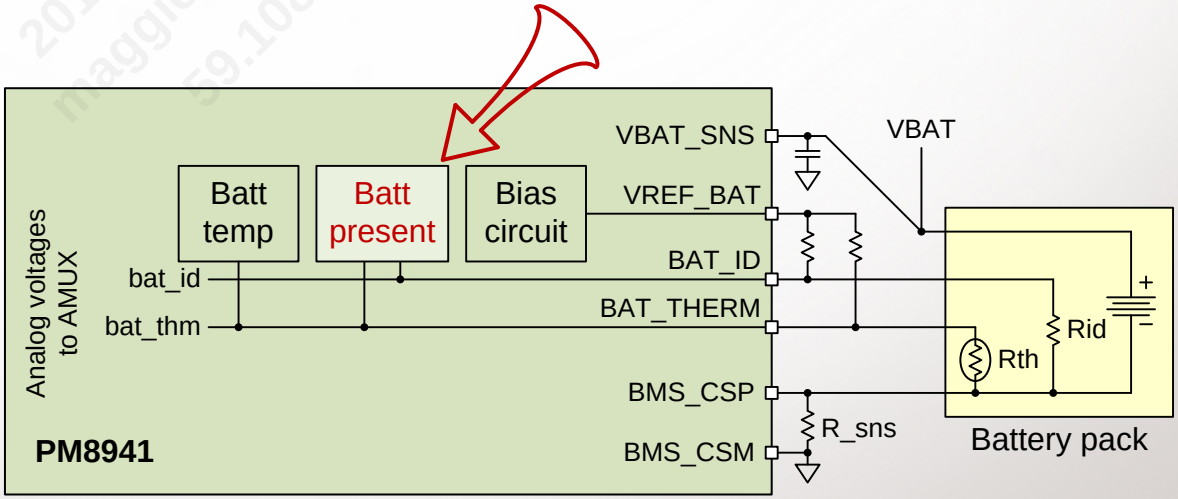
- BPD_CTRL (0x1248) allows software to select whether BPD monitors BAT_THM or BAT_ID or both; each has a dedicated enable bit (BAT_THM_EN and BAT_ID_EN)
  - Enabling each bit depends upon the battery pack, and whether it includes a thermistor and/or ID resistor

Interrupt

- BAT_PRES should be configured to trigger on both edges to ensure both battery insertion and battery removal are captured.

Status

- BAT_PRES_STATUS (0x1208) indicates the overall battery presence or absence and also indicates the individual BAT_THM and BAT_ID information.



Battery Temperature Monitor (1 of 2)

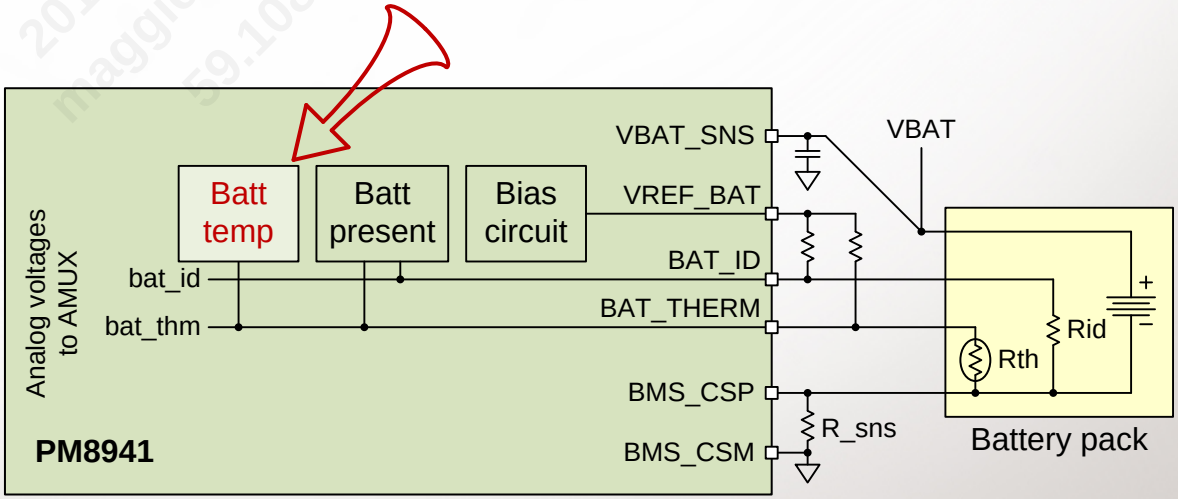
- The battery temperature monitor (BTM) is software-configured during charger initialization, before enabling hardware-managed autonomous charging; BTM initialization parameters are listed on the next slide.
- Once the BTM is enabled by setting CHG_BATT_TEMP_DIS = 0, the analog comparators continuously monitor the battery thermistor voltage and pauses charging whenever the battery is too cold or too hot.
- Interrupts are generated to allow charger software to pause pertinent timers, if appropriate.
  NOTE: By default, the BTM is disabled before the software configuration; this prevents BTM operation during the first hardware-controlled ATC. Since the BTM parameters are backed up by xVdd, once the BTM is configured and enabled, it is available for subsequent ATCs as long as the coin cell voltage VCOIN is above 2 V, even if the battery is removed or deeply discharged.

Control

- BTC_CTRL (0x1249) allows software to enable or disable the battery temperature comparators (BTCs) and to set the thresholds for the cold and hot comparators.

Interrupt

- BAT_TEMP_OK should be configured to trigger on both edges to ensure both battery temperature out-of-range and in-range transitions are captured.



Battery Temperature Monitor (2 of 2)

Status

- BAT_TEMP_STATUS (0x1209) indicates whether the battery temperature is OK, cold, or hot.

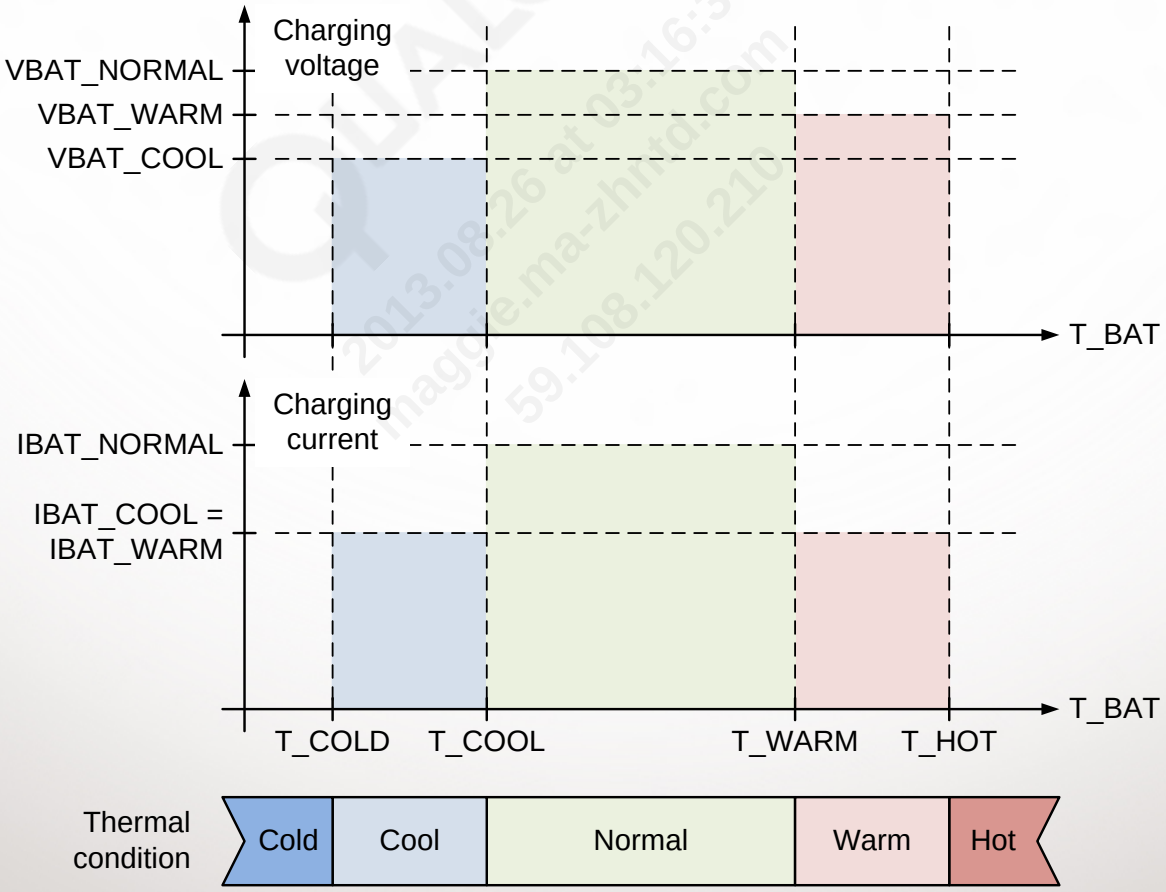
Japan Electronics and Information Technology Industries Association (JEITA) compliance

- The SMBB is JEITA compliant; see details on JEITA Compliance slide.

SMBB BTM initialization parameters			
Parameter bit	**Address**	**Software control instructions**	**MSM8960/ MTP example**
EN_VREF_BATT_THERM		Set to 1 if BAT_THM and BAT_ID pull-up resistors are connected to VREF_BAT	1
CHG_BATT_TEMP_REF_GND		▪ 0 = BMS_CSP if battery thermistor is inside the battery pack. ▪ 1 = CHG_GND if battery thermistor is not inside the battery pack.	0 (BMS_CSP)
CHG_BATT_TEMP_DIS		Set to 0 whenever using SMBB to monitor battery temperature	0
CHG_BATT_TEMP_THR_COLD		70% when charging within traditional battery temperature range (0 ~ 45 ºC) 80% when charging over extended battery temperature range (JEITA)	0 (75%)
CHG_BATT_TEMP_THR_HOT		35% when charging within traditional battery temperature range (0 ~ 45 ºC) 25% when charging over extended battery temperature range (JEITA)	1 (35%)

JEITA Compliance (1 of 3)

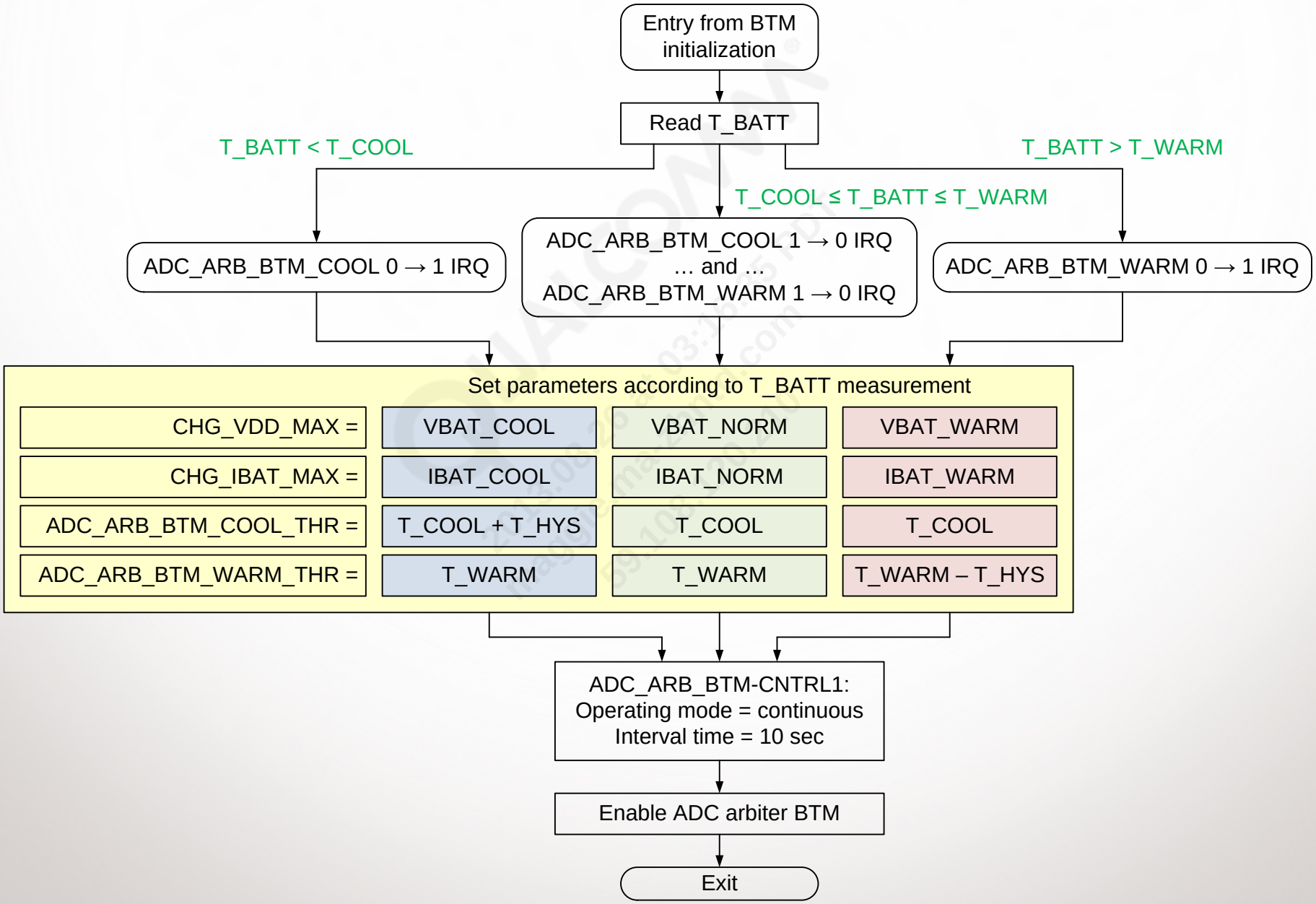
- The JEITA standard allows battery charging with reduced charging voltage and/or current outside the conventional battery temperature range (illustrated below).
  - Temperature threshold points (TCOLD, TCOOL, TWARM, and THOT) are determined by battery chemistry and vary with different battery vendors; the thermistor temperature coefficient also varies.
  - As a result, the BAT_THM voltages corresponding to the temperature points have much variance.
- JEITA compliance is mandatory in Japan after November 2011.
- Also see *A Guide to the Safe Use of Secondary Lithium Ion Batteries in Notebook-type Personal Computers*.



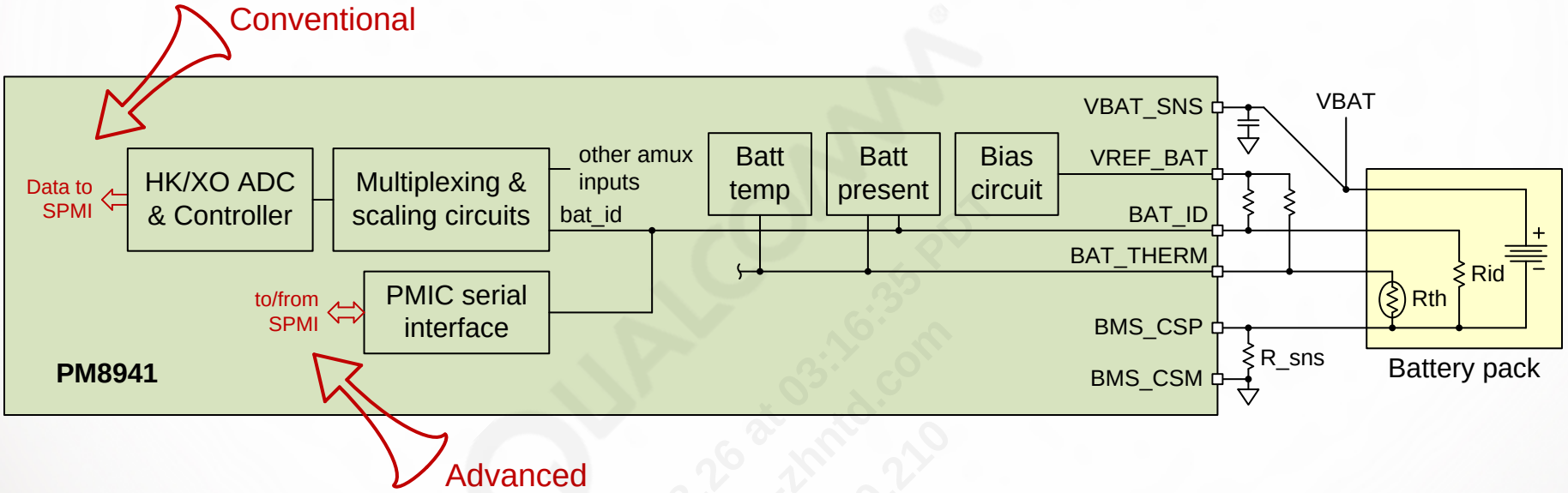
JEITA Compliance (2 of 3)

- SMBB BTM comparators have limited thresholds configurability that helps cover both the traditional battery charging temperature range and the extended JEITA temperature range.
  - 25% or 35% for the COLD comparator; 70% or 80% for the hot comparator
- The TCOLD and THOT trip points can be adjusted by selecting the two external pull-up resistors.
- TCOOL and TWARM thresholds cannot be adjusted.
- The SMBB uses an automated digital BTM routine to monitor the battery cool and warm conditions.
- If enabled, the battery temperature is automatically measured by the ADC arbiter in programmable intervals up to 16 seconds.
- The battery temperature measurement result is compared with programmable cold and warm thresholds; interrupts are generated if either of the thresholds are exceeded.
  - Charger software needs to adjusts the VBAT_MAX and IBAT_MAX accordingly.
  - To prevent oscillation when the battery temperature is near the thresholds, the software also needs to adjust the thresholds to include temperature hysteresis when entering the cool or warm region.
- JEITA-compliant BTM initialization and interrupt response is shown on the next slide.

JEITA Compliance (3 of 3)



Battery ID (1 of 2)



Conventional battery identification method – software determines the battery pack's ID resistor value:

- BAT_ID voltage is measured via PMIC AMUX and HK/XO ADC.
- Knowing VREF_BAT and the external pull-up resistor value, software can determine the ID resistor value.
- The battery type is determined using a prestored, OEM-configurable RBAT_ID look-up table.

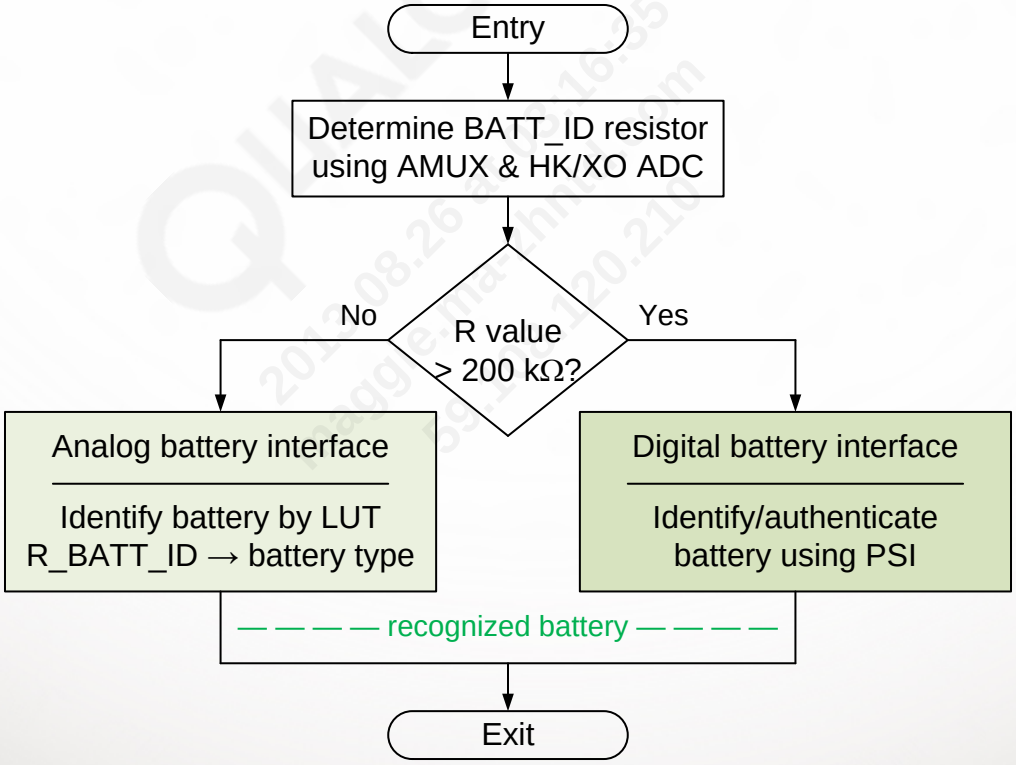
Advanced battery identification/authentication method – digital communication with battery over BAT_ID

- Batteries with digital communication capability have a special ID resistor value.
- If the special ID resistor value is detected (such as RBAT_ID > 200 kΩ in the example below), software starts communicating with the battery digitally using the PMIC Serial Interface (PSI).

The battery ID concept is illustrated on the next slide.

Battery ID (2 of 2)

The battery ID concept is shown here.



Battery MOSFET

- The PMIC includes an integrated NMOS battery FET.
- A control loop is able to regulate the BAT FET Rds(on) to a constant value around 10 mΩ, thereby making it possible for the BMS to sense IBAT.
- The BAT FET and the constant Rds(on) control loop is driven by an internal charge pump that operates in high, normal, or low power mode (HPM/NPM/LPM) depending upon charger presence and PMIC sleep_b.

Control

- BATFET_CTRL1/2/3 (0x1290, 0x1291, 0x1292) for BAT FET constant Rds(on) control loop; use the default.
- BFCP_CLK_CTRL1/2 (0x1294, 0x1295) for BAT FET CP clock rate in HPM, NPM, and LPM; use the default.

Interrupt

- BAT_FET_ON

Status

- BAT_FET_STATUS (0x120B) indicates BAT FET on/off and BAT FET CP status (HPM/NPM/LPM).

Voltage Collapse Protection

The PMIC prevents a sudden load from inadvertently collapsing the VDD voltage.

- When a valid external charger is connected, and the battery is either fully charged or too hot or cold to be charged, the battery FET is opened and the system runs off the external charger.

If the external charger's current limit is exceeded, VCP is executed:

- If VPH_PWR drops 60 mV below VBAT, VCP is activated
- The battery FET is turned on, allowing the battery to supplement the external source
  - Turn-on is a single-step, not a linearly regulated process
- With the added battery current, the system's high current doesn't cause VDD to collapse
- The battery FET is turned off when the excessive current condition ends
  - When > 100 mA flows into the battery … or …
  - When 0 to 5 mA flows into the battery for at least 1 second
- Battery FET turn-on time is fixed at 5 μs max; the turn-off time is 1 μs by default, but can be increased to 10 μs via SPMI

Control

VCP: EN (0x1247<7>) allows software to enable/disable the VCP feature; keep it enabled.

Interrupt

VCP_ON

Status

VCP_STATUS (0x120C) indicates the VCP on/off status, and the VCP_DET comparator output.

Known Issues and Hardware/Software Workarounds

Charger Removal Detection

Issue 1: accidental reverse boosting (ARB)

SMBB 2.0 adds circuits to reliably detect and stop ARB

- Tests show that the HW ARB stopper circuits work properly.
- However, these circuits are not enabled by default in SMBB 2.0, and the enable bits are protected (not accessible by mission software). This is corrected in SMBB 3.0.
- Workaround is needed for mission software to detect and stop ARB for SMBB 2.0.
- ARB happens much more easily on SMBB 2.0, even with low voltage battery: During ATC_B, if the charger is removed, the PMIC reverse boosts the battery voltage. This is due to a SMBB buck zero crossing comparator malfunction, which is also being fixed in SMBB 3.0.

Issue 2: UVD falling threshold

SMBB 2.0 has increased the default UVD falling threshold to 4.05 V, and makes this threshold programmable.

Tests show that this method prevents the OVP FET from being stuck on with high-voltage (4.35 V) batteries.

Voltage Collapse Protection (1 of 2)

Issue 1: VCP not working if BAT FET CNST_RDS_ON is disabled

Root cause

- BAT FET charge pump switch enable is turned off when CNST_RDS_ON is disabled.
- This puts an extra load on the charge pump and causes delay in turning on the BFET.

Fixes

- SMBB 3.0 hardware fix: Remove cnst_rdson from the charge pump switch enable logic.
- SMBB 2.0 software workaround: Keep CNST_RDS_EN = 1 (default).

Issue 2: VCP failure upon charger insertion with high system load

Issue symptom

- If the system load is high prior to charger insertion, VCP does not function after charger insertion.
- This causes system UVLO resets shortly after insertion.

Root cause

- ichg_end comparator default state mistriggers VCP termination; the sequence of events:
  - Before charger insertion, BFET is on (on_bat); VPH is more than 60 mV lower than VBAT due to the high system load.
  - Upon charger insertion, BFET turns off (on_chg); VCP_DET triggers almost instantaneously.

Problem

- ichg_end comparator (also used for VCP termination) is just enabled and warming up, and its output = 0 (meaning IBAT > IBAT_TERM) which causes VCP termination and opens BFET.
  - No more VCP event triggers because VCP_DET remains high and VCP events are triggered by a rising edge on VCP_DE.T
  - VPH drops to UVLO falling threshold (2.5 V), and the PMIC resets.

Voltage Collapse Protection (2 of 2)

Issue 2: VCP failure upon charger insertion with high system load (continued)

Fixes

- SMBB 3.0 hardware fix: Blank ichg_end comparator for 10 to 20 μs during transition to on-chg state (long enough for it to warm up and settle)
- SMBB 2.0 software workaround: multiple steps
  - IUSB_MAX = 100 mA by default, which forces the charger to run from the battery with BFET on (VCP is not required)
  - After USB charger insertion, USB software performs USB charger type detection and enumeration; it then requests charger software to increase IUSB_MAX accordingly
  - When charger software increases IUSB_MAX from its 100 mA default, this procedure is followed:

```
WR SMBB_BUCK_SEC_ACCESS = 0xA5
WR SMBB_BUCK_ COMPARATOR_OVRIDE_3 = 0x0C (Mask 0x0C) // ICHG_END_VCP_CMP_OVRD = 11
Increase IUSB_MAX from 100 mA to XX mA
Delay 200 ms
WR SMBB_BUCK_SEC_ACCESS = 0xA5
WR SMBB_BUCK_ COMPARATOR_OVRIDE_3 = 0x00 (Mask 0x0C) // ICHG_END_VCP_CMP_OVRD = 00
```

Note: This workaround does not work for the DC path; this was acceptable in the MTP8974 reference design because it does not have a DC charging port.

False BAT_HOT Preventing Charging or ATC

Issue 1: BAT_THM and BAT_ID are pulled down by VADC/AMUX when LDO_8 is off

Root cause

- BAT_THM and BAT_ID go through a CMOS transmission gate within the analog multiplexer.
- The PFET body (VDDA) is connected to VREG_L8.
- When L8 is off and BAT_THM and BAT_ID are pulled-up high (to VREF_BAT), the p-n junction turns on and pulls BAT_THM and BAT_ID low.

SW workaround

- Enable L8 during software-initiated charging.

  `LDO8_EN_CTL = 0x80; //` Forces LDO_8 on
- Disable battery temperature comparators for ATC

  `SMBB_BAT_IF_BTC_CTRL bit 7 = 0b0`

SMBB 3.0 hardware fix

- The PFET body is connected to aVdd or dVdd.

CHG_OPTION Detection

The CHG_OPTION detection does not work when powered from the battery.

Useful Scripts

PTE Bench Script to Start Charging – SMBB Version 1.0

_SMBB_INIT_1.0.csv

```
1   ;;;; Unblock SEC_ACCESS & TEST_EN
2   ;;;; UnComment this section of code on PTE or TF bench only as-needed
3   ;Reg_Write_ExtL1,0xD0,0xA5,MISC,SEC_ACCESS
4   ;Reg_Write_ExtL1,0xE0,0x80,MISC,TEST_ACCESS_EN = 1
5   ;DIO_Write_Bit,TEST_EN,0x01,PM_DIO,
6   ;Delay_mS,,10,PM_DIO,
7
8   ;;;; PM8941 1.0
9   ;;;; Required initialization for charging
10  Reg_Write_ExtL1,0x42,0x80,SMBB_MISC,BOOT_DONE=1
11  Reg_Write_ExtL1,0x62,0xA0,SMBB_CHGR,Disable CHG_WDOG
12  Reg_Write_ExtL1,0xE5,0x28,SMBB_BAT_IF,BAT_HOT/COLD Override
13  Reg_Write_ExtL1,0x90,0x72,SMBB_BAT_IF,CNST_RDS_EN = 0
14  Reg_Write_ExtL1,0x47,0x00,SMBB_BAT_IF,VCP_EN = 0
15  Reg_Write_ExtL1,0x5B,0x0B,SMBB_CHGR,IEOC_SEL = 0 (AEoC), 200mA
16  Reg_Write_ExtL1,0x49,0x80,SMBB_CHGR,CHG_EN = 1
```

PTE Bench Script to Start Charging – SMBB Version 2.0 (1 of 3)

_SMBB_INIT_2.0.csv

```
1   ;;;; Unblock SEC_ACCESS & TEST_EN
2   ;; UnComment this section of code on PTE or TF bench only as-needed
3   ;Reg_Write_ExtL1,0xD0,0xA5,MISC,SEC_ACCESS
4   ;Reg_Write_ExtL1,0xE0,0x80,MISC,TEST_ACCESS_EN = 1
5   ;DIO_Write_Bit,TEST_EN,0x01,PM_DIO,
6   ;Delay_mS,,10,PM_DIO,
7
8   ;;;; PM8941 2.0
9   ;; SW blind trim some critical SMBB registers
10  Reg_Read_ExtL1, 0xF3,0x20,SMBB_BUCK,IBAT_SNS_Offset_Trim if reads as 0x20, then blind-trim to
    0x40
11  Reg_Write_ExtL1,0xF3,0x40,SMBB_BUCK,IBAT_SNS_Offset_Trim
12  ;; SW trim BMS/IADC Offset
13  Reg_Read_ExtL1,0xF2,0xC0,IADC1_USR,CADC_OFFSET1(MSB)
14  Reg_Read_ExtL1,0xF3,0x00,IADC1_USR,CADC_OFFSET0(LSB)
15  ; If IADC1_USR:CADC_OFFSET1&0 reads 0xC000, then IADC offset is NOT trimmed.
    Use the corresponding scripts to trim IADC offset
16
17  ;;;; Required initialization for charging
```

PTE Bench Script to Start Charging – SMBB Version 2.0 (2 of 3)

_SMBB_INIT_2.0.csv

```
18  Reg_Write_ExtL1,0x42,0x80,SMBB_MISC,BOOT_DONE=1
19  Reg_Write_ExtL1,0x4E,0x01,SMBB_USB_CHGPTH,ENUM_TIMER_STOP = 1
20  Reg_Write_ExtL1,0x44,0x05,SMBB_USB_CHGPTH,IUSB_MAX = 0.5 A; Set according to
    USB charger detection or enumeration result
21  Reg_Write_ExtL1,0x44,0x0A,SMBB_DC_CHGPTH,IDC_MAX = 1.0 A; Set according to DC charger
    characteristic
22  ;; VDD_MAX/SAFE, IBAT_MAX/SAFE: Set according to battery parameters
23  Reg_Write_ExtL1,0x40,0x60,SMBB_CHGR,VDD_MAX = 4.2 V (default)
24  Reg_Write_ExtL1,0x41,0x60,SMBB_CHGR,VDD_SAFE = 4.2 V (default)
25  ;Reg_Write_ExtL1,0x40,0x6F,SMBB_CHGR,VDD_MAX = 4.35 V
26  ;Reg_Write_ExtL1,0x41,0x6F,SMBB_CHGR,VDD_SAFE = 4.35 V
27  Reg_Write_ExtL1,0x44,0x14,SMBB_CHGR,IBAT_MAX = 1 A
28  Reg_Write_ExtL1,0x45,0x14,SMBB_CHGR,IBAT_SAFE = 1 A
29  ;Reg_Write_ExtL1,0x44,0x28,SMBB_CHGR,IBAT_MAX = 2 A
30  ;Reg_Write_ExtL1,0x45,0x28,SMBB_CHGR,IBAT_SAFE = 2 A
31  ;; Other charger feature configurations
32  Reg_Write_ExtL1,0x47,0x12,SMBB_CHGR,VIN_MIN = 4.3 V (CR-0000162267)
33  Reg_Write_ExtL1,0x43,0x00,SMBB_CHGR,VDDMAX_GSM_ADJ disabled
34  Reg_Write_ExtL1,0x5B,0x88,SMBB_CHGR,IEOC_SEL = 1 (Digital EoC Enabled, Default)
```

PTE Bench Script to Start Charging – SMBB Version 2.0 (3 of 3)

_SMBB_INIT_2.0.csv

```
35  Reg_Write_ExtL1,0x74,0x01,SMBB_BUCK,BCK_VBAT_REG_MODE:SEL = VBAT (Analog IR Drop
    Comp Enabled)
36  Reg_Write_ExtL1,0xE6,0x10,SMBB_BUCK,TEST_SMBC_MODES:BUCK_MAX_DUTY = 25 ns (100%
    Duty-Cycle Disabled, Default)
37  ;Reg_Write_ExtL1,0xE5,0x28,SMBB_BAT_IF,BAT_HOT/COLD Override
38  Reg_Write_ExtL1,0x46,0x80,LDO8,Force-On LDO8 (CR-0000162239)
39
40  ;; Enable Charging
41  Reg_Write_ExtL1,0x49,0x80,SMBB_CHGR,CHG_EN = 1
```

Questions?

https://support.cdmatech.com