PDN Capacitor Optimization Guidelines

Qualcomm Technologies, Inc.

80-VT310-15 Rev. A

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Revision History

Revision	Date	Description
A	March 2013	Initial release

Contents

Overview

Introduction

- PDN capacitor optimization involves simulation of the **Baseband IC + PCB** PDN impedance over a wide frequency range while optimizing the number/value/size of PDN capacitors.
  - The old process used multiple identical caps for PDN.
  - The new process, in contrast, identifies a set of capacitors of different values and sizes for a PCB.

- PCB, capacitors, and Baseband IC are part of this new process. PMIC is not included.

Note: PCB power routing should follow the guidelines as described in the appropriate Baseband IC design guidelines document. PDN capacitor optimization cannot fix a PCB design with poor capacitor placement and routing.

Requirements

Tools

- ADS (Advanced Design System) or equivalent circuit simulator (system analysis)
- PowerSI, SentinelPSI or equivalent EM tool (creation of s-parameter model for PCB)

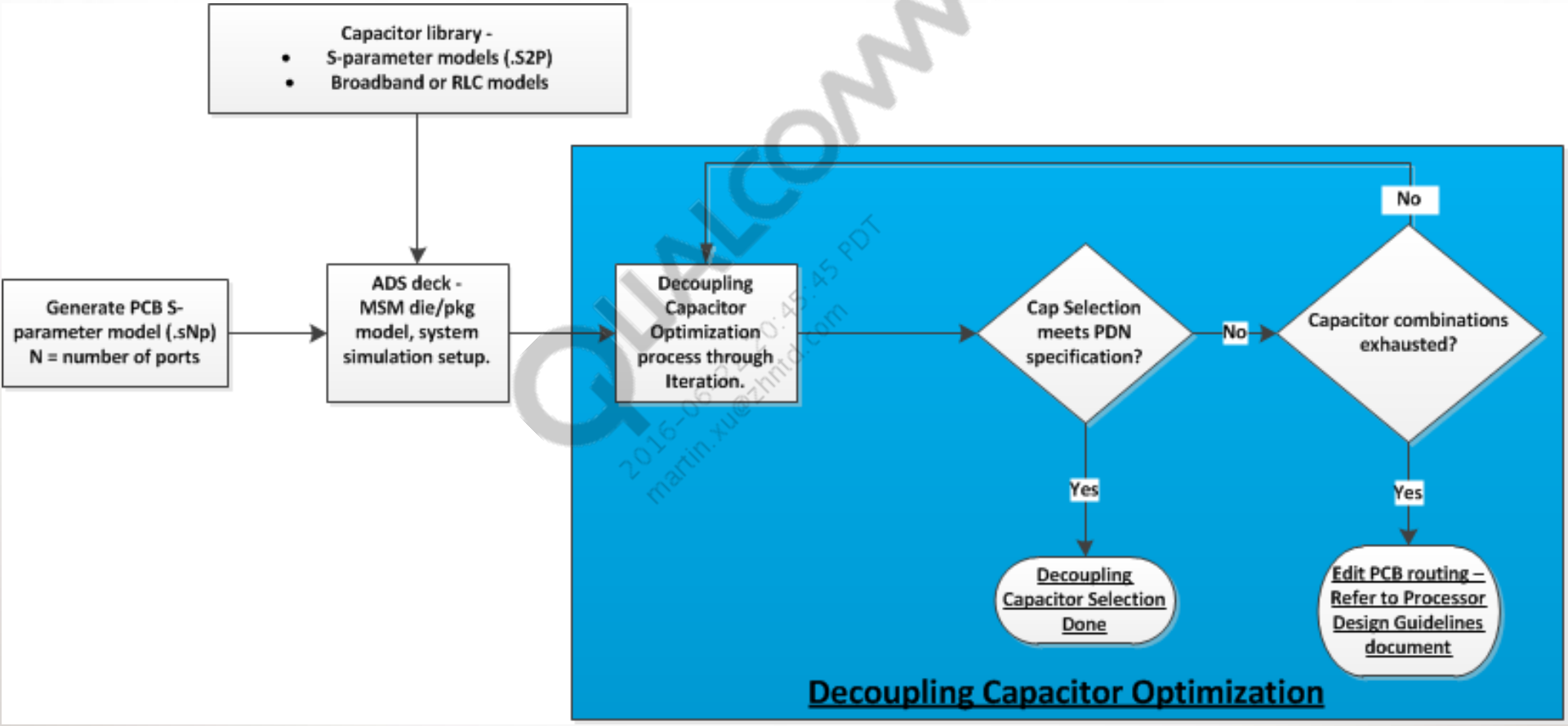
Files and Documents from Qualcomm®

- Baseband IC Device Specifications, Section 3-3 (80-Nxxxx-1, where Nxxxx is the baseband IC family number)
- ADS Template for PDN Capacitor Optimization (HS11-VT310-15HW)
- S-parameter model of Baseband IC (HS11-Nxxxx-10HW, where Nxxxx is the baseband IC family number)
- Training: Power Delivery Network Design (80-VT310-13)
- Baseband IC Breakout Study (DP25-Nxxxx-m, where Nxxxx is the baseband IC family number, m is a random number)

Other files required

- Capacitor models (.s2p). Talk to capacitor vendors for these models.
- S-parameter model of customer PCB (.sNp), where N is the number of ports.
  - The PDN capacitor optimization requires the PCB power routing and placement of capacitors to be completed before you start the optimization process.
  - Important Note: The PCB loop inductance must meet the inductance requirements listed in the “PCB+Baseband IC” table Section 3-3 of the Device Specifications in order to achieve optimum results from the PDN capacitor optimization process.

PDN Capacitor Optimization – Overview



PDN Capacitor Optimization – Detailed

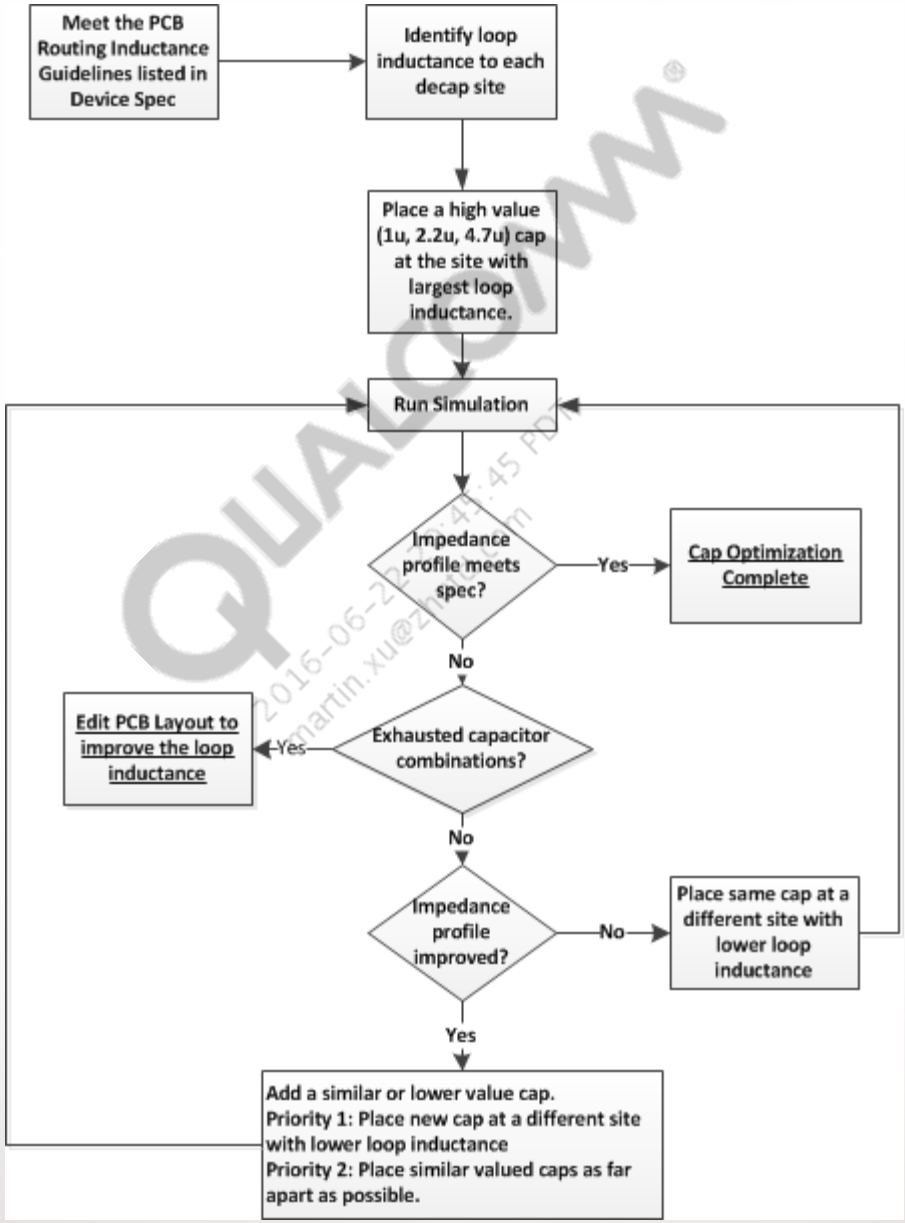
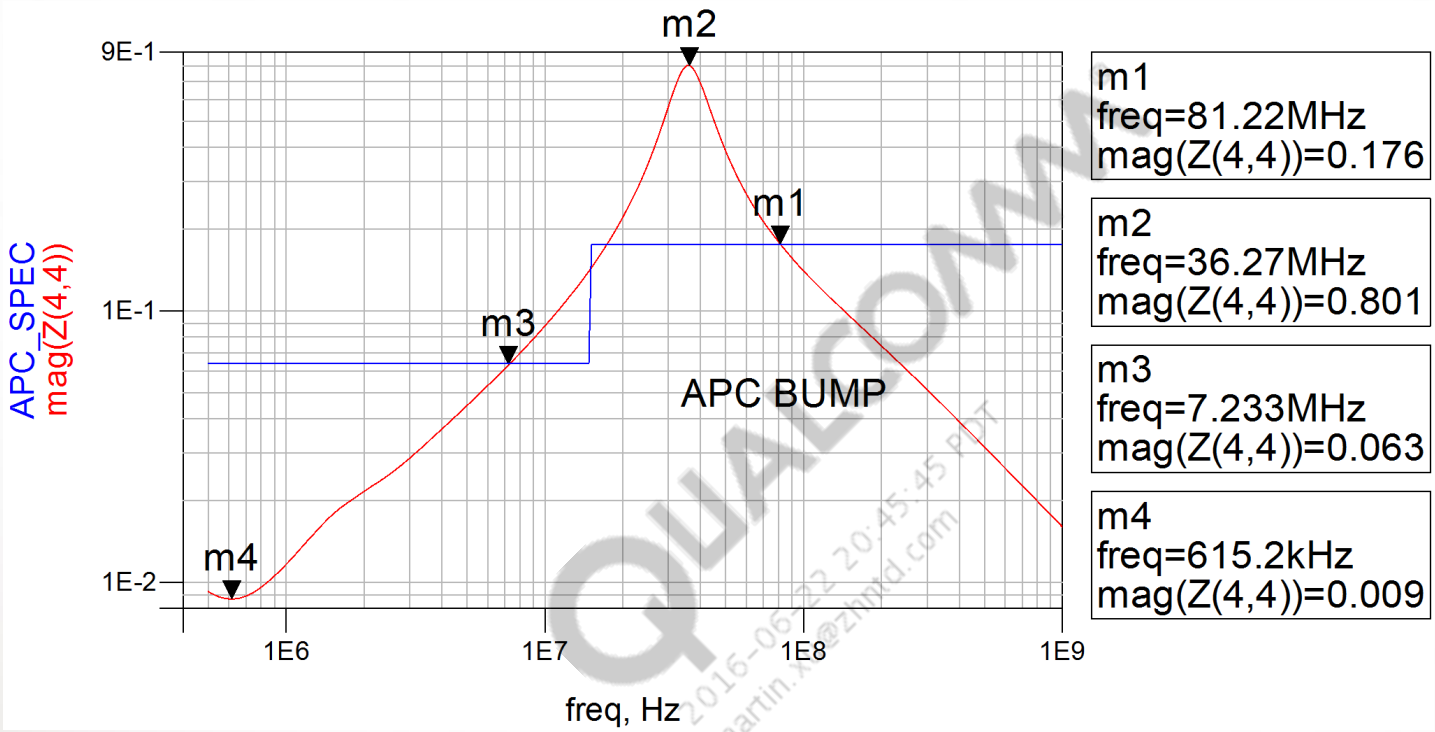


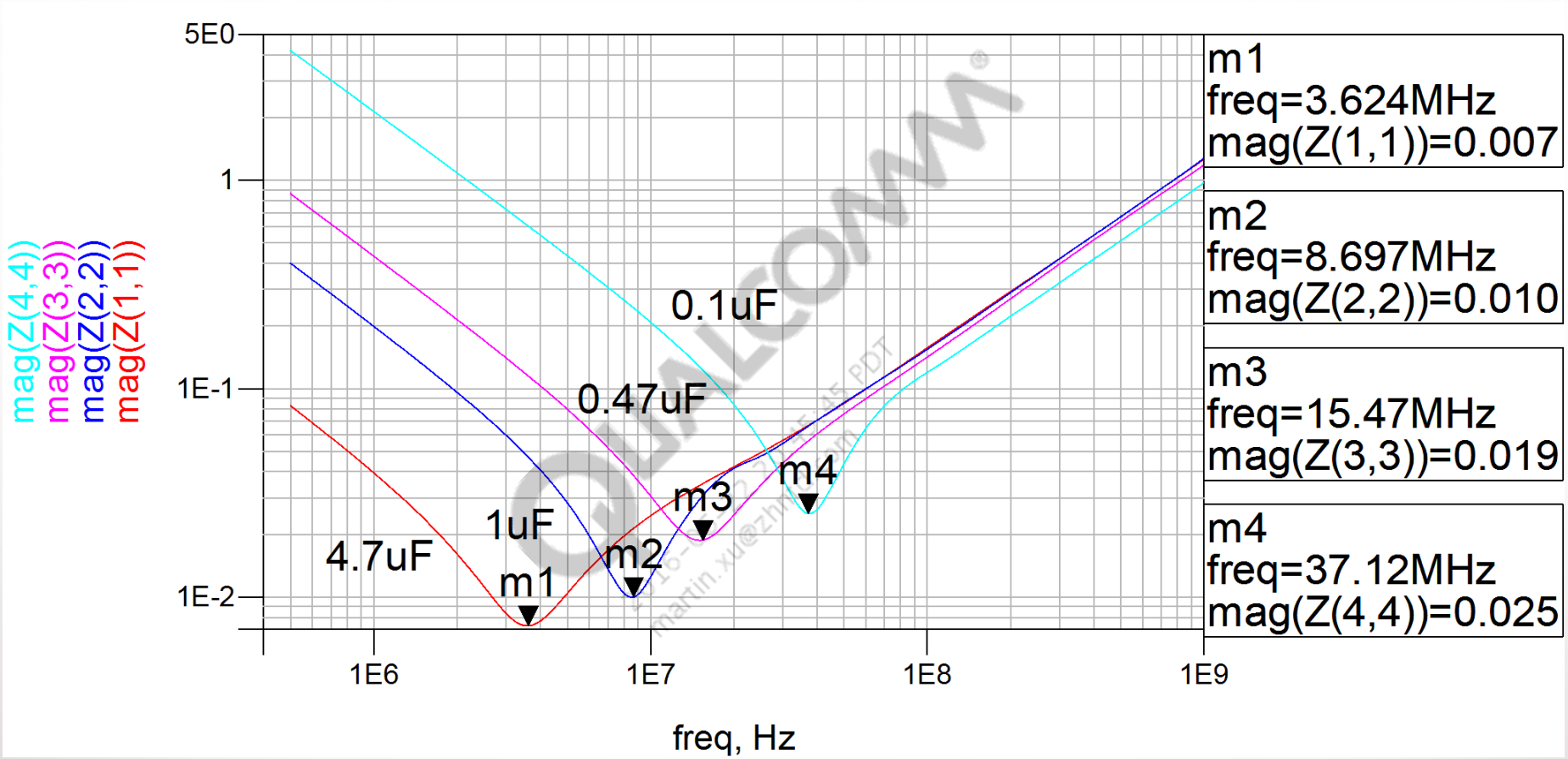
Illustration – How Capacitors Affect Impedance Profile

System Impedance Profile with No Decoupling Capacitors



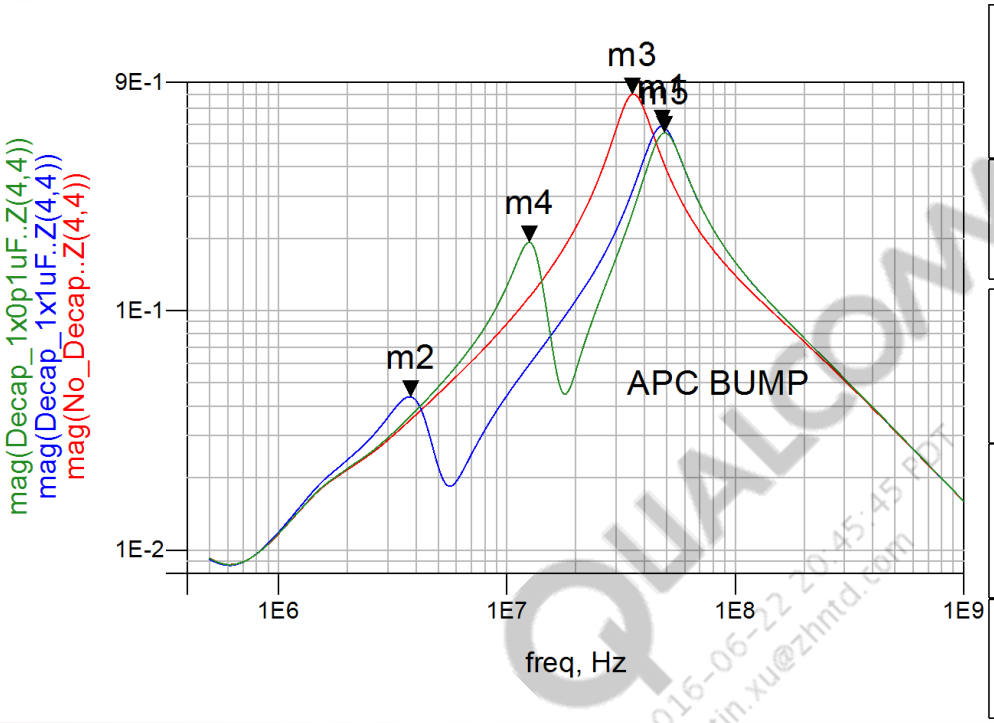
- The system consists of the Baseband IC, PCB routing and PMIC output cap with no decoupling caps.
- The blue line shows the PDN specification. The red line shows the system impedance profile. The red line needs to be below the blue line at all frequencies.
- The simulation is valid from 1 MHz to 500 MHz.

Standalone Impedance Profile of Capacitors – Example



- The standalone impedance profiles of 4.7 µF (red), 1 µF (blue), 0.47 µF (pink) and 0.1 µF (green) cap are shown in the figure above.
- When these capacitors are part of a system, the response of the capacitors will depend on their placement, their routing, and the system parameters.

System Impedance Profile with Decoupling Capacitors - Example



m1
freq=47.82MHz
mag(Decap_1x1uF..Z(4,4))=0.589
Peak

m2
freq=3.795MHz
mag(Decap_1x1uF..Z(4,4))=0.044

m3
freq=35.44MHz
mag(No_Decap..Z(4,4))=0.801
Peak

m4
freq=12.57MHz
mag(Decap_1x0p1uF..Z(4,4))=0.193
Peak

m5
freq=48.93MHz
mag(Decap_1x0p1uF..Z(4,4))=0.553

Scenario 1 (blue) – Add one 1 µF cap on the PCB in addition to the PMIC output cap.

- The impedance profile improves from m2 at 4 MHz to m1 at 48 MHz. This is dependent on cap placement and PCB routing.
- Total number of caps = 2 (1 PMIC output cap + 1 µF)

Scenario 2 (green) – Add one 0.1 µF cap on the PCB in addition to the PMIC output cap.

- The impedance profile improves from m4 at 13 MHz to m5 at 49 MHz. This is dependent on cap placement and PCB routing.
- Total number of caps = 2 (1 PMIC output cap + 0.1 µF)

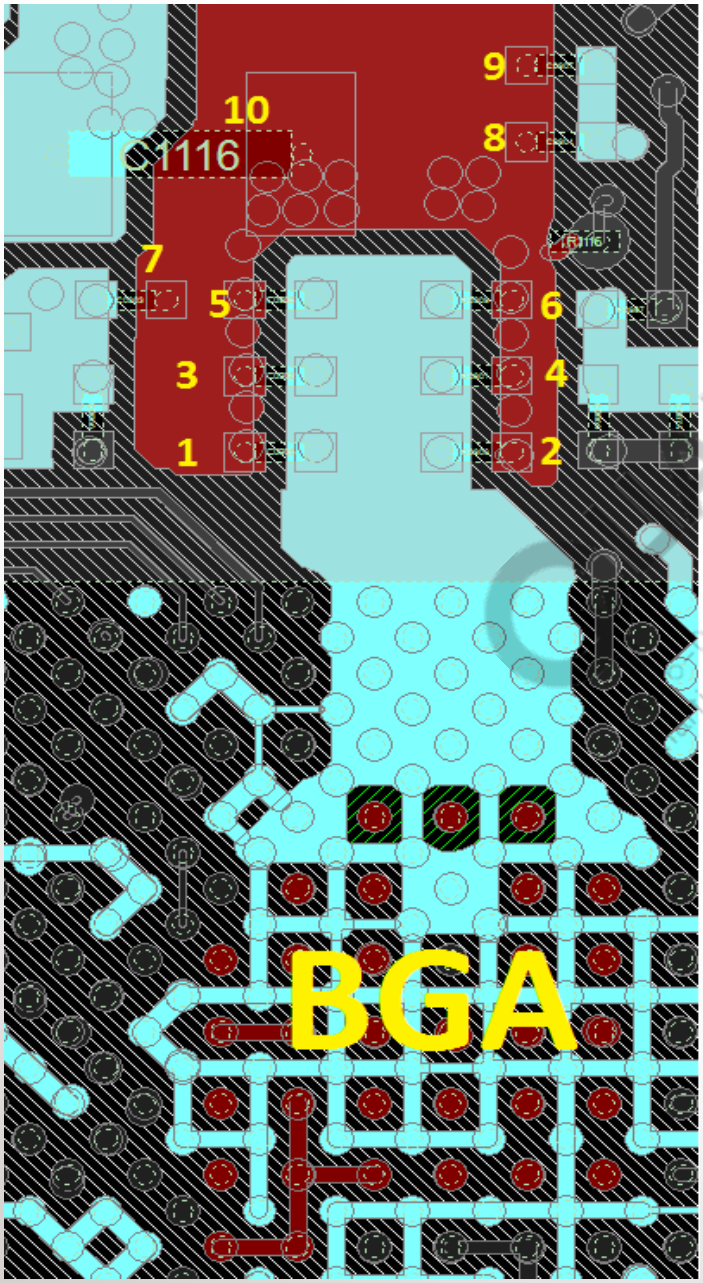
Conclusions

- Different capacitors affect impedance profiles differently.
  - The smaller the capacitor values, the higher the frequencies they are effective at
  - The larger the capacitor values, the lower the frequencies they are effective at
- Multiple capacitors of different values and sizes are required to bring down the system impedance profile and meet the PDN specification.

PDN Capacitor Optimization – Example

The example optimizes capacitors on a single power rail. The same methodology can be followed for designs with multiple power rails.

PCB S-Parameter Model Extraction

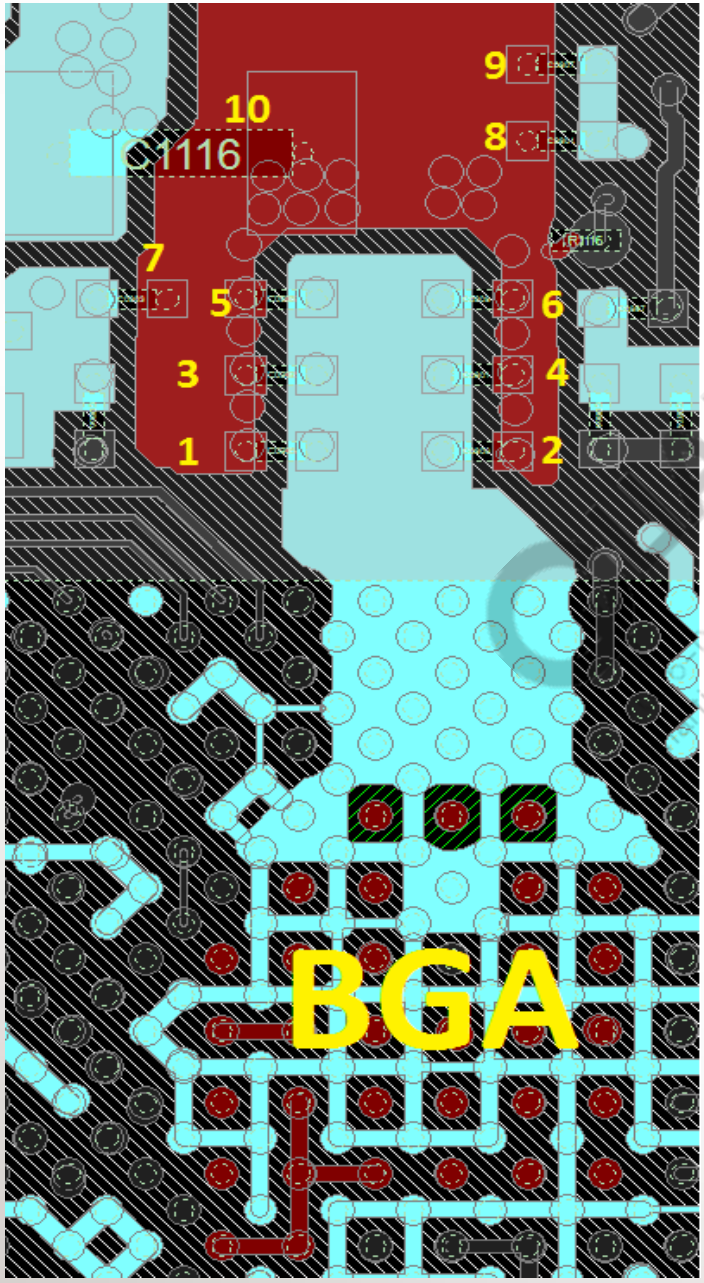


Label each capacitor site as shown in the figure.

Port assignment:

- All Baseband IC BGAs of a given power rail are lumped as a single port.
- Each capacitor is assigned a unique port (use capacitor label as port number).
- Total number of ports, N = 1 (Baseband IC) + number of caps (including PMIC output cap).
- Do not assign any models to capacitors during PCB extraction.
- Output should be .sNp file, where N is the total number of ports.

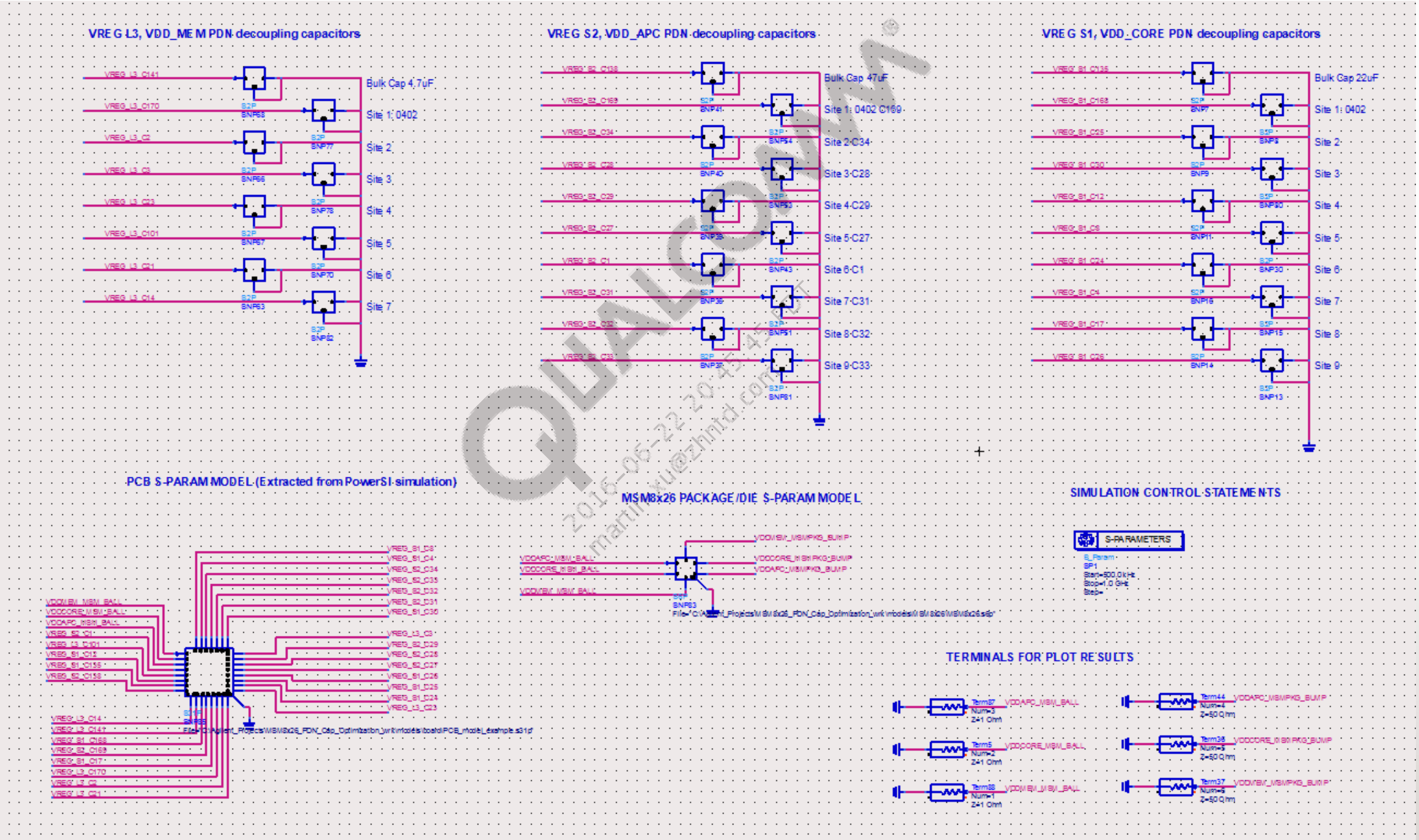
Capacitor Loop Inductance Estimation



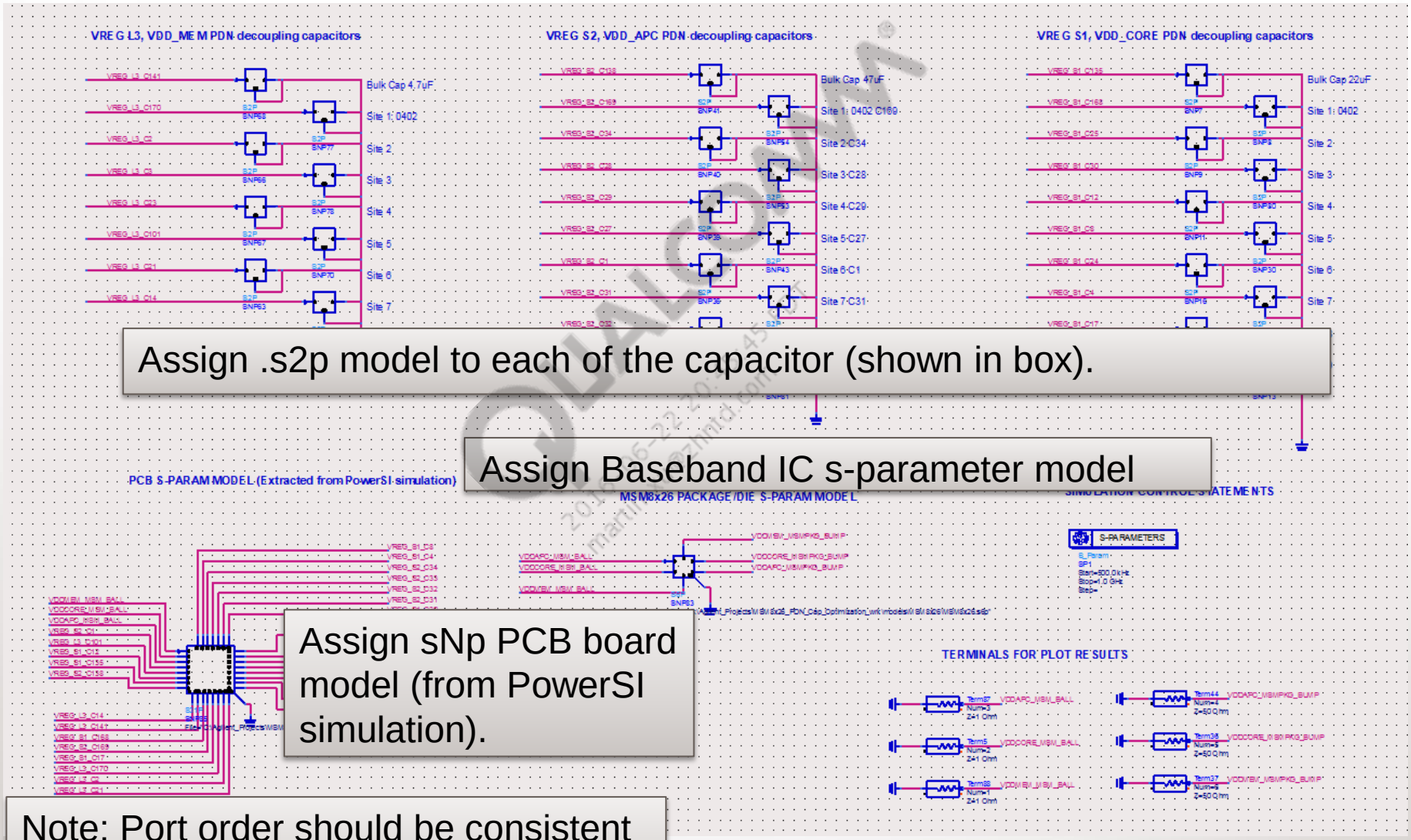
Loop inductance estimation:

- Estimate from layout – larger the Power-Gnd loop area (Baseband IC to capacitor), larger the loop inductance.
- Estimate by simulation – calculate the loop inductance from the Baseband IC BGA to each capacitor site.
- Note the order of loop inductance.
  - For example, in this layout, the order of loop inductance in each decap site is 9 > 8 > 7 > 6 = 5 > 4 = 3 > 2 = 1.
- PMIC output cap placed at site 10.

ADS PDN Capacitor Optimization Deck

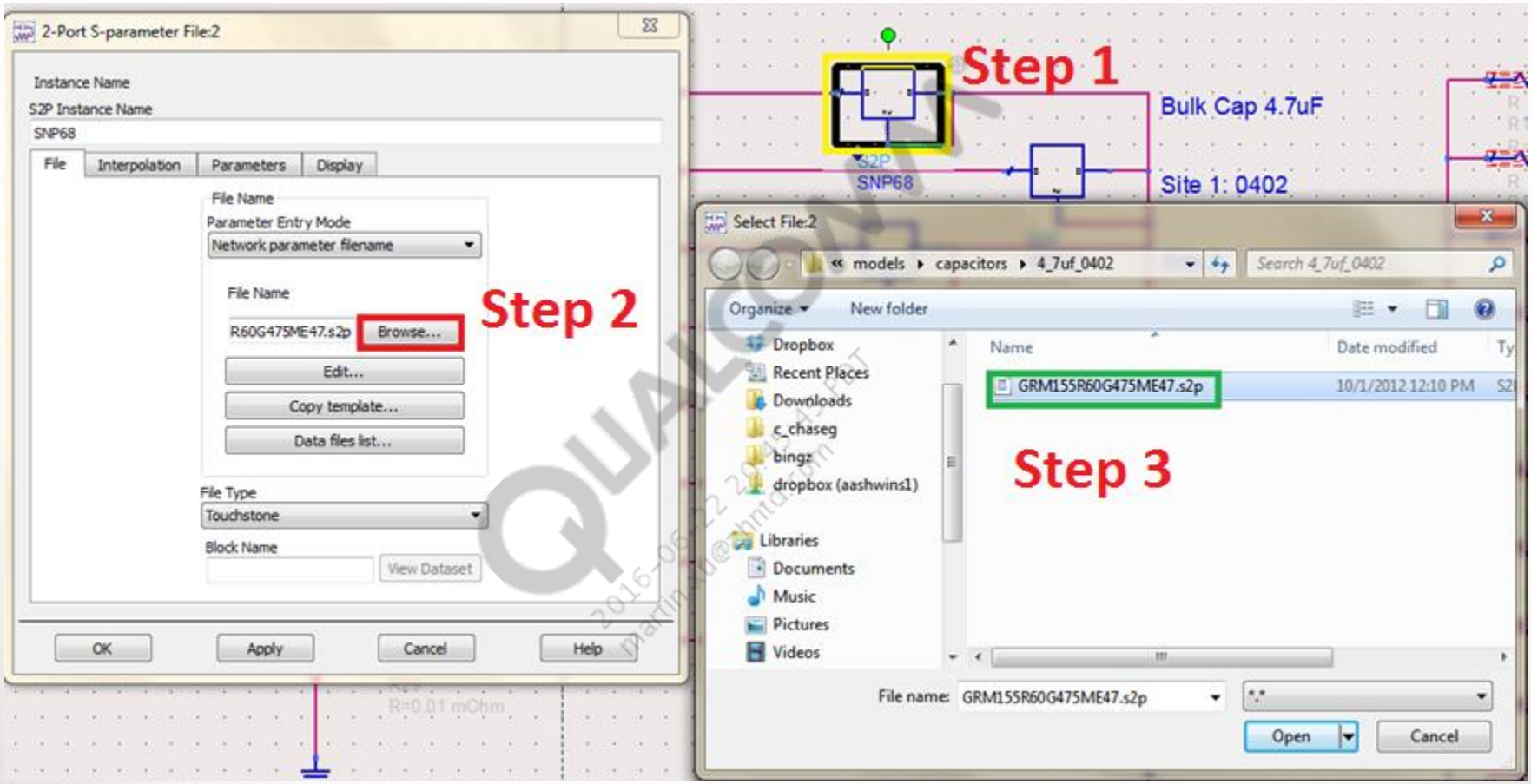


ADS PDN Capacitor Optimization Deck



Note: Port order should be consistent with PCB extraction.

S-parameter Model Assignment



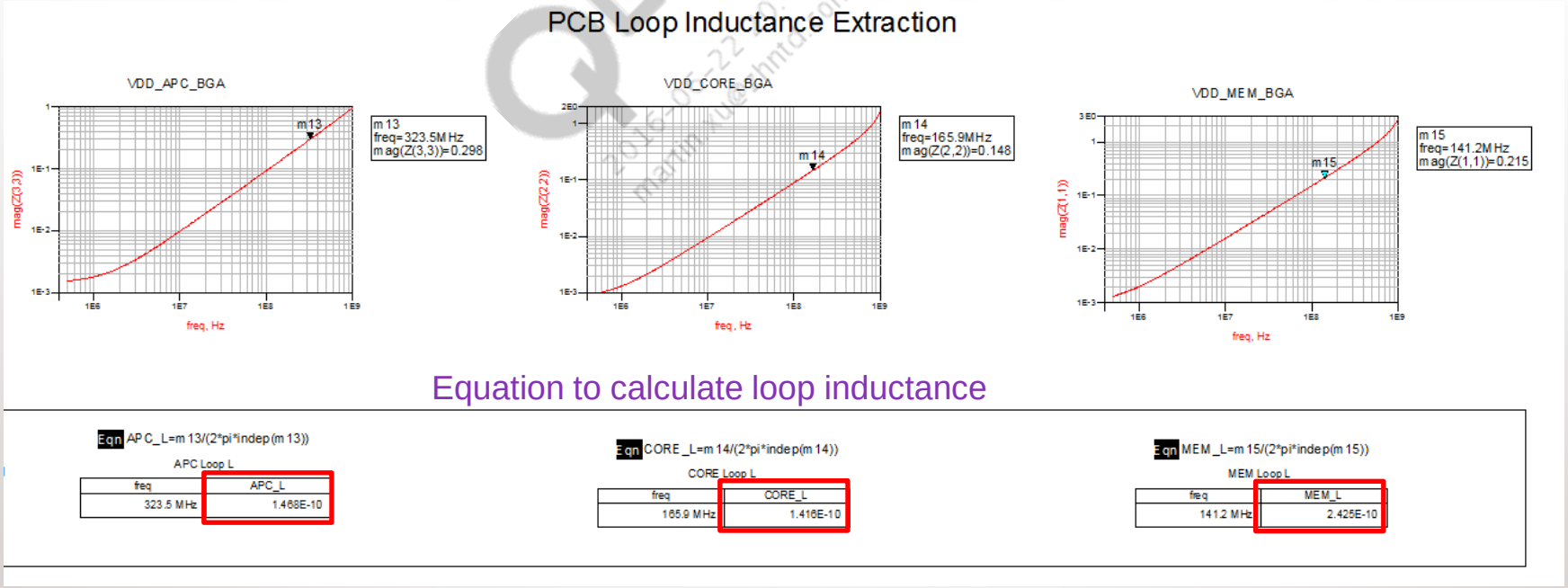
Complete the following steps to assign sNp model:

1. Double-click the component box you want to assign.
2. Click **Browse…**
3. Browse to the corresponding folder and select the model.

PCB Routing Inductance Measurement

Complete the following steps to measure PCB routing inductance:

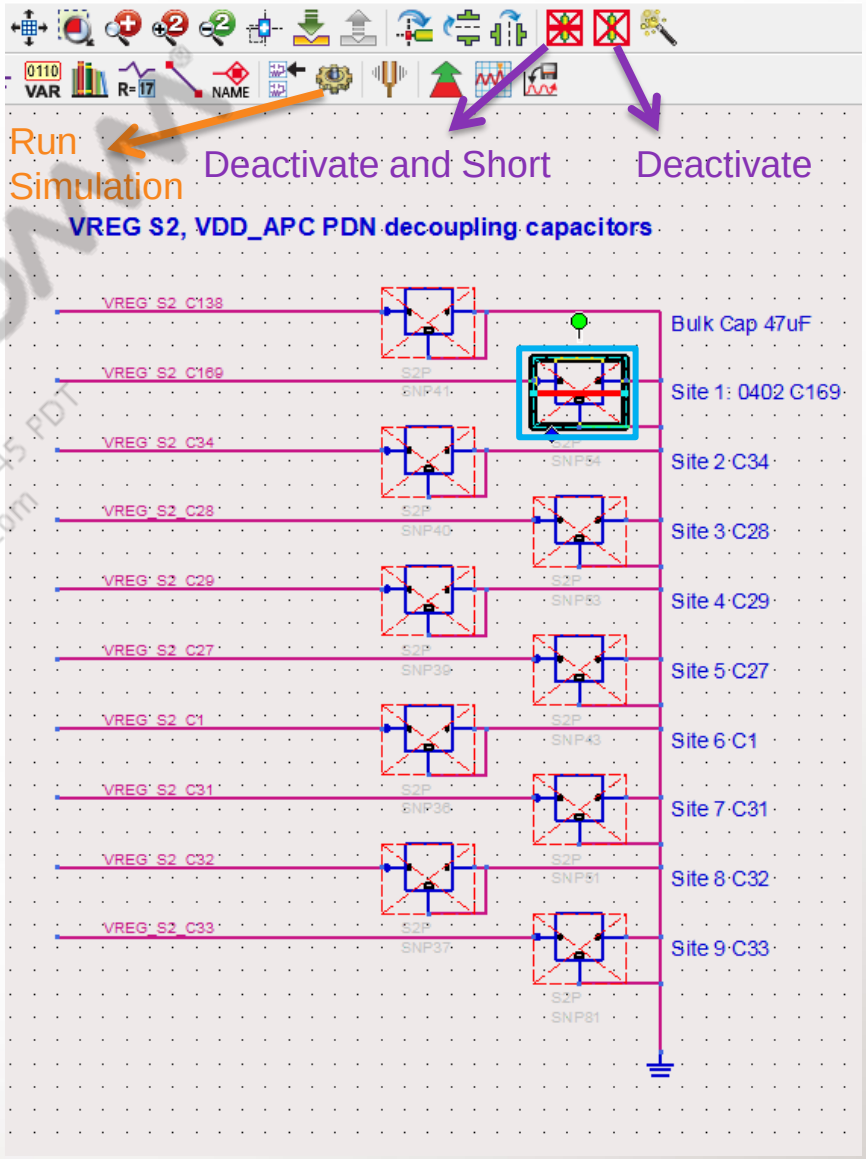
1. Load PCB s-parameter file.
2. Deactivate the Baseband IC s-parameter model.
3. Deactivate and Short all PDN capacitors (including both decoupling capacitors and PMIC bulk capacitors).
4. Run simulation.
5. Measure the impedance at BGAs. PCB routing inductance is calculated by the equation L = Z/(2*pi*f).

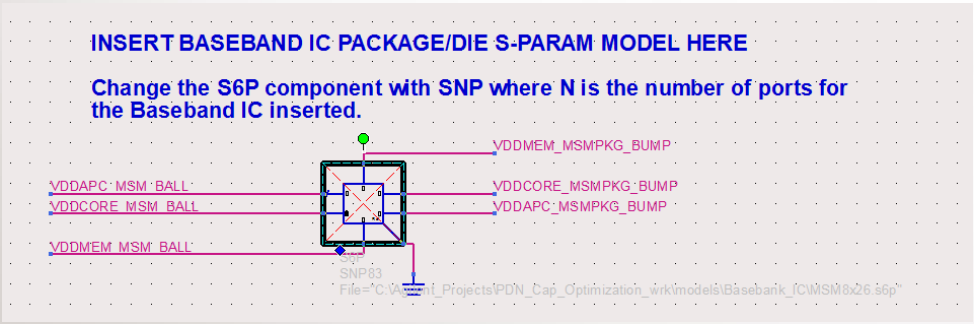


Loop Inductance Calculation to Each Capacitor Site (1 of 2)

Complete the following step to calculate a site:

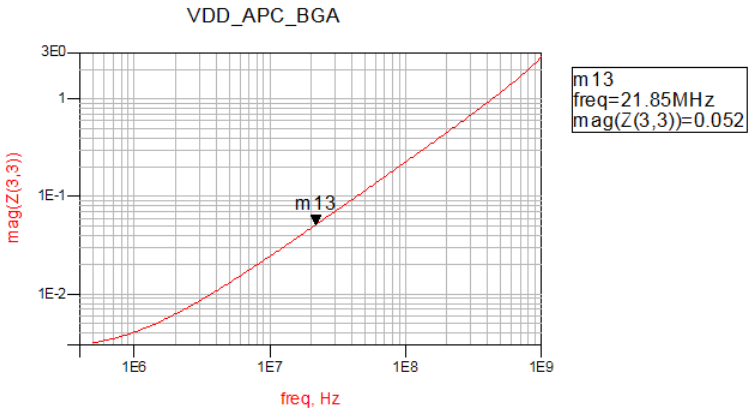
1. Load PCB s-parameter file.
2. Deactivate the Baseband IC s-parameter model.
3. Deactivate all the capacitors connected to a power rail.
4. Deactivate and Short the capacitor (blue box) for the site. This will calculate the loop inductance for that site.
5. Run simulation.





Loop Inductance Calculation to Each Capacitor Site (2 of 2)

6. Measure the impedance at BGAs. Loop inductance is calculated by the equation L = Z/(2*pi*f).
7. Repeat steps 2 through 6 for all the caps.
8. Arrange the sites in decreasing order of impedance. This will give you the loop inductance to the sites starting from the highest to the lowest.



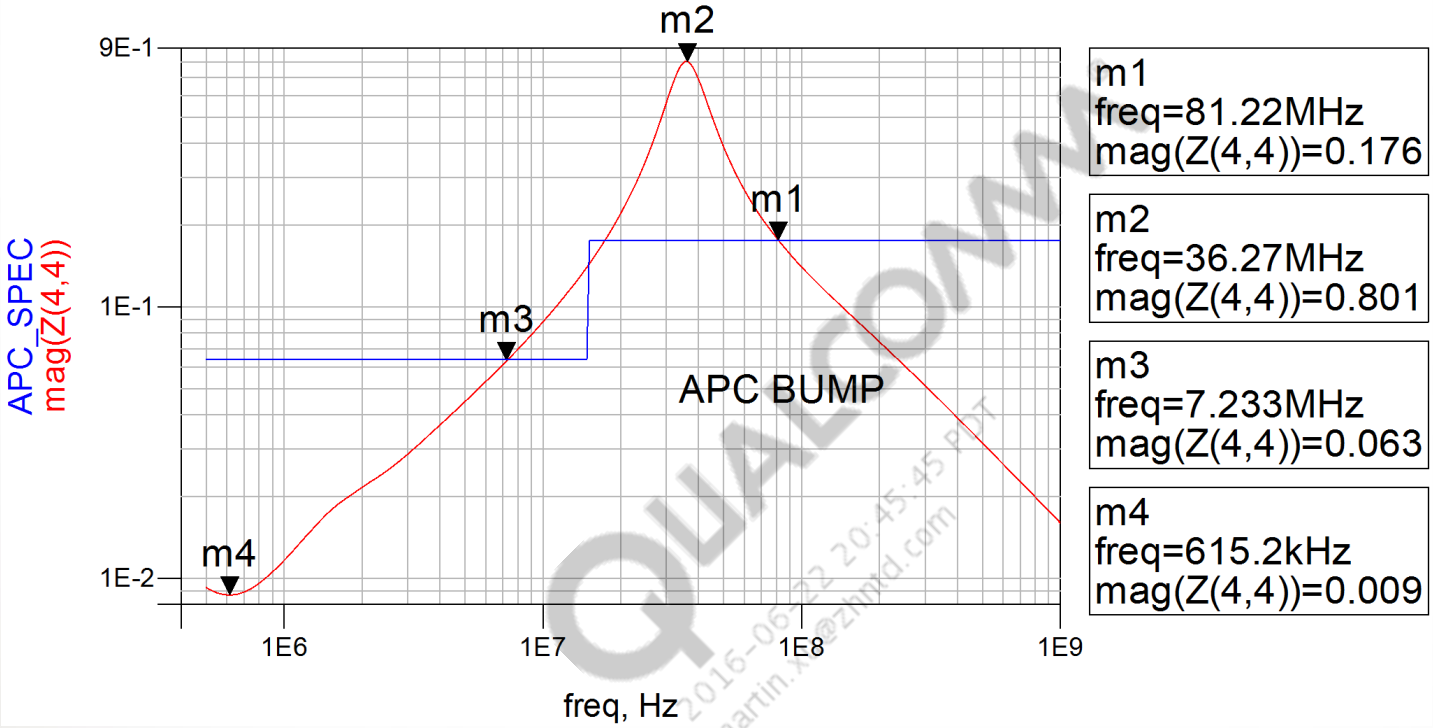
Equation to calculate loop inductance

Eqn APC_L=m13/(2*pi*indep(m13))

APC Loop L

freq	APC_L
21.85 MHz	3.761E-10

Impedance Curve with No Decoupling Capacitor

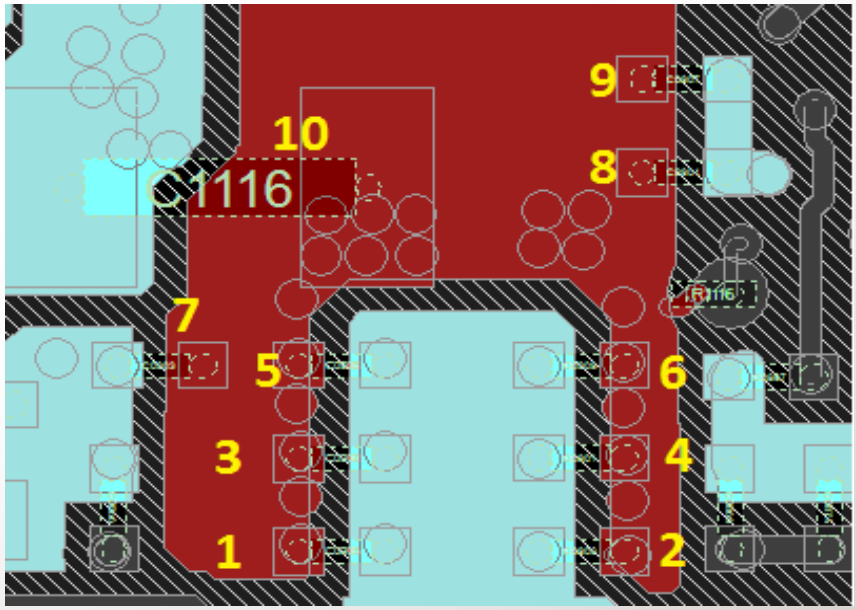


- 47 µF PMIC output cap is effective at low frequencies (up to 600 kHz).
- Impedance is dominated by loop inductance from 615.2 kHz (m4) and goes above the specification at 7.233 MHz (m3).
- It reaches its peak at 36.27 MHz (m2) then falls due to package and die parasitic.

Iteration Summary – PDN Capacitor Optimization

	Cap Site (Cap unit in µF)									
Iteration#	1	2	3	4	5	6	7	8	9	10
1									1	47
2									0.1	47
3									0.47	47
4						0.1			0.47	47
5			0.01			0.1			0.47	47
6			0.022			0.1			0.47	47
7		0.0047	0.022			0.1			0.47	47
8		0.0047	0.022		0.22	0.1			0.47	47
9	0.0068	0.0047	0.022		0.22	0.1			0.47	47
10	0.0068	0.0047	0.022		0.22	0.033			0.47	47
11	0.0068	0.0047			0.22	0.033			0.47	47
12	0.01	0.0047			0.22	0.033			0.47	47
13	0.0047	0.0047	0.01		0.22	0.033			0.47	47
14	0.0047	0.0047	0.01	0.033	0.22	0.47				47
15	0.0047	0.0047	0.01	0.033	0.22				0.47	47

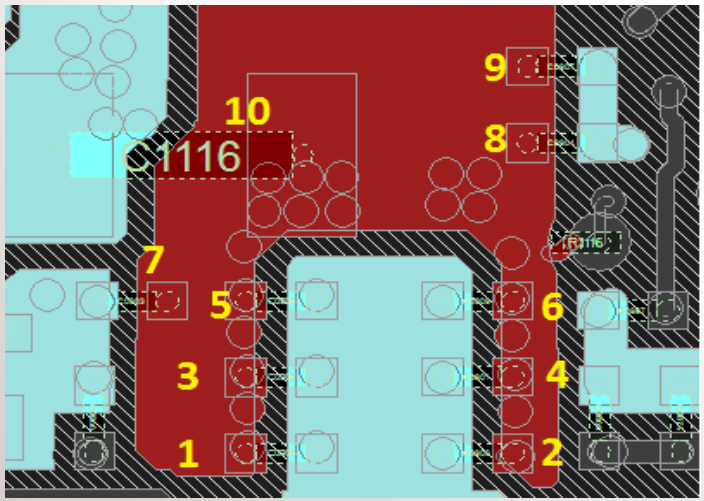
- Design needs several iterations to obtain the optimized set of capacitors.
- The iterations listed are only an example to elaborate the concept of decap optimization process.
- Each layout may have multiple combinations of optimized decaps.
- Actual decap selection should be analyzed on a case by case basis.
- It might be constrained by your capacitor inventory.

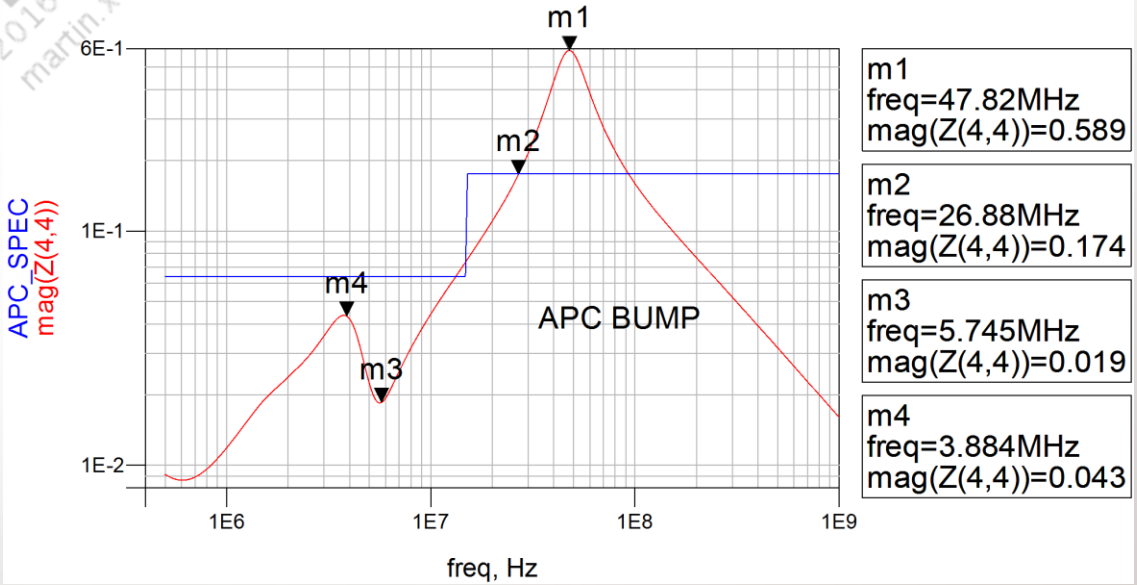


Iteration – 1

	Cap Site (Cap unit in µF)									
Iteration#	1	2	3	4	5	6	7	8	9	10
1									1	47

- Impedance profile improves.
- 1 µF at site 9 becomes effective from 3.8 MHz (m4).
- Impedance peak brought down from 800 mΩ (no decoupling cap) to 589 mΩ (m1).

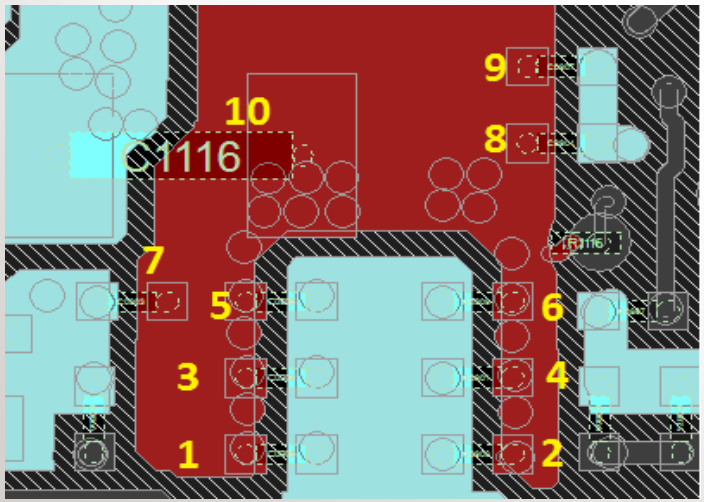


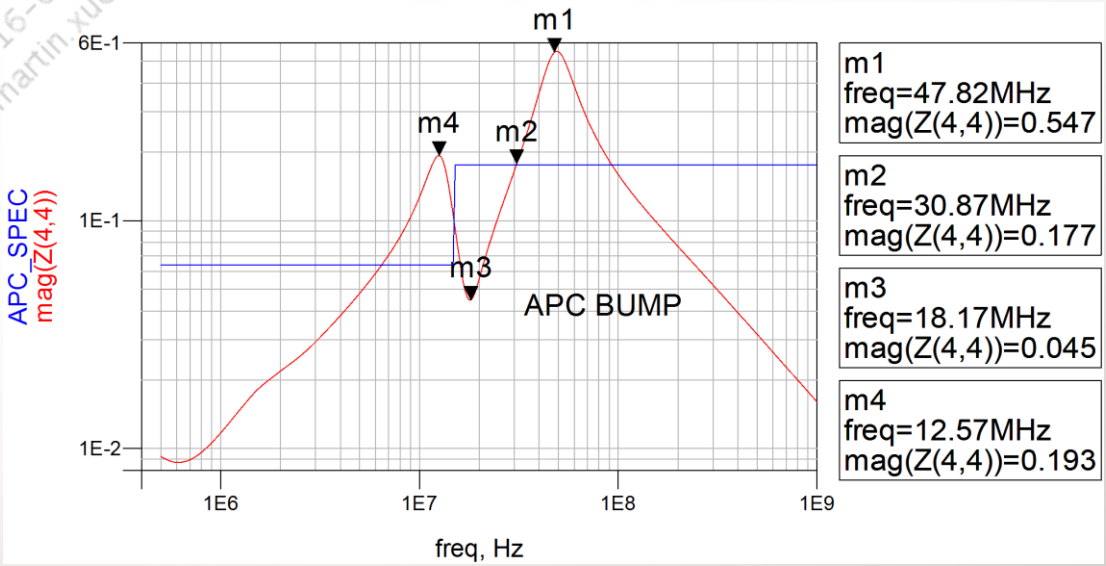


Iteration – 2

	Cap Site (Cap unit in µF)									
Iteration#	1	2	3	4	5	6	7	8	9	10
1									1	47
2									0.1	47

- 0.1 µF at site 9 becomes effective from 12.57 MHz (m4).
- PDN specification not met at low frequencies.
- Need to increase the cap value.

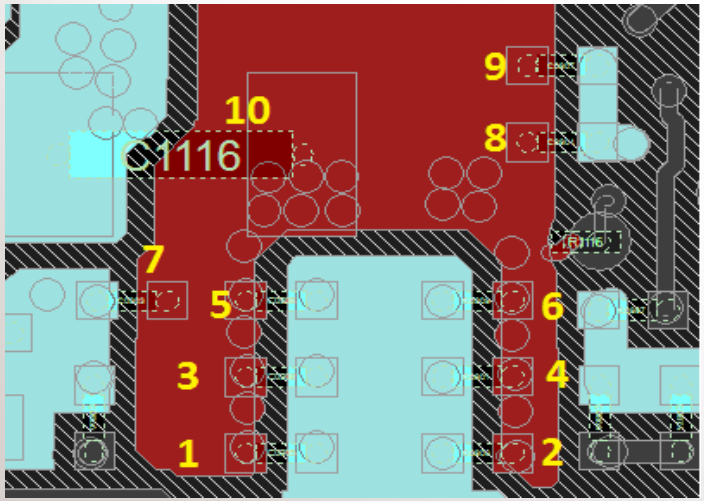


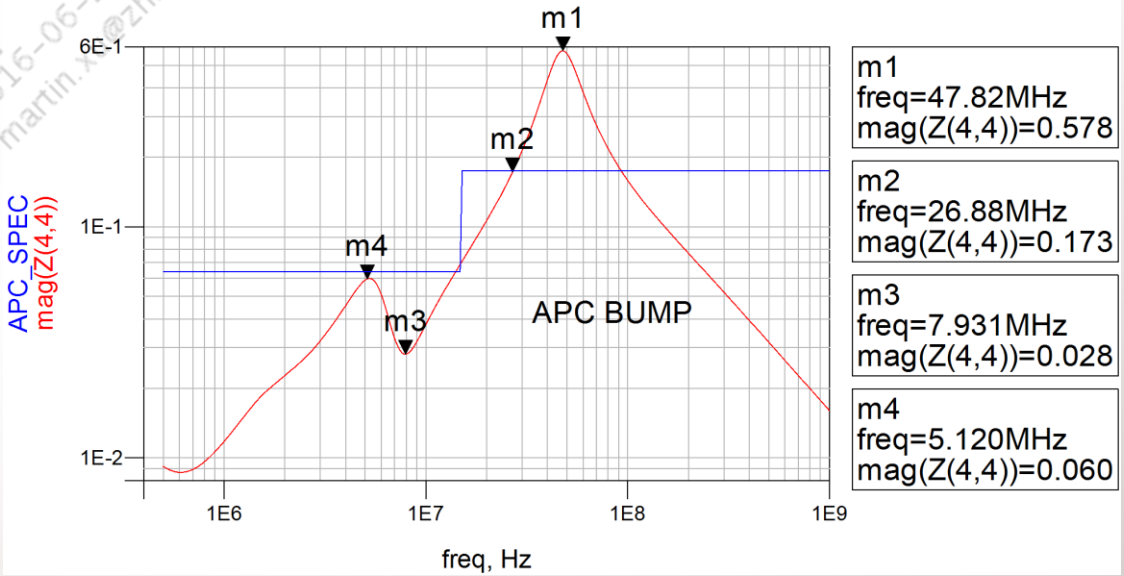


Iteration – 3

	Cap Site (Cap unit in µF)									
Iteration#	1	2	3	4	5	6	7	8	9	10
1									1	47
2									0.1	47
3									0.47	47

- 0.47 µF at site 9 becomes effective from 5.2 MHz (m4).
- PDN spec met from few KHz to ~30 MHz.
- Need to bring down the other peak (m1).
- Summary – iterations 1 to 3:
  - A 0.47 µF or greater cap is required to meet PDN spec between 1 MHz and 10 MHz.

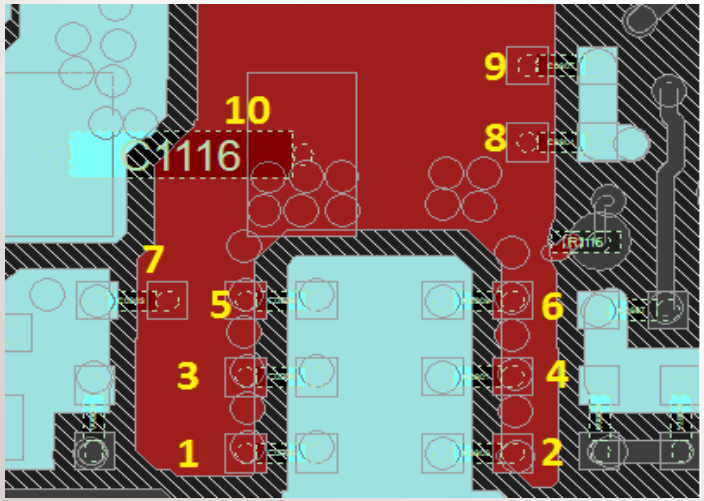


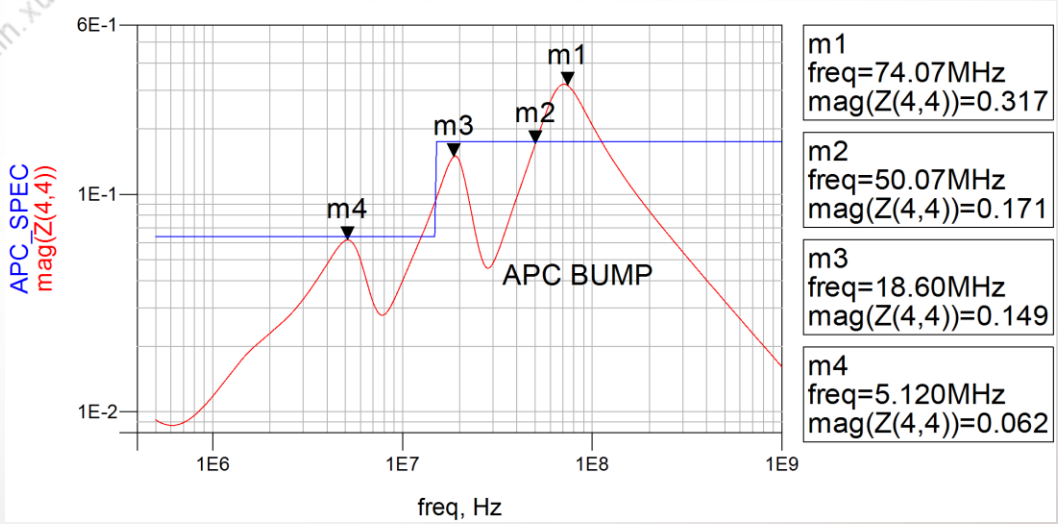


Iteration – 4

	Cap Site (Cap unit in µF)									
Iteration#	1	2	3	4	5	6	7	8	9	10
1									1	47
2									0.1	47
3									0.47	47
4						0.1			0.47	47

- 0.1 µF at site 6 becomes effective from 19.47 MHz (m3).
- Impedance peak brought down to 317 mΩ (m1) from 800 mΩ (zero decoupling capacitors).

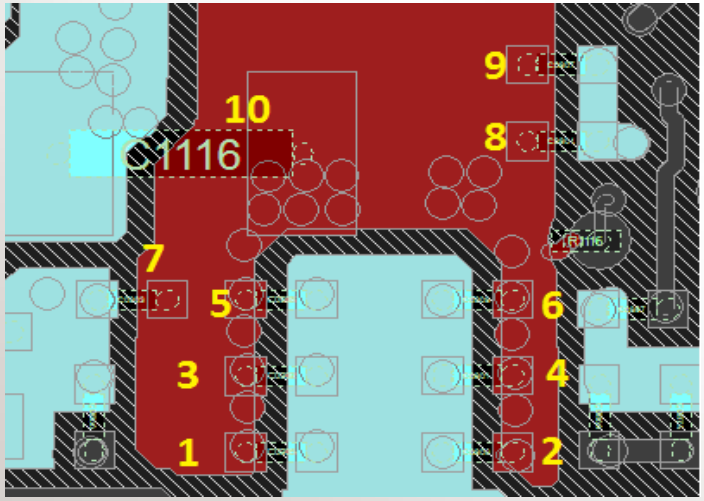


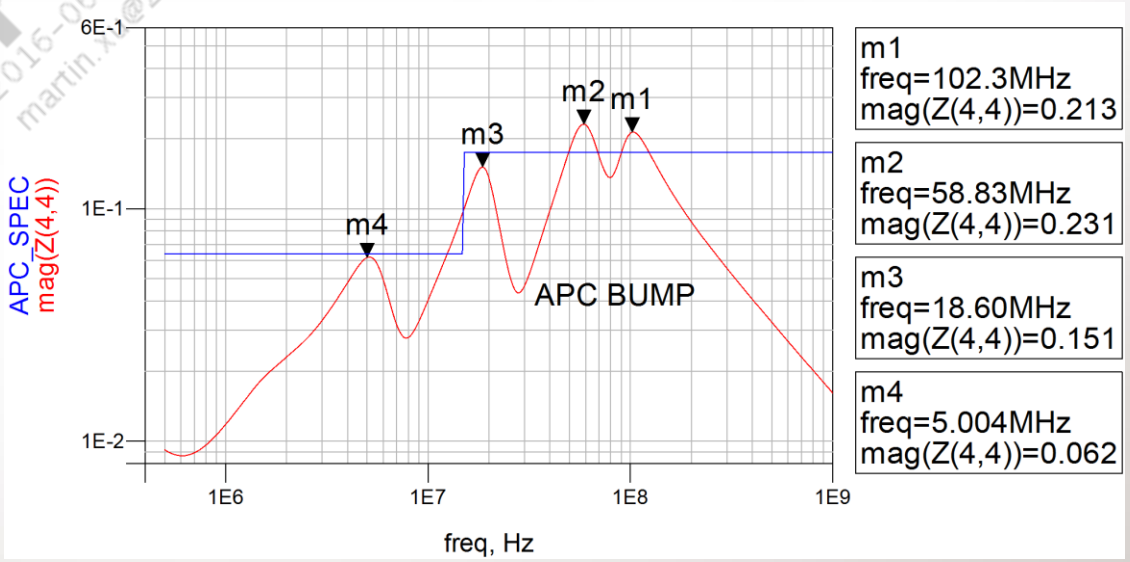


Iteration – 5

	Cap Site (Cap unit in µF)									
Iteration#	1	2	3	4	5	6	7	8	9	10
1									1	47
2									0.1	47
3									0.47	47
4						0.1			0.47	47
5			0.01			0.1			0.47	47

- 0.01 µF at site 3 becomes effective from 58.8 MHz (m2).
- Need to place a slightly larger decap which become effective lower than 58.8 MHz.

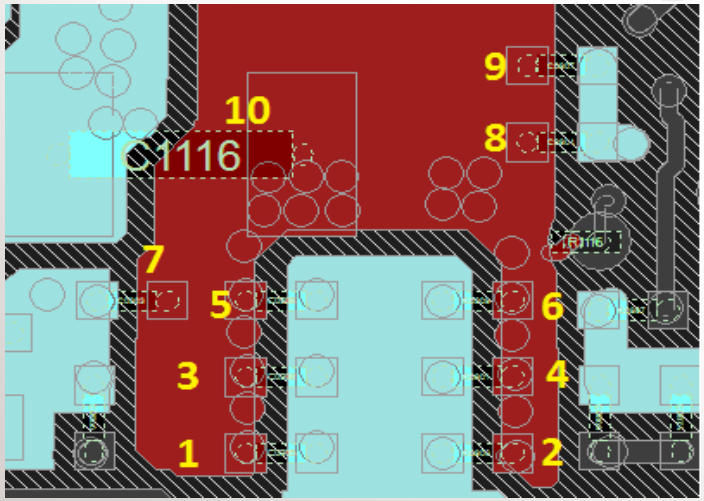


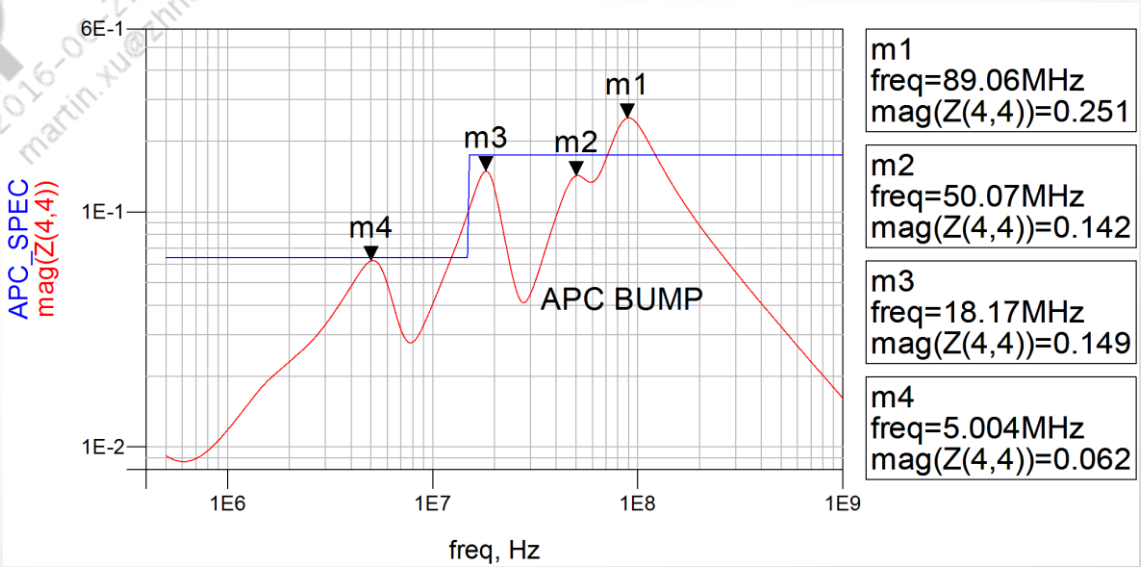


Iteration – 6

	Cap Site (Cap unit in µF)									
Iteration#	1	2	3	4	5	6	7	8	9	10
1									1	47
2									0.1	47
3									0.47	47
4						0.1			0.47	47
5			0.01			0.1			0.47	47
6			0.022			0.1			0.47	47

- 0.022 µF at site 3 become effective from 50 MHz (m2).
- The side effect is that it is out of specification between 10–20 MHz (iteration – 8).
- Need to find a cap with effective frequency of around 70 MHz to turn the curve downwards there.

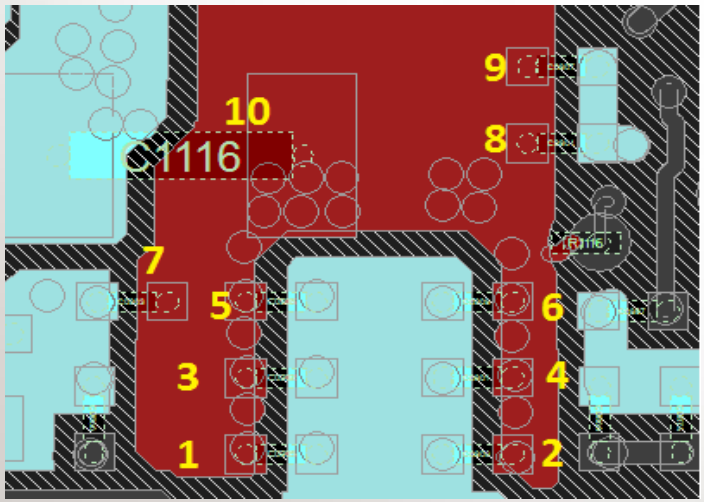


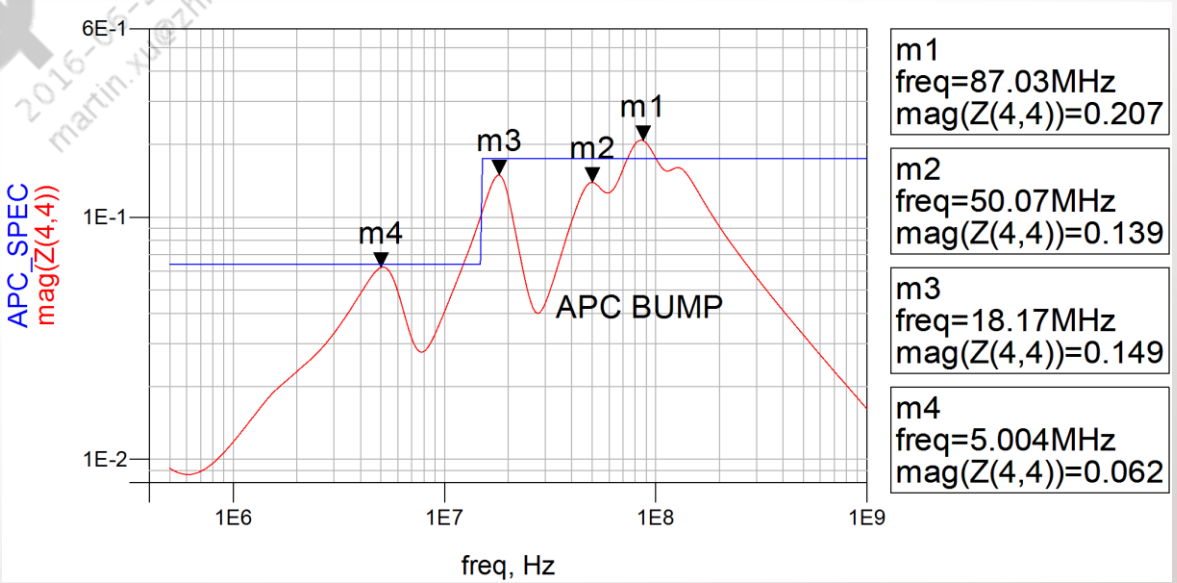


Iteration – 7

	Cap Site (Cap unit in µF)									
Iteration#	1	2	3	4	5	6	7	8	9	10
1									1	47
2									0.1	47
3									0.47	47
4						0.1			0.47	47
5			0.01			0.1			0.47	47
6			0.022			0.1			0.47	47
7		0.0047	0.022			0.1			0.47	47

- 0.0047 µF at site 2 becomes effective from 100 MHz.
- Still need to find a larger cap to suppress the peak of m1 (iteration – 9).

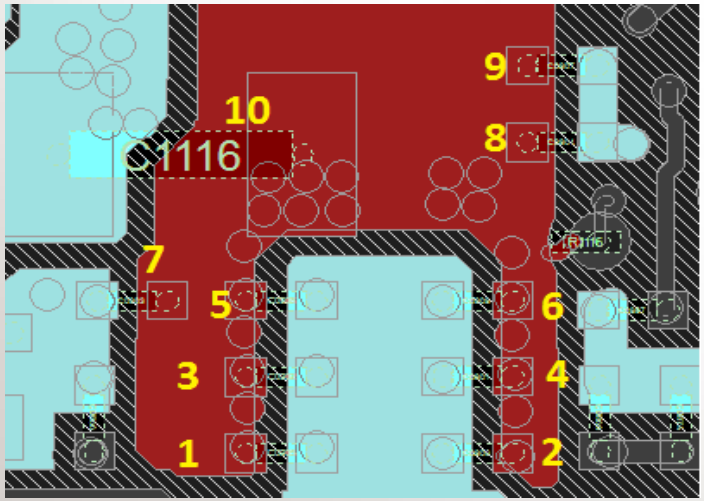


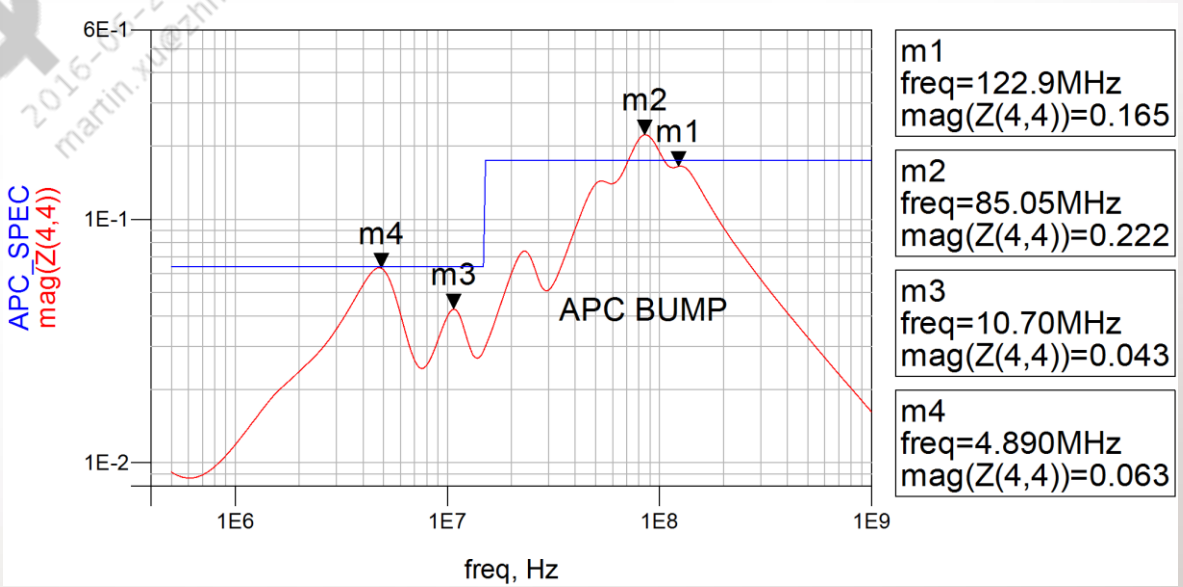


Iteration – 8

	Cap Site (Cap unit in µF)									
Iteration#	1	2	3	4	5	6	7	8	9	10
1									1	47
2									0.1	47
3									0.47	47
4						0.1			0.47	47
5			0.01			0.1			0.47	47
6			0.022			0.1			0.47	47
7		0.0047	0.022			0.1			0.47	47
8		0.0047	0.022		0.22	0.1			0.47	47

- 0.22 µF at site 5 becomes effective from 10 MHz (m3)
- It brings down the waveform below the specification.

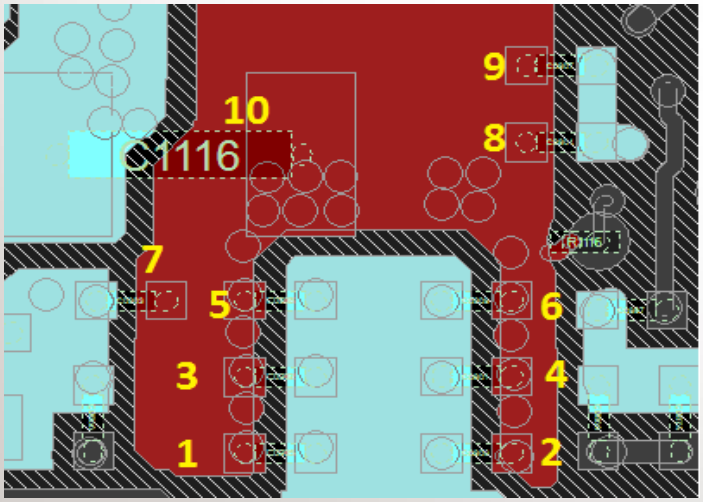


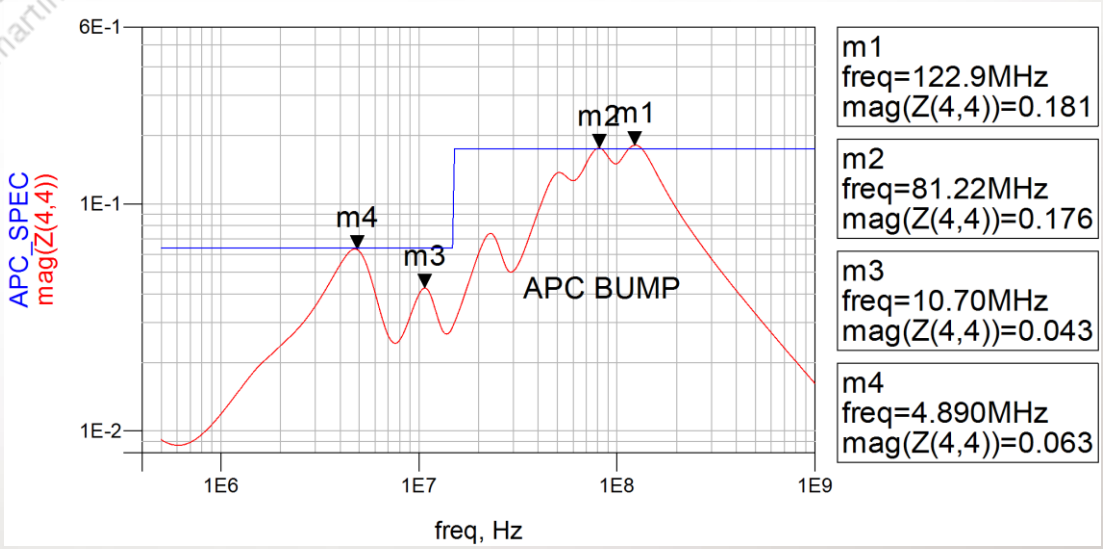


Iteration – 9

	Cap Site (Cap unit in µF)									
Iteration#	1	2	3	4	5	6	7	8	9	10
1									1	47
2									0.1	47
3									0.47	47
4						0.1			0.47	47
5			0.01			0.1			0.47	47
6			0.022			0.1			0.47	47
7		0.0047	0.022			0.1			0.47	47
8		0.0047	0.022		0.22	0.1			0.47	47
9	0.0068	0.0047	0.022		0.22	0.1			0.47	47

- 0.0068 µF at site 1 becomes effective from 81.22 MHz (m1).
- The combined effect of 0.0068 µF at site 1 and 0.0047 µF at site 2 bring down the peak at m1 and m2 significantly.
- Need some fine tuning to further suppress the peaks m1 and m2.
- 0.1 µF cap can be replaced by a smaller value as there is a pretty high margin at the third peak (around 25 MHz).
- The more a cap is moved to a lower loop inductance site, the more effective it will be for high frequency peak reduction.

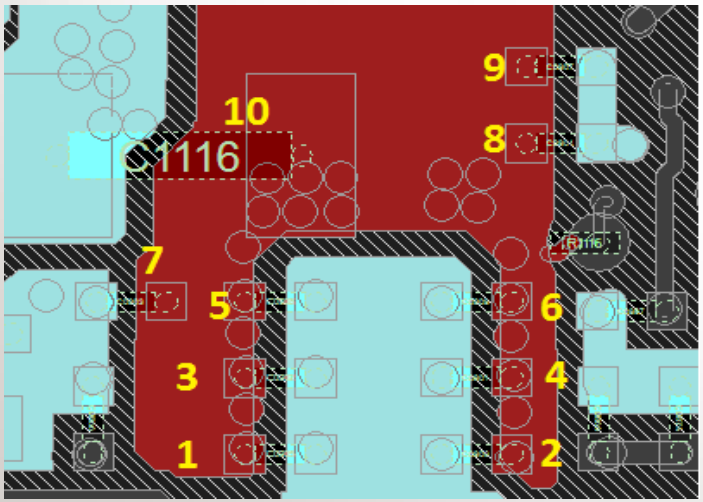


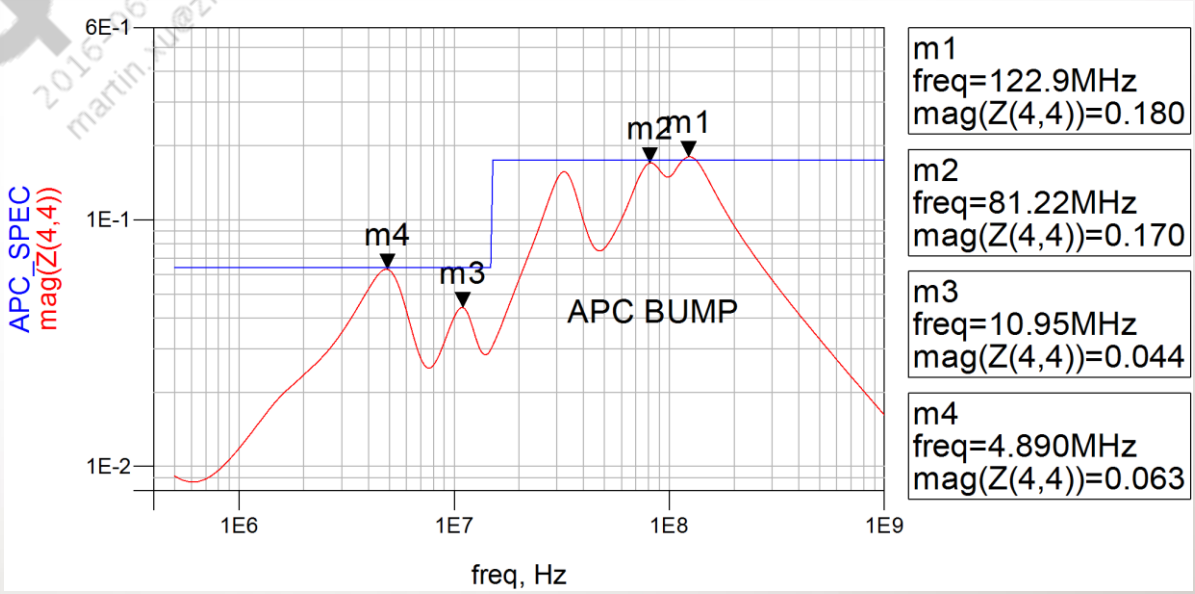


Iteration – 10

	Cap Site (Cap unit in µF)									
Iteration#	1	2	3	4	5	6	7	8	9	10
1									1	47
2									0.1	47
3									0.47	47
4						0.1			0.47	47
5			0.01			0.1			0.47	47
6			0.022			0.1			0.47	47
7		0.0047	0.022			0.1			0.47	47
8		0.0047	0.022		0.22	0.1			0.47	47
9	0.0068	0.0047	0.022		0.22	0.1			0.47	47
10	0.0068	0.0047	0.022		0.22	0.033			0.47	47

- Replace 0.1 µF with 0.033 µF at site 6.
- It becomes effective from 32 MHz.
- It may be possible to remove 0.022 µF, since there is still some margin at 32 MHz and its value is close to 0.033 µF.

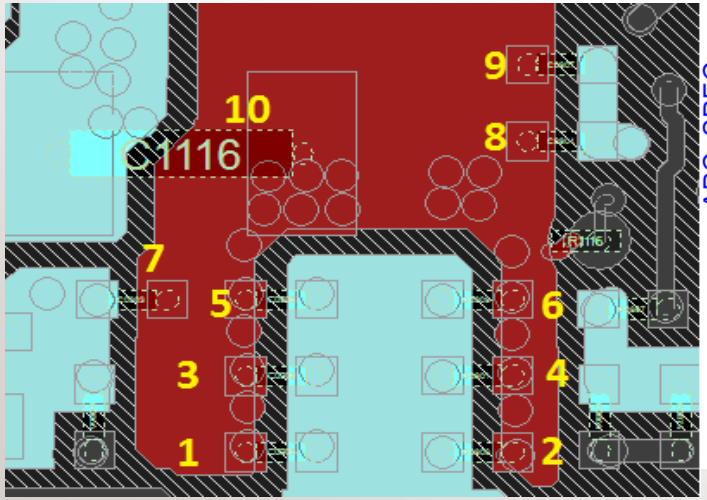


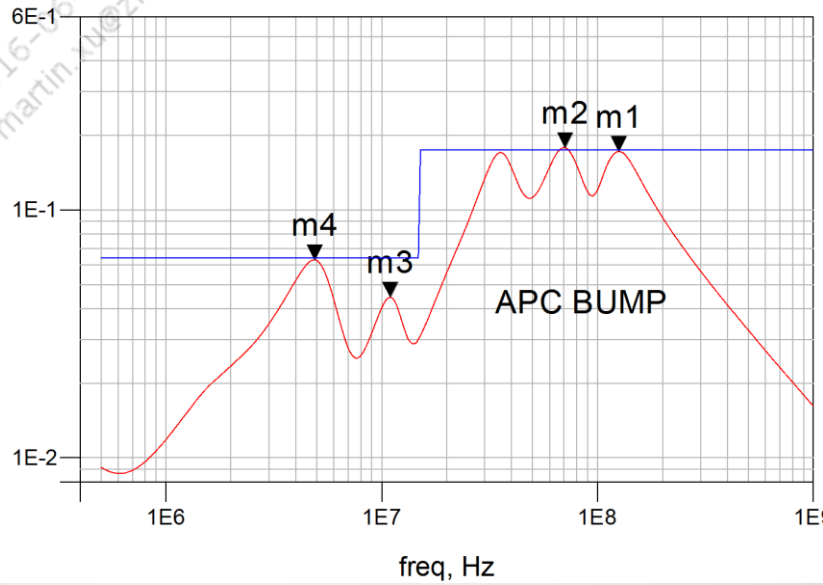


Iteration – 11

	Cap Site (Cap unit in µF)									
Iteration#	1	2	3	4	5	6	7	8	9	10
1									1	47
2									0.1	47
3									0.47	47
4						0.1			0.47	47
5			0.01			0.1			0.47	47
6			0.022			0.1			0.47	47
7		0.0047	0.022			0.1			0.47	47
8		0.0047	0.022		0.22	0.1			0.47	47
9	0.0068	0.0047	0.022		0.22	0.1			0.47	47
10	0.0068	0.0047	0.022		0.22	0.033			0.47	47
11	0.0068	0.0047			0.22	0.033			0.47	47

- Removed 0.022 µF and the third peak is still below the specification.
- Need to increase the value of 0.0068 µF to reduce peak at m2.





m1
freq=125.8MHz
mag(Z(4,4))=0.172

m2
freq=70.74MHz
mag(Z(4,4))=0.178

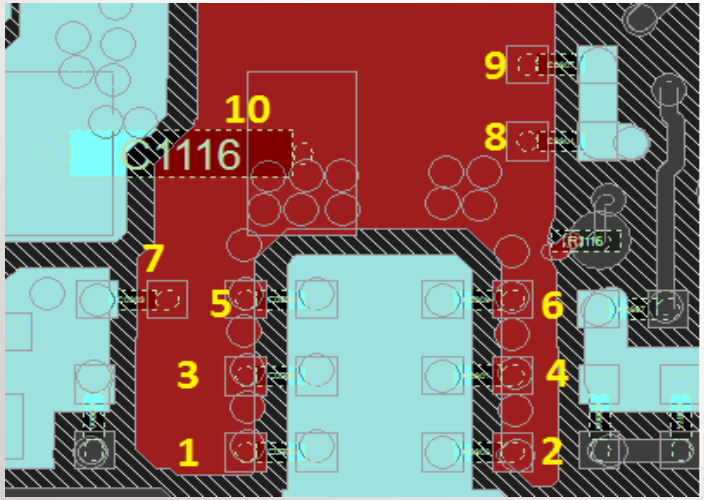
m3
freq=10.95MHz
mag(Z(4,4))=0.044

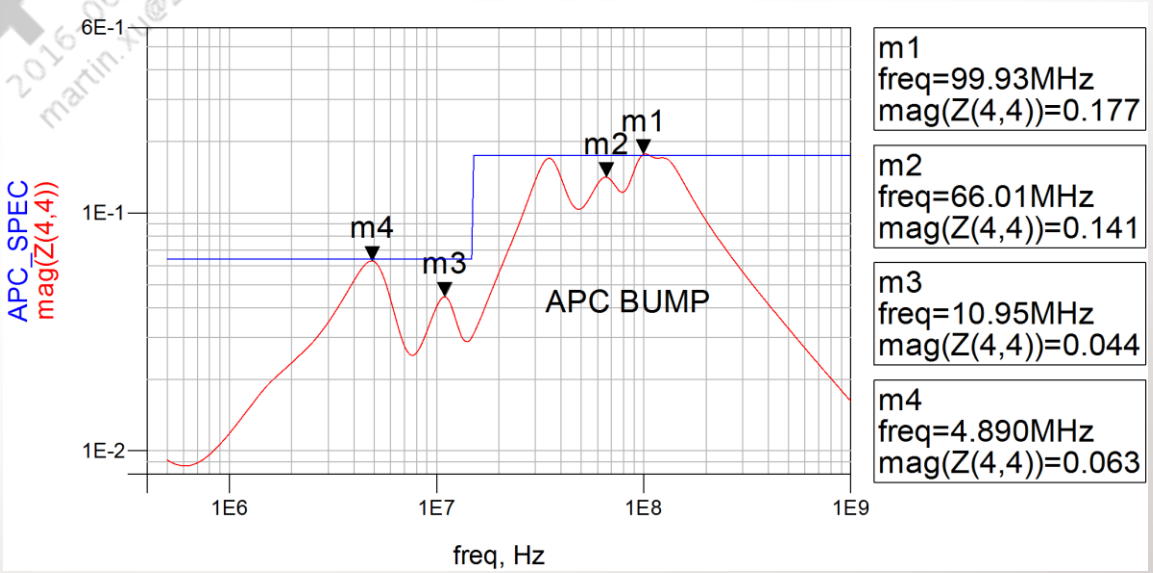
m4
freq=4.890MHz
mag(Z(4,4))=0.063

Iteration – 12

	Cap Site (Cap unit in µF)									
Iteration#	1	2	3	4	5	6	7	8	9	10
1									1	47
2									0.1	47
3									0.47	47
4						0.1			0.47	47
5			0.01			0.1			0.47	47
6			0.022			0.1			0.47	47
7		0.0047	0.022			0.1			0.47	47
8		0.0047	0.022		0.22	0.1			0.47	47
9	0.0068	0.0047	0.022		0.22	0.1			0.47	47
10	0.0068	0.0047	0.022		0.22	0.033			0.47	47
11	0.0068	0.0047			0.22	0.033			0.47	47
12	0.01	0.0047			0.22	0.033			0.47	47

- Change 0.0068 µF at site 1 to 0.01 µF.
- The peak at m2 reduces significantly, but m1 is over the specification.

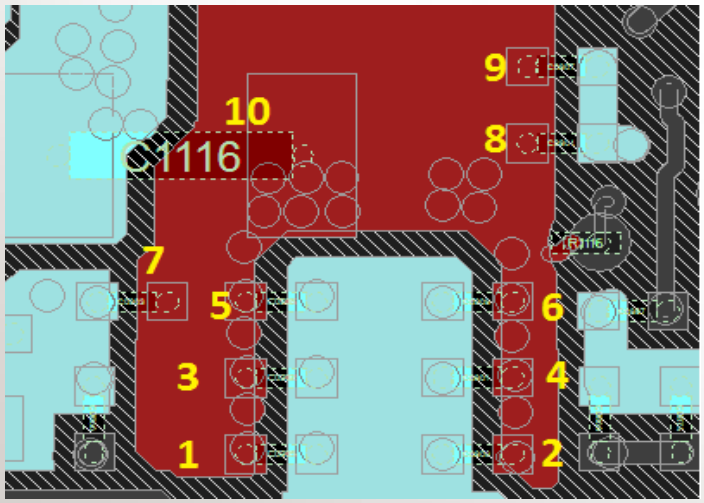


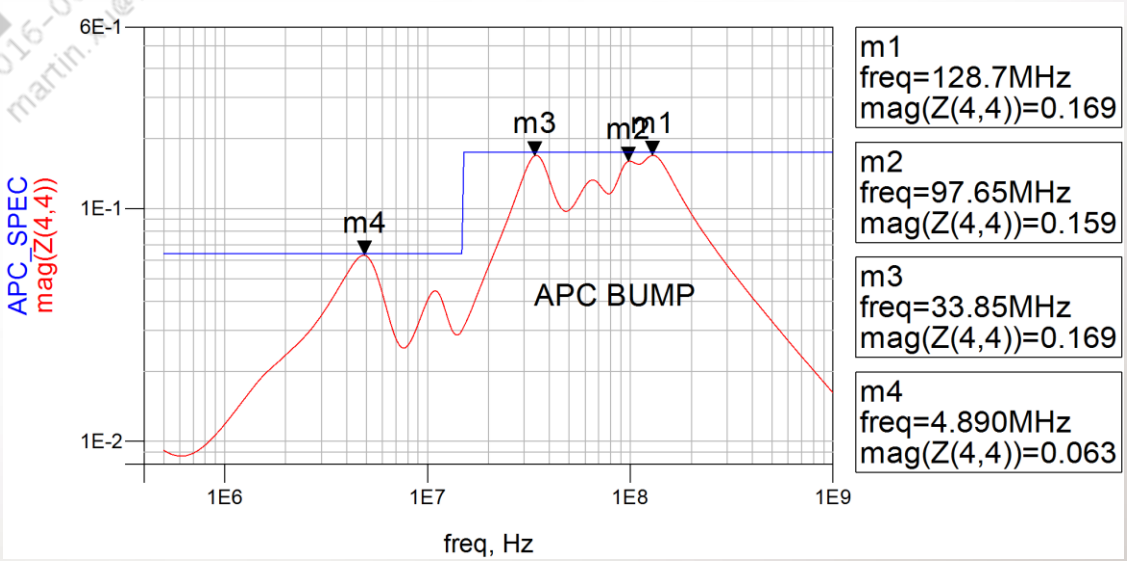


Iteration – 13

	Cap Site (Cap unit in µF)									
Iteration#	1	2	3	4	5	6	7	8	9	10
1									1	47
2									0.1	47
3									0.47	47
4						0.1			0.47	47
5			0.01			0.1			0.47	47
6			0.022			0.1			0.47	47
7		0.0047	0.022			0.1			0.47	47
8		0.0047	0.022		0.22	0.1			0.47	47
9	0.0068	0.0047	0.022		0.22	0.1			0.47	47
10	0.0068	0.0047	0.022		0.22	0.033			0.47	47
11	0.0068	0.0047			0.22	0.033			0.47	47
12	0.01	0.0047			0.22	0.033			0.47	47
13	0.0047	0.0047	0.01		0.22	0.033			0.47	47

- To reduce m1, we added another 0.0047 µF and swapped the capacitor at sites 1 and 3, so that the smaller cap is placed closer to the MSM™.
- It meets the specification over the entire frequency range.
- Need to re-arrange the capacitor placement so that some space can be saved.

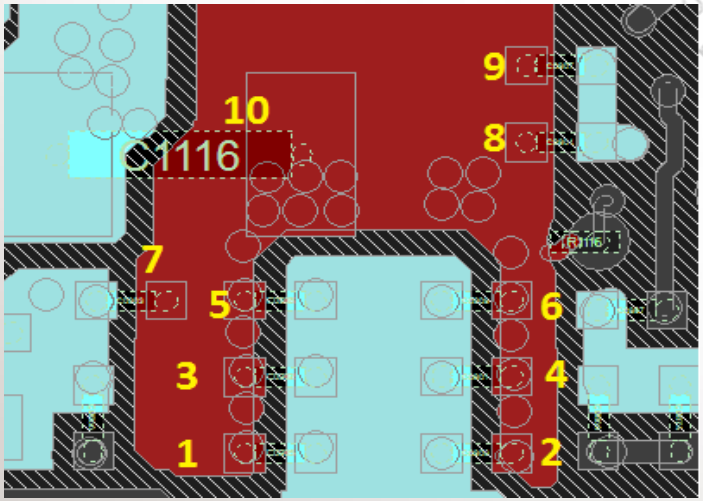


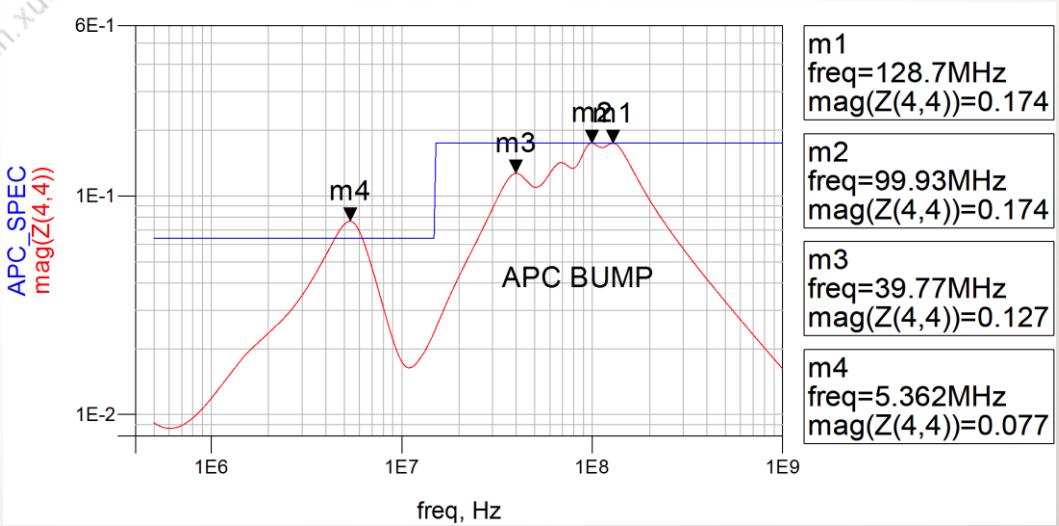


Iteration – 14

	Cap Site (Cap unit in µF)									
Iteration#	1	2	3	4	5	6	7	8	9	10
1									1	47
2									0.1	47
3									0.47	47
4						0.1			0.47	47
5			0.01			0.1			0.47	47
6			0.022			0.1			0.47	47
7		0.0047	0.022			0.1			0.47	47
8		0.0047	0.022		0.22	0.1			0.47	47
9	0.0068	0.0047	0.022		0.22	0.1			0.47	47
10	0.0068	0.0047	0.022		0.22	0.033			0.47	47
11	0.0068	0.0047			0.22	0.033			0.47	47
12	0.01	0.0047			0.22	0.033			0.47	47
13	0.0047	0.0047	0.01		0.22	0.033			0.47	47
14	0.0047	0.0047	0.01	0.033	0.22	0.47				47

- Re-arrange the caps from site 1 to site 6.
- It causes m4 to go over the specification. The reason is 0.47 µF (site 6) and 0.22 µF (site 5) are placed so close together (similar loop inductance) that they merge their effective frequency.
- Need to move 0.47 µF further to have a separate turning frequency.

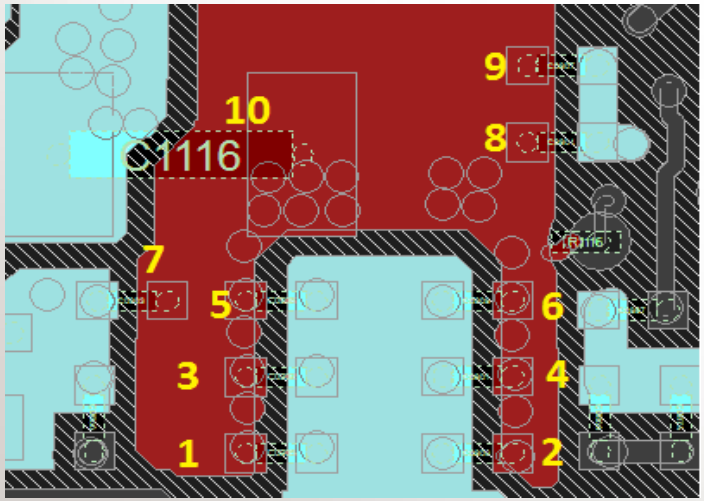


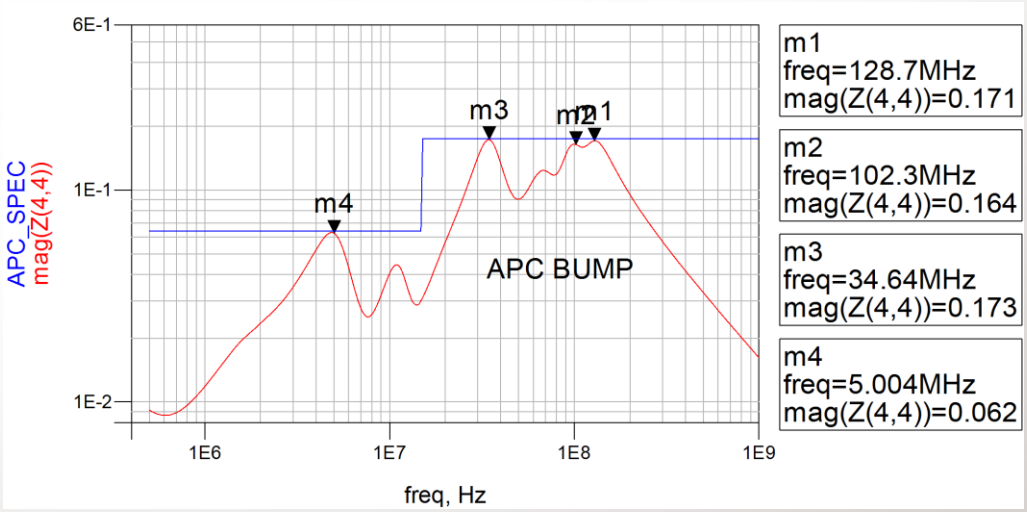


Iteration – 15

	Cap Site (Cap unit in µF)									
Iteration#	1	2	3	4	5	6	7	8	9	10
1									1	47
2									0.1	47
3									0.47	47
4						0.1			0.47	47
5			0.01			0.1			0.47	47
6			0.022			0.1			0.47	47
7		0.0047	0.022			0.1			0.47	47
8		0.0047	0.022		0.22	0.1			0.47	47
9	0.0068	0.0047	0.022		0.22	0.1			0.47	47
10	0.0068	0.0047	0.022		0.22	0.033			0.47	47
11	0.0068	0.0047			0.22	0.033			0.47	47
12	0.01	0.0047			0.22	0.033			0.47	47
13	0.0047	0.0047	0.01		0.22	0.033			0.47	47
14	0.0047	0.0047	0.01	0.033	0.22	0.47				47
15	0.0047	0.0047	0.01	0.033	0.22				0.47	47

- Moved 0.47 µF back to site 9.
- Capacitor set meets PDN specification.
- Three decoupling capacitors can be depopulated.





FAQs

FAQ #1

Question: I have exhausted all possible combinations of capacitors. I still do not meet the PDN specification.

Answer:

- Chances are that the loop inductance from capacitors to the Baseband IC is too high.
- Poorly done capacitor placement and PCB routing renders capacitors ineffective because of very high loop inductance to the capacitors.
- Refer to the appropriate Baseband IC design guidelines document for capacitor placement and PCB routing.
- Fix capacitor placement and PCB routing. Rerun the PDN capacitor optimization flow.

FAQ #2

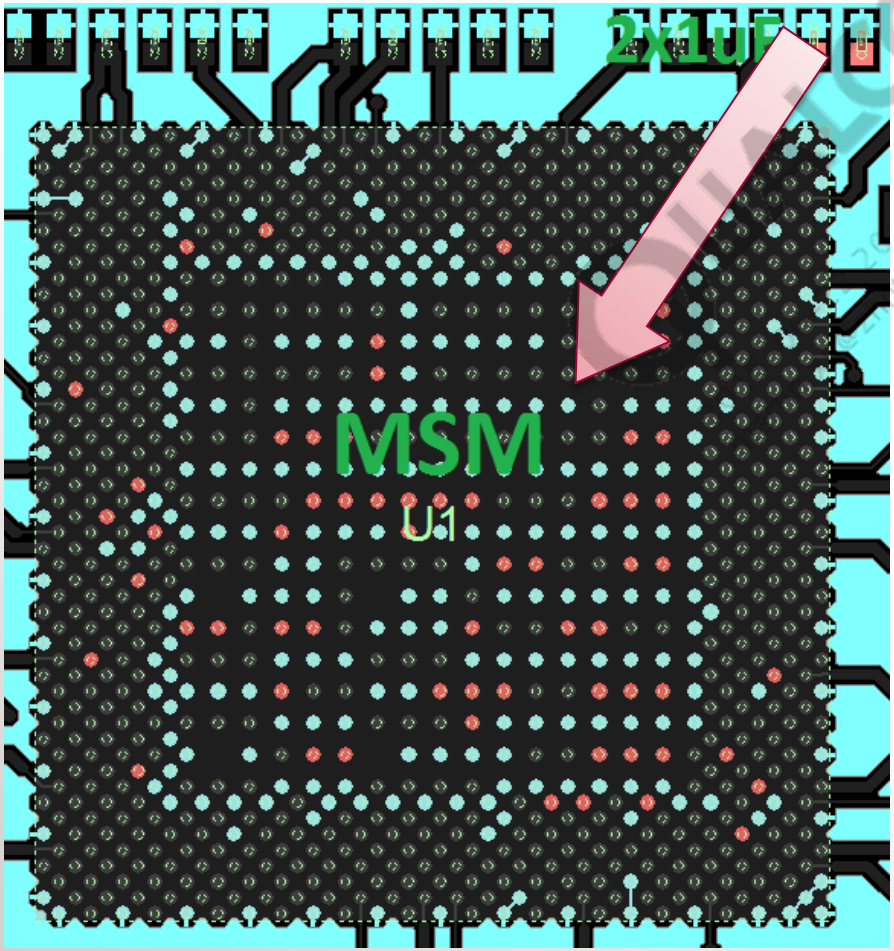
Question: What are recommendations for choice of capacitors?

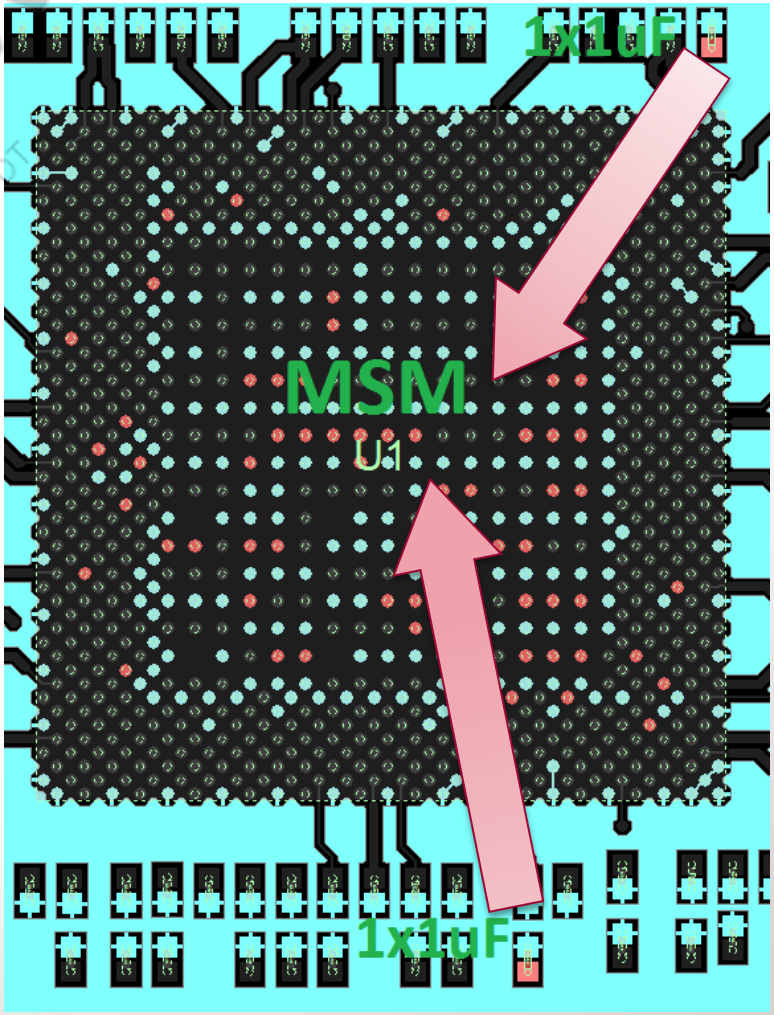
Answer: Capacitors whose capacitance does not change by more than 20% over extremes of temperature and voltage can be considered.

FAQ #3

Question: How to allocate capacitors if it has multiple decap banks?

Answer: Same or similar value caps having same or similar loop inductance from the Baseband IC should be placed as far apart from each other as possible. Below, the second design (on the right) has two parallel current paths and thus lower impedance.





FAQ #4

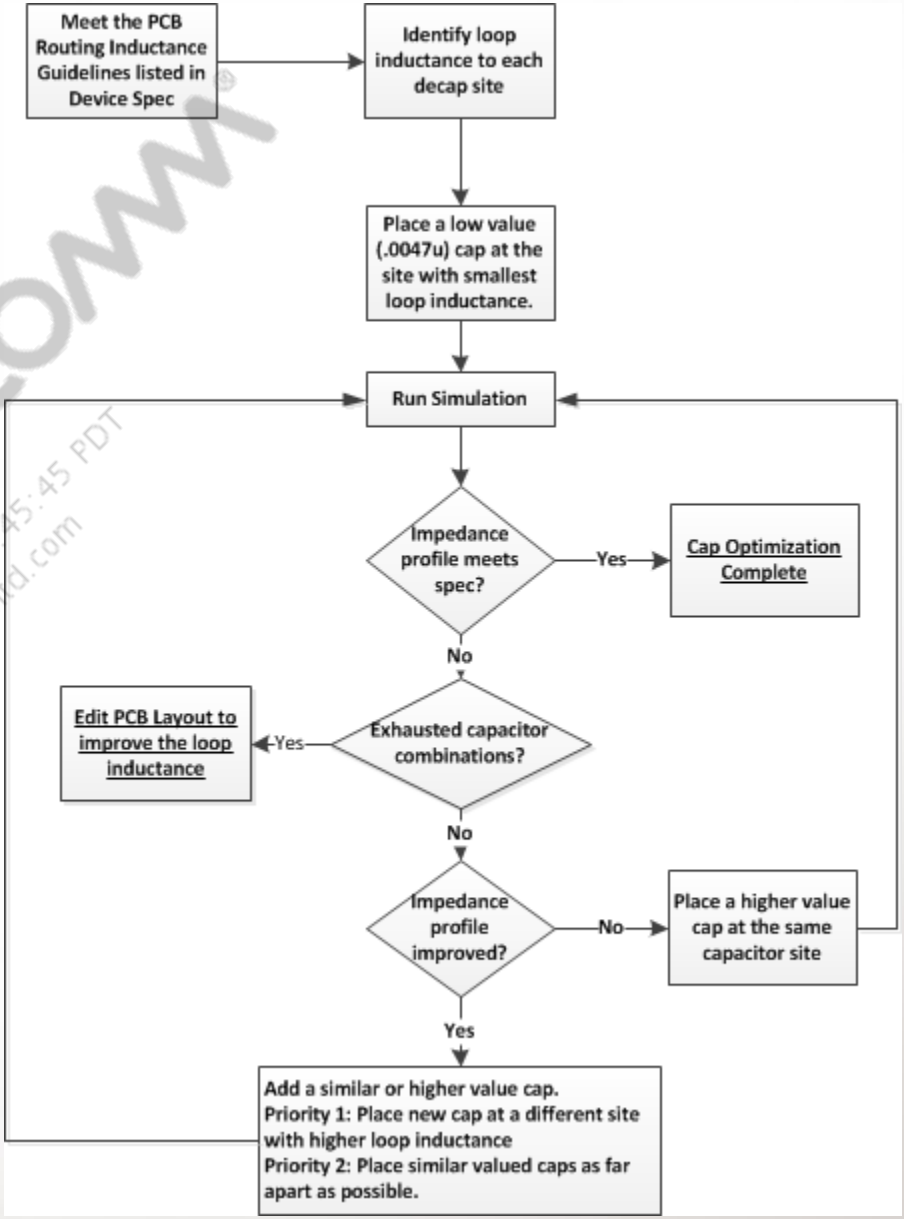
Question: Why do you only run the simulation from 1 MHz to 1 GHz? What about the impedance profile below 1 MHz?

Answer: Impedance profile below 1 MHz is dominated by the PMIC. Follow the PMIC placement and routing guidelines.

FAQ #5

Question: In the example, the impedance profile is optimized from low frequency to high frequency, i.e. the capacitor selection starts with high value and ends with low value. Can I start optimizing the impedance profile from high frequency to low frequency?

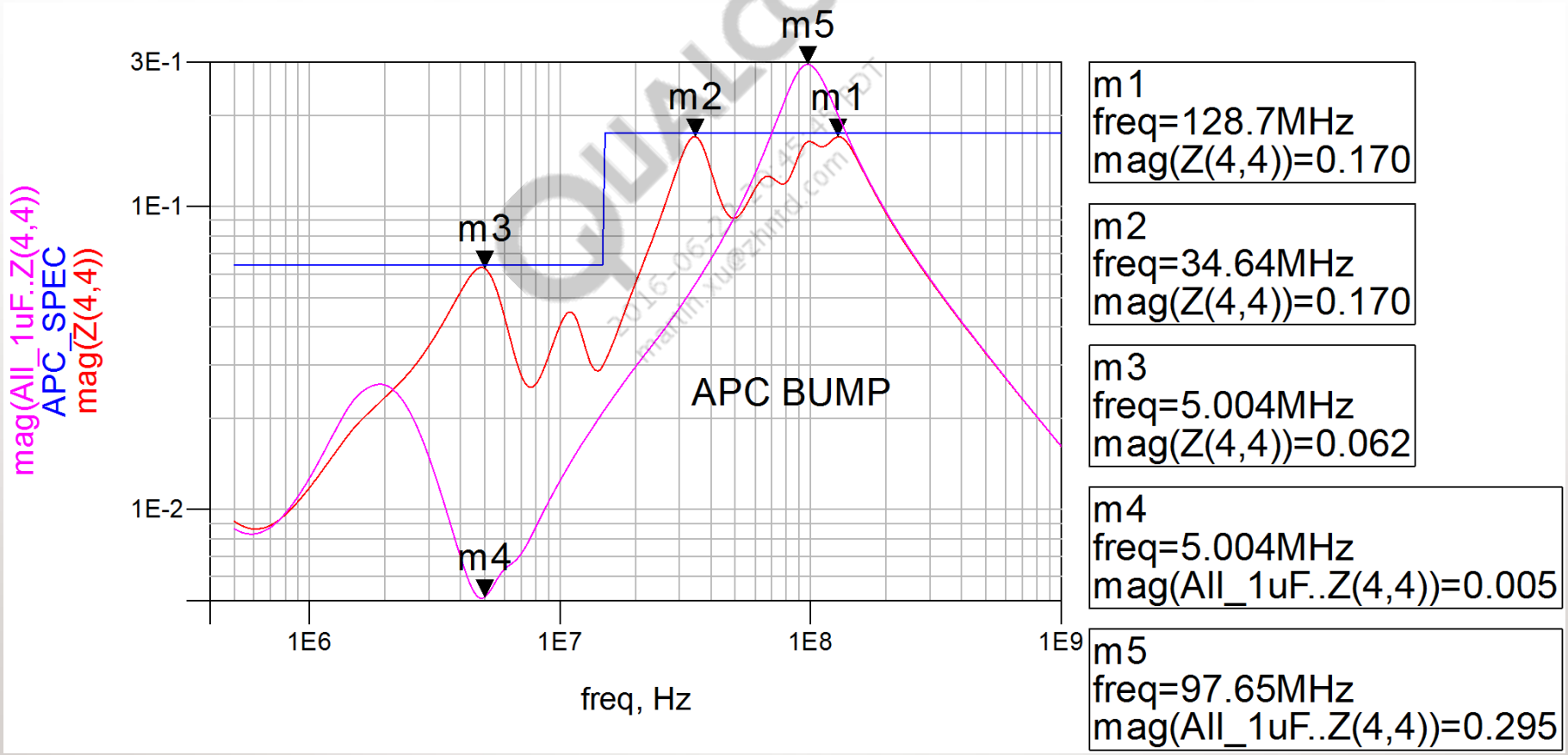
Answer: Yes, either way works. Follow the flowchart on the right, there are several differences.



FAQ #6

Question: Why is it better to place different value caps rather than same value caps? For example, what would happen if I use 1 µF cap everywhere.

Answer: Same value decaps has much higher Q-factor, thus the waveform is sharper. As shown below, it has a much lower valley (m4 at 5 mΩ), but it also causes a much higher peak (m5 at 295 mΩ).

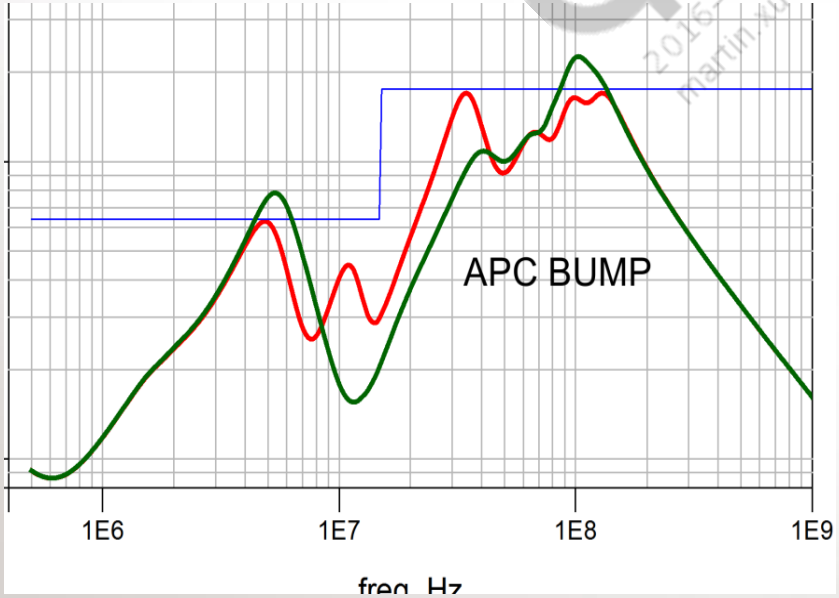


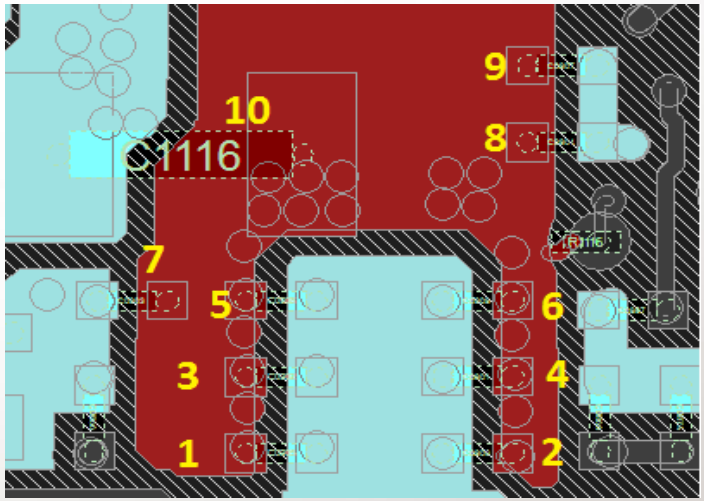
FAQ #7

Question: Why is it better to place larger value caps at higher inductance sites and smaller value caps at lower inductance sites?

Answer: If we place smaller value caps at higher inductance sites, at high frequency the loop inductance dominates the impedance. Small value caps lose their effect at a much lower frequency. The implication is that it would be very difficult to suppress high frequency peaks.

Site (µF)	1	2	3	4	5	6	7	8	9	10	Note
Red	0.0047	0.0047	0.01	0.033	0.22				0.47	47	Right placement
Green	0.47	0.22	0.033	0.01	0.0047				0.0047	47	Wrong placement





Questions?

https://support.cdmatech.com