Qualcomm
TECHNOLOGIES, INC

# Application Note

## System Power Monitor Tool

*80-N1622-16 Rev. G*

*March 13, 2013*

**Submit technical questions at:**
**https://support.cdmatech.com/**





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# Revision history

| Revision | Date | Description |
|---|---|---|
| A | October 2011 | Initial release |
| B | February 2012 | ▪ Added Sections 1 through 9 and Figure 6 through Figure 11 to describe and illustrate how to design and connect an EPM ready board, as well as how to set up the test environment.<br>▪ Added Figure 4 and text to describe the EPM connector alternate pin map. |
| C | July 2012 | ▪ Section 5.3. Replaced all the bullet items for WQEPM version 0.4, and added several items for new features for WQEPM version 0.5<br>▪ Section 5.4. Updated the document reference in step 3.<br>▪ Section 7::<br>▫ Included the connection information for the NRT Viperboard<br>▫ Added Figure 7, Figure 8, Figure 9, and Figure 10<br>▪ Added Section 7 and Section 8<br>▪ Section 10: Updated the document reference |
| D | September 7, 2012 | ▪ Updated the document title<br>▪ Replaced “EPM” with “SPM” throughout<br>▪ Replaced Figure 1<br>▪ Added Figure 2<br>▪ Added Chapter 3, “Obtaining an SPM Daughter Card”<br>▪ Moved the “SPM channel assignment” section (formerly Section 4.1) to Appendix A and renamed it “Recommended Channel Assignment”<br>▪ Replaced Figure 11, Figure 12, and Figure 13; the previous versions had pinout errors<br>▪ Chapter 8: Added a note to item 5c<br>▪ Added Appendix A<br>▪ Added Appendix B<br>▪ Added Appendix C<br>▪ Added Appendix D |
| E | September 12, 2012 | ▪ Corrected “WQSPM” to “WQEPM” throughout<br>▪ Section 1.1: Corrected the name of the Web-based Qualcomm® Embedded Power Monitor (WQEPM) software tool |
| F | February 2013 | ▪ Document re-released to coincide with SPMv3 launch. SPMv1 only information was moved to legacy Section 11. |

| Revision | Date | Description |
|---|---|---|
| G | March 2013 | ▪ Updated Figure 3 and Figure 4, SPM connector pin maps<br>▪ Added Figure 5, layout picture and Figure 6, SPMv3 Mechanical dimensions<br>▪ Updated features in section 6.4 and 6.5<br>▪ Added section 7.1<br>▪ Updated configuration file path in section 9<br>▪ Updated two new FAQs in section 10<br>▪ Added recommended channel assignments for devices based on MSM8x26, MSM8974, and MSM9x25 chipsets in the appendices<br>▪ Updated recommended channel assignments for devices based on MSM8x30, MSM8960 and MDM9x15 chipsets and Fusion 3 devices in the appendices |

# 1 Introduction

## 1.1 Purpose

This application note provides a description of the System Power Monitor (SPM) tool. The SPM tool assesses the impact on power after new or changed software (device driver, applications, or other software) has been added to the power monitoring device environment. The user of the SPM application would typically compare new results for power measurement points to known results before the changed software was applied to the target device environment. The SPM application allows any noticeable power differences for these power measurement points to be observed.

This application note describes the SPM basic specifications, block diagram, application, and Web-based Qualcomm Embedded Power Monitor (WQEPM) software tool.

## 1.2 Scope

This document is for engineers or software developers who want to monitor the power usage of one or more measurement points in a target device. Normally, this occurs after written device drivers or applications have been written to run in the target device, and the power usage needs to be assessed. This document is also to help HW engineers in designing their own SPM daughter card or properly designing their test phone to be SPM ready. Users are expected to be familiar with the target device and its underlying chipset.

## 1.3 Technical assistance

For assistance or clarification on information in this guide, submit a case on the Qualcomm CDMA Tech website at https://support.cdmatech.com/.

# 2 Overview

## 2.1 SPM overview

The SPM intercepts the PMIC device power supplies with sense resistors in the path of the power lines, as illustrated in Figure 1. There are two types of power supplies: a switch regulator and a linear regulator. For the switch regulator, the sense resistor is part of the sensing loop. For the linear regulator, the sense resistor becomes part of the PDN impedance.

The SPM daughter card connects each sense resistor to an operational amplifier to amplify the voltage across it. The operational amplifier also provides noise rejection to filter any common mode noise from the sense resistor.

The operational amplifier output is connected to a Cypress Programmable System-On-Chip (PSOC). The PSOC digitalizes the data and communicates via USB to be read by WQEPM on a PC.

## 2.2 SPM Version 3 (SPMv3)

SPMv3 is the latest version of the SPM daughter card. It replaces the 3 TI ADCs with 2 Cypress PSOC chips with an internal SPI to USB interface. This allows Qualcomm to forgo the need for a 3rd party board, creating a simpler and cheaper user experience as well as giving Qualcomm more flexibility in future SW changes. The reference voltage of the op-amps was increased from 0 to 0.3 V, allowing for more accurate low current measurements. This same reference was used as a reference to the PSOCs ADC and therefore does not affect the measurements. An additional 14 channels were added for voltage readings only. There are still 48 current reading channels. The only cable needed to connect to the PC is a micro-USB cable.

SPMv3 is the recommended version for new and existing designs and is currently the only one with continual software updates and support.

## 2.3 Warning

It is recommended that the SPM daughter card is connected to USB whenever the DUT is powered up.

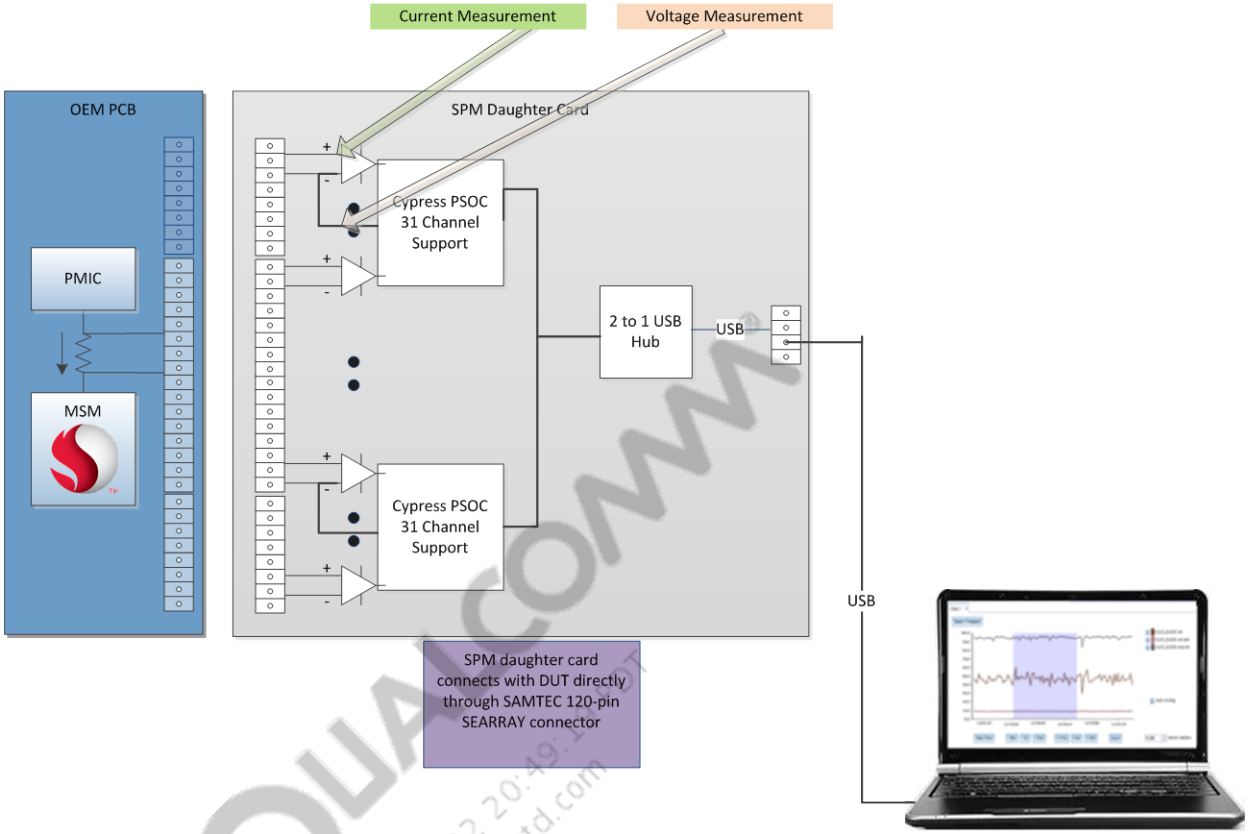



**Figure 1 - SPMv3 Block Diagram**

# 3 Obtaining an SPM Daughter Card

The SPM daughter card can be purchased on QUALCOMM's *Customer Extranet for QTI* https://cp.qti.qualcomm.com.

# 4 Creating Your Own SPM Daughter Card

Qualcomm provides an SPMv3 Daughter card Reference Schematic, 80-N6594-43.

## 4.1 Design Tips for SPMv3

SPMv3 consists of three major blocks. The first block consists of the 48 op-amps. When routing the M and P lines, make sure they are routed as differential pairs. It is recommended that PSOC_SPM_VREG_0P3 is done as a power plane (or half a plane) to make routing easier.

The second major block is the two PSOCs. These are fairly straight forward. Make sure that the main PSOC has P12(0) tied to ground and the secondary PSOC has P12(0) tied to VDD. The main PSOC uses P1(0), P1(1), P1(3) and P12(2) to connect to the MSM™ and initial programming, and the secondary PSOC uses these pins for initial programming.

The third major block is for connectivity and power. It is recommended by Cypress that each PSOC has its own programmer connection. It is also recommended to use an oscillator fan out buffer since the clock is used in both PSOCs and the USB hub. A voltage divider and op-amp circuit are used for the 0.3 V reference. An LDO can be used for this, but the 0.3 V reference has to be driven and cannot be done by *just* a voltage divider. After tests it is also determined that the 0.3 V can come from the PSOC's DAC. This will save space and lower BOM costs.

The 1.8 V rail is purely used to allow the level translator to give the 3.3 V I/O the ability to communicate with the 1.8 V rails from the GPIO power domain on the MSM. This rail is only necessary if you want your design to have Qview functionality and does *not* affect normal WQEPM operation. This power rail should be driven by the OEM device through pin 65. Since this is only used to power two level translators, it has a minor impact on current consumption. The other option is to use an onboard LDO. (To be updated).

A USB hub is needed to run both PSOCs on one PC. The USB hub needs to be setup as self-powered to properly run.

# 5 Specifications

- System accuracy for current measurement: ±3% at room temperature
  - ***This is DC accuracy in normal operating conditions compared to what a DMM would measure across a resistor and compared to what shows up on WQEPM.***
  - ***This is not an accuracy measurement to compare to Power Dashboard numbers.***
  - Accuracy at extreme temperature goes up to ± 6%.
- DC offset calibration possible to adjust absolute accuracy
- Four GPIO pins are dedicated for software triggering
- The ADC sampling rate is 10 kSPS *aggregate per PSOC*
  - If measuring two channels on the same PSOC, sample rate becomes 5kSPS per channel.
  - If measuring one channel from PSOC 0 and one channel from PSOC 1 both channels will have 10 kSPS sampling rate.
  - Voltage and current measurements use different ADCs inside the PSOCs.
- The SPM circuitry only supports external access through WQEPM on the PC.
- The SPM design will provide up to 48 current rails and 14 voltage rails. Each current channel measures a voltage across sense resistor and a current sense amplifier generates up to a 2.048 V full-scale signal.
- PSOC ADC resolution is 16 bits (signed) for current, 12 bits (unsigned) for voltage.
- The SPM can connect with an OEM device under test (DUT) via a Samtech Searray 120-pin (20 × 6) connector (SEAF-20-05.0-S-06-2-A female connector on the DUT and SEAM-20-02.0-S-06-2-A male connector on the SPM).

## 5.1 Error Measurements

Below is the model used to calculate the error measurements from above. It did not take into account error from the sampling rate or noise onto the data lines.

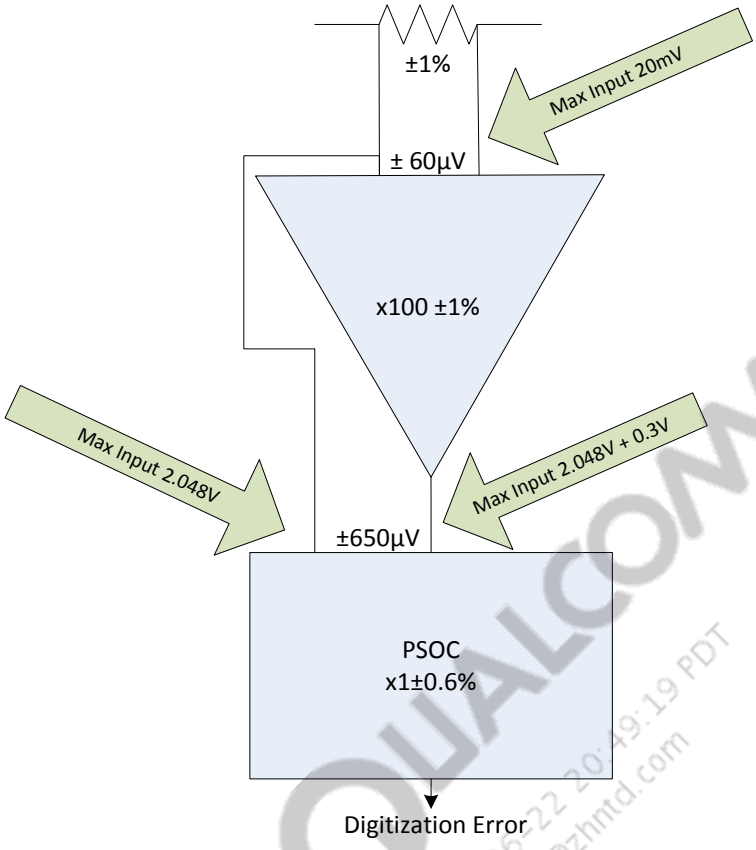



**Figure 2 - SPMv3 Error Calculation Diagram**

# 6 SPM to DUT Interface

The SPM connects to the DUT via a Samtech Searray 20 × 6 connector (SEAF-20-05.0-S-06-2-A female connector on the DUT and SEAM-20-02.0-S-06-2-A male connector on SPM).

## 6.1 SPM connector pin map

There are different ways that the CAD pinout is represented on the schematic. Figure 3 and Figure 4 show two possible pinouts. Make sure the pinout corresponds correctly to the SPM connector pin map shown in Figure 3.

| 120 | 114 | 108 | 102 | 96 | 90 | 84 | 78 | 72 | 66 | 60 | 54 | 48 | 42 | 36 | 30 | 24 | 18 | 12 | 6 | |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| 47+ | 47- | EM1 | 41+ | 41- | 35+ | 35- | GND | 29+ | 29- | 23+ | 23- | EM2 | 17+ | 17- | 11+ | 11- | GND | 5+ | 5- | 6 |
| 46+ | 46- | 40+ | 40- | GND | 34+ | 34- | 28+ | 28- | 1.8V | 22+ | 22- | 16+ | 16- | GND | 10+ | 10- | 4+ | 4- | GND | 5 |
| 45+ | 45- | GND | 39+ | 39- | 33+ | 33- | GND | 27+ | 27- | 21+ | 21- | GND | 15+ | 15- | 9+ | 9- | GND | 3+ | 3- | 4 |
| 44+ | 44- | 38+ | 38- | GND | 32+ | 32- | 26+ | 26- | GND | 20+ | 20- | 14+ | 14- | GND | 8+ | 8- | 2+ | 2- | GND | 3 |
| 43+ | 43- | GND | 37+ | 37- | 31+ | 31- | INT | 25+ | 25- | 19+ | 19- | XO_OU | 13+ | 13- | 7+ | 7- | GND | 1+ | 1- | 2 |
| 42+ | 42- | 36+ | 36- | GND | 30+ | 30- | 24+ | 24- | GND | 18+ | 18- | 12+ | 12- | GND | 6+ | 6- | 0+ | 0- | GND | 1 |
| 115 | 109 | 103 | 97 | 91 | 85 | 79 | 73 | 67 | 61 | 55 | 49 | 43 | 37 | 31 | 25 | 19 | 13 | 7 | 1 | |

**Figure 3 SPM connector pin map**

| 120 | 114 | 108 | 102 | 96 | 90 | 84 | 78 | 72 | 66 | 60 | 54 | 48 | 42 | 36 | 30 | 24 | 18 | 12 | 6 | |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| 120 | 114 | EM1 | 102 | 96 | 90 | 84 | 78 | 72 | 66 | 60 | 54 | EM2 | 42 | 36 | 30 | 24 | 18 | 12 | 6 | 6 |
| 119 | 113 | 107 | 101 | 95 | 89 | 83 | 77 | 71 | 1.8V | 59 | 53 | 47 | 41 | 35 | 29 | 23 | 17 | 11 | 5 | 5 |
| 118 | 112 | 106 | 100 | 94 | 88 | 82 | 76 | 70 | 64 | 58 | 52 | 46 | 40 | 34 | 28 | 22 | 16 | 10 | 4 | 4 |
| 117 | 111 | 105 | 99 | 93 | 87 | 81 | 75 | 69 | 63 | 57 | 51 | 45 | 39 | 33 | 27 | 21 | 15 | 9 | 3 | 3 |
| 116 | 110 | 104 | 98 | 92 | 86 | 80 | INT | 68 | 62 | 56 | 50 | XO_OU | 38 | 32 | 26 | 20 | 14 | 8 | 2 | 2 |
| 115 | 109 | 103 | 97 | 91 | 85 | 79 | 73 | 67 | 61 | 55 | 49 | 43 | 37 | 31 | 25 | 19 | 13 | 7 | 1 | 1 |

**Figure 4 SPM connector alternate pin map**

The 4 digital channels (in blue) need to be connected to open GPIOs for extra functionality. EPM Marker 1 and 2 can go to any open GPIO pin on the MSM device. Code can be programmed on the MSM device to output a digital signal to be read into WQEPM. CXO_EN can be used in the same way (can be used as a separate GPIO). The interrupt signal goes from the PSOC to the MSM device and is there for potential future implantation. The 1.8 V rail is connected to the 1.8 V GPIO power rail on the system. This is currently DNI'd on the SPM and is being powered by an LDO. None of these are needed for WQEPM and can be left floating.

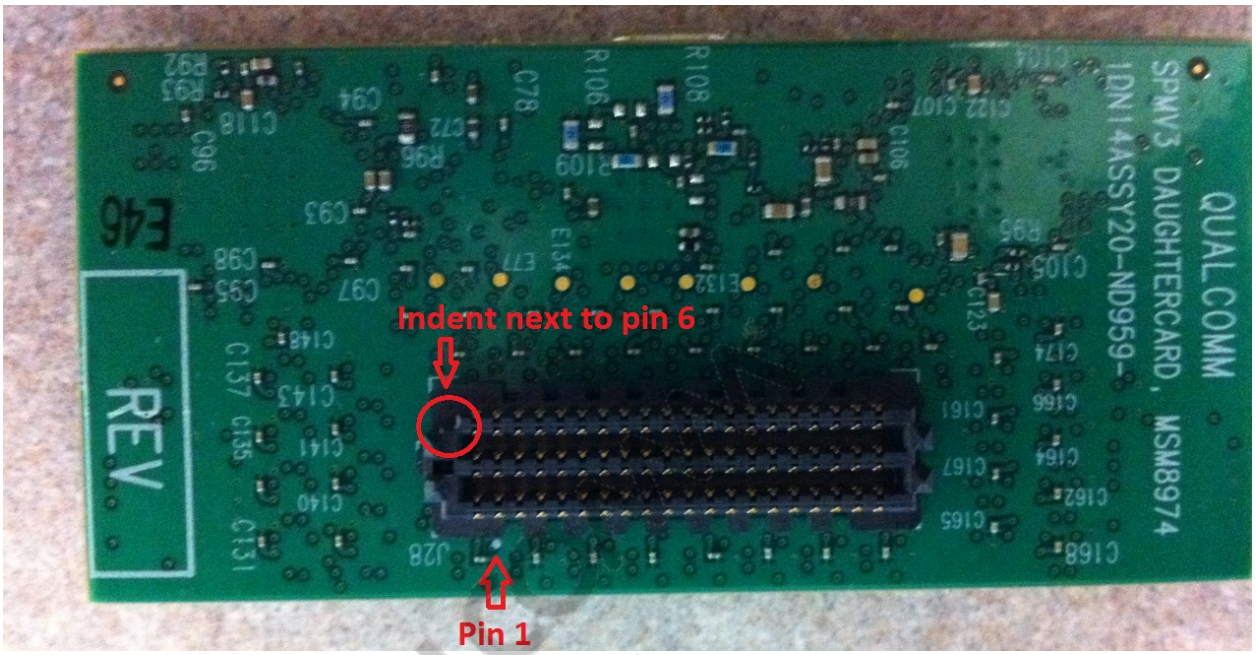



**Figure 5 Layout picture**

In Figure 5, the white dot shows the location of pin 1 on the Samtech connector. Notice the indent next to pin 6. This should line up with the same indent for the female connector on the DUT.

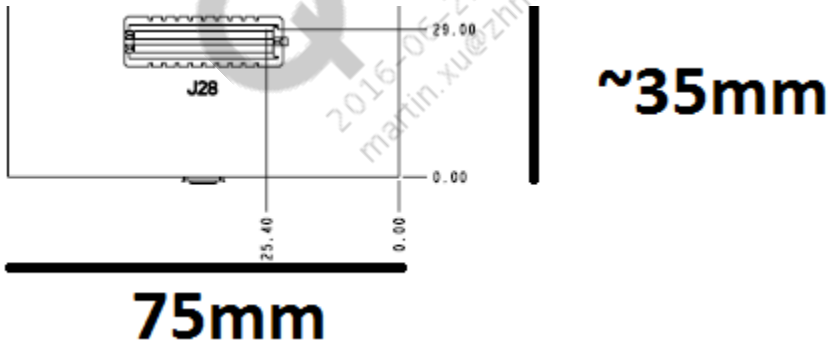



**Figure 6 SPMv3 mechanical dimensions**

## 6.2 Measuring voltage channels

The SPMv3 has 14 current channels that also have the ability to measure the voltage on the non-PMIC side of the sense resistor. The following channels have this capability:

0 – 1 – 29 – 30 – 31 – 32 – 33 – 34 – 35 – 36 – 37 – 38 – 39 – 40

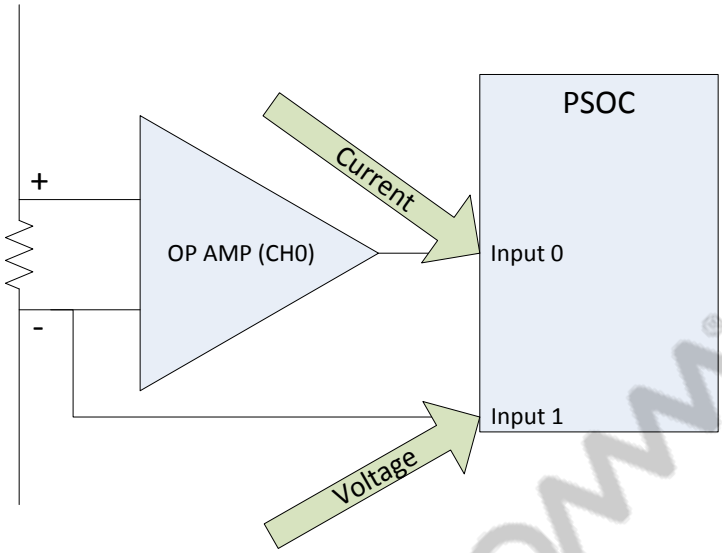



**Figure 7 - Example for channel 0 voltage reading**

## 6.3 WQEPM Overview

The WQEPM is a Windows application that integrates an embedded web server and database to store power data from SPM-enabled targets and to respond to requests for data retrieval from a web browser on the same (local) or remote host machine .

The WQEPM application enables the user to obtain power measurement results from power rails on a supported target device. The results can be viewed and analyzed on any terminal (e.g., Windows, Linux) with any of the following browsers at the specified version or later:

- Chrome 9.0
- Firefox 3.5
- Internet Explorer 9.0
- Safari 12.0

The WQEPM application supports three types of interfaces. These three interfaces are:

- The WQEPM browser user interface from a local or a remote browser to the Windows PC where the WQEPM server/data manager application is installed.
- The shared WQEPM browser user interface from a remote browser to the Windows PC where the WQEPM server/data manager application is installed.
- Client scripts from any location using WQEPM automation interfaces.

These three interfaces use the hypertext transfer protocol (HTTP) WQEPM APIs.

The WQEPM server/data manager application communicates with the onboard PSOCs

## 6.4 Features

The following are the features of the WQEPM version 1.2:

- Supports dual PSoC including SPMv3

- Capability to configure the PSoC sampling rate
- Configures the PSOC on the SPM circuitry for power data collection.
- Collects and graphically displays power data with zoom-able plots.
- Left mouse click-and-drag in the plot area to display detailed power information in the highlighted area.
- Can move forward and backward in time to view collected data.
- Monitors voltage and/or current on multiple system power rails.
- Provides automatic minimum, maximum, and mean calculations on the data.
- Multiple power rails can be plotted per chart/tab.
- Multiple charts/tabs per browser page allowed with time synchronization option.
- Save, restore, delete channel configurations.
- Display gain/resistor/voltage value per channel.
- Disable auto-scale (Y-axis) with user set upper/lower limits (clip display).
- Pause data display (data collection continues in background).
- Display statistics on measurement points while display paused.
- Export channel data (CSV format).
- Share display view (name/save URL).
- Monitor GPIO channels.
- Use dynamic voltage (for channels that provide reading) in power calculations.
- Launch WQEPM browser GUI from WQEPM server GUI command menu.
- Time correlation between WQEPM server/data manager and browser host (remote access).
- Local/remote browser support for the WQEPM browser user interface that internally uses HTTP WQEPM APIs.
- Automation support via HTTP WQEPM APIs (scripts).
- Mongoose 3.0 server and SQLite 3.7.3 database integrated into the WQEPM server/data manager.
- Windows-only host support for the WQEPM server/data manager in WQEPM 0.5.1.

## 6.5 Installing WQEPM

To install the WQEPM, use the following installation steps:

1. Install the provided WQEPM application on the Windows PC. Refer to the *Web-based Qualcomm Embedded Power Monitor Version 1.0 User Guide* (80-N4235-3) for more detailed information.
2. Ensure that the standard USB Type A to USB Type B cable is available.

A channel configuration file is installed for the target power monitoring device by the installation process. This channel configuration file is in one of the following folders and may be edited, if necessary.

- For the 32-bit Windows versions, refer to C:\Program Files\Qualcomm\WQEPM\Config\.
- For the 64-bit Windows versions, refer to C:\Program Files(x86)\Qualcomm\WQEPM\Config\.

3. In some versions of WQEPM, the SPMv3 config file is in the folder CustomizedTargetExample and is labeled CustomziedTargetSPMv3EPMConfiguration.xml. This needs to be copied into the main folder to be read.

## 6.6 Obtaining WQEPM

Currently the only way to obtain WQEPM (HK11-N6521-2) and the WQEPM user manual (80-N4235-3) is to open a Support ticket at https://support.cdmatech.com.

Use the following information when opening a case

- Initial Problem Type = Hardware
- Problem Area 1 = Digital Baseband
- Problem Area 2 = Power Consumption

Be sure to specify that you are looking for the latest version of WQEPM in the subject line.

# 7 Designing an SPM-ready board

To design an SPM-ready board, use the following guidelines:

- Op-amp polarity: It is mandatory that the PMIC side input is connected to the positive side of the op-amp. If the reverse happens, the op-amp will send a negative voltage to the SPM's ADC resulting in an incorrect output.

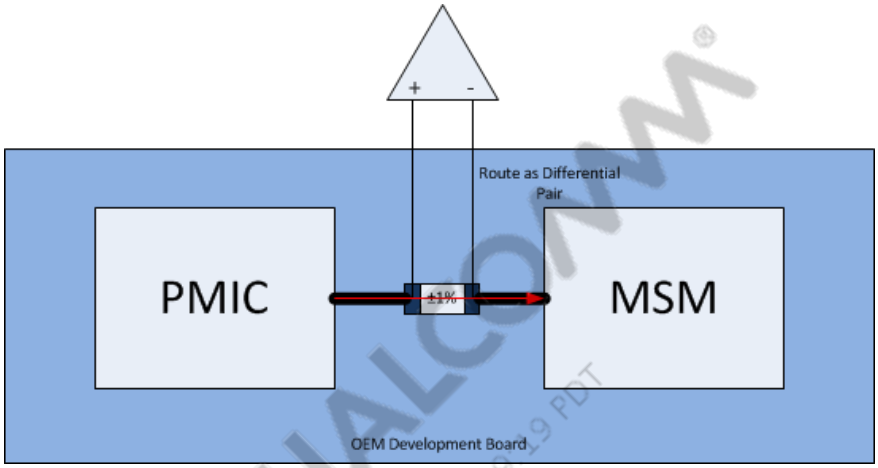



**Figure 8 - Designing an SPM-ready Board**

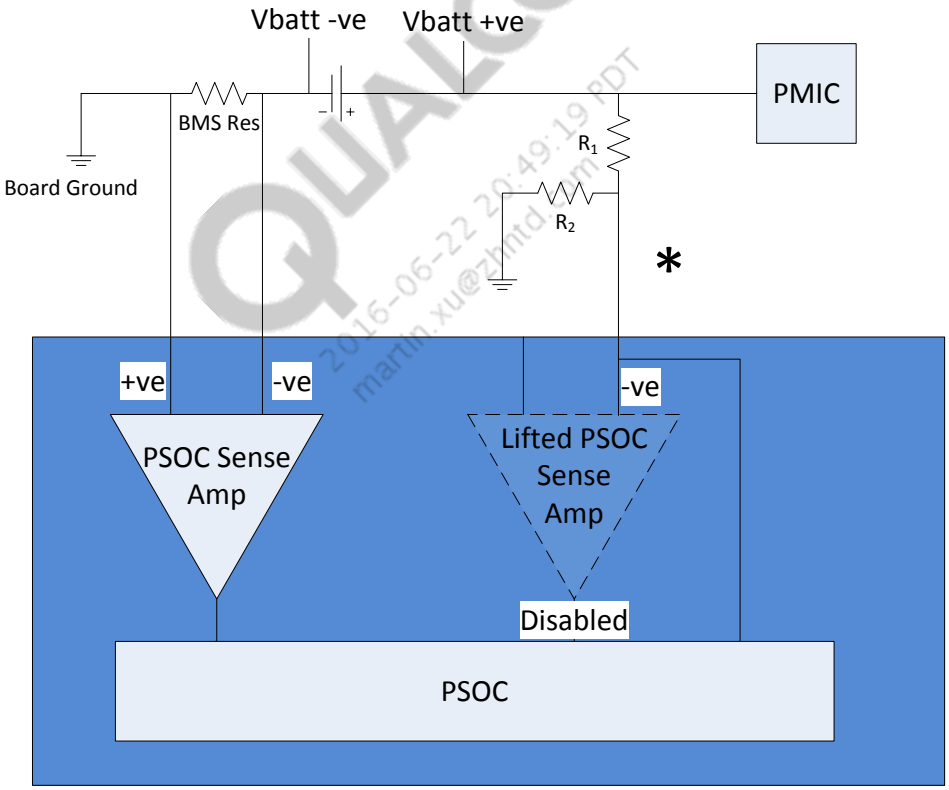
- Use resistors with ±1% (or better) tolerance: Since the WQEPM uses the optimal resistor value input into the config file, mismatched resistance will add more error. If a resistor is 10% off from the nominal, the current readings max error will increase 10%.
- Treat the traces to the op-amp pins as a differential pair: Because the drop across the sense resistors can sometimes be smaller than 1 mV, noise can play a major role on the outcome if the noise only couples onto one of the traces (+1 mV induced onto the + only side would create 100% error). To minimize this, these two traces should run as close together as possible all the way from the sense resistor up to the Samtech connector. Noise coupled onto one line, will be the same on the second line, and will effectively be ignored.
- Traces should start as close to the resistor as possible (Kelvin connected).
- Prevent the sense resistors from greatly affecting the PDN of the power lines: When using sense resistors, make sure to get resistor sizing appropriate to how much current goes through the resistor. Resistors on a Krait power path need to have a higher current rating (MSM8960 should be able to pass at least 2 A). Also make sure that power lines with larger currents have appropriate number of vias going to the sense resistors. If you are running 1.5 A through one micro-via, you will create an issue on the PDN network and potentially damage your PCB, due to thermal issues.
- Aim for a voltage drop across the sense resistors to be a maximum of 15 mV and a minimum of 0.5 mV.
- If 5 micro vias are required to bring a trace from the PMIC to a different layer, then 5 micro vias will be required to bring the trace from that layer to the sense resistor.
- For rails driven by a switching power supply, place sense resistors in series with the inductors and prior to the sense-line used for feedback

## 7.1 Measuring VBatt

To measure battery current, the sense resistor needs to be placed on the negative side of the battery. The voltages are too high to be read if the sense resistor is placed on the positive side. Under most conditions, the BMS resistor should be connected to the SPM connector. The channel assignment also needs to be flipped compared to what all other channels are like. The + connector should be connected to the board ground, while the – connector should be connected to the negative side of the battery (follows the current flow).

To measure the battery voltage, a voltage divider must be used to bring the voltage level below 2 V. It is recommended to do this with resistors that have a large resistance to limit leakage current. The voltage divider needs to be connected to the – side of the connector. The sense amp on the SPM must be removed from the board or else the feedback resistors inside the sense application package will cause the voltage readings to have inaccurate results.

This voltage reading needs to be done on one of the voltage channels. See the chart and blueprint (highlighted in blue) to see which op-amp needs to be lifted.




* Note: The Vbatt voltage sensing voltage divider needs to be connected to the -ve terminal of a voltage capable channel (0,1,29-40). $R_1$ & $R_2$ should be high impedance (>100kΩ to reduce leakage current)

**Figure 9 Battery measurement implementation**

| Channel | Op-Amp | Channel | Op-Amp |
|---|---|---|---|
| 0 | U67 | 34 | U113 |
| 1 | U69 | 35 | U106 |
| 29 | U96 | 36 | U108 |
| 30 | U105 | 37 | U110 |
| 31 | U107 | 38 | U112 |
| 32 | U109 | 39 | U114 |
| 33 | U111 | 40 | U97 |

**Table 1 SPM Channel Op-apm**

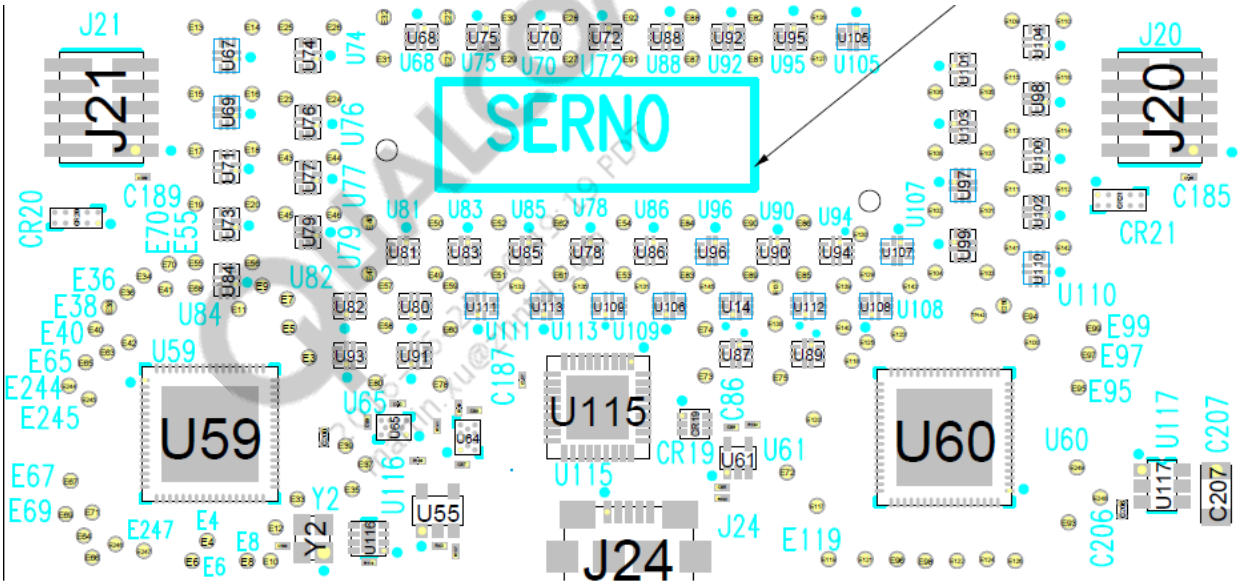



**Figure 10 SPMv3 Blueprint – voltage channels highlighted in blue**

# 8 Running Simulations

To run simulations, use the following steps:

1. Plug the SPM into your SPM-ready device.
2. Connect the SPM to a PC via USB
3. Turn on WQEPM software as follows:
   a. Click Targets > *CustomziedTargetSPMv3EPMConfiguration.xml*

**NOTE:** The target being used does not matter. It is dependent on which configuration file you have edited and want to be selected.

   b. Click File > Start
   c. The top of the program should change from WQEPM …stopped to WQEPM …running
4. If the default browser is not Internet Explorer
   a. Click Command > Start Default Browser
5. If the default browser is Internet Explorer
   a. Open up a non IE browser (Chrome, Firefox, Safari)
   b. Type **`localhost:7376/wqepm/`** into the address bar
   c. Type **`localhost:7376 into the Connect text box`**
6. Calibrate your SPM board (**Optional at room temperature and normal operation**)
   a. Due to the input offset voltage inherent to op-amps, every reading will be slightly off (dependent on sense resistor value and offset voltage). Due to improvements over previous SPM designs, this offset is much less significant at room temperature.
   b. While the phone is off and the SPM is on, select a new chart with every power rail selected. Click Start. You should notice that all of the rails are measuring a current between 0 and a few mA.
   c. Let the program run for a few seconds and pause the chart. Click and drag across the graphs (this obtains data points) and export this information to Excel. You can save this as your offset value and simply subtract these values from your real measurements.
   d. This is still recommended to do at very high or low temperatures as there will be a bigger offset at the op-amp.
   e. It is also recommended to do this at very low currents
7. You are now ready to power on the phone and begin running experiments.

# 9 Configuration File

The configuration files is what the WQEPM system uses to know what the sense resistor values are on your device, as well as how to group different power rails. The default location (on Windows) for the configuration file is `C:\Program Files (x86)\Qualcomm\WQEPM\Src\Config`. The configuration file that should be changed for using this SPM is *CustomziedTargetSPMv3EPMConfiguration.xml*.

**NOTE:** Due to security settings on some computers, it might be required to copy this file and edit it in another directory, and then copy it back into this directory. If the PC complains that the file is in use when it is not, this may be why.

The two most important categories to be edited in the configuration file are *Name* and *Resistance*. The WQEPM calculates the current values.

$$i = \frac{Vin}{Gain * Resistance}$$

- ***Gain*** is meant to offset the gain that the op-amp provides. Gain should be set to 100. If a different op-amp is used with a different gain (not shipped like this), the config file has to be adjusted appropriately.
- ***Resistance*** should match the resistor values on the phone (resistance is in mΩ).
- ***Name*** is the name of the power rail. This shows up in the WQEPM software.
- ***Category*** is used to group the different power rails together. Used for finding different rails as well as toggling rails on and off as a group (in the web browser).
- ***Voltage*** has no obvious affect. Used to quickly state power consumed (P=VI).
- ***Units*** are very important in SPMv3. Depending on whether this is *mA* or *mV* a different ADC is used inside the PSOC. By setting these incorrectly, that respective channel will see a linear error of 0.3/(Gain * Resistance).
- ***Description*** is the description of the channel.
- ***ID*** corresponds to each individual ADC's input. These match up to the channels. ADC0, ID0 corresponds to channel 1, while ADC1, ID0 corresponds to channel 17.

**NOTE:** Voltage rails always have a gain of 1 and a resistance of 1000 mohm.

# 10 WQEPM Browser User Interface

Refer to the *Web-based Qualcomm Embedded Power Monitor Version 1.0 User Guide* (80-N4235-3) for more detailed information about the WQEPM user interface when using a browser.

# 11 FAQ

1. *If I turn on the SPM while it isn't connected to anything, I see a large value on all of the voltage lines. Why?*
   This is caused by the 0.3 V reference used on the op-amps to increase the low voltage accuracy. When IN- and IN+ are left floating the voltage at the REF pin is seen at IN-. Since the voltage channels are configured to go into the ADC that does not reference the 0.3 V, and read IN-, the reference voltage goes into this channel and is seen as a large positive value on WQEPM. When the SPM is plugged into a DUT this issue disappears.

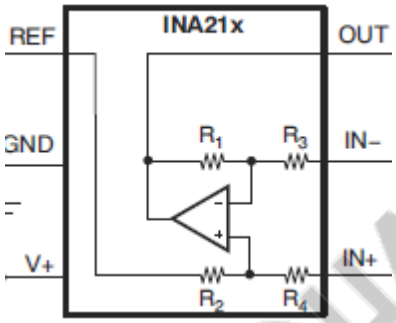



**Figure 11 - TI Operational Amplifier**

2. *The current values that I am obtaining do not match those of the Power Dashboard numbers. Why?*
   SPM is ***not*** meant to be used to match up with Power Dashboard values. QUALCOMM's internal solution (XPM) is a very expensive and very precise tool to do measurement. SPM does not have the same accuracy as XPM, which was used for Power Dashboard.
3. *If SPM is not as accurate as XPM, why not just use XPM?*
4. XPM is a very large, and very complicated system. SPM is very easy to use and it is relatively cheap to buy numerous SPM boards so any engineer can easily test a new SW build to monitor power.
5. *Can SPMv3 work with any Qualcomm chipset?*
   Yes! The SPMv3 can be used with any chipset. Qualcomm will provide support SPMv3 support for all active chipsets.
6. *In the past we had to use the NanoRiver Miniboard/Viperboard. Is this still necessary?*
   One of the great new features of SPMv3 is that the only piece of equipment you need is a PC, SPMv3 and a USB cable.
7. *What are the programmers used for? As an OEM are we responsible for programming?*
   The programmers are used to flash the 2 PSOCs with firmware. This will be done at Qualcomm when the boards are built. If you decide to build your own version of SPMv3 you will need to purchase a PSOC programmer from Cypress.
8. *Can the SPM connect to an MTP?*
   No. The MTP has its own circuitry inside (EPM) that is similar to the SPM daughter card. Like the SPM it utilizes WQEPM.

9. *Why is the data exported to excel not consistent when it shows up?*
   This is caused by USB "hiccups". WQEPM uses normal priority for data collection, allowing other USB devices to impact the data collection. Lowering the sampling rate can help to fix this issue (though it is PC dependent).
10. *I have used WQEPM in the past and after installing a new version I see two icons. Why?*
    There was a small change in the file path. So downloading the new version of WQEPM no longer overwrites the previous one. It is recommended to delete the previous version so you do not accidently open the wrong file.
11. *My laptop has USB3.0 in it. Will this be supported?*
    We have found that some USB3.0 ports have troubles recognizing the PSOCs. It is best to use a USB 2.0 or earlier port while we continue to test this.

# 12 Legacy Section – Connecting SPMv1 to NanoRiver Boards

The following three figures show how the EPM board and the NRT connector should be connected to each other. As shown in these pictures, the brown wire is always connected to pin 1 on the EPM board (designated by a white dot).

When using SPMv1 it is required to use one of the following 2 source files:

- MSM8960CDPEPMConfiguration.xml
- MSM8930CDPEPMConfiguration.xml

These must be edited to reflect the channels and sense resistors used on the DUT. SPMv1 will not work properly with other ml files.

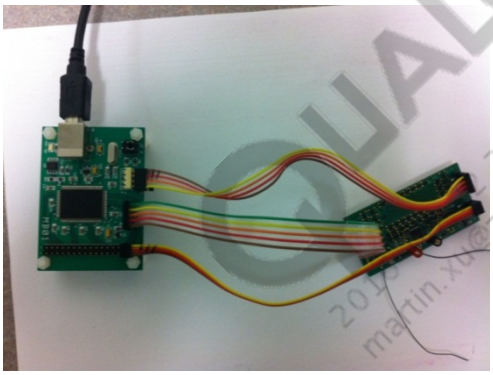


**Figure 12 EPM connected to the NRT connector**

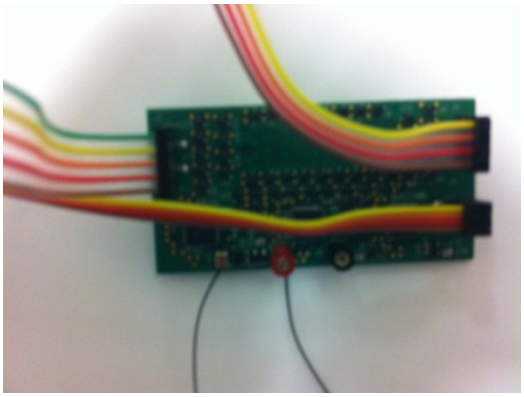


**Figure 13 EPM Connector (brown wire to pin 1)**


**Figure 14 NRT with Miniboard connector**

A similar connection can be made for the NRT ViperBoard. Figure 12 shows a table that highlights the different signals and pins to connect. The ViperBoard increases the sampling rate to 14 kSPS. The same software is used.

| Signal names | SPM (connector – pin number) | NRT card (connector – pin number) | |
|---|---|---|---|
| | | MiniBoard | ViperBoard |
| PWR_MON_ENABLE | J1-4 | X4-4 | X4-1 |
| I2C_ADC_CLK_3.3V | J1-3 | X4-3 | X4-2 |
| I2C_ADC_DAT_3.3V | J1-2 | X4-2 | X4-3 |
| NC | J1-1 | X4-1 | X4-4 |
| ADC1_CS_N (3.3V) | J2-5 | X3-1 | X3-5 |
| EPM_CLK_3P3 | J2-4 | X3-2 | X3-4 |
| EPM_MOSI_3P3 | J2-3 | X3-3 | X3-3 |
| EPM_MISO_3P3 | J2-2 | X3-4 | X3-2 |
| GND | J2-1 | X3-5 | X3-10 |
| ADC3_CS_N (3.3V) | J3-1 | X2-3 | X2-4 |
| ADC2_CS_N (3.3V) | J3-2 | X2-1 | X2-3 |
| EPM_MARKER1_3P3 | J3-3 | X2-2 | X2-7 |
| EPM_MARKER2_3P3 | J3-4 | X2-4 | X2-8 |

**Figure 15 NRT ViperBoard board pinout**

The following images should help in making the connections to the ViperBoard.

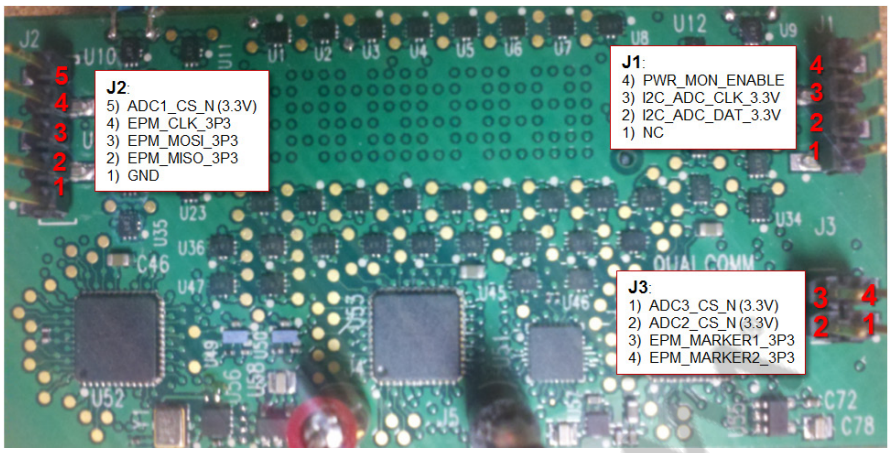



**Figure 16 SPM daughter card pinout**

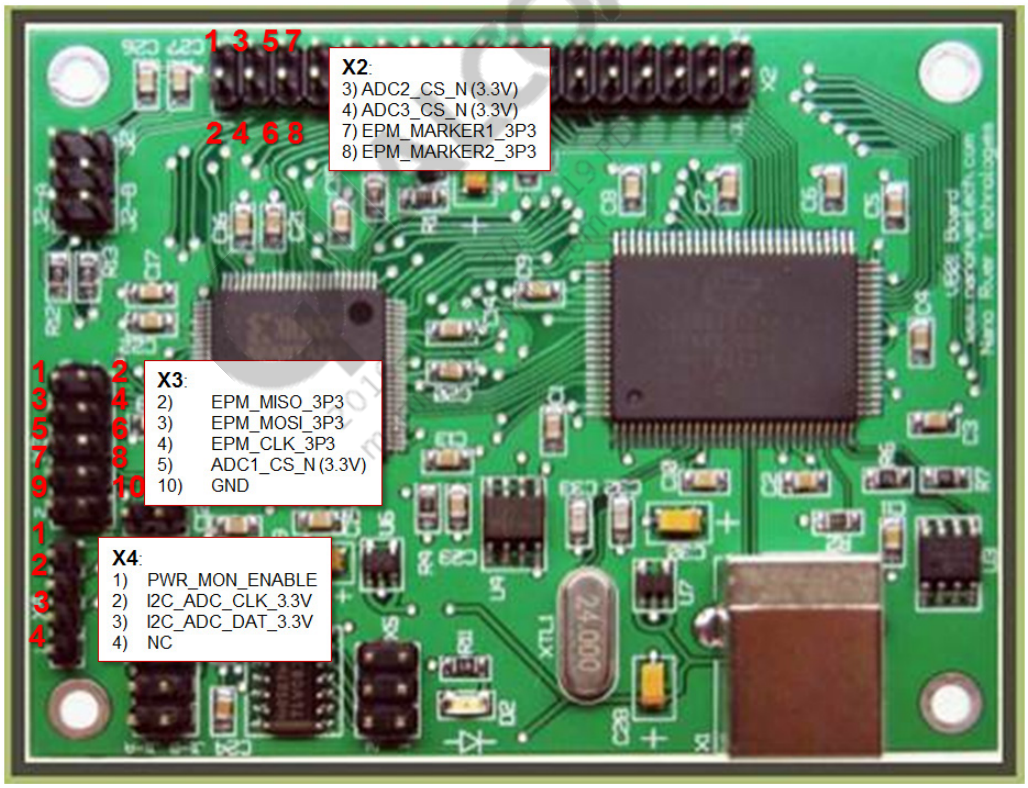



**Figure 17 Viperboard pinout**

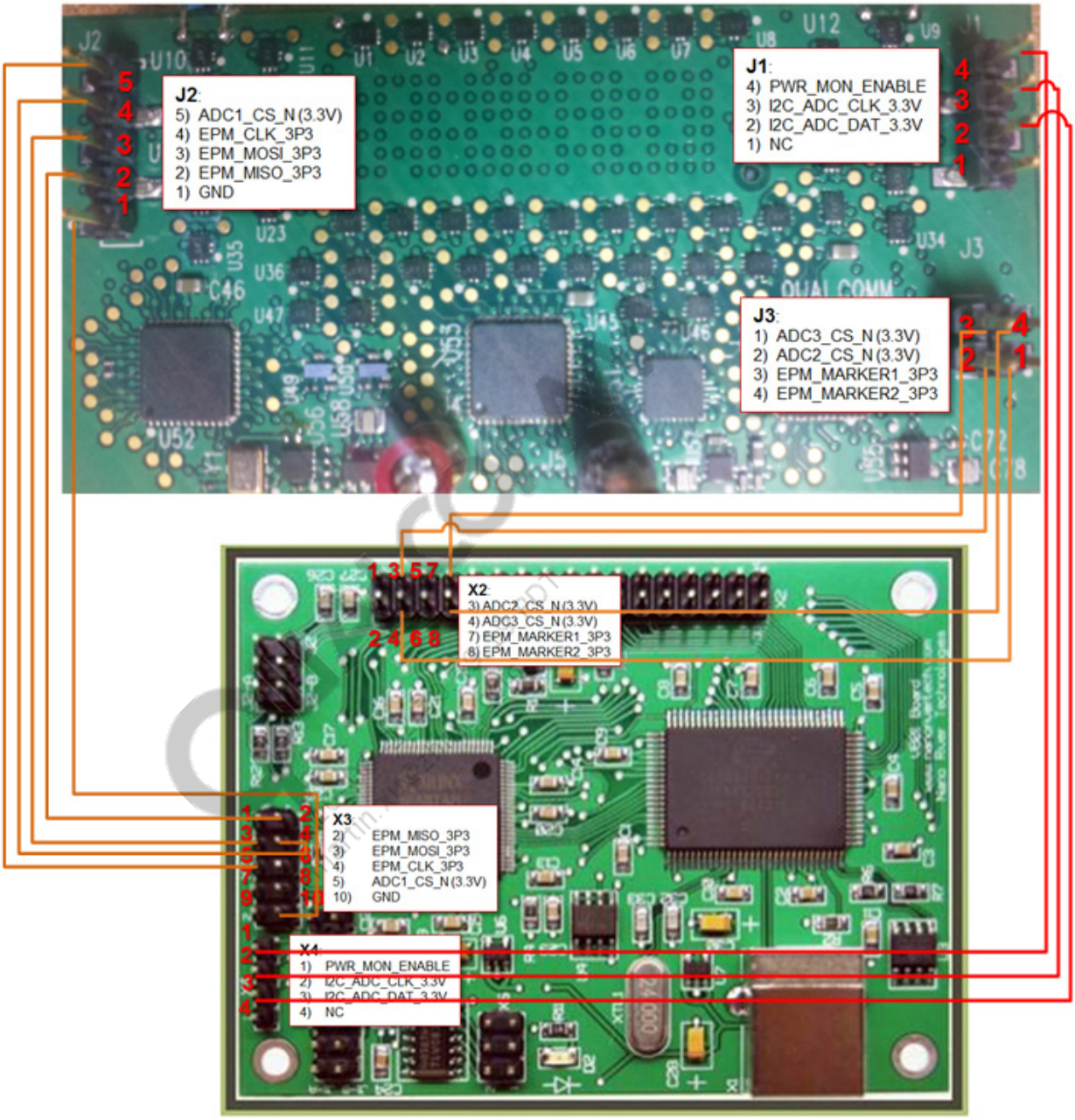



**Figure 18 Viperboard and SPM connections**

**NOTE:** All green channels donate channels that read both current and voltage. This applies to all the chipsets listed in the following sections.

# A MSM8x26 Device: Recommended Channel Assignment

**Table 2 Recommended channel assignment for the MSM8x26 device**

| Channel | Rsense (Ω) | Power rail | PM8921 source | Description | $V_{nom}$ |
|---|---|---|---|---|---|
| 0 | 0.005 | VREG_S1_1P15 | SMPS1 | VDD_USB_CORE, VDD_CORE, VDD_SDC_CDC | 1.15 |
| 1 | 0.005 | VREG_S2_1P05 | SMPS2 | VDD_APC | 1.05 |
| 2 | 0.005 | VBATT | VBATT | VBATT | 3.6 |
| 3 | 0.005 | VPH_PWR | VBATT | VPH_PWR_PMIC | 3.6 |
| 4 | 0.005 | VPH_PWR_RF | VPH_PWR | VPH_PWR_RF | 3.6 |
| 5 | 1 | VDD_WLED | VPH_PWR | Power supply for white LED boost SMPS circuits | 3.6 |
| 6 | 0.07 | VREG_L1_1P225 | LDO1 | VDD_A1 (Power for low voltage analog circuits, GPS ADC and WTR) | 1.225 |
| 7 | 0.05 | VREG_L2_1P2 | LDO2 | VDD_P1 | 1.2 |
| 8 | 0.5 | VREG_L4_1P2 | LDO4 | WCD9306, Power for MIPI_CSI I/Os, MIPI_DSI core circuits | 1.2 |
| 9 | 0.2 | VREG_L5_1P2 | LDO5 | VDD_CORE (CMMB) | 1.2 |
| 10 | 0.1 | VREG_L6_1P8 | LDO6 | VDD_DDR_CORE_1P8, VDD_P4, VDD_P3, WCD9306, NFC | 1.8 |
| 11 | 1 | VREG_L7_1P9 | LDO7 | VDD_A2 | 1.9 |
| 12 | 1 | VREG_L8_1P8 | LDO8 | VDD_PLL2 | 1.8 |
| 13 | 0.1 | VREG_L9_2P05 | LDO9 | Rail goes to WTR1605 | 2.05 |
| 14 | 1 | VREG_L14_2P75 | LDO14 | Rail goes to RF Switches and GPS LNA | 2.75 |
| 15 | 0.2 | VREG_L15_2P8 | LDO15 | LCD1-MIPI and MIPI 12 MP Camera | 2.8 |
| 16 | 0.05 | VREG_L16_3P0 | LDO16 | Rear Camera, WCN FEM, | 3 |
| 17 | 0.2 | VREG_L19_2P8 | LDO19 | Touch Screen, IrDA Sensors, Compass, Gyroscope, Accelerometer, MIPI 12 MP Camera | 2.8 |
| 18 | 1 | VREG_L22_DUAL | LDO22 | VDD_P5 (UIM1 Card) | 1.15 |
| 19 | 0.005 | VREG_S5_1P15 | SMPS5 | VDD_MSS | 1.15 |
| 20 | 1 | VREG_LVS1_1P8 | LDO6 | LVS1 | 1.8 |
| 29 | 0.005 | VREG_S3_1P35 | SMPS3 | To LDO1, LDO2, LDO3, LDO4, LDO5, LDO24 and LDO26 | 1.35 |
| 30 | 0.05 | VREG_L3_1P15 | LDO3 | VDD_EBI0_CDC VDD_PLL1 - Power for low voltage PLL circuits. | 1.15 |
| 31 | 0.005 | VREG_S4_2P1 | SMPS4 | To LDO6, LDO7, LDO8, LDO9, LDO10, LDO11, LDO13, LDO27,WCD9306, | 2.1 |

# B MSM8x30 Device: Recommended Channel Assignment

Note: These resistor sizes were chosen based on the old saturation value of 3 V. This will be updated in a future release.

### Table 3 Recommended channel assignment for the MSM8x30 device

| Channel | Rsense (Ω) | Power rail | PM8038 source | Description | $V_{nom}$ |
|---|---|---|---|---|---|
| 0 | 0.01 | VDD_CORE | S1 | Digital core rail | 1.05 |
| 1 | 0.02 | VDD_MEM | L24 | On-chip memory rail | 1.05 |
| 2 | 0.01 | VBATT | VBATT | Total battery current | 3.6 |
| 3 | 0.01 | WTR0 PA Power | VPH_PWR | WTR0 PA Power | 3.6 |
| 4 | 0.02 | WCN3660 VDD_2P9 | L10 | WCN3660/BT/FM 2P9 | 2.9 |
| 5 | 0.02 | VDD_P1 | L20 | MSM DDR pads | 1.2 |
| 6 | 0.02 | VDD_QDSP6_MSW | L16 | QDSP6 MSW | 1.05 |
| 7 | 0.02 | VDD_QDSP6_MFW | L19 | QDSP6 MFW | 1.05 |
| 8 | 0.05 | VDDP3 | L11 | EBI1 Pads | 1.8 |
| 9 | 0.02 | VDD_QDSP6_APP | L27 | QDSP6 APPS | 1.05 |
| 10 | 0.01 | LCD BKLT DRV | VPH_PWR | Backlight driver | 3.6 |
| 11 | 0.1 | VREG_DISP_2P8 | L8 | MIPI display | 2.8 |
| 12 | 0.05 | TS Ctl VCPIN/Sensor | L9 | 2.85 V for TS and sensors | 2.85 |
| 13 | 0.2 | VDDAL_BBRX_CHx | L1 | BBRX low voltage | 1.3 |
| 14 | 0.1 | MIPI Cam VDIG_1.2V | L12 | 12 megapixel camera 1.2 V | 1.2 |
| 15 | 0.2 | WCD9304 VDDA 1P8 | L11 | WCD9304 VDDRX/TX 1P8 | 1.8 |
| 16 | 0.01 | VBATT Debug | GND | VBATT debug GND | 0 |
| 17 | 0.01 | WTR 1 PA Power | VPH_PWR | WTR 1 PA Power | 3.6 |
| 18 | 0.02 | Total L11 Rail | L11 | L11 total output | 1.8 |
| 19 | 0.1 | VDDAH_BBRX_CHx | L21 | BBRX high voltage | 1.9 |
| 20 | 0.1 | TS Ctl VCPIN/Sensor | LVS2 | 1.8 V for TS and sensors | 1.8 |
| 21 | 0.2 | VDD_UIM1 | L15 | Main UIM card | 1.80/2.95 |
| 22 | 0.2 | VDD_USB_1P8 | L4 | USB MSM IO | 1.8 |
| 23 | 0.05 | WTR0 VDD_1p3 | L1 | WTR1605 device | 1.3 |
| 24 | 0.1 | WTR0 VDD_2P2 | L7 | WTR1605 device | 2.05 |
| 25 | 0.05 | WTR1 VDD_1p3 | L1 | WTR1605L device | 1.3 |
| 26 | 0.1 | WTR1 VDD_2P2 | L7 | WTR1605L device | 2.05 |
| 27 | 0.02 | WCN3660 VDD_1P3 | L1 | WCN3660/BT/FM 1P3 | 1.3 |
| 28 | 0.5 | VDD_GPSADC | L1 | GNSS BBRx | 1.3 |
| 29 | 0.01 | VDD_KR0 | S5 | Krait core 0 | 1.05 |
| 30 | 0.01 | VDD_KR1 | S6 | Krait core 1 | 1.05 |

# C MSM8974 Device: Recommended Channel Assignment

**Table 4 Recommended channel assignment for the MSM8974 device**

| Channel | Rsense (Ω) | Power rail | PM8921 source | Description | $V_{nom}$ |
|---|---|---|---|---|---|
| 0 | 0.002 | PM8841 VREG_S2 | S2 | MSM VDD_CX | 0.9 |
| 1 | 0.002 | PM8841 VREG_KRAIT | KRAIT | All KRAITs | 0.9 |
| 2 | 0.002 | VBATT | VBATT | VBATT | 4.2 |
| 3 | 0.002 | VPH_PWR_RF | VPH_PWR_RF | Power to RFCCA | 4.2 |
| 4 | 0.002 | VBATT_DEBUG | VBATT_DEBUG | VBATT_DEBUG | 4.2 |
| 5 | 0.02 | PM8841 VREG_S1 | S1 | MSM VDD_MX, EBI | 0.95 |
| 6 | 0.07 | PM8941 VREG_L19 | L19 | WCN VDD_2P9V | 2.9 |
| 7 | 0.2 | PM8941 VREG_L18 | L18 | Sensors 2.85V | 2.85 |
| 8 | 0.03 | PM8941 VREG_L1 | L1 | MSM, DDR3, Conn. Card | 1.225 |
| 9 | 0.05 | PM8941 VREG_L4 | L4 | MSM VDDA, WTR VDD | 1.15 |
| 10 | 0.03 | PM8941 VREG_L11 | L11 | MSM VDDA WLAN, WCN | 1.25 |
| 11 | 0.5 | PM8941 VREG_S3 | S3 | VDDPX_3 | 1.8 |
| 12 | 0.03 | PM8941 VREG_S2A | S2A | WCD, LDO's | 2.15 |
| 13 | 0.1 | PM8941 VREG_L12 | L12 | MSM PLL's, MIPI | 1.8 |
| 14 | 0.03 | PM8941 VREG_L15 | L15 | WTR VDD | 2.05 |
| 15 | 0.1 | PM8941 VREG_L14 | L14 | MSM, VDDA | 1.8 |
| 16 | 0.5 | PM8941 VREG_L6 | L6 | MSM USB VDD, WCN | 1.8 |
| 17 | 0.02 | PM8941 VREG_S3A | S3A | MSM, WTR, WCD, LDO's | 1.8 |
| 18 | 0.2 | PM8941 VREG_L16 | L16 | RFswitch, eLNA, QPA, QTF | 2.7 |
| 19 | 1 | PM8941 VREG_LVS1 | LVS1 | Sensors 1.8V | 1.8 |
| 20 | 0.02 | VREG_BOOST_BYP | VREG_BOOST_BYP | Boost/Bypass VPH_PWR | 3.3 |
| 21 | 1 | PM8941 VREG_L24 | L24 | USB_HS1,_HS2 | 3.3 |
| 22 | 1 | PM8941 VREG_L9 | L9 | UIM1 | 2.95 |
| 29 | 0.03 | PM8841 VREG_S3 | S3 | MSM VDD_MSS | 1.15 |
| 30 | 0.01 | PM8841 VREG_S4 | S4 | MSM VDD_GFX | 0.9 |

# D MSM8960 Device: Recommended Channel Assignment

**Table 5 Recommended channel assignment for the MSM8960 device**

| Channel | Rsense (Ω) | Power rail | PM8038 source | Description | $V_{nom}$ |
|---|---|---|---|---|---|
| 0 | 0.02 | VDD_MEM | L24 | On-chip memory rail | 1.05 |
| 1 | 0.01 | VDD_CORE | S3 | Digital core rail | 1.05 |
| 2 | 0.01 | VBATT | VBATT | Total battery current | 4.2 |
| 3 | 0.1 | VDD_P1 | L25 | MSM DDR pads | 1.2 |
| 4 | 0.01 | S1 | S1 | S1 total output | 1.05 |
| 5 | 0.2 | VDD_P3 | S4 | MSM I/O pads | 1.8 |
| 6 | 0.05 | S4 | S4 | S4 total output | 1.8 |
| 7 | 0.2 | VREG_CDC_RXTX | S4 | WCD9310 VDD_Rx/Tx | 1.8 |
| 8 | 0.02 | VDD_QDSP6_APP | L26 | QDSP6 APPS | 1.8 |
| 9 | 0.1 | LCD BKLT DRV | VPH_PWR | Backlight driver | 1.05 |
| 10 | 0.2 | LCD1 MIPI VDD | L8 | MIPI display | 3 |
| 11 | 0.5 | TS Ctl VCPIN/Sensor | L9 | 2.85 V for TP and sensors | 2.8 |
| 12 | 1 | TS Ctl VDD/Sensor | LVS4 | 1.8 V for TP and sensors | 2.85 |
| 13 | 0.2 | MIPI Cam VDIG_1.2V | L12 | 13 megapixel camera 1.2 V | 1.8 |
| 14 | 1 | USBA_USB_HS_1P8 | L4 | USB MSM IO | 1.2 |
| 15 | 0.02 | VDD_QDSP6_MSW | L27 | QDSP6 MSW | 1.8 |
| 16 | 0.02 | VDD_QDSP6_MFW | L28 | QDSP6 MSW | 1.05 |
| 17 | 0.5 | VDDAH_BBRX_CHx | L21 | BBRX high voltage | 1.9 |
| 18 | 0.5 | VDDAL_BBRX_CHx | S2 | BBRX low voltage | 1.3 |
| 19 | 1 | UIM1 Card VDD | L15 | Main UIM card | 1.8/2.95 |
| 20 | 0.1 | RTR0 VDD_1p3 | S2 | RTR8600 device | 1.3 |
| 21 | 0.02 | S2 | S2 | S2 total output | 1.3 |
| 22 | 1 | RTR0 VDD_2p2 | S8 | RTR8600 device | 2.2 |
| 23 | 0.1 | RTR1 SVLTE VDD_1p3 | S2 | RTR8605 device | 1.3 |
| 24 | 1 | RTR1 SVLTE VDD_2p2 | S8 | RTR8605 device | 2.2 |
| 25 | 0.02 | S8 | S8 | S8 total output | 2.2 |
| 26 | 0.1 | WCN3660 VDD_2p9V | L10 | Bluetooth/FM/ WLAN 3.3 V | 2.9 |
| 27 | 0.1 | WCN3660 VDD_1p8V | S4 | Bluetooth/FM/ WLAN 1.3 V | 1.8 |
| 29 | 0.01 | VDD_KR0 | S5 | Krait core 0 | 1.05 |
| 30 | 0.01 | VDD_KR1 | S6 | Krait core 1 | 1.05 |

# E MDM9x15 Device: Recommended Channel Assignment

**Table 6 Recommended channel assignment for the MDM9x15 device**

| Channel | Rsense (Ω) | Power rail | PM8038 source | Description | $V_{nom}$ |
|---|---|---|---|---|---|
| 0 | 0.005 | VDD_CORE | S1 | MDM Digital Core & USB Core | 1.05 |
| 1 | 0.02 | VDD_MEM | L9 | On-chip memory | 1.05 |
| 2 | 0.005 | VOUT_S5 | S5 | Includes the power rails VIN_L10_L11_L12 and VIN_L9 (PMIC inputs to L9, L10, L11 and L12). | 1.15 |
| 3 | 0.02 | VDD_ADSP | L10 | Modem audio digital signal processing circuits | 1.05 |
| 4 | 0.01 | VDD_MDSP_FW | L11 | Modem firmware digital signal processing circuits | 1.05 |
| 5 | 0.01 | VDD_MDSP_SW | L12 | Modem software digital signal processing circuits | 1.05 |
| 6 | 0.01 | VOUT_S2 | S2 | VDD_A1, WCD9310 VDD_TXADC and WLAN | 1.3 |
| 7 | 0.01 | WTR1605 (RF, Dig, GPS 1.3V) | S2 | Primary WTR 1.3V Rail | 1.3 |
| 8 | 0.01 | WTR1605 (RF, Dig, GPS 1.3V) | S2 | Secondary WTR 1.3V Rail | 1.3 |
| 9 | 0.02 | WTR1605 RF (2.0 - 2.2 V) | S4 | Primary WTR 2.0-2.2V Rail | 2.2 |
| 10 | 0.02 | WTR1605 RF (2.0 - 2.2 V) | S4 | Secondary WTR 2.0-2.2V Rail | 2.2 |
| 11 | 0.02 | VDD_A2 | L7 | High voltage analog circuits | 1.85 |
| 12 | 0.005 | VOUT_S3_MISC | S3 | I2C EEPROM, WTR1605 (VDD_MSM_1P8V I/O, GPS,LS), EBI2 NAND D'Card, PMIC VDD_MSM_IO, SPI NOR Memory, JTAG+ DIP Switch pull ups, WLAN VDD_1p8V, WLAN VDD_SDIO_1p8V, WCD 9310 VREG_CDC_RX, WCD9310 VDDA_CDC_TX, WCD9310 VDD_IO, WCD9310 VDD_CP | 1.8 |
| 13 | 0.02 | VDD_P1 | S3 | Digital pad circuits – EBI1 | 1.8 |
| 14 | 0.02 | VDD_DDR (for MDM8215M/9215M/9615M only) | S3 | Stacked LPDDR1 SDRAM core | 1.8 |
| 15 | 0.1 | VDD_P3 | S3 | Digital pad circuits – most digital I/Os | 1.8 |
| 16 | 0.02 | VIN_L8 | S3 | PMIC input to L8 | 1.8 |
| 17 | 0.1 | VIN_L1 | PMIC VPH_PWR | PMIC input to L1 | 3.7 |
| 18 | 0.01 | VPH_PWR | PWR_VBATT | Power to PMIC | 3.7 |

# F MDM9x25 Device: Recommended Channel Assignment

**Table 7 Recommended channel assignment for the MDM9x25 device**

| Channel | Rsense (Ω) | Power rail | PM8038 source | Description | $V_{nom}$ |
|---|---|---|---|---|---|
| 0 | 0.01 | LDO12 | LDO12 | VDD_MODEM | 0.95 |
| 1 | 0.01 | LDO10 | LDO10 | VDD_CORE | 1.05 |
| 2 | 0.005 | VBATT | VBATT | Battery | 3.7 |
| 3 | 0.1 | LDO1 | LDO1 | LVDDA_BBRX | 1.225 |
| 4 | 0.02 | LDO1 | LDO1 | WTR1 | 1.225 |
| 5 | 0.02 | LDO1 | LDO1 | WTR2 | 1.225 |
| 6 | 0.1 | LDO8 | LDO8 | WTR1 | 2.05 |
| 7 | 0.1 | LDO8 | LDO8 | WTR2 | 2.05 |
| 8 | 0.2 | LDO3 | LDO3 | VDD_PLL2/QFPROM_PRG | 1.8 |
| 9 | 0.2 | LDO7 | LDO7 | VDD_A2 | 1.85 |
| 10 | 0.5 | LDO2 | LDO2 | VDD_USB_1P8 | 1.2 |
| 11 | 0.05 | LDO11 | LDO11 | LDO11 | 1.8 |
| 12 | 0.1 | LDO11 | LDO11 | VDD_P3 | 1.8 |
| 13 | 1 | LDO4 | LDO4 | VDD_USB_3P3 | 3.075 |
| 14 | 0.1 | LDO6 | LDO6 | VDD_P4/UIM1 | 1.8 |
| 15 | 0.5 | LDO14 | LDO14 | GPS_LNA | 2.85 |
| 16 | 0.5 | LDO13 | LDO13 | VDD_P2/SDC | 2.85 |
| 29 | 0.01 | SPMS1 | SPMS1 | VDD_MEM | 0.9 |

# G Fusion 3 Device: Recommended Channel Assignment

**Table 8 Recommended channel assignment for the Fusion 3 device**

| Channel | Rsense (Ω) | Power rail | Source | Description | $V_{nom}$ |
|---|---|---|---|---|---|
| 0 | 0.007 | VREG_S5 | PM8921 S5 | Krait core 0 | 1.05 |
| 1 | 0.007 | VREG_S6 | PM8921 S6 | Krait core 1 | 1.05 |
| 2 | 0.005 | VBATT | VBATT | PM8921 battery current | 4.2 |
| 3 | 0.004 | VBATT_DEBUG | VBATT | Total battery current | 4.2 |
| 4 | 0.05 | VREG_L25 | PM8921 L25 | VDD_P1 | 1.8 |
| 5 | 0.05 | VREG_S4 | PM8921 S4 | VDD_P3 | 1.8 |
| 6 | 0.02 | VREG_L26 | PM8921 L26 | VDD_ADSP | 1.05 |
| 7 | 0.01 | VREG_S4 | PM8921 S4 | TOTAL S4 | 1.8 |
| 8 | 0.005 | VREG_S1 | PM8921 S1 | TOTAL S1 | 1.225 |
| 9 | 0.01 | VREG_S3 | PM8921 S3 | TOTAL S3 | 1.05 |
| 10 | 0.2 | VREG_L11 | PM8921 L11 | VDD_DISP | 3 |
| 11 | 0.2 | VREG_L12 | PM8921 L12 | VDD_CAM | 1.2 |
| 12 | 0.05 | VREG_L10 | PM8921 L10 | WCN(BT, FM, WLAN) | 2.9 |
| 13 | 0.1 | VREG_S2 | PM8921 S2 | WCN(BT, FM, WLAN) | 1.3 |
| 14 | 0.02 | VREG_L6 | PM8921 L6 | SD card | 2.95 |
| 15 | 0.02 | VREG_L10 | PM8018 L10 | MDM VDD_ASDP | 1.05 |
| 16 | 0.02 | VREG_L11 | PM8018 L11 | MDM VDD_MDSP_FW | 1.05 |
| 17 | 0.02 | VREG_L12 | PM8018 L12 | MDM VDD_MDSP_SW | 1.05 |
| 18 | 0.1 | SMPS3 | PM8018 SMPS3 | MDM VDD_P1 | 1.8 |
| 19 | 0.2 | SMPS3 | PM8018 SMPS3 | MDM VDD_P3 | 1.8 |
| 20 | 0.02 | SMPS2 | PM8018 SMPS2 | MDM VDD_RF GPS | 1.3 |
| 21 | 0.2 | SMPS4 | PM8018 SMPS4 | MDM VDD_RF | 2.05 |
| 22 | 0.2 | SMPS3 | PM8018 SMPS3 | MDM VDD_RF | 1.8 |
| 23 | 1 | VREG_L8 | PM8018 L8 | MDM VDD_P6 | 1.2 |
| 24 | 0.5 | VREG_L6 | PM8018 L6 | MDM VDD_RUIM | 1.2/2.85 |
| 29 | 0.01 | VREG_S1 | PM8821 S1 | Krait core 2 | 1.05 |
| 30 | 0.01 | VREG_S2 | PM8821 S2 | Krait core 3 | 1.05 |
| 31 | 0.01 | VREG_L24 | PM8921 L24 | VDD_MEM | 1.8 |
| 32 | 0.005 | VREG_S3 | PM8921 S3 | VDD_CORE | 1.05 |
| 33 | 0.01 | SMPS1 | PM8018 | MDM VDD_CORE | 1.05 |
| 34 | 0.01 | VREG_L9 | PM8018 L9 | MDM VDD_MEM | 1.05 |