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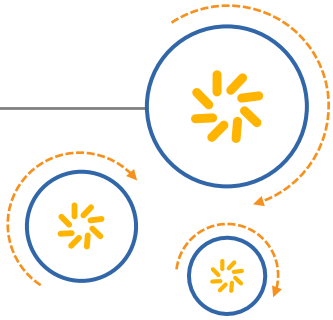

System Power Monitor Version 4

Application Note

80-N6594-16 Rev. E

April 22, 2016

For additonal information or to submit technical questions go to: https://createpoint.qti.qualcomm.com

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Revision history

Revision	Date	Description
A	April 2014	Initial release
B	July 2014	▪ Global: Changed the name of SPM channels to sense inputs; this was done to help clarify the difference between physical measurement channels and software channels used by QEPM ▪ Added a product overview page to the beginning of the document ▪ Added Section 3.6, Low current measurements ▪ Chapter 6, Obtaining an SPM daughter card: Updated the MCN from 20-NJ606-H1 to 30-NJ606-H1.
C	February 2015	Added the following appendices: E MDM9x40, F MSM8992, and G MSM8952
D	May 2015	Added the following appendices: H MSM8956/MSM8976 and I MSM8996
E	April 2016	▪ Chapter 6 Obtaining an SPM daughter card: Updated the MCN number ▪ Section 3.4.1 SPMv4 card SEAM-20-05.0-S-06-2-A connector: Added the MPN information for a SPM compatible connector ▪ Section 3.4.3 Connector on the OEM power breakdown board: Added ▪ Chapter 7 QEPM: Updated the QEPM user guide title to reflect QEPM version 9 ▪ Appendix B APQ8084 + MDM9x25 and Appendix C APQ8084 + MDM9x35: Updated the titles ▪ Appendix I MSM8996: Updated a few R_{sense} values for MSM8996 ▪ Appendix J MSM8998: Added ▪ Appendix K MSM8953: Added

Contents

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Tables

1 Introduction

1.1 Purpose

This application note describes the system power monitor (SPM) version 4 tool. Throughout the remaining parts of this document (and in related documentation) it is referred to as SPMv4 or SPM.

This application note describes the SPM basic specifications, block diagram, application, and briefly mentions the Qualcomm® Embedded Power Monitor (QEPM) software tool.

1.2 Scope

This document is intended for hardware engineers who are responsible for designing a power measurement development board interfacing with SPM. Additionally, this document is to help software/power engineers use SPM and QEPM to measure power.

Users are expected to be familiar with the target device and its underlying chipset.

NOTE: Pay special attention to Chapter 3, as it focuses on proper design techniques for embedded power management.

2 What is SPM

2.1 SPM overview

SPM uses passive current measurement techniques to obtain power numbers for OEM use cases. A sense resistor is (typically) placed on the power rail between the power management IC (PMIC) and the QTI device (MSM™, MDM, APQ, etc.). The SPM measures the voltage drop across the resistor and sends the data to a PC, where QEPM takes the resistor value to display the current. The SPM can also measure the voltage of each rail it is connected to.

2.2 SPMv4

SPMv4, shown in Figure 2-1, is the newest version of the SPM daughter card. While the core concepts of previous versions have been retained, the architecture has been greatly changed. Instead of using op-amps that go to the same analog-to-digital converters (ADCs), each sense input utilizes a dedicated low-voltage ADC, and sends the data over a digital signal instead of an analog signal to the programmable system-on-a-chip (PSoC). The PSoC still sends the data via USB to the host computer. The 120-pin Samtech connector used for SPMv3 is being used for SPMv4.

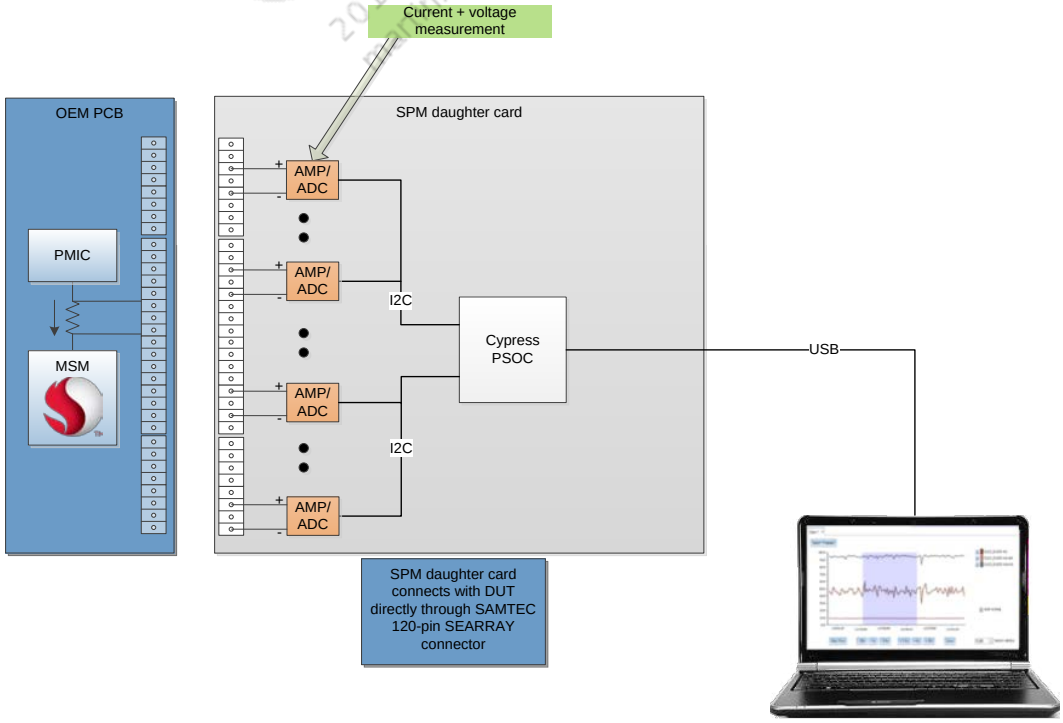


Figure 2-1 SPMv4

3 Designing an SPM-ready board

NOTE: Proper design techniques are the most critical aspect of obtaining accurate measurements when using SPM. Poor layout designs result in problems on the target device when using SPM. Closely study the following information before performing any board design.

3.1 Current sense resistor

Selection and placement of the current sense resistor is the most critical aspect of the target power measurement circuitry. The current sense resistor is a very low impedance resistor that sits in series between the power supply and the load to be measured. The following are some rules and recommendations for the selection, placement, and routing for current sense resistors and associated PCB traces.

- Choose the largest value of the sense resistor up to the value in Table 3-1 for each rail to assure the best low-current accuracy.
- Choose a value of the sense resistor such that, at maximum current, the peak I × R drop across the sense resistor is less than 100 mV and the steady state I × R drop is less than 81 mV. Table 3-1 provides guidance on resistor selection based on the maximum current drawn for maximum accuracy. Any voltage drops over 81 mV is clamped by the ADC.
- While the appendices show what resistors are used on some modem test platform (MTP) power rails, the designer is responsible for calculating resistor values for all other rails. It is strongly recommended to look at the respective chipset power grid to see the maximum theoretical current drawn by each power domain and decide based on that.
- While maximum accuracy is achieved with larger sense resistor, it is important to ensure that the voltage level does not drop below the target device minimum operating voltage. Minimum operating voltage and typical PMIC rail settings can be found in the chipset's device specification.

Table 3-1 Current sense resistor

Resistor value	Resistor wattage	Resistor type	Minimum current (mA) [1]	Maximum current (mA)
1	0.1	Film	0.1	100
0.8	0.1	Film	0.2	125
0.5	0.1	Film	0.3	200
0.2	0.1	Film	0.6	500
0.1	0.1	Film	1.3	1000
0.05	0.1	Film	2.5	1414
0.04	0.1	Film	3.1	1581

Resistor value	Resistor wattage	Resistor type	Minimum current (mA) [1]	Maximum current (mA)
0.02	0.1	Film	6.3	2236
0.015	0.1	Film	8.3	2582
0.01	0.1	Film	12.5	3162
0.008	0.1	Film	15.6	3536
0.005	0.1	Film	25.0	4472
0.02	1	Kelvin	6.3	5000
0.015	1	Kelvin	8.3	6667
0.01	1	Kelvin	12.5	10000
0.008[2]	1	Kelvin	15.6	11180
0.005[2]	1	Kelvin	25.0	14142

1. Expected minimum current to get ±2% accuracy with optimal routing.
2. For accuracy reasons, it is strongly recommended not to use resistors under 10 mΩ.

- Choose a Kelvin-type sense resistor with a 1% accuracy for maximum currents greater than 3 A (2 A if there is board space).
  - Example: CYNTEC Co. Ltd 1 W, 0612, 4-terminal, low-resistance chip resistor part RL1632L4-R010-FNH-39 0.010 Ω, 1 W resistor is suitable for a rail with a maximum current of 10 A and a minimum measurable current of 10 mA.
- Choose a power metal strip resistor, low value, surface mount resistor with a 1% accuracy for maximum currents less than 3 A.
  - Example: Vishey/Dale WSL0603R0200FEA is a 0.020 Ω 0603 1% 0.1 W resistor that is suitable for a rail with a maximum current of 1 A and a minimum measurable current of 0.5 mA.
- For power rails supplied by a switched-mode power supply (SMPS), place the SPM sense resistor inside the feedback loop but after the inductor. It is strongly recommended to keep these resistors at 10 mΩ, since the feedback loops have a maximum resistance tolerance, and poor PDN routing (in the loop) with too large of a sense resistor can affect SMPS stability.

3.2 Sense current differential pair routing

For all sense current differential pairs, it is essential to minimize the differential parasitic resistances due to PCB traces and vias. The differential parasitic resistances must be minimized such that it is no more than 5% of the SPM sense resistor value.

- Example: If the sense resistor is 10 mΩ, the difference between the positive side current sense trace and the negative side current sense trace must be less than 500 μΩ; this equates to a differential trace length difference of 3 mil for a 4 mil wide trace on ½ oz. copper.

Route sense current traces as high speed differential pair from sense resistor to the SPMv4 connector. Since the voltage differential between the SPM sense resistor pair can be as little as 25 μV, it is essential to avoid all differential crosstalk.

- Separate differential pair from any coplaner trace by a minimum of three times the distance between the trace and the nearest ground plane.
- Run non-coplaner traces not separated by a ground plane orthogonal to the differential pair.

- Avoid routing differential pairs near noise sources such as oscillators, crystals, or power inductors.
- When changing layers, place vias associated with differential pair next to each other.

The goal is to reduce the amount of differential crosstalk on the SPM sense resistor traces. Common mode noise is filtered.

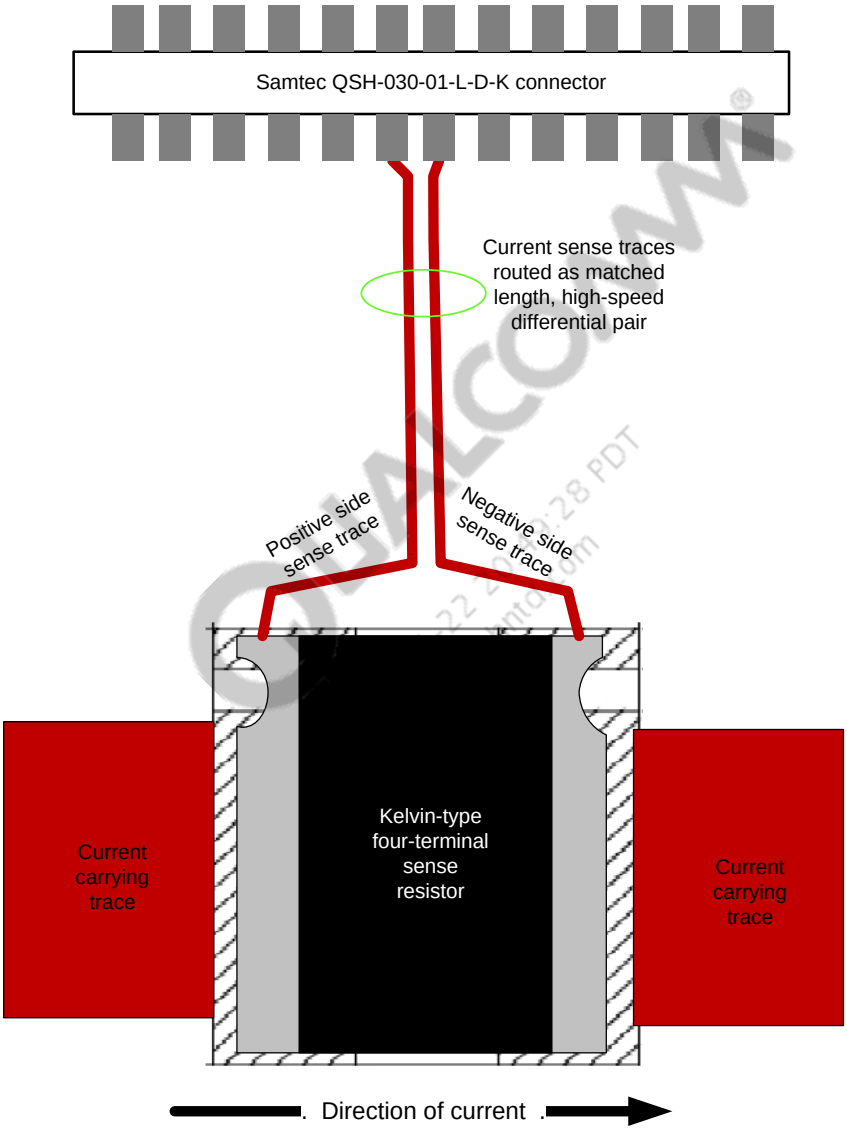


Figure 3-1 Sense trace routing guidelines

3.3 Additional design issues

- All SPM current measurements must be on the forward current path. Do not attempt to measure the return current path.
- Do not place multiple current sense resistors in series

- If multiple loads are driven by a single rail and these loads need to be measured independently, place the sense resistors in parallel as shown in Figure 3-2.

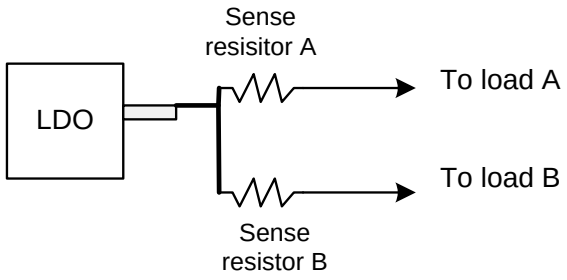


Figure 3-2 Sense resistors in parallel

- Measurement of rails with a maximum current less than 250 µA is not practical due to the limits of the noise floor and the size of the sense resistor needed.

If current measurements are being made to a subset of the load on a rail, make sure that there is no hidden electrical path between the unmeasured portion of the rail and the measured portion of the rail. This is particularly important for the case where a rail is used to power different circuits within the same device or subsystem. See Figure 3-3 for details.

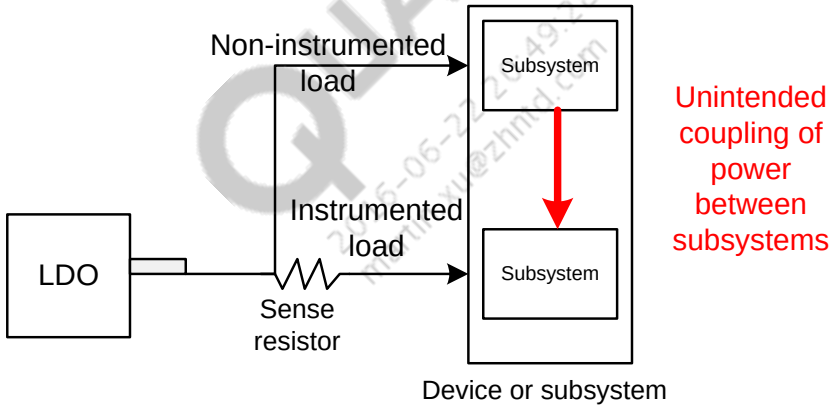


Figure 3-3 Unintended coupling of power between subsystems

3.4 Connectors

3.4.1 SPMv4 card SEAM-20-05.0-S-06-2-A connector

The SPMv4 card connector, shown in Figure 3-4, provides a sufficient interconnect to measure the voltage and current on up to 48 rails concurrently. Additionally, this connector allows for two EPM_Markers for time synchronization between the MSM device and QEPM software, an interrupt for communication back to the MSM device from QEPM, and the ability to monitor the state of the CXO_EN signal to the MSM device. The four signals are optional for power breakdown measurement.

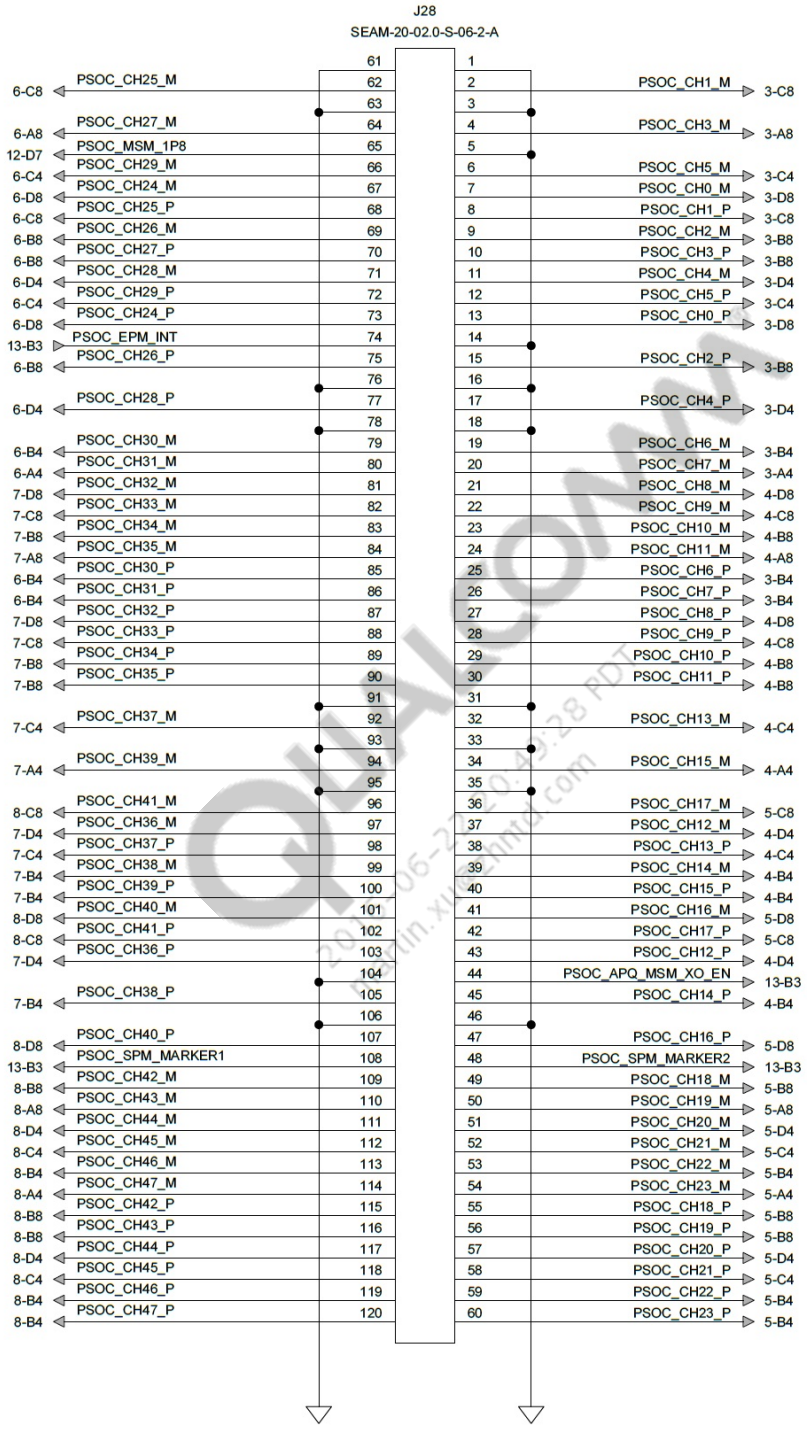


Figure 3-4 SPMv4 card connector

- For all current sense inputs, route the sense resistors differential pair to the _P and _M of each sense input.
- PSOC_SPM_MARKER[1:2] are LVCMOS18 level signals from the MSM device to the QEPM software. These signals can be used by the processor to time synchronize processor events with current rail measurement and are typically routed to GPIO pins of the MSM device (or MDM, APQ, etc.).
- PSOC_XO_OUT_EN is a LVCMOS18 level signal that is an input to the PSoC on the SPMv4 card and is used by QEPM software to verify the target is in XO shutdown.
- PSOC_SPM_INT is an LVCMOS18 level signal that is an output of the PSoC on the SPMv4 card and is used by the QEPM software to generate an interrupt to the MSM device. This signal is typically routed to a GPIO pin on the MSM device.
- When assigning sense inputs, if you assign them in contiguous order, you will take the greatest advantage of the parallel I^2C buses, maximizing your effective sampling rate.

3.4.2 SPMv4 connector pin map

There are different ways that the CAD pinout is represented on the schematic. Figure 3-5 and Figure 3-6 show two possible pinouts. Ensure that the pinout corresponds correctly to the SPM connector pin map shown Figure 3-7.

120	114	108	102	96	90	84	78	72	66	60	54	48	42	36	30	24	18	12	6	
47+	47-	EM1	41+	41-	35+	35-	GND	29+	29-	23+	23-	EM2	17+	17-	11+	11-	GND	5+	5-	6
46+	46-	40+	40-	GND	34+	34-	28+	28-	1.8V	22+	22-	16+	16-	GND	10+	10-	4+	4-	GND	5
45+	45-	GND	39+	39-	33+	33-	GND	27+	27-	21+	21-	GND	15+	15-	9+	9-	GND	3+	3-	4
44+	44-	38+	38-	GND	32+	32-	26+	26-	GND	20+	20-	14+	14-	GND	8+	8-	2+	2-	GND	3
43+	43-	GND	37+	37-	31+	31-	INT	25+	25-	19+	19-	XO_OUT	13+	13-	7+	7-	GND	1+	1-	2
42+	42-	36+	36-	GND	30+	30-	24+	24-	GND	18+	18-	12+	12-	GND	6+	6-	0+	0-	GND	1
115	109	103	97	91	85	79	73	67	61	55	49	43	37	31	25	19	13	7	1	

Figure 3-5 Pinout example 1

120	114	108	102	96	90	84	78	72	66	60	54	48	42	36	30	24	18	12	6	
120	114	EM1	102	96	90	84	78	72	66	60	54	EM2	42	36	30	24	18	12	6	6
119	113	107	101	95	89	83	77	71	1.8V	59	53	47	41	35	29	23	17	11	5	5
118	112	106	100	94	88	82	76	70	64	58	52	46	40	34	28	22	16	10	4	4
117	111	105	99	93	87	81	75	69	63	57	51	45	39	33	27	21	15	9	3	3
116	110	104	98	92	86	80	INT	68	62	56	50	XO_OUT	38	32	26	20	14	8	2	2
115	109	103	97	91	85	79	73	67	61	55	49	43	37	31	25	19	13	7	1	1

Figure 3-6 Pinout example 2

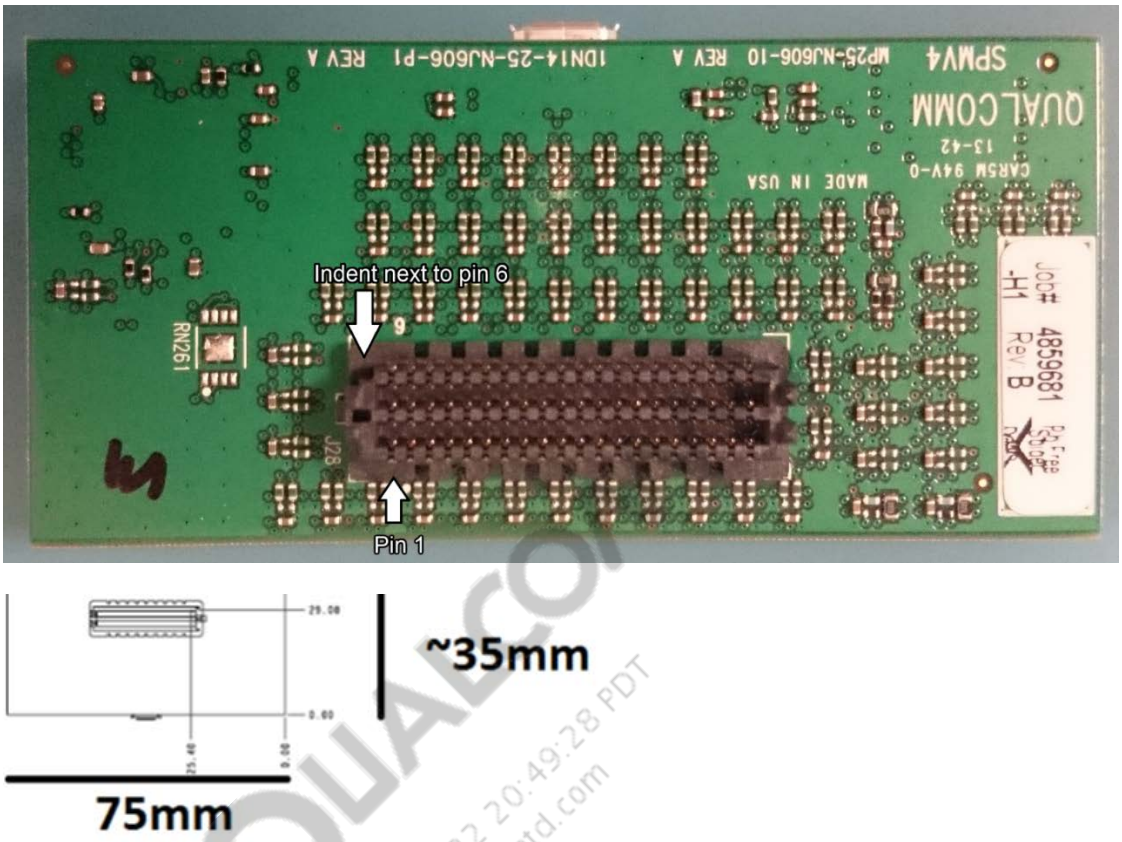


Figure 3-7 SPM connector pin map

3.4.3 Connector on the OEM power breakdown board

To support an SPMv4 card, the connector with part number SEAF-20-05.0-S-06-2-A (or an equivalent connector) should be installed on the OEM power breakdown board.

3.5 Measuring voltage sense inputs

Unlike SPMv3, which was limited to 14 sense inputs for voltage measurement, all sense inputs on SPMv4 can measure voltages up to 28 V. This includes V_{Batt} measurements.

3.6 Low-current measurements

While it is possible to measure very low currents on SPMv4, it is important that expectations match what can be accomplished. Due to the high current draw that is experienced from major rails like core, CPU, GFX, etc., a small sense resistor (typically 10 mΩ) is needed to make sure that the voltage drop on the rail is not too high or that the SMPS loop does not become unstable. This can create an accuracy problem when these same rails are needed to measure a very low current.

The following are examples of how this limitation arises. For all examples, 2.5 µV is used as the least significant bit (LSB).

Example 1 – 10 mΩ resistor, 1 mA current

In this example, the voltage drop across the sense resistor would be 10 µV or exactly 4 LSB. Assuming no noise on the system, the SPM would read this as 10 µV and would output it as 1 mA on QEPM for 0% error.

Example 2 – 10 mΩ resistor, 0.80 mA current

In this example, the voltage drop across the sense resistor would be 8 µV or 3.2 LSB. Assuming no noise on the system, the SPM would read this as 10 µV and would output it as 1.00 mA on QEPM for 25% error.

Examples 1 and 2 describe how a slight difference of current while measuring low currents with a small sense resistor can create a massive error, simply due to the LSB of the system.

Another source of low current error is generated due to an additional current path on the "-" line, needed to accurately measure the voltage. This current is equal to

$$\frac{Vrail}{830\ k}$$

For a 0.9 V, rail this means the "-" line will sink an additional 1.1 µA of current over the "+" line. If these lines are exceptionally long on the device under test (DUT), it is possible to see resistances up to 1 Ω. This would increase the voltage delta between the two inputs by 1.1 µV, which may create an error of 1 LSB. Under most use cases, this is insignificant, but as shown in example 2, at very low currents, 1 LSB can create significant error.

At higher voltages (e.g., 3.3 V → 4 µA), a longer line guarantees at least 1 LSB error.

Finally, an error can be seen due to noise that is coupled onto one line, but not the other. By properly routing each lane, this can be minimized, but it is essentially impossible to eliminate all possibilities of noise as the traces traverse layers, vias, and connectors. While a 5 µV noise spike seen on one line would be negligible in most situations, 2 LSBs can add significant error in low current measurements.

Any voltage drops across the sense resistor that are 25 µV or less have strong potential to see errors of at least 10% (1 LSB at 25 µV). Be careful when measuring values this low.

4 SPMv4 specifications

The SPMv4 specifications are listed in Table 4-1.

- DC offset calibration is not required.
- The SPM circuitry only supports external access through QEPM 5.0 (or later) on the PC.
- Four GPIO pins are dedicated for software triggering.

Table 4-1 SPMv4 specifications

Parameters	Minimum	Typical	Maximum	Unit
Normal operation accuracy	-2	–	2	%
High frequency dynamic measurement [1]	-6	–	6	%
Rock bottom sleep current accuracy [1]	-6	–	6	%
ADC sampling rate [2]	–	7.14	–	ksps
Current/voltage sense inputs [3]	–	48	64	–
ADC resolution (current)	–	16	–	Bits (signed)
ADC resolution (voltage)	–	15	–	Bits (unsigned)
Current range	-81.92	–	81.92	mV/R_{sense}
Current range LSB	–	2.5	–	$\mu V/R_{sense}$
Voltage range	0	–	28	V
Voltage range LSB	–	1.25	–	mV

1. Most use cases will not use this specification. This is for very low current and very high frequency use cases.
2. This is for up to six sense inputs. Beyond that, use the following formula to measure rate (45.454 kHz/NEXT_EVEN#_SENSEINPUTS). For example, for 11 or 12 sense inputs, the rate would be 45.454 kHz/12 = 3.79 kHz
3. There are 48 sense inputs to be connected to the DUT via the Samtech connector. There are an additional 16 sense inputs on the board. See Chapter 5 for more information.

5 Additional sense inputs and features

In addition to the 48 sense inputs used for DUT current and voltage measurements, there are an additional 16 sense inputs used for debug and extra measurement sense inputs. There are three different types of additional sense inputs.

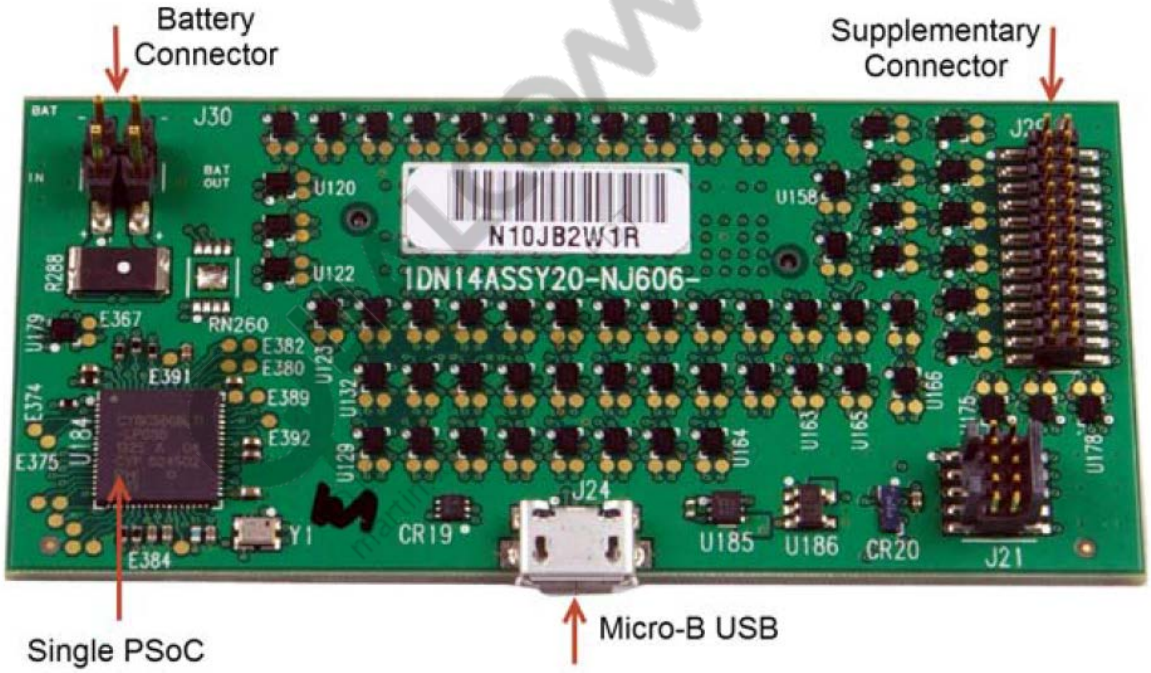


Figure 5-1 SPM front

5.1 Sanity check sense inputs

There are four sense inputs used exclusively to test SPM functionality. These ADCs have no access to them via a connector. These sense inputs should always have the same voltage/current readings (within error) listed in Table 5-1.

Table 5-1 Sanity check sense inputs

Sense inputs	Current (mA)	(V)
CH48	1.001	0.807
CH49	10.122	1.012
CH50	4.995	1.491
CH51	0.501519	1.790

5.2 Additional supplementary sense inputs

There are 11 additional sense inputs that can be used to measure current and voltage by connecting cables to the 26-pin connector (J29) on the right side of the SPMv4. These sense inputs work the same way as the main 48 sense inputs, but can be used with a device that does not have an SPM connector. It is strongly recommended that when connecting cables, to connect them as a twisted pair of equal lengths. It is recommended to use Samtec FFTP-13-D-##.##-01-N where ##.## specifies one of three lengths.

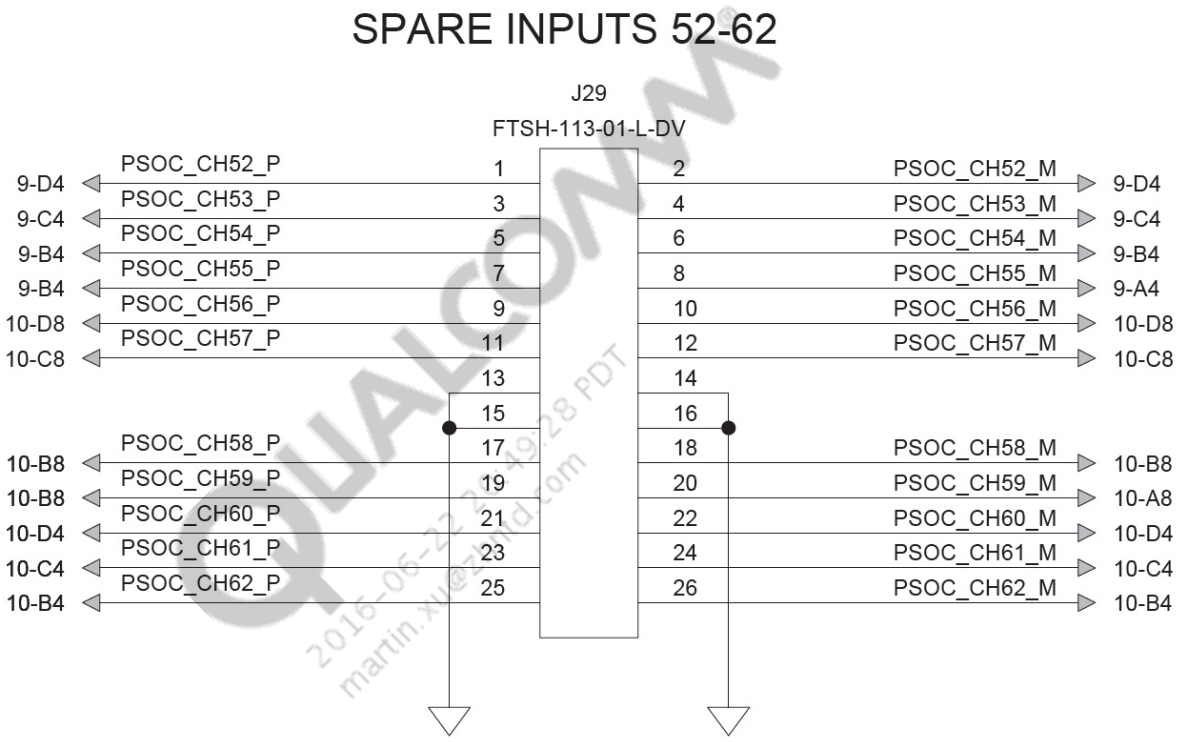


Figure 5-2 Spare connector

5.3 V_{Batt} measurement

There is an additional sense input that is meant to intercept the battery for devices that do not have a sense resistor on the DUT. A 20 mΩ resistor is used here. See Figure 5-3 for an illustration of how to connect to J30.

NOTE: This trace can only handle battery currents up to 4 A. Any higher current may permanently break the SPMv4.

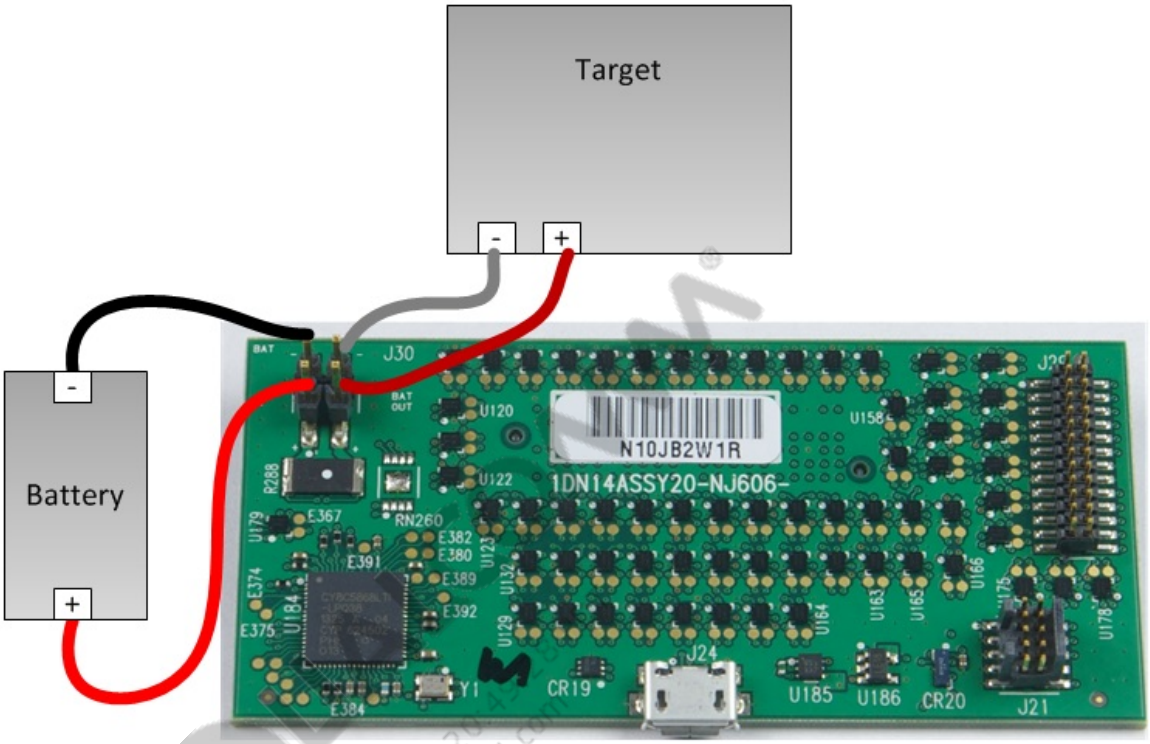


Figure 5-3 Battery connection

6 Obtaining an SPM daughter card

The SPM daughter card can be purchased from the Qualcomm Sales and Support Center https://cp.qti.qualcomm.com.

To order a daughter card, select *SPM4-PowerMonitoringTool* in the SPM section – MCN 30-NJ606-1.

To order a daughter card with the SPM/MTP interposer card, select *SPM4-RCM-Interposer* – MCN 65-NJ606-1.

7 QEPM

7.1 Overview

QEPM is a Windows and Linux application which allows a user to monitor and analyze measurement data for any of the supported measurement points in an EPM-supported target device from a web browser. QEPM 5.0 (and later) is the software that is used alongside SPMv4.

The QEPM application is typically used to assess the impact on power after new or updated software (e.g., device driver, applications, or other software) has been added to the power monitoring device environment. QEPM now supports multiple devices connecting to PC.

The user of the QEPM application would normally compare new results for measurement points to known results before the updated software was applied to the target device environment. The QEPM application allows power differences for these measurement points to be observed.

The QEPM application is a web-based service, and supports three types of interfaces:

- The QEPM browser user interface from a local or a remote browser to the application platform with the QEPM server/data manager application installation
- The shared QEPM Browser User Interface from a browser remote to the application platform with the QEPM server/data manager application installation
- Client scripts from any common network accessible computer using QEPM automation interfaces

The results can be viewed and analyzed on any web-enabled device with any of the following browsers:

- Chrome
- Firefox
- Safari

For full details on QEPM, including installation, see the *Qualcomm Embedded Power Monitor Version 9 User Guide* (80-NH746-1). It can be obtained by opening a Salesforce case at https://createpoint.qti.qualcomm.com.

- Case Type: Hardware
- Problem Area 1: System Power
- Problem Area 2: Other (System Power)

7.2 Obtaining QEPM

Open a Salesforce case at https://createpoint.qti.qualcomm.com for QEPM (HK11-NH758-1).

- Case Type: Hardware
- Problem Area 1: System Power
- Problem Area 2: Other (System Power)

Be sure to specify that you are looking for the latest version of QEPM in the subject line.

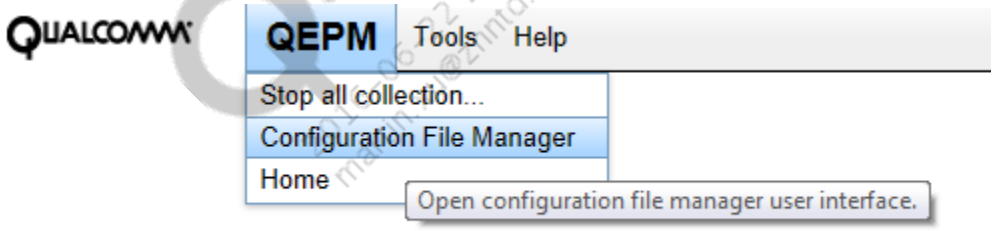
7.3 Configuring your device for QEPM

QEPM must know the resistance used to calculate the current on each sense input. In previous installments of (W)QEPM, this was done by using an XML configuration file. This is now done directly within the QEPM program using the configuration file manager.

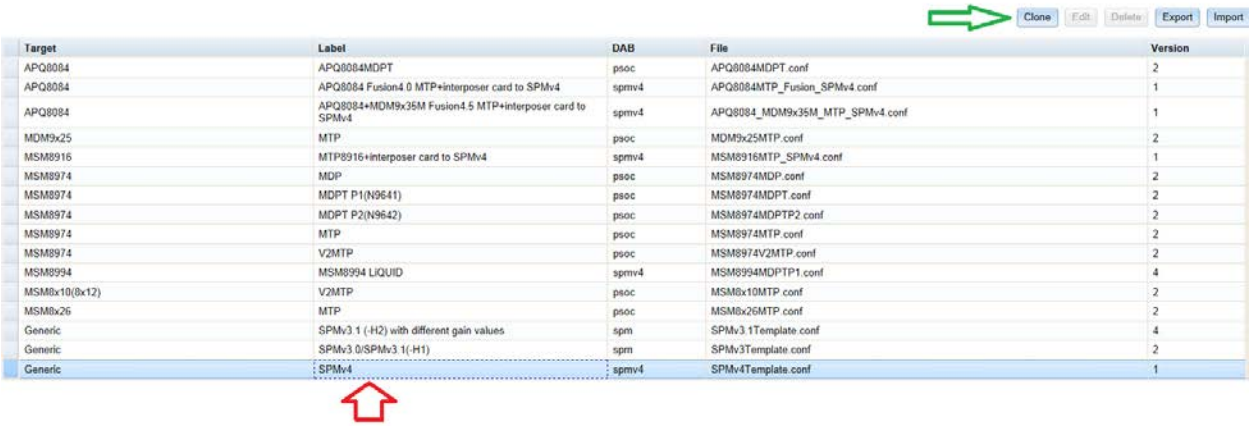
NOTE: The SPMv4 configuration file for QEPM 5.0 is preliminary and will be updated to be made easier in future releases. This section will be updated then.

NOTE: Click **Save** to avoid losing any updates made. It is **strongly** recommended to click save frequently.

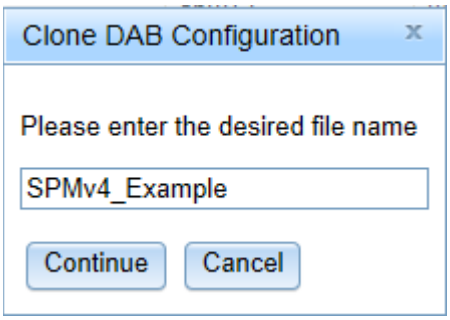
1. Select QEPM → Configuration File Manager.



2. Select the generic SPMv4 configuration file and then click **Clone**.



3. Type a descriptive title (no spaces allowed).



4. The configuration file is set up to be generic initially. Many cells are holdovers from older versions of EPM/SPM and should not be changed when working on SPMv4. These will be in orange below. This will be updated with the next release of QEPM.

Channel	Name	Type	Gain	Resistor	Voltage	Power Coupling
	Category	Description				
0, 0	CH0_SPM_I	Current	1	1000	1.2	CH0_SPM_V
	Category1	Description				
0, 1	CH0_SPM_V	Voltage	1	1000		
	Category1	Description				

Channel – The channel column (in blue above), corresponds to the I^2C numbering and not the physical sense input names given in Section 3.4.2.

Name (current) - The default name has the channel corresponding to the SPM sense inputs in Section 3.4.2. For example, CH0_SPM_I is the current channel that is connected through pins 7 and 13 on the Samtech connector.

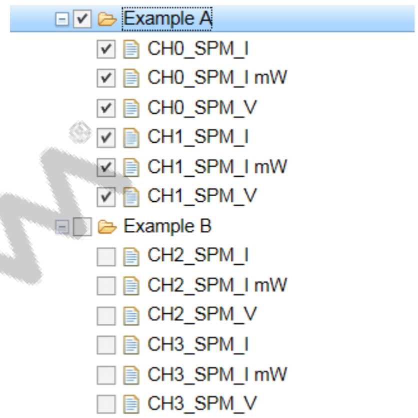
NOTE: It is **strongly** recommended that when changing the name, retain CH# as the prefix to avoid confusion.

Name (voltage) - The default name has the channel corresponding to the SPM sense inputs in Section 3.4.2. For example, CH0_SPM_V is the voltage channel that is connected through pins 7 and 13 on the Samtech connector.

NOTE: It is **strongly** recommended that when changing the name, retain CH# as the prefix to avoid confusion.

Category – Used to group certain sense inputs together while running simulations. The default category separates the sense inputs based off of the types available in Chapter 5. This section groups sense inputs together with the same category name.

Name	Category
CH0_SPM_I	Example A
CH0_SPM_V	Example A
CH1_SPM_I	Example A
CH1_SPM_V	Example A
CH2_SPM_I	Example B
CH2_SPM_V	Example B
CH3_SPM_I	Example B
CH3_SPM_V	Example B



Configuration file category example **How category affects QEPM**

Type – Describes what type of sense input is being used. The options are current, voltage, GPIO, and disabled. Since this is hardwired into SPMv4, these should not be adjusted.

Description – Used to add a description on the sense input for user clarity.

Gain – Legacy value from when SPMv3 used on board op-amps. Adjusting this will give false readings.

Resistor (current) – Value of R_{sense} used on the DUT in mΩ.

Resistor (voltage) – Should always be 1000.

Voltage – Legacy value from SPMv3 when not all sense inputs have voltage readings.

Power coupling – Used to let QEPM know from which voltage channel it should multiply the results to get power.

5. Using an example, where sense input 0 (SPM pins 7 and 13) is connected to a 10 mΩ R_{sense} on VDD_CORE. The first two rows should look like the following.

Channel	Name Category	Type Description	Gain	Resistor	Voltage	Power Coupling
0, 0	CH0_VDD_CORE_I High Current Rails	Current MSM Core Power	1	10	1.2	CH0_VDD_CORE_V
0, 1	CH0_VDD_CORE_V High Current Rails	Voltage MSM Core Power (V)	1	1000		

8 Running simulations

The following section is a quick overview on the basics of measuring power rails. For complete details on all QEPM features, refer to the *Qualcomm Embedded Power Monitor Version 5 User Guide* (80-NH746-1):

1. Connect your SPMv4 (up to six SPMv4) via USB.
   a. If this is the first time you are using this daughter card on your computer, allow the OS at least 15 seconds to install the drivers.
   b. If you are unable to install the drivers, try unplugging and re-plugging in the drivers.
   c. If the driver installation is still unsuccessful, confirm that automatic driver download is enabled in the system settings.
      i In the Control Panel, select **System → Advanced system settings** (select the **Yes** option).
      ii In the System Properties dialog, select the **Hardware** tab and **Device Installation Settings**.
      iii In the Device Installation Settings dialog, check to see if the No option is selected.
      iv If No is selected, click **Yes, do this automatically** (recommended).
      v Click **Save Changes** so the Yes option is applied.
      vi Unplug and plug in the USB cable to the SPMv4 board. Wait a few minutes until the automatic driver installation is complete.
2. Start the QEPM software.
3. Double-click the QEPM icon shown in Figure 8-1.

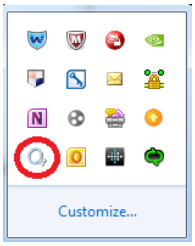


Figure 8-1 QEPM icon

   If your browser cannot load the page, try reloading the browser page.
4. Click the **QEPM** tab at the top of the Configuration File Manager.

   a. Since QEPM is being used on multiple MTPs, this page holds all of the configuration files.

5. Highlight the SPMv4Template and click **Clone.**
6. Type in your configuration file name as described in Section 7.3.
   a. This only needs to be done the first time. For subsequent times, this configuration file can be selected.
7. Click **Save**.
8. Click **Setup**.
9. Click **Probe**. Click **Continue**.
   a. If this fails, read the instructions on the QEPM. Typically you need to disconnect and reconnect the SPMv4.
10. After the device has been recognized, choose the chip and configuration file that you set up in step 6 and click **Save**. You are now ready to do measurements.
11. Click Live View.
12. Click **+** for the folder that corresponds to the DAB you set up while probing.
13. Continue to open the folders that you are interested in. They are grouped by category, which you can change in the configuration file (default is all measurement sense inputs in Category 1).
14. Select the sense inputs you want to measure. If you choose over seven different sense inputs, your bandwidth will start to decrease.
15. Click **Apply**.
16. Click **Start** to start running measurements.

Appendices

The following appendices are used as a guide to show how sense inputs should be configured if the goal of the designer is to be able to use the same SPMv4 to measure a sense inputs on their DUT that will use the same ADC part while measuring on the MTP. The purpose of this exercise is to compare MTP results to DUT results with as many variables eliminated as possible. Since both rails are measured using the same ADC, any delta would be the result of software/hardware differences between the two devices as well as resistor tolerance and SPM layout differences. This includes deltas that can arise from the same part due to process variation. Even with the exact same setup, it is not expected that SPMv4 yields the exact same results going from device to device.

Many times, the MTP does not focus as much on the major rails and may focus on areas like camera rail power, which may not be useful to the designer. This can vary on every chipset, and just because a certain rail was measured on one MTP, it does not guarantee it will be measured on another MTP.

None of these recommendations are required, and the designer has full control on which rails they want to measure and the size of the sense resistor used as long as they follow the rules outlined in Section 3.

As new chipsets are released, these appendices will be updated.

A MDM9x30

Sense inputs	R_{sense} (mΩ)	Power rail	PMIC regulator	Description
2	10	VBATT	VBATT	Total battery current
4	10	VBATT_RFPA	VPH_PWR	VPH_PWR going to RF card
5	1000	VREG_L10_3P075	VREG_L10	HS_USB
6	1000	VREG_L12_2P7	VREG_L12	GPS_LNA, QFE
7	10	VREG_S3_1P0	VREG_S3	Total S3 power
8	25	VREG_RF_1P0_CONN	VREG_L9	WTR
10	10	VREG_S1_0P9	VREG_S1	VDD_MODEM
11	10	VREG_S3_1P0	VREG_S3	VDD_MEM power
12	100	VREG_L4_L16_0P95	VREG_L4_16	ANALOG PCIE, USBSS
13	25	VREG_S2_1P225	VREG_S2	Total S2 power
14	10	VREG_L3_0P9	VREG_L3	VDD_CORE
15	200	VREG_L5_1P7	VREG_L5	VDD_A2
16	100	VREG_L1_1P15	VREG_L1	VDD_A1, WCD DAC
17	1000	VDD_XO_RF	VPH_PWR	XO, RFCLK
19	100	VREG_L2_1P2	VREG_L2	EBI MDM pads only
21	1000	VREG_L6_1P8	VREG_L6	LPDDR2 VDD1 pads only
23	200	VREG_L8_1P8	VREG_L8	USB, PCIE
25	10	VREG_S4_1P85	VREG_S4	Total S4 power
27	50	VREG_L2_1P2	VREG_L2	LPDDR2 VDD2 pads only
41	50	VREG_RF_1P8_WTR0_CONN2	VREG_S4	RF 1P8 power
43	200	VREG_L6_1P8	VREG_L6	Input to VDD_P3 only
44	1000	VREG_L14_2P85	VREG_L14	SDC pads
45	1000	VREG_L7_1P8	VREG_L7	PLL2, QFPROM
46	200	VREG_L11_2P85	VREG_L11	UIM1, VDD_P4
47	200	VREG_L13_2P85	VREG_L13	UIM2, VDD_P5

B APQ8084 + MDM9x25

Sense inputs	R_{sense} (mΩ)	Power rail	PMIC regulator	Description
2	10	VBATT	VBATT	Total battery current
4	25	VPH_PWR for WLAN	WLAN 3.3 V REGULATOR	VPH_PWR going to WLAN card
5	10	VPH_PWR for MDM	PM8019	Total power input to PM8019
7	10	VREG_S1A_0P95	PMA8084 SMPS1	APQ: VDD_MEM, USB_CORE, EBIx_CDC, and EBIx_PLL
8	10	VREG_S2A_0P95	PMA8084 SMPS2, 12	APQ: VDD_CORE, SDC_CDC, and PLL2
9	10	VREG_S3A_1P3	PMA8084 SMPS3	Total PMA S3A power
10	10	VREG_S4A_1P8	PMA8084 SMPS4	Total PMA S4A power
11	10	VREG_GFX_0P95	PMA8084 SMPS6, 7	APQ: VDD_GFX
12	10	VREG_KRAIT_0P95	PMA8084 SMPS8, 9, 10, 11	APQ: VDD_KRAIT
13	10	VREG_S1_0P9	PM8019 SMPS1	MDM: VDD_MODEM
14	10	VREG_S4_1P85	PM8019 SMPS4	Total PM8019 S4A power
15	10	VREG_L3_0P9	PM8019 LDO3	MDM: VDD_CORE
16	10	VREG_S3_1P0	PM8019 SMPS3	Total PM8019 S3A power
17	25	VPH_PWR	DISPLAY: BACKLIGHT DRIVER	Display: backlight driver
19	25	VREG_L20A_2P95	PMA8084 LDO20	EMMC-UFC
21	10	VREG_L1A_1P225	PMA8084 LDO1, 11	APQ: VDD_DDR_C_1P2, VDD_P1, and VDD_P4 WCD: VDD_DIG, VDD_A
23	10	VREG_S5A_L25A_2P15	PMA8084 LDO25, SMPS5	WCD: VDD_BUCK
25	25	VDDPX_3_LPDDR3_VDD1	PMA8084 SMPS4	APQ: VDD_DDR_1P8
27	100	VPH_PWR	BACK UP DISPLAY DRIVER POWER SUPPLY	Back up display driver power supply
41	50	VREG_L17A_2P8	PMA8084 LDO17	PMA LDO 17 for camera
42	10	SD CARD	–	SD card power
43	25	VREG_L1C_1P225	PM8019 LDO1	PM8019 LDO1 going to RF card
44	25	VREG_L9_1P2	PM8019 LDO9	MDM: VDD_DDR_CORE_1P2, VDD_P1, and VDD_P6
45	500	VREG_LVS1A_1P8	PMA8084 LVS1	PMA LVS1 for TS 1.8 V
46	200	VREG_L18A_2P85_SNS	PMA8084 L18	PMA LDO 18 for sensor 2.85 V
47	200	VREG_L18A_2P85	PMA8084 L18	PMA LDO 18 for TS 2.85 V

C APQ8084 + MDM9x35

Sense inputs	R_{sense} (mΩ)	Power rail	PMIC regulator	Description
2	10	VBATT	VBATT	Total battery current
4	25	VPH_PWR for WLAN	WLAN 3.3 V REGULATOR	VPH_PWR going to WLAN card
5	10	VPH_PWR for MDM	PMD9635	Total power input to PMD9635
7	10	VREG_S1A_0P95	PMA8084 SMPS1	APQ: VDD_MEM, USB_CORE, EBIx_CDC, and EBIx_PLL
8	10	VREG_S2A_0P95	PMA8084 SMPS2, 12	APQ: VDD_CORE, SDC_CDC, and PLL2
9	10	VREG_S3A_1P3	PMA8084 SMPS3	Total PMA S3A power
10	10	VREG_S4A_1P8	PMA8084 SMPS4	Total PMA S4A power
11	10	VREG_GFX_0P95	PMA8084 SMPS6, 7	APQ: VDD_GFX
12	10	VREG_KRAIT_0P95	PMA8084 SMPS8, 9, 10, 11	APQ: VDD_KRAIT
13	10	VREG_S1_0P9	PMD9635 SMPS1	MDM: VDD_MODEM
14	10	VREG_S4_1P85	PMD9635 SMPS4	Total PMD S4A power
15	10	VREG_L3_0P9	PMD9635 LDO3	MDM: VDD_CORE
16	10	VREG_S3_1P0	PMD9635 SMPS3	Total PMD S3A power
17	25	VPH_PWR	DISPLAY: BACKLIGHT DRIVER	Display: backlight driver
19	25	VREG_L20A_2P95	PMA8084 LDO20	EMMC-UFC
21	10	VREG_L1A_1P225	PMA8084 LDO1, 11	APQ: VDD_DDR_C_1P2, VDD_P1, and VDD_P4 WCD: VDD_DIG and VDD_A
23	10	VREG_S5A_L25A_2P15	PMA8084 LDO25, SMPS5	WCD: VDD_BUCK
25	25	VDDPX_3_LPDDR3_VDD1	PMA8084 SMPS4	APQ: VDD_DDR_1P8
27	100	VPH_PWR	BACK UP DISPLAY DRIVER POWER SUPPLY	Back up display driver power supply
41	50	VREG_L17A_2P8	PMA8084 LDO17	PMA LDO 17 for camera
42	10	VPH_PWR_WTR		VPH_PWR going to RF card for WTR
43	25	VREG_L9_1P0	PMD9635 LDO9	PMD9635 LDO 9 going to RF card
44	25	VREG_L2_1P2	PMD9635 LDO2	MDM: VDD_DDR_CORE_1P2, VDD_P1, and VDD_P6
45	500	VREG_LVS1A_1P8	PMA8084 LVS1	PMA LVS1 for TS 1.8 V
46	200	VREG_L18A_2P85_SNS	PMA8084 L18	PMA LDO 18 for sensor 2.85 V
47	200	VREG_L18A_2P85	PMA8084 L18	PMA LDO 18 for TS 2.85 V

D MSM8994

Sense inputs	R_{sense} (mΩ)	Power rail	PMIC regulator [1]	Description
2	10	VBATT	VBATT	Total battery current
4	200	VREG_L3A_1P2	VREG_L3A	Total L3A – front camera
5	10	VREG_S7A_1P0	VREG_S7A	Total S7 power – modem
6	10	VREG_APCC0_1P0	VREG_S8A	Total S8 power for A53s
7	10	VREG_APCC1_0P988	VREG_S9A, VREG_S10A, VREG_S11A	Total S9 + S10 + S11 power for A57s
8	100	VREG_L23A_2P6	VREG_L23A	Total L23A – front camera
9	50	VREG_L27A_1P05	VREG_L27A	Total L27A – rear camera
10	400	VREG_L29A_FCAM	VREG_L29A	Total L29A – front camera
11	300	VREG_S4A_1P8	VREG_S4A	VDD_P3 portion only
12	500	VREG_LCD_IO	VREG_L14A	Portion for display IO only
13	5000	VREG_L14A_1P8	VREG_L14A	Portion for touch screen DVDD only
14	500	VREG_L22A_3P0	VREG_L22A	Total L22A – touch screen AVDD
15	10	VPH_PWR_WLED	VPH_PWR	External power for WLED only
16	2000	V_DISP	VPH_PWR	External power for display only V_DISP and VDD_DIS pins of PMI8994
17	1000	VREG_L17A_2P7	VREG_L17A	Total L17A – RCAM
19	3000	VREG_LVS1A_1P8	VREG_LVS1A	Total LVS1A – camera
21	10	VREG_S1A_S6A_1P0	VREG_S1A + VREG_S6A	Total S1A and S6A – VDD_CORE plus VDDA_SDCx_DLL
23	2000	VREG_S4A_1P8	VREG_S4A	Portion for PMI8994 display only
25	10	VREG_LPDDR_1P1	External Switcher	Total power from external switcher for LPDDR and VDD_P1 (interface to LPDDR)
27	1000	VREG_S4A_1P8	VREG_S4A	VDD_DDR_CORE_1P8 portion only
41	10	VREG_S2B_S3B_0P988	VREG_S2B and VREG_S3B	Total for VDD_GFX
42	100	VREG_L26A_1P0	VREG_L26A	Total L26A – VDD_EBI
43	10	VREG_S1B_1P0	VREG_S1B	Total S1B – input to PMIC for LDO1 – WTR
44	50	VREG_S4A_1P8_RF	VREG_S4A	Only portion for RF
45	10	VPH_PWR_RF	VPH_PWR	RF power to QFE1100
46	5000	VREG_L19A_3P3	VREG_L19A	Total L19A power – connectivity
47	10	VREG_S2A_S12A_1P1	VREG_S2A and VREG_S12A	Total S2A + S12A – VDD_MX, AP PLLS, and USB

For PMI8994, PMIC regulators end with the letter B. For PM8994, PMIC regulators end with the letter A.

E MDM9x40

Sense inputs	R_{sense} (mΩ)	Power rail	PMIC regulator	Description
2	10	VBATT	VBATT	Total battery current
4	2000	VDD_USB_HS_3P3	VREG_L10	HS_USB
5	301	VDD_P4	VREG_L11	UIM1
6	499	QFE_RFSWITCH, QFE_TUNER, QFE_QPAD	VREG_L12	QFE 2.7 V
7	10	VDD_MODEM	VREG_S1	Modem power
8	10	VREG_S2	VREG_S2	LDOs from S2 (L1, L2, and L16)
9	10	VREG_S3	VREG_S3	LDOs from S3 (L3 and L4)
10	20	WTR 1P8	VREG_S4	WTR3925 and WTR4905 1.8 V
11	10	VDD_CORE	VREG_S5	Digital core power
12	40	VDD_A1	VREG_L1	Analog core at 1.25 V
13	10	VDD_USB_SS_0P9, VDD_PCIE_0P9	VREG_L4	USB, PCIe at 0.9 V
14	20	VDD_USB_HS_1P8, VDD_USB_SS_1P8, VDD_PCIE_1P8	VREG_L8	USB, PCIe at 1.8 V
15	50	eMCP VDD2	VREG_L2	LPDDR2 VDD2 only
16	50	eMCP VDDQ	VREG_L2	LPDDR2 VDDQ only
17	1000	eMCP VDD1	VREG_L6	LPDDR2 VDD1 only
19	1000	VDD_PLL	VREG_L7	PLL circuits
21	2000	GPS_LNA	VREG_L15	GPS_LNA
23	10	VDD_PA1	VPH_PWR_QPOET	QFE 3.7 V from VPH_PWR
25	402	VDD_A2	VREG_L5	Analog core at 1.8 V
27	10	VDD_P1	VREG_L2	LPDDR2 pads
41	1000	PMIC_XO_VDD	VPH_PWR_XO	XO supply at 3.7 V
42	10	VDD_A3	VREG_L9	Analog core memory
43	50	VDD_P3, VDD_P7	VREG_L6	General I/O pads
44	100	QFE_RFSWITCH, QFE_TUNER	VREG_L15	QFE at 1.8 V
45	20	WTR 1P0	VREG_L3	WTR3925 and WTR4905 1.0 V

F MSM8992

Sense inputs	R_{sense} (mΩ)	Power rail	PMIC regulator	Description
2	10	VBATT	–	Main battery connector
4	200	PM8994: VREG_L3A_1P2	–	VREG_FCAM_1PX (front camera)
5	10	PM8994: VREG_S7A_1P0	–	VDD_MODEM
6	10	PM8994: VREG_S8A_1P0	–	VREG_APCC0_1P0 (A53s)
7	10	PM8994: VREG_S9A_S10A_S11A_0P988	–	VREG_APCC1_0P988 (A57s)
8	100	PM8994: VREG_L23A_2P8	–	VREG_CAM_AF (front and rear camera)
9	50	PM8994: VREG_L27A_1P05	–	VREG_RCAM_1PX (rear camera)
10	400	PM8994: VREG_L29A_2P8	–	VREG_L29A_FCAM (front camera)
11	300	PM8994: VREG_S4A_1P8	–	MSM_VDDPX_3
12	500	PM8994: VREG_L14A_1P8	–	VREG_LCD_IO
13	5000	PM8994: VREG_L14A_1P8	–	TS_DVDD
14	500	PM8994: VREG_L22A_3P0	–	TS_AVDD
15	10	VPH_PWR	–	VPH_PWR_WLED
16	200	VPH_PWR	–	V_DISP
17	1000	PM8994: VREG_L17A_2P7	–	VREG_L17A_RCAM (rear camera)
19	3000	PM8994: VREG_LVS1A_1P8	–	VREG_LVS1A_CAM (front and rear camera)
21	10	PM8994: VREG_S1A_S6A_1P0	–	VDD_CORE
23	2000	PM8994: VREG_S4A_1P8	–	PMI_VDISN_1P8
25	100	LPDDR EXTERNAL REGULATOR output	–	VREG_LPDDR_1P225
27	1000	PM8994: VREG_S4A_1P8	–	VDD_DDR_CORE_1P8
41	10	PM8994: VREG_S2A_S3A_0P988	–	VREG_GFX_0P988
42	100	PM8994: VREG_L26A_1P0	–	VDD_EBI
43	20	PMI8994: VREG_S1B_1P0	–	VDD_L1 of PM8994 (VREG_L1A_1P0 → VREG_WTR_1P0)
44	50	PM8994: VREG_S4A_1P8	–	VREG_S4A_1P8_RF
45	10	VPH_PWR	–	VPH_PWR_RF
46	5000	PM8994: VREG_L19A_3P3	–	QCA DC connector B 3.3 V
47	10	PM8994: VREG_S2A_S12A_1P1	–	VDD_MEM

G MSM8952

Sense inputs	R_{sense} (mΩ)	Power rail	PMIC regulator[1]	Description
2	5	VBATT	VBATT	Battery
4	25	VREG_S4_1P85_SUB	VREG_S4	PM8952, sub-regulators under VREG_S4
5	25	VREG_L9_3P3	VREG_L9	WCN PA branch only (pin 57, connector B on reference schematic)
6	25	VPH_PWR_WLED_BL	VPH_PWR	PMI8952 backlight
7	100	VPH_PWR_DISPLAY	VPH_PWR	PMI8952 display
8	10	VREG_S2_1P15	VREG_S2	MSM8952 VDD_CORE
9	5	VREG_L3_1P15	VREG_L3	MSM8952 VDD_MEM
10	10	VREG_S5_S6_1P15	VREG_S5 + VREG_S6	MSM8952 APC
11	10	VREG_S3_1P3_SUB	VREG_S3	PM8952: sub-regulators under VREG_S3
12	5	VREG_L19_1P3_WCN	VREG_L19	WCN3682
13	5	VREG_L2_1P2_CSI_DSI	VREG_L2	MSM8952, CSI/DSI PHY
14	10	VREG_L2_VDD_P1	VREG_L2	MSM8952, VDD_P1
15	25	VREG_L2_VDD2_LPDDR3	VREG_L2	LPDDR3 VCCCAD, VCCD2, and VCCQD
16	25	VREG_L23_CAM_DVDD	VREG_L23	Camera DVDD
17	200	VPH_PWR_PMIC_CODEC	VPH_PWR	PM8952 CDC
19	50	VREG_L22_2P85	VREG_L22	Camera AVDD
21	25	VREG_L8_2P95	VREG_L8	eMMC VCCM
23	25	VREG_L11_SDC	VREG_L11	SD/MMC CARD
25	200	VPH_PWR_RF	VPH_PWR	RF, QFE
27	500	VREG_L1_1P0_RF	VREG_L1	RF, WTR
41	25	VREG_L4_1P8_RF	VREG_L4	RF, WTR/GPS and QFE
42	25	VREG_L10_2P85_SNS	VREG_L10	Sensors
43	25	VREG_L17_2P85_TS	VREG_L17	Touch screen
44	25	VREG_S1_1P15	VREG_S1	MSM8952 modem
45	25	VREG_L17_2P85_CAMAF	VREG_L17	Camera AF
46	25	VREG_L5_VDD1_LPDDR3	VREG_L5	LPDDR3 VDD1
47	25	VREG_L19_VDD_A1	VREG_L19	VDD_A1, pins AR29 and AR31

H MSM8956/MSM8976

Sense inputs	R_{sense} (mΩ)	Power rail	PMIC regulator	Description
1	10	VBATT	VBATT	Total battery current
2	10	VREG_S4A_2P05	PM8956 SMPS4	PM8956 VDD_L4, VDD_L5, VDD_L6, VDD_7, VDD_16, VDD_XO_RFCLK, VDD_HPH, eLDO WCD VDD, and OV2685 eLDO
3	20	VREG_L9A_3P3	PM8956 LDO9	WCN3660B/WCN3680B 3.3 V
4	50	VPH_PWR_WLED	VPH_PWR	PMI8952 VPH_PWR_WLED
5	10	VREG_S2A_0P9	PM8956 SMPS2	VDD_CORE
6	10	VREG_S6A_0P95	PM8956 SMPS6	VDD_MEM
7	10	VREG_S2C_S4C_0P9	PM8004 SMPS2 PM8004 SMPS4	VDD_A72
8	10	VREG_S5A_0P9	PM8956 SMPS5	VDD_A53
9	10	VREG_S3A_1P325	PM8956 SMPS3	PM8956 VDD_L1_19, VDD_L2_23, and VDD_L3
10	10	VREG_S5C_0P9	PM8004 SMPS5	VDD_GFX
11	10	VREG_S1A_0P9	PM8956 SMPS1	VDD_MODEM
12	10	VREG_L2A_1P2	PM8956 LDO2	VDD_P1
13	10	VREG_L2A_1P2	PM8956 LDO2	VDD_DDR2
14	20	VREG_L3A_1P1	PM8956 LDO3	Rear camera, DVDD
15	10	WCD_VDD_BUCK_1P8	PM8956 SMPS4 → eLDO	WCD9326/WCD9335 VDD_SIDO and VDD_BUCK
16	50	VREG_L22A_2P8	PM8956 LDO22	Rear camera, AVDD
17	20	VREG_L17A_2P85	PM8956 LDO17	Front/rear camera autofocus
18	10	VREG_L8A_2P9	PM895 LDO8	eMMC VCC
19	10	VREG_L11A_2P95	PM8956 LDO11	SD card
20	10	VPH_PWR	VPH_PWR	RF card (QFE2340 and QFE2101)
21	20	VREG_L1C_1P0	PM8004 LDO1	RF card (WTR2955 1.0 V)
22	20	VREG_L4A_1P8	PM8956 LDO4	RF card (WTR2955 1.3 V)
23	20	VREG_L10A_2P85	PM8956 LDO10	Sensors (pressure, magnitude), MIC6 (digital)
24	20	VREG_L19A_1P3_WCN	PM8956 LDO19	WCN3660B/WCN3680B 1.3 V
25	1000	VREG_L10A_2P85	PM8956 LDO10	TS card
26	100	VREG_L6A_1P8	PM8956 LDO6	VDDA_1P8_MIPI_DSI, VDDA_MIPI_DSI0_PLL, VDDA_MIPI_DSI1_PLL, and VDDA_MIPI_CSI0_1
27	50	VPH_PWR	VPH_PWR	PMI8952 VSW_DIS_P

Sense inputs	R_{sense} (mΩ)	Power rail	PMIC regulator	Description
1	10	VBATT	VBATT	Total battery current
2	50	VREG_FCAM_1P0	External LDO powered through PM8996 SMPS5	Front camera DVDD
3	10	VREG_S7A_1P0	PM8996 SMPS7	VDD_MODEM
4	20	VREG_L26A_0P8	PM8996 LDO26	VDD_SSC_CORE
5	10	VREG_APC_0P8	PM8996 SMPS8_9_10_11	Qualcomm® Kryo™ CPU, VDD_APC
6	100	VREG_L23A_VCM_2P8	PM8996 LDO23	Front and rear camera module
7	50	VREG_DVDD_1P1	External LDO powered through PM8996 SMPS3	Rear camera DVDD
8	500	VREG_L29A_FCAM_2P8	PM8996 LDO29	Front camera AVDD
9	400	VREG_S4A_1P8	PM8996 SMPS4	VDD_P3
10	300	VREG_L14A_1P8	PM8996 LDO14	Touchscreen display, 1.8 V
11	200	VREG_LVS2A_1P8	PM8996 LVS2	Sensors, 1.8 V
12	500	VREG_L22A_3P3	PM8996 LDO22	Display LCD touchscreen
13	20	VPH_PWR_DISPLAY	PMI8994 VPH_PWR	Main power for WLED_BACKLIGHT/WLED_DISPLAY
14	100	VREG_L31A_0P875	PM8996 LDO31	VDD_SSC_MEM
15	500	VREG_L17A_RCAM_AVDD_2P7	PM8996 LDO17A	Rear camera, AVDD
16	3000	VREG_LVS1A_CAM	PM8996 LVS1A	Front and rear camera, 1.8 V
17	10	VREG_S1A_S6A_0P8	PM8996 SMPS1_6	VDD_CORE
18	50	VREG_L19A_3P0	PM8996 LDO19	Sensors (3 V)
19	10	VREG_S12A_1P15	PM8996 SMPS12	VDD_DDR_CORE_1P2
20	50	VREG_S4A_1P8	PM8996 SMPS4	VDD_DDR_CORE_1P8
21	10	VREG_S2B_S3B_0P988	PMI8994 SMPS2_3	Graphics, VDD_GFX
22	10	VREG_L3A_0P875	PM8996 LDO3	VDD_EBI_PHY, VDD_EBI_IO, and VDD_EBI_IO_ISO
23	10	VREG_S1B_1P025	PMI8994 SMPS1	WTR3925
24	50	VREG_RF_1P8	PM8996 SMPS4	RF connector 1, 1.8 V
25	10	VPH_PWR_RF	PMI8994: VPH_PWR	RF_CARD_VPH
26	200	VREG_L16A_2P7	PM8996 LDO16	RF connector 2, 2.7 V (RD_ANTENNA_SW)
27	10	VREG_S2A_S12A_0P85	PM8996 SMPS2	VDD_MEM

J MSM8998

Sense inputs	R_{sense} (mΩ)	Power rail	PMIC regulator	Description
1	10	VBATT	VBATT	Total battery current
2	25	CAM_S3A	PM8998 VERG_S3A	Camera power DVDD for primary rear facing camera, front-facing camera, and IRIS camera
3	10	VREG_S2C_0P75	PM8005 SMPS2	VDD_MODEM
4	50	VDD_SSC_CX	PM8998 LDO27	VDD_SSC_CORE
5	10	VREG_S11A_S12A_S13A_0P75	PM8998 SMPS11_12_13	VDD_APC1
6	300	P1V8_CAMD3	PM8998 LVS1	AUX camera DVDD, AUX camera and primary rear-facing camera DOVDD
7	510	P2V5_CAMA1	External LDO powered through PM8998 VREG_S3A	Primary rear-facing camera AVDD, 2.5 V
8	300	P2V8_VCM1	External LDO powered through PM8998 VREG_S3A	Primary rear-facing and front-facing cameras VCM, 2.8 V
9	100	VDDPX_3	PM8998 SMPS4	VDD_P3
10	100	VREG_L14A_1P88	PM8998 LDO14	Touchscreen display, 1.8 V
11	510	VREG_LVS2A_1P8_SENSORS	PM8998 LVS2	Sensors, 1.8 V
12	510	VREG_L6A_1P8	PM8998 LDO16	Display LCD touchscreen
13	100	VDD_WLED	PMI8998 VPH_PWR	Main power for LED_BACKLIGHT/WLED_DISPLAY
14	510	VREG_L4A_0P8_SSC_MX	PM8998 LDO4	VDD_SSC_MEM
15	10	VREG_S3C_0P6	PM8005 SMPS3	VDD_EBI_IO and VDD_DDR_DQ
16	510	P2V8_CAMA2_4	PM8998 LDO22	Primary front-facing and iris cameras AVDD, 2.85 V
17	10	VREG_S1A_S6A_0P75	PM8998 SMPS1_6	VDD_CORE
18	100	VREG_L19A_3P0_SENSORS	PM8998 LDO19	Sensors (3 V)
19	10	VREG_S2A_1P125	PM8998 SMPS2	VDD_DDR_CORE_1P1
20	100	MSM_VDD1	PM8998 SMPS4	VDD_DDR_CORE_1P8
21	10	VREG_S1C_S4C_0P75	PMI8998 SMPS1_4	Graphics, VDD_GFX
22	10	VREG_S8A_0P8	PM8998 SMPS8	VDD_EBI_PHY
23	50	WTR_VDDA_1P0	PMI8998 LDO3	WTR_VDDA
24	300	VREG_RF_1P8	PM8998 SMPS4	RF connector 1, 1.8 V
25	50	VPH_PWR_RF	PMI8998 VPH_PWR	RF_CARD_VPH
26	10	VREG_S10A_0P75	PM8998 SMPS10	VDD_APC0
27	10	VREG_S9A_0P8	PM8998 SMPS9	VDD_MEM

K MSM8953

Sense inputs	R_{sense} (mΩ)	Power rail	PMIC regulator	Description
1	10	VBATT	VBATT	Total system power
2	10	VREG_S4_2P05	VREG_S4	PM8953 S4 total current
3	50	VREG_L9_3P3_WCN_PA	VREG_L9	WCN PA
4	10	VPH_PWR_WLED	VPH_PWR	VPH to backlight
5	50	VPH_PWR_DISPLAY	VPH_PWR	VPH display
6	10	VREG_S2_CX	VREG_S2	PM8953 S2 to CX power
7	10	VREG_S7_MX	VREG_S7	PM8953 S7 to VDDMX
8	10	VREG_S5_S6_APC	VREG_S5_S6	PM8953 S5 and S6 to APCs
9	10	VREG_S3_1P225	VREG_S3	PM8953 S3 total current
10	50	VREG_L19_1P3_WCN	VREG_L19	PM8953 LDO19 to WCN3680
11	100	VREG_S3_DSI_CSI	VREG_S3	PM8953 S3 to MSM DSI and CSI PHY
12	50	VREG_S3_PX1	VREG_S3	PM8953 S3 LDO to VDD_PX1
13	10	VREG_S3_LPDDR3	VREG_S3	PM8953 S3 to LPDDR3 VDD2, VDDQ, and VDDCA
14	50	VREG_L23_8MP_DVDD	VREG_L23	PM8953 L23 LDO to 8 MP front camera DVDD
15	50	VPH_PWR_PMIC_CODEC	VPH_PWR	VPH_PWR to input of PMIC internal codec boost regulator
16	100	VREG_L22_8MP_2MP_AVDD	VREG_L22	PM8953 L22 LDO to 8 MP front and 2 MP rear assisting AVDD
17	50	VREG_L8_2P9	VREG_L8	PM8953 L8 LDO to eMMC VCC
18	100	VPH_PWR_PMIC	VPH_PWR	PMIC internal battery consumption
19	10	VPH_PWR_RF	VPH_PWR	VPH power to RF card
20	25	VREG_L1_1P0_RF	VREG_L1	PM8953 L1 LDO to WTR2965
21	25	VREG_L4_1P8_RF	VREG_L4	PM8953 L4 LDO to WTR2965
22	100	VREG_L6_1P8_SNS	VREG_L6	Sensors, gyro, accel, compass, pressure, and Hall sensors
23	100	VREG_L10_2P85_TS	VREG_L10	Touchscreen
24	10	VREG_S1_MSS	VREG_S1	PM8953 S1 to modem subsystem power
25	100	BBCLK_EN	–	To monitor CXO_ENABLE
26	50	VDD1_L5_1P8_LPDDR3	VREG_L5	PM8953 L5 LDO to LPDDR2 VDD1
27	100	VREG_S3_BBRX	VREG_S3	PM8953 S3 to BBRX