PM8921 Power Management IC

Device Specification

80-N4420-1 Rev. E

November 20, 2011

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Revision history

Bars appearing in the left margin (as shown here) indicate where technical changes have occurred for this revision. The following table lists the technical content changes for all revisions.

Revision	Date	Description
A	February 2011	Initial release
B	April 2011	■ Updated Section 1.3.8 with height information ■ Updated Table 1-2 with height information ■ Updated Figure 3-6, Example high-level power sequence timing diagram ■ Updated Section 4.1 with height information ■ Added Figure 4-1 (obsolete in Revision C), *251-NSP (7.8 × 7.8 × 0.88 mm) package outline drawing* ■ Added Figure 6-1 (obsolete in Revision C), *Recommended 251 NSP land pattern*, and Figure 6-2 (obsolete in Revision C)*, Recommended 251 NSP stencil pattern* ■ Updated Section 7.2 with height information
C	July 2011	■ Changed erroneous references to the PM8058 device throughout to PM8921 device ■ Modified the IC interfaces in Figure 1-1 ■ Removed PA range controls from Section 1.3.6 ■ Updated Table 1-2 □ Changed USB over-voltage protection from 28 V to 30 V □ Updated 19.2 MHz oscillator support in the General housekeeping section □ Updated the PM8921 capability description of UIM support □ Removed entry for PA controller from the IC-level interfaces section ■ Changed pin assignment G17 from USB_VBUS to PHY_VBUS in Figure 2-1 ■ Updated V_XX and V_YY in the Pad voltage groupings section in Table 2-1 ■ Changed pins B7, D8, D6, and D7 in Figure 2-2 from analog to digital; changed pins D7 and D8 from pad type AO to DO ■ Updated pin G17 in Table 2-3 ■ Updated Table 2-5 □ In the Analog multiplexer and HK/XO ADC circuits section, updated the description of pin H14 and deleted rows for pins F13, D14, E14, and P14 □ Updated pins H7, J7, K7, N6, J14, and L7 □ Changed pins in the 32.768 kHz XTAL, sleep clock, and MP3 clock circuits section □ Updated the VREF output section ■ Updated pins in the Current drivers section of Table 2-6

Revision	Date	Description
C (cont.)	July 2011	■ Updated Table 2-7 □ Updated pins in the Poweron circuits section □ Deleted the row for pin P8 from the Primary PM/modem IC interface signals section □ Added pins P10 and R11 to the UIM interfaces section □ Added pins P11 and D7 to the UART multiplexing section ■ Updated Table 2-8 □ Removed obsolete pad information from the MPPs section □ Updated pin information for GPIO_1 through GPIO_44 ■ Updated the first note below Table 2-8 ■ Updated pin K5 in Table 2-10 ■ Updated V_{bat} Table 3-1 ■ Updated V_{ovp} in Table 3-2 ■ Updated power supply currents in Table 3-3 ■ Added V_{weak} info to Table 3-8 ■ Added Table 3-9 ■ Added footnote to Table 3-16 ■ Replaced all the values in Table 3-19 ■ Removed one entry for Overall error from Table 3-24 ■ Added text about LVS 1, 3, 4, 5, 6, and 7 to Section 3.6.7 ■ Modified the ATC current driver sub-heading in Table 3-45 ■ Added Table 3-51 ■ Updated Section 4.1 to include a link to the package outline drawing (NT90) ■ Updated Table 4-2 ■ Updated Section 6.1 to include links to the land/stencil drawing (LS90), and the daisy chain interconnect drawing (DS90)
D	September 2011	■ Revised the document title of the referenced schematic in Section 1.2 ■ Revised general housekeeping features details in Section 1.3.4 ■ Revised the V_XX symbol description in Table 2-1, I/O description (pad type) parameters ■ Revised Table 2-2, Expected maximum currents at PI and PO pad types □ Changed the function of pads A7, B7, and B6 from SO to S1 □ Changed the function of pads A13, B13, and B14 from S1 to S2 ■ Revised Table 2-5, Pin descriptions – general housekeeping functions □ Changed the pad R13 name from MP3_CLK to MP3_CLK1 □ Changed the pad N14 name from MP3_CLK to MP3_CLK2 ■ Revised Table 2-8, Pin descriptions – configurable input/output functions □ Added AI to the pad type of the MPPs □ Revised P10 (GPIO_36) pad function and description from UART_M_TX to UIM1_RMV_DET_N □ Revised R11 (GPIO_37) pad function and description from UART_M_RX to UIM2_RMV_DET_N ■ Revised Table 3-2, Recommended operating conditions □ Revised VOVP and VDCIN values □ Removed VUSBIN ■ Revised the XTAL on typical value and added XTAL off values to the ICOIN parameter and in Table 3-3, DC power supply currents

Revision	Date	Description
D (cont.)	September 2011	■ Revised Table 3-5, Supply detection performance specifications ■ Removed the PMIC user guide document reference from Section 3.5.3.1, Main battery charging ■ Revised the BPD-comparator debounce typical values in Table 3-8, Battery interface specifications ■ Removed Battery FET detection threshold information from Table 3-13 ■ Revised Table 3-15, Sense resistor requirements and insense accuracy ■ Revised specified range (V) for regulators L12, L15, and L17; removed L13; and added a footnote to L6 in Table 3-18, Output power management summary ■ Removed various footnotes for the following tables: Table 3-22, Table 3-23, Table 3-26, and Table 3-34 ■ Removed channel 3 details from Table 3-34, Analog multiplexer and scaling functions ■ Removed Table 3-38, XO controllers, buffers, and circuits performance specifications ■ Revised Table 3-37, Specifications for XO_OUT_D0 and XO_OUT_D1 ■ Revised Section 3.7.3, System clocks ■ Revised the document reference in Section 3.8.1, Light pulse generator ■ Added pulse-width modulation frequency details to Section 3.8.2, LPG controllers (digital driver outputs) ■ Revised Table 3-49, Poweron circuit performance specifications □ Revised sequence time intervals values for t(reg0) □ Removed the document reference □ Revised the footnote for t(reg1) regarding the inclusion of keypad debounce time ■ Added Table 3-53, Special GPIO default state details ■ Revised the title of Figure 3-5, Example high-level power sequence timing diagram for PM8921 IC when paired with MSM8960 IC (OPT1 = VDD, OPT2 = Hi-Z, OPT3 = VDD) ■ Removed the document reference in Section 3.9.2, SSBI and the interrupt managers ■ Revised Table 4-2, Device identification code/ordering information details with additional code information
E	November 2011	■ Added note to GPIO_42 and GPIO_43 in Table 2-8 ■ Updated I_{COIN} parameter entry in Table 3-3 ■ Removed charger removal detection item in Table 3-5 ■ Table 3-6 □ Changed unit for battery charge current programmable range □ Updated footnotes ■ Added Figure 3-2 and Table 3-8 ■ Added text to Section 3.5.3.2 ■ Added Figure 3-3 and Figure 3-10 ■ Updated Irated (mA) number for regulator S3 in Table 3-18 ■ Added Figure 3-3 and Figure 3-4 ■ Updated Section 3.6.3.1 ■ Updated Table 3-22 ■ Updated Section 3.6.4 ■ Updated Table 3-25 and Table 3-28 ■ Deleted previous Table 3-42

Revision	Date	Description
E (cont.)	November 2011	■ Renamed current Table 3-42 ■ Deleted previous Table 3-43 ■ Added LPG channel assignment to the end of Section 3.8.1 ■ Updated **t**(reg0) comment in Table 3-49

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Tables

1 Introduction

1.1 Documentation overview

Technical information for the PM8921™ IC is covered by the documents listed in Table 1-1, and should be studied for a thorough understanding of the IC and its applications. The device introduction given in Section 1.2 is a good place to start. All released PM8921 documents are posted on the CDMATech Support Website (https://support.cdmatech.com) and are available for download.

Table 1-1 Primary PM8921 device documentation

Document number	Title/description
80-N4420-1 (this document)	*PM8921 Power Management IC Device Specification* Provides all PM8921 IC electrical and mechanical specifications. Additional material includes pin assignment definitions; shipping, storage, and handling instructions; PCB mounting guidelines; and part reliability. This document can be used by company purchasing departments to facilitate procurement.
80-N4420-4	*PM8921 Power Management IC Device Revision Guide* Provides a history of PM8921 IC revisions. This document explains how to identify the various IC revisions, and discusses known issues (or bugs) for each revision and how to work around them.
80-N1622-5	*MSM8960 Chipset (RTR860x, PM8921, WCD9310, WCN3660) Schematics and Design Guidelines* ■ Schematic diagram for an MSM8960™ device-based reference design and its parts list. ■ Detailed functional and interface descriptions for all chipset ICs: □ MSM8960 modem IC □ RTR8600™/RTR8601™/RTR8605™ RF transceiver IC □ PM8921 power management IC □ WCD9310 audio codec IC □ WCN3660 wireless connectivity IC ■ Key design guidelines for the chipset are illustrated and explained, including: □ DC power distribution □ PCB layout guidelines □ External component recommendations □ Troubleshooting techniques

This PM8921 device specification is organized as follows:

Chapter 1 Provides an overview of PM8921 IC documentation, shows a high-level PM8921 IC functional block diagram, lists the device features, and lists terms and acronyms used throughout this document.

Chapter 2 Defines the IC pin assignments.

Chapter 3 Defines the IC electrical performance specifications, including absolute maximum ratings and recommended operating conditions.

Chapter 4 Provides IC mechanical information, including dimensions, markings, ordering information, moisture sensitivity, and thermal characteristics.

Chapter 5 Discusses shipping, storage, and handling of PM8921 devices.

Chapter 6 Presents procedures and specifications for mounting the PM8921 device onto printed circuit boards (PCBs).

Chapter 7 Presents PM8921 IC reliability data, including definitions of the qualification samples and a summary of qualification test results.

1.2 PM8921 IC introduction

The PM8921 device (Figure 1-1) integrates all wireless handset power management, general housekeeping, and user interface support functions into a single mixed-signal IC. Its versatile design is suitable for CDMA, UMTS, and GSM phones, and other wireless products, such as data cards and PDAs.

This mixed-signal BiCMOS device is available in the 251-pin nano-scale package (NSP) that includes several ground pins.

Since the PM8921 IC includes so many diverse functions, its operation is more easily understood by considering major functional blocks individually. Therefore, the PM8921 document-set is organized by the following device functionality:

- Input power management
- Output power management
- General housekeeping
- User interfaces
- IC interfaces
- Configurable pins – either MPPs or GPIOs – that can be configured to function within some of the other categories

Most of the information contained in this device specification is organized accordingly – including the circuit groupings within the block diagram (Figure 1-1), pin descriptions (Chapter 2), and detailed electrical specifications (Chapter 3).

See the *MSM8960, PM8921, and WCD9310 Baseband Reference Schematic* (80-N1622-41) for more detailed descriptions of each PM8921 IC function and interface.

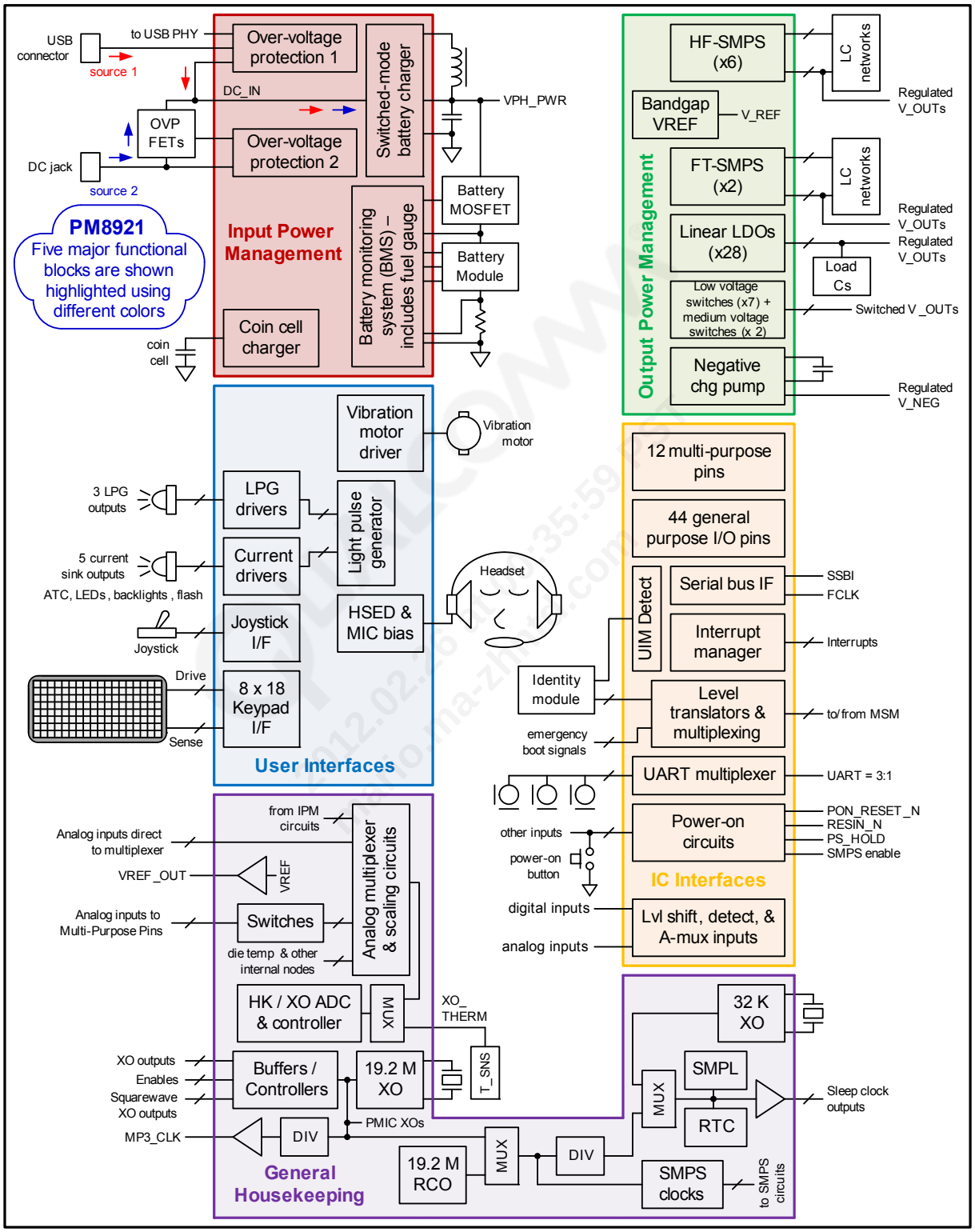


Figure 1-1 High-level PM8921 IC functional block diagram

1.3 PM8921 IC features

NOTE Some hardware features integrated within the PM8921 IC must be enabled through the modem IC software. See the latest version of the applicable software release notes to identify the enabled PMIC features.

1.3.1 New features integrated into the PM8921 IC

- Dual-charger support
  - Fully integrated 30 V USB over-voltage protection
  - 30 V wall charger OVP (external OVP FET required)
- A switched-mode battery charger (SMBC) for better efficiency than linear charging
- Auto-trickle charging (ATC) LED supply; supplements ATC current driver
- Battery fuel gauge for accurate management of battery resources
- High-frequency switched mode power supply (HF-SMPS) ***and*** fast transient switched mode power supply (FT-SMPS) circuits
  - Six HF SMPS with auto mode and switching frequencies up to 6.4 MHz
  - Two FT-SMPS circuits power high performance application processor cores that exhibit highly dynamic load changes
    - High output current rating – 2 A
    - Adaptive and static processor supply voltage control
- Forward clock input from the Mobile Station Modem™ (MSM™) device allows communications, even when the PMIC XO is off
- ***Five*** 19.2 MHz XO outputs with independent controls (three – low noise and two – low power)
- Additional clock outputs to support peripherals with divided down 19.2 MHz clock output options
- 44 configurable GPIO pins (plus 12 MPPs); example GPIO/MPP configurations include:
  - 8 × 18 keypad interface and joystick support
  - Level-shifting and UIM detection
  - Extra sleep clock outputs
  - UART multiplexing
  - External SMPS enable output
  - LPG outputs
  - External switch detection (supporting headset and flip switches)

1.3.2 Input power management features

- Dual-charger support
  - Fully integrated 30 V USB over-voltage protection
  - 30 V wall charger OVP (external OVP FET required)
- Valid external supply attachment and removal detection
- SMBC for better efficiency than linear charging
  - Four regulation control loops: USB input current, DC_IN input voltage, VPH_PWR output voltage, and battery current
- Supports lithium-ion and lithium-ion polymer
- Automated charging modes that allow PMIC battery charging with less software intervention
- Trickle, constant current, and constant voltage charging of the main battery
- ATC LED supply; supplements ATC current driver
- An expanded battery monitoring system (BMS) that includes a battery fuel gauge for accurate management of battery resources
- External battery MOSFET is optional
- Supports coincell backup battery or keep-alive capacitor (including charging)
- Battery voltage alarms with programmable thresholds
- VDD collapse protection
- Under-voltage lockout (UVLO) protection
- Automated recovery from sudden momentary power loss (SMPL)

1.3.3 Output power management

- Eight buck (step-down) switched-mode power supply circuits
  - Six high-frequency (HF-SMPS) circuits rated for 1.5 A each
  - Two fast transient (FT-SMPS) circuits rated for 2 A each
- One negative charge pump (NCP) power supply (-1.8 V for headset circuits)
- 28 low-dropout regulator circuits with programmable output voltages, supporting a wide range of current ratings: 1.2 A (5), 600 mA (2), 300 mA (4), 150 mA (13), and 50 mA (2); in addition, there are two low-noise low-dropout (LDO) regulators for the clock system.
- Seven low-voltage switches and two medium voltage switches for power supply gating to external circuits
  - Soft-start feature reduces in-rush current and avoids voltage drops at the source regulator
  - Over-current protection
- Supports dynamic voltage scaling (DVS) on key regulators

- Regulators can be individually enabled/disabled for power savings
- Low-power mode available on all regulators but the NCP
- All regulated outputs are derived from a common bandgap reference and trimmed for ±1% accuracy

1.3.4 General housekeeping features

- ADC input switches and analog multiplexing selects from several possible inputs (including MPPs)
- Input scaling increases the effective ADC resolution
- Dedicated on-chip HK/XO ADC for monitoring XO temperature and other housekeeping (HK) functions
- ADC arbiter to handle multiple simultaneous conversion requests
- 19.2 MHz XO circuitry and algorithms
- Five 19.2 MHz XO outputs with independent controllers
  - Three low-noise outputs; two low-power outputs
  - Enables XO warm-up, synchronization, deglitching, and buffering
- HS-USB support with 19.2 MHz reference clock output
- MP3 support with 2.4 MHz clock output in a low-power mode
- 32.768 kHz sleep crystal support
- Optional elimination of the 32.768 kHz XTAL
- On-chip RC oscillator for backup; oscillator detectors and automated switch-over
- One dedicated sleep clock output plus two configurable GPIOs for two more
- Realtime clock for tracking time and generating associated alarms
- On-chip adjustments minimize crystal oscillator frequency errors
- Multistage over-temperature protection (smart thermal control)
- Buffered reference voltage outputs via configurable MPPs

1.3.5 User interface features

- Eight-channel LPG for blinking or strobing LEDs and backlights
- One programmable, 5 V-tolerant current driver (up to 300 mA)
- Three programmable, 5 V-tolerant LED drivers (up to 40 mA)
- One 5 mA automatic trickle charging (ATC) indicator
- Three LPG controls for external drivers (GPIOs)
- Vibration motor driver programmable from 1.2 to 3.1 V in 100 mV increments
- One-touch headset controller – headset send/end detection and microphone bias

- 8 × 18 keypad interface support (all via GPIOs)
- External switch detection (supporting headset and flip switches)
- Joystick support

1.3.6 IC-level interface features

- SSBI for efficient initialization, status, and control
- Three internal interrupt managers (modem, secure, and user)
- Many functions monitored and reported through realtime and interrupt status signals
- Dedicated circuits for controlled power sequencing, including the modem IC's reset signal
- Several events continuously monitored for triggering poweron/poweroff sequences
- Dedicated control settings for selecting optional PMIC hardware configurations
- Forward clock input from the MSM device allows communications even when the PMIC XO is off
- Supports and orchestrates soft resets
- External controls (via GPIOs) for enabling external regulators
- 3:1 UART multiplexer (via GPIOs)
- UIM detection (via GPIO) and UIM level translators (via MPPs and GPIOs) enable modem IC interfacing with external modules

1.3.7 Configurable I/O features

- Twelve MPPs that can be configured as digital inputs or outputs; level-translating bidirectional I/Os; analog multiplexer inputs; or buffered VREF analog outputs
- 44 general purpose input/output pins that can be configured as digital inputs or outputs or level-translating I/Os; these configurable I/Os are much faster than MPPs

1.3.8 Package features

- Highly integrated functionality in a small package – 7.8 mm × 7.8 mm × 0.88 mm
- 251-pin NSP with several ground pins

1.3.9 Summary of key PM8921 features

Table 1-2 Key PM8921 features

Feature	PM8921 capability
Input power management	
Supported external power sources	USB and/or wall charger
Over-voltage protection USB Wall charger	 Fully integrated up to +30 V (integrated OVP FET) Up to +30 V with external OVP FET
Supported battery technologies	Lithium-ion, lithium-ion polymer
Charger regulation method	Efficient switched-mode battery charger; four control loops: USB input current, DC_IN input voltage, VPH_PWR output voltage, and battery current
Supported charging modes	Trickle, constant current, and constant voltage modes More automated for less software interaction
ATC indicator supply	ATC LED supply; supplements ATC current driver
External battery MOSFET	Optional
Voltage, current and thermal sensors	Internal and external nodes; reported to on-chip state-machine
Battery monitoring system	Including battery fuel gauge for better accuracy
coincell or capacitor backup	Keep-alive power source; orchestrated charging
Output power management	
Buck switched-mode power supplies HF-SMPS FT-SMPS	 Six, 1.5 A each Two, 2.0 A each
NCP	-1.8 V for headset circuit bias
Low dropout linear regulators	28 total: 1.2 A (5), 600 mA (2), 300 mA (4), 150 mA (13), 50 mA (2) and two custom LDOs for clock system
Medium-voltage switching	Two, suitable for power gating external circuitry
Low-voltage switching	Seven, suitable for power gating external circuitry
General housekeeping	
On-chip ADC	Shared housekeeping (HK) and XO support
Analog multiplexing for ADC HK inputs XO input	 Select from up several inputs including configurable MPPs Dedicated pin (XO_THERM)
Over-temperature protection	Multistage smart thermal control
19.2 MHz oscillator support	XO (with on-chip ADC)
XO controller and XO outputs	Five sets: three low-noise outputs and two low-power outputs
Special purpose clock outputs	Two extra sleep clocks; 19.2 MHz for HS-USB; 2.4 MHz for MP3
32 kHz clock source	XO source eliminates 32.768 kHz crystal if desired
Realtime clock	RTC clock circuits and alarms

Table 1-2 Key PM8921 features (cont.)

Feature	PM8921 capability
User interfaces	
Current drivers	One capable of sinking up to 300 mA; 5 V tolerant Three capable of sinking up to 40 mA; 5 V tolerant One dedicated ATC indicator (5 mA)
LPG	8-channel; enables blinking or strobing of LEDs and backlights
Controls for external current drivers	Three LPG outputs
Vibration motor driver	1.2 to 3.1 V in 100 mV increments
One-touch headset controller	Three, each supporting headset send/end detection and MIC bias
Keypad interface support	Up to 8 x 18 keys
Extra features	Joystick support
IC-level interfaces	
Primary status and control	SSBI Forward clock from the MSM device enables SSBI even when PMIC XO is off
Interrupt managers	Three: modem, secure applications processor, and user applications processor
Optional hardware configurations	OPT bits select hardware configuration
Power sequencing	Poweron, poweroff, and soft resets
UIM support	Level translation and UIM removal and insertion detection
Extra features	External SMPS enable; 3:1 UART multiplexer
Configurable I/Os	
MPPs	12; configurable as digital inputs or outputs; level-translating bidirectional I/Os; analog multiplexer inputs; or VREF analog outputs
GPIO pins	44; configurable as digital inputs or outputs or level-translating I/Os; these configurable I/Os are much faster than MPPs
Package	
Size	7.8 mm × 7.8 mm × 0.88 mm
Pin count and package type	251-pin NSP

1.4 Terms and acronyms

The following table defines terms and acronyms used throughout this document.

Table 1-3 Terms and acronyms

Term or acronym	Definition
ADC	Analog-to-digital converter
API	Application programming interface
ATC	Auto-trickle charger
AVS	Adaptive voltage scaling
BMS	Battery monitoring system
CDMA	Code Division Multiple Access
DVS	Dynamic voltage scaling
FT-SMPS	Fast transient SMPS
GPIO	General-purpose input/output
GSM	Global system for mobile communications
HF-SMPS	High frequency SMPS
HK	Housekeeping
HSED	Headset send/end detect
HS-USB	High-speed USB
ID	Identification
LDO	Low dropout (linear regulator)
Li	Lithium
LPG	Light pulse generator
MPP	Multipurpose pin
MSM™	Mobile Station Modem™ (trademarked by Qualcomm)
MUX	Multiplexer
NCP	Negative charge pump
NSP	Nano scale package
OTG	On-the-go
OVP	Over-voltage protection
PA	Power amplifier
PBM	Pulse burst modulation
PCB	Printed circuit board
PDA	Personal digital assistant
PFM	Pulse frequency modulation
PLL	Phase-locked loop
PM	Power management
PWM	Pulse width modulation

Table 1-3 Terms and acronyms (cont.)

Term or acronym	Definition
QCT	Qualcomm CDMA Technologies division
QSC™	Qualcomm Single-Chip ™ (trademarked by Qualcomm)
RCO	RC oscillator
RTC	Realtime clock
RUIM	Removable user identity module
SBI	Serial bus interface (3-wire unless designated as SSBI)
SMBC	Switched-mode battery charger
SMPL	Sudden momentary power loss
SMPS	Switched-mode power supply (DC-to-DC converter)
SSBI	Single-wire serial bus interface
SSC	SMPS step control
support.cdmatech.com	QCT website address for technical assistance
SVS	Static voltage scaline
TCXO	Temperature-compensated crystal oscillator
UART	Universal asynchronous receiver/transmitter
UICC	Universal integrated circuit card
UIM	User identity module
UMTS	Universal mobile telecommunications system
USB	Universal serial bus
UVLO	Under-voltage lockout
VCO	Voltage-controlled oscillator
VCTCXO	Voltage-controlled temperature-compensated crystal oscillator
XO	Crystal oscillator
Zero-IF or ZIF	Zero intermediate frequency

1.5 Special marks

Table 1-4 defines special marks used in this document.

Table 1-4 Special marks

Mark	Definition
[ ]	Brackets ([ ]) sometimes follow a pin, register, or bit name. These brackets enclose a range of numbers. For example, DATA [7:4] may indicate a range that is 4 bits in length, or DATA[7:0] may refer to eight DATA pins.
_N	A suffix of _N indicates an active low signal. For example, PON_RESET_N.
0x0000	Hexadecimal numbers are identified with an x in the number, (for example, 0x0000). All numbers are decimal (base 10) unless otherwise specified. Non-obvious binary numbers have the term binary enclosed in parentheses at the end of the number, [for example, 0011 (binary)].
|	A vertical bar in the outside margin of a page indicates that a change was made since the previous revision of this document.

2 Pin Definitions

The PM8921 IC is available in the 251 NSP that includes several ground pins. See Chapter 4 for package details. A high-level view of the pin assignments is shown in Figure 2-1.

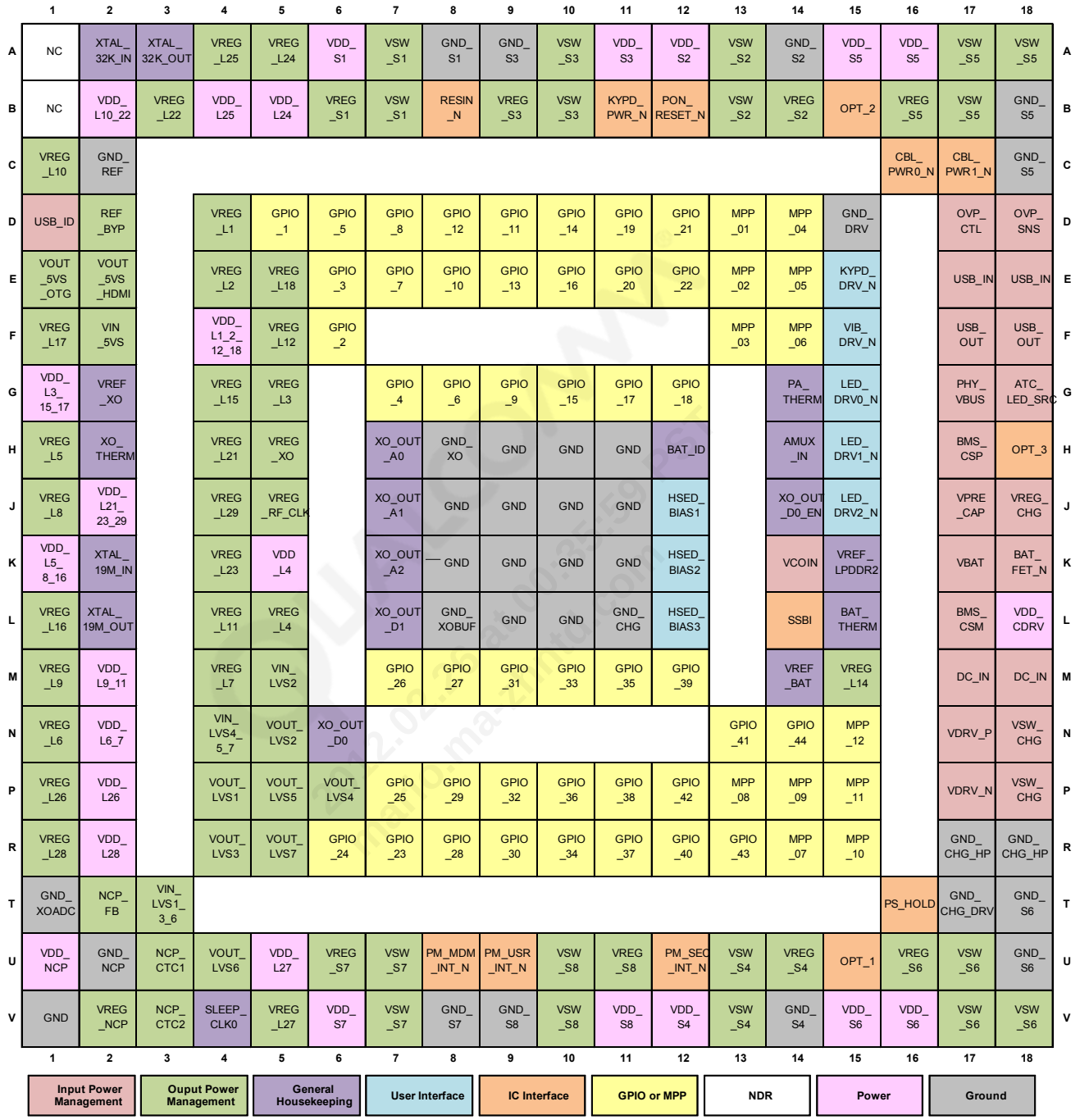


Figure 2-1 PM8921 IC pin assignments (top view)

2.1 I/O parameter definitions

Table 2-1 I/O description (pad type) parameters

Symbol	Description
Pad attribute	
AI	Analog input
AO	Analog output
DI	Digital input (CMOS)
DO	Digital output (CMOS)
HS	High speed
LS	Low speed
PI	Power input; an input pin that handles 10 mA or more [1]
PO	Power output; an output pin that handles 10 mA or more [1]
Z	High-impedance (high-Z) output
GPIO pins, when configured as inputs, have configurable pull settings	
NP	No internal pull enabled
PU	Internal pull-up enabled
PD	Internal pull-down enabled
GPIO pins, when configured as outputs, have configurable drive strengths	
H	High: ~ 0.9 mA at 1.8 V; ~ 1.9 mA at 2.6 V
M	Medium: ~ 0.6 mA at 1.8 V; ~ 1.25 mA at 2.6 V
L	Low: ~ 0.15 mA at 1.8 V; ~ 0.3 mA at 2.6 V
Pad voltage groupings	
V_DIG0	Supply for first of two XO output buffers; connected internally to VREG_L2.
V_DIG1	Supply for second of two XO output buffers; connected internally to VREG_L7.
V_dVdd	Supply for internal digital logic; internally connected to VDD_L0_L1_LVS. All XO enable signals are supplied by V_dVDD, but they can be over-driven to 5.5 V for logic high. Even when over-driven, their logic thresholds (V_{IH} and V_{IL}) are still referenced to V_dVdd.
V_XX	Selectable supply for GPIO circuits; options include: V_G0 = VPH_PWR (VIN_L4) V_G1 = VIN from output of 3.3 V buck boost or from VPH_PWR if no buck-boost is used V_G2 = S4 (1.8 V) V_G3 = LDO15 (2.85V or 1.8 V) V_G4 = LDO4 (1.8V) V_G5 = LDO3 (3.075V) V_G6 = LDO 17 (2.85 V or 1.8V) V_G7 = Reserved

Table 2-1 I/O description (pad type) parameters (cont.)

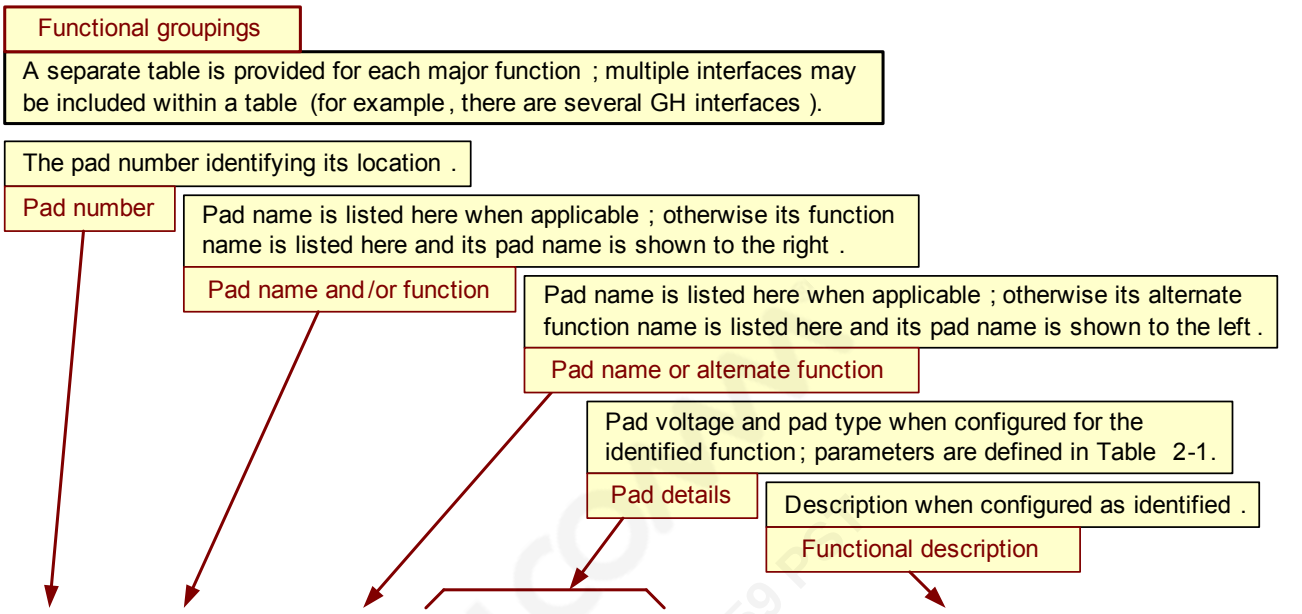
Symbol	Description
V_YY	Selectable supply for MPP circuits; options include: V_M0 = S1 (1.225 V) V_M1 = S4 (1.8 V) V_M3 = LDO15 (2.85 V or 1.8 V) V_M4 = LDO 17 (2.85 V or 1.8 V) V_M7 = VPH_PWR (VIN_L4)
V_XO	Crystal oscillator (XO) supply voltage
V_VDD	VPH_PWR

1. The maximum current levels expected on PI and PO type pads are listed in Table 2-2.

Table 2-2 Expected maximum currents at PI and PO pad types

Pad #	Function	Type	Current (mA) [1]	Pad #	Function	Type	Current (mA) [1]
E15	KYPD_DRV_N	PI	300	A7, B7, B6	S1	PO	1500
G15	LED_DRV0_N	PI	40	A13, B13, B14	S2	PO	1500
H15	LED_DRV1_N	PI	40	A10, B10, B9	S3	PO	1500
J15	LED_DRV2_N	PI	40	U13, V13, U14	S4	PO	1500
P4	VOUT_LVS1	PO	100	A17, B17, A18, B16	S5	PO	2000
N5	VOUT_LVS2	PO	300	U17, V17, V18, U16	S6	PO	2000
R4	VOUT_LVS3	PO	100	U7, V7, U6	S7	PO	1500
P6	VOUT_LVS4	PO	100	U10, V10, U11	S8	PO	1500
P5	VOUT_LVS5	PO	100	D4	VREG_L1	PO	150
U4	VOUT_LVS6	PO	100	E4	VREG_L2	PO	150
R5	VOUT_LVS7	PO	100	G5	VREG_L3	PO	150*/50
E1	VOUT_5VS_OTG	PO	50	L5	VREG_L4	PO	50
E2	VOUT_5VS_HMDI	PO	100	H1	VREG_L5	PO	300
L4	VREG_L11	PO	150	N1	VREG_L6	PO	600
F5	VREG_L12	PO	150	M4	VREG_L7	PO	150
M15	VREG_L14	PO	50	J1	VREG_L8	PO	300
G4	VREG_L15	PO	150	M1	VREG_L9	PO	300
L1	VREG_L16	PO	300	C1	VREG_L10	PO	600
F1	VREG_L17	PO	150				
E5	VREG_L18	PO	150				
H4	VREG_L21	PO	150				
B3	VREG_L22	PO	150				
K4	VREG_L23	PO	150				
A5	VREG_L24	PO	1200				
A4	VREG_L25	PO	1200				
P1	VREG_L26	PO	1200				
V5	VREG_L27	PO	1200				
R1	VREG_L28	PO	1200				
J4	VREG_L29	PO	150				
H5	VREG_XO	PO	5				
J5	VREG_RF_CLK	PO	5				

1. Listed current is the expected maximum.



Pad #	Pad name and/or function	Pad name or alt function	Pad voltage	Pad type	Functional description
Analog multiplexer and HK/ XO ADC circuits					
G2	XOADC_REF		---	AO	Reference voltage for the XO ADC circuits
G12	CDMA_HDET	MPP_03	V_YY	AI DO-Z	Amux input - CDMA power detector Configurable input/output, MPP type.
G13	ALS	MPP_04	V_YY	AI DO-Z	Amux input - ambient light sensor Configurable input/output, MPP type.
G13	IR_PROX_RX			AI DO-Z	Amux input - infra-red sensor Configurable input/output, MPP type.
H13	CHG2_DET	MPP_06	V_YY	AI DO-Z	Amux input - dual charger detection Configurable input/output, MPP type.
J12	BATT_THERM	MPP_07	V_YY	AI DO-Z	Amux input - battery thermistor output Configurable input/output, MPP type.
J13	BATT_ID	MPP_08	V_YY	AI DO-Z	Amux input - battery ID output Configurable input/output, MPP type.
K13	XO_THERM	MPP_09	V_YY	AI DO-Z	Amux input - XO thermistor output; a more direct XO ADC connection Configurable input/output, MPP type.
L13	PA_THERM	MPP_10	V_YY	AI DO-Z	Amux input - PA thermistor output Configurable input/output, MPP type.
In addition to the MPPs listed above, MPP_01, MPP_02, and MPP_05 can be configured as amux inputs					
19.2 MHz XO circuits					
A2	XTAL_19M_IN		V_XO	AI	19.2 MHz crystal input.
A3	XTAL_19M_OUT		V_XO	AO	19.2 MHz crystal output
B7	XO_OUT_A0_EN		V_DIG0	DI	19.2 MHz XO digital output enable, first of two.
D8	XO_OUT_A0		V_XO	DO	19.2 MHz XO digital output, first of two; 0.8 to 2.0 Vpp.
D6	XO_OUT_A1_EN		V_PAD	DI	19.2 MHz XO digital output enable, second of two
D7	XO_OUT_A1		V_XO	DO	19.2 MHz XO digital output, second of two; 0.5 to 1.0 Vpp.

Pad # and pad name are always in the same row

Figure 2-2 Definitions of pin table parameters

2.2 Pin descriptions

Descriptions of all pins are presented in the following tables, organized by functional group:

Table 2-3 Pin descriptions – input power management functions

Pad #	Pad name and/or function	Pad function and/or name	Pad V	Pad type	Functional description
USB charger and OTG switch					
E17	USB_IN		–	PI	Input power from USB source (1 of 2).
E18	USB_IN		–	PI	Input power from USB source (2 of 2).
F17	USB_OUT		–	PO	Protected output via USB source (1 of 2).
F18	USB_OUT		–	PO	Protected output via USB source (2 of 2).
G17	PHY_VBUS		–	PO	Gated (protected) supply to USB_PHY.
D1	USB_ID		–	AI	USB identification input.
Wall charger					
M17	DC_IN		–	PI	Protected V_IN from wall charger; input to charger SMPS circuits (1 of 2).
M18	DC_IN		–	PI	Protected V_IN from wall charger; input to charger SMPS circuits (2 of 2).
D18	OVP_SNS		–	AI	Input voltage from wall charger for sense.
D17	OVP_CTL		–	AO	Control voltage to external OVP FET.

Table 2-3 Pin descriptions – input power management functions (cont.)

Pad #	Pad name and/or function	Pad function and/or name	Pad V	Pad type	Functional description
SMBC circuits					
M17	DC_IN		–	PI	Protected V_IN from wall charger; input to charger SMPS circuits (1 of 2).
M18	DC_IN		–	PI	Protected V_IN from wall charger; input to charger SMPS circuits (2 of 2).
N18	VSW_CHG		–	PO	Charger SMPS switching output (1 of 2).
P18	VSW_CHG		–	PO	Charger SMPS switching output (2 of 2).
J18	VREG_CHG		–	AI	Charger SMPS sense point (VPH_PWR).
N17	VDRV_P		–	AI	Buck driver high-side bypass capacitor.
P17	VDRV_N		–	AI	Buck driver low-side bypass capacitor.
J17	VPRE_CAP		–	AO	VPRE regulator load capacitor.
BMS circuits					
K18	BAT_FET_N		–	AO	External battery MOSFET control.
K17	VBAT		–	AI, AO	Battery sense input; trickle charge output.
G18	ATC_LED_SRC		–	AO	Auto-trickle charge indicator LED supply.
M14	VREF_BAT		–	AO	Reference voltage for battery sensors.
L15	BAT_THERM		–	AI	AMUX direct input 1 – battery thermistor.
H12	BAT_ID		–	AI	AMUX direct input 2 – battery ID.
H17	BMS_CSP		–	AI	Battery current sense – plus.
L17	BMS_CSM		–	AI	Battery current sense – minus.
coincell or keep-alive battery					
K14	VCOIN		–	AI, AO	Sense input or charge output.

Table 2-4 Pin descriptions – output power management functions

Pad #	Pad name and/or function	Pad function and/or name	Pad V	Pad type	Functional description
SMPS circuits					
A7	VSW_S1		–	PO	S1 SMPS switching output (1 of 2).
B7	VSW_S1		–	PO	S1 SMPS switching output (2 of 2).
B6	VREG_S1		–	AI	S1 SMPS sense point.
A13	VSW_S2		–	PO	S2 SMPS switching output (1 of 2).
B13	VSW_S2		–	PO	S2 SMPS switching output (2 of 2).
B14	VREG_S2		–	AI	S2 SMPS sense point.
A10	VSW_S3		–	PO	S3 SMPS switching output (1 of 2).
B10	VSW_S3		–	PO	S3 SMPS switching output (2 of 2).
B9	VREG_S3		–	AI	S3 SMPS sense point.
U13	VSW_S4		–	PO	S4 SMPS switching output (1 of 2).
V13	VSW_S4		–	PO	S4 SMPS switching output (2 of 2).
U14	VREG_S4		–	AI	S4 SMPS sense point.
A17	VSW_S5		–	PO	S5 SMPS switching output (1 of 3).
A18	VSW_S5		–	PO	S5 SMPS switching output (2 of 3).
B17	VSW_S5		–	PO	S5 SMPS switching output (3 of 3).
B16	VREG_S5		–	AI	S5 SMPS sense point.
U17	VSW_S6		–	PO	S6 SMPS switching output (1 of 3).
V17	VSW_S6		–	PO	S6 SMPS switching output (2 of 3).
V18	VSW_S6		–	PO	S6 SMPS switching output (3 of 3).
U16	VREG_S6		–	AI	S6 SMPS sense point.
U7	VSW_S7		–	PO	S7 SMPS switching output (1 of 2).
V7	VSW_S7		–	PO	S7 SMPS switching output (2 of 2).
U6	VREG_S7		–	AI	S7 SMPS sense point.
U10	VSW_S8		–	PO	S8 SMPS switching output (1 of 2).
V10	VSW_S8		–	PO	S8 SMPS switching output (2 of 2).
U11	VREG_S8		–	AI	S8 SMPS sense point.

Table 2-4 Pin descriptions – output power management functions (cont.)

Pad #	Pad name and/or function	Pad function and/or name	Pad V	Pad type	Functional description
LDO linear regulators					
D4	VREG_L1		–	PO	Linear regulator L1 output.
E4	VREG_L2		–	PO	Linear regulator L2 output.
G5	VREG_L3		–	PO	Linear regulator L3 output.
L5	VREG_L4		–	PO	Linear regulator L4 output.
H1	VREG_L5		–	PO	Linear regulator L5 output.
N1	VREG_L6		–	PO	Linear regulator L6 output.
M4	VREG_L7		–	PO	Linear regulator L7output.
J1	VREG_L8		–	PO	Linear regulator L8 output.
M1	VREG_L9		–	PO	Linear regulator L9 output.
C1	VREG_L10		–	PO	Linear regulator L10 output.
L4	VREG_L11		–	PO	Linear regulator L11 output.
F5	VREG_L12		–	PO	Linear regulator L12 output.
M15	VREG_L14		–	PO	Linear regulator L14 output.
G4	VREG_L15		–	PO	Linear regulator L15 output.
L1	VREG_L16		–	PO	Linear regulator L16 output.
F1	VREG_L17		–	PO	Linear regulator L17 output.
E5	VREG_L18		–	PO	Linear regulator L18 output.
H4	VREG_L21		–	PO	Linear regulator L21 output.
B3	VREG_L22		–	PO	Linear regulator L22 output.
K4	VREG_L23		–	PO	Linear regulator L23 output.
A5	VREG_L24		–	PO	Linear regulator L24 output.
A4	VREG_L25		–	PO	Linear regulator L25 output.
P1	VREG_L26		–	PO	Linear regulator L26 output.
V5	VREG_L27		–	PO	Linear regulator L27 output.
R1	VREG_L28		–	PO	Linear regulator L28 output.
J4	VREG_L29		–	PO	Linear regulator L29 output.
J5	VREG_RF_CLK		–	PO	Linear regulator output for RF clock buffers; internal use only.
H5	VREG_XO		–	PO	Linear regulator output for XO circuits; internal use only.

Table 2-4 Pin descriptions – output power management functions (cont.)

Pad #	Pad name and/or function	Pad function and/or name	Pad V	Pad type	Functional description
NCP circuits					
U3	NCP_CTC1		–	AI, AO	NCP charge transfer capacitor 1.
V3	NCP_CTC2		–	AI, AO	NCP charge transfer capacitor 2.
T2	NCP_FB		–	AI	NCP feedback (sense) input.
V2	VREG_NCP		–	PO	NCP output voltage.
Bandgap voltage reference (VREF) circuits					
D2	REF_BYP		–	AO	Bandgap reference circuit bypass cap.
LVS circuits					
T3	VIN_LVS1_3_6		–	PI	Low voltage switches 1, 3, and 6 inputs.
P4	VOUT_LVS1		–	PO	Low voltage switch 1 output.
R4	VOUT_LVS3		–	PO	Low voltage switch 3 output.
U4	VOUT_LVS6		–	PO	Low voltage switch 6 output.
M5	VIN_LVS2		–	PI	Low voltage switch 2 input.
N5	VOUT_LVS2		–	PO	Low voltage switch 2 output.
N4	VIN_LVS4_5_7		–	PI	Low voltage switches 4, 5, and 7 inputs.
P6	VOUT_LVS4		–	PO	Low voltage switch 4 output.
P5	VOUT_LVS5		–	PO	Low voltage switch 5 output.
R5	VOUT_LVS7		–	PO	Low voltage switch 7 output.
F2	VIN_5VS		–	PI	5 V switch input.
E1	VOUT_5VS_OTG		–	PO	5 V switch output for OTG.
E2	VOUT_5VS_HDMI		–	PO	5 V switch output for HDMI.

Table 2-5 Pin descriptions – general housekeeping functions

Pad #	Pad name and/or function	Pad function and/or name	Pad V	Pad type	Functional description
Analog multiplexer and HK/XO ADC circuits					
G2	VREF_XO		–	AO	Reference voltage for XO thermistor.
H2	XO_THERM		–	AI	ADC input – XO thermistor.
K15	VREF_LPDDR2		–	AO	Reference voltage for LPDDR2 memory.
M14	VREF_BAT		–	AO	Reference voltage for battery sensors.
L15	BAT_THERM		–	AI	AMUX direct input 1 – battery thermistor.
H12	BAT_ID		–	AI	AMUX direct input 2 – battery ID.
G14	PA_THERM		–	AI	AMUX direct input 3 – PA thermistor.
H14	AMUX_IN		–	AI	AMUX direct input 4 - hardware ID
19.2 MHz XO circuits					
K2	XTAL_19M_IN		V_XO	AI	19.2 MHz crystal input.
L2	XTAL_19M_OUT		V_XO	AO	19.2 MHz crystal output.
H7	XO_OUT_A0		V_XO	DO	Low noise XO output 0.
J7	XO_OUT_A1		V_XO	DO	Low noise XO output 1.
K7	XO_OUT_A2		V_XO	DO	Low noise XO output 2.
N6	XO_OUT_D0		V_PAD	DO	Low power XO output 0.
J14	XO_OUT_D0_EN		V_PAD	DI	Low power XO output 0 enable.
L7	XO_OUT_D1		V_XX	DO	Low power XO output 1.

Table 2-5 Pin descriptions – general housekeeping functions (cont.)

Pad #	Pad name and/or function	Pad function and/or name	Pad V	Pad type	Functional description
32.768 kHz XTAL, sleep clock, and MP3 clock circuits					
A2	XTAL_32K_IN		–	AI	32.768 kHz crystal input.
A3	XTAL_32K_OUT		–	AO	32.768 kHz crystal output.
V4	SLEEP_CLK0		V_PAD	DO	Sleep clock output – modem IC and others.
R13	SLEEP_CLK1	GPIO_43 [1]	V_XX	LS-DO DO-Z	Extra sleep clock 1 output. Configurable GPIO_43.
N14	SLEEP_CLK2	GPIO_44 [1]	V_XX	LS-DO DO-Z	Extra sleep clock 2 output. Configurable GPIO_44.
R13	MP3_CLK1	GPIO_43 [1]	V_XX	HS-DO DO-Z	Low power clock out; TCXO/8 or /16. Configurable GPIO_43.
N14	MP3_CLK2	GPIO_44 [1]	V_XX	HS-DO DO-Z	Low power clock out; TCXO/8 or /16. Configurable GPIO_44.
M12	CLK_FWD_MSM	GPIO_39 [1]	V_XX	HS-DO DO-Z	SSBI clock in sleep mode Configurable GPIO_39.
VREF output					
F14	VREF_DAC	MPP_06 [1]	–	AO AO-Z	Reference for modem IC combo DAC. Configurable MPP_06; default high-Z out.
E14	VREF_PADS	MPP_05 [1]	–	AO AO-Z	Reference for modem IC 3 V I/Os. Configurable MPP_05; default high-Z out.

1. To assign a GPIO particular function (like the one listed here), identify all of your application's requirements and map each GPIO to its function – carefully avoiding assignment conflicts. All GPIOs are listed in Table 2-8.

Table 2-6 Pin descriptions – user interface functions

Pad #	Pad name and/or function	Pad function and/or name	Pad V	Pad type	Functional description
Current drivers					
E15	KYPD_DRV_N		–	PO	Keypad backlight driver output.
J15	LED_DRV2_N		–	PO AO	LED driver output 2.
H15	LED_DRV1_N		–	PO	LED driver output 1.
G15	LED_DRV0_N	LED_ATC	–	PO	LED driver output 0. Auto trickle charger indicator output
M7	LPG_DRV3	GPIO_26 [1]	V_XX	HS-DO DO-Z	LPG driver enable 3. Configurable GPIO_26.
P7	LPG_DRV2	GPIO_25 [1]	V_XX	HS-DO DO-Z	LPG driver enable 2. Configurable GPIO_25.
R6	LPG_DRV1	GPIO_24 [1]	V_XX	HS-DO DO-Z	LPG driver enable 1. Configurable GPIO_24.
Vibration motor driver					
F15	VIB_DRV_N		–	PO	Vibration motor driver output control.
Keypad interface					
M7	KYPD_DRV18	GPIO_26 [1]	V_XX	LS-DO DO-Z	Keypad drive bit 18. Configurable GPIO_26.
P7	KYPD_DRV17	GPIO_25 [1]	V_XX	LS-DO DO-Z	Keypad drive bit 17. Configurable GPIO_25.
R6	KYPD_DRV16	GPIO_24 [1]	V_XX	LS-DO DO-Z	Keypad drive bit 16. Configurable GPIO_24.
R7	KYPD_DRV15	GPIO_23 [1]	V_XX	LS-DO DO-Z	Keypad drive bit 15. Configurable GPIO_23.
E12	KYPD_DRV14	GPIO_22 [1]	V_XX	LS-DO DO-Z	Keypad drive bit 14. Configurable GPIO_22.
D12	KYPD_DRV13	GPIO_21 [1]	V_XX	LS-DO DO-Z	Keypad drive bit 13. Configurable GPIO_21.
E11	KYPD_DRV12	GPIO_20 [1]	V_XX	LS-DO DO-Z	Keypad drive bit 12. Configurable GPIO_20.
D11	KYPD_DRV11	GPIO_19 [1]	V_XX	LS-DO DO-Z	Keypad drive bit 11. Configurable GPIO_19.
G12	KYPD_DRV10	GPIO_18 [1]	V_XX	LS-DO DO-Z	Keypad drive bit 10. Configurable GPIO_18.
G11	KYPD_DRV9	GPIO_17 [1]	V_XX	LS-DO DO-Z	Keypad drive bit 9. Configurable GPIO_17.

Table 2-6 Pin descriptions – user interface functions (cont.)

Pad #	Pad name and/or function	Pad function and/or name	Pad V	Pad type	Functional description
E10	KYPD_DRV8	GPIO_16 [1]	V_XX	LS-DO DO-Z	Keypad drive bit 8. Configurable GPIO_16.
G10	KYPD_DRV7	GPIO_15 [1]	V_XX	LS-DO DO-Z	Keypad drive bit 7. Configurable GPIO_15.
D10	KYPD_DRV6	GPIO_14 [1]	V_XX	LS-DO DO-Z	Keypad drive bit 6. Configurable GPIO_14.
E9	KYPD_DRV5	GPIO_13 [1]	V_XX	LS-DO DO-Z	Keypad drive bit 5. Configurable GPIO_13.
D8	KYPD_DRV4	GPIO_12 [1]	V_XX	LS-DO DO-Z	Keypad drive bit 4. Configurable GPIO_12.
D9	KYPD_DRV3	GPIO_11 [1]	V_XX	LS-DO DO-Z	Keypad drive bit 3. Configurable GPIO_11.
E8	KYPD_DRV2	GPIO_10 [1]	V_XX	LS-DO DO-Z	Keypad drive bit 2. Configurable GPIO_10.
G9	KYPD_DRV1	GPIO_9 [1]	V_XX	LS-DO DO-Z	Keypad drive bit 1. Configurable GPIO_9.
D7	KYPD_SNS8	GPIO_8 [1]	V_XX	LS-DI DO-Z	Keypad sense bit 8. Configurable GPIO_8.
E7	KYPD_SNS7	GPIO_7 [1]	V_XX	LS-DI DO-Z	Keypad sense bit 7. Configurable GPIO_7.
G8	KYPD_SNS6	GPIO_6 [1]	V_XX	LS-DI DO-Z	Keypad sense bit 6. Configurable GPIO_6.
D6	KYPD_SNS5	GPIO_5 [1]	V_XX	LS-DI DO-Z	Keypad sense bit 5. Configurable GPIO_5.
G7	KYPD_SNS4	GPIO_4 [1]	V_XX	LS-DI DO-Z	Keypad sense bit 4. Configurable GPIO_4.
E6	KYPD_SNS3	GPIO_3 [1]	V_XX	LS-DI DO-Z	Keypad sense bit 3. Configurable GPIO_3.
F6	KYPD_SNS2	GPIO_2 [1]	V_XX	LS-DI DO-Z	Keypad sense bit 2. Configurable GPIO_2.
D5	KYPD_SNS1	GPIO_1 [1]	V_XX	LS-DI DO-Z	Keypad sense bit 1. Configurable GPIO_1.

Table 2-6 Pin descriptions – user interface functions (cont.)

Pad #	Pad name and/or function	Pad function and/or name	Pad V	Pad type	Functional description
Headset send/end detect and microphone bias					
J12	HSED_BIAS1		–	AI, AO	HSED input and mic bias output (1 of 3).
K12	HSED_BIAS2		–	AI, AO	HSED input and mic bias output (2 of 3).
L12	HSED_BIAS3		–	AI, AO	HSED input and mic bias output (3 of 3).

1. To assign a GPIO particular function (like the one listed here), identify all of your application's requirements and map each GPIO to its function – carefully avoiding assignment conflicts. All GPIOs are listed in Table 2-8.

Table 2-7 Pin descriptions – IC-level interface functions

Pad #	Pad name and/or function	Pad function and/or name	Pad V	Pad type	Functional description
Poweron circuits					
C16	CBL_PWR0_N		V_INT	DI	Cable poweron detect bit 0.
C17	CBL_PWR1_N		V_INT	DI	Cable poweron detect bit 1.
B11	KYPD_PWR_N		V_INT	DI	Keypad poweron detect input (gnd sw).
H18	OPT_3		V_INT	DI	Option HW configuration control bit 3.
B15	OPT_2		V_INT	DI	Option HW configuration control bit 2.
U15	OPT_1		V_INT	DI	Option HW configuration control bit 1.
T16	PS_HOLD		V_PAD	DI	Power supply hold control input.
B8	RESIN_N		V_INT	DI	PMIC reset input.
B12	PON_RESET_N		V_PAD	DO	Poweron reset output control.
N13	EXT_REG_EN2	GPIO_41 [1]	V_XX	LS-DO LS-DO	External regulator enable 2 at poweron. Configurable GPIO_41; special default.
R12	EXT_REG_EN1	GPIO_40 [1]	V_XX	LS-DO LS-DO	External regulator enable 1 at poweron. Configurable GPIO_40; special default.
Primary PM/modem IC interface signals					
L14	SSBI		V_PAD	DI, DO	Single-wire serial bus interface.
M12	FCLK	GPIO_39 [1]	V_XX	HS-DI DO-Z	Forward clock; XO substitute for SBI. Configurable GPIO_39.
U8	PM_MDM_INT_N		V_PAD	DO	Modem standard interrupt.
U12	PM_SEC_INT_N		V_PAD	DO	Modem application processor secure interrupt.
U9	PM_USR_INT_N		V_PAD	DO	Modem application processor user interrupt.
UIM interfaces					
R9	UIM1_CLK	GPIO_30 [1]	V_XX	LS-DO DO-Z	Module-side UICC 1 clock signal. Configurable GPIO_30.

Table 2-7 Pin descriptions – IC-level interface functions (cont.)

Pad #	Pad name and/or function	Pad function and/or name	Pad V	Pad type	Functional description
P8	UIM1_M_CLK	GPIO_29 [1]	V_XX	LS-DI DO-Z	MSM-side UICC 1 clock signal. Configurable GPIO_29.
E13	UIM1_DATA	MPP_02 [2]	V_YY –	LS-DI/DO AO-Z	Module-side UICC 1 data signal. Configurable MPP 2; default high-Z out.
D13	UIM1_M_DATA	MPP_01 [2]	V_YY –	LS-DI/DO AO-Z	MSM-side UICC 1 data signal. Configurable MPP 1; default high-Z out.
M8	UIM1_RST	GPIO_27 [1]	V_XX	LS-DI DO-Z	Module-side UICC 1 reset signal. Configurable.
P10	UIM1_RMV_DET_N	GPIO_36	V_XX	DI-Z	Module-side UIM1 remove detect signal
P9	UIM2_CLK	GPIO_32 [1]	V_XX	LS-DO DO-Z	Module-side UICC 2 clock signal. Configurable GPIO_32.
M9	UIM2_M_CLK	GPIO_31 [1]	V_XX	LS-DI DO-Z	MSM-side UICC 2 clock signal. Configurable GPIO_31.
D14	UIM2_DATA	MPP_04 [2]	V_YY –	LS-DI/DO AO-Z	Module-side UICC 2 data signal. Configurable MPP 4; default high-Z out.
F13	UIM2_M_DATA	MPP_03 [2]	V_YY –	LS-DI/DO AO-Z	MSM-side UICC 2 data signal. Configurable MPP 3; default high-Z out.
R8	UIM2_RST	GPIO_28 [1]	V_XX	LS-DO DO-Z	Module-side UICC 2 reset signal. Configurable GPIO_28.
R11	UIM2_RMV_DET_N	GPIO_37	V_XX	DI-Z	Module-side UIM2 remove detect signal
UART multiplexing					
M10	UART_RX1	GPIO_33 [1]	V_XX	HS-DI DO-Z	UART3:1 MUX module-side Rx1 signal. Configurable GPIO_33.
R10	UART_RX2	GPIO_34 [1]	V_XX	HS-DI DO-Z	UART3:1 MUX module-side Rx2 signal. Configurable GPIO_34.
M11	UART_RX3	GPIO_35 [1]	V_XX	HS-DI DO-Z	UART3:1 MUX module-side Rx3 signal. Configurable GPIO_35.
P11	UART_M_RX	GPIO_38 [1]	V_XX	HS-DO DO-Z	UART3:1 MUX MSM-side Rx signal. Configurable GPIO_38.
D12	UART_TX1	GPIO_21 [1]	V_XX	HS-DO DO-Z	UART3:1 MUX module-side Tx1 signal. Configurable GPIO_21.
E12	UART_TX2	GPIO_22 [1]	V_XX	HS-DO DO-Z	UART3:1 MUX module-side Tx2 signal. Configurable GPIO_22.
R7	UART_TX3	GPIO_23 [1]	V_XX	HS-DO DO-Z	UART3:1 MUX module-side Tx3 signal. Configurable GPIO_23.
D7	UART_M_TX	GPIO_8 [1]	V_XX	HS-DI DI-Z	UART3:1 MUX MSM-side Tx signal. Configurable GPIO_8.

1. To assign a GPIO particular function (like the one listed here), identify all of your application's requirements and map each GPIO to its function – carefully avoiding conflicts. All GPIOs are listed in Table 2-8.
2. To assign a MPP particular function (like the one listed here), identify all of your application's requirements and map each MPP to its function – carefully avoiding conflicts. All MPPs are listed in Table 2-8.

Table 2-8 Pin descriptions – configurable input/output functions

Pad #	Pad name and/or function	Pad function and/or name	Pad V	Pad type	Functional description
MPPs					
D13	MPP_01	UIM1_M_DATA	V_YY	AO-Z LS-DI/DO AI	Configurable MPP 1; default high-Z out. MSM-side UICC 1 data signal. Analog input for routing analog signals to AMUX/HKADC.
E13	MPP_02	UIM1_DATA	V_YY	AO-Z LS-DI/DO AI	Configurable MPP 2; default high-Z out. Module-side UICC 1 data signal. Analog input for routing analog signals to AMUX/HKADC.
F13	MPP_03	UIM2_M_DATA	V_YY	AO-Z LS-DI/DO AI	Configurable MPP 3; default high-Z out. MSM-side UICC 2 data signal. Analog input for routing analog signals to AMUX/HKADC.
D14	MPP_04	UIM2_DATA	V_YY	AO-Z LS-DI/DO AI	Configurable MPP 4; default high-Z out. Module-side UICC 2 data signal. Analog input for routing analog signals to AMUX/HKADC.
E14	MPP_05	VREF_PADS		AO-Z AO AI	Configurable MPP 5; defaults to 1.25 V at PON. Reference for modem IC 3 V I/Os. Analog input for routing analog signals to AMUX/HKADC.
F14	MPP_06	VREF_DAC		AO-Z AO AI	Configurable MPP 6; default high-Z out. Reference for modem IC combo DAC. Analog input for routing analog signals to AMUX/HKADC.
R14	MPP_07			AO-Z AI	Configurable MPP 7; default high-Z out. Analog input for routing analog signals to AMUX/HKADC.
P13	MPP_08			AO-Z AI	Configurable MPP 8; default high-Z out. Analog input for routing analog signals to AMUX/HKADC.
P14	MPP_09	XO_OUT_D1_EN		AO AI DI DO	Analog input for routing analog signals to AMUX/HKADC.

Table 2-8 Pin descriptions – configurable input/output functions (cont.)

Pad #	Pad name and/or function	Pad function and/or name	Pad V	Pad type	Functional description
R15	MPP_10	XO_OUT_A0_EN		AO AI DI DO	Analog input for routing analog signals to AMUX/HKADC.
P15	MPP_11	XO_OUT_A1_EN		AO AI DI DO	Analog input for routing analog signals to AMUX/HKADC.
N15	MPP_12	XO_OUT_A2_EN		AO AI DI DO	Analog input for routing analog signals to AMUX/HKADC.
Predefined GPIO functions – available only at the assigned GPIOs					
D5	GPIO_1	KYPD_SNS1	V_XX	DO-Z LS-DI	Configurable GPIO_1. Keypad sense bit 1.
F6	GPIO_2	KYPD_SNS2	V_XX	DO-Z LS-DI	Configurable GPIO_2. Keypad sense bit 2.
E6	GPIO_3	KYPD_SNS3	V_XX	DO-Z LS-DI	Configurable GPIO_3. Keypad sense bit 3.
G7	GPIO_4	KYPD_SNS4	V_XX	DO-Z LS-DI	Configurable GPIO_4. Keypad sense bit 4.
D6	GPIO_5	KYPD_SNS5	V_XX	DO-Z LS-DI	Configurable GPIO_5. Keypad sense bit 5.
G8	GPIO_6	KYPD_SNS6	V_XX	DO-Z LS-DI	Configurable GPIO_6. Keypad sense bit 6.
E7	GPIO_7	KYPD_SNS7	V_XX	DO-Z LS-DI	Configurable GPIO_7. Keypad sense bit 7.
D7	GPIO_8	KYPD_SNS8 UART_M_TX	V_XX	DO-Z HS-DO	Configurable GPIO_8. Low power clock out; TCXO/8 or /16.
G9	GPIO_9	KYPD_DRV1	V_XX	DO-Z LS-DO	Configurable GPIO_9. Keypad drive bit 1.
E8	GPIO_10	KYPD_DRV2	V_XX	DO-Z LS-DO	Configurable GPIO_10. Keypad drive bit 2.
D9	GPIO_11	KYPD_DRV3	V_XX	DO-Z LS-DO	Configurable GPIO_11. Keypad drive bit 3.
D8	GPIO_12	KYPD_DRV4	V_XX	DO-Z LS-DO	Configurable GPIO_12. Keypad drive bit 4.

Table 2-8 Pin descriptions – configurable input/output functions (cont.)

Pad #	Pad name and/or function	Pad function and/or name	Pad V	Pad type	Functional description
E9	GPIO_13	KYPD_DRV5	V_XX	DO-Z LS-DO	Configurable GPIO_13. Keypad drive bit 5.
D10	GPIO_14	KYPD_DRV6	V_XX	DO-Z LS-DO	Configurable GPIO_14. Keypad drive bit 6.
G10	GPIO_15	KYPD_DRV7	V_XX	DO-Z LS-DO	Configurable GPIO_15. Keypad drive bit 7.
E10	GPIO_16	KYPD_DRV8	V_XX	DO-Z LS-DO	Configurable GPIO_16. Keypad drive bit 8.
G11	GPIO_17	KYPD_DRV9	V_XX	DO-Z LS-DO	Configurable GPIO_17. Keypad drive bit 9.
G12	GPIO_18	KYPD_DRV10	V_XX	DO-Z LS-DO	Configurable GPIO_18. Keypad drive bit 10.
D11	GPIO_19	KYPD_DRV11	V_XX	DO-Z LS-DO	Configurable GPIO_19. Keypad drive bit 11.
E11	GPIO_20	KYPD_DRV12	V_XX	DO-Z LS-DO	Configurable GPIO_20. Keypad drive bit 12.
D12	GPIO_21	KYPD_DRV13 UART_TX1	V_XX	DO-Z LS-DO HS-DO	Configurable GPIO_21. Keypad drive bit 13. UART3:1 MUX module-side Tx1 signal.
E12	GPIO_22	KYPD_DRV14 UART_TX2	V_XX	DO-Z LS-DO HS-DO	Configurable GPIO_22. Keypad drive bit 14. UART3:1 MUX module-side Tx2 signal.
R7	GPIO_23	KYPD_DRV15 UART_TX3	V_XX	DO-Z LS-DO HS-DO	Configurable GPIO_23. Keypad drive bit 15. UART3:1 MUX module-side Tx3 signal.
R6	GPIO_24	KYPD_DRV16 LPG_DRV1	V_XX	DO-Z LS-DO HS-DO	Configurable GPIO_24. Keypad drive bit 16. LPG driver enable 1.
P7	GPIO_25	KYPD_DRV17 LPG_DRV2	V_XX	DO-Z LS-DO HS-DO	Configurable GPIO_25. Keypad drive bit 17. LPG driver enable 2.
M7	GPIO_26	KYPD_DRV18 LPG_DRV3	V_XX	DO-Z LS-DO HS-DO	Configurable GPIO_26. Keypad drive bit 18. LPG driver enable 3.
M8	GPIO_27	UIM1_RST	V_XX	DO-Z LS-DI	Configurable GPIO_27. Module-side UICC 1 reset signal.
R8	GPIO_28	UIM2_RST	V_XX	DO-Z LS-DO	Configurable GPIO_28. Module-side UICC 2 reset signal.
P8	GPIO_29	UIM1_M_CLK	V_XX	DO-Z LS-DI	Configurable GPIO_29. MSM-side UICC 1 clock signal.

Table 2-8 Pin descriptions – configurable input/output functions (cont.)

Pad #	Pad name and/or function	Pad function and/or name	Pad V	Pad type	Functional description
R9	GPIO_30	UIM1_CLK	V_XX	DO-Z LS-DO	Configurable GPIO_30. Module-side UICC 1 clock signal.
M9	GPIO_31	UIM2_M_CLK	V_XX	DO-Z LS-DI	Configurable GPIO_31. MSM-side UICC 2 clock signal.
P9	GPIO_32	UIM2_CLK	V_XX	DO-Z LS-DO	Configurable GPIO_32. Module-side UICC 2 clock signal.
M10	GPIO_33	UART_RX1	V_XX	DO-Z HS-DI	Configurable GPIO_33. UART3:1 MUX module-side Rx1 signal.
R10	GPIO_34	UART_RX2	V_XX	DO-Z HS-DI	Configurable GPIO_34. UART3:1 MUX module-side Rx2 signal.
M11	GPIO_35	UART_RX3	V_XX	DO-Z HS-DI Hardware default = op	Configurable GPIO_35. UART3:1 MUX module-side Rx3 signal.
P10	GPIO_36	UIM1_RMV_DET_N	V_XX	DO-Z HS-DI	Configurable GPIO_36. UIM1 removal detection signal.
R11	GPIO_37	UIM2_RMV_DET_N	V_XX	DO-Z HS-DO	Configurable GPIO_37. UIM2 removal detection signal.
P11	GPIO_38	UART_M_RX	V_XX	DO-Z	Configurable GPIO_38.
M12	GPIO_39	FCLK	V_XX	DO-Z HS-DI	Configurable GPIO_39. Forward clock; XO substitute for SBI.
R12	GPIO_40	EXT_REG_EN1	V_XX	LS-DO LS-DO	Configurable GPIO_40; special default. External regulator enable 1 at poweron.
N13	GPIO_41	EXT_REG_EN2	V_XX	DO-Z LS-DO	Configurable GPIO_41; special default. External regulator enable 2 at poweron.
P12	GPIO_42		V_XX	DO-Z	Configurable GPIO_42.
R13	GPIO_43	MP3_CLK SLEEP_CLK1 MP3_CLK1	V_XX	DO-Z	Configurable GPIO_43. This GPIO can be referenced only to 1.8 V.
N14	GPIO_44	MP3_CLK SLEEP_CLK2 MP3_CLK2	V_XX	DO-Z	Configurable GPIO_44. This GPIO can be referenced only to 1.8 V.

NOTE All MPPs and GPIOs except MPP2, MPP4, GPIO_27, GPIO_28, GPIO_30, GPIO_32, GPIO_40, and GPIO_41 default to their high-Z state at powerup, and must be configured after powerup for their intended purposes.

NOTE Configure unused MPPs as 0 mA current sinks (high-Z) and GPIOs as digital inputs with their internal pull-downs enabled.

Table 2-9 Pin descriptions – no connect, do not connect, and reserved

Pad #	Pad name	Functional description
A1, B1	NC	No connect; not connected internally

Table 2-10 Pin descriptions – input DC power

Pad #	Pad name	Functional description
E17, E18	USB_IN	Power supply from USB charger to buck circuits
M17, M18	DC_IN	Power supply from wall charger to buck circuits
L18	VDD_CDRV	Power supply for charger's buck power FET driver
F4	VDD_L1_2_12_18	Power supply for L1, L2, L12, and L18 LDO circuits; also powers digital interface pins to/from modem IC.
G1	VDD_L3_15_17	Power supply for L3, L15, and L17 LDO circuits
K5	VDD_L4_L14_spLDO	Power supply for L4, L14, RF_CLK, and VREG_XO LDO circuits
K1	VDD_L5_8_16	Power supply for L5, L8, and L16 LDO circuits
N2	VDD_L6_7	Power supply for L6 and L7 LDO circuits
M2	VDD_L9_11	Power supply for L9 and L11 LDO circuits
B2	VDD_L10_22	Power supply for L10 and L22 LDO circuits
J2	VDD_L21_23_29	Power supply for L21, L23, and L29 LDO circuits
B5	VDD_L24	Power supply for L24 LDO circuits
B4	VDD_L25	Power supply for L25 LDO circuits
P2	VDD_L26	Power supply for L26 LDO circuits
U5	VDD_L27	Power supply for L27 LDO circuits
R2	VDD_L28	Power supply for L28 LDO circuits
U1	VDD_NCP	Power supply for NCP circuits
A6	VDD_S1	Power supply for S1 buck converter
A12	VDD_S2	Power supply for S2 buck converter
A11	VDD_S3	Power supply for S3 buck converter
V12	VDD_S4	Power supply for S4 buck converter
A15, A16	VDD_S5	Power supply for S5 buck converter
V15, V16	VDD_S6	Power supply for S6 buck converter
V6	VDD_S7	Power supply for S7 buck converter
V11	VDD_S8	Power supply for S8 buck converter

Table 2-11 Pin descriptions – grounds

Pad #	Pad name	Functional description
H9, H10, H11, J8, J9, J10, J11, K8, K9, K10, K11, L9, L10, V1	GND	Ground for all non-specialized circuits.
T17	GND_CHG_DRV	Ground for charger's buck power FET driver.
L11	GND_CHG	Ground for charger buck converter circuits.
R17, R18	GND_CHG_HP	Ground for charger's buck high power circuits.
D15	GND_DRV	Ground for flash drivers and vibration motor driver.
U2	GND_NCP	Ground for NCP circuits.
C2	GND_REF	Ground for bandgap reference circuit.
A8	GND_S1	Ground for S1 buck converter circuits.
A14	GND_S2	Ground for S2 buck converter circuits.
A9	GND_S3	Ground for S3 buck converter circuits.
V14	GND_S4	Ground for S4 buck converter circuits.
B18, C18	GND_S5	Ground for S5 buck converter circuits.
T18, U18	GND_S6	Ground for S6 buck converter circuits.
V8	GND_S7	Ground for S7 buck converter circuits.
V9	GND_S8	Ground for S8 buck converter circuits.
H8	GND_XO	Ground for 19.2 MHz XO circuits.
T1	GND_XOADC	Ground for XO ADC circuits.
L8	GND_XOBUF	Ground for 19.2 MHz XO buffer circuits.

3 Electrical Specifications

3.1 Absolute maximum ratings

Operating the PM8921 device under conditions beyond its absolute maximum ratings (Table 3-1) may damage the device. Absolute maximum ratings are limiting values to be considered individually when all other parameters are within their specified operating ranges. Functional operation and specification compliance under any absolute maximum condition, or after exposure to any of these conditions, is not guaranteed or implied. Exposure may affect device reliability.

Table 3-1 Absolute maximum ratings

Symbol	Parameter	Min	Max	Units
Power supply voltages [1]				
V_{OVP_SNS}	Voltage at the OVP sense pin (OVP_SNS)	-2	+30	V
V_{DCIN}	External charger voltage (DCIN pins)	-2	+12	V
V_{USBIN}	External USB voltage (USB_IN pins)	-2	+30	V
V_{DD}	Handset power supply voltage (VPH_PWR and VDD_XX pins)	-0.5	+6.0	V
V_{BAT_TRAN} (< 10 ms)	Main battery voltage (VBAT pin)	-0.5	+7.0	V
Signal pins [1]				
V_{LED_DRV}	Current driver (LED) output voltage	-0.5	+6.0	V
V_{IN}	Voltage on any non-power supply pin [2]	-0.5	V_{XX} + 0.5	V
ESD protection and thermal conditions – see Section 7.1				

1. Most operational pin voltages are limited by the handset power supply voltage (V_{DD}). Exceptions are listed below:
   - The over-voltage protection sense pin (OVP_SNS) is exposed to the full voltage from the external power supply such as a wall charger, and the DC_IN pins are exposed to USB voltages or voltage-limited wall chargers.
   - The vibration motor driver output (VIB_DRV_N pin) is exposed to V_{DD} plus the diode clamping voltage due to inductive kickback from the motor.
   - The current driver outputs are capable of supporting +5 V operation.
2. V_{XX} is the supply voltage associated with the input or output pin to which the test voltage is applied.

3.2 Recommended operating conditions

Operating conditions include parameters that are under the control of the user: power supply voltage and ambient temperature (Table 3-2). The PM8921 device meets all performance specifications listed in Section 3.3 through Section 3.11 when used within the recommended operating conditions unless otherwise noted in those sections (provided the absolute maximum ratings have never been exceeded).

Table 3-2 Recommended operating conditions

Symbol	Parameter	Min	Typ	Max	Units
Power supply voltages [1]					
V_{OVP}	Voltage at the over-voltage protection pin				
	USB_IN	3.3	–	28	V
	OVP_SNS	3.3	–	28	V
V_{DCIN}	External charger voltage (DCIN pins) [2]	3.3	–	10	V
V_{DD}	Handset power supply voltage (VPH_PWR and VDD_XX pins)	2.5 [3]	3.6	4.5	V
V_{BAT}	Main battery voltage (VBAT pin)	2.5 [3]	3.6	4.5	V
V_{COIN}	Coincell voltage (VCOIN pin)	2	3.0	3.25	V
V_{MSM_IO}	Digital I/O supply voltage	1.75	–	1.85 [4]	V
Signal pins [1]					
V_{LED_DRV}	Current driver (LED) output voltage	0.5	–	+5.0	V
Thermal conditions					
T_C	Operating temperature (case)	-30	+25	+85	°C

1. Most operational pin voltages are limited by the handset power supply voltage (V_{DD}). Exceptions are listed below:
   - The over-voltage protection sense pin (OVP_SNS) is exposed to the full voltage from the external power supply such as a wall charger, and the DC_IN pins are exposed to USB voltages or voltage-limited wall chargers.
   - The vibration motor driver output (VIB_DRV_N pin) is exposed to V_{DD} plus the diode clamping voltage due to inductive kickback from the motor.
   - The current driver outputs are capable of supporting +5 V operation.
2. The stated minimum value defines the threshold for the *charger invalid* interrupt only.
3. Increased maximum to 4.5 V to support “high-voltage” Li batteries. Lower min to 2.5 V to support “low-voltage” Li batteries.
4. Only 1.8 V I/O supported.

3.3 DC power consumption

This section specifies DC power supply currents for the various IC operating modes (Table 3-3). Typical currents are based upon PM8921 IC operation at room temperature (+25°C) using default parameter settings.

Table 3-3 DC power supply currents

Parameter		Comments	Min	Typ	Max	Unit
I_{BAT1}	Supply current, active mode [1]		–	5.3	6.0	mA
I_{BAT2}	Supply current, sleep mode [2] [3]					
	32 kHz XTAL clock		–	160	240	µA
	19.2 MHz XO clock		–	240	360	µA
I_{BAT3}	Supply current, off mode [4]		–	5	18	µA

Table 3-3 DC power supply currents (cont.)

Parameter		Comments	Min	Typ	Max	Unit
I_{COIN}	Coincell supply current [5]					
	Off mode, XTAL on		–	2.5	3	µA
	Off mode, XTAL off [6]		–	2	2.5	µA
	Off mode, RCCA		–	5	8	µA
I_{CHG}	External supply current [7]	Sleep mode	–	13.3	15.0	mA

1. I_{BAT1} is the total supply current from a main battery with the PM8921 IC on, crystal oscillators on, XO_D0 on at 19.2 MHz, driving no load, and these voltage regulators on with no load at the following: VREG_S1 = 1.225 V, VREG_S3 = 1.05 V, VREG_S4 = 1.8 V, VREG_L1 = 1.05 V, VREG_L3 = 3.075 V, VREG_L4 = 1.8 V, VREG_L5 = 2.95 V, VREG_L6 = 2.95 V, VREG_L7 = 2.95 V, VREG_L24 = 1.05 V, VREG_L25 = 1.225 V (bypass mode), and MPP5 = 1.25 V.
2. I_{BAT2} is the total supply current from a main battery with the PM8921 IC on, these voltage regulators on with no load and low-power mode enabled: VREG_S1 = 0.75 V, VREG_S3 = 0.75 V, VREG_S4 = 1.8 V, VREG_L1 = 1.05 V, VREG_L4 = 1.8 V, VREG_L5 = 2.95 V, VREG_L6 = 2.95 V, VREG_L24 = 0.75 V (bypass mode), VREG_L25 = 0.75 V (bypass mode). All other regulators are off, 19.2 MHz crystal oscillator is off, XO buffer off, and all XO_EN signals are low. MBG is in low-power mode.
3. I_{BAT2} is the total supply current from a main battery with the PM8921 IC on, these voltage regulators on with no load and low-power mode enabled: VREG_S1 = 0.75 V, VREG_S3 = 0.75 V, VREG_S4 = 1.8 V, VREG_L1 = 1.05 V, VREG_L4 = 1.8 V, VREG_L5 = 2.95 V, VREG_L6 = 2.95 V, VREG_L24 = 0.75 V (bypass mode), VREG_L25 = 0.75 V (bypass mode). All other regulators are off, 19.2 MHz crystal oscillator is on, XO buffer off, and all XO_EN signals are low. MBG is in low-power mode.
4. I_{BAT3} is the total supply current from a main battery with the PM8921 IC off and the 32 kHz crystal oscillator on. This only applies when the temperature is between -30°C and 60°C.
5. I_{COIN} is the total supply current from a 3.0 V coincell with the PM8921 IC off and the 32 kHz crystal oscillator on. This only applies when the temperature is between -30°C and 60°C.
6. This is the total supply current from a 3.0 V coincell with the PM8921device off, the 32 kHz crystal oscillator off, and RCCAL enabled with nominal settings. This only applies when the temperature is between -30°C and 60°C. This does not include the peak currents when RC Cal is performed and is the average current.
7. I_{CHG} is the total supply current from a charger, with the device configured into the sleep mode as specified in Note 2 above with DC_IN = 7.0 V and VMAXSEL setting = 4.2 V.

3.4 Digital logic characteristics

PM8921 IC digital I/O characteristics such as voltage levels, current levels, and capacitance are specified in Table 3-4.

Table 3-4 Digital I/O characteristics [1]

Parameter		Comments	Min	Max	Unit
V_{IH}	High-level input voltage		$0.65 \cdot V_{IO}$	$V_{IO}+0.3$	V
V_{IL}	Low-level input voltage		-0.3	$0.35 \cdot V_{IO}$	V
V_{SHYS}	Schmitt hysteresis voltage		15	–	mV
I_L	Input leakage current [2]	V_{IO} = max, V_{IN} = 0 V to V_{IO}	-0.20	+0.20	µA
V_{OH}	High-level output voltage	$I_{out} = I_{OH}$	V_{IO}-0.45	V_{IO}	V
V_{OL}	Low-level output voltage	$I_{out} = I_{OL}$	0	0.45	V
I_{OH}	High-level output current [3]	$V_{out} = V_{OH}$	3	–	mA
I_{OL}	Low-level output current [3]	$V_{out} = V_{OL}$	–	-3	mA
I_{OH_XO}	High-level output current [3]	XO digital clock outputs only	6	–	mA
I_{OL_XO}	Low-level output current [3]	XO digital clock outputs only	–	-6	mA
C_{IN}	Input capacitance [4]		–	5	pF

1. V_{IO} is the supply voltage for the MSM/PM IC interface (most PMIC digital I/Os).
2. MPP and GPIO pins comply with the input leakage specification only when configured as a digital input or set to its tri-state mode.
3. Output current specifications apply to all digital outputs unless specified otherwise, and are superseded by specifications for specific pins (such as MPP and GPIO pins).
4. Input capacitance is guaranteed by design but is not 100% tested.

3.5 Input power management

All parameters associated with input power management functions are specified.

3.5.1 Wall charging over-voltage protection

The voltage at OVP_SNS is always monitored. If it is more than about 2 V, the OVP circuits are automatically enabled. Once the circuits are enabled, if OVP_SNS is less than VMAX (7 V nominal), the OVP_CTL output causes the external NMOS switch to close, thereby connecting the external supply voltage to the DC_IN node. If the voltage exceeds VMAX, the OVP_CTL output is immediately driven low to open the NMOS switch and protect the DCIN node.

3.5.2 External supply detection

The PMIC continually monitors the external supply voltage (at DCIN) and the handset supply voltage (V_{DD} at VPH_PWR). Internal detector circuits measure these voltages to recognize when supplies are connected or removed, and verify they are within their valid ranges when connected.

Hysteresis prevents undesired switching near the thresholds, and status is reported to the on-chip state-machine and to the MSM or QSC devices via interrupts.

Circuits detect when the external supply is removed by monitoring the voltage across the internal pass transistor. The detection circuitry is triggered when the DC_IN voltage drops to about 100 mV higher than V_{DD}. As this differential voltage (DC_IN - V_{DD}) drops below 100 mV, the detection circuitry cuts the bias to the pass transistor so that the removal can be detected. Without this circuit, when the external supply is suddenly disconnected the pass transistor can operate in its reverse mode and keep sufficient voltage on DC_IN so that the phone will not realize that the external supply has been disconnected.

Performance specifications for the supply detection functions are presented in Table 3-5.

Table 3-5 Supply detection performance specifications

Symbol	Parameter	Condition	Min	Typ	Max	Unit	Notes
Recommended Input range for the SMBC assuming a 4.2 V battery							
V_{USBIN}	USB input voltage		4.35	–	6.5	V	1
V_{OVP_SNS}	OVP input voltage		4.5	–	9.5	V	1
Undervoltage detection							
	Coarse detect threshold	USBIN and OVP_SNS, rising	1.4	1.7	2.0	V	
$V_{THR\_UVD\_R}$	UVD threshold	USBIN and OVP_SNS, rising	4.15	4.25	4.35	V	2
$V_{THR\_UVD\_F}$	UVD threshold	USBIN and OVP_SNS, falling	3.75	3.85	3.95	V	3
V_{HYST_UVD}	UVD threshold hysteresis	USBIN and OVP_SNS	350	400	450	mV	
$T_{DB\_UVD\_R}$	UVD debounce	USBIN and OVP_SNS, rising	–	40	–	ms	
$T_{DB\_UVD\_F}$	UVD debounce	USBIN and OVP_SNS, falling	–	1	3	µs	
Overvoltage protection							
V_{OVP}	Overvoltage tolerance		30	–	–	V	
$V_{THR\_OVP\_USBIN}$	USBIN OVP threshold programmable settings	USBIN, rising	5.5	6.5	7.0	V	4
$V_{THR\_OVP\_DCIN}$	OVP_SNS threshold programmable settings	OVP_SNS, rising	8.5	9.5	10.0	V	4
	OVP threshold accuracy	USBIN and OVP_SNS	-2		+2	%	5
V_{HYST_OVP}	OVP threshold hysteresis	USBIN and OVP_SNS, falling	150	200	250	mV	
$T_{DB\_OVP\_F}$	OVP debounce	USBIN and OVP_SNS, rising	–	0.4	1	µs	
$T_{DB\_OVP\_R}$	OVP debounce	USBIN and OVP_SNS, falling	–	40	–	ms	
	OVP FET turn-off time		–	1	3	µs	
	USBIN OVP FET Rds(on)	USBIN = 5.0 V	–	150	250	mΩ	6
	OVP_SNS FET V_{GS} ($V_{OVP\_CNTRL} – V_{CHG}$)	External OVP FET turned on	–	5	6	V	
Negative voltage protection							
	Negative voltage tolerance	USBIN and OVP_SNS	–	–	-0.3	V	

Notes:
1. These are recommended operating ranges. The acceptable operating ranges are defined by the corresponding UVD and OVP thresholds.
2. To meet the 4.4 V minimum VBUS voltage from an unloaded bus-powered hub as specified in the USB 2.0 specification.
3. To meet the 4.1 V minimum VBUS undershoot as specified in the USB BC 1.1 specification.
4. In 0.5 V steps.
5. After PMIC poweron.
6. Including package resistance.

3.5.3 SMBC

The PM8921 device uses a new SMBC architecture. Table 3-6 provides the detailed specifications for the SMBC.

Table 3-6 SMBC specifications

Parameter	Condition	Min	Typ	Max	Units
Battery/VDD voltage programmable range [1]		3.4	–	4.5	V
Battery/VDD voltage accuracy	Including line and load regulation	-30	–	30	mV
Battery charge current programmable range [2]		325	–	2025	A
Battery charge current accuracy		-5	–	+5	%
Input voltage limit programmable range [3]		4.3	–	6.5	V
Input voltage limit accuracy		-2	–	2	%
USBIN input current limit [4]	100 mA setting	86	90	95	mA
	500 mA setting	448	471	495	mA
	1.1 A setting	0.991	1.043	1.095	A
	1.5 A setting	1.353	1.424	1.495	A
Rated output (VDD) current	Continuous	–	2.1	–	A
Switching frequency [5]		1.6	–	3.2	MHz
Efficiency 1 [6]	I_{BAT} = 750 A V_{BAT} = 3.7 V USB_IN = 5.0 V or DCIN_SNS = 6.0 V	–	90	–	%
Efficiency 2 [7]	I_{BAT} = 100 mA or 1.5 A V_{BAT} = 3.7 V USB_IN = 5.0 V or DCIN_SNS = 6.0 V	–	85	–	%

1. 20 mA steps, 3.6 V default
2. 50 mA steps, 325 mV default
3. 100 mV steps, 4.3 V default
4. 100 mA default; available settings are 100 mA, 500 mA, 700 mA, 850 mA, 900 mA, 1100 mA, 1300 mA, and 1500 mA
5. 3.2 MHz default
6. FSW = 1.6 MHz; inductor DCR = 100 mΩ
7. FSW = 1.6 MHz; inductor DCR = 100 mΩ

3.5.3.1 Main battery charging

The PM8921 IC conducts battery charging with less software interaction than previous generation designs. This is made possible by the IC's state-machine.

The charging algorithm uses as many as four charging techniques: trickle, constant current, constant voltage, and pulsed. Battery voltage, external supply voltage, and total detected current conditions are available to the on-chip state-machine. (The same measurements are also available to the MSM or QSC device via the analog multiplexer). This allows the state-machine to monitor charging parameters, make decisions, and control the charging process. The end of each stage is detected by the state-machine, and the next stage is executed automatically and autonomously (without software intervention). The state-machine signals the end-of-charge to the MSM or QSC device via an interrupt.

The first step in the automated charging process determines if trickle charging is needed. Charging of a *severely* depleted battery must begin with trickle charging to limit the current, avoid pulling V_{DD} down, and protect the battery from more charging current than it can handle. Once a minimum battery voltage is established using trickle charging, constant-current charging is enabled to charge the battery quickly – this mode is sometimes called fast charging. Once the battery approaches its target voltage, the charge is completed using either constant voltage or pulse charging.

PMIC performance specifications for each of these charging techniques are given in the following subsections.

3.5.3.1.1 Trickle charging

The trickle charger is an on-chip programmable current source that supplies current from V_{DD} to the VBAT pin; pertinent performance specifications are given in Table 3-7.

Table 3-7 Trickle charging performance specifications

Parameter	Condition	Min	Typ	Max	Units
Trickle charge current programmable range [1]		50	–	200	mA
Trickle charge current accuracy		±10% of setting ±5 mA			
Trickle voltage threshold programmable range [2]		2.05	–	2.8	V
Trickle voltage threshold accuracy		-50	–	+50	mV
V_{weak} System weak threshold programmable range (100 mV steps, 3.2 V default)	V_{bat} falling	2.1	3.2	3.6	V
System weak threshold accuracy		-50	–	+50	mV
Voltage hysteresis		15	20	25	mV
Debounce		–	1	–	s

1. 10 mA steps, 50 mA default
2. 50 mV steps, 2.8 mV default

3.5.3.1.2 ATC indication

During ATC, the 5 mA nominal ATC_LED current sink turns on and off at a 0.5 Hz rate. An LED can be connected to the ATC_LED pin, as shown in Figure 3-1.

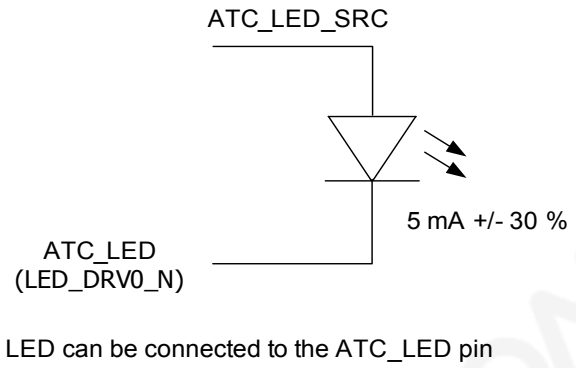


Figure 3-1 LED connected to the ATC_LED pin

The anode can be switched to VPH_PWR, an external boosted 5 V supply, or an internally generated voltage of approximately 5 V that is regulated down from DC_IN. The internal supply will be used during ATC. The ATC_LED_sink pin can also be turned on explicitly by direct SBI transactions or by using the light pulse generator module.

See the ATC LED indicator (Section 3.8) and its supply in General housekeeping (Section 3.7).

3.5.3.1.3 Constant current charging

Constant current charging uses closed-loop control of the pass transistor to regulate the total current (handset electronics plus charging current) to match the programmed value (IMAXSEL). The PMIC parameters associated with constant current charging are specified in the following subsections:

- External supply voltages Section 3.5.2
- Battery voltage detector Section 3.5.4.8

Charging current is a function of the external supply voltage (such as DC_IN) for a fixed battery voltage (VBAT). The charging current will be reduced significantly if DC_IN is not sufficiently larger than VBAT. An example curve showing the charging current versus DC_IN is shown with VBAT fixed at 4.1 V.

Charging current is also a function of the battery voltage for a fixed external supply voltage. Charging current drops off quickly as V_{BAT} approaches DC_IN. An example curve showing the charging current versus V_{BAT} is shown with DC_IN fixed at 5 V.

Additional performance specifications for constant current charging are not required.

3.5.3.1.4 Constant voltage charging

Once constant current charging of a lithium-ion battery is completed, the charging continues using either constant voltage or pulsed techniques. Specifications pertaining to constant voltage charging are addressed in this subsection; pulse charging is covered in Section 3.5.4.

PMIC support of constant voltage charging is very similar to its constant current mode: the battery MOSFET is closed and the pass transistor is closed-loop controlled. But in this case, the closed-loop control regulates the voltage at VBAT to match the programmed value VMAXSEL. This ensures the most accurate final battery voltage – lithium-ion battery manufacturers recommend a voltage accuracy of 1% or better at the end of charge.

The PM8921 IC parameters associated with constant voltage charging are specified in the following subsections:

- External supply voltages Section 3.5.2
- Battery voltage detector Section 3.5.4.8

Additional performance specifications are not required.

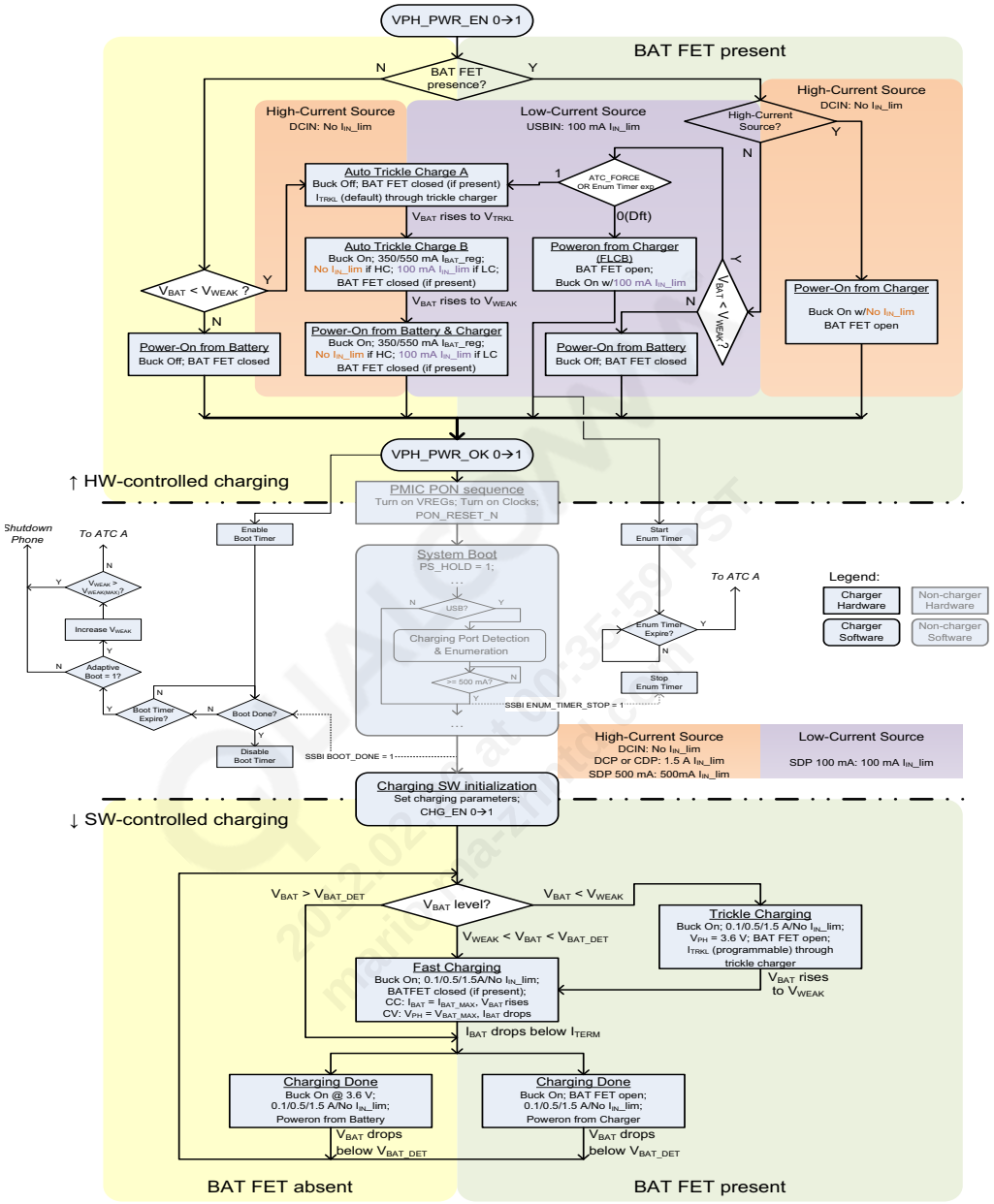


Figure 3-2 Charging flow diagram

Table 3-8 SMBC exception handling

Exception event	Description	Condition	Battery charging	VPH_PWR source	Buck	Trickle charger	BAT FET (if present)	T_{TRKL} and T_{CHG}	T_{CHG_WD}	Note
No exception	Everything OK, actively charging		Run	Chg	B or T		(On/closed)	Run	Run	Baseline
Charging complete		BATFET absent	Stop	Batt	Off	Off	–	Stop	Stop	
		BATFET present	Stop	Chg	On	Off	Off/open	Stop	Stop	
Adapter interface										
Charger not OK	No valid charging source. Both USBIN and DCIN are gone, over-voltage, or under-voltage.		Stop	Batt	Off	Off	(On/closed)	Stop	Stop	
USB suspended	USB port is suspended by the host, and no more than 2.5 mA can be drawn (from SSBI).		Stop	Batt	Off	Off	(On/closed)	Stop	Stop	
Battery interface										
Battery gone	The battery presence detection circuit indicates that the battery is missing.	BATFET absent	Stop	Chg	On	Off	–	rest	Stop	
		BATFET present	Stop	Chg	On	Off	Off/open	rest	Stop	
Battery temp not OK	The battery temperature monitoring circuit indicates that the battery is hot or cold.	BATFET absent	Stop	Batt	Off	Off	–	Stop	Run	1
		BATFET present	Stop	Chg	On	Off	Off/open	Stop	Run	1
		In HW-Ctrl ATC	Stop	N/A	Off	Off	(On/closed)	Run	Stop	4

Table 3-8 SMBC exception handling (cont.)

Exception event	Description	Condition	Battery charging	VPH_PWR source	Buck	Trickle charger	BAT FET (if present)	T_{TRKL} and T_{CHG}	T_{CHG_WD}	Note
Switch-mode charging control										
Charger temp too high	The SMBC buck or trickle charger temp exceeds the limit.	In HW-Ctrl ATC	Stop	None	Off	Off	(On/closed)	Run	Stop	4
		In SW-Ctrl trickle chg	Stop	Chg	On	Off	(Off/open)	Stop	Run	1
		In SW-Ctrl fast chg	Stop	Bat	Off	Off	(On/closed)	Stop	Run	1
Charging disabled	SW disables charger via SSBI.	BATFET absent	Stop	Batt	Off	Off	–	Stop & rest	Stop	
		BATFET present	Stop	Chg	Off	Off	Off/open	Stop & rest	Stop	
Charging paused	SW pauses battery charging via SSBI.	BATFET absent	Stop	Batt	Off	Off	–	Stop	Run	
		BATFET present	Stop	Chg	On	Off	Off/open	Stop	Run	
T_{TRKL} expire	Trickle charging timer expires.	BATFET absent	Stop	Batt	Off		–	Stop	Stop	2
		BATFET present	Stop	Chg	On		Off/open	Stop	Stop	2
T_{CHG} expire	Maximum charging timer expires.	BATFET absent	Stop	Batt	Off		–	Stop	Stop	2
		BATFET present	Stop	Chg	On		Off/open	Stop	Stop	2

Table 3-8 SMBC exception handling (cont.)

Exception event	Description	Condition	Battery charging	VPH_PWR source	Buck	Trickle charger	BAT FET (if present)	T_{TRKL} and T_{CHG}	T_{CHG_WD}	Note
T_{CHG_WD} expire	Charging SW not responding causing charger WD timer expires.	BATFET absent	Stop	Batt	Off		–	Stop	Stop	2
		BATFET present	Stop	Chg	On		Off/open	Stop	Stop	
VTRKL_FAULT	VBAT rises above V_{TRKL_FAULT} during trickle charging.		Stop	Chg	On		Off/open	Stop	Stop	
PMIC infrastructure									Stop	
VPH_PWR_EN: 1 --> 0	PON module requests the charger **not** to bring up VDD.		Stop	Off	Off		Off/open	Stop & rest	Stop	3
PON not OK	PON module gets stuck in the powerup sequence, or the MSM device fails to raise PS_HOLD.		Stop	Chg	On		Off/open	Stop	Stop	
CRIT_SHTDWN	MBG not OK, or PMIC over-temperature stage 2 occurred.	In HW-Ctrl ATC	Stop	OFF			Off/open	Stop & rest	Stop	
		Not in ATC	Stop						Stop	

3.5.3.2 Battery temperature monitoring specifications

If the system does not use a BAT_ID pin, then the unused BAT_ID pin can be grounded.

Starting with ES2 and CS, if BATT_THERM is not needed, Qualcomm recommends grounding the BATT_THERM pin, and it is necessary to disable the feature in the software.

Table 3-9 lists battery interface specifications.

Table 3-9 Battery interface specifications

Parameter	Condition	Min	Typ	Max	Unit	Notes
Battery-temperature monitoring						
Cold-comparator threshold programmable settings	Fraction of $V_{REF\_BAT\_THM}$	70	–	80	%	Selectable as 70% or 80%
Cold-comparator offset		-10	–	10	mV	
Cold-comparator voltage hysteresis, for 70% setting	$V_{REF\_BAT\_THM}$ failing (battery warming)	-80	–	-40	mV	
Cold-comparator voltage hysteresis, for 80% setting	$V_{REF\_BAT\_THM}$ falling (battery warming)	-70	–	-35	mV	
Cold-comparator debounce	$V_{REF\_BAT\_THM}$ rising or falling	1	–	2	s	
Hot-comparator threshold programmable settings	Fraction of $V_{REF\_BAT\_THM}$	25	–	35	%	Selectable as 25% or 35%
Hot-comparator offset		-10	–	10	mV	
Hot-comparator voltage hysteresis, for 35% setting	$V_{REF\_BAT\_THM}$ failing (battery cooling)	25	–	50	mV	
Hot-comparator voltage hysteresis, for 25% setting	$V_{REF\_BAT\_THM}$ falling (battery cooling)	15	–	30	mV	
Hot-comparator debounce	$V_{REF\_BAT\_THM}$ rising or falling	1	–	2	s	
Battery presence detection (BPD)						
BPD-comparator threshold	Fraction of $V_{REF\_BAT\_THM}$	–	95	–	%	
BPD-comparator offset		-50	–	50	mV	
BPD-comparator debounce	$V_{REF\_BAT\_THM}$ rising (battery removal) $V_{REF\_BAT\_THM}$ falling (battery insertion)	1 –	– 1	3 –	µs s	

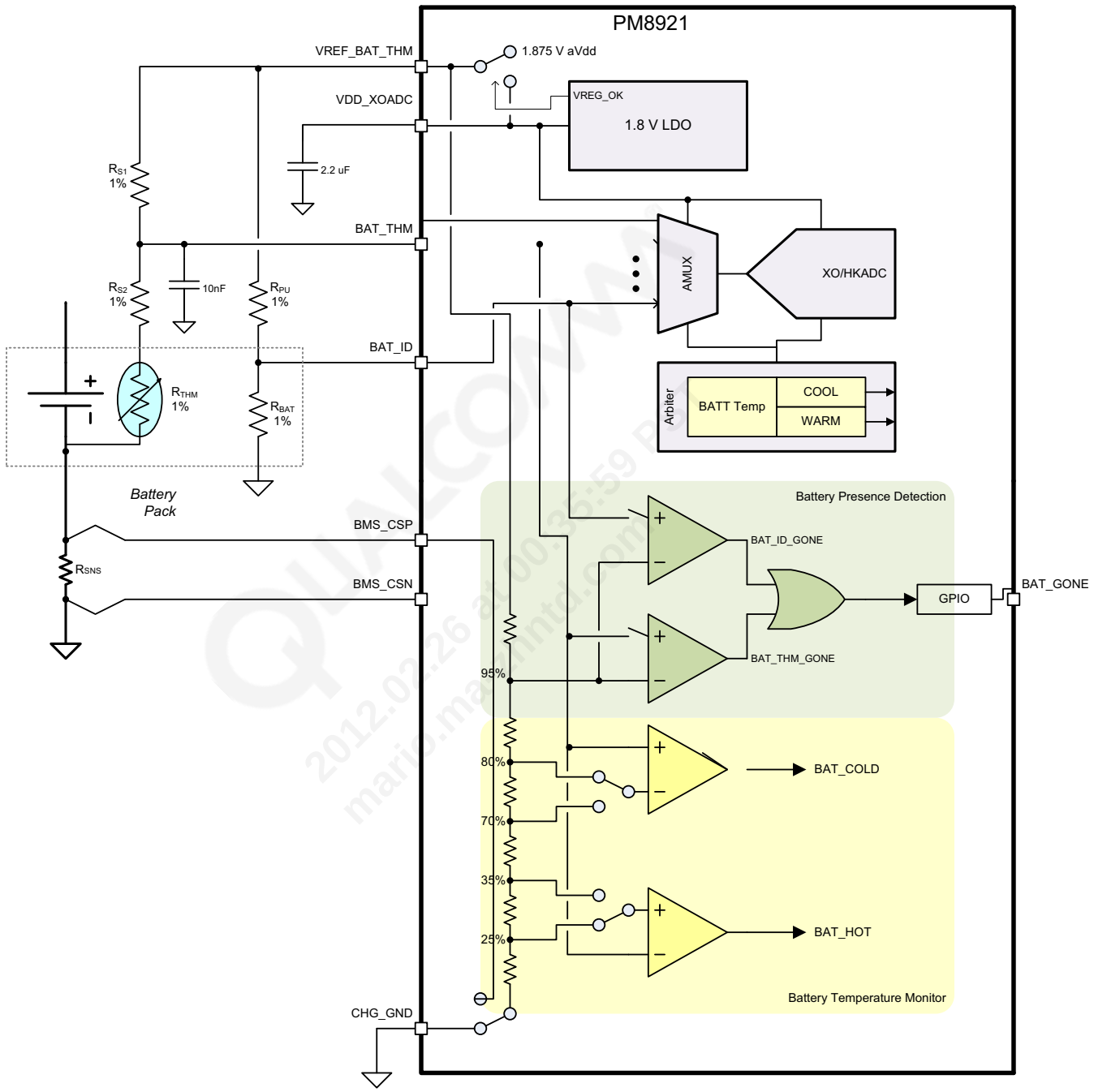


Figure 3-3 BTM diagram

Table 3-10 BTM calculations

Batter charging temperature window	BTM comp. thresholds	R_{s1} and R_{s2} calculation
0°C–40/45°C	70%/35%	$R_{S1} = \frac{39 \cdot (R_{COLD} - R_{HOT})}{70}$ $R_{S2} = \frac{3\,R_{COLD} - 13\,R_{HOT}}{10}$
-10°C–60°C	80%/20%	$R_{S1} = \frac{4 \cdot (R_{COLD} - R_{HOT})}{15}$ $R_{S2} = \frac{R_{COLD} - 16\,R_{HOT}}{15}$

3.5.4 BMS

The module provides function to monitor the battery capacity in conjunction with XOADC, which provides battery voltage information when needed.

3.5.4.1 Battery voltage alarm

A programmable window detector continuously monitors the battery voltage at VBAT. Both thresholds, upper and lower, are programmable and include voltage hysteresis to ensure stability. To prevent brief voltage transients from generating interrupts unnecessarily, the out-of-range condition must stay triggered for a certain amount of time before an interrupt is generated. This delay, referred to as time hysteresis, is also programmable. If the battery voltage returns in-range before the programmed delay, the delay timer is reset and no interrupt is generated.

Performance specifications for the battery voltage alarm circuits are given in Table 3-11.

Table 3-11 Battery voltage alarm performance specifications

Parameter	Min	Max	Comments/conditions
Battery alarm accuracy	-50 mV	+50 mV	Assuming 0.5% accuracy for the 1.25 V release
Battery threshold hysteresis (V_{BATT} < 4.5 V)	20 mV	30 mV	Explicit hysteresis is 1% of V_{BATT} (see Figure 3-4)
Time hysteresis (4.5 V < V_{BATT} < 5.5 V)	60 mV	80 mV	Explicit hysteresis is 1% of V_{BATT} (see Figure 3-4)

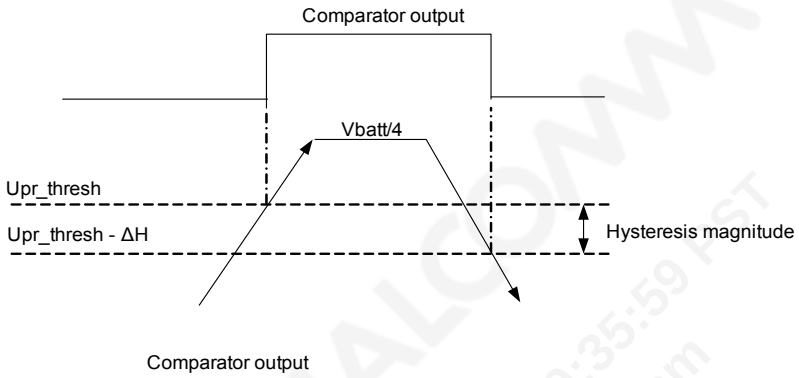


Figure 3-4 Hysteresis

3.5.4.2 UVLO

The handset supply voltage (V_{DD}) is monitored continuously by a UVLO circuit that automatically turns off the device at severely low V_{DD} conditions. However, the programmable UVLO threshold is lower than the low battery threshold, described in Section 3.5.4.8.

Other than the programmable threshold, software is not involved in UVLO detection. Hysteresis and time delays are not programmable, and UVLO events do not generate interrupts. They are reported to the MSM or QSC devices via the PON_RESET_N signal. UVLO-related voltage and timing specifications are listed in Table 3-12.

Table 3-12 UVLO performance specifications

Parameter	Comments	Min	Typ	Max	Units
Threshold voltage, falling	Programmable value	1.500	2.700	3.050	V
Threshold voltage accuracy		-5	–	+5	%
Hysteresis		100	175	250	mV
UVLO detection interval		–	1.0	–	µs

3.5.4.3 SMPL

The PMIC SMPL feature initiates a poweron sequence if the monitored phone voltage (V_{DD}) drops out of range and then returns in-range within a programmable interval. When enabled by software, SMPL achieves immediate and automatic recovery from momentary power loss (such as a brief battery disconnect when the phone is jarred).

If only SMPL support is desired, the 19.2 MHz XO circuits can be disabled – the SMPL function can be clocked by either the 32 kHz crystal or the internal RC oscillator.

SMPL performance specifications are given in Table 3-13.

Table 3-13 SMPL performance specifications

Parameter	Comments	Min	Typ	Max	Units
Minimum SMPL interval [1]	Programmable range	0.1	–	2.0	s

1. The timing accuracy of the SMPL interval is set entirely by the oscillator clocking the counters. Valid settings are: 0.5, 1.0, 1.5, and 2.0 seconds. These settings correspond to the external keep-alive capacitor value used at VCOIN: 1.5, 3.3, 4.7, and 6.8 µF, respectively.

3.5.4.4 Battery MOSFET requirements

Battery transistor (Table 3-14) – this external P-channel MOSFET is required. Without it, depleted batteries could dangerously overheat when charging.

The specifications for the external battery MOSFET are intended for example purposes only; handset designers are encouraged to use their own choices while understanding that overall performance might be affected by an inappropriate choice.

Table 3-14 External battery P-channel MOSFET specifications

Parameter	Comments	Min	Typ	Max	Units
Example specifications based upon International Rectifier model IRF7324					
Drain-source voltage		–	–	-20	V
Continuous drain current	V_{GS} = -4.5 V, T_A = +70°C	–	–	-5.4	A
Pulsed drain current		–	–	-40	A
Power dissipation	T_A = +70°C	–	–	1.3	W
Gate-to-source voltage		-12	–	+12	V
Junction temperature		-55	–	+150	°C
Thermal resistance	Junction-to-ambient	–	–	62.5	°C/W
D-S on resistance	Static, V_{GS} = -2.5 V, I_D = -6.0 A	–	–	0.026	Ω
Gate threshold voltage	V_{DS} = V_{GS}, I_D = -6.0 A	-0.45	–	-1.00	V

3.5.4.5 Battery MOSFET driver

A control driver for the battery MOSFET is included within the PMIC; its drive signal is applied to the external transistor via the BAT_FET_N pin. Specifications for the battery MOSFET driver are listed in Table 3-15. Some specifications depend on suitable external components, as identified in Table 3-14, or they depend on the control mode, as identified in Table 3-15.

Table 3-15 External MOSFET driver specifications

Parameter	Comments	Min	Typ	Max	Units
Battery FET control [1]					
Charge removal to battery switchover time [2]	10% to 90%, 2 nF load, on BAT_FET_N	–	–	5	µs
BAT_FET_N V_{OH}	Source 100 µA to BAT_FET_N	Vddx - 0.1	–	–	V
BAT_FET_N V_{OL}	$I_{BAT\_FET\_DET}$ = 100 µA	–	–	0.25	V
Battery FET detection					
Battery FET detection current		–	100	–	µA
Battery FET detection duration		–	1	–	ms

1. The switchover between charger and battery operational modes must be fast enough to avoid phone shutdown. (Section 3.5.4.8 describes the VDD collapse protection circuit). This switchover time is measured from the time DC_IN drops below VDD to when the BAT_FET_N control signal drops to its 10% level (battery FET nearly full-on)
2. VXX is the higher of either V_{BAT} or V_{DD}.

3.5.4.6 Battery fuel gauge

Table 3-16 Battery fuel gauge specifications

Parameter	Condition	LLimit	ULimit	Units
Resolution on battery current measurement	Battery current peak at 2 A Current sense resistance at 25 mΩ	9	–	bit
Resolution on battery voltage measurement		13	–	bit
Battery current range		-4	4	A
Input referred offset		–	50 µV	–

See Section 3.7 for VREF source and ADC circuit details.

3.5.4.7 Sense resistor requirements

Table 3-17 Sense resistor requirements and insense accuracy

R_{SENSE} (mΩ)	BMS SOC accuracy	BMS $I_{SENSEaccuracy\ (mA)}$		
		Condition	Error (linear)	Error (RMS)
25	+2.3%	10 mA	3.3	2.2
		1 A	23.4	14.4
20	+3.0%	10 mA	4.1	2.8
		1 A	24.3	14.5
15	+3.4%	10 mA	5.3	3.7
		1 A	25.7	14.7

Table 3-17 Sense resistor requirements and insense accuracy (cont.)

R_{SENSE} (mΩ)	BMS SOC accuracy	BMS $I_{SENSEaccuracy}$ (mA)		
		Condition	Error (linear)	Error (RMS)
10	+4.3%	10 mA [1]	7.8	5.6
		1 A	28.5	15.4

1. Qualcomm recommends the use of a 10 mΩ sense resistor with the PM8921 device for BMS applications.

3.5.4.8 V_{DD} collapse protection

Some handset manufacturers may specify a low-current charger that cannot handle the peak phone plus charging current. To prevent a sudden load from inadvertently collapsing the V_{DD} voltage when a low-current charger is used, the PMIC monitors the voltage across the battery MOSFET (through the VPH_PWR and VBAT pins) and automatically turns it on if V_{DD} drops about 40 mV below VBAT.

Performance specifications related to V_{DD} collapse protection are given in Table 3-18.

Table 3-18 VDD collapse protection performance specifications

Parameter	Comments	Min	Typ	Max	Units
BAT_FET_N output, 0 V differential	V_{BAT} - V_{PH_PWR} = 0 V	V_{DD} - 0.1	–	V_{DD}	V
V_{BAT} - V_{PH_PWR}	VCP interrupt triggers	20	60	100	mV
Activation time		–	–	5	µs

3.5.5 Coincell charging

Coincell charging is enabled through software control and powered from VBAT. The on-chip charger is implemented using a programmable voltage source and a programmable series resistor. The MSM or QSC device reads the coincell voltage through the PMIC's analog multiplexer to monitor charging. coincell charging performance is specified in Table 3-19.

Table 3-19 Coincell charging performance specifications

Parameter	Comments	Min	Typ	Max	Units
Target regulator voltage [1]	V_{IN} > 3.3 V, I_{CHG} = 100 µA	2.50	3.10	3.20	V
Target series resistance [2]		800	–	2100	Ω
Coincell charger voltage error	I_{CHG} = 0 µA	-5	–	+5	%
Coincell charger resistor error		-20	–	+20	%
Dropout voltage [3]	I_{CHG} = 2 mA	–	–	200	mV
Ground current, charger enabled VBAT = 3.6 V, T = 27ºC VBAT = 2.5 to 5.5 V	IC = off; VCOIN = open	 – –	 4.5 –	 – 8	 µA µA

1. Valid regulator voltage settings are 2.5, 3.0, 3.1, and 3.2 V.
2. Valid series resistor settings are 800, 1200, 1700, and 2100 Ω.

3. Set the input voltage (V_{BAT}) to 3.5 V. Note the charger output voltage; call this value V_0. Decrease the input voltage until the regulated output voltage drops 100 mV (until DC_IN = V_0 - 0.1 V). The voltage drop across the regulator under this condition is the dropout voltage ($V_{dropout}$ = V_{BAT} - DC_IN).

3.6 Output power management

The PMIC includes all the regulated voltages needed for most wireless handset applications. Independent regulated power sources are required for various electronic functions to avoid signal corruption between diverse circuits, support power management sequencing, and to meet different voltage level requirements. Thirty-two programmable voltage regulators are provided, and all are derived from a common bandgap reference circuit. A high-level summary of all regulators and their intended uses is presented in Table 3-20.

Table 3-20 Output power management summary

Regulator	Type	Default voltage (V) [1]	Specified range (V)	Programmable range	I_{rated} (mA)	Default on	Notes/use on MSM8960 chipset
S1	Buck SMPS	1.225	0.750–1.400	0.375 – 3.050	1500 [2]	Y	Sub-regulation purposes
S2	Buck SMPS	1.300	1.000 –1.400	0.375 – 3.050	1500 [2]	–	MSM device digital core, RF power supply
S3	Buck SMPS	1.050	0.500 –1.400	0.375 – 3.050	2000 [2]	Y	MSM device VDD_CORE, USB
S4	Buck SMPS	1.800	1.700 –1.900	0.375 – 3.050	1500 [2]	Y	MSM device GP, off-chip memory, WCN3660 IC. Do not change from default.
S5	Buck SMPS	1.050	0.500 –1.350	0.350 – 3.300	2000	–	MSM device apps processor #1
S6	Buck SMPS	1.050	0.500 –1.350	0.350 – 3.300	2000	–	MSM device apps processor #2
S7	Buck SMPS	1.150	0.750 –1.350	0.375 – 3.050	1500	–	Sub-regulation purposes
S8	Buck SMPS	2.200	1.500 –2.350	0.375 – 3.050	1500	–	Codec and RF supplies
L1	NMOS LDO	1.050	1.000 –1.450	0.750 – 1.525	150	Y	MSM and multimedia XO
L2	NMOS LDO	1.200	1.100 –1.450	0.750 – 1.525	150	–	MSM device MIPI; MSM temp; audio core
L3	PMOS LDO	3.075	3.000 –3.300	0.750 – 4.900	150 [3]	Y	USB power
L4	PMOS LDO	1.800	1.700 –1.900	0.750 – 4.900	50	Y	MSM device USB analog, PMIC clock driver. Do not change from default.
L5	PMOS LDO	2.950	2.750 –3.000	0.750 – 4.900	300	Y	eMCC
L6	PMOS LDO	2.950	2.750 –3.000	0.750 – 4.900	600 [4]	Y	SD/MCC
L7	PMOS LDO	2.950	2.750 –3.000	0.750 – 4.900	150	Y	VDD_P2
L8	PMOS LDO	2.800	2.600 –3.000	0.750 – 4.900	300	–	LCD1 MIPI
L9	PMOS LDO	2.850	2.600 –3.000	0.750 – 4.900	300	–	Sensors
L10	PMOS LDO	2.900	2.600 –3.300	0.750 – 4.900	600	–	VDD_2P9V
L11	PMOS LDO	2.850	2.600 –3.300	0.750 – 4.900	150	–	MIPI
L12	NMOS LDO	1.200	1.100 –1.500	0.750 – 1.525	150	–	Camera MIPI
L14	PMOS LDO	1.800	1.700 –1.900	0.750 – 4.900	50	–	–
L15	PMOS LDO	3.000	1.700 –3.300	0.750 – 4.900	150	–	UIM
L16	PMOS LDO	2.800	2.600 –3.300	0.750 – 4.900	300	–	LCD2 MIPI
L17	PMOS LDO	3.000	1.700 –3.000	0.750 – 4.900	150	–	UIM

Table 3-20 Output power management summary (cont.)

Regulator	Type	Default voltage (V) [1]	Specified range (V)	Programmable range	I_{rated} (mA)	Default on	Notes/use on MSM8960 chipset
L18	NMOS LDO	1.300	1.000 –1.500	0.750 – 1.525	150	–	–
L19	–	–	–	–	–	–	–
L20	–	–	–	–	–	–	–
L21	PMOS LDO	1.900	1.700–2.100	0.750–4.900	150	–	VIDEO, VDD_A2, BBRX
L22	PMOS LDO	2.600	1.700 –2.850	0.750–4.900	150	–	RF switches
L23	PMOS LDO	1.800	1.700 –1.900	0.750–4.900	150	–	PLL, HDMI, MIPI
L24	NMOS LDO	1.050	0.750 –1.250	0.750–1.525	1200	Y	MEM, PLL
L25	NMOS LDO	1.225	0.750 –1.250	0.750–1.525	1200	Y	DDR, TXADC
L26	NMOS LDO	1.050	0.750 –1.250	0.750–1.525	1200	–	QDSP processor
L27	NMOS LDO	1.050	0.750 –1.250	0.750–1.525	1200	–	QDSP processor
L28	NMOS LDO	1.050	0.750 –1.500	0.750–1.525	1200	–	QDSP processor
L29	PMOS LDO	2.050	1.700 –2.200	0.750–4.900	150	–	–
LVS1	Low V switch	1.800	–	–	100	–	VDD_1P8V
LVS2	Low V switch	1.200	–	–	300	–	VDD_MODEM
LVS3	Low V switch	1.800	–	–	100	–	MSM device Qfuse
LVS4	Low V switch	1.800	–	–	100	–	Sensors
LVS5	Low V switch	1.800	–	–	100	–	MIPI
LVS6	Low V switch	1.800	–	–	100	–	–
LVS7	Low V switch	1.800	–	–	100	–	Digital MIC, RFIC GPS & I/O; MSM I/O
MVS1	Medium V switch	5.000	–	–	500	–	OTG
MVS2	Medium V switch	5.000	–	–	62	–	HDMI
NCP	Charge pump	-1.800	-1.700 to -1.900	-1.800– -3.050	200	–	Headphone
XO	Clock LDO	1.800	–	–	–	Y	Internal use only; XO circuits
RF_CLK	Clock LDO	1.300	–	–	–	–	Internal use only; RF clock circuits

1. The default voltage and power-on state may depend on option pin settings.

2. The HF buck SMPS 1.5 A rating assumes a V_{out} less than or equal to 1.8 V. For V_{out} above 1.8 V, the rating is reduced due to duty-cycle limitations. For 1.8 V < V_{out} < 2.4 V, the rating is reduced to 800 mA.
3. The VREG_L3 used as the USB_LDO is a conventional PMOD LDO (150 mA). The VIN of this LDO is tied to VPH_PWR. The effective rated current is reduced to 50 mA to lower dropout voltage by a factor of 3.
4. L6 has been characterized for 800 mA peak current capability to support micro-SD v 3.0. The regulator meets all the specifications at 800 mA except for overshoot response (measures 3.8%).

Output power management circuits include:

- Bandgap voltage reference circuit
- Buck SMPS circuits
- LDO linear regulators
- NCP
- Voltage switches

All regulators can be set to a low-power mode, except VREG_NCP; the NCP output provides a negative voltage for headphone circuits. Details are provided in the following subsections.

3.6.1 Reference circuit

All PMIC regulator circuits and other internal circuits are driven by a common, on-chip voltage reference circuit. An on-chip series resistor supplements an off-chip 0.1 µF bypass capacitor at the REF_BYP pin to create a lowpass function that filters the reference voltage distributed throughout the device.

NOTE Do not load the REF_BYP pin. Use an MPP configured as an analog output if the reference voltage is needed off-chip.

Applicable voltage reference performance specifications are given in Table 3-21.

Table 3-21 Voltage reference performance specifications

Parameter	Comments	Min	Typ	Max	Units
Nominal internal VREF	At REF_BYP pin	–	1.250	–	V
Output voltage deviations					
Normal operation	Over temperature only, -20 to +120ºC	-0.32	–	+0.32	%
Normal operation	All operating conditions	-0.50	–	+0.50	%
Sleep mode	All operating conditions	-1.00	–	+1.00	%

3.6.2 Buck SMPS

The buck converter is a switched-mode power supply that provides an output voltage lower than its input voltage, and is therefore also known as a step-down converter. The PM8921 IC includes six high frequency SMPS and two fast transient SMPS.The HF bucks support PWM and PFM modes and also support the automatic transition between PWM and PFM modes depending on the load current.

Table 3-22 and Table 3-23 provide details of the HF-SMPS and the FT-SMPS.

Table 3-22 HF-SMPS performance specifications[1]

Parameter	Test condition	LLimit	Typical	ULimit	Units
Rated load current Normal mode (PWM/hysteretic) [2]	PWM mode; UL is specified minimum current for continuous delivery	1.5	–	–	A
Rated load current (PFM) [3]	PFM mode; UL is specified minimum current for continuous delivery	100	–	–	mA
DC error (DC output voltage) Normal mode (PWM/hysteretic) [4]	Vout > 1.0 V, Irated/2 Vout < 1.0 V, Irated/2	-1 -10	0 0	1 10	% mV
DC error (DC output voltage) (PFM) [3]	Vout > 1.0 V, Irated/2 Vout < 1.0 V, Irated/2	-3 -30	0 0	3 +30	% mV
Temperature coefficient		-100	0	+100	ppm/°C
Enable overshoot Slow (normal) turn on	Vout > 1.0 V, no load Vout < 1.0 V, no load	– –	– –	3 30	% mV
Voltage step settling time per LSB [5]	To within 1% of final value	–	–	10	µs
Voltage dip due to low to high load transition (PWM/hysteretic) [6]		–	–	40	mV
Voltage overshoot due to high to load transition (PWM/hysteretic)		–	–	70	mV
Enable settling time Slow start (turning ON an OFF regulator) [7]	From enable to within 1% of final value, no load	–	–	500	µs
Load regulation	Vin ≥ Vout + 1 V with load from I_{rated}/100 to I_{rated}	–	–	0.25	%
Line regulation	Vin from 3.2 V to 4.2 V at 100 mA load	–	–	0.25	%/V
Short circuit/peak current limit (current draw through inductor) when VREG node is shorted to GND [8]	VREG_xxx pin = 0 V, Ilimit is the SBI setting for the current limit.	0.7 Ilimit	Ilimit	1.3 Ilimit	A
Ground current, no load [9]	PWM/hysteretic mode PFM mode	– –	300 15	550 30	µA
Mode transition voltage undershoot PWM/hysteretic ─ PFM	V_{out} > 1.0 V, I_load = 20 mA V_{out} < 1.0 V, I_load = 20 mA	–	–	(-3%)	% mV
Mode transition voltage overshoot PFM ─ PWM/hysteretic	V_{out} > 1.0 V, I_load = 20 mA V_{out} < 1.0 V, I_load = 20 mA	–	–	(+3%)	% mV
Mode transition voltage overshoot Hysteretic PWM or vice versa	V_{out} > 1.0 V V_{out} < 1.0 V	–	–	(+3%)	% mV
Ripple voltage in PWM pulse skipping mode (hysteretic current controlled mode and regular PWM mode) [10]	Tested at the switching frequency at 40 mA (the threshold to enter pulse skipping is programmable) at a 20 MHz BW limit	–	–	50	mVpp

Table 3-22 HF-SMPS performance specifications[1] (cont.)

Parameter	Test condition	LLimit	Typical	ULimit	Units
Buck SMPS output ripple PWM in non-pulse skipping mode (regular PWM mode) (hysteretic current controlled mode and regular PWM mode) [11]	Tested at switching frequency at capacitor rated current or Irated at a 20 MHz BW limit	–	10	20	mVpp
Buck SMPS output ripple PFM mode	Based on PFM limit at 20 MHz BW limit	–	30	50	mVpp
Power supply ripple rejection ratio (PSRR)	50 Hz to 1 kHz 1 kHz to 100 kHz	– –	40 20	– –	dB dB
Buck SMPS efficiency at PWM and V_{bat} = 3.6 V	Vo = 1.8 V, Io = 300 mA Vo = 1.8 V, Io = 10–600 mA Vo = 1.8 V, Io = 800 mA	– – –	90 85 80	– – –	% % %
Buck SMPS efficiency at PFM	Vo = 1.2 V, Io = 5 mA	–	80	–	%
Output noise	Frequency < 5 kHz 5 kHz < freq < 10 kHz 10 kHz < frequency < 500 kHz 500 kHz < frequency < 1 MHz Frequency > 2 MHz WCS based on PMIC3 measurement data	– – – – –	-95 -100 -100 -110 -110	– – – – –	dBm/Hz

1. Ripple dependent on the external capacitor; capacitor ≤ ESR 20 mW.
   All parameters are based on the nominal L and C values over the operating temperature and input supply range, unless noted otherwise.
   The total DC error = DC_error + Temperature_coefficient + line_regulation + load_regulation.
   Transient step performance specifications measured at the output filter capacitor terminal, based on the external component recommendations.
   The transient response performance is strongly affected by the external components and board-level routing. Refer to the external component recommendation and layout guideline sections for details.
   Typical efficiency plots (N versus I with a family of voltage set points and by mode) are included in the typical characteristics section. Actual efficiency is strongly affected by the external components and board-level routing.
   Settling time when stepping down in voltage is a function of output capacitance, output loading, and loop response. A first-order estimate of dt = C * dV/I_load suggests that a 25 mV step at nominal capacitance will be dominated by the loop response for more than approximately 50 mA loading with roughly the same settling as a step up n voltage (~ µs). For lighter loading, the settling time will be dominated by the output capacitor discharge rate by the load current.
   Inductance used for the buck is selected to achieve the best tradeoff between efficiency and current control loop stability. It determines the swing range of the regulated buck's current. A wider swing range makes the loop more tolerant to noise while the resulting efficiency is low. In practice, 1.0–2.2 µH is acceptable at the switching frequency of 2.74 MHz. For 6.4 MHz, 0.5–1.0 µH is recommended since the swing range is reduced.
2. Layout option: scalable bolt-on output stage for load capability by the power domain. Maintain the current software control options over FET sizes and output buffers.
3. Over the entire component range.
4. Measured at the output capacitance at 25°C and trimmed voltage setting.
5. Voltage step at 1 LSB.
6. Depending on the Imax performance over Vin/Vout/Fsw range and also depending on the values of the external L and C used.
7. PON soft-start: 500 µs; configurable soft-start: 100, 500 µs (fast, slow).
8. This specification is for default current limit that is programmable.

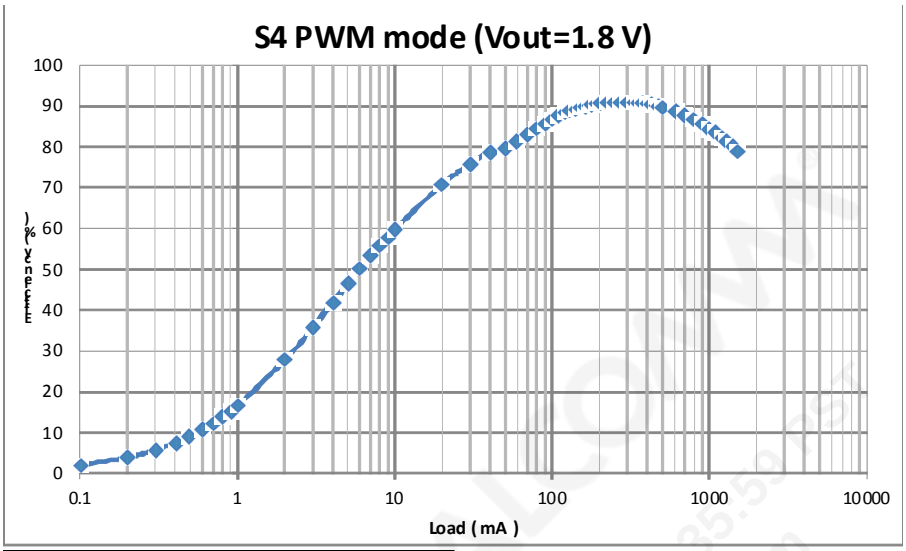
9. Quiescent current (no switching). The ground current sleep current includes extra 50 µA to meet tolerance in peak current Ilimit.
10. Ripple dependent on the external components and layout.
11. Ripple dependent on the external capacitor; capacitor < ESR 20 mΩ.

Table 3-23 2000 mA FT-SMPS performance specifications [1] [2]

Parameter	Comments	Min	Typ	Max	Unit
Rated load current (I_{rated})					
Normal PWM mode		–	–	2000	mA
Low-power PFM mode		–	–	100	mA
V_OUT, programmable range	Selected in SW				
Option 1, power collapsed state	50 mV increments	0.350	0.500	0.650	V
Option 2, active digital core	12.5 mV increments	0.700	1.100	1.4875	V
Option 3, other applications [3]	50 mV increments	1.500	–	3.300	V
V_OUT, guaranteed performance		0.350	–	3.300	V
Voltage error	At half rated current				
V_OUT > 1.000 V		-1	0	+1	%
V_OUT < 1.000 V		-10	0	+10	mV
Temperature coefficient		-100	0	+100	ppm/C
Transient response					
Soft-start settling time at enable	To within 1% of final value	–	–	1	ms
Overshoot at enable		–	–	+3	%
Load changes, PWM mode					
Undershoot	200 to 1500 mA load change	–	–	40	mV
Overshoot	1500 to 200 mA load change	–	–	70	mV
Programmed voltage change					
Overshoot		–	–	1	%
Settling time		–	–	TBD	µs
Load regulation	V_{in} > V_{out} + 1 V; I_{rated}/100 to I_{rated}	–	–	0.25	%
Line regulation	V_{in} = 3.0 to 4.2 V	–	–	0.25	%/V
Output ripple, constant load					
PWM (normal) mode		–	–	20	mVpp
PFM (low-power) mode		–	–	50	mVpp
PSRR	Power supply ripple rejection ratio				
50 to 1000 Hz		–	50	–	dB
1 to 100 kHz		–	30	–	dB
Efficiency – PWM mode	V_{in} = +3.6 V				
I_{load} = 100 to TBD mA	V_{out} = TBD	–	TBD	–	%
I_{load} = 1800 mA	V_{out} = TBD	–	TBD	–	%
Ground current					
No load, PFM mode	PFM – buck low-power mode	–	TBD	TBD	µA
No load, PWM mode	PWM – buck normal mode	–	–	TBD	µA

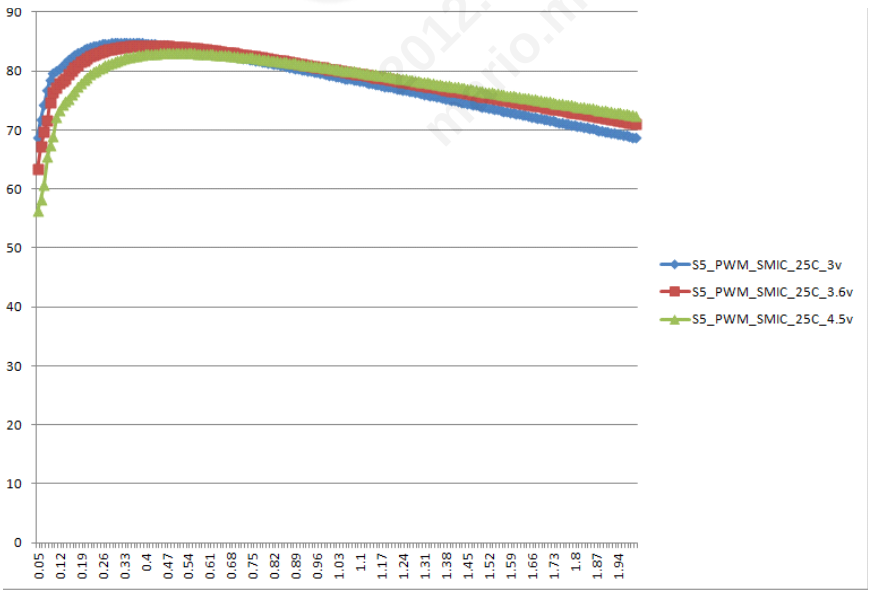
1. All specifications apply over the device's recommended operating conditions, load current range, and capacitor ESR range, unless noted otherwise.

2. Performance characteristics that may degrade if the rated output current is exceeded:
   • Voltage error • Output ripple • Efficiency
3. Range 3 is available for supporting other functions in addition to digital cores – digital I/Os, RF circuits, mixed signal functions, and peripherals.



Vin (V)	3.70
Fsw (MHz)	1.60
InductorID	2p2u_Cyntec_PSE25201B
Vout	1.8

Figure 3-3 Sample measured efficiency of S4 HF SMPS in PWM mode using a Cyntec inductor plot



Fsw (MHz)	3.20
InductorID	1u_Cyntec_PSE25201B
Vout	1.05

Figure 3-4 Sample measured efficiency of S5 FT SMPS in PWM mode using a Cyntec inductor

3.6.3 Linear regulators

Six low dropout linear regulator designs are implemented within the PMIC:

- Design 1 – rated for 1200 mA
- Design 2 – rated for 600 mA
- Design 3 – rated for 300 mA
- Design 4 – rated for 150 mA
- Design 5 – rated for 50 mA
- Design 6 – rated for 5 mA

Performance specifications for each of these designs are presented in the following subsections.

3.6.3.1 1200 mA rating

The PM8921 IC includes five linear regulators that are rated for 1200 mA. The regulator's low-power mode reduces the quiescent current during the phone's sleep mode, but causes some performance degradation as detailed in Table 3-24. With a nominal capacitance of 4.7 µF, the discharge time with pull-down enabled for the 1200 mA LDO is ~ 3 ms.

Table 3-24 Linear regulator performance specifications – 1200 mA rating

Parameter [1]	Test condition	Llimit	Typ	Ulimit	Units
Normal mode					
Rated load current 1200 mA LDO [2 3]		1200	–	–	mA
Overall error [3 4 5]		-2	–	+2	%
Temperature coefficient [4]		-100	0	+100	ppm/°C
Undershoot, overshoot [3 6]	25% to 75% Irated load step	-4	0	4	%
Settling time [3 7]	To within 1% of the final value	20	100	200	µs
Dropout voltage LV NMOS LDO (1200 mA) [8 9]	Load at I_{rated}	–	47	60	mV
Load regulation [3 10]		–	–	0.3	%
Line regulation [3 11]		–	–	0.1	%/V
Short circuit current limit [3 12]	Short regulator output to ground	1.3	1.8	2.6	A
Soft current limit [4 13]	During startup	I_{rated} + 200	–	–	mA
Ground current, no load 1200 mA regulator [8]		–	200	220	µA

Table 3-24 Linear regulator performance specifications – 1200 mA rating (cont.)

Parameter [1]	Test condition	Llimit	Typ	Ulimit	Units
Low-power mode					
Rated load current 1200 mA LDO [2] [14]		10	–	–	mA
Overall error [14]		-4	0	+4	%
Undershoot, overshoot [6] [14]	25% to 75% Irated load step	-3	0	+3	%
Dropout voltage LV NMOS LDO (1200 mA) [9] [14]		–	–	60	mV
Load regulation [10] [14]		–	–	1	%
Line regulation [11] [14]		–	–	0.5	%/V
Ground current, no load 1200 mA regulators [14]		–	21	25	µA
Normal mode and low-power mode					
Ground current, with load [3] [15]		–	–	0.5	%
Bypass mode					
Ground current [16]		–	4	5	µA

1. For all digital interface and trim/BIST related specifications, refer to other appropriate documents.
2. The rated current is the current at which the regulator meets all specifications. Higher currents are allowed, but the regulator may need more headroom, i.e., the difference between input and output, which requires simulations of headroom vs. current up to 2 x Irated while meeting all other specifications. For low-power mode, there is no need to exceed the rated current.
3. These specifications must be met through the full device operating range, load current range, capacitor ESR range, and process corners unless otherwise noted.
4. The error and temperature coefficient specifications include the bandgap reference error (< ± 0.5%). The regulator itself should have less than ±0.85% error, and trim should be used to meet the overall ±1% necessary.
5. At temperature and process corners, the N1200 LV LDO pass device leaks enough to raise the output node to 0.9 V under no load conditions. For the 0.9 V output voltage program setting or less, this leakage must be taken into account with an external minimum load.
6. Overshoot and undershoot specifications should be met with the rated load capacitance and at any of the following conditions: startup, any load step change, line voltage change, program voltage change, and transitions between normal and low-power modes. For low-power mode, only transitions between normal and low-power modes, load change (within limit), and line change apply.
7. The regulator always turns on in normal mode. The settling time is for startup and any voltage change with the rated load capacitance. Time will be increased with larger load capacitance.
8. These specifications must be met with ±6 σ compliance, unless otherwise noted.
9. Dropout only includes module Rds(on) and does not include parasitic package or board resistance. Dropout voltage is defined as follows:
   Apply the specified load current
   Set Vin = Vout + 0.5 V
   Measure the output voltage
   Reduce Vin until Vout is reduced by 100 mV
   Calculate dropout voltage as Vin – Vout in this condition
10. Load regulation is calculated as the output change in percent when Vi>Vo+0.5V with load changing from Irated/100 to Irated: (Vo2-Vo1)/Vo1.

11. Line regulation is the output variation as the input is calculated as the output change in percent divided by the input voltage change, [(Vo2-Vo1)/Vo1]/(Vi2-Vi1), with input changing:

    From 1.1 V to 1.8 V for LV NMOS LDO
12. The current limit test mode will be used while in HPM to evaluate the actual current limit threshold in normal mode. The threshold of test mode is 6% of normal mode, and the test mode accuracy will be within ±20%.
13. The peak inrush current must remain under within this specification. A soft current limit is required to avoid too much instantaneous current draw from battery in the meantime still meeting turn-on time requirement.
14. These low-power mode specifications should be met but negotiable through the full device operating range, load current range, and capacitor ESR range, and process corners
15. Ground current with load is specified as a percentage of the output current load, (Itotal-Iload)/Iload.
16. In bypass mode, there is an active gate to source clamp to protect the LV NMOS.

3.6.4 PMOS LDO

The performance specifications for the PMOS LDOs (600 mA, 300 mA, 150 mA, and 50 mA) are as follows. With a nominal capacitance on the LDO output, the discharge time with pull-down enabled is ~ 3ms.

3.6.4.1 600, 300, 150, and 50 mA rating

Table 3-25 LDO regulator specifications

Parameter [1]	Test condition	LLimit	Typ	ULimit	Units	Notes
Normal mode						
Rated load current					mA	2
50 mA LDO		–	–	50		
150 mA LDO		–	–	150		
300 mA LDO		–	–	300		
USB LDO		–	–	50		
600 mA LDO				600		
Overall error	Including load, line regulation and variation over temperature at default programmed voltage	-2	–	+2	%	3, 5
Temperature coefficient		-100	–	+100	ppm/°C	5
Undershoot, overshoot	With Irated/100 to Irate Istep, time step is 0.1 µs, and 1 µF output capacitor	-50	–	70	mV	4, 6
Settling time	To within 1% of final value	20	100	200	µs	4, 7
Dropout voltage			–		mV	4, 8, 18
PMOS LDO (50 mA, 150 mA, and 300 mA)	Load at I_{rated}	–		300		
USB LDO, VDD input	Load at I_{rated}	–		200		
USB LDO, USB_VBUS and VREG_5V inputs	Load at I_{rated}	–		600		
Load regulation	Measured at the output of the device	–	–	0.3	%	3, 9

Table 3-25 LDO regulator specifications (cont.)

Parameter [1]	Test condition	LLimit	Typ	ULimit	Units	Notes
Line regulation		–	–	0.1	%/V	3, 10
Short circuit current limit	Short regulator output to ground	1.5	2.5	3.5	Irated	3, 11
Soft current limit	During start-up	–	–	I_{rated}+100	mA	4, 12
Ground current, no load					µA	4
50 mA regulators (including USB LDO)		–	45	100		
150 mA regulators		–	55	100		
300 mA regulators		–	65	150		
600 mA regulators		–	90	300		
***Low-power mode*[13]**						
Rated load current					mA	2, 14
50 mA LDO		–	–	5		
150 mA LDO		–	–	10		
300 mA LDO		–	–	10		
600 mA LDO		–	–	10		
USB LDO		–	–	5		
Overall error		-4	0	+4	%	3, 5, 14
Undershoot, overshoot		-3	0	3	%	6, 14
Dropout voltage					mV	8, 15, 18
PMOS LDO (50 mA, 150 mA, 300 mA, and 600 mA)	Load at I_{rated}	–	–	300		
USB LDO, VDD input						
USB LDO, USB_VBUS, and VREG_5V inputs	Load at I_{rated}	–	–	200		
	Load at I_{rated}	–	–	600		
Load regulation		–	–	1.5	%	9, 15, 18
Line regulation		–	–	0.5	%/V	10, 15, 18
Ground current, no load					µA	14, 16
50 mA regulators (including USB LDO)		–	5	6		
150 mA regulators		–	5	6		
300 mA regulators		–	5	6		
600 mA regulators		–	5	6		
Normal mode and low-power mode						
Ground current, with load		–	–	0.2	%	4, 17

Notes:
1. For all digital interface and trim/BIST related specifications, refer to the appropriate documents.

2. The rated current is the current at which the regulator meets all specifications. Higher currents are allowed, but the regulator may need more headroom, i.e., the difference between input and output. This requires simulations of headroom vs. current up to 2 X I_{rated} while meeting all other specifications. For low-power mode, there is no need to exceed the rated current.
3. All the parametric specifications, including accuracy, load regulation, line regulation, short circuit current limit, PSRR, and ground current must be met with $\pm 6\sigma$ compliance, unless otherwise noted.
4. These specifications must be met through the full device operating range, load current range, capacitor ESR range, and process corners unless otherwise noted.
5. The error and temperature coefficient specifications include the bandgap reference error (< $\pm$ 0.5%). The regulator itself should have less than $\pm$0.85% error. Trim could be used if necessary.

   Overshoot and undershoot specifications should be met with the rated load capacitance and as the output change in percent when $V_i > V_o + 0.5$ V with load changing from $I_{rated}/100$ to I_{rated}: $(V_{o2}-V_{o1})/V_{o1}$ and at any of the following conditions: start-up, any load step change, line voltage change, program voltage change, and transitions between normal and low-power modes. For low-power mode, only transitions between normal and low-power modes, load change (within limit), and line change apply.
6. Regulator always turns on in normal mode. The settling time is for start-up and any voltage change with the rated load capacitance. Time is increased with larger load capacitance.
7. Dropout voltage is defined as follows:
   - Apply the specified load current
   - Set Vin = Vout + 0.5 V
   - Measure the output voltage
   - Reduce Vin until Vout is reduced by 100 mV
   - Calculate dropout voltage as Vin – Vout in this condition
8. Load regulation is calculated as the output change in percent when $V_i > V_o + 0.5$ V with load changing from $I_{rated}/100$ to I_{rated}: $(V_{o2}-V_{o1})/V_{o1}$.
9. Line regulation is the output variation as the input is calculated as the output change in percent divided by the input voltage change, $[(V_{o2}-V_{o1})/V_{o1}]/(V_{i2}-V_{i1})$, with input changing:
   - From 3.35 V to 4.35 V for PMOS LDO
   - From 3.8 to 4.8 V for VDD input of USB LDO
   - From 4.5 to 5.5 V for VREG_5V and USB_VBUS inputs of USB LDO
10. The current limit test mode in HPM is used to evaluate the actual current limit threshold in normal mode. The threshold of test mode is 10% of normal mode, the test mode accuracy is within $\pm$10%.
11. A soft current limit is required to avoid too much instantaneous current draw from the battery while still meeting turn-on time requirement.
12. These low-power mode specifications must be met through the full device operating range, load current range, capacitor ESR range, and process corners.
13. These low-power mode specifications should be met but negotiable through the full device operating range, load current range, capacitor ESR range, and process corners.
14. The low-power mode no-load ground current may be higher due to the current limiting mistrigger in low headroom configuration in PMOS LDOs. Disabling the current limiting feature or giving enough headroom per the dropout requirement can prevent the mistriggering and reduce the ground current.
15. Ground current with load is specified as a percentage of the output current load, $(I_{total}-I_{load})/I_{load}$.
16. This specification is with the specified load capacitance and applies to both normal and dynamic pull-down. Higher capacitance increases this discharge time. Active pull-down is required to have a well-behaved power-down. Actual implementation could be using 1 kHz clock, RC timer, or reusing VREG_OK comparator.
17. The time-out is required for not holding regulator output low indefinitely. A crystal oscillator based 1 kHz clock could be available for this purpose. Therefore, a $\pm$0.5 ms error can be assumed for the time-out.
18. On resistance includes pass device Rds(on) and all parasitic resistance and should be around 1 Ω based on drop-out specification.

In addition to the performance specified in Table 3-25, Table 3-26 lists some typical characteristics of the LDO modules.

Table 3-26 LDO regulator typical specifications [1]

Parameter	Test condition	LLimit	Typ	ULimit	Units
Normal mode					
Power supply ripple rejection ratio (PSRR)	50 Hz to 1 kHz 1 kHz to 10 kHz 10 kHz to 100 kHz 100 kHz to 1 MHz	60 50 40 35	70 60 50 45	– – – –	dB
Low-power mode					
Power supply ripple rejection ratio (PSRR)	50 Hz to 1 kHz 1 kHz to 100 kHz	40 30	50 40	– –	dB

1. PSRR is measured with:
   - Vin = Vout + 0.5 V for PMOS LDO.
   - For USB LDO (only used at 3.3 V), when VREG_5V or USB_VBUS is used as input, Vin = Vout + 1 V and VDD, Vin = Vout + 0.5 V.

Table 3-27 lists the performance specifications of the vreg_xo and vreg_rfclk voltage regulators.

Table 3-27 LDO regulator specifications for vreg_xo and vreg_rfclk [1]

Parameter	Test condition	Llimit	Typ	Ulimit	Units	Notes
Normal mode						
Rated load current		–	–	5	mA	
Overall error		–1.15	–	+1.15	%	Including temperature range
Settling time	To within 1% of final value	–	–	250	µs	
Startup current limit	During start-up	–	–	I_{rated}+100	mA	
Ground current, no load		–	–	80	µA	Loaded current = NLGC + 2% of load current
PSRR	With switching load 50 Hz to 1 kHz 1 kHz to 10 kHz 10 kHz to 100 kHz 100 kHz to 1 MHz	 – – – –	 – – – –	 40 40 40 37	dB	

1. For all digital interface and trim/BIST related specifications, refer to the appropriate documents.

3.6.5 NMOS LDO

The detailed specifications for the NMOS LDOs are detailed in Table 3-28.

Table 3-28 Linear regulator performance specifications – 150 mA rating

Parameter	Test condition	LLimit	Typ	ULimit	Units	Notes
Normal mode						
Rated load current 150 mA LDO 300 mA LDO		 – –	 – –	 150 300	 mA mA	1
Overall error		-2	–	+2	%	2, 4
Temperature coefficient		-100	–	+100	ppm/°C	4
Undershoot, overshoot		-3	–	3	%	3, 5
Settling time	To within 1% of final value	20	100	200	µs	3, 6
Dropout voltage NMOS LDO (150 mA, 300 mA)	Load at I_{rated}	–	–	200	mV	3, 7, 17, 18
Load regulation		–	–	0.3	%	2, 8
Line regulation		–	–	0.1	%/V	2, 9
Short circuit current limit	Short regulator output to ground	2	3	4	Irated	2, 10
Soft current limit	During startup	–	–	I_{rated} + 100	mA	3, 11
Ground current, no load 150 mA regulators (including NMOS LDO) 300 mA regulators (including NMOS LDO)		 – –	 100 100	 150 150	 µA	3
Low-power mode[13]						
Rated load current 150 mA LDO 300 mA LDO		 – –	 – –	 10 10	 mA	1, 13
Overall error		-4	0	+4	%	2, 4, 13
Undershoot, overshoot		-3	0	3	%	5, 13
Dropout voltage NMOS LDO (150 mA, 300 mA)	Load at I_{rated}	–	–	200	mV	7, 14, 17, 18
Load regulation		–	–	1.5	%	8, 14, 17
Line regulation		–	–	0.5	%/V	9,14, 17
Ground current, no load 150 mA regulators (including NMOS LDO) 300 mA regulators (including NMOS LDO)		 – –	 5 5	 6 6	 µA	13,15

Table 3-28 Linear regulator performance specifications – 150 mA rating (cont.)

Parameter	Test condition	LLimit	Typ	ULimit	Units	Notes
Normal mode and low-power mode						
Ground current, with load		–	–	0.5	%	3, 16

Notes:

1. The rated current is the current at which the regulator meets all specifications. Higher currents are allowed, but the regulator may need more headroom, i.e., the difference between input and output, which requires simulations of headroom vs. current up to 2 x I_{rated} while meeting all other specifications. For low-power mode, there is no need to exceed the rated current.
2. All the parametric specifications, including accuracy, load regulation, line regulation, short circuit current limit, PSRR, and ground current, must be met with 6σ compliance, unless otherwise noted.
3. These specifications must be met through the full device operating range, load current range, and capacitor ESR range, and process corners, unless otherwise noted.
4. The error and temperature coefficient specifications include the bandgap reference error (< ± 0.5%). The regulator itself should have less than ±0.85% error, and trim could be used if necessary.
5. Overshoot and undershoot specifications should be met with the rated load capacitance and as the output change in percent when $V_i > V_o + 0.5$ V with load changing from $I_{rated}/100$ to I_{rated}: $(V_{o2}-V_{o1})/V_{o1}$ and at any of the following conditions: startup, any load step change, line voltage change, program voltage change, and transitions between normal and low-power modes. For low-power mode, only transitions between normal and low-power modes, load change (within limit), and line change apply.
6. The regulator always turns on in normal mode. The settling time is for startup, and any voltage change with the rated load capacitance. Time is increased with larger load capacitance.
7. Dropout voltage is defined as follows:
   - Apply the specified load current
   - Set Vin = Vout + 0.5 V
   - Measure the output voltage
   - Reduce Vin until Vout is reduced by 100 mV
   - Calculate dropout voltage as Vin – Vout in this condition
8. Load regulation is calculated as the output change in percent when $V_i > V_o + 0.5V$ with load changing from $I_{rated}/100$ to I_{rated}: $(V_{o2}-V_{o1})/V_{o1}$.
9. Line regulation is the output variation as the input is calculated as the output change in percent divided by the input voltage change, $[(V_{o2}-V_{o1})/V_{o1}]/(V_{i2}-V_{i1})$, with input changing:
   - From 3.35 V to 4.35 V for PMOS LDO
   - From 1.8V to 2.8 V for NMOS LDO
   - From 3.8 to 4.8 V for VDD input of USB LDO
   - From 4.5 to 5.5 V for VREG_5V and USB_VBUS inputs of USB LDO
10. The current limit test mode in HPM is used to evaluate the actual current limit threshold in normal mode. The threshold of test mode is 10% of normal mode, the test mode accuracy is within ±10%.
11. A soft current limit is required to avoid too much instantaneous current draw from battery in the meantime still meeting turn-on time requirement.
12. These low-power mode specifications must be met through the full device operating range, load current range, and capacitor ESR range, and process corners.
13. These low-power mode specifications should be met but negotiable through the full device operating range, load current range, and capacitor ESR range, and process corners.
14. The low-power mode no-load ground current may be higher due to the current limiting mistrigger in low headroom configuration in PMOS LDOs. Disabling current limiting feature or giving enough headroom as of the dropout requirement can prevent the mistriggering and reduce the ground current.
15. Ground current with load is specified as a percentage of the output current load, $(I_{total}-I_{load})/I_{load}$.
16. This specification is with the specified load capacitance and applies to both normal and dynamic pull-down. Higher capacitance increases this discharge time. Active pull-down is required to have a well-behaved power-down. Actual implementation could be using 1 kHz clock, RC timer, or reusing VREG_OK comparator.
17. There should be very small ground current in bypass mode when almost all features in LDO disabled and it acts as a switch between input and output voltage.

18. On resistance includes pass device Rds(on) and all parasitic resistance and should be around 1 Ω based on drop-out specification.

Table 3-29 LDO regulator typical specifications

Parameter	Test condition	LLimit	Typ	ULimit	Units	Notes
Normal mode						
Power supply ripple rejection ratio (PSRR)	50 Hz to 1 kHz 1 kHz to 10 kHz 10 kHz to 100 kHz 100 kHz to 1 MHz	60 50 40 35	70 60 50 45	– – – –	dB	
Low-power mode						
Power supply ripple rejection ratio (PSRR)	50 Hz to 1 kHz 1 kHz to 100 kHz	40 30	50 40	– –	dB	

Note:
1. For NMOS LDO, there are two PSRR requirements, one is from LDO input (Vin = Vout + 0.5 V) to output and the other from VDD (2.5 V to 5.5 V) to LDO output.

3.6.6 NCP

The PMIC includes a capacitor-based NCP switching regulator that generates a negative 1.8 V (-1.8 V) supply for capless stereo headphone drivers. Pertinent performance specifications are listed in Table 3-30.

Table 3-30 NCP regulator performance specifications

Parameter	Comments	Min	Typ	Max	Units
Switching frequency	Programmable [1]	0.6	1.6	9.6	MHz
Output voltage	Programmable [1 2]	-2.4	-1.8	-1.5	V
Load current range [1]		0	–	186	mA
Output error	Zero load [3]	–	–	50	mV
Transient overshoot		-200	–	100	mV
Line regulation	Up to 50 mA load [3]	–	20	50	mV/V
Line regulation	Up to 186 mA load [3]	–	25	65	V/A
PSRR at 2 kHz	pVdd to output	-15	-30	–	dB
PSRR at 5 kHz	pVdd to output	-15	-30	–	dB
PSRR at 20 kHz	pVdd to output	-15	-25	–	dB
Output ripple		–	150	350	mV
Load regulation	Up to 93 mA load [3]	–	0.1	0.2	V/A
Load regulation	Up to 150 mA load [3]	–	0.1	0.3	V/A
Load regulation	Up to 186 mA load [3]	–	0.1	0.4	V/A

1. All performance specifications are determined with default output voltage (-1.8 V) and frequency (1.6 MHz) settings, using 0402 X5R 2.2 µF 6.3 V capacitors from Taiyo Yuden Co., maximum load 186 mA, 2.5 V to 5.5 V unregulated input voltage, and operating in “non-sampling” mode.

2. Maximum deviation in output under a given load calculated as follows:
   (Output Error + (Load Regulation * Load Current) + (Line Regulation * pVdd variation)).
3. Performance specifications are not guaranteed for an output voltage beyond -1.8 V. Notable degradation in load regulation and other specifications may be observed beyond -1.8 V.

3.6.7 Voltage switches

The PM8921 has seven low-voltage switches and two medium-voltage switches. The LVS are rated for 100 mA and 300 mA, while the MVS are rated for 100 mA and 500 mA and are used for gating the supply voltages to external circuits like BT, WLAN, UBM and other functions. LVS 1, 3, 4, 5, 6, and 7 are 100 mA LVS, whereas LVS 2 is a 300 mA LVS. The performance specifications for these switches are listed in Table 3-31.

Table 3-31 100 mA low-voltage switch specifications

Parameter	Condition	Min	Typical	Max	Units
Load current [1]	Normal operation	–	–	100	mA
Input voltage range		1.0	–	1.8	V
Soft start time [2]	Cload < 1 µF	–	–	200	µs
Soft start inrush [2]	Cload < 1 µF	–	–	200	mA
Over current threshold		2	4	6	X Irated
ON resistance [3]	The ON resistance of the switch	–	–	0.1	Ω
Ground current [4]	Sleep mode	–	–	1	µA
Ground current	Normal mode without load	–	–	30	µA
Ground current	Normal mode with load	–	–	30+0.03%	µA

1. Other rated current may be required in the future.
2. The load cap should be less than 1 µF, which is mainly estimated for decoupling cap.
3. This specification is measured via the voltage drop and the load current
4. Sleep current means the quiescent current in sleep mode. Sleep mode means only switch is on and all the other functions are disabled. This module does not provide power supply noise rejection.

Table 3-32 300 mA low-voltage switch specifications

Parameter	Condition	Min	Typical	Max	Units
Rated current (Irated)	Normal operation	–	300	–	mA
Slew rate (switch output node)	Always	–	–	100	mV/µS
Switch output ready [1]	Startup	100	300	1200	µs
Input voltage range		1.2		1.875	V
Over current threshold	Normal operation	1.3x	1.5x	2.6x	Irated
Pin-to-pin resistance (pin = package ball) [2]	Switch is ON (fully enhanced)	–	–	150	mΩ
Ground current (sleep mode)	Module is disabled	–	–	1	µA

Table 3-32 300 mA low-voltage switch specifications (cont.)

Parameter	Condition	Min	Typical	Max	Units
Ground current (enabled mode)	Normal operation	–	–	40	µA
Pull-down discharge time	Switch is off	–	–	2	mS

1. This includes soft start time and gate full enhancement time.
2. The intrinsic LVS300 switch Rdson is 50 mΩ. The rest of pin-to-pin resistance is for package and trace resistances.

Table 3-33 100 mA MVS (HDMI) switch specifications

Parameter	Condition	Min	Typical	Max	Units
Rated current (Irated) [1]	Normal operation	55	–	–	mA
Switch output ready [2]	Startup	–	–	200	µs
Input voltage range		4.0	–	5.5	V
Over current threshold		4x	5x	6x	Irated
Pin-to-pin resistance [3] (pin = package ball)		–	–	2000	mΩ
Ground current (sleep and off mode)	Module is disabled	–	10	200	nA
Ground current (enabled mode)		–	40	–	µA
Pull-down discharge time		–	0.5	2	mS
Steady state reverse bias current [4]		–	20	–	nA
Steady state leakage current [5]		–	20	–	nA
Leakage current at max transient [6]		–	350	–	mA

1. Other rated currents may be required in the future.
2. Switch output ready means switch is fully enhanced which include time to get Vout_OK plus the time to fully enhance the switch (pull gate voltage to zero)
3. Pin-to-pin resistance includes switch Rdson, layout routing trace and package trace. Rdson should be below 1900 mΩ.
4. At 5.5 V output
5. At 9.0 V output
6. At 9.0 V output

Table 3-34 500 mA MVS (OTG) switch specifications

Parameter	Condition	Min	Typical	Max	Units
Rated current (Irated) [1]	Normal operation	500	–	–	mA
Switch output ready [2]	Startup	–	–	200	µS
Input voltage range		4.0	–	5.5	V
Over current threshold		1.3x	2x	2.6x	Irated
Pin-to-pin resistance (pin = package ball) [3]		–	–	200	mΩ

Table 3-34 500 mA MVS (OTG) switch specifications (cont.)

Parameter	Condition	Min	Typical	Max	Units
Ground current (sleep and off mode)	Module is disabled	–	10	200	nA
Ground current (enabled mode)		–	40	–	µA
Pull-down discharge time		–	0.5	2	mS
Steady state reverse bias current [4]		–	20	–	nA
Steady state leakage current [5]		–	20	–	nA
Leakage current at max transient [5]		–	350	–	mA

1. Switch output ready means switch is fully enhanced which include time to get Vout_OK plus the time to fully enhance the switch (pull gate voltage to zero)
2. Pin-to-pin resistance includes switch Rdson, layout routing trace and package trace. Rdson should be below 150 mΩ.
3. Other rated current may be required in the future.
4. At 5.5 V output
5. 9.0 V output

3.6.8 Internal voltage regulator connections

Some PM8921 IC modules use the outputs of certain voltage regulators for their operation. These connections are made internally to the device. The module and/or feature will not operate correctly unless the source voltage regulators are also enabled and set to the default voltage. See Table 3-35 for details.

Table 3-35 Internal voltage regulator connections

Module/feature name	Regulator	Default	Notes
AMUX	L14	1.8 V	AMUX supply
Charger	L14	1.8 V	VREF_BAT_THM supply
CLK	VIN_L1_L2_L12_L18	1.8 V	Sleep clock pad (Vio)
GPIO	S4 L4 L6 L15 L17 L3	1.8 V 1.8 V 2.9 V 2.9 V 2.9 V 3.075 V	
HSED<2:0>	L6	2.9 V	SDIO supply
MISC	VIN_L1_L2_L12_L18	1.8	MISC VDD_PAD IO
MPP	L4 L15 L17	1.8 V 2.9 V 2.9 V	
NCP	L6	2.6 V	NCP level shifter supply
PON	VIN_L1_L2_L12_L18	1.8 V	PADIO (Vio)
SEC_INT	VIN_L1_L2_L12_L18	1.8 V	SEC_INT PADIO (Vio)
SSBI	VIN_L1_L2_L12_L18	1.8 V	SSBI pad (Vio)

Table 3-35 Internal voltage regulator connections (cont.)

Module/feature name	Regulator	Default	Notes
CLOCKS	XO	1.8 V	XO core
CLOCKS	RF_CLK	1.3V	Low-noise output buffers (XO_OUT_Ax)
CLOCKS	L4	1.8 V	Low-power output buffers (XO_OUT_Dx)
XO_ADC	L14	1.8 V	XO_ADC supply

3.7 General housekeeping

The PMIC includes many circuits that support handset-level housekeeping functions – various tasks that must be performed to keep the handset in order. Integration of these functions reduces the external parts count and the associated size and cost. Housekeeping functions include an analog switch matrix, multiplexers, and voltage scaling; an HK/XO ADC circuit; system clock circuits; a realtime clock for time and alarm functions; and overtemperature protection.

All parameters associated with general housekeeping functions are specified in the following subsections.

3.7.1 Analog multiplexer and scaling circuits

A set of analog switches, analog multiplexers, and voltage scaling circuits select and condition a single analog signal for routing to the on-chip HK/XO ADC. The multiplexer and scaling functions are summarized in Table 3-36.

Table 3-36 Analog multiplexer and scaling functions

Channel #	Description	Typical input range (V)	Automatic scaling	Typical output range (V)	Notes
0	VCOIN pin	2.0 to 3.25	1/3	0.67 to 1.08	1
1	VBAT pin	2.5 to 4.5	1/3	0.83 to 1.5	
2	DCIN pin (over-voltage protected)	4.5 to 9.5	1/6	0.75 to 1.58	3
3	–	–	–	–	
4	VPH_PWR	2.5 to 4.5	1/3	0.83 to 1.5	1
5	IBAT: battery charge current	0.3 to 1.5	1	0.3 to 1.5	
6	Selected input from MPP, ATEST	0.05 to (VDDA - 0.05)	1	0.05 to (VDDA - 0.05)	2
7	Selected input from MPP, ATEST	0.15 to 3*(VDDA - 0.05)	1/3	0.05 to (VDDA - 0.05)	2
8	BAT_THERM	0.05 to (VDDA - 0.05)	1	0.05 to (VDDA - 0.05)	
9	BAT_ID	0.05 to (VDDA - 0.05)	1	0.05 to (VDDA - 0.05)	
10	USBIN pin (over-voltage protected)	4.35 to 6.5	1/4	1.09 to 1.63	3
11	Die-temperature monitor	0.4 to 0.9	1	0.4 to 0.9	
12	0.625 V reference voltage	0.625	1	0.625	
13	1.25 V reference voltage	1.25	1	1.25	

Table 3-36 Analog multiplexer and scaling functions (cont.)

Channel #	Description	Typical input range (V)	Automatic scaling	Typical output range (V)	Notes
14	CHG_Temp: charger temperature	0.05 to (VDDA - 0.05)	1	0.05 to (VDDA - 0.05)	
15	Module power off	–	–	–	4

Notes:

1. Input voltage must not exceed internal VMAX voltage so as to prevent a forward-biased junction condition where correct module operation will cease. The VMAX voltage is defined as:

$$VMAX(x) = \max\left[vcoin(x), vbat(x), vchg(x), usb\_vbus(x)\right]$$

2. Channels 6 and 7 are the expanded channels for MPP and ATEST measurements. The signal is taken from a 16-to-1 preMUX inside this module.
3. DCIN and USBIN are protected inputs, i.e., no voltage is applied to AMUX if the OVP FETs are off when either of the charging source is above the threshold.
4. Set channel number to 15 when not in use so that the scaler does not load the inputs.

NOTE Gain and offset errors are different through each analog multiplexer channel. Each path should be calibrated individually over its valid gain and offset settings for best accuracy.

Performance specifications pertaining to the analog multiplexer and its associated circuits are listed in Table 3-37.

Table 3-37 Analog multiplexer performance specifications [1]

Parameter	Comments	Min	Typ	Max	Units
Supply voltage		–	1.8	–	V
Output voltage range Full specification compliance		0.200	–		V
Input referred offset errors	Unity scaling				
Channel x1		-2	–	+2	mV
Channel x1/3	Including process and temperature variations	-1.5	–	+1.5	mV
Channel x1/4		-3	–	+3	mV
Channel x1/6		-3	–	+3	mV
Gain errors	Includes scaler; excludes VREF error (see Table 3-21)	-0.3	–	+0.3	%
Channel x1		0.2	–	+0.2	%
Channel x1/3		0.15	–	+0.15	%
Channel x1/4		-0.3	–	+0.3	%
Channel x1/6		-0.3	–	+0.3	%
Integrated non-linearity	INL, after removing offset/gain errors	-3	–	+3	mV
Input resistance	Input referred to account for scaling	1	–	–	MΩ
Channel x1		10	–	–	MΩ
Channel x1/3		1	–	–	MΩ

Table 3-37 Analog multiplexer performance specifications (cont.)[1]

Parameter	Comments	Min	Typ	Max	Units
Channel x1/4		0.5	–	–	MΩ
Channel x1/6		0.5	–	–	MΩ
Channel-to-channel isolation	f = 1 kHz	50	–	–	dB
Output settling time [2]	C_{load} = 65 pF	–	–	25	µs
Output noise level	f = 1 kHz	–	–	2	µV/Hz$^{1/2}$

1. Multiplexer offset error, gain error, and INL are measured as illustrated in Figure 3-5. Supporting comments:
   - The non-linearity curve is exaggerated for illustrative purposes.
   - Input and output voltages must stay within the ranges stated in Table 3-37; voltages beyond these ranges result in non-linearity and are beyond specification.
   - Offset is determined by measuring the slope of the endpoint line (m) and calculating its Y-intercept value (b):
     Offset = b = $y_1 - m \cdot x_1$
   - Gain error is calculated from the ideal response and the endpoint line as the ratio of their two slopes (in percentage):
     Gain_error = [(slope of endpoint line)/(slope of ideal response) - 1]·100%
   - INL is the worst-case deviation from the endpoint line. The endpoint line removes the gain and offset errors to isolate nonlinearity:
     INL(min) = min[V_{out}(actual at V_x input) - V_{out}(endpoint line at V_x input)]
     INL(max) = max[V_{out}(actual at V_x input) - V_{out}(endpoint line at V_x input)]
2. See Figure 3-6 for a model of the typical load circuit. C1 represents parasitic capacitance (0 to 20 pF); C2 is the sampling capacitor (63 pF); and S1 is the sampling switch (1 kΩ maximum). After S1 closes, the voltage across C2 settles within the specified settling time.

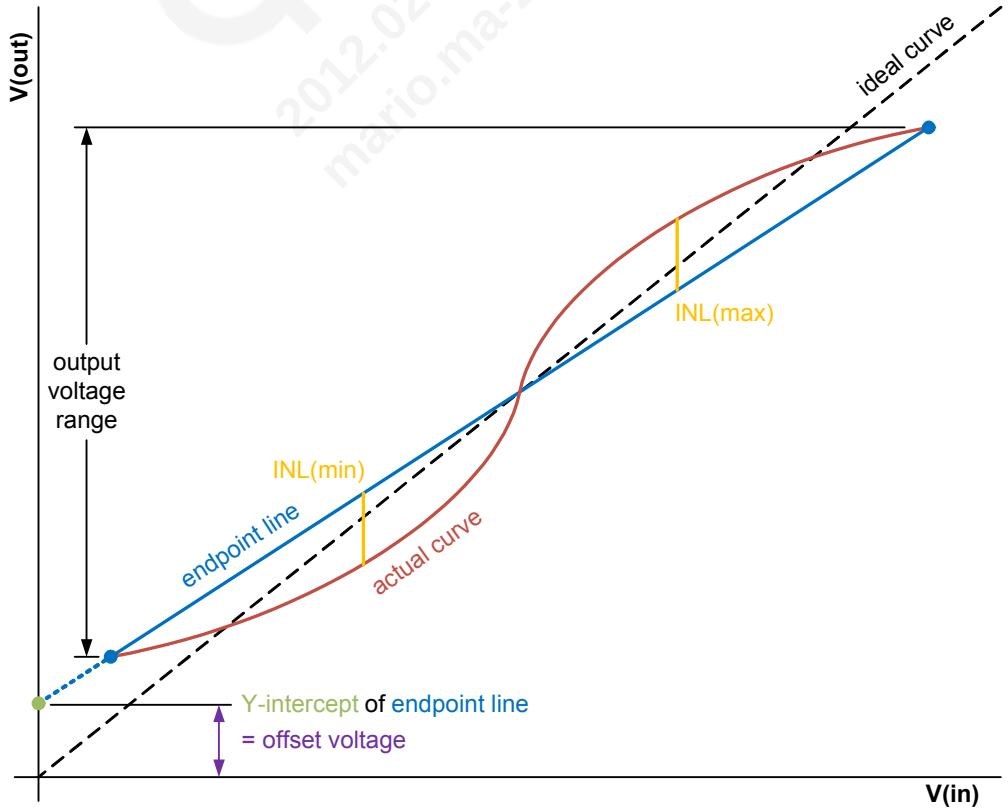


Figure 3-5 Multiplexer offset and gain errors

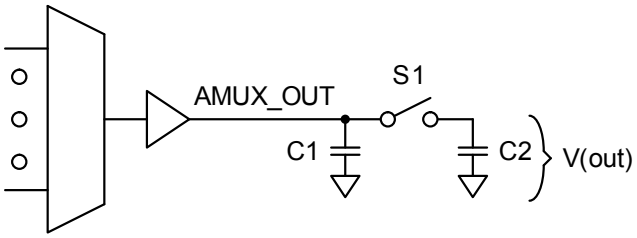


Figure 3-6 Analog multiplexer load condition for settling time specification

3.7.2 HK/XO ADC circuit

The PM8921 IC includes an analog-to-digital converter circuit that is shared by the housekeeping (HK) and 19.2 MHz crystal oscillator (XO) functions. A 2:1 analog multiplexer selects which source is applied to the ADC:

- The HK source – the analog multiplexer output discussed in Section 3.7.1; or
- The XO source – the thermistor network output that estimates the 19.2 MHz crystal temperature.

HK/XO ADC performance specifications are listed in Table 3-38.

Table 3-38 HK/XO ADC performance specifications

Parameter	Comments	Min	Typ	Max	Units
Supply voltage		–	1.8	–	V
Resolution		–	–	15	bits
Analog input bandwidth		–	100	–	kHz
Sample rate	XO/8	–	2.4	–	MHz
Offset error		-1	–	+1	%
Gain error		-1	–	+1	%
INL	15 bit output	-8	–	+8	LSB
DNL	15 bit output	-4	–	+4	LSB

3.7.3 System clocks

The PMIC includes several clock circuits whose outputs are used for general housekeeping functions, and elsewhere within the handset system. These circuits include a 19.2 MHz XO with multiple controllers and buffers, an MP3 clock output, 32.768 kHz crystal support, an RC oscillator, sleep clock outputs, and internal SMPL and SMPS clocks. Performance specifications for these functions are presented in the following subsections.

3.7.3.1 19.2 MHz XO circuits

An external crystal is supplemented by on-chip circuits to generate the desired 19.2 MHz reference signal. Using an external thermistor network, the on-chip ADC, and advanced temperature compensation software, the PMIC eliminates the large and expensive VCTCXO module required by previous generation chipsets. The XO circuits initialize and maintain valid pulse waveforms and measure time intervals for higher-level handset functions. Multiple controllers manage the XO warmup and signal buffering, and generate the desired clock outputs (all derived from one source):

- XO_OUT_A0
- XO_OUT_A1
- XO_OUT_A2
- XO_OUT_D0
- XO_OUT_D1

Since the different controllers and outputs are independent of each other, non-phone circuits can operate even while the phone's baseband circuits are asleep and its RF circuits are powered down.

The PM8921 IC has built-in load capacitors on XTAL_19M_IN and XTAL_19M_OUT. A crystal that specifies 7 pF load caps is recommended because no external load capacitors will be required. This reduces the noise picked up from the GND plane.

The XTAL_19M_IN and XTAL_19M_OUT pins are incapable of driving a load – the oscillator will be significantly disrupted if either pin is externally loaded.

As discussed in Section 3.7.3.5, an RC oscillator is used to drive some clock circuits until the XO source is established.

Table 3-39 Specifications for XO_OUT_D0 and XO_OUT_D1

Parameter	Comments	Specification			Unit	Notes
		Min	Typ	Max		
Frequency	Set by external crystal	–	19.2	–	MHz	
Duty cycle		46	50.0	54	%	
USB 2.0 jitter 1 (0.5 MHz – 2 MHz)		–	–	50	ps p-p period jitter	4
USB 2.0 jitter 2 (> 2 MHz)		–	–	100	ps p-p period jitter	4
Startup time		–	–	6	ms	1
Startup time	Warmup time enhancement feature enabled	–	–	3.5		1, 2
Current consumption		0.94	0.98	1	mA	2
Operating voltage		1.782	1.8	1.818	V	
Output buffer impedance	1x	54/4	80	122	Ω/mA	3
	2x	30/8	42	64		
	3x	21/12	30	44		
	4x	17/16	22	35		

Notes:
1. Duty cycle is defined as the first pulse duty cycle that meets the overall duty cycle specification and frequency settling to within TBD ppm.
2. When the warmup time enhancement feature is enabled, this can be reduced to 3.5 ms (to be finalized after analysis of more characterization data).
3. Output impedance at each drive strength varies 30% over corners. Current drive capabilities included to meet VOH = 0.65 · VDD and VOL = 0.35 · VDD.
4. USB period jitter can be calculated by 14 · $Jitter_{rms}$ based on 10^{-12} BER requirement.

3.7.3.2 Typical 19.2 MHz XO crystal requirements

Table 3-40 Typical 19.2 MHz crystal specifications (2520 size)

Parameter	Min	Typ	Max	Units	Notes
Operating frequency	–	19.2	–	MHz	
Mode of vibration	–	AT-cut fundamental	–	–	
Initial frequency tolerance	–	–	±10	PPM	
Tolerance over temperature	–	–	±12	PPM	
Aging	–	–	±1	PPM/year	
Frequency drift after reflow	–	–	±2	PPM	After two reflows
Operating temperature	-30	–	+85	^{0}C	
Storage temperature	-40	–	+85	^{0}C	
Equivalent series resistance		–	80	Ω	New for2520 crystals
Quality factor (Q)	75,000	–	–	–	Minimum Q value calculated from ESR and L is smaller than this specification
Spurious mode series resistance	1100	–	–	Ω	±1 MHz
Motional capacitance	1.80	–	3.10	fF	New for 2520 crystals
Shunt capacitance	0.3	–	1.3	pF	
Load capacitance	–	7	–	pF	Load capacitance is measured according to IEC standard #60444-7
Third-order curve fitting parameter	8.5	10	11.5	e-5	Curve fitting parameter is obtained from the Qualcomm crystal curve-fitting algorithm
Drive level	10	–	100	µW	
Insulation resistance	500	–	–	MΩ	
Package size	–	2.5 × 2.0	–	mm	

Table 3-41 Specifications for XO_OUT_A0, XO_OUT_A1, and XO_OUT_A2

Parameter	Comments	Specification			Unit	Notes
		Min	Typ	Max		
Frequency	Set by external crystal	–	19.2	–	MHz	
Duty cycle		40	50.0	60.0	%	
Startup time		–	6	–	ms	1
Current consumption	HPM	0.89	1.14	1.38	mA	2
	NPM	1.11	1.23	1.52		
	LPM	1.23	1.39	1.74		
Output voltage swing		1.2	–	1.8	V	
Output buffer impedance	1x	54/4	80	122	Ω/mA	3
	2x	30/8	42	64		
	3x	21/12	30	44		
	4x	17/16	22	35		
Phase noise in LPM	@ 10 Hz	–	–	-86	dBc/Hz	
	@100Hz	–	–	-110		
	@ 1kHz	–	–	-124		
	@ 10 kHz	–	–	-134		
	@ 100 kHz	–	–	-140		
	@ 1MHz	–	–	-137		
Phase noise in NPM	@ 10 Hz	–	–	-86	dBc/Hz	
	@100 Hz	–	–	-116		
	@ 1 kHz	–	–	-134		
	@ 10 kHz	–	–	-144		
	@ 100 kHz	–	–	-144		
	@ 1 MHz	–	–	-144		
Phase noise in HPM	@ 10 Hz	–	–	-86	dBc/Hz	
	@100 Hz	–	–	-116		
	@ 1 kHz	–	–	-134		
	@ 10 kHz	–	–	-144		
	@ 100 kHz	–	–	-148		
	@ 1 MHz	–	–	-150		

Notes:
1. When the warmup time enhancement feature is enabled, this can be reduced to 3.5 ms (to be finalized upon more char data)
2. Includes 15 pF load cap, output swing = 1.8 V.
3. Output impedance at each drive strength varies 30% over corners. Current drive capabilities included to meet VOH = 0.65 · VDD and VOL = 0.35 · VDD.

3.7.3.3 MP3 clock

One GPIO can be configured as a 2.4 MHz clock output to support MP3 in a low-power mode. This clock is a divided down version of the 19.2 MHz XO signal, so its most critical performance features are defined within the XO tables (Section 3.7.3.1). Output characteristics (voltage levels, drive strength, etc.) are defined in Section 3.4.

3.7.3.4 32 kHz oscillator

The following are three options for implementing the 32 kHz oscillator:

- Using the XO signal (19.2 MHz)
- An external 32.768 kHz crystal oscillator
- An external oscillator module

Whichever method is used, this oscillator signal is the primary sleep clock source. In all cases, neither the XTAL_32K_IN nor the XTAL_32K_OUT pins are capable of driving a load – the oscillator will be significantly disrupted if either pin is loaded.

The PMIC includes a circuit that continually monitors this oscillation. If the circuit is enabled but stops oscillating, the device automatically switches to the internal RC oscillator and generates an interrupt.

Performance specifications pertaining to the 32 kHz oscillator are listed in Table 3-42.

Table 3-42 Typical 32 kHz crystal specification

Parameter	Comments	Specification			Unit
		Min	Typ	Max	
Nominal oscillation frequency	F	–	32.768	–	kHz
Load capacitance	CL	7	–	12.5	pF
Frequency tolerance	ΔF/F	-100		100	ppm
Drive level	P	–	0.1	1	µW
Aging first year	ΔF/F	-3	–	3	ppm
Series resistance	Rs	–	50	80	kΩ
Motional capacitance	C1	–	2.1	–	fF
Static capacitance	C0	–	0.9	–	pF

3.7.3.5 RC oscillator

As mentioned in previous sections, the PMIC includes an on-chip RC oscillator that is used during startup and as a backup to the 32 kHz oscillator. Pertinent performance specifications are listed in Table 3-43.

Table 3-43 RC oscillator performance specifications

Parameter	Comments	Min	Typ	Max	Units
Oscillation frequency		14	19.2	24	MHz
Duty cycle		30	50	70	%
Divider in SLEEP_CLK path		–	586	–	–

3.7.3.6 Sleep clock

The sleep clock is generated one of three ways:

- Using the 19.2 MHz XO circuit and dividing its output by 586 to create a 32.7645 kHz signal – this method supports all normal operating modes.
- Using the 32.768 kHz crystal and supporting PMIC circuits – this method supports all normal operating modes.
- Using the on-chip 19.2 MHz RC oscillator and divide-by-586 to create a coarse 32 kHz signal – this method is only used during startup and if the 32.768 kHz XTAL source fails.

The PMIC sleep clock output is routed to the MSM or QSC device circuits using pin C15 (SLEEP_CLK0). It is also available for other applications via GPIO_38 and GPIO_39 (pins J5 and J4) when configured properly (as SLEEP_CLK1 and SLEEP_CLK2).

These clock outputs are derived from other sources specified earlier:

- 19.2 MHz XO circuits (Section 3.7.3.1)
- 32.768 kHz XTAL oscillator (Section 3.7.3.4)
- 19.2 MHz RC oscillator (Section 3.7.3.5)
- Output characteristics (voltage levels, drive strength, etc.) are defined in Section 3.4.

3.7.4 Realtime clock

The realtime clock functions are implemented by a 32-bit realtime counter and one 32-bit alarm, both configurable in one-second increments. The primary input to the RTC circuits is the 32.768 kHz clock from the XTAL oscillator. Even when the phone is off, the oscillator and RTC continue to run off the main battery.

NOTE The RTC function can be disabled using a one-time programmable (OTP) bit to save current while the PMIC is in its off state.

If the main battery is present and an SMPL event occurs, RTC contents are corrupted. As power is restored, the RTC pauses and skips a few seconds. The phone must reacquire system time from the network to resume the usual RTC accuracy. Similarly, if the main battery is not present and the voltage at VCOIN drops too low, RTC contents are again corrupted. In either case, the RTC reset interrupt is generated. A different interrupt is generated if the oscillator stops, also causing RTC errors.

The RTC is an entirely embedded function, without the external I/Os needing to be specified. All its controls and output data are accessed internally, and its accuracy depends entirely on the oscillator source being used – defined elsewhere. Therefore, no RTC performance parameters need to be defined here.

Table 3-44 shows RTC performance.

Table 3-44 RTC performance when using calRC, XO, and 32 kHz performance

Parameter	Comments/conditions	Specification			Unit
		Min	Typ	Max	
RTC tuning resolution	With known calibrated source	–	3.05	–	ppm
RTC tuning Range		-192	–	+192	ppm
RTC accuracy (off)	Using CalRC as RTC source with good phone battery	–	–	200	ppm
RTC accuracy (off)	Using CalRC as RTC source with qualified coincell only	–	–	200	ppm
RTC accuracy (phone off)	19.2 XO as RTC source	–	–	24	ppm
RTC accuracy (phone on)	19.2 XO as RTC source	–	–	24	ppm
RTC accuracy	32 kHz crystal over the phone off temperature range (-30°C to 60°C)	–	–	100	ppm
SMPL (XO)	With a 2.2 µF capacitor (0402 4.7 µF derated 1/2)	2	–	–	s
SMPL (RC)	With a 2.2 µF capacitor (0402 4.7 µF derated 1/2)	2	–	–	s

With the PM8921 CS, the target for RTC accuracy when running off calRC is 50 ppm.

3.7.5 Overtemperature protection (smart thermal control)

The PMIC includes overtemperature protection in stages, depending upon the level of urgency as the die temperature rises:

- Stage 0 – normal operating conditions (less than 105°C).
- Stage 1 – 105°C to 120°C; an interrupt is sent to the MSM or QSC device without shutting down any PMIC circuits.
- Stage 2 – 120°C to 140°C; an interrupt is sent to the MSM or QSC device and high-current drivers (backlight drivers, LED drivers, etc.) are shut down.
- Stage 3 – greater than 140°C; an interrupt is sent to the MSM or QSC device and the PMIC is completely shut down.

Temperature hysteresis is incorporated such that the die temperature must cool significantly before the device can be powered on again. If any start signals are present while at Stage 3, they are ignored until Stage 0 is reached. When the device cools enough to reach Stage 0 and a start signal is present, the PMIC will power up immediately.

3.8 User interfaces

In addition to housekeeping functions, the PMIC also includes these circuits in support of common handset-level user interfaces: an 8-channel light pulse generator; current drivers (and control signals for external current drivers); vibration motor driver; one-touch headset controls and microphone bias outputs; external switch detectors; an 8 × 8 keypad interface; enable; joystick interface.

All parameters associated with user interface functions are specified in the following subsections.

3.8.1 Light pulse generator

The PMIC includes a light pulse generator (LPG) circuit that can be used to control *fun* lights to flash multiple colors in a variety of patterns – from a constant torch mode to a user-programmed pattern. The pattern timing is generated by pulse-width modulator (PWM) circuits.

Since this function is entirely embedded within the PMIC, performance specifications are not appropriate. Instead, the *MSM8960 Chipset Training – PM8921 Power Management Training Topics* (80-N1622-25) provides descriptions of the available features – the number of independent patterns, the types of patterns available, PWM clock rates and resolutions, pattern synchronization, looping, and so on.

The LPG outputs can be used to control the on-chip current drivers, or to control external current drivers through up to three GPIOs (discussed in Section 3.8.2).

The LPG channels are assigned as follows:

Channel	Usage
1	GPIO24
2	GPIO25
3	GPIO26
4	KYPD_DRV
5	LED_DRV0
6	LED_DRV1
7	LED_DRV2
8	VIB_DRV_N

3.8.2 LPG controllers (digital driver outputs)

Up to three GPIOs can be configured as LPG controllers: pins D9 (GPIO_26 = LPG_DRV3), E8 (GPIO_25 = LPG_DRV2), and E7 (GPIO_24 = LPG_DRV1). Output characteristics (voltage levels, drive strength, etc.) were defined in Section 3.4.

The PWM frequency is

$$Fpwm = Fclk/((2^{PwmSize})*(2^{M})*PreDiv)$$

where

Fclk = 19.2 MHz, 32 kHz, or 1 kHz

PwmSize = 6 or 9

M = 0, 1,..., or 7

PreDiv = 2, 3, 5, or 6

The PWM duty cycle is (PWM value)/512 in 9-bit mode and (PWM value[5:0])/64 in 6-bit mode.

3.8.3 Current drivers

Three types of current drivers are available:

- A keypad driver that can operate off +5 V with programmable settings to 300 mA
- Three LED drivers to operate off V_{DD} with programmable settings to 40 mA
- One automatic trickle charging indicator that operates off V_{DD} at a fixed 5 mA

Current driver performance specifications are listed in Table 3-45.

Table 3-45 Current driver performance specifications

Parameter	Comments	Min	Typ	Max	Units
Common to all drivers					
Current accuracy	Any programmed value	-20	–	+20	%
Headroom [1]	Any programmed value	500	–	–	mV
Keypad driver					
Output current	Programmable in 20 mA increments	0	–	300	mA
Power supply voltage		–	5.00	5.25	V
Power supply current Normal operation Off, from supply voltage Off, at driver output pin	At max output current	 – – –	 200 1	 250 100	 µA nA nA
LED current drivers					
Output current	Programmable in 2 mA increments	0	–	40	mA
Power supply voltage		–	V_{DD}	–	V
Power supply current Normal operation Off, from supply voltage Off, at driver output pin		 –	 65 20 1	 80 100 50	 µA nA nA
ATC current driver (shared with LED_DRV0_N)					
Output current (fixed)		–	5	–	mA

Table 3-45 Current driver performance specifications (cont.)

Parameter	Comments	Min	Typ	Max	Units
Current accuracy	Any programmed value	-30	–	+30	%
Headroom [1]	Any programmed value	800	–	–	mV

1. Lowest output voltage while still meeting the current accuracy specification.

3.8.4 Vibration motor driver

The PMIC supports silent incoming call alarms with its vibration motor driver. The vibration driver is a programmable voltage output that is referenced to V_{DD}; when off, its output voltage is V_{DD}. The motor is connected between V_{DD} and the VIB_DRV_N pin.

Performance specifications for the vibration motor driver circuit are listed in Table 3-46.

Table 3-46 Vibration motor driver performance specifications

Parameter	Comments	Min	Typ	Max	Units
Output voltage (V_m) error [1] Relative error Absolute error	V_{DD} > 3.2 V; I_m = 0 to 175 mA; V_m setting = 1.2 to 3.1 V Total error = relative + absolute	 -6 -60	 – –	 +6 +60	 % mV
Headroom [2]	I_m = 175 mA	–	–	200	mV
Short circuit current	VIB_DRV_N = V_{DD}	225	–	600	mA

1. The vibration motor driver circuit is a low-side driver. The motor is connected directly to V_{DD}, and the voltage across the motor is $V_m = V_{DD} - V_{out}$, where V_{out} is the PMIC voltage at VIB_DRV_N.
2. Adjust the programmed voltage until the lowest motor voltage occurs while still meeting the voltage accuracy specification. This *lowest* motor voltage ($V_m = V_{DD} - V_{out}$) is the *headroom*.

3.8.5 One-touch headset control and MIC bias

The headset send/end detect (HSED) circuits communicate the wired headset's send/end button state to the MSM or QSC device through an interrupt. This design allows for simultaneous detection of both normally open (NO) and normally closed (NC) microphone switch types, or allows both a NO button press/release and a headset insertion/removal to be detected.

Three pins support this function: N9, N10, and N11 (HSED_BIAS1, HSED_BIAS2, and HSED_BIAS0). In addition to the detection capabilities, each pin also provides the bias voltage for a microphone.

Pertinent performance specifications are listed in Table 3-47.

Table 3-47 HSED and MIC bias performance specifications

Parameter	Comments	Min	Typ	Max	Units
HSED functions					
Detection accuracy, NO case		-10	–	+10	%
Detection accuracy, NC case		-20	–	+20	%

Table 3-47 HSED and MIC bias performance specifications (cont.)

Parameter	Comments	Min	Typ	Max	Units
MIC bias functions					
Output voltage	Power source is VREG_L5	–	1.8	–	V
Output voltage accuracy		-3	–	+3	%
Output current		20	–	1500	µA
Output load regulation at 600 µA vs. 20 µA load at 1.5 mA vs. 20 µA load	Voltage drop vs. load current	 – –	 – –	 20 50	 mV mV
Noise (227 µA load)	A-weighted; 0.1 µA load capacitor	–	–	8	µVrms
Load capacitor	Required external component	0.1	–	1.0	µF

3.8.6 External switch detection

Any unused or *floating* GPIO (designated as GPIO_XX in this document) can be configured as an external switch detector. This is essentially a Schmitt-triggered input with a selectable pull-up or pull-down. Input and output characteristics (voltage levels, drive strength, etc.) were defined in Section 3.4. There are no detector-specific performance specifications.

3.8.7 Keypad interface

GPIOs can be configured to implement a keypad interface supporting a matrix of up to 18 rows by 8 columns. Performance specifications that are specific to the keypad interface are listed in Table 3-48.

Table 3-48 Keypad interface performance specifications

Parameter	Comments	Min	Typ	Max	Units
Supply voltage		–	1.8	–	V
Load capacitance		5	10	15	pF
Sense lines					
Pull-up current		20.8	31.5	42.2	µA
Pull-down current		400	600	800	µA
Key-stuck delay	Number of 32 kHz cycles = 325,000	7.94	9.92	13.60	sec
Drive lines					
Drive strength	Open-drain outputs	–	0.6	–	mA

3.8.8 Joystick support

Joystick support requires four *floating* GPIOs (designated as GPIO_XX in this document) configured as digital outputs plus one MPP (MPP_05) configured as an analog input to the analog multiplexer. Pertinent performance specifications are available in the following sections:

- Digital I/O characteristics Section 3.4
- GPIO-specific characteristics Section 3.10
- Analog multiplexer and ADC Section 3.7.1 and Section 3.7.2
- MPP-specific characteristics Section 3.11

3.9 IC-level interfaces

The IC-level interfaces include poweron circuits; the SSBI; interrupt managers; UIM detection and level translators; UART multiplexing; and power amplifier controls. All parameters associated with these IC-level interface functions are specified in the following subsections. GPIO and MPP functions are also considered part of the IC-level interface functional block, but they are specified in their own sections (Section 3.10 and Section 3.11, respectively).

3.9.1 Poweron circuits and the power sequences

Dedicated circuits continuously monitor several events that might trigger a poweron sequence. If any of these events occur the PMIC circuits are powered on, the handset's available power sources are determined, the correct source is enabled, and the MSM or QSC device is taken out of reset.

Which regulators are included during the initial poweron sequence is determined by the hardware configuration controls (OPT_1, OPT_2, and OPT_3) as defined in Section 3.9.2. An example sequence is shown in Figure 3-7.

The inputs to the poweron circuits are basic digital control signals that must meet the input voltage level requirements stated in Table 3-4. The KPD_PWR_N and CBLPWRx_N inputs are pulled-up to an internal voltage. The external outputs (PON_RESET_N and EXT_SMPS_EN) must meet the output voltage level and current drive requirements stated in Table 3-4. Additional poweron circuit performance specifications are listed in Table 3-49. More complete definitions for time intervals included in Table 3-49 are provided in the *MSM8960 Chipset (RTR860X, PM8921, WCD9310, WCN3660) Schematics and Design Guidelines* (80-N1622-5).

Table 3-49 Poweron circuit performance specifications

Parameter	Comments	Min	Typ	Max	Units
Internal pull-up resistor [1]	At KPD_PWR_N and CBLPWRx_N pins	150	200	250	kΩ
KPDPWR_N pull up voltage		–	1.8	–	V
CBLPWR_N pull up voltage		–	0.8	–	V

Table 3-49 Poweron circuit performance specifications (cont.)

Parameter	Comments	Min	Typ	Max	Units
Sequence time intervals [2]					
t(reg1)	Poweron event to first regulator on [4]	–	6	10	ms
t(reg)	Time for reg to settle before next enable	100	128	500	µs
t(settle)	Regulator settling time [5]	20	–	500	µs
t(xo)	XO regulator enable to valid XO pulses	–	15	–	ms
t(reset1)	Last regulator on to PON_RESET_N = H	10	20	30	ms
t(pshold)	PS_HOLD timeout	133	200	300	ms
t(reset0)	PON_RESET_N = L to first regulator in group 0 off	6.7	10.0	15	ms
t(reg0)	Time between regulator shutdowns	0.6	1	1.4	ms
t(psholdoff)	Delay from PSHOLD dropping to PON_RESET_N dropping	–	60	90	µs
Regulator accuracy	To continue poweron sequence	4	7	9	%
Debounce timer [3]		16	–	10256	ms

1. This internal resistor is pulled up directly to an internal voltage net (dVdd).
2. All time intervals are derived from the divided-down XO clock source (32.7645 kHz typical); their tolerances are set accordingly. See Figure 3-7 for further discussion.
3. This is the delay between a triggering event (such as a keypad press) and the corresponding interrupt. The value is programmable.
4. The first regulator turn-on time **t**(reg1) depends on the bandgap reference decoupling capacitor at REF_BYP. The specified value is based on 0.1 µF. This time does not include the default 16 ms keypad debounce and the 16 ms UVLO debounce timers. If these debounce timers are increased, then the **t**(reg1) value will also increase.
5. Each regulator will settle to within its stated *regulator accuracy* within the stated *regulator settling time*. The regulators are turned on and off in the orders illustrated in Figure 3-7.

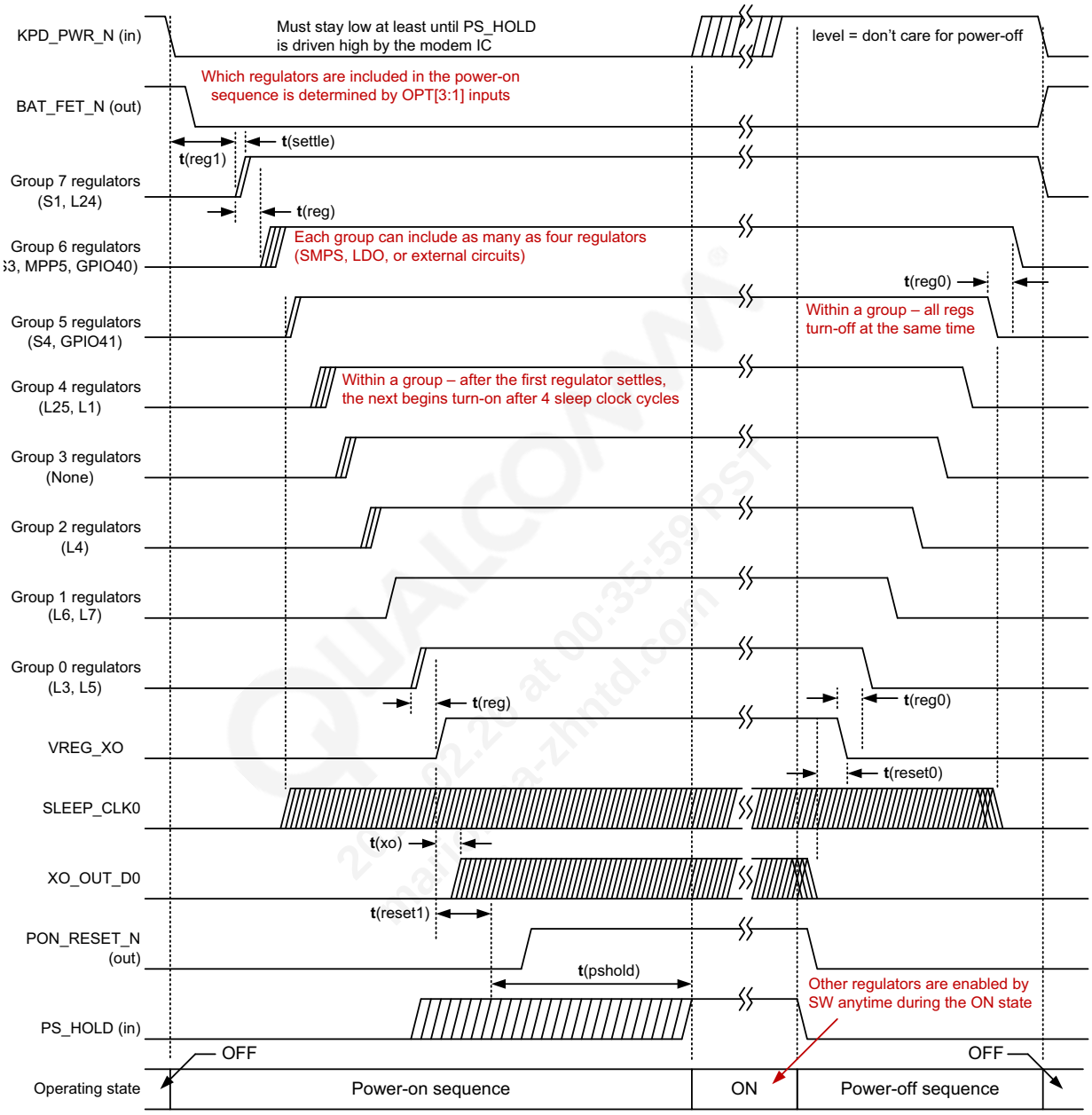


Figure 3-7 Example high-level power sequence timing diagram for PM8921 IC when paired with MSM8960 IC (OPT1 = VDD, OPT2 = Hi-Z, OPT3 = VDD)

3.9.2 SSBI and the interrupt managers

The SSBI is a bidirectional digital signal that meets the voltage and current level requirements stated in Table 3-4.

Three interrupt managers support modem, ADC, and USB functions, and report on numerous conditions, conveying realtime and latched status signals to the MSM or QSC device, thereby supporting the interrupt processing of those devices. The interrupt managers are mostly embedded functions; the three interrupt outputs meet the voltage and current level requirements stated in

Table 3-4. Most other control and status data are accessed via SSBI, supplemented by dedicated, realtime controls where needed.

3.9.3 UIM support

The PMIC includes level translators that enable an MSM or QSC device interface to the phone-level UIM/UICC connector. The three signals (data, clock, and reset) are routed using GPIOs and MPPs (Table 3-50).

Table 3-50 UIM signal paths

PM8291 IC pin	Function
GPIO27	UICC1_RESET_CONN
GPIO28	UICC2_RESET_CONN
GPIO29	UICC1_CLK_MSM
GPIO30	UICC1_CLK_CONN
GPIO31	UICC2_CLK_MSM
GPIO32	UICC2_CLK_CONN
GPIO36	UICC1_RMV_DET_N
GPIO37	UICC2_RMV_DET_N
MPP1	UICC1_DATA_MSM
MPP2	UICC1_DATA_CONN
MPP3	UICC2_DATA_MSM
MPP4	UICC2_DATA_CONN

All seven I/Os abide by the voltage and current specifications given in Table 3-4. Voltage translation options are listed within Table 2-1.

3.9.4 UART multiplexing

The PMIC includes two 3-to-1 multiplexers for routing three phone-level UART interfaces to a single MSM or QSC device interface; one multiplexer for the Rx path and one for the Tx path. The associated I/Os are implemented using GPIOs, and they abide by the voltage and current specifications given in Table 3-4.

Table 3-51 lists the UART functions of the PM8921 device pins.

Table 3-51 PM8921 UART functions

PM8921 device pin	Function
GPIO_21	UART_TX1
GPIO_22	UART_TX2
GPIO_23	UART_TX3
GPIO_33	UART_RX1
GPIO_34	UART_RX2
GPIO_35	UART_RX3

Table 3-51 PM8921 UART functions (cont.)

PM8921 device pin	Function
GPIO_08	UART_M_TX
GPIO_38	UART_M_RX

3.10 General-purpose input/output specifications

The 44 general-purpose input/output (GPIO) ports are digital I/Os that can be programmed for a variety of configurations (Table 3-52). Performance specifications for the different configurations are included in Table 3-4.

NOTE Unused GPIO pins should be configured as inputs with 10 µA pull-down.

Table 3-52 Programmable GPIO configurations

Configuration type	Configuration description
Input	1. No pull-up 2. Pull-up (1.5, 30, or 31.5 µA) 3. Pull-down (10 µA) 4. Keeper
Output	Open-drain or CMOS Inverted or non-inverted Programmable drive current; see Table 2-1 for options
Input/output pair	Requires two GPIOs. Input and output stages can use different power supplies, thereby implementing a level translator. See Table 2-1 for supply options.

Most GPIOs have a high-Z poweron default. Before they can be used for their desired purpose they need to be configured for use. Some GPIOs have non-high Z defaults in order to support certain poweron cases. These GPIOs can then only be used for their intended purpose (unless the alternate purpose can tolerate the poweron default conditions) and are described in Table 3-53.

Table 3-53 Special GPIO default state details

Pin name	Function name	GPIO feature	GPIO	GPIO/MPP poweron default
GPIO_40	External regulator 1	ER1	O	Logic output VIN0: VPH_PWR (~3.6 V) High drive highZ_en = 0
GPIO_41	External regulator 2	ER1	O	Logic output VIN2: S4 (1.8 V) High drive highZ_en = 0

Table 3-53 Special GPIO default state details (cont.)

Pin name	Function name	GPIO feature	GPIO	GPIO/MPP poweron default
GPIO_27	UICC1 reset	UICC1_RST	O	Logic output VIN0: VPH_PWR (~3.6 V) High drive highZ_en = 0
GPIO_28	UICC2 reset	UICC2_RST	O	Logic output VIN0: VPH_PWR (~3.6 V) High drive highZ_en = 0
GPIO_30	UICC1 clock	UICC1_CLK	O	Logic output VIN0: VPH_PWR (~3.6 V) High drive highZ_en = 0
GPIO_32	UICC2 clock	UICC2_CLK	O	Logic output VIN0: VPH_PWR (~3.6 V) High drive highZ_en = 0

GPIOs are designed to run at a 4 MHz rate to support UART applications. The supported rate depends upon the load capacitance and IR drop requirements. If the application specifies load capacitance (like UART applications), then the maximum rate is determined by the IR drop. If the application does not require a specific IR drop, then the maximum rate can be increased by increasing the supply voltage and adjusting the drive strength according to the actual load capacitance.

Table 3-54 lists output voltages for different driver strengths.

Table 3-54 VOL and VOH for different driver strengths

Supply voltage	VOL, VOH	Minimum load current		
		Low-strength driver	Medium-strength driver	High-strength driver
1.8 V	VOH = VDD - 0.3 V = 1.5 V	0.15 mA	0.6 mA	0.9 mA
	VOL = 0.3 V			
2.6 V	VOH = VDD - 0.45 V = 2.15 V	0.3 mA	1.25 mA	1.9 mA
	VOL = 0.45 V			
2.85 V	VOH = VDD - 0.4 V = 2.45 V	0.3 mA	1.1 mA	1.7 mA
	VOL = 0.4 V			
3.3 V	VOH = VDD - 0.45 V = 2.85 V	0.3 mA	1.4 mA	2.1 mA
	VOL = 0.45 V			

3.11 Multipurpose pin specifications

The PM8921 IC includes 12 multipurpose pins (MPPs), but they can be configured for any of the functions specified within Table 3-55.

All MPPs are high-Z (set as disabled current sinks) except MPP_02 and MPP_04, which are pulled low by default for use with UIM1 and UIM2. MPP_05 supplies 1.25 V from REF_BYP for the modem reference voltage.

Table 3-55 Multipurpose pin performance specifications

Parameter	Comments	Min	Typ	Max	Units
MPP configured as digital input [1]					
Logic high input voltage		$0.65 \cdot V_{YY1}$	–	–	V
Logic low input voltage		–	–	$0.35 \cdot V_{YY1}$	V
MPP configured as digital output [2]					
Logic high output voltage	$I_{out} = I_{OH}$	V_{YY2} - 0.45	–	V_{YY2}	V
Logic low output voltage	$I_{out} = I_{OL}$	0	–	0.45	V
MPP configured as bidirectional I/O [3]					
Nominal pull-up resistance	Programmable range [4]	1	–	30	kΩ
Maximum frequency		200	–	–	kHz
Switch on resistance		–	20	50	Ω
Power supply current		–	6	7	µA
MPP configured as analog input (analog multiplexer input)					
Input current		–	–	100	nA
Input capacitance		–	–	10	pF
MPP configured as analog output (buffered VREF output)					
Output voltage error	-50 µA to +50 µA	–	–	12.5	mV
Temperature variation	Due to buffer only; does not include VREF variation (see Table 3-21)	-0.03	–	+0.03	%
Load capacitance		–	–	25	pF
Power supply current		–	0.17	0.20	mA
MPP configured as level translator					
Maximum frequency		4	–	–	MHz

1. V_{YY1} is the programmable supply voltage from which digital input thresholds are referenced; options are listed in Table 2-1. Other specifications are included in Table 3-4.
2. V_{YY2} is the programmable supply voltage from which digital output thresholds are referenced; options are listed in Table 2-1. Other specifications are included in Table 3-4. The input and output supply voltages can be different.
3. MPP pairs are listed in Table 3-56.
4. Pull-up resistance is programmable to values of 1 k, 10 k, 30 k, or open.

Table 3-56 MPP pairs

MPP #	Pin #		MPP #	Pin #
1	D13	<–>	2	E13
3	F13	<–>	4	D14
5	E14	<–>	6	F14
7	R14	<–>	8	P13
9	P14	<–>	10	R15
11	P15	<–>	12	N15

In addition, there are four analog input only pins (AMUX1 through AMUX4) that can be used for purposes such as PA_THERM, BATT_ID, BATT_THERM, and HW_ID.

4 Mechanical Information

The PM8921 IC mechanical specifications are presented in this chapter, including physical dimensions, visible markings, ordering information, moisture sensitivity level, and thermal characteristics. Additional details pertaining to these topics are included in the *BGA Package User Guide* (80-V2560-1), available for download at https://support.cdmatech.com (CDMATech Support Website).

4.1 Device physical dimensions

The PM8921 IC is available in the 251-pin nanoscale package (251 NSP) that includes dedicated ground pins for improved grounding, mechanical strength, and thermal continuity. The 251 NSP package has a 7.8 mm by 7.8 mm body with a maximum height of 0.88 mm. Pin A1 is located by an indicator mark on the top of the package and by the ball pattern when viewed from below.

Click the link below to download the 251 NSP outline drawing (NT90-N2703-1) from the CDMA Tech Support website.

- https://downloads.cdmatech.com/qdc/drl/objectId/09010014814f1f50

Clicking the link above will take you directly to the CDMA Tech Support website (https://support.cdmatech.com), prompting a document download for that specific drawing (assuming you have permission to view it).

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4.2 Device marking

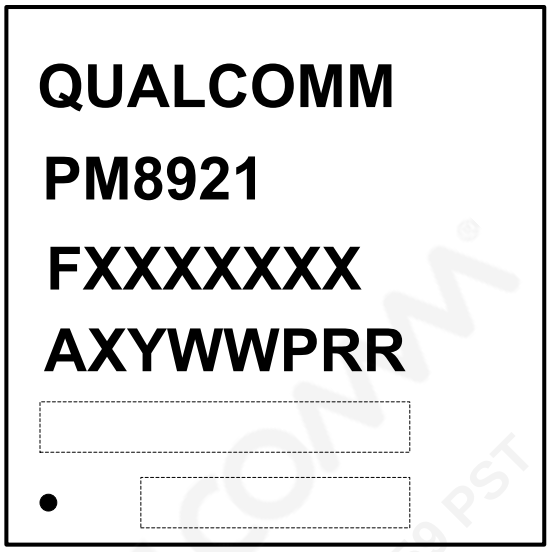

Figure 4-1 PM8921 device marking (top view – not to scale)

Table 4-1 Part marking line descriptions

Line	Marking	Description
1	QUALCOMM	Qualcomm name or logo
2	PM8921	Qualcomm product name
3	FXXXXXXX	F = supply source code ■ F = A (SMIC, Fab1, China) ■ F = B (GF, Fab 3, Singapore) XXXXXXX = traceability number
4	AXYWWPRR	A = assembly site code ■ A = F (ASE, South Korea) ■ A = U (Amkor, Shanghai) ■ A= V (STATSChipPAC, Shanghai) X = traceability number Y = single-digit year code WW = work week (based on calendar year) P = product configuration code (see Table 4-2) RR = product revision (see Table 4-2)
Additional lines may appear on the part marking for some samples; this is manufacturing information that is only relevant to Qualcomm and Qualcomm suppliers.		

NOTE For complete marking definitions of all PM8921 IC revisions, refer to the *PM8921 Power Management IC Device Revision Guide* (80-N1060-4).

4.3 Device ordering information

This device can be ordered using the identification code, shown in Figure 4-2 and explained in this section.

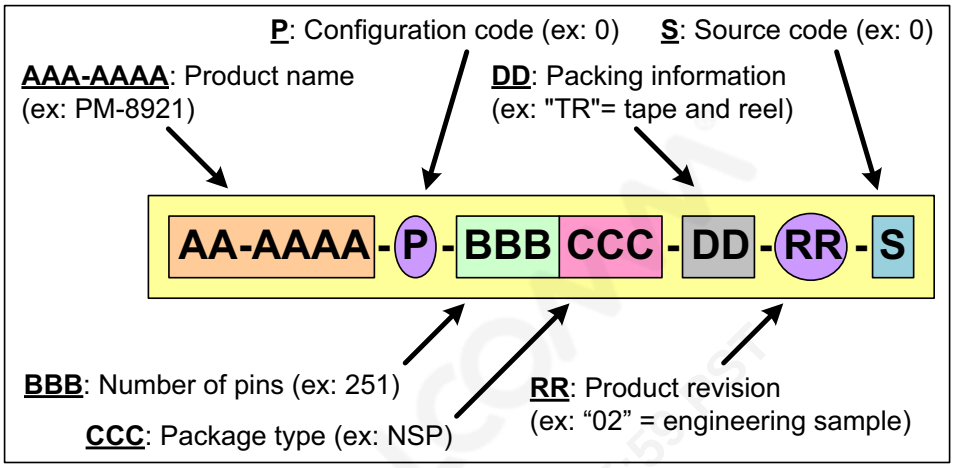

Figure 4-2 Device identification code

An example can be as follows: PM-8921-0-251NSP-TR-02-0.

Device ordering information details for all samples available to date are summarized in Table 4-2.

Table 4-2 Device identification code/ordering information details

PM8921 variant	Product configuration code (*P*)	Product revision (*RR*)	Sample type	Known issues
PM8921	0	02	ES	See Chapter 3 of the *PM8921 Power Management IC Device Revision Guide* (80-N4420-4).
	0	03	ES2	

Table 4-3 Source configuration code

S value	F value = A	F value = B	F value = C
0	TBD	TBD	TBD

4.4 Device moisture-sensitivity level

Plastic-encapsulated surface mount packages are susceptible to damage induced by absorbed moisture and high temperature. Qualcomm follows the latest IPC/JEDEC J-STD-020 standard revision for moisture-sensitivity qualification. ***The PM8921 devices are classified as MSL3 at TBD°C.*** This is the MSL classification temperature, which is defined as the minimum temperature of moisture sensitivity testing during device qualification.

Additional MSL information is included in:

- Section 5.2 – Storage
- Section 5.3 – Handling
- Section 7.1 – Reliability qualifications summary
- *IC Packing Methods and Materials Specification* (80-VK055-1)

4.5 Thermal characteristics

The PM8921 device in its 251 NSP package has typical thermal resistances as listed in Table 4-4.

Table 4-4 Device thermal resistance

Parameter		Comments	Typ	Units
θ_{JA}	Thermal resistance, J-to-A	Junction-to-ambient (still air)[1]	TBD	°C/W
θ_{JC}	Thermal resistance, J-to-C	Junction-to-case[2]	TBD	°C/W

1. Junction-to-ambient thermal resistance (θ_{JA}) is calculated based upon the maximum die junction temperature and the total package power dissipation; ambient temperature is 85°C.
2. Junction-to-case thermal resistance (θ_{JC}) applies to situations in which nearly all the heat flows out the top of the package.

5 Shipping, Storage, and Handling

Information about shipping, storing, and handling the PM8921 IC is presented in this chapter. Additional details are available in the *BGA Package User Guide* (80-V2560-1) that can be downloaded from the CDMATech Support Website (https://support.cdmatech.com).

5.1 Shipping

5.1.1 Tape and reel information

The single-feed tape carrier for the PM8921 device is illustrated in Figure 5-1; this figure also shows the proper part orientation. The tape width is 16 mm and the parts are placed on the tape with a 12 mm pitch. The reels are 330.2 mm in diameter with 102 mm hubs. Each reel can contain up to 4000 devices.

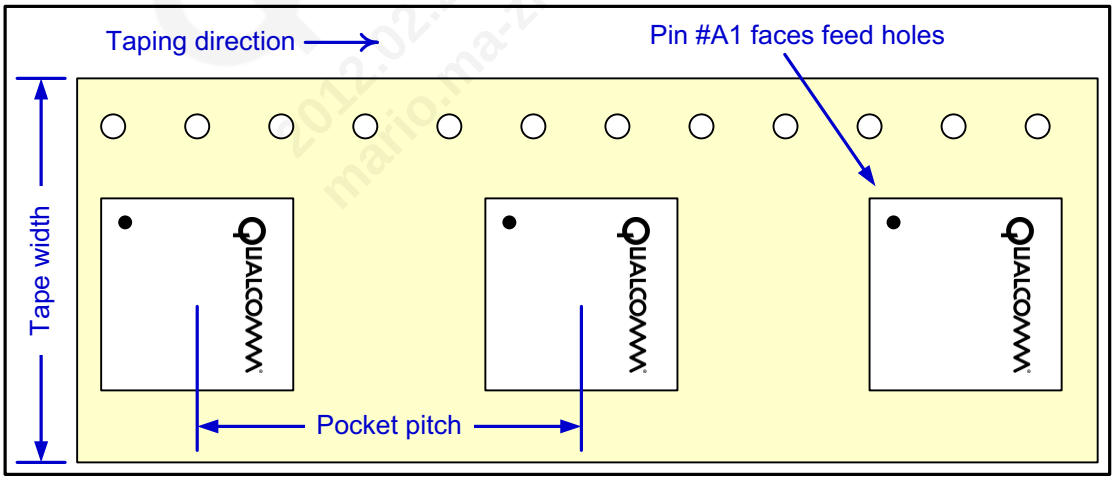

Figure 5-1 Carrier tape drawing with part orientation

The carrier tape and reel features are based upon the EIA-481 standard.

Tape-handling recommendations are shown in Figure 5-2.

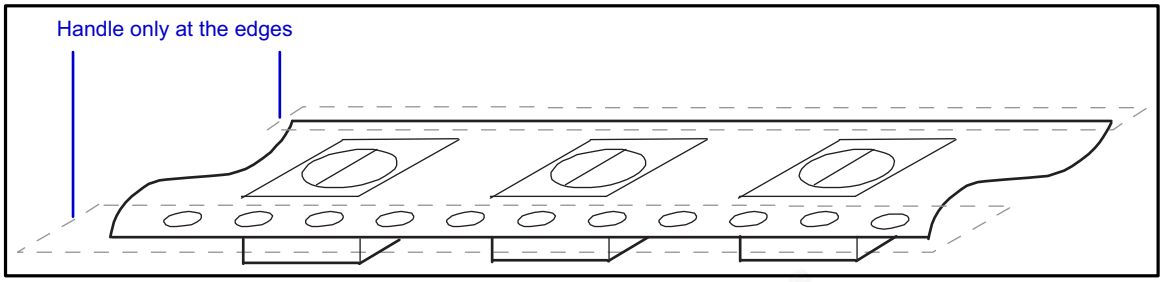

Figure 5-2 Tape handling

5.1.2 Packing for shipment (including barcode label)

Refer to the *IC Packing Methods and Materials Specification* (80-VK055-1) for all packing-related information, including barcode label details.

5.2 Storage

5.2.1 Storage conditions

The PM8921 devices, as delivered in tape and reel carriers, must be stored in sealed, moisture barrier, anti-static bags. The Qualcomm-calculated shelf life in a sealed moisture bag is 60 months; this value requires an ambient temperature less than 40°C and relative humidity less than 90%.

5.2.2 Out-of-bag duration

The PM8921 device must be soldered to a PCB within its factory floor life of ***one week*** after opening the moisture barrier bag (MBB).

NOTE The factory must provide an ambient temperature less than 30°C and relative humidity less than 60%, as specified in the IPC/JEDEC J-STD-033 standard.

5.3 Handling

Tape handling was discussed in Section 5.1.1. Other handling guidelines are presented below.

5.3.1 Baking

It is **not necessary** to bake the PM8921 devices if the conditions specified in Section 5.2.1 and Section 5.2.2 have **not been exceeded**.

It is **necessary** to bake the PM8921 devices if any condition specified in Section 5.2.1 or Section 5.2.2 has **been exceeded**. The baking conditions are specified on the moisture-sensitive caution label attached to each bag; refer to the *IC Packing Methods and Materials Specification* (80-VK055-1) for details.

CAUTION If baking is required, the devices must be transferred into trays that can be baked to at least 125°C. Devices should not be baked in tape and reel carriers at any temperature.

5.3.2 Electrostatic discharge

Electrostatic discharge (ESD) occurs naturally in laboratory and factory environments. An established high-voltage potential is always at risk of discharging to a lower potential. If this discharge path is through a semiconductor device, destructive damage may result.

ESD countermeasures and handling methods must be developed and used to control the factory environment at each manufacturing site.

Qualcomm products must be handled according to the ESD Association standard: ANSI/ESD S20.20-1999, *Protection of Electrical and Electronic Parts, Assemblies, and Equipment*.

Refer to Chapter 7 for the PM8921 device ESD ratings.

6 PCB Mounting Guidelines

Guidelines for mounting the PM8921 device onto a printed circuit board (PCB) are presented in this chapter, including land pad and stencil design details, surface mount technology (SMT) process characterization, and SMT process verification. Additional details are available in the *BGA Package User Guide* (80-V2560-1), which can be downloaded from the CDMATech Support Website (https://support.cdmatech.com).

The PM8921 device is internally and externally lead-free and RoHS-compliant. Its SnAgCu solder balls use SAC125Ni composition.

NOTE Qualcomm defines its lead-free (or Pb-free) semiconductor products as having a maximum lead concentration of 1000 ppm (0.1% by weight) in raw (homogeneous) materials and end products. Qualcomm package environmental programs, RoHS compliance details, and tables defining pertinent characteristics of all Qualcomm IC products are discussed in the *IC Package Environmental Roadmap* (80-V6921-1).

6.1 Land pattern, stencil design, and daisy-chain interconnect drawings

The land pattern and stencil recommendations presented in this section are based upon Qualcomm internal characterizations for SnPb and lead-free solder pastes on a four-layer test PCB and a 127 micron-thick stencil. The PCB land pattern and stencil design for the 251 NSP are the same whether SnPb or lead-free solder is used.

Click the links below to download the 251 NSP land/stencil drawing (LS90-N2703-1) and daisy-chain interconnect drawing (DS90-N2703-1) from the CDMA Tech Support website.

- Land pattern and stencil design – https://downloads.cdmatech.com/qdc/drl/objectId/09010014814e39ef
- Daisy-chain interconnect – https://downloads.cdmatech.com/qdc/drl/objectId/09010014814e3809

Clicking the links above will take you directly to the CDMA Tech Support website (https://support.cdmatech.com), prompting a document download for the drawings (assuming you have permission to view them).

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6.2 SMT development and characterization

The information presented in this section describes Qualcomm board-level characterization process parameters. It is included to assist customers when starting their SMT process development; it is not intended to be a specification for customer SMT processes.

NOTE Qualcomm recommends that customers follow their solder paste vendor recommendations for the screen-printing process parameters and reflow profile conditions.

Qualcomm characterization tests attempt to optimize the SMT process for the best board-level reliability possible. This is done by performing physical tests on evaluation boards, which may include:

- Peel test
- Bend-to-failure
- Bend cycle
- Tensile pull
- Drop shock
- Temperature cycling

Qualcomm recommends characterizing the land patterns according to each customer's processes, materials, equipment, stencil design, and reflow profile ***prior to PCB production***. Review the land pattern and stencil pattern design recommendations in Section 6.1 as a guide for characterization.

Optimizing the solder stencil pattern design and print process is critical to ensure print uniformity, decrease voiding, and increase board-level reliability.

Daisy-chain packages are suitable and available for SMT characterization; ordering information is included in the *BGA Package User Guide* (80-V2560-1).

Reflow profile conditions typically used by Qualcomm for SnPb and lead-free systems are given in Table 6-1.

Table 6-1 Qualcomm typical SMT reflow profile conditions (for reference only)

Profile stage	Description	SnPb (standard) condition limits	Lead-free (high-temp) condition limits
Preheat	Initial ramp	3°C/sec max	3°C/sec max
Soak	Dry out and flux activation	135 to 165°C 60 to 120 sec	135 to 175°C 60 to 120 sec
Reflow	Time above solder paste melting point	30 to 90 sec	40 to 90 sec
	SMT peak package body temperature	230°C	245°C
Cool down	Cool rate – ramp-to-ambient	6°C/sec max	6°C/sec max

6.3 SMT peak package body temperature

Qualcomm recommends the following limits during the SMT board-level solder attach process:

- SMT peak package body temperature of 250°C – the temperature that should not be exceeded as measured on the package body's top surface
- Maximum duration of 40 seconds at this temperature

Although the solder paste manufacturers' recommendations for optimum temperature and duration for solder reflow should be followed, the Qualcomm-recommended limits must not be exceeded.

6.4 SMT process verification

Qualcomm recommends verification of the SMT process prior to high-volume PCB fabrication, including:

- Electrical continuity
- X-ray inspection of the package installation for proper alignment, solder voids, solder balls, and solder bridging
- Visual inspection
- Cross-section inspection of solder joints to confirm registration, fillet shape, and print volume (insufficient, acceptable, or excessive)

7 Part Reliability

7.1 Reliability qualification summary

Table 7-1 PM8921 IC reliability evaluation

Tests, standards, and conditions	Sample size	Results
Average failure rate (AFR) in FIT (λ) failure in billion device-hours **HTOL:** JESD22-A108-C	TBD	TBD
Mean time to failure (MTTF) t = 1/λ in million hours	TBD	TBD
ESD – human-body model (HBM) rating JESD22-A114-E	TBD	TBD
ESD – charge-device model (CDM) rating JESD22-C101-C	TBD	TBD
Latch-up: EIA/JESD78A Temperature = 85°C	TBD	TBD
Moisture resistance test (MRT): J-STD-020-C Reflow at 260 +0/-5°C, MSL = 3	TBD	TBD
Temperature cycle: JESD22-A104-C, Cond. B, 1000 cycles **Preconditioning:** JESD22-A113-E	TBD	TBD
Un-biased highly accelerated stress test (HAST) JESD22-A118; time = 96 hrs **Preconditioning:** JESD22-A113-E	TBD	TBD
High-temperature storage life: JESD22-A103-C Temperature = 150°C; time = 1000 hrs	TBD	TBD
Flammability UL-STD-94 (by mold-compound certification)	TBD	TBD
Physical dimensions JESD22-B100-B	TBD	TBD
Solder ball shear JESD22-B117A	TBD	TBD

7.2 Qualification sample description

Device characteristics:

Device name:	PM8921
Package type:	251 NSP
Package body size:	7.8 mm × 7.8 mm × 0.88 mm
Lead count:	251
Lead composition:	TBD
Processes:	0.18 μ CMOS
Fab sites:	TBD
Assembly sites:	TBD
Solder ball pitch:	0.4 mm