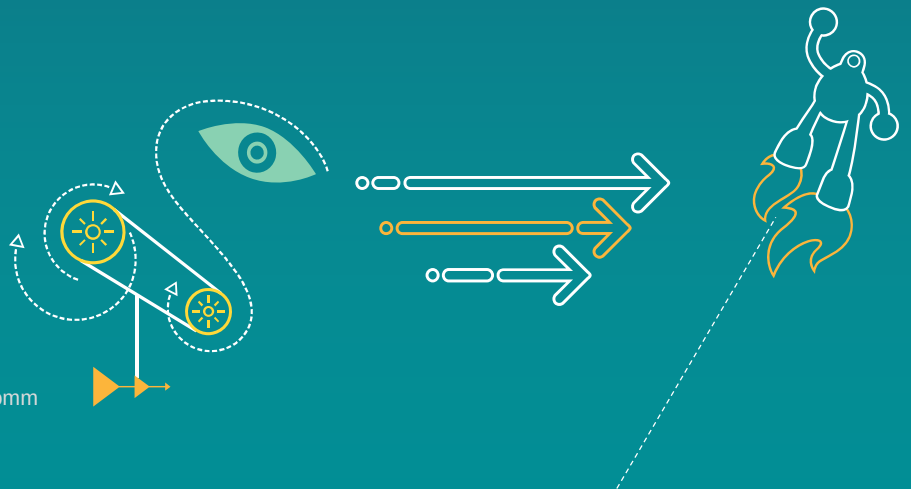
System Power Monitor Version 4 Overview (SPMv4)

Qualcomm Technologies, Inc.



80-N6594-20 Rev. C

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Revision History

Revision	Date	Description
A	April 2014	Initial release
B	April 2014	Page 1 – Updated document title Page 12 – Updated ordering information
C	November 2014	Updated document title from Introduction To System Power Monitor Version 4 to System Power Monitor Version 4 Overview (SPMv4) Page 4 – Clarified the tool usage Page 5 – Updated ordering information Page 6 – Removed some text and magnified the SPMv4 diagram for clarity Page 7 – Added a new slide on SPMv4 Hardware (~75 mm × 35 mm) Page 8 – Updated voltage channel limitations, eight channel bandwidth per channel value for SPMv4, and removed a footnote from single, two, and eight channel bandwidth per channel Page 9 and 10 – Clarified a few important things about the sense resistors Page 12 – Added a new slide on QEPM

What is the System Power Monitoring (SPM) Tool?

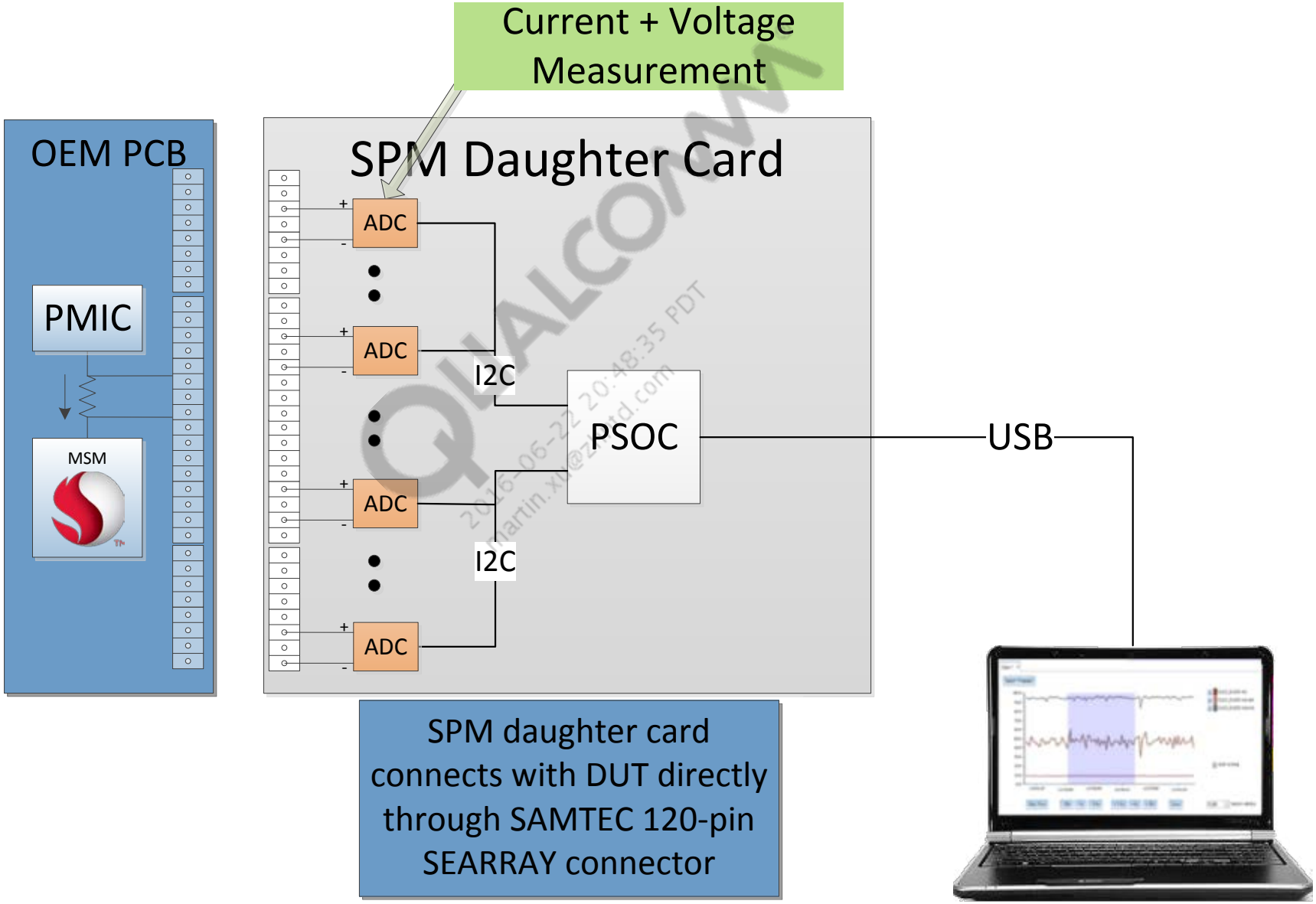
A tool that enables power rail breakdown measurements to enhance debugging efficiencies of power issues. The hardware and software are developed by Qualcomm®. The customer should consider designing bigger power board for use with SPM to avoid potential PDN issues in their product

- Measures voltage and current vs. time for each rail
- Compares relative power between software builds for each rail
- Measures absolute power on each rail including the battery level
  - Supports ±2% accuracy for most use-cases. ±6% accuracy for Rock Bottom Sleep Current (RBSC)
- Verifies the MSM™ chipset power specifications (maximum Dhrystone power and maximum sleep current)
  - See MSM Device Specification section 3.4.x
  - Associated Dhrystone power scripts are located in the MSM folder
- Requires series resistors designed and installed into the power rails of the PCB
  - PMIC SMPS → Inductor → SPM Series Resistor → SMPS Sense Feedback Point → MSM
  - Resistor requirements in: *System Power Monitor Version 4 Application Note* (80-N6594-16)
- Utilizes a power debug connector designed into the PCB
  - Enables monitoring of 48 rails simultaneously and voltages up to 28 V. See *System Power Monitor Version 4 Application Note* (80-N6594-16) for more details.
- QEPM
  - Power monitoring software that takes the SPM inputs and displays it on the PC in an easy to read manner with a lot of data

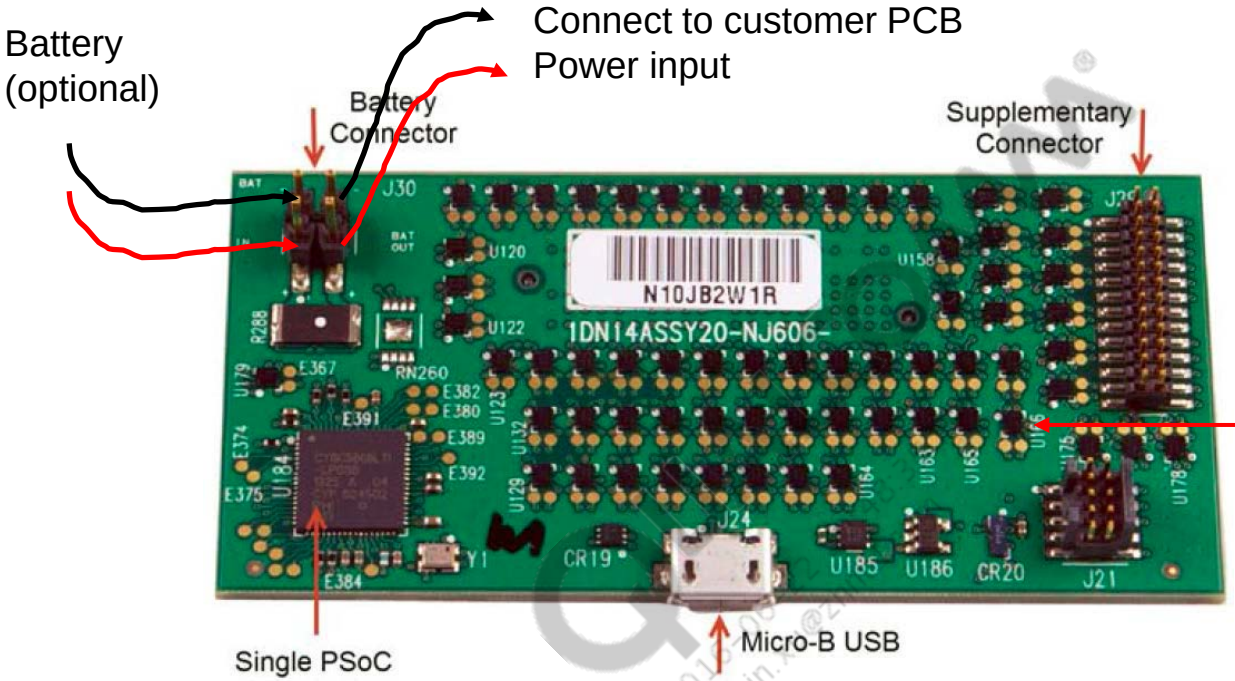
Ordering SPMv4

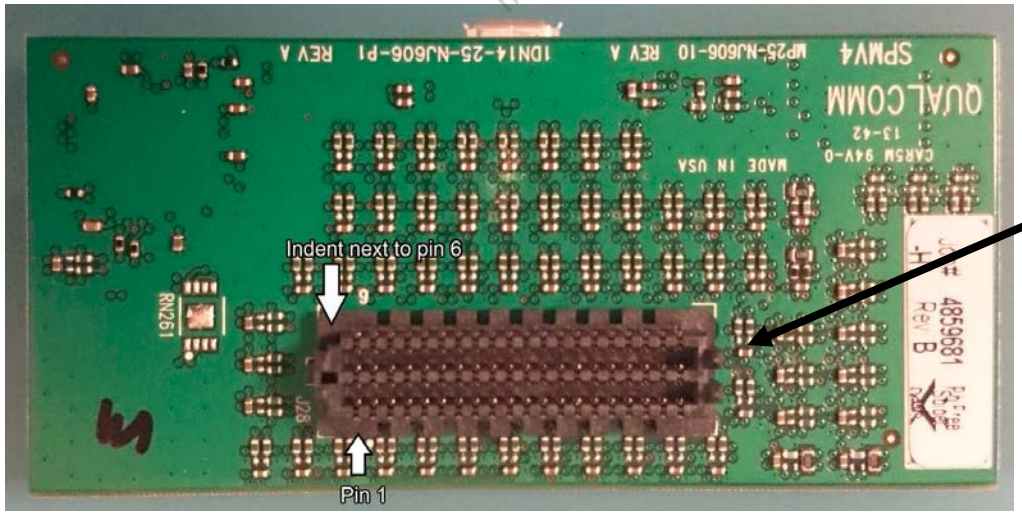
- Hardware: https://cp.qti.qualcomm.com. Under the SPM tab. Part number = 30-NJ606-1 ($500*)
- SPMv4 with MTP interposer (to measure rails on MTPs). Package number = 65-NJ606-1 ($600*)
- Software: Request “QEPM Software” via Sales Force Case. Download *Qualcomm Embedded Power Monitor Version 5 User Guide* (80-NH746-1).
  - Record type of new record = Wireless device support
  - Initial problem type = Software
  - Problem area 1 = BSP/HLOS
  - Problem area 2 = Power/thermal (BSP/HLOS)
  - Problem area 3 = Power-idle power

*Prices are subject to change in the future.



SPMv4 Hardware (~75 mm × 35 mm)





SPM Comparisons at Room Temperature

	SPMv4	SPMv3
Current measurement channels	48	48
Voltage measurement channels	48	14
Voltage channel limitations	No	Yes
Dynamic current range	±8 A on 10 mΩ sense resistor [1]	2 A on 10 mΩ sense resistor
Dynamic voltage range	28 V	+2 V
RBSC accuracy	±6%	±20%
Normal operating accuracy	±2% [2]	±2% [2]
Single channel bandwidth	7 kSps	10 kSps
Two channel bandwidth per channel	7 kSps	10/5 kSps [3]
Eight channel bandwidth per channel	7 kSps (best case) 1.75 kSps (worst case)	2/1.25 kSps [3]
Board connector	Same as SPMv3	120 pin Samtech
Power supply	Micro-USB	Micro-USB
Firmware updater	Yes	No
Configuration channel	GUI	XML
MTP support [4]	Yes	No

[1] 80 mV may exceed maximum rail IR drop.
[2] This is dependent on following proper design rules; low bandwidth measurement.
[3] Each PSOC is limited to 10 kSps, so it is dependent on setup.
[4] A required interposer board comes with the SPMv4 package. Works on RCM-enabled MTPs only (starting with MSM8994, MDM9x30/MDM9x35M, and APQ8084)

Designing an SPM-ready Board (1 of 3)

These are a subset of rules needed for maximum accuracy. Please see the *System Power Monitor Version 4 Application Note* (80-N6594-16) for the full list.

Op-amp polarity

- The PMIC side of any op-amp input should be connected to the positive side of the op-amp. If the reverse happens, a negative current value will be read.

Sense resistors

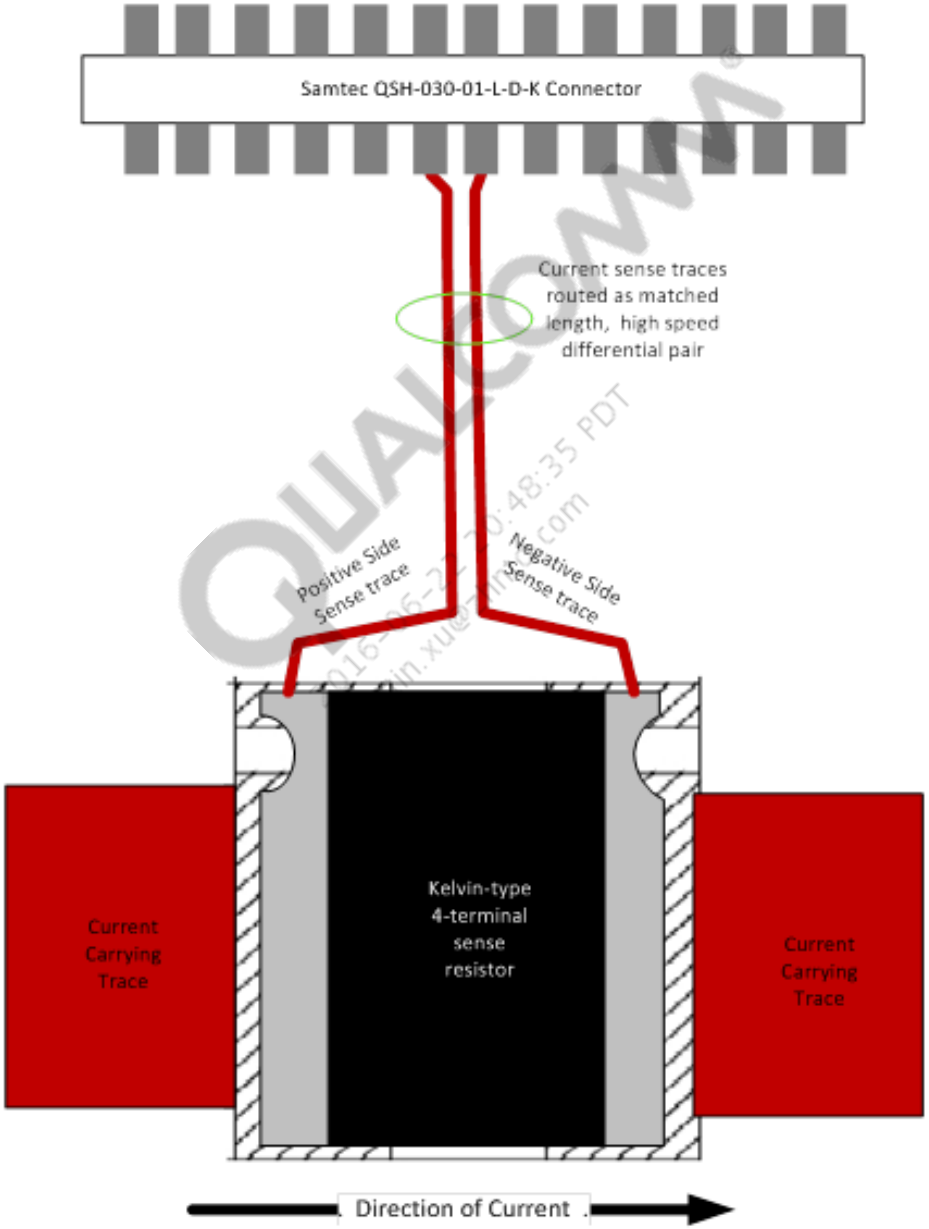
- Selection, placement, and routing of the PDN to the SPM sense resistors is the most important part of the customer power measurement circuitry.
- Use resistors with ±1% (or better) tolerance: Since QEPM uses the optimal resistor value input into the configuration file, mismatched resistance will add more errors. If a resistor is 10% off from the nominal, the current readings maximum error will increase 10x.
- Sense traces must be connected as close to the resistor as possible (with a Kelvin connection).
- Sense resistors affect the PDN of the power rails: Resistors on a Krait™ power path need to have a higher current rating. Ensure that power rails with larger currents have an appropriate number of vias on each side of the sense resistors to avoid violating the PDN DC specifications or thermal damage.
- For rails driven by a switching power supply, place sense resistors between the inductors and the SMPS sense-line used for feedback.
- Recommended resistor values and power ratings are listed in *System Power Monitor Version 4 Application Note* (80-N6594-16).

Designing an SPM-ready Board (2 of 3)

Op-amp traces:

- Power sense traces routed from each SPM sense resistors to the customer SPM power connector **must** be routed as a differential pair, ensuring equal coupling of any noise. Since the voltage drop across the sense resistors can sometimes be smaller than 1 mV, noise coupling onto only one of the traces would impact the accuracy (+1 mv induced onto the + only side would create 100% error). To minimize this, these two traces should run as close together as possible all the way from the sense resistor up to the Samtech connector. Noise coupled onto one line must be the same on the second line to be effectively be ignored.
- Power sense traces should connect as close to the SPM sense resistor as possible.

Designing an SPM-ready Board (3 of 3)



QEPM

- Easy to use and visually pleasing interface
- High speed collection of multiple power rails
  - 48 I and V + customs on SPMv4
  - Software combines up to six SPM devices
- Multiple collection methods:
  - Real-time
  - Post-process
  - Automation
  - Raw data, minimum, maximum (Fetcher)
- Correlation with Snapdragon™ performance visualizer data
- See *Qualcomm Embedded Power Monitor Version 5 User Guide* (80-NH746-1) for more information

Questions?

You may also submit questions to:
https://support.cdmatech.com