电子学基础——第九次作业

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10.51 A student who has a single-ended voltage source constructs the circuit shown in Fig. 10-75, hoping to obtain differential outputs. Assume perfect symmetry but $\lambda = 0$ for simplicity.

(b) Viewing M_1 as a common-source stage degenerated by the impedance seen at the source of M_2, calculate v_X in terms of v_{in}.

(b) Viewing M_1 as a source follower and M_2 as a common-gate stage, calculate v_Y in terms of v_{in}.

(c) Add the results obtained in (a) and (b) with proper polarities. If the voltage gain is defined as $(v_X - v_Y)/v_{in}$, how does it compare with the gain of differentially driven pairs?

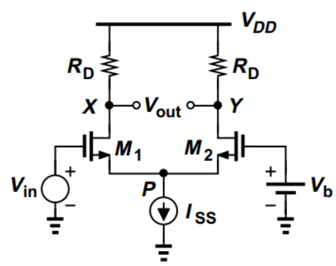

Figure 10-75

解 (a) M_2从源端看入，输入电阻为$\frac{1}{g_{m2}}$，而M_1为源简并放大器。则

$$\frac{v_X}{v_{in}} = -\frac{g_{m1}R_D}{1 + g_{m1} \cdot \frac{1}{g_{m2}}} = -\frac{g_m R_D}{2}$$

(b) M_1为源极跟随器，则M_1源端电压即为$v_{s1} = v_{in}$，而M_2为共栅放大器，则

$$\frac{v_Y}{v_{s1}} = g_{m1}R_D$$

$$\therefore \frac{v_Y}{v_{in}} = g_{m1}R_D$$

(c)

$$\frac{v_X - v_Y}{v_{in}} = -\frac{3}{2}g_m R_D$$

这个增益是普通差分放大器增益的1.5倍。

10.70 Compute the common-mode rejection ratio of the stages illustrated in Fig. 10-89 and compare the results. For simplicity, neglect channel-length modulation in M_1 and M_2 but not in other transistors.

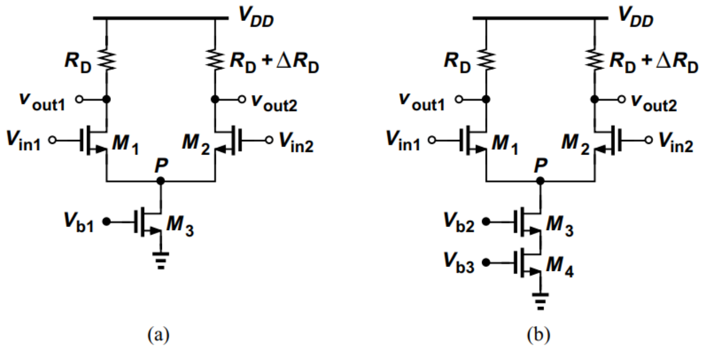

Figure 10-89

解

$$\mathrm{CMRR}=20\log\left|\frac{A_{vd}}{A_{vc}}\right|$$

(a) 电路对称，可考虑半边电路。由交流小信号电路中P为虚地，则

$$A_{vd}=-g_{m1}R_D$$

考虑A_{vc}时，可将M_3视为r_{o3}，进而再半边电路中视为$2r_{o3}$，则M_1为源简并放大器：

$$A_{vc}=\frac{-g_{m1}R_D}{1+2g_{m1}r_{o3}}$$

则

$$\mathrm{CMRR}=20\log(1+2g_{m1}r_{o3})$$

(b) 同(a)，P再交流小信号电路中仍未虚地，则

$$A_{vd}=-g_{m1}R_d$$

再考虑A_{vc}，将M_4视为r_{o4}，则M_3为源简并放大器，可视为电阻$r=(1+g_{m3}r_{o3})r_{o4}+r_{o3}$ 从而半边电路中可将其视为$2r=2[(1+g_{m3}r_{o3})r_{o4}+r_{o3}]$ 此时M_1仍为源简并放大器：

$$\therefore A_{vc}=\frac{-g_{m1}R_D}{1+2g_{m1}[(1+g_{m3}r_{o3})r_{o4}+r_{o3}]}$$

$$\therefore \mathrm{CMRR}=20\log[1+2g_{m1}((1+g_{m3}r_{o3})r_{o4}+r_{o3})]$$