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 $\label{eq:nctuser} NCTUser \mbox{$(/s/profile/0050X0000089Rd|QAU)$ (Community Member) asked a question.} \\ \underline{May 27. 2019 at 6:52 AM \mbox{$(/s/question/0D50X0000At02zOSQO/stm32-general-purpose-timer-update-event-and-glitch-problem)} \\ \\$

STM32 General Purpose Timer Update Event and glitch problem

I use STM32F102 and TIM2 timer in PWM1 mode to generate defined frequency and duty cycle square wave. I have some questions and I hope can get some help from experienced colleagues.

1. I update the ARR/CCR1 register in an interrput which is defined by the communication cycle and independent form timer frequency, which means I write the ARR/CCR1 asynchronusly form Timer Update Event. I was afraid that the update event happens between the writing of ACC and CCR1 and the content of two registers became inconsistent. But if I disable the update event I got a missing pulse. How can I use the Timer to have always consistent ARR/CCR1 pairs and no missing pulses?

TIM2->EGR &= ~TIM_EGR_UG;

/* ... */
TiM2->ARR = periodCh1; // If the UpdateEvent happens here the pulse is missing!
TIM2->CCR1 = pulseCh1;
/* ... */
TiM2->EGR |= TIM_EGR_UG;

2. If the ARR and CCR1 registers are equal (which means for me the 100% duty cycle) I expected constant level on the timer output, but I noticed there is a one timer clock long glitch on the output (one glitch per update event).

Is it the normal behavior? Should I manually force the output in constant state in this situation?

3. How can I force the output of the compare module in known state? The best way to change the Output compare 1 mode (OC1M) to forced mode or should I configure the pin back to GPIO output?

Thank you.

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waclawek.jan (/s/profile/0050X000007vqmpQAA) (Community Member)

Edited May 27, 2019 at 7:20 AM 1.

> TIM2->EGR &= ~TIM_EGR_UG; This does nothing, and > TIM2->EGR |= TIM_EGR_UG; this forces an update event.

You can't stop the update event generation. TIM_EGR.UG *generates* an update event, even if the counter is not matching ARR. You could stop the counter itself (possibly while disabling higher priority interrupts), if a small change in period is not an issue.

C. CCR1 = 0 means no pulse, CCR1 = 1 means pulse 1 cycle long, CCR1 = 2 means pulse 2 cycle long, ..., CCR1 = ARR means pulse ARR cycle long - but the period is ARR+1, so to achieve 100% you have to set CCR1 = ARR + 1 (or higher).

3. Both methods work and it depends on context which one is "better". Changing pin mode to GPIO output preserves the timer's internal state - it may even continue to run and for example throw interrupts, if that's desired. On the other hand, setting output compare mode to forced may allow to have a defined width pulse if you switch it back to PWM in a random time.

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All Answers

waclawek.jan (/s/profile/0050X000007vqmpQAA) (Community Member)

Edited May 27, 2019 at 7:20 AM

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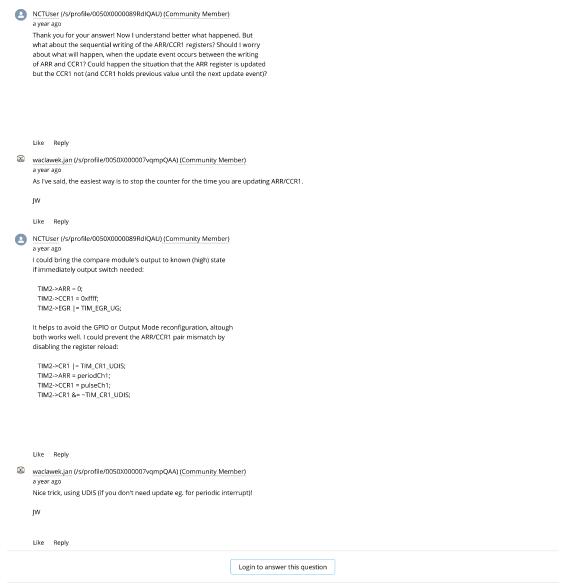
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