imagination. Solutions.

NEC

# Analog Master

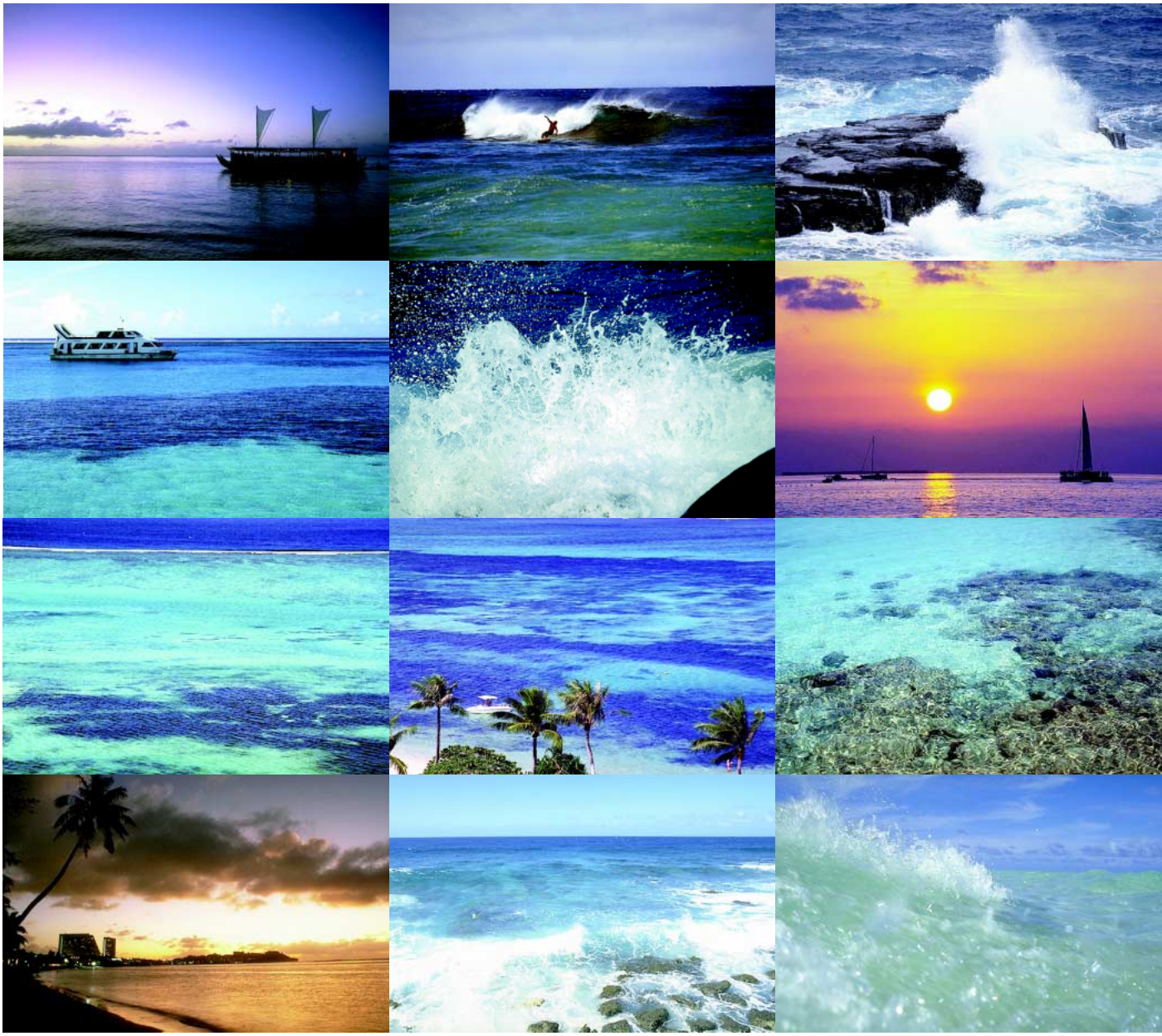
September,2001

# Wave

We can find various size of waves generated in the ocean. The wave is sometimes energetic sometimes week according to the forces of nature and the gravitational effect of the moon, an infinitely continuous activity.

We can also find another kind of wave in electric circuits: the wave of an analog signal. This wave has great significance for humankind, despite it being much smaller than the wave in the ocean.

Engineers seek to control the analog signal, this tiny and great wave, to improve the performance and accelerate downsizing of an application system.

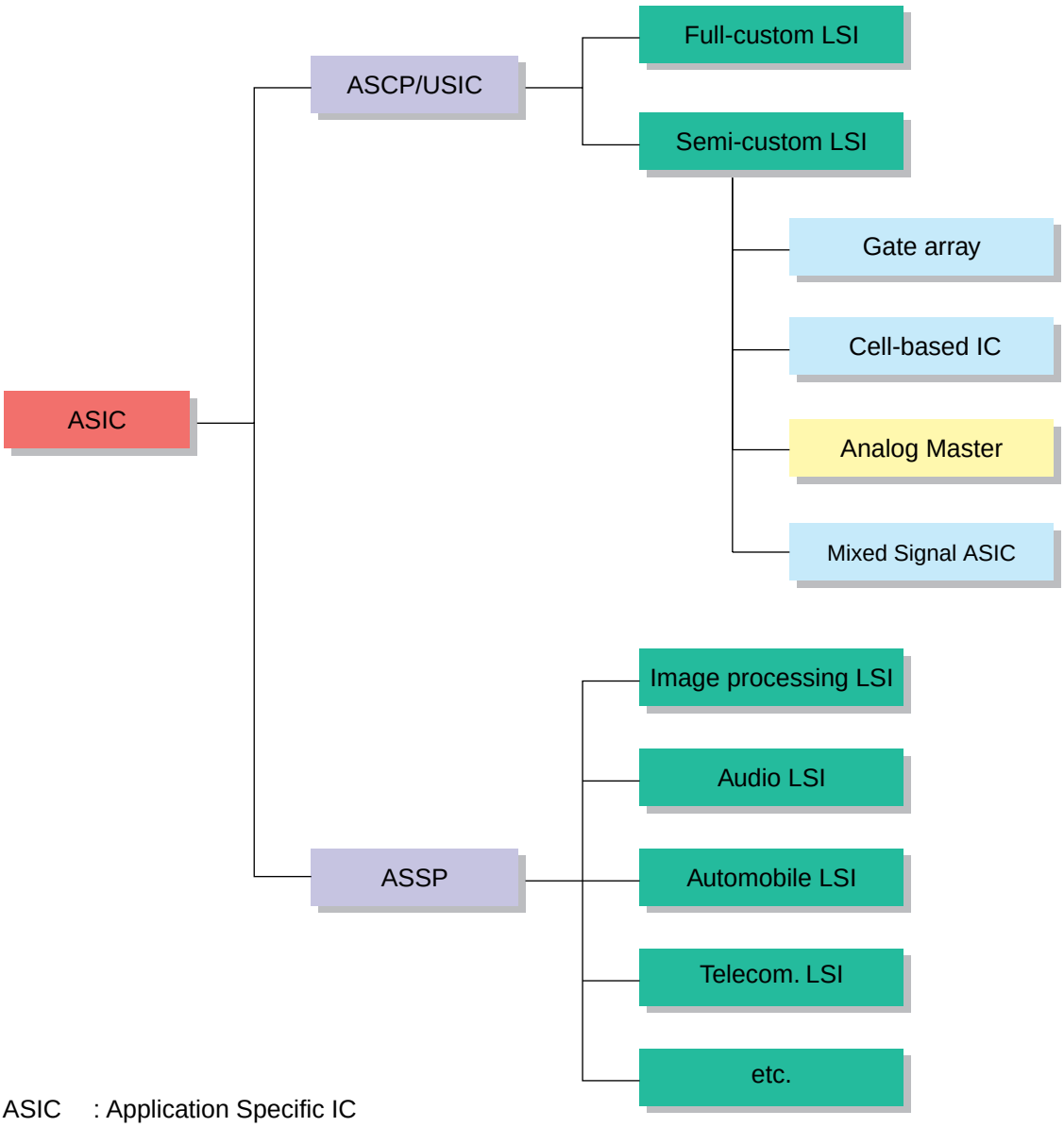


NEC introduces Analog Master, which is a semi-custom LSI just for handling the wave of analog signals, and proposes the use the Analog Master to integrate analog circuits on one-chip, supporting powerful library of macros, variety of masters and reliable development tools.

## *CONTENTS*

# NEC's ASICs

## Classification of ASICs




ASIC : Application Specific IC
ASCP : Application Specific Custom Product
USIC : User Specific IC
ASSP : Application Specific Standard Product

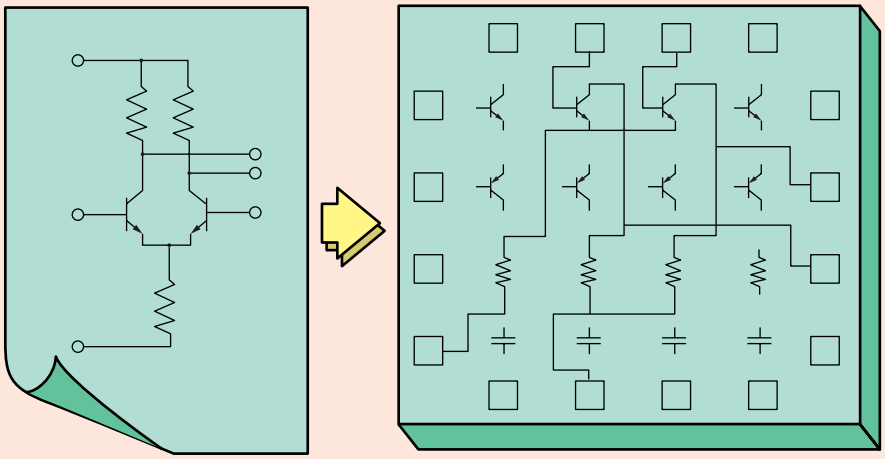
**Remark** For details about the Gate array and Cell-based IC, please refer to **ASIC Line-up Pamphlet(A10696E).**

# What is Analog Master?

The Analog Master is a semi-custom LSI for creating analog circuits on a master wafer by inter-connecting pre-diffused elements (bipolar transistors, resistors, and capacitors, already formed on the wafer) with the user-defined wiring.

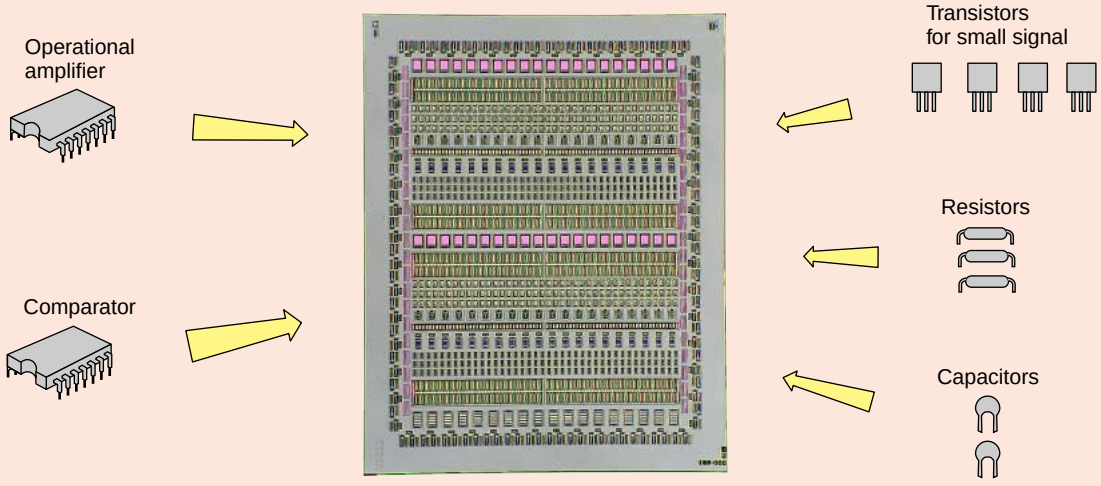
Analog Master is ideal for users who want to develop small-lot analog LSIs with low development cost in a short development period.

## Realization image of an analog LSI by using Analog Master



- Bipolar process
- Transistors, resistors, and capacitors already formed on master wafer
- Elements at fixed positions

## One-chip integration of analog circuits on user's application



# Features of Analog Master

## ■ Very short development period

Four to eight weeks from layout design to ES (Engineering Sample) production

## ■ Powerful line-up

3 families (13 masters) are provided to cover wide range of operating frequency, voltage, and number of elements used.

| | | |
|---|---|---|
| General-purpose Analog Master | CHS family | : 5 masters |
| General-purpose Analog Master | CHS-A family | : 3 masters |
| High voltage Analog Master | M-CHS family | : 5 masters |

## ■ Various macro libraries

To reduce user's works, variety of macros are provided such as operational amplifier, comparator,  regulator, etc.

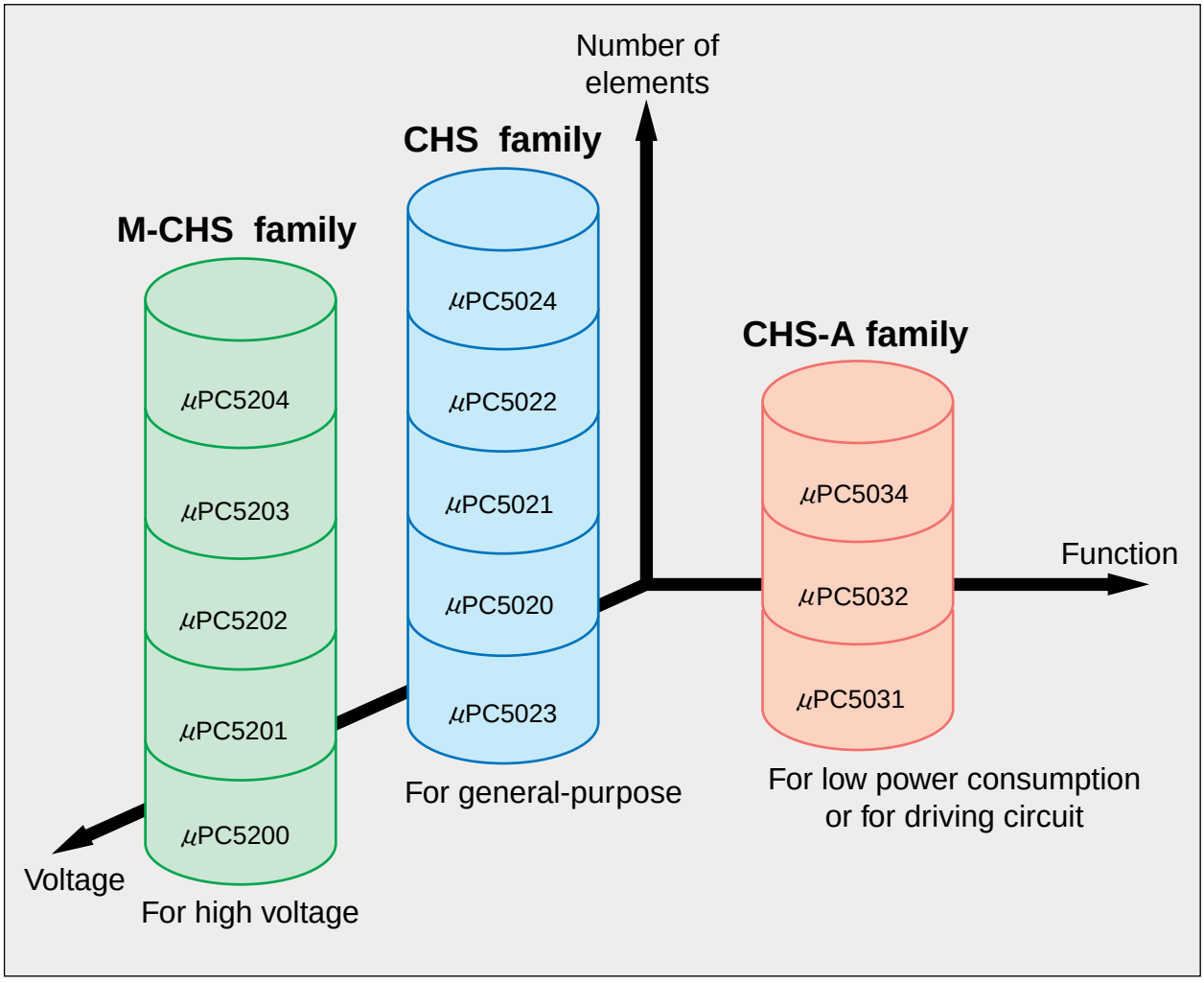
# Product Line-up of Analog Master

NEC's Analog Master is classified in the following 3 families(refer to the figure below).

- CHS family and CHS-A family for wide application field
- M-CHS family for high voltage

From this wide line-up (3 families 13 masters), user can achieve the optimum analog LSI.

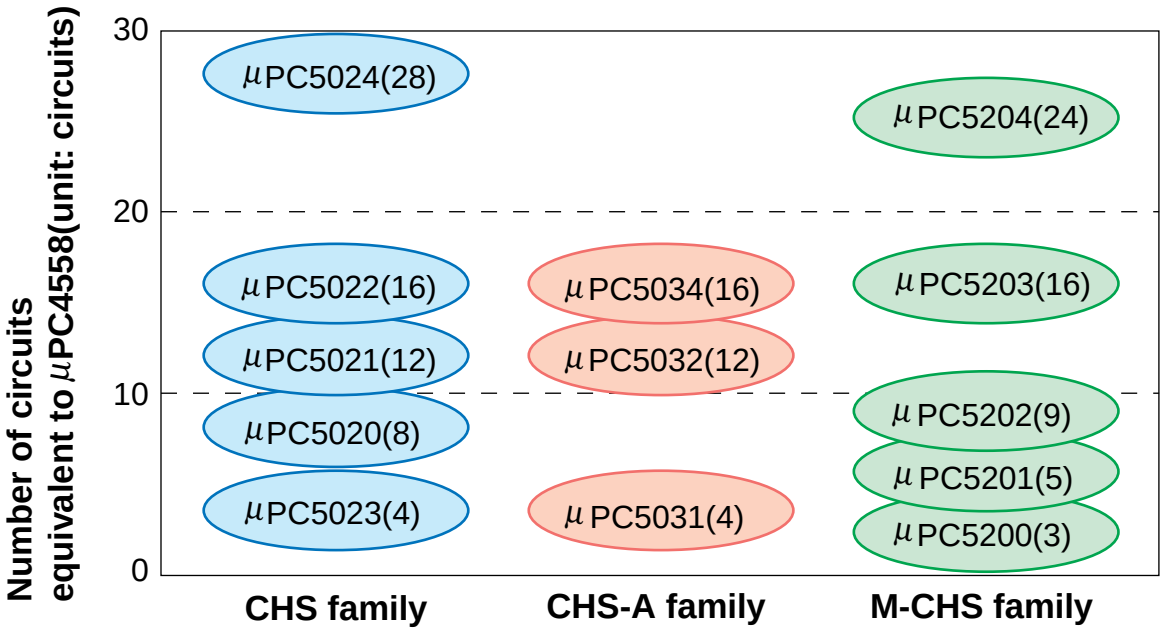
## Line-up and features



# Circuit Scale of Each Family

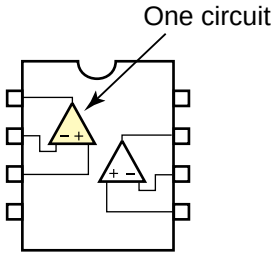
The scale of the circuit that can be integrated on the analog master differs depending on the model of each family.

The scale of the circuit that can be integrated shown below is roughly calculated in terms of the number of circuits where one circuit is equivalent to the general-purpose operational amplifier μPC4558[Note 1].




(Numbers in the parentheses indicate the number of circuits[Note 2] that can be integrated.)

**Notes 1.** One of the two operational amplifiers in the general-purpose operational amplifier μPC4558 package (8-pin DIP) is counted as one circuit.




**2.** The number of circuits shown above is a guideline in which only operational amplifiers are integrated, and does not include operational amplifier peripheral circuits (such as feedback circuits).
When selecting a model, estimate the circuit scale by taking these peripheral circuits into consideration.

## Features of CHS family

- High speed transistors (NPN : 6 GHz, Vertical PNP : 280 MHz)
- Excellent $h_{FE}$ linearity of transistor
- Easy to configure low power circuits
- Adequate for circuit operating at up to 12 V and 50 MHz
- Variety of macro libraries

## Element characteristics of CHS family

### Element characteristics of CHS family

| Element | Item | Description |
|---|---|---|
| **Transistor** | Voltage | 14 V (Absolute maximum ratings) |
| | Transient frequency ($f_T$) | NPN CHT1 : 4.5 GHz<br>CTW4 : 6.0 GHz<br>PNP CLP1 : 7.0 MHz<br>CVP1 : 280 MHz |
| | $h_{FE}$ standard value | NPN CHT1 : 100 ($I_C$ = 500 μA)<br>CTW4 : 100 ($I_C$ = 500 μA)<br>PNP CLP1 : 200 ($I_C$ = 10 μA)<br>CVP1 : 75 ($I_C$ = 10 μA) |
| | $h_{FE}$ linearity (CHT1) | $h_{FE}$ ($I_C$ = 10 μA)/$h_{FE}$ ($I_C$ = 100 μA) = 1.00 |
| **Resistor** | Resistance accuracy | Absolute accuracy : ±15 % (Ion-implanted)<br>: ±20 % (Polysilicon)<br>Relative accuracy (between adjacent resistors)<br>: ±2 % (Ion-implanted)<br>: ±3 % (Polysilicon) |
| **Capacitor** | Capacitance accuracy | Absolute accuracy : ±15 %<br>Relative accuracy : ±2 % (between adjacent resistors) |

# Element configuration of CHS family

- 5 masters are available from μPC5023 to μPC5024 for small to large complexity circuit, respectively.
- The CHS family should be designed so that the utilization rate of each element is up to 70 % (Only μPC5023 should be designed up to 60 %).

## Masters of CHS family

| Part Number | | μPC5020 | μPC5021 | μPC5022 | μPC5023 | μPC5024 | Remarks |
|---|---|---|---|---|---|---|---|
| Technology | | High-speed bipolar technology | | | | | Name : CHS |
| Supply voltage | | 14 V | | | | | Abusolute maximum ratings |
| Number of pads | | 28 | 32 | 50 | 22 | 80 | |
| Total number of elements | | 1627 | 2327 | 3041 | 726 | 6151 | |
| Total number of transistors | | 484 | 688 | 892 | 245 | 1508 | |
| NPN transistors | CHT1 | 224 | 320 | 416 | 112 | 672 | $I_{C(MAX.)}$ = 2 mA[Note1] |
| | CTW4 | 28 | 40 | 52 | 13 | 84 | $I_{C(MAX.)}$ = 18 mA[Note2] |
| | CEW4 | 8 | 8 | 8 | 4 | 80 | $I_{C(MAX.)}$ = 18 mA[Note2] (For electro-static protection) |
| PNP transistors | CLP1 | 168 | 240 | 312 | 84 | 504 | $I_{C(MAX.)}$ = 0.05 mA[Note1] (Lateral type) |
| | CVP1 | 56 | 80 | 104 | 32 | 168 | $I_{C(MAX.)}$ = 0.5 mA[Note1] (Vertical type) |
| Total number of resistors | | 1116 | 1600 | 2098 | 468 | 4560 | |
| Ion-implanted resistors | 500 Ω | 544 | 784 | 1024 | 224 | 1664 | $P^+$ resistor |
| | 5 kΩ | 544 | 784 | 1024 | 200 | 2496 | $P^-$ resistor |
| Polysilicon resistors | 2.5 kΩ | 28 | 32 | 50 | —— | —— | $N^+$ resistor |
| | 3 kΩ | —— | —— | —— | 44 | 400 | $N^+$ resistor |
| Number of capacitors(5 pF) | | 27 | 39 | 51 | 13 | 83 | MOS capacitor |

**Notes 1.** $I_{C(MAX.)}$ is a collector current value that reduces the value of DC current amplification factor $h_{FE}$ by 30 % compared to its peak value.

**2.** Maximum collector current value whose reliability can be guaranteed because it is limited by the maximum current density.

# Macro library

● TEGs are also provided.

## Macro library of CHS family

| Function | Library Name | Feature | Specifications | Equivalent | Availability |
|---|---|---|---|---|---|
| Operational amplifier | OA01A | General-purpose | $V_{IO}$ : 1.4 mV (TYP.) | μPC4558 | Available |
| | OA02A | Single power supply, high-speed | $SR^+$ : 8 V/μs (TYP.) | μPC842 | Available |
| | OA03A | Low power | $I_{CC}$ : 5 μA (TYP., $I_{SET}$ = 1 μA) | μPC4250 | Available |
| | OA04B | High input impedance | $I_B$ : 1 nA (TYP.) | —— | Available |
| | OA06B | Single power supply, stable | $V_{ICM}$ : 0 to $V^+$ – 1.5V | μPC358 | Available |
| | OA06C | Single power supply, $V_{om}^+$ improved | $V_{om}^+$ : $V^+$ – 1.2 V (MIN.) | μPC358 | Available |
| | OA07A | High-speed, high stability | $SR^+$ : 70 V/μs (TYP.) | —— | Available |
| | OA07B | High-speed, wide band | GBW : 200 MHz (TYP.) | —— | Available |
| | OA08 | Low noise | $e_n$: 6.5 nV/$\sqrt{Hz}$ (TYP.) | —— | Available |
| | OA09 | General-purpose (reduced element version) | $V_{IO}$ : 1.2 mV (TYP.) | —— | Available |
| | OA10 | NPN input low noise | $e_n$ : 3 nV/$\sqrt{Hz}$ (TYP.) | —— | Available |
| Comparator | CP02A | High-speed | $t_{PD}$ : 80 ns (TYP.) | μPC319 | Available |
| | CP04 | Single power supply | $t_{PD}$ : 0.5 μs (TYP.) | μPC393 | Available |
| Regulator | RG01A | General-purpose | $V_O$ : 1.3 to 9.0 V | —— | Available |
| | RG02A | General-purpose | $V_O$ : 2.7 to 9.5 V | —— | Available |
| | RG03 | Low saturation | | —— | Available |
| Switch | SW01A | Bi-directional switch (High-active) | | —— | Available |
| | SW01B | Bi-directional switch (Low-active) | | —— | Available |
| | SW02 | Signal switch | | —— | Available |
| Timer | TM01 | Timer | | μPC1555 | Available |

**Remark** TEG (Test Element Group) is a sample of macro.

## Features of CHS-A family

- Compatible with the CHS family (same process as CHS family is employed)
- Many-pin masters solving shortage of number of pins
- Total internal resistance 2 times higher than the CHS family
- Internal transistor for output driver (drive up to 50 mA )
- Super white TEG supporting application to microcontroller's peripheral analog circuits

## Element characteristics of CHS-A family

### Element characteristics of CHS-A family

| Element | Item | Description |
|---|---|---|
| Transistor | Voltage | 14 V (Absolute maximum ratings) |
| | Transient frequency ($f_T$) | NPN CST1 : 4.5 GHz<br>CTW3 : 5.0 GHz<br>PNP CLP1 : 7.0 MHz<br>CVP1 : 280 MHz |
| | $h_{FE}$ standard value | NPN CST1 : 100 ($I_C$ = 500 $\mu$A)<br>CTW3 : 100 ($I_C$ = 500 $\mu$A)<br>PNP CLP1 : 200 ($I_C$ = 10 $\mu$A)<br>CVP1 : 75 ($I_C$ = 10 $\mu$A) |
| | $h_{FE}$ linearity (CST1) | $h_{FE}$ ($I_C$ = 10 $\mu$A)/$h_{FE}$ ($I_C$ = 100 $\mu$A) = 1.00 |
| Resistor | Resistance accuracy | Absolute accuracy : ±15 % (Ion-implanted)<br>±20 % (Polysilicon)<br>Relative accuracy (between adjacent resistors)<br>: ±2 % (Ion-implanted)<br>±3 % (Polysilicon) |
| Capacitor | Capacitance accuracy | Absolute accuracy : ±15 %<br>Relative accuracy : ±2 % (between adjacent resistors) |

# Element configuration of CHS-A family

- Three masters with a different circuit scale and number of output driver transistors are available.
- The CHS-A family should be designed so that the utilization rate of each element is up to 70 %.

## Masters of CHS-A family

| Part Number | | μPC5031 | μPC5032 | μPC5034 | Remarks |
|---|---|---|---|---|---|
| Technology | | High-speed bipolar technology | | | Name : CHS |
| Supply voltage | | 14 V | | | Absolute maximum ratings |
| Number of pads | | 36 | 56 | 82 | |
| Total number of elements | | 575 | 1471 | 2251 | |
| Total number of transistors | | 223 | 578 | 896 | |
| NPN transistors | CST1 | 90 | 240 | 360 | $I_{C(MAX.)}$ = 2 mA Note1 |
| | CTW3 | 15 | 40 | 60 | $I_{C(MAX.)}$ = 18 mA Note2 |
| | CEW4 | 13 Note3 | 18 Note3 | 26 Note3 | $I_{C(MAX.)}$ = 25 mA Note2 (For electro-static protection) |
| PNP transistors | CLP1 | 90 | 240 | 360 | $I_{C(MAX.)}$ = 0.05 mA Note1 (Lateral type) |
| | CVP1 | 15 | 40 | 90 | $I_{C(MAX.)}$ = 0.5 mA Note1 (Vertical type) |
| Total number of resistors | | 338 | 854 | 1266 | |
| Ion-implanted resistors | 2 kΩ | 58 | 154 | 234 | $P^-$ resistor |
| | 10 kΩ | 232 | 616 | 936 | $P^-$ resistor |
| Polysilicon resistors | 3 kΩ | 48 | 84 | 96 | $N^+$ resistor |
| Number of capacitors(5 pF) | | 14 | 39 | 89 | MOS capacitor |

**Notes 1.** $I_{C(MAX.)}$ is a collector current value that reduces the value of DC current amplification factor $h_{FE}$ by 30 % compared to its peak value.

**2.** Maximum collector current value whose reliability can be guaranteed because it is limited by the maximum current density.

**3.** When used as 50-mA output drivers, the number of elements is halved.

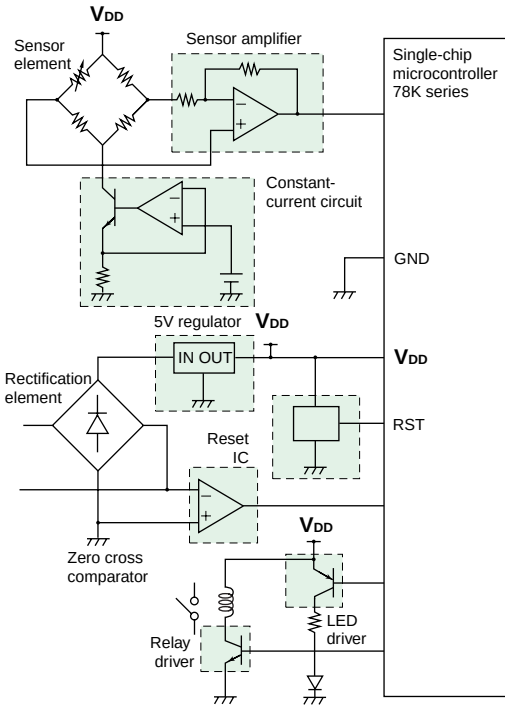
# Macro library

● TEGs are also provided.

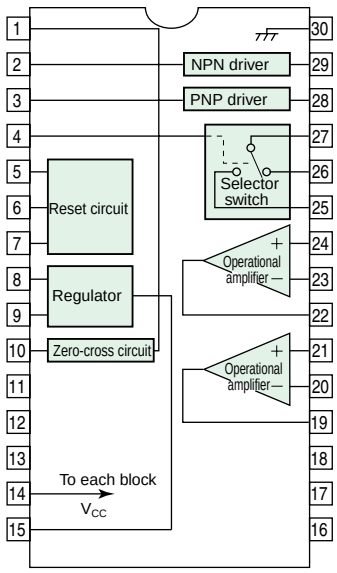
## Macro library of CHS-A family

| Function | Library Name | Feature | Specifications | Equivalent | Availability |
|---|---|---|---|---|---|
| Operational amplifier | OA0301 | General-purpose | $V_{IO}$ : 1.4 mV (TYP.) | μPC4558 | Available |
| | OA0302 | Single power supply, high-speed | $SR^+$ : 5 V/μs (TYP.) | μPC842 | Available |
| | OA0303 | Low power | $I_{CC}$ : 6 μA (TYP.,$I_{SET}$ = 1μA) | μPC4250 | Available |
| | OA0304 | High input impedance | $I_B$ : 1 nA (TYP.) | —— | Available |
| | OA0306B | Single power supply, general-purpose | $V_{ICM}$ : 0 to $V^+$–1.4 V (TYP.) | μPC358 | Available |
| | OA0309 | General-purpose (reduced element version) | | —— | Available |
| Comparator | CP0304 | Single power supply | $t_{PD}$ : 0.5 μs (TYP.) | μPC393 | Available |
| Regulator | RG0301 | General-purpose | $V_O$ : 1.3 to $V_{CC}$ – 2 V | —— | Available |
| Switch | SW0302 | Signal switch | | —— | Available |
| Super white TEG[Note] | WT03A | Operational amplifier x 2, regulator, signal switch, driver x 2 | | —— | Available |

**Note** Provided with an analog circuit for use microcontroller peripherals. (package : 30-pin shrink DIP)




Example of using super white TEG




Super white TEG block diagram

Use the Super White TEG at the locations enclosed by the dotted lines in figure.

## Features of M-CHS family

- Maximum supply voltage : 44 V
- High speed transistors (NPN : 2 GHz, vertical PNP : 50 MHz)
- Incorporates low noise lateral PNP transistors (HLP2A transistor)
- Adequate for circuit operating at up to 40 V and 10 MHz

## Element characteristics of M-CHS family

### Elememt characteristics of M-CHS family

| Element | Item | Description |
|---|---|---|
| Transistor | Voltage | 44 V (Absolute maximum ratings) |
| | Transient frequency ($f_T$) | NPN HDT1 : 2 GHz<br>HTW4 : 2 GHz<br>PNP HLP2 : 2 MHz<br>HVP3 : 50 MHz |
| | $h_{FE}$ standard value | NPN HDT1 : 100 ($I_C$ = 500 $\mu$A)<br>HTW4 : 100 ($I_C$ = 500 $\mu$A)<br>PNP HLP2 : 100 ($I_C$ = 10 $\mu$A)<br>HVP3 : 100 ($I_C$ = 10 $\mu$A) |
| | $h_{FE}$ linearity (HDT1) | $h_{FE}$ ($I_C$ = 10 $\mu$A)/$h_{FE}$ ($I_C$ = 100 $\mu$A) = 1.00 |
| Resistor | Resistance accuracy | Absolute accuracy : ±15 % (Ion-implanted)<br>±20 % (Polysilicon)<br>Relative accuracy (between adjacent resistors)<br>: ±2 % (Ion-implanted)<br>: ±3 % (Polysilicon) |
| Capacitor | Capacitance accuracy | Absolute accuracy : ±15 %<br>Relative accuracy : ±2 % (between adjacent capacitors) |

# Element configuration of M-CHS family

- 5 masters are available from μPC5200 to μPC5204 for small to large complexity circuit, respectively.
- The M-CHS family should be designed so that the utilization rate of each element is up to 70 %.

## Masters of M-CHS family

| Part Number | | μPC5200 | μPC5201 | μPC5202 | μPC5203 | μPC5204 | Remarks |
|---|---|---|---|---|---|---|---|
| Technology | | High-speed, high voltage bipolar technology | | | | | Name : M-CHS |
| Supply voltage | | 44 V | | | | | Absolute maximum ratings |
| Number of pads | | 24 | 28 | 40 | 52 | 62 | |
| Total number of elements | | 653 | 1029 | 1786 | 3087 | 4561 | |
| Total number of transistors | | 189 | 303 | 535 | 932 | 1382 | |
| NPN transistors | HDT1 | 72 | 120 | 216 | 384 | 576 | $I_{C(MAX.)}$ = 1.0 mA[Note1] |
| | HTW4 | 9 | 15 | 27 | 48 | 72 | $I_{C(MAX.)}$ = 10 mA[Note1] |
| | HEW4 | 12 | 14 | 20 | 26 | 31 | $I_{C(MAX.)}$ = 10 mA[Note1] |
| | HTT5 | 12 | 14 | 20 | 26 | 31 | $I_{C(MAX.)}$ = 18 mA[Note2] |
| PNP transistors | HLP2 | 48 | 80 | 144 | 256 | 384 | $I_{C(MAX.)}$ = 0.12 mA[Note1] (Lateral type) |
| | HLP2A | 18 | 30 | 54 | 96 | 144 | Low noise PNP $I_{C(MAX.)}$ = 0.12 mA[Note1] (Lateral type) |
| | HVP3 | 18 | 30 | 54 | 96 | 144 | $I_{C(MAX.)}$ = 1.0 mA[Note1] (Vertical type) |
| Total number of resistors | | 456 | 712 | 1225 | 2108 | 3108 | |
| Ion-implanted resistors | 500 Ω | 144 | 240 | 426 | 760 | 1144 | $P^+$ resistor |
| | 10 kΩ | 216 | 360 | 639 | 1140 | 1716 | $P^-$ resistor |
| Polysilicon resistors | 500 Ω | 96 | 112 | 160 | 208 | 248 | $N^+$ resistor |
| Number of capacitors(5 pF) | | 8 | 14 | 26 | 47 | 71 | MOS capacitor |

**Notes 1.** $I_{C(MAX.)}$ is a collector current value that reduces the value of DC current amplification factor $h_{FE}$ by 30 % compared to its peak value.

**2.** Maximum collector current value whose reliability can be guaranteed because it is limited by the maximum current density.

# Macro library

● TEGs are also provided.

## Macro library of M-CHS family

| Function | LibraryName | Feature | Specifications | Equivalent | Availability |
|---|---|---|---|---|---|
| Operational amplifier | OA201 | General-purpose | $V_{IO}$ : 1.0 mV (TYP.) | μPC4558 | Available |
| | OA202 | Single power supply, stable | $V_{ICM}$ : 0 to $V^+$ – 1.5 V | μPC358 | Available |
| | OA203 | Low power | $I_{CC}$ : 16 μA (TYP., $I_{SET}$ = 2 μA) | μPC4250 | Available |
| | OA204 | High input impedance | $I_B$ : 1.2 nA (TYP.) | —— | Available |
| | OA205A | High-speed, high stability | $SR^+$ : 30 V/μs (TYP.) | —— | Available |
| | OA205B | High-speed, wide band | $f_{unity}$ : 50 MHz (TYP.) | —— | Available |
| | OA205C | High-speed, 1 block version | | —— | Available |
| | OA206 | Low noise | $e_n$ : 4.5 nV/$\sqrt{Hz}$ (TYP.) | μPC4570 | Available |
| | OA207 | Single power supply, high-speed | $SR^+$ : 7.5 V/μs (TYP.) | μPC842 | Available |
| Comparator | CP201 | Single power supply | $t_{PD}$ : 3 μs (TYP.) | —— | Available |
| | CP202 | High-speed | $t_{PD}$ : 180 ns (TYP.) | μPC319 | Available |
| Regulator | RG201 | General-purpose | | —— | Available |
| Switch | SW201A | Bi-directional switch (High-active) | | —— | Available |
| | SW201B | Bi-directional switch (Low-active) | | —— | Available |
| | SW202 | Signal switch | | —— | Available |

**Remark** TEG (Test Element Group) is a sample of macro.

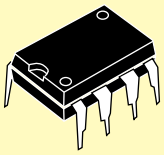
# Packages

To meet various requirements about the package type and the number of pins, variety of packages are available for the Analog Master. User can select optimum combination for each application. For availability, refer to the tables of the following pages.

## Packages available for Analog Master

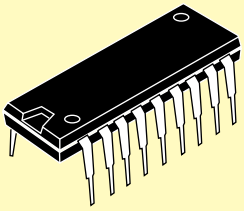
### DIP

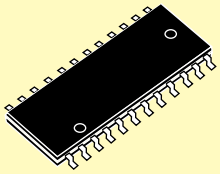
14-pin (7.62 mm(300))
16-pin (7.62 mm(300))
18-pin (7.62 mm(300))
22-pin (10.16 mm(400))



### Shrink DIP

18-pin (7.62 mm(300))
20-pin (7.62 mm(300))
22-pin (7.62 mm(300))
24-pin (7.62 mm(300))
28-pin (10.16 mm(400))
30-pin (10.16 mm(400))
42-pin (15.24 mm(600))
48-pin (15.24 mm(600))



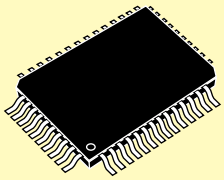


### SOP

8-pin (5.72mm (225))
14-pin (5.72mm (225))
16-pin (5.72mm (225))
16-pin (7.62mm (300))
16-pin (9.53mm (375))
20-pin (7.62mm (300))
24-pin (7.62mm (300))
24-pin (9.53mm (375))
28-pin (9.53mm (375))

### Shrink SOP

14-pin (5.72mm (225))
16-pin (5.72mm (225))
20-pin (5.72mm (225))
20-pin (7.62mm (300))
24-pin (7.62mm (300))
30-pin (7.62mm (300))
36-pin (7.62mm (300))
38-pin (7.62mm (300))



### QFP

48-pin ( 7 × 7 )
48-pin (10 × 10)
48-pin (10 × 14)
56-pin (10 × 10)
64-pin (14 × 20)
68-pin (10 × 14)
72-pin (10 × 10)
80-pin (14 × 14)
80-pin (14 × 20)

### TQFP

48-pin ( 7 × 7 )

## Package availability of CHS family

| Package | | Lead Pitch | μPC5020 | μPC5021 | μPC5022 | μPC5023 | μPC5024 |
|---|---|---|---|---|---|---|---|
| DIP | 8-pin | 2.54 mm | — | — | — | — | — |
| | 14-pin | 2.54 mm | — | — | — | ○ | — |
| | 16-pin | 2.54 mm | — | — | — | ○ | — |
| | 18-pin[Note] | 2.54 mm | — | — | — | ○ | — |
| | 22-pin | 2.54 mm | — | — | ○ | — | — |
| Shrink DIP | 14-pin | 1.778 mm | — | — | — | — | — |
| | 18-pin | 1.778 mm | — | ○ | — | ○ | — |
| | 20-pin | 1.778 mm | — | — | — | ○ | — |
| | 22-pin | 1.778 mm | — | — | — | ○ | — |
| | 24-pin | 1.778 mm | ○ | ○ | — | — | — |
| | 28-pin | 1.778 mm | — | — | ○ | — | — |
| | 30-pin | 1.778 mm | — | ○ | ○ | — | — |
| | 42-pin[Note] | 1.778 mm | — | — | ○ | — | — |
| | 48-pin | 1.778 mm | — | — | — | — | — |
| SOP | 8-pin | 1.27 mm | — | — | — | ○ (5.72 mm) | — |
| | 14-pin | 1.27 mm | — | — | — | ○ (5.72 mm) | — |
| | 16-pin | 1.27 mm | ○ (7.62 mm) | ○ (9.53 mm) | — | ○ (5.72 mm) | — |
| | 20-pin | 1.27 mm | ○ (7.62 mm) | ○ (7.62 mm) | — | ○ (7.62 mm) | — |
| | 24-pin | 1.27 mm | ○ (7.62 mm) | ○ (7.62 mm) | ○ (9.53 mm) | ○ (7.62 mm) | — |
| | 28-pin | 1.27 mm | ○ (9.53 mm) | ○ (9.53 mm) | ○ (9.53 mm) | — | — |
| Shrink SOP | 14-pin | 0.65 mm | — | — | — | ○ (5.72 mm) | — |
| | 16-pin | 0.65 mm | — | — | — | ○ (5.72 mm) | — |
| | 20-pin | 0.65 mm | ○ (5.72 mm) | — | — | ○ (5.72 mm) | — |
| | | 0.65 mm | ○ (7.62 mm) | — | — | — | — |
| | 24-pin | 0.65 mm | ○ (7.62 mm) | — | — | ○ (7.62 mm) | — |
| | 30-pin | 0.65 mm | — | ○ (7.62 mm) | — | — | — |
| | 36-pin | 0.8 mm | ○ (7.62 mm) | — | — | — | — |
| QFP | 48-pin | 0.5 mm | — | ○ (7 x 7) | ○ (7 x 7) | — | — |
| | | 0.65 mm | — | — | ○ (10 x 10) | — | — |
| | | 0.8 mm | — | — | ○ (10 x 14) | — | ○ (10 x 14) |
| | 64-pin | 1.0 mm | — | — | — | — | ○ (14 x 20) |
| | 68-pin | 0.65 mm | — | — | — | — | ○ (10 x 14) |
| | 80-pin | 0.8 mm | — | — | — | — | ○ (14 x 20) |
| TQFP | 48-pin | 0.5 mm | — | ○ (7 x 7) | ○ (7 x 7) | — | — |

**Note** Because the time is required to prepare for production, consult NEC before development. Also consult NEC when you use 42-pin shrink DIP packages.

**Remarks1.** In the above table, '○' indicates a package that is available, and ' – ' indicates a package that is unavailable.

**2.** Some packages may have unavailable pins. Please refer to the **Analog Master Package Manual (A10495E)** for unavailable pins.

# Packages

## Package availability of CHS-A family

| Package | | Lead Pitch | μPC5031 | μPC5032 | μPC5034 |
|---|---|---|---|---|---|
| Shrink DIP | 18-pin | 1.778 mm | — | — | — |
| | 22-pin | 1.778 mm | ◯(7.62 mm) | — | — |
| | 24-pin | 1.778 mm | — | — | — |
| | 28-pin | 1.778 mm | — | — | — |
| | 30-pin | 1.778 mm | — | ◯(10.16mm) | — |
| SOP | 16-pin | 1.27 mm | ◯(7.62 mm) | ◯(7.62 mm) | — |
| | 20-pin | 1.27 mm | ◯(7.62 mm) | ◯(7.62 mm) | — |
| | 24-pin | 1.27 mm | ◯(7.62 mm) | ◯(7.62 mm) | ◯(9.53 mm) |
| | 28-pin | 1.27 mm | — | ◯(9.53 mm) | ◯(9.53 mm) |
| Shrink SOP | 24-pin | 0.65 mm | — | ◯(7.62 mm) | — |
| | 30-pin | 0.65 mm | — | ◯(7.62 mm) | — |
| | 36-pin | 0.80 mm | ◯(7.62 mm) | ◯(7.62 mm) | — |
| | 38-pin | 0.65 mm | — | ◯(7.62 mm) | — |
| QFP | 48-pin | 0.5 mm | ◯ ( 7 x 7 ) | ◯ ( 7 x 7 ) | ◯ ( 7 x 7 ) |
| | 56-pin | 0.65 mm | — | ◯ ( 10 x 10 ) | ◯ ( 10 x 10 ) |
| | 80-pin | 0.65 mm | — | — | ◯ ( 14 x 14 ) |
| TQFP | 48-pin | 0.5 mm | — | ◯ ( 7 x 7 ) | ◯ ( 7 x 7 ) |

**Remarks1.** In the above table, '◯' indicates a package that is available, and ' – ' indicates a package that is unavailable.

**2.** Some packages may have unavailable pins. Please refer to the **Analog Master Package Manual (A10495E)** for unavailable pins.

## Package availability of M-CHS family

| Package | | Lead Pitch | μPC5200 | μPC5201 | μPC5202 | μPC5203 | μPC5204 |
|---|---|---|---|---|---|---|---|
| DIP | 8-pin | 2.54 mm | — | — | — | — | — |
| | 14-pin | 2.54 mm | — | — | — | — | — |
| | 16-pin | 2.54 mm | — | — | — | — | — |
| | 18-pin | 2.54 mm | — | — | — | — | — |
| | 22-pin | 2.54 mm | — | — | — | — | — |
| | 24-pin | 2.54 mm | — | — | — | — | — |
| | 28-pin | 2.54 mm | — | — | — | — | — |
| | 42-pin | 2.54 mm | — | — | — | — | — |
| Shrink DIP | 14-pin | 1.778 mm | — | — | — | — | — |
| | 20-pin | 1.778 mm | — | — | — | — | — |
| | 24-pin | 1.778 mm | ○ | ○ | — | — | — |
| | 28-pin | 1.778 mm | — | — | ○ | — | — |
| | 30-pin | 1.778 mm | — | — | — | — | — |
| | 42-pin[Note] | 1.778 mm | — | — | ○ | — | — |
| | 48-pin[Note] | 1.778 mm | — | — | — | ○ | — |
| SOP | 16-pin | 1.27 mm | ○ (7.62 mm) | — | — | — | — |
| | 20-pin | 1.27 mm | ○ (7.62 mm) | — | — | — | — |
| | 24-pin | 1.27 mm | ○ (7.62 mm) | ○ (7.62 mm) | ○ (9.53 mm) | — | — |
| | 28-pin | 1.27 mm | — | ○ (9.53 mm) | ○ (9.53 mm) | — | — |
| Shrink SOP | 20-pin | 0.65 mm | ○ (7.62 mm) | ○ (7.62 mm) | — | — | — |
| | 24-pin | 0.65 mm | — | ○ (7.62 mm) | — | — | — |
| QFP | 48-pin | 0.5 mm | — | ○ ( 7 x 7 ) | — | — | — |
| | | 0.65 mm | — | — | ○ (10 x 10 ) | — | — |
| | | 0.8 mm | ○ (10 x 14) | — | — | ○ (10 x 14 ) | — |
| | 56-pin | 0.65 mm | — | — | — | — | ○ (10 x 10 ) |
| | 64-pin | 1.0 mm | — | — | — | ○ ( 14 x 20 ) | — |
| | 72-pin | 0.5 mm | — | — | — | — | ○ (10 x 10 ) |
| | 80-pin | 0.65 mm | — | — | — | — | ○ (14 x 14 ) |
| TQFP | 48-pin | 0.5 mm | — | ○ ( 7 x 7 ) | — | — | — |

**Note** Because the time is required to prepare for production, consult NEC before development. Also consult NEC when you use 42-pin, or 48-pin shrink DIP packages.

**Remarks1.** In the above table, '○' indicates a package that is available, and ' – ' indicates a package that is unavailable.

**2.** Some packages may have unavailable pins. Please refer to the **Analog Master Package Manual (A10495E)** for unavailable pins.

# Development of Analog Master

The development of the Analog Master is completed by both the user and NEC. Passing the development work from the user to NEC is called interfacing.

NEC supports only the circuit diagram level interface.

| Interface Level | System Design | Circuit Design | Layout Design | ES Production |
|---|---|---|---|---|
| Circuit design level | User's works | | NEC's works | |

## ● Circuit diagram level interface

User completes up to system design, NEC takes over all subsequent works, such as circuit design and simulation.

This interface level is classified into 3 more levels as shown in the table below, depending on parts configuring the circuit and whether or not to create and estimate a breadboard.

| Level | Creation and Estimation of Breadboard | Parts Configurating the Circuit |
|---|---|---|
| S level | Not necessary | General-purpose SSI[Note 1], Standard SSI[Note 2], Transistor for small signal, Analog Master TEG[Note 3], Resistors, Capacitors |
| A level | Necessary | Standard SSI[Note 2], Transistor for small signal, Analog Master TEG[Note 3], Resistors, Capacitors |
| B level | Necessary | Analog Master TEG[Note 3], Resistors, Capacitors (80 % or more is configured with macro) |

**Notes** **1.** General-purpose SSI : SSI except standard SSI

**2.** Standard SSI : OP amp. ( μPC151/741, 251/1458, 258/4558, 451/324, 458/4741, 802/4250, 842, 844, 1251/358, 4556, and equivalents of other manufacturers)

: Comparator ( μPC177/1339, 271/311, 272/319, 277/393, and equivalents of other manufacturers)

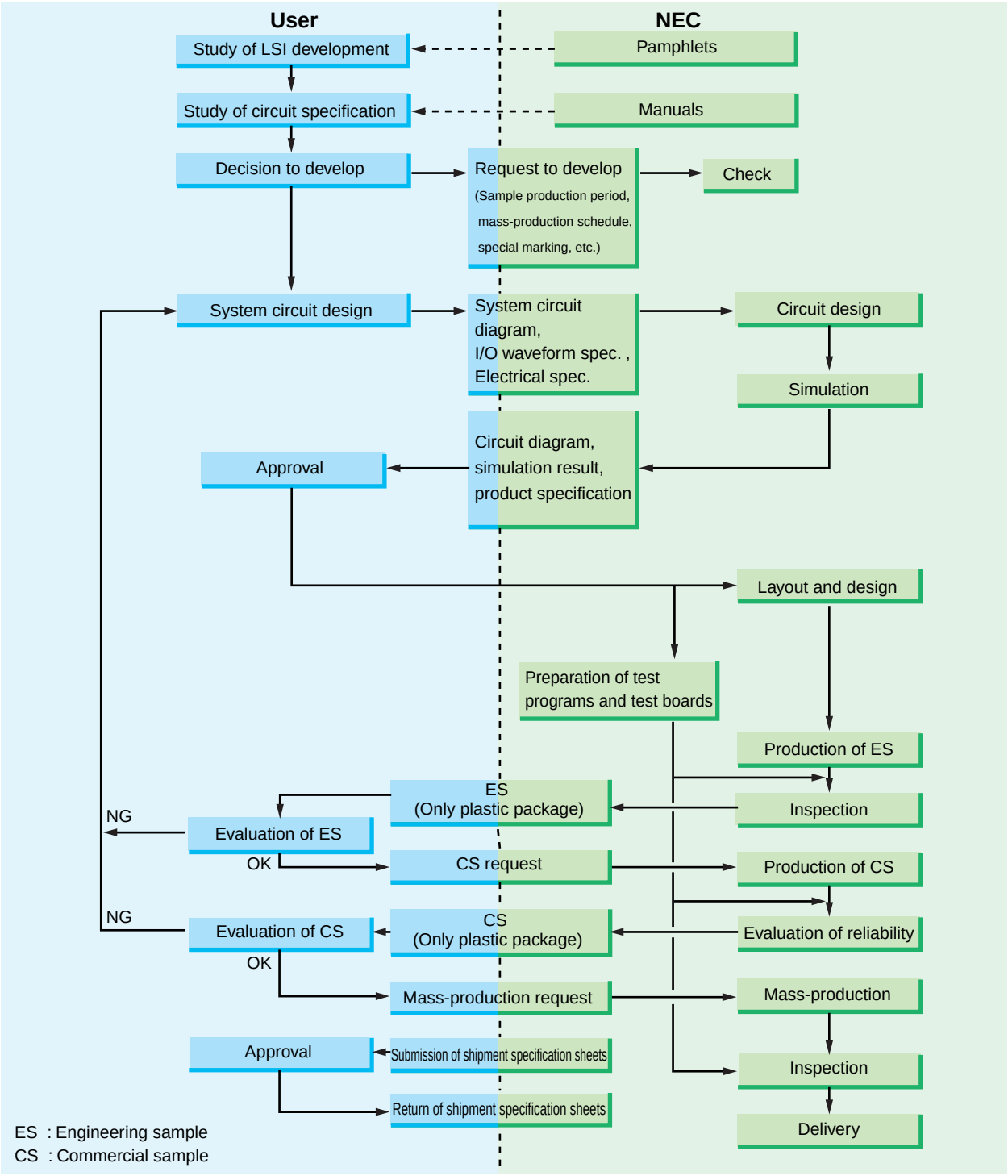
: Regulator (Three-terminal regulator, Shunt regulator)

: Function block ( μPC617/1555, and equivalents of other manufacturers)

**3.** Analog Master TEG : Library TEGs, basic block TEGs, super white TEGs provided by NEC.

**Remark** TEG (Test Element Group) is a sample for evaluation.

# Flow for circuit diagram level interface




**Remark** Unlike CS and mass-produced model, the quality of ES is not guaranteed. Therefore, do not use the ES for production or reliability testing.

## Works by user

### (1) Study of circuit specifications

User checks circuit requirements such as supply voltage range, pin voltages, circuit performance, package, and resistance to electro-static discharge (ESD)damage, according to manuals supplied by NEC.

### (2) Request to develop

User requests NEC to develop the chip, and provides detailed descriptions of the followings.

1. Interface level
2. Master name, package
3. Scheduled interface date, ES/CS delivery date, schedule of mass-production
4. Request of special marking
5. Request of TEG

### (3) Circuit design

User designs circuit configuration so as to realize required function and performance using parts configuring circuit on page 22 (system circuit design).

### (4) Interface (circuit diagram level interface)

**User sends the following interface documents to NEC after completion of system circuit design.**

**1. System block diagram**
**2. System circuit diagram**
**3. I/O waveform specifications**
**4. Electrical specifications**
**5. Check sheet**

**It is recommended that the above documentation be submitted on special forms supplied by NEC.**
**Describe in as much detail as possible because this is important information for IC design and simulation.**

## (5) Approval of circuit diagram

Circuit diagram designed by NEC, simulation result, and product specification are sent to user.
After all items are checked and approved by user, NEC starts layout design and ES production.

## (6) Evaluation of ES and request to prepare CS

User evaluates engineering samples (ES). Two levels of samples are sent. One is standard sample, and the other called variation sample is for assersion of electrical characteristics (note that NEC does not assure characteristic variation to user with this sample). After the samples pass evaluation, user requests NEC to prepare commercial samples (CS) after discussing and determining actual specification of test condition list.

## (7) Evaluation of CS and request to start mass-production

User evaluates commercial samples (CS).
After the samples pass evaluation, user requests NEC to start mass production.

## Works by NEC

### (1) Helping user in studying LSI development

When user plans to develop particular LSIs, NEC is ready to give advices on whether the user's circuit specifications can be achieved from the viewpoint of the number of elements and element characteristics. Please consult NEC after determining the specifications.

### (2) Circuit design

According to user's circuit requirements, NEC completes circuit design, and simulation, and prepares test conditions. This testing is only for DC items.

### (3) Layout design

Layout design requires 1 to 4 weeks. In addition, before completion of layout design, back annotation is performed.
Characteristics will be checked by extracting the parasitic elements to feedback to the circuit design side and performing simulation. Layout design requires one additional week for this checking.

### (4) ES production

The user will usually receive the ES 3 to 4 weeks after completion of layout design.

### (5) CS production

After request by user, NEC starts production of commercial samples.
From CS production request, it takes in general 1 month for standard quality grade device, and 2.5 month for special quality grade device to deliver the CS.
The above schedule is conditional upon whether the product specifications have been determined between the user and NEC.

### (6) Preparation of shipment specification sheets

The shipment specification sheets describe absolute maximum ratings, electrical characteristics, package outline, and marking.

### (7) Mass-production

NEC mass-produces the LSI according to the user's production schedule.

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