Using IEEE 1149.1 Boundary Scan (JTAG) With Cypress Ultra37000™ CPLDs

AN1024

Associated Project: No
Associated Part Family: CY37512, CY37384, CY37256, CY37192, CY37128, CY37064, CY37032
GET FREE SAMPLES HERE
Associated Application Notes: None

Application Note Abstract

As Printed Circuit Boards (PCBs) have become multi-layered with double-sided component mounting and Integrated Circuits have incorporated smaller lead spacing and higher pin counts, the traditional bed of nails approach to PCB testing is becoming impractical. The Joint Test Action Group, JTAG (a consortium of European companies), was formed to identify a standard to test the interconnectivity of devices via a Boundary-Scan register approach. The solution that was agreed upon was Boundary Scan Test (BST). BST is a test technique that simplifies printed circuit board testing by providing a standard chip-board test interface.

Introduction

The Institute of Electrical and Electronics Engineers (IEEE) accepted the JTAG proposal and established the IEEE Standard Test Access Port and Boundary-Scan Architecture (IEEE 1149.1) in 1990. JTAG enables the board manufacturer to test for opens and shorts on a board without directly connecting to the nodes on the board which are often inaccessible with today's fine lead pitch packages.

The Ultra37000 CPLD family is an extension to the FLASH370i™ CPLD family and includes the popular ISR™ programmability and pin locking features as well as BST support. The FLASH370i family supports ISR programming through the JTAG interface; however, these devices do not support BST. It is suggested that the following three application notes, "An Introduction to In-System Reprogramming with the Ultra37000," "An Introduction to In-System Reprogramming with the FLASH370i," and "Designing With Cypress In System Reprogrammable (ISR) CPLDs for PC Cable Programming" be read along with this application note to become familiar with the two product families and ISR.

This application note provides an overview of the BST implementation in the Ultra37000 programmable logic family and shows how to connect the devices in the JTAG chain for BST as well as ISR operations. The following topics are discussed in this application note: the JTAG architecture, the JTAG Boundary Scan Register (BSR) for the Ultra37000 and the other data registers IDcode and Usercode, description of Boundary Scan Operation, the Boundary-Scan Description Language (BSDL), software tools available for ATPG of JTAG vectors for BST, chaining Ultra37000 devices for JTAG and ISR operations, and chaining Ultra37000 and FLASH370i devices in the same chain for JTAG and ISR operations.

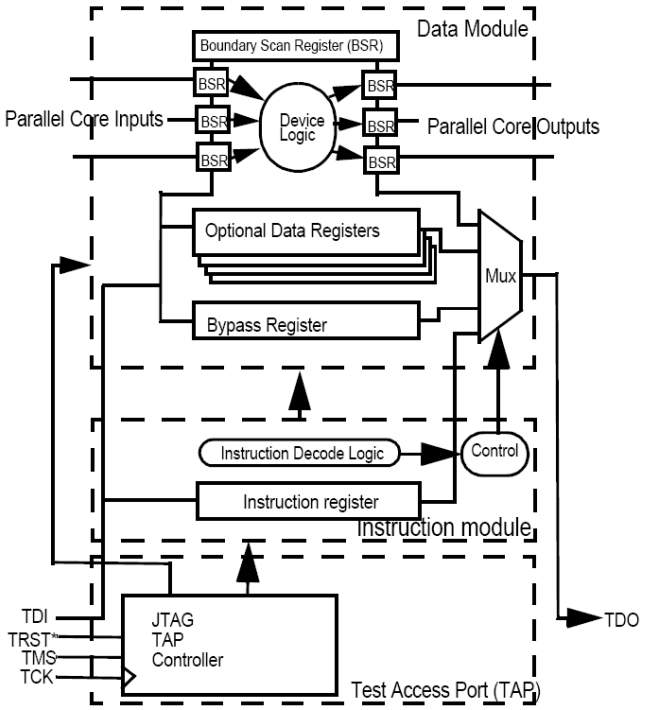
IEEE 1149.1 Basics

The BST technique uses a serial register chain called a Boundary Scan Register (BSR), instead of a traditional "bed of nails" approach, to access Integrated Circuits (ICs) on a Printed Circuit Board (PCB). The scan chain is comprised of the input and output pads of an IC's design, thus allowing access to the primary inputs for stimulus and the outputs for the sampling of data. BST supports the following board-level test functions: testing IC interconnect on a PCB for faults, IC

Cluster testing, identifying missing and wrong components, identifying fixture problems and limited testing of individual chips on board.

Figure 1 shows the basic architecture of a device that supports boundary scan design that complies with the 1149.1 standard. At the top level, the boundary scan logic has three modules: Test Access Port (TAP), the Instruction Module, and the Data Module.

Figure 1. Simplified JTAG 1149.1 Architecture



To “test” a component with the BSR the following simplified procedure must be followed.

1. Shift test patterns into the BSR cells at the component BSR input pins.
2. Drive test signals from the BSR to the device pins.
3. Sample responses into the BSR from the device pins.
4. Shift responses out of the BSR and out of the device for comparison to expected data.

This will be explained in further detail in this application note.

Architecture

The TAP consists of a 16-state finite-state machine that controls the state progression of the JTAG test logic and provides serial access to the instruction and data modules. The state diagram for the TAP controller is shown in Figure 2.

State machine transitions are determined by the value of TMS, and occur on the rising edge of TCK. TDO transitions occur on the falling edge of TCK. The TAP controller resets to the Test-Logic-Reset state in one of three ways: at power on reset, asserting the TRST* pin if available, or by clocking five cycles with TMS held HIGH. Following is an explanation of the states of the TAP.

Test-Logic-Reset: When the boundary-scan logic is in the reset mode the device is in normal operation. The TAP controller is powered up in this state. Holding the TMS to a logic

HIGH and applying five TCK clock cycles will also return the controller to this state regardless of what state the TAP currently resides.

Run-Test/Idle: The operation of the Boundary Scan logic depends on the instruction held in the instruction register. Some JTAG operations, such as BIST, execute in this state where clock cycles are needed.

Select-DR/IR: Either a data or instruction register is selected and placed between TDI and TDO. TDI inputs will be shifted serially into the selected register.

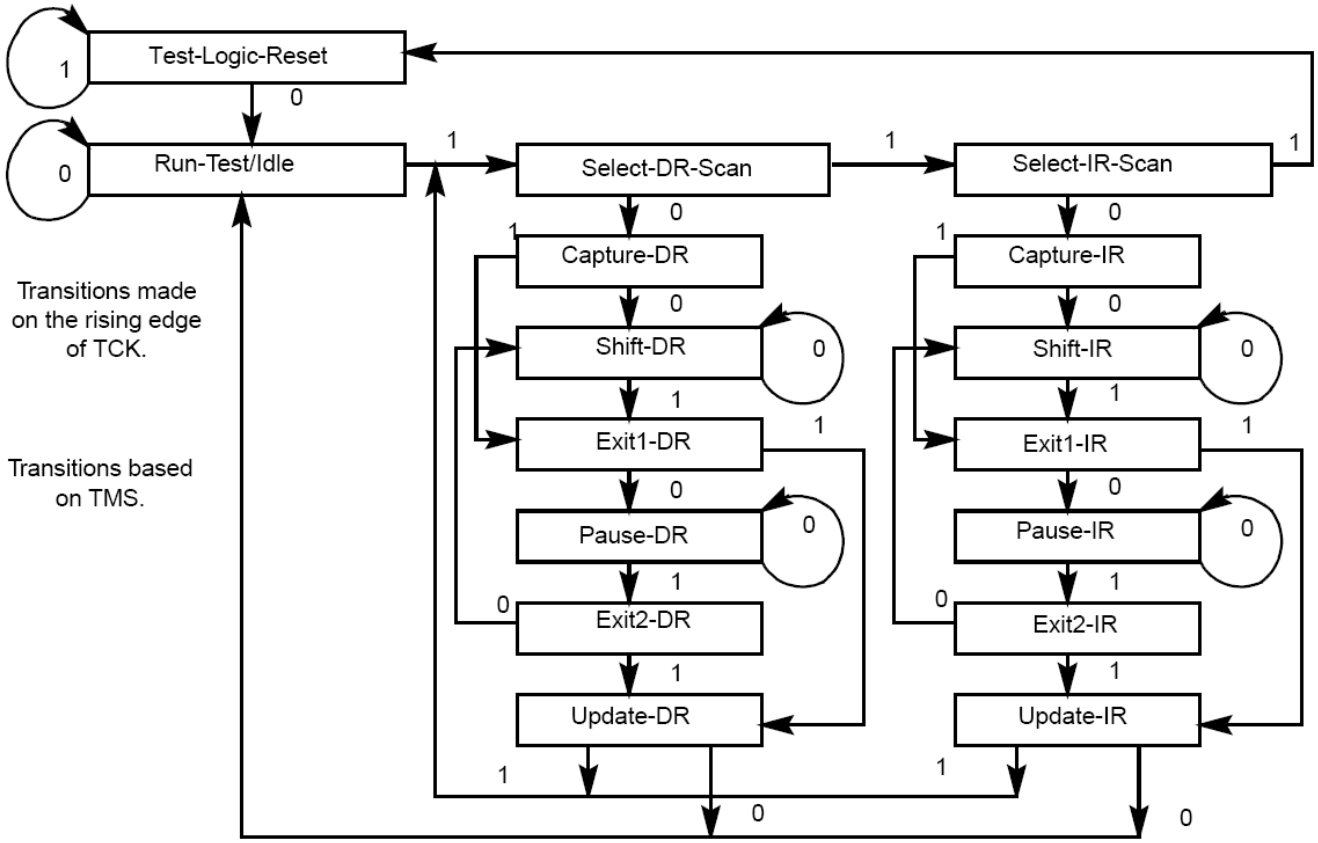
Capture-DR/IR: Data or instructions are loaded in a parallel fashion into the selected shift register chain. If the Boundary Scan register (BSR) is selected then data from external pins or internal nodes in the device can be sampled or captured into the capture register portion of the BSR.

Shift-DR/IR: The captured data (Capture-DR/IR) is shifted out of the TDO pin while new data is shifted into the TDI pin. These are the only TAP states where the TDO pin is driving and not left in the high-impedance state, three-state. The TDO pin exits the three-state on the first falling edge of TCK after entering either of these two states and enters the three-state on the first falling edge of TCK after leaving either of the shift states. No data is shifted upon entry into a shift state. The last bit shifted into the data or instruction registers occurs on the rising TCK edge when the shift state is exited going to the Exit-DR/IR TAP state.

Update-DR/IR: This marks the completion of the shifting process, and either the Instruction register is loaded to implement the next instruction or one of the Data registers is updated. Data from the Capture register of the selected Data register is loaded into the Update register of the selected Data register. If the EXTEST instruction is selected the BSR is given permission to drive the I/O pins of the device.

Other States: The Pause and Exit states are provided to allow the shifting to be halted for any test reason. An example of such a reason is when ATE systems reload tester memory. Next, the description of the JTAG registers is discussed.

Figure 2. JTAG State Diagram



IEEE 1149.1 Internal Registers

Instruction Register

The Instruction register JTAG circuitry operates according to the instructions that are loaded serially into the Instruction register from the TDI input. The Instruction register length for the Ultra37000 is 6 and for the FLASH370i it is 4.

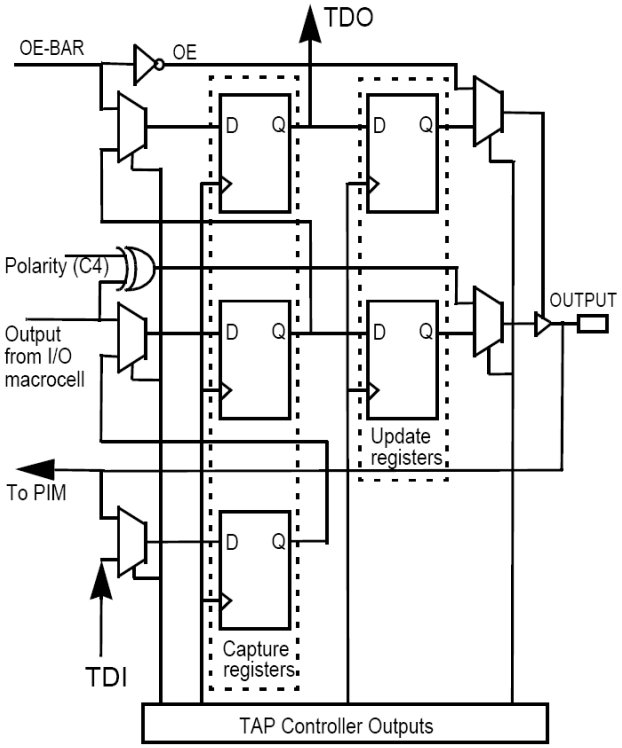
Data Registers

The Data registers are accessed through the control of the TAP state and the instruction loaded into the Instruction register. Only one Data register is accessed at a time. The Ultra37000 family supports the Data registers required by 1149.1 which are: the BSR, the Instruction register, and the Bypass register. In addition the Ultra37000 family supports the Usercode, and IDcode registers.

Boundary Scan Register (BSR)

The BSR is a large serial shift register chain that associates register cells with the I/O pads of a device. Each I/O pin has three register cells associated with it: output enable, output, and I/O feedback as shown in Figure 3.

Figure 3. Boundary Scan for I/O Pins



The only exception is I/O pins that share their functionality with JTAG pins on the dual-function devices. These I/O pins do have a BSR associated with them. The Boundary Scan registers are not placed on buried macrocells. Inspection of this Boundary Scan cell reveals how data can be captured from the external pin and shifted out of the Capture registers for external inspection. This data is captured when entering the Capture-DR state in the TAP with the EXTEST instruction loaded into the Instruction register. During BST when the EXTEST instruction is selected, the TAP chooses the output of the Update register to be the output of the device. The Update register enables fixed data to be forced to external pins when data in the Capture registers is shifted out of the BSR TDO pin for external inspection. This prevents external system biasing conditions on the circuit board from changing when BSR data is shifted out for inspection. In normal PLD operation the TAP chooses the I/O macrocell data to pass through the output mux; hence, the BSR does not affect the normal functionality of the device, except for the small delay of the two input mux. Each individual BSR cell is chained together serially to form the BSR by connection of the TDO output from one BSR cell to the TDI input of the next BSR in the chain.

The I/O BSR cell conforms to the 1149.1 specification in all aspects except for sampling the output enable and the output macrocell data during the Capture/Preload TAP instruction. The captured data is inverted for the output enable and is potentially inverted for the output macrocell data depending upon whether the data is inverted from the output of the register through the polarity architecture bit. This lack of conformance is not a problem for performing typical JTAG BST testing since the data captured from the external pin is correct. Capturing the output enable and macrocell internal data is typically done during the INTEST TAP instruction when testing the internal functionality of the JTAG device. Since the INTEST instruction is not supported, this functionality is therefore not necessary.

Each input or clock pin only has one Boundary Scan register cell associated with it as shown in Figure 4.

Figure 4. Boundary Scan for Dedicated Input and Input/Clock Pins

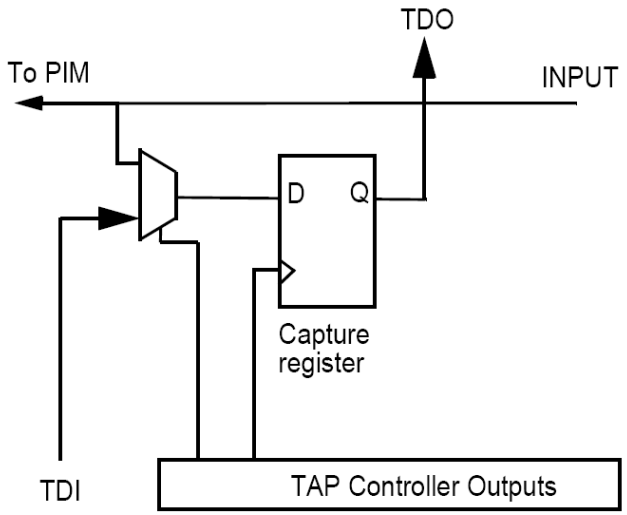


Figure 5. EXTEST with Boundary Scan

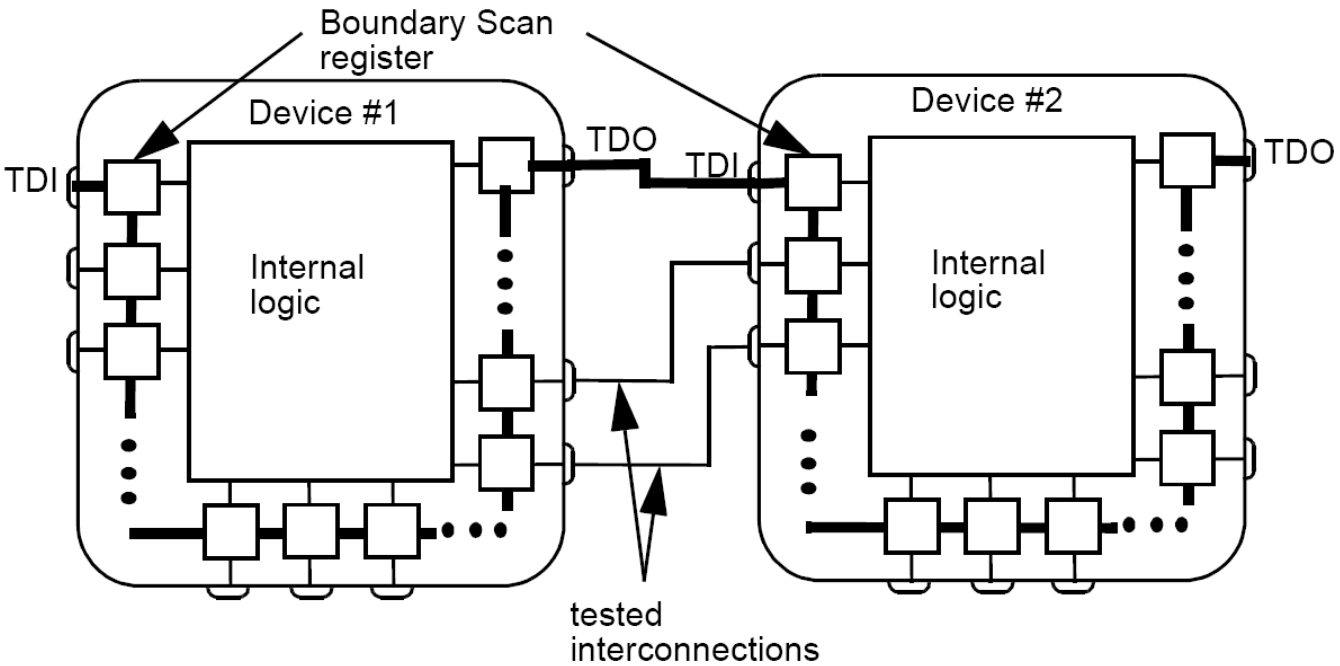


Figure 5 shows the BSR of two devices on a PCB and how the external connections between the devices are tested. All “data” is scanned/shifted into the device from the TDI pin. The data for device one can be “enabled” to the outputs of device one and “sampled” into the inputs of device two. The sampled data is then scanned/shifted out of device two and compared to expected results on the tester for a pass/fail result. The control of shifting, updating, and sampling data is via the TAP controller.

The topic of producing serial test vectors to test all shorts and opens on interconnections between components is a complicated subject and well beyond the scope of this application note; however, vectors to test the two connections of Figure 5 are shown as an example to illustrate how the boundary scan testing works. In this case the patterns “01” and “10” can be forced from the outputs of device#1 and captured into the BSR of device#2. These two serial vectors are sufficient to test for both shorts and opens in these two interconnections. In general the first task of BSR testing is to detect all possible shorts first, then, when it has been verified that no shorts exist on the interconnect lines, to test for opens or discontinuities in the lines. The reason for detecting shorts first is to limit the amount of time a device output driver is overdriven as a result of a short. If a short existed between these two lines then the captured data in device#2 could either be a “00” or a “11” upon application of either vector depending upon which logic level in the output structure, drive HIGH or drive LOW, had the strongest drive. The application of the two vectors tests to make sure that the two lines are not shorted together or shorted to either VCC or GND. In this case they also test for opens since both logic levels of each line are confirmed.

Bypass Register

The bypass register is a mandatory 1-bit register that allows for fast serial transfer of data at the board level from the TDI to the TDO pins (chaining). The bypass register provides a minimum-length path through those chips that are not to be included in the serial test chain.

Device Identification Register

The Device Identification register (IDcode) is loaded with a 32-bit number comprised of the chip design version number, the part number, and the JEDEC manufacturer ID code. Table 1 shows the bit assignment for the fields of the IDcode register. The part number portion of the IDcode is shown in Table 2.

Table 1. IDCODE Register Definition

MSB 31			LSB 0
Version (4 bits)	Part Number (16 bits)	Manufacturing Number (11 bits)	1

Table 2. Part Number Portion of the IDCODE Register for Ultra37000 CPLDs

#mc’s/#IOs	part type (4 bits)	Ultra37000 # macrocells (6 bits)	# I/Os (6 bits)
32/32	1X00	000010	000010
64/32	1X00	000100	000010
64/64	(0/1)X00	000100	000100
128/64	1X00	001000	000100
128/128	1X00	001000	001000
256/128	1X00	010000	001000
256/160	0X00	010000	001010
256/192	0X00	010000	001100
384/160	0X00	011000	001010
384/192	0X00	011000	001100
512/160	0X00	100000	001010
512/192	0X00	100000	001100
512/264	0X00	100000	010000

The Version number begins with XX00 and increments with every substantial device or JTAG functional change of the device. The first 2 MSB bits are “don’t care” bits. An additional third bit, the second MSB location, in the part number section of the IDcode register is reserved as a “don’t care” bit. These bits are reserved for major programming algorithm changes to the device that do not effect JTAG functionality. The Ultra37000V family of devices has the same part number code except for the part type section of four bits. This changes from “0X00” to “0X01” to denote the 3.3V family of devices. The MSB bit of the part type section signifies whether the package type is a dual-function package, the JTAG pins share their functionality with I/O pins, or a single-function package, the JTAG pins are stand alone. For dual-function packages the MSB bit is a ‘1’ value and for single-function packages the MSB bit is a ‘0’ value. The Ultra37064 is offered in both the 100-pin TQFP package, which is a

single-function device, and the 84-pin PLCC package, which is a dual-function device.

The manufacturer ID is defined in the JTAG specification 106A, which assigns a unique number for silicon vendors. The Manufacturer ID code for Cypress devices is 000 0011 0100B. The least significant bit (LSB) of the IDcode register is loaded with a value of ONE, which is purposely designed to be the opposite polarity of the Bypass register initially loaded value of ZERO. This is dictated by 1149.1 to ease initial board scan tests for chain integrity testing.

Usercode Register

The Usercode Register is left for user defined applications. The register is 16 bits in length and can be used to track information such as the version of the JEDEC file used to program the device. The 1149.1 standard requires that the Usercode register be 32 bits long; therefore, the Cypress implementation of the Usercode does not adhere to this requirement. All other 1149.1 requirements for design and operation of the Usercode register are satisfied in the Ultra37000 devices.

Description of Instructions

The Ultra37000 family of CPLDs supports the required 1149.1 instructions: Sample/Preload, Extest, and Bypass. In addition to these required instructions, the IDcode and Usercode instructions are also included. HIGHZ, CLAMP, INTEST and BIST are not supported in the Ultra37000 devices. A brief description of each instruction follows. Table 3 shows the instructions and codes to be loaded into the device to execute the instruction. The left-most bit corresponds to the bit nearest TDI, the right-most bit corresponds to TDO.

Table 3. IEEE 1149.1 (JTAG) Public Test Instruction Codes in the Ultra37000

Code	Instruction
000000	EXTEST
000010	SAMPLE/PRELOAD
000100	IDCODE
000111	USERCODE
111111	BYPASS

Sample/Preload

The Sample/Preload instruction inserts the BSR between the TDI and TDO pins upon entry into the Capture-DR TAP state. It allows signals at the device pins to be captured and examined, which is the sampling function. It also allows for an initial data pattern to be applied at the device output pins when using BST to test connectivity between devices on the circuit board, which is the preload function. The loading of the Sample/ Preload and the shifting of this initial data precedes the loading of the EXTEST instruction which actually forces, or writes, data to the device I/O pins.

Extest

The EXTEST instruction inserts the BSR between the TDI and TDO pins as does the Sample/Preload instruction except now with pin forcing capability. It allows the external circuitry and board-level interconnect to be tested by forcing multiple test patterns at the output pins of one device on the board and sampling the data at the input pins of another device on the board. This instruction allows testing of connections between components on a circuit board which is the main purpose of boundary scan testing. All the bits of the Instruction register need to be ZEROS as specified in 1149.1.

IDcode

The IDCODE instruction inserts the IDcode register between the TDI and TDO pins upon entry into the Capture-DR TAP state. The contents of the register are shifted out for examination. This instruction is useful as a initial board integrity test to make sure the correct devices are loaded into the appropriate places on the circuit board.

Usercode

The Usercode instruction inserts the Usercode register between the TDI and the TDO pins upon entry into the Capture- DR TAP state. The contents of the register are shifted out for examination. This register provides a location where the user can store specific information regarding items such as programming.

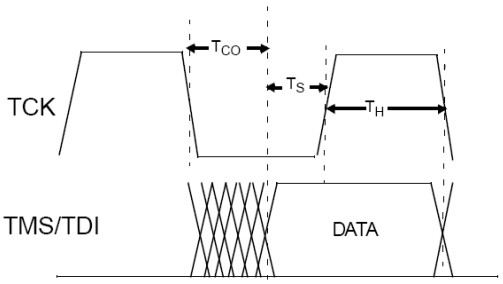
Bypass

The Bypass instruction inserts a single-bit register between the TDI and the TDO pins upon entry into the Capture-DR TAP state. This instruction allows for the fast serial movement of test patterns through the device and is chosen when no operations are desired on the device that is loaded with this instruction. In large JTAG chains this single-bit path through the device shortens the number of cycles necessary to access a particular device in the chain; consequently, the number of bits in the JTAG chain is reduced along with test time. All the bits of the instruction register need to be ONES as specified in 1149.1.

JTAG Timing Parameters

Figure 6 shows the timing parameters associated with JTAG. The parameters are optimized to maximize the frequency of operation of the TAP controller. The clocking of the TDO signal on the falling edge of the clock and the clocking of the TDI and TMS inputs on the rising edge of the clock ensures that there are no set-up and hold time violations, either external to the device or from one BSR element to the next BSR element in the chain, resulting in a race condition.

Figure 6. JTAG Configuration w/o ISR—Single-Function Mode Operation



T_{CO} – (20 ns) falling TCK to TDO output
T_S – (0 ns) TDI,TMS setup time to rising TCK
T_H – (20 ns) TDI,TMS hold time to rising TCK
f_{TAP} – (20 MHz) TCK maximum frequency

Boundary Scan Test Flow Procedure

This next section describes how the TAP controller, instruction module, and Data registers work together to test for opens and shorts between devices that support BST.

The first step is to make sure that the TAP controller starts in the Test-Logic-Reset state. Once the TAP is in this known state, then future desired states can easily be controlled with the TMS and TCK pins.

The next step is to select an instruction. This is accomplished by transitioning through the following TAP states: Run-Test-Idle, Select-DR-Scan, Select-IR-Scan, Capture-IR, Shift-IR, and Exit1-IR. Once in the Shift-IR state, it is required to stay in this state, TMS held LOW, for N – 1 cycles in order to completely fill up the Instruction register of N bits. The last bit is shifted into the Instruction register upon exiting the Shift state and entering the Exit1-IR state. This new instruction is loaded upon entry into the Exit-IR state but only becomes active upon entry into the next TAP state, Update-IR. The new instruction dictates which Data register is activated. If the new instruction is EXTEST then the BSR data register is selected and it forces the data stored in the Update register onto the device I/O pin. If the new instruction is Sample/Preload then the BSR will be selected and placed between the TDI and TDO pins as in EXTEST but the BSR will not force the data to the output pins of the device. If the new instruction is BYPASS, then a single register bit is placed between the TDI and TDO pins.

The next step is to capture data. The TAP transitions to the Capture-DR state by making the following transitions: Update- IR, Select-DR-Scan, and Capture-DR. At the Capture- DR state the appropriate Data register, selected by the loaded instruction, captures data. If the BYPASS instruction is loaded then a single bit of value ZERO is captured. If the BSR is selected, as during EXTEST, then it captures the device pin I/O data.

The next step is shifting out the selected data register for external inspection. From the Capture-DR state the TAP transitions to the Shift-DR and Exit-DR states. The Shift-DR state is held for however many cycles are needed to shift the required data out for inspection. At the same time data is being shifted out new data is shifted in. With EXTEST this applies the next value to be written to the external I/Os. From Exit-DR the TAP moves to Update-DR which transfers the data from the Capture portion of the target register to the parallel hold (Update) portion of the target register. At this point if the EXTEST instruction is loaded, a new value is forced from the BSR to the I/O pins of the device.

At this point a complete cycle of BST testing has completed and the next TAP transitions depend upon what operation is next desired. Typically, during BST, the EXTEST instruction is selected and the TAP will transition back through the Se- lect-DR-Scan, Capture-DR, Shift-DR, and Exit-DR as another pattern of HIGHs and LOWs is applied to the device I/O pins. The data is then captured and shifted out for inspection. Other options such as proceeding to the Run-Test-Idle state for operations such as ISR programming may occur or the TAP can transition to the appropriate states to load a new instruction.

As the reader can see there are many steps associated with the completion of BST testing. As a simpler example, here are the sequences of TAP controller states necessary to implement the Bypass instruction in an Ultra37000 device. The TAP moves through the following transitions: Test-Logic-Reset, Run-Test-Idle, Select-DR-Scan, Select-IR-Scan, Capture-IR, Shift-IR (the Bypass instruction of 11111 is shifted in, 5 cycles after the state is entered), Exit1-IR (on the rising edge of the clock that enters this state the last ‘1’ is shifted into the capture portion of the shift register to decode the Bypass instruction 111111), Update-IR (the Bypass instruction is now the active instruction), Select-DR-Scan, Capture-DR, and Shift-DR. When the Capture-DR state is entered the single register bit captures the value of ZERO which initializes the register to a predictable state. Once in the Shift-DR state the device is implementing the Bypass mode where data is clocked into the single-bit register on the rising clock edge and clocked out to TDO on the falling edge of the same clock.

The basic BST test algorithm, steps 1 through 12, is clearly summarized and explained in Kenneth P. Parker’s “The Boundary-Scan Handbook” and is included below to reinforce the operations performed. This is the procedure followed to test for opens or shorts on the interconnections between components on the board.

Step 1. Initialize the TAP to Test-Logic-Reset

Step 2. Load the Sample/Preload instruction which puts the BSR between TDI and TDO, but does not grant pin permission.

Step 3. Shift the first stimulus pattern into the BSR (preload phase)

Step 4. Load the EXTEST instruction. This puts the BSR between TDI and TDO and grants pin permission upon passing into state Update-IR which writes the first stimulus pattern.

Step 5. Capture (read) the response pattern into the shift portion of the BSR.

Step 6. Shift the captured response pattern out while shifting in the next stimulus pattern.

Step 7. Update (write) the next stimulus pattern.

Step 8. If the last stimulus pattern is written go to step 9 otherwise go to step 5.

Step 9. Capture (read) the last response pattern.

Step 10. Shift in a “safe” stimulus pattern while shifting out the last captured response pattern.

Step 11. Update (write) the safe pattern.

Step 12. Go to Test-Logic-Reset and halt the test.

The Boundary Scan Description Language (BSDL)

Each of the above steps for implementing BST is not too complicated; however, to complete all the tests necessary to provide adequate fault coverage for the entire circuit board, with all of its components, is an enormous task. Fortunately there are software tools that can generate the required bitstreams to implement BST. These tools need to know the exact Boundary Scan implementation of each device to accomplish their task. The BS implementation in a given JTAG device is described by its Boundary Scan Description Language (BSDL) file. BSDL is a subset of the VHDL language. BSDL files are available on the Cypress web page for the Ultra37000 devices. The VHDL constructs that make up the BSDL language are documented in the IEEE 1149.1b-1994 supplement to the IEEE 1149.1 standard. A complete discussion of the items in a BSDL file is not the intention of this application note, and in some cases is not necessary since they are self explanatory, but the main items, or those that are not intuitive, in the file are briefly discussed.

The file first contains a description of all the pin locations of the device documented in the Pin_Map_String constant.

constant pqfp_package:PIN_MAP_STRING:= <all pins including power pins included>

The Compliance_Patterns attribute is needed for the dual function mode Ultra37000 devices to indicate that the JTAGen pin must be driven to a HIGH state to enable the JTAG port.

attribute compliance_patterns of CYP37256_160 : entity is “(JTAGen) (1)”;

The Instruction_Capture attribute is important for initial JTAG integrity testing which verifies that there are no faults in the JTAG chain itself and that future JTAG results can be trusted. This attribute documents the fixed parallel loaded set of bits that are captured into the instruction register when the TAP controller enters the Capture-IR state. 1149.1 requires that the next to the last LSB and the LSB bits must equal ZERO and ONE respectively. When the data is shifted out and examined the number of transitions of HIGH and LOW must be at least as many as the number of devices in the chain.

attribute INSTRUCTION_CAPTURE of CYP37256_160 : entity is “000001”;

The Usercode_Register attribute normally is used to describe this to the Usercode register in BSDL; however, because the Cypress implementation uses 16 bits instead of 32 bits a different Instruction Opcode is required, USERCODEX, as shown below.

attribute INSTRUCTION_OPCODE of D256P160 : entity is

“BYPASS (111111),” &

“SAMPLE(000010),” &

“EXTEST (000000),” &

“IDCODE (000100),” &

“USERCODEX (000111)”;

Instead of the Usercode_Register attribute the Register_Access attribute is needed to access the instruction.

attribute REGISTER_ACCESS of D256P160 : entity is

“USER_CODE[16]

(USERCODEX CAPTURES XXXXXXXXXXXXXXX1)” ;

The Boundary_Length attribute defines the length of the BSR.

attribute BOUNDARY_LENGTH of CYP37256_160 : entity is 377;

The Boundary_Register attribute defines the actual circuit implementation described in a string of individual boundary scan elements. The total sum of these elements is the number defined by the Boundary_Length attribute. Below is an example of a portion of the BSR associated with the first I/O pin in the BSR chain. The first line of the string describes the input capture portion of the BSR. The second line of the string is the BSR associated with the macrocell output data on the I/O pin. The third line of the string is the BSR associated with the output enable on this I/O pin.

attribute BOUNDARY_REGISTER of CYP37256_160 : entity is

“376(BC_4, IO(123), input, X), “ &

“375(BC_1, IO(123), output3, X, 374, 0, Z), “ &

*“374(BC_1, *, control , 0), “ &*

The first port parameter defines which BSR cell design is used. There are eight different kinds of BS register cell designs. In this example BC_4 is used to capture the external pin data and BC_1 is used to capture the internal macrocell and internal output enable data. The figures of all eight different types of cell designs are listed in Chapter 10 of the IEEE 1149.1 1990 standard. The figures are referenced to the actual cell type (BC_1, BC_2, etc.) in section B.8.14 (Boundary- Scan register description) in the supplement to the IEEE 1149.1 1990 standard. In the above example these first three lines in the Boundary_Register attribute describe the schematic of the I/O BSR shown in Figure 3. In this example cell element number 376 connects to the TDI of the device. In the full BSR description cells 373 down to cell 0 would follow after cell number 374. It is an 1149.1 requirement that the BSR

cell element numbered ‘0’ be closest to the TDO pin. For more information on the details of all the port instantiations of the Boundary_Register attribute see Chapter 10 of the IEEE 1149.1 specification.

The second port parameter is the signal from the entity port statement that is attached to the cell. Output enable control or an internal cell has a ‘*’ for this entry.

The third port parameter identifies the cell function. In this example the first cell functions as an input to capture the external pin data. The second cell functions as an output3 which means the cell drives data to a three-state output. The third cell functions as an control which means the cell controls whether a three-state output is enabled or disabled. There are nine different options for this field. See section B.8.14.1.3 (The <function> element) in the supplement to the IEEE 1149.1 1990 standard.

The fourth port parameter is the value that software chooses to place into the capture and update registers to put the boundary scan device in a safe state when the software would otherwise randomly place a HIGH or LOW value into the registers. An example of this usage is disabling output drivers to prevent output contention problems. An ‘X’ entry means that it does not matter what value the software chooses. In this example ‘0’ is chosen on the output enable control BSR to disable the output driver.

The last three port parameters are optional and concern the output disable function. The fifth port parameter identifies the control cell that can disable the outputs. The sixth port parameter identifies the value that must be scanned into the control cell to disable the outputs. The seventh port parameter identifies the state of the output when it is disabled. Possible values are Z, Weak1 or Weak0. The latter options describe drivers that do not go into a three-state, very high impedance, condition when disabled such as a TTL open collector or ECL open emitter.

BST Software Tools

There are a number of software tools that are available to provide BST capability once BSDL files are obtained for the devices on the PCB. The tool takes as input the description of the circuit board with interconnects on the board and generates the necessary JTAG test vectors to implement BST. It reads in BSDL files for all the devices on the board and builds an appropriate model from it. Automatic Test Vector Generation (ATVG) routines create test vectors that can be downloaded from the parallel port of a PC to the PCB. This tests the functionality of the board with all the components, described by their associated BSDL files, on the PCB. Companies providing these or related tools are:

- Asset
- Corelis
- JTAG Technologies
- Goepel

Basic JTAG Connections Without ISR Programming Connections

This application note has covered the basics of the 1149.1 standard regarding architecture and BST procedures and the implementation of BST in the Ultra37000 devices. The next topic is connecting Ultra37000 devices on the circuit board for implementing BST. The devices can be placed inside the JTAG chain with other JTAG compliant devices. For those devices that have a JTAGen pin, it needs to be biased appropriately to permit JTAG and/or ISR operations. The next section of this application note discusses board connections for BST testing alone or BST testing with ISR programming.

The devices are classified into three different categories which are: single-function mode, dual-function operating in single-function mode and dual-function operating in du- al-function mode. These distinctions pertain to the use of the JTAG pins as dedicated JTAG pins or as I/O pins in the design. For the single-function devices the JTAG pins perform only the JTAG function and there is no I/O function also associated with the pin. For the dual-function devices the JTAG pins can function either as JTAG pins or as I/O pins. A du- al-function device operating in single-function mode means that the JTAG pins are configured to always take on their JTAG function. A dual-function device operating in dual-function mode means that the JTAG/IO pins are configured with external circuitry to behave as JTAG pins during JTAG operations as well as I/O pins under normal functional operations.

Cascading Single-Function Devices or Dual-Function Devices in Single-Function Mode

Figure 7 shows how to connect Ultra37000 devices that are either single-function devices or are dual-function mode devices operating in single-function mode. The dual-function mode devices have an extra pin called JTAGen whose function is to decode the JTAG or I/O function on the four du- al-function pins. This pin must be tied HIGH to permanently enable the JTAG function. Notice that the JTAG connections are identical to other JTAG devices with the only difference arising when dual-function devices are used and the JTAGen pin must be driven. For the purposes of simplicity, the JTAG chain is assumed small such that additional signal buffering on the board is not required.

Figure 7. JTAG Configuration w/o ISR—Single-Function Mode Operation

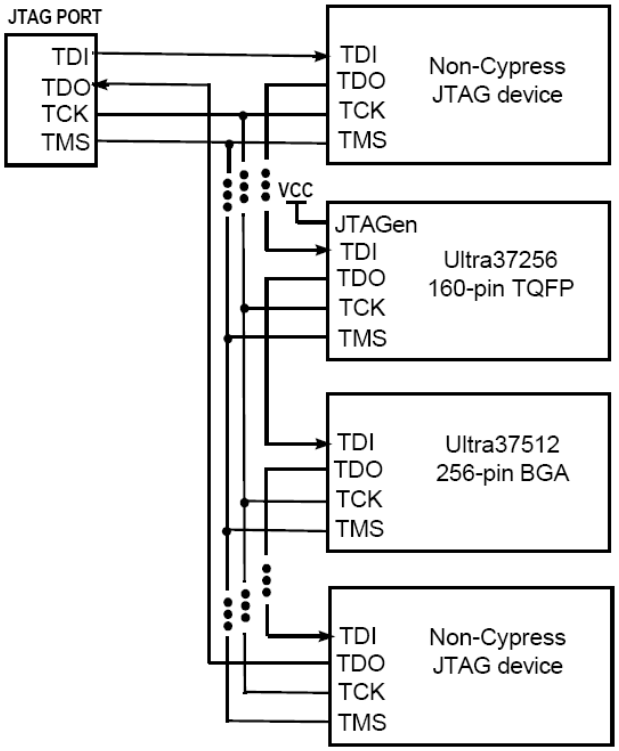
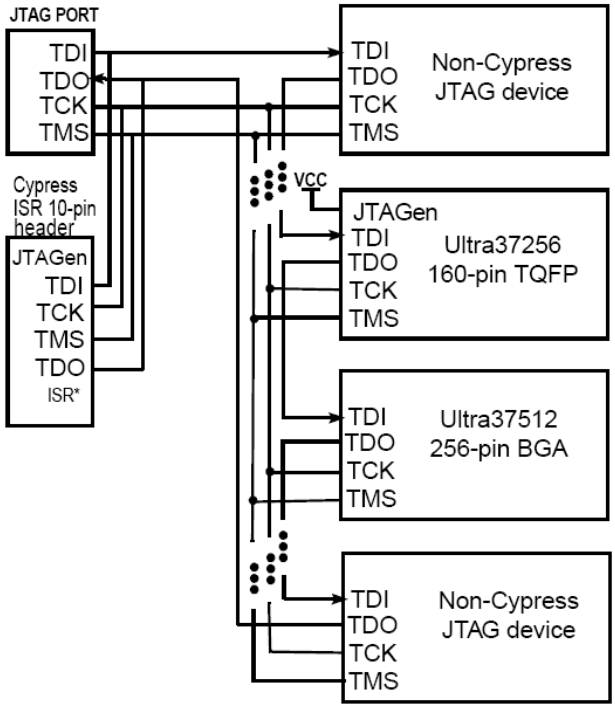


Figure 8. JTAG Configuration With ISR—Single-Function Mode Operation



Cascading Dual-Function ISR Devices in Dual-Function Mode

To use the dual-function mode devices in dual-function mode requires that a fifth JTAG pin be available to drive the JTAGen pin. This pin is driven HIGH when performing JTAG functions and LOW when the device is operating normally in the circuit board. The application note “Designing With Cypress In-System Reprogrammable CPLDs for PC Cable Programming” provides details showing the external circuitry needed to make use of the I/O pin on the dual-function pins. These techniques would need to be incorporated into Figure 7 if ISR is not going to be used or Figure 8 if ISR is going to be used in addition to BST. For those cases where this fifth pin is not available it is important to make sure the design does not use the I/O function on the dual-function pins. Refer to the application note “Designing With Cypress In-System Reprogrammable CPLDs for PC Cable Programming” to set your VHDL code to not use the I/O function on the dual-function pins.

Basic JTAG Connections With ISR Programming Connections

This next section of the application note explains how to connect the Ultra37000 CPLDs in the JTAG chain to perform ISR programming as well as JTAG operations such as BST.

Cascading Single-Function Devices or Dual-Function Devices in Single-Function Mode

Figure 8 shows two Ultra37000 devices in a typical JTAG chain with other non-Cypress devices. This figure shows the Cypress 10-pin header connector and connections from the four JTAG pins to the identical four JTAG pins coming from the other JTAG header on the circuit board. Since there is no standard JTAG connector, it is likely, but not required, that the connector used for performing BST will be different from the connector used for ISR. It is important to make sure that both the JTAG cable and the ISR cable are not plugged in at the same time. The buffers within the ISR cable are permanently enabled; therefore, a contention problem could exist if both cables are plugged in simultaneously. With larger JTAG chains, the user could add buffering on the circuit board which may still drive levels even when the JTAG cable is disconnected. It is therefore important that the connections from the 10-pin connector be made near the JTAG port connector such that there is no buffering in between the connectors. With this configuration all the non-Cypress devices would need to be specified in the set-up file for the ISR software GUI, with their respective instruction register lengths, to put the device into the Bypass mode.

Combining FLASH370i and Ultra37000 Devices in the JTAG Chain With ISR Programming

The FLASH370i family does not support Boundary Scan but the interface follows the JTAG 1149.1 specification with respect to the TAP controller, ISR programming, and the Bypass instruction. This feature enables placement of FLASH370i and Ultra37000 devices in the same JTAG chain to program all the Cypress devices and to perform BST on the Ultra37000 devices. The JTAGen pin of the ISR cable must be connected to the FLASH370i device to

program it. Additionally, during JTAG operations, the FLASH370i devices must be placed into the Bypass mode which requires the JTAGen pin to be forced externally to a TTL HIGH, provided the FLASH370i device is a single-function device. Dual-function devices are discussed later.

The solution shown in Figure 9 works by tying the JTAGen pin to VCC through a resistor. Once the ISR cable is removed the resistor pulls the JTAGen pin HIGH. It is important to remove the ISR cable before performing JTAG operations since it will drive the JTAGen pin LOW when ISR operations complete. The resistor pull-up will need to have a value small enough to overpower the bus-hold latch attached to the JTAGen pin. The value of this resistor must be 6.5 kohms or less to accomplish this task. For more information on the Cypress bus-hold feature see the application note “Understanding Bus-Hold—A Feature of Cypress CPLDs”. If more than one FLASH370i device is in the chain then the value of the resistor must be decreased or the user can place one 6.5 kohm resistor per device. If more than five FLASH370i devices are in the chain then an alternate approach to the resistor makes more sense since the low resistance begins to provide too high of a DC current load for the ISR cable. Figure 10 shows an alternate approach using external logic which must be able to withstand the high supervoltage of 12V from the ISR cable. This is easily achieved using a discrete general purpose NPN transistor (use a 2N3904-ND transistor or equivalent). The base of the transistor is driven by the ISR* signal through a 1 kohm resistor, to prevent overdriving the transistor. The collector is. connected to VCC and the emitter is connected to the JTAGen pin. During programming the ISR* signal drives LOW and turns off the transistor. During JTAG operations the ISR* signal turns the transistor on which drives the JTAGen pin to a TTL HIGH level. The CY7C374i-AC device can now be placed in the Bypass mode so JTAG operations can be performed on the other devices in the chain.

Figure 9. JTAG Configuration With ISR (Both FLASH370i

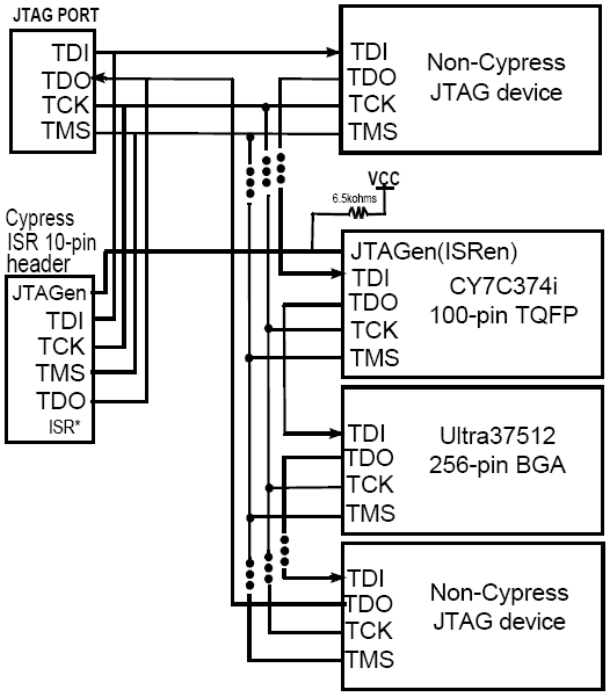
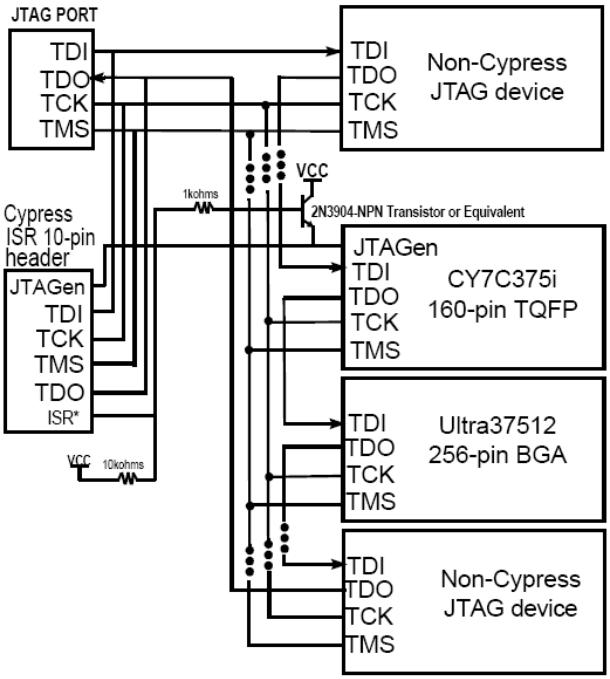


Figure 10. JTAG Configuration With ISR (Many FLASH370i Devices in the Chain)



For operating the dual-function FLASH370i devices in dual-function mode, the JTAGen pin must be driven to a supervoltage of 12.0V to enable the JTAG port. It is not recommended to connect the JTAGen pin to a static 12V level since the pin is not designed for this static high voltage condition and there may be a reliability concern on the JTAGen pin. Instead the 12V should be switched onto the pin when JTAG testing is initiated. This may be difficult

to implement since you will need an extra control signal from the JTAG port to control the switching. In this case an alternative to placing the device in the Bypass mode is recommended.

An alternative to placing the dual-function mode FLASH370i device in Bypass mode is to put it in transparent mode. This involves programming the TDI/IO pin as a functional input and the TDO/IO pin as a functional output such that TDO is a combinatorial function of TDI with simply a propagation delay between the two pins. In this way the dual-function device can be put into the JTAG chain, programmed via ISR, and function as a simple delay path when doing normal JTAG functions. Effectively the device has been put into Bypass mode except there is no register bit placed between the TDI and TDO as occurs in Bypass mode. When describing the JTAG chain the FLASH370i part is left out of the chain description. The application note “Cascading ISR Devices” explains in more detail how to program the transparent mode in VHDL. The du- al-function device can now be treated as a single-function device with respect to bias conditions on the JTAGen pin. Therefore either Figure 8 or Figure 9 can be used to connect the devices in the JTAG chain.

Conclusion

The JTAG circuitry in the Ultra37000 family provides a cost-effective IEEE1149.1-compliant way of testing systems that have become too complex for a traditional bed of nails approach. These devices can be used with other IEEE 1149.1-compliant devices for board-level interconnect testing. This application note provides background information on the IEEE 1149.1 standard, specifics of its implementation in the Ultra37000 family, and specifics of board connections required to perform boundary scan and ISR programming operations.

References

1. IEEE Std 1149.1-1990 Test Access Port and Boundary Scan Architecture, IEEE Computer Society, May 1990.
2. IEEE Std 1149.1b-1994 Supplement to IEEE Std 1149.1-1990 Test Access Port and Boundary Scan Architecture which Specifies the BSDL language.
3. Parker Kenneth P., The Boundary Scan Handbook. Kluwer Academic Publishers.
4. C. M. Maunder & R. E. Tulloss, “An Introduction to the Boundary Scan Standard,” Journal of Electronic Testing and Applications, 1991.

Cypress Semiconductor
198 Champion Court
San Jose, CA 95134-1709
Phone: 408-943-2600
Fax: 408-943-4730
http://www.cypress.com/