CD40107BMS

December 1992

CMOS Dual 2 Input NAND Buffer/Driver

Features

- **High Voltage Type (20V Rating)**
- **32 Times Standard B Series Output Current Drive Sinking Capability**
  - **136mA Typ. at VDD = 10V**
  - **VDS = 1V**
- **100% Tested for Quiescent Current at 20V**
- **5V, 10V and 15V Parametric Ratings**
- **Maximum Input Current of 1μA at 18V Over Full Package Temperature Range; 100nA at 18V and +25°C**
- **Noise Margin (Over Full Package/Temperature Range) RL to VDD = 10kΩ**
  - **1V at VDD = 5V**
  - **2V at VDD = 10V**
  - **2.5V at VDD = 15V**
- **Meets All Requirements of JEDEC Tentative Standard No. 13B, "Standard Specifications for Description of 'B' Series CMOS Devices"**

Applications

- **Driving Relays, Lamps, LEDs**
- **Line Driver**
- **Level Shifter (Up or Down)**

Description

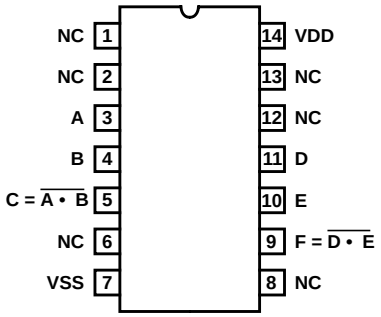
CD40107BMS is a dual 2 input NAND buffer/driver containing two independent 2 input NAND buffers with open drain single n-channel transistor outputs. This device features a wired OR capability and high output sink current capability (136mA typ. at VDD = 10V, VDS = 1V).

The CD40107BMS is supplied in these 14 lead outline packages:

Braze Seal DIP	H4H
Frit Seal DIP	H1B
Ceramic Flatpack	H3W

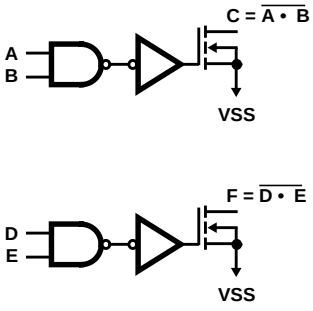
Pinouts

CD40107BF
TOP VIEW



NC = NO CONNECTION

Functional Diagram



Absolute Maximum Ratings

DC Supply Voltage Range, (VDD) . . . . . -0.5V to +20V
(Voltage Referenced to VSS Terminals)
Input Voltage Range, All Inputs . . . . . -0.5V to VDD +0.5V
DC Input Current, Any One Input . . . . . ±10mA
Operating Temperature Range . . . . . -55°C to +125°C
Package Types D, F, K, H
Storage Temperature Range (TSTG) . . . . . -65°C to +150°C
Lead Temperature (During Soldering) . . . . . +265°C
At Distance 1/16 ± 1/32 Inch (1.59mm ± 0.79mm) from case for 10s Maximum

Reliability Information

Thermal Resistance	θ_{ja}	θ_{jc}
Ceramic DIP and FRIT Package	80°C/W	20°C/W
Flatpack Package	70°C/W	20°C/W

Maximum Package Power Dissipation (PD) at +125°C
For T_A = -55°C to +100°C (Package Type D, F, K) 500mW
For T_A = +100°C to +125°C (Package Type D, F, K). . . . . Derate Linearity at 12mW/°C to 200mW
Device Dissipation per Output Transistor 100mW
For T_A = Full Package Temperature Range (All Package Types)
Junction Temperature . . . . . +175°C

TABLE 1. DC ELECTRICAL PERFORMANCE CHARACTERISTICS

PARAMETER	SYMBOL	CONDITIONS (NOTE 1)		GROUP A SUBGROUPS	TEMPERATURE	LIMITS MIN	LIMITS MAX	UNITS
Supply Current	IDD	VDD = 20V, VIN = VDD or GND		1	+25°C	-	2	µA
				2	+125°C	-	200	µA
		VDD = 18V, VIN = VDD or GND		3	-55°C	-	2	µA
Input Leakage Current	IIL	VIN = VDD or GND	VDD = 20	1	+25°C	-100	-	nA
				2	+125°C	-1000	-	nA
			VDD = 18V	3	-55°C	-100	-	nA
Input Leakage Current	IIH	VIN = VDD or GND	VDD = 20	1	+25°C	-	100	nA
				2	+125°C	-	1000	nA
			VDD = 18V	3	-55°C	-	100	nA
Output Drive Voltage	VOL5A	VDD = 5V, IOL = 16mA		1	+25°C	-	0.4	V
Output Drive Voltage	VOL5B	VDD = 5V, IOL = 34mA		1	+25°C	-	1.0	V
	VOL10A	VDD = 10V, IOL = 37mA		1	+25°C	-	0.5	V
Output Drive Voltage	VOL10B	VDD = 10V, IOL = 68mA		1	+25°C	-	1.0	V
	VOL15	VDD = 15V, IOL = 50mA		1	+25°C	-	0.5	V
Output Current (Source)	IOH5A	No Internal Pull-Up Device						
Output Current (Source)	IOH5B							
Output Current (Source)	IOH10							
Output Current (Source)	IOH15							
N Threshold Voltage	VNTH	VDD = 10V, ISS = -10µA		1	+25°C	-2.8	-0.7	V
P Threshold Voltage	VPTH	VSS = 0V, IDD = 10µA		1	+25°C	0.7	2.8	V
Functional (Note 3)	F	VDD = 2.8V, VIN = VDD or GND		7	+25°C	VOH > VDD/2	VOL < VDD/2	V
		VDD = 20V, VIN = VDD or GND		7	+25°C			
		VDD = 18V, VIN = VDD or GND		8A	+125°C			
		VDD = 3V, VIN = VDD or GND		8B	-55°C			
Input Voltage Low (Note 2, 3)	VIL	VDD = 5V, VOH > 4.5V, VOL < 0.5V		1, 2, 3	+25°C, +125°C, -55°C	-	1.5	V
Input Voltage High (Note 2, 3)	VIH	VDD = 5V, VOH > 4.5V, VOL < 0.5V		1, 2, 3	+25°C, +125°C, -55°C	3.5	-	V
Input Voltage Low (Note 2, 3)	VIL	VDD = 15V, VOH > 13.5V, VOL < 1.5V		1, 2, 3	+25°C, +125°C, -55°C	-	4	V
Input Voltage High (Note 2, 3)	VIH	VDD = 15V, VOH > 13.5V, VOL < 1.5V		1, 2, 3	+25°C, +125°C, -55°C	11	-	V
Tri-State Output Leakage High	IOZ	VIN = VDD or GND VOUT = VDD	VDD = 20V	1	+25°C	-	2	µA
				2	+125°C	-	20	µA
			VDD = 18V	3	-55°C	-	2	µA

NOTES: 1. All voltages referenced to device GND, 100% testing being implemented.
2. Go/No Go test with limits applied to inputs.
3. For accuracy, voltage is measured differentially to VDD. Limit is 0.050V max.

TABLE 2. AC ELECTRICAL PERFORMANCE CHARACTERISTICS

PARAMETER	SYMBOL	CONDITIONS (NOTE 1, 2)	GROUP A SUBGROUPS	TEMPERATURE	LIMITS		UNITS
					MIN	MAX	
Propagation Delay	TPHL TPLH	VDD = 5V, VIN = VDD or GND	9	+25°C	-	200	ns
			10, 11	+125°C, -55°C	-	270	ns
Transition Time	TTHL TTLH	VDD = 5V, VIN = VDD or GND	9	+25°C	-	100	ns
			10, 11	+125°C, -55°C	-	135	ns

NOTES:

1. CL = 50pF, RL = 120Ω, Input TR, TF < 20ns.
2. -55°C and +125°C limits guaranteed, 100% testing being implemented.

TABLE 3. ELECTRICAL PERFORMANCE CHARACTERISTICS

PARAMETER	SYMBOL	CONDITIONS	NOTES	TEMPERATURE	LIMITS		UNITS
					MIN	MAX	
Supply Current	IDD	VDD = 5V, VIN = VDD or GND	1, 2	-55°C, +25°C	-	1	µA
				+125°C	-	30	µA
		VDD = 10V, VIN = VDD or GND	1, 2	-55°C, +25°C	-	2	µA
				+125°C	-	60	µA
		VDD = 15V, VIN = VDD or GND	1, 2	-55°C, +25°C	-	2	µA
				+125°C	-	120	µA
Output Voltage	VOL	VDD = 5V, No Load	1, 2	+25°C, +125°C, -55°C	-	50	mV
Output Voltage	VOL	VDD = 10V, No Load	1, 2	+25°C, +125°C, -55°C	-	50	mV
Output Voltage (Note 5)	VOH	VDD = 5V, No Load	1, 2	+25°C, +125°C, -55°C	4.95	-	V
Output Voltage (Note 5)	VOH	VDD = 10V, No Load	1, 2	+25°C, +125°C, -55°C	9.95	-	V
Output Current (Sink)	IOL5A	VDD = 5.0V, VOUT = 0.4V	1, 2	+125°C	12	-	mA
				-55°C	21	-	mA
Output Current (Sink)	IOL5B	VDD = 5V, VOUT = 1.0V	1, 2, 4	+125°C	25	-	mA
				-55°C	44	-	mA
Output Current (Sink)	IOL10A	VDD = 10V, VOUT = 0.5V	1, 2, 4	+125°C	28	-	mA
				-55°C	49	-	mA
Output Current (Sink)	IOL10B	VDD = 10V, VOUT = 1V	1, 2, 4	+125°C	51	-	mA
				-55°C	89	-	mA
Output Current (Sink)	IOL15	VDD = 15V, VOUT = 0.5V	1, 2	+125°C	38	-	mA
				-55°C	66	-	mA
Input Voltage Low	VIL	VDD = 10V, VOH > 9V, VOL < 1V	1, 2, 4	+25°C, +125°C, -55°C	-	3	V
Input Voltage High	VIH	VDD = 10V, VOH > 9V, VOL < 1V	1, 2, 4	+25°C, +125°C, -55°C	+7	-	V

TABLE 3. ELECTRICAL PERFORMANCE CHARACTERISTICS (Continued)

PARAMETER	SYMBOL	CONDITIONS	NOTES	TEMPERATURE	LIMITS		UNITS
					MIN	MAX	
Propagation Delay	TPHL	VDD = 10V	1, 2, 3	+25°C	-	90	ns
		VDD = 15V	1, 2, 3	+25°C	-	60	ns
Propagation Delay	TPLH	VDD = 10V	1, 2, 3	+25°C	-	120	ns
		VDD = 15V	1, 2, 3	+25°C	-	100	ns
Transition Time	TTHL	VDD = 10V	1, 2, 3	+25°C	-	40	ns
		VDD = 15V	1, 2, 3	+25°C	-	20	ns
Transition Time	TTLH	VDD = 10V	1, 2, 3	+25°C	-	70	ns
		VDD = 15V	1, 2, 3	+25°C	-	50	ns
Input Capacitance	CIN	Any Input	1, 2	+25°C	-	7.5	pF

NOTES:

1. All voltages referenced to device GND.
2. The parameters listed on Table 3 are controlled via design or process and are not directly tested. These parameters are characterized on initial design release and upon design changes which would affect these characteristics.
3. CL = 50pF, RL = 120Ω, pull up resistor to VDD, Input TR, TF < 20ns.
4. Measured with external pull-up resistor RL = 10K to VDD

TABLE 4. POST IRRADIATION ELECTRICAL PERFORMANCE CHARACTERISTICS

PARAMETER	SYMBOL	CONDITIONS	NOTES	TEMPERATURE	LIMITS		UNITS
					MIN	MAX	
Supply Current	IDD	VDD = 20V, VIN = VDD or GND	1, 4	+25°C	-	7.5	µA
N Threshold Voltage	VNTH	VDD = 10V, ISS = -10µA	1, 4	+25°C	-2.8	-0.2	V
N Threshold Voltage Delta	ΔVTN	VDD = 10V, ISS = -10µA	1, 4	+25°C	-	±1	V
P Threshold Voltage	VTP	VSS = 0V, IDD = 10µA	1, 4	+25°C	0.2	2.8	V
P Threshold Voltage Delta	ΔVTP	VSS = 0V, IDD = 10µA	1, 4	+25°C	-	±1	V
Functional	F	VDD = 18V, VIN = VDD or GND	1, 5	+25°C	VOH > VDD/2	VOL < VDD/2	V
		VDD = 3V, VIN = VDD or GND					
Propagation Delay Time	TPHL TPLH	VDD = 5V	1, 2, 3, 4	+25°C	-	1.35 x +25°C Limit	ns

NOTES:

1. All voltages referenced to device GND.
2. CL = 50pF, RL = 120Ω, pull up resistor to VDD, Input TR, TF < 20ns.
3. See Table 2 for +25°C limit.
4. Read and Record
5. Measured with external pull-up resistor RL = 10K to VDD

TABLE 5. BURN-IN AND LIFE TEST DELTA PARAMETERS +25°C

PARAMETER	SYMBOL	DELTA LIMIT
Supply Current - MSI-1	IDD	± 0.2µA

TABLE 5. BURN-IN AND LIFE TEST DELTA PARAMETERS +25°C

PARAMETER	SYMBOL	DELTA LIMIT
Output Current (Sink)	IOL5	± 20% x Pre-Test Reading
Output Current (Source)	IOH5A	± 20% x Pre-Test Reading

TABLE 6. APPLICABLE SUBGROUPS

CONFORMANCE GROUP		MIL-STD-883 METHOD	GROUP A SUBGROUPS	READ AND RECORD
Initial Test (Pre Burn-In)		100% 5004	1, 7, 9	IDD, IOL5, IOH5A
Interim Test 1 (Post Burn-In)		100% 5004	1, 7, 9	IDD, IOL5, IOH5A
Interim Test 2 (Post Burn-In)		100% 5004	1, 7, 9	IDD, IOL5, IOH5A
PDA (Note 1)		100% 5004	1, 7, 9, Deltas	
Interim Test 3 (Post Burn-In)		100% 5004	1, 7, 9	IDD, IOL5, IOH5A
PDA (Note 1)		100% 5004	1, 7, 9, Deltas	
Final Test		100% 5004	2, 3, 8A, 8B, 10, 11	
Group A		Sample 5005	1, 2, 3, 7, 8A, 8B, 9, 10, 11	
Group B	Subgroup B-5	Sample 5005	1, 2, 3, 7, 8A, 8B, 9, 10, 11, Deltas	Subgroups 1, 2, 3, 9, 10, 11
	Subgroup B-6	Sample 5005	1, 7, 9	
Group D		Sample 5005	1, 2, 3, 8A, 8B, 9	Subgroups 1, 2 3

NOTE: 1. 5% Parameteric, 3% Functional; Cumulative for Static 1 and 2.

TABLE 7. TOTAL DOSE IRRADIATION

CONFORMANCE GROUPS	MIL-STD-883 METHOD	TEST		READ AND RECORD	
		PRE-IRRAD	POST-IRRAD	PRE-IRRAD	POST-IRRAD
Group E Subgroup 2	5005	1, 7, 9	Table 4	1, 9	Table 4

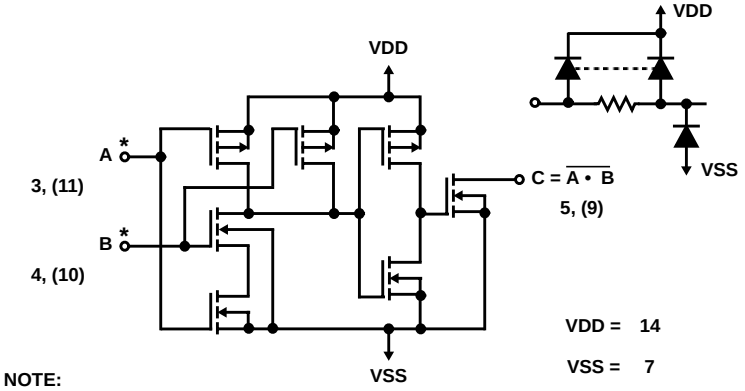
TABLE 8. BURN-IN AND IRRADIATION TEST CONNECTIONS

FUNCTION	OPEN	GROUND	VDD	9V ± -0.5V	OSCILLATOR	
					50kHz	25kHz
Static Burn-In 1 (Note 1)	1, 2, 5, 6, 8, 9, 12, 13	3, 4, 7, 10, 11	14			
Static Burn-In 2 (Note 1)	1, 2, 5, 6, 8, 9, 12, 13	7	3, 4, 10, 11, 14			
Dynamic Burn-In (Note 3)	1, 2, 6, 8, 12, 13	7	14	5, 9	-	3, 4, 10, 11
Irradiation (Note 2)	1, 2, 5, 6, 8, 9, 12, 13	7	3, 4, 10, 11, 14			

NOTE:

1. Each pin except VDD and GND will have a series resistor of 10K ± 5%, VDD = 18V ± 0.5V
2. Each pin except VDD and GND will have a series resistor of 47K ± 5%; Group E, Subgroup 2, sample size is 4 dice/wafer, 0 failures, VDD = 10V ± 0.5V
3. Each pin except VDD and GND will have a series resistor of 4.75K ±5%, VDD = 18V ±.5.

Schematic



* ALL INPUTS ARE PROTECTED BY CMOS PROTECTION NETWORK

TRUTH TABLE

A	B	C	
0	0	1*	Z**
1	0	1*	Z**
0	1	1*	Z**
1	1	0	

* Requires external pull-up resistor (RL) to VDD.

** Without pull-up resistor (3-state).

FIGURE 1. 1 OF 2 GATES

Typical Performance Characteristics

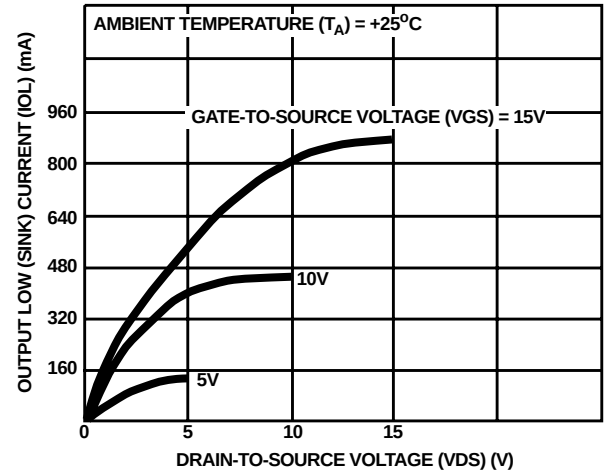


FIGURE 2. TYPICAL OUTPUT LOW (SINK) CURRENT CHARACTERISTICS

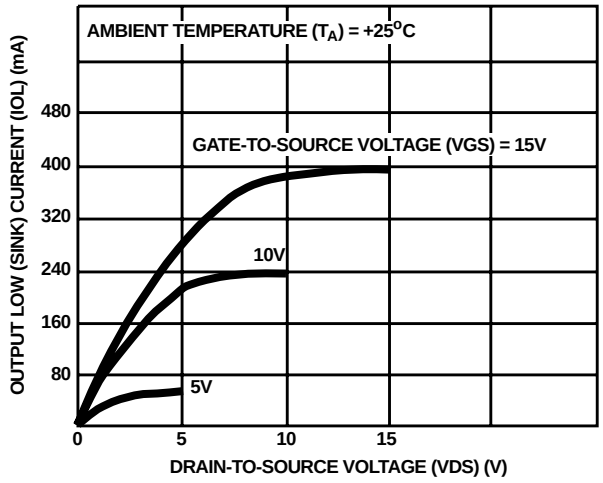


FIGURE 3. MINIMUM OUTPUT LOW (SINK) CURRENT CHARACTERISTICS

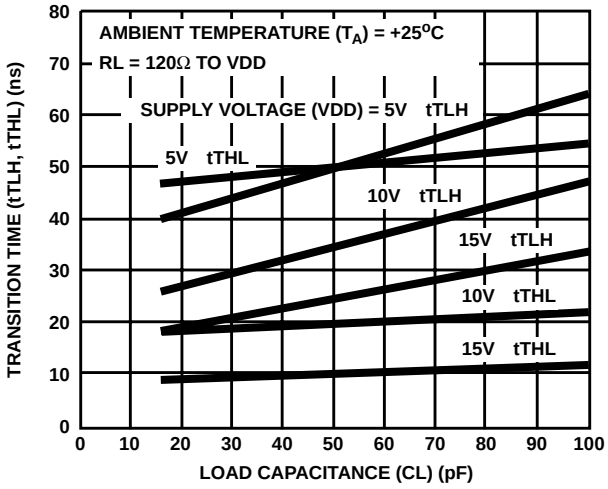


FIGURE 4. TYPICAL TRANSITION TIME AS A FUNCTION OF LOAD CAPACITANCE

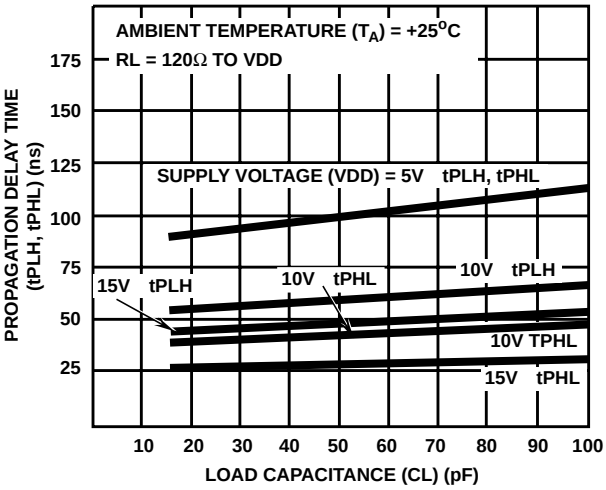


FIGURE 5. TYPICAL PROPAGATION DELAY TIME AS A FUNCTION OF LOAD CAPACITANCE

Typical Performance Characteristics (Continued)

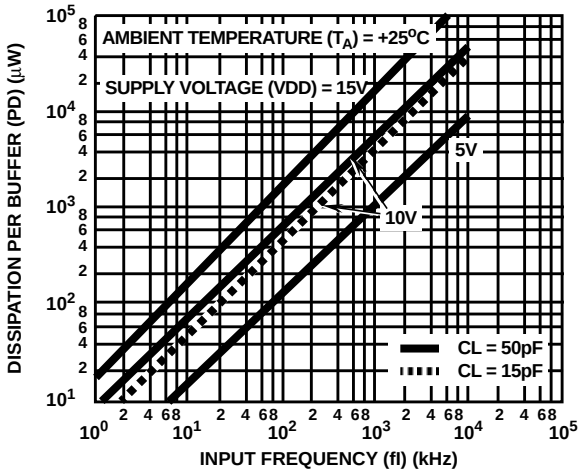
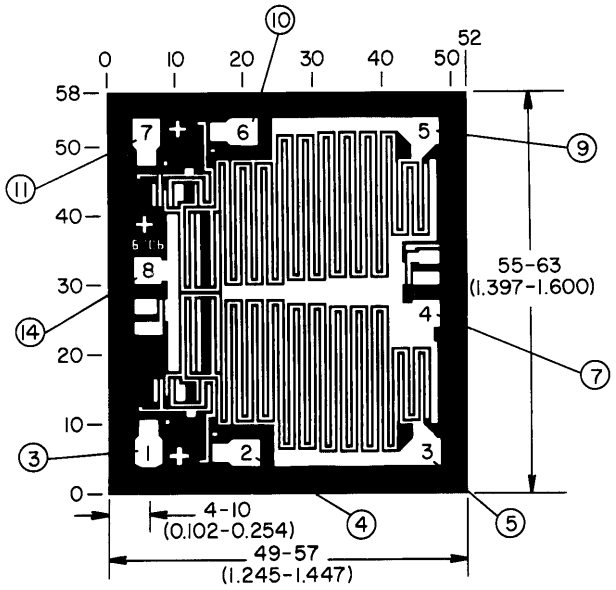


FIGURE 6. TYPICAL POWER DISSIPATION AS A FUNCTION OF INPUT FREQUENCY

Chip Dimensions and Pad Layout



NOTE:
Numbers inside pads for CD40107BE not offered as standard part.
Numbers outside chip are for CD40107BF

Dimensions in parenthesis are in millimeters and are derived from the basic inch dimensions as indicated. Grid graduations are in mils (10^{-3} inch).

METALLIZATION: Thickness: 11kÅ – 14kÅ, AL.

PASSIVATION: 10.4kÅ - 15.6kÅ, Silane

BOND PADS: 0.004 inches X 0.004 inches MIN

DIE THICKNESS: 0.0198 inches - 0.0218 inches

Special Considerations

Limiting Capacitive Currents for CL > 500pF, VDD > 15V

For VDD > 15V, and load capacitance (CL) from output to ground > 500pF, an external 25Ω series limiting resistor should be inserted between the output terminal and CL. No external resistor is necessary if CL < 500pF or VDD < 15V.

Driving Inductive Loads

When using the CD40107BMS to drive inductive loads, the load should be shunted with a diode to prevent high voltages from developing across the CD40107BMS output.