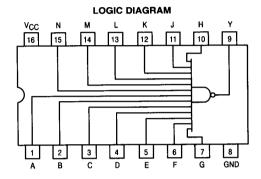
13-Input NAND Gate

ELECTRICALLY TESTED PER: MPG54LS133



TRUTH TABLE													
Inputs										Output			
Α	В	С	D	Е	F	G	Н	J	K	L	М	z	Y
	L	L	L	L	L	L	L	L	L	L	L	I	Н
lι	L	L	L	L	L	L	L	L	L	L	Н	L	н
L	L	L	L	L	L	L	L	L	L	Н	L	L	н
lι	L	L	L	L	L	L	L	L	Н	L	L	L	Н
L	L	L	L	L	L	L	L	Н	L	L	L	L	Н
L	L	L	L	L	L	L	Н	L	L	L	L	L	н
L	L	L	L	L	L	Н	L	L	L	L	L	L	н
L	L	L	L	L	Н	L	L	L	L	L	L	L	Н
L	L	L	L	Н	L	L	L	L	L	L	L	L	Н
L	L	L	Н	L	L	L	L	L	L	L	L	L	н
L	L	Н	L	L	L	L	Ł	L	L	L	L	L	н
اد	Н	L	L	L	L	L	L	L	L	L	L	L	∖ н
Н	L	Ĺ	L	L	L	L	L	L	L	L	L	L	H
L	Ĺ	Ĺ	L	L	L	L	L	L	L	L	L	L	L
ΙĀ	н	н	н	н	н	н	н	н	н	н	н	н	н

Military 54LS133



AVAILABLE AS:

1) JAN: N/A 2) SMD: N/A 3) 883: 54LS133/BXAJC

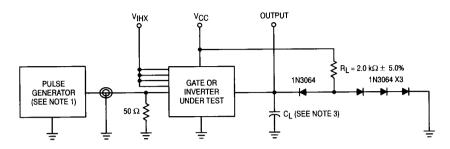
X = CASE OUTLINE AS FOLLOWS: PACKAGE: CERDIP: E CERFLAT: F LCC: 2

THE LETTER "M" APPEARS BEFORE THE / ON LCC.

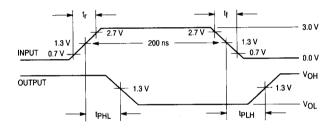
PIN ASSIGNMENTS									
FUNCT.	DIL 620-09	FLATS 650-05	LCC 756A-02	BURN-IN (COND. A)					
Α	1	1	2	GND					
В	2	2	3	VCC					
С	3	3	4	VCC					
D	4	4	5	VCC					
Ε	5	5	7	Vcc					
F	6	6	8	VCC					
G	7	7	9	VCC					
GND	8	8	10	GND					
Υ	9	9	12	Vcc					
Н	10	10	13	Vcc					
J	11	11	14	vcc					
К	12	12	15	VCC					
L	13	13	17	VCC					
М	14	14	18	Vcc					
N	15	15	19	GND					
Vcc	16	16	20	v _{CC}					
BURN-IN CONDITIONS: V _{CC} = 5.0 V MIN/6.0 V MAX									

54LS133

AC TEST CIRCUIT



WAVEFORMS



NOTES:

- 1. Pulse generator has the following characteristics: $t_f \le$ 15 ns, $t_f \le$ 6.0 ns, PRR \le 1.0 MHz, duty cycle = 50% and $Z_{OUT} \approx$ 50 Ω .
- 2. Inputs not under test are at 2.7 V.
- 3. C_L = 50 pF \pm 10%, including scope probe, wiring and stray capacitance.
- 4. $R_1 = 2.0 \text{ k}\Omega \pm 5.0\%$.
- Voltage measurements are to be made with respect to network ground terminal.

54LS133

Symbol	Parameter	Limits						Unit	Test Condition (Unless Otherwise Specified)
		+ 25°C Subgroup 1		+ 125°C Subgroup 2		– 55°C Subgroup 3			
	Static Parameters:								
	T arametere.	Min	Max	Min	Max	Min	Max		
Vон	Logical "1" Output Voltage	2.5		2.5		2.5		٧	$\begin{split} &V_{CC} = 4.5 \text{ V, } I_{OH} = -400 \mu\text{A,} \\ &V_{IL} = 0.7 \text{ V, } V_{IN} = 2.0 \text{ V on other inputs.} \end{split}$
VoL	Logical "0" Output Voltage		0.4		0.4		0.4	٧	V _{CC} = 4.5 V, I _{OL} = 4.0 mA, V _{IH} = 2.0 V on both inputs.
V _{IC}	Input Clamping Voltage		-1.5					٧	V _{CC} = 4.5 V, I _{IN} = -18 mA, other inputs are open.
liн	Logical "1" Input Current		20		20		20	μА	V _{CC} = 5.5 V, V _{IH} = 2.7 V, other inputs = GND.
Iнн Інн	Logical "1" Input Current		100		100		100	μА	V _{CC} = 5.5 V, V _{IHH} = 7.0 V, other inputs = GND.
ΊL	Logical "0" Input Current		-0.4		-0.4		-0.4	mA	$V_{CC} = 5.5 \text{ V}, V_{IL} = 0.4 \text{ V},$ other inputs = 4.5 V.
los	Output Short Circuit Current	-20	-100	-20	-100	-20	-100	mA	V_{CC} = 5.5 V, V_{IN} = GND (all inputs), V_{OUT} = GND.
Іссн	Power Supply Current		0.5		0.5		0.5	mA	V _{CC} = 5.5 V, V _{IN} = GND (all inputs).
ICCL	Power Supply Current		1.1		1.1		1.1	mA	$V_{CC} = 5.5 \text{ V}, V_{IN} = 4.5 \text{ V} \text{ (all inputs)}.$
VIH	Logical "1" Input Voltage	2.0		2.0		2.0		٧	V _{CC} = 4.5 V.
VIL	Logical "0" input Voltage		0.7		0.7		0.7	٧	V _{CC} = 4.5 V.
		Subg	Subgroup 7		Subgroup 8A		Subgroup 8B		
	Functional Tests								per Truth Table with $V_{CC} = 5.0 \text{ V}$, $V_{INL} = 0.4 \text{ V}$, and $V_{INH} = 2.5 \text{ V}$.

Symbol	Parameter	Limits							Test Condition (Unless Otherwise Specified)
		+ 25°C Subgroup 9		+ 125°C Subgroup 10		– 55°C Subgroup 11			
	Switching Parameters:)	
	Parameters.	Min	Max	Min	Max	Min	Max		
PHL PHL	Propagation Delay /Data-Output Output High-Low		70 59		80 74		80 74	ns	$V_{CC} = 5.0 \text{ V}, C_L = 50 \text{ pF}, R_L = 2.0 \text{ k}\Omega.$ $V_{CC} = 5.0 \text{ V}, C_L = 15 \text{ pF}.$
tPLH tPLH	Propagation Delay /Data-Output Output Low-High		20 15		30 19		30 19	ns	$V_{CC} = 5.0 \text{ V}, C_L = 50 \text{ pF}, R_L = 2.0 \text{ k}\Omega.$ $V_{CC} = 5.0 \text{ V}, C_L = 15 \text{ pF}.$

NOTE:

^{1.} The limits specified for C_L = 15 pF are guaranteed but not tested.