CD4045B Types

CMOS 21-Stage Counter

High-Voltage Types (20-Volt Rating)

■ CD4045B is a timing circuit consisting of 21 counter stages, two output-shaping flip-flops, two inverter output drivers, and input inverters for use in a crystal oscillator. The CD4045B configuration provides 21 flip-flop counting stages, and two flip-flops for shaping the output waveform for a 3.125% duty cycle. Push-pull operation is provided by the inverter output drivers.

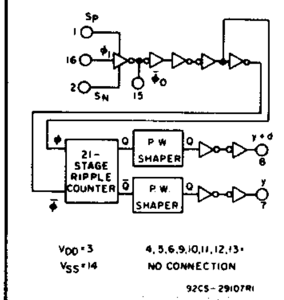
The first inverter is intended for use as a crystal oscillator/amplifier. However, it may be used as a normal logic inverter if desired. A crystal oscillator circuit can be made less sensitive to voltage-supply variations by the use of source resistors. In this device, the sources of the p and n transistors have been brought out to package terminals. If external resistors are not required, the sources must be shorted to their respective substrates (S_p to V_{DD}, S_n to V_{SS}). See Fig. 1. The first inverter in conjunction with an outboard inverter, such as 1/6 CD4069, and R_X, C_X, and R_S can also be used to construct an RC oscillator. The following data is supplied as a guide in the selection of values for R_X, R_S, and C_X used in Fig. 11:

1. R_X max = 10 MΩ with R_S = 10 MΩ and C_X = 50 pF
2. C_X max = 25 µF with R_S = 560 kΩ and R_X = 50 kΩ

The CD4045B types are supplied in 16-lead dual-in-line plastic packages (E suffix), 16-lead small-outline package (NSR suffix), and 16-lead thin shrink small-outline packages (PW and PWR suffixes).

Features:

- **Very low operating dissipation . . . . . <1 mW (typ.) @ V_{DD} = 5 V, fφ = 1 MHz**
- **Output drivers with sink or source capability . . . . . 7 mA (typ.) @ V_{DD} = 5 V**
- **Medium speed (typ.) . . . fφ = 25 MHz @ V_{DD} = 10 V**
- **100% tested for quiescent current at 20 V**
- **5-V, 10-V, and 15-V parametric ratings**
- **Meets all requirements of JEDEC Tentative Standard No. 13B, Standard Specifications for Descripiton of 'B' Series CMOS Devices"**



FUNCTIONAL DIAGRAM

Applications:

- **Digital equipment in which ultra-low dissipation and/or operation using a battery source is required.**
- **Accurate timing from a crystal oscillator for timing applications such as wall clocks, table clocks, automobile clocks, and digital timing references in any circuit requiring accurately timed outputs at various intervals in the counting sequence.**
- **Driving miniature synchronous motors, stepping motors, or external bipolar transistors in push-pull fashion.**

MAXIMUM RATINGS, ***Absolute-Maximum Values:***

DC SUPPLY-VOLTAGE RANGE, (V_{DD})	
Voltages referenced to V_{SS} Terminal)	−0.5V to +20V
INPUT VOLTAGE RANGE, ALL INPUTS	−0.5V to V_{DD} +0.5V
DC INPUT CURRENT, ANY ONE INPUT	±10mA
POWER DISSIPATION PER PACKAGE (P_D):	
For T_A = −55°C to +100°C	500mW
For T_A = +100°C to +125°C	Derate Linearity at 12mW/°C to 200mW
DEVICE DISSIPATION PER OUTPUT TRANSISTOR	
FOR T_A = FULL PACKAGE-TEMPERATURE RANGE (All Package Types)	100mW
OPERATING-TEMPERATURE RANGE (T_A)	−55°C to +125°C
STORAGE TEMPERATURE RANGE (T_{stg})	−65°C to +150°C
LEAD TEMPERATURE (DURING SOLDERING):	
At distance 1/16 ± 1/32 inch (1.59 ± 0.79mm) from case for 10s max	+265°C

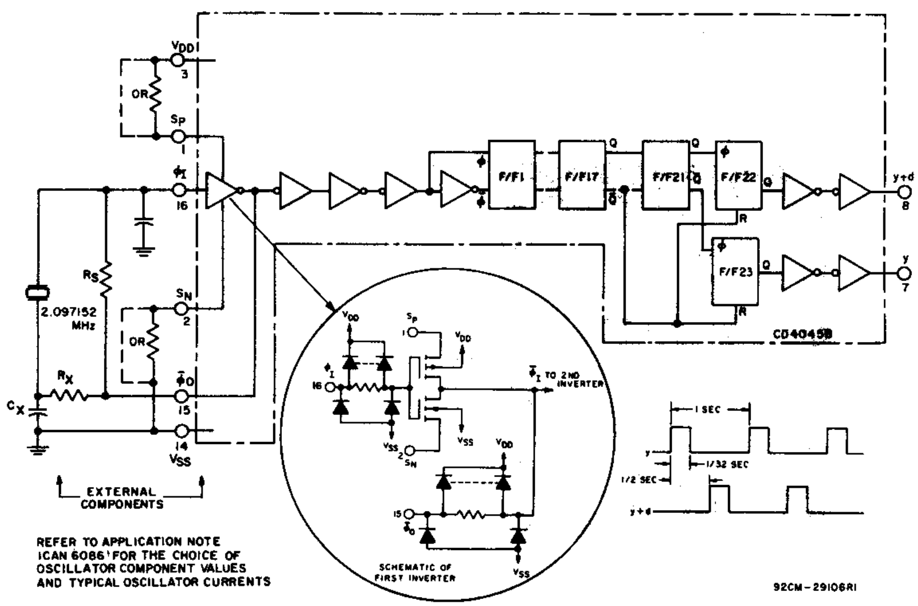


Fig. 1 – CD4045B and outboard components in a typical 21-stage counter application.

STATIC ELECTRICAL CHARACTERISTICS

CHARACTERISTIC	CONDITIONS V_O (V)	V_{IN} (V)	V_{DD} (V)	LIMITS AT INDICATED TEMPERATURES (°C) −55	−40	+85	+125	+25 Min.	+25 Typ.	+25 Max.	UNITS
Quiescent Device Current, I_{DD} Max.	–	0,5	5	5	5	150	150	–	0.04	5	µA
	–	0,10	10	10	10	300	300	–	0.04	10	µA
	–	0,15	15	20	20	600	600	–	0.04	20	µA
	–	0,20	20	100	100	3000	3000	–	0.08	100	µA
Output Low (Sink) Current I_{OL} Min.	0.4	0,5	5	4.5	4.3	2.9	2.5	3.6	7	–	mA
	0.5	0,10	10	11.2	10.5	7.7	6.3	9.1	18	–	mA
	1.5	0,15	15	29.4	28	19.6	16.8	23.8	47	–	mA
Output High (Source) Current, I_{OH} Min.	4.6	0,5	5	−4.5	−4.3	−2.9	−2.5	−3.6	−7	–	mA
	9.5	0,10	10	−11.2	−10.5	−7.7	−6.3	−9.1	−18	–	mA
	13.5	0,15	15	−29.4	−28	−19.6	−16.8	−23.8	−47	–	mA
Pin 15 Output Low and High Current, I_{OL}, I_{OH}	0.4,4.6	0,5	5	–				±0.1	±0.18	–	mA
	0.5,9.5	0,10	10	–				±0.2	±0.3	–	mA
	1.5,13.5	0,15	15	–				±0.5	±1	–	mA
Output Voltage: Low-Level, V_{OL} Max.	–	0,5	5	0.05				–	–	0.05	V
	–	0,10	10	0.05				–	–	0.05	V
	–	0,15	15	0.05				–	–	0.05	V
Output Voltage: High-Level, V_{OH} Min.	–	0,5	5	4.95				4.95	5	–	V
	–	0,10	10	9.95				9.95	10	–	V
	–	0,15	15	14.95				14.95	15	–	V
Input Low Voltage V_{IL} Max.	0.5,4.5	–	5	1.5				–	–	1.5	V
	1,9	–	10	3				–	–	3	V
	1.5,13.5	–	15	4				–	–	4	V
Input High Voltage, V_{IH} Min.	0.5,4.5	–	5	3.5				3.5	–	–	V
	1,9	–	10	7				7	–	–	V
	1.5,13.5	–	15	11				11	–	–	V
Input Current I_{IN} Max.	–	0,18	18	±0.1	±0.1	±1	±1	–	$\pm10^{-5}$	±0.1	µA

RECOMMENDED OPERATING CONDITIONS

For maximum reliability, nominal operating conditions should be selected so that operation is always within the following ranges

CHARACTERISTIC	V_{DD} (V)	LIMITS Min.	LIMITS Max.	UNITS
Supply-Voltage Range (For T_A = Full Package-Temperature Range)	–	3	18	V
Minimum Input-Pulse Width, t_W	5	–	100	ns
	10	–	50	ns
	15	–	40	ns
Maximum Input–Pulse Frequency, $f\phi$ (External Pulse Source)	5	5	–	MHz
	10	12	–	MHz
	15	15	–	MHz

DYNAMIC ELECTRICAL CHARACTERISTICS at T_A = 25°C; Input t_r, t_f = 20 ns, C_L = 50 pF, R_L = 200 kΩ

CHARACTERISTIC	TEST CONDITIONS		LIMITS			UNITS
		V_{DD} V	Min.	Typ.	Max.	
Propagation Delay Time: ϕ_I to y or y+d out t_{PHL}, t_{PLH}		5 10 15	– – –	2.2 0.9 0.65	5.5 2.7 2	µs
Transition Time: t_{THL}, t_{TLH}		5 10 15	– – –	25 13 10	50 25 20	ns
Minimum Input-Pulse Width t_W		5 10 15	– – –	50 25 20	100 50 40	ns
Input-Pulse Rise or Fall Time: $t_r\phi$, $t_f\phi$		5 10 15	– – –	– – –	500 500 500	µs
Maximum Input-Pulse Frequency: (External Pulse Source) f_ϕ		5 10 15	5 12 15	10 25 30	– – –	MHz
Input Capacitance, C_{IN}	Any Input		–	5	7.5	pF
Variation of Output Frequency (Unit-to-Unit)	f = 5 MHz	5 10 15	– – –	0.05 0.03 0.1	– – –	%
RC Oscillator Operation						
Maximum Oscillator Frequency (See Fig. 11) f_{osc}	R_X = 50 kΩ, R_S = 560 kΩ, C_X = 50 pF	5 10 15	45 45 45	60 60 60	75 75 75	kHz

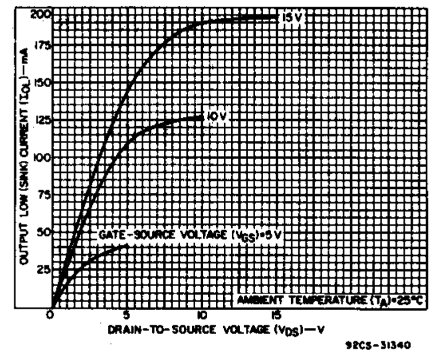


Fig. 2 – Typical output low (sink) current characteristics.

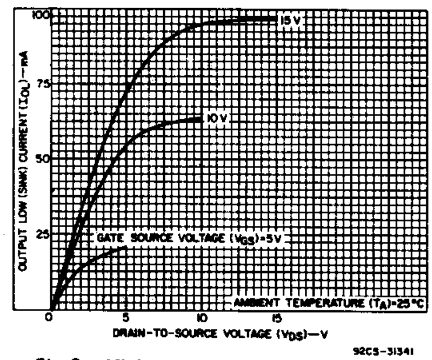


Fig. 3 – Minimum output low (sink) current characteristics.

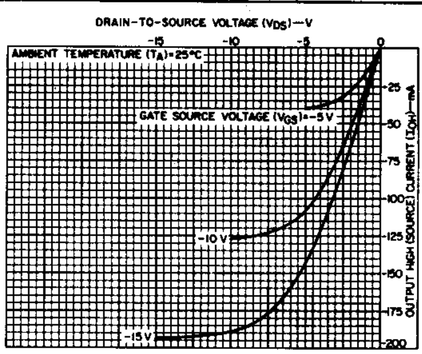


Fig. 4 – Typical output high (source) current characteristics.

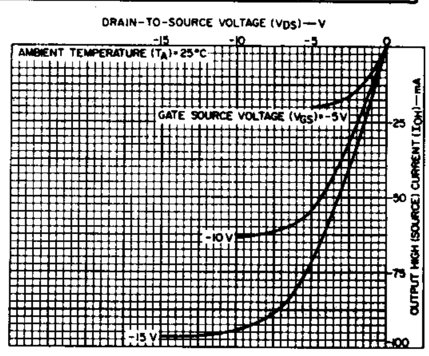


Fig. 5 – Minimum output high (source) characteristics.

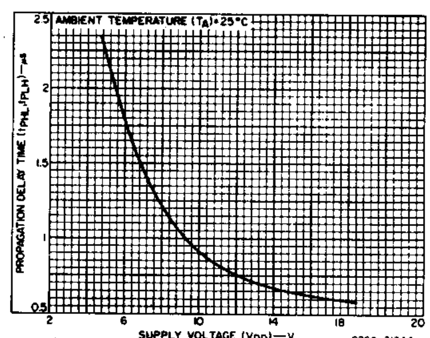


Fig. 6 – Typical propagation delay time as a function of supply voltage (ϕ_I to y or y + d out vs. V_{DD}).

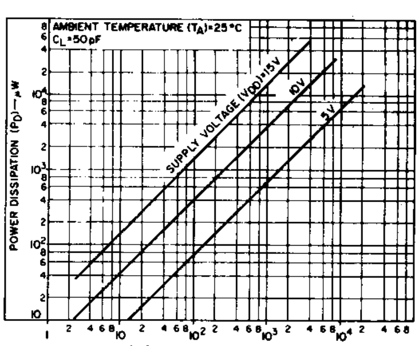


Fig. 7 – Typical power dissipation as a function of input frequency (21 counting stages).

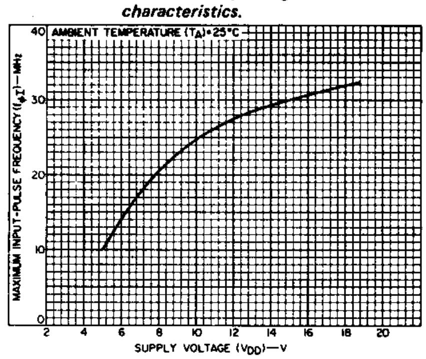


Fig. 8 – Typical maximum input-pulse frequency as a function of supply voltage.

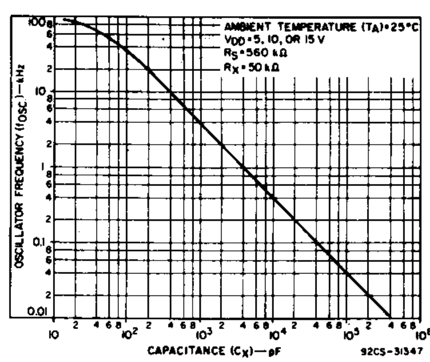


Fig. 9 – Typical RC oscillator frequency as a function of capacitance (C_X), See Fig. 11.

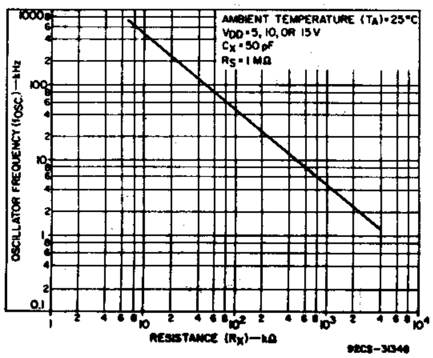


Fig. 10 – Typical RC oscillator frequency as a function of resistance (R_X), See Fig. 11.

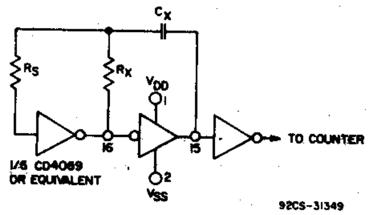


Fig. 11 – Typical RC circuit.

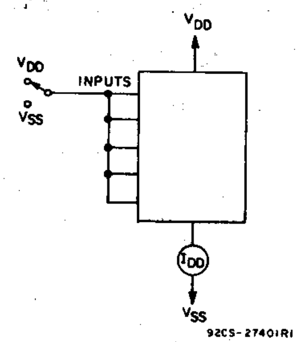


Fig. 12 – Quiescent-device-current test circuit.

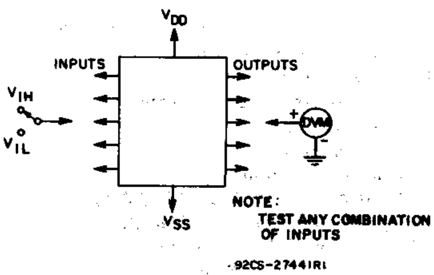


Fig. 13 – Noise-immunity test circuit.

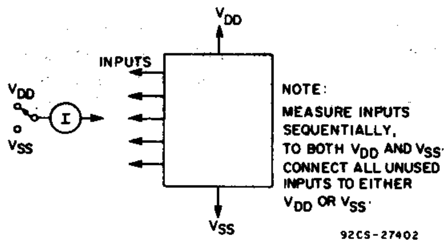


Fig. 14 – Input-leakage-current test circuit.

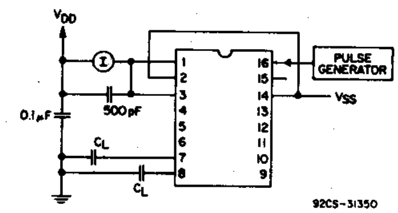
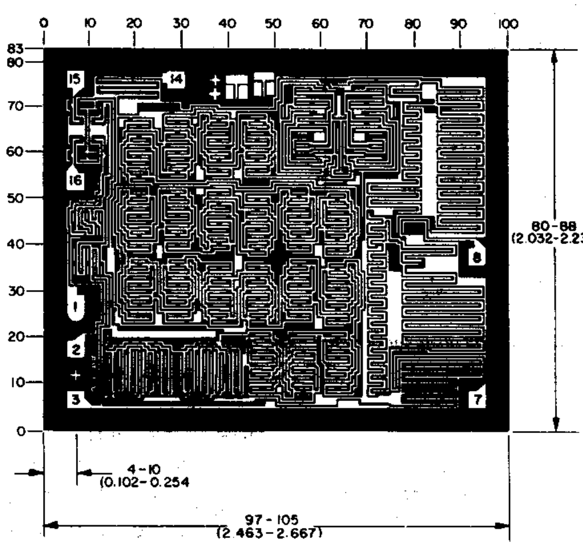


Fig. 15 – Dynamic power dissipation test circuit.

3

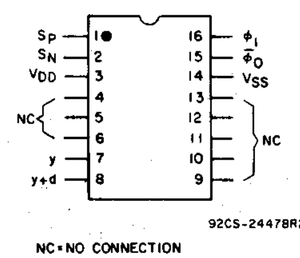
COMMERCIAL CMOS
HIGH VOLTAGE ICs



Chip dimensions and pad layout for CD4045B

Dimensions in parentheses are in millimeters and are derived from the basic inch dimensions as indicated. Grid graduations are in mils (10^{-3} inch).

TERMINAL DIAGRAM
Top View



NC = NO CONNECTION

NOTE Observe power-supply terminal connections, V_{DD} is terminal No. 3 and V_{SS} is terminal No. 14 (not 16 and 8 respectively, as in other CD4000B Series 16-lead devices).

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish	MSL Peak Temp (3)
CD4045BE	ACTIVE	PDIP	N	16	25	Pb-Free (RoHS)	CU NIPDAU	N / A for Pkg Type
CD4045BEE4	ACTIVE	PDIP	N	16	25	Pb-Free (RoHS)	CU NIPDAU	N / A for Pkg Type
CD4045BNSR	ACTIVE	SO	NS	16	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
CD4045BNSRE4	ACTIVE	SO	NS	16	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
CD4045BNSRG4	ACTIVE	SO	NS	16	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
CD4045BPW	ACTIVE	TSSOP	PW	16	90	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
CD4045BPWE4	ACTIVE	TSSOP	PW	16	90	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
CD4045BPWG4	ACTIVE	TSSOP	PW	16	90	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
CD4045BPWR	ACTIVE	TSSOP	PW	16	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
CD4045BPWRE4	ACTIVE	TSSOP	PW	16	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
CD4045BPWRG4	ACTIVE	TSSOP	PW	16	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check http://www.ti.com/productcontent for the latest availability information and additional product content details.
TBD: The Pb-Free/Green conversion plan has not been defined.
Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.
Pb-Free (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.
Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

(3) MSL, Peak Temp. -- The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

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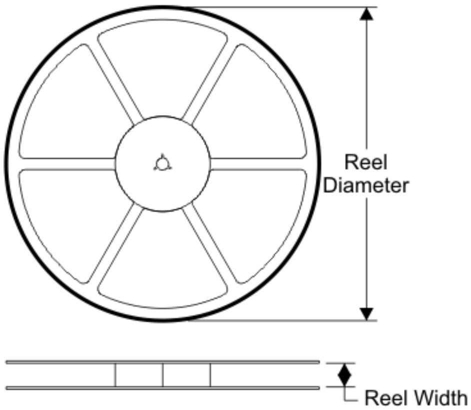
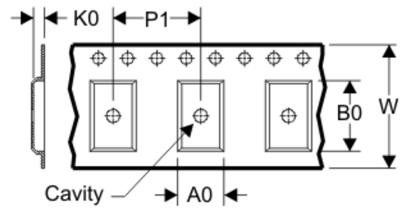
PACKAGE MATERIALS INFORMATION

TAPE AND REEL BOX INFORMATION

REEL DIMENSIONS

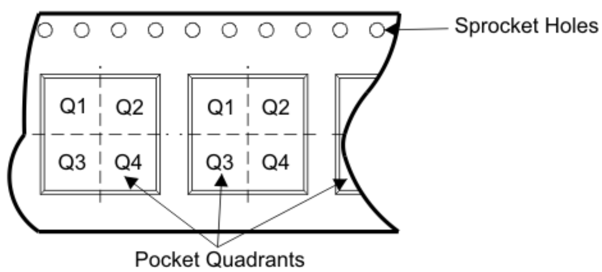


TAPE DIMENSIONS



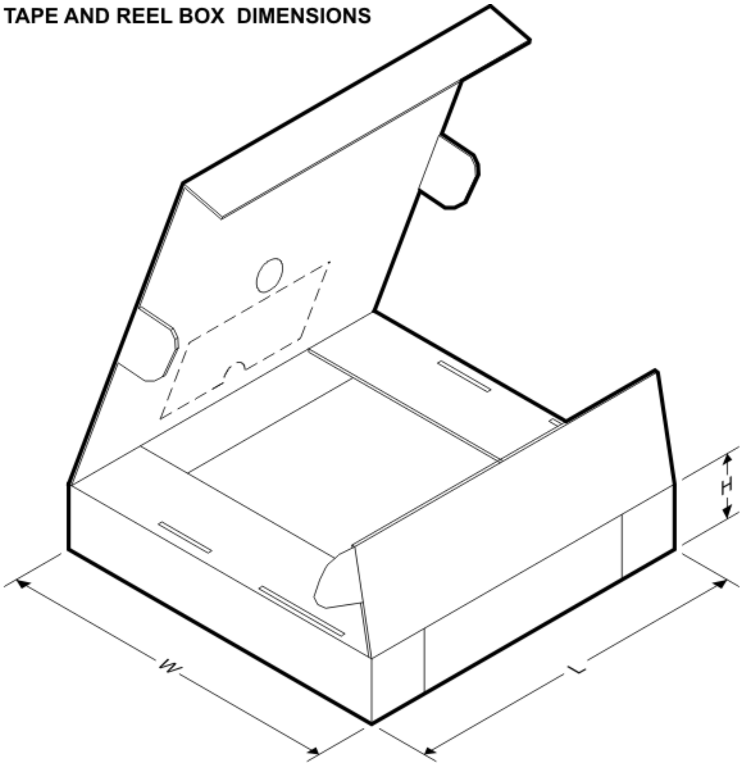
A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



Device	Package	Pins	Site	Reel Diameter (mm)	Reel Width (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
CD4045BNSR	NS	16	SITE 41	330	16	8.2	10.5	2.5	12	16	Q1
CD4045BPWR	PW	16	SITE 41	330	12	7.0	5.6	1.6	8	12	Q1

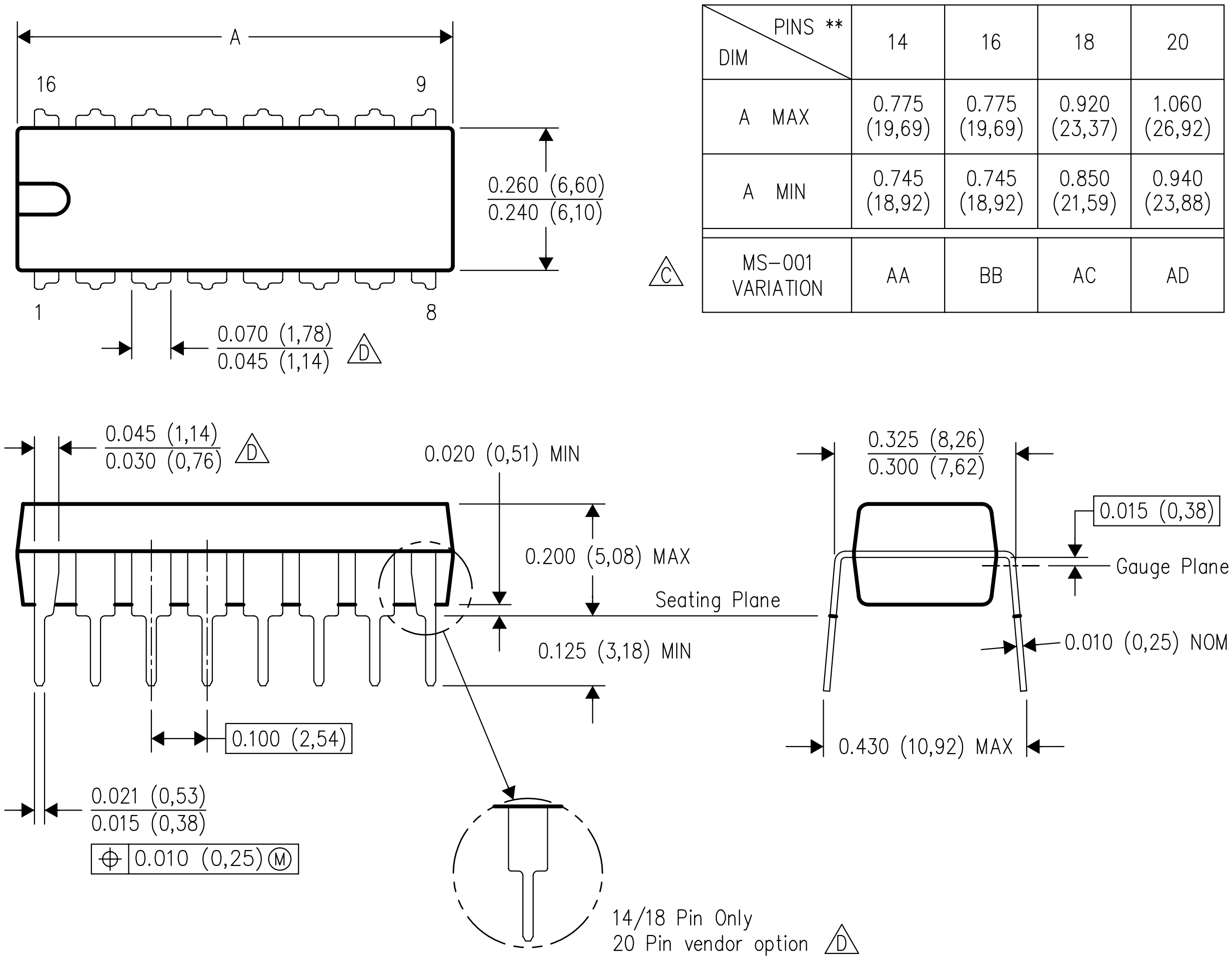
TAPE AND REEL BOX DIMENSIONS



Device	Package	Pins	Site	Length (mm)	Width (mm)	Height (mm)
CD4045BNSR	NS	16	SITE 41	346.0	346.0	33.0
CD4045BPWR	PW	16	SITE 41	346.0	346.0	29.0

N (R–PDIP–T**) PLASTIC DUAL–IN–LINE PACKAGE

16 PINS SHOWN



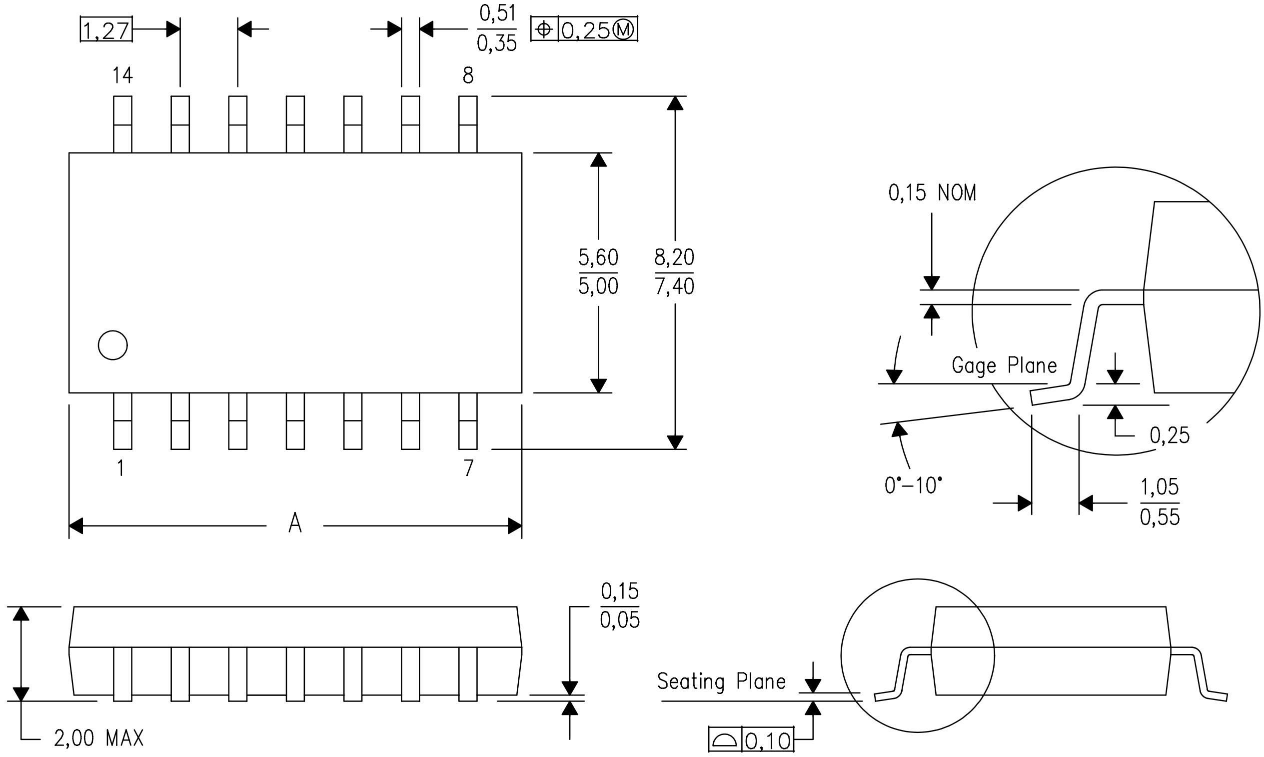
DIM \ PINS **	14	16	18	20
A MAX	0.775 (19,69)	0.775 (19,69)	0.920 (23,37)	1.060 (26,92)
A MIN	0.745 (18,92)	0.745 (18,92)	0.850 (21,59)	0.940 (23,88)
C MS–001 VARIATION	AA	BB	AC	AD

4040049/E 12/2002

NOTES: A. All linear dimensions are in inches (millimeters).
B. This drawing is subject to change without notice.
C. Falls within JEDEC MS–001, except 18 and 20 pin minimum body length (Dim A).
D. The 20 pin end lead shoulder width is a vendor option, either half or full width.

NS (R-PDSO-G)** **PLASTIC SMALL-OUTLINE PACKAGE**

14-PINS SHOWN



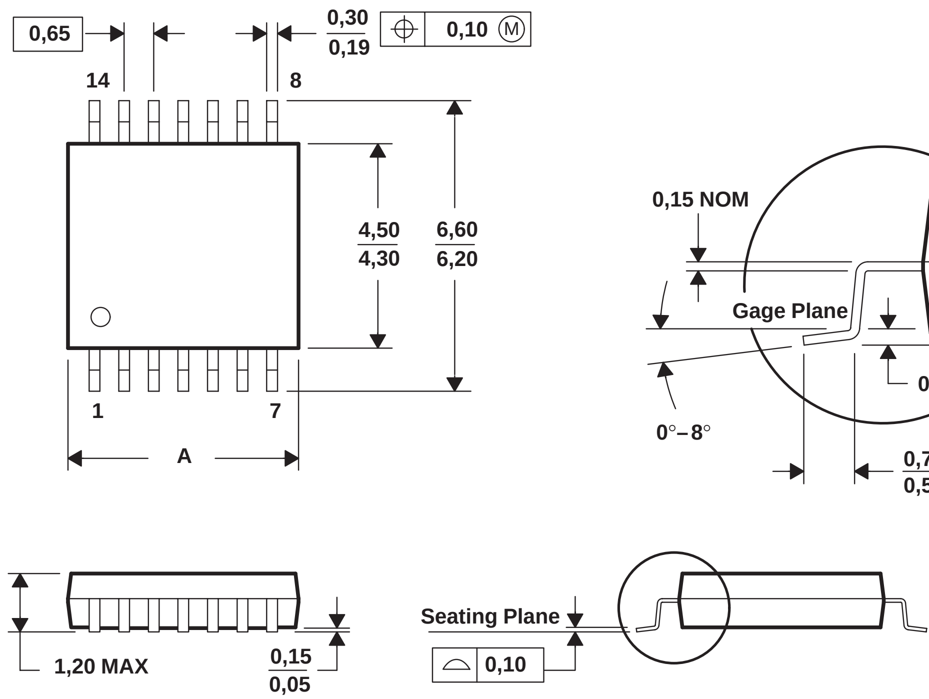
PINS ** / DIM	14	16	20	24
A MAX	10,50	10,50	12,90	15,30
A MIN	9,90	9,90	12,30	14,70

4040062/C 03/03

NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Body dimensions do not include mold flash or protrusion, not to exceed 0,15.

PW (R-PDSO-G)** **PLASTIC SMALL-OUTLINE PACKAGE**

14 PINS SHOWN



PINS ** / DIM	8	14	16	20	24	28
A MAX	3,10	5,10	5,10	6,60	7,90	9,80
A MIN	2,90	4,90	4,90	6,40	7,70	9,60

4040064/F 01/97

NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Body dimensions do not include mold flash or protrusion not to exceed 0,15.
D. Falls within JEDEC MO-153

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