MOTOROLA

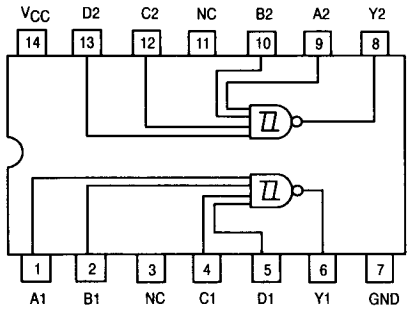
Dual 4-Input Schmitt-Trigger Positive NAND Gate

ELECTRICALLY TESTED PER:
MIL-M-38510/31301

The 54LS13 contains logic gates which accept standard TTL input signals and provide standard TTL output levels. It is capable of transforming slowly changing input signals into sharply defined, jitter-free output signals. Additionally, it has greater noise margin than conventional inverters.

Each circuit contains a Schmitt trigger followed by a Darlington level shifter and a phase splitter driving a TTL totem pole output. The Schmitt trigger uses positive feedback to effectively speed-up slow input transitions, and provide different input threshold voltages for positive and negative-going transitions. This hysteresis between the positive-going and negative-going input thresholds is determined internally by resistor ratios and is essentially insensitive to temperature and supply voltage variations.

LOGIC DIAGRAM



Military 54LS13

AVAILABLE AS:

1) JAN: JM38510/31301BXA
2) SMD: N/A
3) 883: 54LS13/BXAJC

X = CASE OUTLINE AS FOLLOWS:
PACKAGE: CERDIP: C
CERFLAT: D
LCC: 2

THE LETTER "M" APPEARS BEFORE THE / ON LCC.

PIN ASSIGNMENTS

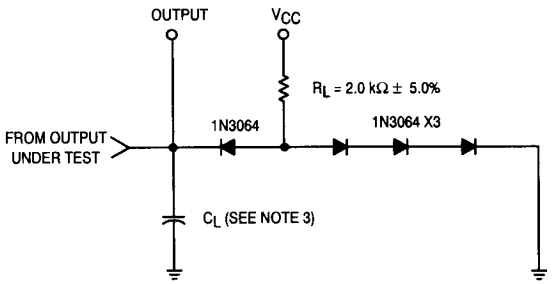
FUNCT.	DIL 632-08	FLATS 717-04	LCC 756A-02	BURN-IN (COND. A)
A1	1	1	2	GND
B1	2	2	3	V_{CC}
NC	3	3	4	GND
C1	4	4	6	V_{CC}
D1	5	5	8	GND
Y1	6	6	9	V_{CC}
GND	7	7	10	GND
Y2	8	8	12	V_{CC}
A2	9	9	13	GND
B2	10	10	14	V_{CC}
NC	11	11	16	GND
C2	12	12	18	V_{CC}
D2	13	13	19	GND
V_{CC}	14	14	20	V_{CC}

BURN-IN CONDITIONS:
V_{CC} = 5.0 V MIN/6.0 V MAX

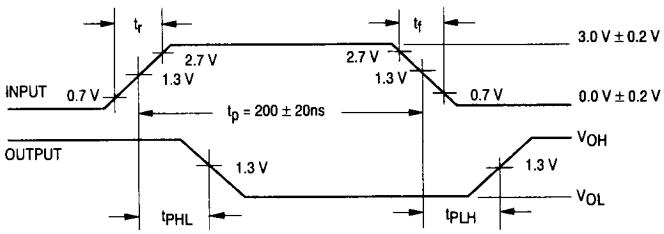
5

AC TEST CIRCUIT

(LOAD FOR OUTPUT UNDER TEST)



WAVEFORMS



NOTES:

1. Pulse generator has the following characteristics: $t_r \leq 15$ ns, $t_f \leq 6.0$ ns, PRR ≤ 1.0 MHz and $Z_{OUT} \approx 50\ \Omega$.
2. Terminal conditions (pins not designated may be high ≥ 1.4 V, low ≤ 1.0 V, or open).
3. $C_L = 50$ pF ± 10%, including scope probe, wiring and stray capacitance.
4. $R_L = 2.0$ kΩ ± 5.0%.
5. Voltage measurements are to be made with respect to network ground terminal.

5

Symbol	Parameter	Limits						Unit	Test Condition (Unless Otherwise Specified)
	Static Parameters:	+ 25°C		+ 125°C		− 55°C			
		Subgroup 1		Subgroup 2		Subgroup 3			
		Min	Max	Min	Max	Min	Max		
V_{OH1}	Logical "1" Output Voltage	2.5		2.5		2.5		V	V_{CC} = 4.5 V, I_{OH} = − 0.4 mA, V_{IL} = 0.5 V, V_{IN} = 1.9 V on other inputs.
V_{OL1}	Logical "0" Output Voltage		0.4		0.4		0.4	V	V_{CC} = 4.5 V, I_{OL} = 4.0 mA, V_{IH} = 1.9 V on all inputs.
V_{OH2}	Logical "1" Output Voltage	2.5		2.5		2.5		V	V_{CC} = 5.0 V, I_{OH} = − 0.4 V, V_{IL} = (See Note 2) all other inputs = 1.9 V.
V_{OL2}	Logical "0" Output Voltage		0.4		0.4		0.4	V	V_{CC} = 5.0 V, I_{OL} = 4.0 mA, V_{IN} = (See Note 3).
V_{IC}	Input Clamping Voltage		-1.5					V	V_{CC} = 4.5 V, I_{IN} = −18 mA, other inputs are open.
I_{IH1}	Logical "1" Input Current		20		20		20	µA	V_{CC} = 5.5 V, V_{IN} = 2.7 V, other inputs = 0 V.
I_{IH2}	Logical "1" Input Current		100		100		100	µA	V_{CC} = 5.5 V, V_{IN} = 5.5 V, other inputs = 0 V.
I_{IL}	Logical "0" Input Current	− 0.12	− 0.36	− 0.12	− 0.36	− 0.12	− 0.36	mA	V_{CC} = 5.5 V, V_{IN} = 0.4 V, other inputs = 5.5 V.
I_{OS}	Output Short Circuit Current	− 15	− 100	− 15	− 100	− 15	− 100	mA	V_{CC} = 5.5 V, V_{IN} = 0 V (all inputs), V_{OUT} = 0 V.
I_{CCH}	Power Supply Current		6.0		6.0		6.0	mA	V_{CC} = 5.5 V, V_{IN} = 0 V (all inputs).
I_{CCL}	Power Supply Current		7.0		7.0		7.0	mA	V_{CC} = 5.5 V, V_{IN} = 5.5 V (all inputs).
V_{IH}	Logical "1" Input Voltage	1.9		1.9		1.9		V	V_{CC} = 4.5 V.
V_{IL}	Logical "0" Input Voltage		0.5		0.5		0.5	V	V_{CC} = 4.5 V.
	Functional Tests	Subgroup 7		Subgroup 8A		Subgroup 8B			per Truth Table with V_{CC} = 5.0 V, V_{INL} = 0.5 V, and V_{INH} = 2.5 V.

Symbol	Parameter	Limits						Unit	Test Condition (Unless Otherwise Specified)
	Switching Parameters:	+ 25°C		+ 125°C		− 55°C			
		Subgroup 9		Subgroup 10		Subgroup 11			
		Min	Max	Min	Max	Min	Max		
t_{PHL} t_{PHL}	Propagation Delay /Data-Output Output High-Low	5.0 —	32 27	5.0 —	52 47	5.0 —	52 47	ns	V_{CC} = 5.0 V, C_L = 50 pF, R_L = 2.0 kΩ. V_{CC} = 5.0 V, C_L = 15 pF, R_L = 2.0 kΩ.
t_{PLH} t_{PLH}	Propagation Delay /Data-Output Output Low-High	5.0 —	32 22	5.0 —	52 47	5.0 —	52 47	ns	V_{CC} = 5.0 V, C_L = 50 pF, R_L = 2.0 kΩ. V_{CC} = 5.0 V, C_L = 15 pF, R_L = 2.0 kΩ.

NOTES:
1. The limits specified for C_L = 15 pF are guaranteed but not tested.
2. Momentary 0.5 V, then 1.4 V without overshoot during test.
3. Momentary 1.9 V, then 1.0 V (all inputs) without undershoot during test.