CD4536BMS

CMOS Programmable Timer

December 1992

Features

- **High Voltage Type (20V Rating)**
- **24 Flip-Flop Stage - Counts from 2^0 to 2^{24}**
- **Last 16 Stages Selectable by BCD Select Code**
- **Bypass Input Allows Bypassing First 8 Stages**
- **On-Chip RC Oscillator Provision**
- **Clock Inhibit Input**
- **Schmitt Trigger in clock Line Permits Operation with Very Long Rise and Fall Times**
- **On-Chip Monostable Output Provision**
- **Typical fCL = 3MHz at VDD = 10V**
- **Test Mode Allows Fast Test Sequence**
- **Set and Reset Inputs**
- **Capable of Driving Two Low Power TTL Loads, One Lower Power Schottky Load, or Two HTL Loads Over the Rated Temperature Range**
- **100% Tested for Quiescent Current at 20V**
- **5V, 10V and 15V Parametric Ratings**
- **Standardized, Symmetrical Output Characteristics**
- **Meets All Requirements of JEDEC Tentative Standard No. 13B, "Standard Specifications for Description of 'B' Series CMOS Devices"**

Description

CD4536BMS is a programmable timer consisting of 24 ripple binary counter stages. The salient feature of this device is its flexibility. The device can count from 1 to 2^{24} or the first 8 stages can be bypassed to allow an output, selectable by a 4-bit code, from any one of the remaining 16 stages. It can be driven by an external clock or an RC oscillator that can be constructed using on-chip components. Input IN1 serves as either the external clock input or the input to the on-chip RC oscillator. OUT1 and OUT2 are connection terminals for the external RC components. In addition, an on-chip monostable circuit is provided to allow a variable pulse width output. Various timing functions can be achieved using combinations of these capabilities.

A logic 1 on the 8-BYPASS input enables a bypass of the first 8 stages and makes stage 9 the first counter stage of the last 16 stages. Selection of 1 of 16 outputs is accomplished by the decoder and the BCD inputs A, B, C and D. MONO IN is the timing input for the on-chip monostable oscillator. Grounding of the MONO IN terminal through a resistor of 10kΩ or higher, disables the one-shot circuit and connects the decoder directly to the DECODE OUT terminal. A resistor to VDD and a capacitor to ground from the MONO IN terminal enables the one-shot circuit and controls its pulse width.

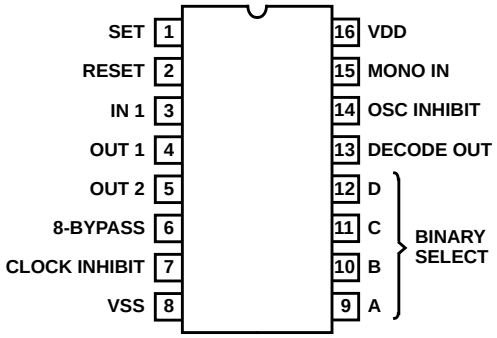
A fast test mode is enabled by a logic 1 on 8-BYPASS, SET, and RESET. This mode divides the 24-stage counter into three 8-stage sections to facilitate a fast test sequence.

The CD4536BMS is supplied in these 16-lead outline packages:

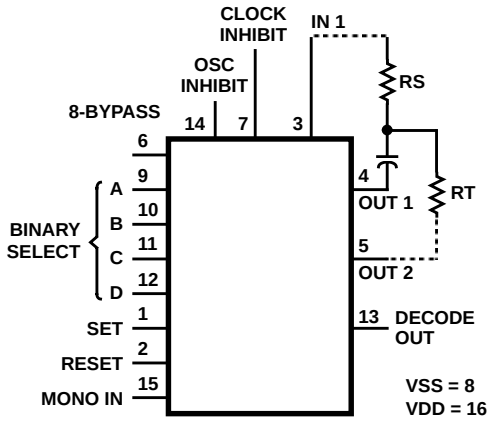
Braze Seal DIP	H4X
Frit Seal DIP	H1F
Ceramic Flatpack	H6W

Pinout

CD4536BMS
TOP VIEW



Functional Diagram



CAUTION: These devices are sensitive to electrostatic discharge; follow proper IC Handling Procedures.

File Number **3345**

Absolute Maximum Ratings

DC Supply Voltage Range, (VDD) . . . . . -0.5V to +20V
(Voltage Referenced to VSS Terminals)
Input Voltage Range, All Inputs . . . . . -0.5V to VDD +0.5V
DC Input Current, Any One Input . . . . . ±10mA
Operating Temperature Range . . . . . -55°C to +125°C
Package Types D, F, K, H
Storage Temperature Range (TSTG) . . . . . -65°C to +150°C
Lead Temperature (During Soldering) . . . . . +265°C
At Distance 1/16 ± 1/32 Inch (1.59mm ± 0.79mm) from case for 10s Maximum

Reliability Information

Thermal Resistance	θ_{ja}	θ_{jc}
Ceramic DIP and FRIT Package	80°C/W	20°C/W
Flatpack Package	70°C/W	20°C/W

Maximum Package Power Dissipation (PD) at +125°C
For T_A = -55°C to +100°C (Package Type D, F, K) 500mW
For T_A = +100°C to +125°C (Package Type D, F, K). . . . . Derate Linearity at 12mW/°C to 200mW
Device Dissipation per Output Transistor 100mW
For T_A = Full Package Temperature Range (All Package Types)
Junction Temperature . . . . . +175°C

TABLE 1. DC ELECTRICAL PERFORMANCE CHARACTERISTICS

PARAMETER	SYMBOL	CONDITIONS (NOTE 1)		GROUP A SUBGROUPS	TEMPERATURE	LIMITS MIN	LIMITS MAX	UNITS
Supply Current	IDD	VDD = 20V, VIN = VDD or GND		1	+25°C	-	10	µA
				2	+125°C	-	1000	µA
		VDD = 18V, VIN = VDD or GND		3	-55°C	-	10	µA
Input Leakage Current	IIL	VIN = VDD or GND	VDD = 20	1	+25°C	-100	-	nA
				2	+125°C	-1000	-	nA
			VDD = 18V	3	-55°C	-100	-	nA
Input Leakage Current	IIH	VIN = VDD or GND	VDD = 20	1	+25°C	-	100	nA
				2	+125°C	-	1000	nA
			VDD = 18V	3	-55°C	-	100	nA
Output Voltage	VOL15	VDD = 15V, No Load		1, 2, 3	+25°C, +125°C, -55°C	-	50	mV
Output Voltage	VOH15	VDD = 15V, No Load (Note 3)		1, 2, 3	+25°C, +125°C, -55°C	14.95	-	V
Output Current (Sink)	IOL5	VDD = 5V, VOUT = 0.4V		1	+25°C	0.53	-	mA
Output Current (Sink)	IOL10	VDD = 10V, VOUT = 0.5V		1	+25°C	1.4	-	mA
Output Current (Sink)	IOL15	VDD = 15V, VOUT = 1.5V		1	+25°C	3.5	-	mA
Output Current (Source)	IOH5A	VDD = 5V, VOUT = 4.6V		1	+25°C	-	-0.53	mA
Output Current (Source)	IOH5B	VDD = 5V, VOUT = 2.5V		1	+25°C	-	-1.8	mA
Output Current (Source)	IOH10	VDD = 10V, VOUT = 9.5V		1	+25°C	-	-1.4	mA
Output Current (Source)	IOH15	VDD = 15V, VOUT = 13.5V		1	+25°C	-	-3.5	mA
N Threshold Voltage	VNTH	VDD = 10V, ISS = -10µA		1	+25°C	-2.8	-0.7	V
P Threshold Voltage	VPTH	VSS = 0V, IDD = 10µA		1	+25°C	0.7	2.8	V
Functional	F	VDD = 2.8V, VIN = VDD or GND		7	+25°C	VOH > VDD/2	VOL < VDD/2	V
		VDD = 20V, VIN = VDD or GND		7	+25°C			
		VDD = 18V, VIN = VDD or GND		8A	+125°C			
		VDD = 3V, VIN = VDD or GND		8B	-55°C			
Input Voltage Low (Note 2)	VIL	VDD = 5V, VOH > 4.5V, VOL < 0.5V		1, 2, 3	+25°C, +125°C, -55°C	-	1.5	V
Input Voltage High (Note 2)	VIH	VDD = 5V, VOH > 4.5V, VOL < 0.5V		1, 2, 3	+25°C, +125°C, -55°C	3.5	-	V
Input Voltage Low (Note 2)	VIL	VDD = 15V, VOH > 13.5V, VOL < 1.5V		1, 2, 3	+25°C, +125°C, -55°C	-	4	V
Input Voltage High (Note 2)	VIH	VDD = 15V, VOH > 13.5V, VOL < 1.5V		1, 2, 3	+25°C, +125°C, -55°C	11	-	V

NOTES: 1. All voltages referenced to device GND, 100% testing being implemented.
2. Go/No Go test with limits applied to inputs.
3. For accuracy, voltage is measured differentially to VDD. Limit is 0.050V max.

TABLE 2. AC ELECTRICAL PERFORMANCE CHARACTERISTICS

PARAMETER	SYMBOL	CONDITIONS (NOTE 1, 2)	GROUP A SUBGROUPS	TEMPERATURE	LIMITS MIN	LIMITS MAX	UNITS
Propagation Delay Clock to Q1 8-Bypass High	TPHL1 TPLH1	VDD = 5V, VIN = VDD or GND	9	+25°C	-	2000	ns
			10, 11	+125°C, -55°C	-	2700	ns
Propagation Delay Clock to Q1 8-Bypass Low	TPHL2 TPLH2	VDD = 5V, VIN = VDD or GND	9	+25°C	-	5000	ns
			10, 11	+125°C, -55°C	-	6750	ns
Propagation Delay Clock to Q16	TPHL3 TPLH3	VDD = 5V, VIN = VDD or GND	9	+25°C	-	8000	ns
			10, 11	+125°C, -55°C	-	10800	ns
Propagation Delay Reset to QN	TPHL4	VDD = 5V, VIN = VDD or GND	9	+25°C	-	6000	ns
			10, 11	+125°C, -55°C	-	8100	ns
Transition Time	TTHL TTLH	VDD = 5V, VIN = VDD or GND	9	+25°C	-	200	ns
			10, 11	+125°C, -55°C	-	270	ns
Maximum Clock Input Frequency	FCL	VDD = 5V, VIN = VDD or GND	9	+25°C	.5	-	MHz
			10, 11	+125°C, -55°C	.37	-	MHz

NOTES:

1. VDD = 5V, CL = 50pF, RL = 200K, Input TR, TF < 20ns.
2. -55°C and +125°C limits guaranteed, 100% testing being implemented.

TABLE 3. ELECTRICAL PERFORMANCE CHARACTERISTICS

PARAMETER	SYMBOL	CONDITIONS	NOTES	TEMPERATURE	LIMITS MIN	LIMITS MAX	UNITS
Supply Current	IDD	VDD = 5V, VIN = VDD or GND	1, 2	-55°C, +25°C	-	5	µA
				+125°C	-	150	µA
		VDD = 10V, VIN = VDD or GND	1, 2	-55°C, +25°C	-	10	µA
				+125°C	-	300	µA
		VDD = 15V, VIN = VDD or GND	1, 2	-55°C, +25°C	-	10	µA
				+125°C	-	600	µA
Output Voltage	VOL	VDD = 5V, No Load	1, 2	+25°C, +125°C, -55°C	-	50	mV
Output Voltage	VOL	VDD = 10V, No Load	1, 2	+25°C, +125°C, -55°C	-	50	mV
Output Voltage	VOH	VDD = 5V, No Load	1, 2	+25°C, +125°C, -55°C	4.95	-	V
Output Voltage	VOH	VDD = 10V, No Load	1, 2	+25°C, +125°C, -55°C	9.95	-	V
Output Current (Sink)	IOL5	VDD = 5V, VOUT = 0.4V	1, 2	+125°C	0.36	-	mA
				-55°C	0.64	-	mA
Output Current (Sink)	IOL10	VDD = 10V, VOUT = 0.5V	1, 2	+125°C	0.9	-	mA
				-55°C	1.6	-	mA
Output Current (Sink)	IOL15	VDD = 15V, VOUT = 1.5V	1, 2	+125°C	2.4	-	mA
				-55°C	4.2	-	mA
Output Current (Source)	IOH5A	VDD = 5V, VOUT = 4.6V	1, 2	+125°C	-	-0.36	mA
				-55°C	-	-0.64	mA
Output Current (Source)	IOH5B	VDD = 5V, VOUT = 2.5V	1, 2	+125°C	-	-1.15	mA
				-55°C	-	-2.0	mA
Output Current (Source)	IOH10	VDD = 10V, VOUT = 9.5V	1, 2	+125°C	-	-0.9	mA
				-55°C	-	-1.6	mA

TABLE 3. ELECTRICAL PERFORMANCE CHARACTERISTICS (Continued)

PARAMETER	SYMBOL	CONDITIONS	NOTES	TEMPERATURE	LIMITS MIN	LIMITS MAX	UNITS
Output Current (Source)	IOH15	VDD =15V, VOUT = 13.5V	1, 2	+125°C	-	-2.4	mA
				-55°C	-	-4.2	mA
Input Voltage Low	VIL	VDD = 10V, VOH > 9V, VOL < 1V	1, 2	+25°C, +125°C, -55°C	-	3	V
Input Voltage High	VIH	VDD = 10V, VOH > 9V, VOL < 1V	1, 2	+25°C, +125°C, -55°C	+7	-	V
Propagation Delay Clock to Q1 8-Bypass High	TPHL1 TPLH1	VDD = 10V	1, 2, 3	+25°C	-	1000	ns
		VDD = 15V	1, 2, 3	+25°C	-	700	ns
Propagation Delay Clock to Q1 8-Bypass Low	TPHL2 TPLH2	VDD = 10V	1, 2, 3	+25°C	-	1600	ns
		VDD = 15V	1, 2, 3	+25°C	-	1200	ns
Propagation Delay Clock to Q16	TPHL3 TPLH3	VDD = 10V	1, 2, 3	+25°C	-	3000	ns
		VDD = 15V	1, 2, 3	+25°C	-	2000	ns
Propagation Delay Qn to Qn+1	TPHL TPLH	VDD = 5V	1, 2, 3	+25°C	-	300	
		VDD = 10V	1, 2, 3	+25°C	-	150	
		VDD = 15V	1, 2, 3	+25°C	-	100	
Propagation Delay Set to Qn	TPLH	VDD = 5V	1, 2, 3	+25°C	-	600	
		VDD = 10V	1, 2, 3	+25°C	-	250	
		VDD = 15V	1, 2, 3	+25°C	-	160	
Propagation Delay Reset to Qn	TPHL4	VDD = 10V	1, 2, 3	+25°C	-	2000	ns
		VDD = 15V	1, 2, 3	+25°C	-	1500	ns
Transition Time	TTHL TTLH	VDD = 10V	1, 2, 3	+25°C	-	100	ns
		VDD = 15V	1, 2, 3	+25°C	-	80	ns
Maximum Clock Input Frequency. Unlimited Input Rise or Fall Time	FCL	VDD = 10V	1, 2, 3	+25°C	1.5	-	MHz
		VDD = 15V	1, 2, 3	+25°C	2.5	-	MHz
Minimum Clock Pulse Width	TW	VDD = 5V	1, 2, 3	+25°C	-	400	ns
		VDD = 10V	1, 2, 3	+25°C	-	150	ns
		VDD = 15V	1, 2, 3	+25°C	-	100	ns
Minimum Set Pulse Width	TW	VDD = 5V	1, 2, 3	+25°C	-	400	ns
		VDD = 10V	1, 2, 3	+25°C	-	200	ns
		VDD = 15V	1, 2, 3	+25°C	-	120	ns
Minimum Reset Pulse Width	TW	VDD = 5V	1, 2, 3	+25°C	-	6	µs
		VDD = 10V	1, 2, 3	+25°C	-	2	µs
		VDD = 15V	1, 2, 3	+25°C	-	1.5	µs
Minimum Set Recovery Time	TREM	VDD = 5V	1, 2, 3	+25°C	-	5	µs
		VDD = 10V	1, 2, 3	+25°C	-	2	µs
		VDD = 15V	1, 2, 3	+25°C	-	1.6	µs
Minimum Reset Recovery Time	TREM	VDD = 5V	1, 2, 3	+25°C	-	7	µs
		VDD = 10V	1, 2, 3	+25°C	-	3	µs
		VDD = 15V	1, 2, 3	+25°C	-	2	µs
Input Capacitance	CIN	Any Input	1, 2	+25°C	-	7.5	pF

NOTES:

1. All voltages referenced to device GND.
2. The parameters listed on Table 3 are controlled via design or process and are not directly tested. These parameters are characterized on initial design release and upon design changes which would affect these characteristics.
3. CL = 50pF, RL = 200K, Input TR, TF < 20ns.

TABLE 4. POST IRRADIATION ELECTRICAL PERFORMANCE CHARACTERISTICS

PARAMETER	SYMBOL	CONDITIONS	NOTES	TEMPERATURE	LIMITS		UNITS
					MIN	MAX	
Supply Current	IDD	VDD = 20V, VIN = VDD or GND	1, 4	+25°C	-	25	µA
N Threshold Voltage	VNTH	VDD = 10V, ISS = -10µA	1, 4	+25°C	-2.8	-0.2	V
N Threshold Voltage Delta	ΔVTN	VDD = 10V, ISS = -10µA	1, 4	+25°C	-	±1	V
P Threshold Voltage	VTP	VSS = 0V, IDD = 10µA	1, 4	+25°C	0.2	2.8	V
P Threshold Voltage Delta	ΔVTP	VSS = 0V, IDD = 10µA	1, 4	+25°C	-	±1	V
Functional	F	VDD = 18V, VIN = VDD or GND	1	+25°C	VOH > VDD/2	VOL < VDD/2	V
		VDD = 3V, VIN = VDD or GND					
Propagation Delay Time	TPHL TPLH	VDD = 5V	1, 2, 3, 4	+25°C	-	1.35 x +25°C Limit	ns

NOTES: 1. All voltages referenced to device GND.
2. CL = 50pF, RL = 200K, Input TR, TF < 20ns.
3. See Table 2 for +25°C limit.
4. Read and Record

TABLE 5. BURN-IN AND LIFE TEST DELTA PARAMETERS +25°C

PARAMETER	SYMBOL	DELTA LIMIT
Supply Current - MSI-2	IDD	± 1.0µA
Output Current (Sink)	IOL5	± 20% x Pre-Test Reading
Output Current (Source)	IOH5A	± 20% x Pre-Test Reading

TABLE 6. APPLICABLE SUBGROUPS

CONFORMANCE GROUP		MIL-STD-883 METHOD	GROUP A SUBGROUPS	READ AND RECORD
Initial Test (Pre Burn-In)		100% 5004	1, 7, 9	IDD, IOL5, IOH5A
Interim Test 1 (Post Burn-In)		100% 5004	1, 7, 9	IDD, IOL5, IOH5A
Interim Test 2 (Post Burn-In)		100% 5004	1, 7, 9	IDD, IOL5, IOH5A
PDA (Note 1)		100% 5004	1, 7, 9, Deltas	
Interim Test 3 (Post Burn-In)		100% 5004	1, 7, 9	IDD, IOL5, IOH5A
PDA (Note 1)		100% 5004	1, 7, 9, Deltas	
Final Test		100% 5004	2, 3, 8A, 8B, 10, 11	
Group A		Sample 5005	1, 2, 3, 7, 8A, 8B, 9, 10, 11	
Group B	Subgroup B-5	Sample 5005	1, 2, 3, 7, 8A, 8B, 9, 10, 11, Deltas	Subgroups 1, 2, 3, 9, 10, 11
	Subgroup B-6	Sample 5005	1, 7, 9	
Group D		Sample 5005	1, 2, 3, 8A, 8B, 9	Subgroups 1, 2 3

NOTE: 1. 5% Parameteric, 3% Functional; Cumulative for Static 1 and 2.

TABLE 7. TOTAL DOSE IRRADIATION

CONFORMANCE GROUPS	MIL-STD-883 METHOD	TEST		READ AND RECORD	
		PRE-IRRAD	POST-IRRAD	PRE-IRRAD	POST-IRRAD
Group E Subgroup 2	5005	1, 7, 9	Table 4	1, 9	Table 4

TABLE 8. BURN-IN AND IRRADIATION TEST CONNECTIONS

FUNCTION	OPEN	GROUND	VDD	9V ± -0.5V	OSCILLATOR	
					50kHz	25kHz
Static Burn-In 1 Note 1	4, 5, 13	1-3, 6-12, 14, 15	16			
Static Burn-In 2 Note 1	4, 5, 13	8	1-3, 6, 7, 9-12, 14-16			
Dynamic Burn-In Note 1	-	1, 2, 6-8, 14, 15	9-12, 16	4, 5, 13	3	
Irradiation Note 2	4, 5, 13	8	1-3, 6, 7, 9-12, 14-16			

NOTE:

1. Each pin except VDD and GND will have a series resistor of 10K ± 5%, VDD = 18V ± 0.5V
2. Each pin except VDD and GND will have a series resistor of 47K ± 5%; Group E, Subgroup 2, sample size is 4 dice/wafer, 0 failures, VDD = 10V ± 0.5V

Logic Diagram

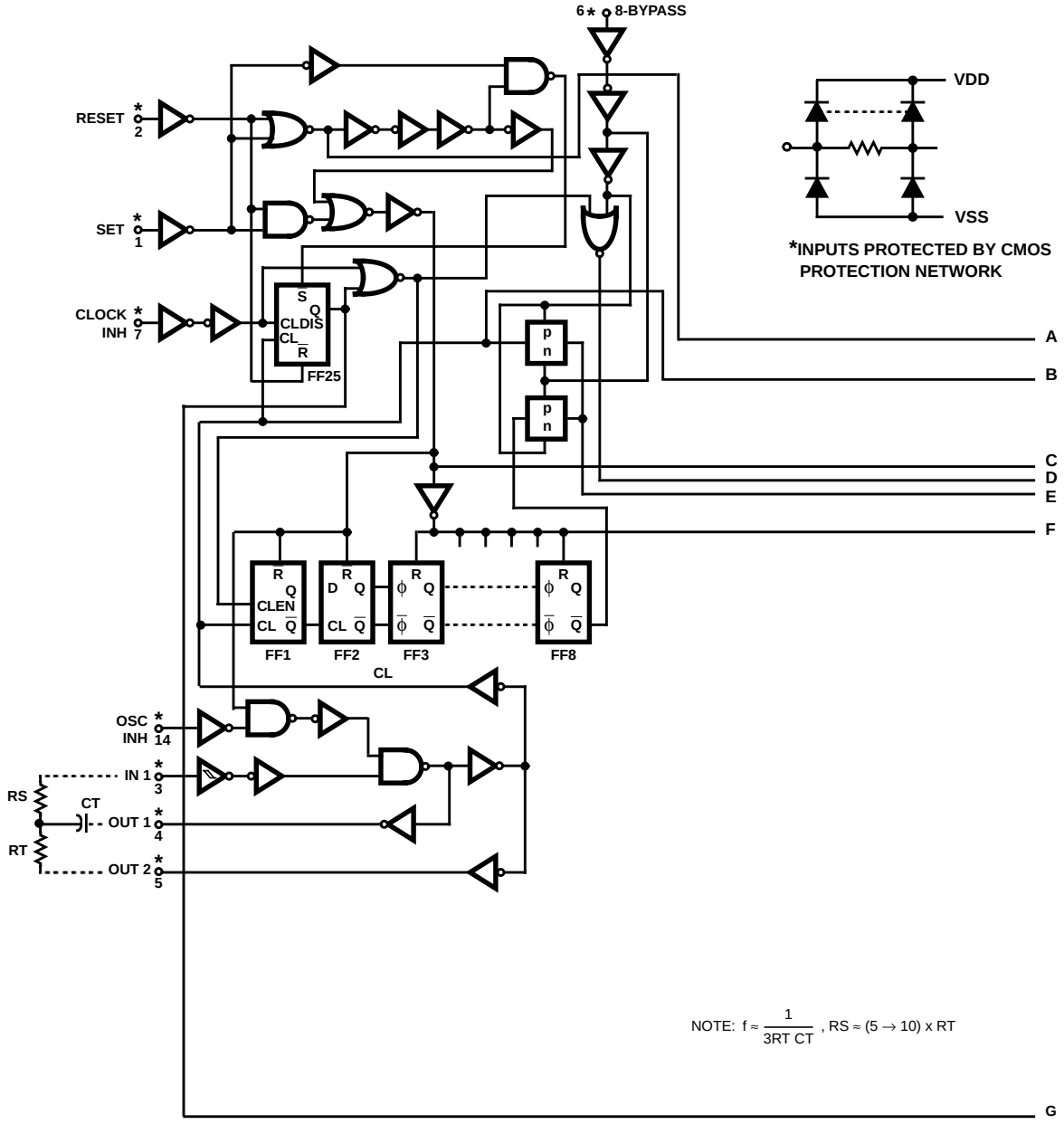
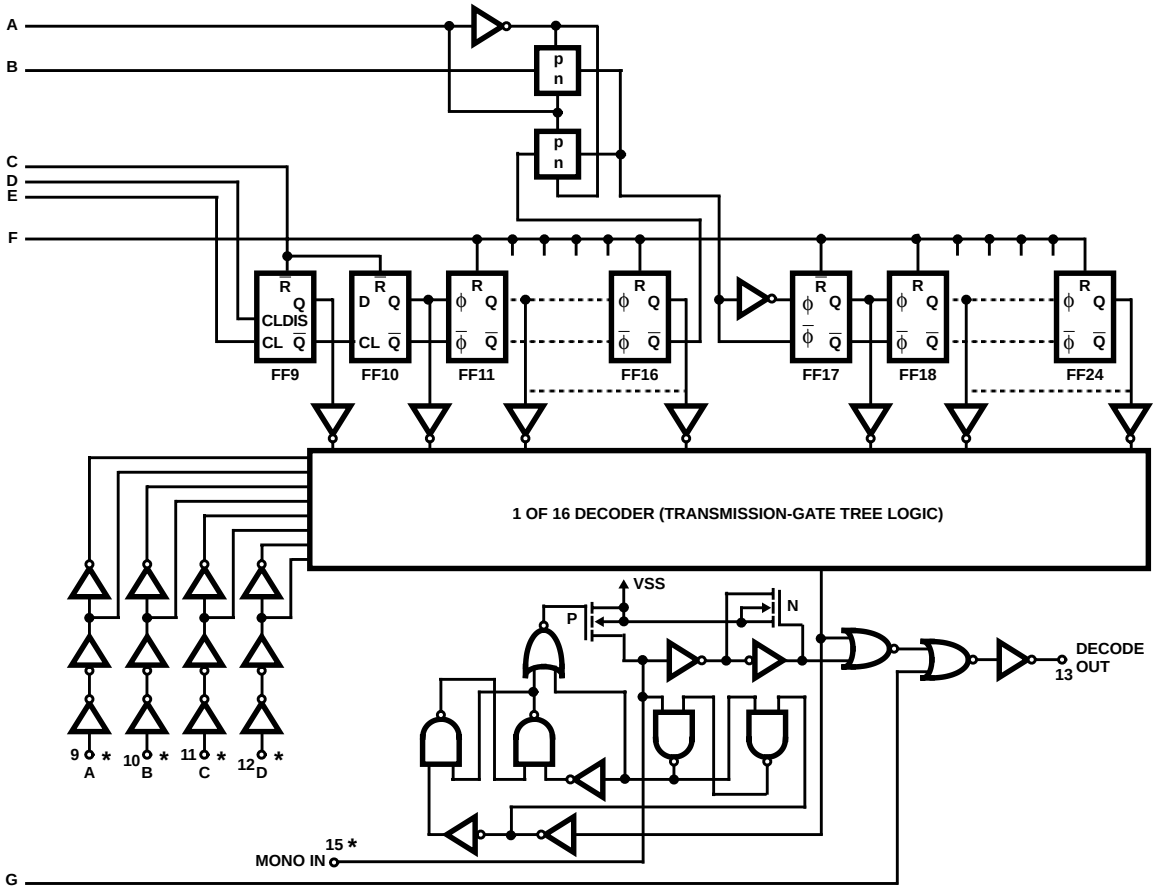
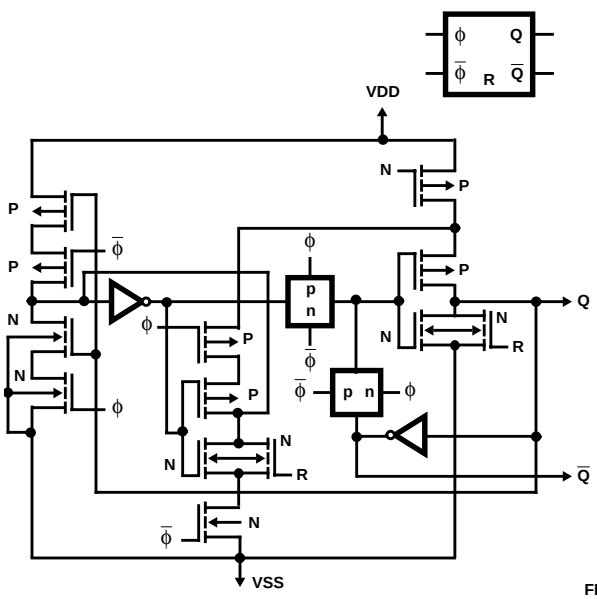


FIGURE 1.

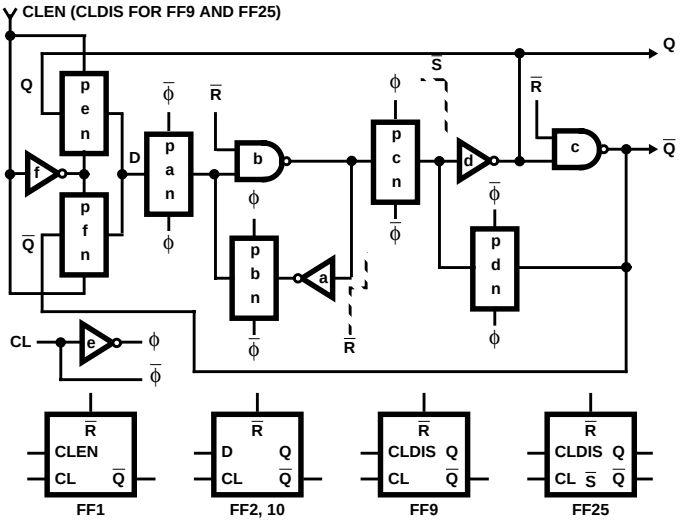
Logic Diagram (Continued)



DETAIL FOR
FF3-8, 11-16, 17-24



DETAIL FOR
FF1, FF2, FF10, FF9, FF25



FF1: AS SHOWN EXCEPT Q NOT BROUGHT OUT

FF9: SAME AS FF1 EXCEPT Q IS BROUGHT OUT AND Q, $\overline{Q}$ GO TO TGf AND TGe RESP.

FF2, FF10: DELETE TGe, TGf, AND INVf; FEED $\overline{Q}$ TO D; DELETE CLEN, CLDIS

FF25: INVa AND INVd BECOME 2-INPUT NAND GATES, WITH ADDED INPUTS $\overline{S}$; FEED Q TO TGf VSS TO TGe PREVIOUS Q INPUT; DELETE $\overline{Q}$ OUTPUT

FIGURE 1. (Continued)

TRUTH TABLE

IN	SET	RESET	CLOCK INH	OSC INH	OUT1	OUT2	DECODE OUT
⎍	0	0	0	0	⎍	⎎	No Change
⎎	0	0	0	0	⎎	⎍	Advance to Next State
X	1	0	0	0	0	1	1
X	0	1	0	0	0	1	0
X	0	0	1	0			No Change
0	0	0	0	X	0	1	No Change
1	0	0	0	⎍	⎎	⎍	Advance to Next State

0 = Low Level 1 = High Level X = Don't Care

Typical Performance Characteristics

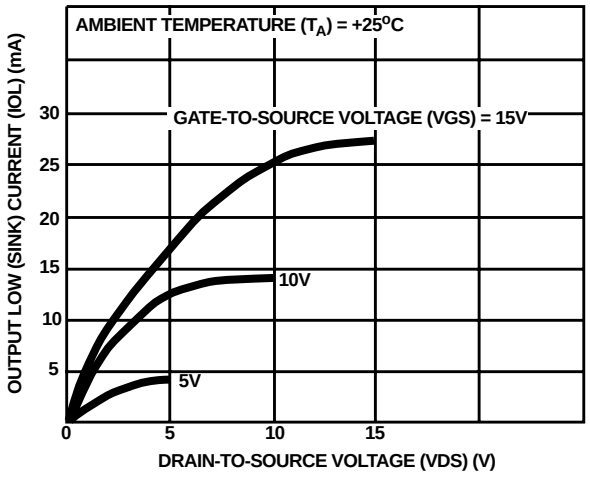


FIGURE 2. TYPICAL OUTPUT LOW (SINK) CURRENT CHARACTERISTICS

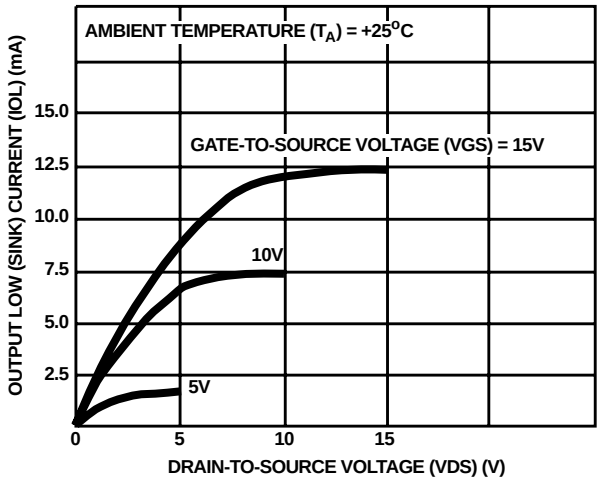


FIGURE 3. MINIMUM OUTPUT LOW (SINK) CURRENT CHARACTERISTICS

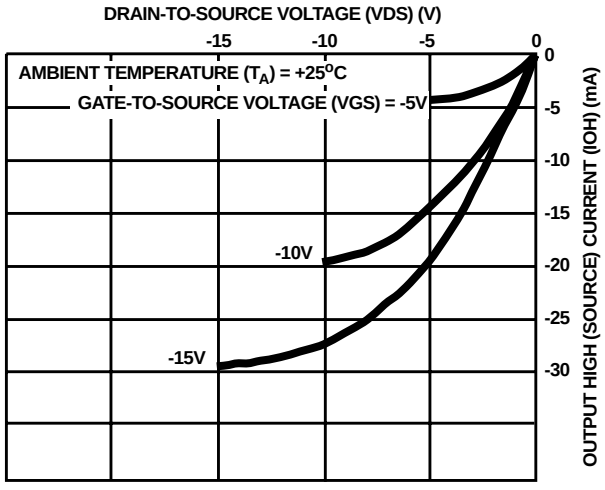


FIGURE 4. TYPICAL OUTPUT HIGH (SOURCE) CURRENT CHARACTERISTICS

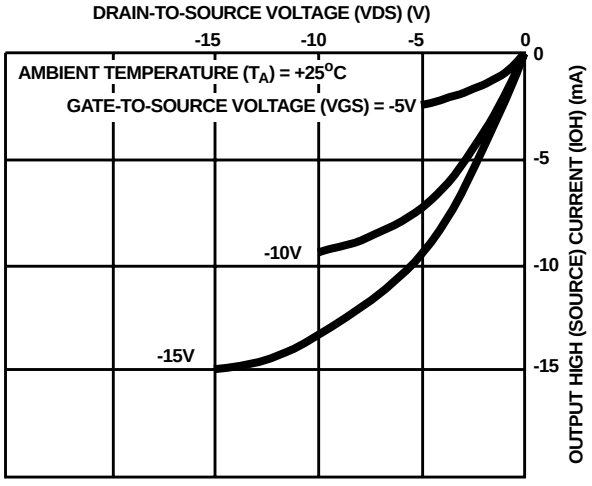


FIGURE 5. MINIMUM OUTPUT HIGH (SOURCE) CURRENT CHARACTERISTICS

Typical Performance Characteristics (Continued)

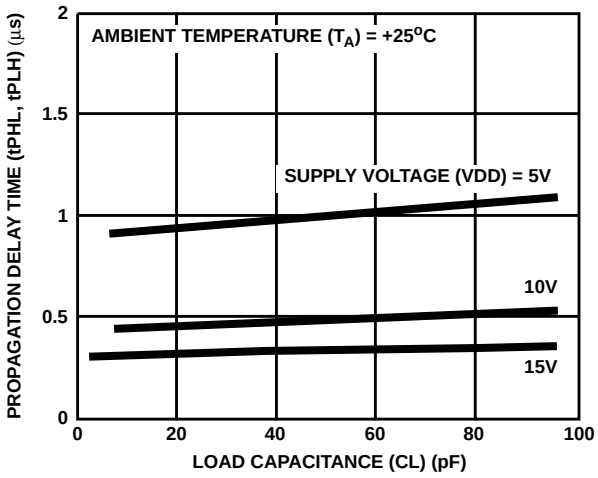


FIGURE 6. TYPICAL PROPAGATION DELAY TIME AS A FUNCTION OF LOAD CAPACITANCE (CLOCK TO Q1, 8-BYPASS HIGH)

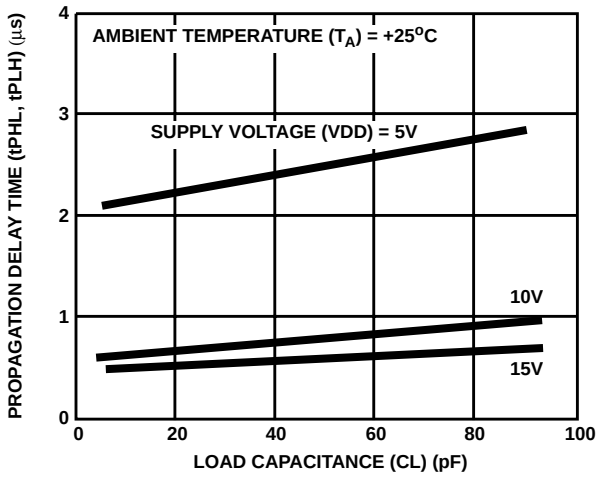


FIGURE 7. TYPICAL PROPAGATION DELAY TIME AS A FUNCTION OF LOAD CAPACITANCE (CLOCK TO Q1, 8-BYPASS LOW)

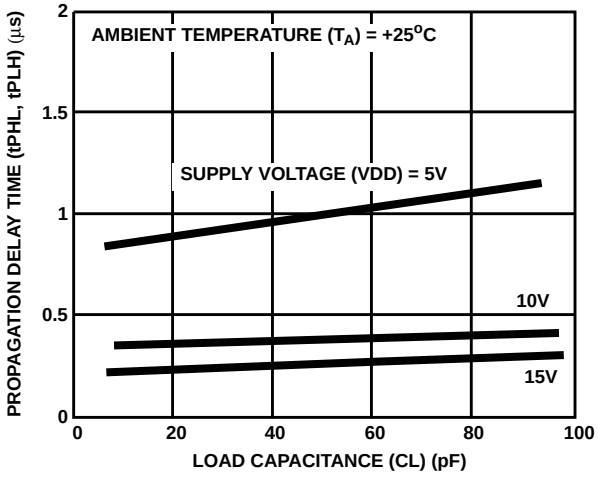


FIGURE 8. TYPICAL PROPAGATION DELAY TIME AS A FUNCTION OF LOAD CAPACITANCE (CLOCK TO Q16, 8-BYPASS HIGH)

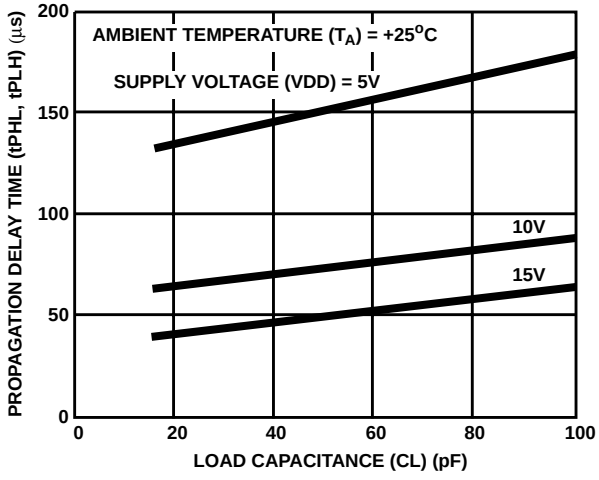


FIGURE 9. TYPICAL PROPAGATION DELAY TIME AS A FUNCTION OF LOAD CAPACITANCE (QN TO QN + 1)

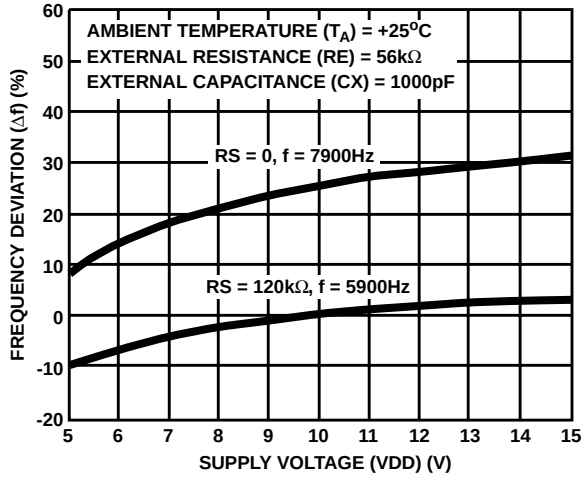


FIGURE 10. TYPICAL RC OSCILLATOR FREQUENCY DEVIATION AS A FUNCTION OF SUPPLY VOLTAGE

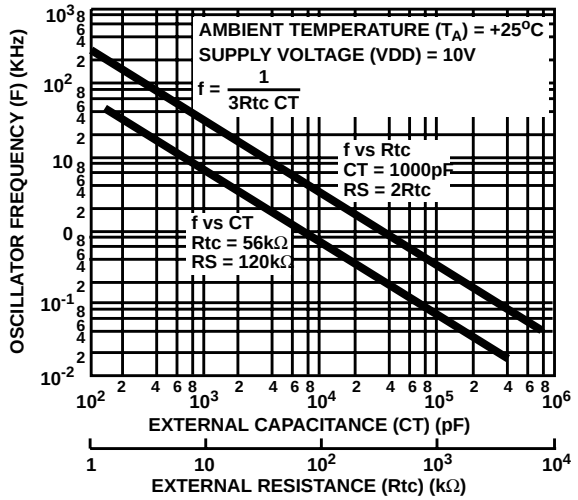


FIGURE 11. TYPICAL RC OSCILLATOR FREQUENCY DEVIATION AS A FUNCTION OF TIME CONSTANT RESISTANCE AND CAPACITANCE

Typical Performance Characteristics (Continued)

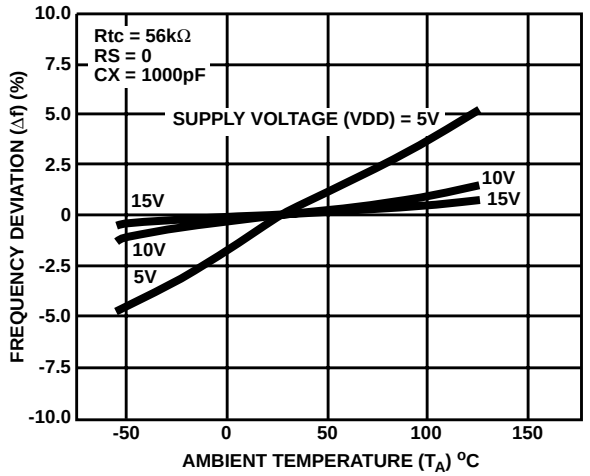


FIGURE 12. TYPICAL RC OSCILLATOR FREQUENCY DEVIATION AS A FUNCTION OF AMBIENT TEMPERATURE (RS = 0)

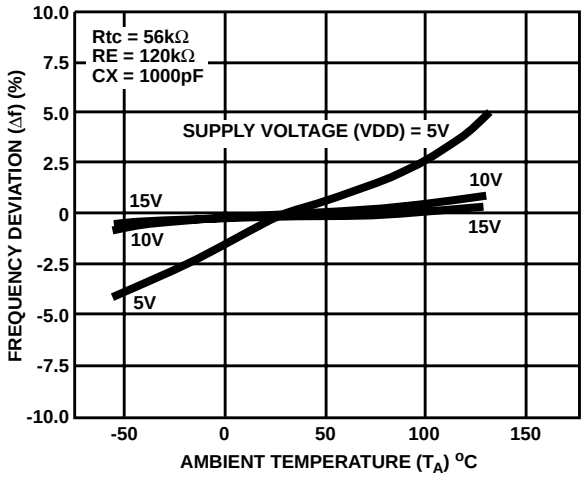


FIGURE 13. TYPICAL RC OSCILLATOR FREQUENCY DEVIATION AS A FUNCTION OF AMBIENT TEMPERATURE (RS = 120kΩ)

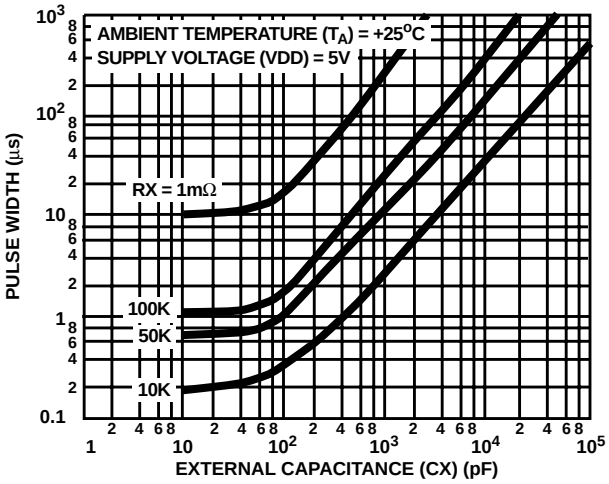


FIGURE 14. TYPICAL PULSE WIDTH AS A FUNCTION OF EXTERNAL CAPACITANCE (VDD = 5V)

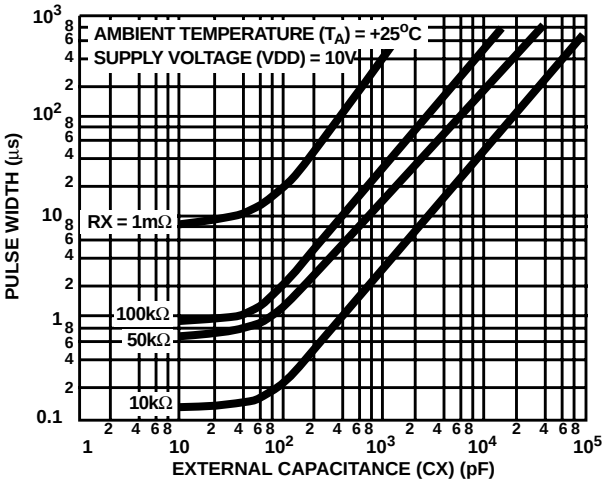


FIGURE 15. TYPICAL PULSE WIDTH AS A FUNCTION OF EXTERNAL CAPACITANCE (VDD = 10V)

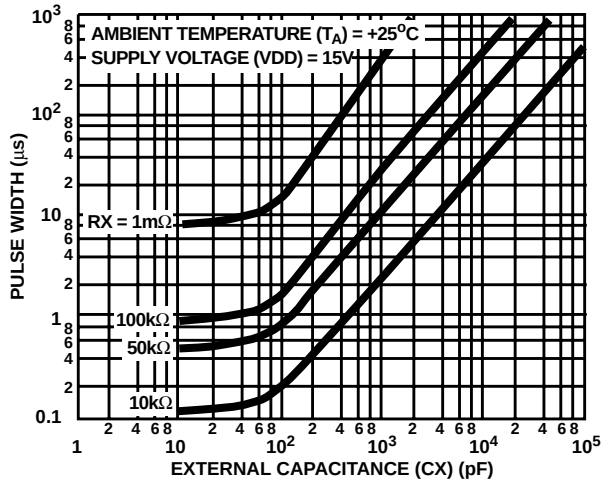


FIGURE 16. TYPICAL PULSE WIDTH AS A FUNCTION OF EXTERNAL CAPACITANCE (VDD = 15V)

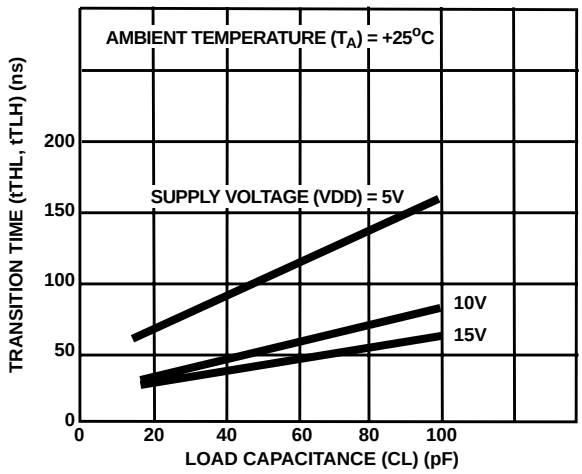


FIGURE 17. TYPICAL TRANSITION TIME AS A FUNCTION OF LOAD CAPACITANCE

Typical Performance Characteristics (Continued)

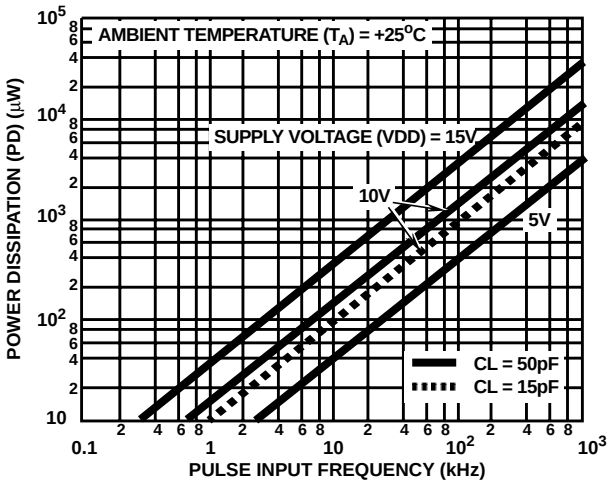


FIGURE 18. TYPICAL DYNAMIC POWER DISSIPATION AS A FUNCTION OF INPUT PULSE FREQUENCY

Applications

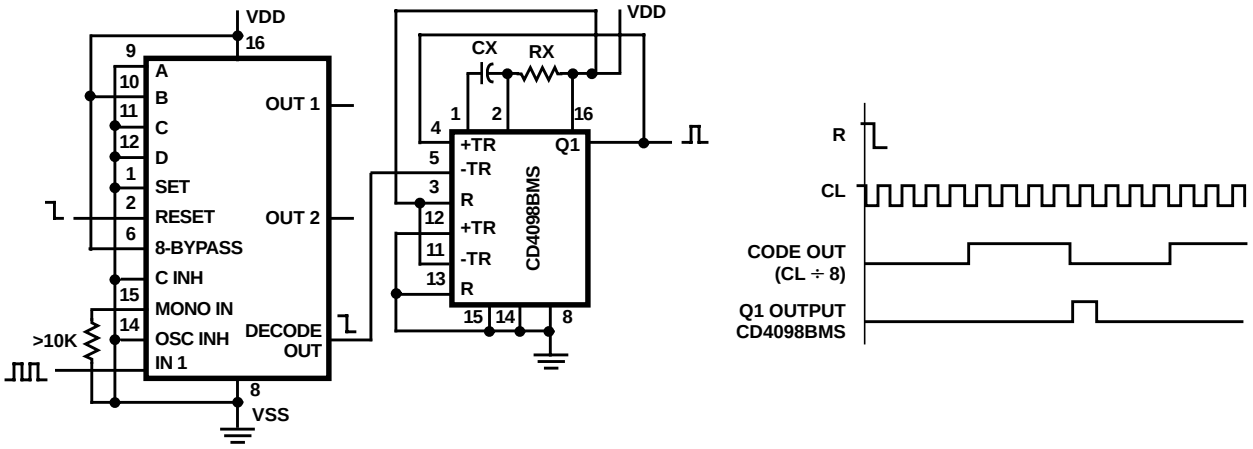


FIGURE 19. APPLICATION SHOWING USE OF CD4098BMS AND CD4536BMS TO GET DECODE PULSE 8 CLOCK PULSES AFTER RESET PULSE

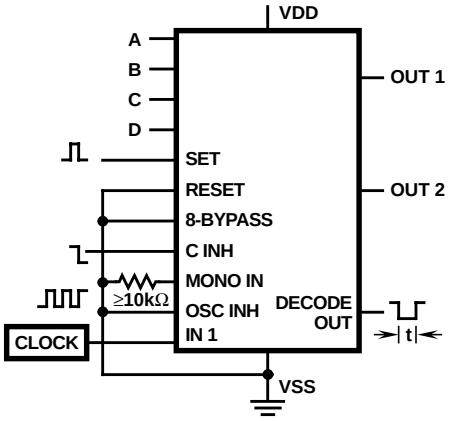


FIGURE 20. TIME INTERVAL CONFIGURATION USING EXTERNAL CLOCK; SET AND CLOCK INHIBIT FUNCTIONS

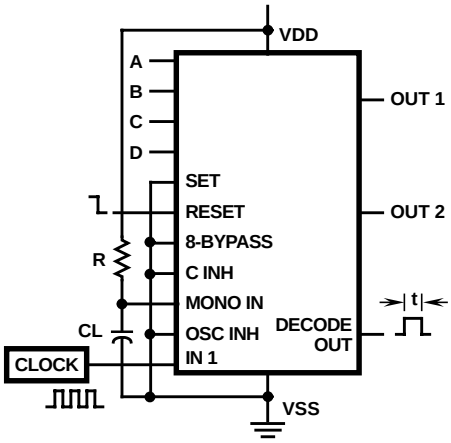


FIGURE 21. TIME INTERVAL CONFIGURATION USING EXTERNAL CLOCK; RESET AND OUTPUT MONOSTABLE TO ACHIEVE A PULSE OUTPUT

Applications (Continued)

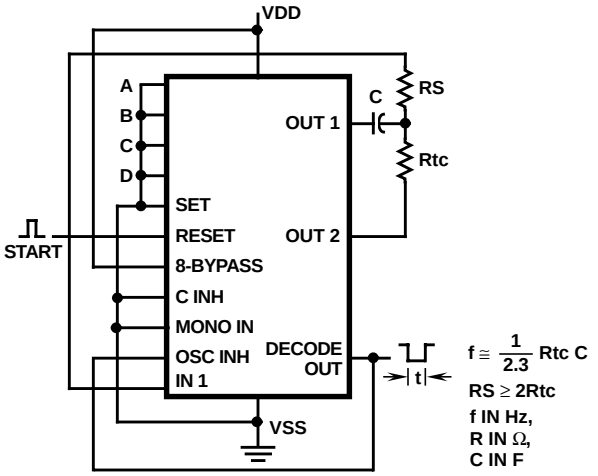


FIGURE 22. TIME INTERVAL CONFIGURATION USING ON-CHIP RC OSCILLATOR AND RESET INPUT TO INITIATE TIME INTERVAL

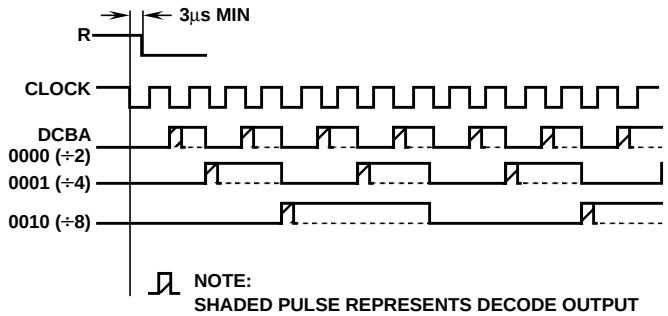


FIGURE 23. TIMING DIAGRAM

DECODE OUT SELECTION TABLE

D	C	B	A	NUMBER OF STAGES IN DIVIDER CHAIN	
				8-BYPASS = 0	8-BYPASS = 1
0	0	0	0	9	1
0	0	0	1	10	2
0	0	1	0	11	3
0	0	1	1	12	4
0	1	0	0	13	5
0	1	0	1	14	6
0	1	1	0	15	7
0	1	1	1	16	8
1	0	0	0	17	9
1	0	0	1	18	10
1	0	1	0	19	11
1	0	1	1	20	12
1	1	0	0	21	13
1	1	0	1	22	14
1	1	1	0	23	15
1	1	1	1	24	16

0 = Low Level 1 = High Level

Functional Block Diagram

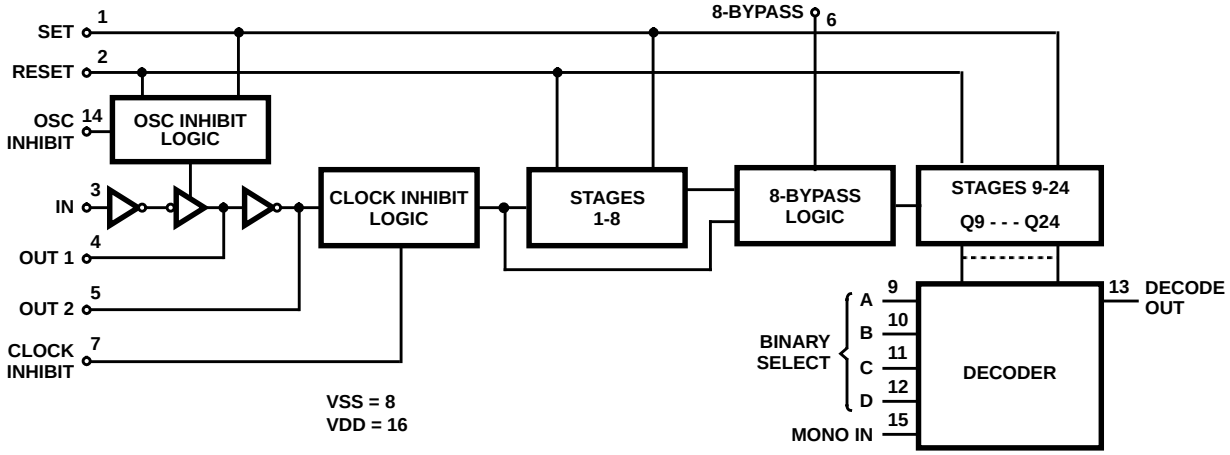


FIGURE 24.

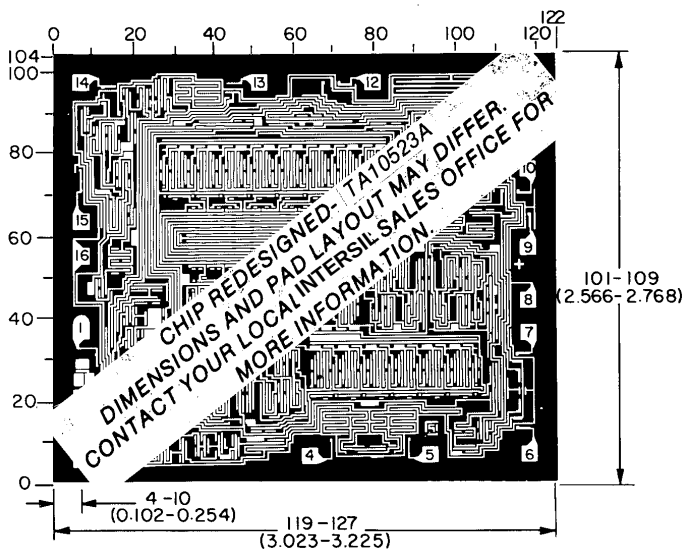
FUNCTIONAL TEST SEQUENCE

INPUTS				OUTPUTS	COMMENTS
IN 1	SET	RESET	8-BYPASS	DECODE OUT Q1 THRU 24	
1	0	1	1	0	ALL 24 STEPS ARE IN RESET MODE
1	1	1	1	0	Counter is in three 8-stage section in parallel mode
0	1	1	1	0	First “1” to “0” transition of clock
1 0 - - -	1	1	1		255 “1” to “0” transitions are clocked in the counter
0	1	1	1	1	The 255 “1” to “0” transition
0	0	0	0	1	Counter converted back to 24 stages in series mode. Set and Reset must be connected together and simultaneously go from “1” to “0”
1	0	0	0	1	In1 Switches to a “1”
0	0	0	0	0	Counter Ripples from an all “1” state to an all “0” state

Functional Test Sequence

Test Function has been included for the reduction of test time required to exercise all 24 counter stages. This test function divides the counter into three 8-stage sections and 255 counts are loaded in each of the 8-stage sections in parallel. All flip-flops are now at a “1”. The counter is now returned to the normal 24 steps in series configuration. One more pulse is entered into In1 which will cause the counter to ripple from an all “1” state to an all “0” state.

Chip Dimensions and Pad Layout



Dimensions in parenthesis are in millimeters and are derived from the basic inch dimensions as indicated. Grid graduations are in mils (10^{-3} inch).

METALLIZATION: Thickness: 11kÅ – 14kÅ, AL.
PASSIVATION: 10.4kÅ - 15.6kÅ, Silane
BOND PADS: 0.004 inches X 0.004 inches MIN
DIE THICKNESS: 0.0198 inches - 0.0218 inches