National Semiconductor

DM74LS563
Octal D-Type Latch with TRI-STATE® Outputs

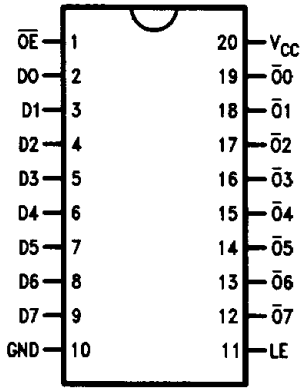
General Description

The 'LS563 is a high speed octal latch with buffered common Latch Enable (LE) and buffered common Output Enable ($\overline{OE}$) inputs.

This device is functionally indentical to the 'LS573, but has inverted outputs.

Connection Diagram

Dual-In-Line Package



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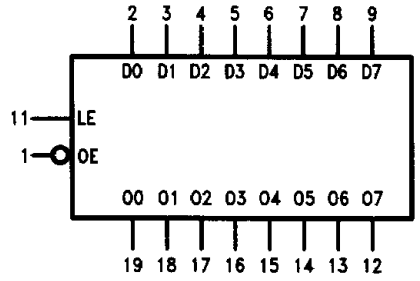
Order Number DM74LS563WM or DM74LS563N
See NS Package Number M20B or N20A

Logic Symbol



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V_{CC} = Pin 20
GND = Pin 10

Pin Names	Description
D0–D7	Data Inputs
LE	Latch Enable Input (Active HIGH)
$\overline{OE}$	TRI-STATE Output Enable Input (Active LOW)
$\overline{O}0$–$\overline{O}7$	TRI-STATE Latch Outputs

Absolute Maximum Ratings (Note)

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/Distributors for availability and specifications.

Supply Voltage	7V
Input Voltage	7V
Operating Free Air Temperature Range	
DM74LS	0°C to +70°C
Storage Temperature Range	−65°C to +150°C

Note: *The "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed. The device should not be operated at these limits. The parametric values defined in the "Electrical Characteristics" table are not guaranteed at the absolute maximum ratings. The "Recommended Operating Conditions" table will define the conditions for actual device operation.*

Recommended Operating Conditions

Symbol	Parameter	DM74LS563			Units
		Min	Nom	Max	
V_{CC}	Supply Voltage	4.75	5	5.25	V
V_{IH}	High Level Input Voltage	2			V
V_{IL}	Low Level Input Voltage			0.8	V
I_{OH}	High Level Output Current			−2.6	mA
I_{OL}	Low Level Output Current			24	mA
T_A	Free Air Operating Temperature	0		70	°C
t_s (H) t_s (L)	Setup Time HIGH or LOW Dn to LE	0 0			ns
t_h (H) t_h (L)	Hold Time HIGH or LOW Dn to LE	10 10			ns
t_w (H) t_w (L)	LE Pulse Width HIGH or LOW	15 15			ns

Electrical Characteristics over recommended operating free air temperature range (unless otherwise noted)

Symbol	Parameter	Conditions	Min	Typ (Note 1)	Max	Units
V_I	Input Clamp Voltage	V_{CC} = Min, I_I = −18 mA			−1.5	V
V_{OH}	High Level Output Voltage	V_{CC} = Min, I_{OH} = Max, V_{IL} = Max, V_{IH} = Min	2.4	3.3		V
V_{OL}	Low Level Output Voltage	V_{CC} = Min, I_{OL} = Max, V_{IL} = Max, V_{IH} = Min		0.35	0.5	V
		I_{OL} = 12 mA, V_{CC} = Min		0.25	0.4	
I_I	Input Current @ Max Input Voltage	V_{CC} = Max, V_I = 7V			0.1	mA
I_{IH}	High Level Input Current	V_{CC} = Max, V_I = 2.7V			20	μA
I_{IL}	Low Level Input Current	V_{CC} = Max, V_I = 0.5V			−20	μA
I_{OZH}	Off-State Output Current with High Level Output Voltage Applied	V_{CC} = Max, V_O = 2.4V V_{IH} = Min, V_{IL} = Max			20	μA
I_{OZL}	Off-State Output Current with Low Level Output Voltage Applied	V_{CC} = Max, V_O = 0.4V V_{IH} = Min, V_{IL} = Max			−20	μA
I_{OS}	Short Circuit Output Current	V_{CC} = Max (Note 2)	−20		−100	mA
I_{CC}	Supply Current	V_{CC} = Max (Note 3)			40	mA

Note 1: All typicals are at V_{CC} = 5V, T_A = 25°C.

Note 2: Not more than one output should be shorted at a time, and the duration should not exceed one second.

Note 3: I_{CC} is measured with the DATA inputs grounded and the OUTPUT CONTROLS at 4.5V.

Switching Characteristics

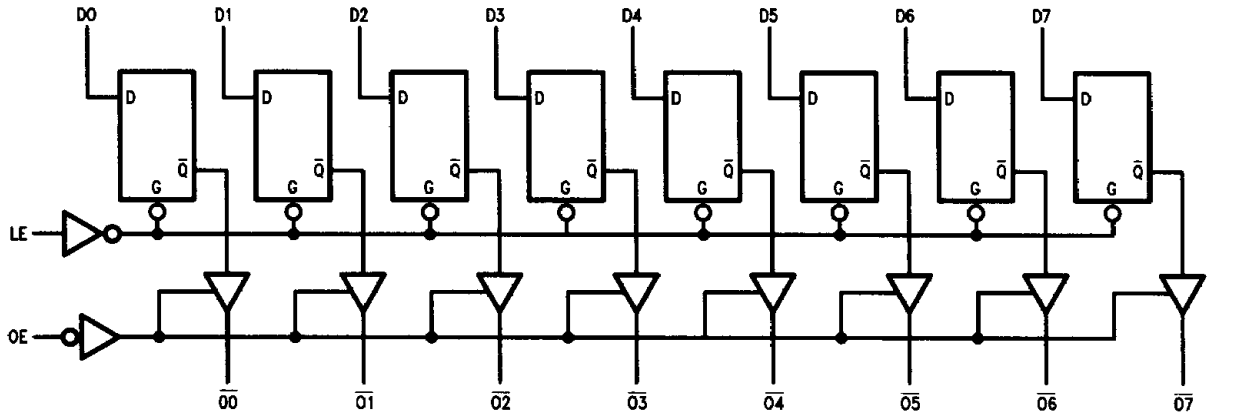
V_{CC} = +5.0V, T_A = +25°C (See Section 1 for test waveforms and output loading)

Symbol	Parameter	R_L = 2 kΩ C_L = 15 pF		Units
		Min	Max	
t_{PLH} t_{PHL}	Propagation Delay Dn to On		23 25	ns
t_{PLH} t_{PHL}	Propagation Delay LE to On		35 35	ns
t_{PZH} t_{PZL}	Output Enable Time		28 36	ns
t_{PHZ} t_{PLZ}	Output Disable Time		20 25	ns

Functional Description

The 'LS563 contains eight D-type latches with TRI-STATE output buffers. When the Latch Enable (LE) input is HIGH, data on the Dn inputs enters the latches. In this condition the latches are transparent, i.e., a latch output will change state each time its D input changes. When LE is LOW the latches store the information that was present on the D inputs a setup time preceding the HIGH-to-LOW transition of LE. The TRI-STATE buffers are controlled by the Output Enable ($\overline{OE}$) input. When $\overline{OE}$ is LOW, the buffers are in the bi-state mode. When $\overline{OE}$ is HIGH the buffers are in the high impedance mode but this does not interfere with entering new data into the latches.

Logic Diagram



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