54/74195
54LS/74LS195A
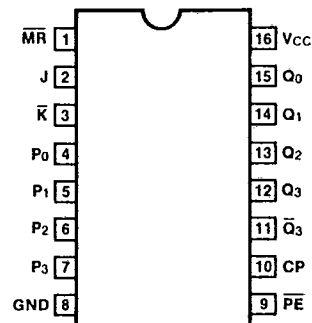## UNIVERSAL 4-BIT SHIFT REGISTER

CONNECTION DIAGRAM
PINOUT A

DESCRIPTION—The '195 is a high speed 4-bit shift register offering typical shift frequencies of 50 MHz. It is useful for a wide variety of register and counting applications. The '195 is pin and functionally identical to the 9300, 93L00 and 93H00.

- **TYPICAL SHIFT RIGHT FREQUENCY OF 50 MHz ('LS195A)**
- **ASYNCHRONOUS MASTER RESET**
- **J, K̄ INPUTS TO FIRST STAGE**
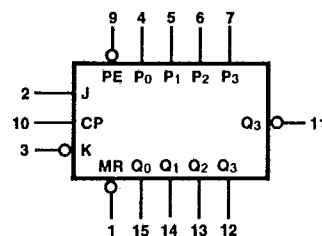- **FULLY SYNCHRONOUS SERIAL OR PARALLEL DATA TRANSFERS**

LOGIC SYMBOL

V_{CC} = Pin 16
Gnd = Pin 8

ORDERING CODE: See Section 9

PKGS	PIN OUT	COMMERCIAL GRADE V_{CC} = +5.0 V ±5%, T_A = 0°C to +70°C	MILITARY GRADE V_{CC} = +5.0 V ±10%, T_A = -55°C to +125°C	PKG TYPE
Plastic DIP (P)	A	74195PC, 74LS195APC		9B
Ceramic DIP (D)	A	74195DC, 74LS195ADC	54195DM, 54LS195ADM	6B
Flatpak (F)	A	74195FC, 74LS195AFC	54195FM, 54LS195AFM	4L

INPUT LOADING/FAN-OUT: See Section 3 for U.L. definitions

PIN NAMES	DESCRIPTION	54/74 (U.L.) HIGH/LOW	54/74LS (U.L.) HIGH/LOW
PE	Parallel Enable Input (Active LOW)	1.0/1.0	0.5/0.25
$P_0 — P_3$	Parallel Data Inputs	1.0/1.0	0.5/0.25
J	First Stage J Input (Active HIGH)	1.0/1.0	0.5/0.25
K̄	First Stage K Input (Active LOW)	1.0/1.0	0.5/0.25
CP	Clock Pulse Input (Active Rising Edge)	1.0/1.0	0.5/0.25
MR	Asynchronous Master Reset Input (Active LOW)	1.0/1.0	0.5/0.25
$Q_0 — Q_3$	Parallel Outputs	20/10	10/5.0 (2.5)
Q̄₃	Complementary Last Stage Output (Active LOW)	20/10	10/5.0 (2.5)

FUNCTIONAL DESCRIPTION — The Logic Diagram and Truth Table indicate the functional characteristics of the '195 4-bit shift register. The device is useful in a wide variety of shifting, counting and storage applications. It performs serial, parallel, serial to parallel, or parallel to serial data transfers at very high speeds.

The '195 has two primary modes of operation, shift right ($Q_0 \rightarrow Q_1$) and parallel load, which are controlled by the state of the Parallel Enable ($\overline{PE}$) input. When the $\overline{PE}$ input is HIGH, serial data enters the first flip-flop Q_0 via the J and $\overline{K}$ inputs and is shifted one bit in the direction $Q_0 \rightarrow Q_1 \rightarrow Q_2 \rightarrow Q_3$ following each LOW-to-HIGH clock transition. The $J\overline{K}$ inputs provide the flexibility of the JK type input for special applications, and the simple D type input for general applications by tying the two pins together. When the $\overline{PE}$ input is LOW, the '195 appears as four common clocked D flip-flops. The data on the parallel inputs P_0, P_1, P_2, P_3 is transferred to the respective Q_0, Q_1, Q_2, Q_3 outputs following the LOW-to-HIGH clock transition. Shift left operation ($Q_3 \rightarrow Q_2$) can be achieved by tying the Q_n outputs to the P_{n-1} inputs and holding the $\overline{PE}$ input LOW.

All serial and parallel data transfers are synchronous, occuring after each LOW-to-HIGH clock transition. Since the '195 utilizes edge-triggering, there is no restriction on the activity of the J, $\overline{K}$, P_n and $\overline{PE}$ inputs for logic operation — except for the setup and release time requirements. A LOW on the asynchronous Master Reset ($\overline{MR}$) input sets all Q outputs LOW, independent of any other input condition.

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MODE SELECT TABLE

OPERATING MODES	INPUTS					OUTPUTS				
	$\overline{MR}$	$\overline{PE}$	J	$\overline{K}$	P_n	Q_0	Q_1	Q_2	Q_3	$\overline{Q_3}$
Asynchronous Reset	L	X	X	X	X	L	L	L	L	H
Shift, Set First Stage	H	h	h	h	X	H	q_0	q_1	q_2	$\overline{q_2}$
Shift, Reset First Stage	H	h	l	l	X	L	q_0	q_1	q_2	$\overline{q_2}$
Shift, Toggle First Stage	H	h	h	l	X	$\overline{q_0}$	q_0	q_1	q_2	$\overline{q_2}$
Shift, Retain First Stage	H	h	l	h	X	q_0	q_0	q_1	q_2	$\overline{q_2}$
Parallel Load	H	l	X	X	p_n	p_0	p_1	p_2	p_3	$\overline{p_3}$

H = HIGH Voltage Level   L = LOW Voltage Level   X = Immaterial
l = LOW voltage level one setup time prior to the LOW to HIGH clock transition.
h = HIGH voltage level one setup time prior to the LOW to HIGH clock transition.
p_n (q_n) = Lower case letters indicate the state of the referenced input (or output) one setup time prior to the LOW to HIGH clock transition.

LOGIC DIAGRAM
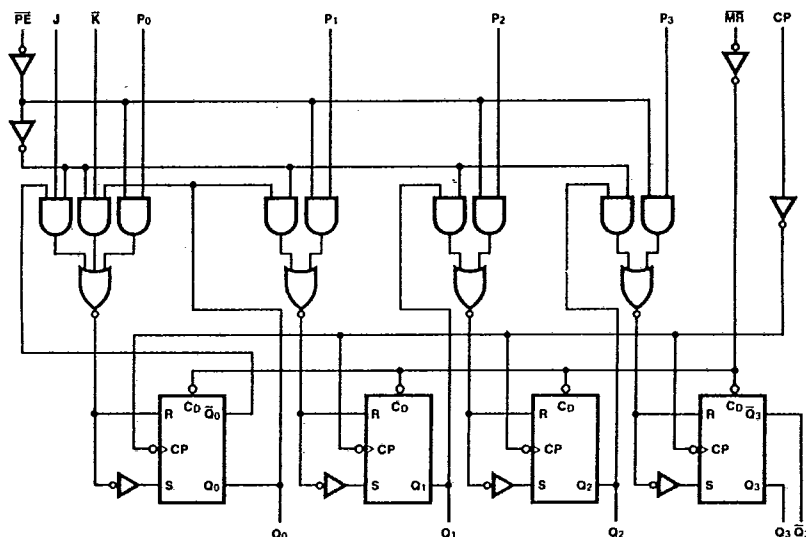
DC CHARACTERISTICS OVER OPERATING TEMPERATURE RANGE (unless otherwise specified)

SYMBOL	PARAMETER	54/74		54/74LS		UNITS	CONDITIONS
		Min	Max	Min	Max		
I_{CC}	Power Supply Current		63		21	mA	V_{CC} = Max, $\overline{PE}$ = Gnd J, $\overline{K}$, P_n, $\overline{MR}$ = 4.5 V CP = ⌐

AC CHARACTERISTICS: V_{CC} = +5.0 V, T_A = +25°C (See Section 3 for waveforms and load configurations)

SYMBOL	PARAMETER	54/74		54/74LS		UNITS	CONDITIONS
		C_L = 15 pF R_L = 400 Ω		C_L = 15 pF			
		Min	Max	Min	Max		
f_{max}	Maximum Clock Frequency	30		30		MHz	Figs. 3-1, 3-8
t_{PLH} t_{PHL}	Propagation Delay CP to Q_n		22 26		21 24	ns	
t_{PHL}	Propagation Delay, $\overline{MR}$ to Q_n		30		26	ns	Figs. 3-1, 3-16

AC OPERATING REQUIREMENTS: V_{CC} = +5.0 V, T_A = +25°C

SYMBOL	PARAMETER	54/74		54/74LS		UNITS	CONDITIONS
		Min	Max	Min	Max		
t_s (H) t_s (L)	Setup Time HIGH or LOW J, $\overline{K}$ or P_n to CP	20 20		15 15		ns	
t_h (H) t_h (L)	Hold Time HIGH or LOW J, $\overline{K}$ or P_n to CP	0 0		0 0		ns	Fig. 3-6
t_s (H) t_s (L)	Setup Time HIGH or LOW $\overline{PE}$ to CP	25 25		25 25		ns	
t_h (H) t_h (L)	Hold Time HIGH or LOW $\overline{PE}$ to CP	-10 -10		0 0		ns	
t_w (H)	CP Pulse Width HIGH	16		16		ns	Fig. 3-8
t_w (L)	$\overline{MR}$ Pulse Width LOW	12		12		ns	Fig. 3-16
t_{rec}	Recovery Time, $\overline{MR}$ to CP	25		20		ns	