

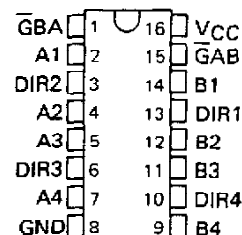
# SN54LS446, SN54LS449, SN74LS446, SN74LS449 QUADRUPLE BUS TRANSCEIVERS WITH INDIVIDUAL DIRECTION CONTROLS

SDLS178

D2613, OCTOBER 1980—REVISED MARCH 1988

SN54LS446, SN54LS449 . . . J PACKAGE  
SN74LS446, SN74LS449 . . . D OR N PACKAGE

(TOP VIEW)



- 3-State Outputs Drive Bus Lines Directly
- P-N-P Inputs Reduce DC Loading on Bus Line
- Hysteresis at Bus Inputs Improves Noise Margins
- Flow-Thru Data Pinout (B Bus Opposite A Bus)
- Choice of True ('LS449) and Inverting ('LS446)

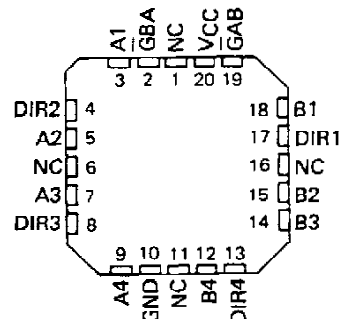
## description

These quadruple bus transceivers are designed for data transmission from individual lines of the A bus to individual lines of the B bus or the reverse, depending on the logic levels at the direction-control pins DIR1 through DIR4. These direction controls (one for each channel) allow maximum flexibility in timing. The enable inputs  $\overline{G}BA$  and  $\overline{G}AB$  can be used to disable the A or B outputs respectively, or to disable both buses for effective isolation.

The SN54LS446 and SN54LS449 are characterized for operation over the full military temperature range of  $-55^{\circ}\text{C}$  to  $125^{\circ}\text{C}$ . The SN74LS446 and SN74LS449 are characterized for operation from  $0^{\circ}\text{C}$  to  $70^{\circ}\text{C}$ .

SN54LS446, SN54LS449 . . . FK PACKAGE

(TOP VIEW)



NC - No internal connection

FUNCTION TABLE

ENABLE		DIRECTION DIR	OPERATION	
$\overline{G}BA$	$\overline{G}AB$		'LS446	'LS449
H	H	X	Isolation	Isolation
X	L	H	$\overline{A}$ data to B Bus	A data to B Bus
L	X	L	$\overline{B}$ data to A Bus	B data to A Bus
X	H	H	Isolation	Isolation
H	X	L	Isolation	Isolation

H = high level, L = low level, X = irrelevant

## absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply voltage, $V_{CC}$ (see Note 1)	7 V
Input voltage	7 V
Off-state output voltage	5.5 V
Operating free-air temperature range: SN54LS'	$-55^{\circ}\text{C}$ to $125^{\circ}\text{C}$
SN74LS'	$0^{\circ}\text{C}$ to $70^{\circ}\text{C}$
Storage temperature range	$-65^{\circ}\text{C}$ to $150^{\circ}\text{C}$

NOTE 1: Voltage values are with respect to the network ground terminal.

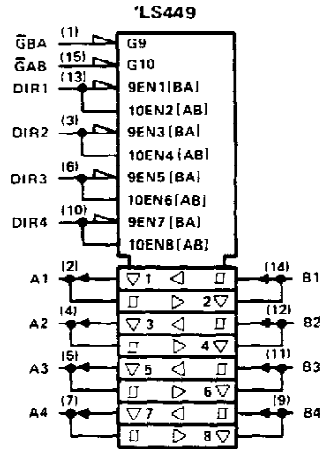
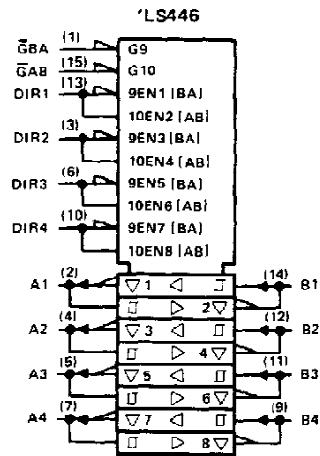
PRODUCTION DATA documents contain information current as of publication date. Products conform to specifications per the terms of Texas Instruments standard warranty. Production processing does not necessarily include testing of all parameters.

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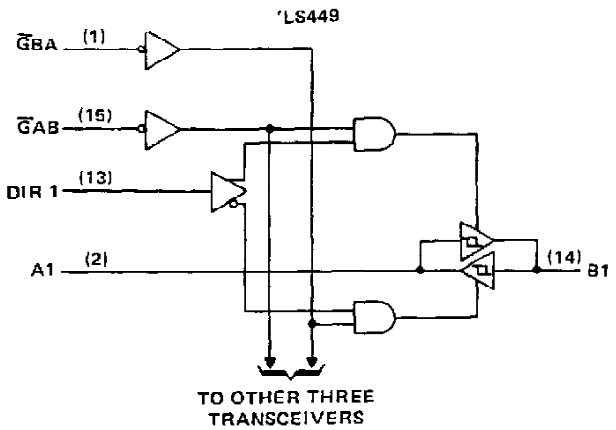
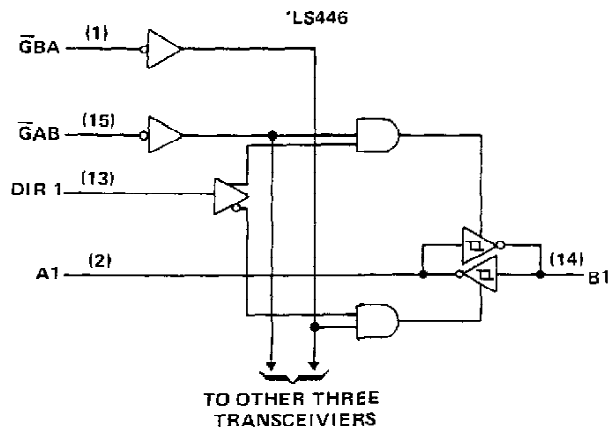
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# **SN54LS446, SN54LS449, SN74LS446, SN74LS449** **QUADRUPLE BUS TRANSCEIVERS WITH INDIVIDUAL DIRECTION CONTROLS**

logic symbols†

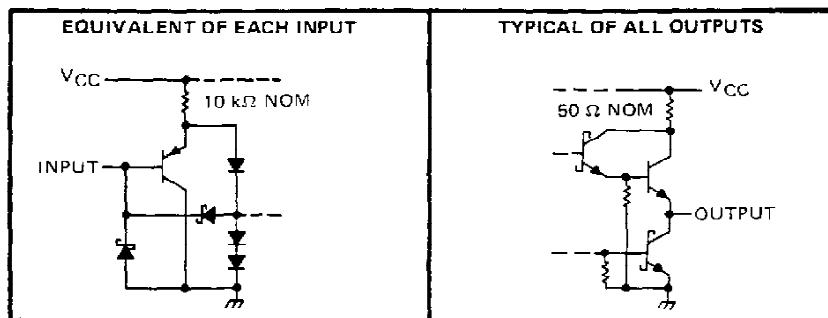


logic diagrams (positive logic)



† These symbols are in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.  
 Pin numbers shown are for D, J, and N packages.

schematics of inputs and outputs



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# SN54LS446, SN54LS449, SN74LS446, SN74LS449 QUADRUPLE BUS TRANSCEIVERS WITH INDIVIDUAL DIRECTION CONTROLS

## recommended operating conditions

PARAMETER	SN54LS446 SN54LS449			SN74LS446 SN74LS449			UNIT
	MIN	NOM	MAX	MIN	NOM	MAX	
Supply voltage, $V_{CC}$ (see Note 1)	4.5	5	5.5	4.75	5	5.25	V
High-level output current, $I_{OH}$			-12			-15	mA
Low-level output current, $I_{OL}$			12			24	mA
Operating free-air temperature, $T_A$	-55		125	0		70	°C

NOTE 1: Voltage values are with respect to network ground terminal.

## electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER			TEST CONDITIONS†		SN54LS446 SN54LS449		SN74LS446 SN74LS449		UNIT
					MIN	TYP‡	MAX	MIN	
V <sub>IH</sub>	High-level input voltage				2		2		V
V <sub>IL</sub>	Low-level input voltage					0.6		0.7	V
V <sub>IK</sub>	Input clamp voltage		V <sub>CC</sub> = MIN, I <sub>I</sub> = -18 mA			-1.5		-1.5	V
Hysteresis (V <sub>T+</sub> - V <sub>T-</sub> ), A or B input			V <sub>CC</sub> = MIN		0.1	0.4	0.2	0.4	V
V <sub>OH</sub>	High-level output voltage	V <sub>CC</sub> = MIN, V <sub>IH</sub> = 2 V, V <sub>IL</sub> = V <sub>IL</sub> max	I <sub>OH</sub> = -3 mA	2.4	3.4	2.4	3.4	V	
			I <sub>OH</sub> = MAX	2		2			
V <sub>OL</sub>	Low-level output voltage	V <sub>CC</sub> = MIN, V <sub>IH</sub> = 2 V, V <sub>IL</sub> = V <sub>IL</sub> max	I <sub>OL</sub> = 12 mA	0.25	0.4	0.25	0.4	V	
			I <sub>OL</sub> = 24 mA			0.35	0.5		
I <sub>OZH</sub>	Off-state output current, high-level voltage applied		V <sub>CC</sub> = MAX, $\bar{G}$ at 2 V, V <sub>O</sub> = 2.7 V			20		20	μA
I <sub>OZL</sub>	Off-state output current, low-level voltage applied		V <sub>CC</sub> = MAX, $\bar{G}$ at 2 V, V <sub>O</sub> = 0.4 V			-0.4		-0.4	mA
I <sub>I</sub>	Input current at maximum input voltage	A or B	V <sub>CC</sub> = MAX, V <sub>I</sub> = 5.5 V		0.1		0.1	mA	
		$\bar{G}AB$ or $\bar{G}BA$		V <sub>I</sub> = 7 V	0.1		0.1		
I <sub>IH</sub>	High-level input current		V <sub>CC</sub> = MAX, V <sub>I</sub> = 2.7 V			20		20	μA
I <sub>IL</sub>	Low-level input current		V <sub>CC</sub> = MAX, V <sub>I</sub> = 0.4 V			-0.4		-0.4	mA
I <sub>OS</sub>	Short-circuit output current§		V <sub>CC</sub> = MAX		-40	-225	-40	-225	mA
I <sub>CC</sub>	Total supply current	'LS446	V <sub>CC</sub> = MAX, Outputs open	Outputs high	35	56	35	56	mA
				Outputs low	39	63	39	63	
				Outputs at Hi-Z	42	68	42	68	
		'LS449		Outputs high	42	68	42	68	
				Outputs low	47	75	47	75	
				Outputs at Hi-Z	50	80	50	80	

† For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions.

‡ All typical values are at  $V_{CC} = 5 \text{ V}$ ,  $T_A = 25^\circ\text{C}$ .

§ Not more than one output should be shorted at a time, and duration of the short-circuit should not exceed one second.



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**SN54LS446, SN54LS449, SN74LS446, SN74LS449**  
**QUADRUPLE BUS TRANSCEIVERS WITH INDIVIDUAL DIRECTION CONTROLS**

switching characteristics at  $V_{CC} = 5\text{ V}$ ,  $T_A = 25^\circ\text{C}$

PARAMETER	FROM (INPUT)	TO (OUTPUT)	TEST CONDITIONS	'LS446			'LS449			UNIT
				MIN	TYP	MAX	MIN	TYP	MAX	
$t_{PLH}$ Propagation delay time, low-to-high-level output	A	B	$C_L = 45\text{ pF}$ ,  $R_L = 667\ \Omega$ ,  See Note 2	8	13		10	15		ns
	B	A		8	13		10	16		
$t_{PHL}$ Propagation delay time, high-to-low-level output	A	B		7	12		11	17		ns
	B	A		7	12		11	17		
$t_{PZL}$ Output enable time to low level	$\overline{G}BA$	A	See Note 2	24	40		21	35		ns
	$\overline{G}AB$	B		24	40		21	35		
$t_{PZH}$ Output enable time to high level	$\overline{G}BA$	A		15	25		18	30		ns
	$\overline{G}AB$	B		15	25		18	30		
$t_{PLZ}$ Output disable time from low level	$\overline{G}BA$	A	$C_L = 5\text{ pF}$ , $R_L = 667\ \Omega$ , See Note 2	14	25		14	25		ns
	$\overline{G}AB$	B		14	25		14	25		
$t_{PHZ}$ Output disable time from high level	$\overline{G}BA$	A		10	15		10	15		ns
	$\overline{G}AB$	B		10	15		10	15		

NOTE 2: Load circuits and voltage waveforms are shown in Section 1.

  
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