CD40109BMS

December 1992

CMOS Quad Low-to-High Voltage Level Shifter

Features

- **High Voltage Type (20V Rating)**
- **Independence of Power Supply Sequence Considerations**
  - **VCC can Exceed VDD**
  - **Input Signals can Exceed Both VCC and VDD**
- **Up and Down Level Shifting Capability**
- **Three-State Outputs with Separate Enable Controls**
- **100% Tested for Quiescent Current at 20V**
- **5V, 10V and 15V Parametric Ratings**
- **Maximum Input Current of 1μA at 18V Over Full Package Temperature Range; 100nA at 18V and +25^{o}C**
- **Noise Margin (Over Full Package/Temperature Range)**
  - **1V at VCC = 5V, VDD = 10V**
  - **2V at VCC = 10V, VDD = 15V**
- **Standardized Symmetrical Output Characteristics**
- **Meets All Requirements of JEDEC Tentative Standard No. 13B, “Standard Specifications for Description of ‘B’ Series CMOS Devices”**

Applications

- **High or Low Level Shifting with Three-State Outputs for Unidirectional or Bidirectional Bussing**
- **Isolation of Logic Subsystems Using Separate Power Supplies from Supply Sequencing, Supply Loss and Supply Regulation Considerations**

Description

CD40109BMS contains four low-to-high voltage level shifting circuits. Each circuit will shift a low voltage digital logic input signal (A, B, C, D) with logical 1 = VCC and logical 0 = VSS to a higher voltage output signal (E, F, G, H) with logical 1 = VDD and logical 0 = VSS.

The CD40109BMS, unlike other low-to-high level shifting circuits, does not require the presence of the high voltage supply (VDD) before the application of either the low voltage supply (VCC) or the input signals. There are no restrictions on the sequence of application of VDD, VCC, or the input signals. In addition, with one exception there are no restrictions on the relative magnitudes of the supply voltages or input signals within the device maximum ratings, provided that the input signal swings between VSS and at least 0.7VCC; VCC may exceed VDD, and input signals may exceed VCC and VDD. When operated in the mode VCC > VDD, the CD40109BMS will operate as a high-to-low level shifter.

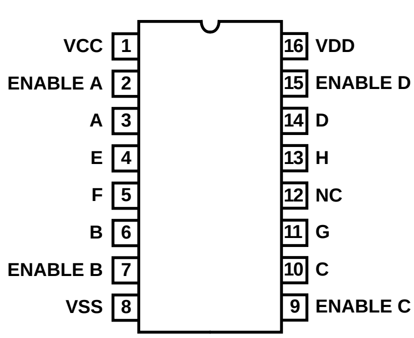
The CD40109BMS also features individual three-state output capability. A low level on any of the separately enabled three-state output controls produces a high impedance state in the corresponding output.

The CD40109BMS is supplied in these 16-lead outline packages:

Braze Seal DIP	H4T
Frit Seal DIP	H1E
Ceramic Flatpack	H6W

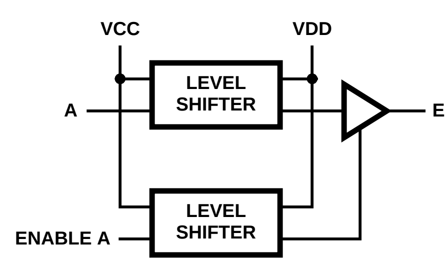
Pinout

CD40109BMS
TOP VIEW



Functional Diagram

1 OF 4 UNITS



Absolute Maximum Ratings

DC Supply Voltage Range, (VDD) . . . . -0.5V to +20V
(Voltage Referenced to VSS Terminals)
Input Voltage Range, All Inputs . . . .-0.5V to VDD +0.5V
DC Input Current, Any One Input . . . .±10mA
Operating Temperature Range. . . . . -55°C to +125°C
Package Types D, F, K, H
Storage Temperature Range (TSTG) . . . . -65°C to +150°C
Lead Temperature (During Soldering) . . . . +265°C
At Distance 1/16 ± 1/32 Inch (1.59mm ± 0.79mm) from case for 10s Maximum

Reliability Information

Thermal Resistance . . . . θ_{ja} θ_{jc}
Ceramic DIP and FRIT Package . . . . . 80°C/W 20°C/W
Flatpack Package . . . . 70°C/W 20°C/W
Maximum Package Power Dissipation (PD) at +125°C
For T_A = -55°C to +100°C (Package Type D, F, K) 500mW
For T_A = +100°C to +125°C (Package Type D, F, K). . . . . .Derate Linearity at 12mW/°C to 200mW
Device Dissipation per Output Transistor 100mW
For T_A = Full Package Temperature Range (All Package Types)
Junction Temperature . . . . +175°C

TABLE 1. DC ELECTRICAL PERFORMANCE CHARACTERISTICS

PARAMETER	SYMBOL	CONDITIONS (NOTE 1)		GROUP A SUBGROUPS	TEMPERATURE	LIMITS MIN	LIMITS MAX	UNITS
Supply Current	IDD	VDD = 20V, VIN = VDD or GND		1	+25°C	-	2	µA
				2	+125°C	-	200	µA
		VDD = 18V, VIN = VDD or GND		3	-55°C	-	2	µA
Input Leakage Current	IIL	VIN = VDD or GND	VDD = 20	1	+25°C	-100	-	nA
				2	+125°C	-1000	-	nA
			VDD = 18V	3	-55°C	-100	-	nA
Input Leakage Current	IIH	VIN = VDD or GND	VDD = 20	1	+25°C	-	100	nA
				2	+125°C	-	1000	nA
			VDD = 18V	3	-55°C	-	100	nA
Output Voltage	VOL15	VDD = 15V, No Load		1, 2, 3	+25°C, +125°C, -55°C	-	50	mV
Output Voltage	VOH15	VDD = 15V, No Load (Note 3)		1, 2, 3	+25°C, +125°C, -55°C	14.95	-	V
Output Current (Sink)	IOL5	VDD = 5V, VOUT = 0.4V		1	+25°C	0.53	-	mA
Output Current (Sink)	IOL10	VDD = 10V, VOUT = 0.5V		1	+25°C	1.4	-	mA
Output Current (Sink)	IOL15	VDD = 15V, VOUT = 1.5V		1	+25°C	3.5	-	mA
Output Current (Source)	IOH5A	VDD = 5V, VOUT = 4.6V		1	+25°C	-	-0.53	mA
Output Current (Source)	IOH5B	VDD = 5V, VOUT = 2.5V		1	+25°C	-	-1.8	mA
Output Current (Source)	IOH10	VDD = 10V, VOUT = 9.5V		1	+25°C	-	-1.4	mA
Output Current (Source)	IOH15	VDD = 15V, VOUT = 13.5V		1	+25°C	-	-3.5	mA
N Threshold Voltage	VNTH	VDD = 10V, ISS = -10µA		1	+25°C	-2.8	-0.7	V
P Threshold Voltage	VPTH	VSS = 0V, IDD = 10µA		1	+25°C	0.7	2.8	V
Functional	F	VDD = 2.8V, VIN = VDD or GND		7	+25°C	VOH > VDD/2	VOL < VDD/2	V
		VDD = 20V, VIN = VDD or GND		7	+25°C			
		VDD = 18V, VIN = VDD or GND		8A	+125°C			
		VDD = 3V, VIN = VDD or GND		8B	-55°C			
Input Voltage Low (Note 2)	VIL	VDD = 10V, VOH > 9V, VOL < 1V VCC = 5V		1, 2, 3	+25°C, +125°C, -55°C	-	1.5	V
Input Voltage High (Note 2)	VIH	VDD = 10V, VOH > 9V, VOL < 1V VCC = 5V		1, 2, 3	+25°C, +125°C, -55°C	3.5	-	V
Input Voltage Low (Note 2)	VIL	VDD = 15V, VOH > 13.5V, VOL < 1.5V, VCC = 10V		1, 2, 3	+25°C, +125°C, -55°C	-	3	V
Input Voltage High (Note 2)	VIH	VDD = 15V, VOH > 13.5V, VOL < 1.5V, VCC = 10V		1, 2, 3	+25°C, +125°C, -55°C	7	-	V
Tri-State Output Leakage	IOZL	VIN = VDD or GND VOUT = 0V	VDD = 20V	1	+25°C	-0.4	-	µA
				2	+125°C	-12	-	µA
			VDD = 18V	3	-55°C	-0.4	-	µA
Tri-State Output Leakage	IOZH	VIN = VDD or GND VOUT = VDD	VDD = 20V	1	+25°C	-	0.4	µA
				2	+125°C	-	12	µA
			VDD = 18V	3	-55°C	-	0.4	µA

NOTES: 1. All voltages referenced to device GND, 100% testing being implemented.
2. Go/No Go test with limits applied to inputs.
3. For accuracy, voltage is measured differentially to VDD. Limit is 0.050V max.

TABLE 2. AC ELECTRICAL PERFORMANCE CHARACTERISTICS

PARAMETER	SYMBOL	CONDITIONS	GROUP A SUBGROUPS	TEMPERATURE	LIMITS MIN	LIMITS MAX	UNITS
Propagation Delay Data In to Out Shift Mode L-H	TPHL1	VDD = 10V, VIN = VCC or GND VCC = 5V (Notes 1, 2)	9	+25°C	-	600	ns
			10, 11	+125°C, -55°C	-	810	ns
Propagation Delay Data In to Out Shift Mode L-H	TPLH1	VDD = 10V, VIN = VCC or GND VCC = 5V (Notes 1, 2)	9	+25°C	-	260	ns
			10, 11	+125°C, -55°C	-	351	ns
Propagation Delay Data In to Out Shift Mode H-L	TPHL2	VDD = 5V, VIN = VCC or GND VCC = 10V (Notes 1, 2)	9	+25°C	-	500	ns
			10, 11	+125°C, -55°C	-	675	ns
Propagation Delay Data In to Out Shift Mode H-L	TPLH2	VDD = 5V, VIN = VCC or GND VCC = 10V (Notes 1, 2)	9	+25°C	-	460	ns
			10, 11	+125°C, -55°C	-	621	ns
Transition Time Shift Mode L-H	TTHL1 TTLH1	VDD = 10V, VIN = VDD or GND VCC = 5V (Notes 1, 2)	9	+25°C	-	100	ns
			10, 11	+125°C, -55°C	-	135	ns
Transition Time Shift Mode H-L	TTHL2 TTLH2	VDD = 5V, VIN = VDD or GND VCC = 10V (Notes 1, 2)	9	+25°C	-	200	ns
			10, 11	+125°C, -55°C	-	270	ns
Propagation Delay 3-State Shift Mode L-H	TPHZ1	VDD = 10V, VIN = VCC or GND VCC = 5V (Notes 2, 3)	9	+25°C	-	120	ns
			10, 11	+125°C, -55°C	-	162	ns
Propagation Delay 3-State Shift Mode H-L	TPHZ2	VDD = 5V, VIN = VCC or GND VCC = 10V (Notes 2, 3)	9	+25°C	-	400	ns
			10, 11	+125°C, -55°C	-	540	ns
Propagation Delay 3-State Shift Mode L-H	TPLZ1	VDD = 10V, VIN = VCC or GND VCC = 5V (Notes 2, 3)	9	+25°C	-	740	ns
			10, 11	+125°C, -55°C	-	999	ns
Propagation Delay 3-State Shift Mode H-L	TPLZ2	VDD = 5V, VIN = VCC or GND VCC = 10V (Notes 2, 3)	9	+25°C	-	500	ns
			10, 11	+125°C, -55°C	-	675	ns
Propagation Delay 3-State Shift Mode L-H	TPZH1	VDD = 10V, VIN = VCC or GND VCC = 5V (Notes 2, 3)	9	+25°C	-	640	ns
			10, 11	+125°C, -55°C	-	864	ns
Propagation Delay 3-State Shift Mode H-L	TPZH2	VDD = 5V, VIN = VCC or GND VCC = 10V (Notes 2, 3)	9	+25°C	-	600	ns
			10, 11	+125°C, -55°C	-	810	ns
Propagation Delay 3-State Shift Mode L-H	TPZL1	VDD = 10V, VIN = VCC or GND VCC = 5V (Notes 2, 3)	9	+25°C	-	200	ns
			10, 11	+125°C, -55°C	-	270	ns
Propagation Delay 3-State Shift Mode H-L	TPZL2	VDD = 5V, VIN = VCC or GND VCC = 10V (Notes 2, 3)	9	+25°C	-	400	ns
			10, 11	+125°C, -55°C	-	540	ns

NOTES:

1. CL = 50pF, RL = 200K, Input TR, TF < 20ns.
2. -55°C and +125°C limits guaranteed, 100% testing being implemented.
3. CL = 50pF, RL = 1K, Input TR, TF < 20ns.

TABLE 3. ELECTRICAL PERFORMANCE CHARACTERISTICS

PARAMETER	SYMBOL	CONDITIONS	NOTES	TEMPERATURE	LIMITS MIN	LIMITS MAX	UNITS
Supply Current	IDD	VDD = 5V, VIN = VDD or GND	1, 2	-55°C, +25°C	-	1	µA
				+125°C	-	30	µA
		VDD = 10V, VIN = VDD or GND	1, 2	-55°C, +25°C	-	2	µA
				+125°C	-	60	µA
		VDD = 15V, VIN = VDD or GND	1, 2	-55°C, +25°C	-	2	µA
				+125°C	-	120	µA
Output Voltage	VOL	VDD = 5V, No Load	1, 2	+25°C, +125°C, -55°C	-	50	mV

TABLE 3. ELECTRICAL PERFORMANCE CHARACTERISTICS (Continued)

PARAMETER	SYMBOL	CONDITIONS	NOTES	TEMPERATURE	LIMITS MIN	LIMITS MAX	UNITS
Output Voltage	VOL	VDD = 10V, No Load	1, 2	+25^oC, +125^oC, -55^oC	-	50	mV
Output Voltage	VOH	VDD = 5V, No Load	1, 2	+25^oC, +125^oC, -55^oC	4.95	-	V
Output Voltage	VOH	VDD = 10V, No Load	1, 2	+25^oC, +125^oC, -55^oC	9.95	-	V
Output Current (Sink)	IOL5	VDD = 5V, VOUT = 0.4V	1, 2	+125^oC	0.36	-	mA
				-55^oC	0.64	-	mA
Output Current (Sink)	IOL10	VDD = 10V, VOUT = 0.5V	1, 2	+125^oC	0.9	-	mA
				-55^oC	1.6	-	mA
Output Current (Sink)	IOL15	VDD = 15V, VOUT = 1.5V	1, 2	+125^oC	2.4	-	mA
				-55^oC	4.2	-	mA
Output Current (Source)	IOH5A	VDD = 5V, VOUT = 4.6V	1, 2	+125^oC	-	-0.36	mA
				-55^oC	-	-0.64	mA
Output Current (Source)	IOH5B	VDD = 5V, VOUT = 2.5V	1, 2	+125^oC	-	-1.15	mA
				-55^oC	-	-2.0	mA
Output Current (Source)	IOH10	VDD = 10V, VOUT = 9.5V	1, 2	+125^oC	-	-0.9	mA
				-55^oC	-	-1.6	mA
Output Current (Source)	IOH15	VDD =15V, VOUT = 13.5V	1, 2	+125^oC	-	-2.4	mA
				-55^oC	-	-4.2	mA
Input Voltage Low	VIL	VDD = 10V, VOH > 9V, VOL < 1V VCC = 5V	1, 2	+25^oC, +125^oC, -55^oC	-	1.5	V
Input Voltage High	VIH	VDD = 10V, VOH > 9V, VOL < 1V VCC = 5V	1, 2	+25^oC, +125^oC, -55^oC	3.5	-	V
Propagation Delay Data In to Data Out Shift Mode L-H	TPHL1	VDD = 15V, VCC = 5V	1, 2, 3	+25^oC	-	440	ns
		VDD = 15V, VCC = 10V	1, 2, 3	+25^oC	-	360	ns
Propagation Delay Data In to Out Shift Mode L-H	TPLH1	VDD = 15V, VCC = 5V	1, 2, 3	+25^oC	-	240	ns
		VDD = 15V, VCC = 10V	1, 2, 3	+25^oC	-	140	ns
Propagation Delay Data In to Out Shift Mode H-L	TPHL2	VDD = 5V, VCC = 15V	1, 2, 3	+25^oC	-	500	ns
		VDD = 10V, VCC = 15V	1, 2, 3	+25^oC	-	240	ns
Propagation Delay Data In to Out Shift Mode H-L	TPLH2	VDD = 5V, VCC = 15V	1, 2, 3	+25^oC	-	460	ns
		VDD = 10V, VCC = 15V	1, 2, 3	+25^oC	-	160	ns
Transition Time Shift Mode L-H	TTHL1 TTLH1	VDD = 15V, VCC = 5V	1, 2, 3	+25^oC	-	80	ns
		VDD = 15V, VCC = 10V	1, 2, 3	+25^oC	-	80	ns
Transition Time Shift Mode H-L	TTHL2 TTLH2	VDD = 5V, VCC = 15V	1, 2, 3	+25^oC	-	200	ns
		VDD = 10V, VCC = 15V	1, 2, 3	+25^oC	-	100	ns
Propagation Delay 3-State Shift Mode L-H	TPHZ1	VDD = 15V, VCC = 5V	1, 2, 4	+25^oC	-	150	ns
		VDD = 15V, VCC = 10V	1, 2, 4	+25^oC	-	70	ns
Propagation Delay 3-State Shift Mode H-L	TPHZ2	VDD = 5V, VCC = 5V	1, 2, 4	+25^oC	-	400	ns
		VDD = 10V, VCC = 15V	1, 2, 4	+25^oC	-	80	ns
Propagation Delay 3-State Shift Mode L-H	TPLZ1	VDD = 15V, VCC = 5V	1, 2, 4	+25^oC	-	600	ns
		VDD = 15V, VCC = 10V	1, 2, 4	+25^oC	-	500	ns

TABLE 3. ELECTRICAL PERFORMANCE CHARACTERISTICS (Continued)

PARAMETER	SYMBOL	CONDITIONS	NOTES	TEMPERATURE	LIMITS MIN	LIMITS MAX	UNITS
Propagation Delay 3-State Shift Mode H-L	TPLZ2	VDD = 5V, VCC = 15V	1, 2, 4	$+25^oC$	-	500	ns
		VDD = 10V, VCC = 15V	1, 2, 4	$+25^oC$	-	260	ns
Propagation Delay 3-State Shift Mode L-H	TPZH1	VDD = 15V, VCC = 5V	1, 2, 4	$+25^oC$	-	460	ns
		VDD = 15V, VCC = 10V	1, 2, 4	$+25^oC$	-	360	ns
Propagation Delay 3-State Shift Mode H-L	TPZH2	VDD = 5V, VCC = 15V	1, 2, 4	$+25^oC$	-	600	ns
		VDD = 10V, VCC = 15V	1, 2, 4	$+25^oC$	-	260	ns
Propagation Delay 3-State Shift Mode L-H	TPZL1	VDD = 15V, VCC = 5V	1, 2, 4	$+25^oC$	-	160	ns
		VDD = 15V, VCC = 10V	1, 2, 4	$+25^oC$	-	80	ns
Propagation Delay 3-State Shift Mode H-L	TPZL2	VDD = 5V, VCC = 15V	1, 2, 4	$+25^oC$	-	400	ns
		VDD = 10V, VCC = 15V	1, 2, 4	$+25^oC$	-	80	ns

NOTES:

1. All voltages referenced to device GND.
2. The parameters listed on Table 3 are controlled via design or process and are not directly tested. These parameters are characterized on initial design release and upon design changes which would affect these characteristics.
3. CL = 50pF, RL = 200K, Input TR, TF < 20ns.
4. CL = 50pF, RL = 1K, Input TR, TF < 20ns.

TABLE 4. POST IRRADIATION ELECTRICAL PERFORMANCE CHARACTERISTICS

PARAMETER	SYMBOL	CONDITIONS	NOTES	TEMPERATURE	LIMITS MIN	LIMITS MAX	UNITS
Supply Current	IDD	VDD = 20V, VIN = VDD or GND	1, 4	$+25^oC$	-	7.5	μA
N Threshold Voltage	VNTH	VDD = 10V, ISS = -10μA	1, 4	$+25^oC$	-2.8	-0.2	V
N Threshold Voltage Delta	ΔVTN	VDD = 10V, ISS = -10μA	1, 4	$+25^oC$	-	±1	V
P Threshold Voltage	VTP	VSS = 0V, IDD = 10μA	1, 4	$+25^oC$	0.2	2.8	V
P Threshold Voltage Delta	ΔVTP	VSS = 0V, IDD = 10μA	1, 4	$+25^oC$	-	±1	V
Functional	F	VDD = 18V, VIN = VDD or GND	1	$+25^oC$	VOH > VDD/2	VOL < VDD/2	V
		VDD = 3V, VIN = VDD or GND					
Propagation Delay Time	TPHL TPLH	VDD = 5V	1, 2, 3, 4	$+25^oC$	-	1.35 x $+25^oC$ Limit	ns

NOTES:
1. All voltages referenced to device GND.
2. CL = 50pF, RL = 200K, Input TR, TF < 20ns.
3. See Table 2 for $+25^oC$ limit.
4. Read and Record

TABLE 5. BURN-IN AND LIFE TEST DELTA PARAMETERS $+25^oC$

PARAMETER	SYMBOL	DELTA LIMIT
Supply Current - MSI-1	IDD	± 0.2μA
Output Current (Sink)	IOL5	± 20% x Pre-Test Reading
Output Current (Source)	IOH5A	± 20% x Pre-Test Reading

TABLE 6. APPLICABLE SUBGROUPS

CONFORMANCE GROUP	MIL-STD-883 METHOD	GROUP A SUBGROUPS	READ AND RECORD
Initial Test (Pre Burn-In)	100% 5004	1, 7, 9	IDD, IOL5, IOH5A

TABLE 6. APPLICABLE SUBGROUPS

CONFORMANCE GROUP		MIL-STD-883 METHOD	GROUP A SUBGROUPS	READ AND RECORD
Interim Test 1 (Post Burn-In)		100% 5004	1, 7, 9	IDD, IOL5, IOH5A
Interim Test 2 (Post Burn-In)		100% 5004	1, 7, 9	IDD, IOL5, IOH5A
PDA (Note 1)		100% 5004	1, 7, 9, Deltas	
Interim Test 3 (Post Burn-In)		100% 5004	1, 7, 9	IDD, IOL5, IOH5A
PDA (Note 1)		100% 5004	1, 7, 9, Deltas	
Final Test		100% 5004	2, 3, 8A, 8B, 10, 11	
Group A		Sample 5005	1, 2, 3, 7, 8A, 8B, 9, 10, 11	
Group B	Subgroup B-5	Sample 5005	1, 2, 3, 7, 8A, 8B, 9, 10, 11, Deltas	Subgroups 1, 2, 3, 9, 10, 11
	Subgroup B-6	Sample 5005	1, 7, 9	
Group D		Sample 5005	1, 2, 3, 8A, 8B, 9	Subgroups 1, 2 3

NOTE: 1. 5% Parametric, 3% Functional; Cumulative for Static 1 and 2.

TABLE 7. TOTAL DOSE IRRADIATION

CONFORMANCE GROUPS	MIL-STD-883 METHOD	TEST		READ AND RECORD	
		PRE-IRRAD	POST-IRRAD	PRE-IRRAD	POST-IRRAD
Group E Subgroup 2	5005	1, 7, 9	Table 4	1, 9	Table 4

TABLE 8. BURN-IN AND IRRADIATION TEST CONNECTIONS

FUNCTION	OPEN	GROUND	VDD	9V ± -0.5V	OSCILLATOR	
					50kHz	25kHz
Static Burn-In 1 (Note 1)	4, 5, 11-13	2, 3, 6-10, 14, 15	1, 16			
Static Burn-In 2 (Note 1)	4, 5, 11-13	8	16	1-3, 4, 7, 9, 10, 14, 15		
Dynamic Burn-In (Note 4)	12	8	16	1, 4, 5, 11, 13	3, 6, 10, 14 (Note 3)	2, 7, 9, 15 (Note 3)
Irradiation (Note 2)	4, 5, 11-13	8	1-3, 6, 7, 9, 10, 14-16			

NOTES:

1. Each pin except Pin 1, VDD and GND will have a series resistor of 10K ± 5%, VDD = 18V ± 0.5V
2. Each pin except Pin 1, VDD and GND will have a series resistor of 47K ± 5%; Group E, Subgroup 2, sample size is 4 dice/wafer, 0 failures, VDD = 10V ± 0.5V
3. Pin voltage is VDD/2
4. Each pin except Pin 1, VDD and GND will have a series resistor of 4.75K ±5%, VDD = 18V ±0.5V.

Logic Diagram

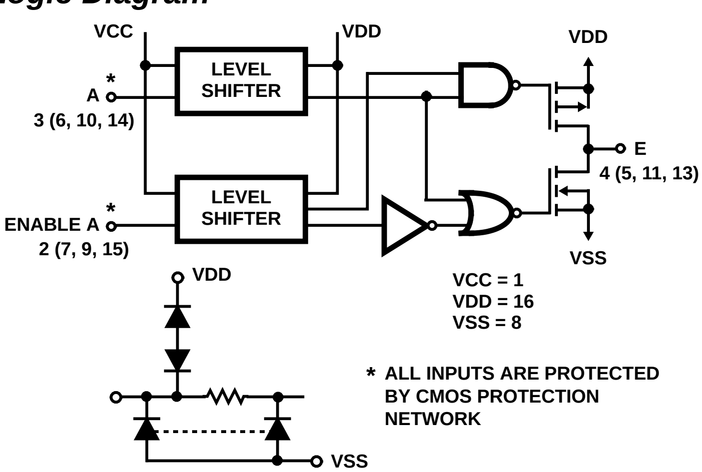


FIGURE 1. 1 OF 4 UNITS

TRUTH TABLE

INPUTS		OUTPUTS
A, B, C, D	ENABLE A, B, C, D	E, F, G, H
0	1	0
1	1	1
X	0	Z

Logic 0 = Low(VSS)
X = Don't care
Z = High impedance
Logic 1 = VCC at Inputs and VDD at Outputs

Typical Performance Characteristics

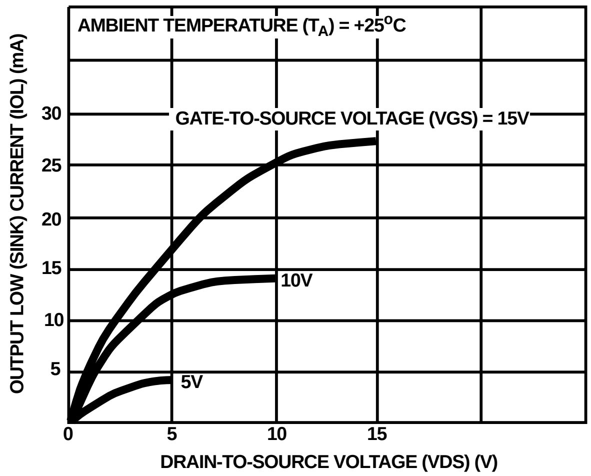


FIGURE 2. TYPICAL OUTPUT LOW (SINK) CURRENT CHARACTERISTICS

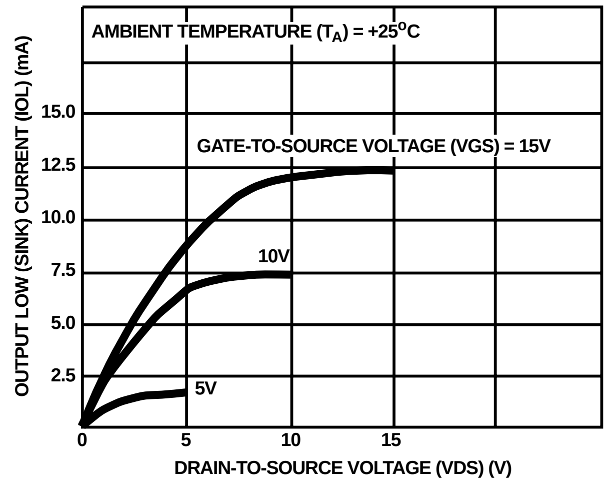


FIGURE 3. MINIMUM OUTPUT LOW (SINK) CURRENT CHARACTERISTICS

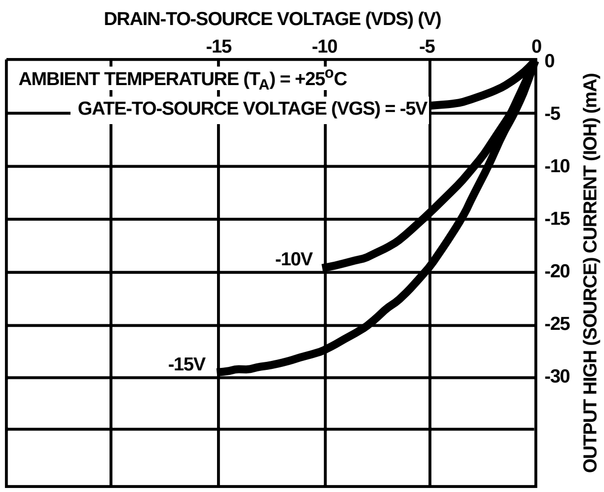


FIGURE 4. TYPICAL OUTPUT HIGH (SOURCE) CURRENT CHARACTERISTICS

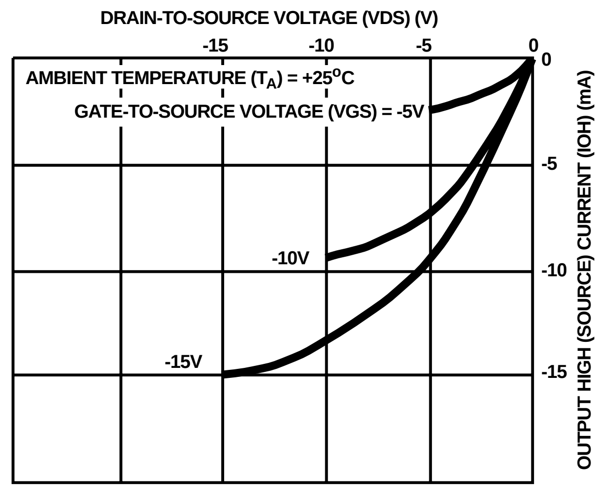


FIGURE 5. MINIMUM OUTPUT HIGH (SOURCE) CURRENT CHARACTERISTICS

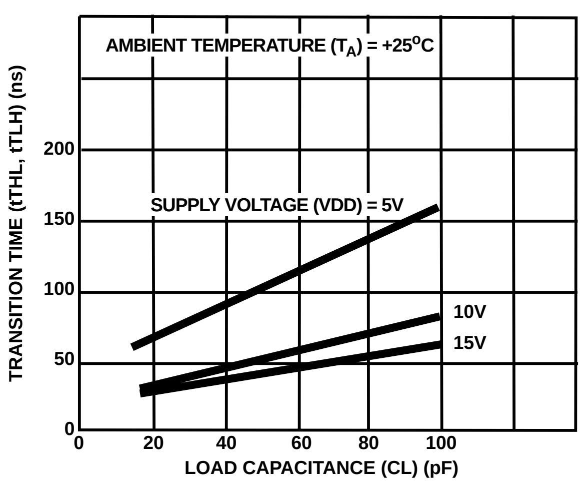


FIGURE 6. TYPICAL TRANSITION TIME AS A FUNCTION OF LOAD CAPACITANCE

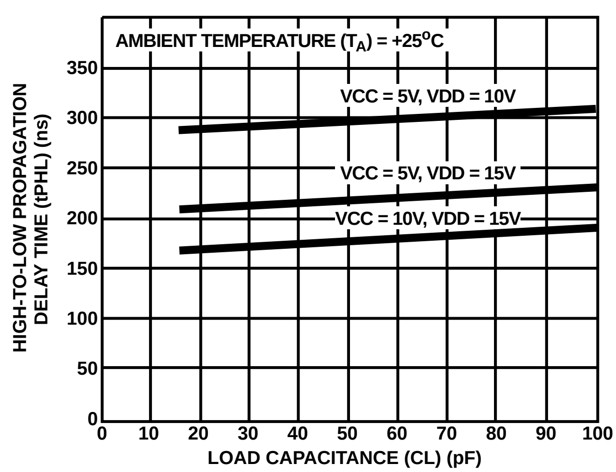


FIGURE 7. TYPICAL HIGH-TO-LOW PROPAGATION DELAY TIME AS A FUNCTION OF LOAD CAPACITANCE

Typical Performance Characteristics (Continued)

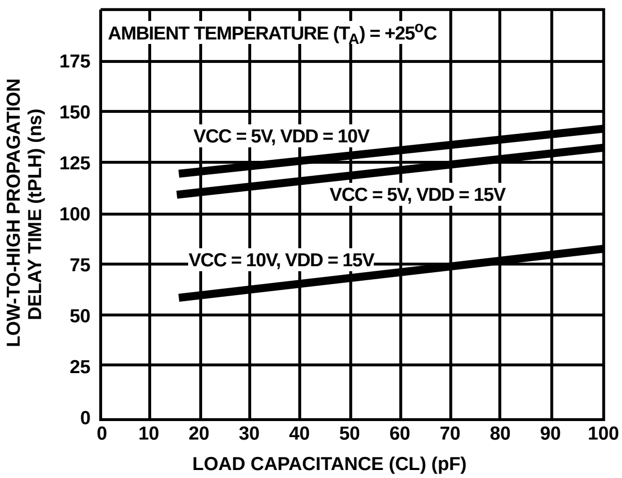


FIGURE 8. TYPICAL LOW-TO-HIGH PROPAGATION DELAY TIME AS A FUNCTION OF LOAD CAPACITANCE

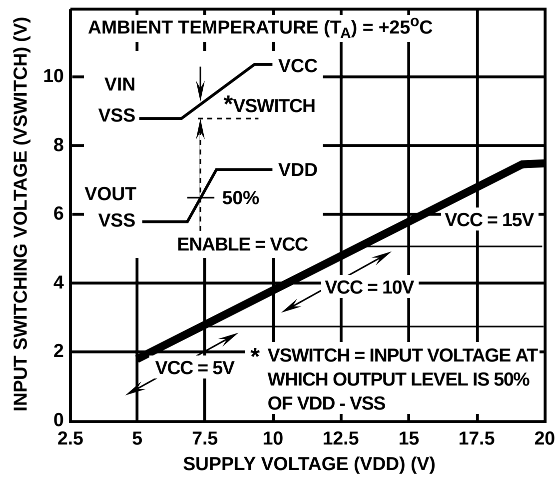


FIGURE 9. TYPICAL INPUT SWITCHING AS A FUNCTION OF HIGH LEVEL SUPPLY VOLTAGE

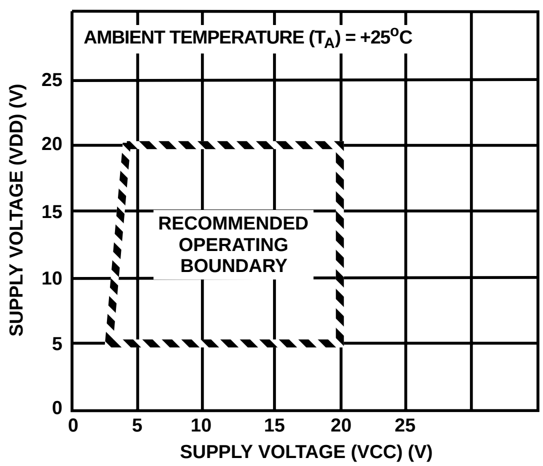


FIGURE 10. HIGH LEVEL SUPPLY VOLTAGE vs LOW LEVEL SUPPLY VOLTAGE

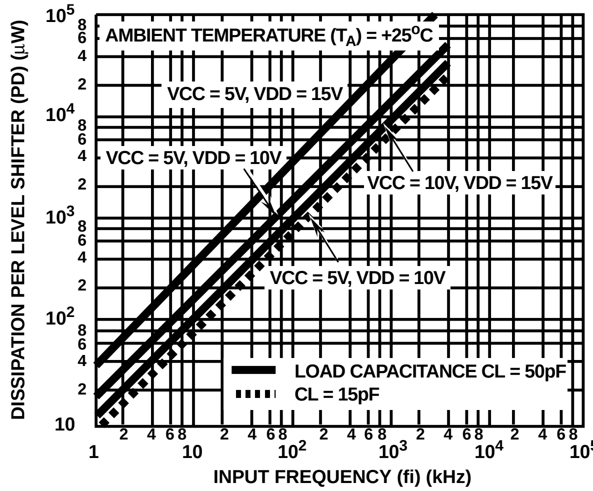
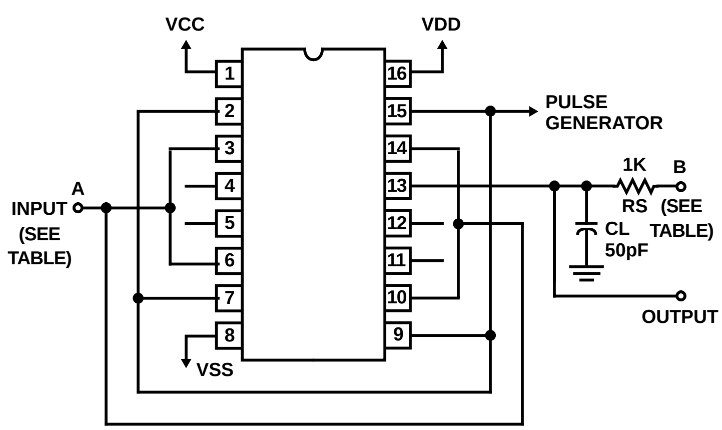


FIGURE 11. TYPICAL DYNAMIC POWER DISSIPATION AS A FUNCTION OF INPUT FREQUENCY

Test Circuit and Waveform



CHAR	TEST VOLTAGE	
	AT A	AT B
tPHZ	VCC	VSS
tPLZ	VSS	VDD
tPZL	VSS	VDD
tPZH	VCC	VSS

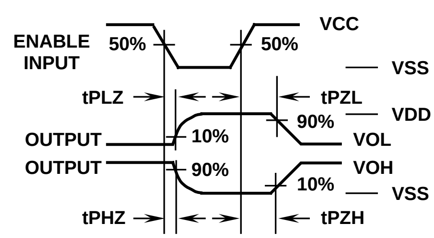
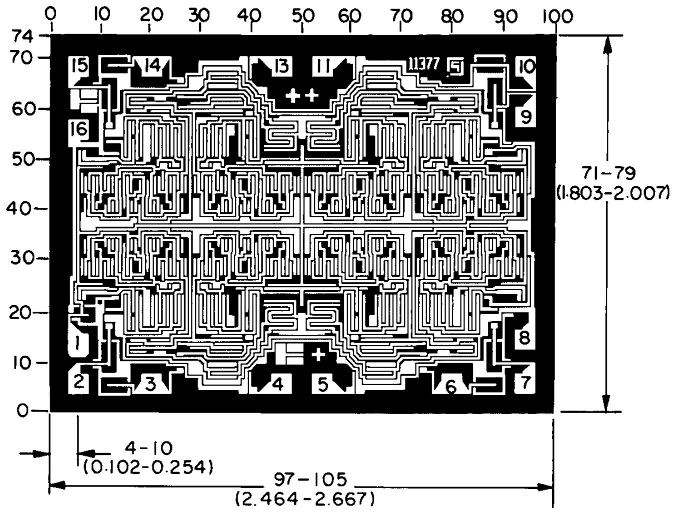


FIGURE 12. OUTPUT ENABLE DELAY TIMES TEST CIRCUIT AND WAVEFORMS

Chip Dimensions and Pad Layout



Dimensions in parenthesis are in millimeters and are derived from the basic inch dimensions as indicated. Grid graduations are in mils (10^{-3} inch).

METALLIZATION: Thickness: 11kÅ – 14kÅ, AL.

PASSIVATION: 10.4kÅ - 15.6kÅ, Silane

BOND PADS: 0.004 inches X 0.004 inches MIN

DIE THICKNESS: 0.0198 inches - 0.0218 inches

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