

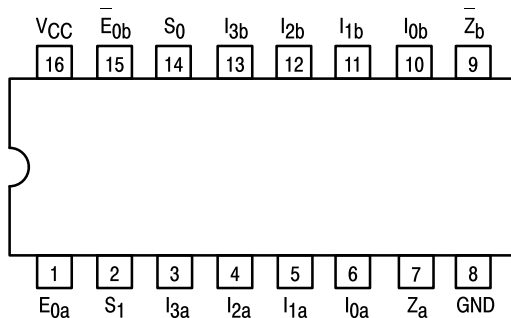


# DUAL 4-INPUT MULTIPLEXER WITH 3-STATE OUTPUTS

The LSTTL/MSI SN54/74LS353 is a Dual 4-Input Multiplexer with 3-state outputs. It can select two bits of data from four sources using common select inputs. The outputs may be individually switched to a high impedance state with a HIGH on the respective Output Enable ( $E_0$ ) inputs, allowing the outputs to interface directly with bus oriented systems. It is fabricated with the Schottky barrier diode process for high speed and is completely compatible with all TTL families.

- Inverted Version of the SN54/74LS253
- Schottky Process for High Speed
- Multifunction Capability
- Input Clamp Diodes Limit High Speed Termination Effects

CONNECTION DIAGRAM DIP (TOP VIEW)



NOTE:  
The Flatpak version has the same pinouts (Connection Diagram) as the Dual In-Line Package.

## PIN NAMES

$S_0, S_1$  Common Select Inputs

### Multiplexer A

$E_{0a}$  Output Enable (Active LOW) Input  
 $I_{0a} - I_{3a}$  Multiplexer Inputs  
 $Z_a$  Multiplexer Output (Note b)

### Multiplexer B

$E_{0b}$  Output Enable (Active LOW) Input  
 $I_{0b} - I_{3b}$  Multiplexer Inputs  
 $Z_b$  Multiplexer Output (Note b)

## LOADING (Note a)

	HIGH	LOW
$S_0, S_1$	0.5 U.L.	0.25 U.L.
$E_{0a}$	0.5 U.L.	0.25 U.L.
$I_{0a} - I_{3a}$	0.5 U.L.	0.25 U.L.
$Z_a$	65 (25) U.L.	15 (7.5) U.L.
$E_{0b}$	0.5 U.L.	0.25 U.L.
$I_{0b} - I_{3b}$	0.5 U.L.	0.25 U.L.
$Z_b$	65 (25) U.L.	15 (7.5) U.L.

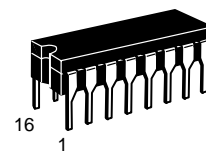
## NOTES:

- a) 1 TTL Unit Load (U.L.) = 40  $\mu$ A HIGH/1.6 mA LOW.  
b) The Output LOW drive factor is 7.5 U.L. for Military (54) and 15 U.L. for Commercial (74) Temperature Ranges. The Output HIGH drive factor is 25 U.L. for Military and 65 U.L. for Commercial Temperature Ranges.

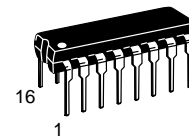
## SN54/74LS353

### DUAL 4-INPUT MULTIPLEXER WITH 3-STATE OUTPUTS

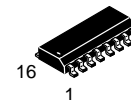
#### LOW POWER SCHOTTKY



**J SUFFIX**  
CERAMIC  
CASE 620-09



**N SUFFIX**  
PLASTIC  
CASE 648-08

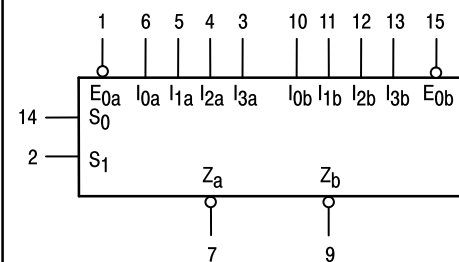


**D SUFFIX**  
SOIC  
CASE 751B-03

## ORDERING INFORMATION

SN54LSXXXJ Ceramic  
SN74LSXXXN Plastic  
SN74LSXXXD SOIC

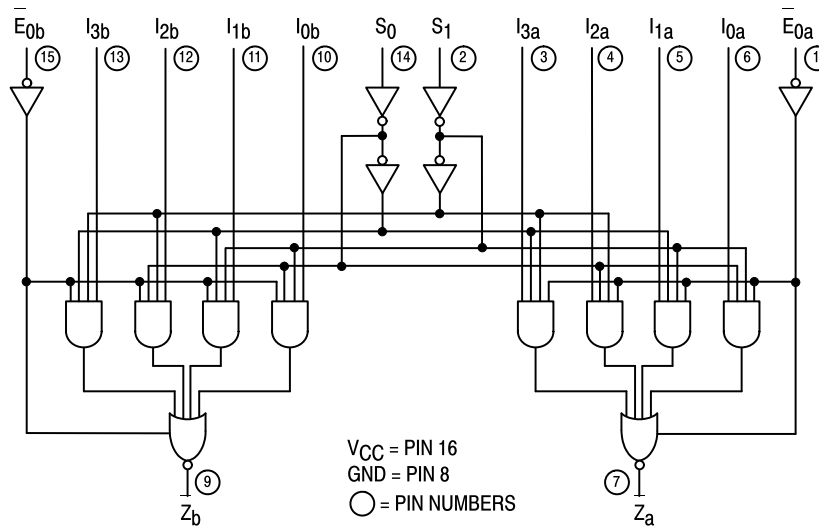
## LOGIC SYMBOL



$V_{CC}$  = PIN 16  
GND = PIN 8

# SN54/74LS353

## LOGIC DIAGRAM



## FUNCTIONAL DESCRIPTION

The SN54/74LS353 contains two identical 4-input Multiplexers with 3-state outputs. They select two bits from four sources selected by common select inputs ( $S_0$ ,  $S_1$ ). The 4-input multiplexers have individual Output Enable ( $E_{0a}$ ,  $E_{0b}$ )

inputs which when HIGH, forces the outputs to a high impedance (high Z) state.

The logic equations for the outputs are shown below:

$$\bar{Z}_a = \bar{E}_{0a} \cdot (I_{0a} \cdot \bar{S}_1 \cdot \bar{S}_0 + I_{1a} \cdot \bar{S}_1 \cdot S_0 + I_{2a} \cdot S_1 \cdot \bar{S}_0 + I_{3a} \cdot S_1 \cdot S_0)$$

$$\bar{Z}_b = \bar{E}_{0b} \cdot (I_{0b} \cdot \bar{S}_1 \cdot \bar{S}_0 + I_{1b} \cdot \bar{S}_1 \cdot S_0 + I_{2b} \cdot S_1 \cdot \bar{S}_0 + I_{3b} \cdot S_1 \cdot S_0)$$

If the outputs of 3-state devices are tied together, all but one device must be in the high impedance state to avoid high currents that would exceed the maximum ratings. Designers

should ensure that Output Enable signals to 3-state devices whose outputs are tied together are designed so that there is no overlap.

## TRUTH TABLE

SELECT INPUTS		DATA INPUTS				OUTPUT ENABLE	OUTPUT
$S_0$	$S_1$	$I_0$	$I_1$	$I_2$	$I_3$	$E_0$	Z
X	X	X	X	X	X	H	(Z)
L	L	L	X	X	X	L	H
L	L	H	X	X	X	L	L
H	L	X	L	X	X	L	H
H	L	X	H	X	X	L	L
L	H	X	X	L	X	L	H
L	H	X	X	H	X	L	L
H	H	X	X	X	L	L	H
H	H	X	X	X	H	L	L

H = HIGH Level

L = LOW Level

X = Immaterial

(Z) = High Impedance (off)

Address inputs  $S_0$  and  $S_1$  are common to both sections.

# SN54/74LS353

## GUARANTEED OPERATING RANGES

Symbol	Parameter		Min	Typ	Max	Unit
V <sub>CC</sub>	Supply Voltage	54 74	4.5 4.75	5.0 5.0	5.5 5.25	V
T <sub>A</sub>	Operating Ambient Temperature Range	54 74	−55 0	25 25	125 70	°C
I <sub>OH</sub>	Output Current — High	54 74			−1.0 −2.6	mA
I <sub>OL</sub>	Output Current — Low	54 74			12 24	mA

## DC CHARACTERISTICS OVER OPERATING TEMPERATURE RANGE (unless otherwise specified)

Symbol	Parameter		Limits			Unit	Test Conditions	
			Min	Typ	Max			
V <sub>IH</sub>	Input HIGH Voltage		2.0			V	Guaranteed Input HIGH Voltage for All Inputs	
V <sub>IL</sub>	Input LOW Voltage	54			0.7	V	Guaranteed Input LOW Voltage for All Inputs	
		74			0.8			
V <sub>IK</sub>	Input Clamp Diode Voltage			−0.65	−1.5	V	V <sub>CC</sub> = MIN, I <sub>IIN</sub> = −18 mA	
V <sub>OH</sub>	Output HIGH Voltage	54	2.4	3.4		V	V <sub>CC</sub> = MIN, I <sub>OH</sub> = MAX, V <sub>IN</sub> = V <sub>IH</sub> or V <sub>IL</sub> per Truth Table	
		74	2.4	3.1		V		
V <sub>OL</sub>	Output LOW Voltage Q <sub>A</sub> –Q <sub>H</sub>	54, 74		0.25	0.4	V	I <sub>OL</sub> = 12 mA	V <sub>CC</sub> = V <sub>CC</sub> MIN, V <sub>IN</sub> = V <sub>IL</sub> or V <sub>IH</sub> per Truth Table
		74		0.35	0.5	V	I <sub>OL</sub> = 24 mA	
I <sub>OZH</sub>	Output Off Current HIGH				20	μA	V <sub>CC</sub> = MAX, V <sub>OUT</sub> = 2.7 V	
I <sub>OZL</sub>	Output Off Current LOW				−20	μA	V <sub>CC</sub> = MAX, V <sub>OUT</sub> = 0.4 V	
I <sub>IH</sub>	Input HIGH Current				20	μA	V <sub>CC</sub> = MAX, V <sub>IN</sub> = 2.7 V	
					0.1	mA	V <sub>CC</sub> = MAX, V <sub>IN</sub> = 7.0 V	
I <sub>IL</sub>	Input LOW Current				−0.4	mA	V <sub>CC</sub> = MAX, V <sub>IN</sub> = 0.4 V	
I <sub>OS</sub>	Short Circuit Current (Note 1)		−20		−130	mA	V <sub>CC</sub> = MAX	
I <sub>CC</sub>	Power Supply Current Total, Output 3-State				14	mA	V <sub>CC</sub> = MAX	
	Total, Output LOW				12			

Note 1: Not more than one output should be shorted at a time, nor for more than 1 second.

## AC CHARACTERISTICS (T<sub>A</sub> = 25°C, V<sub>CC</sub> = 5.0 V)

Symbol	Parameter		Limits			Unit	Test Conditions	
			Min	Typ	Max			
t <sub>PLH</sub> t <sub>PHL</sub>	Propagation Delay, Data to Output			11 13	25 20	ns	Figure 1	C <sub>L</sub> = 15 pF
t <sub>PLH</sub> t <sub>PHL</sub>	Propagation Delay, Select to Output			20 21	45 32	ns	Figure 1 or 2	
t <sub>PZH</sub>	Output Enable Time to HIGH Level			11	23	ns	Figures 4, 5	
t <sub>PZL</sub>	Output Enable Time to LOW Level			15	23	ns	Figures 3, 5	
t <sub>PLZ</sub>	Output Disable Time to LOW Level			12	27	ns	Figures 3, 5	C <sub>L</sub> = 5.0 pF
t <sub>PHZ</sub>	Output Disable Time to HIGH Level			27	41	ns	Figures 4, 5	

SN54/74LS353

3-STATE WAVEFORMS

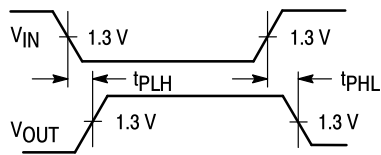


Figure 1

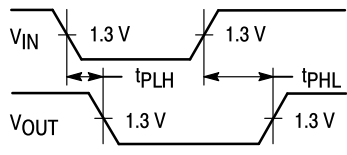


Figure 2

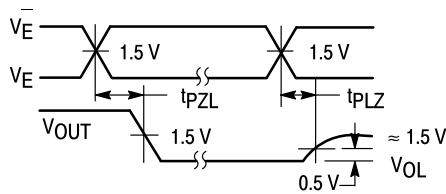


Figure 3

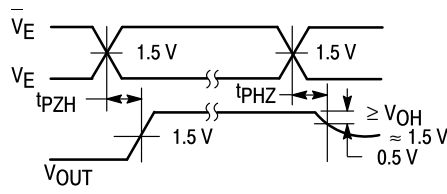
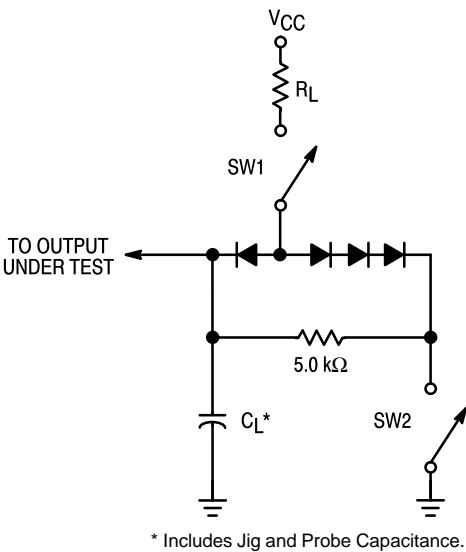


Figure 4

AC LOAD CIRCUIT



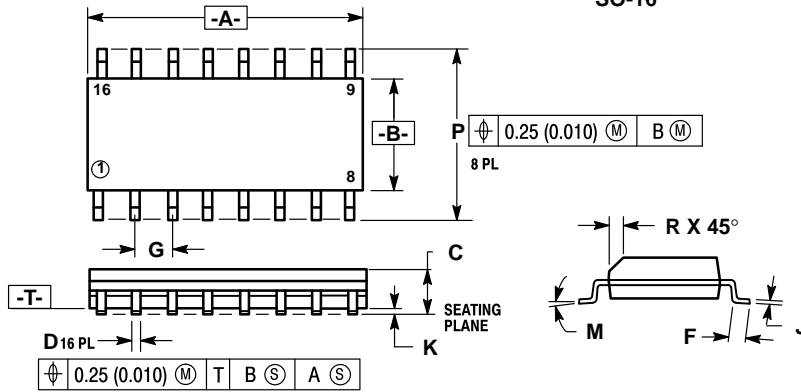
\* Includes Jig and Probe Capacitance.

SWITCH POSITIONS

SYMBOL	SW1	SW2
t <sub>PZH</sub>	Open	Closed
t <sub>PZL</sub>	Closed	Open
t <sub>PLZ</sub>	Closed	Closed
t <sub>PHZ</sub>	Closed	Closed

Figure 5

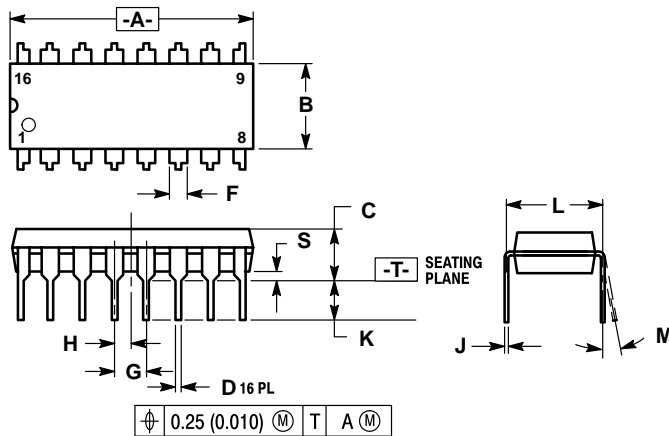
**Case 751B-03 D Suffix**  
**16-Pin Plastic**  
**SO-16**



- NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
  2. CONTROLLING DIMENSION: MILLIMETER.
  3. DIMENSION A AND B DO NOT INCLUDE MOLD PROTRUSION.
  4. MAXIMUM MOLD PROTRUSION 0.15 (0.006) PER SIDE.
  5. 751B-01 IS OBSOLETE, NEW STANDARD 751B-03.

DIM	MILLIMETERS		INCHES	
	MIN	MAX	MIN	MAX
A	9.80	10.00	0.386	0.393
B	3.80	4.00	0.150	0.157
C	1.35	1.75	0.054	0.068
D	0.35	0.49	0.014	0.019
F	0.40	1.25	0.016	0.049
G	1.27 BSC		0.050 BSC	
J	0.19	0.25	0.008	0.009
K	0.10	0.25	0.004	0.009
M	0°	7°	0°	7°
P	5.80	6.20	0.229	0.244
R	0.25	0.50	0.010	0.019

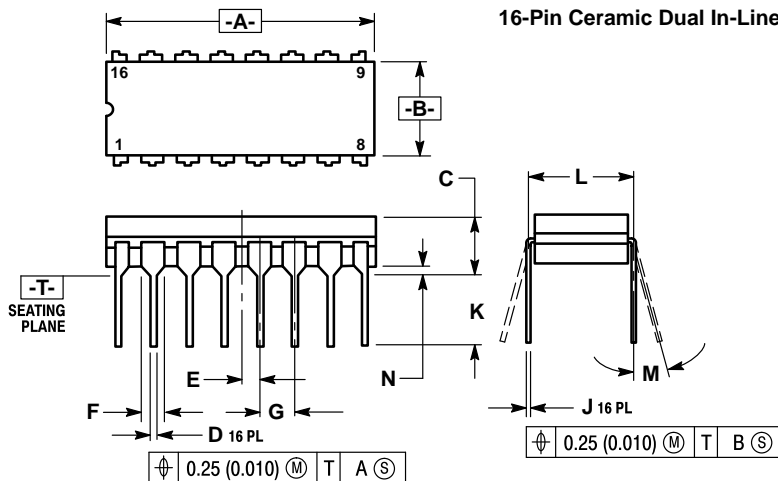
**Case 648-08 N Suffix**  
**16-Pin Plastic**



- NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
  2. CONTROLLING DIMENSION: INCH.
  3. DIMENSION "L" TO CENTER OF LEADS WHEN FORMED PARALLEL.
  4. DIMENSION "B" DOES NOT INCLUDE MOLD FLASH.
  5. ROUNDED CORNERS OPTIONAL.
  6. 648-01 THRU -07 OBSOLETE, NEW STANDARD 648-08.


DIM	MILLIMETERS		INCHES	
	MIN	MAX	MIN	MAX
A	18.80	19.55	0.740	0.770
B	6.35	6.85	0.250	0.270
C	3.69	4.44	0.145	0.175
D	0.39	0.53	0.015	0.021
F	1.02	1.77	0.040	0.070
G	2.54 BSC		0.100 BSC	
H	1.27 BSC		0.050 BSC	
J	0.21	0.38	0.008	0.015
K	2.80	3.30	0.110	0.130
L	7.50	7.74	0.295	0.305
M	0°	10°	0°	10°
S	0.51	1.01	0.020	0.040

**Case 620-09 J Suffix**  
**16-Pin Ceramic Dual In-Line**



- NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
  2. CONTROLLING DIMENSION: INCH.
  3. DIMENSION L TO CENTER OF LEAD WHEN FORMED PARALLEL.
  4. DIM F MAY NARROW TO 0.76 (0.030) WHERE THE LEAD ENTERS THE CERAMIC BODY.
  5. 620-01 THRU -08 OBSOLETE, NEW STANDARD 620-09.

DIM	MILLIMETERS		INCHES	
	MIN	MAX	MIN	MAX
A	19.05	19.55	0.750	0.770
B	6.10	7.36	0.240	0.290
C	—	4.19	—	0.165
D	0.39	0.53	0.015	0.021
E	1.27 BSC		0.050 BSC	
F	1.40	1.77	0.055	0.070
G	2.54 BSC		0.100 BSC	
J	0.23	0.27	0.009	0.011
K	—	5.08	—	0.200
L	7.62 BSC		0.300 BSC	
M	0°	15°	0°	15°
N	0.39	0.88	0.015	0.035

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