

October 1988 Revised March 2000

DM74LS533 Octal Transparent Latch with 3-STATE Outputs

General Description

The DM74LS533 consists of eight latches with 3-STATE outputs for bus organized system applications. The flipflops appear transparent to the data when Latch Enable (LE) is HIGH. When LE is LOW, the data that meets the setup times is latched. Data appears on the bus when the Output Enable ($\overline{\text{OE}}$) is LOW. When $\overline{\text{OE}}$ is HIGH the bus output is in the high impedance state. The DM74LS533 is the same as the DM74LS373, except that the outputs are inverted. For detailed specifications please see the DM74LS373 data sheet, but note that the propagation delays from data to output are 5.0 ns longer for the DM74LS533 than for the DM74LS373.

Features

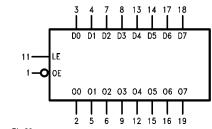
- Eight latches in a single package
- 3-STATE outputs for bus interfacing

Ordering Code:

Order Number	Package Number	Package Description
DM74LS533WM	M20B	20-Lead Small Outline Integrated Circuit (SOIC), JEDEC MS-013, 0.300 Wide
DM74LS533N	DM74LS533N N20A 20-Lead Plastic Dual-In-Line Package (PDIP), JEDEC	

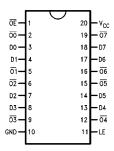
Devices also available in Tape and Reel. Specify by appending the suffix letter "X" to the ordering code.

Logic Symbol



V_{CC} = Pin 20 GND = Pin 10

Connection Diagram



Pin Descriptions

ſ	Pin Names	Description
П	,	Data Inputs
ı	LE	Latch Enable Input (Active HIGH)
Ī		Output Enable Input (Active LOW)
(0 0– 0 7	Complementary 3-STATE Outputs

Function Table

OUTPUT Enable	Latch Enable	D	Output O
L	Н	Н	L
L	Н	L	Н
L	L	Χ	\overline{Q}_O
Н	X	X	Z

- L = LOW State
- H = HIGH State X = Don't Care
- Z = High Impedance State
- \overline{Q}_{O} = Previous Condition of \overline{O}

Absolute Maximum Ratings(Note 1)

Supply Voltage 7V Input Voltage 7V Operating Free Air Temperature Range 0° C to +70 $^{\circ}$ C Storage Temperature Range -65° C to +150 $^{\circ}$ C

Note 1: The "Absolute Maximum Ratings are those values beyond which the safety of the device cannot be guaranteed. The device should not be operated at these limits. The parametric values defined in the Electrical Characteristics tables are not guaranteed at the absolute maximum ratings. The "Recommended Operating Conditions" table will define the conditions for actual device operation.

Recommended Operating Conditions

Symbol	Parameter	Min	Nom	Max	Units
V _{CC}	Supply Voltage	4.75	5	5.25	V
V _{IH}	High Level Input Voltage	2			V
V _{IL}	Low Level Input Voltage			0.8	V
I _{OH}	High Level Output Current			-2.6	mA
I _{OL}	Low Level Output Current			24	mA
T _A	Free Air Operating Temperature	0		70	°C

Electrical Characteristics

Over recommended operating free air temperature range (unless otherwise noted)

Symbol	Parameter	Conditions	Min	Typ (Note 2)	Max	Units
VI	Input Clamp Voltage	$V_{CC} = Min, I_I = -18 \text{ mA}$			-1.5	V
V _{OH}	HIGH Level	V _{CC} = Min, I _{OH} = Max,	2.4	3.4		V
	Output Voltage	$V_{IL} = Max$				
V _{OL}	LOW Level	V _{CC} = Min, I _{OL} = Max,		0.35	0.5	
	Output Voltage	V _{IH} = Min		0.55	0.5	V
		$I_{OL} = 12 \text{ mA}, V_{CC} = \text{Min}$			0.4	
II	Input Current @ Max Input Voltage	$V_{CC} = Max, V_I = 7V$			0.1	mA
I _{IH}	HIGH Level Input Current	$V_{CC} = Max, V_I = 2.7V$			20	μΑ
I _{IL}	LOW Level Input Current	$V_{CC} = Max, V_I = 0.4V$			-0.4	mA
Ios	Short Circuit	V _{CC} = Max	-20		-100	mA
	Output Current	(Note 3)	-20		-100	IIIA
I _{CCZ}	Supply Current	V _{CC} = Max			46	mA
I _{OZL}	3-STATE Output Off	V _{CC} = V _{CCH}			-20.0	
	Current LOW	$V_{OZL} = 0.4V$			-20.0	μΑ
I _{OZH}	3-STATE Output Off	V _{CC} = V _{CCH}			20.0	μА
	Current HIGH	V _{OZH} = 2.7V			20.0	μΑ

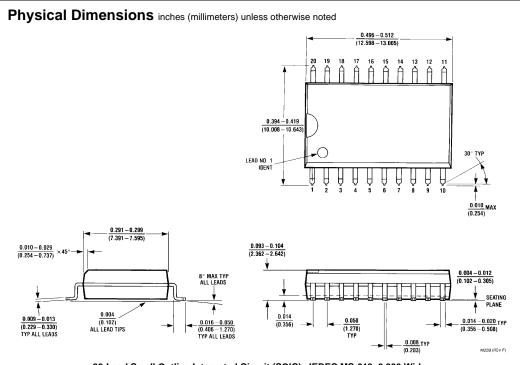
Note 2: All typicals are at $V_{CC} = 5V$, $T_A = 25^{\circ}C$.

Note 3: Not more than one output should be shorted at a time, and the duration should not exceed one second.

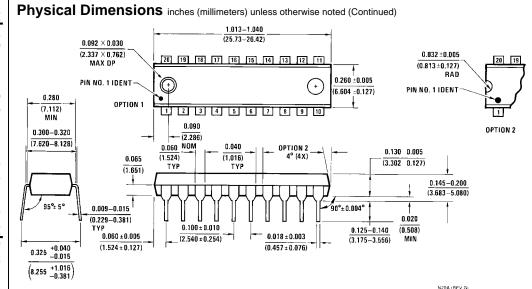
Switching Characteristics

 $V_{CC} = +5.0V, T_A = +25^{\circ}C$

Symbol	l Parameter	$C_L = 50 \text{ pF}$ $R_L = 2 \text{ k}\Omega$		Units	
		Min	Max		
t _{PLH}	Propagation Delay		23	20	
t _{PHL}	Data to \overline{Q}_{x}		23	ns	
t _{PLH}	Propagation Delay		30	ns	
t _{PHL}	LE to \overline{Q}_x		25		
t _{PZL}	Output Enable Time		22		
t _{PZH}	\overline{OE} to \overline{Q}_{X}		20	ns	
t _{PHZ}	Output Enable Time		20	ns	
t _{PLZ}	\overline{OE} to \overline{Q}_{X}		25		



20-Lead Small Outline Integrated Circuit (SOIC), JEDEC MS-013, 0.300 Wide Package Number M20B



20-Lead Plastic Dual-In-Line Package (PDIP), JEDEC MS-001, 0.300 Wide Package Number N20A

Fairchild does not assume any responsibility for use of any circuitry described, no circuit patent licenses are implied and Fairchild reserves the right at any time without notice to change said circuitry and specifications.

LIFE SUPPORT POLICY

FAIRCHILD'S PRODUCTS ARE NOT AUTHORIZED FOR USE AS CRITICAL COMPONENTS IN LIFE SUPPORT DEVICES OR SYSTEMS WITHOUT THE EXPRESS WRITTEN APPROVAL OF THE PRESIDENT OF FAIRCHILD SEMICONDUCTOR CORPORATION. As used herein:

- Life support devices or systems are devices or systems which, (a) are intended for surgical implant into the body, or (b) support or sustain life, and (c) whose failure to perform when properly used in accordance with instructions for use provided in the labeling, can be reasonably expected to result in a significant injury to the user.
- A critical component in any component of a life support device or system whose failure to perform can be reasonably expected to cause the failure of the life support device or system, or to affect its safety or effectiveness.

www.fairchildsemi.com