SN54LS604, SN54LS606, SN54LS607, SN74LS604, SN74LS606, SN74LS607 OCTAL 2-INPUT MULTIPLEXED LATCHES

SDLS183

D2545, JULY 1979-REVISED MARCH 1988

(TIM99604, TIM99606, TIM99607)

- Choice of Outputs: Three State ('LS604, 'LS606)
 Open-Collector ('LS607)
- 16 D-Type Registers, One for Each Data Input
- Multiplexer Selects Stored Data from Either A Bus or B Bus
- Application Oriented:
 Maximum Speed ('LS604)
 Glitch-Free Operation ('LS606, 'LS607)

description

The 'LS604, 'LS606, and 'LS607 multiplexed latches are ideal for storing data from two input buses, A and B, and providing the output bus with stored data from either the A or B register.

The clock loads data on the positive-going (low-level to high-level) transition. The clock pin also controls the active and high-impedance states of the outputs. When the clock pin is low, the outputs are in the high-impedance or off state. When the clock pin is high, the outputs are enabled.

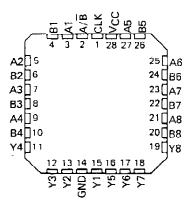
The 'LS604 is optimized for high-speed operation. The 'LS606 and 'LS607 are especially designed to eliminate decoding voltage spikes.

These functions are ideal for interface from a 16-bit microprocessor to a 64K RAM board. The row and column addresses can be loaded as one word from the microprocessor and then multiplexed sequentially to the RAM during the time that RAS and CAS are active.

SN54LS604, SN54LS606, SN54LS607 . . . JD PACKAGE SN74LS604, SN74LS606, SN74LS607 . . . JD OR N PACKAGE (TOP VIEW)

CLK[1 1	J ₂₈ [Jvcc
A/B[2	27]A5
A1[3	26	∃ 6 5
B1[4	25	∃A6
A2_	5	24]в6
B2	6	23]A7
A3	7	22	⊒в7
B3[_	8	21	3AE
A4[_	9	20]в8
B4[10	19]Y8
Y4[_	11	18]Y7
Y3[12	17]ү6
Y2[13	16	_Y5
GND□	14	15]Y1

SN54LS604, SN54LS606, SN54LS607 . . . FK PACKAGE (TOP VIEW)



The SN54LS604, SN54LS606, and SN54LS607 are characterized for operation over the full military temperature range of $-55\,^{\circ}\text{C}$ to 125 $\,^{\circ}\text{C}$; the SN74LS604, SN74LS606, and SN74LS607 are characterized for operation from 0 $\,^{\circ}\text{C}$ to 70 $\,^{\circ}\text{C}$.

FUNCTION TABLE

		INPUTS		OUTPUTS
A1-A8	B1-B8	SELECT A/B	CLOCK	Y1-Y8
A data	B data	L	t	B data
A data	B data	н	t	A data
×	×	×	L	Z or Off
×	×	L	Н	B register stored data
X	x	н	Н	A register stored data

H = high level (steady state)

L = low level (steady state)

X = irrelevant

Z = high-impedance state

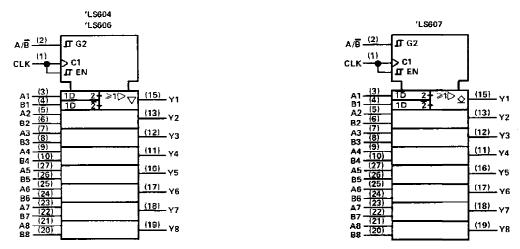
Off = H if pull-up resistor is connected to open-collector output

† = transistion from low to high level

SN54LS604, SN54LS606, SN54LS607, SN74LS604, SN74LS606, SN74LS607 OCTAL 2-INPUT MULTIPLEXED LATCHES

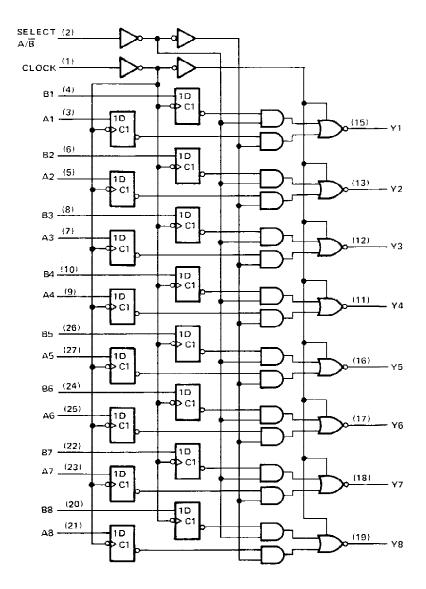
schematics of inputs and outputs EQUIVALENT OF SELECT INPUTS EQUIVALENT OF A AND B INPUTS **EQUIVALENT OF CLOCK INPUTS** v_{cc} VCC - $4 k\Omega$ 22 ks2 10 kΩ NOM NOM NOM INPUT: INPUT INPUT TYPICAL OF ALL OUTPUTS TYPICAL OF ALL OUTPUTS ('LS604, 'LS606) ('LS607) -∨cc \$100 Ω NOM OUTPUT OUTPUT

logic symbols†



[†]These symbols are in accordance with ANSI/IEEE Std. 91-1984 and IEC Publication 617-12. Pin numbers shown are for JD and N packages.

logic diagram (positive logic)



SN54LS604, SN54LS606, SN74LS604, SN74LS606 OCTAL 2-INPUT MULTIPLEXED LATCHES WITH 3-STATE OUTPUTS

recommended operating conditions

		SN54LS604 SN54LS606		SN74LS604 SN74LS606			UNIT
	MIN	NOM	MAX	MIN	NOM	MAX	
Supply voltage, V _{CC} (see Note 1)	4.5	5	5.5	4.75	5	5.25	V
High-level output current, IOH			-1			-2,6	mΑ
Low-level output current, IOL			12			24	mΑ
Width of clock pulse, t _W	20			20			ns
Setup time, t _{su}	20↑			20↑			ns
Hold time, th	01			10			ns
Operating free-air temperature, TA	~55		125	0		70	°C

NOTE 1: Voltage values are with respect to network ground terminal.

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

	PARAMETER	TEST CONDITIONS [†]		SN54LS604 SN54LS606			SN74LS604 SN74LS606			UNIT	
					MIN	TYPÌ	MAX	MIN	TYP÷	MAX	<u> </u>
v_{IH}	High-level input voltage				2			2			V
VIL	Low-level input voltage						0.7			0.8	V
v_{ik}	Input clamp voltage	V _{CC} = MIN,	$I_1 = -18 \text{ mA}$				1.5			-1.5	V
VOH	High-level output voltage	$V_{CC} = MIN$. $V_{IL} = V_{IL} max$,	V _{IH} = 2 V, I _{OH} = MAX		2.4	3.1	-	2.4	3,1		V
VOL	Low-level output voltage	V _{CC} = MIN, V _{IL} - V _{IL} max,	V _{IH} = 2 V,	I _{OL} = 12 mA		0.25	0.4		0.25 0.35	0.4 0,5	v
IOZH	Off-state output current, high-level voltage applied	V _{CC} = MAX, V _{IL} = V _{IL} max,	V _{IH} = 2 V, V _O = 2.7 V				20		·	20	μА
lozL	Off-state output current, low-level voltage applied	V _{CC} = MAX, V _{IL} = V _{IL} max,	V _{IH} = 2 V, V _O = 0.4				-20			-20	μА
l _į	Input current at maximum input voltage	V _{CC} = MAX,	V = 7 V	A, B CLK, SELECT		_	0.1	<u>-</u>		0.1	mA
ΉΗ	High-level input current	V _{CC} = MAX,	V ₁ = 2.7 V	A, B CLK, SELECT			20 20			20 20	μД
l)L	Low-level input current	V _{CC} = MAX,	V ₁ = 0.4 V	A, B CLK, SELECT			-0.4 -0.2			-0.4 -0.2	mA
los	Short-circuit output current §	V _{CC} = MAX		<u>, </u>	-30		-130	-30		-130	mΑ
ICC	Supply current	VCC = MAX,	See Note 2	_		55	70		55	70	mΑ

[†]For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions.

switching characteristics, $V_{CC} = 5 \text{ V}$, $T_A = 25^{\circ}\text{C}$

PARAMETER	FROM	TEST CONDITIONS			'LS604			'LS606		
	(INPUT)			MIN	TYP	MAX	MIN	TYP	MAX	UNIT
†PLH	Select A/B				15	25		36	50	
^t PHL	(Data: A = H, B = L)				23	35		16	30	ns
tPLH	Select A/B	CL = 45 pF,	$R_{\perp} = 667 \Omega$,		31	45		22	35	
†PHL	(Data: A = L, B = H)	See Note 3			19	30	j	22	35	ns
[†] PZH	Clock				19	30		27	40	пѕ
tPZL	GIOCK				28	40		35	50	""
TPH2	Clock	CL = 5 pF, See Note 3	$R_L = 667 \Omega$.	L	20	30		20	30	ns
^t PLZ	CIUCK				15	25		15	25	113

tp_{LH} ≡ propagation delay time, low-to-high-level output tp_{HL} ≡ propagation delay time, low-to-high-level output

tpzh = output enable time to high level

tPHZ == output disable time from high level

NOTE 3: Load circuits and voltage waveforms are shown in Section 1.



 $[\]ddagger$ All typical values are at $V_{CC} = 5 \text{ V, T}_{A} = 25^{\circ}\text{C}$.

[§] Note more than one output should be shorted at a time, and duration of the short-circuit should not exceed one second.

NOTE 2: ICC is tested with all inputs grounded and all outputs open.

SN54LS607, SN74LS607 OCTAL 2-INPUT MULTIPLEXED LATCHES WITH OPEN-COLLECTOR OUTPUTS

recommended operating conditions

		SN54LS607		SN74LS607			UNIT
	MIN	NOM	MAX	MIN	NOM	MAX	
Supply voltage, VCC (see Note 1)	4.5	5	5.5	4.75	5	5.25	V
High-level output voltage, VOH			6.5			5.5	V
Low-level output current, IOL			12			24	mΑ
Width of clock pulse, tw	20			20			пѕ
Setup time, t _{su}	20↑			20↑			пs
Hold time, th	01			0↑			пѕ
Operating free-air temperature, TA	-55		125	0		70	°C

NOTE 1: Voltage values are with respect to network ground terminal.

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

	PARAMETER	TEST CONDITIONS [†]		SN54LS607			5	07	UNIT		
				MIN	TYPŤ	MAX	MIN	TYP‡	MAX		
ViΗ	High-level input voltage				2			2			V
VIL	Low-level input voltage						0.7		_	8.0	V
VIK	Input clamp voltage	V _{CC} = MIN,	I _I = -18 mA				-1.5			1.5	V
IOH	High-level output current	V _{CC} = MIN, V _{IL} = V _{IL} max,	V _{IH} = 2 V, V _{OH} = 6.5 V				250			250	μΑ
	Low-level output voltage	V _{CC} = MIN,	V _{1H} = 2 V,	I _{OL} = 12 mA		0.25	0.4		0.25	0.4	V
VOL		VIL = VIL max		I _{OL} = 24 mA					0.35 0.	0.5	, v
	Input current at	V - U6V	V ₁ = 7 V	A,B			0.1			0.1	mA
ij	maximum input voltage	V _{CC} = MAX,	V - / V	CLK, SELECT			0.1			0.1	III.A
		11 - 446V	V - 07V	A,B			20			20	μД
11H	High-level input current	V _{CC} = MAX,	V ₁ = 2.7 V	CLK, SELECT			20			20	μΑ.
	1 1 1 1 1	31.31		A,B			-0.4			-0.4	mA
liL.	Low-level input current	V _{CC} = MAX,	V _i = 0.4 V	CLK, SELECT			-0.2			0 <u>.2</u>	IIIA
lcc	Supply current	Vcc = MAX,	See Note 2	-		40	60		40	60	mΑ

[†]For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions.

NOTE 2: $1_{\mbox{CC}}$ is tested with all inputs grounded and all outputs open,

switching characteristics, VCC = 5 V, TA = 25 °C

	FROM			'LS607				
PARAMETER	(INPUT)	TEST CONDITIONS	MIN	TYP	MAX	UNIT		
[†] PLH	Select A/B			51	70	ns		
tPHL	(Data: A = H, B = L)	C_L = 45 pF, R_L = 667 Ω , See Note 3		21	30	113		
[†] PLH	Select A/B			28	40			
^t PHL	(Data: A = L, B = H)			28	40	ns		
[†] PLH				30	45			
t _{PHL}	Clock			32	45	ns		

NOTE 3: Load circuits and voltage waveforms are shown in Section 1.

 $^{^\}ddagger$ All typical values are at V_{CC} = 5 V, T_A = 25°C.

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