

CD40174BM/CD40174BC Hex D Flip-Flop CD40175BM/CD40175BC Quad D Flip-Flop

General Description

The CD40174B consists of six positive-edge triggered D-type flip-flops; the true outputs from each flip-flop are externally available. The CD40175B consists of four positive-edge triggered D-type flip-flops; both the true and complement outputs from each flip-flop are externally available.

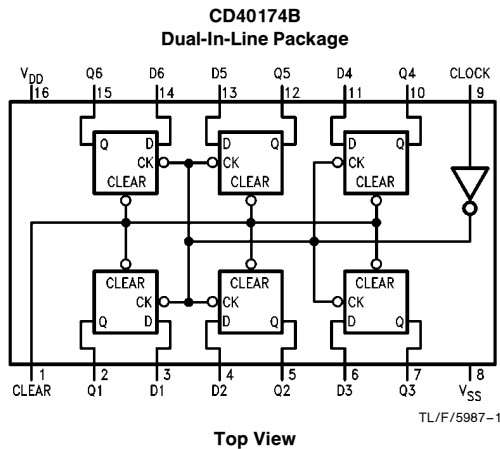
All flip-flops are controlled by a common clock and a common clear. Information at the D inputs meeting the set-up time requirements is transferred to the Q outputs on the positive-going edge of the clock pulse. The clearing operation, enabled by a negative pulse at Clear input, clears all Q outputs to logical "0" and Qs (CD40175B only) to logical "1".

All inputs are protected from static discharge by diode clamps to V_{DD} and V_{SS} .

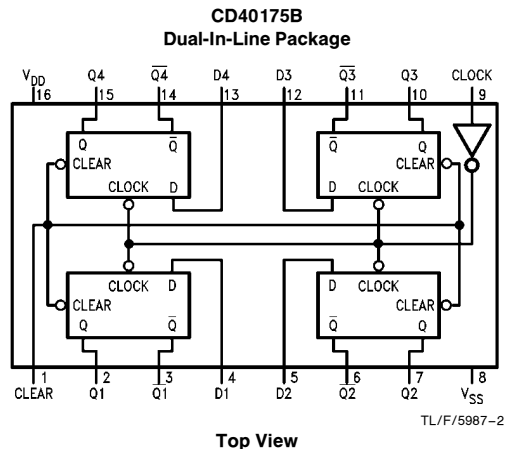
Features

- Wide supply voltage range 3V to 15V
- High noise immunity 0.45 V_{DD} (typ.)
- Low power TTL compatibility fan out of 2 driving 74L or 1 driving 74 LS
- Equivalent to MC14174B, MC14175B
- Equivalent to MM74C174, MM74C175

Connection Diagrams



Top View



Top View

Order Number CD40174B or CD40175B

Truth Table

Inputs			Outputs	
Clear	Clock	D	Q	\bar{Q}^*
L	X	X	L	H
H	↑	H	H	L
H	↑	L	L	H
H	H	X	NC	NC
H	L	X	NC	NC

H = High level
L = Low level
X = Irrelevant
↑ = Transition from low to high level
NC = No change
* = \bar{Q} for CD40175B only

Absolute Maximum Ratings (Notes 1 & 2)

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/Distributors for availability and specifications.

DC Supply Voltage (V_{DD})	–0.5V to +18V
Input Voltage (V_{IN})	–0.5V to V_{DD} + 0.5V _{DC}
Storage Temperature Range (T_S)	–65°C to +150°C
Power Dissipation (P_D)	
Dual-In-Line	700 mW
Small Outline	500 mW
Lead Temperature (T_L)	
(Soldering, 10 seconds)	260°C

Recommended Operating Conditions (Note 2)

DC Supply Voltage (V_{DD})	3V to 15 V _{DC}
Input Voltage (V_{IN})	0V to V_{DD} V _{DC}
Operating Temperature Range (T_A)	–55°C to +125°C
CD40XXXBM	–40°C to +85°C
CD40XXXBC	

DC Electrical Characteristics CD40174BM/CD40175BM (Note 2)

Symbol	Parameter	Conditions	–55°C		+25°C			+125°C		Units
			Min	Max	Min	Typ	Max	Min	Max	
I_{DD}	Quiescent Device Current	$V_{DD} = 5V, V_{IN} = V_{DD}$ or V_{SS}		1.0			1.0		30	μA
		$V_{DD} = 10V, V_{IN} = V_{DD}$ or V_{SS}		2.0			2.0		60	μA
		$V_{DD} = 15V, V_{IN} = V_{DD}$ or V_{SS}		4.0			4.0		120	μA
V_{OL}	Low Level Output Voltage	$ I_O < 1 \mu A$								
		$V_{DD} = 5V$		0.05			0.05		0.05	V
		$V_{DD} = 10V$		0.05			0.05		0.05	V
V_{OH}	High Level Output Voltage	$ I_O < 1 \mu A$								
		$V_{DD} = 5V$	4.95		4.95	5		4.95		V
		$V_{DD} = 10V$	9.95		9.95	10		9.95		V
V_{IL}	Low Level Input Voltage	$V_{DD} = 5V, V_O = 0.5V$ or 4.5V		1.5			1.5		1.5	V
		$V_{DD} = 10V, V_O = 1V$ or 9V		3.0			3.0		3.0	V
		$V_{DD} = 15V, V_O = 1.5V$ or 13.5V		4.0			4.0		4.0	V
V_{IH}	High Level Input Voltage	$V_{DD} = 5V, V_O = 0.5V$ or 4.5V	3.5		3.5			3.5		V
		$V_{DD} = 10V, V_O = 1V$ or 9V	7.0		7.0			7.0		V
		$V_{DD} = 15V, V_O = 1.5V$ or 13.5V	11.0		11.0			11.0		V
I_{OL}	Low Level Output Current (Note 3)	$V_{DD} = 5V, V_O = 0.4V$	0.64		0.51	0.88		0.36		mA
		$V_{DD} = 10V, V_O = 0.5V$	1.6		1.3	2.25		0.9		mA
		$V_{DD} = 15V, V_O = 1.5V$	4.2		3.4	8.8		2.4		mA
I_{OH}	High Level Output Current (Note 3)	$V_{DD} = 5V, V_O = 4.6V$	–0.64		–0.51	–0.88		–0.36		mA
		$V_{DD} = 10V, V_O = 9.5V$	–1.6		–1.3	–2.25		–0.9		mA
		$V_{DD} = 15V, V_O = 13.5V$	–4.2		–3.4	–8.8		–2.4		mA
I_{IN}	Input Current	$V_{DD} = 15V, V_{IN} = 0V$		–0.1		-10^{-5}	–0.1		–1.0	μA
		$V_{DD} = 15V, V_{IN} = 15V$		0.1		10^{-5}	0.1		1.0	μA

DC Electrical Characteristics CD40174BC/CD40175BC (Note 2)

Symbol	Parameter	Conditions	–40°C		+25°C			+85°C		Units
			Min	Max	Min	Typ	Max	Min	Max	
I_{DD}	Quiescent Device Current	$V_{DD} = 5V, V_{IN} = V_{DD}$ or V_{SS}		4			4		30	μA
		$V_{DD} = 10V, V_{IN} = V_{DD}$ or V_{SS}		8			8		60	μA
		$V_{DD} = 15V, V_{IN} = V_{DD}$ or V_{SS}		16			16		120	μA

Note 1: “Absolute Maximum Ratings” are those values beyond which the safety of the device cannot be guaranteed. They are not meant to imply that the devices should be operated at these limits. The tables of “Recommended Operating Conditions” and “Electrical Characteristics” provide conditions for actual device operation.

Note 2: $V_{SS} = 0V$ unless otherwise specified.

Note 3: I_{OH} and I_{OL} are tested one output at a time.

DC Electrical Characteristics CD40174BC/CD40175BC (Note 2) (Continued)

Symbol	Parameter	Conditions	−40°C		+25°C			+85°C		Units
			Min	Max	Min	Typ	Max	Min	Max	
V _{OL}	Low Level Output Voltage	V _{DD} = 5V		0.05			0.05		0.05	V
		V _{DD} = 10V		0.05			0.05		0.05	V
		V _{DD} = 15V		0.05			0.05		0.05	V
V _{OH}	High Level Output Voltage	V _{DD} = 5V	4.95		4.95	5		4.95		V
		V _{DD} = 10V	9.95		9.95	10		9.95		V
		V _{DD} = 15V	14.95		14.95	15		14.95		V
V _{IL}	Low Level Input Voltage	V _{DD} = 5V, V _O = 0.5V or 4.5V		1.5			1.5		1.5	V
		V _{DD} = 10V, V _O = 1V or 9V		3.0			3.0		3.0	V
		V _{DD} = 15V, V _O = 1.5V or 13.5V		4.0			4.0		4.0	V
V _{IH}	High Level Input Voltage	V _{DD} = 5V, V _O = 0.5V or 4.5V	3.5		3.5			3.5		V
		V _{DD} = 10V, V _O = 1V or 9V	7.0		7.0			7.0		V
		V _{DD} = 15V, V _O = 1.5V or 13.5V	11.0		11.0			11.0		V
I _{OL}	Low Level Output Current (Note 3)	V _{DD} = 5V, V _O = 0.4V	0.52		0.44	0.88		0.36		mA
		V _{DD} = 10V, V _O = 0.5V	1.3		1.1	2.25		0.9		mA
		V _{DD} = 15V, V _O = 1.5V	3.6		3.0	8.8		2.4		mA
I _{OH}	High Level Output Current (Note 3)	V _{DD} = 5V, V _O = 4.6V	−0.52		−0.44	−0.88		−0.36		mA
		V _{DD} = 10V, V _O = 9.5V	−1.3		−1.1	−2.25		−0.9		mA
		V _{DD} = 15V, V _O = 13.5V	−3.6		−3.0	−8.8		−2.4		mA
I _{IN}	Input Current	V _{DD} = 15V, V _{IN} = 0V		−0.30		−10 ^{−5}	−0.30		−1.0	μA
		V _{DD} = 15V, V _{IN} = 15V		0.30		10 ^{−5}	0.30		1.0	μA

AC Electrical Characteristics*

T_A = 25°C, C_L = 50 pF, R_L = 200k and t_r = t_f = 20 ns, unless otherwise specified

Symbol	Parameter	Conditions	Min	Typ	Max	Units
t _{PHL} , t _{PLH}	Propagation Delay Time to a Logical “0” or Logical “1” from Clock to Q or \bar{Q} (CD40175 Only)	V _{DD} = 5V		190	300	ns
		V _{DD} = 10V		75	110	ns
		V _{DD} = 15V		60	90	ns
t _{PHL}	Propagation Delay Time to a Logical “0” from Clear to Q	V _{DD} = 5V		180	300	ns
		V _{DD} = 10V		70	110	ns
		V _{DD} = 15V		60	90	ns
t _{PLH}	Propagation Delay Time to a Logical “1” from Clear to \bar{Q} (CD40175 Only)	V _{DD} = 5V		230	400	ns
		V _{DD} = 10V		90	150	ns
		V _{DD} = 15V		75	120	ns
t _{SU}	Time Prior to Clock Pulse that Data must be Present	V _{DD} = 5V		45	100	ns
		V _{DD} = 10V		15	40	ns
		V _{DD} = 15V		13	35	ns
t _H	Time after Clock Pulse that Data Must be Held	V _{DD} = 5V		−11	0	ns
		V _{DD} = 10V		−4	0	ns
		V _{DD} = 15V		−3	0	ns
t _{THL} , t _{TLH}	Transition Time	V _{DD} = 5V		100	200	ns
		V _{DD} = 10V		50	100	ns
		V _{DD} = 15V		40	80	ns
t _{WH} , t _{WL}	Minimum Clock Pulse Width	V _{DD} = 5V		130	250	ns
		V _{DD} = 10V		45	100	ns
		V _{DD} = 15V		40	80	ns

AC Electrical Characteristics*

$T_A = 25^\circ\text{C}$, $C_L = 50\text{ pF}$, $R_L = 200\text{ k}\Omega$ and $t_r = t_f = 20\text{ ns}$, unless otherwise specified (Continued)

Symbol	Parameter	Conditions	Min	Typ	Max	Units
t_{WL}	Minimum Clear Pulse Width	$V_{DD} = 5\text{V}$ $V_{DD} = 10\text{V}$ $V_{DD} = 15\text{V}$		120 45 40	250 100 80	ns ns ns
t_{RCL}	Maximum Clock Rise Time	$V_{DD} = 5\text{V}$ $V_{DD} = 10\text{V}$ $V_{DD} = 15\text{V}$	15 5.0 5.0			μs μs μs
t_{fCL}	Maximum Clock Fall Time	$V_{DD} = 5\text{V}$ $V_{DD} = 10\text{V}$ $V_{DD} = 15\text{V}$	15 5.0 5.0	50 50 50		μs μs μs
f_{CL}	Maximum Clock Frequency	$V_{DD} = 5\text{V}$ $V_{DD} = 10\text{V}$ $V_{DD} = 15\text{V}$	2.0 5.0 6.0	3.5 10 12		MHz MHz MHz
C_{IN}	Input Capacitance	Clear Input Other Input		10 5.0	15 7.5	pF pF
C_{PD}	Power Dissipation	Per Package (Note 4)		130		pF

*AC Parameters are guaranteed by DC correlated testing.

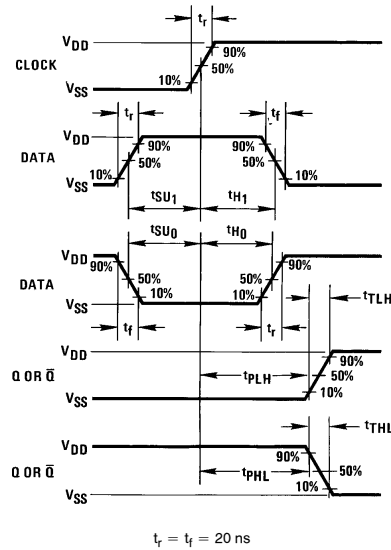
Note 1: "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed. They are not meant to imply that the devices should be operated at these limits. The tables of "Recommended Operating Conditions" and "Electrical Characteristics" provide conditions for actual device operation.

Note 2: $V_{SS} = 0\text{V}$ unless otherwise specified.

Note 3: I_{OH} and I_{OL} are tested one output at a time.

Note 4: C_{PD} determines the no load AC power consumption of any CMOS device. For complete explanation, see 54C/74C Family Characteristics application note, AN-90.

Switching Time Waveforms



TL/F/5987-3

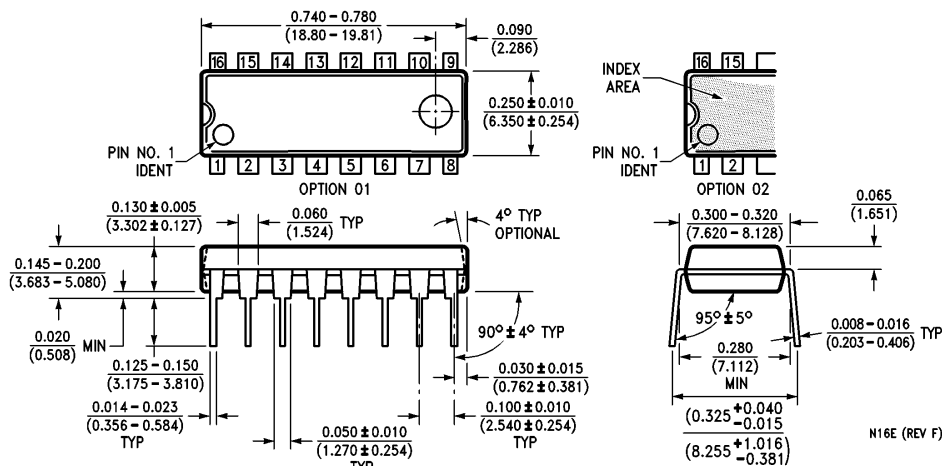
The drawing consists of three views of the J16A (REV L) component:

- Top View:** Shows a rectangular component with 16 pins. Dimensions include a total width of 0.785 [19.94] MAX, a pin pitch of 0.037 ± 0.005 [0.94 ± 0.13] TYP, and a pin diameter of 0.025 [0.64]. The component has a thickness of 0.220-0.310 [5.59-7.87] and a corner radius of R 0.005-0.020 [0.13-0.51] TYP.
- Side View:** Shows the component's profile with a height of 0.290-0.320 [7.37-8.13]. It features a glass sealant layer and a base with a thickness of 0.180 MAX [4.57]. The base has a width of 0.310-0.410 [7.87-10.41] and a 95° ± 5° TYP angle.
- End View:** Shows the component's end profile with a height of 0.200 [5.08] MAX TYP and a base thickness of 0.100 ± 0.010 [2.54 ± 0.25]. The base has a width of 0.125-0.200 [3.18-5.08] TYP and a 90° ± 4° TYP angle.

J16A (REV L)

J16A (REV L)

Physical Dimensions inches (millimeters) (Continued)



Molded Dual-In-Line Package (N)

Order Number CD40174BMN, CD40174BCN, CD40174BMN or CD40175BCN

NS Package Number N16E

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