

# DM54LS502/DM74LS502 8-Bit Successive Approximation Register

## **General Description**

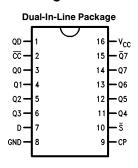
The LS502 is an 8-bit register with the interstage logic necessary to perform serial-to-parallel conversion and provide an active LOW Conversion Complete  $(\overline{\text{CC}})$  signal coincident with storage of the eighth bit. An active LOW Start  $(\overline{S})$  input performs synchronous initialization which forces Q7 LOW and all other outputs HIGH. Subsequent clocks shift this Q7 LOW signal downstream which simultaneously backfills the register such that the first serial data (D input) bit is stored in Q7, the second bit in Q6, the third in Q5, etc. The serial input data is also synchronized by an auxiliary flip-flop and brought out on Qp.

Designed primarily for use in the successive approximation technique for analog-to-digital conversion, the LS502 can also be used as a serial-to-parallel converter ring counter and as the storage and control element in recursive digital routines.

### **Features**

- Low power Schottky version of 2502
- Storage and control for successive approximation A to
- Performs serial-to-parallel conversion

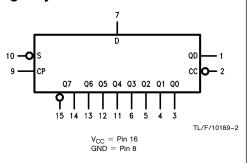
## **Connection Diagram**



TL/F/10189-1

Order Number DM54LS502J, DM54LS502W, DM74LS502WM or DM74LS502N See NS Package Number J16A, M16B, N16E or W16A

# **Logic Symbol**



Pin Names	Description							
D	Serial Data Input							
S	Start Input (Active LOW)							
CP	Clock Pulse Input (Active Rising Edge)							
$Q_D$	Synchronized Serial Data Output							
CC	Conversion Complete Output (Active LOW)							
Q0-Q7	Parallel Register Outputs							
Q7	Complement of Q7 Output							

# **Absolute Maximum Ratings (Note)**

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/Distributors for availability and specifications.

Supply Voltage 7V
Input Voltage 7V
Operating Free Air Temperature Range

DM54LS −55°C to +125°C DM74LS 0°C to +70°C

Storage Temperature Range  $-65^{\circ}\text{C}$  to  $+150^{\circ}\text{C}$ 

Note: The "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed. The device should not be operated at these limits. The parametric values defined in the "Electrical Characteristics" table are not guaranteed at the absolute maximum ratings. The "Recommended Operating Conditions" table will define the conditions for actual device operation.

# **Recommended Operating Conditions**

Symbol	Parameter		DM54LS502	2		Units			
Зушьог	raiametei	Min	Nom	Max	Min	Nom	Max	Jillis	
V <sub>CC</sub>	Supply Voltage	4.5	5	5.5	4.75	5	5.25	٧	
V <sub>IH</sub>	High Level Input Voltage	2			2			V	
V <sub>IL</sub>	Low Level Input Voltage			0.7			0.8	٧	
loh	High Level Output Current			-0.4			-0.4	mA	
l <sub>OL</sub>	Low Level Output Current			4			8	mA	
T <sub>A</sub>	Free Air Operating Temperature	-55		125	0		70	°C	
t <sub>s</sub> (H)	Setup Time HIGH or LOW  S to CP	5 5			16 16			ns	
t <sub>h</sub> (H)	Hold Time HIGH or LOW  S to CP	5 5			0			ns	
t <sub>s</sub> (H)	Setup Time HIGH or LOW D to CP	5 5			8 8			ns	
t <sub>h</sub> (H)	Hold Time HIGH or LOW D to CP	5 5			10 10			ns	
t <sub>w</sub> (H)	CP Pulse Width HIGH or LOW	20 20			46 46			ns	

# **Electrical Characteristics** over recommended operating free air temperature range (unless otherwise noted)

Symbol	Parameter	Conditions	Min	Typ (Note 1)	Max	Units	
VI	Input Clamp Voltage	$V_{CC} = Min, I_I = -18 \text{ mA}$				-1.5	V
V <sub>OH</sub>	High Level Output	$V_{CC} = Min, I_{OH} = Max,$	DM54	2.5			V
	Voltage	V <sub>IL</sub> = Max	DM74	2.7			
V <sub>OL</sub>	Low Level Output	V <sub>CC</sub> Min, I <sub>OL</sub> = Max,	DM54			0.4	V
	Voltage	V <sub>IH</sub> = Min	DM74			0.5	
		I <sub>OL</sub> = 4 mA, V <sub>CC</sub> = Min	DM74			0.4	
I <sub>I</sub>	Input Current @ Max Input Voltage	$V_{CC} = Max, V_I = 7V$ $V_I = 10V$	DM74 DM54			0.1	mA
I <sub>IH</sub>	High Level Input Current	$V_{CC} = Max, V_I = 2.7V$				20	μΑ
I <sub>IL</sub>	Low Level Input Current	$V_{CC} = Max, V_I = 0.4V$				-0.8	mA
los	Short Circuit	V <sub>CC</sub> = Max	DM54	-20		-100	mA
	Output Current	(Note 2)	DM74	-20		-100	IIIA
I <sub>CC</sub>	Supply Current	V <sub>CC</sub> = Max				65	mA

**Note 1:** All typicals are at  $V_{CC} = 5V$ ,  $T_A = 25$ °C.

Note 2: Note more than one output should be shorted at a time, and the duration should not exceed one second.

Switching	<b>Characteristics</b> $V_{CC} = +5.0V, T_A = +25^{\circ}C$
-----------	---

		DM54	LS502	DM74			
Symbol	Parameter		Units				
		Min	Max	Min	Max		
f <sub>max</sub>	Maximum Clock Frequency	25		15		MHz	
t <sub>PLH</sub>	Propagation Delay CP to Q <sub>n</sub> or <del>CC</del>		35 25		35 25	ns	

# **Functional Description**

The register stages are composed of transparent RS latches arranged in master/slave pairs. The master and slave latches are enabled separately by non-overlapping complementary signals \$1 and \$2\$ derived internally from the CP input. Master latches are enabled when CP is LOW and slave latches are enabled when CP is HIGH. Information is transferred from master to slave, and thus to the outputs, by the LOW-to-HIGH transition of CP.

Initializing the register requires a LOW signal on \$\overline{S}\$ while exercising CP. With \$\overline{S}\$ and CP LOW, all master latches are SET (Q side HIGH). A LOW-to-HIGH CP transition, with  $\overline{S}$ remaining LOW, then forces the slave latches to the condition wherein Q7 is LOW and all other register outputs, including CC, are HIGH. This condition will prevail as long as S remains LOW, regardless of subsequent CP rising edge. To start the conversion process,  $\overline{S}$  must return to the HIGH state. On the next CP rising edge, the information stored in the serial data input latch is transferred to QD and Q7, while Q6 is forced to the LOW state. On the rising edge of the next seven clocks, this LOW signal is shifted downstream, one bit at a time, while the serial data enters the register position one bit behind this LOW signal, as shown in the Truth Table. Note that after a serial data bit appears at a particular output, that register position undergoes no further changes. After the shifted LOW signal reaches CC, the register is locked up and no further changes can occur until the register is initialized for the next conversion process.

Figure a shows a simplified hook-up of a LS502, a D/A converter and a comparator arranged to convert an analog input voltage into an 8-bit binary number by the successive approximation technique. Figure b is an idealized graph showing the various values that the D/A converter output voltage can assume in the course of the conversion. The vertical axis is calibrated in fractions of the full-scale output capability of the D/A converter and the horizontal axis represents the successive states of the Truth Table. At time t1, Q7 is LOW and Q6-Q0 are HIGH, causing the D/A output to be one-half of full scale. If the analog input voltage is greater than this voltage the comparator output (hence the D input of the LS502) will be LOW, and at times t2 the D/A output will rise to three-fourths of full scale because Q7 will remain LOW and contribute 50% while Q6 is forced LOW and contributes another 25%. On the other hand, if the analog input voltage is less than one-half of full scale, the comparator output will be HIGH and Q7 will go HIGH at t2. Q6 will still be forced LOW at t2, and the D/A output will decrease to 25% of full scale. Thus with each successive clock, the D/A output will change by smaller increments. When the conversion is completed at t9, the binary number represented by the register outputs will be the numerator of the fraction n/256, representing the analog input voltage as a fraction of the full scale output D/A converter.

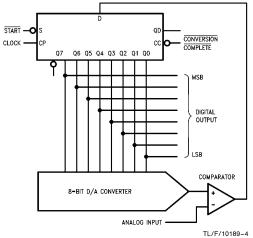
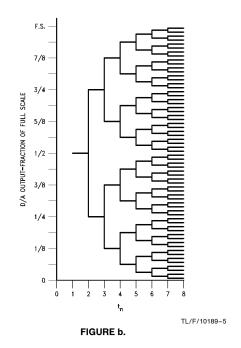


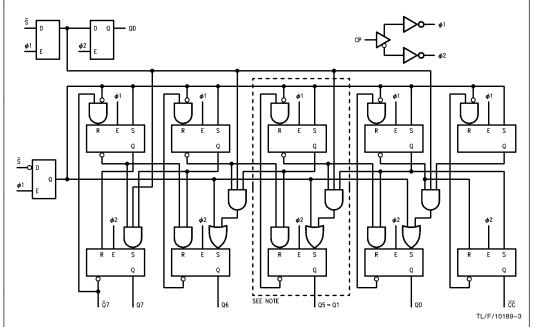
FIGURE a.



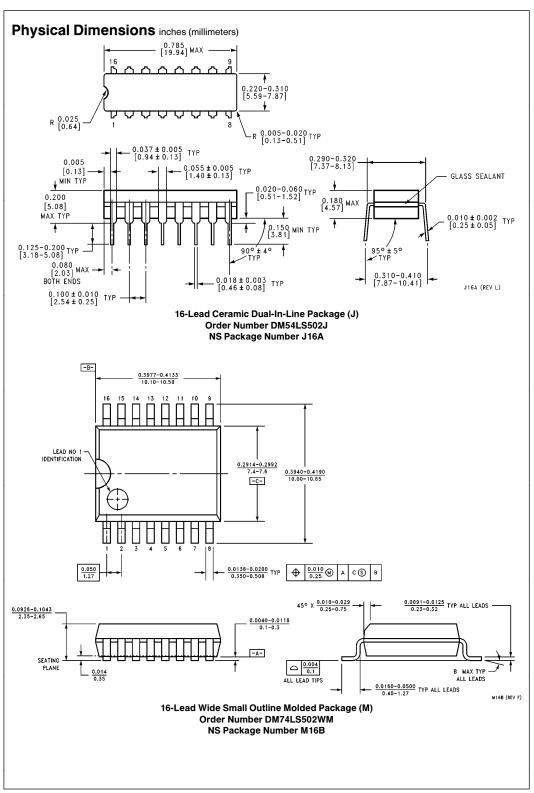
Truth Table												
Time	Inp	Inputs		Outputs								
t <sub>n</sub>	D	s	$Q_D$	Q7	Q6	Q5	Q4	Q3	Q2	Q1	Q0	CC
0	Х	L	Х	Х	Х	Х	Х	Х	Х	Х	Х	Χ
1	D7	Н	Х	L	Н	Н	Н	Н	Н	Н	Н	Н
2	D6	Н	D7	D7	L	Н	Н	Н	Н	Н	Н	Н
3	D6	Н	D6	D7	D6	L	Н	Н	Н	Н	Н	Н
4	D4	Н	D5	D7	D6	D5	L	Н	Н	Н	Н	Н
5	D3	Н	D4	D7	D6	D5	D4	L	Н	Н	Н	Н
6	D2	Н	D3	D7	D6	D5	D4	D3	L	Н	Н	Н
7	D1	Н	D2	D7	D6	D5	D4	D3	D2	L	Н	Н
8	D0	Н	D1	D7	D6	D5	D4	D3	D2	D1	L	Н
9	Х	Н	D0	D7	D6	D5	D4	D3	D2	D1	D0	L
10	Х	Н	Х	D7	D6	D5	D4	D3	D2	D1	D0	L

- $\begin{array}{l} H = \mbox{HIGH Voltage Level} \\ L = \mbox{LOW Voltage Level} \\ X = \mbox{Immaterial} \end{array}$

# **Logic Diagram**



Note: Cell logic is repeated for register stages Q5 to Q1.



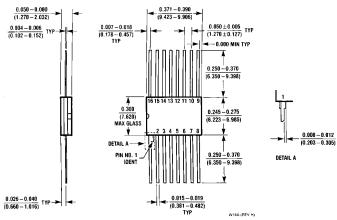
#### Physical Dimensions inches (millimeters) (Continued) $\frac{0.740 - 0.780}{(18.80 - 19.81)}$ $\frac{0.090}{(2.286)}$ 16 15 INDEX AREA 0.250 ± 0.010 (6.350 ± 0.254) $\Omega$ PIN NO. 1 IDENT PIN NO. 1 IDENT 1 2 3 4 5 6 7 8 1 2 \_ OPTION 01 OPTION 02 $\frac{0.065}{(1.651)}$ $\frac{0.130 \pm 0.005}{(3.302 \pm 0.127)}$ $\frac{0.060}{(1.524)}$ TYP 0.300 - 0.320 4° TYP (7.620 - 8.128) OPTIONAL 0.145 - 0.200 (3.683 - 5.080) 95°±5° 0.008 = 0.016 (0.203 = 0.406) TYP 90°±4° TYP 0.280 (7.112) MIN 0.125 - 0.150 (3.175 - 3.810) 0.030 ± 0.015 (0.762 ± 0.381)

 $\frac{0.050 \pm 0.010}{(1.270 \pm 0.254)}$ 

16-Lead Molded Dual-In-Line Package (N) Order Number DM74LS502N NS Package Number N16E

0.100 ± 0.010

(2.540 **±** 0.254) TYP



16-Lead Ceramic Flat Package (W) Order Number DM54LS502W NS Package Number W16A

#### LIFE SUPPORT POLICY

0.014 - 0.023

(0.356 = 0.584) TYP

NATIONAL'S PRODUCTS ARE NOT AUTHORIZED FOR USE AS CRITICAL COMPONENTS IN LIFE SUPPORT DEVICES OR SYSTEMS WITHOUT THE EXPRESS WRITTEN APPROVAL OF THE PRESIDENT OF NATIONAL SEMICONDUCTOR CORPORATION. As used herein:

- 1. Life support devices or systems are devices or systems which, (a) are intended for surgical implant into the body, or (b) support or sustain life, and whose failure to perform, when properly used in accordance with instructions for use provided in the labeling, can be reasonably expected to result in a significant injury to the user.
- 2. A critical component is any component of a life support device or system whose failure to perform can be reasonably expected to cause the failure of the life support device or system, or to affect its safety or effectiveness.

(0.325 +0.040

(8.255 +1.016) -0.381

N16E (REV F)



**National Semiconductor** 

National Semiconducto Corporation 1111 West Bardin Road Arlington, TX 76017 Tel: 1(800) 272-9959 Fax: 1(800) 737-7018

**National Semiconductor** Europe

Fax: (+49) 0-180-530 85 86 Fax: (+49) U-18U-35U oo oo Email: onjwege tevm2.nsc.com Deutsch Tel: (+49) 0-180-530 85 85 English Tei: (+49) 0-180-532 78 32 Français Tel: (+49) 0-180-532 93 58 Italiano Tel: (+49) 0-180-534 16 80 National Semiconductor

Hong Kong Ltd.
13th Floor, Straight Block,
Ocean Centre, 5 Canton Rd. Tsimshatsui, Kowloon Hong Kong Tel: (852) 2737-1600 Fax: (852) 2736-9960

National Semiconductor

Japan Ltd.
Tel: 81-043-299-2309
Fax: 81-043-299-2408