

UNISONIC TECHNOLOGIES CO., LTD

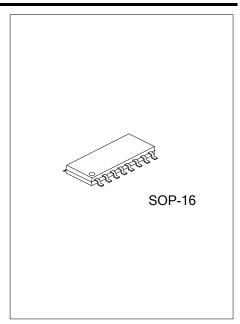
CD4014B Preliminary CMOS IC

CMOS 8-STAGE STATIC SHIFT REGISTERS

■ DESCRIPTION

The **UTC CD4014** is a 8-stage synchronous parallel or serial input/serial output registers having common CLOCK and PARALLEL/SERIAL CONTROL inputs, a SERIAL data input, and individual parallel inputs to each register stage. Each register is a D-type master-slave flip-flop. Q6, Q7, and Q8 are outputs. With the positive clock line transition in the **CD4014** parallel/serial entry is made into the register synchronously.

In CD4014 serial entry is controlled by the PARALLEL/SERIAL CONTROL input. When the PARALLEL/SERIAL CONTROL input is low, data is serially shifted into the 8-stage register synchronously with the positive transition of the clock line. When the PARALLEL/SERIAL CONTROL input is high, data is jammed into the 8-stage register via the parallel input lines and synchronous with the positive transition of the clock line.



■ FEATURES

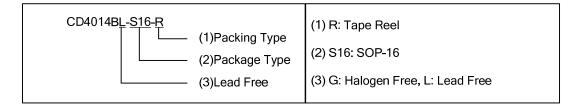
- * Up to 20V operation voltage
- * 12MHz (typ.) clock rate at 10V
- * Maximum input current of 1µA at 18V
- * Fully static operation
- * 8 master-slave flip-flops plus output buffering and control gating

■ APPLICATIONS

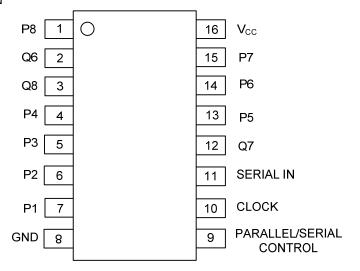
- * General-purpose register
- * Parallel input/serial output data queueing
- * Parallel to serial data conversion

■ ORDERING INFORMATION

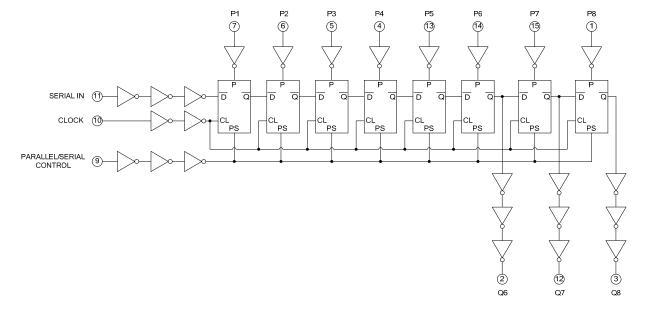
Ordering	Number	Dookogo	Dooking	
Lead Free	Halogen Free	Package	Packing	
CD4014BL-S16-R	CD4014BG-S16-R	SOP-16	Tape Reel	



■ PIN CONFIGURATION



■ LOGIC DIAGRAM



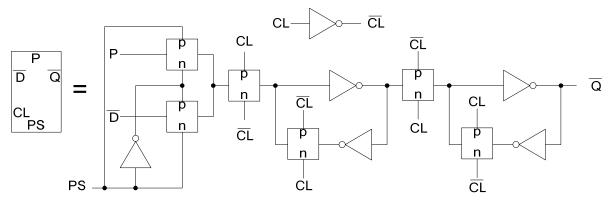


Fig.1 logic diagram

■ TRUE TABLE

CL	SER IN	PAR SER CONTROL	P ₁	P _n	Q ₁ (INTERNAL)	Qn
	X	1	0	0	0	0
	Х	1	1	0	1	0
	Х	1	0	1	0	1
	Х	1	1	1	1	1
	0	0	х	х	0	Q_{n-1}
	1	0	Х	Х	1	Q_{n-1}
	Х	Х	х	Х	Q ₁ (NC)	Q _N (NC)

Note: X = Don't Care Case, NC = No Change

■ ABSOLUTE MAXIMUM RATING (T_A =25°C, unless otherwise specified)

PARAMETER		SYMBOL	RATINGS	UNIT
Supply Voltage		V _{CC}	-0.5 ~ 20	V
Input Voltage		V_{IN}	-0.5 ~ V _{CC} + 0.5	V
Output Voltage		V_{OUT}	-0.5 ~ V _{CC} + 0.5	V
Input Clamp Current (V _{IN} <0, or V _{IN} >V _{CC})		l _{IK}	±10	mA
T ₄ =-55°C to +100°C		Б	500	mW
Power Dissipation	T _A =+100°C to +125°C	P_D	200	mW
Storage Temperature		T _{STG}	-65 ~ +150	°C

Note: 1. Absolute maximum ratings are those values beyond which the device could be permanently damaged.

Absolute maximum ratings are stress ratings only and functional device operation is not implied.

■ RECOMMENDED OPERATING COMDITIONS

PARAMETER	SYMBOL	CONDITIONS	MIN	MAX	UNIT	
Supply Voltage	V _{CC}		3	18	V	
		V _{CC} = 5V	180	-		
Clock Pulse Width	t _W	V _{CC} = 10V	80	-	ns	
		V _{CC} = 15V	50	-		
		V _{CC} = 5V	-	3		
Clock Frequency	f _{CL}	V _{CC} = 10V	-	6	MHz	
		V _{CC} = 15V	-	8.5		
	t _r , t _f	V _{CC} = 5V	-	15	μs	
Clock Rise and Fall Time		V _{CC} = 10V	-	15		
		V _{CC} = 15V	-	15		
		V _{CC} = 5V	120	-	ns	
Set-up Time, Serial Input		V _{CC} = 10V	80	-		
		V _{CC} = 15V	60	-	1	
		V _{CC} = 5V	80	-		
Set-up Time, Parallel Input	ts	V _{CC} = 10V	50	-	ns	
		V _{CC} = 15V	40	-		
Set-up Time, Parallel/Serial Control		V _{CC} = 5V	180	-		
		V _{CC} = 10V	80	-	ns	
		V _{CC} = 15V	60	-		

^{2.} The input and output voltage ratings may be exceeded if the input and output current ratings are observed.

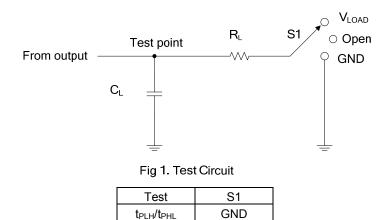
■ ELECTRICAL CHARACTERISTICS (T_A =25°C , unless otherwise specified)

PARAMETER	SYMBOL	TEST CONDITIONS	MIN	TYP	MAX	UNIT	
		$V_{IN} = 0, 5 \text{ V}, V_{CC} = 5 \text{ V}$		0.04	5		
				0.04	10		
Quiescent Supply Current	I _{CC}	V _{IN} = 0, 15V, V _{CC} = 15V		0.04	20	μA	
				0.08	100		
		$V_{OUT} = 0.4V, V_{IN} = 0, 5V, V_{CC} = 5V$	0.51	1			
Output Low (Sink) Current	I _{OL}	$V_{OUT} = 0.5V$, $V_{IN} = 0$, $10V$, $V_{CC} = 10V$	1.3	2.6		mA	
		$V_{OUT} = 1.5V, V_{IN} = 0, 15V, V_{CC} = 15V$	3.4	6.8			
		$V_{OUT} = 4.6V, V_{IN} = 0, 5V, V_{CC} = 5V$	-0.51	-1			
Output High (Source) Current	I _{OH}	$V_{OUT} = 2.5V, V_{IN} = 0, 5V, V_{CC} = 5V$	-1.6	-3.2		mA	
Output riigh (Source) Current	ЮН	$V_{OUT} = 9.5V, V_{IN} = 0, 10V, V_{CC} = 10V$	-1.3	-2.6			
		$V_{OUT} = 13.5V, V_{IN} = 0, 15V, V_{CC} = 15V$	-3.4	-6.8			
		$V_{IN} = 0, 5V, V_{CC} = 5V$		0	0.05		
Output Voltage: Low-Level	V_{OL}	$V_{IN} = 0$, 10V, $V_{CC} = 10V$		0	0.05		
		$V_{IN} = 0$, 15V, $V_{CC} = 15V$		0	0.05		
		$V_{IN} = 0, 5V, V_{CC} = 5V$	4.95	5			
Output Voltage: High-Level	V _{OH}	$V_{IN} = 0$, 10V, $V_{CC} = 10V$	9.95	10		V	
		$V_{IN} = 0$, 15V, $V_{CC} = 15V$	14.95	15			
		$V_{OUT} = 0.5, 4.5V, V_{CC} = 5V$			1.5		
Input Low Voltage	V_{IL}	$V_{OUT} = 1, 9V, V_{CC} = 10V$			3	V	
		$V_{OUT} = 1.5, 13.5V, V_{CC} = 15V$			4		
Input High Voltage		$V_{OUT} = 0.5, 4.5V, V_{CC} = 5V$	3.5				
	V_{IH}	$V_{OUT} = 1, 9V, V_{CC} = 10V$	7			V	
		$V_{OUT} = 1.5, 13.5V, V_{CC} = 15V$	11	_			
Input Leakage Current	I _{I(LEAK)}	$V_{IN} = 0$, 18 V, $V_{CC} = 18V$		±10 ⁻⁵	±0.1	μΑ	

■ SWITCHING CHARACTERISTICS ($T_A = 25$ °C, Input t_r , $t_f = 20$ ns, $C_L = 50$ Pf, $R_L = 200$ K Ω)

PARAMETER	SYMBOL	TEST CONDITIONS	MIN	TYP	MAX	UNIT
Propagation Delay Time		V _{CC} =5V		160	320	ns
	t _{PLH} / t _{PHL}	V _{CC} =10V		80	160	
		V _{CC} =15V		60	120	
		V _{CC} =5V		100	200	ns
Transition Time	t_{THL}/t_{TLH}	V _{CC} =10V		50	100	
		V _{CC} =15V		40	80	
		V _{CC} =5V	3	6		MHz
Maximum Clock Input Frequency	f_CL	V _{CC} =10V	6	12		
		V _{CC} =15V	8.5	17		
	t _W	V _{CC} =5V		90	180	ns
Minimum Clock Pulse Width		V _{CC} =10V		40	80	
		V _{CC} =15		25	50	
	t _r / t _f	V _{CC} =5V			15	
Clock Rise and Fall Time		V _{CC} =10V			15	μs
		V _{CC} =15V			15	
		V _{CC} =5V		60	120	
Minimum Setup Time, Serial Inputs	ts	V _{CC} =10V		40	80	ns
		V _{CC} =15V		30	60	
	ts	V _{CC} =5V		40	80	
Minimum Setup Time, Parallel Inputs		V _{CC} =10V		25	50	ns
·		V _{CC} =15V		20	40	
Minimum Hold Time, Serial In, Parallel In, Parallel/Serial Control		V _{CC} =5V			0	
	t _H	V _{CC} =10V			0	ns
		V _{CC} =15V			0	
Average Input Capacitance	Cı	Any Input		5	7.5	pF

■ TEST CIRCUITS AND WAVEFORMS



Inp	outs	V	V	C	R_L	
V_{IN}	t _r , t _f	VM	VLOAD	C_L		
V _{CC}	20 ns	V _{CC} /2	V _{CC}	50 pF	200 ΚΩ	

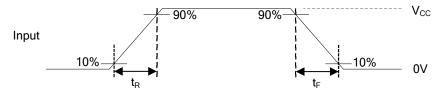


Fig 2. Voltage Waveforms Input Rise and Fall Times

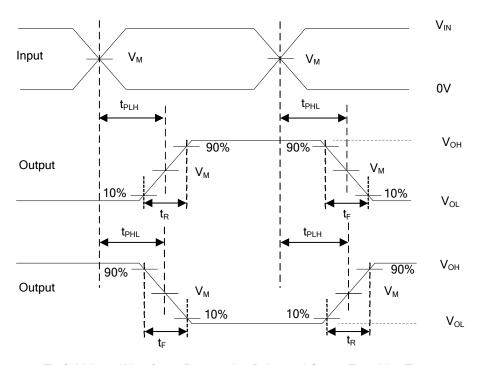


Fig 3. Voltage Waveforms Propagation Delay and Output Transition Times

Notes: 1. C_L includes probe and jig capacitance.

2. All input pulses are supplied by generators having the following characteristics: PRR \leq 1MHz, Z_0 = 50Ω .

■ TEST CIRCUITS AND WAVEFORMS(Cont.)

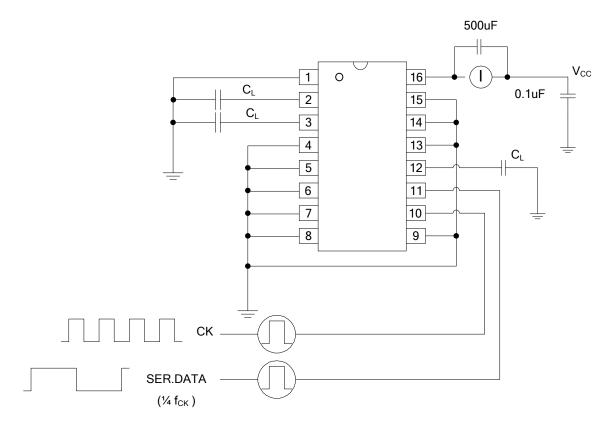


Fig 4. Dynamic power dissipation test circuit

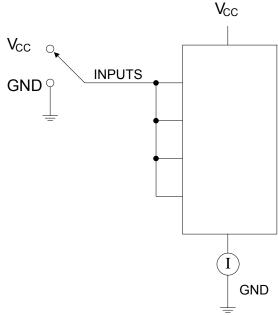


Fig 5. Quiescent device current test circuit

■ TEST CIRCUITS AND WAVEFORMS(Cont.)

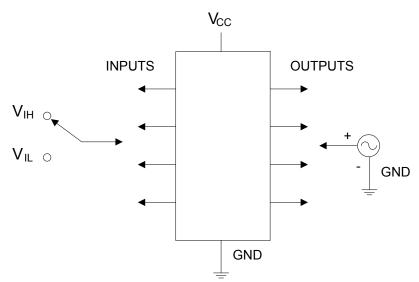


Fig 6. Input voltage test circuit

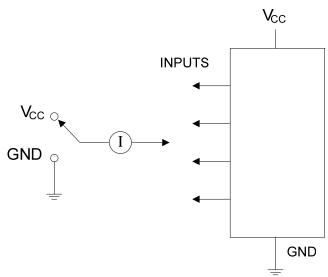


Fig 7. Input current test circuit

Note: measure inputs sequentially, to both V_{CC} and GND; connect all unused inputs to either V_{CC} or GND.

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