

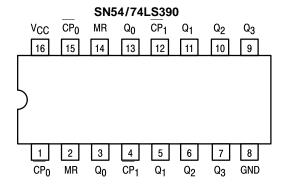
# DUAL DECADE COUNTER; DUAL 4-STAGE BINARY COUNTER

The SN54/74LS390 and SN54/74LS393 each contain a pair of high-speed 4-stage ripple counters. Each half of the LS390 is partitioned into a divide-by-two section and a divide-by five section, with a separate clock input for each section. The two sections can be connected to count in the 8.4.2.1 BCD code or they can count in a biquinary sequence to provide a square wave (50% duty cycle) at the final output.

Each half of the LS393 operates as a Modulo-16 binary divider, with the last three stages triggered in a ripple fashion. In both the LS390 and the LS393, the flip-flops are triggered by a HIGH-to-LOW transition of their CP inputs. Each half of each circuit type has a Master Reset input which responds to a HIGH signal by forcing all four outputs to the LOW state.

- Dual Versions of LS290 and LS293
- LS390 has Separate Clocks Allowing ÷2, ÷2.5, ÷5
- · Individual Asynchronous Clear for Each Counter
- Typical Max Count Frequency of 50 MHz
- Input Clamp Diodes Minimize High Speed Termination Effects

# **CONNECTION DIAGRAM DIP (TOP VIEW)**



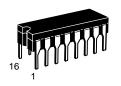
# SN54/74LS393 VCC CP MR Q<sub>0</sub> Q<sub>1</sub> Q<sub>2</sub> Q<sub>3</sub> 14 13 12 11 10 9 8 1 2 3 4 5 6 7 CP MR Q<sub>0</sub> Q<sub>1</sub> Q<sub>2</sub> Q<sub>3</sub> GND

NOTE: The Flatpak version has the same pinouts (Connection Diagram) as the Dual In-Line Package.

# SN54/74LS390 SN54/74LS393

DUAL DECADE COUNTER; DUAL 4-STAGE BINARY COUNTER

LOW POWER SCHOTTKY



J SUFFIX CERAMIC CASE 620-09



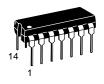
N SUFFIX PLASTIC CASE 648-08



D SUFFIX SOIC CASE 751B-03



J SUFFIX CERAMIC CASE 632-08



N SUFFIX PLASTIC CASE 646-06



**D SUFFIX** SOIC CASE 751A-02

### ORDERING INFORMATION

SN54LSXXXJ Ceramic SN74LSXXXN Plastic SN74LSXXXD SOIC

PIN NAME	S	LOADIN	G (Note a)
		HIGH	LOW
CP	Clock (Active LOW going edge) Input to +16 (LS393)	0.5 U.L.	1.0 U.L.
CP <sub>0</sub>	Clock (Active LOW going edge) Input to ÷2 (LS390)	0.5 U.L.	1.0 U.L.
CP <sub>1</sub>	Clock (Active LOW going edge)	0.5 U.L.	1.5 U.L.
MR	Input to ÷5 (LS390)  Master Reset (Active HIGH) Input	0.5 U.L. 0.5 U.L.	0.25 U.L.
$Q_0-Q_3$	Flip-Flop outputs (Note b)	10 U.L.	5 (2.5) U.L.

### NOTES:

- a) 1 TTL Unit Load (U.L.) = 40  $\mu$ A HIGH/1.6 mA LOW.
- b) The Output LOW drive factor is 2.5 U.L. for Military (54) and 5 U.L. for Commercial (74) Temperature Ranges.

# **FUNCTIONAL DESCRIPTION**

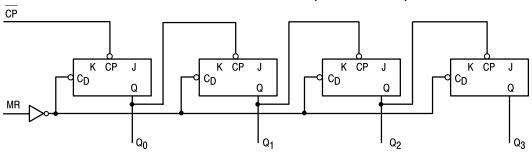
Each half of the SN54/74LS393 operates in the Modulo 16 binary sequence, as indicated in the ÷16 Truth Table. The first flip-flop is triggered by HIGH-to-LOW transitions of the CP input signal. Each of the other flip-flops is triggered by a HIGH-to-LOW transition of the Q output of the preceding flip-flop. Thus state changes of the Q outputs do not occur simultaneously. This means that logic signals derived from combinations of these outputs will be subject to decoding spikes and, therefore, should not be used as clocks for other counters, registers or flip-flops. A HIGH signal on MR forces all outputs to the LOW state and prevents counting.

Each half of the LS390 contains a  $\div 5$  section that is independent except for the common MR function. The  $\div 5$ 

section operates in 4.2.1 binary sequence, as shown in the  $\div$ 5 Truth Table, with the third stage output exhibiting a 20% duty cycle when the input frequency is constant. To obtain a  $\div$ 10 function <u>having</u> a 50% duty cycle output, con<u>nect</u> the input signal to CP<sub>1</sub> and connect the Q<sub>3</sub> output to the CP<sub>0</sub> input; the Q<sub>0</sub> output provides the desired 50% duty cycle output. If the input frequency is connected to CP<sub>0</sub> and the Q<sub>0</sub> output is connected to CP<sub>1</sub>, a decade divider operating in the 8.4.2.1 BCD code is obtained, as shown in the BCD Truth Table. Since the flip-flops change state asynchronously, logic signals derived from combinations of LS390 outputs are also subject to decoding spikes. A HIGH signal on MR forces all outputs LOW and prevents counting.

### SN54/74LS390 LOGIC DIAGRAM (one half shown) CP<sub>1</sub> CP<sub>0</sub> Κ Κ CP K CP K CP CP CD $C_D$ $C_D$ $C_D$ Q Q Q Q MR $Q_2$ $Q_0$ $I_{Q_1}$

# SN54/74LS393 LOGIC DIAGRAM (one half shown)



SN54/74LS390 BCD TRUTH TABLE\_\_\_ (Input on CP<sub>0</sub>; Q<sub>0</sub> CP<sub>1</sub>)

COLINIT					
COUNT	Q <sub>3</sub>	Q <sub>2</sub>	Q <sub>1</sub>	Q <sub>0</sub>	
0 1	┙┙	∟ ∟	∟ ∟	ıπ	•
2	L	L	Н	L	
3	L	L	Н	Н	
3 4 5	L	H	L	l L H	
	_			П.	
6 7 8	L L H	H H L	H H L	L H L	
9	Н	L	L	Н	

SN54/74LS390 ÷5 TRUTH TABLE (Input on CP<sub>1</sub>)

COLINIT	Ol			
COUNT	Q <sub>3</sub>	$Q_2$	Q <sub>1</sub>	
0	L	L	L	-
1	L	L	Н	
2	L	Н	L	
3	L	Н	Н	
4	Н	L	L	

 $\begin{array}{c} \text{SN54/74LS390} \div \text{10 (50\% @ Q}_0) \\ \text{TRUTH TABLE} \\ \text{(Input on CP}_1, Q_3 \text{ to CP}_0) \end{array}$ 

` .		• •		•	
COUNT					
COUNT	$Q_3$	$Q_2$	Q <sub>1</sub>	$Q_0$	
0	L	L	L	L	<b>-</b>
1	L	L	Н	L	
2	L	Н	L	L	
3	L	Н	Н	L	1
4 5	Н	L	L	L	1
5	┙	L	L	Н	
6	L	L	Н	Н	
7	L	Н	L	Н	1
8	L	Н	Н	Н	
9	Н	L	L	Н	

SN54/74LS393 TRUTH TABLE

COLINIT		OUTF	PUTS		
COUNT	Q <sub>3</sub>	$Q_2$	Q <sub>1</sub>	Q <sub>0</sub>	
0	L	L	L	L	<b>-</b>
1	L	L	L	Н	
1 2 3			Н	H L H	
3	L	L	Н	Н	
4 5	L	Н	L	L	
	L	Н	L	Н	
6		Н	Н	L H	
7	L	Н	Н	Н	
8	Н	L	L	L	
9	Н		L H	H L	
10	Н	L	Н	L	
11	Н	L	Н	Н	
12	Н	Н	L	L	
13	Н	Н	L	H L H	
14	Н	Н	Н	L	
15	Η	Η	Н	Н	

H = HIGH Voltage Level L = LOW Voltage Level

# **GUARANTEED OPERATING RANGES**

Symbol	Parameter		Min	Тур	Max	Unit
VCC	Supply Voltage	54 74	4.5 4.75	5.0 5.0	5.5 5.25	V
T <sub>A</sub>	Operating Ambient Temperature Range	54 74	-55 0	25 25	125 70	°C
ІОН	Output Current — High	54, 74			-0.4	mA
lOL	Output Current — Low	54 74			4.0 8.0	mA

# DC CHARACTERISTICS OVER OPERATING TEMPERATURE RANGE (unless otherwise specified)

				Limits				
Symbol	Parameter		Min	Тур	Max	Unit	Tes	t Conditions
VIH	Input HIGH Voltage		2.0			V	Guaranteed Input All Inputs	HIGH Voltage for
\/	Input LOW Voltage	54			0.7	V	Guaranteed Input	LOW Voltage for
VIL	input LOW voltage	74			0.8	ľ	All Inputs	
VIK	Input Clamp Diode Volta	ige		-0.65	-1.5	V	V <sub>CC</sub> = MIN, I <sub>IN</sub> =	-18 mA
V	Output HIGH Voltage	54	2.5	3.5		V	V <sub>CC</sub> = MIN, I <sub>OH</sub>	= MAX, V <sub>IN</sub> = V <sub>IH</sub>
VOH	Output HIGH voltage	74	2.7	3.5		V	or V <sub>IL</sub> per Truth T	able
Vo	Output LOW Voltage	54, 74		0.25	0.4	V	I <sub>OL</sub> = 4.0 mA V <sub>CC</sub> = V <sub>CC</sub> MIN,	
VOL	Output LOW Voltage	74		0.35	0.5	٧	I <sub>OL</sub> = 8.0 mA	VIN = VIL or VIH per Truth Table
I	Innut I IICI I Current				20	μΑ	V <sub>CC</sub> = MAX, V <sub>IN</sub>	= 2.7 V
lН	Input HIGH Current				0.1	mA	V <sub>CC</sub> = MAX, V <sub>IN</sub>	= 7.0 V
		MR			-0.4	mA		
I <sub>IL</sub>	Input LOW Current CP, CP <sub>0</sub>				-1.6	mA	V <sub>CC</sub> = MAX, V <sub>IN</sub> = 0.4 V	
		CP <sub>1</sub>			-2.4	mA		
los	Short Circuit Current (No	ote 1)	-20		-100	mA	V <sub>CC</sub> = MAX	
Icc	Power Supply Current				26	mA	V <sub>CC</sub> = MAX	

Note 1: Not more than one output should be shorted at a time, nor for more than 1 second.

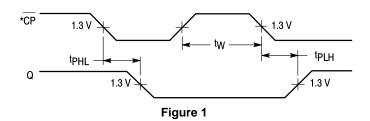
# AC CHARACTERISTICS ( $T_A = 25^{\circ}C$ , $V_{CC} = 5.0 \text{ V}$ )

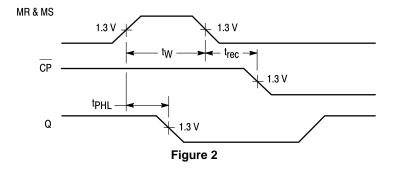
				Limits			
Symbol	Paramete	er	Min	Тур	Max	Unit	Test Conditions
f <sub>MAX</sub>	M <u>axi</u> mum Clock Freq CP <sub>0</sub> to Q <sub>0</sub>	uency	25	35		MHz	
f <sub>MAX</sub>	Maximum Clock Freq CP <sub>1</sub> to Q <sub>1</sub>	uency	20			MHz	
<sup>t</sup> PLH <sup>t</sup> PHL	Propagation Delay, CP to Q <sub>0</sub>	LS393		12 13	20 20	ns	
<sup>t</sup> PLH <sup>t</sup> PHL	CP <sub>0</sub> to Q <sub>0</sub>	LS390		12 13	20 20	ns	
<sup>t</sup> PLH <sup>t</sup> PHL	CP to Q <sub>3</sub>	LS393		40 40	60 60	ns	C <sub>L</sub> = 15 pF
<sup>t</sup> PLH <sup>t</sup> PHL	CP <sub>0</sub> to Q <sub>2</sub>	LS390		37 39	60 60	ns	
<sup>t</sup> PLH <sup>t</sup> PHL	CP <sub>1</sub> to Q <sub>1</sub>	LS390		13 14	21 21	ns	
<sup>t</sup> PLH <sup>t</sup> PHL	CP <sub>1</sub> to Q <sub>2</sub>	LS390		24 26	39 39	ns	
<sup>t</sup> PLH <sup>t</sup> PHL	CP <sub>1</sub> to Q <sub>3</sub>	LS390		13 14	21 21	ns	
<sup>t</sup> PHL	MR to Any Output	LS390/393		24	39	ns	

# AC SETUP REQUIREMENTS ( $T_A = 25^{\circ}C$ , $V_{CC} = 5.0 \text{ V}$ )

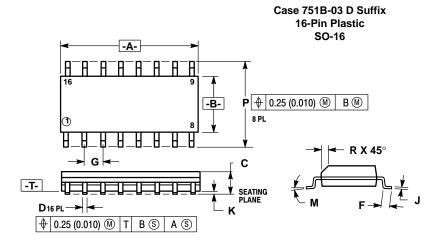
			Limits				
Symbol	Parame	ter	Min	Тур	Max	Unit	Test Conditions
t₩	Clock Pulse Width	LS393	20			ns	
tW	CP <sub>0</sub> Pulse Width	LS390	20			ns	
tW	CP <sub>1</sub> Pulse Width	LS390	40			ns	V <sub>CC</sub> = 5.0 V
tW	MR Pulse Width	LS390/393	20			ns	
t <sub>rec</sub>	Recovery Time	LS390/393	25			ns	

# AC WAVEFORMS

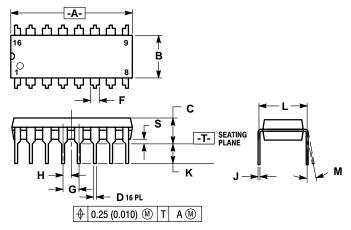


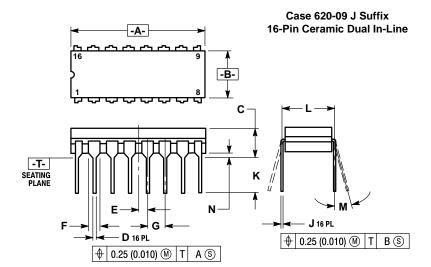


<sup>\*</sup>The number of Clock Pulses required between tpHL and tpLH measurements can be determined from the appropriate Truth Table.



# Case 648-08 N Suffix 16-Pin Plastic





- NOTES:
  1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
- CONTROLLING DIMENSION: MILLIMETER.
  DIMENSION A AND B DO NOT INCLUDE MOLD PROTRUSION.
  MAXIMUM MOLD PROTRUSION 0.15 (0.006)
- PER SIDE. 751B-01 IS OBSOLETE, NEW STANDARD 751B-03.

	MILLIM	ETERS	INC	HES	
DIM	MIN	MAX	MIN	MAX	
Α	9.80	10.00	0.386	0.393	
В	3.80	4.00	0.150	0.157	
С	1.35	1.75	0.054	0.068	
D	0.35	0.49	0.014	0.019	
F	0.40	1.25	0.016	0.049	
G	1.27	BSC	0.050 BSC		
J	0.19	0.25	0.008	0.009	
K	0.10	0.25	0.004	0.009	
M	0°	7°	0°	7°	
P	5.80	6.20	0.229	0.244	
R	0.25	0.50	0.010	0.019	

### NOTES:

- DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
- CONTROLLING DIMENSION: INCH.
  DIMENSION "L" TO CENTER OF LEADS WHEN
  FORMED PARALLEL.
- DIMENSION "B" DOES NOT INCLUDE MOLD
- ROUNDED CORNERS OPTIONAL. 648-01 THRU -07 OBSOLETE, NEW STANDARD

	MILLIM	ETERS	INC	HES	
DIM	MIN	MAX	MIN	MAX	
Α	18.80	19.55	0.740	0.770	
В	6.35	6.85	0.250	0.270	
С	3.69	4.44	0.145	0.175	
D	0.39	0.53	0.015	0.021	
F	1.02	1.77	0.040	0.070	
G	2.54	BSC	0.100 BSC		
Н	1.27	BSC	0.050	BSC	
J	0.21	0.38	0.008	0.015	
K	2.80	3.30	0.110	0.130	
L	7.50	7.74	0.295	0.305	
M	0°	10°	0°	10°	
S	0.51	1.01	0.020	0.040	

- OTES:

  1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.

  2. CONTROLLING DIMENSION: INCH.

  3. DIMENSION L TO CENTER OF LEAD WHEN FORMED PARALLEL.

  4. DIM F MAY NARROW TO 0.76 (0.030) WHERE THE LEAD ENTERS THE CERAMIC BODY.

  5. 620-01 THRU -08 OBSOLETE, NEW STANDARD 620.09
- 620-09.

	MILLIM	ETERS	INC	HES
DIM	MIN	MAX	MIN	MAX
Α	19.05	19.55	0.750	0.770
В	6.10	7.36	0.240	0.290
С	_	4.19	_	0.165
D	0.39	0.53	0.015	0.021
E	1.27	BSC	0.050 BSC	
F	1.40	1.77	0.055	0.070
G	2.54	BSC	0.100 BSC	
J	0.23	0.27	0.009	0.011
K	_	5.08	_	0.200
L	7.62	BSC	0.300	BSC
M	0°	15°	0°	15°
N	0.39	0.88	0.015	0.035

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