OV7649 Color CMOS VGA (640 x 480) CAMERACHIP™
OV7149 B&W CMOS VGA (640 x 480) CAMERACHIP™

General Description

The OV7649 (color) and OV7149 (black and white) CAMERACHIPS™ are low voltage CMOS image sensors that provide the full functionality of a single-chip VGA (640 x 480) camera and image processor in a small footprint package. The OV7649/OV7149 provides full-frame, sub-sampled or windowed 8-bit images in a wide range of formats, controlled through OmniVision's Serial Camera Control Bus (SCCB) interface.

This product family has an image array capable of operating at up to 30 frames per second (fps) with complete user control over image quality, formatting and output data transfer. All required image processing functions, including exposure control, gamma, white balance, color saturation, hue control and more, are also programmable through the SCCB interface. In addition, OmniVision CAMERACHIPS use proprietary sensor technology to improve image quality by reducing or eliminating common lighting/electrical sources of image contamination such as fixed pattern noise, smearing, blooming, etc. to produce a clean, fully stable color image.

Features

- High sensitivity for low-light operation
- 2.5V operating voltage for embedded portable apps
- Standard Serial Camera Control Bus (SCCB) interface
- VGA, QVGA (sub-sampled) and Windowed outputs with Raw RGB, RGB (GRB 4:2:2), YUV (4:2:2) and YCbCr (4:2:2) formats
- Automatic image control functions including: Automatic Exposure Control (AEC), Automatic Gain Control (AGC), Automatic White Balance (AWB), Automatic Brightness Control (ABC), Automatic Band Filter (ABF) for 60Hz noise and Automatic Black-Level Calibration (ABLC)
- Image quality controls including color saturation, hue, gamma, sharpness (edge enhancement), anti-blooming and zero smearing

Ordering Information

Product	Package
OV07649-K06A (Color, w/ lead)	CSP-22
OV07149-K06A (B&W w/ microlens, w/ lead)	CSP-22
OV07649-KL6A (color, lead-free)	CSP-22
OV07149-KL6A (B&W w/ microlens, lead-free)	CSP-22

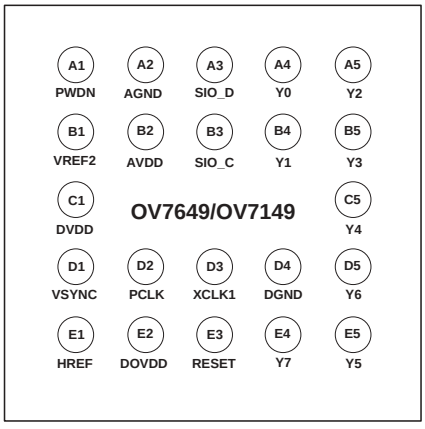
Applications

- Cellular Phones
- Picture Phones
- Toys
- PC Multimedia

Key Specifications

Array Size		640 x 480 (VGA)
Power Supply	**Core**	2.5VDC ± 10%
	Analog	2.5VDC ± 4%
	I/O	2.25V to 3.3V
Power Requirements	**Active**	40 mW (30 fps, including I/O power)
	Standby	30 µW
Temperature Range	**Operation**	-10°C to 70°C
	Stable Image	0°C to 50°C
Output Formats (8-bit)		• YUV/YCbCr 4:2:2 • RGB 4:2:2 • Raw RGB Data
Lens Size		1/4"
Maximum Image Transfer Rate	**VGA**	30 fps
	QVGA	60 fps
Sensitivity	**B&W**	2.20 V/Lux-sec
	Color	1.12 V/Lux-sec
S/N Ratio		46 dB
Dynamic Range		62 dB
Scan Mode		Progressive/Interlaced
Maximum Exposure Interval		523 x t_{ROW}
Gamma Correction		0.45
Pixel Size		5.6 µm x 5.6 µm
Dark Current		30 mV/s
Well Capacity		60 Ke
Fixed Pattern Noise		< 0.03% of $V_{PEAK-TO-PEAK}$
Image Area		3.6 mm x 2.7 mm
Package Dimensions		4930 µm x 4760 µm

Figure 1 OV7649/OV7149 Pin Diagram



Functional Description

Figure 2 shows the functional block diagram of the OV7649/OV7149 image sensor. The OV7649/OV7149 includes:

- Image Sensor Array (640 x 480 resolution)
- Timing Generator
- Analog Processing Block
- A/D Converters
- Output Formatter
- Digital Video Port
- SCCB Interface

Figure 2 OV7649/OV7149 Functional Block Diagram

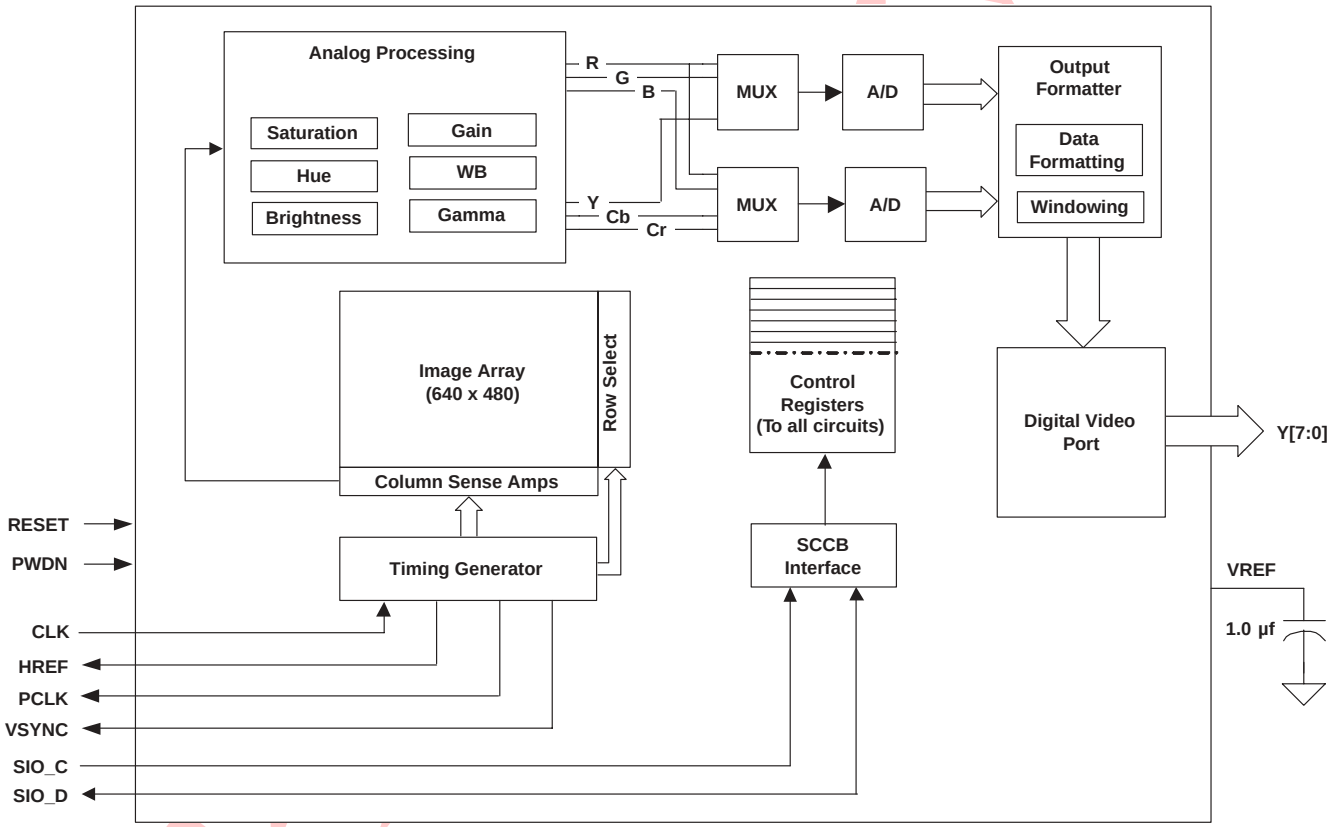
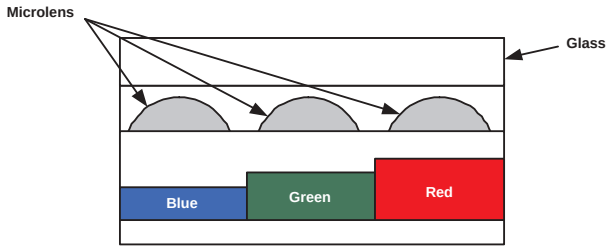


Image Sensor Array

The OV7649/OV7149 CAMERACHIPS has an active image array size of 640 columns x 480 rows (307,200 pixels). However, the full array contains 652 columns and 488 rows, with the extra 6 rows used for black-level calibration (“Optical Black”) and color interpolation information. However, the maximum output valid image window size is 652 columns by 482 rows. Figure 3 shows a cross-section of the image sensor array.

Figure 3 Image Sensor Array Cross-Section



Timing Generator

In general, the timing generator controls these functions:

- Array control and frame generation (VGA and QVGA outputs)
- Internal timing signal generation and distribution
- Frame rate timing
- Automatic Exposure Control (AEC)
- External timing outputs (VSYNC, HREF and PCLK)

Analog Processing Block

This block performs all analog image functions including:

- Automatic Gain Control (AGC)
- Automatic White Balance (AWB)
- Image quality controls including:
  - Color saturation
  - Hue
  - Gamma
  - Sharpness (edge enhancement)
  - Anti-blooming
  - Zero smearing

A/D Converters

After the Analog Processing Block, the color channel data signal is fed to two 8-bit Analog-to-Digital (A/D) converters via the multiplexers, one for the Y/G channel and one shared by the CbCr/BR channels. These A/D converters operate at speeds up to 12MHz, and are fully synchronous to the pixel rate (actual conversion rate is related to the frame rate).

In addition to the A/D conversion, this block also has the following functions:

- Digital Black-Level Calibration (BLC)
- Optional U/V channel delay
- Additional A/D range controls

In general, the combination of the A/D Range Multiplier and A/D Range Control sets the A/D range and maximum value to allow the user to adjust the final image brightness as a function of the individual application.

Output Formatter

This block controls all output and data formatting required prior to sending the image out.

Digital Video Port

Register bits COME[0] and COMK[6] increase I_{OL} / I_{OH} drive current and can be adjusted as a function of the customer’s loading:

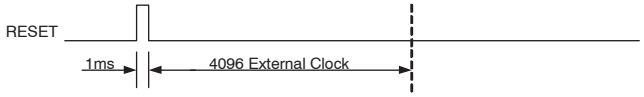
SCCB Interface

The Serial Camera Control Bus (SCCB) interface controls the CAMERACHIP operation. Refer to *OmniVision Technologies Serial Camera Control Bus (SCCB) Specification* for detailed usage of the serial control port.

RESET Timing

The RESET pin (E3) is active high. There is an internal pull-down (weak) resistor in the sensor so the default status of the RESET pin is low.

Figure 4 RESET Timing Diagram



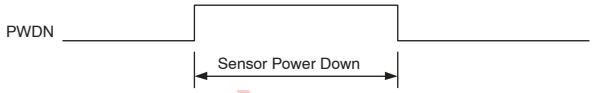
There are two ways for a sensor reset:

1. Hardware reset - Pulling the RESET pin high and keeping it high for at least 1 ms. As shown in Figure 4, after a reset has been initiated, the sensor will be most stable after the 4096 External Clock period.
2. Software reset - Writing 0x80 to register 0x12 (see “COMA” on page 13) for a software reset. If a software reset is used, a reset operation done twice is recommended to make sure the sensor is stable and ready to access registers. When performing a software reset twice, the second reset should be initiated after the 4096 External Clock period as shown in Figure 4.

PWDN Timing

The PWDN pin (A1) is active high. There is an internal pull-down (weak) resistor in the sensor so the default status of the PWDN pin is low.

Figure 5 PWDN Timing Diagram



Other Considerations

1. After writing to register COMC (0x14) to change the sensor mode, registers related to the sensor’s cropping window will be reset back to its default value.
2. After changing registers FRARH (0x2A) and FRARL (0x2B) to adjust the dummy pixels, it is necessary to write to register CLKRC (0x11) to reset the counter.

Pin Description

Table 1 Pin Description

Pin Number	Name	Pin Type	Function/Description
A1	PWDN	Input (0)[a]	Power Down Mode Selection 0: Normal mode 1: Power down mode
A2	AGND	Power	Analog ground
A3	SIO_D	I/O	SCCB serial interface data I/O
A4	Y0	Output	YUV video component output bit[0]
A5	Y2	Output	YUV video component output bit[2]
B1	VREF2	V_{REF}	Internal voltage reference (2.3V). Connect to ground through 1µF capacitor
B2	AVDD	Power	Analog power supply (+2.5 VDC)
B3	SIO_C	Input	SCCB serial interface clock input
B4	Y1	Output	YUV video component output bit[1]
B5	Y3	Output	YUV video component output bit[3]
C1	DVDD	Power	Power supply (+2.5 VDC) for digital core
C5	Y4	Output	YUV video component output bit[4]
D1	VSYNC	Output	Vertical sync output
D2	PCLK	Output	Pixel clock output
D3	XCLK1	Input	Crystal clock input
D4	DGND	Power	Digital ground
D5	Y6	Output	YUV video component output bit[6]
E1	HREF	Output	HREF output
E2	DOVDD	Power	Digital power supply (+2.5 to 3.3VDC) for I/O
E3	RESET	Input (0)	Clears all registers and resets them to their default values.
E4	Y7	Output	YUV video component output bit[7]
E5	Y5	Output	YUV video component output bit[5]

a. Input (0) represents an internal pull-down resistor.

Electrical Characteristics

Table 2 Absolute Maximum Ratings

Ambient Storage Temperature		-40ºC to +125ºC
Supply Voltages (with respect to Ground)	**V_{DD-A}**	5V
	V_{DD-C}	5V
	V_{DD-IO}	5V
All Input/Output Voltages (with respect to Ground)		-0.3V to VDD_IO+1V
Lead Temperature, Surface-mount process		216.7ºC
Lead-free Temperature, Surface-mount process		245ºC
ESD Rating, Human Body model		2000V

NOTE: Exceeding the Absolute Maximum ratings shown above invalidates all AC and DC electrical specifications and may result in permanent device damage.

Table 3 DC Characteristics (0°C < T_A < 70°C)

Symbol	Parameter	Condition	Min	Typ	Max	Unit
V_{DD-A}	DC supply voltage – Analog	—	2.40	2.5	2.60	V
V_{DD-C}	DC supply voltage – Core	—	2.25	2.5	2.75	V
V_{DD-IO}	DC supply voltage – I/O	—	2.25	—	3.3	V
I_{DDA}	Active (Operating) Current	See Note [a]		15		mA
$I_{DDS-SCCB}$	Standby Current	See Note [b]		1		mA
$I_{DDS-PWDN}$	Standby Current			10		µA
V_{IH}	Input voltage HIGH	CMOS	0.7 x V_{DD-IO}			V
V_{IL}	Input voltage LOW				0.3 x V_{DD-IO}	V
V_{OH}	Output voltage HIGH	CMOS (I_{OH} / I_{OL})	0.9 x V_{DD-IO}			V
V_{OL}	Output voltage LOW				0.1 x V_{DD-IO}	V
I_{OH}	Output current HIGH	See Note [c]	8			mA
I_{OL}	Output current LOW		15			mA
I_L	Input/Output Leakage	GND to V_{DD-IO}			± 1	µA

a. V_{DD-A} = V_{DD-C} = 2.5V, V_{DD-IO} = 3.0V
$I_{DDA} = \Sigma\{I_{DD-IO} + I_{DD-C} + I_{DD-A}\}$, f_{CLK} = 24MHz at 30 fps, no I/O loading

b. V_{DD-A} = V_{DD-C} = 2.5V, V_{DD-IO} = 3.0V
$I_{DDS:SCCB}$ refers to a SCCB-initiated Standby, while $I_{DDS:PWDN}$ refers to a PWDN pin-initiated Standby

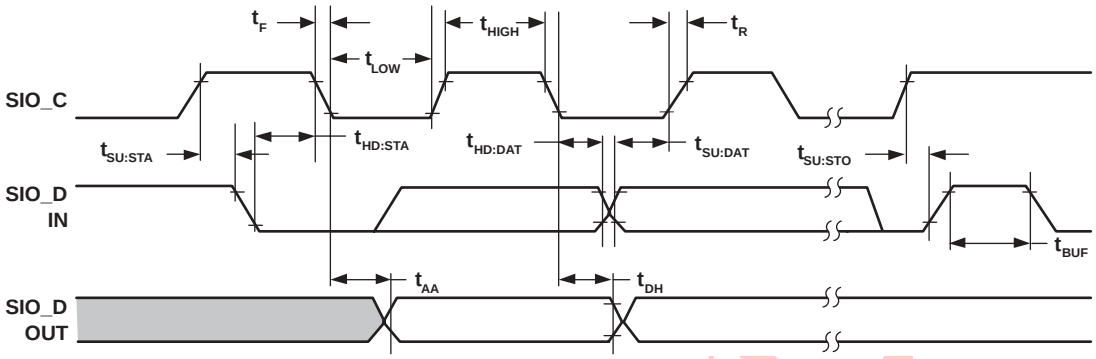
c. Standard Output Loading = 25pF, 1.2KΩ to 3V

Table 4 Functional and AC Characteristics (0°C < T_A < 70°C)

Symbol	Parameter	Min	Typ	Max	Unit
Functional Characteristics					
	A/D Differential Non-Linearity		± 1/2		LSB
	A/D Integral Non-Linearity		± 1		LSB
	AGC Range			21	dB
	Red/Blue Adjustment Range			12	dB
Inputs (PWDN, CLK, RESET)					
f_{CLK}	Input Clock Frequency	10	24	27	MHz
t_{CLK}	Input Clock Period	100	42	37	ns
$t_{CLK:DC}$	Clock Duty Cycle	45	50	55	%
$t_{S:RESET}$	Setting time after software/hardware reset			1	ms
$t_{S:REG}$	Settling time for register change (10 frames required)			300	ms
SCCB (SIO_C and SIO_D - see Figure 6)					
f_{SIO_C}	Clock Frequency			400	KHz
t_{LOW}	Clock Low Period	1.3			µs
t_{HIGH}	Clock High Period	600			ns
t_{AA}	SIO_C low to Data Out valid	100		900	ns
t_{BUF}	Bus free time before new START	1.3			µs
$t_{HD:STA}$	START condition Hold time	600			ns
$t_{SU:STA}$	START condition Setup time	600			ns
$t_{HD:DAT}$	Data-in Hold time	0			µs
$t_{SU:DAT}$	Data-in Setup time	100			ns
$t_{SU:STO}$	STOP condition Setup time	600			ns
t_{R}, t_{F}	SCCB Rise/Fall times			300	ns
t_{DH}	Data-out Hold time	50			ns
Outputs (VSYNC, HREF, PCLK, and Y[7:0] - see Figure 7, Figure 8, and Figure 9)					
t_{PDV}	PCLK[↓] to Data-out Valid			5	ns
t_{SU}	Y[7:0] Setup time	15			ns
t_{HD}	Y[7:0] Hold time	8			ns
t_{PHH}	PCLK[↓] to HREF[↑]	0		5	ns
t_{PHL}	PCLK[↓] to HREF[↓]	0		5	ns
AC Conditions:	• V_{DD}: V_{DD-A} = V_{DD-C} = 2.5V, V_{DD-IO} = 3.3V • Rise/Fall Times: I/O: 5ns, Maximum SCCB: 300ns, Maximum • Input Capacitance: 10pf • Output Loading: 25pF, 1.2KΩ to 3V • f_{CLK}: 24MHz				

Timing Specifications

Figure 6 SCCB Timing Diagram



Note: For the following timing diagrams, VSYNC changes at rising edge of PCLK position and HREF/HSYNC changes at falling edge of PCLK position.

Figure 7 Row Output Timing Diagram

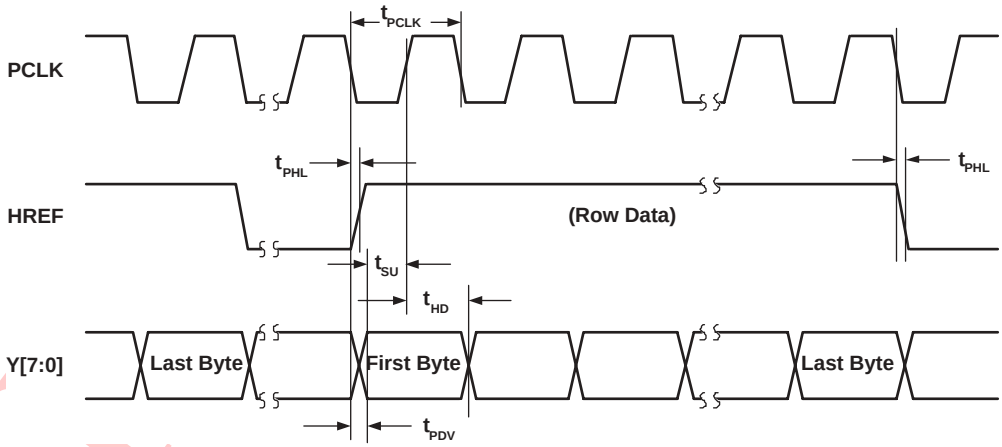


Figure 8 VGA Frame Timing Diagram

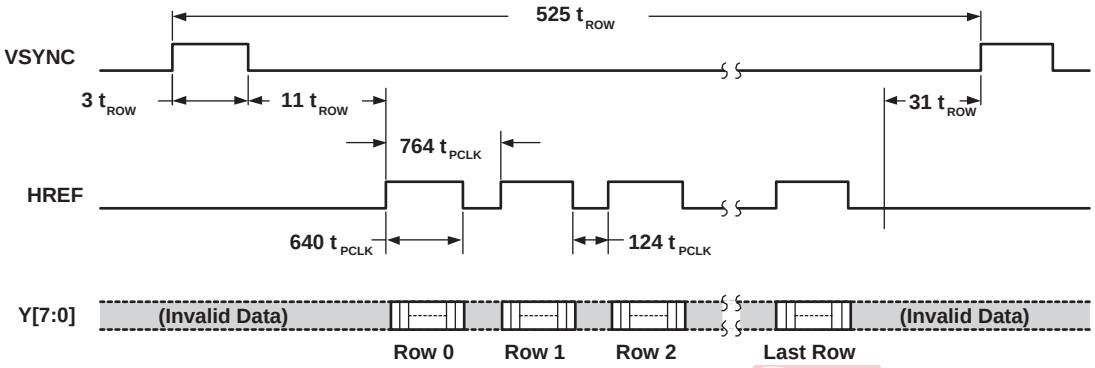
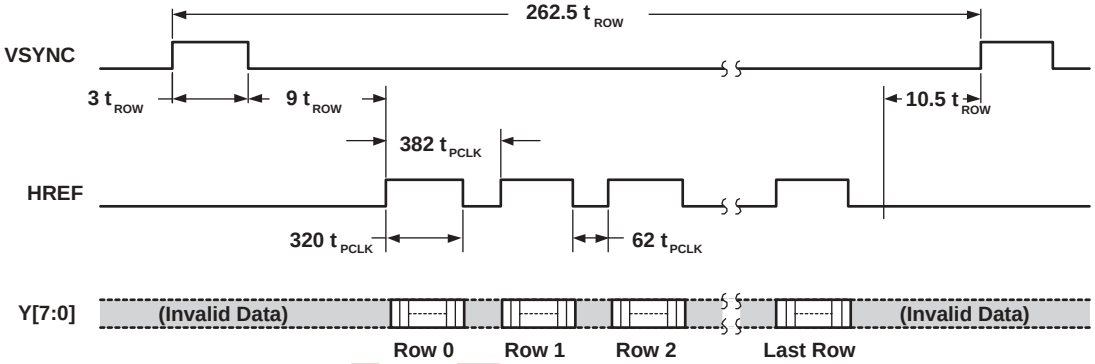


Figure 9 QVGA Frame Timing Diagram



Note: As the RGB, YUV and YCbCr formats use the Bayer pattern for interpolation, the first row transferred out on the Y[7:0] bus will be invalid, as there is no row above Row #1 to provide the 'pair data' required. Because of this, the OV7649 does not enable the HREF signal during the first row read (shown above in the 'invalid data' zone).

Figure 10 RGB:565 Output Timing Diagram

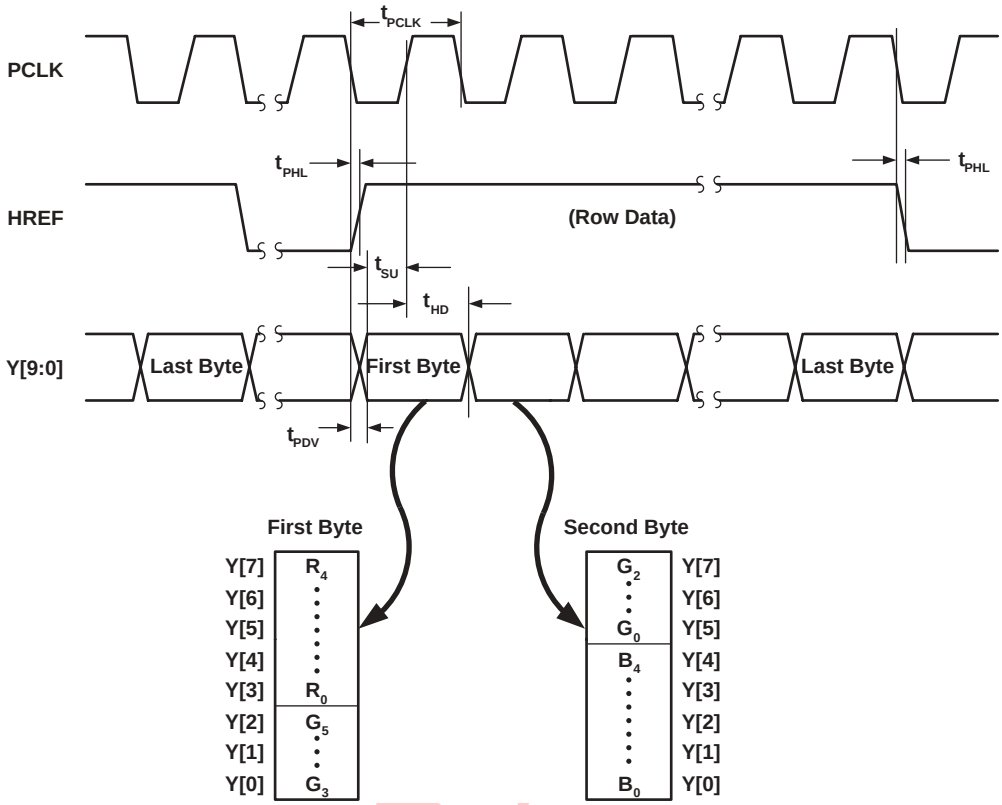
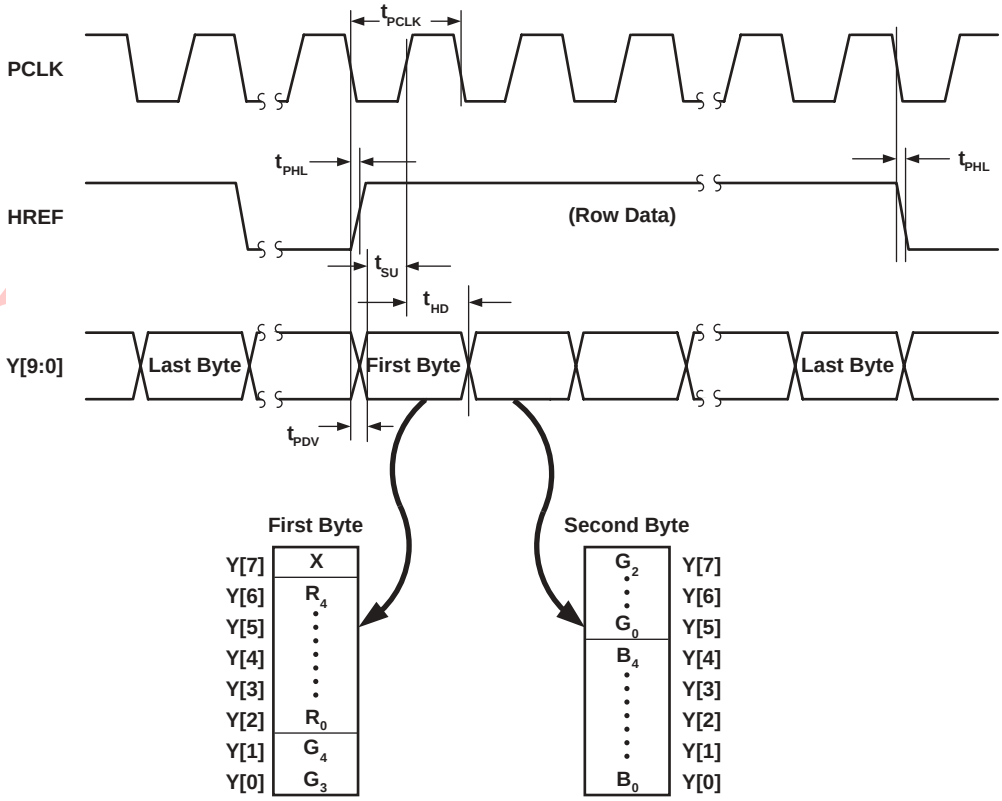
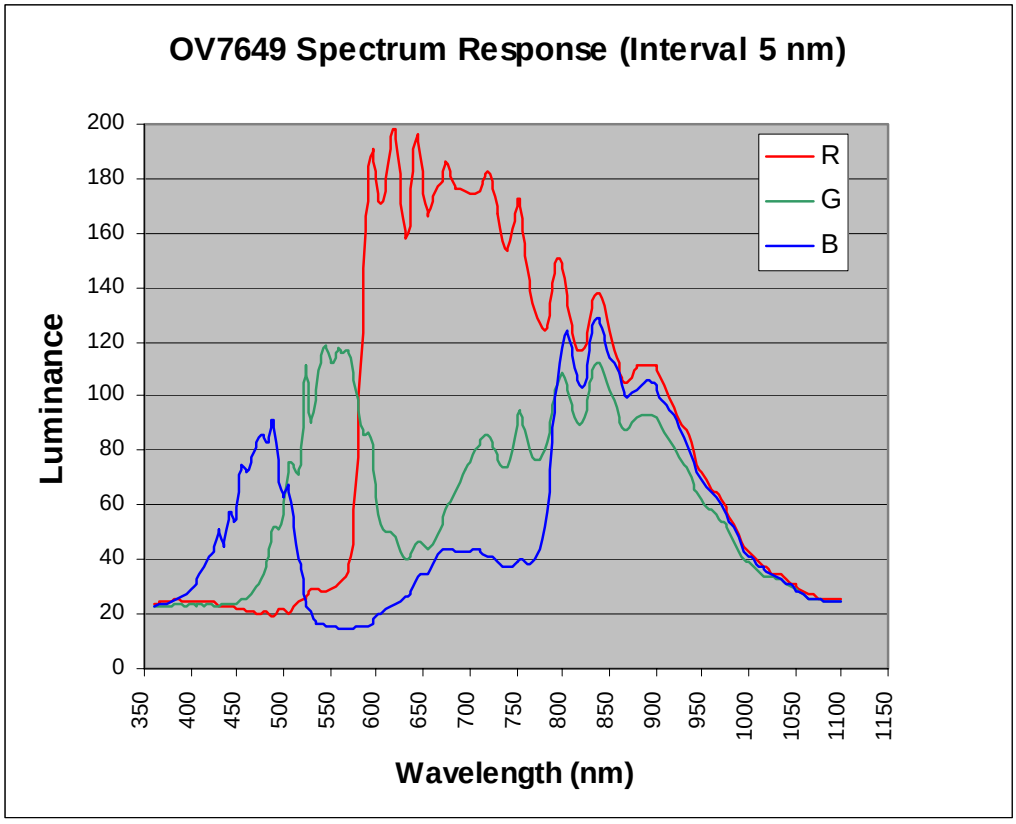


Figure 11 RGB:555 Output Timing Diagram



OV7649 Light Response

Figure 12 OV7649 Light Response



Register Set

Table 5 provides a list and description of the Device Control registers contained in the OV7649/OV7149. For all register Enable/Disable bits, ENABLE=1 and DISABLE=0. The device slave addresses for the OV7649/OV7149 are 42 for write and 43 for read.

Table 5 SCCB Register List

Address (Hex)	Register Name	Default (Hex)	R/W	Description
00	GAIN	00	RW	AGC – Gain control gain setting Bit[7:6]: Reserved Bit[5:0]: Gain control gain setting • Range: [00] to [3F]
01	BLUE	80	RW	AWB – Blue channel gain setting • Range: [00] to [FF] ***Note:*** *This function is not available on the B&W OV7149.*
02	RED	80	RW	AWB – Red channel gain setting • Range: [00] to [FF] ***Note:*** *This function is not available on the B&W OV7149.*
03	SAT	84	RW	Image Format – Color saturation value Bit[7:4]: Saturation value • Range: [0] to [F] Bit[3:0]: Reserved ***Note:*** *This function is not available on the B&W OV7149.*
04	HUE	34	RW	Image Format – Color hue control Bit[7:6]: Reserved Bit[5]: Hue Enable Bit[4:0]: Hue setting ***Note:*** *This function is not available on the B&W OV7149.*
05	CWF	3E	RW	AWB – Red/Blue Pre-Amplifier gain setting Bit[7:4]: Red channel pre-amplifier gain setting • Range: [0] to [F] Bit[3:0]: Blue channel pre-amplifier gain setting • Range: [0] to [F] ***Note:*** *This function is not available on the B&W OV7149.*
06	BRT	80	RW	ABC – Brightness setting • Range: [00] to [FF]
07-09	RSVD	XX	–	Reserved
0A	PID	76	R	Product ID number (Read only)
0B	VER	48	R	Product version number (Read only)
0C-0F	RSVD	XX	–	Reserved
10	AECH	41	RW	Exposure Value

Table 5 SCCB Register List

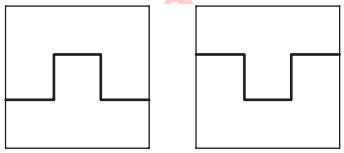
Address (Hex)	Register Name	Default (Hex)	R/W	Description
11	CLKRC	00	RW	Data Format and Internal Clock Bit[7:6]: Data Format – HSYNC/VSYNC Polarity 00: HSYNC = NEG VSYNC = POS 01: HSYNC = NEG VSYNC = NEG 10: HSYNC = POS VSYNC = POS 11: HSYNC = NEG VSYNC = POS  POS NEG Bit[5:0]: Internal Clock Pre-Scalar • Range: [0] to [3F]
12	COMA	14	RW	Common Control A Bit[7]: SCCB – Register Reset 0: No change 1: Reset all registers to default values Bit[6]: Output Format – Mirror Image Enable Bit[5]: Reserved Bit[4]: Data Format – YUV formatting (when register COMD[0] = 0) 0: Y U Y V Y U Y V 1: U Y V Y U Y V Y (when register COMD[0] = 1) 0: Y V Y U Y V Y U 1: V Y U Y V Y U Y Bit[3]: Output Format – Output Channel Select A 0: YUV/YCbCr 1: RGB/Raw RGB Bit[2]: AWB – Enable Bit[1:0]: Reserved ***Note:*** *This function is not available on the B&W OV7149.*
13	COMB	A3	RW	Common Control B Bit[7:5]: Reserved Bit[4]: Data Format – ITU-656 Format Enable 0: YUV/YCbCr 4:2:2 1: ITU-656 format enabled Bit[3]: Reserved Bit[2]: SCCB – Tri-State Enable – Y[7:0] Bit[1]: AGC – Enable Bit[0]: AEC – Enable

Table 5 SCCB Register List

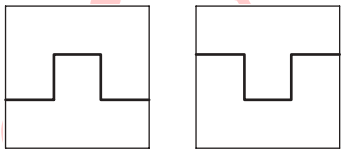
Address (Hex)	Register Name	Default (Hex)	R/W	Description
14	COMC	04	RW	Common Control C Bit[7:6]: Reserved Bit[5]: Output Format – Resolution 0: VGA (640x480) 1: QVGA (320x240) Bit[4]: Reserved Bit[3]: Data Format – HREF Polarity 0: HREF Positive 1: HREF Negative  POS NEG Bit[2:0]: Reserved
15	COMD	00	RW	Common Control D Bit[7]: Data Format – Output Flag Bit Disable 0: Frame = 254 data bits (00/FF = Reserved flag bits) 1: Frame = 256 data bits Bit[6]: Data Format – Y[7:0]-PCLK Reference Edge 0: Y[7:0] data out on PCLK falling edge 1: Y[7:0] data out on PCLK rising edge Bit[5:1]: Reserved Bit[0]: Data Format – UV Sequence Exchange (when register COMA[4] = 0) 0: Y U Y V Y U Y V 1: Y V Y U Y V Y U (when register COMA[4] = 1 0: U Y V Y U Y V Y 1: V Y U Y V Y U Y ***Note:*** *Bit[0] is not programmable on the B&W OV7149.*
16	RSVD	XX	–	Reserved
17	HSTART	1A	RW	Output Format – Horizontal Frame (HREF Column) Start
18	HSTOP	BA	RW	Output Format – Horizontal Frame (HREF Column) Stop
19	VSTRT	03	RW	Output Format – Vertical Frame (Row) Start
1A	VSTOP	F3	RW	Output Format – Vertical Frame (Row) Stop
1B	PSHFT	00	RW	Data Format – Pixel Delay Select (Delays timing of the Y[7:0] data relative to HREF in pixel units) • Range: [00] (No delay) to [FF] (256 pixel delay)
1C	MIDH	7F	R	Manufacturer ID Byte – High (Read only = 0x7F)
1D	MIDL	A2	R	Manufacturer ID Byte – Low (Read only = 0xA2)
1E	RSVD	XX	–	Reserved

Table 5 SCCB Register List

Address (Hex)	Register Name	Default (Hex)	R/W	Description
1F	FACT	01	RW	Output Format – Format Control Bit[7:5]: Reserved Bit[4]: RGB:565/555 Enable Control 0: Disabled 1: Enabled ***Note:*** *Bit[4] is not programmable on the B&W OV7149.* Bit[3]: Reserved Bit[2]: RGB:565/555 Mode Select 0: RGB:565 output format 1: RGB:555 output format ***Note:*** *Bit[2] is not programmable on the B&W OV7149.* Bit[1:0]: Reserved
20	COME	C0	RW	Common Control E Bit[7]: Reserved Bit[6]: AEC – Digital Averaging Enable Bit[5]: Reserved Bit[4]: Image Quality – Edge Enhancement Enable Bit[3:1]: Reserved Bit[0]: Y[7:0] 2X I_{OL} / I_{OH} Enable
21-23	RSVD	XX	–	Reserved
24	AEW	10	RW	AGC/AEC – Stable Operating Region – Upper Limit
25	AEB	8A	RW	AGC/AEC – Stable Operating Region – Lower Limit
26	COMF	A2	RW	Common Control F Bit[7:3]: Reserved Bit[2]: Data Format – Output Data MSB/LSB Swap Enable (LSB → MSB (Y[7]) and MSB → LSB (Y[0]) Bit[1:0]: Reserved
27	COMG	E2	RW	Common Control G Bit[7:5]: Reserved Bit[4]: Color Matrix – RGB Crosstalk Compensation Disable (Used to increase each color filter's efficiency) ***Note:*** *Bit[4] is not programmable on the B&W OV7149.* Bit[3:2]: Reserved Bit[1]: Data Format – Output Full Range Enable 0: Output Range = [10] to [F0] (224 bits) 1: Output Range = [01] to [FE] (254/256 bits) Bit[0]: Reserved

Table 5 SCCB Register List

Address (Hex)	Register Name	Default (Hex)	R/W	Description
28	COMH	20	RW	Common Control H Bit[7]: Output Format – RGB Output Select 0: RGB 1: Raw RGB ***Note:*** *Bit[7] is NOT programmable when COMA[3] = 0.* Bit[6]: Device Select 0: OV7649 1: OV7149 Bit[5]: Output Format – Scan Select 0: Interlaced 1: Progressive Bit[4:0]: Reserved
29	COMI	00	R	Common Control I Bit[7:2]: Reserved Bit[1:0]: Device Version (Read-only)
2A	FRARH	00	RW	Output Format – Frame Rate Adjust High Bit[7]: Data Format – Frame Rate Adjust Enable Bit[6:5]: Data Format – Frame Rate Adjust Setting MSB FRA[9:0] = MSB + LSB = FRARH[6:5] + FRARL[7:0] Bit[4]: A/D – UV Channel '2 Pixel Delay' Enable ***Note:*** *Bit[4] is not programmable on the B&W OV7149.* Bit[3:0]: Reserved
2B	FRARL	00	RW	Data Format – Frame Rate Adjust Setting LSB FRA[9:0] = MSB + LSB = FRARH[6:5] + FRARL[7:0]
2C	RSVD	XX	–	Reserved
2D	COMJ	81	RW	Common Control J Bit[7:3]: Reserved Bit[2]: AEC – Band Filter Enable Bit[1:0]: Reserved
2E-5F	RSVD	XX	–	Reserved
60	SPCB	06	RW	Signal Process Control B Bit[7]: AGC – 1.5x Multiplier (Pre-amplifier) Enable Bit[6:0]: Reserved
61-6B	RSVD	XX	–	Reserved
6C	RMCO	11	RW	Color Matrix – RGB Crosstalk Compensation – R Channel ***Note:*** *This function is not available on the B&W OV7149.*
6D	GMCO	01	RW	Color Matrix – RGB Crosstalk Compensation – G Channel ***Note:*** *This function is not available on the B&W OV7149.*
6E	BMCO	06	RW	Color Matrix – RGB Crosstalk Compensation– B Channel ***Note:*** *This function is not available on the B&W OV7149.*
6F	RSVD	XX	–	Reserved

Table 5 SCCB Register List

Address (Hex)	Register Name	Default (Hex)	R/W	Description
70	COMK	01	RW	Common Mode Control K Bit[7]: Reserved Bit[6]: Y[7:0] 2X I_{OL} / I_{OH} Enable Bit[5:0]: Reserved
71	COML	00	RW	Common Mode Control L Bit[7]: Reserved Bit[6]: Data Format – PCLK output gated by HREF Enable Bit[5]: Data Format – Output HSYNC on HREF Pin Enable Bit[4]: Reserved Bit[3:2]: Data Format – HSYNC Rising Edge Delay MSB Bit[1:0]: Data Format – HSYNC Falling Edge Delay MSB
72	HSDYR	10	RW	Data Format – HSYNC Rising Edge Delay LSB HSYNCR[9:0] = MSB + LSB = COML[3:2] + HSDYR[7:0] • Range 000 to 762 pixel delays
73	HSDYF	50	RW	Data Format – HSYNC Falling Edge Delay LSB HSYNCF[9:0] = MSB + LSB = COML[1:0] + HSDYF[7:0] • Range 000 to 762 pixel delays
74	COMM	20	RW	Common Mode Control M Bit[7]: Reserved Bit[6:5]: AGC – Maximum Gain Select 00: +6 dB 01: +12 dB 10: +6 dB 11: +18 dB Bit[4:0]: Reserved
75	COMN	02	RW	Common Mode Control N Bit[7]: Output Format – Vertical Flip Enable Bit[6:0]: Reserved
76	COMO	00	RW	Common Mode Control O Bit[7:6]: Reserved Bit[5]: Standby Mode Enable Bit[4:0]: Reserved
77-7D	RSVD	XX	–	Reserved
7E	AVGY	00	RW	AEC – Digital Y/G Channel Average (Automatically updated by AGC/AEC, user can only read the values)
7F	AVGR	00	RW	AEC – Digital R/V Channel Average (Automatically updated by AGC/AEC, user can only read the values) ***Note:*** *This function is not available on the B&W OV7149.*
80	AVGB	00	RW	AEC – Digital B/U Channel Average (Automatically updated by AGC/AEC, user can only read the values) ***Note:*** *This function is not available on the B&W OV7149.*
NOTE: All other registers are factory-reserved. Please contact OmniVision Technologies for reference register settings.				

Package Specifications

The OV7649/OV7149 uses a 22-ball Chip Scale Package (CSP). Refer to Figure 13 for package information, Table 6 for package dimensions and Figure 14 for the array center on the chip.

Note: For OVT devices that contain lead, all part marking letters are upper case. For OVT devices that are lead-free, all part marking letters are lower case

Figure 13 OV7649/OV7149 Package Specifications

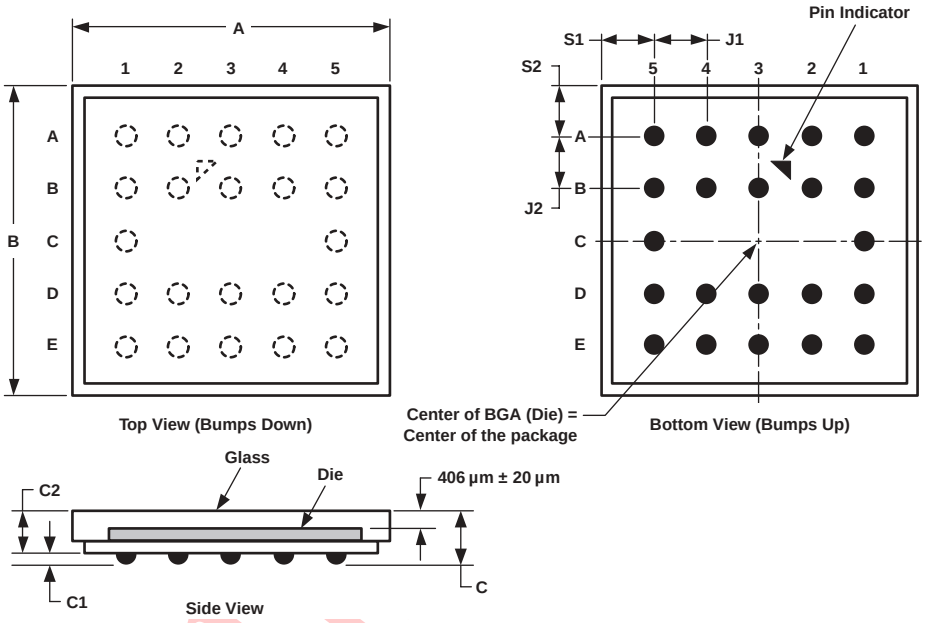
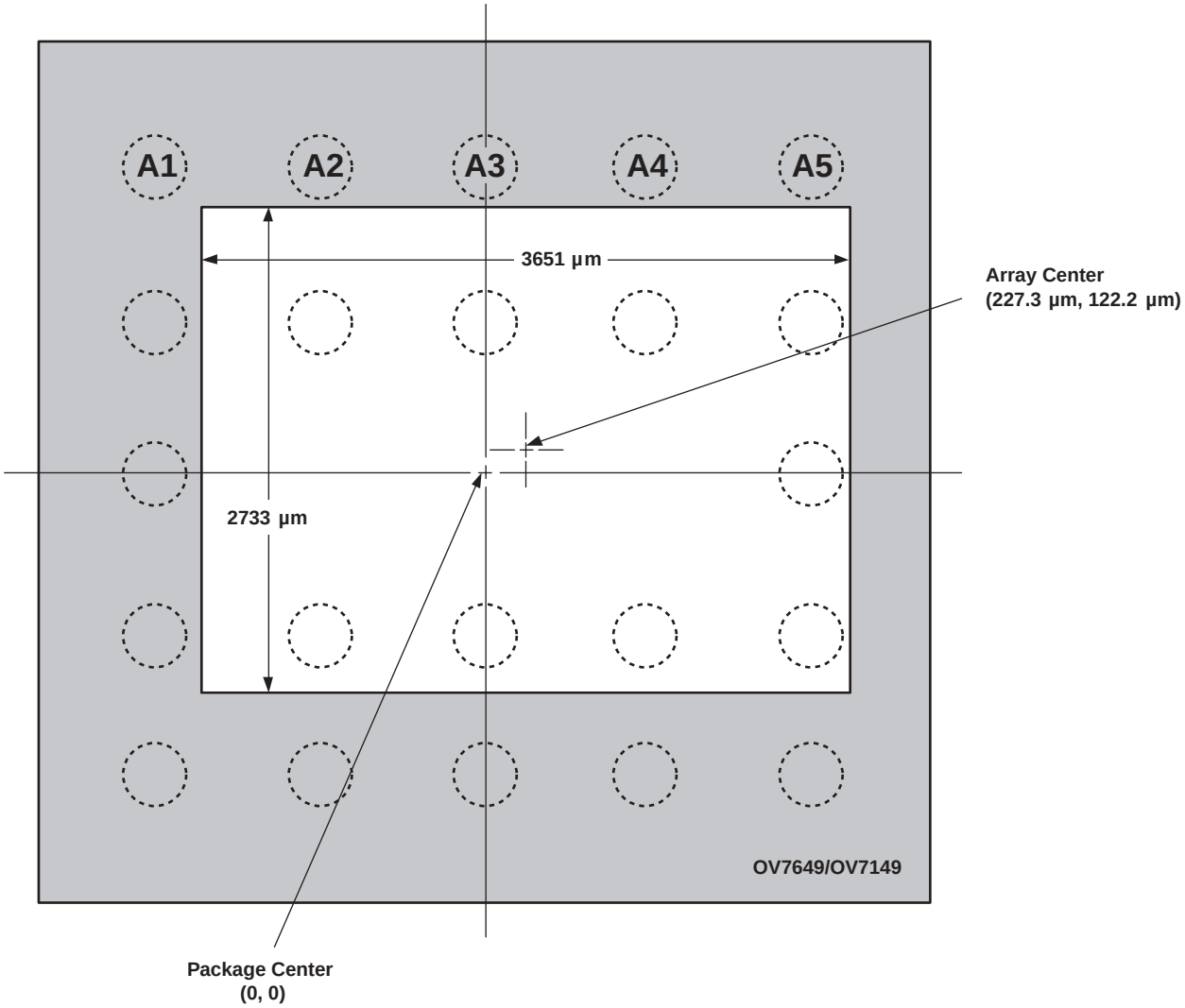


Table 6 OV7649/OV7149 Package Dimensions

Parameter	Symbol	Minimum	Nominal	Maximum	Unit
Package Body Dimension X	A	4905	4930	4955	µm
Package Body Dimension Y	B	4735	4760	4785	µm
Package Height	C	760	820	880	µm
Package Body Thickness	C2	605	640	675	µm
Ball Height	C1	150	180	210	µm
Ball Diameter	D	320	350	380	µm
Total Pin Count	N		22		
Pin Count X-axis	N1		5		µm
Pin Count Y-axis	N2		5		µm
Pins Pitch X-axis	J1		800		µm
Pins Pitch Y-axis	J2		800		µm
Edge-to-Pin Center Distance Analog X	S1	840	865	890	µm
Edge-to-Pin Center Distance Analog Y	S2	755	780	805	µm

Sensor Array Center

Figure 14 OV7649/OV7149 Sensor Array Center



Note: Due to the lens inversion, in order for the image to be right-side up, the OV7649/OV7149 must be mounted with pins A1 to A5 down.

The recommended lens chief ray angle for the OV7649 is 16 degrees.

IR Reflow Ramp Rate Requirements

OV7649/OV7149 Lead-Free Devices

Note: For OVT devices that contain lead, all part marking letters are upper case. For OVT devices that are lead-free, all part marking letters are lower case

Figure 15 IR Reflow Ramp Rate Requirements

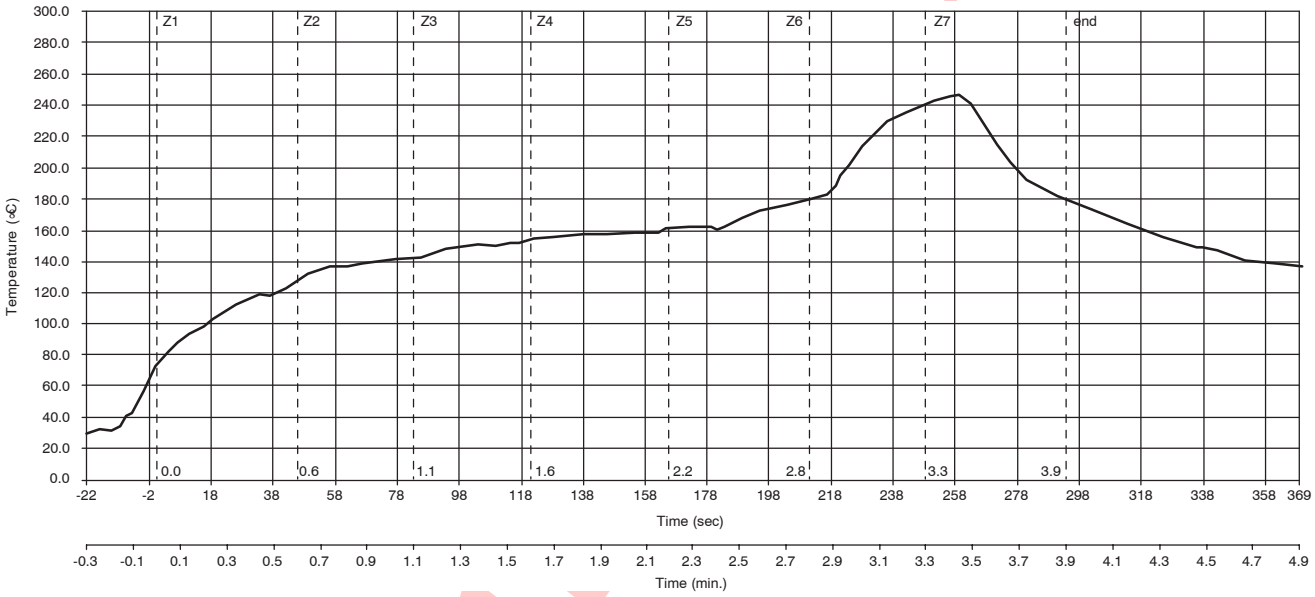


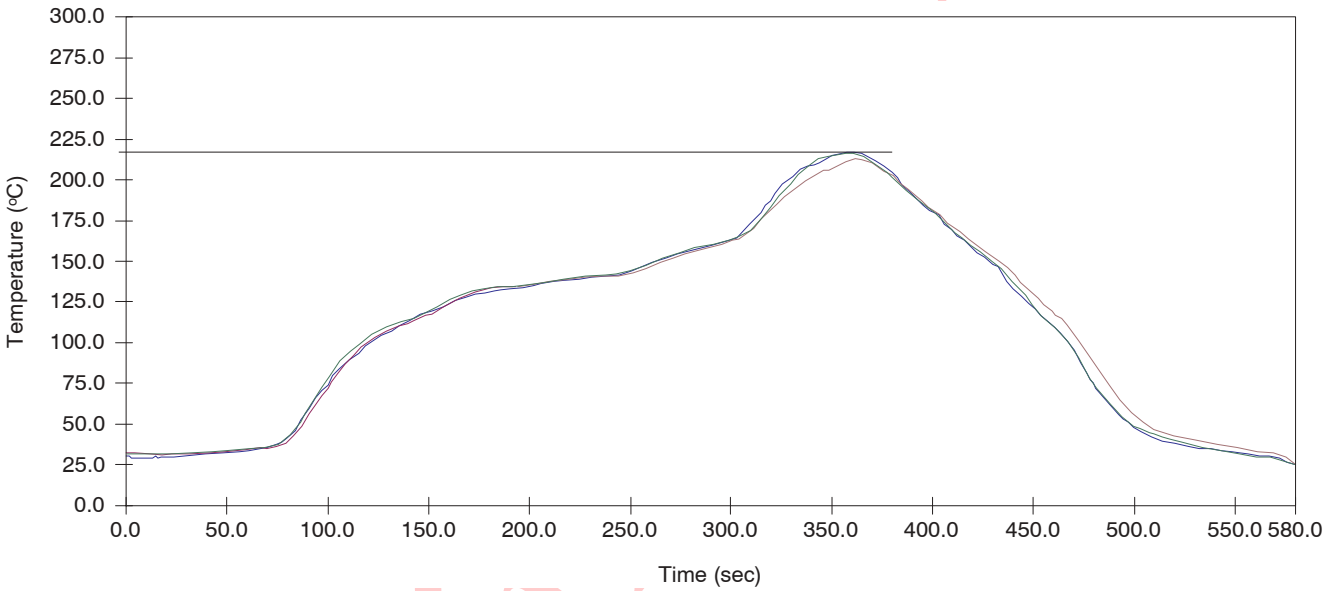
Table 7 Reflow Conditions

Condition	Exposure
Average Ramp-up Rate (30°C to 217°C)	Less than 3°C per second
> 100°C	Between 330 - 600 seconds
> 150°C	At least 210 seconds
> 217°C	At least 30 seconds (30 ~ 120 seconds)
Peak Temperature	245°C
Cool-down Rate (Peak to 50°C)	Less than 6°C per second
Time from 30°C to 255°C	No greater than 390 seconds

OV7649/OV7149 Devices Containing Lead

Note: For OVT devices that contain lead, all part marking letters are upper case. For OVT devices that are lead-free, all part marking letters are lower case

Figure 16 IR Reflow Ramp Rate Requirements



Peak Temperature (°C)	Peak Time (sec)	≥ 100°C Time (sec)	≥ 150°C Time (sec)	≥ 190°C Time (sec)
216.7	358.00	347.00	167.00	70.00

Environmental Specifications

Table 8 OV7649/OV7149 Reliability Test Results

Parameter	Test Condition
Temperature/Humidity	85°C/85% Relative Humidity, 1000 hrs.[a]
Temperature Cycling (Air-to-Air)	-25°C / +125°C, 72 cycles/day, 1000 cycles[a]
Highly Accelerated Stress Test (HAST)	110°C / 85% Relative Humidity, 168 hrs.[a]
High Temperature Storage (HTS)	150°C, 1000 hrs.[a]
High Temperature Static Bias (HTSB)	125°C, 1000 hrs.[a]

a. Pre-Condition (Moisture Level II): 125°C, 24h → 85°C/60% RH/168h → IR Reflow 235°C, 10 sec, 3 cycles

Note:

- *All information shown herein is current as of the revision and publication date. Please refer to the OmniVision web site (http://www.ovt.com) to obtain the current versions of all documentation.*

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