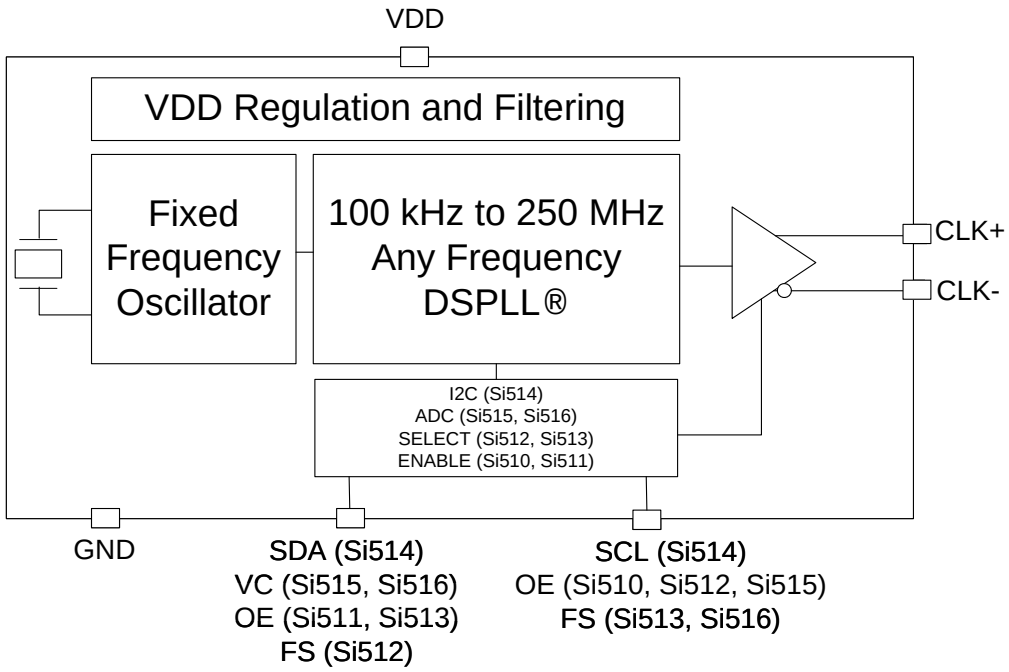
Termination Options for Any-Frequency Si51x XOs, VCXOs

1. Introduction

This application note provides termination recommendations for connecting output clock signals to the Si51x family of XO and VCXO ICs and is not applicable to any other Silicon Laboratories devices.

The Si51x family of Any-Frequency XOs, VCXOs greatly simplifies the task of interfacing between many of today's common signal types. The outputs are compatible with single-ended CMOS or differential signals (LVPECL, LVDS, HCSL) and support multiple voltage levels (3.3, 2.5, or 1.8 V). A block diagram of the devices is shown in Figure 1.

The Si510 and Si511 are single-frequency XOs with an output enable. The Si512 and Si513 are dual-frequency XOs with an output enable. The Si514 is a frequency programmable device using I^2C control. The Si515 and Si516 are VCXOs with either an output enable (Si515) or dual-frequency (Si516).



Notes: CLK- is no-connect for single-ended CMOS output format. See ordering information.
CMOS format is limited to 100 kHz to 212.5 MHz.

Figure 1. Block Diagram of Si51x Devices

2. Outputs

The Si51x devices can be ordered to provide an output that can be differential or single-ended (CMOS). When configured as differential CMOS, the driver generates two signals that can be configured as either in-phase or complementary. The output format is determined by the ordered part type and can be one of the following signal types: CMOS, LVPECL, LVDS, and HCSL (see your part's data sheet).

2.1. CMOS Outputs

The CMOS output driver has an output impedance of about 40 Ω. For this reason, an external Rs series resistor of 10 Ω provides the optimal termination for boards having 50 Ω traces as diagrammed in Figure 2 (single output), Figure 3 (dual output—in phase), and Figure 4 (dual output—complementary). If the board trace impedance is higher than 50 Ω, the value of Rs should be the sum of 10 Ω plus the difference between the board trace impedance and 50 Ω. Figure 5, Figure 6, and Figure 7 show scope waveforms with single, dual in-phase, and dual complementary CMOS outputs, respectively.

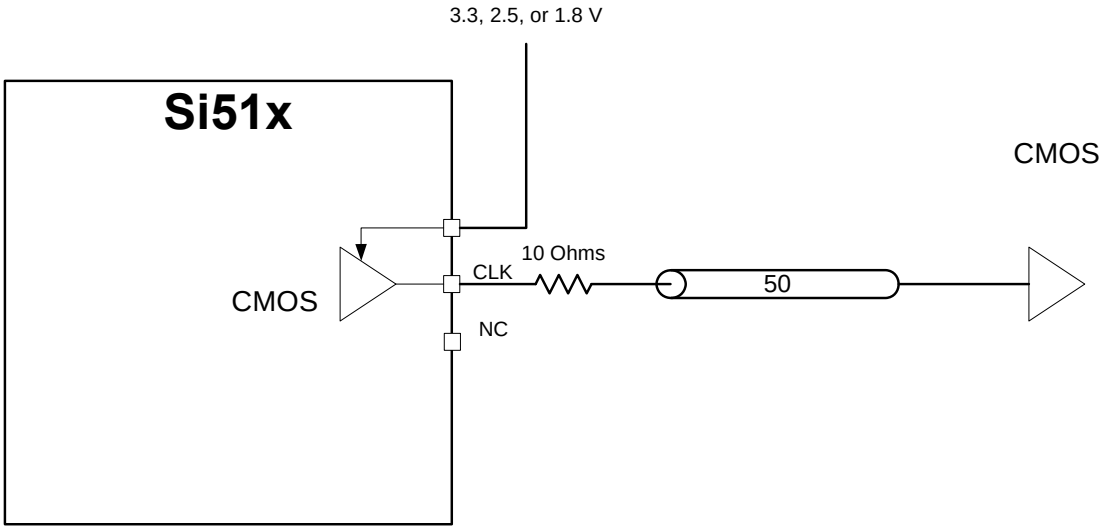


Figure 2. Interfacing to a CMOS Receiver—Single Output

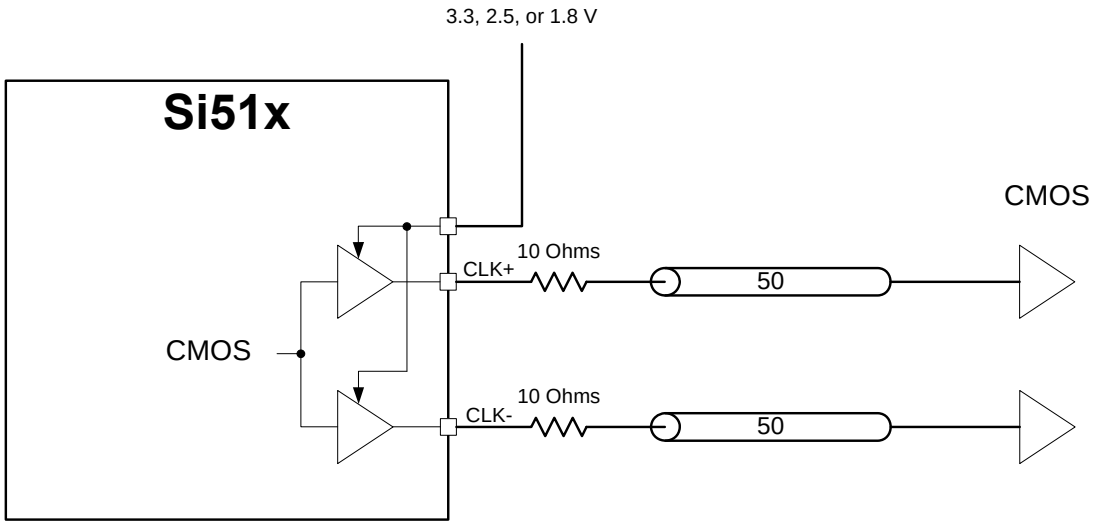


Figure 3. Interfacing to a CMOS Receiver—Dual Output In-Phase

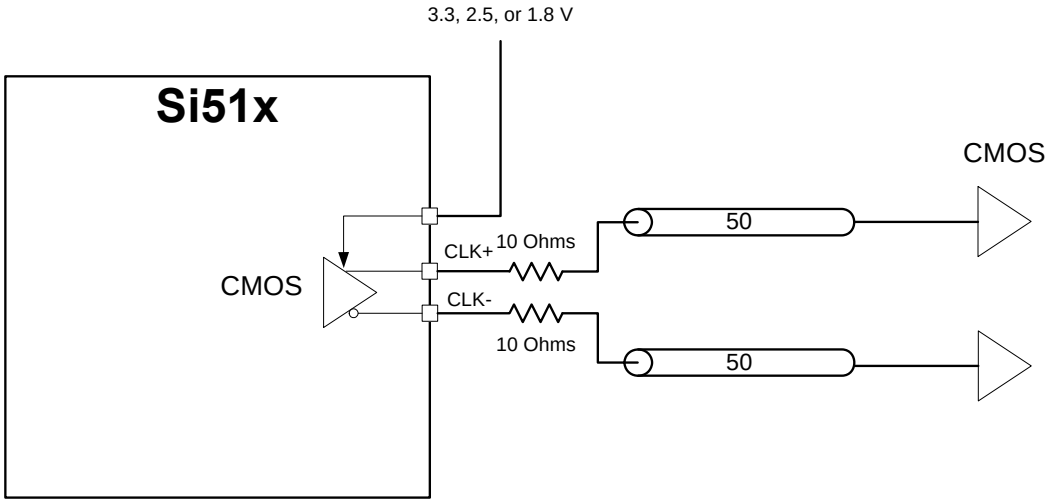


Figure 4. Interfacing to a CMOS Receiver—Dual Output Complementary

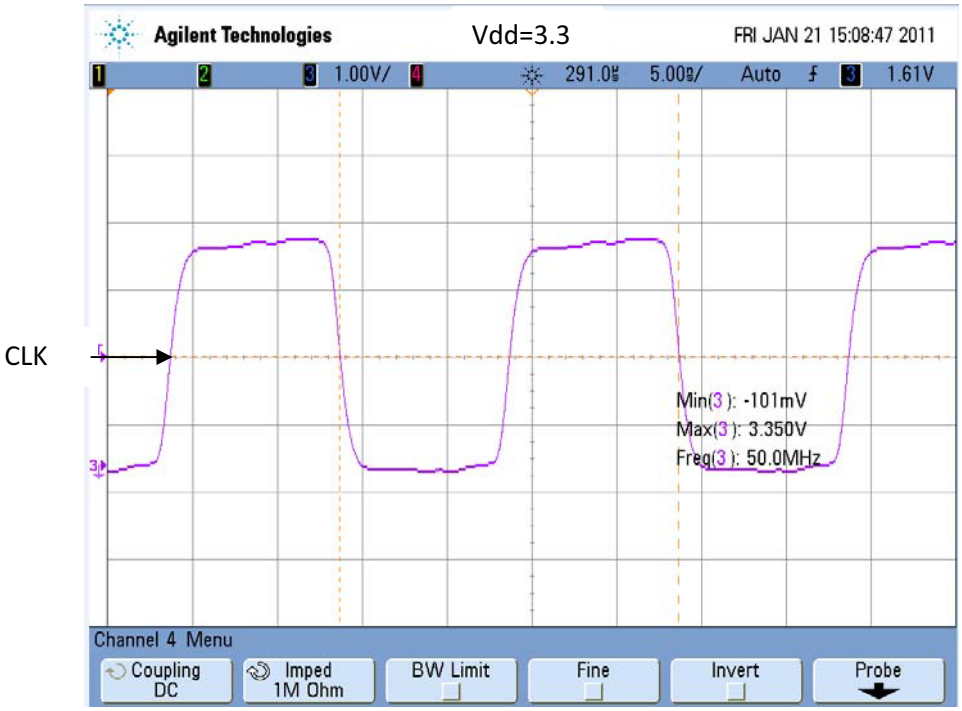


Figure 5. CMOS Output Series Terminated with 10 Ω—Single Output

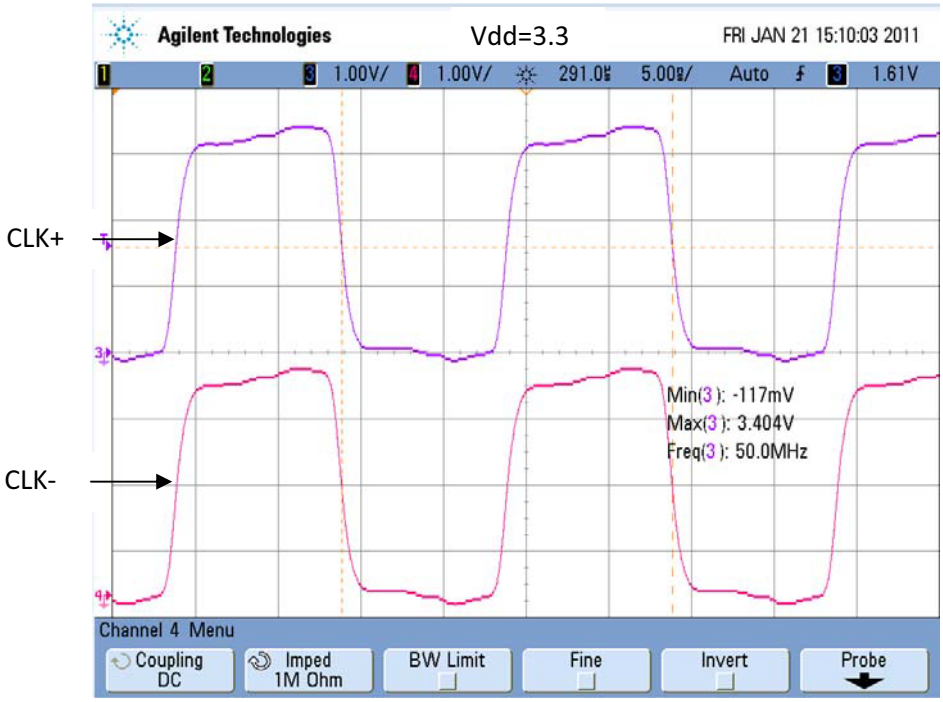


Figure 6. CMOS Outputs Series Terminated with 10 Ω—Dual Output In-phase

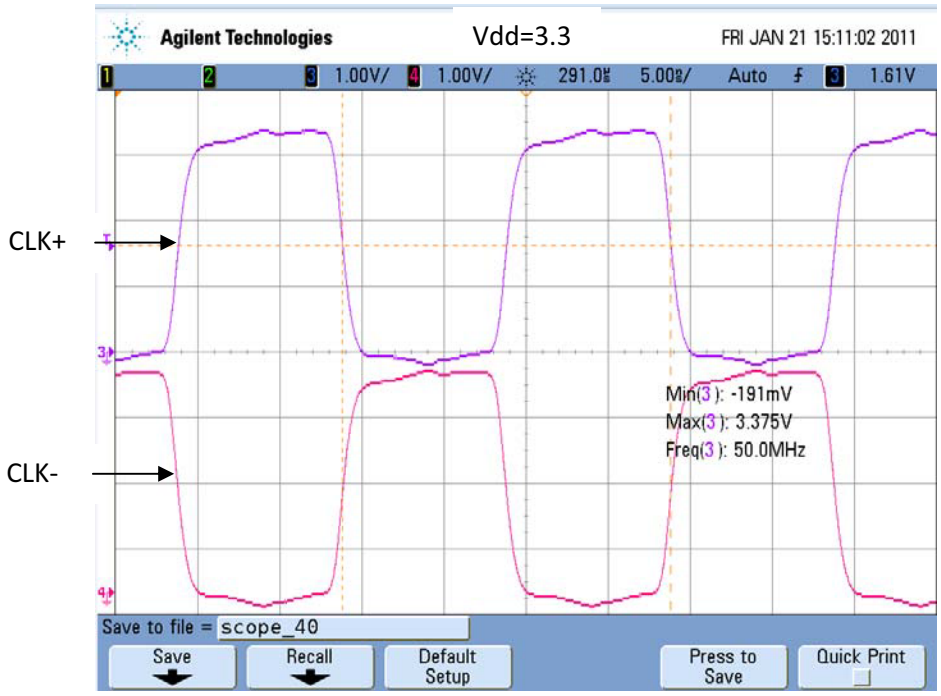


Figure 7. CMOS Outputs Series Terminated with 10 Ω—Dual Output Complementary

2.2. LVPECL Outputs

The LVPECL driver can be ordered as either 3.3 or 2.5 V standard LVPECL modes. The output driver can be ac-coupled or dc-coupled to the receiver.

2.2.1. DC-Coupled LVPECL Outputs

The standard LVPECL driver supports two commonly used dc-coupled configurations. Both of these are shown in Figure 8 and Figure 9. LVPECL drivers were designed to be terminated with 50 Ω to V_{DD}–2 V, which is illustrated in Figure 8. VTT can be supplied with a simple voltage divider as shown in Figure 8.

An alternative method of terminating LVPECL is shown in Figure 9, which is the Thevenin equivalent to the termination in Figure 8. It provides a 50 Ω load terminated to V_{DD}–2.0 V. For 3.3 V LVPECL, use R1 = 127 Ω and R2 = 82.5 Ω; for 2.5 V LVPECL, use R1 = 250 Ω and R2 = 62.5 Ω. The only disadvantage to this type of termination is that the Thevenin circuit consumes additional power from the V_{DD} supply. Figure 10 shows a scope waveform with 3.3 V LVPECL outputs dc-coupled 50 Ω to V_{DD}–2.0 V using a Thevenin equivalent termination.

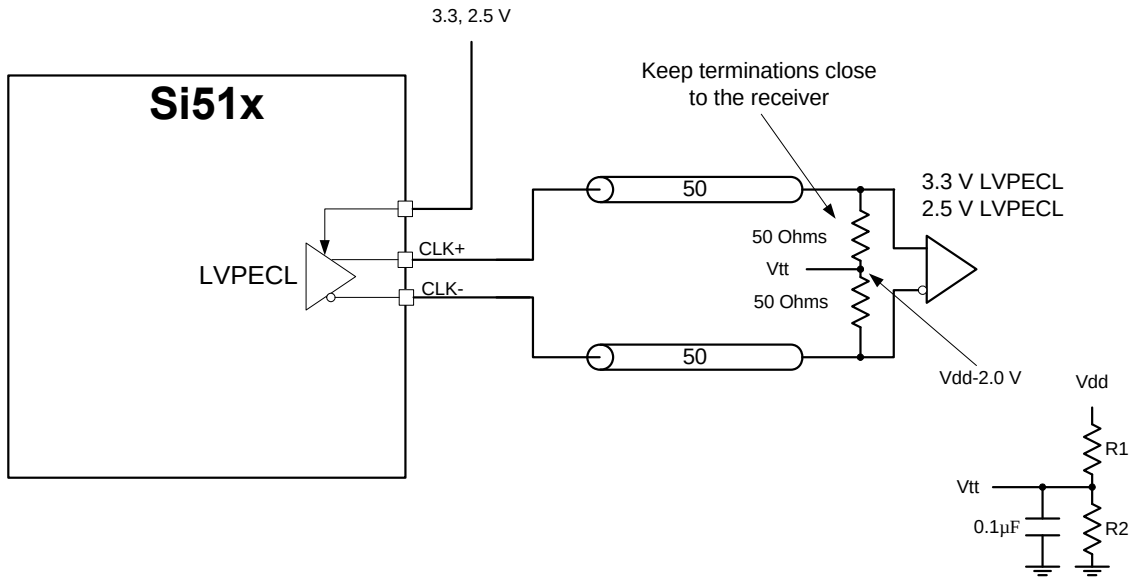


Figure 8. Interfacing to LVPECL—DC-Coupled with 50 Ω to V_{DD}–2.0 V

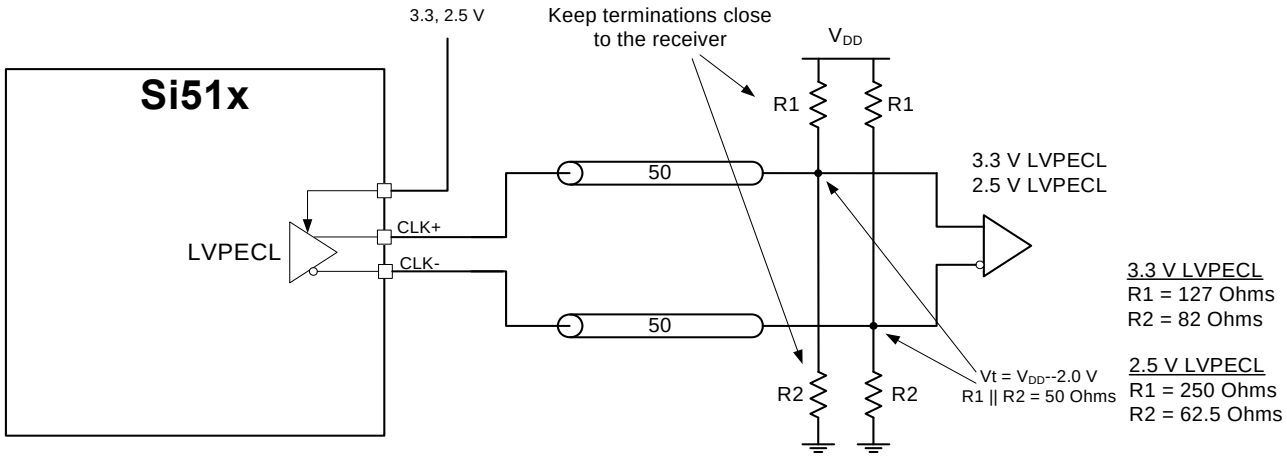


Figure 9. Interfacing to LVPECL—DC-Coupled with Thevenin Termination

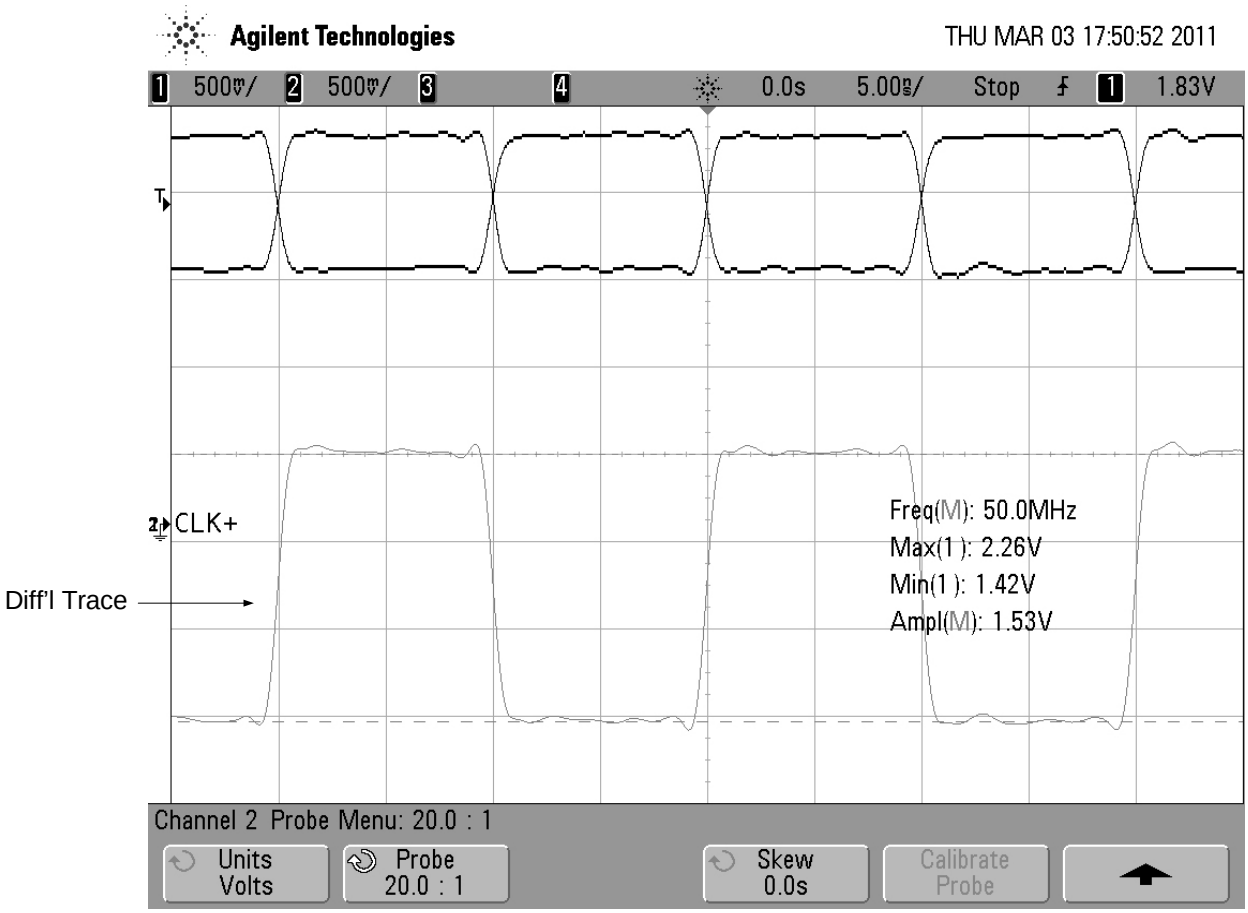


Figure 10. LVPECL Outputs DC-Coupled with Thevenin Equivalent Termination

2.2.2. AC-Coupled LVPECL Outputs

AC coupling is necessary when a receiver and a driver have compatible voltage swings but different common mode voltages. AC coupling works well for dc-balanced signals, such as for 50% duty cycle clocks. Figure 11 describes two methods for ac coupling the standard LVPECL driver. The Thevenin termination shown in Figure 11 is a convenient and common approach when a VBB (V_{DD}–1.3 V) supply is not available; however, it does consume additional power. The termination method shown in Figure 12 consumes less power. A VBB supply can be generated from a simple voltage divider circuit as shown in Figure 12. Figure 13 shows a scope waveform with 3.3 V LVPECL outputs ac-coupled 50 Ω to V_{DD}–1.3 V using a Thevenin equivalent termination.

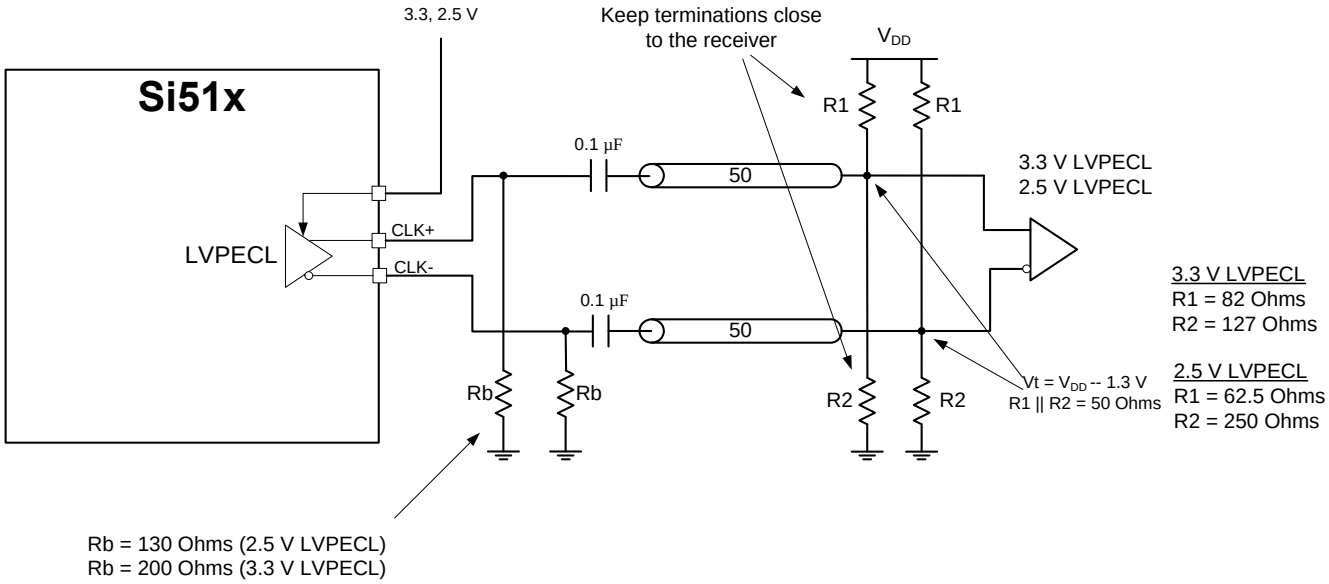


Figure 11. Interfacing to LVPECL—AC-Coupled with Thevenin Termination

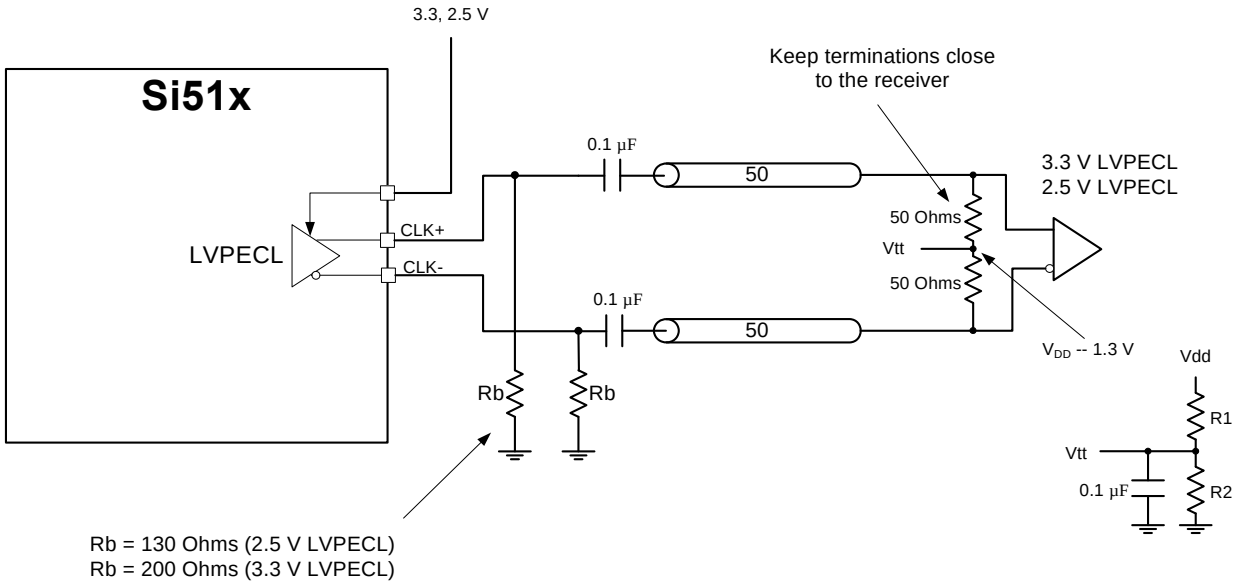


Figure 12. Interfacing to LVPECL—AC-Coupled with 100 Ω Termination

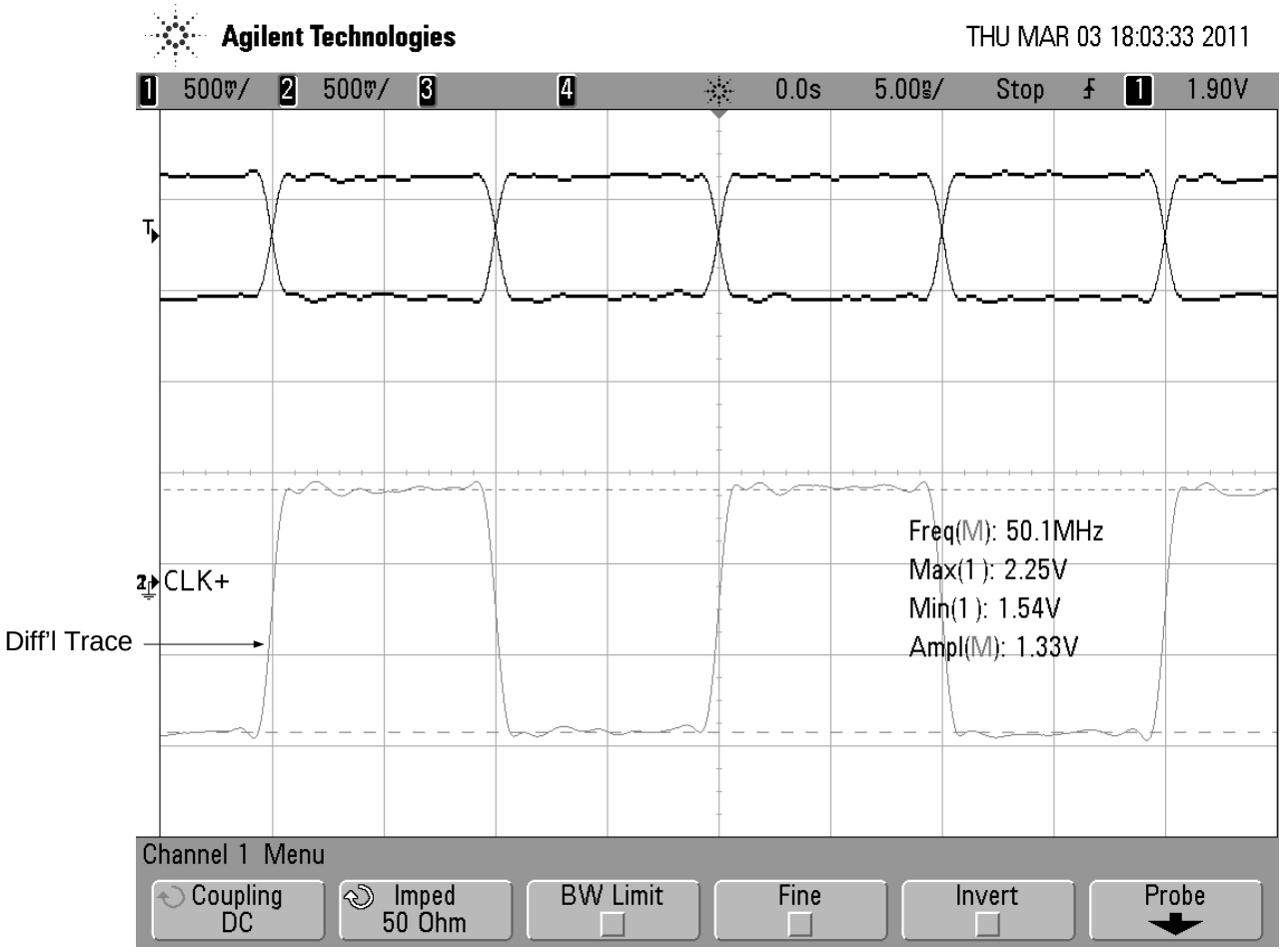


Figure 13. LVPECL Outputs AC-Coupled with Thevenin Equivalent Termination

2.3. LVDS Outputs

The LVDS output option provides a very simple and power-efficient interface that requires no external biasing when connected to an LVDS receiver. The LVDS driver may be dc-coupled or ac-coupled to the receiver.

2.3.1. DC-Coupled LVDS Outputs

When using a 3.3 or 2.5 V supply voltage, the Si51x provides standard LVDS output levels. Although the LVDS standard does not specify a 1.8 V supply voltage, the Si51x has been characterized using a 1.8 V supply (refer to the data sheet for guaranteed spec levels). Figure 14 displays the dc-coupled LVDS termination scheme and Figure 15 shows the scope waveforms with LVDS outputs dc-coupled.

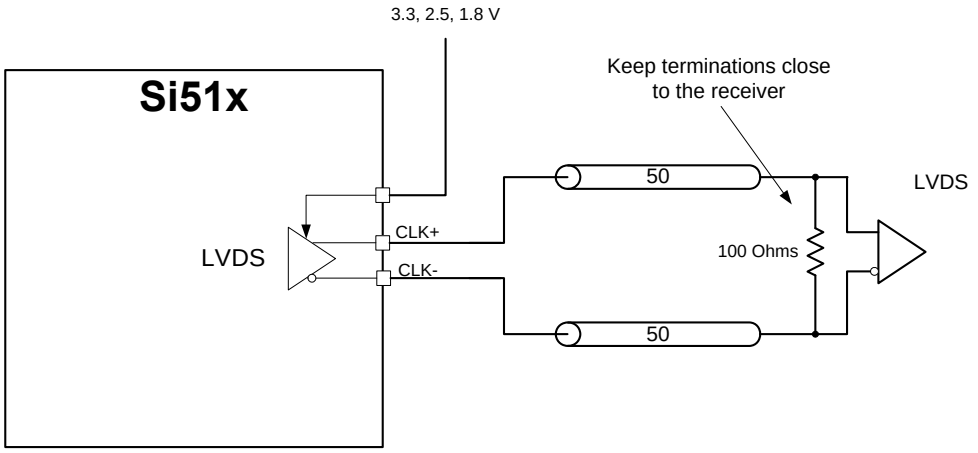


Figure 14. Interfacing to LVDS—DC-Coupled with 100 Ω Differential Termination

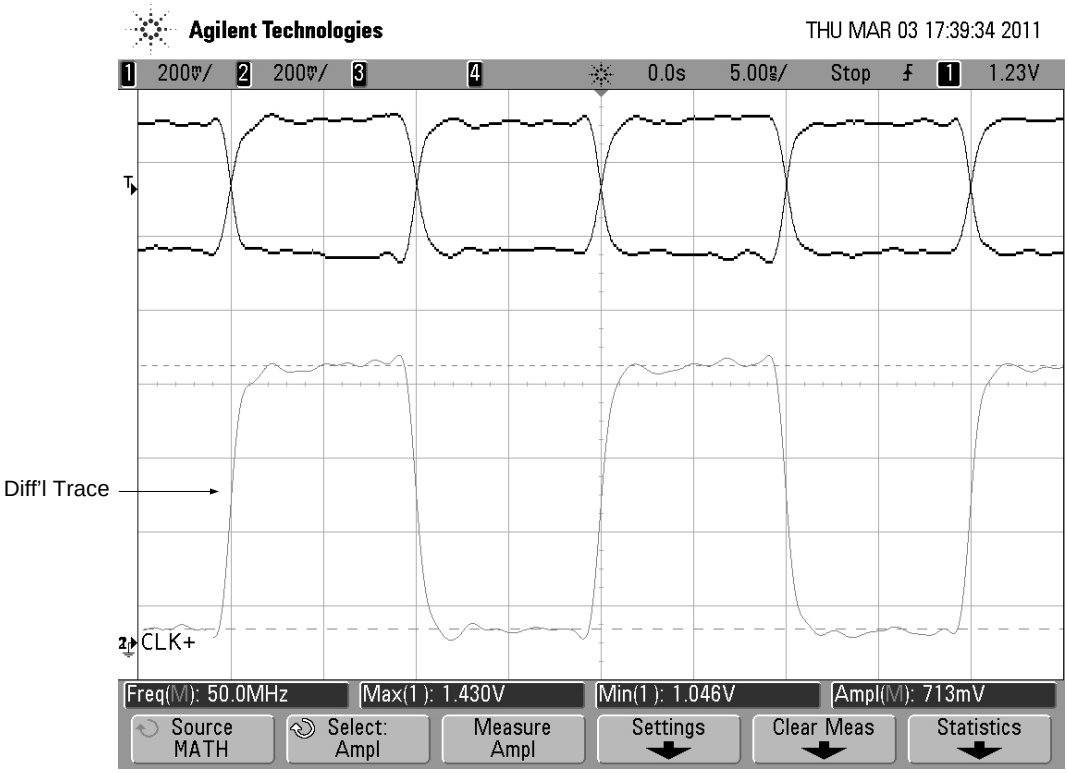


Figure 15. LVDS Outputs DC-Coupled

2.3.2. AC-Coupled LVDS Outputs

The Si51x LVDS output can drive an ac-coupled load. The ac-coupling capacitors may be placed at either the driver or receiver end, as long as they are placed prior to the 100 Ω termination resistor. Keep the 100 Ω termination resistor as close to the receiver as possible, as shown in Figure 16.

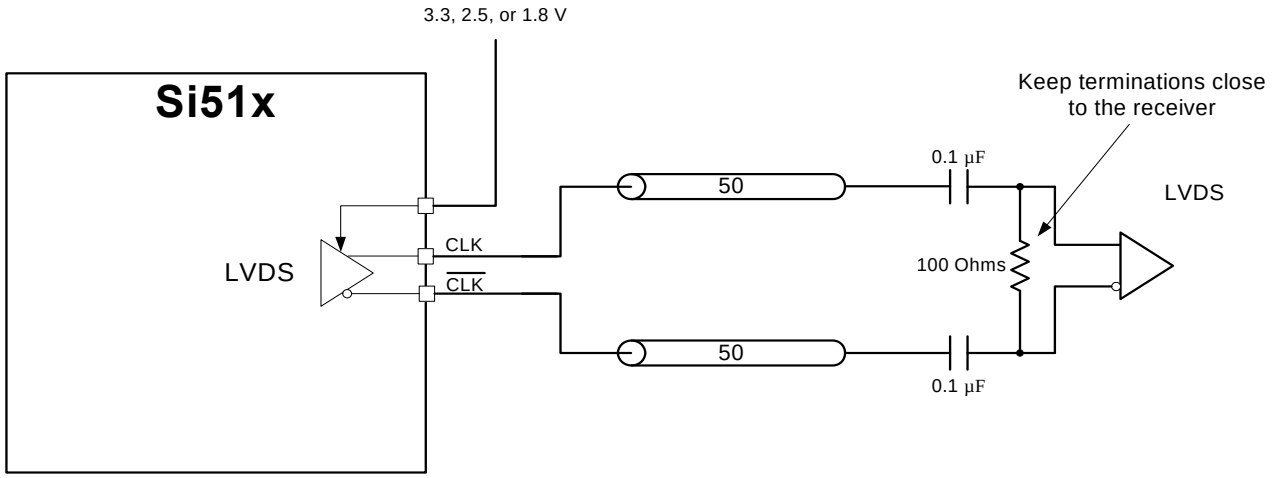


Figure 16. Interfacing to LVDS—AC-Coupled

2.4. HCSL Outputs

High Speed Current Steering Logic (HCSL) outputs are commonly used in PCI Express applications. There are three configurations that require different termination schemes. The first scheme applies to when the driver and load are on different boards and is referred to as the “Add-In Card” configuration. In order to provide proper termination with or without the Add-In Card plugged into the connector, series and parallel resistors are added near the driver as shown in Figure 17. Since the Add-In Card receiver presents a high-impedance load to the transmission line, the mismatch in impedance between the characteristic impedance of the line versus the load causes a reflection. The driver should be designed so that the reflection, or Ring Back, provides a minimum of ±100 mV margin from the differential midpoint of 0 V. Figure 18 displays the Si51x HCSL driver's output waveform (measured at the receiver's input) and shows the Ring Back voltage margin when driving a 12-inch transmission line using a 33 Ω series resistor.

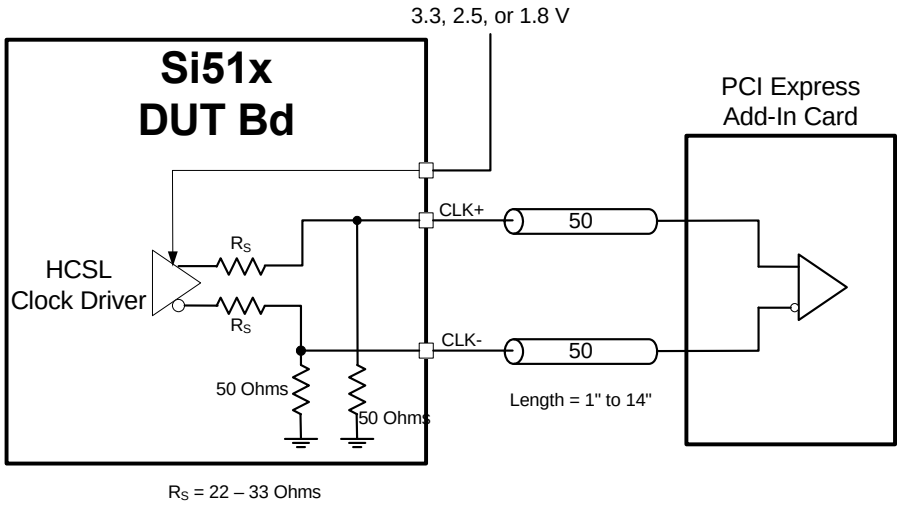


Figure 17. Interfacing the Si51x to an HCSL Receiver—“Add-In Card” Configuration with External Termination

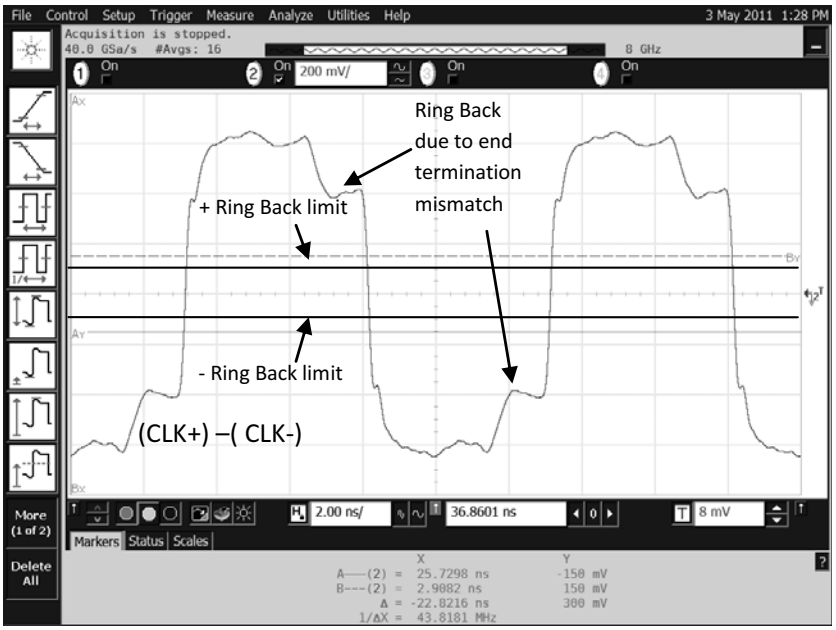


Figure 18. HCSL Outputs—“Add-In Card” Configuration with Rs = 33 Ω, L = 12 Inches

The second HCSL configuration is also an “Add-In Card” configuration without any external termination as shown in Figure 19. This configuration takes advantage of the driver’s internal termination to eliminate any external components. Without the external termination, the HCSL output has ~600 mV of single-ended amplitude or ~1.2 V differential amplitude between Ring Back reflections, well beyond the required ±100mV Ring Back limits. Figure 20 displays the Si51x HCSL driver’s output waveform (measured at the receiver’s input) and shows the Ring Bank voltage margin when driving a 12-inch transmission line using only internal termination.

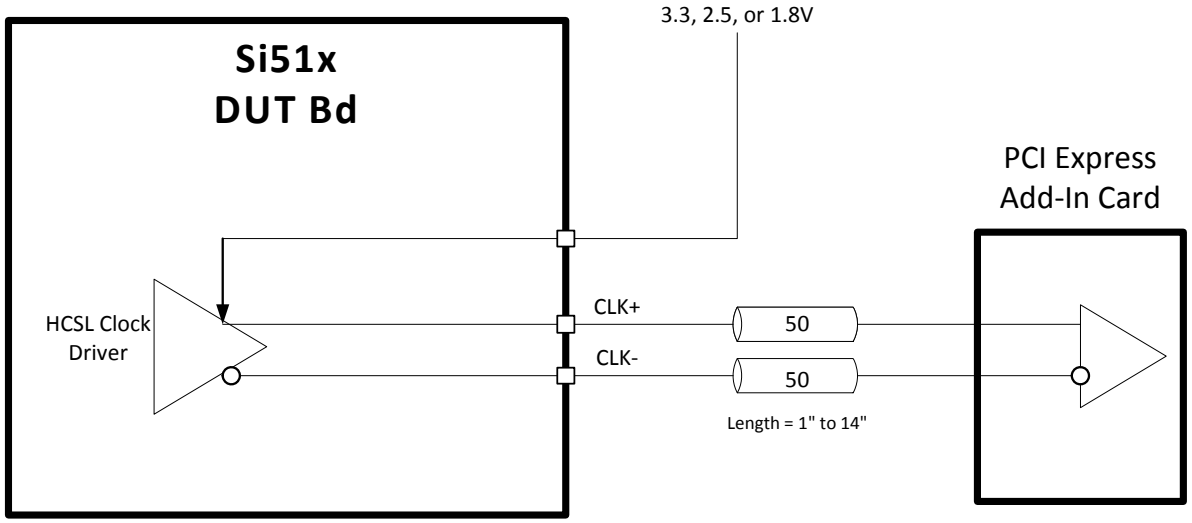


Figure 19. Interfacing the Si51x to an HCSL Receiver—“Add-In Card” Configuration with External Termination

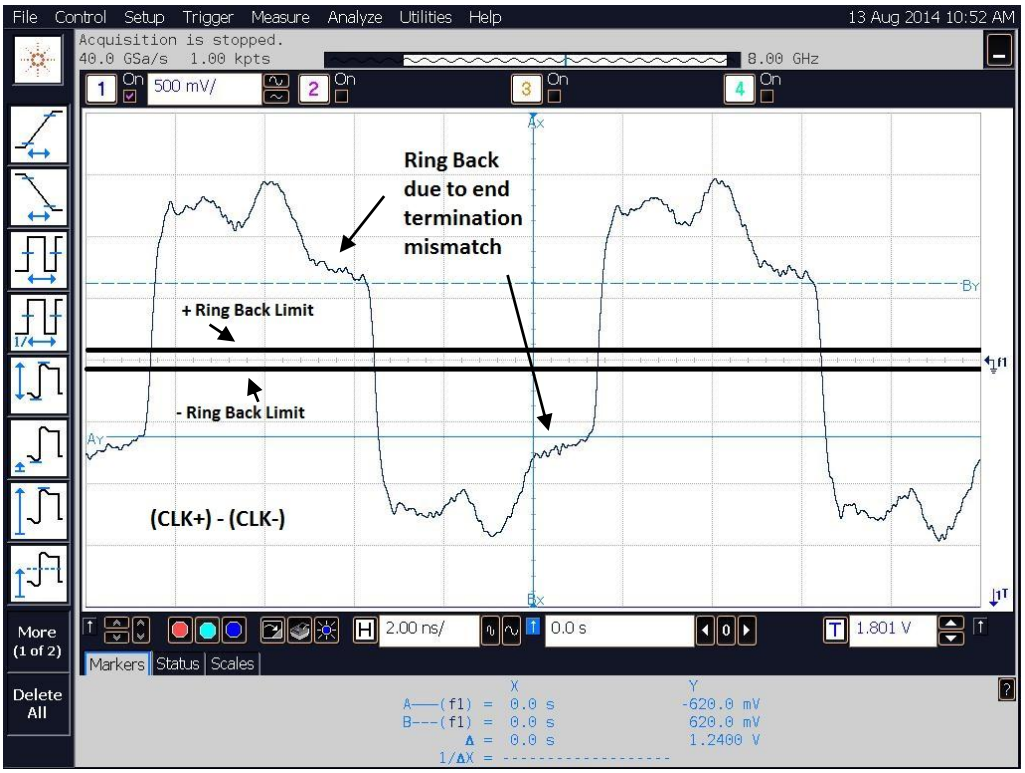


Figure 20. HCSL Outputs—“Add-In Card” Configuration with Internal Termination

The third HCSL configuration is when the clock driver and load reside on the same board and is referred to as the “Same Board” configuration. In this case, the transmission line should be terminated with 50 Ω ohms at the input to the clock receiver as shown in Figure 21. Figure 22 displays the HCSL driver's output waveform for this configuration (measured at the receiver').

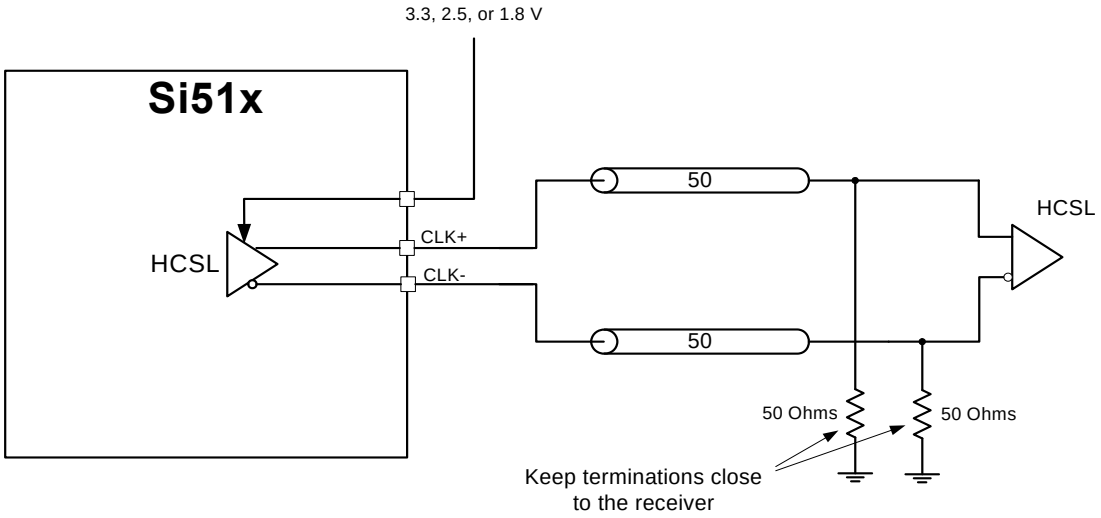


Figure 21. Interfacing the Si51x to an HCSL Receiver—“Same Board” Configuration

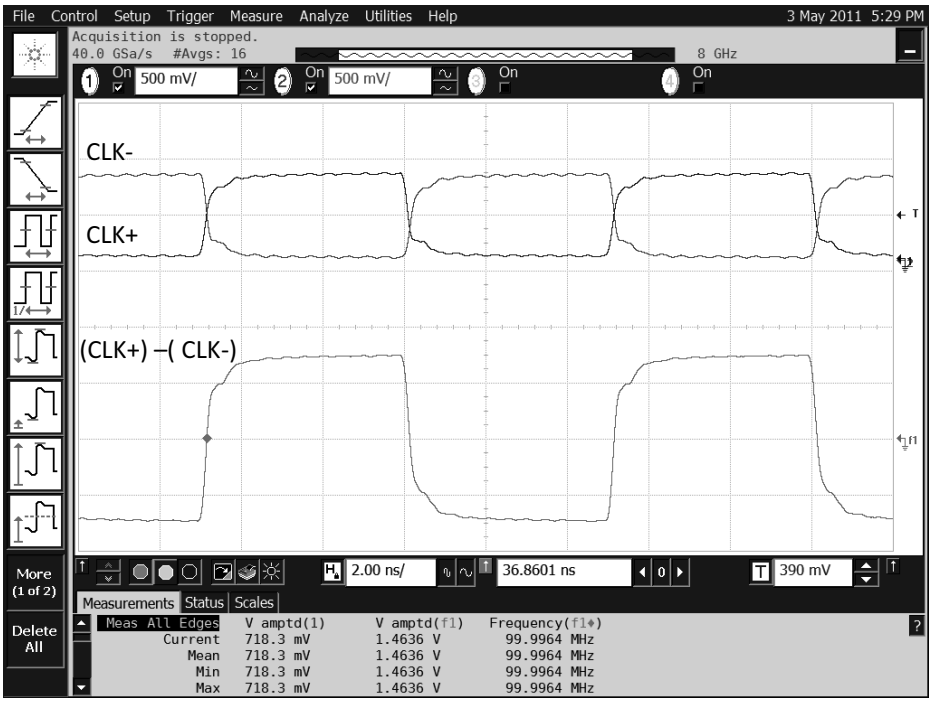


Figure 22. HCSL Outputs—“Same Board” Configuration

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