

RTD 2261W/2271W/2281W Family**Dual-Input Display Controller**

Spec

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1. Features

General

- Embedded 3 DDC with DDC1/2B/CI
- Zoom scaling up and down
- Embedded one MCU with SPI flash controller.
- It contains 4 ADCs in key pad application
- Require only one crystal to generate all timing.
- Programmable internal low-voltage-reset (LVR)
- High resolution 6 channels PWM output, and wide range selectable PWM frequency.
- Support input format up to FHD
- Embedded 1.2V LDO

Crystal

- 27MHz/24MHz/14.318MHz

Analog RGB Input Interface

- 1 Analog input supported
- Integrated 8-bit triple-channel 210MHz ADC/PLL
- Embedded programmable Schmitt trigger of HSYNC
- Support Sync-On-Green (SOG) and various kinds of composite sync modes
- On-chip high-performance hybrid PLLs
- High resolution true 64 phase ADC PLL
- YPbPr support up to HDTV 1080p resolution

DVI 1.0 Compliant Digital Input Interface with HDCP

- Single link on-chip TMDS receiver
- Long cable support to 1.65GHz
- Adaptive algorithm for TMDS capability
- Data enable only mode support
- High-Bandwidth Digital Content Protection (HDCP 1.1)
- Enhanced protection of HDCP secret key

Embedded MCU

- Industrial standard 8051 core with external serial flash
- Low speed ADC for various application
- I2C Master or Slave hardware supported

Auto Detection /Auto Calibration

- Input format detection
- Compatibility with standard VESA mode and support user-defined mode
- Smart engine for Phase/Image position/Color calibration

Scaling

- Fully programmable zoom ratios
- Independent horizontal/vertical scaling
- Advanced zoom algorithm provides high image quality
- Sharpness/Smooth filter enhancement
- Support non-linear scaling from 4:3 to 16:9 or 16:9 to 4:3

Color Processor

- True 10 bits color processing engine
- sRGB compliance
- Advanced dithering logic for 18-bit panel color depth enhancement
- Dynamic overshoot-smear canceling engine
- Brightness and contrast control
- Programmable 10-bit gamma support
- Peaking/Coring function for video sharpness

VividColor™

- Independent color management (ICM)
- Dynamic contrast control (DCC)
- Precise color management (PCM)
- Image adaptive power saving (IAPS)

Output Interface

- Fully programmable display timing generator
- Flexible data pair swapping for easier system design.
- Programmable TCON function support
- 1 and 2 pixel/clock panel support and up to FHD resolution. 135MHz for single LVDS. 210MHz for dual LVDS.
- LVDS -output interface
- Support 8-bit LVDS output
- Spread-Spectrum DPLL to reduce EMI
- Fixed Last Line output for perfect panel capability

Embedded OSD

- Embedded 16.5K SRAM dynamically stores OSD command and fonts
- Support multi-color RAM font, 1, 2 and 4-bit per pixel
- 64 color palette
- Maximum 18 window with alpha-blending/gradient / gradient target color / gradient reversed color/ dynamic fade-in/fade-out, bordering/ shadow/3D window type
- Rotary 90,180,270 degree
- Independent row shadowing/bordering
- Programmable blinking effects for each character
- OSD-made internal pattern generator for factory

mode

- Support 12x18~4x18 proportional font
- Hardware decompression for OSD font
- Support OSD scrolling
- Support 2 independent font based OSD

Power Supply

- 3.3V

2. Ordering Information

Part No.	VGA	DVI	HDCP	OD	FRC		Max. Resolution	Output	PKG
					FRC				
RTD2281W-GR	Yes (210MHz)	Yes	Yes	No	No	1920x1080	Dual-LVDS	QFP128 (green package)	
RTD2271W-GR	Yes (210MHz)	Yes	Yes	No	No	1680x1050	Dual-LVDS	QFP128 (green package)	
RTD2261W-GR	Yes (165MHz)	Yes	Yes	No	No	1440x900	Dual-LVDS	QFP128 (green package)	



3. Chip Data Path Block Diagram

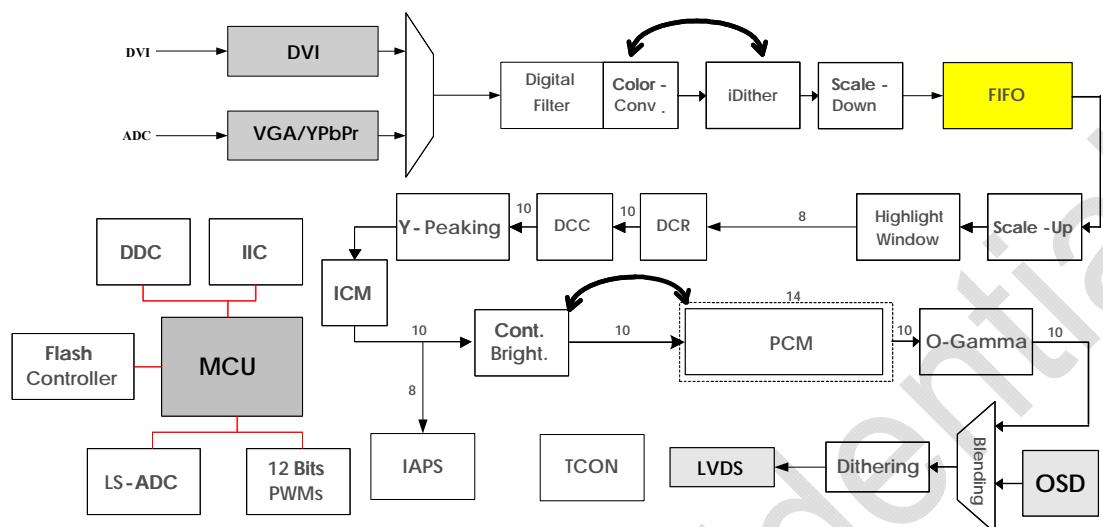
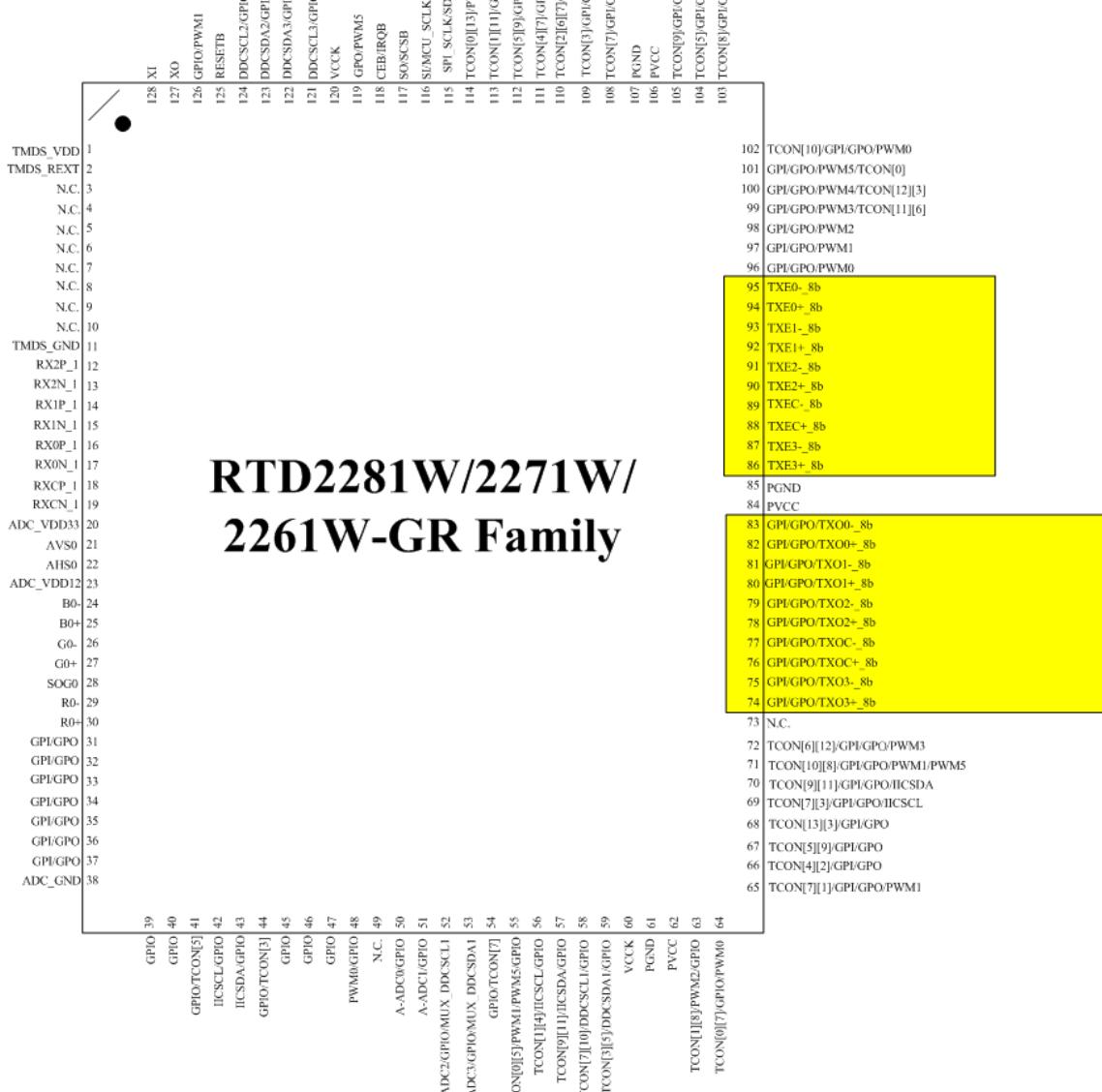


Figure1

4. Pin Diagram

128 Pin QFP



(Pin 119 : Power on latch Pin)

(when AC Power On , Power on latch pin must be “High”)



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Table of Pin Assignment

Name	Pin #	Description	Note
TMDS_VDD	1	TMDS power	(3.3 V)
TMDS_REXT	2	Impedance Match Reference Resistor For Scan mode,it should be pulled low Scan mode: SI[7:0] is assigned to {124~121,114~111} SO[7:0] is assigned to {110~108,105~101} SE is assigned to 100.	Ref value: 6.2 K ohm
N.C.	3	Not connected	
N.C.	4	Not connected	
N.C.	5	Not connected	
N.C.	6	Not connected	
N.C.	7	Not connected	
N.C.	8	Not connected	
N.C.	9	Not connected	
N.C.	10	Not connected	
TMDS_GND	11	TMDS ground	
RX2P_1	12	TMDS Differential signal Input	
RX2N_1	13	TMDS Differential signal Input	
RX1P_1	14	TMDS Differential signal Input	
RX1N_1	15	TMDS Differential signal Input	
RX0P_1	16	TMDS Differential signal Input	
RX0N_1	17	TMDS Differential signal Input	
RXCP_1	18	TMDS Differential signal Input	
RXCN_1	19	TMDS Differential signal Input	
ADC_VDD33	20	Embedded ADC 3.3V	(3.3 V)
AVS0	21	ADC vertical sync input	5V tolerance even when power-off
AHS0	22	ADC horizontal sync input AVS0 and AHS0 could be used to select one of three scan chain. AHS0/AVS0: 2'b00: {i_chain[2:0], mcu_chain[1:0], vbi_chain[2:0]} 2'b01: d_chain 2'b10: vdec_chain Other are reserved	5V tolerance even when power-off
ADC_VDD12	23	ADC 1.2V Power (supplied by embedded 1.2V regulator)	(1.2V)
B0-	24	Negative BLUE analog input (Pb-)	
B0+	25	Positive BLUE analog input (Pb+)	
G0-	26	Negative GREEN analog input (Y-)	
G0+	27	Positive GREEN analog input (Y+)	
SOG0	28	Sync-On-Green	
R0-	29	Negative RED analog input (Pr-)	
R0+	30	Positive RED analog input (Pr+)	
GPI/GPO	31	MCU GPIO	3.3 V tolerance
GPI/GPO	32	MCU GPIO	3.3 V tolerance
GPI/GPO	33	MCU GPIO	3.3 V tolerance
GPI/GPO	34	MCU GPIO	3.3 V tolerance



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GPI/GPO	35	MCU GPIO/GPO	3.3 V tolerance
GPI/GPO	36	MCU GPIO/GPO	3.3 V tolerance
GPI/GPO	37	MCU GPIO/GPO	3.3 V tolerance
ADC GND	38	ADC ground	
GPIO	39	MCU GPIO	5V tolerance even when power-off
GPIO	40	MCU GPIO	5V tolerance even when power-off
GPIO/ TCON[5]	41	MCU GPIO/TCON	5V tolerance even when power-off
GPIO/IIC SCL	42	MCU GPIO/IIC BUS	5V tolerance even when power-off
GPIO/IIC SDA	43	MCU GPIO/IIC BUS	5V tolerance even when power-off
GPIO/TCON[3]	44	MCU GPIO/TCON	5V tolerance even when power-off
GPIO	45	MCU GPIO	5V tolerance even when power-off
GPIO	46	MCU GPIO	5V tolerance even when power-off
GPIO	47	MCU GPIO	5V tolerance even when power-off
GPIO/PWM0	48	MCU GPIO/PWM	5V tolerance even when power-off
N.C.	49	Not Connected	
A-ADC0/GPIO	50	MCU ADC Input /MCU GPIO	3.3V tolerance even when power-off (GPIO open-drain)
A-ADC1/GPIO	51	6-bit MCU ADC Input/MCU GPIO	3.3V tolerance even when power-off (GPIO open-drain)
A-ADC2/GPIO /MUX_DDCSCL1	52	6-bit MCU ADC Input /MCU GPIO /MUX_DDCSCL1 when (Page 10 , 0xA2[0] = 1) && (pin55 = 1), disable ddc function of pin58, 59 and swap to pin52, 53.	3.3V tolerance even when power-off (GPIO open-drain)
A-ADC3/GPIO /MUX_DDCSDA1	53	6-bit MCU ADC Input/MCU GPIO /MUX_DDCSDA1 when (Page 10 , 0xA2[0] = 1) && (pin55 = 1), disable ddc function of pin58, 59 and swap to pin52, 53.	3.3V tolerance even when power-off (GPIO open-drain)
GPIO/ TCON[7]	54	MCU GPIO/TCON	5V tolerance



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			even when power-off (GPIO open-drain)
GPIO/PWM1/PWM5/TCON[5] [0]	55	MCU GPIO/PWM/TCON	5V tolerance even when power-off (GPIO open-drain)
GPIO/IIC SCL/TCON[4] [1]	56	MCU GPIO/IIC BUS/TCON	5V tolerance even when power-off (GPIO open-drain)
GPIO/IIC SDA/TCON[11] [9]	57	MCU GPIO/IIC BUS/TCON	5V tolerance even when power-off (GPIO open-drain)
DDCSCL1/GPIO/TCON[10] [7]	58	DDC1(Open drain I/O)/MCU GPIO/TCON	5V tolerance even when power-off (GPIO open-drain)
DDCSDA1/GPIO/TCON[5] [3]	59	DDC1(Open drain I/O)/MCU GPIO/TCON	5V tolerance even when power-off (GPIO open-drain)
VCCK	60	Digital Power (supplied by embedded 1.2V)	(1.2V)
PGND	61	Pad ground	
PVCC	62	Pad power	(3.3V)
GPIO/PWM2/TCON[8] [1]	63	MCU GPIO/PWM/TCON	5V tolerance even when power-off (GPIO open-drain)
TCON[7] [0]/GPIO/PWM0	64	TCON/MCU GPIO/PWM	5V tolerance even when power-off (GPIO open-drain)
GPI/GPO/TCON[7][1]/PWM1	65	MCU GPIO/ TCON/PWM	5V tolerance
TCON[4][2]/GPI/GPO	66	TCON/MCU GPIO	5V tolerance
TCON[5][9]/GPI/GPO	67	TCON/MCU GPIO	5V tolerance
TCON[13][3]/GPI/GPO	68	TCON/MCU GPIO	5V tolerance
TCON[7][3]/GPI/GPO/IIC SCL	69	TCON/MCU GPIO/IIC BUS	5V tolerance
TCON[9][11]/GPI/GPO/IIC SDA	70	TCON/MCU GPIO/IIC bus	5V tolerance
TCON[10][8]/GPI/GPO/PWM1/PWM5	71	TCON/MCU GPIO/PWM	5V tolerance
GPI/GPO/PWM3/TCON[12][6]	72	MCU GPIO/PWM/TCON	5V tolerance
N.C.	73	Not connected	
TXO3+_8b/GPI/GPO	74	LVDS 8bit/MCU GPIO	3.3 V tolerance
TXO3-_8b /GPI/GPO	75	LVDS 8bit/MCU GPIO	3.3 V tolerance



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TXOC+_8b/GPI/GPO	76	LVDS 8bit/MCU GPIO	3.3 V tolerance
TXOC-_8b/GPI/GPO	77	LVDS 8bit/MCU GPIO	3.3 V tolerance
TXO2+_8b/GPI/GPO	78	LVDS 8bit/MCU GPIO	3.3 V tolerance
TXO2-_8b/GPI/GPO	79	LVDS 8bit/MCU GPIO	3.3 V tolerance
TXO1+_8b/GPI/GPO	80	LVDS 8bit/MCU GPIO	3.3 V tolerance
TXO1-_8b/GPI/GPO	81	LVDS 8bit/MCU GPIO	3.3 V tolerance
TXO0+_8b/GPI/GPO	82	LVDS 8bit/MCU GPIO	3.3 V tolerance
TXO0-_8b/GPI/GPO	83	LVDS 8bit/MCU GPIO	3.3 V tolerance
PVCC	84	Pad power	3.3V
PGND	85	Pad ground	
TXE3+_8b	86	LVDS 8bit	3.3 V tolerance
TXE3-_8b	87	LVDS 8bit	3.3 V tolerance
TXEC+_8b	88	LVDS 8bit	3.3 V tolerance
TXEC-_8b	89	LVDS 8bit	3.3 V tolerance
TXE2+_8b	90	LVDS 8bit	3.3 V tolerance
TXE2-_8b	91	LVDS 8bit	3.3 V tolerance
TXE1+_8b	92	LVDS 8bit	3.3 V tolerance
TXE1-_8b	93	LVDS 8bit	3.3 V tolerance
TXE0+_8b	94	LVDS 8bit	3.3 V tolerance
TXE0-_8b	95	LVDS 8bit	3.3 V tolerance
GPI/GPO/PWM0	96	MCU GPIO/PWM	5V tolerance
GPI/GPO/PWM1	97	MCU GPIO/PWM	5V tolerance
GPI/GPO/PWM2	98	MCU GPIO/PWM	5V tolerance
GPI/GPO/PWM3/TCON[11][6]	99	MCU GPIO/PWM/TCON	5V tolerance
GPI/GPO/PWM4/TCON[12][3]	100	MCU GPIO/PWM/TCON	5V tolerance
GPI/GPO/PWM5/TCON[0]	101	MCU GPIO/PWM/TCON	5V tolerance
TCON[10]/GPI/GPO/PWM0	102	TCON/MCU GPIO/ PWM	5V tolerance
TCON[8]/GPI/GPO/IICS CL/PWM1	103	TCON[8]/MCU GPIO/IICSL/PWM1	5V tolerance
TCON[5]/GPI/GPO /IRQB/IICSDA/PWM2	104	TCON[5]/MCU GPIO/IRQ Bar/IICSDA/PWM2	5V tolerance
TCON[9]/GPI/GPO	105	TCON/MCU GPIO	5V tolerance
PVCC	106	Pad 3.3V power	(3.3V)
PGND	107	Pad 3.3V GND	



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TCON[7]/GPI/GPO	108	TCON/MCU GPIO	5V tolerance
TCON[3]/GPI/GPO	109	TCON/MCU GPIO	5V tolerance
TCON[7][6][2]/GPIO	110	TCON/MCU GPIO	5V tolerance even when power-off (GPIO open-drain)
TCON[7][4]/GPIO	111	TCON/MCU GPIO	5V tolerance even when power-off (GPIO open-drain)
TCON[9][5]/GPIO	112	TCON/MCU GPIO	5V tolerance even when power-off (GPIO open-drain)
TCON[11][1]/GPIO	113	TCON/MCU GPIO	5V tolerance even when power-off (GPIO open-drain)
TCON[13][0]/GPIO/PWM4	114	TCON/MCU GPIO/PWM	5V tolerance even when power-off (GPIO open-drain)
SPI_SCLK/SDIO	115	SPI flash serial data input/external MCU serial control I/F data in	5V tolerance even when power-off (GPIO open-drain)
SI/MCU_SCLK	116	SPI flash serial clock/external MCU serial control I/F clock	5V tolerance even when power-off (GPIO open-drain)
SO/SCSB	117	SPI flash serial data output /external MCU serial control I/F chip select	5V tolerance even when power-off (GPIO open-drain)
CEB/IRQB	118	SPI flash chip enable bar/IRQ Bar Note:It should be pulled down to 0 v or pulled up to 3.3 v in order to designate the MCU type(Internal MCU(3.3 volts) or External MCU(0 volts)).	5V tolerance even when power-off (GPIO open-drain)
GPO/PWM5	119	MCU GPO/PWM (Power on latch Pin.) (when AC Power On , Power on latch Pin must be "High")	5V tolerance even when power-off
VCCK	120	Digital 1.2V Power (supplied by embedded 1.2V)	(1.2V)
DDCSCL3/GPIO	121	DDC3(Open drain I/O)/MCU GPIO	5V tolerance



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			even when power-off (GPIO open-drain)
DDCSDA3/GPIO	122	DDC3(Open drain I/O)/MCU GPIO	5V tolerance even when power-off (GPIO open-drain)
DDCSDA2/GPIO	123	DDC2(Open drain I/O)/MCU GPIO	5V tolerance even when power-off (GPIO open-drain)
DDCSCL2/GPIO	124	DDC2(Open drain I/O)/MCU GPIO	5V tolerance even when power-off (GPIO open-drain)
RESETB	125	Chip Reset Bar	Low active; 5V tolerance even when power-off (GPIO open-drain)
GPIO/PWM1	126	MCU GPIO/PWM	Pull up 27k ohm resistance to 3.3V power; 5V tolerance (GPIO open-drain)
XO	127	Crystal Output	
XI	128	Crystal Input	

Note: Pin65~pin102 cannot work in power saving/power down mode.



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MCU GPIO Assignment

PIN No.	MCU GPIO Name	PIN No.	MCU GPIO Name	PIN No.	MCU GPIO Name
31	PD.7	70	P1.6	122	P7.2
32	PD.6	71	P1.7	123	P7.1
33	PD.5	72	PC.2	124	P7.0
34	PD.4	74	P9.0	126	PC.0
35	PD.3	75	P9.1		
36	PD.2	76	P9.2		
37	PD.1	77	P9.3		
39	PD.0	78	P9.4		
40	PC.4	79	PA.0		
41	PB.7	80	PA.1		
42	PB.6	81	PA.2		
43	PB.5	82	PA.3		
44	PB4	83	PA.4		
45	PB.3	94	P5.0 (removed)		
46	PB.2	95	P5.1 (removed)		
47	PB.1	96	P5.2		
48	PB.0	97	P5.3		
50	P6.0	98	P5.4		
51	P6.1	99	P5.5		
52	P6.2	100	P5.6		
53	P6.3	101	P5.7		
54	P6.4	102	P7.6		
55	P6.5	103	P7.5		
56	P6.6	104	P7.4		
57	P6.7	105	P8.0		
58	P3.0/RXD(I/O)	108	P8.1/CLK01(O)		
59	P3.1/TXD(O)	109	P3.2/INT0(I)		
63	PC.3 /INT0(I)	110	P3.3/INT1(I)		
64	P1.0/T2(I) /INT1(I)	111	P3.4/T0		
65	P1.1/T2EX(I)	112	P3.5(BS)/T1		
66	P1.2/CLK02(O)	113	P3.6		
67	P1.3	114	P3.7		
68	P1.4	119	PC.1		



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P1.5

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P7.3

GPIO Pin List	Name	GPI	GPO <push-pull>	GPO <Open-Drain>	GPIO	3.3V Tolerance	5V Tolerance	5V Tolerance (When Power Off)	Pin Share Register	MCU Control
31	PD.7	Y	Y	Y		Y			Page10 , 0xB7	0xFF77
32	PD.6	Y	Y	Y		Y			Page10 , 0xB7	0xFF78
33	PD.5	Y	Y	Y		Y			Page10 , 0xB7	0xFF79
34	PD.4	Y	Y	Y		Y			Page10 , 0xB7	0xFF7A
35	PD.3	Y	Y	Y		Y			Page10 , 0xB8	0xFF7B
36	PD.2	Y	Y	Y		Y			Page10 , 0xB8	0xFF7C
37	PD.1	Y	Y	Y		Y			Page10 , 0xB8	0xFF7D
39	PD.0	Y	Y	Y	Y			Y	Page10 , 0xB8	0xFF7E
40	PC.4	Y	Y	Y	Y			Y	Page10 , 0xB9	0xFFA4
41	PB.7	Y	Y	Y	Y			Y	Page10 , 0xA0	0xFF7F
42	PB.6	Y	Y	Y	Y			Y	Page10 , 0xA0	0xFF89
43	PB.5	Y	Y	Y	Y			Y	Page10 , 0xA0	0xFF8A
44	PB4	Y	Y	Y	Y			Y	Page10 , 0xA8	0xFF8B
45	PB.3	Y	Y	Y	Y			Y	Page10 , 0xA1	0xFF8C
46	PB.2	Y	Y	Y	Y			Y	Page10 , 0xA3	0xFF8D
47	PB.1	Y	Y	Y	Y			Y	Page10 , 0xA6	0xFF8E
48	PB.0	Y	Y	Y	Y			Y	Page10 , 0xA7	0xFF8F
50	P6.0	Y	Y	Y	Y			Y	Page10 , 0xAB	0xFFC7
51	P6.1	Y	Y	Y	Y			Y	Page10 , 0xA3	0xFFC8
52	P6.2	Y	Y	Y	Y			Y	Page10 , 0xA4	0xFFC9
53	P6.3	Y	Y	Y	Y			Y	Page10 , 0xA5	0xFFCA
54	P6.4	Y	Y	Y	Y			Y	Page10 , 0xA0	0xFFCB
55	P6.5	Y	Y	Y	Y			Y	Page10 , 0xA6	0xFFCC
56	P6.6	Y	Y	Y	Y			Y	Page10 , 0xAF	0xFFCD
57	P6.7	Y	Y	Y	Y			Y	Page10 , 0xAF	0xFFCE
58	P3.0	Y	Y	Y	Y			Y	Page10 , 0xA2	SFR Access
59	P3.1	Y	Y	Y	Y			Y	Page10 , 0xA2	SFR Access
63	PC.3	Y	Y	Y	Y			Y	Page10 , 0xA6	0xFFA0
64	P1.0	Y	Y	Y	Y			Y	Page10 , 0xA3	SFR Access
65	P1.1	Y	Y				Y		Page10 , 0xB1	SFR Access
66	P1.2	Y	Y	Y	Y		Y		Page10 , 0xA4	SFR Access
67	P1.3	Y	Y	Y	Y		Y		Page10 , 0xA4	SFR Access
68	P1.4	Y	Y	Y	Y		Y		Page10 , 0xA7	SFR Access
69	P1.5	Y	Y	Y	Y		Y		Page10 , 0xA5	SFR Access
70	P1.6	Y	Y	Y	Y		Y		Page10 , 0xA5	SFR Access
71	P1.7	Y	Y				Y		Page10 , 0xA7	SFR Access
72	PC.2	Y	Y				Y		Page10 , 0xB2	0xFFA1
74	P9.0	Y	Y	Y		Y			Page10 , 0xA9	0xFFD8
75	P9.1	Y	Y	Y		Y			Page10 , 0xA9	0xFFD9
76	P9.2	Y	Y	Y		Y			Page10 , 0xA9	0xFFDA
77	P9.3	Y	Y	Y		Y			Page10 , 0xA9	0xFFDB
78	P9.4	Y	Y	Y		Y			Page10 , 0xA9	0xFFDC
79	PA.0	Y	Y	Y		Y			Page10 , 0xA9	0xFFDD
80	PA.1	Y	Y	Y		Y			Page10 , 0xA9	0xFFDE
81	PA.2	Y	Y	Y		Y			Page10 , 0xA9	0xFFDF
82	PA.3	Y	Y	Y		Y			Page10 , 0xA9	0FFE0
83	PA.4	Y	Y	Y		Y			Page10 , 0xA9	0FFE1

Note: Pin 74~Pin 83 (GPI,GPO,GPIO) can not work when power saving & power Down.
 Please don't use Pin 74~Pin 83 for power status detect function.
(Power Saving CR[01] Bit1 Enable, Power Down CR[01] Bit2 Enable)



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GPIO Pin List	Name	GPI	GPO <push-pull>	GPO <Open-Drain>	GPIO	3.3V Tolerance	5V Tolerance	5V Tolerance (When Power Off)	Pin Share Register	MCU Control
96	P5.2	Y	Y				Y		Page10 , 0xA8	0xFFC1
97	P5.3	Y	Y	Y	Y		Y		Page10 , 0xA8	0xFFC2
98	P5.4	Y	Y	Y	Y		Y		Page10 , 0xAA	0xFFC3
99	P5.5	Y	Y	Y	Y		Y		Page10 , 0xA9	0xFFC4
100	P5.6	Y	Y	Y	Y		Y		Page10 , 0xA9	0xFFC5
101	P5.7	Y	Y				Y		Page10 , 0xAB	0xFFC6
102	P7.6	Y	Y	Y	Y		Y		Page10 , 0xAA	0xFFD5
103	P7.5	Y	Y	Y	Y		Y		Page10 , 0xAC	0xFFD4
104	P7.4	Y	Y	Y	Y		Y		Page10 , 0xAC	0xFFD3
105	P8.0	Y	Y	Y	Y		Y		Page10 , 0xAA	0xFFD6
108	P8.1	Y	Y	Y	Y		Y		Page10 , 0xAB	0xFFD7
109	P3.2	Y	Y	Y	Y		Y		Page10 , 0xAD	SFR Access
110	P3.3	Y	Y	Y	Y			Y	Page10 , 0xAD	SFR Access
111	P3.4	Y	Y	Y	Y			Y	Page10 , 0xAE	SFR Access
112	P3.5	Y	Y	Y	Y			Y	Page10 , 0xAE	SFR Access
113	P3.6	Y	Y	Y	Y			Y	Page10 , 0xB0	SFR Access
114	P3.7	Y	Y	Y	Y			Y	Page10 , 0xB2	SFR Access
119	PC.1	N	Y	Y	Y			Y	Page10 , 0xA1	0xFFA2
121	P7.3	Y	Y	Y	Y			Y	Page10 , 0xB0	0xFFD2
122	P7.2	Y	Y	Y	Y			Y	Page10 , 0xB0	0xFFD1
123	P7.1	Y	Y	Y	Y			Y	Page10 , 0xB1	0xFFD0
124	P7.0	Y	Y	Y	Y			Y	Page10 , 0xB1	0xFFCF
126	PC.0	Y	Y	Y	Y		Y		Page10 , 0xA1	0xFFA3

PWM Assignment

GPIO Pin List	Name	PWM (Push-	PWM (Open-drain)	3.3V Tolerance	5V Tolerance	5V Tolerance (When Power Off)	Pin Share Register
48	PWM0	Y				Y	Page10 , 0xA7
55	PWM1	Y	Y			Y	Page10 , 0xA6
55	PWM5	Y				Y	Page10 , 0xA6
63	PWM2	Y	Y			Y	Page10 , 0xA6
64	PWM0	Y	Y			Y	Page10 , 0xA3
65	PWM1	Y	Y		Y		Page10 , 0xB1
71	PWM1	Y			Y		Page10 , 0xA7
71	PWM5	Y			Y		Page10 , 0xA7
72	PWM3	Y	Y		Y		Page10 , 0xB2
96	PWM0	Y			Y		Page10 , 0xA8
97	PWM1	Y	Y		Y		Page10 , 0xA8
98	PWM2	Y			Y		Page10 , 0xAA
99	PWM3	Y	Y		Y		Page10 , 0xA9
100	PWM4	Y	Y		Y		Page10 , 0xA9
101	PWM5	Y			Y		Page10 , 0xAB
102	PWM0	Y	Y		Y		Page10 , 0xAA
103	PWM1	Y			Y		Page10 , 0xAC
114	PWM4	Y				Y	Page10 , 0xB2
119	PWM5	Y	Y			Y	Page10 , 0xA1
126	PWM1	Y	Y		Y		Page10 , 0xA1

**TCON Assignment**

Pin 55	TCON[0]	TCON[5]	
Pin 56	TCON[1]	TCON[4]	
Pin 57	TCON[9]	TCON[11]	
Pin 58	TCON[7]	TCON[10]	
Pin 59	TCON[3]	TCON[5]	
Pin 63	TCON[1]	TCON[8]	
Pin 64	TCON[0]	TCON[7]	
Pin 65	TCON[1]	TCON[7]	
Pin 66	TCON[2]	TCON[4]	
Pin 67	TCON[5]	TCON[9]	
Pin 68	TCON[3]	TCON[13]	
Pin 69	TCON[3]	TCON[7]	
Pin 70	TCON[9]	TCON[11]	
Pin 71	TCON[8]	TCON[10]	
Pin 72	TCON[6]	TCON[12]	
Pin 99	TCON[6]	TCON[11]	
Pin 100	TCON[3]	TCON[12]	
Pin 101	TCON[0]		
Pin 102	TCON[10]		
Pin 103	TCON[8]		
Pin 104	TCON[5]		
Pin 105	TCON[9]		
Pin 108	TCON[7]		
Pin 109	TCON[3]		
Pin 110	TCON[2]	TCON[6]	TCON[7]
Pin 111	TCON[4]	TCON[7]	
Pin 112	TCON[5]	TCON[9]	
Pin 113	TCON[1]	TCON[11]	
Pin 114	TCON[0]	TCON[13]	



5. Register Description

Global Event Flag

Register::ID_Reg						0x00
Name	Bit	R/W	Default	Description	Config	
ID	7:0	R	0x51	MSB 4 bits: 0101 product code LSB 4 bits: 0001 rev. code		

Register:: Host_ctrl						0x01
Name	Bit	R/W	Default	Description	Config.	
XTAL_PWDN	7	R/W	0	Power Gated XTAL (active high)		
Reset_chk	6	R/W	0	Reset Check Once scalar is reset, this value will be cleared to 0. The purpose of it is to check if LVR has been triggered. It should be written to 1 ahead, then read it.. LVR has been triggered if the value is 0, else LVR has not.		
Rev	5:3	---	---	Reserved		
PD_EN	2	R/W	1	Power Down Mode Enable 0: Normal 1: Enable power down mode(Default) Turn off ADC RGB Channel/ ADC Band-gap/ SOG/ DPLL/ LVDS/ADC PLL/ SYNC- PROC/ TMDS /AUTO SOY ADC/m2pll Note: For LVDS Power Control, refer to following table.		
PS_EN	1	R/W	1	Power Saving Mode Enable 0: Normal 1: Enable power saving mode (Default) Turn off ADC RGB channel/ DPLL/ LVDS/ ADC PLL/ m2pll When power down or power saving function is enabled, internal mcu clock is forced to crystal clock. Note: For LVDS Power Control, refer to following table.		
Sft_Reset	0	R/W	0	Software Reset Whole Chip (Low pulse at least 8ms) 0: Normal (Default) 1: Reset All registers are reset to default except HOST_CTRL and power-on-latch.		



DISP_TYPE <u>CR 8C-00[1:0]</u>	DATA_TYPE <u>CR 28[2]</u>	Port	Power Control
LVDS [01]	Double [1]	LVDS Even	Power Down/Power Saving <u>CR01 [2]/CR 01[1]</u>
LVDS [01]	Double [1]	LVDS Odd	
LVDS [01]	Single [0]	LVDS Even	Power Up LVDS Even-Port <u>CR8C-A0 [5]</u>
LVDS [01]	Single [0]	LVDS Odd	Power Up LVDS Odd-Port <u>CR8C-A0 [4]</u>

Register:: STATUS0					0x02
Name	Bit	R/W	Default	Description	Config.
ADCPLL_nonlock	7	R	0	ADC_PLL Non-Lock If the ADC_PLL non-lock occurs, this bit is set to “1”.	
IVS_error	6	R	0	Input VSYNC Error If the input vertical sync occurs within the programmed active period, this bit is set to “1”.	
IHS_error	5	R	0	Input HSYNC Error If the input horizontal sync occurs within the programmed active period, this bit is set to “1”.	
ODD_Occur	4	R	0	Input ODD Toggle Occur (For internal field odd toggle, refer to CR1A[5]) If the ODD signal (From SAV/EAV or V16_ODD) toggle occurs, this bit is set to “1”.	
V8HV_Occur	3	R	0	Video8 Input Vertical/Horizontal Sync Occurs If the YUV input V or H sync edge occurs, this bit is set to “1”.	
ADCHV_Occur	2	R	0	ADC Input Vertical/Horizontal Sync Occurs Input V or H sync edge occurs; this bit is set to “1”.	
Buffer_Ovf1	1	R	0	Input Overflow Status (Frame Sync Mode) * ¹ If an overflow in the input data capture buffer occurs, this bit is set to “1”.	
Buffer_Udf1	0	R	0	Line Buffer Underflow Status (Frame Sync Mode) If an underflow in the line-buffer occurs, this bit is set to “1”.	

Write to clear status.

*¹Only first event of input overflow/underflow is recorded if both of them occurs.



Register:: STATUS1						0x03
Name	Bit	R/W	Default	Description	Config.	
Buffer_Ovf2	7	R	0	Line Buffer Overflow Status 1: Line Buffer overflow has occurred since the last status cleared		
Buffer_Udf2	6	R	0	Line Buffer Underflow Status 1: Line Buffer underflow has occurred since the last status cleared		
DENA_Stop	5	R	0	DENA Stop Event Status 1: If the DENA stop event occurred since the last status cleared		
DENA_Start	4	R	0	DENA Start Event Status 1: If the DENA start event occurred since the last status cleared as an interrupt source		
DVS_Start	3	R	0	DVS Start Event Status 1: If the DVS start event occurred since the last status cleared		
IENA_Stop	2	R	0	IENA Stop Event Status 1: If the IENA stop event occurred since the last status cleared		
IENA_Start	1	R	0	IENA Start Event Status 1: If the IENA start event occurred since the last status cleared		
IVS_Start	0	R	0	IVS Start Event Status 1: If the IVS start event occurred since the last status cleared		

Write to clear status.

Register::IRQ_CTRL0						0x04
Name	Bit	R/W	Default	Description	Config.	
IRQ_EN	7	R/W	0	Internal IRQ Enable: (Global) 0: Disable these interrupt. 1: Enable these interrupt.		
IRQ_ADCPLL	6	R/W	0	IRQ (ADC_PLL Non-Lock) 0: Disable the ADC_PLL non-lock error event as an interrupt source 1: Enable the ADC_PLL non-lock error event as an interrupt source		
IRQ_IHV	5	R/W	0	IRQ (Input VSYNC/HSYNC Error) (DEN across Vsync or Hsync) 0: Disable the Input VSYNC/HSYNC error event as an interrupt source 1: Enable the Input VSYNC/HSYNC error event as an interrupt source		
IRQ_ODD	4	R/W	0	IRQ (Input ODD Toggle Occur) (EAV/SAV from Video8)		



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				0: Disable Input ODD toggle event as an interrupt source 1: Enable the Input ODD toggle event as an interrupt source	
IRQ_V8_HV	3	R/W	0	IRQ (Video8 Input Hsync/Vertical Sync Occurs) 0: Disable the Video8 Input Hsync or Vsync event as an interrupt source 1: Enable the Video8 Input Hsync or Vsync event as an interrupt source	
IRQ_ADC_HV	2	R/W	0	IRQ (ADC Input Hsync/Vertical Sync Occurs) 0: Disable the ADC Input Hsync or Vsync event as an interrupt source 1: Enable the ADC Input Hsync or Vsync event as an interrupt source	
IRQ_Buffer	1	R/W	0	IRQ (Line Buffer Underflow/Overflow Status) 0: Disable the Line Buffer underflow/overflow event as an interrupt source 1: Enable the Line Buffer underflow/overflow event as an interrupt source	
IRQ_IENA	0	R/W	0	IRQ (Input ENA Start Event Occurred Status) 0: Disable IENA start as interrupt source 1: Enable IENA start as interrupt source	

Register:: HDMI_STATUS0 0x05					
Name	Bit	R/W	Default	Description	Config.
HDMI status 0	7:0	R	---	Reference to CRCB for HDMI Function (Page 2)(write 1 clear)	

Register:: HDMI_STATUS1 0x06					
Name	Bit	R/W	Default	Description	Config.
HDMI status 1	7:0	R	---	Reference to CRCC for HDMI Function (Page 2)(write 1 clear)	



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Register:: New_added_status0						0x07
Name	Bit	R/W	Default	Description	Config.	
Wstate	7	R	---	Wait state status		
New_m_state	6	R	---	New mode state		
Change_m_happen	5	R	---	Change mode happen (it will not be triggered while VGIP active signal is low)		
Wstate_IRQ_en	4	R/W	0	IRQ enable of Wait state status 0:disable 1:enable		
New_m_state_IRQ_en	3	R/W	0	IRQ enable of New mode status 0:disable 1:enable		
Change_m_happen_IRQ_en	2	R/W	0	IRQ enable of change mode happen status 0:disable 1:enable		
Reserved	1	—	—	Reserved to DP_IRQ		
Reserved	0	—	—	Reserved to VBI_Status		

Register:: New_added_status1						0x08
Name	Bit	R/W	Default	Description	Config.	
Reserved	7:6	---	---	Reserved-		
Reserved	5:0	---	---	Reserved		

Power Control

Register:: Power_Ctrl0						0x09
Name	Bit	R/W	Default	Description	Config.	
Powoff_EO	7	R	-	Top power off block power cut cell strong control signal flag. When all power cut strong control enable, the flag will be 1.		
Powoff_EWO	6	R	-	Top power off block power cut cell weak control signal flag. When all power cut weak control enable, the flag will be 1.		
Powoff_EI_FW	5	R/W	1	Top power off block power cut cell strong control enable by F/W. Not control power cut cell directly, decided by 0x0B[7]		
Powoff_EWI	4	R/W	1	Top power off block power cut cell weak control enable.		
Xtal clock select	3	R/W	0	X'tal clock select 0: external xtal 1: internal OSC Reset to default value only when		



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				external reset/por happen	
Xtal power off	2	R/W	0	0: normal mode 1: disable xtal	
Top_Pwr_off_blk_i so ctrl	1	R/W	0	Top power off block isolation control 0: normal mode 1: isolation mode	
Top_pwr_off_blk_s oft_rst	0	R/W	0	0: normal 1: reset	

Register:: Power_Ctrl1					0x0A
Name	Bit	R/W	Default	Description	Config.
Reserved	7	-	-	Reserved to GDIoff_EO	
Reserved	6	-	-	Reserved to GDIoff_EWO	
Reserved	5	-	0	Reserved to GDIoff_EI_FW	
Reserved	4	-	0	Reserved to GDIoff_EWI	
Analog_block_pwr _off_det_sel	3	R/W	0	analog block power off detection select, LVDSPPLL only 0: register control (bit2) 1: power-off region power line (no use)	
Analog_blk_pwr_o ff_ctrl	2	R/W	0	analog block power off control , LVDSPPLL only 0: normal mode 1: isolation mode	
Reserved	1	-	0	Reserved to GDI_pwr_off_blk_iso_ctrl	
Reserved	0	-	0	Reserved to GDI_pwr_off_blk_soft_rst	

Register:: Power_Ctrl2					0x0B
Name	Bit	R/W	Default	Description	Config.
Powoff_EI_sel	7	WR/W	0	Top power off block power cut cell strong control enable select 0: controlled by F/W 0x09[5] 1: controlled by power cut cell weak control flag, so the flow will be weak on -> strong on	
reserved	6:43	W	0	Reserved	
ldo_on	2	R	--	1: LDO controlled by Page0, 0xDF, 0xE0 0: LDO is disabled in this chip	
sync_pro_sync_sel	1	R/W	0	Select Sync processor V-sync2/H-sync2 source 0: from PAD_AVSS1(pin40) / PAD_AHS1(pin39) 1: from d-domain DVS/DHS	
OSC_27M_EN	0	WR/W	0	EMB_OSC 27MHz and 14.318MHz select 0: 14.318MHz 1: 27MHz	

Watch Dog

Address: 0C WATCH_DOG_CTRL0

Default: 00h

Bit	Mode	Function
-----	------	----------



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7	R/W	Auto Switch When Input HSYNC/VSYNC Error 0: Disable (Default) 1: Enable (See CR02[6] and CR02[5])
6	R/W	Auto Switch When Input HSYNC/VSYNC Timeout or Overflow 0: Disable (Default) 1: Enable (See CR52[4] and CR54[5:4])
5	R/W	Auto Switch When Display VSYNC Timeout 0: Disable (Default) 1: Enable
4	R/W	Auto Switch When ADC-PLL Unlock 0: Disable (Default) 1: Enable
3	R/W	Auto Switch When Overflow or Underflow (for Frame-Sync Display) 0: Disable (Default) 1: Enable
2	R/W	Watch-Dog Action if Event Happened (for Display Timing) 0: Disable (Default) 1: Free Run
1	R/W	Watch-Dog Action if Event Happened (for Display Data) 0: Disable (Default) 1: Background (Turn off overlay function and switch to background display simultaneously)
0	R	Display VSYNC Timeout Flag (for CR0C[5]) 0: DVS is present 1: DVS is timeout The line number of Display HS is equal to Display Vertical Total; this bit is set to “1”. (Write to clear status).

Address: 0D

WATCH_DOG_CTRL1

Default: 00h

Bit	Mode	Function
7	R/W	Auto Switch When Input HSYNC Changed 0: Disable (Default) 1: Enable (See CR58[3])
6	R/W	Auto Switch When Input VSYNC Changed 0: Disable (Default)



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		1: Enable (See CR58[2])
5	R/W	Wstate WD enable 0:Disable(Default) 1:enable
4	R/W	New_m_state 0:Disable(Default) 1:enable
3	R/W	Change_mode_happen 0:Disable(Default) 1:enable
2:0	---	Reserved

Address: 0E~0F Reserved

Input Video Capture

Address: 10 VGIP_CTRL (Video Graphic Input Control Register) Default: 00h

Bit	Mode	Function				
7	R/W	8 bit Random Generator 0: Disable(Default) 1: Enable				
6	R/W	Input Test Mode: 0: Disable (Default) 1: Video8 input will go through RGB channel, AVS=>IVS, AHS=>IHS, VCLK=>ICLK				
5	R/W	VGIP Double Buffer Ready 0: Not Ready to Apply 1: Ready to Apply When the list table of CR10[4] is set, then enable CR10[5] . Finally, hardware will auto load these values into VGIP double buffer registers as the trigger event happens and clear CR10[5] to 0.				
4	R/W	VGIP Double Buffer Mode Enable (Each register described below has its own double buffer) 0: Disable (Original- Write instantly by MCU write cycles) 1: Enable (Double Buffer Function Write Mode) <table border="1" style="width: 100%; border-collapse: collapse;"> <tr> <th style="text-align: center;">Register</th> <th style="text-align: center;">Trigger Event</th> </tr> <tr> <td style="padding: 2px;">PLLPHASE(CRB3,CRB4) Add 1-clk Delay to IHS Delay (CR12[4]) HSYNC Synchronize Edge (CR12[3])</td> <td style="padding: 2px;">Falling edge of Ivactive</td> </tr> </table>	Register	Trigger Event	PLLPHASE(CRB3,CRB4) Add 1-clk Delay to IHS Delay (CR12[4]) HSYNC Synchronize Edge (CR12[3])	Falling edge of Ivactive
Register	Trigger Event					
PLLPHASE(CRB3,CRB4) Add 1-clk Delay to IHS Delay (CR12[4]) HSYNC Synchronize Edge (CR12[3])	Falling edge of Ivactive					



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		IPH_ACT_STA (CR14[2:0],CR15)	Falling edge of Ivactive	
		IPV_ACT_STA (CR18[2:0],CR19)	Falling edge of Ivactive	
		IV_DV_LINES (CR40)		
		IVS_DELAY (for capture) (CR1C,CR1E[1])	Falling edge of Ivactive	
		IHS_DELAY (for capture) (CR1D, CR1E[0])	Falling edge of Ivactive	
3:2	R/W	Input Pixel Format		
		00: Embedded ADC (ADC_HS)(Default)		
		01: Embedded TMDS		
		10: Video8		
		11: Reserved		
1	R/W	Input Graphic/Video Mode		
		0: From analog input (input captured by ‘Input Capture Window’) (Default)		
		1: From digital input (captured start by ‘enable signal’, but still stored in ‘capture window size’)		
0	R/W	Input Sampling Run Enable		
		0: No data is transferred (Default)		
		1: Sampling input pixels		

Address: 11

VGIP_SIGINV (Input Control Signal Inverted Register)

Default: 00h

Bit	Mode	Function
7	R/W	Safe Mode 0: Normal (Default) 1: Safe Mode Enable, mask 1 frame IVS of every 2 frame IVS, slow down input frame rate.
6	R/W	IVS Sync with IHS Control (Avoid VS bouncing) 0: Enable (Default) 1: Disable
5	R/W	HS Signal Inverted for Field Detection 0: Negative Edge (Default) 1: Positive Edge
4	R/W	Input Video ODD Signal Invert Enable 0: Not inverted (ODD = positive polarity) (Default) 1: Inverted (ODD = negative polarity)
3	R/W	Input VS Signal Polarity Inverted 0: Not inverted (VS = positive polarity) (Default) 1: Inverted (VS = negative polarity)
2	R/W	Input HS Signal Polarity Inverted 0: Not inverted (HS = positive polarity) (Default) 1: Inverted (HS = negative polarity)



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1	R/W	Input ENA Signal Polarity Inverted 0: Not inverted (input high active) (Default) 1: Inverted (while input low active)
0	R/W	Video Input Clock Polarity 0: Rising edge latched (Default) 1: Falling edge latched

Address: 12 VGIP_DELAY_CTRL**Default: 00h**

Bit	Mode	Function
7	R	6-Iclk-delay HS Level Latched by VS Rising Edge
6	R	HS Level Latched by VS Rising Edge
5	R	HS Level Latched by 6-Iclk-delay VS Rising Edge
4	R/W/D	Add One Clock Delay to IHS Delay 0: Disable (Default) 1: Enable
3	R/W/D	HSYNC Synchronize Edge 0: HSYNC is synchronized by the positive edge of the input clock 1: HSYNC is synchronized by the negative edge of the input clock (HSYNC source is selected by CR48[0] and then synchronized)
2	R/W	VSYNC Synchronize Edge 0: Latch VS by the negative edge of input HSYNC (Default) 1: Latch VS by the positive edge of input HSYNC
1:0	R/W	Video Input Clock Delay Control: 00: Normal (Default) 01: 1ns delay 10: 2ns delay 11: 3ns delay

Address: 13 VGIP_ODD_CTRL (Video Graphic Input ODD Control Register)**Default: 00h**

Bit	Mode	Function
7	R/W	ODD Inversion for ODD-Controlled-IVS-Delay 0: Not Invert (Default) 1: Invert
6	R/W	ODD-Controlled-IVS-Delay One-Line Enable 0: Disable (Default) 1: Enable (Both for Auto and Capture)
5	R/W	Safe Mode ODD Inversion 0: Not inverted (Default)



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		1: Inverted
4	R/W	Force ODD Toggle Enable (Without ODD/EVEN Toggle Select in Safe Mode) 0: Disable (Default) 1: Enable
3	---	Reserved
2	R/W	Decode Video8 when ADC or TMDS Active 0: Disable (Default) 1: Enable
1	R/W	EAV Error Correction Enable in Video-8 0: Disable 1: Enable
0	R/W	Internal ODD Signal Selection 0: ODD signal from EAV, SAV or HDMI (Default) 1: Internal Field Detection ODD signal by CR1A[5] (Also support under VGA, DVI input)



Input Frame Window

(All capture window setting unit is 1)

Address: 14 IPH_ACT_STA_H (Input Horizontal Active Start)

Default: 00h

Bit	Mode	Function
7:4	R/W/D	Input Video Horizontal Active Width -- High Byte [11:8]
3:0	R/W/D	Input Video Horizontal Active Start -- High Byte [11:8]

Address: 15 IPH_ACT_STA_L (Input Horizontal Active Start Low)

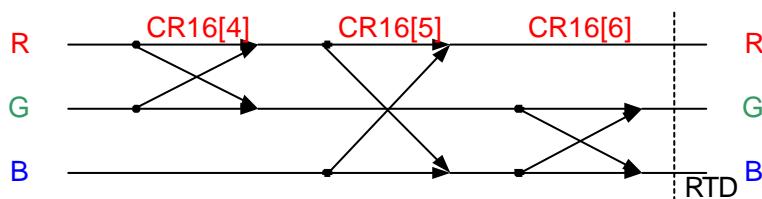
Default: 00h

Bit	Mode	Function
7:0	R/W/D	Input Video Horizontal Active Start -- Low Byte [7:0]

- In analog mode, **IPH_ACT_STA** means the delay number of pixel clock from the leading edge of HS to the first pixel of each active line. Actual delay number of pixel clock = **IPH_ACT_STA(>=2) +2**,
- In digital mode, **IPH_ACT_STA** means the delay number of pixel clock from the leading edge of DE to the first pixel of each active line. Actual delay number of pixel clock = **IPH_ACT_STA(>=0)**

Address: 16 IPH_ACT_WID_H (Input Horizontal Active Width High) **Default: 00h**

Bit	Mode	Function
7	R/W	Video8 -C-Port Input Latch Bus MSB to LSB Swap Control: 0: Normal (Default) 1: Swap Video8 -C-port MSB to LSB sequence into LSB to MSB
6	R/W	ADC Input G/B Swap 0: No Swap 1: Swap
5	R/W	ADC Input R/B Swap 0: No Swap 1: Swap
4	R/W	ADC Input R/G Swap 0: No Swap 1: Swap
3	R/W	Double Clock Input 0: Single Clock 1: Double Clock this bit should be set double clock when using video 8 input
2:0	R/W	Reserved





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Address: 17 IPH_ACT_WID_L (Input Horizontal Active Width Low) Default: 00h

Bit	Mode	Function
7:0	R/W	Input Video Horizontal Active Width -- Low Byte [7:0]

This register defines the number of active pixel clocks to be captured.

Address: 18 IPV_ACT_STA_H (Input Vertical Active Start High) Default: 00h

Bit	Mode	Function
7:4	R/W	Input Video Vertical Active Lines – High Byte [11:8]
3:0	R/W/D	Input Video Vertical Active Start – High Byte [11:8]

Address: 19 IPV_ACT_STA_L (Input Vertical Active Start Low) Default: 00h

Bit	Mode	Function
7:0	R/W/D	Input Video Vertical Active Start – Low Byte [7:0]

The numbers of lines from the leading edge of selected input video VSYNC to the first line of the active window.

The value above should be larger than 1.

Address: 1A IPV_ACT_LEN_H (Input Vertical Active Lines) Default: 00h

Bit	Mode	Function
7	R	SAV/EAV 2-Bit Error Happened (Set if happened and write to clear)
6	R	SAV/EAV 1-Bit Error Happened (Set if happened and write to clear)
5	R	Internal Field Detection ODD Toggle Happened (Set if happened and write to clear) The function should be worked under no input clock
4:3	R	Number of Input HS between 2 Input VS (LSB bit [1:0])
2:0	R/W	Reserved

Address: 1B IPV_ACT_LEN_L (Input Vertical Active Lines) Default: 00h

Bit	Mode	Function
7:0	R/W	Input Video Vertical Active Lines – Low Byte [7:0]

This register defines the number of active lines to be captured.

Address: 1C IVS_DELAY (Internal Input-VS Delay Control Register) Default: 00h

Bit	Mode	Function
7:0	R/W/D	Input VSYNC Delay for Capture[7:0] (Counted by Input HSYNC) It's IVS delay for capture and digital filter, not for auto function

Address: 1D IHS_DELAY (Internal Input-HS Delay Control Register) Default: 00h

Bit	Mode	Function
7:0	R/W/D	Input HSYNC Delay for Capture [7:0] (Counted by Input Pixel Clock) It's IHS delay for capture and digital filter, not for auto function



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Address: 1E VGIP_HV_DELAY

Default: 00h

Bit	Mode	Function
7:6	R/W	Input HSYNC Delay for Auto Function (Counted by Input Pixel Clock) 00: No delay 01: 32 pixels 10: 64 pixels 11: 96 pixels
5:4	R/W	Input VSYNC Delay for Auto Function (Counted by Input HSYNC) 00: No delay 01: 3 line 10: 7 line 11: 15 line
3	R/W	Select DataEnable or HSync to adjust clock phase 0: use DataEnable to adjust clock phase (Default) 1: use HSync to adjust clock phase (while input source as ADC)
2	---	Reserved
1	R/W/D	Input VSYNC Delay for Capture[8] (Counted by Input HSYNC)
0	R/W/D	Input HSYNC Delay for Capture[8] (Counted by Input Pixel Clock)

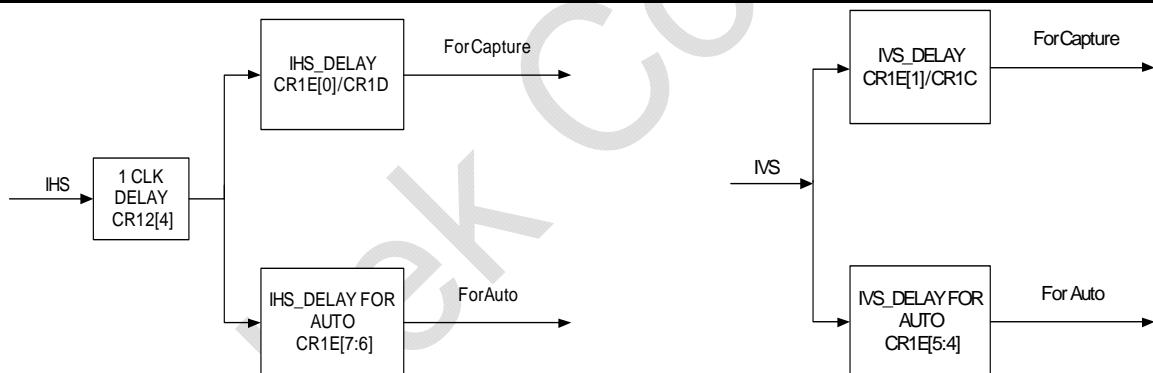


Figure 15: Input HSYNC/VSYNC Delay Path Diagram

Address: 1F V8 Source Select & YUV422 to YUV444Conversion

Default: 20h

Bit	Mode	Function
7	R/W	Reorder the data flow 0: dfilter -> color_conversion -> dithering -> HSD (Default) 1: dfilter -> dithering -> color_conversion -> HSD
6	R/W	V8 source select 0: From Pin 31~39 (excluding pin 38) 1: From Pin 41~48
5:4	R/W	Reserved to 2'b10
3	R/W	Video 4:2:2->4:4:4 Enable before Scale-Down 0: Disable (Default)



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		1: Enable (This bit should be always enable when in Video8/ HDMI YUV422 mode.)
2	R/W	Video 4:2:2->4:4:4 Mode Select 0: Interpolation (Default) 1: Duplicate (This bit would be work only while CR1F[3] is enable)
1	R/W	Output 444 Format (only work in Interpolation Mode) 0: $Y_0U_0V_0, Y_1\frac{[U_0+U_2]/2}{[V_0+V_2]/2}, Y_2U_2V_2, Y_3\frac{[U_2+U_4]/2}{[V_2+V_4]/2}...$ 1: $Y_0U_0V_1, Y_1\frac{[U_0+U_2]/2}{V_1}, Y_2U_2\frac{[V_1+V_3]/2}{[U_2+U_4]/2}V_3...$
0	R/W	UV Swap (for YUV422 to YUV444) (only work in Interpolation Mode) 0: Sequence 444 result: Y, U, V 1: Sequence 444 result: Y, V, U

Address: 20 V8CLK_SEL (v8clk selection setting)

Default: 00h

Bit	Mode	Function
7:6	---	Reserved
5:4	R/W	V8clk divider: 00: div 2 (Default) 01: div 4 10: div 8 11: reserved
3	---	Reserved
2:0	R/W	V8clk_phase: 000: phase 0 (Default) 001: phase 1 010: phase 2 (not work while div2) 011: phase 3 (not work while div2) 100: phase 4 (not work while div2 & div4) 101: phase 5 (not work while div2 & div4) 110: phase 6 (not work while div2 & div4) 111: phase 7 (not work while div2 & div4)



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FIFO Frequency

Address: 22

FIFO Frequency

Default: 00h

Bit	Mode	Function
7	R/W	Test Mode 0: Disable 1: Input data of VGIP Replaced by Background Color in CR6D
6:3	R/W	Reserved to 0
2	R/W	Internal Xtal Frequency 0: Fxtal 1: Fxtal * M2PLL_M / M2PLL_N / 10
1:0	R/W	FIFO Frequency 00: M2PLL 01: ICLK 10: DCLK 11: Test clock

Scaling Down Control

Address: 23

SCALE_DOWN_CTRL (Scale Down Control Register)

Default:00h

Bit	Mode	Function
7	R/W	Vertical scale down function mode selection: 0: Use line interpolation mode (Default) 1: Use drop line mode (Note: This bit is only valid while CR23[0]=1'b1.)
6	R	Bist for Line Buffer one & two ok 0: Fail 1: Ok
5	R/W	FIFO Line Buffer Bist Function Start (Auto clear to 0 when finish) 0: Finish 1: Start
4	R/W	Reserved
3	R/W	Horizontal non-linear scale down 0: linear 1: non-linear
2	R/W	Vertical Scale-Down Compensation 0: Disable (Default) 1: Enable
1	R/W	Horizontal scale down function enable:



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		0: Disable scale down function (Default) 1: Enable scale down function
0	R/W	Vertical scale down function enable: 0: Disable scale down function (Default) 1: Enable scale down function (Note: There is a bit to select interpolation or dropping for vertical scale down at CR23[7].)

Address: 24 Scale_Down_Access_Port Control Default: 00h

Bit	Mode	Function
7	R/W	Enable scale-down access port
6:5	--	Reserved to 0
4:0	R/W	Scale-down port address

Address: 25-00 V_SCALE_INIT

Bit	Mode	Function
7:6	--	Reserved
5:0	R/W	Vertical Scale Down Initial Select [5:0]

- Scale Down Initial Point Select: for example, if the value is 43, we select the initial point is 43/64

Address: 25-01 V_SCALE_DH (Vertical scale down factor register)

Bit	Mode	Function
7:3	R/W	Reserved
2:0	R/W	Vertical Scale Down Factor [18:16]

Address: 25-02 V_SCALE_DM (Vertical scale down factor register)

Bit	Mode	Function
7:0	R/W	Vertical Scale Down Factor [15:8]

Address: 25-03 V_SCALE_DL (Vertical scale down factor register)

Bit	Mode	Function
7:0	R/W	Vertical Scale Down Factor [7:0]

- Registers {V_SCALE_DH, V_SCALE_DM, V_SCALE_DL} = $(Y_i/Y_m) * (2^{17})$.
- The largest scale down ratio is 1/4 (integer part 2 bits)
- Meanwhile, Y_i = vertical input length; Y_m =vertical memory write length

Address: 25-04 H_SCALE_INIT

Bit	Mode	Function
7:6	--	Reserved
5:0	R/W	Horizontal Scale Down Initial Select [5:0]

- Scale Down Initial Point Select: for example, if the value is 43, we select the initial point is 43/64

Address: 25-05 H_SCALE_DH

Bit	Mode	Function
7:0	R/W	Horizontal Scale Down Factor [23:16]



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Address: 25-06 H_SCALE_DM

Bit	Mode	Function
7:0	R/W	Horizontal Scale Down Factor [15:8]

Address: 25-07 H_SCALE_DL

Bit	Mode	Function
7:0	R/W	Horizontal Scale Down Factor [7:0]

- For linear scale down, registers {H_SCALE_DH, HSCALE_DM, HSCALE_DL} = $(X_i/X_m) * (2^{20})$.
- Meanwhile, X_i = vertical input length; X_m =vertical memory write length

Address: 25-08 H_SCALE_ACCH

Bit	Mode	Function
7	--	Reserved
6:0	R/W	Horizontal Scale Down Accumulated Factor [14:8]

Address: 25-09 H_SCALE_ACCL

Bit	Mode	Function
7:0	R/W	Horizontal Scale Down Accumulated Factor [7:0]

Address: 25-0A SD_ACC_WIDTHH

Bit	Mode	Function
7:2	--	Reserved
1:0	R/W	Horizontal Scale Down Accumulated Width [9:8]

Address: 25-0B SD_ACC_WIDTHL

Bit	Mode	Function
7:0	R/W	Horizontal Scale Down Accumulated Width [7:0]

Address: 25-0C SD_FLAT_WIDTHH

Bit	Mode	Function
7:3	--	Reserved
2:0	R/W	Horizontal Scale Down Flat Width [10:8]

Address: 25-0D SD_FLAT_WIDTHL

Bit	Mode	Function
7:0	R/W	Horizontal Scale Down Flat Width [7:0]

Address: 25-0E, 25-0F reserved**Address: 25-10 Input Pattern Generator Ctrl 0**

Default: 8'h00

Bit	Mode	Function
7	R/W	Pattern reset to initial value 0 : 1 frame 1 : 16 frame
6	R/W	Random generator mode 0 : $x^9 + x^3 + 1$ 1 : $x^{29}+x^{16}+x^4+x+1$ (Green, Blue, Red)
5	R/W	Data update (RED) 0 : reference data enable(pixel base) 1: reference horizontal data enable end(line base)
4	R/W	Data update (GREEN) 0 : reference data enable 1: reference horizontal data enable end
3	R/W	Data update (BLUE)



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		0 : reference data enable 1: reference horizontal data enable end
2	R/W	Pattern generator mode (RED) 0 : random generator (ref. CR25-10[6] 1 : pattern generator (reg. CR25-11[2]))
1	R/W	Pattern generator mode (GREEN) 0 : random generator (ref. CR25-10[6] 1 : pattern generator (reg. CR25-11[1]))
0	R/W	Pattern generator mode (BLUE) 0 : random generator (ref. CR25-10[6] 1 : pattern generator (reg. CR25-11[0]))

Address: 25-11 Input Pattern Generator Ctrl 1**Default: 8'h00**

Bit	Mode	Function
7-3	R/W	Reserved to 0
2	R/W	Pattern generator (RED) 0 : Out(n) = Out(n-1) 1: Out(n) = Out(n-1) + 1
1	R/W	Pattern generator (GREEN) 0 : Out(n) = Out(n-1) 1: Out(n) = Out(n-1) + 1
0	R/W	Pattern generator (BLUE) 0 : Out(n) = Out(n-1) 1: Out(n) = Out(n-1) + 1

Address: 25-12 Input Pattern Generator RED Initial Value**Default: 8'h01**

Bit	Mode	Function
7-0	R/W	RED Initial Value [7:0]

Address: 25-13 Input Pattern Generator GREEN Initial Value**Default: 8'h01**

Bit	Mode	Function
7-0	R/W	Green Initial Value [7:0]

Address: 25-14 Input Pattern Generator BLUE Initial Value**Default: 8'h01**

Bit	Mode	Function
7-0	R/W	BLUE Initial Value [7:0]

Address: 25-15 Input Pattern Generator RED/GREEN/BLUE Initial Value Default: 8'h00

Bit	Mode	Function
7-6	R/W	Reserved to 0
5-4	R/W	RED Initial Value [9:8]
3-2	R/W	GREEN Initial Value [9:8]
1-0	R/W	BLUE Initial Value [9:8]

Address: 26~27 are Reserved

Display Format

Address: 28 VDIS_CTRL (Video Display Control Register)**Default: 20h**

Bit	Mode	Function



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7	R/W	Force Display Timing Generator Enable: (Should be set when in Free-Run mode) 0: wait for input IVS trigger 1: force enable
6	R/W	Display Data Output Inverse Enable 0: Disable (Default) 1: Enable (only when data bus clamp to 0)
5	R/W	Display Output Force to Background Color 0: Display output operates normally 1: Display output is forced to the color as selected by background color (CR6D) (Default)
4	R/W	Display 18 bit RGB Mode Enable 0: All individual output pixels are full 24-bit RGB (Default) 1: All individual output pixels are truncated to 18-bit RGB (LSB 2 bits = 0)
3	R/W	Frame Sync Mode Enable 0: Free running mode (Default) 1: Frame sync mode
2	R/W	Display Output Double Port Enable 0: Single port output (Default) (Not effective if CR8C-A0[1]=1'b1) 1: Double port output
1	R/W	Display Output Run Enable 0: DHS, DVS, DEN & DATA bus are clamped to "0" (Default) 1: Display output normal operation.
0	R/W	Display Timing Run Enable 0: Display Timing Generator is halted, Zoom Filter halted (Default) 1: Display Timing Generator and Zoom Filter enabled to run normally

Steps to disable output: First set CR28[1]=0, set CR28[6], then set CR28[0]=0 to disable output.

Address: 29 VDISP_SIGINV (Display Control Signal Inverted) Default: 00h

Bit	Mode	Function
7	R/W	DHS Output Format Select (only available in Frame Sync) 0: The first DHS after DVS is active (Default) 1: The first DHS after DVS is inactive
6	R/W	Display Data Port Even/Odd Data Swap: 0: Disable (Default) 1: Enable
5	R/W	Display Data Port Red/Blue Data Swap 0: Disable (Default) 1: Enable
4	R/W	Display Data Port MSB/LSB Data Swap



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		0: Disable (Default) 1: Enable
3	R/W	Skew Display Data Output 0: Non-skew data output (Default) 1: Skew data output
2	R/W	Display Vertical Sync (DVS) Output Invert Enable: 0: Display Vertical Sync output normal active high logic (Default) 1: Display Vertical Sync output inverted logic
1	R/W	Display Horizontal Sync (DHS) Output Invert Enable: 0: Display Horizontal Sync output normal active high logic (Default) 1: Display Horizontal Sync output inverted logic
0	R/W	Display Data Enable (DEN) Output Invert Enable: 0: Display Data Enable output normal active high logic (Default) 1: Display Data Enable output inverted logic

Address: 2A DISP_ADDR (Display Format Address Port)

Bit	Mode	Function								
7	R/W	Display Setting Double buffer enable 0 : Disable 1 : Enable <table border="1" style="margin-left: 20px;"> <tr> <td>Register</td> <td>Trigger Event</td> </tr> <tr> <td>DH_TOTAL</td> <td>DVS Rising</td> </tr> <tr> <td>ODD_FIXED_LAST</td> <td>DVS Rising</td> </tr> <tr> <td>EVEN_FIXED_LAST</td> <td></td> </tr> </table>	Register	Trigger Event	DH_TOTAL	DVS Rising	ODD_FIXED_LAST	DVS Rising	EVEN_FIXED_LAST	
Register	Trigger Event									
DH_TOTAL	DVS Rising									
ODD_FIXED_LAST	DVS Rising									
EVEN_FIXED_LAST										
6	R/W	Display Double Buffer Ready 0: Not Ready to Apply 1: Ready to Apply When the list table of DISP_ADDR[7] is set, then enable DISP_ADDR[6], finally, hardware will auto load these value into RTD as the trigger event happens and clear DISP_ADDR[6] to 0.								
5:0	R/W	Display Format Address								

Address: 2B DISP_DATA (Display Format Data Port)

Bit	Mode	Function
7:0	R/W	Display Format Data

Address: 2B-00 DH_TOTAL_H (Display Horizontal Total Pixels)

Bit	Mode	Function
7	R/W	Series four line buffer



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6:4	--	Reserved to 0
3:0	R/W	Display Horizontal Total Pixel Clocks: High Byte[11:8]

Address: 2B-01 DH_TOTAL_L (Display Horizontal Total Pixels)

Bit	Mode	Function
7:0	R/W	Display Horizontal Total Pixel Clocks: Low Byte[7:0]

Real DH_Total (Target value)= DH_Total (Register value)+ 4

Address: 2B-02 DH_HS_END (Display Horizontal Sync End)

Bit	Mode	Function
7:0	R/W	Display Horizontal Sync End[7:0]: Determines the width of DHS pulse in DCLK cycles

Address: 2B-03 DH_BKGD_STA_H (Display Horizontal Background Start)

Bit	Mode	Function
7:4	--	Reserved to 0
3:0	R/W	Display Horizontal Background Start: High Byte [11:8]

Address: 2B-04 DH_BKGD_STA_L (Display Horizontal Background Start)

Bit	Mode	Function
7:0	R/W	Display Horizontal Background Start: Low Byte [7:0]

Determines the number of DCLK cycles from leading edge of DHS to first pixel of Background region.

Real DH_BKGD_STA (Target value)= DH_BKGD_STA (Register value)+ 10

Address: 2B-05 DH_ACT_STA_H (Display Horizontal Active Start)

Bit	Mode	Function
7:4	--	Reserved to 0
3:0	R/W	Display Horizontal Active Region Start: High Byte [11:8]

Address: 2B-06 DH_ACT_STA_L (Display Horizontal Active Start)

Bit	Mode	Function
7:0	R/W	Display Horizontal Active Region Start: Low Byte [7:0]

Determines the number of DCLK cycles from leading edge of DHS to first pixel of Active region.

Real DH_ACT_STA (Target value)= DH_ACT_STA (Register value)+ 10

Address: 2B-07 DH_ACT_END_H (Display Horizontal Active End)

Bit	Mode	Function
7:4	--	Reserved to 0
3:0	R/W	Display Horizontal Active End: High Byte [11:8]

Address: 2B-08 DH_ACT_END_L (Display Horizontal Active End)

Bit	Mode	Function
7:0	R/W	Display Horizontal Active End: Low Byte [7:0]

Determines the number of DCLK cycles from leading edge of DHS to the pixel of background region.



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Real DH_ACT_END (Target value)= DH_ACT_END (Register value)+ 10

Address: 2B-09 DH_BKGD_END_H (Display Horizontal Background End)

Bit	Mode	Function
7:4	--	Reserved to 0
3:0	R/W	Display Horizontal Background end: High Byte [11:8]

Address: 2B-0A DH_BKGD_END_L (Display Horizontal Background End)

Bit	Mode	Function
7:0	R/W	Display Horizontal Background end: Low Byte [7:0]

Real DH_BKGD-END (Target value) = DH_BKGD-END (Register value)+ 10

Address: 2B-0B DV_TOTAL_H (Display Vertical Total Lines)

Bit	Mode	Function
7:4	--	Reserved to 0
3:0	R/W	Display Vertical Total: High Byte [11:8]

Address: 2B-0C DV_TOTAL_L (Display Vertical Total Lines)

Bit	Mode	Function
7:0	R/W	Display Vertical Total: Low Byte [7:0]

CR2B-0B, CR2B-0C are used as watch dog reference value in *frame sync* mode, the event should be the line number of display HS is equal to DV Total.

Address: 2B-0D DVS-END (Display Vertical Sync End)

Bit	Mode	Function
7:5	--	Reserved to 0
4:0	R/W	Display Vertical Sync End[4:0]: Determines the duration of DVS pulse in lines

Address: 2B-0E DV_BKGD_STA_H (Display Vertical Background Start)

Bit	Mode	Function
7:4	--	Reserved to 0
3:0	R/W	Display Vertical Background Start: High Byte [11:8] Determines the number of lines from leading edge of DVS to first line of background region.

Address: 2B-0F DV_BKGD_STA_L (Display Vertical Background Start)

Bit	Mode	Function
7:0	R/W	Display Vertical Background Start: Low Byte [7:0]

Address: 2B-10 DV_ACT_STA_H (Display Vertical Active Start)

Bit	Mode	Function
7:4	--	Reserved to 0
3:0	R/W	Display Vertical Active Region Start: High Byte [11:8] Determines the number of lines from leading edge of DVS to first line of active region.



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Address: 2B-11 DV_ACT_STA_L (Display Vertical Active Start)

Bit	Mode	Function
7:0	R/W	Display Vertical Active Region Start: Low Byte [7:0]

Address: 2B-12 DV_ACT_END_H (Display Vertical Active End)

Bit	Mode	Function
7:4	--	Reserved to 0
3:0	R/W	Display Vertical Active Region End: High Byte [11:8]

Address: 2B-13 DV_ACT_END_L (Display Vertical Active End)

Bit	Mode	Function
7:0	R/W	Display Vertical Active Region End: Low Byte [7:0]

Determine the number of lines from leading edge of DVS to the line of following background region.

Address: 2B-14 DV_BKGD_END_H (Display Vertical Background End)

Bit	Mode	Function
7:4	--	Reserved to 0
3:0	R/W	Display Vertical Background end: High Byte [11:8]

Address: 2B-15 DV_BKGD_END_L (Display Vertical Background End)

Bit	Mode	Function
7:0	R/W	Display Vertical Background End: Low Byte [7:0]

Determine the number of lines from leading edge of DVS to the line of start of vertical blanking.

Address: 2B-16~2B-1F Reserved

Display Fine Tune

Address: 2B-20 DIS_TIMING (Display Clock Fine Tuning Register)

Default: 00h

Bit	Mode	Function
7	R/W	Reserved to 0
6:4	R/W	Display Output Clock Fine Tuning Control: 000: DCLK rising edge corresponds with output display data 001: 1ns delay 010: 2ns delay 011: 3ns delay 100: 4ns delay 101: 5ns delay 110: 6ns delay 111: 7ns delay
3	---	Reserved



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2	---	Reserved
1	R/W	DCLK Output Enable 0: Disable 1: Enable
0	R/W	DCLK Polarity Inverted 0: Disable 1: Enable

Address: 2B-21 OSD_REFERENCE_DEN Default: 00h

Bit	Mode	Function
7:0	R/W	Position Of Reference DEN for OSD[7:0]

Address: 2B-22 NEW_DV_CTRL Default: 00h

Bit	Mode	Function
7	R/W	New Timing Enable 0: Disable 1: Enable
6	R/W	Line Compensation Enable 0: Disable 1: Enable
5	R/W	Pixel Compensation Enable 0: Disable 1: Enable
4	R/W	Reserve to 0
3:0	R/W	DCLK_Delay[11:8]

Address: 2B-23 NEW_DV_DLY Default: 00h

Bit	Mode	Function
7:0	R/W	DCLK_Delay[7:0]

When CR2B-22[7]=1, DCLK_Delay[11:0] can't be 0.

Address: 2B-24 SSCG_NEW_Timing_Mode Setting Default: 00h

Bit	Mode	Function
7	R/W	SSCG New Timing Mode Even/Odd last line setting iverse 0: no inverse 1: inverse
6	R/W	SSCG New Timing Mode Even/Odd last line setting enable 0: disable 1: enable
5:0	R/W	Reserve



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Cyclic-Redundant-Check

Address: 2c **OP_CRC_CTRL (Output CRC Control Register)** **Default:** 00h

Bit	Mode	Function
7:6	R/W	CRC Selector 0x: CRC after scale-down 10: CRC after all-processing 11: reserved
5:1	--	Reserved to 0
0	R/W	Output CRC Control: 0: Stop or finish (Default) 1: Start

CRC function = $X^{24} + X^{15} + X^2 + X + 1$.

Address: 2d **OP_CRC_CHECKSUM (Output CRC Checksum)**

Bit	Mode	Function
7:0	R/W	1 st read=> Output CRC-24 bit 23~16 2 nd read=> Output CRC-24 bit 15~8 3 rd read=> Out put CRC-24 bit 7~0

- The read pointer should be reset when 1. OP_CRC_BYTEx is written 2. Output CRC Control starts.
- The read back CRC value address should be auto-increase, the sequence is shown above

FIFO Window

Address: 30 **FIFO_WIN_ADDR (FIFO Window Address Port)**

Bit	Mode	Function
7:5	--	Reserved to 0
4:0	R/W	FIFO Window Address Port

Address: 31 **FIFO_WIN_DATA (FIFO Window Data Port)**

Bit	Mode	Function
7:0	R/W	FIFO Window Data Port

- Port address will increase automatically after read/write.

Address: 31-00 **DRL_H_BSU (Display Read High Byte Before Scaling-Up)** **Default:** 00h

Bit	Mode	Function
7:4	R/W	Display window read width before scaling up: High Byte [11:8]
3:0	R/W	Display window read length before scaling up: High Byte [11:8]

Address: 31-01 **DRW_L_BSU (Display Read Width Low Byte Before Scaling-Up)** **Default:** 00h



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Bit	Mode	Function
7:0	R/W	Display window read width before scaling up: Low Byte [7:0]

Address: 31-02 DRL_L_BSU (Display Read Length Low Byte Before Scaling-Up) Default: 00h

Bit	Mode	Function
7:0	R/W	Display window read length before scaling up: Low Byte [7:0]

- The setting above should be use 2 as unit
- The setting above should be use 2 as unit

Scaling Up Function

Address: 32 SCALE_CTRL (Scale Control Register) Default: 00h

Bit	Mode	Function
7	R/W	Video mode compensation: 0: Disable (Default) 1: Enable
6	R/W	Internal ODD-signal inverse for video-compensation 0: No invert (Default) 1: invert
5	R	Display Line Buffer Ready 0: Busy 1: Ready
4	R/W	Enable Full Line buffer: 0: Disable (Default) 1: Enable
3	R/W	Vertical Line Duplication 0: Disable 1: Enable
2	R/W	Horizontal pixel Duplication 0: Disable 1: Enable
1	R/W	Enable the Vertical Filter Function: 0: By pass the vertical filter function block (Default) 1: Enable the vertical filter function block
0	R/W	Enable the Horizontal Filter Function: 0: By pass the horizontal filter function block (Default) 1: Enable the horizontal filter function block



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- When using H/V duplication mode, FIFO window width set original width, but FIFO window height should be 2X the original height.

Address: 33 SF_ACCESS_Port**Default: 00h**

Bit	Mode	Function
7	R/W	Enable scaling-factor access port
6	R/W	Merge two line buffer to 1 line buffer when scale up (for resolution over line buffer size)
5	R/W	I domain Share display line buffer & display MAC when vertical scale down
4:0	R/W	Scaling factor port address

- When disable scaling factor access port, the access port pointer will reset to 0

Address: 34-00 HOR_SCA_H (Horizontal Scale Factor High)

Bit	Mode	Function
7:4	--	Reserved
3:0	R/W	Bit [19:16] of horizontal scale factor

Address: 34-01 HOR_SCA_M (Horizontal Scale Factor Medium)

Bit	Mode	Function
7:0	R/W	Bit [15:8] of horizontal scale factor

Address: 34-02 HOR_SCA_L (Horizontal Scale Factor Low)

Bit	Mode	Function
7:0	R/W	Bit [7:0] of horizontal scale factor

Address: 34-03 VER_SCA_H (Vertical Scale Factor High)

Bit	Mode	Function
7:4	--	Reserved
3:0	R/W	Bit [19:16] of vertical scale factor

Address: 34-04 VER_SCA_M (Vertical Scale Factor Medium)

Bit	Mode	Function
7:0	R/W	Bit [15:8] of vertical scale factor

Address: 34-05 VER_SCA_L (Vertical Scale Factor Low)

Bit	Mode	Function
7:0	R/W	Bit [7:0] of vertical scale factor

This scale-up factor includes a 20-bit fraction part to present a vertical scaled up size over the stream input. For example, for 600-line original picture scaled up to 768-line, the factor should be as follows:

$$(600/768) \times 2^{20} = 0.78125 \times 2^{20} = 819200 = C8000h = 0Ch, 80h, 00h.$$

Address: 34-06 Horizontal Scale Factor Segment 1 Pixel**Default: 00h**

Bit	Mode	Function
7:3	--	Reserved
2:0	R/W	Bit [10:8] of Scaling Factor Segment 1 pixel



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Address: 34-07 Horizontal Scale Factor Segment 1 Pixel			Default: 00h
Bit	Mode	Function	
7:0	R/W	Bit [7:0] of Scaling Factor Segment 1 pixel	
Address: 34-08 Horizontal Scale Factor Segment 2 Pixel			Default: 00h
Bit	Mode	Function	
7:3	--	Reserved	
2:0	R/W	Bit [10:8] of Scaling Factor Segment 2 pixel	
Address: 34-09 Horizontal Scale Factor Segment 2 Pixel			Default: 00h
Bit	Mode	Function	
7:0	R/W	Bit [7:0] of Scaling Factor Segment 2 pixel	
Address: 34-0A Horizontal Scale Factor Segment 3 Pixel			Default: 00h
Bit	Mode	Function	
7:3	--	Reserved	
2:0	R/W	Bit [10:8] of Scaling Factor Segment 3 pixel	
Address: 34-0B Horizontal Scale Factor Segment 3 Pixel			Default: 00h
Bit	Mode	Function	
7:0	R/W	Bit [7:0] of Scaling Factor Segment 3 pixel	
Address: 34-0C Horizontal Scale Factor Delta 1			Default: 00h
Bit	Mode	Function	
7:5	--	Reserved	
4:0	R/W	Bit [12:8] of Horizontal Scale Factor delta 1	
Address: 34-0D Horizontal Scale Factor Delta 1			Default: 00h
Bit	Mode	Function	
7:0	R/W	Bit [7:0] of Horizontal Scale Factor delta 1	
Address: 34-0E Horizontal Scale Factor Delta 2			Default: 00h
Bit	Mode	Function	
7:5	--	Reserved	
4:0	R/W	Bit [12:8] of Horizontal Scale Factor delta 2	
Address: 34-0F Horizontal Scale Factor Delta 2			Default: 00h
Bit	Mode	Function	
7:0	R/W	Bit [7:0] of Horizontal Scale Factor delta 2	
Address: 34-10 Horizontal Filter Coefficient Initial Value			Default: C4h
Bit	Mode	Function	
7:0	R/W	Accumulate Horizontal filter coefficient initial value	
Address: 34-11 Vertical Filter Coefficient Initial Value			Default: C4h



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Bit	Mode	Function
7:0	R/W	Accumulate Vertical filter coefficient initial value

Address: 35 FILTER_CTRL (Filter Control Register) Default: 00h

Bit	Mode	Function
7	R/W	Enable Filter Coefficient Access 0: Disable (Default) 1: Enable
6	R/W	Select H/V User Defined Filter Coefficient Table for Access Channel 0: 1 st coefficient table (Default) 1: 2 nd coefficient table
5	R/W	Select Horizontal user defined filter coefficient table 0: 1 st Horizontal Coefficient Table (Default) 1: 2 nd Horizontal Coefficient Table
4	R/W	Select Vertical user defined filter coefficient table 0: 1st Vertical Coefficient Table (Default) 1: 2 nd Vertical Coefficient Table
3:0	---	Reserved to 0

- The User Defined Filter Coefficient Table can be modified on-line. Only the non-active coefficient-table can be modified, and then switch it to active.

Address: 36 FILTER_PORT (User Defined Filter Access Port) Default: 00h

Bit	Mode	Function
7:0	W	Access port for user defined filter coefficient table

- When enable filter coefficient accessing, the first write byte is stored into the LSB(bit[7:0]) of coefficient #1 and the second byte is into MSB (bit[8:11]). Therefore, the valid write sequence for this table is c0-LSB, c0-MSB, c1-LSB, c1-MSB, c2-LSB, c2-MSB ... c63-LSB & c63-MSB, totally 64 * 2 cycles. Since the 128 taps is symmetric, we need to fill the 64-coefficient sequence into table only.

Address: 37~3F Reserved

Frame Sync Fine Tune

Address: 40 IVS2DVS_DELAY_LINES (IVS to DVS Lines) Default: 00h

Bit	Mode	Function
7:0	R/W	IVS to DVS Lines: (Only for FrameSync Mode) The number of input HS from IVS to DVS. Should be double buffer by CR10[5:4]

Address: 41 IV_DV_DELAY_CLK_ODD (Frame Sync Delay Fine Tuning) Default: 00h

Bit	Mode	Function



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7:0	R/W	Frame Sync Mode Delay Fine Tune [7:0] Applied to all fields when Interlaced_FS_Delay_Fine_Tuning is disabled (CR43[1] = 0) Only for odd-field when Interlaced_FS_Delay_Fine_Tuning is enabled (CR43[1] = 1)
-----	-----	--

In Frame Sync Mode , CR41[7:0] represents output VS delay fine-tuning. It delays the number of (CR41 [7:0] *16 + 16) input clocks if CR41[7:0] is not equal to 0. (No delay fine-tune if CR41[7:0] = 0)

Address: 42 IV_DV_DELAY_CLK_EVEN (Frame Sync Delay Fine Tuning) Default: 00h

Bit	Mode	Function
7:0	R/W	Frame Sync Mode Delay Fine Tune [7:0] “00” to disable Only for even-field when Interlaced_FS_Delay_Fine_Tuning is enabled (CR43[1] = 1)

Address: 43 FS_DELAY_FINE_TUNING Default: 00h

Bit	Mode	Function
7	R/W	Enable measure last line by field 0 : disable 1: enable
6	R/W	Reference field in last line measure 0 : Odd 1 : Even
5:2	R/W	Reserved to 0
1	R/W	Interlaced_FS_Delay_Fine_Tuning 0: Disable (Default) 1: Enable
0	R/W	Internal ODD-signal inverse for Interlaced_FS_Delay_Fine_Tuning 0: No invert (Default) 1: Invert

Address: 44 LAST_LINE_H Default: 00h

Bit	Mode	Function
7	R/W	Last-line-width / DV-Total Selector : 0: CR44 [3:0] and CR45 indicate last-line width counted by display clock (Default) 1: CR44 [3:0] and CR45 indicate DHS total number between 2 DVS.
6	R/W	DV sync with 4X clock 0: Disable 1: Enable
5	R/W	BIST Test Enable 0: Disable 1: Enable (Auto clear when finish)



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4	R/W	BIST Test Result 0: Fail 1: Ok
3:0	R	DV Total or Last Line Width[11:8] Before Sync in Frame Sync Mode

Address: 45 LAST_LINE_L

Bit	Mode	Function
7:0	R	DV Total or Last Line Width[7:0] Before Sync in Frame Sync Mode

Address: 46 Reserved as page selector for new sync-processor feature

Sync Processor

Address: 47 SYNC_SELECT Default: 00h

Bit	Mode	Function
7	R/W	On line Sync Processor Power Down (Stop Crystal Clock In) 0: Normal Run (Default) 1: Power Down
6	R/W	Hsync Type Detection Auto Run 0: manual (Default) 1: automatic
5	R/W	De-composite circuit enable 0: Disable (Default) 1: Enable
4	R/W	Input Sync. Source selection 0: HS_RAW(SS/CS) (Default) 1: SOG/SOY
3	R/W	SOG Source Selection 0: SOG0/SOY0 (Default) 1: SOG1/SOY1 (Useless)
2	R/W	VGA-ADC HS/VS Source 0: 1 ST HS/VS (Default) (Original HS/VS of ADC source) 1: 2 ND HS/VS (HS/VS from D domain)
1	R/W	Measured by Crystal Clock (Result shown in CR59) (in Digital Mode) 0: Input Active Region (Vertical IDEN start to IDEN stop) (measure at IDEN STOP) (Default) 1: Display Active Region(Vertical DEN start to DEN stop) (measure at DEN STOP) The function should work correctly when IVS or DVS occurs and enable by CR50[4].
0	R/W	Hsync & Vsync Measured Mode 0: HS period counted by crystal clock & VS period counted by HS (Analog mode) (Default) 1: H resolution counted by input clock & V resolution counted by ENA (Digital mode)



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		(Get the correct resolution which is triggered by enable signal, ENA)
--	--	---

Address: 48 SYNC_INVERT Default: 00h

Bit	Mode	Function
7	R/W	COAST Signal Invert Enable: 0: Not inverted (Default) 1: Inverted
6	R/W	COAST Signal Output Enable: 0: Disable (Default) 1: Enable
5	R/W	HS_OUT Signal Invert Enable: 0: Not inverted (Default) 1: Inverted
4	R/W	HS_OUT Signal Output Enable: 0: Disable (Default) 1: Enable
3	R/W	CS_RAW Inverted Enable 0: Normal (Default) 1: Invert
2	R/W	CLAMP Signal Output Enable 0: Disable (Default) 1: Enable
1	R/W	HS Recovery in Coast 0: Disable (Default) (SS/SOY) 1: Enable (CS or SOG)
0	R/W	Hsync Synchronize source 0: AHS (Default) 1: Feedback HS

Address: 49 SYNC_CTRL (SYNC Control Register) Default: 00h

Bit	Mode	Function
7	R/W	CLK Inversion to latch Feedback HS for Coast Recovery (Coast Recovery means HS feedback to replace input HS) 0: Non Inversion (Default) 1: Inversion
6	R/W	Select HS_OUT Source Signal 0: Bypass (SeHs)(Use in Separate Mode) 1: Select De-Composite HS out(DeHs) (In Composite mode)
5	R/W	Select ADC_VS Source Signal (Auto switch in Auto Run Mode)



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		0: VS_RAW 1: DeVs
4	R/W	CLK Inversion to latch ADC HS for Clamp 0: Non Inversion (Default) 1: Inversion
3	R/W	Inversion of HSYNC to measure VSYNC 0: Non Inversion (Default) 1: Inversion
2	R/W	HSYNC Measure Source(ADC_HS1) 0: Select ADC_HS(Default) 1: Select SeHS or DeHS by CR49[6]
1:0	R/W	Measure HSYNC/VSYNC Source Select: 00: TMDS (Default) 01: VIDEO8 10: ADC_HS1/ADC_VS 11: CS_RAW/VS_RAW

Address: 4A

STABLE_HIGH_PERIOD_H

Default: 00h

Bit	Mode	Function
7	R	Even/Odd Field of YPbPr (By Line-Count Mode) 0: Even 1: Odd
6	R	The Toggling of Polarity of YPbPr Field Happened (By Line-Count Mode) 0: No toggle 1: Toggle
5	R	Even/Odd Field of YPbPr (By VS-Position Mode) 0: Even 1: Odd
4	R	The Toggling of Polarity of YPbPr Field Happened (By VS-Position Mode) 0: No toggle 1: Toggle
3	R/W	Odd Detection Mode 0: Line-Count Mode (Default) 1: VS-Position Mode
2:0	R	Stable High Period[10:8] Compare each line's high pulse period, if we get continuous 64 lines with the same one, the period is updated as the stable period.

Address: 4B

STABLE_HIGH_PERIOD_L



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Bit	Mode	Function
7:0	R	Stable High Period[7:0] Compare each line's high pulse period, if we get continuous 64 lines with the same one, the period is updated as the stable period.

Address: 4C

VSYNC_COUNTER_LEVEL_MSB

Default: 03h

Bit	Mode	Function
7	R	Hsync Type Detection Auto Run Result ready
6:4	R	Hsync Type Detection Auto Run Result 000: No Signal 001: Not Support 010: YPbPr 011: Serration Composite SYNC 100: XOR/OR-Type Composite SYNC with Equalizer 101: XOR/OR-Type Composite SYNC without Equalizer 110: HSync with VS_RAW (Separate HSync) 111: HSync without VS_RAW (HSync only) Reference when Hsync type detection auto run result ready (CR4C[7])
3	R/W	Reserved to 0
2:0	R/W	VSYNC counter level count [10:8] MSB VSYNC detection counter start value.

Address: 4D

VSYNC_COUNTER_LEVEL_LSB

Default: 00h

Bit	Mode	Function
7:0	R/W	VSYNC counter level count [7:0] LSB

Address: 4E

Hsync_Type_Detection_Flag

Bit	Mode	Function
7	R	Hsync Overflow (16-bits)
6	R	Stable Period Change (write clear when CR4E[6]=1 or CR4F[0]=1)
5	R	Stable Polarity Change (write clear when CR4E[5]=1 or CR4F[0]=1)
4	R	VS_RAW Edge Occurs (write clear when CR4E[4]=1 or CR4F[0]=1) If VS_RAW edge occurs, this bit is set to "1".
3	R	Detect Capture Window Unlock Repeated 32 Times (write clear when CR4E[3]=1 or CR4F[0]=1)
2	R	Hsync with Equalization (write clear when CR4E[2]=1 or CR4F[0]=1)
1	R	Hsync Polarity Change (write clear when CR4E[1]=1 or CR4F[0]=1)
0	R	Detect Capture Window Unlock (write clear when CR4E[0]=1 or CR4F[0]=1)

Address: 4F

STABLE_MEASURE

Default: 00h

Bit	Mode	Function



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7	R	Stable Flag 0: Period or polarity can't get continuous stable status. 1: Both polarity and period are stable.
6	R	Stable Polarity 0: Negative 1: Positive Compare each line's polarity; if we get continuous ≥ 64 lines with the same one, the polarity is updated as the stable polarity.
5:4	R/W	Feedback HSYNC High Period Select by ADC Clock: 00: 32 (Default) 01: 64 10: 96 11: 128
3	R/W	Stable Period Tolerance 0: ± 2 crystal clks (Default) 1: ± 4 crystal clks
2	R/W	VSYNC measure invert Enable 0: Disable (Default) 1: Enable
1	R/W	Pop Up Stable Value 0: No Pop Up (Default) 1: Pop Up Result, (CR4A[2:0], CR4B[7:0], CR4F[6], CR50[2:0], CR51[7:0])
0	R/W	Stable Measure Start 0 : Stop (Default) 1 : Start

Address: 50

Stable_Period_H

Default: 00h

Bit	Mode	Function
7	R	Measure One Frame Status 0: Finished after 1 frame measuring / Measure finished 1: Measuring Now
6	R	CS_RAW Inverted by Auto Run Mode 0: Not inverted 1: Inverted
5	R/W	HS_OUT Bypass PLL into VGIP 0: Disable (Default) 1: Enable
4	R/W	Active Region Measure Enable



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		0: Disable (Default) 1: Enable
3	R/W	ADC_VS Source Select in Test Mode 0: Select ADC_VS Source in Normal Mode or Auto Mode by CR47[6] (Default) 1: Select ADC_VS Source in Test Mode (Select VS_RAW or DeVS by CR49[5])
2:0	R	Stable Period[10:8] Compare each line's period, if we get continuous 64 lines with the same one, the period is updated as the stable period.

Address: 51 Stable_Period_L

Bit	Mode	Function
7:0	R	Stable Period[7:0] Compare each line's period, if we get continuous 64 lines with the same one, the period is updated as the stable period.

Address: 52 MEAS_HS_PER_H (HSYNC Period Measured Result) Default: 8'b000xxxxx

Bit	Mode	Function
7	R/W	Auto Measure Enable 0: Disable (Default) 1: Enable
6	R/W	Pop Up Period Measurement Result 0: No Pop Up (Default) 1: Pop Up Result
5	R/W	Start a HS & VS period / H & V resolution & polarity measurement (on line monitor) 0: Finished/Disable (Default) 1: Enable to start a measurement, auto cleared after finished
4	R	Over-flow bit of Input HSYNC Period Measurement 0: No Over-flow occurred 1: Over-flow occurred
3:0	R	Input HSYNC Period Measurement Result: High Byte[11:8]

Address: 53 MEAS_HS_PER_L (HSYNC Period Measured Result)

Bit	Mode	Function
7:0	R	Input HSYNC Period Measurement Result: Low Byte[7:0]

- The result is expressed as the average number of crystal clocks (CR47[0]=0), or input clocks (CR47[0]=1) between 2 HSYNC.
- The result is the total number of crystal/input clocks inside 16-HSYNC periods divided by 16.
- Fractional part of measure result is stored in CR56[3:0].

Address: 54 MEAS_VS_PER_H (VSYNC Period Measured Result)

Bit	Mode	Function



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7	R	Input VSYNC Polarity Indicator 0: negative polarity (high period is longer than low one) 1: positive polarity (low period is longer than high one)
6	R	Input HSYNC Polarity Indicator 0: negative polarity (high period is longer than low one) 1: positive polarity (low period is longer than high one)
5	R	Time-Out bit of Input VSYNC Period Measurement (No VSYNC occurred) 0: No Time Out 1: Time Out occurred (512 time_clk ref CR5D-18[7:6])
4	R	Over-flow bit of Input VSYNC Period Measurement 0: No Over-flow occurred 1: Over-flow occurred
3:0	R	Input VSYNC Period Measurement Result: High Byte[11:8]

Address: 55 MEAS_VS_PER_L (VSYNC Period Measured Result)

Bit	Mode	Function
7:0	R	Input VSYNC Period Measurement Result: Low Byte[7:0]

- This result is expressed in terms of input HS pulses.
- When measured digitally, the result is expressed as the number of input ENA signal within a frame.

Address: 56 MEAS_HS&VS_HI_H (HSYNC&VSYNC High Period Measured Result)

Bit	Mode	Function
7:4	R	Input HSYNC High Period Measurement Result: High Byte[11:8] (CR58[0] = 0) Input VSYNC High Period Measurement Result: High Byte[11:8] (CR58[0] = 1)
3:0	R	Input HSYNC Period Measurement Fractional Result (See CR52,53)

Address: 57 MEAS_HS&VS_HI_L (HSYNC&VSYNC High Period Measured Result)

Bit	Mode	Function
7:0	R	Input HSYNC High Period Measurement Result: Low Byte[7:0] (CR58[0] = 0) Input VSYNC High Period Measurement Result: Low Byte[7:0] (CR58[0] = 1)

- This result of HSYNC high-period is expressed in terms of crystal clocks. When measured digitally, the result of HSYNC high-period is expressed as the number of input clocks inside the input enable signal.
- This result of VSYNC high-period is expressed in terms of input HS pulses

Address: 58 MEAS_HS&VS_HI_SEL (VSYNC High Period Measured Result) Default:00h

Bit	Mode	Function
7:6	R/W	HSYNC_MAX_DELTA 00: Don't care (CR58[3] will never go high) 01: 4-clock 10: 8-clock 11: 16-clock



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5:4	R/W	VSYNC_MAX_DELTA 00: Don't care (CR58[2] will never go high) 01: 2-HSYNC 10: 4-HSYNC 11: 8-HSYNC
3	R	HSYNC_OVER_RANGE Set to 1 if variation of HSYNC larger than VSYNC_MAX_DELTA is detected by on-line measurement (CR52[7]=1). Write to clear this flag.
2	R	VSYNC_OVER_RANGE Set to 1 if variation of VSYNC larger than VSYNC_MAX_DELTA is detected by on-line measurement (CR52[7]=1). Write to clear this flag.
1	R/W	Start Measurement after Mode Detection Auto-mode 0: Disable (Default) 1: Enable
0	R/W	HSYNC/VSYNC High Period Measurement Result Select 0: HSYNC 1: VSYNC (See CR56~CR57)

Address: 59 MEAS_ACTIVE_REGION_H (Active Region Measured by CRSTL_CLK Result)

Bit	Mode	Function
7:0	R/W	Active Region Measured By Crystal Clock 1st read: Measurement Result: High Byte[23:16] 2nd read: Measurement Result: High Byte[15:8] 3rd read: Measurement Result: High Byte[8:0] Read pointer is auto increase, if write, the pointer is also reset to 1 st result.

Address: 5A SYNC_TEST_MISC

Default: 00h

Bit	Mode	Function
7	R/W	Clamp Reference Source Selection 0: Clamp source from normal HS 1: Clamp source from CS_RAW
6	R/W	HS/ENA source swap for measurement 0: HS for analog mode, ENA for digital mode 1: HS for digital mode, ENA for analog mode
5:4	R/W	Active Region Measurement Option 00: Active Data Region (first ENA rising to last ENA falling) 01: Whole Frame (VS rising to VS rising) 10: Back Porch (VS rising to first EAN rising) 11: Front Porch (last ENA falling to VS Rising)



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		Sync Processor Test Signals Output Selection ===> 5D-18 Bit0_2
3	R/W	vs/vs_org select option 0: vs/vs_org (vs generated by down counter during decomposite progress) 1: vs_raw/vs_raw
2:0	R	The Number of Input HS between 2 Input VSYNC. LSB bit [2:0] for YPbPr

Address: 5B HS_DETECT**Default: 00h**

Bit	Mode	Function
7	R/W	HS detected flag, write clear. 0: no detect result 1: HS detected. (enable by CR5D-19[7])
6	R/W	SOG detected flag, write clear. 0: no detect result 1: SOG detected. (enable by CR5D-19[6])
5:0	R/W	Reserved to 0

Address: 5C SYNC_PROC_PORT_ADDR**Default: 00h**

Bit	Mode	Function
7:5	R/W	Reserved
4:0	R/W	Sync Processor Access Port Address

Address: 5D SYNC_PROC_PORT_DATA**Default: 00h**

Bit	Mode	Function
7:0	R/W	Sync Processor Access Port Data

- Port address will increase automatically after read/write.

Address: 5D-00 G_CLAMP_START (Clamp Signal Output Start)**Default: 04h**

Bit	Mode	Function
7:0	R/W	Start of Output Clamp Signal Pulse for Y/G Channel[7:0]: Determine the number of input double-pixel between the trailing edge of input HSYNC and the start of the output CLAMP signal.

Address: 5D-01 G_CLAMP_END (Clamp Signal Output End)**Default: 10h**

Bit	Mode	Function
7:0	R/W	End of Output Clamp Signal Pulse for Y/G Channel [7:0]: Determine the number of input double-pixel between the trailing edge of input



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		HSYNC and the end of the output CLAMP signal.
--	--	---

Address: 5D-02 BR_CLAMP_START (Clamp Signal Output Start) **Default: 04h**

Bit	Mode	Function
7:0	R/W	Start of Output Clamp Signal Pulse for B/Pb and R/Pr Channel [7:0]: Determine the number of input double-pixel between the trailing edge of input HSYNC and the start of the output CLAMP signal.

Address: 5D-03 BR_CLAMP_END (Clamp Signal Output End) **Default: 10h**

Bit	Mode	Function
7:0	R/W	End of Output Clamp Signal Pulse for B/Pb and R/Pr Channel [7:0]: Determine the number of input double-pixel between the trailing edge of input HSYNC and the end of the output CLAMP signal.

Address: 5D-04 CLAMP_CTRL0 **Default: 00h**

Bit	Mode	Function
7	R/W	Clamp Trigger Edge Inverse for Y/G Channel 0: Trailing edge (Default) 1: Leading edge
6	R/W	Clamp Trigger Edge Inverse for B/Pb and R/Pr Channel 0: Trailing edge (Default) 1: Leading edge
5:0	R/W	Mask Line Number before DeVS [5:0]

Address: 5D-05 CLAMP_CTRL1 **Default: 00h**

Bit	Mode	Function
7	R/W	Clamp Mask Enable 0: Disable (Default) 1: Enable
6	R/W	Select Clamp Mask as De VS 0: Disable 1: Enable
5:0	R/W	Mask Line Number after DeVS [5:0]

CR5D-04[5:0] and CR5D-05[5:0] will set number of Mask Line before/after DeVS for Clamp Mask.

Address: 5D-06 CLAMP_CTRL2 **Default: 00h**

Bit	Mode	Function
7	R/W	Clamp Clock Source 0: ADC_Clock (Default) 1: Crystal Clock
6	R/W	Clamp Counter Unit (0x5D-00 – 0x5D-03)



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		0: Double Pixels (Default) 1: Single Pixel
5	R/W	ADC1_clamp_enable 0: Disable (Default) 1: Enable (useless, because there is no ADC1)
4	R/W	ADC0_clamp_enable 0: Disable (Default) 1: Enable
3	R/W	ADC-3 Clamp Source 0: Clamp-G (Default) 1: Clamp-BR
2	R/W	ADC-2 Clamp Source 0: Clamp-G (Default) 1: Clamp-BR
1	R/W	ADC-1 Clamp Source 0: Clamp-G (Default) 1: Clamp-BR
0	R/W	ADC-0 Clamp Source 0: Clamp-G (Default) 1: Clamp-BR

Address: 5D-07 COAST_CTRL Default: 21h

Bit	Mode	Function
7:4	R/W	Start of COAST before DeVS Leading Edge [3:0]
3:0	R/W	End of COAST after DeVS Trailing Edge [3:0]

Address: 5D-08 CAPTURE_WINDOW_SETTING Default: 04h

Bit	Mode	Function
7	R/W	Coast_sel 0: de_coast (Default) 1: coast_org
6	R/W	Capture Miss Limit during Hsync Extraction 0: 32 (Default) 1: 16
5	R/W	Capture Window add step as Miss Lock 0: ± 1 crystal clks (Default) 1: ± 2 crystal clks
4:0	R/W	Capture Window Tolerance 5'h00: ± 6 crystal clks for capture window 5'h01 ~ 5'b1F : $\pm 1 \sim \pm 31$ crystal clks for capture window



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Address: 5D-09 DETECTION_TOLERANCE_SETTING**Default: 04h**

Bit	Mode	Function
7	R/W	Reserved to 0
6:5	R/W	Stable Period Tolerance Extension 00: Use 0x4F[3] Setting (Default) 01: ±4 crystal clks 10: ±8 crystal clks 11: ±16 crystal clks
4:0	R/W	H-sync for De-composite De-bounce Length 5'h00: Disable De-bounce Function 5'h01 ~ 5'h1F : De-bounce 1 ~ 31 crystal clks for de-composite

Address: 5D-0A DEVS_CAP_NUM_H**Default: 00h**

Bit	Mode	Function
7:4	--	Reserved to 0
3:0	R	The munber of Capture window between DeVs high period: High Byte[11:8]

Address: 5D-0B DEVS_CAP_NUM_L**Default: 00h**

Bit	Mode	Function
7:0	R	The munber of Capture window between DeVs high period: High Byte[7:0]

Address: 5D-0C~0F Reserved

Macro Vision

Address: 5D-10 MacroVision Control**Default: 00h**

Bit	Mode	Function
7:4	R/W	Skip Line[3:0] Skip Lines after Vsync detected
3:2	R/W	Reserved to 0
1	R	MacroVision Detected (On-line monitor) When detected Macrovision occurred, this bit set to 1, else clear to 0.
0	R/W	MacroVision Enable 0: Disable (Default) 1: Enable

Address: 5D-11 MacroVision Start Line in Even Field

Bit	Mode	Function
7	R/W	Reserved to 0
6:0	R	MacroVision Start Line in Even Field [6:0]

Address: 5D-12 MacroVision End Line in Even Field

Bit	Mode	Function
7	R	Indicate the validity of Macro Vision Line in Even Field



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		0: not valid 1: valid
6:0	R	MacroVision End Line 0 [6:0]

Address: 5D-13 MacroVision Start Line in Odd Field

Bit	Mode	Function
7	R/W	Reserved to 0
6:0	R	MacroVision Start Line in Odd Field [6:0]

Address: 5D-14 MacroVision End Line in Odd Field

Bit	Mode	Function
7	R	Indicate the validity of Macro Vision Line in Odd Field 0: not valid 1: valid
6:0	R	MacroVision End Line in Odd Field [6:0]

Address: 5D-15 Macro Vision Detect De-bounce **Default: 00h**

Bit	Mode	Function
7:5	R/W	Reserved to 0
4:0	R/W	H-sync for Macro-Vision Detection De-bounce Length 5'h00 ~ 5'h07: De-bounce 7 crystal clks for de-composite (Default) 5'h08 ~ 5'h1F: De-bounce 8 ~ 31 crystal clks for de-composite

Address: 5D-16~17 Reserved**Address: 5D-18 Sync Processor Test Mode** **Default: 00h**

Bit	Mode	Function
7	R/W	Sync Processor Time-Clock Test Mode 0: Normal (Default) ((time_clk ref CR5D-18[6])) 1: Enable Test Mode; (switch xclk -ck to the time-out & polarity counters)
6	R/W	Time Clock Select 0: 2048 xclk (Default) 1: 4096 xclk
5	R	Half Time-Out bit of Input VSYNC Period Measurement 0: No Half Time Out 1: Half Time Out occurred (256 time_clk ref CR5D-18[7:6])
4	R/W	Stable Pulse Width Ignore 0: consider pulse width when stable comparing 1: ignore pulse width when stable comparing
3	R/W	select adc measure hs source



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		0: DeHS (default) 1: from capture window
2:0	R/W	<p>Sync Processor Test Signals Output Selection</p> <p>000: Disable On-line Sync-Processor Test-Signal Output (Default)</p> <p>001: adc_vs, adc_hs, adc_field, sog, vs_raw, cs_raw, hs_out, coast</p> <p>010: cs_hs, hs_yprpb_postiv, input_signal_be_inverted, search_finish, load_search_stable48_result, load_finish_stable48_result, cap_hit, cap_miss</p> <p>011: cs_hs, cap_window, de_hs, de_vs, de_coast, clamp_mask, cap_hit, cap_miss</p> <p>100: cs_raw, hs_for_decmp, auto_det_rdy, auto_result_rdy, flg_cnt_is50ms, flg_cnt_is80ms, hs_for_mv, mv_occur</p> <p>101: mode_det_of, stb_per_chg, stb_pol_chg, vs_raw_vld, cap_32unlock, eq_occur, hs_pol_chg, cap_unlock</p> <p>110: vs1_meas, hs1_meas, meas_clk, ms_now, reg_ms_1_frame_now, hsper_of, vsper_of, ms_timeout</p> <p>111: adc_vs, clamp_mask, hs_clamp_g, hs_clamp_rb, vga_online_clamp3, vga_online_clamp2, vga online clamp1, vga online clamp0</p>

Address: 5D-19 HS_DETECT_SETTING**Default: 00h**

Bit	Mode	Function
7	R/W	<p>HS detection enable</p> <p>0: disable HS detection 1: enable HS detection</p>
6	R/W	<p>SOG detection enable</p> <p>0: disable SOG detection 1: enable SOG detection</p>
5	R/W	<p>Interrupt enable</p> <p>0: disable interrupt 1: enable interrupt</p>
4:0	R/W	<p>HS/SOG detection debounce number.</p> <p>0: no debounce 1~31: debounced by crystal clock/IOSC for 1~31 cycles</p>

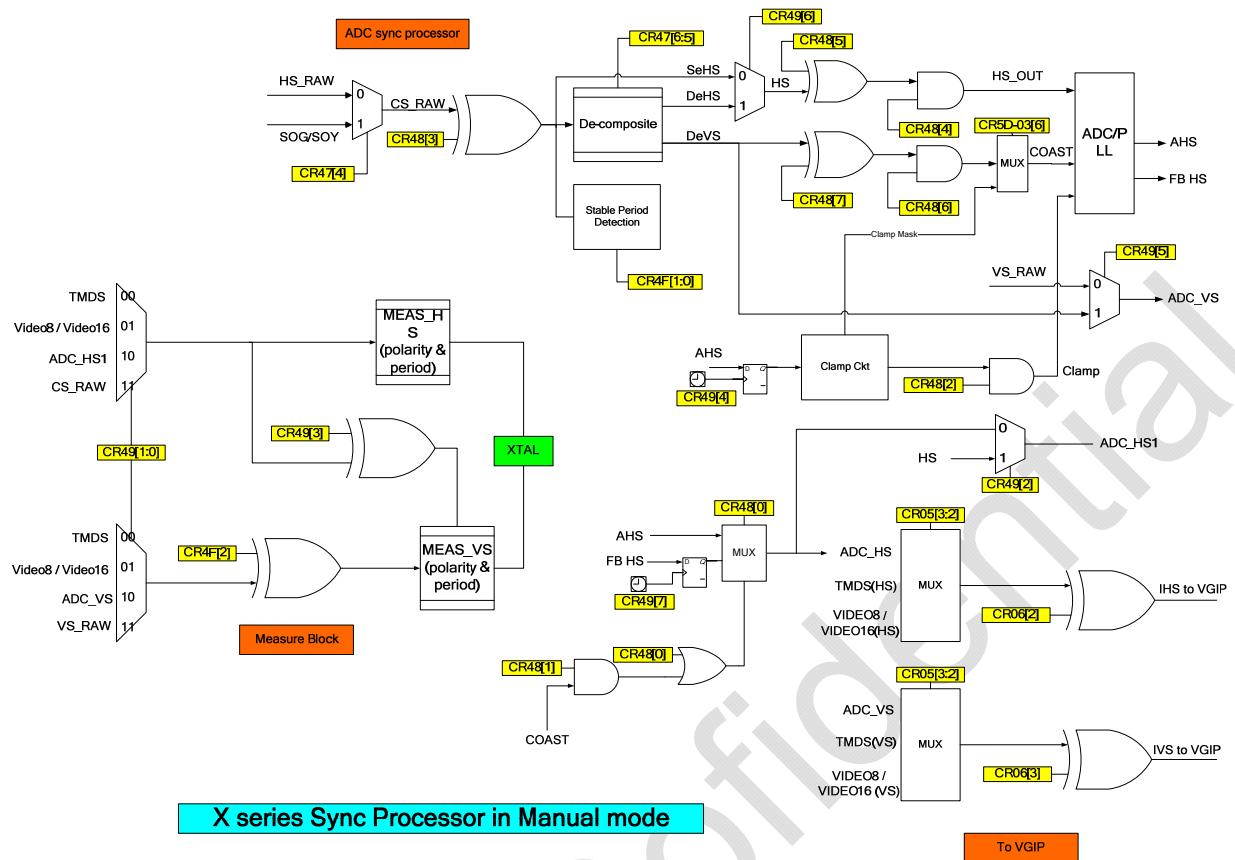
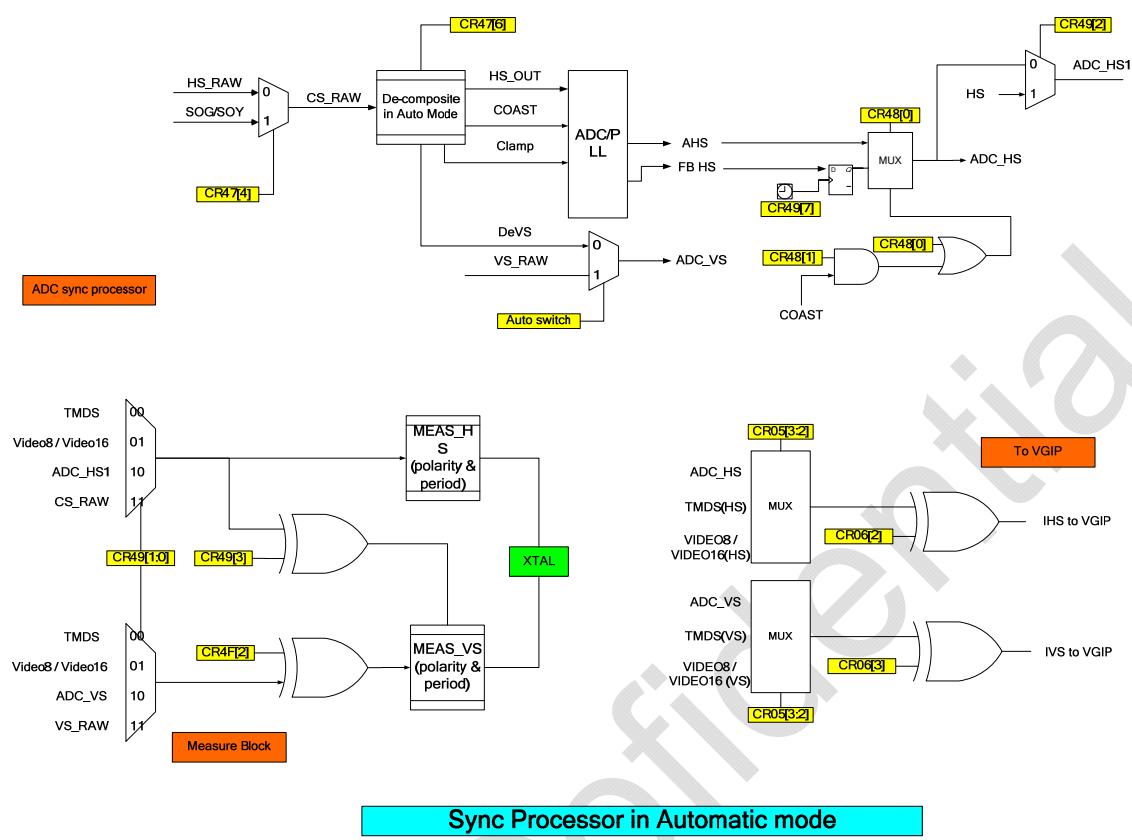


Figure 16: Sync processor



Sync processor in Automatic mode

Address 0x5E is reserved

Highlight window

Address: 60 Highlight Window Access Port control

Default: 00h

Bit	Mode	Function
7	R/W	Enable highlight window access port
6	R/W	Enable highlight window
5:4	--	Reserved
3:0	R/W	Highlight-window port address

Address: 61-00 Highlight Window Horizontal Start

Bit	Mode	Function
7:4	--	Reserved
3:0	R/W	Highlight window horizontal start[11:8]

Address: 61-01 Highlight Window Horizontal Start

Bit	Mode	Function



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7:0	R/W	Highlight window horizontal start[7:0]
-----	-----	---

Address: 61-02 Highlight Window Horizontal End

Bit	Mode	Function
7:4	--	Reserved
3:0	R/W	Highlight window horizontal end[11:8]

Address: 61-03 Highlight Window Horizontal End

Bit	Mode	Function
7:0	R/W	Highlight window horizontal end[7:0]

Address: 61-04 Highlight Window Vertical Start

Bit	Mode	Function
7:4	--	Reserved
3:0	R/W	Highlight window vertical start[11:8]

Address: 61-05 Highlight Window Vertical Start

Bit	Mode	Function
7:0	R/W	Highlight window vertical start[7:0]

Address: 61-06 Highlight Window Vertical End

Bit	Mode	Function
7:4	--	Reserved
3:0	R/W	Highlight window vertical end[11:8]

Address: 61-07 Highlight Window Vertical End

Bit	Mode	Function
7:0	R/W	Highlight window vertical end[7:0]

Highlight window horizontal/vertical reference point is DEN (display background start).

Address: 61-08 Highlight Window Border

Bit	Mode	Function
7:4	--	Reserved
3:0	R/W	Highlight window border width

Address: 61-09 Highlight Window Border Color

Bit	Mode	Function
7:6	--	Reserved
5:0	R/W	Highlight window border red color MSB 6bit (red color 2-bit LSB = 00)

Address: 61-0A Highlight Window Border Color

Bit	Mode	Function
7:6	--	Reserved
5:0	R/W	Highlight window border green color MSB 6bit (green color 2-bit LSB = 00)

Address: 61-0B Highlight Window Border Color



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Bit	Mode	Function
7:6	--	Reserved
5:0	R/W	Highlight window border blue color MSB 6bit (blue color 2-bit LSB = 00)

Address: 61-0C **Highlight Window Control 0** **Default : 00h**

Bit	Mode	Function																																																
7:6	R/W	<p>Contrast / brightness application control</p> <p>00: Set A used on full region 01: Set B used inside highlight window 10: Set A used outside highlight window 11: Set A used outside highlight window, and Set B used inside highlight window</p> <table border="1"> <thead> <tr> <th>Contrast (CR62[1])</th> <th>Application control</th> <th>Inside window</th> <th>Outside window</th> </tr> </thead> <tbody> <tr> <td>0</td> <td>X</td> <td>bypass</td> <td>bypass</td> </tr> <tr> <td>1</td> <td>CR61-0C[7:6]=00 CR60[6]=0</td> <td>Set A</td> <td>Set A</td> </tr> <tr> <td>1</td> <td>CR61-0C[7:6]=01 && CR60[6]=1</td> <td>Set B</td> <td>bypass</td> </tr> <tr> <td>1</td> <td>CR61-0C[7:6]=10 && CR60[6]=1</td> <td>bypass</td> <td>Set A</td> </tr> <tr> <td>1</td> <td>CR61-0C[7:6]=11 && CR60[6]=1</td> <td>Set B</td> <td>Set A</td> </tr> </tbody> </table> <table border="1"> <thead> <tr> <th>Brightness (CR62[0])</th> <th>Application control</th> <th>Inside window</th> <th>Outside window</th> </tr> </thead> <tbody> <tr> <td>0</td> <td>X</td> <td>bypass</td> <td>bypass</td> </tr> <tr> <td>1</td> <td>CR61-0C[7:6]=00 CR60[6]=0</td> <td>Set A</td> <td>Set A</td> </tr> <tr> <td>1</td> <td>CR61-0C[7:6]=01 && CR60[6]=1</td> <td>Set B</td> <td>bypass</td> </tr> <tr> <td>1</td> <td>CR61-0C[7:6]=10 && CR60[6]=1</td> <td>bypass</td> <td>Set A</td> </tr> <tr> <td>1</td> <td>CR61-0C[7:6]=11 && CR60[6]=1</td> <td>Set B</td> <td>Set A</td> </tr> </tbody> </table>	Contrast (CR62[1])	Application control	Inside window	Outside window	0	X	bypass	bypass	1	CR61-0C[7:6]=00 CR60[6]=0	Set A	Set A	1	CR61-0C[7:6]=01 && CR60[6]=1	Set B	bypass	1	CR61-0C[7:6]=10 && CR60[6]=1	bypass	Set A	1	CR61-0C[7:6]=11 && CR60[6]=1	Set B	Set A	Brightness (CR62[0])	Application control	Inside window	Outside window	0	X	bypass	bypass	1	CR61-0C[7:6]=00 CR60[6]=0	Set A	Set A	1	CR61-0C[7:6]=01 && CR60[6]=1	Set B	bypass	1	CR61-0C[7:6]=10 && CR60[6]=1	bypass	Set A	1	CR61-0C[7:6]=11 && CR60[6]=1	Set B	Set A
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		1	CR61-0C[5:4]=10 && CR60[6]=1	bypass	Gamma																																									
3:2	R/W	DCC/ICM application control 00: DCC/ICM used on full region 01: DCC/ICM used inside window 10: DCC/ICM used outside window 11: Reserved	<table border="1"> <thead> <tr> <th>ICM (CRD0[7])</th> <th>Application control</th> <th>Inside window</th> <th>Outside window</th> </tr> </thead> <tbody> <tr> <td>0</td> <td>X</td> <td>bypass</td> <td>bypass</td> </tr> <tr> <td>1</td> <td>CR61-0C[3:2]=00 CR60[6]=0</td> <td>ICM</td> <td>ICM</td> </tr> <tr> <td>1</td> <td>CR61-0C[3:2]=01 && CR60[6]=1</td> <td>ICM</td> <td>bypass</td> </tr> <tr> <td>1</td> <td>CR61-0C[3:2]=10 && CR60[6]=1</td> <td>bypass</td> <td>ICM</td> </tr> </tbody> </table> <table border="1"> <thead> <tr> <th>DCC (CRC7[7])</th> <th>Application control</th> <th>Inside window</th> <th>Outside window</th> </tr> </thead> <tbody> <tr> <td>0</td> <td>X</td> <td>bypass</td> <td>bypass</td> </tr> <tr> <td>1</td> <td>CR61-0C[3:2]=00 CR60[6]=0</td> <td>DCC</td> <td>DCC</td> </tr> <tr> <td>1</td> <td>CR61-0C[3:2]=01 && CR60[6]=1</td> <td>DCC</td> <td>bypass</td> </tr> <tr> <td>1</td> <td>CR61-0C[3:2]=10 && CR60[6]=1</td> <td>bypass</td> <td>DCC</td> </tr> </tbody> </table>	ICM (CRD0[7])	Application control	Inside window	Outside window	0	X	bypass	bypass	1	CR61-0C[3:2]=00 CR60[6]=0	ICM	ICM	1	CR61-0C[3:2]=01 && CR60[6]=1	ICM	bypass	1	CR61-0C[3:2]=10 && CR60[6]=1	bypass	ICM	DCC (CRC7[7])	Application control	Inside window	Outside window	0	X	bypass	bypass	1	CR61-0C[3:2]=00 CR60[6]=0	DCC	DCC	1	CR61-0C[3:2]=01 && CR60[6]=1	DCC	bypass	1	CR61-0C[3:2]=10 && CR60[6]=1	bypass	DCC			
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1	CR61-0C[3:2]=01 && CR60[6]=1	DCC	bypass																																											
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1:0	R/W	Peaking/Coring application control 00:Full region 01: Inside window 10: Outside window 11: Reserved	<table border="1"> <thead> <tr> <th>Peaking (CRD6[6])</th> <th>Application control</th> <th>Inside window</th> <th>Outside window</th> </tr> </thead> <tbody> <tr> <td>0</td> <td>X</td> <td>bypass</td> <td>bypass</td> </tr> <tr> <td>1</td> <td>CR61-0C[5:4]=00 CR60[6]=0</td> <td>Peaking</td> <td>Peaking</td> </tr> <tr> <td>1</td> <td>CR61-0C[5:4]=01 && CR60[6]=1</td> <td>Peaking</td> <td>bypass</td> </tr> <tr> <td>1</td> <td>CR61-0C[5:4]=10 && CR60[6]=1</td> <td>bypass</td> <td>Peaking</td> </tr> </tbody> </table>	Peaking (CRD6[6])	Application control	Inside window	Outside window	0	X	bypass	bypass	1	CR61-0C[5:4]=00 CR60[6]=0	Peaking	Peaking	1	CR61-0C[5:4]=01 && CR60[6]=1	Peaking	bypass	1	CR61-0C[5:4]=10 && CR60[6]=1	bypass	Peaking																							
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Address: 61-0D Highlight Window Control 1

Default : 00h

Bit	Mode	Function
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7:6	R/W	sRGB application control 00: sRGB used on full region 01: sRGB used inside highlight window 10: sRGB used outside highlight window 11: Reserved																				
		<table border="1"> <thead> <tr> <th>sRGB (CR62[2])</th><th>Application control</th><th>Inside window</th><th>Outside window</th></tr> </thead> <tbody> <tr> <td>0</td><td>X</td><td>bypass</td><td>bypass</td></tr> <tr> <td>1</td><td>CR61-0D[7:6]=00 CR60[6]=0</td><td>sRGB</td><td>sRGB</td></tr> <tr> <td>1</td><td>CR61-0D[7:6]=01 && CR60[6]=1</td><td>sRGB</td><td>bypass</td></tr> <tr> <td>1</td><td>CR61-0D[7:6]=10 && CR60[6]=1</td><td>bypass</td><td>sRGB</td></tr> </tbody> </table>	sRGB (CR62[2])	Application control	Inside window	Outside window	0	X	bypass	bypass	1	CR61-0D[7:6]=00 CR60[6]=0	sRGB	sRGB	1	CR61-0D[7:6]=01 && CR60[6]=1	sRGB	bypass	1	CR61-0D[7:6]=10 && CR60[6]=1	bypass	sRGB
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5:4	R/W	DCR/CABC application control 00: DCR/CABC used on full region. 01: DCR/CABC used inside highlight window. 10: DCR/CABC used outside highlight window. 11: Reserved.																				
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DCR(Page 7) CRD8[0])	Application control	Inside window	Outside window																			
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1	CRB6-0D[5:4]=00 CR60[6]=0	DCR/CABC	DCR/CABC																			
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1	CRB6-0D[5:4]=10 && CR60[6]=1	bypass	DCR/CABC																			
3:0	--	Reserved to 0																				

Color Processor Control

Address: 62 COLOR_CTRL (Color Control Register) Default: 00h

Bit	Mode	Function
7	R/W	sRGB Coefficient Write Ready 0: Not ready or cleared after finished 1: Ready to write (wait for DVS to apply)
6	R/W	sRGB Precision 0: Normal (Default) 1: Multiplier Coefficient Bit Left Shift
5:3	R/W	sRGB Coefficient Write Enable



		000: Disable 001: Write R Channel (RRH,RRL,RGH,RGL,RBH,RBL) (address reset to 0 when written) 010: Write G Channel (GRH,GBL,GGH,GGL,GBH,GBL) (address reset to 0 when written) 011: Write B Channel (BRH,BRL,BGH,BGL,BBH,BBL) (address reset to 0 when written) 100: R Offset (RoffsetH, RoffsetL) (address reset to 0 when written) 101: G Offset (GoffsetH, GoffsetL) (address reset to 0 when written) 110: B Offset (BoffsetH, BoffsetL) (address reset to 0 when written)
2	R/W	Enable sRGB Function 0: Disable (Default) 1: Enable
1	R/W	Enable Contrast Function: 0: disable the coefficient (Default) 1: enable the coefficient
0	R/W	Enable Brightness Function: 0: disable the coefficient (Default) 1: enable the coefficient

Address: 63 SRGB_ACCESS_PORT

Bit	Mode	Function
7:0	W	sRGB_COEF[7:0]

- For Multiplier coefficient: 9 bit: 1 bit sign, 8 bit fractional part
- For filling multiplier coefficient, the sequence should be SIGN bit (High Byte), 8 bit fractional (Low Byte)
- For Offset Coefficient: 1 sign, 8 integer, 4 bit fractional part
- R G : 8 bit integer, 2bit fractional
- sRGB output saturation to 1023 and Clamp to 0
- sRGB Output is 10 bit

$$\begin{bmatrix} R' \\ G' \\ B' \end{bmatrix} = \begin{bmatrix} 1+RR & RG & RB \\ GR & 1+GG & GB \\ BR & BG & 1+BB \end{bmatrix} \begin{bmatrix} R \\ G \\ B \end{bmatrix} + \begin{bmatrix} Roffset \\ Goffset \\ Boffset \end{bmatrix}$$



New SRGB(RL6093/RTD2382)	
{62[6], 68[6:5]}	Bit Definition
100	1-bit shift-left
101	2-bit shift-left (S1.7)
110	3-bit shift-left (S2.6)
111	0-bit shift-left (S0.08)
0xx	0-bit shift-left (S0.08)
Old SRGB (RTD2472D,RTD2472RD)	
{62[6], 68[6]}	Bit Definition
10	1-bit shift-left (S0.8)
11	2-bit shift-left (S1.7)
0x	0-bit shift-left (S0.08)

Contrast/Brightness Coefficient

Address: 64 Contrast /Brightness Access Port Control

Default: 00h

Bit	Mode	Function
7	R/W	Enable Contrast /Brightness access port
6	R/W	Contrast/Brightness and sRGB swap 0: sRGB before Contrast/Brightness (default) 1: Contrast/Brightness before sRGB (for PCM)
5:0	R/W	Contrast /Brightness port address

Access data port continuously will get address auto increase.

Address: 65-00 BRI_RED_COE (Set A)

Bit	Mode	Function
7:0	R/W	Brightness Red Coefficient: Valid range: -128(00h) ~ 0(80h) ~ +127(FFh)

Address: 65-01 BRI_GRN_COE (Set A)

Bit	Mode	Function
7:0	R/W	Brightness Green Coefficient: Valid range: Valid range: -128(00h) ~ 0(80h) ~ +127(FFh)

Address: 65-02 BRI_BLU_COE (Set A)

Bit	Mode	Function
7:0	R/W	Brightness Blue Coefficient: Valid range: -128(00h) ~ 0(80h) ~ +127(FFh)

Address: 65-03 CTS_RED1_COE (Set A)

Bit	Mode	Function
7:0	R/W	Contrast Red Coefficient: Valid range: 0(00h) ~ 1(80h) ~ 2(FFh)

Address: 65-04 CTS_GRN1_COE (Set A)



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Bit	Mode	Function
7:0	R/W	Contrast Green Coefficient: Valid range: 0(00h) ~ 1(80h) ~ 2(FFh)

Address: 65-05 CTS_BLU1_COE (Set A)

Bit	Mode	Function
7:0	R/W	Contrast Blue Coefficient: Valid range: 0(00h) ~ 1(80h) ~ 2(FFh)

Address: 65-06 BRI_RED_COE (Set B)

Bit	Mode	Function
7:0	R/W	Brightness Red Coefficient: Valid range: -128(00h) ~ 0(80h) ~ +127(FFh)

Address: 65-07 BRI_GRN_COE (Set B)

Bit	Mode	Function
7:0	R/W	Brightness Green Coefficient: Valid range: Valid range: -128(00h) ~ 0(80h) ~ +127(FFh)

Address: 65-08 BRI_BLU_COE (Set B)

Bit	Mode	Function
7:0	R/W	Brightness Blue Coefficient: Valid range: -128(00h) ~ 0(80h) ~ +127(FFh)

Address: 65-09 CTS_RED1_COE (Set B)

Bit	Mode	Function
7:0	R/W	Contrast Red Coefficient: Valid range: 0(00h) ~ 1(80h) ~ 2(FFh)

Address: 65-0A CTS_GRN1_COE (Set B)

Bit	Mode	Function
7:0	R/W	Contrast Green Coefficient: Valid range: 0(00h) ~ 1(80h) ~ 2(FFh)

Address: 65-0B CTS_BLU1_COE (Set B)

Bit	Mode	Function
7:0	R/W	Contrast Blue Coefficient: Valid range: 0(00h) ~ 1(80h) ~ 2(FFh)

When highlight window is disable, coefficient set A is used.

Address: 65-0C CTS_RED2_COE (Set A)**Default: 80h**

Bit	Mode	Function
7:0	R/W	Contrast Red Coefficient:



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		Valid range: 0(00h) ~ 1(80h) ~ 2(FFh)
--	--	---------------------------------------

Address: 65-0D CTS_GRN2_COE (Set A) Default: 80h

Bit	Mode	Function
7:0	R/W	Contrast Green Coefficient: Valid range: 0(00h) ~ 1(80h) ~ 2(FFh)

Address: 65-0E CTS_BLU2_COE (Set A) Default: 80h

Bit	Mode	Function
7:0	R/W	Contrast Blue Coefficient: Valid range: 0(00h) ~ 1(80h) ~ 2(FFh)

Address: 65-0F CTS_RED2_COE (Set B) Default: 80h

Bit	Mode	Function
7:0	R/W	Contrast Red Coefficient: Valid range: 0(00h) ~ 1(80h) ~ 2(FFh)

Address: 65-10 CTS_GRN2_COE (Set B) Default: 80h

Bit	Mode	Function
7:0	R/W	Contrast Green Coefficient: Valid range: 0(00h) ~ 1(80h) ~ 2(FFh)

Address: 65-11 CTS_BLU2_COE (Set B) Default: 80h

Bit	Mode	Function
7:0	R/W	Contrast Blue Coefficient: Valid range: 0(00h) ~ 1(80h) ~ 2(FFh)

Address: 65-12

Register:: CTS_Threshold (Set A)

Name	Bit	R/W	Default	Description	Config
CTS Threshold	7:0	R/W	0xFF	Threshold of GAIN1 and GAIN2 of Set A	

Address: 65-13

Register:: CTS_Threshold (Set B)

Name	Bit	R/W	Default	Description	Config
CTS Threshold	7:0	R/W	0xFF	Threshold of GAIN1 and GAIN2 of Set B	

If input value > threshold, the CTS_ADDING_VALUE will be applied.

Address: 65-14

Register:: CTS_GAIN_ADDING_VALUE_H (Set A)

Name	Bit	R/W	Default	Description	Config
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CTS_R GAIN ADDING VALUE H	7:0	R/W	0x00	The adding value High byte [11:8] of GAIN2 region	
--------------------------------------	-----	-----	------	---	--

Address: 65-15

Register:: CTS_GAIN_ADDING_VALUE_L (Set A)					
Name	Bit	R/W	Default	Description	Config
CTS_R GAIN ADDING VALUE L	7:0	R/W	0x00	The adding value Low byte [7:0] of GAIN2 region	

Address: 65-16

Register:: CTS_G_GAIN_ADDING_VALUE_H (Set A) 0x5B-0C					
Name	Bit	R/W	Default	Description	Config
CTS_G_GAIN_ADDING_V ALUE_H	7:0	R/W	0x00	The green channel adding value High byte [11:8] of GAIN2 region	

Address: 65-17

Register:: CTS_G_GAIN_ADDING_VALUE_L (Set A)					
Name	Bit	R/W	Default	Description	Config
CTS_G_GAIN_ADDING_V ALUE_L	7:0	R/W	0x00	The green channel adding value Low byte [7:0] of GAIN2 region	

Address: 65-18

Register:: CTS_B_GAIN_ADDING_VALUE_H (Set A)					
Name	Bit	R/W	Default	Description	Config
CTS_B_GAIN_ADDING_V ALUE_H	7:0	R/W	0x00	The blue channel adding value High byte [11:8] of GAIN2 region	

Address: 65-19

Register:: CTS_B_GAIN_ADDING_VALUE_L (Set A)					
Name	Bit	R/W	Default	Description	Config
CTS_B_GAIN_ADDING_V ALUE_L	7:0	R/W	0x00	The blue channel adding value Low byte [7:0] of GAIN2 region	

Address: 65-1A

Register:: CTS_GAIN_ADDING_VALUE_H (Set B)					
Name	Bit	R/W	Default	Description	Config
CTS_R GAIN ADDING VALUE H	7:0	R/W	0x00	The adding value High byte [11:8] of GAIN2 region	

Address: 65-1B

Register:: CTS_GAIN_ADDING_VALUE_L (Set B)					
Name	Bit	R/W	Default	Description	Config
CTS_R GAIN ADDING VALUE L	7:0	R/W	0x00	The adding value Low byte [7:0] of GAIN2 region	

Address: 65-1C

Register:: CTS_G_GAIN_ADDING_VALUE_H (Set B)					
Name	Bit	R/W	Default	Description	Config
CTS_G_GAIN_ADDING_V ALUE_H	7:0	R/W	0x00	The green channel adding value High byte [11:8] of GAIN2 region	

Address: 65-1D

Register:: CTS_G_GAIN_ADDING_VALUE_L (Set B)					
Name	Bit	R/W	Default	Description	Config
CTS_G_GAIN_ADDING_V ALUE_L	7:0	R/W	0x00	The green channel adding value Low byte [7:0] of GAIN2 region	

**Address: 65-1E****Register:: CTS_B_GAIN_ADDING_VALUE_H (Set B)**

Name	Bit	R/W	Default	Description	Config
CTS_B_GAIN_ADDING_V ALUE_H	7:0	R/W	0x00	The blue channel adding value High byte [11:8] of GAIN2 region	

Address: 65-1F**Register:: CTS_B_GAIN_ADDING_VALUE_L (Set B)**

Name	Bit	R/W	Default	Description	Config
CTS_B_GAIN_ADDING_V ALUE_L	7:0	R/W	0x00	The blue channel adding value Low byte [7:0] of GAIN2 region	

Gamma Control**Address: 66 GAMMA_PORT**

Bit	Mode	Function
7:0	R/W	Access port for gamma correction table

- The Gamma Table written to this port should follow the sequences as expressed below:

{2'b0, g0[9:4]}, {g0[3:0]}, 2'b0, g4[9:8]}, {g4[7:0]}, <- addr = 0

{2'b0, g8[9:4]}, {g8[3:0]}, 2'b0, g12[9:8]}, {g12[7:0]}, <- addr = 1

...,

{2'b0, g1016[9:4]}, {g1016[3:0]}, 2'b0, g1020[9:8]}, {g1020[7:0]}, <- addr = 127

{2'b0, g1023[9:4]}, {g1023[3:0]}, 4'b0}, {8'b0} <- addr = 128

- When CR67[3] is set to 1, we can directly specify the initial address of Gamma Table in this port.
- When CR67[3] is set to 1, the value of this port is the address of Gamma Table that you are going to R/W.
- When CR67[3] is set to 0, we can read the value of Gamma Table in the following order.

{2'b0, g_4*2n [9:4]}, {g_4*2n [3:0]}, 2'b0, g4*(2n+1)[9:8]}, {g4*(2n+1)[7:0]},

{2'b0, g_4*(2n+2)[9:4]}, {g_4*(2n+2) [3:0]}, 2'b0, g4*(2n+3) [9:8]}, {g4*(2n+3)[7:0]},

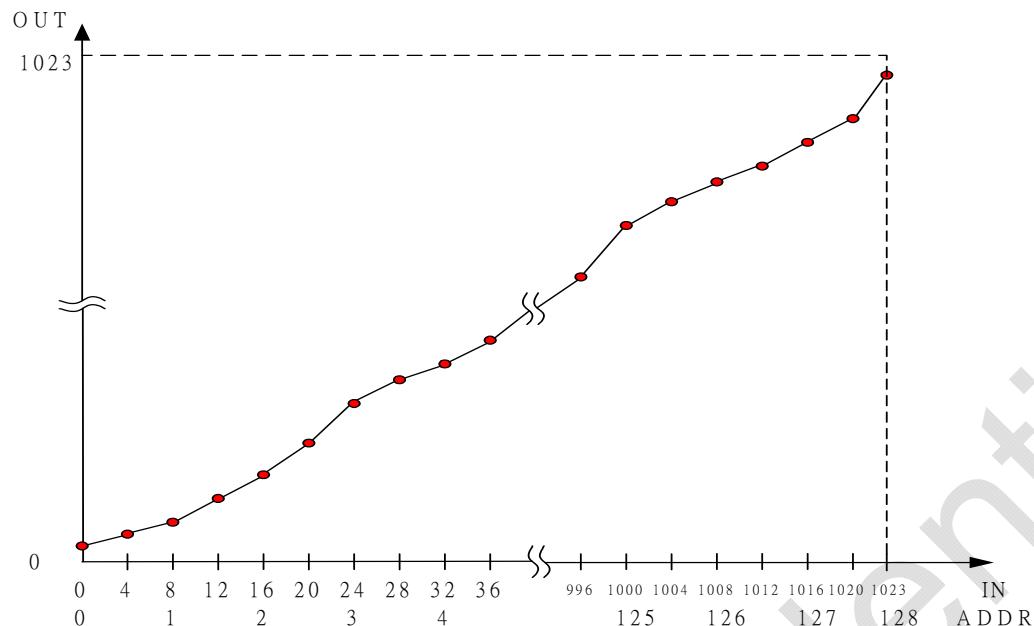
...,

{2'b0, g_1023[9:4]}, {g_1023*(2n+2) [3:0]}, 4'b0}, {8'b0}



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Address: 67 GAMMA CTRL Default: 00h

Bit	Mode	Function
7	R/W	Enable Access Channels for Gamma Correction Coefficient: 0: disable these channels (Default) 1: enable these channels
6	R/W	Gamma table enable 0: by pass (Default) 1: enable
5:4	R/W	Color Channel of Gamma Table 00: Red Channel (Default) 01: Green Channel 10: Blue Channel 11: Red/Green/Blue Channel (R/G/B Gamma are the same)
3	R/W	Gamma Port Address Access Enable 0: Normal function. (Default) 1: Gamma Port is used as specifying initial address.
2	R/W	Write Table to SRAM or Latch Select 0: to SRAM (Default) 1: to Latch
1:0	--	Reserved to 0

Address: 68 GAMMA_BIST (Color Control Register) Default: 60h

Bit	Mode	Function
7	R/W	Test_mode 0: Disable, dither_out = dither_result[9:2]; // truncate to integer number (Default) 1: Enable, dither_out = dither_result[7:0]; // propagate decimal part for test
6:5	R/W	sRGB multiplier coefficient precision 00: 1-bit Shift-left



		10: 3-bit Shift-left 01: 2-bit Shift-left 11: 0-bit shift-left (Default)
4:3	--	Reserved to 0
2	R/W	Gamma BIST_En 0: BIST disable (Default) 1: BIST enable
1	R	Gamma BIST_Period Progress 0: BIST is done (Default) 1: BIST is running
0	R	Gamma BIST Test Result (It will go low first during BIST period) 0: SRAM Fail 1: SRAM OK

Dithering Control(For Display Domain)

Register:: DITHERING DATA ACCESS					0x69
Name	Bits	Read/Write	Reset State	Comments	Config
DITHERING_DA_TA_ACCESS	7:0	W	0	Refer to following description	

A. When CR6A[7:6] is 2'b01, dithering sequence table access is enabled:

- There are three set of dithering sequence table, each table contains 32 elements, s0, s1, ..., s31.
- Each element has 2 bit to index one of 4 dithering table.
- Input data sequence is {sr3,sr2,sr1,sr0}, {sr7,sr6,sr5,sr4}, ..., {sr31,sr30,sr29,sr28}, {sg3,sg2,sg1,sg0}, ..., {sg31,sg30,sg29,sg28}, {sb3,sb2,sb1,sb0}, ..., {sb31,sb30,sb29,sb28} for red, green and blue channel.
- R + (2R+1) * C choose sequence element, where R is Row Number / 2, and C is Column Number / 2.

B. When CR6A[7:6] is 2'b10, dithering table access is enabled:

- For dithering table access, the red, green, blue each channel has 4 dithering table, each table is 2x2 elements, and one element has 4 bit for 10B/8B, the elements should fill 0 to 3, for 10B/6B, the elements should fill 0 to 15.



- Input data sequence is [Dr00 Dr01], [Dr02,Dr03], ..., [Dr30,Dr31], [Dr32,Dr33],
 [Dg00,Dg01], [Dg02,Dg03], ..., [Dg30,Dg31], [Dg32,Dg33], [Db00,Db01], [Db02,Db03], ...,
 [Db30,Db31], [Db32,Db33].

D00	D01
D02	D03

D10	D11
D12	D13

D20	D21
D22	D23

D30	D31
D32	D33

C. When CR6A[7:6] is 2'b11, temporal offset access is enabled:

- There are 16 element for temporal offset table, t0, t1, ..., t15.
Each element has 2 bit to index one of 4 temporal offset.
- Input data sequence is {t3,t2,t1,t0}, {t7,t6,t5,t4}, {t11,t10,t9,t8}, {t15,t14,t13,t12}.

Register:: DITHERING_CTRL1					0x6A
Name	Bits	Read/ Write	Reset State	Comments	Config
Dither_Access	7:6	R/W	0	Enable Access Control 00: disable (Default) 01: enable access dithering sequence table 10: enable access dithering table 11: enable access temporal offset	
Dither_en	5	R/W	0	Enable Dithering Function 0: disable (Default) 1: enable	
Dither_temp	4	R/W	0	Temporal Dithering 0: Disable (Default) 1: Enable	
Dither_table	3	R/W	0	Dithering Table Value Sign 0: unsigned 1: signed (2's complement)	
Dither_mode	2	R/W	0	Dithering Mode 0: New (Default) 1: Old	
Dither_V_Fram_M	1	R/W	0	Vertical Frame Modulation 0: Disable (Default) 1: Enable	
Dither_VH_Fram_M	0	R/W	0	Horizontal Frame Modulation 0: Disable (Default) 1: Enable	



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Dithering Control (Display Domain)

Register:: DITHERING_CTRL2 0x6B					
Name	Bits	Read/Write	Reset State	Comments	Config
DITHER_THD_SE_L_EN	7	R/W	0x0	Dither RGB level threshold select enable 0: disable 1: enable (reserved in 6093)	
DITHER_THD_SE_L	6:4	R/W	0x00	Dither RGB level threshold select (0x66) 000: {6'h0, R_THD[9:8]} 001: R_THD[7:0] 010: {6'h0, G_THD[9:8]} 011: G_THD[7:0] 100: {6'h0, B_THD[9:8]} 101: B_THD[7:0] 110: {6'h0, ALL R/G/B[9:8]} 111: ALL R/G/B[7:0] (reserved in 6093)	
RESERVED	3	--	0	Reserved	
DITHER_SEQ_SE_T	2	R/W	0	Sequence table select 0: all select setting0 1: select setting1 only if R/G/B < THD (reserved in 6093)	
Reserved	1	R/W	0	Reserved	
Dither_Table_Ref	0	R/W	1	Table reference 0: By VS/HS 1: By DEN (Default)	

Overlay/Color Palette/Background Color Control

Address: 6C OVERLAY_CTRL (Overlay Display Control Register)

Default: 00h

Bit	Mode	Function
7:6	--	Reserved to 0
5	R/W	Background color access enable 0: Disable(Reset CR6D Write Pointer to R) 1: Enable
4:2	R/W	Alpha blending level (Also enable OSD frame control register 0x003 byte 1[3:2]) 000: Disable (Default) 001 ~111: 1/8~ 7/8
1	R/W	Overlay Sampling Mode Select: 0: single pixel per clock (Default)



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		1: dual pixels per clock (The OSD will be zoomed 2X in horizontal scan line)
0	R/W	<p>Overlay Port Enable:</p> <p>0: Disable (Default) 1: Enable</p> <p>Turn off overlay enable and switch to background simultaneously when auto switch to background.</p>

Address: 6D **BGND_COLOR_CTRL** **Default: 00h**

Bit	Mode	Function
7:0	R/W	Background color RGB 8-bit value[7:0]

- There are 3 bytes color select of background R, G, B, once we enable Background color access channel(CR6C[5] and the continuous writing sequence is R/G/B

Address: 6E **OVERLAY_LUT_ADDR (Overlay LUT Address)** **Default: 00h**

Bit	Mode	Function
7	R/W	<p>Enable Overlay Color Plate Access:</p> <p>0: Disable (Default) 1: Enable</p>
6	R/W	<p>Double buffer write enable (auto clear)</p> <p>0: disable 1: enable</p>
5:0	R/W	Overlay-64*24 Look-Up-Table Write Address [5:0]

- Auto-increment while every accessing “Overlay LUT Access Port”.
- While OSDON, enable double buffer write is necessary for modifying color palette LUT.
 - Write [6] to be 1 and set LUT write address first
 - Write 3 data R[7:0], G[7:0], B[7:0] to 6F
 - Wait for [6] auto clear to be 0, then repeat the flow until the procedure is done

Address: 6F **COLOR_LUT_PORT (LUT Access Port)**

Bit	Mode	Function
7:0	W	Color Palette 64*24 Look-Up-Table access port [7:0]

- Using this port to access overlay color plate which addressing by the above registers.
- The writing sequence into LUT is [R0, G0, B0, R1, G1, B1, ...R63, G63, and B63] and the address counter will be automatic increment and circular from 0 to 63.



Image Auto Function

Address: 70 H_BOUNDARY_H

Bit	Mode	Function
7:4	R/W	Horizontal Boundary Start: High Byte [11:8]
3:0	R/W	Horizontal Boundary End: High Byte [11:8]

Address: 71 H_BOUNDARY_STA_L

Bit	Mode	Function
7:0	R/W	Horizontal Boundary Start: Low Byte [7:0]

Address: 72 H_BOUNDARY_END_L

Bit	Mode	Function
7:0	R/W	Horizontal Boundary End: Low Byte [7:0]

Address: 73 V_BOUNDARY_H

Bit	Mode	Function
7:4	R/W	Vertical Boundary Start: High Byte [11:8]
3:0	R/W	Vertical Boundary End: High Byte [11:8]

Vertical boundary search should be limited by Vertical boundary start.

Address: 74 V_BOUNDARY_STA_L

Bit	Mode	Function
7:0	R/W	Vertical Boundary Start: Low Byte [7:0]

Address: 75 V_BOUNDARY_END_L

Bit	Mode	Function
7:0	R/W	Vertical Boundary End: Low Byte [7:0]

Address: 76 RED_NOISE_MARGIN (Red Noise Margin Register)

Bit	Mode	Function
7:2	R/W	Red pixel noise margin setting register
1:0	--	Reserved to 0

Address: 77 GRN_NOISE_MARGIN (Green Noise Margin Register)

Bit	Mode	Function
7:2	R/W	Green pixel noise margin setting register
1:0	--	Reserved to 0

Address: 78 BLU_NOISE_MARGIN (Blue Noise Margin Register)

Bit	Mode	Function
7:2	R/W	Blue pixel noise margin setting register
1	R/W	Auto phase result address write 0: CR-86 read only



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		1: CR-86 for result index
0	R/W	Auto phase result mode 0: old mode (default) 1: new mode

Address: 79 DIFF_THRESHOLD

Bit	Mode	Function
7:0	R/W	Difference Threshold (Threshold for DIFF no matter CR7D[2] = 0 or 1)

Address: 7A AUTO_ADJ_CTRL0**Default: 00h**

Bit	Mode	Function
7	R/W	Field_Select_Enable: Auto-Function only active when Even or Odd field. 0: Disable (Default) 1: Enable
6	R/W	Field_Select: Select Even or Odd field. Active when Field_Select_Enable . 0: Active when ODD signal is “0” (Default) 1: Active when ODD signal is “1”
5	R/W	Low Pass Filter (121-LPF) 0: Disable (Default) 1: Enable
4	R/W	Auto Function Acceleration : 0: Disable (Default) 1: Enable For auto-balance (CR7D[1]=0), this function must be disabled.
3:2	R/W	Vertical boundary search: 00: 1 pixel over threshold (Default) 01: 2 pixel over threshold 10: 4 pixel over threshold 11: 8 pixel over threshold
1:0	R/W	Color Source Select for Detection: 00: B color (Default) 01: G color 10: R color 11: ALL (the result will be divided by 2)

Address: 7B HW_AUTO_PHASE_CTRL0**Default: 00h**

Bit	Mode	Function
7:3	R/W	Number of Auto-Phase Step (Value+1) (How many times (steps reference CR7B[2:0]) jumps when using Hardware Auto)



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2:0	R/W	Hardware Auto Phase Step 000: Step =1 (Default) 001 Step =2 010: Step =4 011: Step =8 1xx: Step =16
-----	-----	---

Address: 7C HW_AUTO_PHASE_CTRL1 Default: 00h

Bit	Mode	Function
7	R/W	Hardware Auto Phase Select Trigger 0: IVS 1: Vertical Boundary End
6:0	R/W	Initial phase of Auto-Phase (0~127)

Address: 7D AUTO_ADJ_CTRL1 Default: 00h

Bit	Mode	Function
7	R/W	Measure Digital Enable Info when boundary search active 0: Normal Boundary Search (Default) 1: Digital Enable Info Boundary Search.(Digital mode)
6	R/W	Hardware / Software Auto Phase Switch 0: Software (Default) 1: Hardware
5	R/W	Color Max or Min Measured Select: 0: MIN color measured (Only when Balance-Mode, result must be complemented) (Default) 1: MAX color measured
4	R/W	Accumulation or Compare Mode 0: Compare Mode (Default) 1: Accumulation Mode
3	R/W	Mode Selection For SOD 0: SOD Edge Mode (Default) 1: SOD Edge + Pulse Mode
2	R/W	Type Selection For DIFF 0: DIFF 1: (DIFF/4) * (DIFF/4) Total result for each color is divided by 8 if this bit is 1.
1	R/W	Function (Phase/Balance) Selection 0: Auto-Balance (Default) 1: Auto-Phase
0	R/W	Start Auto-Function Tracking Function:



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		0: stop or finished (Default)
		1: start

Control Table/ Function	Sub-Function	CR7D.6	CR7D.5	CR7D.4	CR7D.3	CR7D.1	CR7C
Auto-Balance	Max pixel	X	1	0	0	0	X
	Min pixel	X	0	0	0	0	X
Auto-Phase Type	Mode1	1	1	1	0	1	Th
	Mode2	1	1	1	1	1	Th
Accumulation	All pixel	1	1	1	0	0	0

Table 1 Auto-Tracking Control Table

Address: 7E VER_START_END_H (Active region vertical start Register)

Bit	Mode	Function
7:4	R	Active region vertical START measurement result: bit[11:8]
3:0	R	Active region vertical END measurement result: bit[11:8]

Address: 7F VER_START_L (Active region vertical start Register)

Bit	Mode	Function
7:0	R	Active region vertical start measurement result: bit[7:0]

Address: 80 VER_END_L (Active region vertical end Register)

Bit	Mode	Function
7:0	R	Active region vertical end measurement result: bit[7:0]

Address: 81 H_START_END_H (Active region horizontal start Register)

Bit	Mode	Function
7:4	R	Active region horizontal START measurement result: bit [11:8]
3:0	R	Active region horizontal END measurement result: bit[11:8]

Address: 82 H_START_L (Active region horizontal start Register)

Bit	Mode	Function
7:0	R	Active region horizontal start measurement result: bit[7:0]

Address: 83 H_END_L (Active region horizontal end Register)

Bit	Mode	Function
7:0	R	Active region horizontal end measurement result: bit[7:0]

Address: 84 AUTO_PHASE_3 (Auto phase result byte3 register)

Bit	Mode	Function
7:0	R	Auto phase measurement result: bit[31:24]

Address: 85 AUTO_PHASE_2 (Auto phase result byte2 register)

Bit	Mode	Function



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7:0	R	Auto phase measurement result: bit[23:16]
-----	---	--

Address: 86 AUTO_PHASE_1 (Auto phase result byte1 register)

Bit	Mode	Function
7:0	R	Auto phase measurement result: bit[15:8] When CR-78[1] set to 1, auto phase result read index 0~255 indicates for maximum 64 auto phase results (4 Bytes every result)

Address: 87 AUTO_PHASE_0 (Auto phase result byte0 register)

Bit	Mode	Function
7:0	R	Auto phase measurement result: bit[7:0] The measured value of R or G or B color max or min. (Auto-Balance) When CR-78[0] set to 1, read CR-87 continuously for auto phase results

- CR-87 can be read continuously for totally 256 Bytes (64 results).

The multiple results, Address: 84~87, are stored in mcu's xdata space.

Range from 0xFA00 to 0xFAFF.

Xdata access method is suggested method.

- Set CR-78[1] and CR-86 for read index before read CR-87.
- Once CR-87 has been read 4 times, read index in CR-86 will increase automatically.

When input is 2560x1600, there will be three case for Register 0x84~0x87:

a. Only SOD + Pulse for RGB

$2560 \times 1600 \times 255 \times 2 \times 3 = 6266880000$ need 33 bits to indicate.

CR 84~87 will give bit [32:1].

b. $(SOD/4)^2 / 8 +$ Pulse for RGB

$2560 \times 1600 \times (255/4)^2 / 8 \times 2 \times 3 = 12484800000$ need 34 bits to indicate.

CR 84~87 will give bit [33:2]

c. $(SOD/4)^2 / 8 +$ Pulse only for one color

$2560 \times 1600 \times (255/4)^2 / 8 \times 2 = 4161600000$ need 32 bits to indicate.

CR 84~87 will give bit [31:0]

Dithering Control (For Input Domain)

Register:: I_DITHERING DATA ACCESS					0x88
Name	Bits	Read/Write	Reset State	Comments	Config
DITHERING_DATA_ACCESS	7:0	W	0	Refer to following description	

A. When CR88[7:6] is 2'b01, dithering sequence table access is enabled:



- There are three set of dithering sequence table, each table contains 32 elements, s0, s1, ..., s31. Each element has 2 bit to index one of 4 dithering table.
- Input data sequence is {sr3,sr2,sr1,sr0}, {sr7,sr6,sr5,sr4}, ..., {sr31,sr30,sr29,sr28}, {sg3,sg2,sg1,sg0}, ..., {sg31,sg30,sg29,sg28}, {sb3,sb2,sb1,sb0}, ..., {sb31,sb30,sb29,sb28} for red, green and blue channel.
- R + (2R+1) * C choose sequence element, where R is Row Number / 2, and C is Column Number / 2.

B. When CR88[7:6] is 2'b10, dithering table access is enabled:

- For dithering table access, the red, green, blue each channel has 4 dithering table, each table is 2x2 elements, and one element has 4 bit for 10B/8B, the elements should fill 0 to 3, for 10B/6B, the elements should fill 0 to 15.
- Input data sequence is [Dr00 Dr01],[Dr02,Dr03], ..., [Dr30,Dr31],[Dr32,Dr33], [Dg00,Dg01],[Dg02,Dg03], ..., [Dg30,Dg31],[Dg32,Dg33], [Db00,Db01],[Db02,Db03], ..., [Db30,Db31],[Db32,Db33].

D00	D01
D02	D03

D10	D11
D12	D13

D20	D21
D22	D23

D30	D31
D32	D33

C. When CR88[7:6] is 2'b11, temporal offset access is enabled:

- There are 16 element for temporal offset table, t0, t1, ..., t15. Each element has 2 bit to index one of 4 temporal offset.
- Input data sequence is {t3,t2,t1,t0}, {t7,t6,t5,t4}, {t11,t10,t9,t8}, {t15,t14,t13,t12}.

Register:: I_DITHERING_CTRL1					0x89
Name	Bits	Read/Write	Reset State	Comments	Config
Dither_Access	7:6	W	0	Enable Access Control 00: disable (Default) 01: enable access dithering sequence table 10: enable access dithering table 11: enable access temporal offset	
Dither_en	5	R/W	0	Enable Dithering Function 0: disable (Default) 1: enable	
Dither_temp	4	R/W	0	Temporal Dithering 0: Disable (Default) 1: Enable	
Dither_table	3	R/W	0	Dithering Table Value Sign 0: unsigned 1: signed (2's complement)	
Dither_mode	2	R/W	0	Dithering Mode	



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				0: New (Default) 1: Old	
Dither_V_Fram_M	1	R/W	0	Vertical Frame Modulation 0: Disable (Default) 1: Enable	
Dither_VH_Fram_M	0	R/W	0	Horizontal Frame Modulation 0: Disable (Default) 1: Enable	

Register:: I_DITHERING_CTRL2					0x8A
Name	Bits	Read/ Write	Reset State	Comments	Config
Reserved	7:1	R/W	0	Reserved	
Dither_Table_Ref	0	R/W	1	Table reference 0: By VS/HS 1: By DEN (Default)	

Embedded Timing Controller

Address: 8B TCON_ADDR_PORT

Default: 00h

Bit	Mode	Function
7:0	R/W	Address port for embedded TCON access

Address: 8C TCON_DATA_PORT Default: 00h

Bit	Mode	Function
7:0	R/W	Data port for embedded TCON access

Address: 8C-00 TC_CTRL0 (Timing Controller control register1) Default: 01h

Bit	Mode	Function
7	R/W	Enable Timing Controller Function (Global) 0: Disable (Default) 1: Enable All TCON pins will be initialized when enabled and goes low when disabled.
6	R/W	TCON [n] Toggle Function Reset 0: Not reset (Default) 1: reset by DVS
5	R/W	Inactive Period Data Controlled by internal TCON [13]



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		0: DEN (Default) 1: TCON [13]
4	R/W	TCON_HS compensation 0: Real TCON_HS = TCON_HS-4 1: Real TCON_HS = TCON_HS-27 If setting TCON_HS > DH_Total, then setting TCON_HS must subtract DH_Total.
3	---	Reserve to 0
2	---	Reserve to 0
1:0	R/W	DISP_TYPE 00: Reserved 01: LVDS (Default) 10: reserve others are reserved

Address: 8C-01 TC_CTRL1 (Timing Controller control register1) Default: 00h

Bit	Mode	Function
7:0	R/W	Reserved to 0

Address: 8C-02 Line-Threshold (THL) Default: 00h

Bit	Mode	Function
7	R/W	2-Line Sum of Difference Threshold 1 Value: bit [8], ie:TH1 (also refer to CR8C-03)
6	R/W	2-Line Sum of Difference Threshold 2 Value: bit [8], ie:TH2 (also refer to CR8C-04)
5:0	R/W	Over Difference Line Threshold Value: bit [9:4] Notes: Bit[3:0] are zeros

Address: 8C-03 Pixel Threshold High Value for Smart Polarity (TH1) Default: 00h

Bit	Mode	Function
7:0	R/W	2 line Sum of Difference Threshold 1 Value: bit [7:0], ie:TH1 (Also refer to CR8C-02[7])

Address: 8C-04 Pixel Threshold Low Value for Smart Polarity (TH2) Default: 00h

Bit	Mode	Function
7:0	R/W	2 line Sum of Difference Threshold 2 Value: bit [7:0], ie:TH2 (Also refer to CR8C-02[6])

Address: 8C-05 Line Threshold Value for Smart Polarity Default: 00h

Bit	Mode	Function
7	R/W	Measure Dot Pattern over Threshold 1: Run. Auto: always measure (Reference to CR8C-05[5]) Manual: start to measure, clear after finish 0: Stop



6	R	Dot Pattern Sum of Difference Measure Result 1: Over threshold 0: Under threshold
5	R/W	Anti-Flicker Auto-Measure Control 1: Auto 0: Manual
4:1	R/W	Reserved
0	R/W	Anti-Flicker Measure Mode 0: Dot-Based (Original) 1: Pixel-Based

Over Difference Line Threshold Value shall not exceed 0x190.

Address: 8C-06~07 Reserved to 0

TCON Horizontal/Vertical Timing Setting

Address: 8C-08 TCON [0]_VS_LSB (TCON [0] Vertical Start LSB Register)

Bit	Mode	Function
7:0	W	Line number [7:0] at which TCON control generation begins

Address: 8C-09 TCON [0]_VS_MSB (TCON [0] Vertical Start/End MSB Register)

Bit	Mode	Function
7:4	W	Line number [11:8] at which TCON control generation ends
3:0	W	Line number [11:8] at which TCON control generation begins

Address: 8C-0A TCON [0]_VE_LSB (TCON [0] Vertical End LSB Register)

Bit	Mode	Function
7:0	W	Line number [7:0] at which TCON control generation ends

Address: 8C-0B TCON [0]_HS_LSB (TCON [0] Horizontal Start LSB Register)

Bit	Mode	Function
7:0	W	Pixel count [7:0] at which TCON goes active

Address: 8C-0C TCON [0]_HS_MSB (TCON [0] Horizontal Start/End MSB Register)

Bit	Mode	Function
7:4	W	Pixel count [11:8] at which TCON goes inactive
3:0	W	Pixel count [11:8] at which TCON goes active

To be triggered on rising edge of the DCLK

Address: 8C-0D TCON [0]_HE_LSB (TCON [0] Horizontal End LSB Register)

Bit	Mode	Function
7:0	W	Pixel count [7:0] at which TCON goes inactive

If the register number is large than display format, the horizontal component is always on.



Real TCON_HS = TCON_HS-4, Real TCON_HS = TCON_HS-4

Address: 8C-0E TCON [0]_CTRL (TCON [0] Control Register)

Default: 00h

Bit	Mode	Function
7	R/W	TCON [n] Enable (Local) 0: Disable (TCON [n] output clamp to ‘0’) (Default) 1: Enable
6	R/W	Polarity Control 0: Normal output (Default) 1: Inverted output
5:4	--	Reserved to 0
3	R/W	Toggle Circuit Enable/Disable 0: Normal TCON output (Default) 1: Toggle Circuit enable When using toggle circuit enable mode, the TCON[n] will be 1 clock earlier than TCON[n-1] and then toggling together, finally output will be 1 clock delay comparing to toggling result.
2:0	R/W	TCON [13:10] & TCON [7:4] (TCON Combination Select) TCON [13] has inactive data controller function. TCON [13]~[10] has dot masking function TCON [7] has flicking reduce function. 000: Normal TCON output (Default) 001: Select TCON [n] “AND” with TCON [n-1] 010: Select TCON [n] “OR” with TCON [n-1] 011: Select TCON [n] “XOR” with TCON [n-1] 100: Select TCON [n-1] rising edge as toggle trigger signal (when toggle enable) 101: Select TCON [n-1] rising edge as toggle trigger signal, then “AND” (when toggle enable) 110: Select TCON [n-1] rising edge as toggle trigger signal, then “OR” (when toggle enable) 111: Select TCON [n] and TCON [n-1] on alternating frames. <hr/> TCON [9:8] (TCON Combination Select) 000: Normal TCON output 001: Select TCON [n] “AND” with TCON [n-1] 010: Select TCON [n] “OR” with TCON [n-1] 011: Select TCON [n] “XOR” with TCON [n-1] 100: Select TCON [n-1] rising edge as toggle trigger signal (when toggle enable) 101: Select TCON [n-1] rising edge as toggle trigger signal, then “AND” (when toggle enable) 110: Select TCON [n-1] rising edge as toggle trigger signal, then “OR” (when toggle enable) 111: Select TCON [n] and TCON [n-1] reference ODD signal as alternating frames.



	<p>TCON [3] (TCON Combination Select)</p> <p>000: Normal TCON output</p> <p>001: Select TCON [3] “AND” with TCON [2]</p> <p>010: Select TCON [3] “OR” with TCON [2]</p> <p>011: Select TCON [3] “XOR” with TCON [2]</p> <p>100: Select TCON [2] rising edge as toggle trigger signal (when toggle enable)</p> <p>101: Select TCON [2] rising edge as toggle trigger signal, then “AND” (when toggle enable)</p> <p>110: Select TCON [2] rising edge as toggle trigger signal, then “OR” (when toggle enable)</p> <p>111: Select reset(ODD=0) or set(ODD=1) TCON [3] by DVS, when toggle function enable</p>
	<p>TCON [2] (Clock Toggle Function)//toggle function is inactive</p> <p>00x: Normal TCON output</p> <p>010: Select DCLK/2 when TCON [2] is “0”</p> <p>011: Select DCLK/2 when TCON [2] is “1”</p> <p>100: Select DCLK/4 when TCON [2] is “0”</p> <p>101: Select DCLK/4 when TCON [2] is “1”</p> <p>110: Select DCLK/8 when TCON [2] is “0”</p> <p>111: Select DCLK/8 when TCON [2] is “1”</p>
	<p>TCON [1]</p> <p>xx0: Normal TCON output</p> <p>xx1: Reverse-Control Signal output</p>
	<p>TCON [0]</p> <p>00x: Normal TCON output</p> <p>010: EVEN “REV” 18/24-bit function (“REV0” on TCON [0]) ODD “REV” 18/24-bit function (“REV1” on TCON [1])</p> <p>011: ALL “REV” 36/48-bit function (“REV” on TCON [0], can also on TCON [1])</p> <p>100: EVEN data Output Inversion Controlled by TCON [0] is “0” ODD data Output Inversion Controlled by TCON [1] is “0”</p> <p>101: EVEN data Output Inversion Controlled by TCON [0] is “1” ODD data Output Inversion Controlled by TCON [1] is “1”</p>

Dot Masking

Address: 8C-5F/67/6F/77 TC_DOT_MASKING_CTRL

Default: 00h



Bit	Mode	Function
7:3	R/W	Reserved to 0
2	R/W	Red Dot Masking Enable 0: Disable (Default) 1: Enable
1	R/W	Green Dot Masking Enable 0: Disable (Default) 1: Enable
0	R/W	Blue Dot Masking Enable 0: Disable (Default) 1: Enable

When applying dot masking, the timing setting for TCON will be

Real TCON_Mask_STA = TCON_STA+2

Real TCON_Mask_END = TCON_END +2

TCON [0] ~ TCON [13] Control Registers Address Map

Address	Data(# bits)	Default
0A,09,08	TCON [0]_VS_REG (11)	
0D,0C,0B	TCON [0]_HS_REG (11)	
0E	TCON [0]_CTRL_REG	00
0F	Reserved	
12,11,10	TCON [1]_VS_REG (11)	
15,14,13	TCON [1]_HS_REG (11)	
16	TCON [1]_CTRL_REG	00
17	Reserved	
1A,19,18	TCON [2]_VS_REG (11)	
1D,1C,1B	TCON [2]_HS_REG (11)	
1E	TCON [2]_CTRL_REG	00
1F	Reserved	
22,21,20	TCON [3]_VS_REG (11)	
25,24,23	TCON [3]_HS_REG (11)	
26	TCON [3]_CTRL_REG	00
27	Reserved	



2A,29,28	TCON [4]_VS_REG (11)	
2D,2C,2B	TCON [4]_HS_REG (11)	
2E	TCON [4]_CTRL_REG	00
2F	Reserved	
32,31,30	TCON [5]_VS_REG (11)	
35,34,33	TCON [5]_HS_REG (11)	
36	TCON [5]_CTRL_REG	00
37	Reserved	
3A,39,38	TCON [6]_VS_REG (11)	
3D,3C,3B	TCON [6]_HS_REG (11)	
3E	TCON [6]_CTRL_REG	00
3F	Reserved	
42,41,40	TCON [7]_VS_REG (11)	
45,44,43	TCON [7]_HS_REG (11)	
46	TCON [7]_CTRL_REG	00
47	Reserved	
4A,49,48	TCON [8]_VS_REG (11)	
4D,4C,4B	TCON [8]_HS_REG (11)	
4E	TCON [8]_CTRL_REG	00
4F	Reserved	
52,51,50	TCON [9]_VS_REG (11)	
55,54,53	TCON [9]_HS_REG (11)	
56	TCON [9]_CTRL_REG	00
57	Reserved	
5A,59,58	TCON [10]_VS_REG (11)	
5D,5C,5B	TCON [10]_HS_REG (11)	
5E	TCON [10]_CTRL_REG	00
5F	TCON [10]_CTRL_REG	



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62,61,60	TCON [11]_VS_REG (11)	
65,64,63	TCON [11]_HS_REG (11)	
66	TCON [11]_CTRL_REG	00
67	TCON [11]_CTRL_REG	00
6A,69,68	TCON [12]_VS_REG (11)	
6D,6C,6B	TCON [12]_HS_REG (11)	
6E	TCON [12]_CTRL_REG	00
6F	TCON [12]_CTRL_REG	00
72,71,70	TCON [13]_VS_REG (11)	
75,74,73	TCON [13]_HS_REG (11)	
76	TCON [13]_CTRL_REG	00
77	TCON [13]_CTRL_REG	00

Control for LVDS

Address: 8C-A0

LVDS_CTRL0

Default: 00h

Bit	Mode	Function
7	R/W	Power Up LVDS IBGen 0: Power down (Default) 1: Normal
6	R/W	Reserved
5	R/W	Power Up LVDS Even-Port (pin 86~95) 0: Power down (Default) 1: Normal
4	R/W	Power Up LVDS Odd-Port (pin 74~83) 0: Power down (Default) 1: Normal
3:2	R/W	Watch Dog Model 00: Enable Watch Dog(Default) 01: Keep PLL VCO = 1V 1x: Disable Watch Dog
1	R/W	LVDS bit type 0: 8 bits (pin 74~83, 86~95) 1: 10bits (useless, because there is no 10b lvds function)



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0	R	Watch Dog Control Flag 0: Watch dog not active (Default) 1: Watch dog active, Reset PLL and set VCO = 0.9V
---	---	---

Address: 8C-A1 LVDS_CTRL1 Default: 14h

Bit	Mode	Function
7	R/W	CKLAGL(Odd port) : Inverse the CK7X 0: lead (Default) 1: lag T/14
6	R/W	CKLAGL(Even Port) : Inverse the CK7X 0: lead (Default) 1: lag T/14
5:3	R/W	STSTL [2:0]: select test attribute 000: WD 001: VCOM 010: IB40u (default) 011: IBVOCM 100: PLLTST-fbak 101: PLLTST-fin 110: LVTST-CKDIN 111: LVTST-LVDSIN[6]
2:0	R/W	LVDS Output Common Mode (Default: 100) 000 : 1.07v 001 : 1.12v 010 : 1.17v 011 : 1.22v 100 : 1.29v (Default) 101 : 1.33v 110 : 1.38v 111 : 1.43v

Address: 8C-A2 LVDS_CTRL2 Default: 43h

Bit	Mode	Function
7:6	R/W	SBGL 00: 1.164V 01: 1.244V (Default) 10: 1.324V 11: 1.404V
5	R/W	ENIB40UX2L: Double the LVDS output swing 0: 1X



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		1: 2X
4	R/W	SIBXL : select 20uA source If DISP_TYPE=LVDS 0: from Bandgap (Default) 1: from ADC
3	R/W	PLL lock edge 0: positive 1: negative
2:0	R/W	SIBGENL (LVDS Current Source correction) 000 : 25uA/62.5uA 001 : 30uA/75uA 010 : 35uA/87.5uA 011 : 40uA/100uA (Default) 100 : 45uA/112.5uA 101 : 50uA/125uA 110 : 55uA/137.5uA 111 : 60uA/150uA

Address: 8C-A3

LVDS_CTRL3

Default: 1Ch

Bit	Mode	Function
7	R/W	ENVBPBL: Enable VCO_D2S Current Up 0: disable (Default) 1: enable
6	R/W	LVDS Mirror 0: Normal (TXE3+, TXE3-, TXEC+, TXEC-, TXE2+, TXE2-, TXE1+, TXE1-, TXE0+, TXE0-, TXO3+, TXO3-, TXOC+, TXOC-, TXO2+, TXO2-, TXO1+, TXO1-, TXO0+, TXO0-) 1: Mirror (TXE0-, TXE0+, TXE1-, TXE1+, TXE2-, TXE2+, TXEC-, TXEC+, TXE3-, TXE3+, TXO0-, TXO0+, TXO1-, TXO1+, TXO2-, TXO2+, TXOC-, TXOC+, TXO3-, TXO3+)
5:3	R/W	SIL [2:0] : PLL charge pump current ($I = 5\mu A + 5\mu A * \text{code}$) (Default: 011)
2:1	R/W	SRL [1:0] : PLL resistor ($R = 6K + 2K * \text{code}$) (Default: 10)
0	R/W	BMTS: Bit-Mapping Table Select 0: Table 1 (Default) 1: Table 2

TCLK+

LVDS	Bit 1	Bit 0	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Bit 6	Bit 5
TXE0	ER1	ER0	EG0	ER5	ER4	ER3	ER2	ER1	ER0	EG0	ER5
TXE1	EG2	EG1	EB1	EB0	EG5	EG4	EG3	EG2	EG1	EB1	EB0
TXE2	EB3	EB2	DEN	VS	HS	EB5	EB4	EB3	EB2	DEN*6	VS*5



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TXE3	ER7	ER6	RSV	EB7	EB6	EG7	EG6	ER7	ER6	RSV*7	EB7
TXO0	OR1	OR0	OG0	OR5	OR4	OR3	OR2	OR1	OR0	OG0	OR5
TXO1	OG2	OG1	OB1	OB0	OG5	OG4	OG3	OG2	OG1	OB1	OB0
TXO2	OB3	OB2	DEN	VS	HS	OB5	OB4	OB3	OB2	DEN*2	VS*1
TXO3	OR7	OR6	RSV	OB7	OB6	OG7	OG6	OR7	OR6	RSV*3	OB7

TABLE 1 Bit-Mapping 6bit(5~0)+2bit(7~6)



LVDS	Bit 1	Bit 0	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Bit 6	Bit 5
TXE0	ER3	ER2	EG2	ER7	ER6	ER5	ER4	ER3	ER2	EG2	ER7
TXE1	EG4	EG3	EB3	EB2	EG7	EG6	EG5	EG4	EG3	EB3	EB2
TXE2	EB5	EB4	DEN	VS	HS	EB7	EB6	EB5	EB4	DEN*6	VS*5
TXE3	ER1	ER0	RSV	EB1	EB0	EG1	EG0	ER1	ER0	RSV*7	EB1
TXO0	OR3	OR2	OG2	OR7	OR6	OR5	OR4	OR3	OR2	OG2	OR7
TXO1	OG4	OG3	OB3	OB2	OG7	OG6	OG5	OG4	OG3	OB3	OB2
TXO2	OB5	OB4	DEN	VS	HS	OB7	OB6	OB5	OB4	DEN*2	VS*1
TXO3	OR1	OR0	RSV	OB1	OB0	OG1	OG0	OR1	OR0	RSV*3	OB1

TABLE 2 Bit-Mapping 6bit(7~2)+2bit(1~0)

Address: 8C-A4

LVDS_CTRL4

Default: 80h

Bit	Mode	Function
7:6	R/W	E_RSV: even port reserve signal select 11: Always '1' 10: Always '0' 01: TCON [11] 00: PWM_0
5:4	R/W	E_DEN: even port data enable signal select 11: Always '1' 10: Always '0' 01: TCON [9] 00: DENA
3:2	R/W	E_VS: even port VS signal select 11: Always '1' 10: DENA 01: TCON [7] 00: DVS
1:0	R/W	E_HS: even port HS signal select 11: Always '1' 10: DENA 01: TCON [5] 00: DHS



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Address: 8C-A5**LVDS_CTRL5****Default: 80h**

Bit	Mode	Function
7:6	R/W	O_RSV: odd port reserve signal select 11: Always '1' 10: Always '0' 01: TCON [13] 00: PWM_1
5:4	R/W	O_DEN: odd port data enable signal select 11: Always '1' 10: Always '0' 01: TCON [9] 00: DENA
3:2	R/W	O_VS: odd port VS signal select 11: Always '1' 10: DENA 01: TCON [7] 00: DVS
1:0	R/W	O_HS: odd port HS signal select 11: Always '1' 10: DENA 01: TCON [5] 00: DHS

Address: 8C-A6**LVDS_CTRL6****Default: 00h**

Bit	Mode	Function
7:4	--	Reserved to 0
3	R/W	Odd DALAGL: Inverse the Data port 0: lead (Default) 1: lag T/14
2	R/W	Even DALAGL: Inverse the Data port 0: lead (Default) 1: lag T/14
1	R/W	ENDUL: TXEC even port clock pair current double 0: 1X Default) 1: 2X
0	R/W	Power Up LVDS PLL (global power down/ global power saving CR_01[2:1] have higher priority) 0: Power down (Default)



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		1: Normal
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Address: 8C-A7**LVDS_CTRL7****Default: 00h**

Bit	Mode	Function
7:4	R/W	Even DATA port skew control SKEW=50ps x ESKEWL[3:0]
3:0	R/W	Odd DATA port skew control SKEW=50ps x OSKEWL[3:0]

Address: 8C-A8**LVDS_CTRL8****Default: 00h**

Bit	Mode	Function
7:4	R/W	Even B clock port skew control SKEW=50ps x ESKEWCKBL[3:0] (skew period must be less than $\frac{1}{2} \times T/7$)
3:0	R/W	Even D clock port skew control SKEW=50ps x ESKEWCKDL[3:0] (skew period must be less than $\frac{1}{2} \times T/7$)

Address: 8C-A9**LVDS_CTRL9****Default: 00h**

Bit	Mode	Function
7:4	R/W	Odd B clock port skew control SKEW=50ps x OSKEWCKBL[3:0] (skew period must be less than $\frac{1}{2} \times T/7$)
3:0	R/W	Odd D clock port skew control SKEW=50ps x OSKEWCKDL[3:0] (skew period must be less than $\frac{1}{2} \times T/7$)

Address: 8C-C0**RSDS Output Control****Default: 00h**

Bit	Mode	Function
7:1	R/W	Reserved to 0
0	R/W	LVDS Differential pair PN swap (data) (Also refer to <u>CR29[6:4]</u>) 0: No Swap (Default) 1: Swap



Test function

Register::Pin_config_Addr_Port						0x8D
Name	Bit	R/W	Default	Description	Config	
Pin_config_Addr_Port	7:0	R/W	00	Address port for pin configuration control access		

Register::Pin_config_Data_Port						0x8E
Name	Bit	R/W	Default	Description	Config	
Pin_config_Data_Port	7:0	R/W	00	Data port for pin configuration control access		

Pin 55	TCON[0]	TCON[5]	
Pin 56	TCON[1]	TCON[4]	
Pin 57	TCON[9]	TCON[11]	
Pin 58	TCON[7]	TCON[10]	
Pin 59	TCON[3]	TCON[5]	
Pin 63	TCON[1]	TCON[8]	
Pin 64	TCON[0]	TCON[7]	
Pin 65	TCON[1]	TCON[7]	
Pin 66	TCON[2]	TCON[4]	
Pin 67	TCON[5]	TCON[9]	
Pin 68	TCON[3]	TCON[13]	
Pin 69	TCON[3]	TCON[7]	
Pin 70	TCON[9]	TCON[11]	
Pin 71	TCON[8]	TCON[10]	
Pin 72	TCON[6]	TCON[12]	
Pin 99	TCON[6]	TCON[11]	
Pin 100	TCON[3]	TCON[12]	
Pin 101	TCON[0]		
Pin 102	TCON[10]		
Pin 103	TCON[8]		
Pin 104	TCON[5]		
Pin 105	TCON[9]		
Pin 108	TCON[7]		
Pin 109	TCON[3]		
Pin 110	TCON[2]	TCON[6]	TCON[7]
Pin 111	TCON[4]	TCON[7]	
Pin 112	TCON[5]	TCON[9]	
Pin 113	TCON[1]	TCON[11]	
Pin 114	TCON[0]	TCON[13]	



Name	8D-00[7] = 1'b0	8D-00[7] = 1'b1	PLL clock	scan	72pin	128pin
PAD_GPIO119				scan_mode	62	119
PAD_TXO3P			audio_pll	si[0]	37	74
PAD_TXO3N				si[1]	38	75
PAD_TXO2P	tst[0]	tst[0]	ck108_pll27x	si[2]	39	78
PAD_TXO2N	tst[1]	tst[1]		si[3]	40	79
PAD_TXO1P	tst[2]	tst[16]		fav4	41	80
PAD_TXO1N	tst[3]	tst[17]		si[5]	42	81
PAD_TXOOP	tst[4]	tst[18]		xclk	si[6]	82
PAD_TXOON	tst[5]	tst[19]			si[7]	83
PAD_TXE3P	tst[6]	tst[20]		dpll	so[0]	45
PAD_TXE3N	tst[7]	tst[21]			so[1]	46
PAD_TXECP	tst[8]	tst[22]		test2out	so[2]	47
PAD_TXECN	tst[9]	tst[23]			so[3]	48
PAD_TXE2P	tst[10]	tst[24]		dpll_status	so[4]	49
PAD_TXE2N	tst[11]	tst[25]			so[5]	50
PAD_TXE1P	tst[12]	tst[26]		test1out	so[6]	51
PAD_TXE1N	tst[13]	tst[27]			so[7]	52
PAD_TXEOP	tst[14]	tst[28]		m2pll		93
PAD_TXEON	tst[15]	tst[29]				53
PAD_TCON0				scan_en		94
PAD_GPIO63				scan_clk		54
						95
						64
						63



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72 pin	128 pin		GPIO	Scan	Test Mode	Clock Out
71	1	TMDS_VDD				
72	2	PAD_REXT				
1	3	PAD_RX2P0				
2	4	PAD_RX2N0				
3	5	PAD_RX1P0				
4	6	PAD_RX1N0				
5	7	PAD_RX0P0				
6	8	PAD_RX0N0				
7	9	PAD_RXCP0				
8	10	PAD_RXCN0				
	11	TMDS_GND				
	12	PAD_RX2P1				
	13	PAD_RX2N1				
	14	PAD_RX1P1				
	15	PAD_RX1N1				
	16	PAD_RX0P1				
	17	PAD_RX0N1				
	18	PAD_RXCP1				
	19	PAD_RXCN1				
	20	TMDS_VDD				
9	21	PAD_AVSO			AVS_I	
10	22	PAD_AHSO			AHS_I	
11	23	ADC_VDD12_GDI				
11	23	ADC_VDD12				
12	24	PAD_BIN0N				
13	25	PAD_BIN0P				
14	26	PAD_GIN0N				
15	27	PAD_GIN0P				
	28	PAD_SOGINO				
16	29	PAD_RIN0N				
17	30	PAD_RIN0P				
	31	PAD_BIN1N	PD.7		V8[7]_I	
	32	PAD_32	PD.6		V8[6]_I	
	33	PAD_33	PD.5		V8[5]_I	
	34	PAD_34	PD.4		V8[4]_I	
	35	PAD_35	PD.3		V8[3]_I	
	36	PAD_36	PD.2		V8[2]_I	
	37	PAD_37	PD.1	si[0]	V8[1]_I	
18	38	ADC_GND12		si[1]		
18	38	ADC_GNDOFF				
18	38	ADC_AUD_GNDOFF				
18	38	Audio_ADC_GND				
19	39	PAD_39	PD.0	si[2]	V8[0]_I	
20	40	PAD_40	PC.4	si[3]		
	41	PAD_VIN0P	PB.7	si[4]		
	42	PAD_VIN0N	PB.6	si[5]		
	43	PAD_VIN1P	PB.5	si[6]		
	44	PAD_VIN1N	PB.4	si[7]		
	45	PAD_VIN2P	PB.3	so[0]		
	46	PAD_VIN2N	PB.2	so[1]		
	47	PAD_VIN3P	PB.1	so[2]		
	48	PAD_VIN3N	PB.0	so[3]		
	49	AVDD_SARADC_APAD		so[4]		
	49	AVDD_BB0_APAD				
	49	AVDD_BB1_DACVREF_APAD				
21	50	PAD_ADCA0	P6.0	so[5]		
22	51	PAD_ADCA1	P6.1	so[6]		
23	52	PAD_ADCA2	P6.2	so[7]		
24	53	PAD_ADCA3	P6.3			
	54	PAD_ADCA4	P6.4			
25	55	PAD_ADCB0	P6.5		DCLK_I	
26	56	PAD_ADCB1	P6.6		ADC_CLK_I	
27	57	PAD_ADCB2	P6.7		M2PLL_CLK_I	
28	58	PAD_DDCSCL1	P3.0/RXD(I/O)		HDMI_CP_ACLK_I	
72 pin	128 pin		GPIO 103	Scan	Test Mode	Clock Out
29	59	PAD_DDCSDA1	P3.1/TXD(O)		HDMI_CP_CLK_I	
30	60	PAD_VCCK				
	61	PAD_GND				



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72 pin	128 pin		GPIO	Scan	Test Mode	Clock Out
29	59	PAD_DDCSDA1	P3.1/TXD(O)		HDMI CP CLK I	
30	60	PAD_VCCK				
	61	PAD_GND				
31	62	PAD_PVCC		scan_mode		
32	63	PAD_GPIO63	PC.3 /INT0(I)	scan_clk		
33	64	PAD_TCON0	P1.0/T2(I) /INT1(I)	scan_en		clk_pll27x
34	65	PAD_TCON1	P1.1/T2EX(I)			
35	66	PAD_TCON2	P1.2/CLKO2(O)			
36	67	PAD_TCON5	P1.3			
	68	PAD_TCON13	P1.4			
	69	PAD_TCON3	P1.5			
	70	PAD_TCON9	P1.6			
	71	PAD_TCON8	P1.7			
	72	PAD_TCON6	PC.2			
	73	PAD_VCCK				
37	74	PAD_TXO3P	P9.0			audio_pll
38	75	PAD_TXO3N	P9.1			
	76	PAD_TXOCP	P9.2			
	77	PAD_TXOCN	P9.3			
39	78	PAD_TXO2P	P9.4		Test_IO[0]	ck108_pll27x
40	79	PAD_TXO2N	PA.0		Test_IO[1]	
41	80	PAD_TXO1P	PA.1		Test_IO[2]	fav4
42	81	PAD_TXO1N	PA.2		Test_IO[3]	
43	82	PAD_TXO0P	PA.3		Test_IO[4]	xclk
44	83	PAD_TXO0N	PA.4		Test_IO[5]	
	84	PAD_PVCC				
	85	PAD_PGND				
45	86	PAD_TXE3P			Test_IO[6]	dpll
46	87	PAD_TXE3N			Test_IO[7]	
47	88	PAD_TXECP			Test_IO[8]	test2out
48	89	PAD_TXEBCN			Test_IO[9]	
49	90	PAD_TXE2P			Test_IO[10]	dpll status
50	91	PAD_TXE2N			Test_IO[11]	
51	92	PAD_TXE1P			Test_IO[12]	test1out
52	93	PAD_TXE1N			Test_IO[13]	
53	94	PAD_TXE0P			Test_IO[14]	m2pll
54	95	PAD_TXEON			Test_IO[15]	
	96	PAD_PWM0	P5.2		Test_IO[16]	
	97	PAD_PWM1	P5.3		Test_IO[17]	
	98	PAD_PWM2	P5.4		Test_IO[18]	
	99	PAD_PWM3	P5.5		Test_IO[19]	
	100	PAD_PWM4	P5.6		Test_IO[20]	
	101	PAD_PWM5	P5.7		Test_IO[21]	
	102	PAD_SPDIF3	P7.6		Test_IO[22]	
55	103	PAD_SPDIF2	P7.5		Test_IO[23]	
56	104	PAD_SPDIF1	P7.4		Test_IO[24]	
	105	PAD_SPDIFO	P8.0		Test_IO[25]	
57	106	PAD_PVCC				
	107	PAD_PGND				
	108	PAD_MCK	P8.1/CLKO1(O)		Test_IO[26]	
	109	PAD_SCK	P3.2/INT0(I)		Test_IO[27]	
	110	PAD_WS	P3.3/INT1(I)		Test_IO[28]	
	111	PAD_SD0	P3.4/T0		Test_IO[29]	
	112	PAD_SD1	P3.5(BS)/T1			
	113	PAD_SD2	P3.6			
	114	PAD_SD3	P3.7			
58	115	PAD_SPI_SCLK				
59	116	PAD_SI				
60	117	PAD_SO				
61	118	PAD_CS				
62	119	PAD_GPIO119	PC.1			
63	120	PAD_VCCK				



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72 pin	128 pin		GPIO	Scan	Test Mode	Clock Out
63	120	PAD_VCCK				
64	121	PAD_DDCSCL3	P7.3			
65	122	PAD_DDCSDA3	P7.2			
66	123	PAD_DDCSDA2	P7.1		ISP_DDCSCL	
67	124	PAD_DDCSCL2	P7.0		ISP_DDCSDA	
68	125	PAD_RESETB				
	126	PAD_126	PC.0			
69	127	PAD_XO				
70	128	PAD_XI				

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Register::TEST_MODE						0x00
Name	Bit	R/W	Default	Description	Config	
Select_data_test_mode	7	R/W	0	<p>Select Data Test mode LSB</p> <p>A. for 72 pin, pin54~45, 44~39</p> <p>0 : select Data test mode [15:0] 1: select Data test mode [29:16],[1:0]</p> <p>B. for 128 pin, pin95~86, 83~78</p> <p>0 : select Data test mode [15:0] 1 : select Data test mode [29:16],[1:0]</p> <p>pin 111~108, 105~96 is Data test mode [29:16]</p>		
Test mode select	6:5	R/W	00	<p>00:Normal 01:test_output mode Others are Reserved</p>		
Test_output_Mode	4	R/W	0	<p>0:Select Data test mode Select Data test output to 128pin 95~86, 83~78 or 64pin 49~40, 38~33 depend on bit7, bit3~bit0</p> <p>1:PLL test mode {dpll, m2pll, tie to GND, tie to GND , IOSC, ck108_pll27x, dpllstatus,test1out, test2out, fav4, xclk, dpll(digital pad)} will be outputted to 128 pin {86, 94, X, X, 64, 90, 92, 88, 80, 82, 126} or 72 pin {40, 48, 31, X, 30, 33, 44, 46, 42, 35, 37} when set to 1, clock frequency of some test pin could be divided by assigning its corresponding TST_CLK_CTRL</p>		
Data_Test_mode	3:0	R/W	0	<p>0000: 1'b0, Z0TST[3:0], pclk_tst, Red[9:2], Green[9:2], Blue[9:2] through VGIP</p> <p>0001: 1'b0, Z0TST[3:0], adc_clk, Blue[7:0], Red[7:0], Green[7:0]After Scale Down</p> <p>0010: Z0TST[3:0], adc_clk, IVS_DLY,</p>		



				IHS_DLY, IFD_ODD, IENA, VSD_DEN, VSD_ACT, Auto_hs, Auto_vs, auto_field, 1'b0, COAST, test_s1, test_s2, CLAMP_G/CLAMP_BR, CLAMP_G/CLAMP_BR, SOG_IN0, SOG_IN1, FAV4, final_pe_com, t_s[1:0], pe_extrab, high_88, recur_delay_chain_en, high_127 0011: adc_clk, MCUWR, MCURD, MCU_ADR_INC, MIN[7:0], MCUWR, MCURD, MADR[7:0], MPLL_SDMOUT_TST[3:0], SDMOUT_TST[3:0] 0100: 1'b0, adc_clk, RAW_VS, RAW_HS, RAW_ODD, RAW_DEN, SDMOUT_TST[3:0], Green[9:0], Red[9:0] through VGIP 0101: 1'b0, adc_clk, Red[9:0], Green[9:0], raw_vs, raw_hs, en_flag, meas_ihs, HSOUT_sync_proc, coast, CLAMP_G, CLAMP_BR 0110: 1'b0, adc_clk, raw_vs, raw_hs, test_s1, test_s2, raw_filed, Blue[9:0], Green[9:0], hs0_schmitt, hs1_schmitt, ~appl_por 0111: 3'b0, adc_clk, Green[9:0], iclk_tst, raw_vs, raw_hs, raw_filed, fifo_clk, internal_crystal, test_s1, test_s2, sync_pro_tst[7:0] 1000: reserved 1001: VSDMAIN test mode: pclk_tst,, vsd_pr[7:0], vsd_y[7:0], vsd_pb[7:0, den, dvs, dhs, ch 1_ivs, vsd_den, 1010: Reserved	
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				<p>1011: color processor test mode output</p> <p>1100: Embedded MCU test out mode</p> <p>1101: HDMI test in mode</p> <p>HDMI_TST_IN [0:29] will be assigned to {124~121, 114~108, 105~100, 72~64, 54~51}</p> <p>1110: HDMI test out mode</p> <p>HDMI_TST_OUT [0:29] will be assigned to {111~108, 105~96 , 95~86, 83~78 }</p> <p>1111: 6'b0, new_fifo_odata_g, new_fifo_odata_b, new_fifo_odata_r When set to 0010/0110/0111,test_s1 & test_s2 can be assigned by "Select_Tst_s1s2"</p> <p>Others are reserved</p>	
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Register::TST_CLK_CTRL0					0x01
Name	Bits	Read/ Write	Reset State	Comments	Config
DPLL_OEN	7	R/W	0	DPLL frequency output enable 0: output disabled 1: output enabled	
M2pll_OEN	6	R/W	0	M2PLL frequency output enable 0: output disabled 1: output enabled	
Reserved	4	R/W	0	Reserved to 0	
Reserved	4	R/W	0	Reserved to 0	
CLK108_PLL27X_OEN	3	R/W	0	CLK108_PLL27X frequency output enable (M_domain clk, refer to CR_22[1:0]) 0: output disabled 1: output enabled	
Test1out_OEN	2	R/W	0	Test1out frequency output enable 0: output disabled 1: output enabled	
Test2out_OEN	1	R/W	0	Test2out frequency output enable 0: output disabled 1: output enabled	
Fav4_OEN	0	R/W	0	Fav4 frequency output enable 0: output disabled	



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				1: output enabled	
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Register::TST_CLK_CTRL1					0x02
Name	Bits	Read/ Write	Reset State	Comments	Config
XCLK_OEN	7	R/W	0	XCLK frequency output enable 0: output disabled 1: output enabled	
CKT_PLL27X_OEN	6	R/W	0	CKT_PLL27X frequency output enable 0: output disabled 1: output enabled	
Rev	5:0	---	---	Reserved	

Register::TST_CLK_CTRL2					0x03
Name	Bit	R/W	Default	Description	Config
Rev	7:6	---	---	Reserved	
DPLL_DIV_CTRL	5:4	R/W	00	DPLL frequency is divided by 00:1 01:2 10:4 11:8	
M2pll_DIV_CTRL	3:2	R/W	11	M2PLL frequency is divided by 00:1 01:2 10:4 11:8	
Rev	1:0	---	---	Reserved	

Register:: TST_CLK_CTRL3					0x04
Name	Bit	R/W	Default	Description	Config
Fav4_DIV_CTRL	7:6	R/W	00	Fav frequency is divided by 00:1 01:2 10:4 11:8	
Test1out_DIV_CTRL	5:4	R/W	00	Test1out frequency is divided by 00:1 01:2 10:4 11:8	



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Test2out_DIV_CTRL	3:2	R/W	00	Test2out frequency is divided by 00:1 01:2 10:4 11:8	
CLK108_pll27xDIV_CTRL	1	R/W	0	(M_domain clk DIV) 0:Divided by 1 1:Divided by 4	
Ckt_pll27xDIV_CTRL	0	R/W	0	0:divided by 1 1:divided by4	

Register:: Select_Tst_s1s2					0x05
Name	Bit	R/W	Default	Description	Config
Reserved	7	R/W	0	Reserved	
Select_Tst_s1	6:4	R/W	001	Select test function of test_s1 3'b000: DPLL clock (TIE LOW NOW) 3'b001: PLLS fbk clock 3'b010: CKOAD2(High Speed) 3'b011: PLL status 3'b100: HSOUT 3'b101: ADC clock(from PLLS)(High Speed) 3'b110: Empty Flag 3'b111: BVS(Video8)	
Reserved	3	R/W	0	Reserved	
Select_Tst_s2	2:0	R/W	010	Select test function of test_s1 3'b000: PLLS phase swallow clock (High speed) 3'b001: DPLL status(TIE LOW NOW) 3'b010: PLLS phase0 clock(High speed) 3'b011: M2PLL clock(Not in APLL) 3'b100: HSFB 3'b101: TP2_MX5 3'b110: Full Flag 3'b111: BHS(Video8)	



Register:: Select_Tstinclock						0x06
Name	Bit	R/W	Default	Description	Config	
DPLL_TST_IN	7	R/W	0	0:Normal 1:DCLK enter from pin 55 50		
ADCPLL_TST_IN	6	R/W	0	0:Normal 1:ADC CLK enter from pin 56-51		
M2PLL_TST_IN	5	R/W	0	0:Normal 1:M2PLL CLK enter from pin 57 52		
HDMI_CP_ACLK_TST_IN	4	R/W	0	0:Normal 1:HDMI_CP_ACLK enter from pin 58		
HDMI_CP_CLK_TST_IN	3	R/W	0	0:Normal 1:HDMI_CP_CLK enter from pin 59		
SCAN_CLK_TST_IN	2	R/W	1	0:Normal 1:SCAN CLK enter from pin 9863		
DPLL_NDIV2_EN	1	R/W	0	DPLL Test Mode Divider Enable 0:use pin 50 div2 as dclk 1:use pin 50 as dclk		
Reserved	0	R/W	0	Reserved		

TEST MODE in FIFO

Register:: ADC TEST MODE						0x07
Name	Bit	R/W	Default	Description	Config	
ADC_TEST_MODE	7	R/W	0	0:Disable 1:Enable		
ADC_TEST_MODE_2	6	R/W	0	Useless		
FIFO_TEST_MODE	5	R/W	0	0:Disable 1:Enable test the CRC from FIFO , and open the Pattern Gen to d domain. Pattern Gen Seed (R = 01,G=00,B=00)		
ADC_TEST_START	4	R	0	Under ADC_TEST_MODE = 1, ADC_TEST_START will high when the new fifo is full , then read out data from		



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				FIFO by sending DCLK from outside test pin.	
Rev	3:0	---	---	Reserved	

Register:: ADC TEST MODE ADDR MSB					0x08
Name	Bit	R/W	Default	Description	Config
ADC_TEST_ADDR[1:0]	7:6	R/W	0X00	Read the FIFO initial Addr.	
Rev	5:0	---	---	Reserved	

Register:: ADC TEST MODE ADDR LSB					0x09
Name	Bit	R/W	Default	Description	Config
ADC_TEST_ADDR[7:0]	7:0	R/W	0X04	Read the FIFO initial Addr.	

Register:: ADC FIFO CRC					0x0A
Name	Bit	R/W	Default	Description	Config
NEW_FIFO_CRC[3:16]	7:0	R	0	NEW FIFO CRC	

Register:: ADC FIFO CRC					0x0B
Name	Bit	R/W	Default	Description	Config
NEW_FIFO_CRC[5:8]	7:0	R	0	NEW FIFO CRC	

Register:: ADC FIFO CRC					0x0C
Name	Bit	R/W	Default	Description	Config
NEW_FIFO_CRC[7:0]	7:0	R	0	NEW FIFO CRC	

Register:: Auto_soy_test					0x0D
Name	Bit	R/W	Default	Description	Config
Auto_soy_test_mode	7	R/W	0	0: Normal 1: Test mode clk will be from pin51 & 6 bits data will	



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				be from {pin 32~pin37}	
Auto_soy_test_sel	6:4	R/W	0	Test function sel	
Reserved	3:0	---	---	Reserved	

Embedded OSD

Address: 90 OSD_ADDR_MSB (OSD Address MSB 8-bit)

Bit	Mode	Function
7:0	R/W	OSD MSB 8-bit address

Address: 91 OSD_ADDR_LSB (OSD Address LSB 8-bit)

Bit	Mode	Function
7:0	R/W	OSD LSB 8-bit address

Address: 92 OSD_DATA_PORT (OSD Data Port)

Bit	Mode	Function
7:0	W	Data port for embedded OSD access

Refer to the embedded OSD application note for the detailed.

Address: 93 OSD_SCRAMBLE

Default: 05h

Bit	Mode	Function
7	R/W	BIST Start 0: stop (Default) 1: start (auto clear)
6	R	BIST Result 0: fail (Default) 1: success
5	R/W	BIST SELECT 0: 16.5K byte FONT SRAM 1: 192 byte LUT SRAM
4	R	Double_Buffer_Write_Status 0: double buffer write out is finish, or data write to double buffer is not ready, or no double buffer function. 1: after data write to dbuf and before dbuf write out, such that double buffer is busy.
3	R/W	OSDADRHSB 0: If initial address lower than or equal to 12K



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		1: If initial address higher than 12K The bit will be designed to control 16.5K bytes SRAM. However it will have no effect for WINDOW setting. Also please remember to set {OSDADRHSB, OSDADRMSB(CR90), OSDADRLSB(CR91) } again while you like to R/W a new address.
2:0	R/W	Double buffer depth (Default=6) 000~101=>1~6

Address: 94 OSD_TEST

Bit	Mode	Function
7:0	R/W	Testing Pattern

Digital Filter

Address: 98 DIGITAL_FILTER_CTRL

Default: 00h

Bit	Mode	Function
7:4	R/W	Access Port Write Enable 0000: disable 0001: phase access port 0010: negative smear access port 0011: positive smear access port 0100: negative ringing access port 0101: positive ringing access port 0110: mismatch access port 0111: Y(B)/Pb(G)/Pr(R) channel digital filter enable 1xxx: noise reduction access port
3:2	R/W	Two condition occur continuous (ringing to smear) 00: disable(hardware is off , depend on firmware) 01: only reduce ringing condition 10: only reduce smear condition 11: no adjust (hardware is on, but do nothing)
1	R/W	When noise reduction and mismatch occur, select 0: mismatch 1: noise reduction
0	--	Reserved to 0

Address: 99 DIGITAL_FILTER_PORT

Default: 00h

DIGITAL_FILTER_CTRL[7:4] =0 000 ~ 0110

Bit	Mode	Function



7	R/W	Y EN (G) : function enable 0: function disable 1: function enable
6	R/W	Pb EN (B) : function enable 0: function disable 1: function enable
5	R/W	Pr EN (R) : function enable 0: function disable 1: function enable
4	R/W	Initial value: 0: raw data 1: extension
3:0	--	Reserved to 0

DIGITAL_FILTER_CTRL[7:4] = 0000 ~0 110		
Bit	Mode	Function
7	R/W	EN : function enable 0: function disable 1: function enable
6:4	R/W	THD_OFFSET Threshold value of phase and mismatch and noise reduction or offset value of smear and ringing
3:2	R/W	DIV : divider value of phase and mismatch or offset value of smear and ringing 00: 0 01: 1 10: 2 11: 3
1:0	--	Reserved to 0

THD_OFFSET define:

The THD value definition of phase enhance function

Bit6~4	000	001	010	011	100	101	110	111
Value	112	128	144	160	176	192	208	224

The offset value definition of smear and ringing reduce function

Bit6~4	000	001	010	011	100	101	110	111
Value	no use	16	32	48	64	80	96	112

The THD value definition of mismatch enhance function

Bit6~4	000	XX1
Value	1	2



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The THD value definition of noise reduction function

Bit6~4	000	001	010	011	100	101	110	111
Value	0	1	2	3	4	5	6	7

Video Color Space Conversion

YUV2RGB

Register:: YUV2RGB_CTRL 0x9C					
Name	Bits	Read/Write	Reset State	Comments	Config
Dummy	7:2	R/W	0	Reserved	
Access	1	R/W	0	Enable YUV/RGB coefficient Access 0: Disable 1: Enable	
Enable	0	R/W	0	Enable YUV to RGB Conversion 0: Disable YUV-to-RGB conversion 1: Enable YUV-to-RGB conversion	

Register:: YUV2RGB_ACCESS 0x9D					
Name	Bits	Read/Write	Reset State	Comments	Config
Write_Enabled	7:3	R/W	0	YUV Coefficient Write Enable: 00000: K11 high byte 00001: K11 low byte 00010: K13 high byte 00011: K13 low byte 00100: K22 high byte 00101: K22 low byte 00110: K23 high byte 00111: K23 low byte 01000: K32 high byte 01001: K32 low byte 01010: Roffset high byte 01011: Roffset low byte 01100: Goffset high byte 01101: Goffset low byte 01110: Boffset high byte 01111: Boffset low byte 10000: Rgain high byte 10001: Rgain low byte 10010: Ggain high byte 10011: Ggain low byte 10100: Bgain high byte 10101: Bgain low byte 10110~11111: reserved	
Cb_Cr_Clamp	2	R/W	0	Cb Cr Clamp 0: Bypass 1: Cb-(128), Cr-(128)	
Y_Clamp	1	R/W	0	Y Clamp 0: Bypass 1: Y-(16)	



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Y Signed	0	R/W	0	Y Signed Selection 0: (Y-16)-> Unsigned 1: (Y-16)-> Signed	
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Register:: YUV_RGB_COEF_DATA					0x9E
Name	Bits	Read/Write	Reset State	Comments	Config
COEF	7:0	W	-	COEF DATA[7:0]	

$$\text{YUV/RGB matrix} \begin{bmatrix} R' \\ G' \\ B' \end{bmatrix} = \begin{bmatrix} K_{11} & 0 & K_{13} \\ K_{11} & -K_{22} & -K_{23} \\ K_{11} & K_{32} & 0 \end{bmatrix} \begin{bmatrix} Y \text{ or } (Y-16) \\ U \text{ or } (U-128) \\ V \text{ or } (V-128) \end{bmatrix} + \begin{bmatrix} R_{\text{offset}} \\ G_{\text{offset}} \\ B_{\text{offset}} \end{bmatrix}$$

Then,

$$\begin{bmatrix} R \\ G \\ B \end{bmatrix} = \begin{bmatrix} R_{\text{gain}} \times R' \\ G_{\text{gain}} \times G' \\ B_{\text{gain}} \times B' \end{bmatrix}$$

Where

- Y: S(9,0)./ U(9,0) when CR C0[0]=0
- U, V: S(8,0).
- K11: U(12, 10) 12 bits, 2 bit integer and 10-bit fractional bits. (Default: 0x0400h)
- K13: U(11, 10) 11 bits, 1 bit integer and 10-bit fractional bits (Default: 0x048Fh)
- K22, K23: U(10, 10) 10 bits, all fractional bits (Default: K22: 0x0194h, K23: 0x0252h)
- K32: U(12, 10) 12 bits, 2 bit integer and 10-bit fractional bits (Default: 0x0820h)
- K11': S(15,4)
- Roffset, Goffset, Boffset: S(14,4) 14 bits, 10 bit signed integer and 4-bit fractional bits. (Default: 0x000h)
- K13': S(15,4)
- K22', K23': S(11,2)
- K32': S(13,2)
- Rgain, Ggain, Bgain: U(10, 9) 10bits, 1 bit integer and 9-bit fractional bits. (Default: 0x0200h)

Operation	Description
K11' = K11*Y	U(12,10) * S(9,0) = S(21,10) truncating to S(15,4)
K13' = K13*V	U(11,10) * S(8,0) = S(19,10) truncating to S(13,4)
R'' = K11'+K13'	S(15,4) + S(13,4) = S(15,4)
R' = R'' + Roffset	S(15,4) + S(14,4) = S(15,4) truncating to S(13,2)
K22' = K22*U	U(10,10) * S(9,0) = S(19,10) truncating to S(13,4)
K23' = K23*V	U(10,10) * S(8,0) = S(18,10) truncating to S(13,4)
G'' = K11'-K22'-K23'	S(15,4)+ S(13,4)+ S(13,4) = S(15,4)
G' = G'' + Goffset	S(15,4) + S(14,4) = S(15,4) truncating to S(13,2)
K32' = K32*U	U(12,10) * S(8,0) = S(20,10) truncating to S(14,4)
B'' = K11'+K32'	S(15,4)+ S(14,4) = S(15,4)
B' = B'' + Boffset	S(15,4) + S(14,4) = S(15,4) truncating to S(13,2)
R=Rgain*R'	U(10,9)*S(13,2)=S(23,11) rounding to U(10,0) (clamp)
G=Ggain*G'	U(10,9)*S(13,2)=S(23,11) rounding to U(10,0) (clamp)
B=Bgain*B'	U(10,9)*S(13,2)=S(23,11) rounding to U(10,0) (clamp)



Paged Control Register

Address: 9F PAGE_SEL

Default: 00h

Bit	Mode	Function
7:5	R/W	Reserved to 0
4:0	R/W	Page Selector (CRA0~CRFF) <u>Page 0: Embedded ADC/ABL/LVR/Schmitt trigger/ Embedded LDO</u> <u>Page 1: PLL</u> <u>Page 2: HDMI</u> <u>Page 3: Reserved</u> <u>Page 4: Reserved</u> <u>Page 5: Reserved</u> <u>Page 6: IOSC</u> <u>Page 7: Vivid color/DCC/ICM/CABC</u> <u>Page 8: Reserved</u> <u>Page 9: Input Gamma</u> <u>Page A: Reserved</u> <u>Page B: GDI PHY</u> <u>Page C: GDI MAC</u> <u>Page D: MCU</u> <u>Page E: MCU</u> <u>Page F: MCU</u> <u>Page 10: Pin Share Control</u> Others: reserved



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Embedded ADC (Page 0)

Register::ADC_POWER_SOG_SOY_CONTROL[7:0]					0xBA
Name	Bit	R/W	Default	Description	Config
Reserved	7:1	R/W	0x10	Reserved	
ADC_VIDEO	0	R/W	0b0	Video8 input control (0: analog input, 1: video8 input) (pin 31~40) (useless, because there is no ADC2)	

Register:: ADC_2X_SAMPLE[7:0]					0xBB
Name	Bit	R/W	Default	Description	Config
ADC_2X_SAMPLE[7]	7	R/W	0b0	ADC 2x over sample (0:1x 1:2x)	
ADC_2X_SAMPLE[6]	6	R/W	0b1	2x Clock Polarity (0: Negative 1: Positive)	
ADC_2X_SAMPLE[5]	5	R/W	0b1	1x Clock Polarity (0: Negative 1: Positive)	
ADC_2X_SAMPLE[4:3]	4:3	R/W	0b000	Reserved	
ADC_2X_SAMPLE [2]	2	R/W	0b0	clock input select (0:from CKOAD_V33, 1:from CKOAD_V12)	
Reserved	1	R/W	0b0	Reserved	
Reserved	0	R/W	0b0	Reserved	

Register:: ADC_CLOCK[7:0]					0xBC
Name	Bit	R/W	Default	Description	Config
ADC_CLOCK[7]	7	R/W	0b0	Input Clock Polarity (0:Negative 1:Positive)	
ADC_CLOCK[6]	6	R/W	0b0	Output Divider Clock Polarity (0:Normal 1:Inverted)	
ADC_CLOCK[5:4]	5:4	R/W	0b0	ADC_OUT_PIXEL Delay (00:1.05n 01:1.39n 10:1.69n 11:1.97n)	
ADC_CLOCK[3]	3	R/W	0b0	1X or 2X from APLL (0:1X 1:2X)	
ADC_CLOCK[2]	2	R/W	0b0	Single Ended or Diff. Clock from APLL	



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				(0:Diff. 1:Single Ended)	
ADC_CLOCK[1:0]	1:0	R/W	0b1	Duty Staiblizer(00: 48% 01:50% 10: 51% 11:52%)	

Register:: ADC_TEST[7:0]					0xBD
Name	Bit	R/W	Default	Description	Config
ADC_TEST[7]	7	R/W	0b0	Reserved, original function mapping to ADC_SOG_CMP[4](CRD2)	
ADC_TEST[6:4]	6:4	R/W	0b000	Test Ouput Selection (PAD: SOGIN0,) SOGIN0 (000:X 001:gnd 010:vrefn 011:vcm 100:vrefp 101:vdd 110:vdd 111:vdd)	
Reserved	3:2	R/W	0b0	Reserved	
ADC_TEST[1:0]	1:0	R/W	0b00	Clock Output Divider (00: 1/1 01: 1/2 10: 1/3 11: 1/4)	

Register::RGB gain_LSB					0xBE
Name	Bit	R/W	Default	Description	Config
Reserved	7:6	R/W	0b0	Reserved	
Reserved	5:4	R/W	0x0	Reserved to Red Channel Gain Adjust LSB	
Reserved	3:2	R/W	0x0	Reserved to Green Channel Gain Adjust LSB	
Reserved	1:0	R/W	0x0	Reserved to Blue Channel Gain Adjust LSB	

Register::RGB offset_LSB					0XBF
Name	Bit	R/W	Default	Description	Config
Reserved	7:6	R/W	0b0	Reserved	
Reserved	5:4	R/W	0x0	Reserved to Red Channel Offset Adjust LSB	
Reserved	3:2	R/W	0x0	Reserved to Green Channel Offset Adjust LSB	



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Reserved	1:0	R/W	0x0	Reserved to Blue Channel Offset Adjust LSB	
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Register::red_gain_MSB 0xC0					
Name	Bit	R/W	Default	Description	Config
ADC_GAI_RED[7:0]	7:0	R/W	0x80	Red Channel Gain Adjust[7:0]	

Register::green_gain_MSB 0xC1					
Name	Bit	R/W	Default	Description	Config
ADC_GAI_GRN[7:0]	7:0	R/W	0x80	Green Channel Gain Adjust[7:0]	

Register::blue_gain_MSB 0xC2					
Name	Bit	R/W	Default	Description	Config
ADC_GAI_BLU[7:0]	7:0	R/W	0x80	Blue Channel Gain Adjust[7:0]	

Register::RED_OFFSET_MSB 0xC3					
Name	Bit	R/W	Default	Description	Config
ADC_OFF_RED[7:0]	7:0	R/W	0x80	Red Channel Offset Adjust[7:0]	

Register::GREEN_OFFSET_MSB 0xC4					
Name	Bit	R/W	Default	Description	Config
ADC_OFF_GRN[7:0]	7:0	R/W	0x80	Green Channel Offset Adjust[7:0]	

Register::BLUE_OFFSET_MSB 0xC5					
Name	Bit	R/W	Default	Description	Config
ADC_OFF_BLU[7:0]	7:0	R/W	0x80	Blue Channel Offset Adjust[7:0]	

Register:: ADC_POWER[7:0] 0xC6					
Name	Bit	R/W	Default	Description	Config
ADC_POWER[7]	7	R/W	0	ADC VCM Power On (0: Power Down, 1: Power On)	
ADC_POWER[6]	6	R/W	0	ADC clock Power On (0: Power Down 1: Power On)	
ADC_POWER[5]	5	R/W	0b0	SOG_ADC0 Power On (0: Power Down 1: Power On)	
ADC_POWER[4]	4	R/W	0b0	ADC Regulator Power On	



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				(0: Power Down 1: Power On)	
ADC_POWER[3]	3	R/W	0b0	Bandgap/IBIAS[4:0] Power On (0: Power Down 1: Power On)	
ADC_POWER[2]	2	R/W	0b0	Red Channel ADC Power On (0: Power Down 1: Power On) not controller by CR01[2:1] global power down/saving	
ADC_POWER[1]	1	R/W	0b0	Green Channel ADC Power On (0: Power Down 1: Power On) not controller by CR01[2:1] global power down/saving	
ADC_POWER[0]	0	R/W	0b0	Blue Channel ADC Power On (0: Power Down 1: Power On) not controller by CR01[2:1] global power down/saving	

Register:: ADC_IBIAS0[7:0]					0xC7
Name	Bit	R/W	Default	Description	Config
ADC_IBIAS0[7:6]	7:6	R/W	0b01	[7:6]: PGA Input GM Current, High 2 bits Low 2 bits=ADC_IBIAS1<7:6> (0000: 0u, 0001: 50u, 0010: 100u, 0011: 150u 0100: 200u, 0101: 250u, 0110: 300u, 0111: 350u 1000: 400u, 1001: 450u, 1010: 500u, 1011: 550u 1100: 600u, 1101: 650u, 1110: 700u, 1111: 750u)	
ADC_IBIAS0[5:4]	5:4	R/W	0b01	Reserved	
ADC_IBIAS0[3:2]	3:2	R/W	0b01	Reserved	
ADC_IBIAS0[1:0]	1:0	R/W	0b01	Reserved	

Register:: ADC_IBIAS1[7:0]	0xC8
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RTD2261W/2271W/2281W Series-GR

Name	Bit	R/W	Default	Description	Config
ADC_IBIAS1[7:6]	7:6	R/W	0b01	Reserved	
ADC_IBIAS1[5:4]	5:4	R/W	0b01	Reserved	
ADC_IBIAS1[3:2]	3:2	R/W	0b01	Reserved	
ADC_IBIAS1[1:0]	1:0	R/W	0b01	Reserved	

Register:: ADC_IBIAS2[7:0]					0xC9
Name	Bit	R/W	Default	Description	Config
ADC_IBIAS2[7:6]	7:6	R/W	0b00	Reserved	
ADC_IBIAS2[5]	5	R/W	0b0	Reserved	
ADC_IBIAS2[4:2]	4:2	R/W	0b001	Reserved	
ADC_IBIAS2[1:0]	1:0	R/W	0b01	Reserved	

Register:: ADC_IBIAS3[7:0]					0xCA
Name	Bit	R/W	Default	Description	Config
ADC_IBIAS3[7:6]	7:6	R/W	0b01	Reserved	
ADC_IBIAS3[5:3]	5:3	R/W	0b011	Reserved	
ADC_IBIAS3[2:0]	2:0	R/W	0b001	Bias Current of SH,MDAC (000:12u 001:18u 010:24u 011:27u) (100:30u 101:33u 110:50u 111:39u) Bias Current of SUBADC (000:10u 001:10u 010:10u 011:10u) (100:20u 101:20u 110:20u 111:20u)	

Register:: ADC_IBIAS4[7:0]					0xCB
Name	Bit	R/W	Default	Description	Config
ADC_IBIAS4[7:6]	7:6	R/W	0b01	Reserved	
ADC_IBIAS4[5:4]	5:4	R/W	0b01	Reserved	
ADC_IBIAS4[3:2]	3:2	R/W	0b01	Reserved	
ADC_IBIAS4[1:0]	1:0	R/W	0b01	Reserved	

Register:: ADC_VBIAS0[7:0]					0XCC
Name	Bit	R/W	Default	Description	Config
ADC_VBIAS0[7:6]	7:6	R/W	0b00	Reserved	
ADC_VBIAS0[5:4]	5:4	R/W	0b01		



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				Select output voltage of ADC Regulator (00:1.2 01:1.3 10:1.4 11:1.5)	
ADC_VBIAS0[3:2]	3:2	R/W	0b00	Reserved	
ADC_VBIAS0[1:0]	1:0	R/W	0b01	Bandgap Voltage (00:1.15 01:1.25 10:1.34 11:1.42)	

Register:: ADC_VBIAS1[7:0] 0xCD					
Name	Bit	R/W	Default	Description	Config
ADC_VBIAS1[7]	7	R/W	0b0	Reserved	
ADC_VBIAS1[6]	6	R/W	0b0	R Channel Clamp to -300mV (0: 0mV 1:-300mV)	
ADC_VBIAS1[5]	5	R/W	0b0	G Channel Clamp to -300mV (0: 0mV 1:-300mV)	
ADC_VBIAS1[4]	4	R/W	0b0	B Channel Clamp to -300mV (0: 0mV 1:-300mV)	
ADC_VBIAS1[3]	3	R/W	0b1	SH boot enable (0:no boost, 1: boost)	
ADC_VBIAS1[2]	2	R/W	0b0	SH boot adjust (0:0.8, 1:0.85)	
ADC_VBIAS1[1]	1	R/W	0b0	Reserved	
ADC_VBIAS1[0]	0	R/W	0b1	PGA Input GM Power On (0: Power Down, 1: Power On)	

Register:: ADC_CTL_RGB[7:0] 0xCE					
Name	Bit	R/W	Default	Description	Config
ADC_CTL_RGB[7:4]	7:4	R/W	0b1000	SH gain(0000:0.95, 0001:1, 0010:1.05, 0011:1.1, 0100:1.15, 0101:1.2, 0110:1.25, 0111:1.3, 1000:1.35, 1001:1.4, 1010:1.45)	
ADC_CTL_RGB[3]	3	R/W	0b0	Dual (0: Input0 1: force to ground)	
ADC_CTL_RGB[2]	2	R/W	0b1	Single Ended or Diff. Input (0: Single Ended 1: Diff)	
ADC_CTL_RGB[1:0]	1:0	R/W	0b10	Bandwidth (00: 75M 01: 150M 10: 300M 11: 500M)	



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Register:: ADC_CTL_RED[7:0]

0xCF

Name	Bit	R/W	Default	Description	Config
ADC_CTL_RED[7]	7	R/W	0b0	RGB/YPrPb Clamp (0: RGB 1:YPrPB) //ADC_VBIAS1[6]==0	
ADC_CTL_RED[6:4]	6:4	R/W	0b100	Clamp Voltage (0V~700mV, Step=100mV)	
ADC_CTL_RED[3]	3	R/W	0b0	Offset Depends on Gain (0: RGB Yes, YPrPb No 1:RGB No, YPrPb No)	
ADC_CTL_RED[2:0]	2:0	R/W	0b000	Red Channel ADC Fine Tune Delay, Step=90ps	

Register:: ADC_CTL_GRN[7:0]

0XD0

Name	Bit	R/W	Default	Description	Config
ADC_CTL_GRN[7]	7	R/W	0b0	RGB/YPrPb Clamp (0: RGB 1:YPrPB) //ADC_VBIAS1[6]==0	
ADC_CTL_GRN[6:4]	6:4	R/W	0b100	Clamp Voltage (0V~700mV, Step=100mV)	
ADC_CTL_GRN[3]	3	R/W	0b0	Offset Depends on Gain (0: RGB Yes, YPrPb No 1:RGB No, YPrPb No)	
ADC_CTL_GRN[2:0]	2:0	R/W	0b0	Green Channel ADC Fine Tune Delay, Step=90ps	

Register:: ADC_CTL_BLU[7:0]

0xD1

Name	Bit	R/W	Default	Description	Config
ADC_CTL_BLU[7]	7	R/W	0b0	RGB/YPrPb Clamp (0: RGB 1:YPrPB) //ADC_VBIAS1[6]==0	
ADC_CTL_BLU[6:4]	6:4	R/W	0b100	Clamp Voltage (0V~700mV, Step=100mV)	
ADC_CTL_BLU[3]	3	R/W	0b0	Offset Depends on Gain (0: RGB Yes, YPrPb No 1:RGB No, YPrPb No)	
ADC_CTL_BLU[2:0]	2:0	R/W	0b0	Blue Channel ADC Fine Tune Delay, Step=90ps	



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Register:: ADC_SOG_CMP[7:0] 0xD2

Name	Bit	R/W	Default	Description	Config
ADC_SOG_CMP[7]	7	R/W	0b0	ADC Gain Calibration, OFF PAD to Circuit Path (0: Normal 1: Calibration)	
ADC_SOG_CMP[6]	6	R/W	0b0	Select Absolute VDD (0: from 3.3V, 1: from 1.2V)	
ADC_SOG_CMP[5]	5	R/W	0b0	ADC Gain Calibration, Always Enable Clamp Signal (0: ADC_CLAMP[7:0]= from sync processor 1: ADC_CLAMP[7:0]=H)	
ADC_SOG_CMP[4]	4	R/W	0b0	ADC Gain Calibration Voltage Source (0: from RGB+Bandgap, 1: from Gain_Cal_DAC3B) Refer to ADC_SOG_CMP[2:0]	
ADC_SOG_CMP[3]	3	R/W	0b0	ADC Gain Calibration Voltage Source of Gain_Cal_DAC3B (0: from Absolute VDD, 1:from Bandgap)	
ADC_SOG_CMP[2:0]	2:0	R/W	0b000	ADC Gain Calibration Gain_Cal_DAC3B Voltage, (Measure method is the same as VMID, VOFFSET) Positive side : (000:0.40V 001:0.50V 010:0.60V 011:0.70V) (100:0.80V 101:0.90V 110:1.00V 111:1.10V) Negative side: 0.7V	

Register:: ADC_DCR_CTRL[7:0] 0xD3

Name	Bit	R/W	Default	Description	Config
ADC_DCR_CTRL[7]	7	R/W	0	Reserved	
ADC_DCR_CTRL[6]	6	R/W	0	Reserved	
ADC_DCR_CTRL[5]	5	R/W	0	Reserved	



ADC_DCR_CTRL[4]	4	R/W	0	SOG0 DC Restore Enable(0:Disable 1:Enable)	
ADC_DCR_CTRL[3]	3	R/W	0	Reserved	
ADC_DCR_CTRL[2]	2	R/W	0	Reserved	
ADC_DCR_CTRL[1]	1	R/W	0	Reserved	
ADC_DCR_CTRL[0]	0	R/W	0	Reserved	

Register:: ADC_CLAMP_CTRL0[7:0] 0xD4					
Name	Bit	R/W	Default	Description	Config
ADC_CLAMP_CTRL0[7]	7	R/W	0	Reserved	
ADC_CLAMP_CTRL0[6]	6	R/W	0	Reserved	
ADC_CLAMP_CTRL0[5]	5	R/W	0	Reserved	
ADC_CLAMP_CTRL0[4]	4	R/W	0	SOG0 Clamp Enable(0:Disable 1:Enable)	
ADC_CLAMP_CTRL0[3]	3	R/W	0	Reserved	
ADC_CLAMP_CTRL0[2]	2	R/W	0	Reserved	
ADC_CLAMP_CTRL0[1]	1	R/W	0	Reserved	
ADC_CLAMP_CTRL0[0]	0	R/W	0	Reserved	

Register:: ADC_CLAMP_CTRL1[7:0] 0xD5					
Name	Bit	R/W	Default	Description	Config
ADC_CLAMP_CTRL1[7]	7	R/W	0	Reserved	
ADC_CLAMP_CTRL1[6]	6	R/W	0	Reserved	
ADC_CLAMP_CTRL1[5]	5	R/W	0	Reserved	
ADC_CLAMP_CTRL1[4]	4	R/W	0	ADC 1.2V Generated by Resistor, PS/PD mode (0: Disable, 1: Enable)	
ADC_CLAMP_CTRL1[3]	3	R/W		ADC Regulator Output Voltage Switch (0: 1.3V not short to ground 1: 1.3V short to ground) If use internal ADC Regulator, PS/PD mode set ADC_CLAMP_CTRL1[3]=1	
ADC_CLAMP_CTRL1[2]	2	R/W	0	SOG0 Bias Current Source (0: from	



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				POR, 1: from ADC)	
ADC_CLAMP_CTRL1[1]	1	R/W	0	SOG0 clamp -300mV (0: noraml clamp 1:clamp -300m) //IR	
ADC_CLAMP_CTRL1[0]	0	R/W	0	Bias Current of SOG (0: Normal Mode, 1: Low Standby Mode)	

Register:: ADC_CLAMP_CTRL2[7:0]					0XD6
Name	Bit	R/W	Default	Description	Config
ADC_CLAMP_CTRL2[7:6]	7:6	R/W	0b01	SOG0 DC restore resister (00:open 01:500k 10:1M 11:5M) (500k/1M are Poly R)	
ADC_CLAMP_CTRL2[5:4]	5:4	R/W	0b01	Reserved	
ADC_CLAMP_CTRL2[3]	3	R/W	1	RGB Input Range Adjust 0: 0.5V-1.0V, 1: 0.25-1.25V,	
ADC_CLAMP_CTRL2[2]	2	R/W	0	Red channel clamp to top (0: noraml 1: top)	
ADC_CLAMP_CTRL2[1]	1	R/W	0	Green channel clamp to top (0: noraml 1: top)	
ADC_CLAMP_CTRL2[0]	0	R/W	0	Blue channel clamp to top (0: noraml 1: top)	

Register::ADC_SOG_DAC_SOY_CONTROL[7:0]					0xD7
Name	Bit	R/W	Default	Description	Config
Reserved	7:6	---	0b00	Reserved	
ADC_SOG0_DAC[5:0]	5:0	R/W	0b100000	SOG0 DAC input	

Address:D8 PTNPOS_H Default: 00h		
Bit	Mode	Function
7:4	R/W	Test Pattern V Position Register [11:8] Assign the test pattern digitized position in line after V_Start.
3:0	R/W	Test Pattern H Position Register [11:8] Assign the test pattern digitized position in pixel after H_Start.

Address: D9 PTNPOS_V_L		
Bit	Mode	Function
7:0	R/W	Test Pattern V Position Register [7:0] Assign the test pattern digitized position in line after V_Start..

Address:DA PTNPOS_H_L		
Bit	Mode	Function
7:0	R/W	Test Pattern H Position Register [7:0] Assign the test pattern digitized position in line after H_Start..

Use PTNPOS to assign the pixel position after HSYNC leading edge that input signal digitized. Each time the



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PTNPOS is written, the digitized results will be loaded into PTNRD, PTNGD and PTNBD. For test issue, make the input signal a fixed pattern before PTNPOS is written. Then the same digitized output will be got.

Address: DB PTNRD

Bit	Mode	Function
7:0	R	Test Pattern Red-Channel Digitized Result.

Address: DC PTNGD

Bit	Mode	Function
7:0	R	Test Pattern Green-Channel Digitized Result.

Address: DD PTNBD

Bit	Mode	Function
7:0	R	Test Pattern Blue-Channel Digitized Result.

Address: DE TEST_PATTERN_CTRL

Default: 00h

Bit	Mode	Function
7	R/W	Enable Test 0: Finish (and result sequence is R-G-B) (Default) 1: Start
6:0	--	Reserved to 0

Embedded LDO(Page 0)

Register:: EBD_REGULATOR_A_CTRL					0XDF
Name	Bit	R/W	Default	Description	Config
POWLDO_L_A	7	R/W	1	Analog Regulator Enable 0: disable regulator 1: enable regulator	
CONNECT_AV12DV12_L_A	6	R/W	00	Analog and Digital VCC connection 0: disconnect 1: connect, maximum 10 mA to digital. (digital regulator will disable)	
TUNE_LDOCUR_LA	5:3	R/W	0	Select Opamp current control: 000 : normal(default) ; 001 : 1/2 ; 010 : 1/4 ; 011 : 1/6 ; 100 : 1/8 101 : 1/10 110 : 1/12 111 : 1/14	
TUNE_VREF_LA	2:0	R/W	010	Select output voltage of regulator 000 : 1.008 ; 001 : 1.044 ; 010 : 1.092 ; (default)	



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				011 : 1.140 ; 100 : 1.2 101 : 1.248 110 : 1.296 111 : 1.344	
--	--	--	--	---	--

External capacitor must be 10uF.

Register:: EBD_REGULATOR_DB_CTRL					0XE0
Name	Bit	R/W	Default	Description	Config
POWLDO_L_D	7	R/W	1	Digital Regulator Enable 0: disable regulator 1: enable regulator	
EBD_REG_5_D	6	R/W	00	Reserved to 0	
TUNE_LDOCUR_L_D	5:3	R/W	0	Select Opamp current control: 000 : normal(default) ; 001 : 1/2 ; 010 : 1/4 ; 011 : 1/6 ; 100 : 1/8 101 : 1/10 110 : 1/12 111 : 1/14	
ENHANCE_LDO_L_D	2	R/W	0	LDO_D driving ability control : 0 : can drive 60mA current 1: can drive 250mA current	
EBD_REG_1_D	1	R/W	--	Reserved to 0	
ENHANCE_LDO_L_A	0	R/W	0	LDO_A driving ability control : 0 : can drive 30mA current 1: can drive 170mA current	

External capacitor must be 10uF.

Analog 1.2V and Digital 1.2V on PCB must be opened.



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ABL(Page 0)

Address: E2 AUTO_BLACK_LEVEL_CTRL1

Default: 00h

Bit	Mode	Function
7	R/W	ABL Mode 0: RBG (Default) 1: YPbPr
6	R/W	On-line/Off-line ABL Mode 0: Off-line (Default) 1: On-line
5:4	R/W	Width of ABL region in each line 00: 16 pixels (Default) 01: 32 pixels 10: 64 pixels 11: 4 pixels
3	R	R/Pr Channel ABL Result (write clear) 0: not equal 1: equal (Black Level = Target Value) On-line mode: Black Level - Target Value <=LOCK_MGN Off-line mode: Black Level - Target Value <= EQ_MGN
2	R	G/Y Channel ABL Result (write clear) 0: not equal 1: equal (Black Level = Target Value) On-line mode: Black Level - Target Value <= LOCK_MGN Off-line mode: Black Level - Target Value <= EQ_MGN
1	R	B/Pb Channel ABL Result (write clear) 0: not equal 1: equal (Black Level = Target Value) On-line mode: Black Level - Target Value <= LOCK_MGN Off-line mode: Black Level - Target Value <= EQ_MGN
0	R/W	Auto Black Level Enable (write 0 force stop) 0: Finished/Disable (Default) 1: Enable to start ABL, auto cleared after finished Cleared to 0 when off-line mode completes.

- Parameters can only be changed when EN_ABL is 0
- The on-line mode never stops unless EN_ABL is 0.
- Off-line mode completes when MAX_FRAME is measured or the result is equal.
- ABL must be disabled before switching On-line/Off-line mode and then enable again.



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Address: E3 AUTO_BLACK_LEVEL_CTRL2

Default: 84h

Bit	Mode	Function
7:6	R/W	Line averaged for each ABL adjustment 00: 8 01: 16 10: 32 (Default) 11: 64
5	--	Reserved
4:0	R/W	Start Vertical Position of ABL in each line Determine the start line of auto-black-level after the leading edge of Vsync

Address: E4 AUTO_BLACK_LEVEL_CTRL3

Default: 10h

Bit	Mode	Function
7:4	R/W	Y/R/G/B Target value 0000: 1 0001: 2 (Default) 0010: 3 0011: 4 1111:16 (Pb/Pr Target level is fixed 128)
3:2	R/W	Lock Margin 00: 1 (Default) 01: 2 10: 4 11: 6
1:0	R/W	End Vertical Position of ABL measurement region [9:8] Determine the last line of auto-black-level measurement for every frame/field countd by double line

- Off-line mode rule:
Measures once for each field / frame, and the offset is the delta.
- On-line mode rule:
If (delta <= EQ_MGN) offset = 0
Else if (delta < L_MGN) offset = +/-1
Else offset = +/-L_MGN
- ADC offset is updated immediately.



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Address: E5 AUTO_BLACK_LEVEL_CTRL4**Default: 82h**

Bit	Mode	Function
7:0	R/W	End Vertical Position of ABL measurement region [7:0] Determine the last line of auto-black-level measurement for every frame/field counted by double line.

- Note: ABL will fail if End Vertical Position < Start Vertical Position + Average Line(CRC1[7:6])

Address: E6 AUTO_BLACK_LEVEL_CTRL5**Default: 04h**

Bit	Mode	Function
7:0	R/W	Start Position of ABL in Each Line Determine the start position of auto-black-level after the trailing edge of reference signal. (When ABL mode in YPbPr, the reference signal is input Hsync. In RGB mode, the reference signal is clamp signal.)

- In each region, hardware compare the average value in the target region (fixed 16 input pixels after start position of ABL) with target value and add +1/-1 or +L_MGN / - L_MGN to ADC offset. (+ for greater than target value, - for smaller than target value).

Address: E7 AUTO_BLACK_LEVEL_CTRL6**Default: C0h**

Bit	Mode	Function
7:6	R/W	Large Error Margin (L_MGN) (For on-line Mode) 00: 2 01: 4 10: 6 11: 8 (Default)
5:4	R/W	Max. Frame/Field Count (For off-line mode) 00: 4 (Default) 01: 5 10: 6 11: 7
3	--	Reserved
2:0	R/W	Lines delayed between each measurement region (For on-line Mode) 000: 16 (Default) 001: 32 010: 64 011: 128 100: 192 101: 256



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		110: 384 111: 640
--	--	----------------------

Address: E8 AUTO_BLACK_LEVEL_CTRL7

Default: 60h

Bit	Mode	Function
7	--	Reserved
6	R/W	Equal Condition (Off-line mode) 0: To trigger status until measurement achieve Max Frame/Field Count. 1: To trigger status once if Black Level - Target Value <= EQ_MGN. (Default) (If set 0, the ABL Result will not go low even noise comes for the next frames.)
5	R/W	Measure Pixels Method 1: Minimum value (Default) 0: Average value
4	R/W	Measure Error Flag Reset 0: Normal 1: Reset
3	R	Measure Error Flag 0: Normal 1: Error (This flag is occurred when Hsync trailing edge is met during measurement.)
2	R/W	Hsync Start Reference Select 0: HS leading edge (Default) 1: HS trailing edge
1:0	R/W	Equal margin (EQ_MGN) 00: 0 (Default) 01: 1 10: 2 11: 3

Address: E9 AUTO_BLACK_LEVEL_RED_VALUE

Bit	Mode	Function
7:0	R	Minimum/Average Value of Red Channel in Test Mode (only show MSB 8bit.)

Address: EA AUTO_BLACK_LEVEL_GREEN_VALUE

Bit	Mode	Function
7:0	R	Minimum/Average Value of Green Channel in Test Mode (only show MSB 8bit.)

Address: EB AUTO_BLACK_LEVEL_BLUE_VALUE



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Bit	Mode	Function
7:0	R	Minimum/Average Value of Blue Channel in Test Mode (only show MSB 8bit.)

Address: EC AUTO_BLACK_LEVEL_NOISE_VALUE_OF_RED_CHANNEL

Bit	Mode	Function
7:0	R	Noise Value of Red Channel in Test Mode after Equal status is triggered. (only show MSB 8bit.)

Address: ED AUTO_BLACK_LEVEL_NOISE_VALUE_OF_GREEN_CHANNEL

Bit	Mode	Function
7:0	R	Noise Value of Green Channel in Test Mode after Equal status is triggered. (only show MSB 8bit.)

Address: EE AUTO_BLACK_LEVEL_NOISE_VALUE_OF_BLUE_CHANNEL

Bit	Mode	Function
7:0	R	Noise Value of Blue Channel in Test Mode after Equal status is triggered. (only show MSB 8bit.)

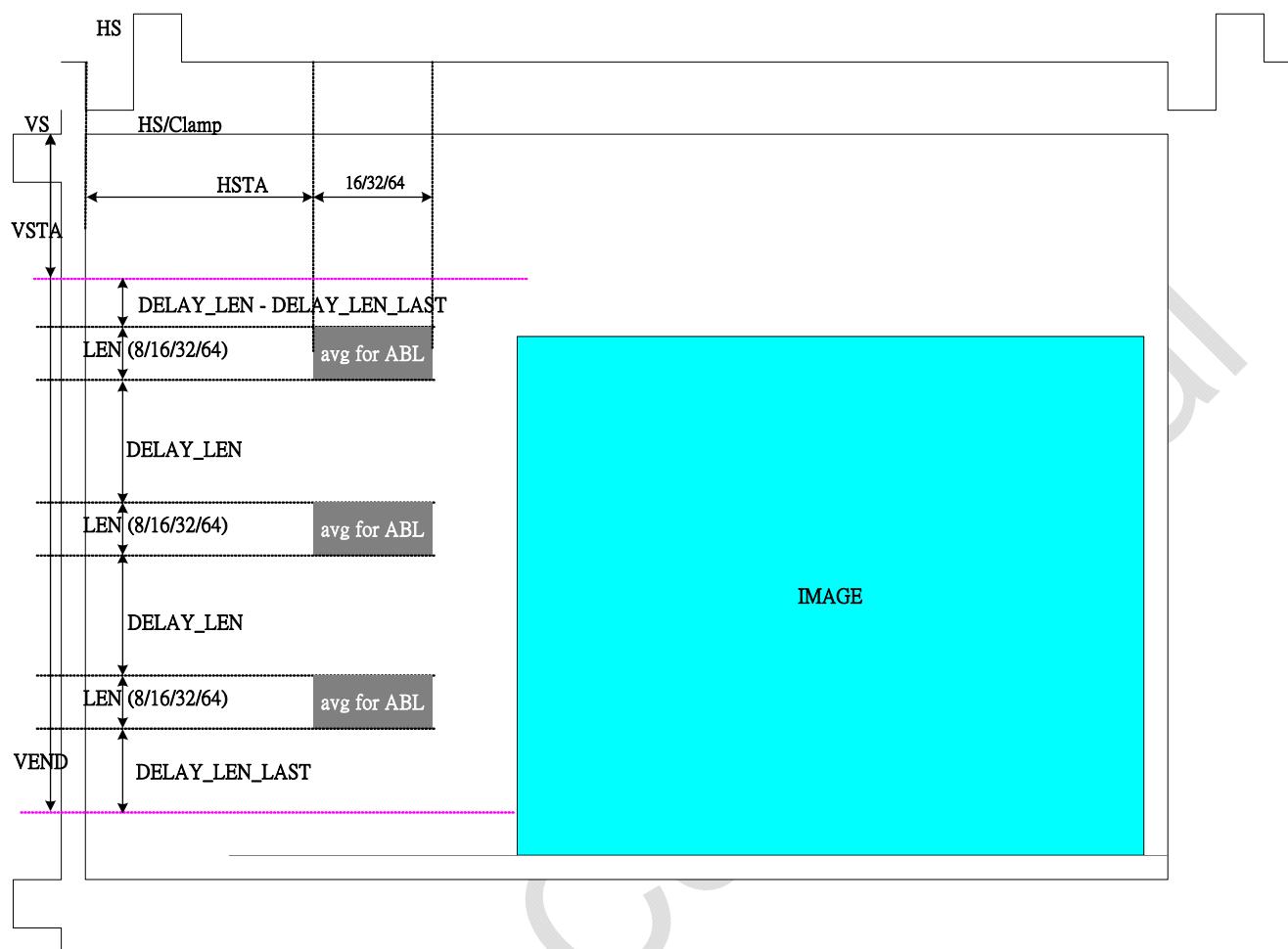


Figure-1: Auto Black Level active region – case 1

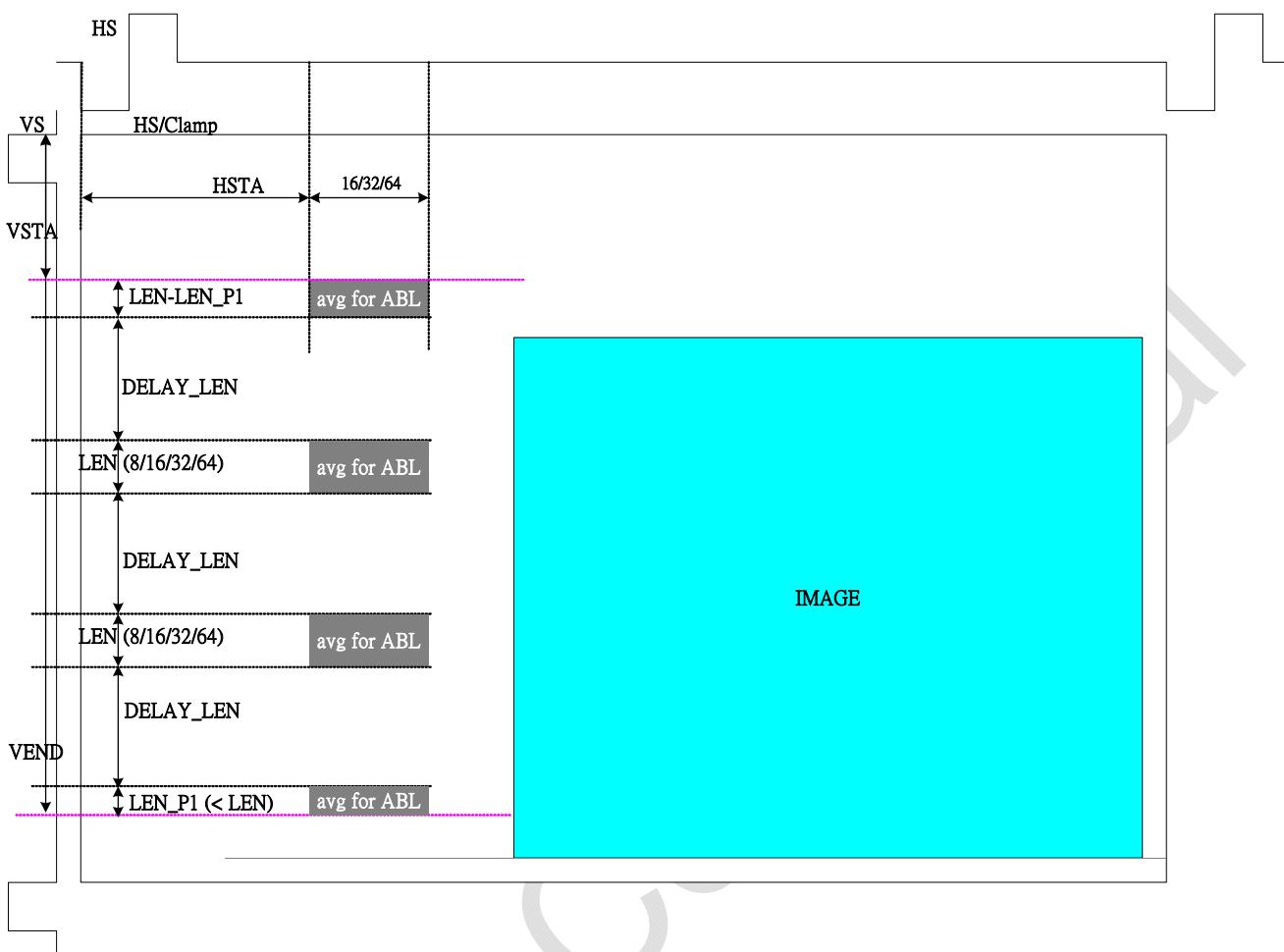


Figure-2: Auto Black Level active region – case 2

LVR(Page 0)**Address: F3 POWER_ON_RESET****Default: C4h**

Bit	Mode	Function
7:6	R/W	Negative Threshold Value For Power on Reset (POR reset time=160ms) (VTP=2.8V) 00:2.4V 01: 2.6V 10: 2.5V 11:2.7V(Default) When in scan mode,[7:6] is tied to 2'b00
5:4	R/W	PORMCUVSET (LVR Threshold Voltage) (VTN=0.66, VTP=0.88) (Core LVR voltage: tied to 2'b00 by hardware)
3	R/W	DET_VCCKOFF_12V, DET_VCCKOFF_33V output select: 0: Manual mode : from REG_PWR_ISO_ON (bit2) (default) 1: Auto mode : from the comparator in the POR circuit



2	R/W	REG_PWR_ISO_ON: power isolation on/off control register 0: normal mode, (V12_VDD_DET is on) (default) 1: power isolation mode (V12_VDD_DET is off)
1:0	R/W	XI/XO Pad Driving 00: Strong (default) 01: Medium 10: Medium 11: Weak

Schmitt trigger (Page 0)

Address:F 4 HS_SCHMITT_TRIGGER_CTRL

Default: 41h

Bit	Mode	Function
7	R/W	HSYNC Schmitt Power Down (Only for Schmitt trigger new mode) 0: Power down (Default) 1: Normal
6	R/W	Polarity Select 0: Negative HSYNC (high level) 1: Positive HSYNC (low level) (Default)
5	R/W	Schmitt Trigger Mode 0: Old mode 1: New mode(Default)
4	R/W	Threshold Voltage Fine Tune (only for Schmitt trigger new mode) 0: 0V (Default) 1: -0.1V
3:2	R/W	Positive Threshold Voltage
1:0	R/W	Negative Threshold Voltage

- There is a mode of the HSYNC Schmitt trigger.

- New mode: Fully programmable Schmitt trigger.

The following table will determine the Schmitt Trigger positive and negative voltage:

bit[6]=1 (Positive HSYNC)			bit[6] = 0 (Negative HSYNC)		
bit[3:2]	V _t ⁺	bit[1:0]	V _t ⁻	bit[3:2]	V _t ⁺
00	1.4V	00	V _t ⁺ - 1.2V	00	1.8V
01	1.6V	01	V _t ⁺ - 1.0V	01	2.0V
10	1.8V	10	V _t ⁺ - 0.8V	10	2.2V
11	2.0V	11	V _t ⁺ - 0.6V	11	2.4V
					V _t ⁻ - 1.2V
					V _t ⁻ - 1.0V
					V _t ⁻ - 0.8V
					V _t ⁻ - 0.6V

- After we get the threshold voltage by the table, we still can fine tune it:

$$\text{Final Positive Threshold Voltage} = V_t^+ - 0.1 * \text{bit}[4]$$

$$\text{Final Negative Threshold Voltage} = V_t^- - 0.1 * \text{bit}[4]$$



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ADC PLL (Page 1)

Address: A0 PLL DIV CTRL

Default: 08h

Bit	Mode	Function
7	R/W	DDS Tracking Edge 0: HS positive edge (Default) 1: HS negative edge
6	R/W	Tracking direction inversion 0: if HS leads HSFBD => phase lead => m, k ↑ (Default) 1: if HS lags HSFBD => phase lag => m, k ↓
5:4	R/W	Waiting HS lines to start counting divider for Fast Lock function 00: 4 (default) 01: 3 10: 2 11: 1
3:2	R/W	Delay Compensation Mode 00: Mode 0 No delay from PLL phase0 to DDS pfd input 01: Mode 1 Delay the path from PLL phase0 to DDS pfd input to be around 4.2 ns 10: Mode 2 (default) Delay the path from PLL phase0 to DDS pfd input to be around 4.6 ns 11: Mode 3 Delay the path from PLL phase0 to DDS pfd input to be around 5 ns
1	R/W	Reserved to 0
0	R/W	Reserved to 0

Address: A1 I_CODE_M

Default: 01h

Bit	Mode	Function
7	R/W	Reserved to 0
6:0	R/W	I_CODE[14:8]

Address: A2 I_CODE_L

Default: 04h

Bit	Mode	Function
7:0	R/W	I_CODE[7:0]

Address: A3 P_CODE

Default: 20h

Bit	Mode	Function
7:0	R/W	P_CODE[7:0]

Address: A4 PFD_CALIBRATED_RESULTS

Default: 8'b0xxxxxxxx

Bit	Mode	Function
7	R/W	PFD Calibration Enable (auto clear when finished) Overwrite 0 to 1 return a new PFD calibrated value.
6:4	R/W	Reserved to 0
3:0	R	PFD Calibrated Results [11:8]



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Address: A5 PFD_CALIBRATED_RESULTS**Default: 8'bxxxxxxxxx**

Bit	Mode	Function
7:0	R	PFD Calibrated Results [7:0]

Address: A6 PE_MEASURE**Default: 8'b0xxxxxxxx**

Bit	Mode	Function
7	R/W	PE Measure Enable (auto clear when finished) 0: Disable (Default) 1: Start PE Measurement, clear after finish.
6:4	R/W	Reserved to 0
3:0	R	PE Value Result [11:8]

Address: A7 PE_MEASURE**Default: 8'bxxxxxxxxx**

Bit	Mode	Function
7:0	R	PE Value Result [7:0]

Address: A8 PE_MAX_MEASURE**Default: 8'b0xxxxxxxx**

Bit	Mode	Function
7	R/W	PE Max. Measure Enable 0: Disable (Default) 1: Start PE Max. Measurement
6:4	R/W	Reserved to 0
3:0	R	PE Max Value [11:8]

Address: A9 PE_MAX_MEASURE**Default: 8'bxxxxxxxxx**

Bit	Mode	Function
7:0	R	PE Max Value [7:0]

Address: AA FAST_PLL_CTRL**Default: 00h**

Bit	Mode	Function
7	R/W	PE Max. Measure Clear 0: clear (Default) 1: write '1' to clear PE Max. Value
6	R/W	Enable APLL Setting 0: Disable (Default) 1: Enable (Auto clear when finished) When CRAA[5] enabled, enable this bit will write P_CODE, I_CODE, PLL M/N, PLL K, PLLDIV



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		and DDS SUM_I at the end of input vertical data enable
5	R/W	Enable Fast PLL Mechanism 0: Disable (Default) 1: Enable (Auto clear when finished)
4	R/W	Force APPLL Setting Enable Force to write PLL M/N, K, PLLDIV and SUM_I while got no V_ACTIVE signal 0: Disable (Default) 1: Enable (Auto clear when finished)
3	R/W	DDS SUM_I Setting Updated Enable 0: Disable (Default) 1: Enable (Auto clear when finished)
2	R/W	Measure SUM_I 0: Disable 1: Enable (Auto clear after finish)
1	R/W	Enable Port AB 0: Disable Port AB Access 1: Enable Port AB Access When this bit is 0, port address will be reset to 00, and will auto increase when read or write
0	R/W	Select SUM_I for Read 1: Select SUM_I_NOW [26:0] for read 0: Select SUM_I_PRE [26:0] for read

Address: AB FAST_PLL_SUM_I

Bit	Mode	Function
7:0	R/W	SUM_I_PRE (Auto Increase) 1 st [00000, SUM_I [26:24]] 2 nd SUM_I [23:16] 3 rd SUM_I [15:8] 4 th SUM_I [7:0]

SUM_I [26] is the signed bit

The operation steps are as following:

SUM_I Access Port Indexing=0,

SUM_I Access Port Indexing=1,

SUM_I selection =1, Fast Lock Function=1

Latch SUM_I_NOW=1



Read SUM_I_NOW from SUM_I_ACCESS_PORT for 4 times:

SUM_I_NOW [26:24]

SUM_I_NOW [23:16]

SUM_I_NOW [15:8]

SUM_I_NOW [7:0]

Calculate new freq. SUM_I_PRE and write to SUM_I_ACCESS_PORT for 4 times:

SUM_I_PRE [26:24]

SUM_I_PRE [23:16]

SUM_I_PRE [15:8]

SUM_I_PRE [7:0]

SUM_I_PRE_SET =1

Write PLL2 M/N code and DDS feed back divider

Write New P/I code

Setting Auto Load =1

Wait for next frame start or polling Reg [2E].6

Address: AC PLL_M (M Parameter Register)			Default: 09h
Bit	Mode	Function	
7:0	R/W	PLLM[7:0] (PLL DPM value – 3)	
Address: AD PLL_N (N Parameter Register)			Default: 20h
Bit	Mode	Function	
7:4	R/W	PLLSPHNEXT[3:0] (K) (default is 0000)	
3	R/W	PLLSNBP 0: N is followed by the value of REGAD [3:1] 1: N is always 1	
2:0	R/W	PLLN[2:0] (PLL DPN value – 2) (default is 000) It is supposed to be always bigger than 2	

- PLL1_N modify to only 4-bit.
- Assume PLL1_M=0x0B, P1M=0x0B+3=14; PLL1_N=0x03, P1N=0x03+2=5; K=7; F_IN = 24.576MHz.
 $F_{PLL} = F_{IN} \times ((P1M + 7/16) / P1N) = 24.576 \times 14.4375 / 5 = 70.9632\text{MHz}$
- If the target frequency is F_ADC, the constraint of F_PLL is $(M + 7/16)/N * XTCLK < F_{PLL} < (M + 8/16)/N * XTCLK$
- Although the new dds provides +15/-16 phase margin for tracking. However it is better not to set M, N and K to be some freq. that PLL has to swallow +15/-16 phases. Because under that condition, SDM will get saturation problem.
- For NO shrink IC => PLLN setting will have no limitation
- For shrink IC and timing factor predicted as 0.8 => crystal clock 27 MHZ => PLLN can't be 0 while APLL VCO is lower than 167MHZ
 crystal clock 24.576 MHZ => PLLN can't be 0 while APLL VCO is lower than 84 MHZ
- For shrink IC and timing factor predicted as 0.9 => crystal clock 27 MHZ => PLLN can't be 0 while APLL VCO is lower than 74 MHZ
 crystal clock 24.576 MHZ => PLLN can't be 0 while APLL VCO is lower than 52 MHZ

Address: AE	PLL_CRNT (PLL Current/Resistor Register)	Default: 6Fh
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Bit	Mode	Function
7:5	R/W	PLLVR [2:0] (PLL Loop Filter Resister Control) 000: 7K 001: 9.5K 010: 12K 011: 14.5K(Default) 100: 17K 101: 19.5K 110: 22K 111: 24.5K
4:0	R/W	PLLSI [4:0] (PLL Charger Pump Current IchDpll) (Default: 00011b) $I_{cp} = 2.5\mu A + 2.5\mu A * \text{bit}[0] + 5\mu A * \text{bit}[1] + 10\mu A * \text{bit}[2] + 20\mu A * \text{bit}[3] + 30\mu A * \text{bit}[4]$

- Keep Icp/DPM constant

Address: AF PLL_WD (PLL Watch Dog Register) Default: 09h

Bit	Mode	Function
7	R	PLLSTATUS (PLL WD Status) 0: Normal (Default) 1: Abnormal
6	R/W	PLLWDRST (PLL WD Reset) 0: Normal (Default) 1: Reset
5	R/W	PLLWDSET (PLL WD Set) 0: Normal (Default) 1: Set
4:3	R/W	PLLWDVSET[1:0] (PLL WD Voltage Set) 00: 2.46V 01: 1.92V(Default) 10: 1.36V 11: 1.00V
2	R/W	HS_dds2synp latch edge 0: falling edge (Default) 1: rising
1	R/W	Reset DDS 0: normal (Default) 1: reset whole DDS
0	R/W	PLLPWDN (PLL Power Down) 0: Normal Run 1: Power Down (Default)

- HSFB_dds2synp & HS_dds2synp will be both sampled by AF [2]

**Address: B0 PLL MIX****Default: 8'b0000_000x**

Bit	Mode	Function
7	R/W	PLLSVR3
6	---	Reserved to 0
5	R/W	PLLSVC3
4	---	Reserved to 0
3	---	Reserved to 0
2:1	R/W	ADCKMODE [1:0] (ADC Input Clock Select Mode) 00: Single Clock Mode (Default) 01: Single Inverse-Clock Mode 10: External Clock Mode 11: Dual Clock Mode (1x and 2x Clock)
0	R	Swallow phase enable (K mask disabled) The pll can't enable swallow phase function while pll just be power up. Waiting for 64 clock cycles then start to enable phase swallow function. While power down, the counter will be reset. While power up, the counter start to work

Address: B1 PLLDIV_H**Default: 45h**

Bit	Mode	Function
7	---	Reserved to 0
6	R/W	Phase_Select_Method 0: Manual 1: Look-Up-Table (default)
5	R/W	PLLPH0PATH 0: Short Path (Default) 1: Long Path (Compensate PLL_ADC path delay)
4	R/W	PLLD2 0: ADC CLK=1/2 VCO CLK (Default) 1: ADC CLK=1/4 VCO CLK
3:0	R/W	PLL Divider Ratio Control. High-Byte [11:8]. (Default: 5h)

Address: B2 PLLDIV_L**Default: 2Eh**

Bit	Mode	Function
7:0	R/W	PLL Divider Ratio Control. Low-Byte [7:0]. PLLDIV should be double buffered when PLLDIV_LO changes and IDEN_STOP occurs.

- This register determines the number of output pixel per horizontal line. PLL derives the sampling clock and data output clock (DCLK) from input HSYNC. *The real operation Divider Ratio = PLLDIV+1*
- The power up default value of PLLDIV is 053Fh(=1343, VESA timing standard, 1024x768 60Hz, Horizontal time).



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- The setting of PLLDIV must include sync, back-porch, left border, active, right border, and front-porch times.
- Control-Register B1 & B2 will filled in when Control-Register B2 is written.

Address: B3**PLLPHASE_CTRL0 (Select Phase to A/D)****Default: 30h**

Bit	Mode	Function
7	R/W	PLLD2X control (Default=0)
6	R/W	PLLD2Y control (Default=0)
5	R/W	PLLX (PLL X Phase control) (Default=1)
4	R/W	PLLY (PLL Y Phase control) (Default=1)
3:0	R/W	PLLSCK [4:1] (PLL 32 Phase Pre-Select Control) (Default=0h)

Address: B4**PLLPHASE_CTRL1 (Select Phase to A/D)****Default: 00h**

Bit	Mode	Function
7	R/W	PLLSCK [0] (PLL 32 Phase Pre-Select Control) (Default=0)
6	R/W	MSB of 128 phase (Only for ADC CLK=1/4 VCO CLK) (Default=0)
5:0	R/W	Phase Select the index of Look-Up-Table[5:0] (Default=0)

- When Phase_Select_Method=1, Phase is selected by CRB4[6:0].**
- When Phase_Select_Method=0, PLLD2X, PLLD2Y, PLLX, PLLY, PLLSCLK[4:0] Should be double buffered when PLLSCK[0] is updated**

Address: B5**PLL_PHASE_INTERPOLATION****Default: 50h**

Bit	Mode	Function
7:6	R/W	PLL Phase Interpolation Control Load (Default: 01)
5:3	R/W	PLL Phase Interpolation Control Source (Default: 010)
2:1	R/W	PLL Add Phase Delay 00: Original phase selected by X,Y and 16-phase pre-select 01-11: Add 1-3 delay to Original phase selected by X,Y and 32-phase pre-select
0	R/W	Reserved to 0

Phase	[XY^^^^^]	Phase	[XY ^^^^^]	Phase	[XY ^^^^^]	Phase	[XY ^^^^^]
0	[11 00000]	16	[01 10000]	32	[10 00000]	48	[00 10000]
1	[11 00001]	17	[01 10001]	33	[10 00001]	49	[00 10001]
2	[11 00010]	18	[01 10010]	34	[10 00010]	50	[00 10010]
3	[11 00011]	19	[01 10011]	35	[10 00011]	51	[00 10011]
4	[11 00100]	20	[01 10100]	36	[10 00100]	52	[00 10100]
5	[11 00101]	21	[00 10101]	37	[10 00101]	53	[00 10101]
6	[11 00110]	22	[00 10110]	38	[10 00110]	54	[00 10110]



7	[11 00111]	23	[01 10111]	39	[10 00111]	55	[00 10111]
8	[11 01000]	24	[01 11000]	40	[10 01000]	56	[00 11000]
9	[11 01001]	25	[01 11001]	41	[10 01001]	57	[00 11001]
10	[01 01010]	26	[10 11010]	42	[10 01010]	58	[11 11010]
11	[01 01011]	27	[10 11011]	43	[10 01011]	59	[11 11011]
12	[01 01100]	28	[10 11100]	44	[00 01100]	60	[11 11100]
13	[01 01101]	29	[10 11101]	45	[00 01101]	61	[11 11101]
14	[01 01110]	30	[10 11110]	46	[00 01110]	62	[11 11110]
15	[01 01111]	31	[10 11111]	47	[00 01111]	63	[11 11111]

Address: B6 P_CODE mapping methods

Default: 18h

Bit	Mode	Function
7:6	R/W	<p>Mapping method:</p> <p>00: normal mapping P_CODE x G value (default)</p> <p>01: nonlinear mapping I smaller than Q(PE) 2 4 8 16 32 64 P_CODE x 1 2 4 8 32 128 128</p> <p>10: nonlinear mapping II P_CODE x 1 2 2 8 32 256 256</p> <p>11: nonlinear mapping III P_CODE x 1 2 8 16 32 128 512</p>
5:2	R/W	<p>G value</p> <p>0000: 0</p> <p>0001: 1</p> <p>0010: 4</p> <p>0011: 16</p> <p>0100: 64</p> <p>0101: 128</p> <p>0110: 256 (default)</p> <p>0111: 512</p> <p>1000: 1/4</p> <p>1001: 1/16</p> <p>1010: 1/64</p> <p>1011: reserved to 0</p> <p>1100: reserved to 0</p> <p>1101: reserved to 0</p> <p>1110: reserved to 0</p> <p>1111: reserved to 0</p>



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1	R/W	Adaptive tracking enable for I_CODE 0: disable to use adaptive I_CODE (default) 1: enable to use adaptive I_CODE
0	R/W	Adaptive tracking enable for P_CODE 0: disable to use adaptive P_CODE (default) <i>I: enable to use adaptive P_CODE</i>

Address: B7		PE tracking method	Default: 02h
Bit	Mode	Function	
7:6	R/W	Threshold value of Q (PE) to decide if starting adaptive tracking 00: 2 (default) 01: 4 10: 8 11: 15	
5:4	R/W	Threshold times to decide if starting adaptive tracking while Q(PE) < Threshold value successively 00: 3 (default) 01: 7 10: 11 11: 15	
3	R/W	Mask high speed testing pins (test1out, test2out, fav4) 0: normal 1: mask	
2	R/W	Adaptive tracking enable => refer to B6 [1:0] to decide if I_CODE or P_CODE enables adaptive tracking or not 0: disable (default) 1: enable	
1:0	R/W	Decrease ratio for adaptive tracking Adaptive tracking will be enabled while getting Q (PE) <=2 for over 8 times, and it will be triggered only under delay-chain mode 00: 1/2 01: 1/4 10: 1/8 (default) 11: 1/16	

Address: B8		DDS_MIX_1	Default: 06h
Bit	Mode	Function	
7:6	R	DDS tracking state [1:0]	



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		00: not lock 01: lock 10: unlock but not using new tracking mode yet 11: unlock & using new tracking mode
5:4	R/W	Reserved to 0
3:1	R/W	Judge threshold lock already => while Q (PE) keep smaller than threshold for 32 HS 000: 2 001: 4 010: 6 011: 8 (default) 100: 16 101: 32 110: 64 111: 120
0	R	PLL lock already 0: not lock already 1: lock already

Address: B9 DDS_MIX_2 Default: 00h

Bit	Mode	Function
7:0	R/W	P_code_max[16:9] Set p_code_max value to clamp the GAIN of APLL

Address: BA DDS_MIX_3 Default: 00h

Bit	Mode	Function
7:0	R/W	P_code_max[8:1] Set p_code_max value to clamp the GAIN of APLL

Address: BB DDS_MIX_4 Default: 1Bh

Bit	Mode	Function
7	R/W	P_code_max[0] Set p_code_max value to clamp the GAIN of APLL
6	R/W	New mode enable 0: disable new mode tracking (default) 1: enable new mode tracking
5:3	R/W	New mode enable threshold 000: 8 001: 20 010: 60 011: 120 (default)



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		100: 200 101: 450 110: 800 111: 1200
2:0	R/W	New mode lock threshold=> while Q (PE) keep smaller than threshold for 32 HS 000: 2 001: 4 010: 6 011: 8 (default) 100: 16 101: 32 110: 64 111: 120

- New mode enable threshold should be larger than new mode lock threshold, otherwise, the track state will always be at lock state and new mode function will not be enabled while new mode enable threshold < Q (PE) < new mode lock threshold

Address: BC**DDS_MIX_5****Default: A0h**

Bit	Mode	Function
7:6	R/W	Delay chain length select (only valid while new mode enable and track state is 01 10 11) 00: cnt=7 => 59.6ns 01: cnt=15 => 117ns 10: cnt=23 => 184.4ns (default) 11: cnt=31 => 246.8ns
5:4	R/W	Phase error sample period choose (only valid while new mode enable and track state is 01 10 11) 00: every 1 cycle sample 01: every 2 cycle sample 10: every 3 cycle sample (default) 11: every 4 cycle sample
3	R/W	Delay chain reset period select 0: short reset (2ns) (default) 1: long reset (1 fbck)
2	R/W	Reset delay chain saturation flag 0: normal (default) 1: reset flag
1	R	Delay chain saturation flag 0: not saturate 1: saturate => it need to enlarge the sample period or set bigger N code



0	R/W	APLL_free_run enable 0: normal state (default) 1: force APLL to free run state
---	-----	---

- While we got delay chain saturation flag 1'b1, that means that the big jitter is bigger than what we image and we have to reset the delay chain length setting BC [7:6]. Also we have to enlarge the sampling period & delay chain length
- The choice for sampling period will be set by the rule as following:
(Delay chain length * 78 +50) * each tap delay + 10(ns) must be < N * T_{XCLK} * sample period
if delay chain saturation flag goes high, then we must enlarge the delay chain length & set bigger sampling period
- While we enable free run mode, DDS will keep reset status until disable free run

Address: BD DDS_MIX_6

Bit	Mode	Function
7:0	R	Final M code to APLL

- While we like to read final M code & K code, we have to enable measure PE 9E[7] first.
Otherwise we will get glitch value

Address: BE DDS_MIX_7 Default: 00h

Bit	Mode	Function
7:4	R	Final K code to APLL
3:1	R/W	Change mode threshold => triggered by any Q (PE) > threshold 000: 600 (default) 001: 850 010: 1100 011: 1350 100: 1600 101: 1850 110: 2100 111: 2350
0	R/W	new_mode_i_code_en 0: while new mode enable, I code will have no effect on SUM_I. All phase error will be compensated by P code (default) 1: while new mode enable, I code will be operated as normal state

- For APLL interrupt status that include 4 different types:

No lock: initial is 1 => over lock threshold B8 [3:1] => 1

Wait state: initial is 1 => valid only while u enable new mode => over new mode enable threshold BB [5:3] =>



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New mode state: initial is 1 => valid only while u enable new mode => over new mode lock threshold BB [2:0]
=> 1

Change mode happen state: initial is 1 => over change mode threshold BE [3:1] => 1

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DISPLAY PLL (Page 1)

Register::DPLL_M						0xBF
Name	Bits	R/W	Default	Comments		Config
DPLL_M[7:0]	7:0	R/W	4E	DPLL DPM value - 2		

Register::DPLL_N						0xC0
Name	Bits	R/W	Default	Comments		Config
DPLL_RESERVED1	7	R/W	0	Reserved		
DPLL_BPN	6	R/W	0	DPLLBPN 0: N divider enable. 1: N divider disable, OUT=ckxtal.		
DPLL_O[1:0]	5:4	R/W	1	DPLL Output Divider 00: Div1 01: Div2 (Default) 10: Div4 11: Div8		
DPLL_N[3:0]	3:0	R/W	3	DPLL DPN value - 2		

- Assume DPLL_M=0x7D, DPM=0x7D+2=127; DPLL_N=0x0A, DPN=0x0A+2=12; Divider=1/4, F_IN = 24.576MHz. F_DPLL = F_IN x DPM / DPN x Divider = 24.576 x 127 / 12 / 4 = 65.024MHz.

CRBF~CRC0 are double buffer.

Register::DPLL_CRNT						0xC1
Name	Bits	R/W	Default	Comments		Config
DPLL_RS[2:0]	7:5	R/W	3	DPLL Loop Filter Resister Control 000: 16K 001: 18K 010: 20K 011: 22K (Default) 100: 24K 101: 26K 110: 28K 111: 30K		
DPLL_CS[1:0]	4:3	R/W	2	DPLL Loop Filter Capacitor Control 00: 18p		



				01: 20p 10: 24p (Default) 11: 28p	
DPLL_IP[2:0]	2:0	R/W	2	DPLL Charger Pump Current Control $I_{cp} = (2.5\mu A + 2.5\mu A * \text{bit}[0] + 5\mu A * \text{bit}[1] + 10\mu A * \text{bit}[2])$ Keep DPM/Icp constant=10.67	

DCLK Spread Spectrum (Page 1)

Register::DPLL_WD					0xC2
Name	Bits	R/W	Default	Comments	Config
DPLL_WDO	7	R	0	DPLL WD Status 0: Normal 1: Abnormal	
DPLL_WDRST	6	R/W	0	DPLL WD Reset 0: Normal (Default) 1: Reset	
DPLL_WDSET	5	R/W	0	DPLL WD Set 0: Normal (Default) 1: Set	
DPLL_FUPDN	4	R/W	1	DPLL Frequency Tuning 0: Freq Up 1: Freq Dn(Default)	
DPLL_STOP	3	R/W	1	DPLL Frequency Tuning 0: Disable 1: Enable (Default)	
DPLL_FREEZE	2	R/W	0	DPLL Output Freeze 0: Normal (Default) 1: Freeze Active high.	
DPLL_VCORSTB	1	R/W	0	Reset VCO 0: Normal (Default) 1: Reset Active high.	



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DPLL_PWDN	0	R/W	1	Power Down DPLL 0: Power on 1: Power down(Default) Active high.	
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Register::DPLL_CAL 0xC3					
Name	Bits	R/W	Default	Comments	Config
DPLL_VCOMD[1:0]	7:6	R/W	3	DPLL VCO Default Mode 00: VCO slowest 11: VCO fastest (Default)	
DPLL_CALBP	5	R/W	0	DPLL Bypass Calibration 0: Reference by Calibration result(Default) 1: Reference by CRC3[7:6] Active high.	
DPLL_CALSW	4	R/W	0	Calibration Validated Go high after power on 1200us. 0: Reference by CRC3[7:6] 1: Refernect by cal result	
DPLL_CALLCH	3	R/W	0	Latch Calibration Go high after power on 1100us. 0: Disable Latch 1: Enable Latch	
DPLL_CMPEN	2	R/W	0	CMP Enable Go high after power on 1000us. 0: Diable CMPEN 1: Enable CMPEN	
DPLL_CP	1	R/W	0	CP Control 0: 1.77pF 1: 2.1pF	
DPLL_RESERVE	0	R/W	1	Reserved for DPLL Phase Swallow Circuit 0: Path0 1: Path1	



Register:: Initial DCLK_FINE_TUNE_OFFSET_MSB 0xC4					
Name	Bits	R/W	Default	Comments	Config
DPLL_LINEAR_CHANGE	7	R/W	0	Linear change offset value function 0 : disable 1: enable (auto clear when finish) It should work on DDS Spread Spectrum Output function enable. When function is done, the initial offset and DPLLUPDN value would be the target offset and DPLLUPDN value.	
DPLL_EVEN_OLD_EN	6	R/W	0	Only Even / Odd Field Mode Enable 0: Disable (Default) 1: Enable	
DPLL_EVEN_OD_SEL	5	R/W	0	Even / Odd Field Select 0: Even (Default) 1: Odd	
DPLL_FUPDN	4	R/W	1	DPLL FUPDN (DPLL Frequency Tuning) 0: Freq Up 1: Freq Down (Default)	
DCLK_OFFSET[11:8]	3:0	R/W	0	Initial DCLK Offset [11:8] in Fixed Last Line DVTOTAL & DHTOTAL	

Register:: Initial DCLK_FINE_TUNE_OFFSET_LSB 0xC5					
Name	Bits	R/W	Default	Comments	Config
DCLK_OFFSET[7:0]	7:0	R/W	0	Initial DCLK Offset [7:0] in Fixed Last Line DVTOTAL & DHTOTAL	

Register:: DCLK_SPREAD_SPECTRUM 0xC6					
Name	Bits	R/W	Default	Comments	Config
DCLK_SPREAD_RANGE	7:4	R/W	0	DCLK Spreading range (0.0~7.5%) The bigger setting, the spreading range will bigger, but not uniform	
DCLK_FMDIV	3	R/W	0	Spread Spectrum FMDIV (SSP_FMDIV)//(0) 0: 33K 1: 66K	



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DCLK_READY	2	R/W	0	Spread Spectrum Setting Ready for Writing (Auto Clear) 0: Not ready 1: Ready to write	
FREQ_SYNTHESIS_SEL	1:0	R/W	0	Frequency Synthesis Select (F & F-N*dF) 00~11: N=1~4	

- The “Spread Spectrum Setting Ready for Writing” means 4 kinds of registers will be set after this bit is set:
 1. DCLK spreading range
 2. Spread spectrum FMDIV
 3. DCLK offset setting
 4. Frequency synthesis select

Register:: EVEN_FIXED_LAST_LINE_MSB 0xC7					
Name	Bits	R/W	Default	Comments	Config
EVEN_FIXED_LAST_LINE[11:8]	6:4	R/W	--	Even Fixed Last Line Length [11:8]	
EVEN_FIXED_DVTOTAL[11:8]	3:0	R/W	--	Even Fixed DVTOTAL [11:8]	

Register:: EVEN_FIXED_LAST_LINE_LSB 0xC8					
Name	Bits	R/W	Default	Comments	Config
EVEN_FIXED_DVTOTAL[7:0]	7:0	R/W	--	Even Fixed DVTOTAL [7:0]	

Register:: EVEN_FIXED_LAST_LINE_LENGTH_LSB 0xC9					
Name	Bits	R/W	Default	Comments	Config
EVEN_FIXED_DVTOTAL[7:0]	7:0	R/W	--	Even Fixed Last Line Length [7:0]	

- If Even / Odd mode disable, we use EVEN_FIXED_LAST only.
- If Even/Odd mode enable, the even / odd field would be reference different setting.
- Fixed last line value can't be zero, and can't smaller than DH_Sync width.

Register:: FIXED_LAST_LINE_CTRL 0xCA					
Name	Bits	R/W	Default	Comments	Config
DEGLITCH	7	R/W	0	Deglitch sscg asynchronous interface data function 0: disable 1: enable	
RSV_CA_6	6	--	0	Reserved to 0	



MEASURE_PHASE	5	R/W	0	Measure the Phase about Fixed DVTOTAL & Last Line DHTOTAL Function 0 : Disable 1 : Enable (Auto clear when finish)	
MARK_PHASE_TRACKING	4	R/W	0	Mark Phase tracking about Fixed DVTOTAL & Last Line DHTOTAL Function 0 : Disable 1 : Enable	
NED_FIXED_LAST_LINE_MODE	3	R/W	0	Enable New Design Function in Fixed Last Line Mode 0: Disable (Default) 1: Enable	
DCLK_DDS	2	R/W	0	DDS Spread Spectrum Test Enable 0: Disable (Default) 1: Enable	
DCLK_FIXED_LAST_LINE_EN	1	R/W	0	Enable the Fixed DVTOTAL & Last Line DHTOTAL Function 0: Disable (Default) 1: Enable	
DCLK_DDS_EN	0	R/W	0	Enable DDS Spread Spectrum Output Function 0: Disable (Default) 1: Enable	

Procedure:

- First, we have set M/N code and then we need to tune DCLK OFFSET to achieve frame-sync, every step of offset frequency is $DCLK/2^{15}$.
- When we finished the frame-sync, we turn on CRCA[1] to let the system running in to free-run mode, at this time, the CRC7,CRC8,CRC9 are the reference DV and DH total and Fixed last Line Length.
- But the free-run mode DVS' should be close to frame-sync mode DVS to achieve pseudo-frame-sync(actually, it is free run mode now)
- Then we use CRC6[1:0] (F-N*dF) to keep DVS' and DVS very closely to achieve pseudo-frame-sync.

Notice:

- In RTD2485XD, when all the setting above is ready, then we open spread spectrum function, the DCLK OFFSET will shift, please keep the DCLK OFFSET keeps steady when we open spread spectrum function.
- In Real free-run mode, the DV_TOTAL refers to CR2B-0B/CR2B-0C, and in Fixed-Last-Line mode, and disable “Even/Odd mode” then the free-run timing DV_TOTAL refers to CRC7/CRC8, at this time CR2B-0B/CR2B-0C serve for Vsync-timeout watch dog reference.



Register:: ODD_FIXED_LAST_LINE_MSB						0xCB
Name	Bits	R/W	Default	Comments	Config	
ODD_FIXED_LAST_LINE LENG[11:8]	6:4	R/W	--	ODD Fixed Last Line Length [11:8]		
ODD_FIXED_DVTOTAL[11:8]	3:0	R/W	--	ODD Fixed DVTOTAL [11:8]		

Register:: ODD_FIXED_LAST_LINE_DVTOTAL_LSB						0xCC
Name	Bits	R/W	Default	Comments	Config	
ODD_FIXED_DVTOTAL[7:0]	7:0	R/W	--	ODD Fixed DVTOTAL [7:0]		

Register:: ODD_FIXED_LAST_LINE_LENGTH LSB						0xCD
Name	Bits	R/W	Default	Comments	Config	
ODD_FIXED_LAST_LINE LENG[7:0]	7:0	R/W	--	ODD Fixed Last Line Length [7:0]		

Register:: DCLK_SPREAD_SPECTRUM						0xCE
Name	Bits	R/W	Default	Comments	Config	
RSV_CE_72	7:2	---	0	Reserved		
FIXED_LAST_LINE_HIT	1	R	0	Fixed Last Line Tracking time hit Field one 0:hit field zero (If field zero is odd → hit odd field) 1:hit field one (If field one is even → hit even field)		
IVS_LEAD_LAG_TO_DVS	0	R	0	IVS Lead/Lag to DVS 0 : Lag 1 : Lead		

Register:: PHASE_RESULT_MSB						0xCF
Name	Bits	R/W	Default	Comments	Config	
RSV_CF_7	7	---	0	Reserved		
PHASE_LINE[11:8]	6:4	R	0	Phase Line [11:8]		



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PHASE_PIXEL[11:8]	3:0	R	0	Phase Pixel [11:8]	
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Register:: PHASE_LINE_LSB 0xD0					
Name	Bits	R/W	Default	Comments	Config
PHASE_LINE[7:0]	7:0	R	0	Phase Line [7:0]	

Register:: PHASE_PIXEL_PIXEL 0xD1					
Name	Bits	R/W	Default	Comments	Config
PHASE_PIXEL[7:0]	7:0	R	0	Lead Phase Pixel [7:0]	

Register:: TARGET_DCLK_FINE_TUNE_OFFSET_MSB 0xD2					
Name	Bits	R/W	Default	Comments	Config
RSV_D2_75	7:5	---	0	Reserved	
TARGET_DPLLUPDB	4	R/W	0	Target DPLLUPDN (DPLL Frequency Tuning Up/Down) 0: Freq Up (Default) 1: Freq Down	
TARGET_DCLK_OFFSET[11:8]	3:0	R/W	0	Target DCLK Offset [11:8] in Fixed Last Line DVTOTAL & DHTOTAL	

Register:: TARGET_DCLK_FINE_TUNE_OFFSET_LSB 0xD3					
Name	Bits	R/W	Default	Comments	Config
TARGET_DCLK_OFFSET[7:0]	7:0	R/W	0	Target DCLK Offset [7:0] in Fixed Last Line DVTOTAL & DHTOTAL	

Register::DPLL_RESULT 0xD4					
Name	Bits	R/W	Default	Comments	Config
DPLL_REF_CLK_SEL	7	R/W	0	DPLL reference clk select: 0: xtal_clk, 1: m2pll_clk	
RSV_D4_74	6:4	---	0	Reserved	
DPLL_VO2	3	R	0	DPLL CAL OUT2	



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DPLL_VO1	2	R	0	DPLL CAL OUT1	
DPLL_CAL[1:0]	1:0	R	0	DPLL calibrated VCO code	

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Multiply PLL for Input Cyrstal (Page 1)

Register::M2PLL_M						0xE0
Name	Bits	R/W	Default	Comments	Config	
M2PLL_M[7:0]	7:0	R/W	63	M2PLL DPM value – 2 (M) * PLL output=input*(M/P)		

Register::M2PLL_N						0xE1
Name	Bits	R/W	Default	Comments	Config	
M2PLL_CP	7	R/W	0	CP Control 0:CP=1.77pF 1:CP=2.1pF		
M2PLL_BPN	6	R/W	0	M2PLLBPN=0 , N divider enable M2PLLBPN=1, N divider disable , OUT=ckxtal		
M2PLL_O[1:0]	5:4	R/W	1	M2PLL Output divider 00:Div1, 01:Div2, 10:Div4, 11:Div8		
M2PLL_N[3:0]	3:0	R/W	3	M2PLL DPN value - 2		

Note: CRE0~E1 are double buffer

CRE2~E3 are not controlled by software reset.

Register::M2PLL_CRNT						0xE4
Name	Bits	R/W	Default	Comments	Config	
M2PLL_RS[2:0]	7:5	R/W	3	M2PLL Loop Filter Resister Control(Rs) 000:16K, 001:18K, 010:20K, 011:22K 100: 24K, 101: 26K, 110:28K, 111:30K		
M2PLL_CS[1:0]	4:3	R/W	2	M2PLL Loop Filter Capacitor Control(Cs) 00:18p, 01:20p, 10:24p, 11:28p		
M2PLL_IP[2:0]	2:0	R/W	2	M2PLL Charge Pump Current Control Icp=(2.5uA+2.5uA*bit[0]+5uA*bit[1]+10uA*bit[2]) Keep DPM/Icp constant=10.67		

Register::M2PLL_WD						0xE5
Name	Bits	R/W	Default	Comments	Config	
M2PLL_WDO	7	R	0	M2PLL WD Status register 0:Normal 1:Abnormal		



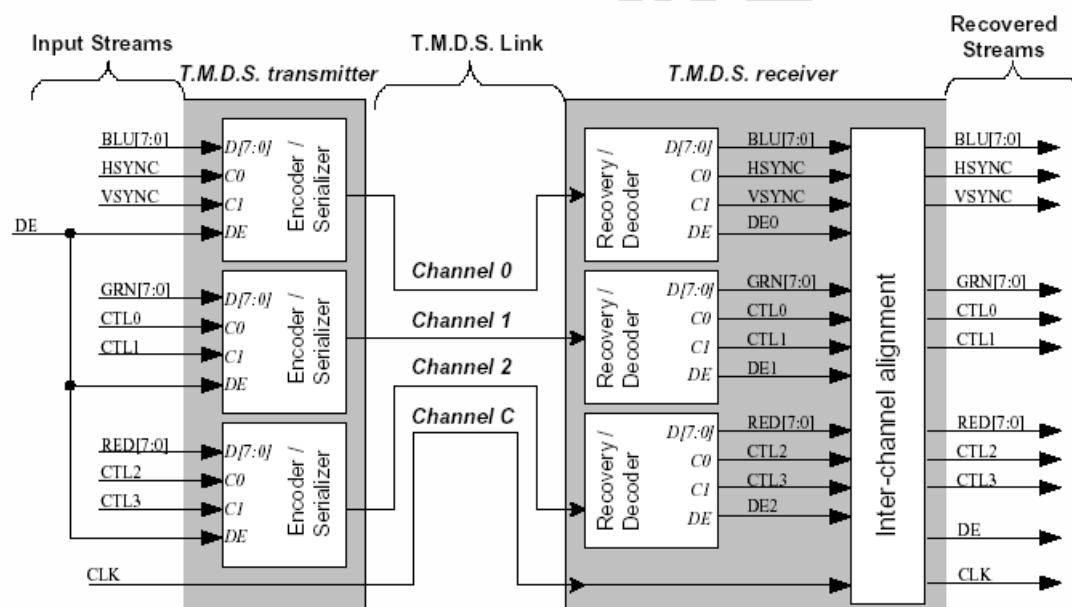
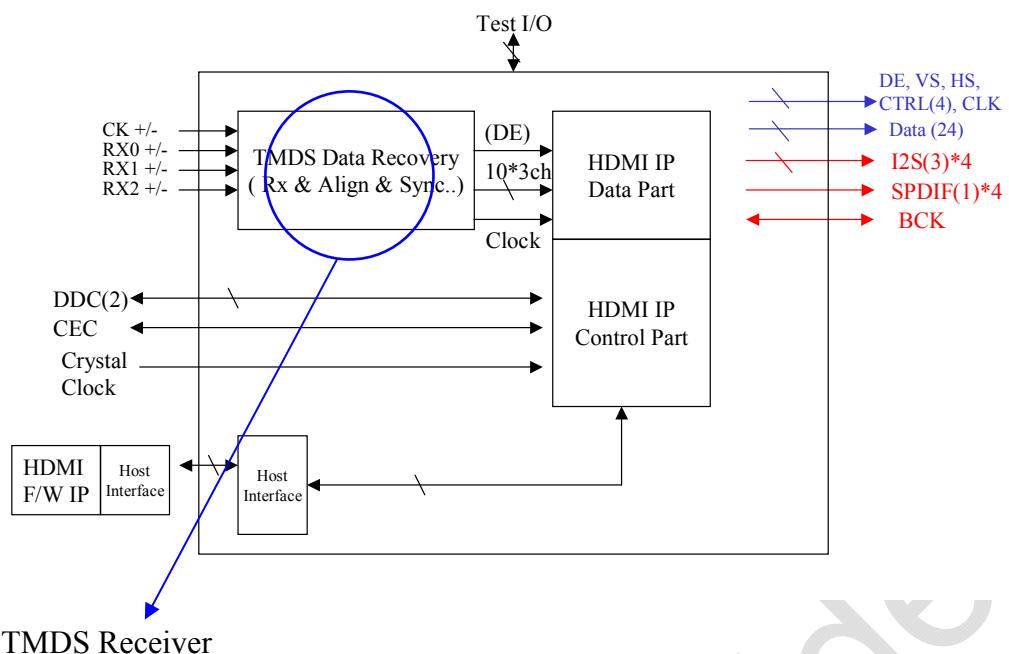
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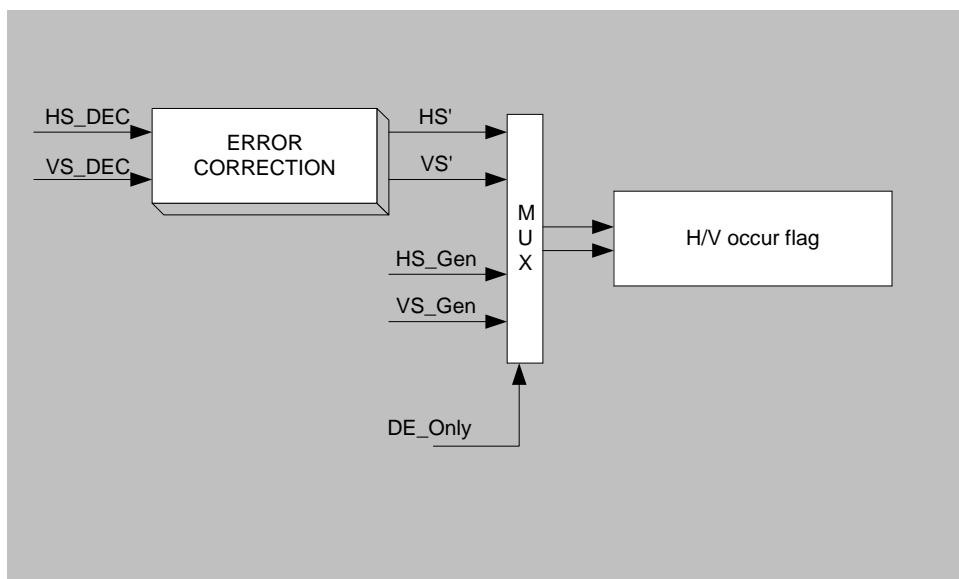
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M2PLL_WDRST	6	R/W	0	M2PLL WD Reset 0:Normal 1:Reset
M2PLL_WDSET	5	R/W	0	M2PLL WD Set 0:Normal 1:Set
M2PLL_VCOMD[1:0]	4:3	R/W	3	M2PLL VCO Default mode 00: VCO slowest 11: VCO fastest
M2PLL_FREEZE	2	R/W	0	M2PLL Output Freeze 0:Normal 1:Freeze (active high)
M2PLL_VCOSTB	1	R/W	0	RESET VCO (active high)
M2PLL_PWDN	0	R/W	0	Power Down M2PLL (active high) 0: Power On 1: Power Down



Overall DVI System Function Block (Page 2)





Register: TMDS_MSR 0XA1				
Name	Bits	R/W	Reset State	Comments
TMM (reg_new_method)	7	R/W	0	<p>(greg → equalsel) Transition measurement method of hsync or data enable</p> <p>0: old method => Measure the number of transition for N-clock duration (TMDS_NCP[3:0]: [3:0]*(1/12) ms)</p> <p>1: new method => Measure the number of transition smaller than 16 or 64 clock period (TMDS_CTC: 0xA2[0]) for 1-frame duration(vsync)</p>
MT (reg_time_sel)	6:4	R/W	0	<p>(greg → equalsel) Measure times(exponential of 2)</p> <p>000: 1 ($2^{\{0\}}=1$ time window) 001: 2 ($2^{\{1\}}=2$ time window) 010: 4 ($2^{\{2\}}=4$ time window) 011: 8 ($2^{\{3\}}=8$ time window) 100: 16 ($2^{\{4\}}=16$ time window) 101: Not available 110: Not available 111: Not available</p> <p>This function will do bit [6:4] times, each time lasts for bit [3:0]*(1/12) ms.</p>
NCP (reg_perd)	3:0	R/W	0	<p>(greg → equalsel) Numbers of Clock Period, measurement window duration (where clock frequency is 12KHz)</p> <p>0000: 16 0001: 1 0010: 2 0011: 3 1111: 15</p> <p>This function will do bit [6:4] times, each time lasts for bit [3:0]*(1/12) ms.</p>



Register: TMDS_MRR0					0XA2
Name	Bits	R/W	Reset State	Comments	
TMS (reg_start)	7	R/W	0	(greg → equalsel) Transition Measurement Start 0: Stop measure, Cleared after finish (Default) 1: Start measure	
MRS (reg_meas_sel)	6:5	R/W	0	(greg → equalsel) The selection of Measure Result 00: AVE Value (Default) 01: Max Value 10: Min Value	
MS (reg_dehs_sel)	4:3	R/W	0	(greg → equalsel) The Selection of transition measurement of Hsync and Data_enable (select Hsync or Data enable) 00: Measure Hsync transition times before error correction(errc) [from channel decoder]. 01: Measure Hsync transition times after error correction(errc) [from errc]. 10: Measure Data Enable transition times before error correction(errc) [from channel decoder]. 11: Measure Data Enable transition times after error correction(errc) [from errc].	
DE_INV_DISA BLE (reg_de_inv_dis)	2	R/W	0	(greg → hdmi_rx_top) Disable The Inversion of RGB channel Data Enable from data align (RGB channel together change polarity) 0: Invert Data Enable 1: Keep the original polarity of Data Enable	
CRC_NONSTA BLE (crc_non_stable _ro)	1	R	0	(crc_check → greg) Check CRC is stable or not (write 1 clear) 0: means CRC is stable. 1: means CRC is not stable.	
CTC (reg_dbnc_sel)	0	R/W	0	(greg → equalsel) Criterion of Transition Count(debounce times), duration smaller than 0: 16 clock 1: 64 clock	

Register: TMDS_MRR1					0XA3
Name	Bit s	R/W	Reset State	Comments	
CRC_DONE (crc_done)	7	R	0	(crc_check → greg) CRC Calculation Finished flag (Calculation starts when 0xA4 bit 0 setting to 1) 0: not finished. 1: finished.	
VMR (meas_result)	6:0	R	0	(equalsel → greg) Transition measure result [6:0] of hsync or data_enable (Item refer to MS)	



Register::: TMDS_CTRL 0XA4				
Name	Bits	R/W	Reset State	Comments
BCD (de_low128_b)	7	R	x	(channel_status_fw → greg) Blue-Channel Detect whether data_enable is low 128 clk (DE low 128 clock)(write 1 clear) 0: no 1: yes
GCD (de_low128_g)	6	R	x	(channel_status_fw → greg) Green-Channel Detect whether data_enable is low 128 clk (DE low 128 clock)(write 1 clear) 0: no 1: yes
RCD (de_low128_r)	5	R	x	(channel_status_fw → greg) Red-Channel Detect whether data_enable is low 128 clk (DE low 128 clock)(write 1 clear) 0: no 1: yes
HO (hs_ocr)	4	R	x	(greg) The source of Hsync is from HDCP. Detect whether Hsync Occurs (write 1 clear) 0: no 1: yes
YO (vs_ocr)	3	R	x	(greg) The source of Vsync is from HDCP. Detect whether Vsync Occurs (write 1 clear) 0: no 1: yes
CRCTS (reg_crc_sel)	2:1	R/W	0	(greg → crc_check) The selection of CRC calculation type 00: do CRC calculation only with DE 01: do CRC calculation only with DIEN (Data Island Enable) 10: do CRC calculation with both DE and DIEN 11: reserved
CRCC (reg_crc_en)	0	R/W	0	(greg → crc_check) CRC calculation enable 1: enable CRC calculation 0: disable CRC calculation

Register::: TMDS_CRCOB2 0XA5				
Name	Bits	R/W	Reset State	Comments
CRCOB2 (crc_result)	7:0	R	--	(crc_check → greg) 1 st read=> Output CRC-48 bit 47~40 2 nd read=> Output CRC-48 bit 39~32 3 rd read=> Out put CRC-48 bit 31~24 4 th read=> Out put CRC-48 bit 23~16 5 th read=> Out put CRC-48 bit 15~8



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			6 th read=> Out put CRC-48 bit 7~0
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- The read pointer should be reset when 1. CRC Output Byte is written 2. CRC Check starts.
- The read back CRC value address should be auto-increase, the sequence is shown above

Register::: TMDS_OUTCTL 0XA6				
Name	Bits	R/W	Reset State	Comments
AOE (reg_video_out_md)	7	R/W	0	(greg → video_fsm) Auto Output Enable (video output fsm mode) 0: Disable (Default), manual mode, determined by [6:3] 1: Enable, auto mode, determined by de_low128 from channel status
TRCOE (reg_ch_r_out_en_fw)	6	R/W	0	(greg → video_fsm) TMDS R Channel Output Enable 0: Disable (Default) 1: Enable
TGCOE reg_ch_g_out_en_fw)	5	R/W	0	(greg → video_fsm) TMDS G Channel Output Enable 0: Disable (Default) 1: Enable
TBCOE reg_ch_b_out_en_fw)	4	R/W	0	(greg → video_fsm) TMDS B Channel Output Enable 0: Disable (Default) 1: Enable
OCKE (reg_vclk_out_en_fw)	3	R/W	0	(greg → video_fsm) OCLK Enable (vclk output) 0: Disable (Default) 1: Enable
OCKIE (reg_vclk_out_inv)	2	R/W	0	(greg → video_ckgen) OCLK Invert Enable 0: Normal (Default), not invert vclk out 1: Enable, invert vclk out
de_err_pulse_en (reg_de_err_pulse_en)	1	R/W	0	(greg → channel_status) Enable reset de_low128 according to data_enable error pulse, data_enable error pulse comes from data_align function (0: disable) (1: enable)
CLK25XINV (greg:reg_clk25_i_nv) (video_ckgen: reg_clkin_inv)	0	R/W	0	(greg → video_ckgen) Input 1x Clock Invert (invert b/g/rclk10_in_mux, RGB clk together invert) 0: No Invert (Default) 1: Invert

Register: TMDS_PWDCTL 0xA7				
Name	Bits	R/W	Reset State	Comments
DEO (reg_de_on_ly)	7	R/W	0	(greg → channel_sync, errc, video_fsm, hdmi_rx_top) DE-only: Generate VS/HS from DE signal 0: Disable (Default) (vsync/hsync from the data which HDMI solve) 1: Enable (vsync/hsync from sync_autogen)
BRCW (reg_br_sw_ap)	6	R/W	0	(greg → hdmi_rx_top) B/R channel swap 0: No swap (Default)



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				1: Swap
PNSW (reg_pn_sw_ap)	5	R/W	0	(greg → hdmi_rx_top) P/N Swap, invert data (RGB channel together invert) 0:No swap(Default) 1:swap
ICCAF (reg_video_in_md)	4	R/W	0	(greg → video_fsm) Input Channel control by auto function (video output fsm mode) 0: Manual mode, determined by [3:0] 1: Auto mode (Default)
ECC (reg_vclk_i_n_en_fw)	3	R/W	0	(greg → video_fsm) Enable Clock channel: turn on clock channel PLL (For manual use) 0: Disable (Default) 1: Enable
ERIP (reg_ch_r_i_n_fw)	2	R/W	0	(greg → video_fsm) Enable Red input port (For manual use, cut off 50ohm internal resistor) 0: Disable (Default) 1: Enable
EGIP (reg_ch_g_in_en_fw)	1	R/W	0	(greg → video_fsm) Enable Green input port (For manual use, cut off 50ohm internal resistor) 0: Disable (Default) 1: Enable
EBIP (reg_ch_b_in_en_fw)	0	R/W	0	(greg → video_fsm) Enable Blue input port (For manual use, cut off 50ohm internal resistor) 0: Disable (Default) 1: Enable

Register:: TMDS_ACC0 0XA8				
Name	Bits	R/W	Reset State	Comments
TUNE_UP_DOWN (reg_avmut_e_win_tune[7])	7	R/W	0	(greg → Ireg) AVMUTE Window Range Tune Up or Tune Down 0: Tune Down, decrease AVMUTE Window Range 1: Tune Up, increase AVMUTE Window Range
TUNE_RANGE (reg_avmut_e_win_tune[6:0])	6:0	R/W	0	(greg → Ireg) AVMUTE Window Range If tune up, valid window = 384 cycle + 2*AVMUTE window range. If tune down, valid window = 384 cycle - 2*AVMUTE window range.

Register:: TMDS_ACC1 0XA9				
Name	Bits	R/W	Reset State	Comments
WR_AKSV_FLAG (wr_aksv_flag)	7	R	0	(I2C → greg, Ireg) Write AKSV Flag When TX writing AKSV done, this flag will be asserted.



				This flag will be clear by 0xAA[7].
RD_RI_FLAG (rd_ri_flag)	6	R	0	<p>(I2C → greg, lreg) Read Ri Flag When TX reading HDCP's Ri, this flag will be asserted. When TX reading HDCP's Ri, this flag will be asserted. This flag will be clear by 0xAA[6].</p>
RD_BKSV_FLAG (rd_bksv_flag)	5	R	0	<p>(I2C → greg, lreg) Read BKSV Flag When TX reading HDCP's BKSV, this flag will be asserted. When TX reading HDCP's BKSV, this flag will be asserted. This flag will be clear by 0xAA[5].</p>
Reserved (reg_spadtst1)	4:0	--	0	Reserved

Register::: TMDS_ABC 0xAA				
Name	Bits	R/W	Reset State	Comments
CLR_AKSV_FL AG	7	R/W	0	<p>(greg) Clear Write AKSV Flag Used to clear 0xA9 bit 7 by making a falling edge manually. (write 1 -> 0 -> 1 : clear flag)</p>
CLR_RI_FLAG	6	R/W	0	<p>Clear Read Ri Flag Used to clear 0xA9 bit 6 by making a falling edge manually. (write 1 -> 0 -> 1 : clear flag)</p>
CLR_BKSV_FL AG	5	R/W	1	<p>Clear Read BKSV Flag Used to clear 0xA9 bit 5 by making a falling edge manually. (write 1 -> 0 -> 1 : clear flag)</p>
IRQ_AKSV_EN (wr_aksv_irq_en)	4	R/W	1	<p>(greg → lreg) IRQ Control For AKSV(WR_AKSV_FLAG) (when wr_aksv_flag =1, whether to enable irq_fw) 0: Disable 1: Enable</p>
IRQ_RI_EN (rd_ri_irq_en)	3	R/W	0	<p>(greg → lreg) IRQ Control For Ri (RD_RI_FLAG) (when rd_ri_flag = 1, whether to enable irq_fw) 0: Disable 1: Enable</p>
IRQ_BKSV_E_N (rd_bksv_irq_e n)	2	R/W	0	<p>(greg → lreg) IRQ Control For BKSV(RD_BKSV_FLAG) (when rd_bksv_flag = 1, whether to enable irq_fw) 0: Disable 1: Enable</p>



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Reserved	1:0	--	1	Reserved
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Register::: TMDS_ACC2 0XAB				
Name	Bits	R/W	Reset State	Comments
FCOF (result_xv_ovfl)	7	R	0	(ackg_regmap → greg) (ackg_regmap → greg) Frequency Counter Overflow Flag for low-frequency input clk. If input clk is less than or equal to 12.5MHz, this flag will be 1. This flag will be clear when enable input clk measurement (0x28[3]).
HDCP_VS_SEL (greg: reg_pagainl[1]) (hdcp_rx_fsm: reg_hdcp_vs_s el)	6	R/W	0	(greg → hdcp_rx_fsm) HDCP Vsnc Selection 0: Choose original Vsnc. (from erre) 1: Choose Virtual Vsnc. (from sync_autogen)
DP_BLAN K_KEEP_EN (reg_dp_blank_k eep_en)	5	R/W	0	(greg → DP) reserved
DP_BLAN K_EN (reg_dp_blank_e n)	4	R/W	0	(greg → DP) reserved
DP_BLAN K_PRE_EN (reg_dp_blank_p re_en)	3	R/W	0 1	(greg → DP) reserved
Reserved	2:1	--	0 2	Reserved.
REG_HS_WIDTH_SEL (greg: reg_sibinl) (sync_autogen:re g_hd_width_sel)	0	R/W	0	(greg → sync_autogen) Hsync Pulse Width Selection 0: 8 clock cycle width, clk is dclk 1: 72 clock cycle width, clk is dclk

Register::: TMDS_Z0CC2 0xAC				
Name	Bits	R/W	Reset State	Comments
DDCDBNC (greg:reg_stunel)	7	R/W	1	(greg → i2c, video_ckgen) HDCP DDC DEBOUNCE



) (i2c:reg_ddc_dly)				0: Disable 1: Enable
HDE (reg_hdmi_en)	6	R/W	0	(greg → gdi_rx_ctrl) HDMI/DVI function enable (HDCP enable is moved to HDCP) 0: Disable, gated clock and cut off TMDS pull up resistor for saving power. [disable rx_pow/rx_cmu_en, z0_en] 1: Enable.
DBNC_LEVEL (greg: reg_adjrl[3]), (hdcp: dbnc_level_se el)	5	R/W	1	(greg → i2c) HDCP Debounce Level Selection 0: Crystal period * 4 1: Crystal period * 8 When using 14.318 Mhz crystal clock, debounce level should be set to 0.
KM_CLK_SEL (greg: reg_adjrl[2]), (hdcp: reg_kmclk_se l)	4	R/W	0	(greg → HDCP) Clock Selection for KM Calculation 0: Choose EMCU non-stop clock 1: Choose crystal clock
Reserved (reg_adjrl[1:0], reg_srextl[1:0])	3:0	R/W	3	(greg) Reserved to 0

Register::: TMDS_CPS					0xAD
Name	Bits	R/W	Reset State	Comments	
PLL_DIV2_EN (greg: reg_crf5_b7 _rsv) (hdmi_rx_to p: reg_pll_div2 _en)	7	R/W	0	(greg → hdmi_rx_top) HDMI output clock div 2 (enable this register if 2x clock is needed) (vcclk div2) 0: disable 1: enable	
CLKV_ME_AS_SEL (greg: reg_sckvcset l), Hdmi_rx_to p:	6:5	R/W	01	(greg → hdmi_rx_top) Input Clock Source(dp_clk from PHY) Selection. 00: Red clock (Lane 0 clock) 01: Blue clock (Lane 2 clock)) 10: Green clock (Lane 1 clock) 11: TMDS clock (Lane 3 clock)	



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reg_clxsrc_c lkv_sel				
CLKC_ME AS_SEL (greg_reg_sc kil[2]), hdmi_rx_top : reg_clksrc_c lkx_sel)	4	R/W	1	(greg → hdmi_rx_top) Detection Clock Source Selection. 0: Use TMDS clock(dp_clk[3]) as reference clock to detect input clock frequency. 1: Use crystal clock(xclk) as reference clock to detect input clock frequency.
CLR_INFO FRAME_D VI (greg_reg_sc kil[1]), hdmi_rx_top : reg_dvi_clr_inform)	3	R/W	0	(greg → hdmi_rx_top) Clear info-frame data 0: Disabled. 1: Enabled.
AUTO_DVI 2HDMI (greg_reg_sc kil[0]), hdmi_rx_top : reg_auto_hd mi2dvi)	2	R/W	0	(greg → channel_dec) Auto switch to DVI mode when no signal being detected. 0: Disabled. 1: Enabled
Reserved (reg_sckrl)	1:0	--	10	Reserved.

Register::: TMDS_RPS 0XAE				
Name	Bits	R/W	Reset State	Comments
AVMUTE_FLAG (greg: reg_crf6 _b7_rsv), (packet:	7	R/W	0	(greg → packet_class) Ignore AVMUTE Flag 0: Disable 1: Enable (clear avmute)



reg_auto_avmute_clr_en)				
reg_ssavcs_etl	6:5	-- R/W	01	Reserved
reg_ssail	4:2	R/W	010	Reserved
HDCP_KE_Y_RDY (reg_key_rdy)	1	R/W	0	<p>HDCP KEY Ready Flag</p> <p>This flag is for F/W to indicate HW that HDCP key is READY!</p> <p>0: HDCP key not ready.</p> <p>1: HDCP key ready.</p>
AUTHST_MODE_SEL (reg_authst_pls_sel)	0	R/W	0	<p>Selection of AUTHST mode.</p> <p>0: Original mode.</p> <p>1: New mode, H/W will keep authst signal until HDCP key is ready.</p>

Register::: TMDS_WDC 0xAF				
Name	Bits	R/W	Reset State	Comments
Reserved	7:4	--	--	reserved
CKWDCO_N	3:2	R/W	0	(greg) Reserved to 0
SAWDCO_NL	1:0	R/W	0	(greg) Reserved to 0

Register::: TMDS_UDC0 0XB5				
Name	Bits	R/W	Reset State	Comments
Reserve	7	R/W	0	Reserve
Reserved (reg_nl_auto)	6:3	--	B	(greg) Reserved.



,				
reg_stable_c nt)				
CPTEST (reg_cptest)	2	R	0	<p>(greg → video_ckgen) CPTEST (RGB channel together change) 0: normal mode, in which clock and data from Analog PHY are used. 1: select TSTCKIN/TSTDIN as input 2X5 clock and data respectively, for TESTING.</p>
HMTM (reg_enc_ mode)	1:0	R/W	0	<p>(greg → channel_dec) HDCP MP TESTING MODE Force CTL[3:0] always equal to 00:Original, from channel_sync 01:CTRL=1001 10:CTRL= 0001 11:CTRL=0000</p> <p>6093: HDCP MP TESTING MODE Force CTL[3:0] always equal to 00:Original 01:CTRL=1001 (F/W) 10:CTRL=1000 11:CTRL=0000</p>

Register::: TMDS_UDC1 0XB6				
Name	Bits	R/W	Reset State	Comments
no_clk_in	7	R	0	<p>(freqdet → greg)</p> <p>No clock input.</p> <p>0: normal</p> <p>1: no clock</p>
cdr_rdy_red	6	R	0	<p>(hdmi_rx_top → greg)</p> <p>CDR ready of red channel from digital PHY</p>
cdr_rdy_grn	5	R	0	<p>(hdmi_rx_top → greg)</p> <p>CDR ready of green channel from digital PHY</p>
cdr_rdy_blu	4	R	0	<p>(hdmi_rx_top → greg)</p> <p>CDR ready of blue channel from digital PHY</p>
reserved	3:0	--	0	Reserved.

Register::: TMDS_UDC2 0XB7				
Name	Bits	R/W	Reset State	Comments
NL (reg_errc_s el)	7:5	R/W	0	<p>(greg →errc) The selection of error correction ERRC_SEL<2:0> 000: original signal 001: 1 cycle debouncing</p>



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				010: 1+8 cycle debouncing 011: 1+8 cycle debouncing + de masking transition of vs/hs 100: 1+8 cycle debouncing + de masking transition of vs/hs + masking first 8-line de
NLFW (reg_dbg_s el)	4:0	R/W	0	(greg → dbgbox) The selection of debug signal, total has 32 kinds of debug signals. 00000: dbg_out_0 00001: dbg_out_1 11111: dbg_out_31

Register:: TMDS_OUT_CTRL					0xB9
Name	Bits	R/W	Reset State	Comments	
TMDS_BYP ASS (reg_tmds_by pass)	7	R/W	1	(greg → hdmi_rx_top) TMDS Bypass Control 0: RGB values will be assigned by register's setting when it is out of data enable region(determined by 0xBA ~ 0xBF) 1: RGB values will be set to 16'b0 when it is out of the data enable region	
Rev	6:0	---		Reserved	

Register:: TMDS_ROUT_HIGH_BYTE					0xBA
Name	Bits	R/W	Reset State	Comments	
TMDS_RO UT_H (reg_rout_h)	7:0	R/W	0	(greg) TMDS Rout High Byte Register Value High Byte [15:8]	

Register:: TMDS_ROUT_LOW_BYTE					0xBB
Name	Bits	R/W	Reset State	Comments	
TMDS_RO UT_L (reg_rout_l)	7:0	R/W	0	(greg) TMDS Rout Low Byte Register Value Low Byte [7:0]	

Register:: TMDS_GOUT_HIGH_BYTE					0xBC
Name	Bits	R/W	Reset State	Comments	
TMDS_GO UT_H (reg_gout_h)	7:0	R/W	0	(greg) TMDS Gout High Byte Register Value High Byte [15:8]	



Register:: TMDS_GOUT_LOW_BYTE					0xBD
Name	Bits	R/W	Reset State	Comments	
TMDS_GO_UT_L (reg_gout_l)	7:0	R/W	0	(greg) TMDS Gout Low Byte Register Value Low Byte [7:0]	

Register:: TMDS_BOUT_HIGH_BYTE					0xBE
Name	Bits	R/W	Reset State	Comments	
TMDS_BO_UT_H (reg_bout_h)	7:0	R/W	0	(greg) TMDS Bout High Byte Register Value High Byte [15:8]	

Register:: TMDS_BOUT_LOW_BYTE					0xBF
Name	Bits	R/W	Reset State	Comments	
TMDS_BO_UT_L (reg_bout_l)	7:0	R/W	0	(greg) TMDS Bout Low Byte Register Value Low Byte [7:0]	



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Register::: HDCP_CR 0XC0				
Name	Bits	R/W	Reset State	Comments
Reserve (key_bist_en_lt)	7	R	0	(hdcp_rx_reg) Reserved.
Reserve	6	R	0	Reserved.
IVSP (vs_por)	5	R	0	Indicate VSYNC Polarity 0: Positive Vsync, which means VS pulse is high. 1: Negative Vsync
INVVS (vs_ctrl)	4	R/W	0	(hdcp_rx_reg) Invert VSYNC for HDCP when vs_manual mode (bit[3] = 1) 1: Inverte vsync 0: Not inverte vsync
IVSPM (vs_manual)	3	R/W	0	(hdcp_rx_reg) Indicate VSYNC Polarity Mode: 1: manual mode, decided by INVVS (vs_ctrl) 0: auto mode, indicate by IVSP
MADDF (mcufirst)	2	R/W	0	(hdcp_rx_reg → i2c) MCU Access DDC data first (when download key from MCU, force only MCU could work) 0: enable DDC channel and MCU access only when DDC is not busy 1: disable DDC channel and MCU access only
DKAPDE (key_dl_en)	1	R/W	0	(hdcp_rx_reg → km_add) Device Key Access Port download enable (download key from MCU) 1: enable 0: disable, this would reset the address of Device Key Access Port to 0.
Enable (hdcp_en)	0	R/W	0	(hdcp_rx_reg → hdcp_rx_fsm, i2c) HDCP Enable 1: Auto Enable HDCP function, when Tx I2C write Aksv 0: Disable HDCP, except for output.

Register::: HDCP_DKAP 0XC1				
Name	Bits	R/W	Reset State	Comments
DKAP	7:0	R/W	0	When enable device key accessing 40x56 table, the 56-bit key table will be transferred to 64-bit pseudo data with 7 th , 15 th , 23rd, 31st, 39 th , 47 th , 55 th bits inserted. The inserted data are ‘0’.And the write sequence is: {D0-Byte0, D0-Byte1, D0-Byte2, D0-Byte3, D0-Byte4, D0-Byte5, D0-Byte6, D0-Byte7}, {D1-Byte0, D1-Byte1, 1-Byte2, D1-Byte3, D1-Byte4, D1-Byte5, D1-Byte6, D1-Byte7}, Accessing this port must be coded/decoded by REALTEK protection code.



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Register::: HDCP_PCR 0xC2				
Name	Bits	R/W	Reset State	Comments
Rev	7:5	R/W	0	Reserved
ENC_TOG	4	R	0	ENC toggled.
AVMUTE_DIS (reg_avmuted_enc_dis)	3	R/W	1	(hdcp_rx_reg → decrypt_out) Auto enc_dis when AVMUTE (when avmute, reg_avmuted_enc_dis=1 => decrypt_en =0) 0: non active 1: active
DDCSEL (reg_ddc_chsel)	2:1	R/W	0	(hdcp_rx_reg → hdmi_rx_top) DDC Channel SEL for Key Access 00: DDCSCL2/DDCSDA2(pin 123~124) 01: DDCSCL3/DDCSDA3(pin 121~122) 1x: reserved
APAI (ddc_inc_dis)	0	R/W	0	(hdcp_rx_reg) HDCP Accessing Port Auto Increase (For Host Side) (ddc_adr_inc, when access 0xC3, APAI=0 means that address will auto increase) 0: auto increase 1: keep in the same address.

Register::: HDCP_AP 0XC3				
Name	Bits	R/W	Reset State	Comments
AP	7:0	R/W	0	Address port for embedded HDCP access , auto increase after DATA_PORT being accessed. (For Host Side controlled by APAI)

Register::: HDCP_DP 0XC4				
Name	Bits	R/W	Reset State	Comments
DP	7:0	R/W	0	Data port for embedded HDCP access

Note : When accessing this DDC register map by DDC, the address should increase automatically, except for the first accessing address is KSV_FIFO, 0x43.

Following register is assigned by “HDCP-address port”, “HDCP-data port”

Register::: HDCP_BCAPS 0x40				
Name	Bits	R/W	Reset State	Comments
HDMI_RESERVED (hdmi_rsv)	7	R/W	1	HDMI_RESERVED Use of this bit is reserved. HDCP Receivers not capable of supporting HDMI must clear this bit to 0.
REPEATER	6	R	0	REPEATER HDCP Repeater capability. When set to one, this HDCP



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				Receiver supports downstream connections as permitted by the Digital Content Protection LLC license. This bit does not change while the HDCP Receiver is active.
READY	5	R	0	READY KSV FIFO ready. When set to one, this HDCP Repeater has built the list of attached KSVs and computed the verification value V'. This value is always zero during the computation of V'. See states C0 and C2.
FAST	4	R	1	FAST When set to one, this device supports 400 KHz transfers. When zero, 100 KHz is the maximum transfer rate supported. Note that 400KHz transfers are not permitted to any device unless all devices on the I2C bus are capable of 400KHz transfer. The transmitter may not be able to determine if the EDID ROM, present on the HDCP Receiver, is capable of 400KHz operation. This bit does not change while the HDCP Receiver is active.
Reserved	3:2	R	0	Reserved to 0
1.1_FEATURES (hdmi_feature)	1	R/W	1	1.1_FEATURES When set to one, this HDCP Receiver supports Enhanced Encryption Status Signaling (EESS), Advance Cipher, and Enhanced Link Verification options. For the HDMI protocol, Enhanced Encryption Status Signaling (EESS) capability is assumed regardless of this bit setting. This bit does not change while the HDCP Receiver is active.
FAST_REALERTIFICATION	0	R	1	FAST_REALERTIFICATION When set to 1, the receiver is capable of receiving (unencrypted) video signal during the session re-authentication. All HDMI-capable receivers shall be capable of performing the fast reauthentication even if this bit is not set. This bit does not change while the HDCP Receiver is active.

Register::: HDCP_FCR 0xC0				
Name	Bits	R/W	Reset State	Comments
Reserved	7	R	--	Reserved
FC	6:0	R	0	HDCP frame counter[6:0]

Register::: HDCP_SIR 0xC1				
Name	Bits	R/W	Reset State	Comments
AST	7	R	0	Authst (Means bksv of RTD pass Tx authorization, Tx is ready to do HDCP transaction)
AKM	6	R	0	Authkm (Means RTD finish computing KM, ri)
ADNE	5	R	0	Authdone (means TX admitted ri value, start to do HDCP transmission)



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REA	4	R/W	0	RE AUTH
ENCM	3	R/W	0	ENC Method
ENCE	2	R	0	ENC_ERROR
NC	1	R	0	NO CTRL(HDCP1.0: no ctrl[3], HDCP1.1: ctrl is not 1001 nor 0001)
IB	0	R	0	Internal buffer for Ainfo[1]. Since Ainfo[1] in DDC port is 0 at most of time, we need to know what Tx wrote.

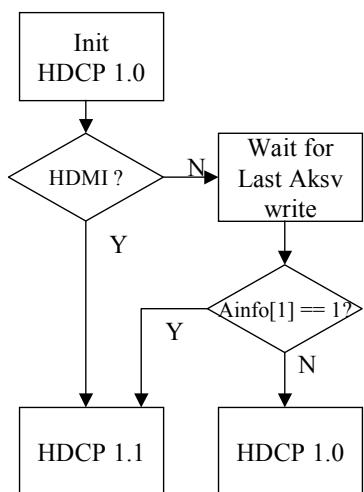
Register::: HDCP SLAVE ADD 0xC2				
Name	Bits	R/W	Reset State	Comments
Reserved	7	R	0	---
Slave_AD DR	6:0	R/W	3A	HDCP Slave_Addr[6:0] Ex. HDCP address = 0x74, 8'b 0111 0100 Reg_Slave_Addr[6:0] = 0111 010 ... the last bit is ignored.

HDCP 1.1/1.0 decide flow.

1. If HDMI conditions happen, HDCP 1.1 is used.
2. When last byte of Aksv is written, Ainfo[1] indicates HDCP 1.0/1.1 mode.

OESS is the same as HDCP 1.0. We could tell it by Ainfo[1] in DDC.

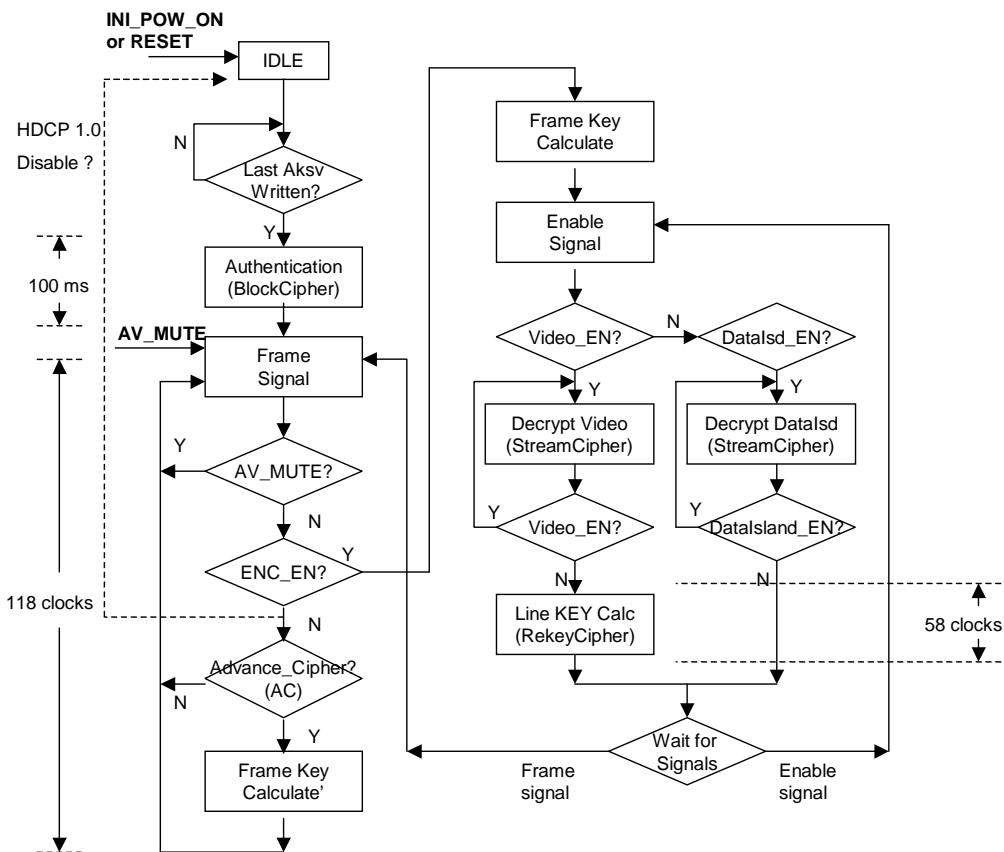
HDCP 1.0/1.1 decide flow
(Before Auth)



Initial flow.



HDCP Total Flow



HDCP 1.0/1.1 difference

Item	Description	HDCP 1.0	HDCP 1.1
1	Fast Reset	No constraint in 1.0	It must be done
2	DDC : Ainfo	Useless	Double buffer
3	DDC : Pj	No this feature	Update per 16 frames
4	DDC : Bcaps[1]	No this feature	It is used to tell if Rx supports 1.1
5	DDC : Bstatus	No this feature	HDMI mode mapping
6	DDC : short read	Read Ri.	Read Ri & Pj.
7	OESS/EESS	Only OESS compatible	Depend on DDC info. Sync.
8	Support protocol	DVI (DE only)	DVI & HDMI (DE & DIEN)
9	CTLx position	CTL3 follows VS	All info must be in opp. window.
10	Error correction	No the requirement	Error correction for ENC_EN/DIS
11	VS polarity distinction	No clear description	1. init is neg. 2. VS debouncing before DE. 3. VS por for open opp window.

12			
13			

Frame counter

HDCP 1.0 : Increase by VS(CTL3).

HDCP 1.1 : In OESS mode, increase by ENC_EN

In EESS mode, increase when a. AV_MUTE = false. & b. AC = 1 or ENC_EN = 1.

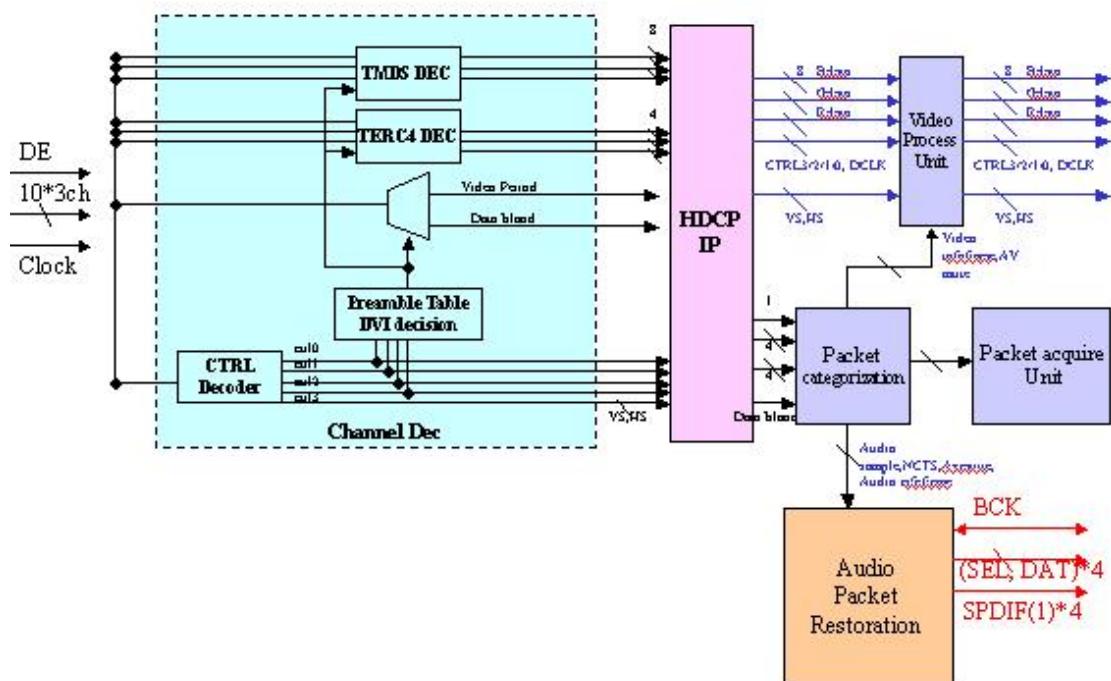
NOTE :

1. HDCP output must be always enable for DVI/HDMI.
2. The sub-descriptions i of Ri & j of Pj are the same.

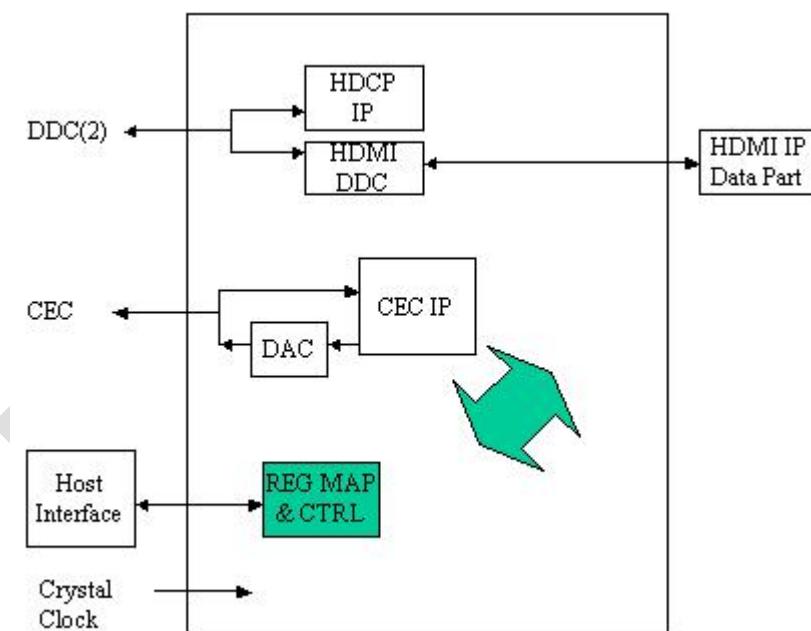


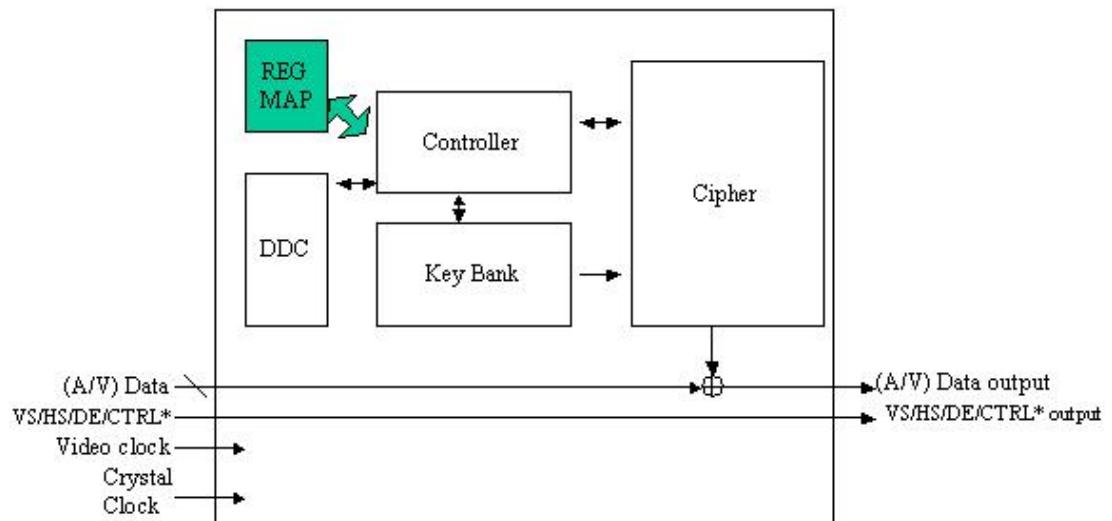
DVI Video Part (Page 2)

HDMI IP Data Part



HDMI IP Control Part



**HDCP IP**

Register:: HDMI_AP_C 0xC8				
Name	Bits	R/W	Reset State	Comments
Reserved	7:1	R/W	0	Reserved to 0
AAIF (reg_lreg_i nc_en)	0	R/W	0	(greg) Address auto increase function 0: If read/write “HDMI data port” continuously without assign “HDMI address port”, address would be not added by one automatically. 1: If read/write “HDMI data port” continuously without assign “HDMI address port”, address would be added by one automatically.

Register:: HDMI_AP 0xC9				
Name	Bits	R/W	Reset State	Comments
AP (reg_lreg_a dr)	7:0	R/W	0	(greg) Address port for HDMI

Register:: HDMI_DP 0xCA				
Name	Bits	R/W	Reset State	Comments
DP	7:0	R/W	0	(greg) Data port for HDMI

HDMI Register in Address Data Port

Access	Name	Description



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Addr.		
0x00	HDMI_SCR	System Control
0x01	HDMI_N_VAL	N times of Condition A
0x02	HDMI_BCHCR	BCH Control Bits
0x03	HDMI_AFCR	Audio Flow Control
0x04	HDMI_AFSR	Audio FIFO Status
0x05	HDMI_MAGCR	Manual Audio Gain Coefficient
0x06	HDMI_AAGCR	Auto Audio Gain Control
0x10	HDMI_CMCR	Clock MUX Control
0x11	HDMI_MCAPR	M Code of Audio PLL
0x12	HDMI_SCAPR	S Code of Audio PLL
0x13	HDMI_DCAPR0	MSB of D Code of Audio PLL
0x14	HDMI_DCAPR1	LSB of D Code of Audio PLL
0x15	HDMI_PSCR	Phase Swallow Control
0x16	HDMI_FDDR	FIFO Depth at DE Rising
0x17	HDMI_FDDF	FIFO Depth at DE Falling
0x18	HDMI_MFDDR	Maximum FIFO Depth at DE Rising
0x19	HDMI_MFDDF	Minimum FIFO Depth at DE Falling
0x1A	HDMI_FTR	FIFO Trend Register
0x1B	HDMI_FBR	FIFO Boundary Register
0x1C	HDMI_ICPSNCR0	I Code of Phase Swallow and N/CTS Register 0
0x1D	HDMI_ICPSNCR1	I Code of Phase Swallow and N/CTS Register 1
0x1E	HDMI_PCPSNCR0	P Code of Phase Swallow and N/CTS Register 0
0x1F	HDMI_PCPSNCR1	P Code of Phase Swallow and N/CTS Register 1
0x20	HDMI_ICTPSR0	I Code of Trend for Phase Swallow Register 0
0x21	HDMI_ICTPSR1	I Code of Trend for Phase Swallow Register 1
0x22	HDMI_PCTPSR0	P Code of Trend for Phase Swallow Register 0
0x23	HDMI_PCTPSR1	P Code of Trend for Phase Swallow Register 1
0x24	HDMI_ICBPSR0	I Code of Boundary for Phase Swallow Register 0
0x25	HDMI_ICBPSR1	I Code of Boundary for Phase Swallow Register 1
0x26	HDMI_PCBPSR0	P Code of Boundary for Phase Swallow Register 0
0x27	HDMI_PCBPSR1	P Code of Boundary for Phase Swallow Register 1
0x28	HDMI_NTx1024TR0	Number of Tx in 1024 Tv Register 0



0x29	HDMI_PCBPSR1	Number of Tx in 1024 Tv Register 1
0x2A	HDMI_STBPR	Stop Time for Boundary PE Register
0x2B	HDMI_NCPER	N and CTS Phase Error Register
0x2C	HDMI_PETR	Phase Error Threshold Register
0x2D	HDMI_AAPNR	Action for Audio PLL Non-Lock Register
0x2E	HDMI_APDMCR	Audio PLL Debug Mode Control Register
0x30	HDMI_AVMCR	Audio and Video Mute Control Register
0x31	HDMI_WDCR0	Watch Dog Control Register 0
0x32	HDMI_WDCR1	Watch Dog Control Register 1
0x33	HDMI_WDCR1	Watch Dog Control Register 2
0x34	HDMI_DBCR	HDMI Double Buffer Control Register
0x35	HDMI_APTMCR0	Audio PLL Test Mode Control Register 0
0x36	HDMI_APTMCR1	Audio PLL Test Mode Control Register 1
0x38	HDMI_DPCR0	DPLL Control Register 0
0x39	HDMI_DPCR1	DPLL Control Register 1
0x3A	HDMI_DPCR2	DPLL Control Register 2
0x3B	HDMI_DPCR3	DPLL Control Register 3
0x40	HDMI_AWDSR	Audio Watch Dog Status Register
0x41	HDMI_VWDSR	Video Watch Dog Status Register
0x42	HDMI_PAMICR	Packet Acquire Mechanism Interrupt Control Register
0x43	HDMI_PTRSV1	Packet Type of RSV1 Packet
0x44	HDMI_PTRSV2	Packet Type of RSV2 Packet
0x45	HDMI_PVGCR0	Packet Variation Global Control Register 0
0x46	HDMI_PVGCR1	Packet Variation Global Control Register 1
0x47	HDMI_PVGCR2	Packet Variation Global Control Register 2
0x48	HDMI_PVSR0	Packet Variation Status Register 0
0x49	HDMI_PVSR1	Packet Variation Status Register 1
0x4A	HDMI_PVSR2	Packet Variation Status Register 2
0x50	HDMI_VCR	Video Control Register
0x51	HDMI_ACRCR	ACR Control Register
0x52	HDMI_ACRSR0	ACR Status Register 0
0x53	HDMI_ACRSR1	ACR Status Register 1
0x54	HDMI_ACRSR2	ACR Status Register 2



0x55	HDMI_ACRSR3	ACR Status Register 3
0x56	HDMI_ACRSR4	ACR Status Register 4
0x57	HDMI_ACS0	Audio Channel Status 0
0x58	HDMI_ACS1	Audio Channel Status 1
0x59	HDMI_ACS2	Audio Channel Status 2
0x5A	HDMI_ACS3	Audio Channel Status 3
0x5B	HDMI_ACS4	Audio Channel Status 4
0x60	HDMI_INTCR	HDMI Interrupt Control Register
0x61	HDMI_ALCR	Audio Layout Control Register
0x62	HDMI_AOCR	Audio Output Control Register
0x70	HDMI_BCSR	HDMI Basic Coding Status Register
0x71	HDMI_ASR0	Audio Status Register 0
0x72	HDMI_ASR1	Audio Status Register 1

Register:: HDMI_SR					0xCB
Name	Bits	R/W	Reset State	Comments	
AVMUTE_BG	7	R	0	(packet_class → greg) AV_MUTE Flag under Background (write 1 clear) 1: Means HW receive Set_AVMUTE flag of General Control packet	
AVMUTE	6	R	0	(packet_class → greg) AV_MUTE flag of General Control Packet 0: If HW receive Clear_AVMUTE flag of General Control Packet ,this bit shall assign to 0 until HW receive Set_AVMUTE 1: If HW receive Set_AVMUTE flag of General Control Packet ,this bit shall assign to 1 until HW receive Clear_AVMUTE Note : If HW never receives “General Control Packet”, this bit shall set to 0. If HW receive “General Control Packet” with Clear_AVMUTE flag = 0 & Set_AVMUTE flag = 0, this bit shall keep previous value. If HW receive “General Control Packet” with Clear_AVMUTE flag = 1 & Set_AVMUTE flag = 1, this bit shall keep previous value, but set “General Control Packet error flag”.	
VIC(chg_info_avi_vic_ke ep)	5	R	0	(packet_class → greg) If VIC(In AVI Infoframe) is different with pervious value ,this bit would be assigned to 1 until clear this bit. (write 1 clear for each bit)	
Reserved	4:1	R	0	Reserved	
MODE(hdmi_md)	0	R	0	(chanel_dec → greg) HDMI/DVI mode detected by auto function, even in manual mode, this	



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auto)				bit could indicate decision of auto function. 0: DVI 1: HDMI
-------	--	--	--	---

FW should read “PLL status” after 0.66ms~3 ms from FW clear this bit.

Register::: HDMI GPVS 0xCC				
Name	Bits	R/W	Reset State	Comments
NPS (new_pck_ null_ocr_k eep)	7	R	0	(packet_class → greg) Null Packet Status
PIS 6: new_pck_r sv1_ocr_ke ep 5: new_pck_r sv0_ocr_ke ep	6:5	R	0	(packet_class → greg) Packet Input Status 6: RSV1 received 5: RSV0 received
PVS	4:0	R	0	(lreg → greg) Packet Variation Status 0: AVI infoframe 1: Audio infoframe 2: ACP 3: ISRC1 4: MPEG infoframe

Note. Write 1 Clear

“Packet variation status”:

1. “Packet variation status” means packet content variation, bit4 ~ bit 0 corresponds to AVI info-frame, audio info-frame, ACP, ISRC1, and MPEG info-frame respectively.
2. Before FW process the corresponding action item, FW should clear the corresponding bit of “Global Packet variation status”.
3. Then FW read the content of the corresponding packet, polling “Global Packet variation status”, check if corresponding bit of “Global Packet variation status” is 0, and execute follow-up action item if this bit is 0.
4. Jump to step 2 if this bit is 1.
5. The variation result appears in “Global Packet variation status” after the corresponding packet finish transmitting.

“Packet input status”:

1. “Packet input status” represents updated status of RSV1, RSV0 respectively. If it is updated, “Packet input status” is assigned to 1 until F/W clear this bit.
2. “Null Packet status” :When receive null packet, “Null Packet status” is assigned to 1until F/W clear this bit
3. If one bit of “Packet variation status” is cleared, the corresponding bit of “local variation flag for detail info” is also cleared.

Register::: HDMI PSAP 0xCD				
Name	Bits	R/W	Reset State	Comments
APSS	7:0	R/W	0	Address for Packet Storage SRAM

Register::: HDMI PSDP 0xCE				
Name	Bits	R/W	Reset State	Comments
DPSS	7:0	R	0	Data Port for Packet Storage SRAM

BCH is stored in the 1st address of each packet type, its content is stated as following;

Bit0: 2-bit error for bch header (0: 2-bit error doesn't occur; 1: 2-bit error occurs)

Bit1: 2-bit error for bch block 0 (0: 2-bit error doesn't occur; 1: 2-bit error occurs)

Bit2: 2-bit error for bch block 1 (0: 2-bit error doesn't occur; 1: 2-bit error occurs)

Bit3: 2-bit error for bch block 2 (0: 2-bit error doesn't occur; 1: 2-bit error occurs)



Bit4: 2-bit error for bch block 3 (0: 2-bit error doesn't occur; 1: 2-bit error occurs)
 Bit5: checksum result (0: checksum error doesn't occur; 1: checksum error occurs)

Packet Type and Address

Packet type	Variation status	Storage (byte) (+ means BCH)	Address needed (8 bits/add)	Address
AVI info	9+1(global)	16+	17	0~16
Audio info	4+1	8+	9	17~25
ACP	3+1	4+	5	26~30
ISRC1	1+1	18+	19	31~49
ISRC2	X	18+	19	50~68
MPEG info	3+1	8+	9	69~77
RSV0	1, only global	30+	31	78~108
RSV1	1, only global	30+	31	109~139

Table 2 Packet Type and Address SRAM map Table

Following register is assigned by “HDMI-address port”, “HDMI-data port”

Register:: HDMI_SCR 0x00				
Name	Bits	R/W	Reset State	Comments
Reserved	7:5	--	0	Reserved to 0
REG_PACK ET_IGNORE (reg_apll_pd)	4	R/W	1 0	(lreg → channel_dec) HDMI/DVI Mode Detection Method Selection 0: Detect by both Video and Data Island Guard Band. 1: Detect by only Video Guard Band.
MODE (reg_md_sel_ctrl)	3	R/W	0	(lreg → channel_dec) HDMI/DVI switch mode 0: Auto detect flow is as fig.1 1: Manual, determined by bit[2]
MSMODE (reg_md_sel)	2	R/W	0	(lreg → channel_dec) When manual mode, select HDMI or DVI 0: DVI 1: HDMI
CABS (reg_md_sel_cond)	1	R/W	0	(lreg → channel_dec) DVI/HDMI condition A, B select 0: condition A: Detect data island preamble + data island guard band (appear count is decided by “N”) condition B: Detect if data island preamble + data island guard band appear in continuous 30 or 2 frames(decide by bit 0) 1: condition A: Detect data island preamble + data island guard band & video preamble + video guard band(appear count is decided by “N”) condition B: Detect if data island preamble + data island guard band & video preamble + video guard band appear in continuous 30 or 2



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				frames(decide by bit 0)
FCDDIP (reg_cond_b_time)	0	R/W	0	(lreg → channel_dec) Frame count to detect data island packet (Condition B) 0: 2 frames 1: 30 frames

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1. HDMI/DVI auto switch mode , the information must be passed to HDCP :

DVI/HDMI decision flow is shown as below.

DVI/ HDMI decide flow

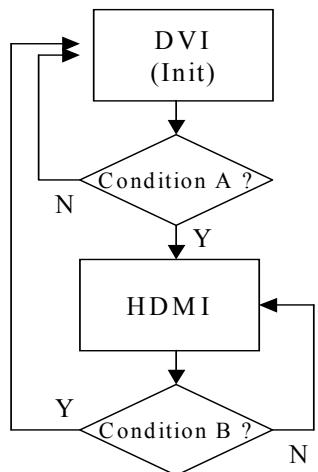


Fig 1

2. Power Saving for HDMI/HDCP :

In Power saving mode, TMDS channel Green/Red are always turn off. HDMI is power down.

There are only TMDS clock input frequency detect and channel blue DE decoder working.

The channel blue DE decoder is active after clock frequency is OK.

Register:: HDMI_N_VAL 0x01				
Name	Bits	R/W	Reset State	Comments
NVAL (reg_cond_a_time)	7:0	R/W	1	(lreg → channel_dec) Condition A counter N: 00 : X 01 : 1 FF : 255 N = 1 ~ 255 , N can't be assigned to 0x00

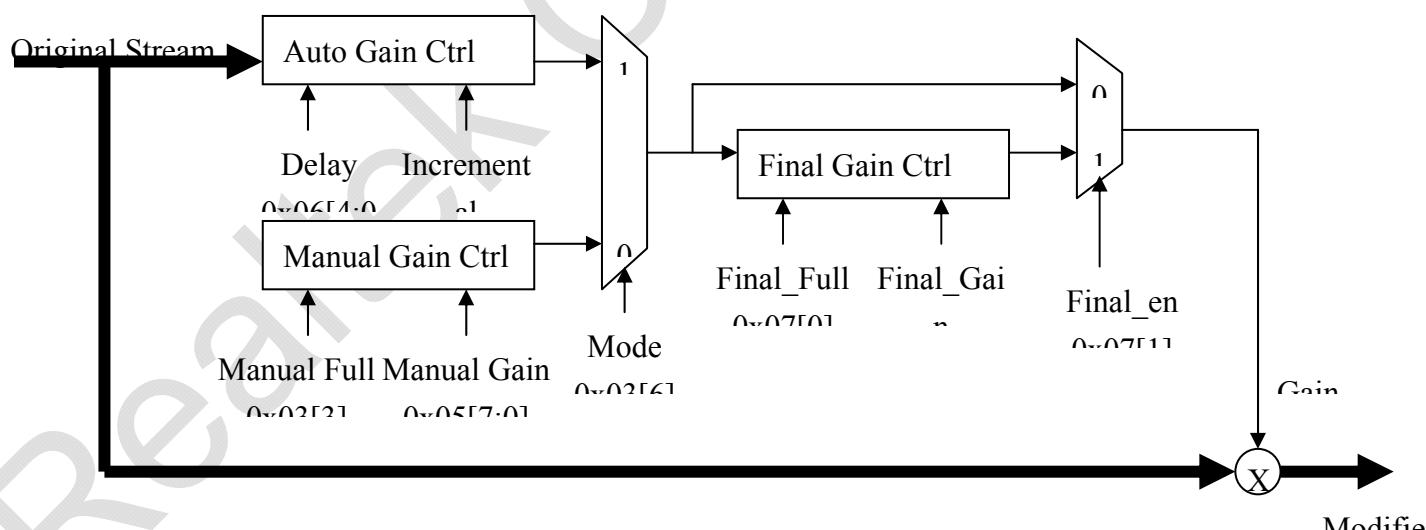
Register:: HDMI_BCHCR 0x02				
Name	Bits	R/W	Reset State	Comments
Reserved	7	---	0	Reserved to 0
BCH_FLA_G_CLR_DVI	6	R/W	0	In DVI mode, clear BCH error flag (0x02[2:1]) 0: keep old method (write 0 to clear) 1: auto clear BCH flag
Reserved	5:4	---	---	Reserved
BCHE (reg_bch_en)	3	R/W	1	(lreg → bch) BCH function enable 1: Enable BCH function



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				0: Disable BCH function, bit[2:1] are always 2'b00.
BCHES (bch_err1_flag)	2	R	0	<p>(bch → lreg) BCH function's result, one bit error. It is set by this case, and cleared by write 0.</p> <p>This bit is the result of ORing 5 bits BCH 1 bit error. 1: One bit error occurs. 0: No error occurs Note: If BCH detect 1-bit error, this bit would be assigned to 1 until clear this bit</p>
BCHES2 (bch_err2_flag)	1	R	0	<p>(bch → lreg) BCH function's result, two bits error. It is set by this case, and cleared by write 0.</p> <p>This bit is the result of ORing 5 bits BCH 1 bit error. 1: 2-bit error occurs 0: 2-bit error don't occurs If BCH detect 2-bit error, this bit would be assigned to 1 until clear this bit</p>
PE (reg_err2_proc)	0	R/W	0	<p>(lreg → packet_class) The processing for Packet with two or more BCH error (not include Audio packet)</p> <p>1: Block Info frame message 0: As correct frame, decided by F/W NOTE! Audio samples always go to FIFO</p>





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Register:: HDMI_NTx1024TR0 0x28				
Name	Bits	R/W	Reset State	Comments
Reserved	7:5	---	0	Reserved to 0
Reserved	4	---	0	Reserved to 0
RM (reg_x_me as_v_en)	3	R/W	0	(ackg_regmap) Restart measure. Measure the length of 1024 Tv by crystal. The result is readable from the following bits. 1: enable measure. Writing 1 would clear the answer. This bit would be auto cleared after measure done. 0: indicating measure is done.
NT (reg_result _xv_mmm)	2:0	R	0	(ackg_regmap) Number of Tx for 1024 Tv [10:8], (How many Tx = 1024 * Tv)

Register:: HDMI_NTx1024TR1 0x29				
Name	Bits	R/W	Reset State	Comments
NT (reg_result _xv)	7:0	R	0	(ackg_regmap) Number of Tx for 1024 Tv [7:0], (How many Tx = 1024 * Tv)



Register:: HDMI AVMCR 0x30				
Name	Bits	R/W	Reset State	Comments
AVMUTE_WIN_EN (reg_avmute_win_en)	7	R/W	0	(lreg → packet_class) Avmute Window Enable (AVMute tune up/down) 1: Enable 0: Disable If this bit is enabled, avmute signal will be blocked when in the invalid region. The valid region depends on the setting of register 0xA8
Reserved	6:4	---	---	Reserved
VE (reg_video_en)	3	R/W	0	(lreg → video_fsm → video_ckgen) Video clock output Enable (the control signal of GCK cell) 1: Enable video clock output 0: disable video clock output
Reserved	2	---	---	Reserved
VDPIC (reg_video_dis_pin_in_v)	1	R/W	0	(lreg, unuseful, 1: ~reg_video_en, 0: reg_video_en) Video Disable Pin Invert Control 0: when event (video disable) occurred, set this pin to low voltage, others maintain high. 1: when event (video disable) occurred, set this pin to high voltage, others maintain low.
NFPSS (reg_irq_pin_inv)	0	R/W	0	(lreg) IRQ Output Pin Polarity Inverse 0: no inverse, which means H : IRQ, L : no IRQ 1: inverse, which means H : no IRQ L : IRQ

Definition:

Disable Video Assign “DE pins”, “VS pin”, “HS pin”, “CTRL(4) pins”, “CLK pin”, “Data(24) pins” to zero , refer to “Global System”

Register:: HDMI WDCR0 0x31				
Name	Bits	R/W	Reset State	Comments
ASMFE (reg_wd_b_y_avmute)	7	R/W	1	(lreg) Auto SET_AVMUTE function enable (the control signal of wd_avmute) 0: If HW receives SET_AVMUTE flag, don't mute/disable audio & disable video by HW. 1: If HW receives SET_AVMUTE flag, mute/disable audio & disable video by HW. Note: If “CLEAR_AVMUTE” and “SET_AVMUTE” of the General Control Packet are all 1, keep previous A/V output state, and pull up “General Control Packet error flag”
Reserved	6	---	0	Reserved to 0
Reserved	5	---	0	Reserved to 0



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Reserved	4:0	---	---	Reserved
----------	-----	-----	-----	----------

Video watch dog for “packet acquire mechanism” is listed in Packet acquire mechanism Unit.

Register:: HDMI_WDCR1 0x32				
Name	Bits	R/W	Reset State	Comments
Reserved	7:6	---	---	Reserved
Rev (reg_video_o_wd_by_vic)	5	---	0	(Ireg) Reserved
VWDACT (reg_video_wd_by_atype)	4	R/W	0	(Ireg) Video Watch Dog For Audio Coding Type ([the enable/disable signal of video_wd_chg_atype for video wd]) 1: If coding type is different with previous type, disable video 0: If coding type is different with previous type, don't disable video
Reserved	3:0	---	---	Reserved

Register:: HDMI_WDCR2 0x33				
Name	Bits	R/W	Reset State	Comments
VWDAP (reg_video_wd_by_pll)	7	R/W	0	(Ireg) Video Watch dog enable for audio PLL [the enable/disable signal of video_wd_apll_nonlock] 1: If audio PLL is non-lock, disable video 0: If audio PLL is non-lock, don't disable video
VWDLF (reg_video_wd_by_lyo)	6	R/W	0	(Ireg) Video watch dog for layout field of audio sample packet 1: If layout field is different with previous value, disable Video. 0: If layout field is different with previous value, don't disable Video.
VWDAFO (reg_video_wd_by_ovf)	5	R/W	0	(Ireg) Video watch dog function for audio FIFO overflow. 1: If audio FIFO is overflow for “X” samples, disable Video. 0: If audio FIFO is overflow for “X” samples, don't disable Video.
VWDAFU (reg_video_wd_by_udf)	4	R/W	0	(Ireg) Video watch dog function for audio FIFO underfloww . 1: If audio FIFO is underflow for “Y” samples, disable Video. 0: If audio FIFO is overflow for “Y” samples, don't disable Video
Reserved	3:0	R/W	---	Reserved

Register:: HDMI_DBCR 0x34				
Name	Bits	R/W	Reset State	Comments
COLOR_D EBUG_SE L_1 (reg_color_dbg_sel)	7:4	R/W	0	Bit[7:6] Color Debug Selection For Sampling Clock rate 00: 1X sampling clock rate 01: 2X sampling clock rate 10: 4X sampling clock rate 11: 1X sampling clock rate Bit[5:4] Color Debug Selection For Sampling Data Channel 00: Red data channel 01: Green data channel 10: Blue data channel 11: Red data channel



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Reserved	3:0	---	---	Reserved
----------	-----	-----	-----	----------

In test mode, PLL shift its phase by 16 steps periodically. The steps which are performed in 1st phase each 16 steps could be assigned by “Number of 1st phase shift step”, remaining steps are performed in 2nd phase.

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Packet Acquire Mechanism

Register:: HDMI_AWDSR 0x40				
Name	Bits	R/W	Reset State	Comments
Reserved	7:5	---	0	Reserved to 0
AWDPVSB (reg_audio_wd_var)	4:0	R/W	0	(lreg) Audio watch dog for Packet variation status bit (enable/disable), including: chg_pck_info_avi_ocr chg_pck_info_aud_ocr chg_pck_acp_ocr chg_pck_isrc1_ocr chg_pck_info_mpg_ocr

If a bit is assigned to 1 and the corresponding bit of “Global Packet variation status” is 1, audio output will be disabled/muted.

Register:: HDMI_VWDSR 0x41				
Name	Bits	R/W	Reset State	Comments
Reserved	7:5	---	0	Reserved to 0
VWDPVSB (reg_video_wd_var)	4:0	R/W	0	(lreg) Video watch dog for Packet variation status bit (enable/disable), including: chg_pck_info_avi_ocr chg_pck_info_aud_ocr chg_pck_acp_ocr chg_pck_isrc1_ocr chg_pck_info_mpg_ocr

If a bit is assigned to 1 and the corresponding bit of “Global Packet variation status” is 1, video output will be disabled.

Register:: HDMI_PAMICR 0x42				
Name	Bits	R/W	Reset State	Comments
Reserved	7:5	---	0	Reserved to 0
ICPVSB (reg_irq_packet_var)	4:0	R/W	0	(lreg) IRQ control for Packet variation status bit (enable/disable), including: chg_pck_info_avi_ocr chg_pck_info_aud_ocr chg_pck_acp_ocr chg_pck_isrc1_ocr chg_pck_info_mpg_ocr

If a bit is assigned to 1 and the corresponding bit of “Global Packet variation status” is 1, issue IRQ signal.

Note: The corresponding bit of “Global Packet variation status” means bit0 maps to bit 0 of “Global Packet variation status ,bit1” maps to bit 1 of “Global Packet variation status”,...etc.

Register:: HDMI_PTRSV1 0x43				
Name	Bits	R/W	Reset State	Comments
PT (reg_packet_port0)	7:0	R/W	0	(lreg → packet_class) Packet Type of RSV1 packet



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Register:: HDMI_PTRSV2 0x44				
Name	Bits	R/W	Reset State	Comments
PT (reg_packet_p ort1)	7:0	R/W	0	(lreg → packet_class) Packet Type of RSV2 packet

Register:: HDMI_PVGCR0 0x45				
Name	Bits	R/W	Reset State	Comments
PVSEF (reg_packet_v ar_en[7:0])	7:0	R/W	FF	(lreg) Bit7 ~ Bit0 of packet variation status enable flag

Register:: HDMI_PVGCR1 0x46				
Name	Bits	R/W	Reset State	Comments
PVSEF (reg_packet_v ar_en[15:8])	7:0	R/W	FF	(lreg) Bit15 ~ Bit8 of packet variation status enable flag

Register:: HDMI_PVGCR2 0x47				
Name	Bits	R/W	Reset State	Comments
Reserved	7:4	---	0	Reserved
PVSEF (reg_packet_v ar_en[19:16])	3:0	R/W	F	(lreg) Bit19 ~ Bit16 of packet variation status enable flag

When the bits of enable “Packet Variation Global Control Register” are set, the corresponding “Packet Variation Status Register” bits will OR to “Packet Variation Global Control Register”.

Note: 0x45 ~ 0x47 are the enable/disable control of each packet variation status, packet variation status consists of chg_pck_info_avi_ocr, chg_pck_info_aud_ocr, chg_pck_acp_ocr, chg_pck_isrc1_ocr and chg_pck_info_mpg_ocr.

Register:: HDMI_PVSR0 0x48				
Name	Bits	R/W	Reset State	Comments
PVS	7:0	R	0	(packet_class → lreg) Bit7 ~ Bit0 of packet variation status

Register:: HDMI_PVSR1 0x49				
Name	Bits	R/W	Reset State	Comments
PVS	7:0	R	0	(packet_class → lreg) Bit15 ~ Bit8 of packet variation status

Register:: HDMI_PVSR2 0x4A				
Name	Bits	R/W	Reset State	Comments
Reserved	7:4	---	0	Reserved
PVS	3:0	R	0	(packet_class → lreg) Bit19 ~ Bit16 of packet variation status

There are 20 bits “Enable flags to global Packet variation”. Each bit is set to watching a standard type of received packet content, and checking if it changed from the previous received packet.

If received packet content changed from previous received one, the relative bit in “local variation flag for detail



info.” register will be set, and it will trigger the “global packet variation status” set. The following table presents the detail of “local variation flag for detail info.”

InfoFrame	Bit	Description
AVI	0	Y0Y1change
	1	A0,R0,R1,R2,R3 change
	2	S0,S1 any bit change
	3	C0,C1 change
	4	M0,M1 change
	5	VIC0 ~ VIC6 change
	6	PR0 ~ PR6 change
	7	SC1,SC0 change
	8	B0,B1,Top bar, bottom bar, left bar , right bar change
Audio	9	CC0~CC3 change
	10	CA0~CA7 change
	11	LSV0~LSV3 change
	12	DM_INH any bit change
ACP	13	ACP_Type change
	14	DVD-audio_type_dependent_generation change
	15	Copy_Permission, Copy_Number,Quality,& Transaction change
ISRC1	16	ISRC_status change
MPEG	17	MB#3~MB#0 change
	18	FR0 change
	19	MF1, MF0 change

Register:: HDMI_VCR 0x50				
Name	Bits	R/W	Reset State	Comments
EOI (reg_odd_gen_inv)	7	R/W	0	(lreg → sync_autogen) EVEN/ODD Inverse 0: Normal 1: Inverse
EOT (odd_tog)	6	R	0	(sync_autogen → lreg) EVEN/ODD Toggle (write 1 clear) 0: Progressive 1: Interlace
SE (odd_err)	5	R	0	(sync_autogen → lreg) EVEN/ODD signal error (write 1 clear) 0: Normal 1: Error
RS (reg_double_buf_time)	4	R/W	0	(lreg) The reference signal for executing Info-frame automatically. 0: DEN



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				1: VSYNC
DSC (reg_down_sp_ctrl)	3:0	R/W	0	<p>(lreg) Down sample control (only valid if Video Down Sampling Auto Mode Disable, 0x51[2] = 0)</p> <p>0000: pixel down sample for 1 time(no down sample) 0001: pixel down sample for 2 times 0010: pixel down sample for 3 times 0011: pixel down sample for 4 times 0100: pixel down sample for 5 times 0101: pixel down sample for 6 times 0110: pixel down sample for 7 times 0111: pixel down sample for 8 times 1000: pixel down sample for 9 times 1001: pixel down sample for 10 times others : XXX</p>

Register:: HDMI_ACRCR 0x51				
Name	Bits	R/W	Reset State	Comments
HDIRQ (reg_cr51_b7_rsv)	7	R/W	0	<p>(lreg) HDMI/DVI change interrupt enable [the enable/disable signal of irq_chg_hdmi_md]</p> <p>0:disable 1:enable</p>
CSAM (reg_color_md_auto)	6	R/W	0	<p>(lreg) Color Space Translation</p> <p>0: Manual mode, determined by 0x51[5:4] 1: Auto mode, signal from oacket_class</p>
CSC (reg_color_md_fw)	5:4	R/W	1	<p>(lreg) Color Space Control (if CSAM=1, CSC will be read-only)</p> <p>00: RGB 01: YCrCb-422 10: YCrCb-444 11: Reserved</p>
Reserved	3	--	0	Reserved to 0
PRDSAM (reg_down_sp_ctrl_auto)	2	R/W	1	<p>(lreg) Pixel Repetition down sampling auto mode</p> <p>1: auto mode, the circuit resolve the repeat number, and enable it in next frame. The result could be read in bits for repeat number. 0: manual mode, F/W sets repeat number(0x50[3:0]), the number is set in bits for repeat number.</p>
PUCNR (reg_cts_n_pup)	1	R/W	0	<p>(lreg → packet_class) Pop up CTS&N result (read value is always tied to 0)</p> <p>0: No pop up 1: Pop up result (Pop up CTS & N which is acquired completely. If present N & CTS is acquiring, pop up previous complete N & CTS) If the info is updating, HW will refuse this command.</p>
Reserved	0	---	---	Reserved

Register:: HDMI_ACRSR0 0x52				
Name	Bits	R/W	Reset State	Comments
CTS (clkg_cts_to)	7:0	R	0	<p>(packet_class → lreg) CTS in usage, CTS[19:12]</p>



fw[19:12])				
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Register:: HDMI_ACRSR1 0x53				
Name	Bits	R/W	Reset State	Comments
CTS (clkg_cts_to_fw[11:4])	7:0	R	0	(packet → Ireg) CTS in usage, CTS[11:4]

Register:: HDMI_ACRSR2 0x54				
Name	Bits	R/W	Reset State	Comments
CTS (clkg_cts_to_fw[3:0])	7:4	R	0	(packet → Ireg) CTS in usage, CTS[3:0]
N (clkg_n_to_fw[19:16])	3:0	R	0	(packet → Ireg) N in usage, N[19:16]

Register:: HDMI_ACRSR3 0x55				
Name	Bits	R/W	Reset State	Comments
N (clkg_n_to_fw[15:8])	7:0	R	0	(packet → Ireg) N in usage, N[15:8]

Register:: HDMI_ACRSR4 0x56				
Name	Bits	R/W	Reset State	Comments
N (clkg_n_to_fw[7:0])	7:0	R	0	(packet → Ireg) N in usage, N[7:0]

Register:: HDMI_INTCR 0x60				
Name	Bits	R/W	Reset State	Comments
PENDING (irq_fw_keep)	7	R	0	(Ireg) When IRQ occurred, this bit would be assigned to 1 by HW, and IRQ would be pended until FW clear this bit.(write 1 clear)
AVMUTE (reg_irq_by_avmute)	6	R/W	0	(Ireg) If get General control packet and the corresponding Set_AVMUTE flag & Clear_AVMUTE flag is different with previous values [the enable/disable signal of irq_chg_avmute] 0: IRQ don't occur. 1: IRQ occur.
Reserved	5:1	--	--	Reserved
VC (reg_irq_by_no sig)	0	R/W	0	(freqdet → Ireg) (the enable/disable signal of no_vclk_in) 0: If video clock is higher than 165Mhz or lower than 25Mhz (refer to NL)(no vclk in), IRQ doesn't occur. 1: If video clock is higher than 165Mhz or lower than 25Mhz (refer to NL)(no vclk in), IRQ occurs.



Register:: HDMI_BCSR 0x70				
Name	Bits	R/W	Reset State	Comments
Reserved	7:6	---	0	Reserved to 0
NVLGB (no_vgb_aft_vpre_keep)	5	R	0	(channel_dec → Ireg) Video No Leading Guard Band If no leading GB after video preamble (It is only triggered in HDMI mode), this bit would be assigned to 1 until clear this bit Write 1 to clear.
NALGB (no_agb_aft_apre_keep)	4	R	0	(channel_dec → Ireg) Audio No Leading Guard Band If no leading GB after audio preamble (It is only triggered in HDMI mode), this bit would be assigned to 1 until clear this bit Write 1 to clear.
NATGB (no_trailing_a_gb_keep)	3	R	0	(channel_dec → Ireg) Audio No Trailing Guard Band If audio packets without trailing GB, this bit would be assigned to 1 until clear this bit. Write 1 to clear.
NGB (no_gb_rgb_sync_keep)	2	R	0	(channel_dec → Ireg) No Guard Band If any type of GB is not synchronous in 3 channels(audio is only 2 channel), this bit would be assigned to 1 until clear this bit. Write 1 to clear.
PE (no_packet_length_32n_keep)	1	R	0	(packet_class → Ireg) Packet Error If size of Data Island Packet is not times of 32, this bit would be assigned to 1 until clear this bit. Write 1 to clear.
GCP (err_set_cln_avmute_keep)	0	R	0	(packet_class → Ireg) General Control Packet error flag: If HW receive General Control Packet with Clear_AVMUTE=1 & Set_AVMUTE=1 ,assign this bit to 1 until clear this bit Write 1 to clear.

Register:: HDMI_ASRO 0x71				
Name	Bits	R/W	Reset State	Comments
Reserved	7:3	---	0	Reserved to 0
FsRE (cts_n_are_0_keep)	2	R	0	(packet_class → Ireg) Fs Regeneration Error If CTS & N received 0, this bit would be assigned to 1 until clear this bit Write 1 to clear.
FsIF (fa_from_info_ready_keep)	1	R	0	(packet_class → Ireg) Fs from InfoFrame If audio frequency from InfoFrame ready, this bit would be assigned to 1 until clear this bit Write 1 to clear.
Reserved	0	---	---	Reserved

Register:: HDMI_ASRI 0x72				
---------------------------	--	--	--	--



Name	Bits	R/W	Reset State	Comments
Reserved (reg_cr72_b7_rsv)	7	---	0	Reserved
FBIF (fa_from_info)	6:4	R	0	<p>(packet_class → lreg)</p> <p>Frequency bits from info frame</p> <p>000: refer to channel status bits</p> <p>001: 32k</p> <p>010: 44.1k</p> <p>011: 48k</p> <p>100: 88.2k</p> <p>101: 96k</p> <p>110: 176.4k</p> <p>111: 192k</p>
Reserved	3:0	---	---	Reserved

-TMDS Decoding Error Detection

To check whether data enable is correct or not.

Register:: TMDS DET_0					0x84
Name	Bits	R/W	Reset State	Comments	
Reserved	7	---		Reserved	
DE_SEL	6	R/W	0	<p>Source of DE Selection</p> <p>0: Choose DE from Post Stage</p> <p>1: Choose DE from Pre-Stage</p>	
POS_DE_LOWBD	5:0	R/W	36	<p>DE =1 Low Bound Setting</p> <p>Setting Positive DE Period Low Bound Value</p> <p>0~63</p>	

Register:: TMDS DET_1					0x85
Name	Bits	R/W	Reset State	Comments	
NEG_DE_LOWBD	7:1	R/W	12	<p>DE =0 Low Bound Setting</p> <p>Setting Negative DE Period Low Bound Value</p> <p>0~127</p>	
RED_TRA_N_ERR_FLAG	0	R	0	<p>RED Channel Transition Error Flag (write 1 clear)</p> <p>0: Means No Transition Error Occurs at Red Channel</p> <p>1: Means Transition Error occurs</p>	

Register:: TMDS DET_2					0x86
Name	Bits	R/W	Reset State	Comments	
GRN_TRA_N_ERR_FLAG	7	R	0	<p>Green Channel Transition Error Flag (write 1 clear)</p> <p>0: Means No Transition Error Occurs at Green Channel</p> <p>1: Means Transition Error occurs</p>	



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BLU_TRA_N_ERR_FLAG	6	R	0	Blue Channel Transition Error Flag (write 1 clear) 0: Means No Transition Error Occurs at Blue Channel 1: Means Transition Error occurs
RED_POS_DE_ERR_FLAG	5	R	0	Red Channel Positive DE Period Measurement Flag (write 1 clear) 0: Means DE Period is Valid under Red Channel 1: Means DE Period is Invalid under Red Channel
GRN_POS_DE_ERR_FLAG	4	R	0	Green Channel Positive DE Period Measurement Flag (write 1 clear) 0: Means DE Period is Valid under Green Channel 1: Means DE Period is Invalid under Green Channel
BLU_POS_DE_ERR_FLAG	3	R	0	Blue Channel Positive DE Period Measurement Flag (write 1 clear) 0: Means DE Period is Valid under Blue Channel 1: Means DE Period is Invalid under Blue Channel
RED_NEG_DE_ERR_FLAG	2	R	0	Red Channel Negative DE Period Measurement Flag (write 1 clear) 0: Means DE Period is Valid under Red Channel 1: Means DE Period is Invalid under Red Channel
GRN_NEG_DE_ERR_FLAG	1	R	0	Green Channel Negative DE Period Measurement Flag (write 1 clear) 0: Means DE Period is Valid under Green Channel 1: Means DE Period is Invalid under Green Channel
BLU_NEG_DE_ERR_FLAG	0	R	0	Blue Channel Negative DE Period Measurement Flag (write 1 clear) 0: Means DE Period is Valid under Blue Channel 1: Means DE Period is Invalid under Blue Channel

Register::: TMDS DET_3					0x87
Name	Bits	R/W	Reset State	Comments	
TRAN_ER_R_THRD	7:4	R/W	0	Transition Error Count Threshold Value Setting 0~15	
POS_DE_ERR_THRD	3:0	R/W	0	Positive DE Error Count Threshold Value Setting 0~15	

Register::: TMDS DET_4					0x88
Name	Bits	R/W	Reset State	Comments	
Rev	7:4	---		Reserved	
NEG_DE_ERR_THRD	3:0	R/W	0	Negative DE Error Count Threshold Value Setting 0~15	



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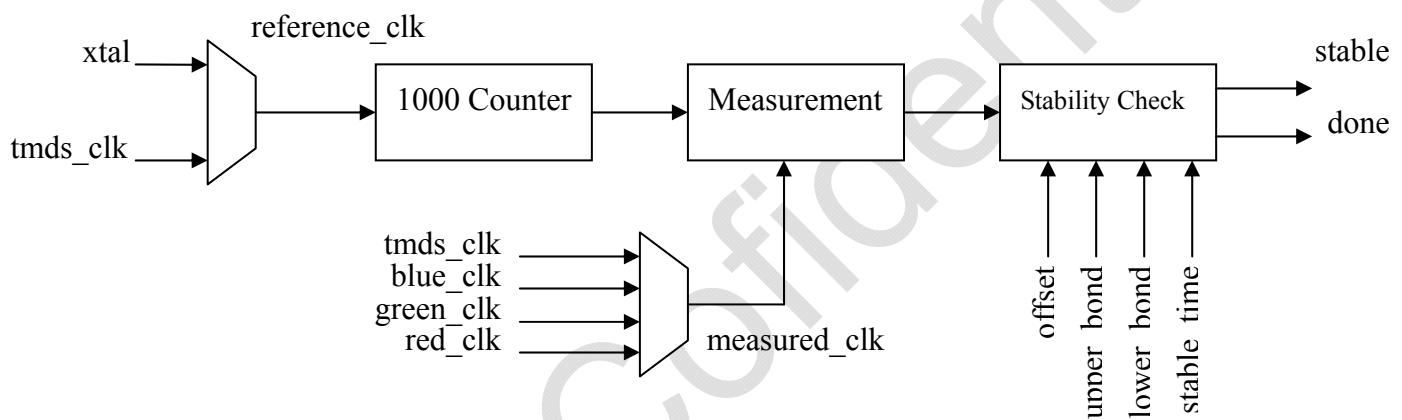
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Power-Saving Mode Domain Input Video clock frequency detection

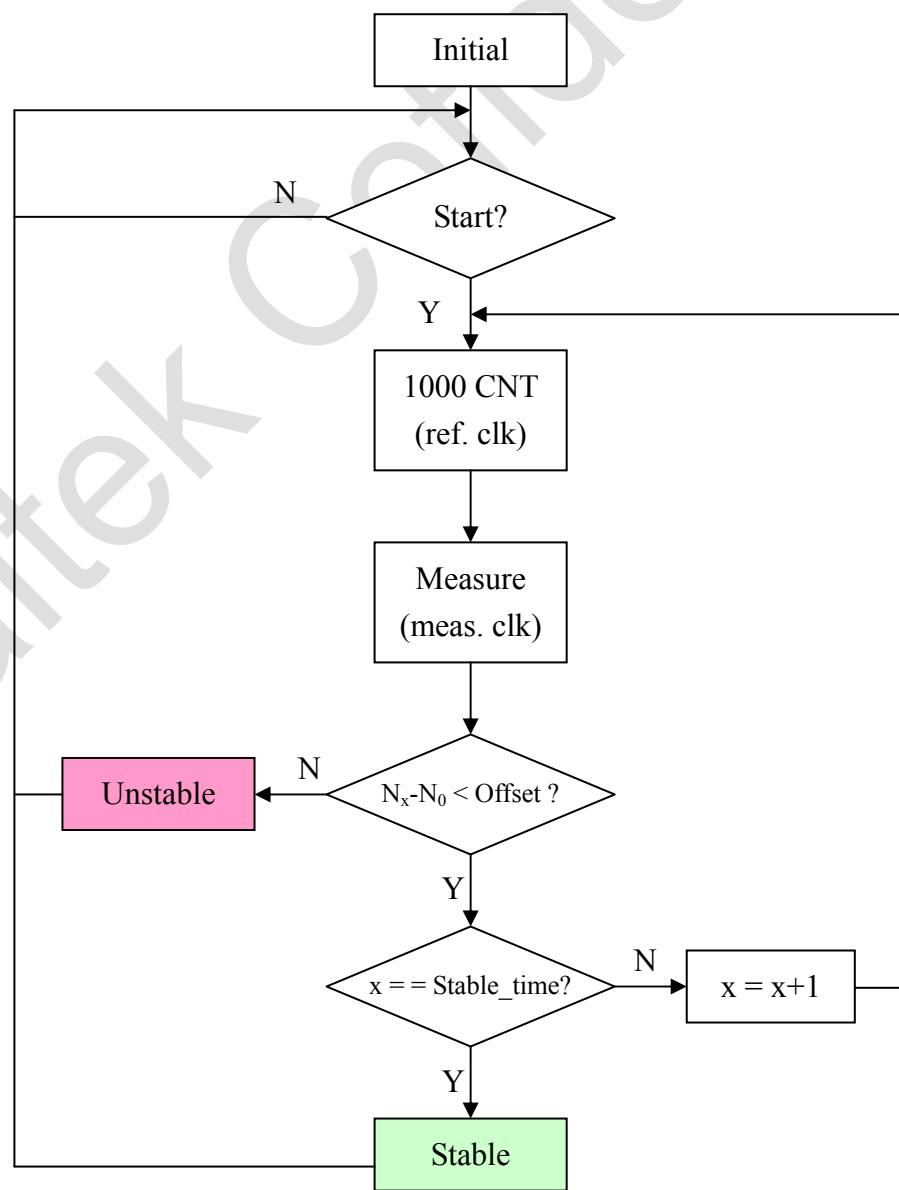
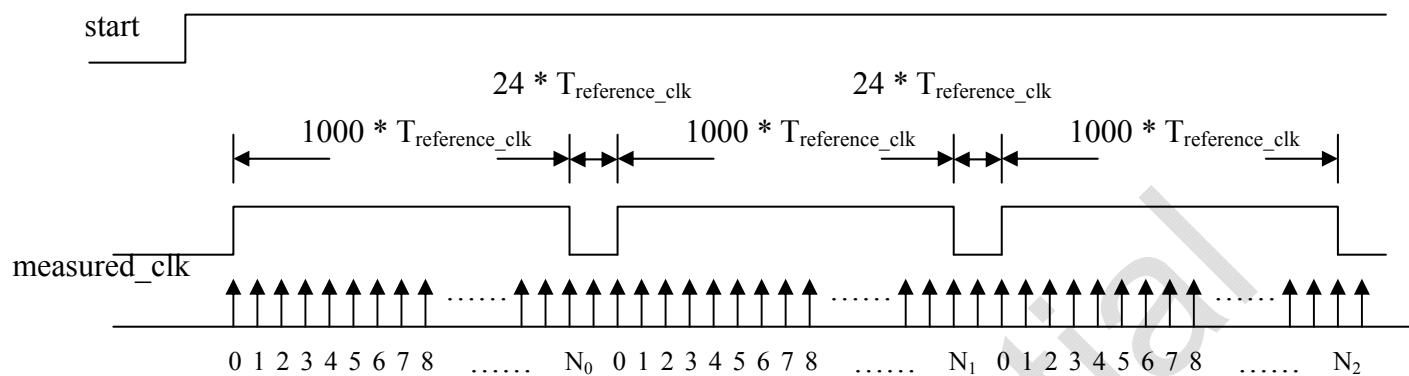
Frequency detection formula: $1000 \times T_{ref_clk} = counter \times T_{measure_clk}$





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Register:: HDMI_FREQDET_CTRL					0xE6
Name	Bit	R/W	Default	Description	Config
FREQDET_START	7	R/W	0	Start the frequency detection process. Once the bit has been set, this process won't stop until disabling this bit. 0: Disabled 1: Started	
FREQDET_DONE	6	R	0	The first frequency detection process has done. 0: Not done yet. 1: Done.	
FREQ_SOURCE	5:4	R/W	0	Choose which clock to be measured. 00: TMDS clock. 01: Blue channel clock. 10: Green channel clock. 11: Red channel clock.	
FREQ_REFERENCE	3	R/W	0	Choose which clock as reference clock. 0: Xtal clock. (14.318~27MHz are preferred) 1: TMDS clock.	
FREQ_UNSTABLE	2	R	0	The freq status has been unstable. (Write 1 to clear) 0: Disabled 1: Enabled	
IRQ_FREQ_UNSTABLE	1	R/W	0	Interrupt as long as the freq is unstable. 0: Disabled 1: Enabled	
VWD_FREQ_UNSTABLE	0	R/W	0	Trigger video watch-dog as long as the freq is unstable. 0: Disabled 1: Enabled	Wport Rport

Register:: HDMI_FREQDET_OFFSET					0xE7
Name	Bit	R/W	Default	Description	Config
CP_MEAS_CLK_SEL	7	R/W	0	The selection of measure clk 0: meas_clk from 0xE6[5:4] 1: hdmi_cp_clk	
FREQDET_OFFSET	6:0	R/W	2	Determine the pre-set threshold, within which means the frequency is still stable. 0: No variation is allowed. 1: $\pm F_x / 1000$ 2: $\pm 2 * F_x / 1000$ 3: $\pm 3 * F_x / 1000$... 127: $\pm 127 * F_x / 1000$, where F_x is frequency of xtal clock.	

Register:: HDMI_FREQDET_UPPER_M					0xE8
Name	Bit	R/W	Default	Description	Config
RESERVED_FREQ2	7	R/W	0	Reserved.	
UPPER_BOUND[14:8]	6:0	R/W	2D	Once the frequency counter exceeds this value, then it will be treated as unstable.	

Register:: HDMI_FREQDET_UPPER_L					0xE9
Name	Bit	R/W	Default	Description	Config
UPPER_BOUND[7:0]	7:0	R/W	ED	Once the frequency counter exceeds this value, then it will be treated as unstable.	

Register:: HDMI_FREQDET_LOWER_M					0xEA
Name	Bit	R/W	Default	Description	Config



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RESERVED_FREQ3	7	R/W	0	Reserved.	
LOWER_BOUND[14:8]	6:0	R/W	2	Once the frequency counter is smaller than this value, then it will be treated as unstable.	

Register:: HDMI_FREQDET_LOWER_L					0xEB
Name	Bit	R/W	Default	Description	Config
LOWER_BOUND[7:0]	7:0	R/W	F6	Once the frequency counter is smaller than this value, then it will be treated as unstable.	

Register:: HDMI_FREQDET_STABLE					0xEC
Name	Bit	R/W	Default	Description	Config
RESULT_POPUP	7	W	0	POP UP the counter value in HW The result will be shown in 0xED[7], 0xED[6:0], 0xEE[7:0]	Wclr_out
STABLE_TIME	6:0	R/W	A	Determine how much times that freq needs to be within the pre-set threshold then the freq can be regarded as stable. 0: 1 time. 1: 2 time. 2: 3 times. ... 127: 128 times.	

Register:: HDMI_FREQDET_RESULT_M					0xED
Name	Bit	R/W	Default	Description	Config
NO_CLOCK	7	R	0	No input clock	
FREQDET_RESULT[14:8]	6:0	R		The result of frequency counter	

Register:: HDMI_FREQDET_RESULT_L					0xEE
Name	Bit	R/W	Default	Description	Config
FREQDET_RESULT	7:0	R		The result of frequency counter	

Register:: HDMI_ERROR_TH					0xEF
Name	Bit	R/W	Default	Description	Config
FREQ_STABLE_IRQ_EN	7	R/W	0	Interrupt as long as the freq is stable. 0: Disabled 1: Enabled	
FREQ_STABLE	6	R	0	Determine if clock frequency is stable in measure process. (write 1 to clear) 0: Not stable yet 1: Stable at least once.	Wclr_out
HDMI_ERR_RESERV_ED	5	R/W	0	Reseved.	
FREQ_ERROR_TH	4:0	R/W	0	Error Count Upper Limit When accumulated error below this value, frequency unstable will not occur.	



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				0: means 1 error 1: means 2 errors 31: means 32 errors.	
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Internal OSC (Page 6)

Register::OSC TRIM_CTRL0					0xA0
Name	Bits	R/W	Default	Comments	Config
TRIM_EN	7	R/W	0x0	Trimming Enable 0: Disable 1: Enable	
TRIM_DONE	6	R	0x1	Trimming is done 0: In progress 1: Done	
TRIM_RESOLUTION	5	R/W	0x1	Trimming Counter Set (counted by Tref) 0: 125 1: 250 (higher resolution)	
TRIM_WCNT_1ms	4	R/W	0x1	Wait time for "Initial OSC stable" 0: 1* 2^10 *Tref 1: 15* 2^10 *Tref (1ms at Tref=70ns)	
TRIM_WCNT	3:2	R/W	0x1	Wait time for trimming" 00: 1* 2^10 *Tref 01: 2* 2^10 *Tref 10: 3 * 2^10 *Tref 11: 4 * 2^10 *Tref	
IOSC_DIV	1:0	R/W	0	IOSC Divider 00: Div 1 (default) 01: Div 2 10: Div 4 11: Div 8	

Register::OSC TRIM_CTRL1					0xA1
Name	Bits	R/W	Default	Comments	Config
TRIM_TARGET	7:0	R/W	0xFB	Trimming Comparison Target (default when Tref = 70ns)	

Register::OSC TRIM_CTRL2					0xA2
Name	Bits	R/W	Default	Comments	Config
TRIM_MANUAL_EN	7	R/W	0	Trimming Manual mode Enable 0: Trimming Auto Mode 1: Trimming Manual Mode	
TRIM_LT	6	R	0	0: Trimming Counter Result more than target 1: Trimming Counter Result less than target	
TRIM_VC_RESULT	5:3	R	0	Trimming VC Result	
TRIM_MOS_RESULT	2:0	R	0	Trimming MOS Result	

Register::EMBEDDED_OSC_CTRL					0xA3
Name	Bits	R/W	Default	Comments	Config
OSC_EN	7	R/W	01	EMB OSC ENABLE, (need waiting 1ms after enable) 0: DISABLE 1: ENABLE	



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OSC_AUTO	6	R/W	1	0: manual mode (by A2[5:0]) 1: auto switch to trimming result	
OSC_VR_VC	5:3	R/W	0	bit[5:3] OSC VC Tune (fine tune) active when manual mode (bit6=0)	
OSC_VR_MOS	2:0	R/W	0x3	bit[2:0] OSC MOS Tune (coarse tune) active when manual mode (bit6=0)	

Note: all Page6 registers reset to default value only when external reset/por happen



Vivid color-DCC (Page 7)

Register:: DCC_CTRL_0 0xc7					
Name	Bits	R/W	Default	Comments	Config
DCC_EN	7	R/W	0	DCC_ENABLE 0: Disable 1: Enable	
Y_FORMULA	6	R/W	0	Y_FORMULA 0: $Y = (2R+5G+B)/8$ 1: $Y = (5R+8G+3B)/16$	
SC_EN	5	R/W	0	SOFT_CLAMP 0: Disable 1: Enable	
DCC_MODE	4	R/W	0	DCC_MODE 0: Auto Mode 1: Manual Mode	
SCG_EN	3	R/W	0	SCENE_CHANGE 0: Disable Scene-Change Function 1: Enable Scene-Change Function in Auto Mode	
BWL_EXP	2	R/W	0	BWL_EXP 0: Disable Black/White Level Expansion 1: Enable Black/White Level Expansion in Auto Mode	
PAGE_SEL	1:0	R/W	0	DCC_PAGE_SEL 00: Page 0 (for Histogram / Ymin-max / Soft-Clamping / Scene-Change) 01: Page 1 (for Y-Curve / WBL Expansion) 10: Page 2 (for Calculation Parameter) 11: Page 3 (for Testing and Debug)	

Register:: DCC_CTRL_1 0xc8					
Name	Bits	R/W	Default	Comments	Config
GAIN_EN	7	R/W	0	DCC gain control enable 0: Disable 1: Enable Note: DCC gain control enable must delay MOV_AVG_LEN frame after DCC enable.	
DCC_FLAG	6	R	0	1: time to write highlight window position & normalized factor, write to clear	
SAT_COMP_EN	5	R/W	0	Saturation Compensation Enable 0: Disable 1: Enable	
BLD_MODE	4	R/W	0	Blending Factor Control Mode 0: old mode 1: new mode (diff. regions have diff. blending factor)	
Reserved	3:0	--	0x00	Reserved to 0	

Register:: DCC Address Port 0xc9					
Name	Bits	R/W	Default	Comments	Config
DCC_ADDR	7:0	R/W	0x00	DCC address	



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Register:: DCC Data Port					0xca
Name	Bits	R/W	Default	Comments	Config
DCC_DATA	7:0	R/W	0x00	DCC data	

Register:: NOR_FACTOR_H (page0)					(ACCESS[C9,CA]) 0x00
Name	Bits	R/W	Default	Comments	Config
Reserved	7:6	--	--	Reserved	
NOR_FAC_H	5:0	R/W	0x00	Bit[21:16] of Normalized Factor; NF=(255/N)*(2^22)	

Register:: NOR_FACTOR_M (page0)					(ACCESS[C9,CA]) 0x01
Name	Bits	R/W	Default	Comments	Config
NOR_FAC_M	7:0	R/W	0x00	Bit[15:8] of Normalized Factor; NF=(255/N)*(2^22)	

Register:: NOR_FACTOR_L (page0)					(ACCESS[C9,CA]) 0x02
Name	Bits	R/W	Default	Comments	Config
NOR_FAC_L	7:0	R/W	0x00	Bit[7:0] of Normalized Factor; NF=(255/N)*(2^22)	

Register:: BBE_CTRL (page0)					(ACCESS[C9,CA]) 0x03
Name	Bits	R/W	Default	Comments	Config
BBE_EN	7	R/W	0	BBE_ENA 0: Disable Black-Background Exception 1: Enable Black-Background Exception	
Reserved	6:4	--	--	Reserved	
BBE_THD	3:0	R/W	0x4	BBE_THD 8-bit RGB Threshold for Black-Background Exception	

Register:: NFLT_CTRL (page0)					(ACCESS[C9,CA]) 0x04
Name	Bits	R/W	Default	Comments	Config
HNFLT_EN	7	R/W	0	HNFLT_ENA 0: Disable Histogram Noise Filter 1: Enable Histogram Noise Filter	
HNFLT_THD	6:4	R/W	0	HNFLT_THD Threshold for Histogram Noise Filter	
YNFLT_EN	3	R/W	0	YNFLT_ENA 0: Disable Ymax / Ymin Noise Filter 1: Enable Ymax / Ymin Noise Filter	
YNFLT_THD	2:0	R/W	0	YNFLT_THD Threshold for Ymax/Ymin Noise Filter (=4*YNFLT_THD)	



REALTEK

RTD2261W/2271W/2281W Series-GR

Register:: HIST_CTRL (page0)				(ACCESS[C9,CA]) 0x05	
Name	Bits	R/W	Default	Comments	Config
RH0_LIMITER	7	R/W	0	RH0_LIMITER 0: Disable RH0 Limiter 1: Enable RH0 Limiter	
RH1_LIMITER	6	R/W	0	RH1_LIMITER 0: Disable RH1 Limiter 1: Enable RH1 Limiter	
REAL_MA_LEN	5:3	R	--	Real MOV_AVG_LEN may be different with MOV_AVG_LEN, if SCG enable	
MOV_AVG_LEN	2:0	R/W	0	MOV_AVG_LEN 000: Histogram Moving Average Length = 1 001: Histogram Moving Average Length = 2 010: Histogram Moving Average Length = 4 011: Histogram Moving Average Length = 8 100: Histogram Moving Average Length = 16 101~111: reserved	

Register:: SOFT_CLAMP (page0)				(ACCESS[C9,CA]) 0x06	
Name	Bits	R/W	Default	Comments	Config
SOFT_CLAMP	7:0	R/W	0xB0	Slope of Soft-Clamping (= SOFT_CLAMP / 256)	

Register:: Y_MAX_LB (page0)				(ACCESS[C9,CA]) 0x07	
Name	Bits	R/W	Default	Comments	Config
Y_MAX_LB	7:0	R/W	0xFF	Lower Bound of Y_MAX (= 4*Y_MAX_LB)	

Register:: Y_MIN_HB (page0)				(ACCESS[C9,CA]) 0x08	
Name	Bits	R/W	Default	Comments	Config
Y_MIN_HB	7:0	R/W	0x00	Higher Bound of Y_MIN (= 4*Y_MIN_HB)	

Register:: SCG_PERIOD (page0)				(ACCESS[C9,CA]) 0x09	
Name	Bits	R/W	Default	Comments	Config
SCG_MODE	7	R/W	0	Scene-Change Control Mode 0: old mode (2553V) 1: new mode (2622)	
Reserved	6:5	--	--	Reserved	
SCG_PERIOD	4:0	R/W	0x10	Scene-Change Mode Period = 1~32. Note: SCG_PERIOD >= MOV_AVG_LEN, CRED-05[2:0](page0)	

Register:: SCG_LB (page0)				(ACCESS[C9,CA]) 0x0A	
Name	Bits	R/W	Default	Comments	Config
SCG_LB	7:0	R/W	0x00	SCG_DIFF Lower Bound for Exiting Scene-Change Mode	



REALTEK

RTD2261W/2271W/2281W Series-GR

Register:: SCG_HB (page0)				(ACCESS[C9,CA]) 0x0B	
Name	Bits	R/W	Default	Comments	Config
SCG_HB	7:0	R/W	0xFF	SCG_DIFF Higher Bound for Exiting Scene-Change Mode	

Register:: POPUP_CTRL (page0)				(ACCESS[C9,CA]) 0x0C	
Name	Bits	R/W	Default	Comments	Config
Reserved	7:1	--	--	Reserved	
POPUP_BIT	0	R	--	Reg[0D]~Reg[16] are updated every frame. Once POPUP_BIT is read, the value of Reg[0D] ~ Reg[16] will not be updated until Reg[16] is read.	

Register:: SCG_DIFF (page0)				(ACCESS[C9,CA]) 0x0D	
Name	Bits	R/W	Default	Comments	Config
SCG_DIFF	7:0	R	--	= (Histogram Difference between Current Frame and Average) / 8	

Register:: Y_MAX_VAL (page0)				(ACCESS[C9,CA]) 0x0E	
Name	Bits	R/W	Default	Comments	Config
Y_MAX_VAL	7:0	R	--	= Max { Y_MAX_LB, (Y Maximum in Current Frame / 4) }	

Register:: Y_MIN_VAL (page0)				(ACCESS[C9,CA]) 0x0F	
Name	Bits	R/W	Default	Comments	Config
Y_MIN_VAL	7:0	R	--	= Min { Y_MIN_HB, (Y Minimum in Current Frame / 4) }	

Register:: S0_VALUE (page0)				(ACCESS[C9,CA]) 0x10	
Name	Bits	R/W	Default	Comments	Config
S0_VALUE	7:0	R	--	Normalized Histogram S0 Value	

Register:: S1_VALUE (page0)				(ACCESS[C9,CA]) 0x11	
Name	Bits	R/W	Default	Comments	Config
S1_VALUE	7:0	R	--	Normalized Histogram S1 Value	

Register:: S2_VALUE (page0)				(ACCESS[C9,CA]) 0x12	
Name	Bits	R/W	Default	Comments	Config
S2_VALUE	7:0	R	--	Normalized Histogram S2 Value	



REALTEK

RTD2261W/2271W/2281W Series-GR

Register:: S3_VALUE (page0)				(ACCESS[C9,CA]) 0x13	
Name	Bits	R/W	Default	Comments	Config
S3_VALUE	7:0	R	--	Normalized Histogram S3 Value	

Register:: S4_VALUE (page0)				(ACCESS[C9,CA]) 0x14	
Name	Bits	R/W	Default	Comments	Config
S4_VALUE	7:0	R	--	Normalized Histogram S4 Value	

Register:: S5_VALUE (page0)				(ACCESS[C9,CA]) 0x15	
Name	Bits	R/W	Default	Comments	Config
S5_VALUE	7:0	R	--	Normalized Histogram S5 Value	

Register:: S6_VALUE (page0)				(ACCESS[C9,CA]) 0x16	
Name	Bits	R/W	Default	Comments	Config
S6_VALUE	7:0	R	--	Normalized Histogram S6 Value	

Register:: YHL_THD (page0)				(ACCESS[C9,CA]) 0x17	
Name	Bits	R/W	Default	Comments	Config
YHL_THD	7:0	R/W	0x00	Y_H and Y_L Threshold When DIFF[10:0] < YHL_THD[7:0], Y_H and Y_L keep the previous values	

Register:: DEF_CRV[01] (page1)				(ACCESS[C9,CA]) 0x00	
Name	Bits	R/W	Default	Comments	Config
DEF_CRV01	7:0	R/W	0x10	Pre-Defined Y-Curve; Keep DEF_CRV[N] ≥ DEF_CRV[N-1]	

Register:: DEF_CRV[02] (page1)				(ACCESS[C9,CA]) 0x01	
Name	Bits	R/W	Default	Comments	Config
DEF_CRV02	7:0	R/W	0x20	Pre-Defined Y-Curve; Keep DEF_CRV[N] ≥ DEF_CRV[N-1]	

Register:: DEF_CRV[03] (page1)				(ACCESS[C9,CA]) 0x02	
Name	Bits	R/W	Default	Comments	Config
DEF_CRV03	7:0	R/W	0x30	Pre-Defined Y-Curve; Keep DEF_CRV[N] ≥ DEF_CRV[N-1]	



REALTEK

RTD2261W/2271W/2281W Series-GR

Register:: DEF_CRV[04] (page1)				(ACCESS[C9,CA]) 0x03	
Name	Bits	R/W	Default	Comments	Config
DEF_CRV04	7:0	R/W	0x40	Pre-Defined Y-Curve; Keep DEF_CRV[N] ≥ DEF_CRV[N-1]	

Register:: DEF_CRV[05] (page1)				(ACCESS[C9,CA]) 0x04	
Name	Bits	R/W	Default	Comments	Config
DEF_CRV05	7:0	R/W	0x50	Pre-Defined Y-Curve; Keep DEF_CRV[N] ≥ DEF_CRV[N-1]	

Register:: DEF_CRV[06] (page1)				(ACCESS[C9,CA]) 0x05	
Name	Bits	R/W	Default	Comments	Config
DEF_CRV06	7:0	R/W	0x60	Pre-Defined Y-Curve; Keep DEF_CRV[N] ≥ DEF_CRV[N-1]	

Register:: DEF_CRV[07] (page1)				(ACCESS[C9,CA]) 0x06	
Name	Bits	R/W	Default	Comments	Config
DEF_CRV07	7:0	R/W	0x70	Pre-Defined Y-Curve; Keep DEF_CRV[N] ≥ DEF_CRV[N-1]	

Register:: DEF_CRV[08] (page1)				(ACCESS[C9,CA]) 0x07	
Name	Bits	R/W	Default	Comments	Config
DEF_CRV08	7:0	R/W	0x80	Pre-Defined Y-Curve; Keep DEF_CRV[N] ≥ DEF_CRV[N-1]	

Register:: DEF_CRV[09] (page1)				(ACCESS[C9,CA]) 0x08	
Name	Bits	R/W	Default	Comments	Config
DEF_CRV09	7:0	R/W	0x90	Pre-Defined Y-Curve; Keep DEF_CRV[N] ≥ DEF_CRV[N-1]	

Register:: DEF_CRV[10] (page1)				(ACCESS[C9,CA]) 0x09	
Name	Bits	R/W	Default	Comments	Config
DEF_CRV10	7:0	R/W	0xA0	Pre-Defined Y-Curve; Keep DEF_CRV[N] ≥ DEF_CRV[N-1]	

Register:: DEF_CRV[11] (page1)				(ACCESS[C9,CA]) 0x0A	
Name	Bits	R/W	Default	Comments	Config
DEF_CRV11	7:0	R/W	0xB0	Pre-Defined Y-Curve; Keep DEF_CRV[N] ≥ DEF_CRV[N-1]	



REALTEK

RTD2261W/2271W/2281W Series-GR

Register:: DEF_CRV[12] (page1)				(ACCESS[C9,CA]) 0x0B	
Name	Bits	R/W	Default	Comments	Config
DEF_CRV12	7:0	R/W	0xC0	Pre-Defined Y-Curve; Keep DEF_CRV[N] ≥ DEF_CRV[N-1]	

Register:: DEF_CRV[13] (page1)				(ACCESS[C9,CA]) 0x0C	
Name	Bits	R/W	Default	Comments	Config
DEF_CRV13	7:0	R/W	0xD0	Pre-Defined Y-Curve; Keep DEF_CRV[N] ≥ DEF_CRV[N-1]	

Register:: DEF_CRV[14] (page1)				(ACCESS[C9,CA]) 0x0D	
Name	Bits	R/W	Default	Comments	Config
DEF_CRV14	7:0	R/W	0xE0	Pre-Defined Y-Curve; Keep DEF_CRV[N] ≥ DEF_CRV[N-1]	

Register:: DEF_CRV[15] (page1)				(ACCESS[C9,CA]) 0x0E	
Name	Bits	R/W	Default	Comments	Config
DEF_CRV15	7:0	R/W	0xF0	Pre-Defined Y-Curve; Keep DEF_CRV[N] ≥ DEF_CRV[N-1]	

Register:: DEF_CRV[16] (page1)				(ACCESS[C9,CA]) 0x0F	
Name	Bits	R/W	Default	Comments	Config
DEF_CRV16	7:0	R/W	0x00	Pre-Defined Y-Curve; Keep DEF_CRV[N] ≥ DEF_CRV[N-1] Note : default = 0x00 means 0x100 (256)	

When y-curve boundary is changed (DEF_CRV[16] != 0x00), disable histogram noise filter.

Registers below is effective only when auto mode is disable and black/white level expansion is enabled.

When auto mode is enabled (DCC_MODE=0), Y_BL_BIAS and Y_WL_BIAS are read-only.

Register:: Y_BL_BIAS (page1)				(ACCESS[C9,CA]) 0x10	
Name	Bits	R/W	Default	Comments	Config
Y_BL_BIAS	7:0	R/W	0x00	Y Offset for Black-Level Expansion (Y_L' = 4*Y_BL_BIAS)	

Register:: Y_WL_BIAS (page1)				(ACCESS[C9,CA]) 0x11	
Name	Bits	R/W	Default	Comments	Config
Y_WL_BIAS	7:0	R/W	0x00	Y Offset for While-Level Expansion (1023-Y_H' = 4*Y_WL_BIAS)	

Load double buffer CRED-00 ~ CRED-11 (page1) after write CRED-11 when DCC enable



Register:: SAT_FACTOR (page1)				(ACCESS[C9,CA]) 0x12	
Name	Bits	R/W	Default	Comments	Config
Reserved	7:6	--	--	Reserved	
SAT_FACTOR	5:0	R/W	0x00	Saturation Compensation Factor = 0 ~ 32.	

Registers below is effective only when auto mode is enabled.

In manual mode (DCC_MODE=1), BLD_VAL will be fixed to 0. It means Y-curve is fully determined by DEF_CUR[01~15]

Register:: BLD_UB (page1)				(ACCESS[C9,CA]) 0x13	
Name	Bits	R/W	Default	Comments	Config
BLD_UB	7:0	R/W	0x00	Upper Bound of Blending Factor	

Register:: BLD_LB (page1)				(ACCESS[C9,CA]) 0x14	
Name	Bits	R/W	Default	Comments	Config
BLD_LB	7:0	R/W	0x00	Lower Bound of Blending Factor	

Register:: DEV_FACTOR (page1)				(ACCESS[C9,CA]) 0x15	
Name	Bits	R/W	Default	Comments	Config
DEV_FACTOR	7:0	R/W	0x00	Deviation Weighting Factor	

Register:: BLD_VAL_SEL (page1)				(ACCESS[C9,CA]) 0x16	
Name	Bits	R/W	Default	Comments	Config
WL_RANGE	7:6	R/W	0x00	White-Level Range 00: Yi = 512 (Z8) 01: Yi = 576 (Z9) 10: Yi = 640 (Z10) 11: Yi = 704 (Z11)	
WL_BLD_VAL	5:4	R/W	0x00	White-Level Blending Factor 00: 0 (user-defined curve) 01: R/2 10: R 11: 2R	
BL_RANGE	3:2	R/W	0x00	Black-Level Range 00: Yi = 448 (Z7) 01: Yi = 384 (Z6) 10: Yi = 320 (Z5) 11: Yi = 256 (Z4)	
BL_BLD_VAL	1:0	R/W	0x00	Black-Level Blending Factor 00: 0 (user-defined curve) 01: R/2 10: R 11: 2R	



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Register:: BLD_VAL (page1) (ACCESS[C9,CA]) 0x17				
Name	Bits	R/W	Default	Comments
BLD_VAL	7:0	R	--	= Max{ BLD_UB – [(DEV_VAL*DEV_FACTOR)/256], BLD_LB}

Register:: DEV_VAL_HI (page1) (ACCESS[C9,CA]) 0x18				
Name	Bits	R/W	Default	Comments
DEV_VAL_HI	7:0	R	--	Bit[8:1] of Deviation Value

Register:: DEV_VAL_LO (page1) (ACCESS[C9,CA]) 0x19				
Name	Bits	R/W	Default	Comments
DEV_VAL_LO	7	R	--	Bit[0] of Deviation Value
Reserved	6:0	--	--	Reserved

Register:: SRAM initial value (page2) (ACCESS[C9,CA]) 0x00~0x8F				
Name	Bits	R/W	Default	Comments
SRAM_XX	7:0	W	--	Addr 00: SRAM_00 Addr 01: SRAM_01 Addr 8F : SRAM_8F

Register:: SRAM_BIST (page3) (ACCESS[C9,CA]) 0x00				
Name	Bits	R/W	Default	Comments
BIST_EN	7	R/W	0	BIST_EN 0: disable 1: enable
RAM_Mode	6	R/W	0	RAM_Mode 0: dclk domain mode (normal mode, BIST) 1: MCU domain mode (SCG test)
Reserved	5:2	--	--	Reserved
BIST_PERIOD	1	R	--	BIST_Period 0: BIST is done 1: BIST is running
BIST_OK	0	R	--	BIST_OK 0: SRAM fail 1: SRAM ok

ICM(Page 7)

Address: D0 ICM Control

Default: 00h



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RTD2261W/2271W/2281W Series-GR

Bit	Mode	Function
7	R/W	ICM Enable 0: Disable 1: Enable
6	R/W	Y Correction Mode 0: $dY = (8dU+dV)/8$ 1: $dY = (6dU+dV)/8$
5	R/W	ICM U/V Delta Range: 0: Original -128~+127 1: Double -256~254
4	R/W	CM0 Enable 0: Disable 1: Enable
3	R/W	CM1 Enable 0: Disable 1: Enable
2	R/W	CM2 Enable 0: Disable 1: Enable
1	R/W	CM3 Enable 0: Disable 1: Enable
0	R/W	CM4 Enable 0: Disable 1: Enable

Address: D1 ICM_SEL

Default: 00h

Bit	Mode	Function
7:5	R/W	ICM Test Mode 000: disable 001: bypass U, V result 010: bypass hue/saturation result 011: bypass dU, dV value 1xx: R,B as LUT input, and bypass LUT output to R/G/B output
4	R/W	delta U/V range extend 0: delta U/V x1 (default) 1: delta U/V x4
3	R/W	CM5 Enable 0: Disable 1: Enable
2:0	R/W	CM Select 000: Select Chroma Modifier 0 for Accessing Through Data Port 001: Select Chroma Modifier 1 for Accessing Through Data Port 010: Select Chroma Modifier 2 for Accessing Through Data Port 011: Select Chroma Modifier 3 for Accessing Through Data Port 100: Select Chroma Modifier 4 for Accessing Through Data Port 101: Select Chroma Modifier 5 for Accessing Through Data Port 110~111: reserved

Address: D2 ICM_ADDR

Default: 00h

Bit	Mode	Function
7:0	R/W	ICM port address

Address: D3 ICM_Data

Bit	Mode	Function
7:0	R/W	ICM port data

ICM_ADDR will be increased automatically after each byte of ICM_DATA has been accessed.



REALTEK

RTD2261W/2271W/2281W Series-GR

Address: D3-00 MST HUE HB

Default: x0h

Bit	Mode	Function
7:4	--	Reserved
3:0	W	High Byte[11:8] of Master Hue for Chroma Modifier N.

Address: D3-01 MST HUE LB

Default: 00h

Bit	Mode	Function
7:0	W	Low Byte[7:0] of Master Hue for Chroma Modifier N.

Address: D3-02 HUE SET

Default: 00h

Bit	Mode	Function
7:6	W	CM[N].LWID 00: CM[N] left width = 64 01: CM[N] left width = 128 10: CM[N] left width = 256 11: CM[N] left width = 512
5:4	W	CM[N].LBUF 00: CM[N] left Buffer = 0 01: CM[N] left Buffer = 64 10: CM[N] left Buffer = 128 11: CM[N] left Buffer = 256
3:2	W	CM[N].RWID 00: CM[N] right width = 64 01: CM[N] right width = 128 10: CM[N] right width = 256 11: CM[N] right width = 512
1:0	W	CM[N].RBUF 00: CM[N] right Buffer = 0 01: CM[N] right Buffer = 64 10: CM[N] right Buffer = 128 11: CM[N] right Buffer = 256

Address: D3-03~32 U/V Offset

Default: 00h

Bit	Mode	Function
7:0	W	Addr 03: U Offset 00, -128~127 Addr 04: V Offset 00, -128~127 Addr 05: U Offset 01, -128~127 Addr 06: V Offset 01, -128~127 Addr 07: U Offset 02, -128~127 Addr 08: V Offset 02, -128~127 Addr 09: U Offset 03, -128~127 Addr 0A: V Offset 03, -128~127 Addr 0B: U Offset 04, -128~127 Addr 0C: V Offset 04, -128~127 Addr 0D: U Offset 05, -128~127 Addr 0E: V Offset 05, -128~127 Addr 0F: U Offset 06, -128~127 Addr 10: V Offset 06, -128~127 Addr 11: U Offset 07, -128~127 Addr 12: V Offset 07, -128~127 Addr 13: U Offset 10, -128~127 Addr 14: V Offset 10, -128~127 Addr 15: U Offset 11, -128~127 Addr 16: V Offset 11, -128~127 Addr 17: U Offset 12, -128~127 Addr 18: V Offset 12, -128~127 Addr 19: U Offset 13, -128~127 Addr 1A: V Offset 13, -128~127 Addr 1B: U Offset 14, -128~127 Addr 1C: V Offset 14, -128~127



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	Addr 1D: U Offset 15, -128~127 Addr 1E: V Offset 15, -128~127 Addr 1F: U Offset 16, -128~127 Addr 20: V Offset 16, -128~127 Addr 21: U Offset 17, -128~127 Addr 22: V Offset 17, -128~127 Addr 23: U Offset 20, -128~127 Addr 24: V Offset 20, -128~127 Addr 25: U Offset 21, -128~127 Addr 26: V Offset 21, -128~127 Addr 27: U Offset 22, -128~127 Addr 28: V Offset 22, -128~127 Addr 29: U Offset 23, -128~127 Addr 2A: V Offset 23, -128~127 Addr 2B: U Offset 24, -128~127 Addr 2C: V Offset 24, -128~127 Addr 2D: U Offset 25, -128~127 Addr 2E: V Offset 25, -128~127 Addr 2F: U Offset 26, -128~127 Addr 30: V Offset 26, -128~127 Addr 31: U Offset 27, -128~127 Addr 32: V Offset 27, -128~127
--	--

Y-Peaking and coring (D-Domain) (Page 7)

Address: D6 peaking/coring access port control **Default: 00h**

Bit	Mode	Function
7	R/W	Enable peaking / coring access port
6	R/W	Peaking/coring Enable 0: Disable 1: Enable
5	R/W	Y peaking Coefficient Resolution 0: n/32 1: n/64
4:3	--	Reserved
2:0	R/W	Peaking/coring port address

Address: D7-00 Peaking_Coef0

Bit	Mode	Function
7:0	R/W	Coefficient C0 of Peaking filter: Valid Range: -128/32(-128) ~ 127/32 (127) (2's complement)

Address: D7-01 Peaking_Coef1

Bit	Mode	Function



REALTEK

RTD2261W/2271W/2281W Series-GR

7:0	R/W	Coefficient C1 of Peaking filter: Valid Range: -128/32(-128) ~ 127/32 (127) (2's complement)
-----	-----	--

Address: D7-02 Peaking_Coef2

Bit	Mode	Function
7:0	R/W	Coefficient C2 of Peaking filter: Valid Range: -128/32(-128) ~ 127/32 (127) (2's complement)

Address: D7-03 Coring_Min

Bit	Mode	Function
7:5	R/W	Reserved
4:0	R/W	Coring Minimum value

Address: D7-04 Coring_Max_Pos

Bit	Mode	Function
7:0	R/W	Coring Maximum Positive value

Address: D7-05 Coring_Max_Neg

Bit	Mode	Function
7:0	R/W	Coring Maximum Negative value (2's complement)

$$Y'[n] = C0*Y[n] + C1*(Y[n-1]+Y[n+1]) + C2*(Y[n-2]+Y[n+2]), -256 \leq Y' \leq 255$$

$$Y_{peak} = Y'[n] - \text{Coring_Min}, \quad \text{if } Y'[n] \geq 0,$$

$$= Y'[n] + \text{Coring_Min}, \quad \text{if } Y'[n] < 0$$

$$\text{if } (|Y'[n]| \leq \text{Coring_Min})$$

$$Y''[n] = 0,$$

$$\text{else if } Y_{peak} \geq \text{Coring_Max_Pos}$$

$$Y''[n] = \text{Coring_Max_Pos}$$

$$\text{else if } Y_{peak} \leq \text{Coring_Max_Neg}$$

$$Y''[n] = \text{Coring_Max_Neg}$$

else

$$Y''[n] = Y_{peak}$$

$$Y_o[n] = Y[n] + Y''[n], 0 \leq Y_o[n] \leq 255$$



DCR (Page 7)

Register::DCR Address Port					0xD8
Name	Bits	R/W	Default	Comments	Config
DCR_ADDR	7:2	--	0	DCR address	
RESULT_READ	1	R/W	0	0: Disable Read to refresh measure result. 1: Read DCR measure result.	
MEASURE_START	0	R/W	0	0: Finish or disable 1: Start DCR computation.	

Register:: DCR Data Port					0xD9
Name	Bits	R/W	Default	Comments	Config
DCR_DATA	7:0	R/W	0x00	DCR data	

Register:: DCR_THRESHOLD1					(ACCESS[D8,D9]) 0x00
Name	Bits	R/W	Default	Comments	Config
THRESHOLD1_VALUE	7:0	R/W	0x08	DCR threshold1. (R+G+B)*0.75	

If we want to set threshold1 = 200. THRESHOLD1_VALUE = 200*0.75 = 150.

Register:: DCR_THRESHOLD2					(ACCESS[D8,D9]) 0x01
Name	Bits	R/W	Default	Comments	Config
THRESHOLD2_VALUE	7:0	R/W	0x60	DCR threshold2. (threshold2 > threshold1) (R+G+B)*0.75	

If we want to set threshold2 = 200. THRESHOLD2_VALUE = 200*0.75 = 150.

Register::DCR_ABOVE_TH1_NUM_2					(ACCESS[D8,D9]) 0x02
Name	Bits	R/W	Default	Comments	Config
ABOVE_TH1_NUM_2	7:0	R	0	Total pixel number above threshold1: bit[23:16]	



REALTEK

RTD2261W/2271W/2281W Series-GR

Register::DCR_ABOVE_TH1_NUM_1 (ACCESS[D8,D9]) 0x03				
Name	Bits	R/W	Default	Comments
ABOVE_TH1_NUM_1	7:0	R	0	Total pixel number above threshold1: bit[15:8]

Register::DCR_ABOVE_TH1_NUM_0 (ACCESS[D8,D9]) 0x04				
Name	Bits	R/W	Default	Comments
ABOVE_TH1_NUM_0	7:0	R	0	Total pixel number above threshold1: bit[7:0]

Register::DCR_ABOVE_TH1_VAL_3 (ACCESS[D8,D9]) 0x05				
Name	Bits	R/W	Default	Comments
ABOVE_TH1_VAL_3	7:0	R	0	Total sum (R+G+B) of pixel value above threshold1: bit[31:24]

Register::DCR_ABOVE_TH1_VAL_2 (ACCESS[D8,D9]) 0x06				
Name	Bits	R/W	Default	Comments
ABOVE_TH1_VAL_2	7:0	R	0	Total sum (R+G+B) of pixel value above threshold1: bit[23:16]

Register::DCR_ABOVE_TH1_VAL_1 (ACCESS[D8,D9]) 0x07				
Name	Bits	R/W	Default	Comments
ABOVE_TH1_VAL_1	7:0	R	0	Total sum (R+G+B) of pixel value above threshold1: bit[15:8]

Register::DCR_ABOVE_TH1_VAL_0 (ACCESS[D8,D9]) 0x08				
Name	Bits	R/W	Default	Comments
ABOVE_TH1_VAL_0	7:0	R	0	Total sum (R+G+B) of pixel value above threshold1: bit[7:0]

Register::DCR_ABOVE_TH2_NUM_2 (ACCESS[D8,D9]) 0x09				
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Name	Bits	R/W	Default	Comments	Config
ABOVE_TH2_NUM_2	7:0	R	0	Total pixel number above threshold2: bit[23:16]	

Register::DCR_ABOVE_TH2_NUM_1 (ACCESS[D8,D9]) 0x0A					
Name	Bits	R/W	Default	Comments	Config
ABOVE_TH2_NUM_1	7:0	R	0	Total pixel number above threshold2: bit[15:8]	

Register::DCR_ABOVE_TH2_NUM_0 (ACCESS[D8,D9]) 0x0B					
Name	Bits	R/W	Default	Comments	Config
ABOVE_TH2_NUM_0	7:0	R	0	Total pixel number above threshold2: bit[7:0]	

Register::DCR_ABOVE_TH2_VAL_3 (ACCESS[D8,D9]) 0x0C					
Name	Bits	R/W	Default	Comments	Config
ABOVE_TH2_VAL_3	7:0	R	0	Total sum (R+G+B) of pixel value above threshold2: bit[31:24]	

Register::DCR_ABOVE_TH2_VAL_2 (ACCESS[D8,D9]) 0x0D					
Name	Bits	R/W	Default	Comments	Config
ABOVE_TH2_VAL_2	7:0	R	0	Total sum (R+G+B) of pixel value above threshold2: bit[23:16]	

Register::DCR_ABOVE_TH2_VAL_1 (ACCESS[D8,D9]) 0x0E					
Name	Bits	R/W	Default	Comments	Config
ABOVE_TH2_VAL_1	7:0	R	0	Total sum (R+G+B) of pixel value above threshold2: bit[15:8]	

Register::DCR_ABOVE_TH2_VAL_0 (ACCESS[D8,D9]) 0x0F					
Name	Bits	R/W	Default	Comments	Config



ABOVE_TH2_VAL_0	7:0	R	0	Total sum (R+G+B) of pixel value above threshold2: bit[7:0]	
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Register::DCR_HIGH_LV_NUM_R_1 (ACCESS[D8,D9]) 0x10					
Name	Bits	R/W	Default	Comments	Config
HIGH_LV_NUM_R_1	7:0	R	0	Dynamically detect highest level pixel number of red channel. RMAX_NUM[15:8]	

Register::DCR_HIGH_LV_NUM_R_0 (ACCESS[D8,D9]) 0x11					
Name	Bits	R/W	Default	Comments	Config
HIGH_LV_NUM_R_0	7:0	R	0	Dynamically detect highest level pixel number of red channel. RMAX_NUM[7:0]	

Register::DCR_LOW_LV_NUM_R_1 (ACCESS[D8,D9]) 0x12					
Name	Bits	R/W	Default	Comments	Config
LOW_LV_NUM_R_1	7:0	R	0	Dynamically detect the lowest level pixel number of red channel. RMIN_NUM[15:8]	

Register::DCR_LOW_LV_NUM_R_0 (ACCESS[D8,D9]) 0x13					
Name	Bits	R/W	Default	Comments	Config
LOW_LV_NUM_R_0	7:0	R	0	Dynamically detect the lowest level pixel number of red channel. RMIN_NUM[7:0]	

Register::DCR_HIGH_LV_VAL_R (ACCESS[D8,D9]) 0x14					
Name	Bits	R/W	Default	Comments	Config
HIGH_LV_VAL_R	7:0	R	0	Dynamically detect highest level value of red channel.	

Register::DCR_LOW_LV_VAL_R (ACCESS[D8,D9]) 0x15					
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Name	Bits	R/W	Default	Comments	Config
LOW_LV_VAL_R	7:0	R	0	Dynamically detect the lowest level value of red channel.	

Register::DCR_HIGH_LV_NUM_G_1 (ACCESS[D8,D9]) 0x16					
Name	Bits	R/W	Default	Comments	Config
HIGH_LV_NUM_G_1	7:0	R	0	Dynamically detect the highest level pixel number of green channel. GMAX_NUM[15:8]	

Register::DCR_HIGH_LV_NUM_G_0 (ACCESS[D8,D9]) 0x17					
Name	Bits	R/W	Default	Comments	Config
HIGH_LV_NUM_G_0	7:0	R	0	Dynamically detect the highest level pixel number of green channel. GMAX_NUM[7:0]	

Register::DCR_LOW_LV_NUM_G_1 (ACCESS[D8,D9]) 0x18					
Name	Bits	R/W	Default	Comments	Config
LOW_LV_NUM_G_1	7:0	R	0	Dynamically detect the lowest level pixel number of green channel. GMIN_NUM[15:8]	

Register::DCR_LOW_LV_NUM_G_0 (ACCESS[D8,D9]) 0x19					
Name	Bits	R/W	Default	Comments	Config
LOW_LV_NUM_G_0	7:0	R	0	Dynamically detect the lowest level pixel number of green channel. GMIN_NUM[7:0]	

Register::DCR_HIGH_LV_VAL_G (ACCESS[D8,D9]) 0x1A					
Name	Bits	R/W	Default	Comments	Config
HIGH_LV_VAL_G	7:0	R	0	Dynamically detect the highest level value of green channel.	

Register::DCR_LOW_LV_VAL_G (ACCESS[D8,D9]) 0x1B					
Name	Bits	R/W	Default	Comments	Config



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LOW_LV_VAL_G	7:0	R	0	Dynamically detect the lowest level value of green channel.	
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Register::DCR_HIGH_LV_NUM_B_1 (ACCESS[D8,D9]) 0x1C					
Name	Bits	R/W	Default	Comments	Config
HIGH_LV_NUM_B_1	7:0	R	0	Dynamically detect the highest level pixel number of blue channel. BMAX_NUM[15:8]	

Register::DCR_HIGH_LV_NUM_B_0 (ACCESS[D8,D9]) 0x1D					
Name	Bits	R/W	Default	Comments	Config
HIGH_LV_NUM_B_0	7:0	R	0	Dynamically detect the highest level pixel number of blue channel. BMAX_NUM[7:0]	

Register::DCR_LOW_LV_NUM_B_1 (ACCESS[D8,D9]) 0x1E					
Name	Bits	R/W	Default	Comments	Config
LOW_LV_NUM_B_1	7:0	R	0	Dynamically detect the lowest level pixel number of blue channel. BMIN_NUM[15:8]	

Register::DCR_LOW_LV_NUM_B_0 (ACCESS[D8,D9]) 0x1F					
Name	Bits	R/W	Default	Comments	Config
LOW_LV_NUM_B_0	7:0	R	0	Dynamically detect the lowest level pixel number of blue channel. BMIN_NUM[7:0]	

Register:: DCR_HIGH_LV_VAL_B (ACCESS[D8,D9]) 0x20					
Name	Bits	R/W	Default	Comments	Config
HIGH_LV_VAL_B	7:0	R	0	Dynamically detect the highest level value of blue channel.	

Register:: DCR_LOW_LV_VAL_B (ACCESS[D8,D9]) 0x21					
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Name	Bits	R/W	Default	Comments	Config
LOW_LV_VAL_B	7:0	R	0	Dynamically detect the lowest level value of blue channel.	

IAPS Histogram (Page7)

Register::CABC_Ctrl					0xDB
Name	Bits	R/W	Default	Comments	Config
reserved	7:6	R/W	0x00	<p>Tese Mode:</p> <p>0x00: dither_rout,dither_gout,dither_bout, dither_dat_den, dither_lsb_rout,dither_lsb_gout,1'b0</p> <p>0x01: dvs,dhs,disp_all_den,colin_den,inwin_den, bri_all_den,bri_dat_den,bri_inwin_den,bri_bor_den, cabc_den_pre, cabc_inwin_den_pre,d_frame_start,cabc_den_end, dcclcr_vs,dcclcr_den_start,dcclcr_den_pre,dcclcr_inwin_den_pre, srgb_r_infoout[2:0],srgb_g_infoout[2:0],srgb_b_infoout[2:0], gma_all_den,gma_dat_den,gma_inwin_den_rtc,gma_bor_den</p> <p>0x10 : histo_test_port1,2'h0</p> <p>0x11 : 1 'b0 ,dcr_test_port ,cabc_test_port ,histo_test_port2 , 5 'h0</p>	
reserved	5:4	--	--	Reserved	
DCR_DATA_SRC	3	R/W	0	<p>DCR data from</p> <p>0: Original DCR (default)</p> <p>1: the same as CABC</p>	
CABC_EN	2	R/W	0	<p>CABC Histogram Enable</p> <p>0: Disable 1: Enable</p>	
Reserved	1	---	---	Reserved	
CABC/DCR_Crtl	0	R/W	00	CABC / DCR Data Update :	



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				0 : CABC / DCR data Update independently 1 : CABC / DCR data Update simultaneously	
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Register:: CABC Address Port 0xDC					
Name	Bits	R/W	Default	Comments	Config
CABC_ADDR	7:0	R/W	0x00	CABC address	

Register:: CABC Data Port 0xDD					
Name	Bits	R/W	Default	Comments	Config
CABC_DATA	7:0	R/W	0x00	CABC data	

Register:: NOR_FACTOR_H (ACCESS[DC,DD]) 0x00					
Name	Bits	R/W	Default	Comments	Config
Reserved	7:6	--	--	Reserved	
NOR_FAC_H	5:0	R/W	0x00	Bit[21:16] of Normalized Factor; NF=(255/N)*(2^22)	

Register:: NOR_FACTOR_M (ACCESS[DC,DD]) 0x01					
Name	Bits	R/W	Default	Comments	Config
NOR_FAC_M	7:0	R/W	0x00	Bit[15:8] of Normalized Factor; NF=(255/N)*(2^22)	

Register:: NOR_FACTOR_L (ACCESS[DC,DD]) 0x02					
Name	Bits	R/W	Default	Comments	Config
NOR_FAC_L	7:0	R/W	0x00	Bit[7:0] of Normalized Factor; NF=(255/N)*(2^22)	

Register:: S0_VALUE (ACCESS[DC,DD]) 0x03					
Name	Bits	R/W	Default	Comments	Config
S0_VALUE	7:0	R	--	Normalized Histogram S0 Value	

Register:: S1_VALUE (ACCESS[DC,DD]) 0x04					
Name	Bits	R/W	Default	Comments	Config
S1_VALUE	7:0	R	--	Normalized Histogram S1 Value	



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Register:: S2_VALUE (ACCESS[DC,DD]) 0x05						
Name	Bits	R/W	Default	Comments	Config	
S2_VALUE	7:0	R	--	Normalized Histogram S2 Value		

Register:: S3_VALUE (ACCESS[DC,DD]) 0x06						
Name	Bits	R/W	Default	Comments	Config	
S3_VALUE	7:0	R	--	Normalized Histogram S3 Value		

Register:: S4_VALUE (ACCESS[DC,DD]) 0x07						
Name	Bits	R/W	Default	Comments	Config	
S4_VALUE	7:0	R	--	Normalized Histogram S4 Value		

Register:: S5_VALUE (ACCESS[DC,DD]) 0x08						
Name	Bits	R/W	Default	Comments	Config	
S5_VALUE	7:0	R	--	Normalized Histogram S5 Value		

Register:: S6_VALUE (ACCESS[DC,DD]) 0x09						
Name	Bits	R/W	Default	Comments	Config	
S6_VALUE	7:0	R	--	Normalized Histogram S6 Value		

Register:: S7_VALUE (ACCESS[DC,DD]) 0x0A						
Name	Bits	R/W	Default	Comments	Config	
S7_VALUE	7:0	R	--	Normalized Histogram S7 Value		

Register:: S8_VALUE (ACCESS[DC,DD]) 0x0B						
Name	Bits	R/W	Default	Comments	Config	
S8_VALUE	7:0	R	--	Normalized Histogram S8 Value		

Register:: S9_VALUE (ACCESS[DC,DD]) 0x0C						
Name	Bits	R/W	Default	Comments	Config	
S9_VALUE	7:0	R	--	Normalized Histogram S9 Value		

Register:: S10_VALUE (ACCESS[DC,DD]) 0x0D						
Name	Bits	R/W	Default	Comments	Config	



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S10_VALUE	7:0	R	--	Normalized Histogram S10 Value	
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Register:: S11_VALUE (ACCESS[DC,DD]) 0x0E					
Name	Bits	R/W	Default	Comments	Config
S11_VALUE	7:0	R	--	Normalized Histogram S11 Value	

Register:: S12_VALUE (ACCESS[DC,DD]) 0x0F					
Name	Bits	R/W	Default	Comments	Config
S12_VALUE	7:0	R	--	Normalized Histogram S12 Value	

Register:: S13_VALUE (ACCESS[DC,DD]) 0x10					
Name	Bits	R/W	Default	Comments	Config
S13_VALUE	7:0	R	--	Normalized Histogram S13 Value	

Register:: S14_VALUE (ACCESS[DC,DD]) 0x11					
Name	Bits	R/W	Default	Comments	Config
S14_VALUE	7:0	R	--	Normalized Histogram S14 Value	

Register:: POPUP_CTRL (ACCESS[DC,DD]) 0x12					
Name	Bits	R/W	Default	Comments	Config
Reserved	7:1	--	--	Reserved	
POPUP_BIT	0	R	--	Reg[0D]~Reg[16] are updated every frame. Once POPUP_BIT is read, the value of Reg[0D] ~ Reg[16] will not be updated until Reg[16] is read.	

DCR and CABC refresh can be controlled by Read_Result bit in DCR or POPUP_CTRL in CABC. By Read_Result, DCR and CABC will refresh when this bit set to 0. By POPUP_CTRL, DCR and CABC will refresh after reading S14 value.

Register:: TH0_VALUE (ACCESS[DC,DD]) 0x20					
Name	Bits	R/W	Default	Comments	Config
TH0_VALUE	7:0	R/W	--	Threshold 0 of the histogram	

Register:: TH1_VALUE (ACCESS[DC,DD]) 0x21					
Name	Bits	R/W	Default	Comments	Config
TH1_VALUE	7:0	R/W	--	Threshold 1 of the histogram	



Register:: TH2_VALUE (ACCESS[DC,DD]) 0x22				
Name	Bits	R/W	Default	Comments
TH2_VALUE	7:0	R/W	--	Threshold 2 of the histogram

Register:: TH3_VALUE (ACCESS[DC,DD]) 0x23				
Name	Bits	R/W	Default	Comments
TH3_VALUE	7:0	R/W	--	Threshold 3 of the histogram

Register:: TH4_VALUE (ACCESS[DC,DD]) 0x24				
Name	Bits	R/W	Default	Comments
TH4_VALUE	7:0	R/W	--	Threshold 4 of the histogram

Register:: TH5_VALUE (ACCESS[DC,DD]) 0x25				
Name	Bits	R/W	Default	Comments
TH5_VALUE	7:0	R/W	--	Threshold 5 of the histogram

Register:: TH6_VALUE (ACCESS[DC,DD]) 0x26				
Name	Bits	R/W	Default	Comments
TH6_VALUE	7:0	R/W	--	Threshold 6 of the histogram

Register:: TH7_VALUE (ACCESS[DC,DD]) 0x27				
Name	Bits	R/W	Default	Comments
TH7_VALUE	7:0	R/W	--	Threshold 7 of the histogram

Register:: TH8_VALUE (ACCESS[DC,DD]) 0x28				
Name	Bits	R/W	Default	Comments
TH8_VALUE	7:0	R/W	--	Threshold 8 of the histogram

Register:: TH9_VALUE (ACCESS[DC,DD]) 0x29				
Name	Bits	R/W	Default	Comments
TH9_VALUE	7:0	R/W	--	Threshold 9 of the histogram

Register:: TH10_VALUE (ACCESS[DC,DD]) 0x2A				
Name	Bits	R/W	Default	Comments
TH10_VALUE	7:0	R/W	--	Threshold 10 of the histogram



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Register:: TH11_VALUE (ACCESS[DC,DD]) 0x2B				
Name	Bits	R/W	Default	Comments
TH11_VALUE	7:0	R/W	--	Threshold 11 of the histogram

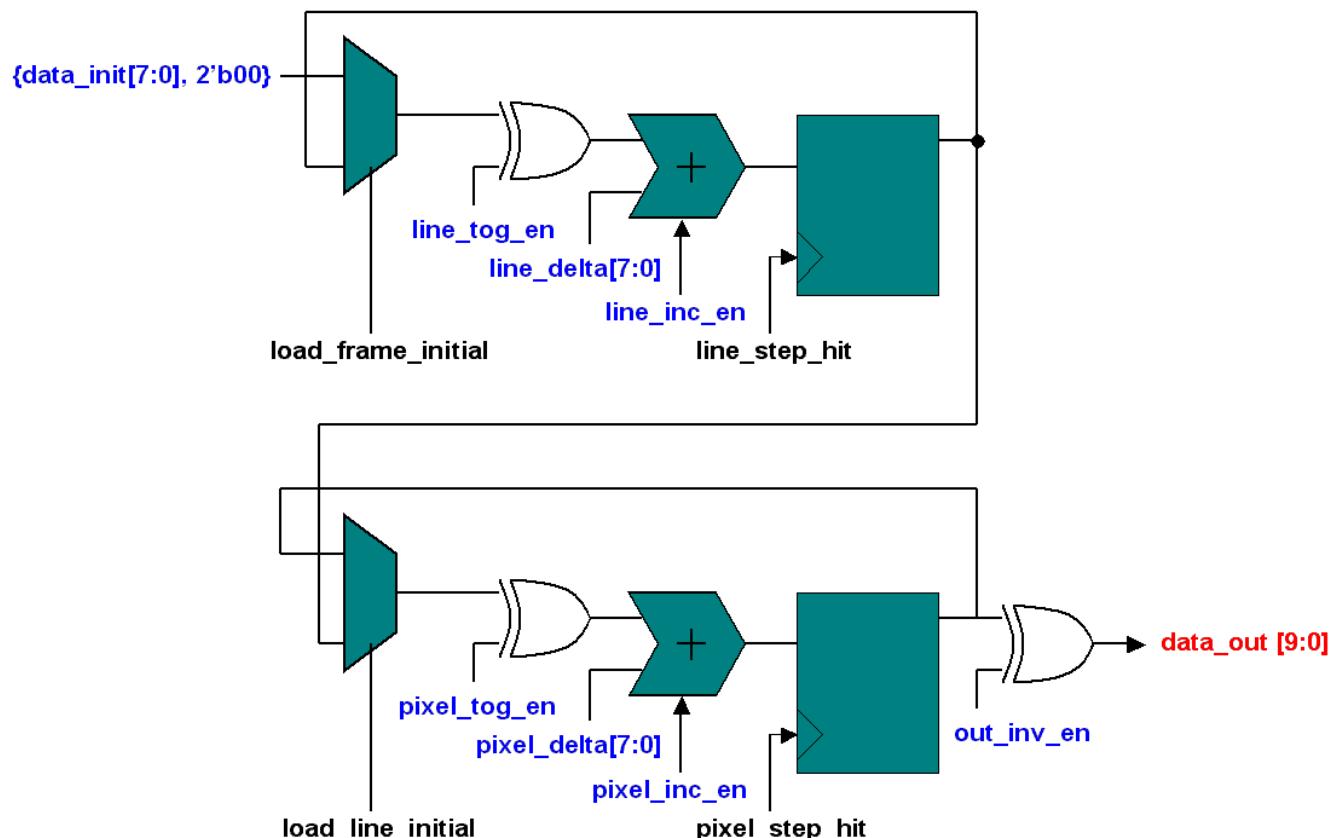
Register:: TH12_VALUE (ACCESS[DC,DD]) 0x2C				
Name	Bits	R/W	Default	Comments
TH12_VALUE	7:0	R/W	--	Threshold 12 of the histogram

Register:: TH13_VALUE (ACCESS[DC,DD]) 0x2D				
Name	Bits	R/W	Default	Comments
TH13_VALUE	7:0	R/W	--	Threshold 13 of the histogram



Pattern Generator in D-Domain (Page 7)

RTD2485XD supports programmable patterns, such as gray-level, chessboard, dot-pattern, etc., for display image testing.



Register::DISP_PG_R_CTRL						0xF0
Name	Bits	R/W	Default	Comments	Config	
PG_ENABLE	7	R/W	0	Display Pattern Gen. Function Enable		
PG_R_CTRL_DUM	6	R/W	0	Dummy		
PG_ROUT_INV_EN	5	R/W	0	Inverse Data Output		
PG_R_CLAMP_EN	4	R/W	0	Adder result clamp to 10'h3FFF		



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LINE_R_TOG_EN	3	R/W	0	Data toggled in each line -step	
LINE_R_INC_EN	2	R/W	0	Data increment in each line-step	
PIXEL_R_TOG_EN	1	R/W	0	Data toggled in each pixel-step	
PIXEL_R_INC_EN	0	R/W	0	Data incremented in each pixel-step	

Register::DISP_PG_G_CTRL						0xF1
Name	Bits	R/W	Default	Comments	Config	
PG_G_CTRL_DUM	7:6	R/W	0	Dummy		
PG_GOUT_INV_EN	5	R/W	0	Inverse Data Output		
PG_G_CLAMP_EN	4	R/W	0	Adder result clamp to 10'h3FFF		
LINE_G_TOG_EN	3	R/W	0	Data toggled in each line -step		
LINE_G_INC_EN	2	R/W	0	Data increment in each line-step		
PIXEL_G_TOG_EN	1	R/W	0	Data toggled in each pixel-step		
PIXEL_G_INC_EN	0	R/W	0	Data incremented in each pixel-step		

Register::DISP_PG_B_CTRL						0xF2
Name	Bits	R/W	Default	Comments	Config	
PG_B_CTRL_DUM	7:6	R/W	0	Dummy		
PG_BOUT_INV_EN	5	R/W	0	Inverse Data Output		
PG_B_CLAMP_EN	4	R/W	0	Adder result clamp to 10'h3FFF		
LINE_B_TOG_EN	3	R/W	0	Data toggled in each line -step		
LINE_B_INC_EN	2	R/W	0	Data increment in each line-step		
PIXEL_B_TOG_EN	1	R/W	0	Data toggled in each pixel-step		
PIXEL_B_INC_EN	0	R/W	0	Data incremented in each pixel-step		



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Register::DISP_PG_R_Initial						0xF3
Name	Bits	R/W	Default	Comments		Config
PG_R_INIT	7:0	R/W	0	Initial Pattern Value for Red Data [9:2]		

Register::DISP_PG_G_Initial						0xF4
Name	Bits	R/W	Default	Comments		Config
PG_G_INIT	7:0	R/W	0	Initial Pattern Value for Green Data [9:2]		

Register::DISP_PG_B_Initial						0xF5
Name	Bits	R/W	Default	Comments		Config
PG_B_INIT	7:0	R/W	0	Initial Pattern Value for Blue Data [9:2]		

Register::DISP_PG_Pixel_Delta						0xF6
Name	Bits	R/W	Default	Comments		Config
PG_PIXEL_DELTA	7:0	R/W	0	Pixel Delta value for incremental		

Register::DISP_PG_Line_Delta						0xF7
Name	Bits	R/W	Default	Comments		Config
PG_LINE_DELTA	7:0	R/W	0	Line Delta value for incremental		

Register::DISP_PG_Pixel_Step_MSB						0xF8
Name	Bits	R/W	Default	Comments		Config
PG_PIXEL_STEP_M	7:0	R/W	01h	Pixel Step for toggle/incremental, can not be 0		

Register::DISP_PG_Line_Step_MSB						0xF9
Name	Bits	R/W	Default	Comments		Config
PG_LINE_STEP_M	7:0	R/W	01h	Line Step for toggle/incremental, can not be 0		

Register::DISP_PG Step_LSB						0xFA
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Name	Bits	R/W	Default	Comments	Config
LINE_STEP_DUM	7:6	R/W	0	Dummy	
PG_LINE_STEP_L	5:4	R/W	0	Decimal part for Line-step	
PIXEL_STEP_DUM	3:2	R/W	0	Dummy	
PG_PIXEL_STEP_L	1:0	R/W	0	Decimal part for Pixel-step	

Ex: If the pattern is 256 gray level in 640 pixels, the wanted pixel_step is $640/256 = 2.5$. Hence,
 $PG_PIXEL_STEP_M = 2h$ and $PG_PIXEL_STEP_L = 2'b10$.

($\{PG_PIXEL_STEP_M, PG_PIXEL_STEP_L\} = 2.5$).



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Reserved (Page8)

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Input Gamma Control (Page 9)

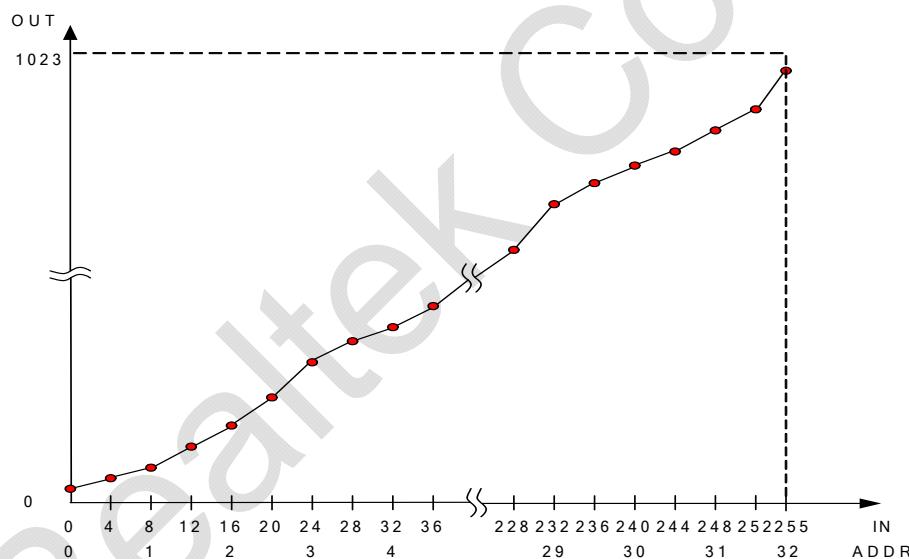
Address: A0 INPUT_GAMMA_PORT

Bit	Mode	Function
7:0	R/W	Access port for input gamma correction table

- The Gamma Table written to this port should follow the sequences as expressed below:

```
{2'b0, g0[9:4]}, {g0[3:0]}, 2'b0, g16[9:8]}, {g16[7:0]},           <- addr = 0
{2'b0, g32[9:4]}, {g32[3:0]}, 2'b0, g48[9:8]}, {g48[7:0]},           <- addr = 1
...
{2'b0, g992[9:4]}, {g992[3:0]}, 2'b0, g1008[9:8]}, {g1008[7:0]},   <- addr = 31
{2'b0, g1023[9:4]}, {g1023[3:0]}, 4'b0}, {8'b0}                      <- addr = 32
```

- There are two thresholds divide Input Gamma Table into three divisions.
 - From 0 to threshold 1 is the first division.
 - From (threshold 1 + 1) to threshold 2 is the second division.
- Above threshold 2 is the third division



Address: A1 INPUT_GAMMA_CTRL

Default: 00h

Bit	Mode	Function
7	R/W	Enable Access Channels for Input Gamma Correction Coefficient: 0: disable these channels (Default) 1: enable these channels
6	R/W	Input Gamma table enable 0: by pass (Default) 1: enable



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5:0	--	Reserved to 0

Address: A2 INPUT GAMMA LOW THRE**Default: 11h**

Bit	Mode	Function
7	R/W	Reserved to 0
6:0	R/W	Input Gamma low threshold value

Both threshold values are restricted in 0~64

Address: A3 INPUT GAMMA HIGH THRE**Default: 22h**

Bit	Mode	Function
7	R/W	Reserved to 0
6:0	R/W	Input Gamma high threshold value

High threshold value has to be greater than low threshold value.

Both threshold values are restricted in 0~64

Reserved (Page A)

GDI Phy(Page B)

PHY CONTROL

Register::CDR_00					0xA0
Name	Bits	R/W	Default	Comments	Config
lpf_cp05p_sel	7	R/W	0	select CDR lpf cp 0.5pF	
rfvco_lane0	6:0	R/W	3F	lane0 vco band selection=0~127	

Register::CDR_01					0XA1
Name	Bits	R/W	Default	Comments	Config
vco_div	7:6	R/W	0	VCO Divider Mcode: 00=VCO/1, 01=VCO/2, 10=VCO/4, 11=VCO/8	
sel_bb	5	R/W	1	0=linear PD 1=Binary PD	
sel_half	4	R/W	1	0=Full rate PD 1=Half rate PD ,	
sel_vcmfb	3	R/W	0 1	Charge pump common mode voltage Setting 0: set charge pump common mode voltage to CPVREF, i.e.	



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				0.7/0.65/0.6/0.55V 1: set charge pump common mode voltage to Vdd/2	
vco_vc_manual	2	R/W	0	1'b0: Cs=20pF, 1'b1: Cs=46pF	
reserved	1:0 1	R/W	0 1	reserved	
reserved	0	R/W	0	reserved	

Register::CDR_02					0xA2
Name	Bits	R/W	Default	Comments	Config
cp_sel	7:4	R/W	1	Charge pump current 0000: 3.75uA 0001: 7.5uA 0010: 11.25uA 0011: 15uA 0100: 7.5uA 0101: 15uA 0110: 22.5uA 0111: 30uA 1000:11.25uA 1001: 22.5uA 1010:33.75uA 1011: 45uA 1100: 15uA 1101: 30uA 1110: 45uA 1111: 60uA	
cpsr	3:2	R/W	1	Loop resister: 00=2K, 01=4K, 10=8K, 11=10K	
kvco	1:0	R/W	1	Kvco boost: 00=388MHz/V, 01=526MHz/V, 10=640MHz/V, 11=832MHz/V	

A1[7:4],A2,A3[0] enable when AF[6]=1



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RTD2261W/2271W/2281W Series-GR

Register:: CDR_03						0XA3
Name	Bits	R/W	Default	Comments		Config
bpdgain	7	R/W	1	BPD gain 1'b1= binary PD gain double		
sel_cont3	6	R/W	1	1=binary PD UP/DN pulse div3 0=binary PD UP/DN pulse div4		
sel_ibx	5	R/W	0	VCO bias current 0: ibn, 1: ibx		
sel_ib90	4:3	R/W	1	90u bias current: 00=80u, 01=90u, 10=100u, 11=110u		
sel_ib25	2:1	R/W	2	25u bias current: 00=15u, 01=20u, 10=25u, 11=30u.		
cpsc	0	R/W	0	Loop capacitor: 0=2p disable, 1=2p enable		

Register:: FLD_00						0XA4
Name	Bits	R/W	Default	Comments		Config
Reserved	7	R/W	0 1	Reserved		
Reserved	6	R/W	1	Reserved		
rxcom_sel	5:4	R/W	1	rx amplifier input common mode voltage: 2'b00=0.9V, 2'b01=0.95V(default), 2'b10=1V, 2'b11=1.05V		
rstb_z0	3	R/W	1	Reset 50 Ohm calibration		
z0_manual	2	R/W	0	Manual set 50 Ohm value		
en_vco_biasr	1	R/W	0	0:disable VCO bias R when processing FLD 1:enable VCO bias R when processing FLD		
vco_vc	0	R/W	0	Cp is controlled by vco_vc and cpSC(PageB CRA3[0]) cpSC=0, vco_vc =0 , Cp=0pF,		



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RTD2261W/2271W/2281W Series-GR

				cpsc=0,vco_vc =1 , Cp=0pF, cpsc=1,vco_vc =0 , Cp=2pF, cpsc=1,vco_vc =1 , Cp=1pF,	
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Register:: FLD_01					0XA5
Name	Bits	R/W	Default	Comments	Config
Reserved	7:5	--	0	RESERVED	
z0_tst	4:0	R	0	50 Ohm termination debug output	

Register:: FLD_02					0XA6
Name	Bits	R/W	Default	Comments	Config
offset_tst	7:3	R	0	OFFSET_TST<4:0>	
reserved	2:0		0		

Register::FLD_04					0xA8
Name	Bits	R/W	Default	Comments	Config
Reserved	7	R	0 1	Reserved	
data_rdy	6:4	R	0	CDR[2:0] Data Ready of Each Lane 0: unlock, 1:lock	
Reserved	3:2	R	0	RESERVED	
Reserved	1:0	R	0	Reserved	

Register::FLD_05					0XA9
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RTD2261W/2271W/2281W Series-GR

Name	Bits	R/W	Default	Comments	Config
bg_psm	7	R/W	0	bandgap power saving mode 1'b1=power saving mod	
loop_ok_in_regb	6	R/W	0	1'b0 = loop_ok =1 when manual mode	
Loop_f_sel	5	R/W	0	select output result of mode detect 0: no need FLD reset 1:need FLD reset	
vr_reg[3]	4	R/W	0	Reserved	
vr_reg[2:1]	3:2	R/W	3	reserved	
vr_reg[0]	1	R/W	1	Reserved	
reg_xtal_sel	0	R/W	1	1'b1= FLD xtal div 8 1'b0= FLD xtal no div	

Register::FLD_06 0XAA					
Name	Bits	R/W	Default	Comments	Config
reserved	7	R/W	0	reserved	
reserved	6:0	R/W	20	Reserved	

Register::FLD_07 0XAB					
Name	Bits	R/W	Default	Comments	Config
reserved	7:3	R/W	0	reserved	
reserved	2:0	R/W	2	reserved	

Register::FLD_08 0XAC					
Name	Bits	R/W	Default	Comments	Config
Reserved	7:6	R/W	0	Reserved	
Reserved	5	R/W	0	Reserved	
psm	4	R/W	0	1=CDR in power saving mode,only output ref clock	



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P1_Z0_EN	3:0	R/W	0	P1_Z0_EN[3:0] Port 1 50 Ohm enable 0 : disable 50 Ohm, 1 : 50 Ohm turn on	
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Register::FLD_09 0XAD					
Name	Bits	R/W	Default	Comments	Config
cdrcpop_en	7	R/W	0	1=enable CDR charge pump charge sharing OP	
eqcpop_en	6	R/W	0	1=enable EQ charge pump charge sharing OP	
sel_csop_in	5	R/W	0	0=CDR CP CSOP input from Rs 1=CDR CP CSOP input from Cs	
cp_adj_en	4	R/W	1	enable adjust charge pump current when tracking	
adp_eq_off	3	R/W	0	enable adaptive equalizer in the FLD auto mode	
adp_time	2:0	R/W	7	adaptive equalizer turn on time delay	

Register::RXMISC_01 0XAE					
Name	Bits	R/W	Default	Comments	Config
cpvref_sel	7:6	R/W	1	CDR CP CMFB Vref: 00: 0.55V, 01: 0.60V, 10: 0.65V, 11: 0.50V	
eqvref_sel	5:4	R/W	1	EQ CP Vref: 00: 0.55V, 01: 0.60V, 10: 0.65V, 11: 0.50V	
eqvc_selini	3	R/W	0	EQ VC initial value: 0: Vcp=Vcn, 1: Vcp-Vcn=0.2V	
eqvc_sel	2	R/W	0	0:select eq vc initial 0.2V 1: select eq vc initial -0.2V (only valid when 0xAE[3]=1)	
Reserved	1	R/W	0	Reserved	
sel_sync	0	R/W	1	Div5 & div2p5 out phase: 0: clock edge at middle point of data, 1:clock edge align with data edge	



Register::RXMISC_02					0XAF
Name	Bits	R/W	Default	Comments	Config
auto_mode	7	R/W	1	FLD auto mode: 0=manual, 1=auto set by FLD,	
Reserved	6	R/W	0	Reserved	
cp_en_manual	5	R/W	0	CP enable when auto_mode=0 1'b0=disable CP, 1'b1=manual enable CP	
band_RST	4	R/W	0	VCO band reset: 0=not reset when FLD detect unlock, 1=reset when FLD detect lock unlock	
calib_manual	3	R/W	0	data_rdy <= calib_manual when auto_mode=0	
calib_time	2:0	R/W	7	data_rdy output delay time <2:0>	

Register:: OOBS_RXAMP					0XB0
Name	Bits	R/W	Default	Comments	Config
reserved	7	R/W	0		
reserved	6:0	R/W	3F	reserved	

Register:: OOBS					0XB1
Name	Bits	R/W	Default	Comments	Config
reserved	7:6	R	0		
fld_st_lane1	5:3	R	0	fld_st_lane1[2:0]: lane1 FLD state	
fld_st_lane0	2:0	R	0	fld_st_lane0[2:0]: lane0 FLD state	



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Register:: A_EQ						0XB2
Name	Bits	R/W	Default	Comments		Config
adp_en_manual	7	R/W	0	Adaptive Equalizer hand mode enable when FLD auto_mode=0: 0: disable 1: enable		
koffset_en	6	R/W	1	Adaptive Equalizer offset calibration enable: 0: disable 1: enable		
offset_autom	5	R/W	1	Adaptive Equalizer offset calibration using auto mode: 0: disable 1: enable		
more_hpf	4:3	R/W	0 3	Adaptive Equalizer transfer function more like HPF: 00:weak...11:strong		
eqsc	2	R/W	1	Adaptive Equalizer Loop filter C: 0: 5p, 1: 10p		
eqcp_sel	1:0	R/W	2	Adaptive Equalizer Loop Charge Pump current: 00: 2.5u, 01: 7.5u, 10:5u(default), 11: 15u		

Register:: AUX_00						0XB3
Name	Bits	R/W	Default	Comments		Config
reserved	7:0	R/W	12	Reserved		

Register:: Power Control						0XB4
Name	Bits	R/W	Default	Comments		Config
cmu_en	7:4	R/W	0	CMU_EN[7:0], power control for VCO of lane3..0 0:disable 1:enable		
rx_en	3:0	R/W	0	RX_EN[3:0], power control for Rx channel 3..0, 0:disable 1:enable		

Register:: switch_2D						0XB5
Name	Bits	R/W	Default	Comments		Config
Reserved	7	R/W	0	RESERVED		
freqadd	6	R/W	0	1=VCO frequency shift up		



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freqsub	5	R/W	0	1=VCO frequency shift down	
reserved	4:3	R/W	0	reserved	
reserved	2	R/W	0	Reserved	
z0_autok	1	R/W	1	50 Ohm calibration 0: Register, 1: Auto-Calibration	
rstb_fsm	0	R/W	1	reset mode_det and FLD 0=reset,1=power on	

Register:: Z0 Calibration					0XB6
Name	Bits	R/W	Default	Comments	Config
Reserved	7:4	R/W	F	Reserved	
z0_adjr	3:0	R/W	8	z0_adjr[3:0] Manual Control for 50 ohm resistor	

Register:: CEC					0XB7
Name	Bits	R/W	Default	Comments	Config
Reserved	7:0	--	F0	Reserved	

Register:: AUX_01					0XB8
Name	Bits	R/W	Default	Comments	Config
Reserved	7	R/W	0	Reserved	
Reserved	6	R/W	1	Reserved	
Reserved	5	R/W	1	Reserved	
rev_reg[4:0]	4:0	R/W	1	Reserved	



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Register:: AUX_02					0XB9
Name	Bits	R/W	Default	Comments	Config
rev_reg[7:5]	7:5	R/W	1	Reserved	
reserved	4	R/W	0	Reserved	
reserved	3	R/W	0	Reserved	
reserved	2	R/W	0	Reserved	
reserved	1	R/W	0	Reserved	
Reserved	0	R/W	0	Reserved	

Register:: Reserved_00					0XBA
Name	Bits	R/W	Default	Comments	Config
offset_adjr	7:4	R/W	8	OFFSET_ADJR<3:0> set offset calibration value when offset_autom=0	
offset_idiv	3:2	R/W	0	Offset calibration current range: offset_idiv[1:0] 2'b00=+/-22.5u (default), 2'b01=+/-45u, 2'b10=+/-45u, 2'b11=+/-90u,	
bypass_ok	1	R/W	0	bypass calibration ok signal 1'b1=bypass, 1'b0=auto use calibration ok (default)	
entst	0	R/W	0	enable EQ amp test mode	

Register:: Reserved_01					0XBB
Name	Bits	R/W	Default	Comments	Config
bg_en	7	R/W	1	BG_EN	
bg_db	6:4	R/W	2 4	3'b000=1.184V, 3'b001=1.195V, 3'b010=1.201V 3'b011=1.206V, 3'b100=1.212V, 3'b101=1.217V 3'b110=1.223V, 3'b111=1.228V,	
reserved	5 3		0 1	reserved	
reserved	2	R/W	0	reserved	
reserved	1	R/W	0	reserved	



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RTD2261W/2271W/2281W Series-GR

reserved	0	R/W	1	reserved	
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Register:: Reserved_02					0XBC
Name	Bits	R/W	Default	Comments	Config
Reserved	7	R/W	0	reserved	
Reserved	6	R/W	0	Reserved	
Reserved	5:0	--	0	RESERVED	

Register:: Reserved_03					0XBD
Name	Bits	R/W	Default	Comments	Config
Reserved	7:6	--	0	RESERVED	
Reserved	5:0	R	0	reserved	

Register:: Reserved_04					0XBE
Name	Bits	R/W	Default	Comments	Config
Reserved	7:6	--	0	RESERVED	
Reserved	5:0	R	0	Reserved	

Register:: Reserved_05					0XBF
Name	Bits	R/W	Default	Comments	Config
vdc16_sel	7:6	R/W	1	Select inductive peaking bias voltage 2'b00=1.5V 2'b01=1.6V (default) 2'b10=1.7V 2'b11=1.8V	
en_peak	5:4	R/W	3	en_peak[1:0] Enable equalizer inductive peaking amplifier: En_peak[0]:enable summing stage En_peak[1]:enable boost stage (1: enable, 0: disable)	



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reserved	3	R/W	0	reserved	
sel_vp	2	R/W	0	1'b0=inductive peaking bias voltage from IR 1'b1=inductive peaking bias voltage from replica bias*1/gm	
adppeak_sel	1:0	R/W	1	inductive peaking CML replica bias voltage selection. 2'b00=0.85V 2'b01=0.895V (default) 2'b10=0.94V 2'b11=0.985V	

Register:: CMU_00					0XC0
Name	Bits	R/W	Default	Comments	Config
reserved	7	R/W	1	Reserved	
reserved	6	R/W	0	Reserved	
reserved	5	R/W	0	Reserved	
reserved	4	R/W	0	Reserved	
reserved	3	R/W	0	reserved	
reserved	2:0	R/W	0		

Register:: CMU_01					0XC1
Name	Bits	R/W	Default	Comments	Config
reserved	7:0	R/W	DA	Reserved	

Register:: CMU_02					0XC2
Name	Bits	R/W	Default	Comments	Config
reserved	7:0	R/W	ED	Reserved	

Register:: CMU_03					0XC3
Name	Bits	R/W	Default	Comments	Config
reserved	7:0	R/W	76	Reserved	



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Register:: CMU_04

0XC4

Name	Bits	R/W	Default	Comments	Config
reserved	7:0	R/W	3B	Reserved	

Register:: CMU_05

0XC5

Name	Bits	R/W	Default	Comments	Config
reserved	7:0	--	18	Reserved	

Register:: CMU_06

0XC6

Name	Bits	R/W	Default	Comments	Config
reserved	7	R/W	0		
reserved	6:0	R/W	0		

Register:: CMU_07

0XC7

Name	Bits	R/W	Default	Comments	Config
fld_cdr_cont0[8]	7	R/W	1	fld_cdr_cont0[8]	
fld_ref_cont0[8]	6	R/W	1	fld_ref_cont0[8]	
reserved	5	R/W	0	reserved	
fld_cdr_delta	4:0	R/W	5	fld_cdr_delta	

Register:: CMU_08_cal

0XC8

Name	Bits	R/W	Default	Comments	Config
fld_cdr_cont0[7:0]	7:0	R/W	40	fld_cdr_cont0[7:0]	

Register:: TX

0XC9

Name	Bits	R/W	Default	Comments	Config
fld_ref_cont0[7:0]	7:0	R/W	40	fld_ref_cont0[7:0]	



Register:: SSCG					0XCA
Name	Bits	R/W	Default	Comments	Config
reserved	7	R	0	reserved	
dfvco_lane0	6:0	R	0	Bit[6:0] dfvco_lane0[6:0]: lane0 VCO auto calibration result	

Register:: TX Z0 Calibration					0XCB
Name	Bits	R/W	Default	Comments	Config
reserved	7	R	0	reserved	
dfvco_lane1	6:0	R	0	Bit[6:0] dfvco_lane1[6:0]: lane1 VCO auto calibration result	

Register:: Reserved_06					0XCC
Name	Bits	R/W	Default	Comments	Config
SAMPLE	7:4	R/W	0	SAMPLE edge selector of each lane 0:positive clock edge of CDR(PHY) clock 1:negative clock edge of CDR(PHY) clock	
REG_PN_SWAP	3:0	R/W	0	Inverse 10-bit CDR data of each lane swap pn to avoid pn mismatch (physical lane) 0: not inverse 1: inverse	

Register:: Reserved_07					0XCD
Name	Bits	R/W	Default	Comments	Config
LANE_MUX_SEL	7:0	R/W	E4	select the data mapping between physical lane and MAC lane [7:6]: lane3 data/ck1x/ck2x/pn_swap comes from physical lane # 2'b00: physical lane0 2'b01: physical lane1	



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				<p>2'b10: physical lane2</p> <p>2'b11: physical lane3 (default)</p> <p>[5:4]: lane2 data/ck1x/ck2x/pn_swap comes from physical lane #</p> <p>2'b00: physical lane0</p> <p>2'b01: physical lane1</p> <p>2'b10: physical lane2 (default)</p> <p>2'b11: physical lane3</p> <p>[3:2]: lane1 data/ck1x/ck2x/pn_swap comes from physical lane #</p> <p>2'b00: physical lane0</p> <p>2'b01: physical lane1 (default)</p> <p>2'b10: physical lane2</p> <p>2'b11: physical lane3</p> <p>[1:0]: lane0 data/ck1x/ck2x/pn_swap comes from physical lane #</p> <p>2'b00: physical lane0 (default)</p> <p>2'b01: physical lane1</p> <p>2'b10: physical lane2</p> <p>2'b11: physical lane3</p>	
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Register:: Reserved_08					0xCE
Name	Bits	R/W	Default	Comments	Config
reserved	7	R	1	reserved	
Reserved	6:0	R	70	reserved	

Register:: Reserved_09					0xCF
Name	Bits	R/W	Default	Comments	Config
reserved	7	R	1	reserved	
Reserved	6:0	R	70	reserved	

Register:: RXBIST_00					0XD0
Name	Bits	R/W	Default	Comments	Config



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reserved	7	R/W	0 1	reserved	
reserved	6	R/W	0 1	reserved	
reserved	5	R/W	0 1	reserved	
reserved	4	R/W	0 1	reserved	
Reserved	3:0	R/W	F	reserved	

Register:: RXBIST_01					0XD1
Name	Bits	R/W	Default	Comments	Config
reserved	7:0	R/W	E0		

Register:: RXBIST_02					0XD2
Name	Bits	R/W	Default	Comments	Config
reserved	7:0	R/W	FF		

Register:: RXBIST_03					0XD3
Name	Bits	R/W	Default	Comments	Config
reserved	7:0	R/W	A0		

Register:: RXBIST_04					0XD4
Name	Bits	R/W	Default	Comments	Config
reserved	7:0	R/W	5F		

Register:: RXBIST_05					0XD5
Name	Bits	R/W	Default	Comments	Config
reserved	7	R/W	0		



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reserved	6	R/W	0		
reserved	5	R/W	0		
reserved	4:0	R/W	0		

Register:: TXBIST_00					0XD6
Name	Bits	R/W	Default	Comments	Config
reserved	7	R/W	0		
reserved	6	R/W	0		
reserved	5	R/W	0		
reserved	4	R/W	0		
reserved	3	R/W	0		
reserved	2:0	R/W	0		

Register:: TXBIST_01					0XD7
Name	Bits	R/W	Default	Comments	Config
reserved	7:0	R/W	00		

Register:: TXBIST_02					0XD8
Name	Bits	R/W	Default	Comments	Config
reserved	7:0	R/W	00		

Register:: TXBIST_03					0XD9
Name	Bits	R/W	Default	Comments	Config
reserved	7:0	R/W	00		



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Register:: TXBIST_04						0XDA
Name	Bits	R/W	Default	Comments		Config
Reserved	7	R/W	0			
rfvco_lane1	6:0	R/W	3F	rfvco_lane1<6:0> lane1 VCO band manual selection=0~127		

Register:: TXBIST_05						0xDB
Name	Bits	R/W	Default	Comments		Config
reserved	7	R/W	0			
rfvco_lane2	6:0	R/W	3F	rfvco_lane2<6:0> lane2 VCO band manual selection=0~127		

Register:: TXBIST_06						0xDC
Name	Bits	R/W	Default	Comments		Config
Reserved	7:4	R	0			
fld_st_lane2	3:1	R	0	fld_st_lane2<2:0> Lane2 FLD state		
Reserved	0	R	0	Reserved		

Register:: TXBIST_07						0xDD
Name	Bits	R/W	Default	Comments		Config
reserved	7:0	R	0			

Register:: TXBIST_08						0xDE
Name	Bits	R/W	Default	Comments		Config
Reserved	7	R	0			
dfvco_lane2	6:0	R	0	dfvco_lane2<6:0> lane2 VCO auto calibration result		



Register:: TXBIST_09					0xDF
Name	Bits	R/W	Default	Comments	Config
reserved	7	R	0	reserved	
reserved	6:0	R/W	0	reserved	

Register:: DIG_00					0xE0
Name	Bits	R/W	Default	Comments	Config
CTL_SEL	7	R/W	1	CTL_SEL, select primary control signal 0:from primary input(gdi) 1:from SI (page B register)	
SI_X1X2_SEL	6	R/W	1	Interface clock rate selector 0:16 bits 1:8 bits	
SI_ENCH_MODE	5	R/W	0	reserved	
SI_HD_DP_SEL	4	R/W	1	HDMI/DP selector 0: DP, 1: HDMI	
HDMI_X4_SEL	3:0	R/W	0	HDMI clock divided by 4 mode 0: disable 1: enable	

Register:: DIG_01					0xE1
Name	Bits	R/W	Default	Comments	Config
DP_CLK_INV	7:4	R/W	0	DP_CLK_INV, inverse dp_clk clock of each lane	
DP_CLKX2_INV	3:0	R/W	0	DP_CLKX2_INV, inverse dp_clkx2 clock of each lane	

Register:: DIG_02					0xE2
Name	Bits	R/W	Default	Comments	Config
DIG_02	7:0	R/W	00	Bit [7]: reserved Bit [6]: reserved Bit [5:3]: reserved	



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			Bit [2]: PRBS_REVERSE, reverse PRBS7 pattern generator 0: disable 1: enable Bit[1:0]: reserved	
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Register:: DIG_03					0xE3
Name	Bits	R/W	Default	Comments	Config
DIG_03	7:0	R/W	00	Bit [7]: error count clear 1'b0: disable 1'b1: enable Bit [6:5]: RXBIST_SOURCE, rx bist source selection 2'b00: from PMA(normal function) 2'b01: from comdet input 2'b10: reserved 2'b11: reserved Bit [4:3]: RXBIST_DEST, rx bist destination selection 2'b00: disable rxbist 2'b01: to comdet output 2'b10: reserved 2'b11: reserved Bit [2]: PRBS_SEL, prbs pattern selection 1'b0: prbs 7 1'b1: prbs31 Bit [1:0]: reserved	

Register:: DIG_04					0xE4
Name	Bits	R/W	Default	Comments	Config
DIG_04	7:0	R/W	00	reserved	

Register:: DIG_05					0xE5
Name	Bits	R/W	Default	Comments	Config
DIG_05	7:0	R/W	00	RX digital debug, select debug bus Bit[6:5]: debug sel 00: rxbist_err_cnt0 01: rxbist_err_cnt1	



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				10: rxbist_err_cnt2 11: rxbist_err_cnt3 Bit[4:0]: reserved 6093: Bit [7:0]: RX digital debug	
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Register:: DIG_06 0xE6					
Name	Bits	R/W	Default	Comments	Config
DIG_06	7:0	R	00	gdi_logic0_bus 6093: Bit [7:0]: BYTE_COUNT[15:8], received packet number	

Register:: DIG_07 0xE7					
Name	Bits	R/W	Default	Comments	Config
DIG_07	7:0	R	00	gdi_logic0_bus 6093: Bit [7:0]: BYTE_COUNT[7:0], received packet number	

Register:: DIG_08 0xE8					
Name	Bits	R/W	Default	Comments	Config
RXBIST_ERR_CNT	7:0	R	00	Bit [7:0], RXBIST_ERR_CNT, received error counter The selection of RXBIST_ERR_CNT is determined by 0xE5[6:5].	

Register:: SSCG_DIG 0xE9					
Name	Bits	R/W	Default	Comments	Config
SSCG_DIG	7:0	R/W	00	Bit[7:0]: reserved	



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Register:: DIG_TX_00 0xEA					
Name	Bits	R/W	Default	Comments	Config
DIG_TX_00	7:0	R/W	00	Bit[7:0]: reserved	

Register:: DIG_TX_01 0xEB					
Name	Bits	R/W	Default	Comments	Config
DIG_TX_01	7:0	R/W	00	Bit [7:0]: reserved	

Register:: DIG_TX_02 0xEC					
Name	Bits	R/W	Default	Comments	Config
DIG_TX_02	7:0	R/W	00	Bit [7:0]: reserved	

Register:: DIG_TX_03 0xED					
Name	Bits	R/W	Default	Comments	Config
DIG_TX_03	7:0	R/W	00	Bit [7:0]: reserved	

Register:: Reserved_0A 0xEF					
Name	Bits	R/W	Default	Comments	Config
Reserved_0A	7:0	R/W	FF	Bit [7:0]: reserved	

Register:: Reserved_0B 0xF0					
Name	Bits	R/W	Default	Comments	Config
Reserved_0B	7:0	R/W	F0	reserved	

Register:: Reserved_0C 0xF1					
Name	Bits	R/W	Default	Comments	Config
Reserved_0C	7:0	R/W	F0	reserved	



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Register:: Reserved_0D					0xF2
Name	Bits	R/W	Default	Comments	Config
Reserved_0D	7:0	R/W	F0	reserved	

Register:: Reserved_0E					0xF3
Name	Bits	R/W	Default	Comments	Config
Reserved_0E	7:0	R/W	F0	reserved	

Register:: Reserved_0F					0xF4
Name	Bits	R/W	Default	Comments	Config
Reserved_0F	7:0	R/W	F0	reserved	

Register:: DEBUG_SEL					0xF5
Name	Bits	R/W	Default	Comments	Config
phy_debug_sel	7	R/W	0	The selection of PHY debug signal 0: debug_fld_lane0 1: debug_fld_lane1	
reserved	6:0	--	0	reserved	

Register:: LVDS_MODE					0xF6
Name	Bits	R/W	Default	Comments	Config
BG_PSM_SEL	7	R/W	0	The selection of bg_psm to analog PHY 0: original mode: depend on 0xA9[7] 1: New mode: when lvds_ibpowl = 1, bg_psm = 0; when lvds_ibpowl = 0, bg_psm = 0xA9[7]	



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BG_EN_SEL	6	R/W	0	The selection of bg_en to analog PHY 0: original mode: depend on 0xBB[7] 1: New mode: when lvds_ibpowl = 1, bg_en = 1; when lvds_ibpowl = 0, bg_en = 0xBB[7]	
BG_DB_SEL	5	R/W	0	The selection of bg_db to analog PHY 0: original mode: depend on 0xBB[6:4] 1: New mode: when lvds_ibpowl = 1, bg_db= 3'b100; when lvds_ibpowl = 0, bg_db = 0xBB[6:4]	
LVDS_RSV	4:0	R/W	0	Reserved	

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GDI MAC (Page C)
MAC CONTROL

Register:: DP_CTRL 0xA1					
Name	Bits	R/W	Default	Comments	Config
RESERVED	7:6	--	1	reserved	
HD_DP_SEL	5	R/W	1	HDMI/DisplayPort Seletor 0: DisplayPort 1: HDMI	
RESERVED	4:0	---	18	reserved	

Register:: DP_DEBUG_SEL0 0xB5					
Name	Bits	R/W	Default	Comments	Config
PHY_DBG_EN	7	R/W	0	Enable phy test output. 0: test hdmi 1: test phy	
RESERVED	6:0	---	0	reserved	

Register:: DP_GPI_FUNCTION 0xBA					
Name	Bits	R/W	Default	Comments	Config
Reserved	7:0	R/W	0	Reserved	

Register:: DP_RESERVE1 0xBB					
Name	Bits	R/W	Default	Comments	Config
Reserved	7	R/W	0	Reserved	
RESERVED	6:0	--	0	Reserved	

Register:: DP_HDCP_BIST 0xE9					
Name	Bits	R/W	Default	Comments	Config
RSV_E4_7_3	7:3	R/W	0	Reserved	
HDCP_BIST_MODE	2	R/W	0	BIST ENABLE.	
HDCP_BIST_DONE	1	R	0	BIST IS DONE.	
HDCP_BIST_FAIL_0	0	R	0	Active when BIST_DONE = 1. 1: BIST Fail. 0: BIST success.	

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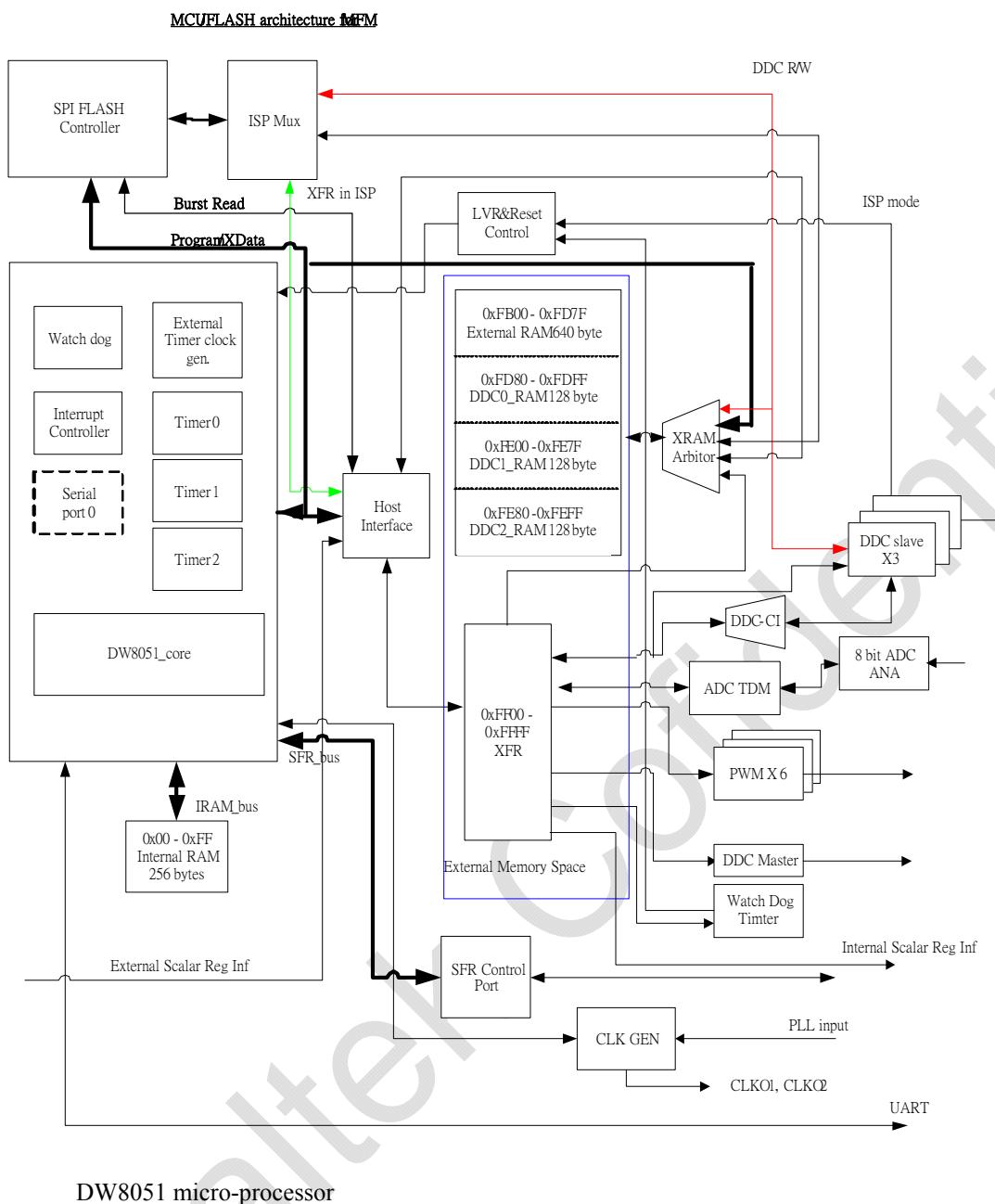
MCU register 1(page D)

Embedded MCU Function

Designware DW8051 of Synopsys is integrated into this chip and is compatible with other industry 8051 series. A lot of peripherals are integrated and accessed by XFR (eXternal Function Register). When embedded MCU is used, scalar-related registers are access via XFR, too. The program code is stored in external serial FLASH. If the external MCU is used, the integrated peripherals can be accessed via special page in scalar's register map.

Features

- 8051 core, CPU operating frequency up to 50MHz
- 256-byte IRAM, 256~1024 byte shared XRAM
- external serial FLASH, support GPIO bank switching for 128K byte and up to 16M bytes for XFR bank switching
- Compliant with VESA DDC1/2B/2Bi/CI
- Embedded triple ports DDC RAM(0~768 bytes shared with XRAM)
- Six channels of PWM DAC
- Watchdog timer with programmable interval
- Three 16-bit counters/timers (T0, T1, and ET2)
- Programmable frequency clock output, 2 clock output ports
- One full-duplex serial port
- Six interrupt sources with 2 external interrupts
- Four channels of 8-bit ADC
- Hardware ISP, no boot code required
- Built-in Low voltage reset circuit



The DW8051 is compatible with industry standard 803x/805x and provides the following design features and enhancements to the standard 8051 microcontroller:

High speed architecture

Compared to standard 8051, the DW8051 processor core provides increased performance by executing instructions in a 4-clock bus cycle, as opposed to the 12-clock bus cycle in the standard 8051. The shortened bus timing improves the instruction execution rate for most instructions by a factor of three over the standard 8051 architectures. The average speed improvement for the entire instruction set is



approximately 2.5X.

Stretch Memory Cycles

The stretch memory cycle feature enables application software to adjust the speed of data memory access. The DW8051 can execute the MOVX instruction in as little as 2 instruction cycles. However, it is sometimes desirable to stretch this value; for example, to access slow memory or slow memory-mapped peripherals such as UARTs or LCDs.

The three LSBs of the Clock Control Register (at SFR location 8Eh) control the stretch value. You can use stretch values between zero and seven. A stretch value of zero adds zero instruction cycles, resulting in MOVX instructions executing in two instruction cycles. A stretch value of seven adds seven instruction cycles, resulting in MOVX instructions executing in nine instruction cycles. The stretch value can be changed dynamically under program control.

By default, the stretch value resets to one (three cycle MOVX). For full-speed data memory access, the software must set the stretch value to zero. The stretch value affects only data memory access. The only way to reduce the speed of program memory (ROM) access is to use a slower clock.

Dual Data Pointers

The DW8051 employs dual data pointers to accelerate data memory block moves. The standard 8051 data pointer (DPTR) is a 16-bit value used to address external data RAM or peripherals. The DW8051 maintains the standard data pointer as DPTR0 at SFR locations 82h and 83h. It is not necessary to modify code to use DPTR0.

The DW8051 adds a second data pointer (DPTR1) at SFR locations 84h and 85h. The SEL bit in the DPTR Select register, DPS (SFR 86h), selects the active pointer. When SEL = 0, instructions that use the DPTR will use DPL0 and DPH0. When SEL = 1, instructions that use the DPTR will use DPL1 and DPH1. SEL is the bit 0 of SFR location 86h. No other bits of SFR location 86h are used.

All DPTR-related instructions use the currently selected data pointer. To switch the active pointer, toggle the SEL bit. The fastest way to do so is to use the increment instruction (INC DPS). This requires only one instruction to switch from a source address to a destination address, saving application code from having to save source and destination addresses when doing a block move.

Using dual data pointers provides significantly increased efficiency when moving large blocks of data.

Timer Rate Control

One important difference exists between the DW8051 and 80C32 regarding timers. The original 80C32 used a 12 clock per cycle scheme for timers and consequently for some serial baud



rates(depending on the mode). The DW8051 architecture normally runs using 4 clocks per cycle. However, in the area of timers, it will default to a 12 clock per cycle scheme on a reset. This allows existing code with real-time dependencies such as baud rates to operate properly. If an application needs higher speed timers or serial baud rates, the timers can be set to run at the 4 clock rate.

The Clock Control register (CKCON – 8Eh) determines these timer speeds. When the relevant CKCON bit is a logic 1, the device uses 4 clocks per cycle to generate timer speeds. When the control bit is set to a zero, the device uses 12 clocks for timer speeds. The reset condition is a 0. CKCON.5 selects the speed of Timer 2. CKCON.4 selects Timer 1 and CKCON.3 selects Timer zero. Note that unless a user desires very fast timing, it is unnecessary to alter these bits. Note that the timer controls are independent.

RESET

There are five reset sources.

- RST pin
The external reset is high active and its pulse width must be larger than 8 clock cycles. The RST pin can reset the DW8051
- Low voltage reset(LVR) and power on reset(POR)
- Software can use SOF_RST register to reset whole chip
- Watchdog can reset DW8051
- When entering ISP mode, DW8051 will be in reset state. When exiting ISP mode, DW8051 will also assert a reset, too.

Special Function Registers

Register	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Addr
SP									81h
DPL0									82h
DPH0									83h
DPL1									84h
DPH1									85h
DPS	0	0	0	0	0	0	0	SEL	86h
PCON	SMOD 0		1	1	GF1	GF0	STOP	IDLE	87h
TCON	TF1	TR1	TF0	TR0	IE1	IT1	IE0	IT0	88h
TMOD	GATE	C/T	M1	M0	GATE	C/T	M1	M0	89h



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TL0									8Ah
TL1									8Bh
TH0									8Ch
TH1									8Dh
CKCON			T2M	T1M	T0M	MD2	MD1	MD0	8Eh
SPC_FNC	0	0	0	0	0	0	0	WRS	8Fh
P1_W	P1.7	P1.6	P1.5	P1.4	P1.3	P1.2	P1.1	P1.0	90h
MPAGE									92h
P1_R	P1.7	P1.6	P1.5	P1.4	P1.3	P1.2	P1.1	P1.0	93h
SCON0	SM0	SM1	SM2	REN	TB8	RB8	TI	RI	98h
SBUF0									99h
P2	P2.7	P2.6	P2.5	P2.4	P2.3	P2.2	P2.1	P2.0	A0h
IE	EA	0	ET2	ES0	ET1	EX1	ET0	EX0	A8h
P3_W	P3.7	P3.6	P3.5	P3.4	P3.3	P3.2	P3.1	P3.0	B0h
P3_R	P3.7	P3.6	P3.5	P3.4	P3.3	P3.2	P3.1	P3.0	B3h
IP	1	0	PT2	PS0	PT1	PX1	PT0	PX0	B8h
T2CON	TF2	EXF2	RCLK	TCLK	EXEN2	TR2	C/T2	CP/ RL2	C8h
RCAP2L									CAh
RCAP2H									CBh
TL2									CCh
TH2									CDh
PSW	CY	AC	F0	RS1	RS0	OV	F1	P	D0h
ACC									E0h
B									F0h

SFR reset value

Register	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Addr
SP	0	0	0	0	0	1	1	1	81h
DPL0	0	0	0	0	0	0	0	0	82h
DPH0	0	0	0	0	0	0	0	0	83h



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DPL1	0	0	0	0	0	0	0	0	84h
DPH1	0	0	0	0	0	0	0	0	85h
DPS	0	0	0	0	0	0	0	0	86h
PCON	0	0	1	1	0	0	0	0	87h
TCON	0	0	0	0	0	0	0	0	88h
TMOD	0	0	0	0	0	0	0	0	89h
TL0	0	0	0	0	0	0	0	0	8Ah
TL1	0	0	0	0	0	0	0	0	8Bh
TH0	0	0	0	0	0	0	0	0	8Ch
TH1	0	0	0	0	0	0	0	0	8Dh
CKCON	0	0	0	0	0	0	0	1	8Eh
SPC_FNC	0	0	0	0	0	0	0	0	8Fh
P1_W	1	1	1	1	1	1	1	1	90h
MPAGE	0	0	0	0	0	0	0	0	92h
SCON0	0	0	0	0	0	0	0	0	98h
SBUF0	0	0	0	0	0	0	0	0	99h
P2	0	0	0	0	0	0	0	0	A0h
IE	0	0	0	0	0	0	0	0	A8h
P3_W	1	1	1	1	1	1	1	1	B0h
IP	1	0	0	0	0	0	0	0	B8h
T2CON	0	0	0	0	0	0	0	0	C8h
RCAP2L	0	0	0	0	0	0	0	0	CAh
RCAP2H	0	0	0	0	0	0	0	0	CBh
TL2	0	0	0	0	0	0	0	0	CCh
TH2	0	0	0	0	0	0	0	0	CDh
PSW	0	0	0	0	0	0	0	0	D0h
ACC	0	0	0	0	0	0	0	0	E0h
B	0	0	0	0	0	0	0	0	F0h

DW8051 user-modifiable parameters

ram_256	1
timer2	1
rom_addr_size	0
Serial	1
extd_intr	0



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REG_XFR_WRAPPER is the eXternal Function Register defined in 0xFF00 ~ 0xFFFF in DW8051's XDATA memory space. There are three possible input sources for REG_XFR_WRAPPER. In embedded MCU mode, DW8051 has the power of control.

	PAGE D						PAGE E						PAGE F			
	A	B	C	D	E	F	A	B	C	D	E	F	A	B	C	D
0xFFXX	0X	1X	2X	3X	4X	5X	6X	7X	8X	9X	AX	BX	CX	DX	EX	FX
X0	IRQ		ADC_DDC	DDC-CI	PWM	PWM	SPI-FLASH	SPI-FLASH		PWM	GPIO		GPIO	GPIO	GPIO	SPI_WP
X1	IRQ		ADC_DDC	DDC-CI	PWM	PWM	SPI-FLASH	SPI-FLASH		PWM	GPIO		GPIO	GPIO	GPIO	
X2	Dummy		VSYNC_Sel	DDC-CI	PWM	PWM	SPI-FLASH	SPI-FLASH		PWM	GPIO		GPIO	GPIO	SFR	Dummy
X3	OSD turbo		DDC-CI	DDC-CI	PWM	PWM	SPI-FLASH	SPI-FLASH	I2C	PWM	GPIO		GPIO	GPIO	SFR	SCA
X4	OSD turbo		DDC-CI	DDC-CI	PWM	PWM	SPI-FLASH	SPI-FLASH	I2C	PWM	GPIO		GPIO	GPIO		SCA
X5	OSD turbo		DDC-CI	DDC-CI	PWM	I2C	SPI-FLASH	SPI-FLASH	I2C	PWM	Flash		GPIO	GPIO		SCA
X6	OSD turbo		DDC-CI	PWM	PWM	I2C	SPI-FLASH	SPI-FLASH	I2C	PWM	Flash		GPIO	GPIO	GPIO	SCA
X7	OSD turbo		DDC-CI	PWM	PWM	I2C	SPI-FLASH	GPIO	I2C	PWM	Flash		GPIO	GPIO	CEC	SCA
X8	ADC turbo	OSD	DDC-CI	PWM	PWM	I2C	SPI-FLASH	GPIO	I2C	PWM	Flash		GPIO	GPIO	CEC	SCA
X9	ADC	ADC_DDC	DDC-CI	PWM	PWM	I2C	SPI-FLASH	GPIO	GPIO	PWM	Flash		GPIO	GPIO	Dummy	SCA
XA	ADC	ADC_DDC	DDC-CI	PWM	PWM	I2C	SPI-FLASH	GPIO	GPIO	PWM	CEC		GPIO	GPIO	WD	SCA
XB	ADC	ADC_DDC	DDC-CI	PWM	PWM	I2C	SPI-FLASH	GPIO	GPIO	PWM			GPIO	GPIO	WD	SCA
XC	ADC	ADC_DDC	DDC-CI	PWM	PWM	I2C	SPI-FLASH	GPIO	GPIO	PWM			GPIO	GPIO	ISP	Bank-Switch
XD	ADC	ADC_DDC	DDC-CI	PWM	PWM	I2C	SPI-FLASH	GPIO	GPIO	Flash			GPIO	GPIO	ISP	Bank-Switch
XE		ADC_DDC	DDC-CI	PWM	PWM	I2C	SPI-FLASH	GPIO	GPIO	Flash			GPIO	GPIO	ISP	Bank-Switch
XF		ADC_DDC	DDC-CI	PWM	PWM	I2C	SPI-FLASH	GPIO	GPIO	Flash			GPIO	GPIO	ISP	Bank-Switch



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0xFF00	(Page D) 0xA0	0xFF10	(Page D) 0xB0	0xFF20	(Page D) 0xC0	0xFF30	(Page D) 0xD0	0xFF40	(Page D) 0xE0	0xFF50	(Page D) 0xF0
0xFF01	(Page D) 0xA1	0xFF11	(Page D) 0xB1	0xFF21	(Page D) 0xC1	0xFF31	(Page D) 0xD1	0xFF41	(Page D) 0xE1	0xFF51	(Page D) 0xF1
0xFF02	(Page D) 0xA2	0xFF12	(Page D) 0xB2	0xFF22	(Page D) 0xC2	0xFF32	(Page D) 0xD2	0xFF42	(Page D) 0xE2	0xFF52	(Page D) 0xF2
0xFF03	(Page D) 0xA3	0xFF13	(Page D) 0xB3	0xFF23	(Page D) 0xC3	0xFF33	(Page D) 0xD3	0xFF43	(Page D) 0xE3	0xFF53	(Page D) 0xF3
0xFF04	(Page D) 0xA4	0xFF14	(Page D) 0xB4	0xFF24	(Page D) 0xC4	0xFF34	(Page D) 0xD4	0xFF44	(Page D) 0xE4	0xFF54	(Page D) 0xF4
0xFF05	(Page D) 0xA5	0xFF15	(Page D) 0xB5	0xFF25	(Page D) 0xC5	0xFF35	(Page D) 0xD5	0xFF45	(Page D) 0xE5	0xFF55	(Page D) 0xF5
0xFF06	(Page D) 0xA6	0xFF16	(Page D) 0xB6	0xFF26	(Page D) 0xC6	0xFF36	(Page D) 0xD6	0xFF46	(Page D) 0xE6	0xFF56	(Page D) 0xF6
0xFF07	(Page D) 0xA7	0xFF17	(Page D) 0xB7	0xFF27	(Page D) 0xC7	0xFF37	(Page D) 0xD7	0xFF47	(Page D) 0xE7	0xFF57	(Page D) 0xF7
0xFF08	(Page D) 0xA8	0xFF18	(Page D) 0xB8	0xFF28	(Page D) 0xC8	0xFF38	(Page D) 0xD8	0xFF48	(Page D) 0xE8	0xFF58	(Page D) 0xF8
0xFF09	(Page D) 0xA9	0xFF19	(Page D) 0xB9	0xFF29	(Page D) 0xC9	0xFF39	(Page D) 0xD9	0xFF49	(Page D) 0xE9	0xFF59	(Page D) 0xF9
0xFF0A	(Page D) 0xAA	0xFF1A	(Page D) 0xBA	0xFF2A	(Page D) 0xCA	0xFF3A	(Page D) 0xDA	0xFF4A	(Page D) 0xEA	0xFF5A	(Page D) 0xFA
0xFF0B	(Page D) 0xAB	0xFF2B	(Page D) 0xBB	0xFF2B	(Page D) 0xCB	0xFF3B	(Page D) 0xDB	0xFF4B	(Page D) 0xEB	0xFF5B	(Page D) 0xFB
0xFF0C	(Page D) 0xAC	0xFF1C	(Page D) 0xBC	0xFF2C	(Page D) 0xCC	0xFF3C	(Page D) 0xDC	0xFF4C	(Page D) 0xEC	0xFF5C	(Page D) 0xFC
0xFF0D	(Page D) 0xAD	0xFF1D	(Page D) 0xBD	0xFF2D	(Page D) 0xCD	0xFF3D	(Page D) 1xDD	0xFF4D	(Page D) 0xED	0xFF5D	(Page D) 0xFD
0xFF0E	(Page D) 0xAE	0xFF1E	(Page D) 0xBE	0xFF2E	(Page D) 0xCE	0xFF3E	(Page D) 2xDE	0xFF4E	(Page D) 0xEE	0xFF5E	(Page D) 0xFE
0xFF0F	(Page D) 0xAF	0xFF1F	(Page D) 0xBF	0xFF2F	(Page D) 0xCF	0xFF3F	(Page D) 2xFD	0xFF4F	(Page D) 0xEF	0xFF5F	(Page D) 0xFF

0xFF60	(Page E) 0xA0	0xFF70	(Page E) 0xB0	0xFF80	(Page E) 0xC0	0xFF90	(Page E) 0xD0	0xFFA0	(Page E) 0xE0	0xFFB0	(Page E) 0xF0
0xFF61	(Page E) 0xA1	0xFF71	(Page E) 0xB1	0xFF81	(Page E) 0xC1	0xFF91	(Page E) 0xD1	0xFFA1	(Page E) 0xE1	0xFFB1	(Page E) 0xF1
0xFF62	(Page E) 0xA2	0xFF72	(Page E) 0xB2	0xFF82	(Page E) 0xC2	0xFF92	(Page E) 0xD2	0xFFA2	(Page E) 0xE2	0xFFB2	(Page E) 0xF2
0xFF63	(Page E) 0xA3	0xFF73	(Page E) 0xB3	0xFF83	(Page E) 0xC3	0xFF93	(Page E) 0xD3	0xFFA3	(Page E) 0xE3	0xFFB3	(Page E) 0xF3
0xFF64	(Page E) 0xA4	0xFF74	(Page E) 0xB4	0xFF84	(Page E) 0xC4	0xFF94	(Page E) 0xD4	0xFFA4	(Page E) 0xE4	0xFFB4	(Page E) 0xF4
0xFF65	(Page E) 0xA5	0xFF75	(Page E) 0xB5	0xFF85	(Page E) 0xC5	0xFF95	(Page E) 0xD5	0xFFA5	(Page E) 0xE5	0xFFB5	(Page E) 0xF5
0xFF66	(Page E) 0xA6	0xFF76	(Page E) 0xB6	0xFF86	(Page E) 0xC6	0xFF96	(Page E) 0xD6	0xFFA6	(Page E) 0xE6	0xFFB6	(Page E) 0xF6
0xFF67	(Page E) 0xA7	0xFF77	(Page E) 0xB7	0xFF87	(Page E) 0xC7	0xFF97	(Page E) 0xD7	0xFFA7	(Page E) 0xE7	0xFFB7	(Page E) 0xF7
0xFF68	(Page E) 0xA8	0xFF78	(Page E) 0xB8	0xFF88	(Page E) 0xC8	0xFF98	(Page E) 0xD8	0xFFA8	(Page E) 0xE8	0xFFB8	(Page E) 0xF8
0xFF69	(Page E) 0xA9	0xFF79	(Page E) 0xB9	0xFF89	(Page E) 0xC9	0xFF99	(Page E) 0xD9	0xFFA9	(Page E) 0xE9	0xFFB9	(Page E) 0xF9
0xFF6A	(Page E) 0xAA	0xFF7A	(Page E) 0xBA	0xFF8A	(Page E) 0xCA	0xFF9A	(Page E) 0xDA	0xFFAA	(Page E) 0xEA	0xFFBA	(Page E) 0xFA
0xFF6B	(Page E) 0xAB	0xFF7B	(Page E) 0xBB	0xFF8B	(Page E) 0xCB	0xFF9B	(Page E) 0xDB	0xFFAB	(Page E) 0xEB	0xFFBB	(Page E) 0xFB
0xFF6C	(Page E) 0xAC	0xFF7C	(Page E) 0xBC	0xFF8C	(Page E) 0xCC	0xFF9C	(Page E) 0xDC	0xFFAC	(Page E) 0xEC	0xFFBC	(Page E) 0xFC
0xFF6D	(Page E) 0xAD	0xFF7D	(Page E) 0xBD	0xFF8D	(Page E) 0xCD	0xFF9D	(Page E) 0xDD	0xFFAD	(Page E) 0xED	0xFFBD	(Page E) 0xFD
0xFF6E	(Page E) 0xAE	0xFF7E	(Page E) 0xBE	0xFF8E	(Page E) 0xCE	0xFF9E	(Page E) 0xDE	0xFFAE	(Page E) 0xEE	0xFFBE	(Page E) 0xFE
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0xFFC0	(Page F) 0xA0	0xFFFFD0	(Page F) 0xB0	0xFFFFE0	(Page F) 0xC0	0xFFFFF0	(Page F) 0xD0				
0xFFC1	(Page F) 0xA1	0xFFFFD1	(Page F) 0xB1	0xFFFFE1	(Page F) 0xC1	0xFFFFF1	(Page F) 0xD1				
0xFFC2	(Page F) 0xA2	0xFFFFD2	(Page F) 0xB2	0xFFFFE2	(Page F) 0xC2	0xFFFFF2	(Page F) 0xD2				
0xFFC3	(Page F) 0xA3	0xFFFFD3	(Page F) 0xB3	0xFFFFE3	(Page F) 0xC3	0xFFFFF3	(Page F) 0xD3				
0xFFC4	(Page F) 0xA4	0xFFFFD4	(Page F) 0xB4	0xFFFFE4	(Page F) 0xC4	0xFFFFF4	(Page F) 0xD4				
0xFFC5	(Page F) 0xA5	0xFFFFD5	(Page F) 0xB5	0xFFFFE5	(Page F) 0xC5	0xFFFFF5	(Page F) 0xD5				
0xFFC6	(Page F) 0xA6	0xFFFFD6	(Page F) 0xB6	0xFFFFE6	(Page F) 0xC6	0xFFFFF6	(Page F) 0xD6				
0xFFC7	(Page F) 0xA7	0xFFFFD7	(Page F) 0xB7	0xFFFFE7	(Page F) 0xC7	0xFFFFF7	(Page F) 0xD7				
0xFFC8	(Page F) 0xA8	0xFFFFD8	(Page F) 0xB8	0xFFFFE8	(Page F) 0xC8	0xFFFFF8	(Page F) 0xD8				
0xFFC9	(Page F) 0xA9	0xFFFFD9	(Page F) 0xB9	0xFFFFE9	(Page F) 0xC9	0xFFFFF9	(Page F) 0xD9				
0xFFCA	(Page F) 0xAA	0xFFFFDA	(Page F) 0xBA	0xFFFFEA	(Page F) 0xCA	0xFFFFFA	(Page F) 0xDA				
0xFFCB	(Page F) 0xAB	0xFFFFDB	(Page F) 0xBB	0xFFFFEB	(Page F) 0xCB	0xFFFFFB	(Page F) 0xDB				
0xFFCC	(Page F) 0xAC	0xFFFFDC	(Page F) 0xBC	0xFFFFEC	(Page F) 0xCC	0xFFFFFC	(Page F) 0xDC				
0xFFCD	(Page F) 0xAD	0xFFFFDD	(Page F) 0xBD	0xFFFFED	(Page F) 0xCD	0xFFFFFD	(Page F) 0xDD				
0xFFCE	(Page F) 0xAF	0xFFFFDE	(Page F) 0xBE	0xFFFFEE	(Page F) 0xCF	0xFFFFFE	(Page F) 0xDE				
0xFFCF	(Page F) 0xAF	0xFFFFDF	(Page F) 0xBF	0xFFFFEF	(Page F) 0xCF	0xFFFFFF	(Page F) 0xDF				

In external MCU mode, external host interface has the privilege to access REG_XFR_WRAPPER. The total 256 addresses are separated into 3 pages. 0xFF00 ~ 0xFF5F is Page D, 0xFF60 ~ 0xFFFF is Page E and 0xFFC0 ~ 0xFFFF is Page F. External host control signals are passed to scalar register interface. Host interface must integrate the output of scalar interface and REG_XFR_WRAPPER depends on page selection. When ISP is activated, REG_XFR_WRAPPER is accessed by ISP interface, it has the highest priority. DW8051 and external host is selected by power-on-latch signal, ext_host_sel.

**Interrupt Control**

Register::IRQ_Status						0xFF00
Name	Bits	R/W	Default	Comments	Config	
Reserved	7	--	--	Reserved		
M2PLL_IRQ_EVENT	6	R/W	0	M2PLL-abnormal Event Status 1. Select M2PLL as clock source, but M2PLL power down, power saving or output disable, clear this bit to disable the interrupt	Rport Wport	
Reserved	5	--	--	Reserved		
SCA_IRQ_EVENT	4	R/W	0	Scalar-related Event Status 1. IF Scalar integrated IRQ event occurred since the last status cleared	Rport Wport	
I2CM_IRQ_EVENT	3	R/W	0	I2C Master Event Status 1. IF I2C Master IRQ event occurred since the last status cleared	Rport Wport	
ADC_IRQ_EVENT	2	R/W	0	ADC Event Status 1: If the ADC IRQ event occurred since the last status cleared	Rport Wport	
Reserved	1	--	--	Reserved		
DDC_IRQ_EVENT	0	R/W	0	DDC Event Status 1: If the DDC IRQ event occurred since the last status cleared	Rport Wport	

Register::IRQ_Priority						0xFF01
Name	Bits	R/W	Default	Comments	Config	
Reserved	7	--	--	Reserved		
M2PLL_IRQ_PRI	6	R/W	0	M2PLL-abnormal IRQ Priority 0: Connected to int0 1: Connected to int1		



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Reserved	5	--	--	Reserved	
SCA_IRQ_PRI	4	R/W	0	Scalar integrated IRQ Priority 0: Connected to int0 1: Connected to int1	
I2CM_IRQ_PRI	3	R/W	0	I2C Master IRQ Priority 0: Connected to int0 1: Connected to int1	
ADC_IRQ_PRI	2	R/W	0	ADC IRQ Priority 0: Connected to int0 1: Connected to int1	
Reserved	1	--	--	Reserved	
DDC_IRQ_PRI	0	R/W	0	DDC IRQ Priority 0: Connected to int0 1: Connected to int1	

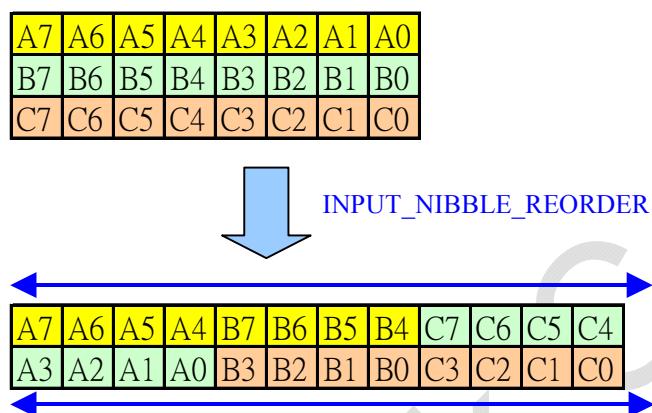
Register:: REV_DUMMY1 0xFF02					
Name	Bits	R/W	Default	Comments	Config
VS1_IRQ_PRI	7	R/W	1	VS1 IRQ Priority 0: Connected to int0 1: Connected to int1	
VS0_IRQ_PRI	6	R/W	0	VS0 IRQ Priority 0: Connected to int0 1: Connected to int1	
VS1_IRQ_EVENT	5	R/W	0	VS1 Event Status, write 0 to clear	
VS0_IRQ_EVENT	4	R/W	0	VS0 Event Status, , write 0 to clear	
VS1_INT_EN	3	R/W	0	VS1 Interrupt enable 0: disable 1 :enable	



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VS1_trigger_type	2	R/W	0	VS1 trigger type 0: posedge trigger 1: bypass mode (level trigger)	
VS0_INT_EN	1	R/W	0	VS0 Interrupt enable 0: disable 1: enable	
VS0_trigger_type	0	R/W	0	VS1 trigger type 0: posedge trigger 1: bypass mode (level trigger)	

OSD reorder

Register::Triple_Bytes_Operation						0xFF03
Name	Bits	R/W	Default	Comments	Config	
GLOBAL_NIBBLE_REORDER_EN	7	R/W	0	1: The input bit sequence of three bytes, A[7:0], B[7:0] C[7:0] will be reordered to A[7:4], B[7:4], C[7:4], A[3:0], B[3:0], C[3:0] before any operation and change back to input sequence at the end 0: No modification		
INPUT_NIBBLE_REORDER_EN	6	R/W	1	1: The input bit sequence of three bytes, A[7:0], B[7:0], C[7:0] will be reordered to {A[7:4], B[7:4], C[7:4]}, {A[3:0], B[3:0], C[3:0]} before any operation 0: No modification		
OUTPUT_NIBBLE_REORDER_EN	5	R/W	0	1: The output bit sequence of three bytes,		



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				A[7:4], B[7:4], C[7:4], A[3:0], B[3:0], C[3:0] will be reordered to A[7:0], B[7:0], C[7:0] before output 0: No modification	
TBO_dummy	4	R/W	0	Dummy Bit	
FIRST_BYTE_SHIFT_DIRECTION	3	R/W	1	1: LEFT SHIFT 0: RIGHT SHIFT	
LEFT_BYTE_SHIFT_DIRECTION	2	R/W	0	1: LEFT SHIFT 0: RIGHT SHIFT	
RESTART_FROM_LAST	1	R/W	0	1: Restart from last three bytes (auto_clear)	RPORT WPoRT
RESTART_FROM_FIRST	0	R/W	0	1: Restart from input first bytes (auto_clear)	RPORT WPoRT

Register::Shift_Bits_Number						0xFF04
Name	Bits	R/W	Default	Comments	Config	
FIRST_BITS_SHIFT	7:4	R/W	0	The left/right bit shift times.		
SECOND_BITS_SHIFT	3:0	R/W	0	The left/right bit shift times.		

Register::Byte_Address						0xFF05
Name	Bits	R/W	Default	Comments	Config	
THIRD_BITS_SHIFT	7:4	R/W	0	The left/right bit shift times.		
LEFT_BITS_SHIFT	3:0	R/W	0	The left/right bit shift times.		

Register::Input_Triple_Bytes						0xFF06
Name	Bits	R/W	Default	Comments	Config	
INPUT_OP_BYTES	7:0	R/W	0	Three bytes input by sequence here.	Rport Wport	

Register::Result_Triple_Bytes						0xFF07
Name	Bits	R/W	Default	Comments	Config	
OUTPUT_OP_BYTES	7:0	R/W	0	Output bytes input by sequence here.	RPORT WPoRT	

Register::Byte_Address						0xFF18
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Name	Bits	R/W	Default	Comments	Config
ALL_ADDR_RST	7	R/W	0	1: Write 1 to reset input/result triple bytes address to 0	RPORT WPORt
Reserved	6:3	R/W	--	Reserved	
INPUT_OUTPUT_CONTROL	2	R/W	0	1: Write BYTE_ADDR to control address of result triple bytes 0: Write BYTE_ADDR to control address of input triple bytes	Rport Wport
BYTE_ADDR	1:0	R/W	0	Byte Address for Current Input or Result bytes	Rport Wport

ADC

A/D Converter

RTD2485XD has embedded 4 channels of analog-to-digital converter by A_circuit. The ADCs_ACKT convert analog input voltage on the four A/D input pins to four 8-bit digital data stored in XFRs (FF09 ~ FF0C) sequentially.

The ADC conversion range is from GND to VDD and the conversion is linear and monotonic with no missing codes. To start A/D conversion, set STRT_ADCx = 1 and the conversion will be completed in less than 12us for 4 channels.

ADC_Ackt block diagram (for Key Sensing, D-connector)

Register::ADC_Acontrol

0xFF08



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Name	Bits	R/W	Default	Comments	Config
STRT_ADC_ACKT	7	R/W	0	Write 1 to start the A/D conversion. Auto clear when A/D Conversion has been completed. 0:A/D Conversion has been completed 1:A/D Conversion is not completed yet	Rport Wport
ADC_ATEST	6	R/W	0	0: Normal operation 1: ADC test mode	
Reserved	5:3	R/W	0	Reserved	
ADC_A_BIAS_ADJ	2:1	R/W	1	ADC bias current adjust 00: 15u 01: 20u 10: 25u 11: 30u	
ADC_A_CK_SEL	0	R/W	0	Inverse ADC input clock pos/neg 0: pos 1: neg	

Register::ADC_A0_convert_result 0xFF09					
Name	Bits	R/W	Default	Comments	Config
ADC_A0_DATA	7:0	R	FF	Converted data of ADC_A0	

Register::ADC_A1_convert_result 0xFF0A					
Name	Bits	R/W	Default	Comments	Config
ADC_A1_DATA	7:0	R	FF	Converted data of ADC_A1	

Register::ADC_A2_convert_result 0xFF0B					
Name	Bits	R/W	Default	Comments	Config
ADC_A2_DATA	7:0	R	FF	Converted data of ADC_A2	

Register::ADC_A3_convert_result 0xFF0C					
Name	Bits	R/W	Default	Comments	Config
ADC_A3_DATA	7:0	R	FF	Converted data of ADC_A3	



Register::ADC_CLK_DIV						0xFF0D
Name	Bits	R/W	Default	Comments	Config	
ADC_CLK_SEL	7	R/W	0	ADC clk from 0: Xtal/IOSC 1: M2PLL		
ADC_CLK_DIV	6:0	R/W	0x04	ADC clk divider 0x00 is DIV1, 0x01 is DIV1, 0x02 is DIV2 and so on. ADC clk target is 3Mhz.		

Register:: Auto_Mode_Ctrl01						0xFF0E
Name	Bits	R/W	Default	Comments	Config	
ADC_INT_flag	7	R/W	0	Interrupt flag Write "1" to clear	Rport Wport	
Reserved	6:3	R/W	0	Reserved		
ADC_Auto_Mode_EN	2	R/W	0	0: Disable 1: Enable auto mode		
ADC_EN_DEBU	1	R/W	1	0: disable de-bounce 1: enable de-bounce. meas 3 times (based on waiting time)		
ADC_INT_EN	0	R/W	0	(L_Threshold < Meas < H_Threshold), Meas_Cnt +1, Meas_Cnt > debounce times, into ISR 0: disable INT 1: enable INT		

Register::ADC0_THRESHOLD_H						0xFF0F
Name	Bits	R/W	Default	Comments	Config	
ADC0_HI_THRESHOLD	7:0	R/W	00	High threshold value for auto mode		

Register::ADC0_THRESHOLD_L						0xFF10
Name	Bits	R/W	Default	Comments	Config	
ADC0_LO_THRESHOLD	7:0	R/W	00	Low threshold value for auto mode		

Register::ADC1_THRESHOLD_H						0xFF11
Name	Bits	R/W	Default	Comments	Config	
ADC1_HI_THRESHOLD	7:0	R/W	00	High threshold value for auto mode		

Register::ADC1_THRESHOLD_L						0xFF12
Name	Bits	R/W	Default	Comments	Config	
ADC1_LO_THRESHOLD	7:0	R/W	00	Low threshold value for auto mode		



Register::ADC2_THRESHOLD_H 0xFF13					
Name	Bits	R/W	Default	Comments	Config
ADC2_HI_THRESHOLD	7:0	R/W	00	High threshold value for auto mode	

Register::ADC2_THRESHOLD_L 0xFF14					
Name	Bits	R/W	Default	Comments	Config
ADC2_LO_THRESHOLD	7:0	R/W	00	Low threshold value for auto mode	

Register::ADC3_THRESHOLD_H 0xFF15					
Name	Bits	R/W	Default	Comments	Config
ADC3_HI_THRESHOLD	7:0	R/W	00	High threshold value for auto mode	

Register::ADC3_THRESHOLD_L 0xFF16					
Name	Bits	R/W	Default	Comments	Config
ADC3_LO_THRESHOLD	7:0	R/W	00	Low threshold value for auto mode	

Register::CTRL0_WAIT_TIME_VALUE 0xFF17					
Name	Bits	R/W	Default	Comments	Config
ADC_Wait_Value	7:0	R/W	0x01	Wait time= wait_value * 1.3ms (0.75Khz), 1.3ms < wait time < 340ms	

DDC

RTD2485XD has three DDC ports. The MCU can access the following three DDC interface:

- DDC_RAM1 (FD80~FDFF) through pin ASDL and ASDA by ADC DDC channel.
- DDC_RAM2 (FE00~FE7F) through pin DSDL and DSDA by DVI DDC channel.
- DDC_RAM3 (FE80~FEFF) through pin HSDL and HSDA by HDMI DDC channel.

Besides, the DDC_RAM1, DDC_RAM2, DDC_RAM3 can be assigned from 128 to 256bytes.

The actual sizes of each DDC_RAM are determined by the combination of ADDCRAM_ST, DDDCRAM_ST, and HDDCRAM_ST. The DDC RAMs are shared with MCU's XSRAM, configuration must be take care for reserving XSRAM for programming. For example, Set ADDCRAM_ST = 0x2, DDDCRAM_ST = 0x3, HDDCRAM_ST = 0x2 and disable , DVI DDC. The XSRAM for MCU is 512 bytes and ADC DDC/HDMI DDC is used with 256 bytes.

The DDC of RTD2485XD is compliant with VESA DDC standard. All DDC slaves are in DDC1 mode after reset. When a high to low transition is detected on ASCL/DSCL/HSCL pin, the DDC slave will enter DDC2 transition mode. The DDC slave can revert to DDC1 mode if the SCL signal keeps unchanged for 128 VSYNC periods in DDC2 transition mode and RVT_A_DDC1_EN / RVT_D_DDC1_EN / RVT_H_DDC1_EN = 1. In DDC2 transition mode, the DDC slave will lock in DDC2 mode if a valid control byte is received. Furthermore, user can force the DDC slave to operate DDC2 mode by setting A_DDC2 / D_DDC2/ H_DDC2 = 1.



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Register:: ADC_SEGMENT_ADDRESS 0xFF19					
Name	Bits	R/W	Default	Comments	Config
ADC_SEG_ADDR	7:1	R/W	0x30	ADC slave address for segment control	
Reserved	0	--	--	Reserved	

Register:: ADC_SEGMENT_DATA 0xFF1A					
Name	Bits	R/W	Default	Comments	Config
ADC_SEG_DATA	7:0	R/W	0x00	Data Access for Slave ID, ADC_SEGMENT_ADDRESS, in ADC DDC	Rport Wport

Register::ADC_DDC_enable 0xFF1B					
Name	Bits	R/W	Default	Comments	Config
A_DDC_ADDR	7:5	R/W	0	ADC DDC Channel Address Least Significant 3 Bits (The default DDC channel address MSB 4 Bits is "A")	
A_SCL_DBN_SEL	4	R/W	0	SCL Debounce Clock Selection 0: De-bounce clock (after clock divider) 1: De-bounce reference clock	
A_DDC_W_STA	3	R/W	0	ADC DDC Write Status (for external DDC access only) It is cleared after write. (No matter what the data are)	Rport wport
A_DDCRAM_W_EN	2	R/W	0	ADC DDC SRAM Write Enable (for external DDC access only) 0: Disable 1: Enable	
A_DBN_EN	1	R/W	1	ADC DDC De-bounce Enable 0: Disable 1: Enable (with crystal/4)	
A_DDC_EN	0	R/W	0	ADC DDC Channel Enable Bit 0: MCU access Enable 1: DDC channel Enable	



Register::ADC_DDC_control_1 0xFF1C					
Name	Bits	R/W	Default	Comments	Config
A_DBN_CLK_SEL	7:6	R/W	0	De-bounce clock divider 00: 1/1 reference clock 01: 1/2 reference clock 1X: 1/4 reference clock	
A_STOP_DBN_SEL	5:4	R/W	3	De-bounce sda stage 00: no latch stage 01: latch one stage 10: latch two stage 11: latch three stage	
A_SYS_CK_SEL	3	R/W	0	De-bounce reference clock 0: crystal clock 1. Serial flash clock (M2PLL / Flash_DIV)	
A_DDC2	2	R/W	0	Force to ADC DDC to DDC2 mode 0: Normal operation 1: DDC2 is active	
RST_A_DDC	1	R/W	0	Reset ADC DDC circuit 0: Normal operation 1: reset (auto cleared)	Rport wport
RVT_A_DDC1_EN	0	R/W	0	ADC DDC revert to DDC1 enable(SCL idle for 128 VSYNC) 0: Disable 1: Enable	

Register::ADC_DDC_control_2 0xFF1D					
Name	Bits	R/W	Default	Comments	Config
A_SEG_WR_EN	7	R/W	0	Enable interrupt of ADC segment address write 0: Disable 1: Enable	
Reserved	6:5	--	--	Reserved	
ADC_DDCCI_EN	4	R/W	1	ADC DDC-CI Channel Enable Switch 0: Disable 1: Enable	



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ADC_DDCISP_EN	3	R/W	1	ADC DDC ISP Channel Enable Switch 0: Disable 1: Enable If all of DDC ISP Channel are disable, ADC DDC ISP Channel will be enable.	
ADC_DDCSEG_EN	2	R/W	1	ADC DDC Segment Channel Enable Switch 0: Disable 1: Enable	
A SEG WR	1	R/W	0	ADC DDC Segment Write Status 0: no external write after clear 1: new external write after clear It is cleared after write	Wport Rport
A_FORCE_SCL_L	0	R/W	0	Force external SCL bus low 1: Driving SCL = 0 after external SCL = 0 0: Release SCL	

Register::DVI_DDC_enable 0xFF1E					
Name	Bits	R/W	Default	Comments	Config
D_DDC_ADDR	7:5	R/W	0	DVI DDC Channel Address Least Significant 3 Bits (The default DDC channel address MSB 4 Bits is "A")	
D_SCL_DBN_SEL	4	R/W	0	SCL Debounce Clock Selection 0: De-bounce clock (after clock divider) 1: De-bounce reference clock	
D_DDC_W_STA	3	R/W	0	DVI DDC External Write Status (for external DDC access only) It is cleared after write.	Wport Rport
D_DDRCRAM_W_EN	2	R/W	0	DVI DDC External Write Enable (for external DDC access only) 0: Disable 1: Enable	
D_DBN_EN	1	R/W	1	DVI DDC Debounce Enable 0: Disable 1: Enable (with crystal/4)	
D_DDC_EN	0	R/W	0	DVI DDC Channel Enable Switch	



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				0: MCU access Enable 1: External DDC access Enable	
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Register::DVI_DDC_control_1					0xFF1F
Name	Bits	R/W	Default	Comments	Config
D_DBN_CLK_SEL	7:6	R/W	0	De-bounce clock divider 00: 1/1 reference clock 01: 1/2 reference clock 1X: 1/4 reference clock	
D_STOP_DBN_SEL	5:4	R/W	3	De-bounce sda stage 00: no latch stage 01: latch one stage 10: latch two stage 11: latch three stage	
D_SYS_CK_SEL	3	R/W	0	De-bounce reference clock 0: crystal clock 1. Serial flash clock (M2PLL / Flash_DIV)	
D_DDC2	2	R/W	0	Force to DVI DDC to DDC2 mode 0: Normal operation 1: DDC2 is active	
RST_D_DDC	1	R/W	0	Reset DVI DDC circuit 0: Normal operation 1: reset (auto cleared)	Rport wport
RVT_D_DDC1_EN	0	R/W	0	DVI DDC revert to DDC1 enable(SCL idle for 128 VSYNC) 0: Disable 1: Enable	

Register::DVI_DDC_control_2					0xFF20
Name	Bits	R/W	Default	Comments	Config
D_SEG_WR_EN	7	R/W	0	Enable interrupt of DVI segment address write 0: Disable 1: Enable	
Reserved	6:5	--	--	Reserved	
DVI_DDCCI_EN	4	R/W	1	DVI DDC-CI Channel Enable Switch	



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				0: Disable 1: Enable	
DVI_DDCISP_EN	3	R/W	1	DVI DDC ISP Channel Enable Switch 0: Disable 1: Enable	
DVI_DDCSEG_EN	2	R/W	1	DVI DDC Segment Channel Enable Switch 0: Disable 1: Enable	
D_SEG_WR	1	R/W	0	DVI DDC Segment Write Status 0: no external write after clear 1: new external write after clear It is cleared after write	Wport Rport
D_FORCE_SCL_L	0	R/W	0	Force external SCL bus low 1: Driving SCL = 0 after external SCL = 0 0: Release SCL	

Register::DDCRAM_partition					0xFF21
Name	Bits	R/W	Default	Comments	Config
ISP_DDC2B_SW_ITCH	7	R/W	0	0: Not Allow DDC2B access in ISP Mode, ddc can program 1: Allow DDC2B access in ISP Mode, but can not program	
FORCE_DDCRAM_ST	6	R/W	0	Force ADC/DVI/HDMI DDC RAM Start Address to be 0xFD00 1: enable 0: disable (RAM start address decided by bit[5:4], bit[3:2], bit[1:0])	
ADDCRAM_ST	5:4	R/W	0x3	ADDC RAM Start Address is 0xFC00 + ADDCRAM_ST*0x80, ADDCRAM SIZE = DDDCRAM_ST – ADDCRAM_ST	
DDDCRAM_ST	3:2	R/W	0x3	DDDC RAM Start Address is 0xFC80 + DDDCRAM_ST*0x80,	



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				DDDCRAM SIZE = HDDCRAM_ST – DDDCRAM_ST	
HDDCRAM_ST	1:0	R/W	0x3	HDDC RAM Start Address is 0xFD00 + ADDCRAM_ST*0x80, HDDCRAM SIZE = 0xFF00 – HDDCRAM_ST	

XRAM Arbitor	Byte	Start	End	
External RAM	640	0xFB00	0xFD7F	xData
DDC0_RAM	128	0xFD80	0xFDFF	VGA
DDC1_RAM	128	0xFE00	0xFE7F	DVI 1
DDC2_RAM	128	0xFE80	0xFEFF	DVI 2
External RAM	384	0xFB00	0xFC7F	xData
DDC0_RAM	128	0xFC80	0xFCFF	VGA
DDC1_RAM	256	0xFD00	0xFDFF	HDMI 1
DDC2_RAM	256	0xFE00	0xFEFF	HDMI 2

Register::VSYNC_Sel					0xFF22
Name	Bits	R/W	Default	Comments	Config
Reserved	7:4	-			
VS_CON1	3:2	R/W	0	00: VSYNC1 signal is connected to ADC DDC 01: VSYNC1 signal is connected to DVI DDC 1x: VSYNC1 signal is connected to HDMI DDC	
Reserved	1:0	R/W	0	Reserved	

DDC-CI

Register::IIC_set_slave					0xFF23
Name	Bits	R/W	Default	Comments	Config
IIC_ADDR	7:1	R/W	37	IIC Slave Address to decode	
CH_SEL	0	R/W	0	Channel Select, overridden by HCH_SEL(0xFF2B[0]) = 1 0: from ADC DDC 1: from DVI DDC	



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pin121 / pin122 → DDCSCL3 / DDCSDA3, (HDMI DDC) → **0xFF2B** Bit 0 Enable
 pin123/ pin124 → DDCSCL2 / DDCSDA2, (DVI DDC), → **0xFF23** Bit 0 Enable

Register::IIC_sub_in						0xFF24
Name	Bits	R/W	Default	Comments	Config	
IIC_SUB_ADDR	7:0	R	00	IIC Sub-Address Received		

Register::IIC_data_in						0xFF25
Name	Bits	R/W	Default	Comments	Config	
IIC_D_IN	7:0	R	00	IIC data received. 16-bytes depth read in buffer mode	RPORT	

Register::IIC_data_out						0xFF26
Name	Bits	R/W	Default	Comments	Config	
IIC_D_OUT	7:0	W	00	IIC data to be transmitted	Rport Wport	

Register::IIC_status						0xFF27
Name	Bits	R/W	Default	Comments	Config	
A_WR_I	7	R/W	0	If ADC DDC detects a STOP condition in write mode, this bit is set to “1”. Write 0 to clear.	Rport	Wport
D_WR_I	6	R/W	0	If DVI DDC detects a STOP condition in write mode, this bit is set to “1”. Write 0 to clear.	Rport	Wport
DDC_128VS1_I	5	R/W	0	In DDC2 Transition mode, SCL idle for 128 VSYNC. Write 0 to clear.	Rport	Wport
STOP_I	4	R/W	0	If IIC detects a STOP condition(slave address must match), this bit is set to “1”. Write 0 to clear.	Rport	Wport
D_OUT_I	3	R	0	If IIC_DATA_OUT loaded to serial-out-byte, this bit is set to “1”. Write IIC_data_out (FF25) to clear.		
D_IN_I	2	R	0	If IIC_DATA_IN latched, this bit is set to “1”. Read IIC_data_in (FF24) to clear.		



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SUB_I	1	R/W	0	If IIC_SUB latched, this bit is set to "1" Write 0 to clear.	Rport Wport
SLV_I	0	R/W	0	If IIC_SLAVE latched, this bit is set to "1" Write 0 to clear.	Rport Wport

Register::IIC_IRQ_control					0xFF28
Name	Bit s	R/W	Default	Comments	Config
AWI_EN	7	R/W	0	0: Disable the A_WR_I signal as an interrupt source 1: Enable the A_WR_I signal as an interrupt source	
DWI_EN	6	R/W	0	0: Disable the D_WR_I signal as an interrupt source 1: Enable the D_WR_I signal as an interrupt source	
DDC_128VSI1_EN	5	R/W	0	0: Disable the 128VSI1_I signal as an interrupt source 1: Enable the 128VSI1_I signal as an interrupt source	
STOPI_EN	4	R/W	0	0: Disable the STOP_I signal as an interrupt source 1: Enable the STOP_I signal as an interrupt source	
DOI_EN	3	R/W	0	0: Disable the D_OUT_I signal as an interrupt source 1: Enable the D_OUT_I signal as an interrupt source	
DII_EN	2	R/W	0	0: Disable the D_IN_I signal as an interrupt source 1: Enable the D_IN_I signal as an interrupt source	
SUBI_EN	1	R/W	0	0: Disable the SUB_I signal as an interrupt source 1: Enable the SUB_I signal as an interrupt source	
SLVI_EN	0	R/W	0	0: Disable the SLV_I signal as an interrupt source 1: Enable the SLV_I signal as an interrupt source	

Register::IIC_status2					
Name	Bits	R/W	Default	Comments	Config
IIC_FORCE_SCL_L	7	R/W	0	Force SCL = 0 when one of the following tow case happen: 1. IIC_BUF_FULL = 1 in write mode 2. IIC_BUF_EMPTY = 1 in read mode	
FORCE_NACK	6	R/W	0	Force IIC return NACK when one of the following tow case happen:	



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				IIC_BUF_FULL = 1 in write mode	
IIC_BUF_OV	5	R/W	0	IIC_DATA_BUFFER Overflow. Write ‘0’ to clear	Rport Wport
IIC_BUF_UN	4	R/W	0	IIC_DATA_BUFFER Underflow. Write ‘0’ to clear	Rport Wport
DDC_128VS2_I	3	R/W	0	In DDC2 Transition mode, SCL idle for 128 VSYNC. Write 0 to clear. Write ‘0’ to clear	Rport Wport
IIC_BUF_FULL	2	R	0	IIC_DATA_BUFFER Full If IIC_DATA buffer is full, this bit is set to “1”. (On-line monitor) The IIC_DATA buffer Full status will be on-line-monitor the condition, once it becomes full, it kept high, if it is not-full, then it goes low.	
IIC_BUF_EMPTY	1	R	0	IIC_DATA_BUFFER Empty If IIC_DATA buffer is empty, this bit is set to “1”. (On-line monitor) The IIC_DATA buffer Empty status will be on-line-monitor the condition, once it becomes empty, it kept high, if it is not-empty, then it goes low.	
H_WR_I	0	R/W	0	If HDMI DDC detects a STOP condition in write mode, this bit is set to “1” . Write 0 to clear.	rport Wport

Register::IIC_IRQ_control2						0xFF2A
Name	Bits	R/W	Default	Comments	Config	
AUTO_RST_BUF	7	R/W	0	Auto reset IIC_DATA Buffer 0: disable 1: enable In host (pc) write enable, when IIC write (No START after IIC_SUB), reset IIC_DATA buffer.		
RST_DATA_BUF	6	R/W	0	Reset IIC_DATA buffer 0: Finish 1: Reset	Wport	Rport



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DATA_BUF_WEN	5	R/W	0	IIC_DATA buffer write enable 0: host (pc) write enable 1: slave (mcu) write enable Both PC and MCU can read IIC_DATA buffer, but only one can write IIC_DATA buffer.	
Dummy_2	4	R/W	0	Reserved	
DDC_128VSI2_EN	3	R/W	0	0: Disable the 128VS2_I signal as an interrupt source 1: Enable the 128VS2_I signal as an interrupt source	
DDC_BUF_FULL_EN	2	R/W	0	0: Disable the DDC_DATA_BUFFER Full signal as an interrupt source 1: Enable the DDC_DATA_BUFFER Full signal as an interrupt source	
DDC_BUF_EMPTY_EN	1	R/W	0	0: Disable the DDC_DATA_BUFFER Empty signal as an interrupt source 1: Enable the DDC_DATA_BUFFER Empty signal as an interrupt source	
HWI_EN	0	R/W	0	0: Disable the H_WR_I signal as an interrupt source 1: Enable the H_WR_I signal as an interrupt source	

Register::IIC_channel_control						0xFF2B
Name	Bits	R/W	Default	Comments	Config	
Reserved	7:2	--	0	Reserved		
RLS_SCL_SU	1	R/W	0	Set IIC data Setup Time When holding SCL low 0: Use Delay Chain (~5ns) 1: Use Crystal Clock to increase data setup time relative to SCL clock line		
HCH_SEL	0	R/W	0	Channel Select of DDC-CI 1: from HDMI DDC 0: controlled by CH_SEL		

pin121 / pin122 → DDCSCL3 / DDCSDA3, (HDMI DDC) → 0xFF2B Bit 0 Enable

pin123/ pin124 → DDCSCL2 / DDCSDA2, (DVI DDC), → 0xFF23 Bit 0 Enable

Register::HDMI_DDC_enable						0xFF2C
Name	Bits	R/W	Default	Comments	Config	



H_DDC_ADDR	7:5	R/W	0	HDMI DDC Channel Address Least Significant 3 Bits (The default DDC channel address MSB 4 Bits is “A”)	
H_SCL_DBN_SEL	4	R/W	0	SCL Debounce Clock Selection 0: De-bounce reference clock 1: De-bounce clock (after clock divider)	
H_DDC_W_STA	3	R/W	0	HDMI DDC Write Status (for external DDC access only) It is cleared after write.	Rport Wport
H_DDRCRAM_W_EN	2	R/W	0	HDMI DDC SRAM Write Enable (for external DDC access only) 0: Disable 1: Enable	
H_DBN_EN	1	R/W	1	HDMI DDC De-bounce Enable 0: Disable 1: Enable (with crystal/4)	
H_DDC_EN	0	R/W	0	HDMI DDC Channel Enable Bit 0: MCU access Enable 1: DDC channel Enable	

Register::HDMI_DDC_control_1						0xFF2D
Name	Bits	R/W	Default	Comments	Config	
H_DBN_CLK_SEL	7:6	R/W	0	De-bounce clock divider 00: 1/1 reference clock 01: 1/2 reference clock 1X: 1/4 reference clock		
H_STOP_DBN_SEL	5:4	R/W	3	De-bounce sda stage 00: no latch stage 01: latch one stage 10: latch two stage 11: latch three stage		
H_SYS_CK_SEL	3	R/W	0	De-bounce reference clock 0: crystal clock 1: Serial flash clock (M2PLL / Flash_DIV)		
H_DDC2	2	R/W	0	Force to HDMI DDC to DDC2 mode 0: Normal operation		



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				1: DDC2 is active	
RST_H_DDC	1	R/W	0	Reset HDMI DDC circuit 0: Normal operation 1: reset (auto cleared)	Rport Wport
RVT_H_DDC1_EN	0	R/W	0	HDMI DDC revert to DDC1 enable(SCL idle for 128 VSYNC) 0: Disable 1: Enable	

Register::HDMI_DDC_control_2 0xFF2E					
Name	Bits	R/W	Default	Comments	Config
H_SEG_WR_EN	7	R/W	0	Enable interrupt of HDMI segment address write 0: Disable 1: Enable	
Dummy_3	6:5	R/W	0		
HDMI_DDCCI_EN	4	R/W	1	HDMI DDC-CI Channel Enable Switch 0: Disable 1: Enable	
HDMI_DDCISP_EN	3	R/W	1	HDMI DDC ISP Channel Enable Switch 0: Disable 1: Enable	
HDMI_DDCSEG_EN	2	R/W	1	HDMI DDC Segment Channel Enable Switch 0: Disable 1: Enable	
H_SEG_WR	1	R/W	0	HDMI DDC Segment Write Status 0: no external write after clear 1: new external write after clear It is cleared after write	Wport Rport
H_FORCE_SCL_L	0	R/W	0	Force external SCL bus low 1: Driving SCL = 0 after external SCL = 0 0: Release SCL	

The access ports below are used for external host interface only.



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Register::ADC_DDC_INDEX					0xFF2F
Name	Bits	R/W	Default	Comments	Config
A_DDC_INDEX	7:0	R/W	0	DDC SRAM Read/Write Index Register [7:0]	Rport Wport

Register::ADC_DDC_ACCESS_PORT					0xFF30
Name	Bits	R/W	Default	Comments	Config
A_DDC_ACCESS_PORT	7:0	R/W	0	DDC SRAM Read/Write Port	Rport Wport

Register::DVI_DDC_INDEX					0xFF31
Name	Bits	R/W	Default	Comments	Config
D_DDC_INDEX	7:0	R/W	0	DDC SRAM Read/Write Index Register [7:0]	Rport Wport

Register::DVI_DDC_ACCESS_PORT					0xFF32
Name	Bits	R/W	Default	Comments	Config
D_DDC_ACCESS_PORT	7:0	R/W	0	DDC SRAM Read/Write Port	Rport Wport

Register::HDMI_DDC_INDEX					0xFF33
Name	Bits	R/W	Default	Comments	Config
H_DDC_INDEX	7:0	R/W	0	DDC SRAM Read/Write Index Register [7:0]	Rport Wport

Register::HDMI_DDC_ACCESS_PORT					0xFF34
Name	Bits	R/W	Default	Comments	Config
H_DDC_ACCESS_PORT	7:0	R/W	0	DDC SRAM Read/Write Port	Rport Wport

Register:: DDCCI_REMAIN_DATA					0xFF35
Name	Bits	R/W	Default	Comments	Config
Reserved	7:5	--	0	Reserved	
DDCCI_REMAIN_LEN	4:0	R	0	DDCCI Remaining data length (= write_pointer – read_pointer)	



Register:: DVI_SEGMENT_ADDRESS 0xFF36					
Name	Bits	R/W	Default	Comments	Config
DVI_SEG_ADDR	7:1	R/W	0x30	DVI DDC slave address for segment control	
Reserved	0	--	--	Reserved	

Register:: DVI_SEGMENT_DATA 0xFF37					
Name	Bits	R/W	Default	Comments	Config
DVI_SEG_DATA	7:0	R/W	0x00	Data Access for Slave ID, DVI_SEGMENT_ADDRESS, in DVI DDC	Rport Wport

Register:: HDMI_SEGMENT_ADDRESS 0xFF38					
Name	Bits	R/W	Default	Comments	Config
HDMI_SEG_ADDR	7:1	R/W	0x30	HDMI DDC slave address for segment control	
Reserved	0	--	--	Reserved	

Register:: HDMI_SEGMENT_DATA 0xFF39					
Name	Bits	R/W	Default	Comments	Config
HDMI_SEG_DATA	7:0	R/W	0x00	Data Access for Slave ID, HDMI_SEGMENT_ADDRESS, in HDMI DDC	Rport Wport

PWM

RTD2485XD supports 6 channels of PWM DAC. The resolution of each PWM is 12-bit. PWM0, PWM1, PWM2, PWM3, PWM4 and PWM5 are connected to DA0, DA1, DA2, DA3, DA4 and DA5 respectively. The figure below represents the PWM clock generator. Based on the clock, we make up the PWM waveform which frequency is 1/4096 of the PWM clock.

The PWM duty registers have 12-bit resolution. These registers have double buffer mechanism. When write the MSB bit, the 12-bit data will be loaded.

The PWM frequency is :

$$F_{\text{PWM}} = f_{\text{clk}} / 2^M / (N+1) / \text{DUT}$$

Where each variables are controlled by:



M: PWMx_M

N: PWMxH_N * 256 + PWMxL_N

DUT: (PWMx_DUT_8B == 1)? 256 : 4096

The 12bit duty PWM frequency range is :

fclk=14.3M, fpwm = 3.5KHz ~ 0.1Hz

fclk=27M, fpwm = 6.6KHz ~ 0.2Hz

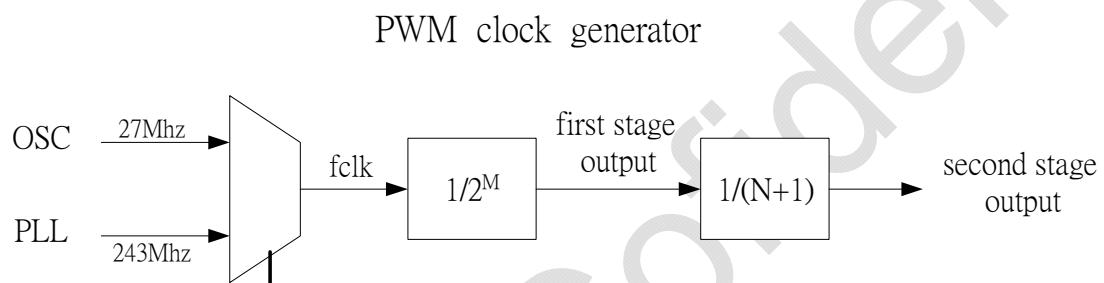
fclk=243M, fpwm = 60KHz ~ 1.8Hz

The 8bit duty PWM frequency range is :

fclk=14.3M, fpwm = 56KHz ~ 1.6Hz

fclk=27M, fpwm = 105.6KHz ~ 3.2Hz

fclk=243M, fpwm = 960KHz ~ 28.8Hz



Register::PWM_CK_SEL						0xFF3A
Name	Bits	R/W	Default	Comments		Config
PWM_CK_SEL_DUMMY	7:6	R/W	0	dummy		
PWM5_CK_SEL	5	R/W	0	PWMx clock generator input source 0: Crystal 1: PLL output (When PWM5_CK_SEL_HS = 0)		
PWM4_CK_SEL	4	R/W	0	PWMx clock generator input source 0: Crystal 1: PLL output (When PWM5_CK_SEL_HS = 0)		
PWM3_CK_SEL	3	R/W	0	PWMx clock generator input source 0: Crystal 1: PLL output (When PWM5_CK_SEL_HS = 0)		
PWM2_CK_SEL	2	R/W	0	PWMx clock generator input source 0: Crystal 1: PLL output		



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				(When PWM5_CK_SEL_HS = 0)	
PWM1_CK_SEL	1	R/W	0	PWMx clock generator input source 0: Crystal 1: PLL output (When PWM5_CK_SEL_HS = 0)	
PWM0_CK_SEL	0	R/W	0	PWMx clock generator input source 0: Crystal 1: PLL output (When PWM5_CK_SEL_HS = 0)	

Register::PWM03_M					0xFF3B
Name	Bits	R/W	Default	Comments	Config
PWM3_M	7:6	R/W	0	PWMx clock first stage divider	
PWM2_M	5:4	R/W	0	PWMx clock first stage divider	
PWM1_M	3:2	R/W	0	PWMx clock first stage divider	
PWM0_M	1:0	R/W	0	PWMx clock first stage divider	

Register::PWM45_M					0xFF3C
Name	Bits	R/W	Default	Comments	Config
PWM_M_DUMMY	7:4	R/W	0	dummy	
PWM5_M	3:2	R/W	0	PWMx clock first stage divider	
PWM4_M	1:0	R/W	0	PWMx clock first stage divider	

Register::PWM01_N_MSB					0xFF3D
Name	Bits	R/W	Default	Comments	Config
PWM1H_N	7:4	R/W	0	PWMx clock Second stage divider MSB[11:8]	
PWM0H_N	3:0	R/W	0	PWMx clock Second stage divider MSB[11:8]	

Register::PWM0_N_LSB					0xFF3E
Name	Bits	R/W	Default	Comments	Config
PWM0L_N	7:0	R/W	0	PWMx clock Second stage divider LSB[7:0]	

Register::PWM1_N_LSB					0xFF3F
Name	Bits	R/W	Default	Comments	Config



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PWM1L_N	7:0	R/W	0	PWMx clock Second stage divider LSB[7:0]	
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Register::PWM23_N_MSB 0xFF40					
Name	Bits	R/W	Default	Comments	Config
PWM3H_N	7:4	R/W	0	PWMx clock Second stage divider MSB[11:8]	
PWM2H_N	3:0	R/W	0	PWMx clock Second stage divider MSB[11:8]	

Register::PWM2_N_LSB 0xFF41					
Name	Bits	R/W	Default	Comments	Config
PWM2L_N	7:0	R/W	0	PWMx clock Second stage divider LSB[7:0]	

Register::PWM3_N_LSB 0xFF42					
Name	Bits	R/W	Default	Comments	Config
PWM3L_N	7:0	R/W	0	PWMx clock Second stage divider LSB[7:0]	

Register::PWM45_N_MSB 0xFF43					
Name	Bits	R/W	Default	Comments	Config
PWM4H_N	7:4	R/W	0	PWMx clock Second stage divider MSB[11:8]	
PWM5H_N	3:0	R/W	0	PWMx clock Second stage divider MSB[11:8]	

Register::PWM4_N_LSB 0xFF44					
Name	Bits	R/W	Default	Comments	Config
PWM4L_N	7:0	R/W	0	PWMx clock Second stage divider LSB[7:0]	

Register::PWM5_N_LSB 0xFF45					
Name	Bits	R/W	Default	Comments	Config
PWM5L_N	7:0	R/W	0	PWMx clock Second stage divider LSB[7:0]	

Register::PWML 0xFF46					
Name	Bits	R/W	Default	Comments	Config
PWM_W_DB_WR	7	R/W	0	Write 1 to Set PWM_Width if PWM_W_DB_EN = 1'b1. Auto-Clear after PWM_Width was loaded	Rport Wport
PWM_W_DB_MODE	6	R/W	0	PWM Width Setting Double-Buffer Mode 0: Setting active after PWM_W_DB_WR = 1 1: Setting active after PWM_W_DB_WR = 1 & DVS.	
PWM5L	5	R/W	0	0: enable Active H 1: enable Active L	
PWM4L	4	R/W	0	0: enable Active H 1: enable Active L	



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PWM3L	3	R/W	0	0: enable Active H 1: enable Active L	
PWM2L	2	R/W	0	0: enable Active H 1: enable Active L	
PWM1L	1	R/W	0	0: enable Active H 1: enable Active L	
PWM0L	0	R/W	0	0: enable Active H 1: enable Active L	

Register::PWM_VS_CTRL					0xFF47
Name	Bits	R/W	Default	Comments	Config
PWM_VS_CTRL_DUM	7:6	R/W	0	dummy	
PWM5_VS_RST_EN	5	R/W	0	0: Disable 1: Enable PWM5 reset by DVS	
PWM4_VS_RST_EN	4	R/W	0	0: Disable 1: Enable PWM4 reset by DVS	
PWM3_VS_RST_EN	3	R/W	0	0: Disable 1: Enable PWM3 reset by DVS	
PWM2_VS_RST_EN	2	R/W	0	0: Disable 1: Enable PWM2 reset by DVS	
PWM1_VS_RST_EN	1	R/W	0	0: Disable 1: Enable PWM1 reset by DVS	
PWM0_VS_RST_EN	0	R/W	0	0: Disable 1: Enable PWM0 reset by DVS	

Register::PWM_EN					0xFF48
Name	Bits	R/W	Default	Comments	Config
PWM_W_DB_EN	7	R/W	0	0: PWM Width set when write MSB 1: PWM Width setting double-buffered enable	
PWM_WIDTH_SEL	6	R/W	0	0: PWMxL_DUT is active 1: PWMxL_DUT is inactive, forced to 4'h0 internally	
PWM5_EN	5	R/W	0	0: PWM output disable 1: PWM output enable	
PWM4_EN	4	R/W	0	0: PWM output disable 1: PWM output enable	
PWM3_EN	3	R/W	0	0: PWM output disable 1: PWM output enable	
PWM2_EN	2	R/W	0	0: PWM output disable 1: PWM output enable	
PWM1_EN	1	R/W	0	0: PWM output disable 1: PWM output enable	
PWM0_EN	0	R/W	0	0: PWM output disable 1: PWM output enable	



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Register::PWM_CK						0xFF49
Name	Bits	R/W	Default	Comments	Config	
PWM_CK_DUMMY	7:6	R/W	0	Dummy		
PWM5_CK	5	R/W	0	0: Select first stage output 1: Select second stage output		
PWM4_CK	4	R/W	0	0: Select first stage output 1: Select second stage output		
PWM3_CK	3	R/W	0	0: Select first stage output 1: Select second stage output		
PWM2_CK	2	R/W	0	0: Select first stage output 1: Select second stage output		
PWM1_CK	1	R/W	0	0: Select first stage output 1: Select second stage output		
PWM0_CK	0	R/W	0	0: Select first stage output 1: Select second stage output		

Register::PWM0H_DUT						0xFF4A
Name	Bits	R/W	Default	Comments	Config	
PWM0H_DUT	7:0	R/W	0	PWM0[11:4] duty width When write the MSB bit (PWM_W_DB_EN=0) , the 12-bit data will be loaded.	Rport	Wport

Register::PWM1H_DUT						0xFF4B
Name	Bits	R/W	Default	Comments	Config	
PWM1H_DUT	7:0	R/W	0	PWM1[11:4] duty width When write the MSB bit (PWM_W_DB_EN=0) , the 12-bit data will be loaded.	Rport	Wport

Register::PWM01L_DUT						0xFF4C
Name	Bits	R/W	Default	Comments	Config	
PWM1L_DUT	7:4	R/W	0	PWM1[3:0] duty width	Rport	Wport
PWM0L_DUT	3:0	R/W	0	PWM0[3:0] duty width	Rport	Wport

Register::PWM2H_DUT						0xFF4D
Name	Bits	R/W	Default	Comments	Config	
PWM2H_DUT	7:0	R/W	0	PWM2[11:4] duty width When write the MSB bit (PWM_W_DB_EN=0) , the 12-bit data will be loaded.	Rport	Wport

Register::PWM3H_DUT						0xFF4E
Name	Bits	R/W	Default	Comments	Config	
PWM3H_DUT	7:0	R/W	0	PWM3[11:4] duty width	Rport	



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			When write the MSB bit (PWM_W_DB_EN=0) , the 12-bit data will be loaded.	Wport
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Register::PWM23L_DUT					0xFF4F
Name	Bits	R/W	Default	Comments	Config
PWM3L_DUT	7:4	R/W	0	PWM3[3:0] duty width	Rport Wport
PWM2L_DUT	3:0	R/W	0	PWM2[3:0] duty width	Rport Wport

Register::PWM4H_DUT					0xFF50
Name	Bits	R/W	Default	Comments	Config
PWM4H_DUT	7:0	R/W	0	PWM4[11:4] duty width When write the MSB bit (PWM_W_DB_EN=0) , the 12-bit data will be loaded.	Rport Wport

Register::PWM5H_DUT					0xFF51
Name	Bits	R/W	Default	Comments	Config
PWM5H_DUT	7:0	R/W	0	PWM5[11:4] duty width When write the MSB bit (PWM_W_DB_EN=0) , the 12-bit data will be loaded.	Rport Wport

Register:: PWM45L_DUT					0xFF52
Name	Bits	R/W	Default	Comments	Config
PWM5L_DUT	7:4	R/W	0	PWM5[3:0] duty width	Rport Wport
PWM4L_DUT	3:0	R/W	0	PWM4[3:0] duty width	Rport Wport

Register:: PWM_DUT_TYPE					0xFF53
Name	Bits	R/W	Default	Comments	Config
PWM_DUT_TYPE_DUMMY	7:6	R/W	0	Dummy	
PWM5_DUT_8B	5	R/W	0	PWM5 duty width type When PWM5_DUT_8B =1, only PWM5H_DUT is used as 8bit-resolution duty, and increase the PWM frequency x 16	
PWM4_DUT_8B	4	R/W	0	PWM4 duty width type When PWM4_DUT_8B =1, only PWM4H_DUT is used as 8bit-resolution duty, and increase the PWM frequency x 16	
PWM3_DUT_8B	3	R/W	0	PWM3 duty width type When PWM3_DUT_8B =1, only PWM3H_DUT is used as 8bit-resolution duty, and increase the PWM frequency x 16	
PWM2_DUT_8B	2	R/W	0	PWM2 duty width type When PWM2_DUT_8B =1, only PWM2H_DUT is used as 8bit-resolution duty, and increase the PWM frequency x 16	
PWM1_DUT_8B	1	R/W	0	PWM1 duty width type When PWM1_DUT_8B =1, only PWM1H_DUT is used as 8bit-resolution duty, and increase the PWM frequency x 16	



PWM0_DUT_8B	0	R/W	0	frequency x 16 PWM0 duty width type When PWM0_DUT_8B =1, only PWM0H_DUT is used as 8bit-resolution duty, and increase the PWM frequency x 16	
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Register::PWM_CNT_MODE					0xFF54
Name	Bits	R/W	Default	Comments	Config
Reserved	7:6	--	0	Reserved	
PWM5_CNT_MODE	5	R/W	0	0: duty mode 1: high/total counter mode. The total level count is {PWMxH_TOTALCNT, PWMxL_TOTALCNT}, high level count is {PWMxH_DUT, PWMxL_DUT}, and limited H/L transition number by PWMx_CYCLE_MAX	
PWM4_CNT_MODE	4	R/W	0	0: duty mode 1: high/total counter mode. The total level count is {PWMxH_TOTALCNT, PWMxL_TOTALCNT}, high level count is {PWMxH_DUT, PWMxL_DUT}, and limited H/L transition number by PWMx_CYCLE_MAX	
PWM3_CNT_MODE	3	R/W	0	0: duty mode 1: high/total counter mode. The total level count is {PWMxH_TOTALCNT, PWMxL_TOTALCNT}, high level count is {PWMxH_DUT, PWMxL_DUT}, and limited H/L transition number by PWMx_CYCLE_MAX	
PWM2_CNT_MODE	2	R/W	0	0: duty mode 1: high/total counter mode. The total level count is {PWMxH_TOTALCNT, PWMxL_TOTALCNT}, high level count is {PWMxH_DUT, PWMxL_DUT}, and limited H/L transition number by PWMx_CYCLE_MAX	
PWM1_CNT_MODE	1	R/W	0	0: duty mode 1: high/total counter mode. The total level count is {PWMxH_TOTALCNT, PWMxL_TOTALCNT}, high level count is {PWMxH_DUT, PWMxL_DUT}, and limited H/L transition number by PWMx_CYCLE_MAX	
PWM0_CNT_MODE	0	R/W	0	0: duty mode 1: high/total counter mode. The total level count is {PWMxH_TOTALCNT, PWMxL_TOTALCNT}, high level count is {PWMxH_DUT, PWMxL_DUT}, and limited H/L transition number by PWMx_CYCLE_MAX	

I2C Control Module

RTD2485XD provides one I2C master interface only.

Master

In the Random read operation, the slave address and data are clocked in and acknowledged by the slave. The master will generate another start condition. In Current address read operation, the internal data word address counter maintains the data word address accessed during the last read or write operation, incremented by one. The data word address stays valid between operations as long as the power is maintained. A Write operation requires data words following the slave address word and acknowledgment. The master terminates the write sequence with a stop condition. In Write with restart operation, master will generate another start condition after transmitting the slave address and data. If slave needs stop condition between data and restart command (Sr) in the Random read operation, software can transmit the Current address read operation following A Write operation. The maximum value of data FIFO (N) is 24. The slave address byte will be written into FIFO register together with data. Software must write the eighth bit of slave address byte to decide the access is read or write.

NOTE:

- (a) RTD2485XD only supports master and slave function
- (b) RTD2485XD doesn't support arbitration mechanism while one system exists over 2 masters
- (c) FIFO can't support R/W at the same time. It means that you can't transmit data successively while the byte counts over 24, since MCU have to refresh the FIFO data for the next transmit
- (d) Master supports the function that slave can hold SCL to zero after ACK when slave can't give master data that master wanted.

Signal Name	Type	Function	Note
SCL	O		
SDA	I/O		



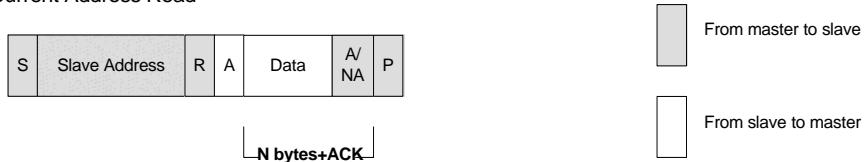
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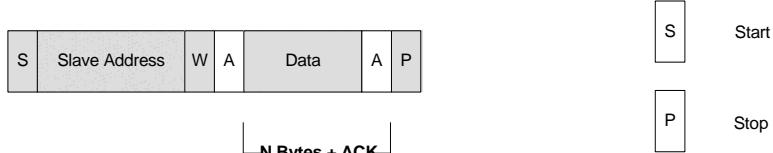
Random Read



Current Address Read



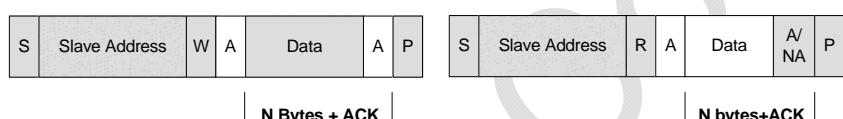
Write



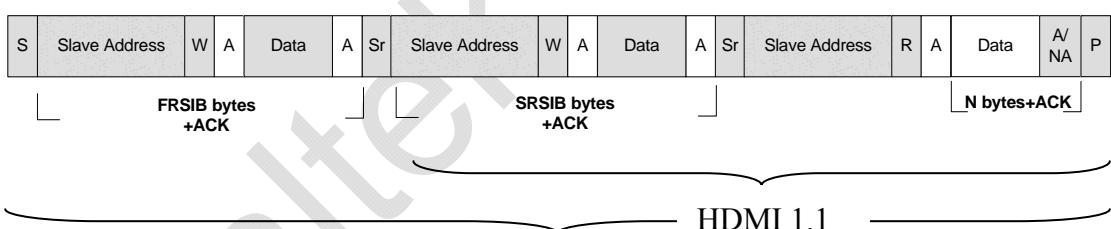
Write with restart



Write + Current Address Read



Read with two restart



HDMI 1.3

So we can identify whether HDMI 1.1 or 1.3 by receiving the first 2 ACK from slaves

Register:: I2CM_CR0						0xFF55	
Name	Bits	R/W	Default	Comments			Config
IICM_SW_RSTN	7	R/W	0	IIC master software reset 0: Reset, Blocking IICM module 1: Enable IICM module			
CS	6	R/W	0	Command Start 0 = Stop, after completing whole transaction, it returns to zero 1 = Start			wport rport



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RWL	5:1	R/W	0	Read/Write data Length for related commands. Not includes slave address byte in FIFO register. When access, controller will parse the byte followed last start (or Sr) byte to know the command type. 0x00 = 1 bytes : 0x17 = 24 bytes	
TORE	0	R/W	1	TOR enable If TOR is desired, I2C rate must be constrained form 25kb/s~ 400kb/s. This constraint is due to the time-out register bit.	

Register:: I2CM_CR1					0xFF56
Name	Bits	R/W	Default	Comments	Config
TOR	7:0	R/W	0x3A	Time-out register Time-out = TOR x 2 x ((FD10+1)/input clock) (For receive/transmit one bit) If time-out occur, it will trigger Transaction Error Interrupt Flag Note: time-out must > (1 SCL low period + repeat start setup time)	

Register:: I2CM_CR2					0xFF57
Name	Bits	R/W	Default	Comments	Config
reserved	7	-	0	Reserved to 0	
BURST	6	R/W	0	Burst mode enabled to write over 24 bytes to slave devices. While burst is enabled, whole I2C will be halted to let MCU write another more bytes to FIFO. After the job done, we have to set I2CM_SR to be high to continue the I2C write job	
SBAIFD	5	R/W	0	Second byte ACK in FRSIB data (for identifying HDMI 1.3 needed) SBAIFD indicates that whether master checks ACK from slave or not after emitting second data in FRSIB data. 0: To check 1: Not check	
FBAIFD	4	R/W	0	First byte ACK in FRSIB data (for identifying HDMI 1.3 needed) FBAIFD indicates that whether master checks ACK from slave or not after emitting first data in FRSIB data. 0: To check 1: Not check	
SRSIB	3:2	R/W	0	Second repeat start interval byte (For HDMI need) After transmitting SRSIB bytes that, include slave address & data bytes, follow the first repeat start command, the master will produce second repeat start command. The slave address or device address byte is included in this interval. Default interval is one byte. 0 = 1 bytes; 1=2 byte etc. Note: The eighth bit of slave address or device address byte followed by second repeat start command must be Read.	
FRSIB	1:0	R/W	0	First repeat start interval byte (For HDMI need) After transmitting FRSIB bytes that, include slave address & data bytes, follow the original start command, the master will produce first repeat start command. The original slave address or device address byte is included	



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			in this interval. Default interval is one byte. 0 = 1 bytes; 1=2 bytes, etc.	
--	--	--	--	--

Register:: I2CM_CR3					0xFF58
Name	Bits	R/W	Default	Comments	Config
reserved	7:5	-	0	Reserved to 0	
RSC	4:3	R/W	0	Repeat start count 00: No repeat start 01: one repeat start 10: two repeat start 11: forbidden	
TEIE	2	R/W	0	Transaction Error Interrupt Enable	
MRCIE	1	R/W	0	Master Receive complete Interrupt Enable	
MTCIE	0	R/W	0	This Interrupt enable bit serve two conditions, one is “Master Transmit complete Interrupt Enable in single mode” and the other is “Master Transmit partial Done Interrupt Enable in burst mode”	

Register:: I2CM_STR0					0xFF59
Name	Bits	R/W	Default	Comments	Config
reserved	7	-	0	Reserved to 0	
I2CMD	6:4	R/W	0	I2C master debounce 0: sample rate=(input clk / (FD10+1)) 1: sample rate=(input clk / (FD10+1)) / 2 : 7: sample rate= (input clk / (FD10+1)) / 8	
FTPC	3:0	R/W	0x3	Fall time period count If the value of (Bus clock/FD10) does not approximate 10Mhz, FTPC can make sure that fall time of SCL is more than 300ns.	

Register:: I2CM_STR1					0xFF5A
Name	Bits	R/W	Default	Comments	Config
STA_SUGPIO_C	7:0	R/W	0x09	STA setup time period count In repeat start, the setup time of SCL must match the I2C spec.	

Register:: I2CM_STR2					0xFF5B
Name	Bits	R/W	Default	Comments	Config
SHPC	7:0	R/W	0x09	SCL high period counter (SCL High period=100ns*SHPC) SHPC must include rising time in the I2C spec.	

Register:: I2CM_STR3					0xFF5C
Name	Bits	R/W	Default	Comments	Config
SLPC	7:0	R/W	0x10	SCL low period counter (SCL low period=100ns*SLPC) SLPC must include falling time in the I2C spec.	

Register:: I2CM_SR					0xFF5D
Name	Bits	R/W	Default	Comments	Config
reserved	7:5	-	0	Reserved to 0	



BSA	4	R/W	0	Send again Control bit in burst mode 1: Send 0: Not action Write “1” to clear	wport rport
BMPIF	3	R/W	0	Burst Mode Pending Interrupt Flag While setting as burst mode and I2C master transmit data in TDD , this flag is asserted. Write “1” to clear	wport rport
TEIF	2	R/W	0	Transaction Error Interrupt Flag When master transmit/receive fault or time-out occurrence, I2C controller will lift the flag up and return to bus idle. Write “1” to clear	wport rport
MRCIF	1	R/W	0	Master Receive complete Interrupt flag Write “1” to clear	wport rport
MTCIF	0	R/W	0	This Interrupt enable bit serves two conditions, one is “Master Transmit complete Interrupt Enable in single mode” and the other is “Master Transmit partial Done Interrupt Enable in burst mode” Write “1” to clear	wport rport

Register:: I2CM_TD					0xFF5E
Name	Bits	R/W	Default	Comments	Config
TDD	7:0	R/W	0	Target Device Data to receive or transmit	wport rport

Register:: I2CM_CCR					0xFF5F
Name	Bits	R/W	Default	Comments	Config
reserved	7:6	-	0	Reserved to 0	
FD10	5:0	R/W	0x01	Frequency 10M Divisor 0 are forbidden 10M=input clock/(FD10+1) When power on, software must write FD10 to let I2C controller generate ~10 Mhz clock.	



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MCU Register2(Page E) SPI-FLASH**Common Instruction Register**

Register::common_inst_en						0xFF60
Name	Bits	R/W	Default	Comments		Config
com_inst	7:5	R/W	0x0	000: no operation 001 : write 010 : Read 011 : write after WREN 100 : write after EWSR 101 : Erase		
write_num	4:3	R/W	0x0	Common instruction write number		
rd_num	2:1	R/W	0x0	Common instruction read number		
com_inst_en	0	R/W	0x0	Common instruction enable (auto clear when finish)		Wport Rport

Register::common_op_code						0xFF61
Name	Bits	R/W	Default	Comments		Config
com_op	7:0	R/W	0x0	Common instruction op code		

Register::wren_op_code						0xFF62
Name	Bits	R/W	Default	Comments		Config
wren_op	7:0	R/W	0x06	Write enable op code		

Register::ewsr_op_code						0xFF63
Name	Bits	R/W	Default	Comments		Config
ewsr_op	7:0	R/W	0x50	Enable write register op code		



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Register::Flash_prog_ISP0						0xFF64	
Name	Bits	R/W	Default	Comments			Config
prog_h	7:0	R/W	0x00	Flash program/write/dummy/read byte[23:16]	CRC	high	Wport Rport

Register::Flash_prog_ISP1						0xFF65	
Name	Bits	R/W	Default	Comments			Config
prog_m	7:0	R/W	0x00	Flash program/write/dummy/read byte[15:8]	CRC	middle	Wport Rport

Register::Flash_prog_ISP2						0xFF66	
Name	Bits	R/W	Default	Comments			Config
prog_l	7:0	R/W	0x00	Flash program/write/dummy/read byte[7:0]	CRC	low	Wport Rport

Register::common_inst_read_port0						0xFF67	
Name	Bits	R/W	Default	Comments			Config
com_rd_h	7:0	R	0x00	Common instruction read high byte[23:16]			

Register::common_inst_read_port1						0xFF68	
Name	Bits	R/W	Default	Comments			Config
com_rd_m	7:0	R	0x00	Common instruction read middle byte[15:8]			

Register::common_inst_read_port2						0xFF69	
Name	Bits	R/W	Default	Comments			Config
com_rd_l	7:0	R	0x00	Common instruction read low byte[7:0]			

Common Instruction Usage :

1. Set common instruction type.
2. Set common instruction OP code.
3. Set write number (0 ~ 3).
4. Set read number if common instruction type is read.
5. Write data to **Flash_prog_write_dum_readCRC_ISP** if write number > 0 .



6. Execution common instruction enable.
7. Polling common instruction enable in ISP mode → If it is finished and the instruction is read, read the Data in **common_inst_read_port**.
8. It would auto clear in normal mode. Then read the Data in **common_inst_read_port** if the instruction type is read.

Common Instruction Setting Example :

Write function

	com_op	write_num=0				rd_num =0			
WREN	06h	X	X	X	X	X	X	X	X
WRDI	04h	X	X	X	X	X	X	X	X
EWSR	50h	X	X	X	X	X	X	X	X
DP	B9h	X	X	X	X	X	X	X	X
RDP	ABh	X	X	X	X	X	X	X	X

Read function

write_num =0 , rd_num=3

	com_op	rd_num setting					
RDID	9Fh	ID23-ID16	ID15-ID8	ID7-ID0			
JEDEC ID READ*1	9Fh	ID2	ID1	Device ID			

write_num=0, rd_num=1

RDCR	A1h	RD_CR					
RDSR	05h	RD_SR					

write_num=3, rd_num=1 or 2

RES	ABh	DUMMY	DUMMY	DUMMY	Electronic Signature		
REMS	90h	DUMMY	DUMMY	00h	ID	Device ID	

Write after WREN function

	com_op	write_num=1	rd_num=0				
WRSR	01h	WR_SR					

Write after WRSSR function

	com_op	write_num=1	rd_num=0				



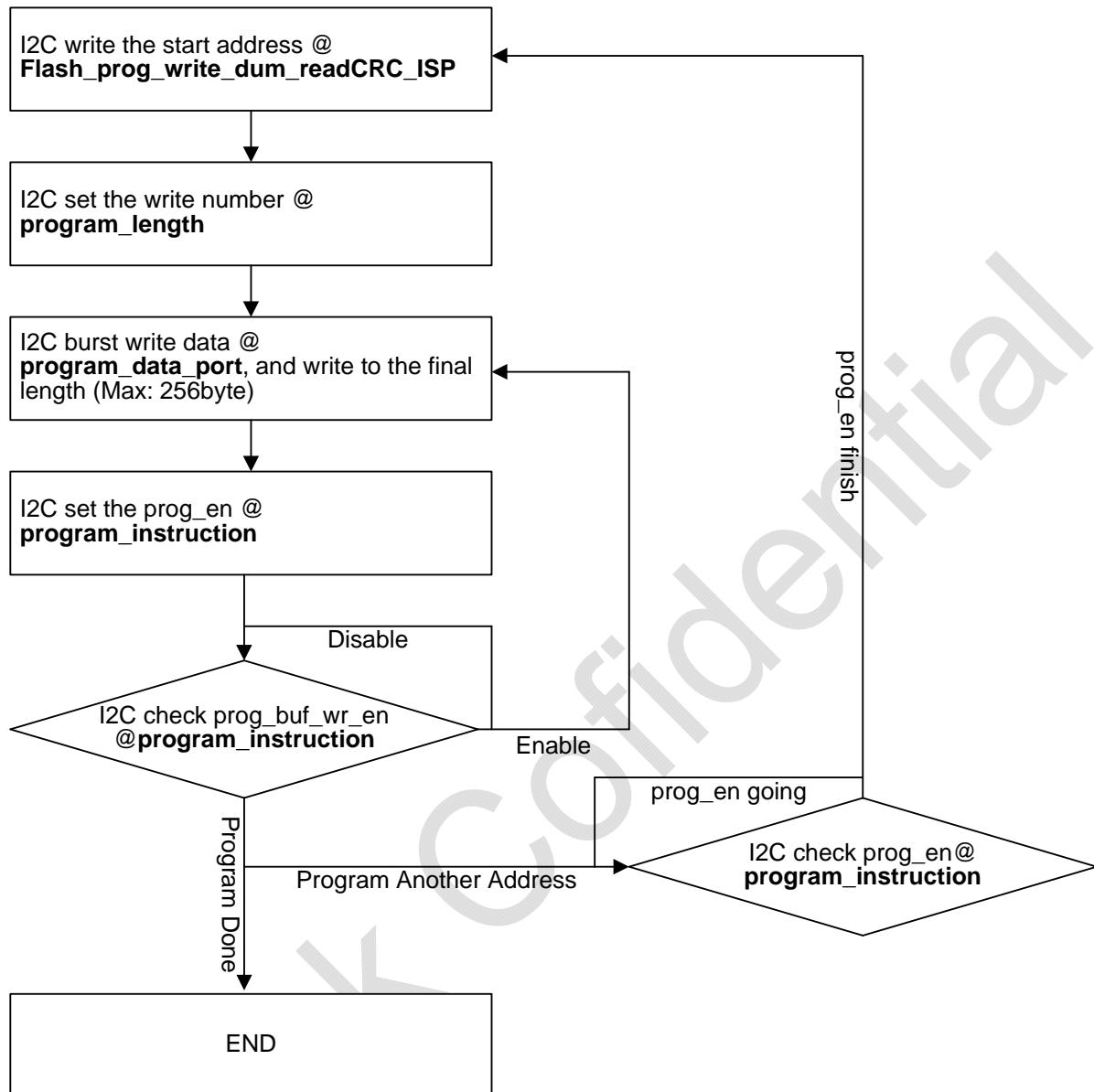
WRCR	F1h	WR_CR					
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Erase function

	com_op	write_num = 0 or 3			rd_num=0		
SECTOR_ER (4k byte)	20h	AD1	AD2	AD3			
BLOCK_ER (64k byte)	D8h	AD1	AD2	AD3			
Page Erase	DBh	AD1	AD2	AD3			
CHIP_ER	C7h						

Program/Read/ISP/CRC Register

ISP Protocol of Program Data :



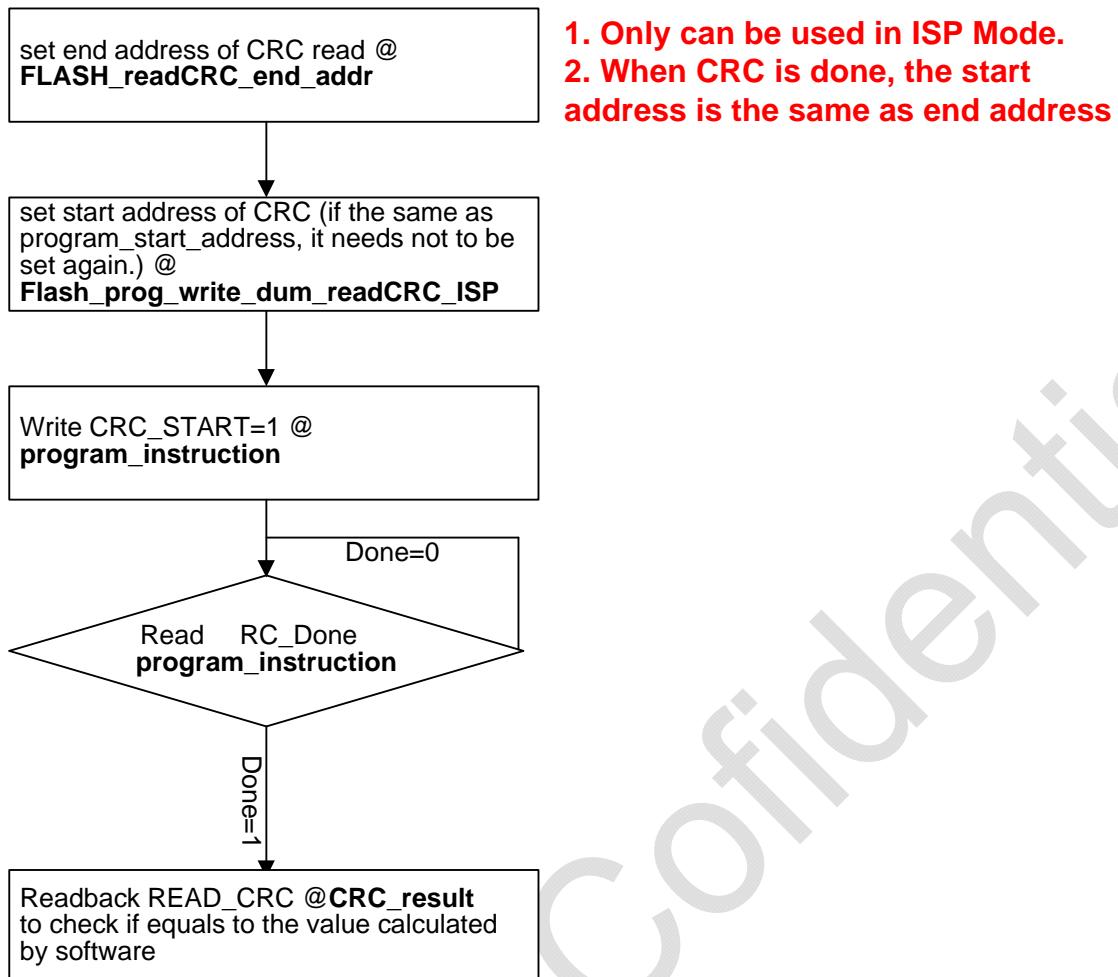
In SPI Mode

1. We use two 256 bytes buffer for Program.
2. We write buffer by DDC Channel.
3. We auto switch two buffer during program.
→ If `prog_buf_wr_en = 1`, you can keep write data to buffer.

In Normal mode

1. We use one 256 bytes buffer for Program.
2. We write buffer by uP.
3. We only use one buffer during program.
→ We can program Max. 256 bytes one time.

Protocol of CRC of read Data :



Register:::read_op_code 0xFF6A					
Name	Bits	R/W	Default	Comments	Config
read_op	7:0	R/W	0x03	Read command op code	Wen_out

Note : 1 It would force flash controller to idle state when write this byte.

Register:::fast_read_op_code 0xFF6B					
Name	Bits	R/W	Default	Comments	Config
Fast_read_op	7:0	R/W	0x0B	Fast read command op code	Wen_out

Note : 1 It would force flash controller to idle state when write this byte.

Register:::read_instruction 0xFF6C					
Name	Bits	R/W	Default	Comments	Config



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read_mode	7:6	R/W	0x0	00: normal read 01: fast read 10: fast dual data read	Wen_out
latch_so_rise	5	R/W	0x0	0: latch Flash SO Data in rising edge 1: latch Flash SO Data in falling edge	Wen_out
drive_si_fall	4	R/W	0x0	0: Output Flash SI Data in falling edge 1: Output Flash SI Data in rising edge	Wen_out
si_dly_sel	3:2	R/W	0x0	00: 0ns 01: 2ns 10: 4ns 11: 6ns	Wen_out
Reserved	1:0	R/W	0x0	00: 0ns 01: Reserved 10: Reserved 11: Reserved	Wen_out

Note: 1. Normally, SPI Flash drive data in falling edge and sample data in rising edge !!!!

2. It would force flash controller to idle state when write this byte.

Register::program_op_code 0xFF6D					
Name	Bits	R/W	Default	Comments	Config
prog_op	7:0	R/W	0xff	Program command op code	

Register::read_status_register_op_code 0xFF6E					
Name	Bits	R/W	Default	Comments	Config
rdsr_op	7:0	R/W	0x05	Read status register register command op code	

Register::program_instruction 0xFF6F					
Name	Bits	R/W	Default	Comments	Config
isp_en	7	R/W	0x0	Enable ISP program : all registers except this register can't write/read when ISP_ENABLE=0 0: disable 1: enable (gating 8051 clock)	Rport Wport
prog_mode	6	R/W	0x0	0: normal mode (other select reference 0xFF6F[3]) 1: AAI mode	



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prog_en	5	R/W	0x0	0: finish 1: program on-going (write 1 to start, auto clear when finish)	Rport Wport
prog_buf_wr_en	4	R	0x1	0: can't write data to sram 1: can write data to sram	
Prog_normal_mode	3	R/W	0x0	Program normal mode select 0: page program (1byte OP code + 3byte address + N byte data) 1: single byte program , hardware implement single byte write (1Byte OP + 3Byte Addr + Data0, 1Byte OP + 3Byte Addr + Data1, ...)	
crc_start	2	R/W	0x0	When write one, read data from PROG_ST_ADDR to PROG_END_ADDR. And at the same time the CRC is calculated by IC automatically. This bit will be auto cleared when crc_done is 1.(Can be trigger in ISP Mode only)	Rport Wport
crc_done	1	R	0x1	It will show 1 when CRC is done, and will return to 0 when CRC_START is set.	
rst_flash_ctrl	0	R/W	0x0	0: disable 1: software reset flash controller	Rport Wport

No Use Parser::program_data_port 0xFF70					
Name	Bits	R/W	Default	Comments	Config
prog_port	7:0	W		Program write data port to SRAM	

Register::program_length 0xFF71					
Name	Bits	R/W	Default	Comments	Config
prog_length	7:0	R/W	0xFF	Program write number	

Register::CRC_end_addr0 0xFF72					
Name	Bits	R/W	Default	Comments	Config



rdcrc_end_addr_h	7:0	R/W	0x00	Read CRC end address high byte [23:16]	
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Register::CRC_end_addr1 0xFF73					
Name	Bits	R/W	Default	Comments	Config
rdcrc_end_addr_m	7:0	R/W	0x00	Read CRC end address middle byte [15:8]	

Register::CRC_end_addr2 0xFF74					
Name	Bits	R/W	Default	Comments	Config
rdcrc_end_addr_l	7:0	R/W	0x00	Read CRC end address low byte [7:0]	

Register::CRC_result 0xFF75					
Name	Bits	R/W	Default	Comments	Config
crc_result	7:0	R	-	CRC value of data between PROG_ST_ADDR and RDCRC_END_ADDR	

Flash timing Register

Register::cen_ctrl 0xFF76					
Name	Bits	R/W	Default	Comments	Config
cen_high_num	7:4	R/W	0x9	Chip enable high number[3:0] (based on flash clock) Cycle : 1 ~ 16 (0x0 ~ 0xF)	Wen_out
cen_setup_num	3:2	R/W	0x0	Chip enable setup number (based on flash clock) Cycle : 0.5 ~ 3.5 Cycle : 1 ~ 4 (if drive_si_fall)	Wen_out
cen_hold_num	1:0	R/W	0x0	Chip enable hold number (based on flash clock) Cycle : 1 ~ 4 Cycle : 0.5 ~ 3.5 (if drive_si_fall)	Wen_out

Note : 1 It would force flash controller to idle state when write this byte.

Register::AAI_Mode_Byte_Num 0xFF80					
Name	Bits	R/W	Default	Comments	Config



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AAI_Mode_Byte_Num	7:0	R/W	0x1	SST flash, AAI mode, transfer number 0x00: transfer 1 byte 0x01: transfer 1byte 0x02: transfer 2bytes and so on	
-------------------	-----	-----	-----	---	--

Register::ISP_CMD_INSERT					0xFF81
Name	Bits	R/W	Default	Comments	Config
Reserved	7:6	R/W	0	Reserved	
ISP_CMD_WAIT_RESO_M0	5:4	R/W	0	cmd wait time resolution, m0 divider divide value = 2^{m0} 00: divide 1 01: divide 2 10: divide 4 11: divide 8	
ISP_CMD_WAIT_RESO_M1	3:1	R/W	0	cmd wait time resolution, m1 divider divide value = 2^{m1}	
ISP_CMD_INSERT_EN	0	R/W	0	Enable insert CMD before isp program 0: disable 1: enable	

Register::ISP_CMD_LENGTH					0xFF82
Name	Bits	R/W	Default	Comments	Config
ISP_CMD_LENGTH	7:0	R/W	0xFF	Total max length of ISP CMD: 0x00: length=1 0x01: length=2 ... 0xFF: length=256	

ISP Command Format:

cmd_length(=1+n1) + cmd_wait_length + cmd_opcode + n1 byte data

cmd_length(=1+n2) + cmd_wait_length + cmd_opcode + n2 byte data

...

cmd_length=0 (end)

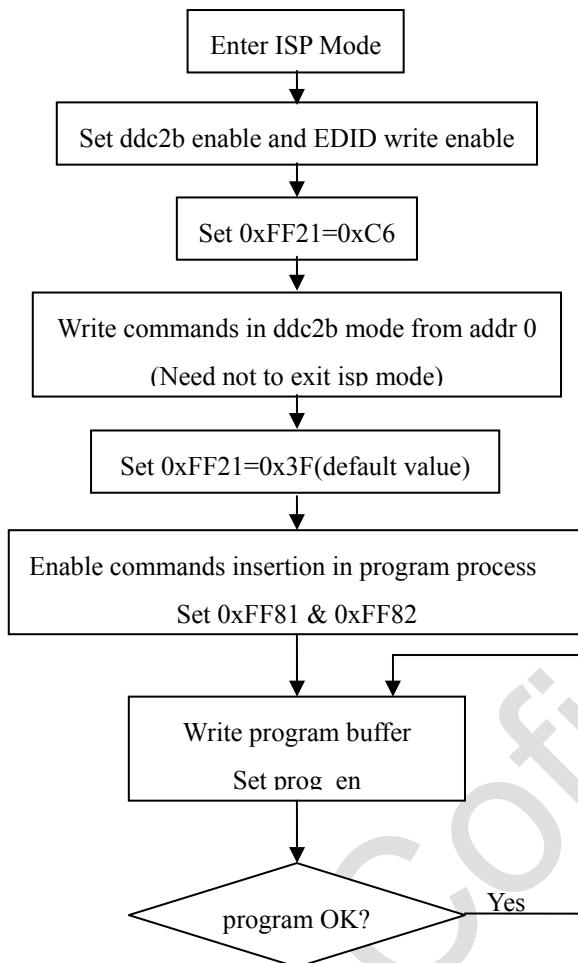
wait time = cmd_wait_length * $2^{m1} * 2^{m0} * (\text{flash_clk period})$

wait time is inserted after current command execution

**Example:**

01 00 06 → opcode=0x06, no data, no wait time
02 80 01 7C → opcode=0x01, data=0x7C, wait time= $128 * 2^{m1} * 2^{m0} * (\text{flash_clk period})$
01 00 C3 → opcode=0xC3, no data, no wait time
01 00 A5 → opcode=0xA5, no data, no wait time
01 00 C3 → opcode=0xC3, no data, no wait time
01 00 A5 → opcode=0xA5, no data, no wait time
01 00 06 → opcode=0x06, no data, no wait time
02 FF 01 00 → opcode=0x01, data=0x00, wait time= $255 * 2^{m1} * 2^{m0} * (\text{flash_clk period})$
00 → end

To execute the above 8 commands, you need to write 27 bytes to RAM at one time.



ISP command insertion program flow (e.g. for MXIC new flash)

MCU Register2(Page E) I2C Slave Module

The RTD2220 supports the I2C-bus specification for functional control. This I2C slave supports programmable slave address and max. bit rate of 400Kbps. With this interface, external I2C master, ex. MCU, can communicate with RTD2220 for specific application. The following working scenario is as an example. I2C master issues the read command to poll the system status, **I2CS_SW_STATUS** and as the **busy** bit is 0, MCU can issue the WRITE command for some request which is supported by RTD2220. After received the I2C WRITE command, the **busy** bit of this I2C slave module is asserted, and after finish the WRITE transaction (with STOP condition), **wcmdfsh** bit is set also to inform CPU to parse and decode the command and/or parameters stored in 16-bytes data FIFO. In the case of data length is larger than 16 bytes in th I2C WRITE command, this I2C slave will not ACKnowledge the transaction to inform the I2C master that



RTD2220 do not receive this command well and asserts the **data_of** bit to inform CPU also. Otherwise, after completing WRITE command decoding and further operations, CPU stores the data that I2C master requested into the data FIFO and clear **busy** bit. During RTD2220 processed the WRITE command, I2C master shall poll the status(the status byte return to I2C master is I2CS_SW_STATUS[7:0]) periodically. As the RTD2220's processing is completed, the status with “**NOT BUSY**” and data will be transmitted to I2C master at the same time. In addition, the I2C slave can be used to wake up CPU as system enters the power-saving mode. In order to implement this function, CPU shall set **wcmdfsh_ie** to 1 before entering power-saving mode and some I2C master issues one write command to RTD2220 that will trigger interrupt to wake up CPU. In order to enhance the compatibility and noise rejection, debounce circuit and re-time function are included in this I2C slave module. Re-time function can be used to adjust the SCL finely to prevent fault Start or Stop condition because of skew between SCL and SDA after the de-bounce processing. Note that re-start condition is not supported in this I2C slave module.

I2C Master and I2C Slave share the same fifo. When Slave 1 is enabled, TDD (0xFF5E) of I2C master 1 is used to access fifo data. When Slave 2 is enabled, TDD_2 (0xFF81) of I2C master 2 is used to access fifo data.

Write

S	Slave ID	W	A C K	Cmd	A C K	Parameter	AC K/ NA K	P
---	----------	---	-------------	-----	-------------	-----------	---------------------	---

N bytes+ACK

Read (RDY = 0)

S	Slave ID	R	A C K	Status	AC K/ NA K	P
---	----------	---	-------------	--------	---------------------	---

Read (RDY = 1)

S	Slave ID	R	A C K	Status	AC K/ NA K	Data	AC K/ NA K	P
---	----------	---	-------------	--------	---------------------	------	---------------------	---

N bytes+ACK



REALTEK

RTD2261W/2271W/2281W Series-GR

Name	Bits	R/W	Default	Comments	Config
SLVID	7:1	R/W	0x38	Slave ID	
I2CS_EN	0	R/W	0	I2C slave module enable 1: Enable 0: Disable	

Register:: I2CS_CTRL1 0xFF84					
Name	Bits	R/W	Default	Comments	Config
TIMEOUT_VAL	7:0	R/W	0x00	Timeout = TIMEOUT_VAL * Tcrystal * 8	

Register:: I2CS_CTRL2 0xFF85					
Name	Bits	R/W	Default	Comments	Config
WCMDFSH_IE	7	R/W	0	Interrupt enable bit for WCMDFSH status	
CMDERR_IE	6	R/W	0	Interrupt enable bit for CMDERR status	
TIMEOUT_IE	5	R/W	0	Interrupt enable bit for TIMEOUT status	
BUSY_IE	4	R/W	0	Interrupt enable bit for BUSY status	
DEBOUNCE_M	3:2	R/W	0	Debounce Mode: 00: 3 clock debounce 01: 2 clock debounce 10: 1 clock debounce 11: 0 clock debounce	
RESET	1	R	0	Whether i2c slave has been reset before. It is cleared by the sw_status read from i2c bus. 0: no reset event happens. 1: once reset (by any reset).	
TIMEOUT_EN	0	R/W	0	Timeout function enable bit. When enable, the internal time_cnt will start counting, and is reset to zero every the ACK bit occurs. A timeout status bit is set when internal time_cnt reaches the timeout_val.	

Register:: I2CS_STATUS0 0xFF86					
Name	Bits	R/W	Default	Comments	Config
CMDFSM	7:0	R	-	I2C Slave Command FSM	

Register:: I2CS_STATUS1 0xFF87					
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Name	Bits	R/W	Default	Comments	Config
WCMDFSH	7	R/W	0	Write command finish status	Wport Rport
DATA_OF	6	R	0	Number of data bytes received from i2c bus write command Overflow (>16)	
CMDERR	5	R/W	0	Command Error Status	Wport Rport
TIMEOUT	4	R/W	0	Timeout Write 1 clear by cpu.	Wport Rport
BUSY	3	R/W	0	Internal system is busy responding to the commands sent before. Only i2c bus write command will set this bit. Write 1 clear by cpu. 0: not busy 1: busy	Wport Rport
RETIME_M	2:0	R/W	0	Retime Mode: 000: no delay Others: SDA delay N clock, N = RETIME_M	

Register:: I2CS_BUflen						0xFF88
Name	Bits	R/W	Default	Comments	Config	
I2CS_sw_rstn	7	R/W	1	IIC slave software reset 0: Reset, Data buffer point 1: Enable IICS module	Wport Rport	
Reserved	6:5	-	-			
DATA_LEN	4:0	R	-	Number of data bytes received from i2c bus write command.		



REALTEK

RTD2261W/2271W/2281W Series-GR

MCU Register2 (Page E) PWM

Register::PWM01_TOTALCNT_MSB						0xFF90
Name	Bits	R/W	Default	Comments		Config
PWM1H_TOTALCNT	7:4	R/W	0	PWMx , total level count MSB[11:8]		wport rport
PWM0H_TOTALCNT	3:0	R/W	0	PWMx , total level count MSB[11:8]		wport rport

Register::PWM0_TOTALCNT_LSB						0xFF91
Name	Bits	R/W	Default	Comments		Config
PWM0L_TOTALCNT	7:0	R/W	0	PWMx , total level count LSB[7:0]		wport rport

Register::PWM1_TOTALCNT_LSB						0xFF92
Name	Bits	R/W	Default	Comments		Config
PWM1L_TOTALCNT	7:0	R/W	0	PWMx , total level count LSB[7:0]		wport rport

Register::PWM23_TOTALCNT_MSB						0xFF93
Name	Bits	R/W	Default	Comments		Config
PWM3H_TOTALCNT	7:4	R/W	0	PWMx , total level count MSB[11:8]		wport rport
PWM2H_TOTALCNT	3:0	R/W	0	PWMx , total level count MSB[11:8]		wport rport

Register::PWM2_TOTALCNT_LSB						0xFF94
Name	Bits	R/W	Default	Comments		Config
PWM2L_TOTALCNT	7:0	R/W	0	PWMx , total level count LSB[7:0]		wport rport

Register::PWM3_TOTALCNT_LSB						0xFF95
Name	Bits	R/W	Default	Comments		Config
PWM3L_TOTALCNT	7:0	R/W	0	PWMx , total level count LSB[7:0]		wport rport

Register::PWM45_TOTALCNT_MSB						0xFF96
Name	Bits	R/W	Default	Comments		Config
PWM5H_TOTALCNT	7:4	R/W	0	PWMx , total level count MSB[11:8]		wport rport
PWM4H_TOTALCNT	3:0	R/W	0	PWMx , total level count MSB[11:8]		wport



REALTEK

RTD2261W/2271W/2281W Series-GR

rport

Register::PWM4_TOTALCNT_LSB						0xFF97
Name	Bits	R/W	Default	Comments	Config	
PWM4L_TOTALCNT	7:0	R/W	0	PWMx , total level count LSB[7:0]	wport rport	

Register::PWM5_TOTALCNT_LSB						0xFF98
Name	Bits	R/W	Default	Comments	Config	
PWM5L_TOTALCNT	7:0	R/W	0	PWMx , total level count LSB[7:0]	wport rport	

Register::PWM_CK_SEL_HS						0xFF99
Name	Bits	R/W	Default	Comments	Config	
PWM_CK_SEL_HS_DUMMY	7:6	R/W	0	Dummy		
PWM5_CK_SEL_HS	5	R/W	0	PWMx clock generator input source 0: reference PWM5_CK_SEL 1: using DHS as reference clock The total level count is {PWM5H_TOTALCNT, PWM5L_TOTALCNT}, high level count is {PWM5H_DUT, PWM5L_DUT}, and limited H/L transition number by PWM5_CYCLE_MAX		
PWM4_CK_SEL_HS	4	R/W	0	PWMx clock generator input source 0: reference PWM4_CK_SEL 1: using DHS as reference clock The total level count is {PWM4H_TOTALCNT, PWM4L_TOTALCNT}, high level count is {PWM4H_DUT, PWM4L_DUT}, and limited H/L transition number by PWM4_CYCLE_MAX		
PWM3_CK_SEL_HS	3	R/W	0	PWMx clock generator input source 0: reference PWM3_CK_SEL 1: using DHS as reference clock The total level count is {PWM3H_TOTALCNT, PWM3L_TOTALCNT}, high level count is {PWM3H_DUT, PWM3L_DUT}, and H/L transition number is limited by PWM3_CYCLE_MAX		
PWM2_CK_SEL_HS	2	R/W	0	PWMx clock generator input source 0: reference PWM2_CK_SEL 1: using DHS as reference clock The total level count is {PWM2H_TOTALCNT, PWM2L_TOTALCNT}, high level count is {PWM2H_DUT, PWM2L_DUT}, and H/L transition number is limited by PWM2_CYCLE_MAX		



REALTEK

RTD2261W/2271W/2281W Series-GR

PWM1_CK_SEL_HS	1	R/W	0	PWMx clock generator input source 0: reference PWM1_CK_SEL 1: using DHS as reference clock The total level count is {PWM1H_TOTALCNT , PWM1L_TOTALCNT }, high level count is {PWM1H_DUT, PWM1L_DUT}, and H/L transition number is limited by PWM1_CYCLE_MAX	
PWM0_CK_SEL_HS	0	R/W	0	PWMx clock generator input source 0: reference PWM0_CK_SEL 1: using DHS as reference clock The total level count is {PWM0H_TOTALCNT , PWM0L_TOTALCNT }, high level count is {PWM0H_DUT, PWM0L_DUT}, and H/L transition number is limited by PWM0_CYCLE_MAX	

Register:::PWM01_CYCLE_MAX						0xFF9A
Name	Bits	R/W	Default	Comments	Config	
PWM0_CYCLE_MAX	7:4	R/W	0	PWM0 maximum H/L cycle count Output PWM0 clock cycle number between two DVS. When set to 0, there is no limitation. This setting can only make effect by using DHS as reference clock		
PWM1_CYCLE_MAX	3:0	R/W	0	PWM1 maximum H/L cycle count Output PWM1 clock cycle number between two DVS. When set to 0, there is no limitation. This setting can only make effect by using DHS as reference clock		

Register:::PWM23_CYCLE_MAX						0xFF9B
Name	Bits	R/W	Default	Comments	Config	
PWM2_CYCLE_MAX	7:4	R/W	0	PWM2 maximum H/L cycle count Output PWM2 clock cycle number between two DVS. When set to 0, there is no limitation. This setting can only make effect by using DHS as reference clock		
PWM3_CYCLE_MAX	3:0	R/W	0	PWM3 maximum H/L cycle count Output PWM3 clock cycle number between two DVS. When set to 0, there is no limitation. This setting can only make effect by using DHS as reference clock		

Register:::PWM45_CYCLE_MAX						0xFF9C
Name	Bits	R/W	Default	Comments	Config	



REALTEK

RTD2261W/2271W/2281W Series-GR

PWM4_CYCLE_MAX	7:4	R/W	0	PWM4 maximum H/L cycle count Output PWM4 clock cycle number between two DVS. When set to 0, there is no limitation. This setting can only make effect by using DHS as reference clock	
PWM5_CYCLE_MAX	3:0	R/W	0	PWM5 maximum H/L cycle count Output PWM5 clock cycle number between two DVS. When set to 0, there is no limitation. This setting can only make effect by using DHS as reference clock	



MCU register 3 (page F)

GPIO Control

Register::PortD7_pin_reg						0xFF77
Name	Bits	R/W	Default	Comments	Config	
Reserved	7:1	--	0	Reserved		
PD7	0	R/W	1	Input/output value of PD.7	Rport wport	

Register::PortD6_pin_reg						0xFF78
Name	Bits	R/W	Default	Comments	Config	
Reserved	7:1	--	0	Reserved		
PD6	0	R/W	1	Input/output value of PD.6	Rport wport	

Register::PortD5_pin_reg						0xFF79
Name	Bits	R/W	Default	Comments	Config	
Reserved	7:1	--	0	Reserved		
PD5	0	R/W	1	Input/output value of PD.5	Rport wport	

Register::PortD4_pin_reg						0xFF7A
Name	Bits	R/W	Default	Comments	Config	
Reserved	7:1	--	0	Reserved		
PD4	0	R/W	1	Input/output value of PD.4	Rport wport	



Register::PortD3_pin_reg						0xFF7B
Name	Bits	R/W	Default	Comments	Config	
Reserved	7:1	--	0	Reserved		
PD3	0	R/W	1	Input/output value of PD.3	Rport wport	

Register::PortD2_pin_reg						0xFF7C
Name	Bits	R/W	Default	Comments	Config	
Reserved	7:1	--	0	Reserved		
PD2	0	R/W	1	Input/output value of PD.2	Rport wport	

Register::PortD1_pin_reg						0xFF7D
Name	Bits	R/W	Default	Comments	Config	
Reserved	7:1	--	0	Reserved		
PD1	0	R/W	1	Input/output value of PD.1	Rport wport	

Register::PortD0_pin_reg						0xFF7E
Name	Bits	R/W	Default	Comments	Config	
Reserved	7:1	--	0	Reserved		
PD0	0	R/W	1	Input/output value of PD.0	Rport wport	

Register::PortB7_pin_reg						0xFF7F
Name	Bits	R/W	Default	Comments	Config	
Reserved	7:1	--	0	Reserved		



REALTEK

RTD2261W/2271W/2281W Series-GR

PB7	0	R/W	1	Input/output value of PB.7	Rport wport
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Register::PortB6_pin_reg						0xFF89
Name	Bits	R/W	Default	Comments	Config	
Reserved	7:1	--	0	Reserved		
PB6	0	R/W	1	Input/output value of PB.6	Rport wport	

Register::PortB5_pin_reg						0xFF8A
Name	Bits	R/W	Default	Comments	Config	
Reserved	7:1	--	0	Reserved		
PB5	0	R/W	1	Input/output value of PB.5	Rport wport	

Register::PortB4_pin_reg						0xFF8B
Name	Bits	R/W	Default	Comments	Config	
Reserved	7:1	--	0	Reserved		
PB4	0	R/W	1	Input/output value of PB.4	Rport wport	

Register::PortB3_pin_reg						0xFF8C
Name	Bits	R/W	Default	Comments	Config	
Reserved	7:1	--	0	Reserved		
PB3	0	R/W	1	Input/output value of PB.3	Rport wport	

Register::PortB2_pin_reg						0xFF8D
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REALTEK

RTD2261W/2271W/2281W Series-GR

Name	Bits	R/W	Default	Comments	Config
Reserved	7:1	--	0	Reserved	
PB2	0	R/W	1	Input/output value of PB.2	Rport wport

Register::PortB1_pin_reg					0xFF8E
Name	Bits	R/W	Default	Comments	Config
Reserved	7:1	--	0	Reserved	
PB1	0	R/W	1	Input/output value of PB.1	Rport wport

Register::PortB0_pin_reg					0xFF8F
Name	Bits	R/W	Default	Comments	Config
Reserved	7:1	--	0	Reserved	
PB0	0	R/W	1	Input/output value of PB.0	Rport wport

Register::PortC3_pin_reg					0xFFA0
Name	Bits	R/W	Default	Comments	Config
Reserved	7:1	--	0	Reserved	
PC3	0	R/W	1	Input/output value of PC.3	Rport wport

Register::PortC2_pin_reg					0xFFA1
Name	Bits	R/W	Default	Comments	Config
Reserved	7:1	--	0	Reserved	



REALTEK

RTD2261W/2271W/2281W Series-GR

PC2	0	R/W	1	Input/output value of PC.2	Rport wport
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Register::PortC1_pin_reg						0xFFA2
Name	Bits	R/W	Default	Comments	Config	
Reserved	7:1	--	0	Reserved		
PC1	0	R/W	1	Input/output value of PC.1	Rport wport	

Register::PortC0_pin_reg						0xFFA3
Name	Bits	R/W	Default	Comments	Config	
Reserved	7:1	--	0	Reserved		
PC0	0	R/W	1	Input/output value of PC.0	Rport wport	

Register::PortC4_pin_reg						0xFFA4
Name	Bits	R/W	Default	Comments	Config	
Reserved	7:1	--	0	Reserved		
PC4	0	R/W	1	Input/output value of PC.4	Rport wport	

Register::Port_read_control						0xFFC0
Name	Bits	R/W	Default	Comments	Config	
PA_pin_reg_n	7	R/W	0	Source selection for PA read back 0: register 1: bus value		



REALTEK

RTD2261W/2271W/2281W Series-GR

P9_pin_reg_n	6	R/W	0	Source selection for P9 read back 0: register 1: bus value	
P8_pin_reg_n	5	R/W	0	Source selection for P8 read back 0: register 1: bus value	
P7_pin_reg_n	4	R/W	0	Source selection for P7 read back 0: register 1: bus value	
P6_pin_reg_n	3	R/W	0	Source selection for P6 read back 0: register 1: bus value	
P5_pin_reg_n	2	R/W	0	Source selection for P5 read back 0: register 1: bus value	
P3_pin_reg_n	1	R/W	0	Source selection for P3 read back* 0: register 1: bus value	
P1_pin_reg_n	0	R/W	0	Source selection for P1 read back* 0: register 1: bus value	

*: only effect in external MCU control, embedded MCU will control the source by assembly code.

Register::Port52_pin_reg						0xFFC1
Name	Bits	R/W	Default	Comments		Config
Reserved	7:1	--	0	Reserved		
P52	0	R/W	1	Input/output value of P5.2		Rport wport

Register::Port53_pin_reg						0xFFC2
Name	Bits	R/W	Default	Comments		Config
Reserved	7:1	--	0	Reserved		



REALTEK

RTD2261W/2271W/2281W Series-GR

P53	0	R/W	1	Input/output value of P5.3	Rport wport
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Register::Port54_pin_reg					0xFFC3
Name	Bits	R/W	Default	Comments	Config
Reserved	7:1	--	0	Reserved	
P54	0	R/W	1	Input/output value of P5.4	Rport wport

Register::Port55_pin_reg					0xFFC4
Name	Bits	R/W	Default	Comments	Config
Reserved	7:1	--	0	Reserved	
P55	0	R/W	1	Input/output value of P5.5	Rport wport

Register::Port56_pin_reg					0xFFC5
Name	Bits	R/W	Default	Comments	Config
Reserved	7:1	--	0	Reserved	
P56	0	R/W	1	Input/output value of P5.6	Rport wport

Register::Port57_pin_reg					0xFFC6
Name	Bits	R/W	Default	Comments	Config
Reserved	7:1	--	0	Reserved	
P57	0	R/W	1	Input/output value of P5.7	Rport wport

Register::Port60_pin_reg					0xFFC7
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REALTEK

RTD2261W/2271W/2281W Series-GR

Name	Bits	R/W	Default	Comments	Config
Reserved	7:1	--	0	Reserved	
P60	0	R/W	1	Input/output value of P6.0	Rport wport

Register::Port61_pin_reg					0xFFC8
Name	Bits	R/W	Default	Comments	Config
Reserved	7:1	--	0	Reserved	
P61	0	R/W	1	Input/output value of P6.1	Rport wport

Register::Port62_pin_reg					0xFFC9
Name	Bits	R/W	Default	Comments	Config
Reserved	7:1	--	0	Reserved	
P62	0	R/W	1	Input/output value of P6.2	Rport wport

Register::Port63_pin_reg					0xFFCA
Name	Bits	R/W	Default	Comments	Config
Reserved	7:1	--	0	Reserved	
P63	0	R/W	1	Input/output value of P6.3	Rport wport

Register::Port64_pin_reg					0xFFCB
Name	Bits	R/W	Default	Comments	Config
Reserved	7:1	--	0	Reserved	
P64	0	R/W	1	Input/output value of P6.4	Rport wport



Register::Port65_pin_reg						0xFFCC
Name	Bits	R/W	Default	Comments		Config
Reserved	7:1	--	0	Reserved		
P65	0	R/W	1	Input/output value of P6.5		Rport wport

Register::Port66_pin_reg						0xFFCD
Name	Bits	R/W	Default	Comments		Config
Reserved	7:1	--	0	Reserved		
P66	0	R/W	1	Input/output value of P6.6		Rport wport

Register::Port67_pin_reg						0xFFCE
Name	Bits	R/W	Default	Comments		Config
Reserved	7:1	--	0	Reserved		
P67	0	R/W	1	Input/output value of P6.7		Rport wport

Register::Port70_pin_reg						0xFFCF
Name	Bits	R/W	Default	Comments		Config
Reserved	7:1	--	0	Reserved		
P70	0	R/W	1	Input/output value of P7.0		Rport wport

Register::Port71_pin_reg						0xFFD0
Name	Bits	R/W	Default	Comments		Config
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REALTEK

RTD2261W/2271W/2281W Series-GR

Reserved	7:1	--	0	Reserved	
P71	0	R/W	1	Input/output value of P7.1	Rport wport

Register::Port72_pin_reg					0xFFD1
Name	Bits	R/W	Default	Comments	Config
Reserved	7:1	--	0	Reserved	
P72	0	R/W	1	Input/output value of P7.2	Rport wport

Register::Port73_pin_reg					0xFFD2
Name	Bits	R/W	Default	Comments	Config
Reserved	7:1	--	0	Reserved	
P73	0	R/W	1	Input/output value of P7.3	Rport wport

Register::Port74_pin_reg					0xFFD3
Name	Bits	R/W	Default	Comments	Config
Reserved	7:1	--	0	Reserved	
P74	0	R/W	1	Input/output value of P7.4	Rport wport

Register::Port75_pin_reg					0xFFD4
Name	Bits	R/W	Default	Comments	Config
Reserved	7:1	--	0	Reserved	
P75	0	R/W	1	Input/output value of P7.5	Rport wport



Register::Port76_pin_reg						0xFFD5
Name	Bits	R/W	Default	Comments		Config
Reserved	7:1	--	0	Reserved		
P76	0	R/W	1	Input/output value of P7.6		Rport wport

Register::Port80_pin_reg						0xFFD6
Name	Bits	R/W	Default	Comments		Config
Reserved	7:1	--	0	Reserved		
P80	0	R/W	1	Input/output value of P8.0		Rport wport

Register::Port81_pin_reg						0xFFD7
Name	Bits	R/W	Default	Comments		Config
Reserved	7:1	--	0	Reserved		
P81	0	R/W	1	Input/output value of P8.1		Rport wport

Register::Port90_pin_reg						0xFFD8
Name	Bits	R/W	Default	Comments		Config
Reserved	7:1	--	0	Reserved		
P90	0	R/W	1	Input/output value of P9.0		Rport wport

Register::Port91_pin_reg						0xFFD9
Name	Bits	R/W	Default	Comments		Config
Reserved	7:1	--	0	Reserved		



REALTEK

RTD2261W/2271W/2281W Series-GR

P91	0	R/W	1	Input/output value of P9.1	Rport wport
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Register::Port92_pin_reg					0xFFDA
Name	Bits	R/W	Default	Comments	Config
Reserved	7:1	--	0	Reserved	
P92	0	R/W	1	Input/output value of P9.2	Rport wport

Register::Port93_pin_reg					0xFFDB
Name	Bits	R/W	Default	Comments	Config
Reserved	7:1	--	0	Reserved	
P93	0	R/W	1	Input/output value of P9.3	Rport wport

Register::Port94_pin_reg					0xFFDC
Name	Bits	R/W	Default	Comments	Config
Reserved	7:1	--	0	Reserved	
P94	0	R/W	1	Input/output value of P9.4	Rport wport

Register::Porta0_pin_reg					0xFFDD
Name	Bits	R/W	Default	Comments	Config
Reserved	7:1	--	0	Reserved	
PA0	0	R/W	1	Input/output value of PA.0	Rport wport

Register::Porta1_pin_reg					0xFFDE
Name	Bits	R/W	Default	Comments	Config



REALTEK

RTD2261W/2271W/2281W Series-GR

Reserved	7:1	--	0	Reserved	
PA1	0	R/W	1	Input/output value of PA.1	Rport wport

Register::Porta2_pin_reg					0xFFDF
Name	Bits	R/W	Default	Comments	Config
Reserved	7:1	--	0	Reserved	
PA2	0	R/W	1	Input/output value of PA.2	Rport wport

Register::Porta3_pin_reg					0xFFE0
Name	Bits	R/W	Default	Comments	Config
Reserved	7:1	--	0	Reserved	
PA3	0	R/W	1	Input/output value of PA.3	Rport wport

Register::Porta4_pin_reg					0xFFE1
Name	Bits	R/W	Default	Comments	Config
Reserved	7:1	--	0	Reserved	
PA4	0	R/W	1	Input/output value of PA.4	Rport wport

SFR Access

When embedded MCU is selected, the P1, P3 GPIO is controlled by SFR. Both of the port groups must be access by below registers when using external MCU. Below registers are useless when embedded MCU is adopted.

Register::Port1_pin_reg					0xFFE2
Name	Bits	R/W	Default	Comments	Config



REALTEK

RTD2261W/2271W/2281W Series-GR

P1	7:0	R/W	0xFF	Input/output value of P1 In 8051 mode, register is READ only In ISP mode, register can be READ and WRITE.	Rport Wport
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Register::Port3_pin_reg					0xFFE3
Name	Bits	R/W	Default	Comments	Config
P3	7:0	R/W	0xFF	Input/output value of P3 In 8051 mode, register is READ only In ISP mode, register can be READ and WRITE.	Rport Wport

Register:: DVI_EDID_IRQ					0xFFE4
Name	Bits	R/W	Default	Comments	Config
SOD_ACCESS_DISABLE	7	R/W	0	0: Enable SOD Access Xram 1 : Disable SOD Access Xram	
REV_DUMMY_FFE4	6	R/W	0	Dummy	
DVI_FORCE_NACK	5	R/W	0	In DDC2B Mode, force DVI SDA no output 0:disable 1:enable	
DVI_FORCE_ACK_ZERO	4	R/W	0	In DDC2B Mode, force DVI SDA Output 0 (ACK) 0:disable 1:enable	
DVI_SCL_IRQ_EN	3	R/W	0	DVI SCL Toggle IRQ enable 0:disable 1:enable	
DVI_SCL_IRQ_STATUS	2	R/W	0	DVI SCL Toggle status , wite 1 to clear 0: no scl toggle after clear 1: new scl toggle after clear	Rport Wpor t
DVI_EDIDRD_IRQ_EN	1	R/W	0	DVI EDID READ IRQ enable 0:disable 1:enable	
DVI_EDIDRD_STATUS	0	R/W	0	DVI EDID READ STATUS , wite 1 to clear 0: no edid read after clear 1: new edid read after clear	Rport Wpor



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				t
--	--	--	--	---

Register:: HDMI_EDID_IRQ						0xFFE5
Name	Bits	R/W	Default	Comments	Config	
REV_DUMMY_FFE5	7:6	R/W	0	Dummy		
HDMI_FORCE_NACK	5	R/W	0	In DDC2B Mode, force HDMI SDA output 1(NACK) 0:disable 1:enable		
HDMI_FORCE_ACK_ZERO	4	R/W	0	In DDC2B Mode force HDMI SDA Output 0 (ACK) 0:disable 1:enable		
HDMI_SCL_IRQ_EN	3	R/W	0	HDMI SCL Toggle IRQ enable 0:disable 1:enable		
HDMI_SCL_IRQ_STATUS	2	R/W	0	HDMI SCL Toggle status , wite 1 to clear 0: no scl toggle after clear 1: new scl toggle after clear	Rport Wpor t	
HDMI_EDIDRD_IRQ_EN	1	R/W	0	HDMI EDID READ IRQ enable 0:disable 1:enable		
HDMI_EDIDRD_STATUS	0	R/W	0	HDMI EDID READ STATUS , wite 1 to clear 0: no edid read after clear 1: new edid read after clear	Rport Wpor t	

Register::Port_read_control_2						0FFE6
Name	Bits	R/W	Default	Comments	Config	



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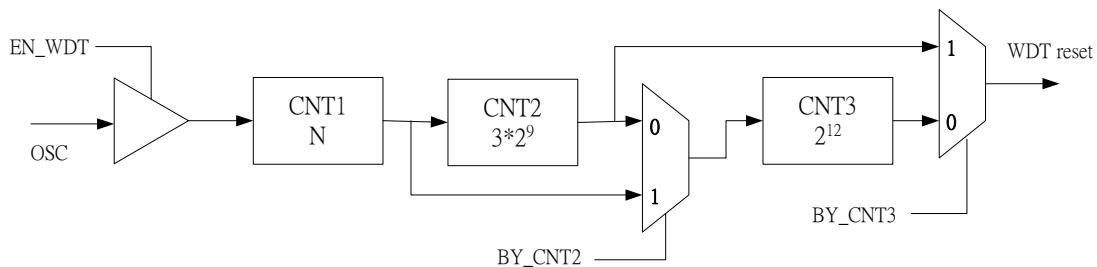
RTD2261W/2271W/2281W Series-GR

PC_pin_reg_n	7	R/W	0	Source selection for PC read back 0: register 1: bus value	
PB_pin_reg_n	6	R/W	0	Source selection for PB read back 0: register 1: bus value	
PD_pin_reg_n	5	R/W	0	Source selection for PD read back 0: register 1: bus value	
Reserved	4:0	--	0	Reserved	

Register::: REV_DUMMY4						0xFFE9
Name	Bits	R/W	Default	Comments	Config	
REV_DUMMY4	7:0	R/W	00	Dummy4		

Watchdog Timer

The Watchdog Timer automatically generates a device reset when it is overflowed. The interval of overflow is about 0.44 sec to 3.5 sec(assume crystal is 14.3MHz) and can be programmed via register CNT1.



Register::WATCHDOG_timer						0xFFEA
Name	Bits	R/W	Default	Comments	Config	
WDT_EN	7	R/W	1	0: Disable watchdog timer 1: Enable watchdog timer		
CLR_WDT	6	W	0	0: No effect 1: Clear all counters of watchdog	Rport Wport	
SF_HLT_WDT_EN	5	R/W	0	1: Stop watchdog counter by SPI-FLASH access		
BW_HLT_WDT_EN	4	R/W	0	1: Stop watchdog counter by scalar burst write action		
Reserved	3	--	0	Reserved		
CNT1	2:0	R/W	0	The number N of counter1 000~111: 1~8		

- When ISP mode is enabled, watchdog will be disabled by hardware.

Register::WDT_test						0xFFEB
Name	Bits	R/W	Default	Comments	Config	
Reserved	7:2	--	--	Reserved		
BY_CNT2	1	R/W	0	Signal bypass counter2* 0: signal pass through counter2 1: bypass		
BY_CNT3	0	R/W	0	Signal bypass counter3* 0: signal pass through counter3 1: bypass		

*When BY_CNT2 and BY_CNT3 are all assigned one (bypass), watchdog will be counted by CNT3



In System Programming

User can program the external serial FLASH by internal hardware without removing serial FLASH from the system. RTD2485XD utilizes DDC channel (ADC/DVI/HDMI DDC) to communicate with IIC host for ISP function. The ISP protocol is mainly compatible with DDC protocol. However, one significant difference is that the LSB of 7-bit ISP address is the address auto increase bit. Thus, we can improve the flash program speed.

Register::ISP_slave_address						0xFFEC
Name	Bits	R/W	Default	Comments	Config	
ISP_ADDR	7:2	R/W	25	ISP slave address		
ISP_ADDR_INC_A	1	R	0	Received LSB of ISP slave address of ADC DDC channel 0: address is nonincrease 1: address is auto-increase		
ISP_ADDR_INC_D	0	R	0	Received LSB of ISP slave address of DVI DDC channel 0: address is nonincrease 1: address is auto-increase		

Register::MCU_control						0xFFED
Name	Bits	R/W	Default	Comments	Config	
PORT_PIN_REG	7	R/W	1	port_pin_reg_n enable 0: port_pin_reg_n signal is disabled 1: port_pin_reg_n signal is enabled		
ISP_ADDR_INC_H	6	R	0	Received LSB of ISP slave address of HDMI DDC channel 0: address is nonincrease 1: address is auto-increase		



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FLASH_CLK_DIV	5:2	R/W	2	SPI-FLASH clock divider, its clock source is selected by MCU_CLK_SEL, default is MCU_CLK_SEL/2	
MCU_CLK_SEL	1	R/W	0	CPU clock source select 0: CPU clock is from Crystal divided by DIV 1: CPU clock is from PLL divided by DIV	
CKOUT_SEL	0	R/W	0	CLKO select 0: Select Crystal output 1: Select Mcu clk output	

Register::MCU_clock_control					
Name	Bits	R/W	Default	Comments	Config
ISP_MODE	7	R/W	0	ISP Mode Select 0: Normal ISP mode, I2C protocol (Device_ID, address, Data...) 1: AIO Block Write mode I2C protocol (Device_ID, addr, Length, Data...)	Rport Wport
MCU_PERI_NON_STOP	6	R/W	0	1: keep mcu peripheral running when mcu stopped by spi flash access 0: peripheral will be stopped with mcu*.	
MCU_CLK_DIV	5:2	R/W	1	MCU clock is FLASH clock/MCU_CLK_DIV.	
SOF_RST	1	R/W	0	Software reset mcu 0: No effect 1: reset RTD2485XD	Rport Wport
SCA_HRST	0	R/W	0	Hardware reset for Scalar 0: No effect 1: reset SCALAR module	

*note: this register bit[6] only has effect on peripheral built in SFR, which are timer 0, 1, 2 and serial port 1.

Register::RAM_test					
Name	Bits	R/W	Default	Comments	Config



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MCU_TSTCLK_SEL	7	R/W	0	1: MCU clock is from external pin 0: MCU clock is from crystal/PLL divided by DIV (0xFFED[1])	
SOD_DATA_LOCATION	6:5	R/W	3	Decide sod data wr/rd location 0: Not used 1: FCXX 2: FDXX 3: FEXX Xram FAXX space will map to this addr	
Test_mode	4	R/W	0	When test_mode of scalar is enabled for embedded mcu output, the bus is decided by following settins. 0: 10'b0, adc8_out[7:0], adc8_out_valid, adc8_ckini, flash_mcu_gated, bist_clk, xram_clk, 1'b0, adc_div8_clk , eclk_ng , eclk_n , eclk , shift_in_clk, fclk 1: 5'b0, fc_addr[23:0], fc_rd_n	
EXT_RAM_BIST	3	R/W	0	Start BIST function for MCU external RAM (512 bytes) 0: finished and clear 1: start	Rport Wport
EXT_RAM_STA	2	R	0	Test result about MCU external RAM 0: fail 1: ok	
INT_RAM_BIST	1	R/W	0	Start BIST function for MCU internal RAM (256 bytes) 0: finished and clear 1: start	Rport Wport
INT_RAM_STA	0	R	0	Test result about MCU internal RAM 0: fail 1: ok	

mode = 0	mode = 1
fclk	irin



shift_in_clk	remote_in2
eclk	rmtin
eclk_n	st_search
eclk_ng	st_lead
adc_div9_clk	st_data
adc_div270_clk	find_str
xram_clk	find_rpt
bist_clk	find_d01
flash_mcu_gated	find_d01_value
adca_ckini	st_ph[0]
adca_out_valid	st_ph[1]
adca_out[0]	st_ph[2]
adca_out[1]	st_ph[3]
adca_out[2]	st_cmd[0]
adca_out[3]	st_cmd[1]
adca_out[4]	st_cmd[2]
adca_out[5]	cec_tst[0]
adcb_ckini	cec_tst[1]
adcb_out_valid	cec_tst[2]
adcb_out[0]	cec_tst[3]
adcb_out[1]	cec_tst[4]
adcb_out[2]	cec_tst[5]
adcb_out[3]	cec_z0_ok
adcb_out[4]	
adcb_out[5]	
adcb_out[6]	
adcb_out[7]	
adcb_out[8]	
adcb_out[9]	

Xdata-SPI-FLASH Write Protect

Register:: Xdata_SPI_FLASH_Write_Protect					0xFFFF
Name	Bits	R/W	Default	Comments	Config
Reserved	7:5	R/W	0	Reserved	



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Serial_stop_en	4	R/W	0	Stop 8051 serial 0: run 1: stop	
Timer2_stop_en	3	R/W	0	Stop 8051 timer2 0: run 1: stop	
IdleMode_Stop8051_en	2	R/W	0	Stop 8051 clock in idle mode 0: disable 1: enable	
Timer01_stop_en	1	R/W	0	Stop 8051 timer0 and timer1 0: run 1: stop	
XDATA_Flash_En	0	R/W	0	0: Enable xData write to Flash Function (Default) 1: Disable xData write to Flash Function	

Register:: REV_DUMMY5 0xFFFF1					
Name	Bits	R/W	Default	Comments	Config
REV_DUMMY5	7:0	R/W	00	Dummy5	

Register:: PWM_I2C_CLOCK_STOP 0xFFFF2					
I2C_CKXTAL_STOP	7	R/W	0	I2c crystal clock stop control 0: run 1: stop	
PWM_CKXTAL_STOP	6	R/W	0	PWM crystal clock stop control 0: run 1: stop	
PWM5_OUTCLK_STOP	5	R/W	0	PWM5 output clock stop control 0: run 1: stop	
PWM4_OUTCLK_STOP	4	R/W	0	PWM4 output clock stop control 0: run 1: stop	
PWM3_OUTCLK_STOP	3	R/W	0	PWM3 output clock stop control 0: run 1: stop	
PWM2_OUTCLK_STOP	2	R/W	0	PWM2 output clock stop control 0: run	



				1: stop	
PWM1_OUTCLK_STOP	1	R/W	0	PWM1 output clock stop control 0: run 1: stop	
PWM0_OUTCLK_STOP	0	R/W	0	PWM0 output clock stop control 0: run 1: stop	

Scalar Interface

Scalar Interface Related Register

External host interface is selected by power-on latch. The internal XFR access will be auto-switched to external host interface by power-on latch, too.

Scalar's register map must reserve addresses for mapping necessary XFR when using external host interface.

Register:: SCA_INF_CONTROL					0xFFFF3
Name	Bits	R/W	Default	Comments	Config
REG_READ_EN	7	R	0	Enable Read Action of Scalar Interface	
REG_WRITE_EN	6	R	0	Enable Write Action of Scalar Interface	
ADDR_NON_INC	5	R/W	0	1: turn-off address auto inc	
REG_BURCMD_WR	4	R/W	0	Enable burst write function, mcu will halt till action done or an interrupt triggered. *	Rport Wport
REG_BURDAT_WR	3	R/W	0	Enable burst write data to HOST_ADDR, mcu will halt till action done or an interrupt triggered *	Rport Wport
BURST_CMD_ERR	2	R	0	Burst write command error, value of SCA_INF_BWR_COUNT mismatch the length in content	
DIS_INT_RLS	1	R/W	0	1: disable the function of releasing mcu by interrupt	
PAGE_ADDR_MAP	0	R/W	0	0: Using normal XFR address to access all XFR 1: Using external page address for XFR. XFR can only be accessed by SCA_INF_ADDR, SCA_INF_DATA	

*: MCU will be released when interrupt is triggered. The bit value will maintain 1 before the operation is done. Rewriting this bit to 1 to continue the burst cmd/data write mode.



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Register:: SCA_INF_ADDR					0xFFFF4
Name	Bits	R/W	Default	Comments	Config
HOST_ADDR	7:0	R/W	0x00	Host Interface Access Address	Rport Wport

Register:: SCA_INF_DATA					0xFFFF5
Name	Bits	R/W	Default	Comments	Config
HOST_DATA	7:0	R/W	0x00	Host Interface Access Data In/Out Continuously R/W with/without address auto-increment depends on ADDR_NON_INC	Rport Wport

Register:: SCA_INF_BWR_ADRH					0xFFFF6
Name	Bits	R/W	Default	Comments	Config
BWR_ADRH	7:0	R/W	0x00	Burst Write Command Start Address [23:16]	Rport Wport

Register:: SCA_INF_BWR_ADRM					0xFFFF7
Name	Bits	R/W	Default	Comments	Config
BWR_ADRM	7:0	R/W	0x00	Burst Write Command Start Address [15:8]	Rport Wport

Register:: SCA_INF_BWR_ADRL					0xFFFF8
Name	Bits	R/W	Default	Comments	Config
BWR_ADRL	7:0	R/W	0x00	Burst Write Command Start Address [7:0]	Rport Wport

Register:: SCA_INF_BWR_COUNT_H					0xFFFF9
Name	Bits	R/W	Default	Comments	Config
BWR_BYTE_COUNT_H	7:0	R/W	0x00	Burst Write Command Data Length. Left byte count when interrupt is asserted	Rport Wport

Register:: SCA_INF_BWR_COUNT_L					0xFFFFA
Name	Bits	R/W	Default	Comments	Config
BWR_BYTE_COUNT_L	7:0	R/W	0x00	Burst Write Command Data Length, left byte count when interrupt is asserted	Rport Wport

Register:: SCA_INF_PERIOD					0xFFFFB
---------------------------	--	--	--	--	---------



Name	Bits	R/W	Default	Comments	Config
SCA_INF_PERIOD	7:0	R/W	0x02	Interval Between Two Command TI = SYS_PERIOD * 2 * BWR_PERIOD, it will halt mcu extra time TI in normal access and maintain the interval TI between two access in burst write mode.	

*For 50MHz system clock, BWR_PERIOD can be delayed to 10.2us > 10us for special requirement of OSD register

Table Format for register burst write command format

```
BYTE code tFONT_GLOBAL[] = {
Length_A, AUTOINC_A, ADDR_A, DATA_A0, DATA_A1.....,
Length_B, AUTOINC_B, ADDR_B, DATA_B0, DATA_B1.....,
.....
-END
0x4 , 0x0, 0xA0, 01
0x6, 0x0, 0x90, 0x01, 0x02, 0x03
.....
0x0
}
```

note: AUTOINC = 0 means enable address auto-increment

Example for firmware reference:

1. OSD font table

```
// set initial address of data = 0x102030
BWR_ADRH = 0x10
BWR_ADRM = 0x20
BWR_ADRL = 0x30
// set data byte count = 0x0890
BWR_BYTE_COUNT_H = 0x08
BWR_BYTE_COUNT_L = 0x90
// set scalar's target register address = 0x58
SCA_INF_ADDR = 0x58
// enable burst data write
SCA_INF_CONTROL[3] = 1' b1
```

2. Command table

```
// set initial address of data = 0x102030
BWR_ADRH = 0x10
BWR_ADRM = 0x20
BWR_ADRL = 0x30
```



```

// set data byte count = 0x0890
BWR_BYTE_COUNT_H = 0x08
BWR_BYTE_COUNT_L = 0x90
// enable burst command write
SCA_INF_CONTROL[4] = 1' b1

```

Bank Switch

Due to only one external SPI-FLASH is used for embedded MCU, it is necessary to allocate the non-volatile memory for both program code and external data (XDATA). In default, the 0x0 ~ 0xFFFF is used for program code, and the 0x10000 ~ 0x1FFFF is used for external data. When 64K-byte FLASH is used, there is no space in FLASH reserved for XDATA. XRAM and XFR are still accessible. More than 64K-byte FLASH can be used by designer's plan. GPIO mode for bank switch is used for 128K-byte FLASH and up to 256x64K bytes FLASH is supported by XFR mode. Both of them are supported by KeilC. The start bank of XDATA is defined by XDATA_BSTART. XRAM is allocated to 0xFB00 – 0xFEFF of XDATA's Bank0. Besides, except XFR address 0xFFFFE and 0xFFFF, XFR and XRAM can be chosen if occupy only one bank of XDATA. Designer can set program address to include the whole FLASH address space without using the range reserved for XDATA to avoid partitioning the boundary in the power of 2. The following table is an example. Program is designed to use only 0x00000 – 0x4FFF, but declare a 0x00000 – 0x7FFFF address space. Bank 5 ~ Bank 7 of program code will be empty and not programmed into FLASH. XDATA is allocated in 0x50000 – 0x7FFFF via setting of XFR.

SPI FLASH Address	Program Address	Xdata	XRAM	XFR
00000-0FFFF	Bank0, 0000-FFFF			
10000-1FFFF	Bank1, 0000-FFFF			
20000-2FFFF	Bank2, 0000-FFFF			
30000-3FFFF	Bank3, 0000-FFFF			
40000-4FFFF	Bank4, 0000-FFFF			
50000-5FFFF	Bank5, 0000-FFFF	Bank0, 0000-FFFF	FB00 - FEFF	FF00-FFFF
60000-6FFFF	Bank6, 0000-FFFF	Bank1, 0000-FFFF		FF00-FFFF
70000-7FFFF	Bank7, 0000-FFFF	Bank2, 0001-FFFF		FF00-FFFF

Register:::Bank_swich_control						0xFFFC
Name	Bits	R/W	Default	Comments	Config	
Reserved	7:5	--	0	Reserved		



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Scalar_Addr_Remapping	4	R/W	0	Scalar Addresss remapping to Xdata, (0x00_00 ~ 0x10_FF) 0: Disable 1: Enable	
GLOBAL_XFR	3	R/W	1	1: XFR will occupy the address space of all XDATA banks. 0: only 0xFFFF will occupy the address of all XDATA banks.	
GLOBAL_XRAM	2	R/W	0	1: XRAM will occupy the address space of all XDATA banks. 0: XRAM only occupy XDATA bank 0	
SW_MODE	1	R/W	0	0: using P3.5 as A16 1: using Pbank_switch (0xFFFF)	
BANK_EN	0	R/W	0	1: Enable Bank Switching Function for program address space 0: Disable Bank Switching, program memory space is 64K byte and GLOBAL_XFR, GLOBAL_XRAM, XDATA_BSTART, XDATA_BSEL still can be used to control XDATA memory space.	

Register::XDATA_bank_start						0xFFFFD
Name	Bits	R/W	Default	Comments	Config	
XDATA_BSTART	7:0	R/W	0xff	The start bank number for XDATA access.		

Register::XDATA_bank_sel						0xFFFFE
Name	Bits	R/W	Default	Comments	Config	
XDATA_BSEL	7:0	R/W	0	First bank number for XDATA access.		

Register::Pbank_switch						0xFFFFF
Name	Bits	R/W	Default	Comments	Config	



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PBANK_SEL	7:0	R/W	0	Bank number for program code access.	
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Pin Share Register (page 10)

GPIO Pin List

GPIO Pin List	Name	GPI	GPO <push-pull>	GPO <Open-Drain>	GPIO	3.3V Tolerance	5V Tolerance	5V Tolerance (When Power Off)	Pin Share Register	MCU Control
31	PD.7	Y	Y	Y		Y			Page10 , 0xB7	0xFF77
32	PD.6	Y	Y	Y		Y			Page10 , 0xB7	0xFF78
33	PD.5	Y	Y	Y		Y			Page10 , 0xB7	0xFF79
34	PD.4	Y	Y	Y		Y			Page10 , 0xB7	0xFF7A
35	PD.3	Y	Y	Y		Y			Page10 , 0xB8	0xFF7B
36	PD.2	Y	Y	Y		Y			Page10 , 0xB8	0xFF7C
37	PD.1	Y	Y	Y		Y			Page10 , 0xB8	0xFF7D
39	PD.0	Y	Y	Y	Y			Y	Page10 , 0xB8	0xFF7E
40	PC.4	Y	Y	Y	Y			Y	Page10 , 0xB9	0xFFA4
41	PB.7	Y	Y	Y	Y			Y	Page10 , 0xA0	0xFF7F
42	PB.6	Y	Y	Y	Y			Y	Page10 , 0xA0	0xFF89
43	PB.5	Y	Y	Y	Y			Y	Page10 , 0xA0	0xFF8A
44	PB4	Y	Y	Y	Y			Y	Page10 , 0xA8	0xFF8B
45	PB.3	Y	Y	Y	Y			Y	Page10 , 0xA1	0xFF8C
46	PB.2	Y	Y	Y	Y			Y	Page10 , 0xA3	0xFF8D
47	PB.1	Y	Y	Y	Y			Y	Page10 , 0xA6	0xFF8E
48	PB.0	Y	Y	Y	Y			Y	Page10 , 0xA7	0xFF8F
50	P6.0	Y	Y	Y	Y			Y	Page10 , 0xAB	0xFFC7
51	P6.1	Y	Y	Y	Y			Y	Page10 , 0xA3	0xFFC8
52	P6.2	Y	Y	Y	Y			Y	Page10 , 0xA4	0xFFC9
53	P6.3	Y	Y	Y	Y			Y	Page10 , 0xA5	0xFFCA
54	P6.4	Y	Y	Y	Y			Y	Page10 , 0xA0	0xFFCB
55	P6.5	Y	Y	Y	Y			Y	Page10 , 0xA6	0xFFCC
56	P6.6	Y	Y	Y	Y			Y	Page10 , 0xAF	0xFFCD
57	P6.7	Y	Y	Y	Y			Y	Page10 , 0xAF	0xFFCE
58	P3.0	Y	Y	Y	Y			Y	Page10 , 0xA2	SFR Access
59	P3.1	Y	Y	Y	Y			Y	Page10 , 0xA2	SFR Access
63	PC.3	Y	Y	Y	Y			Y	Page10 , 0xA6	0xFFA0
64	P1.0	Y	Y	Y	Y			Y	Page10 , 0xA3	SFR Access
65	P1.1	Y	Y				Y		Page10 , 0xB1	SFR Access
66	P1.2	Y	Y				Y		Page10 , 0xA4	SFR Access
67	P1.3	Y	Y				Y		Page10 , 0xA4	SFR Access
68	P1.4	Y	Y				Y		Page10 , 0xA7	SFR Access
69	P1.5	Y	Y				Y		Page10 , 0xA5	SFR Access
70	P1.6	Y	Y				Y		Page10 , 0xA5	SFR Access
71	P1.7	Y	Y				Y		Page10 , 0xA7	SFR Access
72	PC.2	Y	Y				Y		Page10 , 0xB2	0xFFA1
74	P9.0	Y	Y	Y		Y			Page10 , 0xA9	0xFFD8
75	P9.1	Y	Y	Y		Y			Page10 , 0xA9	0xFFD9
76	P9.2	Y	Y	Y		Y			Page10 , 0xA9	0xFFDA
77	P9.3	Y	Y	Y		Y			Page10 , 0xA9	0xFFDB
78	P9.4	Y	Y	Y		Y			Page10 , 0xA9	0xFFDC
79	PA.0	Y	Y	Y		Y			Page10 , 0xA9	0xFFDD
80	PA.1	Y	Y	Y		Y			Page10 , 0xA9	0xFFDE
81	PA.2	Y	Y	Y		Y			Page10 , 0xA9	0xFFDF
82	PA.3	Y	Y	Y		Y			Page10 , 0xA9	0FFE0
83	PA.4	Y	Y	Y		Y			Page10 , 0xA9	0FFE1

Note: Pin 74~Pin 83 (GPI,GPO,GPIO) can not work when power saving & power Down.

Please don't use Pin 74~Pin 83 for power status detect function.

(Power Saving CR[01] Bit1 Enable, Power Down CR[01] Bit2 Enable)



PWM Pin List

GPIO Pin List	Name	(Push-pull)	PWM (Open-drain)	3.3V Tolerance	5V Tolerance	5V Tolerance (When Power Off)	Pin Share Register
48	PWM0	Y				Y	Page10 , 0xA7
55	PWM1	Y	Y			Y	Page10 , 0xA6
55	PWM5	Y				Y	Page10 , 0xA6
63	PWM2	Y	Y			Y	Page10 , 0xA6
64	PWM0	Y	Y			Y	Page10 , 0xA3
65	PWM1	Y	Y		Y		Page10 , 0xB1
71	PWM1	Y			Y		Page10 , 0xA7
71	PWM5	Y			Y		Page10 , 0xA7
72	PWM3	Y	Y		Y		Page10 , 0xB2
96	PWM0	Y			Y		Page10 , 0xA8
97	PWM1	Y	Y		Y		Page10 , 0xA8
98	PWM2	Y			Y		Page10 , 0xAA
99	PWM3	Y	Y		Y		Page10 , 0xA9
100	PWM4	Y	Y		Y		Page10 , 0xA9
101	PWM5	Y			Y		Page10 , 0xAB
102	PWM0	Y	Y		Y		Page10 , 0xAA
103	PWM1	Y			Y		Page10 , 0xAC
104	PWM2	Y			Y		Page10 , 0xAC
114	PWM4	Y				Y	Page10 , 0xB2
119	PWM5	Y	Y			Y	Page10 , 0xA1
126	PWM1	Y	Y		Y		Page10 , 0xA1

Pin Share (Page 10)

Register:: PIN_SHARE_CTRL00 0xA0					
Name	Bits	Read/Write	Reset State	Comments	Config
PBD7	7:6	R/W	0x0	Pin41 (PAD_V8_7) 00: PBD7i <I> <default> 01: PBD7o <O> <open-drain> 10: PBD7o <O> <push-pull> 11: TCON5 <O> Effectively only if CR1F[5:4]=2'b10	
PBD6	5:4	R/W	0x0	Pin 42 (PAD_V8_6) 00: PBD6i <I> <default> 01: PBD6o <O> <open-drain> 10: PBD6o <O> <push-pull> 11: IICCSCL <IO> <open-drain> Effectively only if CR1F[5:4]=2'b10	
PBD5	3:2	R/W	0x0	Pin43 (PAD_V8_5) 00: PBD5i <I> <default> 01: PBD5o <O> <open-drain> 10: PBD5o <O> <push-pull> 11: IICSDA <IO> <open-drain> Effectively only if CR1F[5:4]=2'b10	
P6D4	1:0	R/W	0x0	Pin54 (PAD_ADCA4) 00: P6D4i <I> <default>	



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				01: P6D4o <O> <open-drain> 10: P6D4o <O> <push-pull> 11: TCON[7]	
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Register:: PIN_SHARE_CTRL01 0xA1					
Name	Bits	Read/Write	Reset State	Comments	Config
PBD3	7:6	R/W	0x0	Pin45 (PAD_V8_3) 00: PBD3i <I> <default> 01: PBD3o <O> <open-drain> 10: PBD3o <O> <push-pull> 11: reserved Effectively only if CR1F[5:4]=2'b10	
PCD1	5:3	R/W	0x0	Pin119 (PAD_PWM5) 000: Reserved 001: PCD1o <O> <open-drain> 010: PCD1o <O> <push-pull> 011: PWM5 <O> <push-pull> 100: reserved 101: PWM5 <O> <open-drain> (Pin 119 : Power on latch Pin) (when AC Power On , Power on latch pin must be "High") Please don't let Pin119 be "Input Pin".	
PCD0	2:0	R/W	0x0	Pin126 (PAD_CEC) 000: PCD0i <I> 001: PCD0o <O> <open-drain> 010: PCD0o <O> <push-pull> 011: PWM1 <O> <push-pull> 100: Reserved 101: reserved 110: PWM1 <O> <open-drain>	

Register:: PIN_SHARE_CTRL02 0xA2					
Name	Bits	Read/Write	Reset State	Comments	Config
DDC1	7	R/W	0x0	Pin58 (PAD_DDCSCL1) 0: DDCSCL1 <IO> <open-drain> <default> 1: reserved //normal output(refer bit6~4) Pin59 (PAD_DDCSDA1) 0: DDCSDA1 <IO> <open-drain> <default> 1: reserved //normal output(refer bit3~1)	
DDCSCL1	6:4	R/W	0x0	Pin58 000: P3D0i <I> 001: P3D0o <O> <open-drain> 010: P3D0o <O> <push-pull> 011: RXD <IO> <open-drain> 100: TCON7 <O> 101: TCON10 <O>	
DDCSDA1	3:1	R/W	0x0	Pin59	



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				000: P3D1i <I> 001: P3D1o <O> <open-drain> 010: P3D1o <O> <push-pull> 011: TXD <O> <open-drain> 100: TCON3 <O> 101: TCON5 <O>	
MUX_DDC1	0	R/W	0	when (Page 10 , 0xA2[0] = 1) && (pin55 = 1), disable ddc function of pin58, 59 and swap to pin52, 53.	

Register:: PIN_SHARE_CTRL03 0xA3					
Name	Bits	Read/Write	Reset State	Comments	Config
PBD2	7:6	R/W	0x0	Pin46 (PAD_V8_2) 00: PBD2i <I> <default> 01: PBD2o <O> <open-drain> 10: PBD2o <O> <push-pull> 11: reserved Effectively only if CR1F[5:4]=2'b10	
P6D1	5:4	R/W	0x0	Pin51 (PAD_ADCA1) 00: P6D1i <I> <default> 01: P6D1o <O> <open-drain> 10: P6D1o <O> <push-pull> 11: ADCA1(8Bit) <I>	
P1D0	3:0	R/W	0x00	Pin64 (PAD_TCON0) 0000: P1D0i <I> <default> 0001: P1D0o <O> <open-drain> 0010: P1D0o <O> <push-pull> 0011: T2 <I> 0100: reserved 0101: reserved 0110: TCON[0] <O> 0111: PWM0 <O> <push-pull> 1000: TCON[7] <O> 1001: PWM0 <O> < open-drain > 1010: INT1<I> 1111: DPLL Output Test Mode	

Register:: PIN_SHARE_CTRL_04 0xA4					
Name	Bits	Read/Write	Reset State	Comments	Config
P6D2	7:6	R/W	0x0	Pin52 (PAD_ADCA2) 00: P6D2i <I> <default> 01: P6D2o <O> <open-drain> 10: P6D2o <O> <push-pull>	



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				11: ADCA2 (8Bit) <I>	
P1D2	5:3	R/W	0x0	Pin66 (PAD_TCON2) 000: P1D2i <I> 001: P1D2o <O> <push-pull> 010: Reserved 011: CLKO <O> 100: reserved 101: TCON[2] <O> 110: TCON[4] <O>	
P1D3	2:0	R/W	0x0	Pin67 (PAD_TCON5) 000: P1D3i <I> 001: P1D3o <O> <push-pull> 010: Reserved 011: reserved 100: TCON[5] <O> 101: TCON[9] <O>	

Register:: PIN SHARE CTRL05 0xA5					
Name	Bits	Read/Write	Reset State	Comments	Config
P6D3	7:6	R/W	0x0	Pin53 (PAD_ADCA3) 00: P6D3i <I> <default> 01: P6D3o <O> <open-drain> 10: P6D3o <O> <push-pull> 11: ADCA3 (8Bit) <I>	
P1D5	5:3	R/W	0x0	Pin69 (PAD_TCON3) 000: P1D5i <I> 001: P1D5o <O> <push-pull> 010: Reserved 011: reserved 100: TCON[3] <O> 101: TCON[7] <O> 110: reserved 111: IICSCL <IO> <open-drain>	
P1D6	2:0	R/W	0x0	Pin70 (PAD_TCON9) 000: P1D6i <I> 001: P1D6o <O> <push-pull> 010: Reserved 011: reserved 100: TCON[9] <O> 101: TCON[11] <O> 110: reserved 111: IICSDA <IO> <open-drain>	



Register:: PIN_SHARE_CTRL06 0xA6					
Name	Bits	Read/Write	Reset State	Comments	Config
PBD1	7:6	R/W	0x0	Pin47 (PAD_V8_1) 00: PBD1i <I> <default> 01: PBD1o <O> <open-drain> 10: PBD1o <O> <push-pull> 11: reserved Effectively only if CR1F[5:4]=2'b10	
P6D5	5:3	R/W	0x0	Pin55 (PAD_ADCB0) 000: P6D5i <I> <default> 001: P6D5o <O> <open-drain> 010: P6D5o <O> <push-pull> 011: PWM1 <O><open-drain> 100: PWM1 <O><push-pull> 101: PWM5 <O><push-pull> 110: TCON0 <O> 111: TCON5 <O>	
PCD3	2:0	R/W	0x0	Pin63 (PAD_GPIO63) 000: PCD3i <I> <default> 001: PCD3o <O> <open-drain> 010: PCD3o <O> <push-pull> 011: PWM2 <O><push-pull> 100: TCON1 <O> 101: TCON8 <O> 110: : PWM2 <O><open-drain> 111 :INT0<I> Effectively only if CRBB[5] = 0	

Register:: PIN_SHARE_CTRL07 0xA7					
Name	Bits	Read/Write	Reset State	Comments	Config
PBD0	7:6	R/W	0x0	Pin48 (PAD_V8_0) 00: PBD0i <I> <default> 01: PBD0o <O> <open-drain> 10: PBD0o <O> <push-pull> 11: PWM0 <O> <push-pull> Effectively only if CR1F[5:4]=2'b10	
P1D4	5:3	R/W	0x0	Pin68 (PAD_TCON13) 000: P1D4i <I> 001: P1D4o <O> <push-pull> 010: Reserved 011: reserved 100: TCON[3] <O> 101: TCON[13] <O> 110: reserved	
P1D7	2:0	R/W	0x0	Pin71 (PAD_TCON8)	



			000: P1D7i <I> 001: P1D7o <O> <push-pull> 010: PWM5 <O><push-pull> 011: reserved 100: TCON[8] <O> 101: TCON[10] <O> 110: reserved 111: PWM1 <O><push-pull>	
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Register:: PIN SHARE CTRL08 0xA8					
Name	Bits	Read/ Write	Reset State	Comments	Config
PBD4	7:5	R/W	0x0	Pin44 (PAD_V8_4) 000: PBD4i <I> <default> 001: PBD4o <O> <open-drain> 010: PBD4o <O> <push-pull> 011: reserved 100: reserved 111:TCON[3] Effectively only if CR1F[5:4]=2'b10	
P5D2	4:3	R/W	0x0	Pin96 (PAD_PWM0) 00: P5D2i <I> 01: P5D2o <O> <push-pull> 10: Reserved <O> 11: PWM0 <O> <push-pull>	
P5D3	2:0	R/W	0x0	Pin97 (PAD_PWM1) 000: P5D3i <I> 001: P5D3o <O> <push-pull> 010: Reserved 011: PWM1 <O> <push-pull> 100: Reserved <O> 101: PWM1 <O> <open-drain>	

Register:: PIN SHARE CTRL09 0xA9					
Name	Bits	Read/ Write	Reset State	Comments	Config
P9PA	7:6	R/W	0x0	Pin74-83 (Pin74-Pin78 P9.0~P9.4) (Pin79-Pin83 PA.0~PA.4) 00: None <default>	



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				01: P9PAi <I> 10: P9PAo <O> (push-pull) 11: P9PAo <O> (Open-drain) ie. active if single-port LVDS without E/O swap (for Pin 74,75,78,79 , 0xB6 is effectively only if 0xA9(Bit7:6)=2'b10) Pin 74,75,78,79 : Pin share for P9PAo(push-pull) ,	
P5D5	5:3	R/W	0x0	Pin99 (PAD_PWM3) 000: P5D5i <I> 001: P5D5o <O> <push-pull> 010: Reserved 011: PWM3 <O><push-pull> 100: TCON[6] <O> 101: TCON[11] <O> 110: PWM3 <O><open-drain>	
P5D6	2:0	R/W	0x0	Pin100 (PAD_PWM4) 000: P5D6i <I> 001: P5D6o <O> <push-pull> 010: Reserved 011: PWM4 <O><push-pull> 100: TCON[3] <O> 101: TCON[12] <O> 110: PWM4 <O><open-drain>	

Register:: PIN SHARE CTRL0A 0xAA					
Name	Bits	Read/ Write	Reset State	Comments	Config
P5D4	7:6	R/W	0x0	Pin98 (PAD_PWM2) 00: P5D4i <I> 01: P5D4o <O> <push-pull> 10: Reserved 11: PWM2 <O> <push-pull>	
P7D6	5:3	R/W	0x0	Pin102 (PAD_SPDIF3) 00: P7D6i <I> 01: P7D6o <O> <push-pull>	



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				011: PWM0 <O><push-pull> 010: Reserved 100: reserved 101: reserved 110: TCON[10] <O> 111: PWM0 <O><open-drain>	
P8D0	2:0	R/W	0x0	Pin105 (PAD_SPDIF0) 000: P8D0i <I> 001: P8D0o <O> <push-pull> 010: Reserved 011: TCON[9] <O> 100: reserved 101: reserved	

Register:: PIN_SHARE_CTRL0B 0xAB					
Name	Bits	Read/ Write	Reset State	Comments	Config
P6D0	7:5	R/W	0x0	Pin50 (PAD_ADCA0) 000: P6D0i <I> <default> 001: P6D0o <O> <open-drain> 010: P6D0o <O> <push-pull> 011: ADCA0(8Bit) <I> 100: Reserved 101: Reserved <I>	
P5D7	4:3	R/W	0x0	Pin101 (PAD_PWM5) 00: P5D7i <I> 01: P5D7o <O> <push-pull> 10: TCON[0] <O> 11: PWM5 <O>	
P8D1	2:0	R/W	0x0	Pin108 (PAD_MCK) 000: P8D1i <I> 001: P8D1o <O> <push-pull> 010: Reserved 011: CLKO <O> 100: reserved 101: TCON[7] <O>	

Register:: PIN_SHARE_CTRL0C 0xAC					
Name	Bits	Read/ Write	Reset State	Comments	Config
Reserved	7	R/W	0	reserved to 0	



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P7D5	6:4	R/W	0x0	Pin103 (PAD_SPDIF2) 000: P7D5i <I> 001: P7D5o <O> <push-pull> 010: Reserved 011: PWM1 <O><push-pull> 100: reserved 101: reserved 110: TCON[8] <O> 111: IICSCL <IO> <open-drain> Effectively only if CRBB[4]=0	
P7D4	3:1	R/W	0x0	Pin104 (PAD_SPDIF1) 000: P7D4i <I> 001: P7D4o <O> <push-pull> 010: PWM2<O><push-pull> 011: reserved 100: IRQ <O> 101: TCON[5] <O> 110: reserved 111: IICSDA <IO> <open-drain>	
Reserved	0	R/W	0	reserved to 0	

Register:: PIN_SHARE_CTRL0D 0xAD					
Name	Bits	Read/Write	Reset State	Comments	Config
Reserved	7	R/W	0x0	Reserved	
P3D2	6:4	R/W	0x0	Pin109 (PAD_SCK) 000: P3D2i <I> 001: P3D2o <O> <push-pull> 010: Reserved 011: INT0 <I> 100: TCON[3] <O> 101: reserved	
Reserved	3	R/W	0	reserved to 0	
P3D3	2:0	R/W	0x0	Pin110 (PAD_WS) 000: P3D3i <I> <default> 001: P3D3o <O> <open-drain> 010: P3D3o <O> <push-pull> 011: INT1 <I> 100: TCON[6] <O> 101: reserved 110: TCON[2] <O> 111: TCON[7] <O>	

Register:: PIN_SHARE_CTRL0E 0xAE					
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REALTEK

RTD2261W/2271W/2281W Series-GR

Name	Bits	Read/ Write	Reset State	Comments	Config
Reserved	7	R/W	0	reserved to 0	
P3D4	6:4	R/W	0x0	Pin111 (PAD_SD0) 000: P3D4i <I> <default> 001: P3D4o <O> <open-drain> 010: P3D4o <O> <push-pull> 011: T0 <I> 100: TCON[4] <O> 101: reserved 110: reserved 111: TCON[7] <O>	
Reserved	3	R/W	0	reserved to 0	
P3D5	2:0	R/W	0x0	Pin112 (PAD_SD1) 000: P3D5i <I> <default> 001: P3D5o <O> <open-drain> 010: P3D5o <O> <push-pull> 011: T1 <I> 100: TCON[9] <O> 101: reserved 110: reserved 111: TCON[5] <O>	

Register:: PIN_SHARE_CTRL0F 0xAF					
Name	Bits	Read/ Write	Reset State	Comments	Config
P6D6_7	7	R/W	0	Pin56 (PAD_ADCB1) 0: reserved //normal output(refer bit6~4) <default> 1: IICSCL <IO> <open-drain> Pin57 (PAD_ADCB2) 0: reserved //normal output(refer bit3~1) <default> 1: IICSDA <IO> <open-drain>	
P6D6	6:4	R/W	0x0	Pin56 000: P6D6i <I> <default> 001: P6D6o <O> <open-drain> 010: P6D6o <O> <push-pull> 011: Reserved 100: TCON1 <O> 101: TCON4 <O>	
P6D7	3:1	R/W	0x0	Pin57 000: P6D7i <I> <default> 001: P6D7o <O> <open-drain> 010: P6D7o <O> <push-pull> 011: Reserved 100: TCON9 <O> 101: TCON11 <O>	
PIN58_59	0	R/W	0	PIN58_59_Low_Leak 0: normal mode (47K pull up with 4.3~4.4v pin level) 1: low leak mode with duty penalty. (47K pull up with over 4.5v pin level)	

Register:: PIN_SHARE_CTRL10	0xB0
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RTD2261W/2271W/2281W Series-GR

Name	Bits	Read/ Write	Reset State	Comments	Config
P3D6	7:5	R/W	0x0	Pin113 (PAD_SD2) 000: P3D6i <I> <default> 001: P3D6o <O> <open-drain> 010: P3D6o <O> <push-pull> 011: TCON[1] <O> 100: reserved 101: reserved 110: Reserved 111: TCON[11] <O>	
DDC3	4	R/W	0x0	Pin121 (PAD_DDCSCL3) 0: DDCSCL3 <IO> <open-drain> <default> 1: reserved //normal output(refer bit3~2) Pin122 (PAD_DDCSDA3) 0: DDCSDA3 <IO> <open-drain> <default> 1: reserved //normal output(refer bit1~0)	
DDCSCL3	3:2	R/W	0x0	Pin121 (PAD_DDCSCL3) 00: P7D3i <I> 01: P7D3o <O> <open-drain> 10: P7D3o <O> <push-pull> 11: Reserved	
DDCSDA3	1:0	R/W	0x0	Pin122 (PAD_DDCSDA3) 00: P7D2i <I> 01: P7D2o <O> <open-drain> 10: P7D2o <O> <push-pull> 11: Reserved	

Register:: PIN_SHARE_CTRL11 0xB1					
Name	Bits	Read/ Write	Reset State	Comments	Config
P1D1	7:5	R/W	0x00	Pin65 (PAD_TCON1) 000: P1D1i <I> 001: P1D1o <O> <push-pull> 010: PWM1 <O><push-pull> 011: T2EX <I> 100: TCON[1] <O> 101: TCON[7] <O> 110: reserved 111: PWM1 <O><open-drain>	
DDC2	4	R/W	0	Pin123 (PAD_DDCSDA2) 0: DDCSDA2 <IO> <open-drain> <default> 1: reserved //normal output(refer bit3~2) Pin124 (PAD_DDCSCL2) 0: DDCSCL2 <IO> <open-drain> <default> 1: reserved //normal output(refer bit1~0)	
DDCSDA2	3:2	R/W	0x0	Pin123 (PAD_DDCSDA2) 00: P7D1i <I>	



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				01: P7D1o <O> <open-drain> 10: P7D1o <O> <push-pull> 11: Reserved	
DDCSCL2	1:0	R/W	0x0	Pin124 (PAD_DDCSCL2) 00: P7D0i <I> 01: P7D0o <O> <open-drain> 10: P7D0o <O> <push-pull> 11: Reserved	

Register:: PIN_SHARE_CTRL12 0xB2					
Name	Bits	Read/Write	Reset State	Comments	Config
PCD2	7:5	R/W	0x0	Pin72 (PAD_TCON6) 000: PCD2i <I> <default> 001: PCD2o <O> <push-pull> 010: TCON[6] <O> 011: TCON[12] <O> 100: PWM3 <O> <push-pull> 101: PWM3 <O> <open-drain>	
P3D7	4:2	R/W	0x0	Pin114 (PAD_SD3) 000: P3D7i <I> <default> 001: P3D7o <O> <open-drain> 010: P3D7o <O> <push-pull> 011: TCON[13] <O> 100: reserved 101: reserved 110: PWM4 <O> <push-pull> 111: TCON[0] <O>	
PIN121_122	1	R/W	0	PIN121_122_Low_Leak 0: normal mode (47K pull up with 4.3~4.4v pin level) 1: low leak mode with duty penalty. (47K pull up with over 4.5v pin level)	
PIN123_124	0	R/W	0	PIN123_124_Low_Leak 0: normal mode (47K pull up with 4.3~4.4v pin level) 1: low leak mode with duty penalty. (47K pull up with over 4.5v pin level)	

Register:: PIN_DRIVING_CTRL1 0xB3					
Name	Bits	Read/Write	Reset State	Comments	Config
PIN50_54	7	R/W	0	Driving Current Control00 – Pin50~54 0: Low 1: High	
PIN55_57	6	R/W	0	Driving Current Control01 – Pin55~57 0: Low 1: High	
PIN58_59	5	R/W	0	Driving Current Control02 – Pin58~59 0: Low 1: High	



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PIN63_64	4	R/W	0	Driving Current Control03 – Pin63~64 0: Low 1: High	
PIN65_109	3:2	R/W	0x3	Driving Current Control04 – Pin65~72 -74~83- 86~105- 108~109 - LVDS 00: 2.0mA 01: 2.5mA 10: 3.0mA 11: 3.5mA Driving Control for (LVDS Data) Pair Bit(3:2) → User msut set the same as Bit(1:0)	
	1:0	R/W	0x3	Driving Control for (LVDS CLOCK)Pair 00: 2.0mA 01: 2.5mA 10: 3.0mA 11: 3.5mA Bit(1:0) → User msut set the same as Bit(3:2)	

Register:: PIN_DRIVING_CTRL2 0xB4					
Name	Bits	Read/Write	Reset State	Comments	Config
Reserved	7	R/W	0	reserved to 0	
PIN41_48	6	R/W	0	Driving Current Control05 – Pin41~48 0: Low 1: High	
PIN110_114	5	R/W	0	Driving Current Control06 – Pin110~114 0: Low 1: High	
PIN115	4	R/W	0	Driving Current Control07 – Pin115 0: 4mA 1: 2mA	
PIN121_124	3	R/W	0	Driving Current Control08 – Pin121~124-119-126 0: Low 1: High	
PIN74_95	2	R/W	0	Driving Current Control09 – Pin74~95 0: Low 1: High	
Reserved	1:0	R/W	0	reserved to 0	

Register:: PIN_PULLUP_CTRL3 0xB5					
Name	Bits	Read/Write	Reset State	Comments	Config
PIN50_54	7	R/W	0	Pull Up Control00 – Pin50~54 0: Disable 1: Enable (active only in GPI or open-drain case)	
PIN55_57	6	R/W	0	Pull Up Control01 – Pin55~57 0: Disable	



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				1: Enable (active only in GPI or open-drain case)	
PIN58_59	5	R/W	0	Pull Up Control02 – Pin58~59 0: Disable 1: Enable (active only in GPI or open-drain case)	
PIN64_126	4	R/W	0	Pull Up Control03 – Pin63~64-119-126 0: Disable 1: Enable (active only in GPI or open-drain case)	
PIN110_114	3	R/W	0	Pull Up Control04 – Pin110~114 0: Disable 1: Enable (active only in GPI or open-drain case)	
PIN121_124	2	R/W	0	Pull Up Control05 – Pin121~124 0: Disable 1: Enable (active only in GPI or open-drain case)	
PIN41_48	1	R/W	0	Pull Up Control06 – Pin41~48 0: Disable 1: Enable (active only in GPI or open-drain case)	
Reserved	0	R/W	0	reserved to 0	

(for Pin 74,75,78,79 0xB6 is effectively only if 0xA9(Bit7:6)=2'b10)

Register:: PIN SHARE CTRL13 0xB6					
Name	Bits	Read/ Write	Reset State	Comments	Config
P9D0	7:6	R/W	0x00	Pin74 00: P9D0o (push-pull) <O> 01: reserved 10: reserved 11: Reserved TXO3+_8b when DISP_TYPE(8C-00) set to LVDS	
P9D1	5:4	R/W	0x00	Pin75 00: P9D1o (push-pull) <O> 01: reserved 10: reserved 11: Reserved TXO3-_8b when DISP_TYPE(8C-00) set to LVDS	
P9D4	3:2	R/W	0x00	Pin78 00: P9D4o (push-pull) <O> 01: reserved 10: reserved 11: Reserved TXO2+_8b when DISP_TYPE(8C-00) set to LVDS	
PAD0	1:0	R/W	0x00	Pin79 00: PAD0o (push-pull) <O> 01: reserved 10: reserved 11: Reserved TXO2-_8b when DISP_TYPE(8C-00) set to LVDS	

Register:: PIN SHARE CTRL14 0xB7					
Name	Bits	Read/ Write	Reset	Comments	Config



		Write	State	
PDD7	7:6	R/W	0x00	Pin31 00: PDD7i <I><default> 01: PDD7o <O><Push-Pull> 10: PDD7o <O><Open-drain> 11: Reserved
PDD6	5:4	R/W	0x00	Pin32 00: PDD6i <I><default> 01: PDD6o <O><Push-Pull> 10: PDD6o <O><Open-drain> 11: Reserved
PDD5	3:2	R/W	0x00	Pin33 00: PDD5i <I><default> 01: PDD5o <O><Push-Pull> 10: PDD5o <O><Open-drain> 11: Reserved
PDD4	1:0	R/W	0x00	Pin34 00: PDD4i <I><default> 01: PDD4o <O><Push-Pull> 10: PDD4o <O><Open-drain> 11: Reserved

Note :If Pin 31~Pin 39 is GPI Function

- (1) 0x10 Bit 3:2 (b00)
- (2) 0xFFE6 Bit5 PD_pin_reg_n =1

Register:: PIN SHARE CTRL15 0xB8					
Name	Bits	Read/ Write	Reset State	Comments	Config
PDD3	7:6	R/W	0x00	Pin35 00: PDD3i <I><default> 01: PDD3o <O><Push-Pull> 10: PDD3o <O><Open-drain> 11: Reserved	
PDD2	5:4	R/W	0x00	Pin36 00: PDD2i <I><default> 01: PDD2o <O><Push-Pull> 10: PDD2o <O><Open-drain> 11: Reserved	
PDD1	3:2	R/W	0x00	Pin37 00: PDD1i <I><default> 01: PDD1o <O><Push-Pull> 10: PDD1o <O><Open-drain> 11: Reserved	
PDD0	1:0	R/W	0x00	Pin39 00: PDD0i <I><default> 01: PDD0o <O><Push-Pull> 10: PDD0o <O><Open-drain> 11: Reserved	

Register:: PIN SHARE CTRL16 0xB9					
Name	Bits	Read/ Write	Reset State	Comments	Config



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PIN116_118	7	R/W	0	Driving Current Control07 – Pin116~118 0: 4mA 1: 2mA	
V8_ADC_SEL	6	R/W	0	Video 8 From ADC selection 0: From Pin 31-37, 39 1: From Pin 5-57, 63-67, 39 (For 72 pin package)	
Reserved	5:4	R/W	0x00	Reserved	
Xtal_SPREAD_EN	3	R/W	0	Xtal Spread Spectrum Enable 0: Disable, reset capacitor select 1: Enable	
Xtal_SPREAD_M ANUAL_SWITCH	2	R/W	0	Xtal Spread Spectrum Source Manual Switch 0: No Change 1: Switch to different frequency User must set “0: No Change” before “1: Switch to different frequency” (Only take effect when Page 10 CRBA[7:6] = 2'b11)	
PCD4	1:0	R/W	0x00	Pin40 00: PCD4i <I> <default> 01: PCD4o <O> <push-pull> 10: PCD4o <O> <open-drain> 11: Reserved	

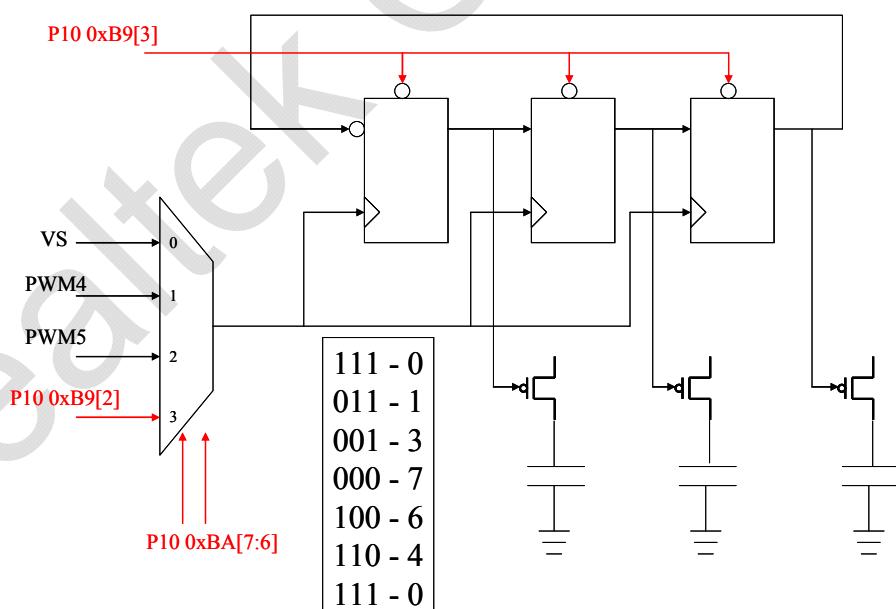
Register:: Test Function for 64-128 Pin Change					0xBA
Name	Bits	Read/ Write	Reset State	Comments	Config
Xtal_SPREAD_SO URCE_SEL	7:6	R/W	0x00	Xtal Spread Spectrum Source Select 00: Reference to VS 01: Reference to PWM4 10: Reference to PWM5 11: Adjust by FW (reference to Page 10 CRB9[2])	
Reserved	5:4	R/W	0x00	Reserved	
Reserved	3:2	R/W	0x00	Reserved	
64-128 Pin Change	1:0	R/W	0x00	00: 128 Pin <Default> 01: Dual-LVDS No use Pin : (Pin : 11~20(10) <TMDS1> Pin:28(1) <SOG0> Pin:31~37 (7) <V8,VGA1> Pin:39~49 (11) <GPIO> Pin:61~62 (2) <PGND,PVCC> Pin:65~73 (9) <GPIO> Pin:76~77 (2) <GPIO,LVDS> Pin:85 (1) <PGND> Pin:96~102 (7) <GPIO> Pin:105~114 (10) <GPIO> Pin:119 (1) <GPIO>	



			Pin:121~122 (2) <GPIO> Pin:125 (1) <RESETB>	
			10: Single-LVDS No use Pin : (Pin : 11~20(10) <TMDS1> Pin:28(1) <SOG0> Pin:31~37 (7) <V8,VGA1> Pin:39~49 (11) <GPIO> Pin:61~62 (2) <PGND,PVCC> Pin:65~73 (9) <GPIO> Pin:76~77 (2) <GPIO,LVDS> Pin:85 (1) <PGND> Pin:96~102 (7) <GPIO> Pin:105~114 (10) <GPIO> Pin:119 (1) <GPIO> Pin:121~122 (2) <GPIO> Pin:125 (1) <RESETB> 11:Reserved	

CRBA[7:6] is used to choose switch reference source, the default capacitor setting is 111(minimum offset). Once VS / PWM signal latched, capacitor will change (111→011→001...,000 is maximum offset).

In manual switch mode, user set CRB9[2] will change the capacitor only one time. If user want to change capacitor again, must set “0: No Change” and then set “1: Switch to different frequency”.





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Register:: DVI_CTRL_OUT_SEL 0xBB					
Name	Bits	Read/ Write	Reset State	Comments	Config
Reserved	7:6	R/W	0x00	Reserved	
PCD3	5	R/W	0	DVI CTRL OUT1 (Pin63) output enable 0: Disable (ref. original Pin63 pin share) 1: Enable	
P7D5	4	R/W	0x00	DVI CTRL OUT2 (Pin103) output enable 0: Disable (ref. original Pin103 pin share) 1: Enable	
DVI_CTRL_OUT1	3:2	R/W	0x00	DVI CTRL OUT1 select 00:CTRL0, 01:CTRL1, 10:CTRL2, 11:CTRL3	
DVI_CTRL_OUT2	1:0	R/W	0x00	DVI CTRL OUT2 select 00:CTRL0, 01:CTRL1, 10:CTRL2, 11:CTRL3	



Embedded OSD

Addressing and Accessing Register

ADDRESS	BIT							
	7	6	5	4	3	2	1	0
High Byte	-	-	-	-	-	-	-	A12
Med Byte	A15	A14	A13	A12	A11	A10	A9	A8
Low Byte	A7	A6	A5	A4	A3	A2	A1	A0

Figure 3. Addressing and Accessing Registers

Date	BIT							
Byte 0	D7	D6	D5	D4	D3	D2	D1	D0
Byte 1	D7	D6	D5	D4	D3	D2	D1	D0
Byte 2	D7	D6	D5	D4	D3	D2	D1	D0

Figure 2. Data Registers

All kind of registers can be controlled and accessed by these 2 bytes, and each address contains 3-byte data, details are described as follows:

Write mode: [A15:A14] select which byte to write

-00: Byte 0 -01:Byte 1 -10: Byte 2 -11: All

*All data are sorted by these three Bytes (Byte0~Byte2)

[A13] Auto Load (Double Buffer)

[A12] Address indicator

-0: Window and frame control registers.

-1: Font Select and font map SRAM

[A12:A0] Address mapping

- Font Select and font map SRAM address: 000~1A9F 6.67k*3byte

-Frame control register address: 000~0xx (**Latch**)

-Window control register address: 100~1xx (**Latch**)

* Selection of SRAM address or Latch address selection is determined by A12!

Example:

Bit [15:14]=00

-All data followed are written to byte0 and address increases.

Byte0 → Byte0 → Byte0... (Address will auto increase)

Bit [15:14]=01



-All data followed are written to byte1 and address increases.

Byte1 → Byte1 → Byte1... (Address will auto increase)

Bit [15:14]=11

- Address will be increased after each 3-byte data written.

Byte0 → Byte1 → Byte2 → Byte0 → Byte1 → Byte2... (Address will auto increase)

Window control registers

- Windows all support shadow/border/3D button
- Window0, 5, 6, 7, 8, 9 support gradient functions.
- Window 0, 1, 2, 3, 4, 4-1~4-8, 5, 6, 7, 8, 9 start/end resolution are 1line(pixel)
- All window start and end position include the **special effect (border/shadow/3D button)** been assigned
- Font comes after windows by 10 pixels, so you should compensate 10 pixels on windows to meet font position

Window 0 Shadow/Border/Gradient

Address: 100h

Byte 0

Bit	Mode	Function
7	W	Window 0 shadow color index in 64-color LUT [4]
6	W	Window 0 border color index in 64-color LUT [4]
5:3	W	Window 0 shadow/border width or 3D button thickness in pixel unit 000~111: 1 ~ 8 pixel
2:0	W	Window 0 shadow/border height in line unit 000~111: 1 ~ 8 line It must be the same as bit [5:3] for 3D button thickness

Byte 1

Bit	Mode	Function
7:4	W	Window 0 shadow color index in 64-color LUT [3:0] For 3D window, it is the left-top/bottom border color
3:0	W	Window 0 border color index in 64-color LUT [3:0] For 3D window, it is the right-bottom/top border color

Byte 2

Bit	Mode	Function
7	W	R Gradient Polarity 0: Decrease 1: Increase



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6	W	G Gradient Polarity 0: Decrease 1: Increase
5	W	B Gradient Polarity 0: Decrease 1: Increase
4:3	W	Gradient level 00: 1 step per level 01: Repeat 2 step per level 10: Repeat 3 step per level 11: Repeat 4 step per level
2	W	Enable Red Color Gradient
1	W	Enable Green Color Gradient
0	W	Enable Blue Color Gradient

**Window 0 start position****Address: 101h**

Byte 0

Bit	Mode	Function
7:4	W	Window 0 horizontal start[11:8]
3:0	W	Window 0 vertical start [11:8]

Byte 1

Bit	Mode	Function
7:0	W	Window 0 horizontal start[7:0]

Byte 2

Bit	Mode	Function
7:0	W	Window 0 vertical start [7:0]

Start position must be increments of four.

Window 0 end position**Address: 102h**

Byte 0

Bit	Mode	Function
7:4	W	Window 0 horizontal end [11:8]
3:0	W	Window 0 vertical end [11:8]

Byte 1

Bit	Mode	Function
7:0	W	Window 0 horizontal end [7:0]

Byte 2

Bit	Mode	Function
7:0	W	Window 0 vertical end [7:0]

- End position must be increments of four.

Window 0 control**Address: 103h**

Byte 0

Bit	Mode	Function
7	W	Window 0 shadow color index in 64-color LUT [5]
6	W	Window 0 border color index in 64-color LUT [5]
5	W	Window 0 color index in 64-color LUT [5]
4	W	Saturated color mode for gradient (refer to ADDR 150 for saturated color setting) 0: disable 1: enable



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RTD2261W/2271W/2281W Series-GR

3	W	Reversed color mode for gradient (valid while [4] is 1) 0: disable 1: enable
2:0	--	Reserved

Byte 1

Bit	Mode	Function
7:5	W	111: 7 level per gradient 110: 6 level per gradient 101: 5 level per gradient 100: 4 level per gradient 011: 3 level per gradient 010: 2 level per gradient 001: 1 level per gradient 000: 8 level per gradient
4:0	W	Window 0 color index in 64-color LUT [4:0]

Byte 2

default: 00h

Bit	Mode	Function
7	W	Blend function 0: Disable 1: Enable
6	W	Gradient function 0: Disable 1: Enable
5	W	Gradient direction 0: Horizontal 1: Vertical
4	W	Shadow/Border/3D button 0: Disable 1: Enable
3:1	W	Window 0 Type 000: Shadow Type 1 001: Shadow Type 2 010: Shadow Type3 011: Shadow Type 4 100: 3D Button Type 1 101: 3D Button Type 2



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RTD2261W/2271W/2281W Series-GR

		110: Reserved 111: Border
0	W	Window 0 Enable 0: Disable 1: Enable

Window 1 Shadow/Border/Gradient**Address: 104h**

Byte 0

Bit	Mode	Function
7	W	Window 1 shadow color index in 64-color LUT [4]
6	W	Window 1 border color index in 64-color LUT [4]
5:3	W	Window 1 shadow/border width or 3D button thickness in pixel unit 000~111: 1 ~ 8 pixel
2:0	W	Window 1 shadow/border height in line unit 000~111: 1 ~ 8 line It must be the same as bit [5:3] for 3D button thickness

Byte 1

Bit	Mode	Function
7:4	W	Window 1 shadow color index in 64-color LUT [3:0] For 3D window, it is the left-top/bottom border color
3:0	W	Window 1 border color index in 64-color LUT [3:0] For 3D window, it is the right-bottom/top border color

Byte 2

Bit	Mode	Function
7:0	W	Reserved

Window 1 start position**Address: 105h**

Byte 0

Bit	Mode	Function
7:4	W	Window 1 horizontal start [11:8]
3:0	W	Window 1 vertical start [11:8]



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RTD2261W/2271W/2281W Series-GR

Byte 1

Bit	Mode	Function
7:0	W	Window 1 horizontal start [7:0]

Byte 2

Bit	Mode	Function
7:0	W	Window 1 vertical start [7:0]

Window 1 end position

Address: 106h

Byte 0

Bit	Mode	Function
7:4	W	Window 1 horizontal end [11:8]
3:0	W	Window 1 vertical end [11:8]

Byte 1

Bit	Mode	Function
7:0	W	Window 1 horizontal end [7:0]

Byte 2

Bit	Mode	Function
7:0	W	Window 1 vertical end [7:0]



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RTD2261W/2271W/2281W Series-GR

Window 1 control**Address: 107h**

Byte 0

Bit	Mode	Function
7	W	Window 1 shadow color index in 64-color LUT [5]
6	W	Window 1 border color index in 64-color LUT [5]
5	W	Window 1 color index in 64-color LUT [5]
4:0	--	Reserved

Byte 1

Bit	Mode	Function
7:5	--	Reserved
4:0	W	Window 1 color index in 64-color LUT [4:0]

Byte 2

default: 00h

Bit	Mode	Function
7	W	Blend function 0: Disable 1: Enable
6:5	W	Reserved
4	W	Shadow/Border/3D button 0: Disable 1: Enable
3:1	W	Window 1 Type 000: Shadow Type 1 001: Shadow Type 2 010: Shadow Type3 011: Shadow Type 4 100: 3D Button Type 1 101: 3D Button Type 2 110: Reserved 111: Border
0	W	Window 1 Enable 0: Disable 1: Enable

Window 2 Shadow/Border/Gradient**Address: 108h**

Byte 0

Bit	Mode	Function



REALTEK

RTD2261W/2271W/2281W Series-GR

7	W	Window 2 shadow color index in 64-color LUT [4]
6	W	Window 2 border color index in 64-color LUT [4]
5:3	W	Window 2 shadow/border width or 3D button thickness in pixel unit 000~111: 1 ~ 8 pixel
2:0	W	Window 2 shadow/border height in line unit 000~111: 1 ~ 8 line It must be the same as bit [5:3] for 3D button thickness

Byte 1

Bit	Mode	Function
7:4	W	Window 2 shadow color index in 64-color LUT [3:0] For 3D window, it is the left-top/bottom border color
3:0	W	Window 2 border color index in 64-color LUT [3:0] For 3D window, it is the right-bottom/top border color

Byte 2

Bit	Mode	Function
7:0	W	Reserved

Window 2 start position**Address: 109h**

Byte 0

Bit	Mode	Function
7:4	W	Window 2 horizontal start [11:8]
3:0	W	Window 2 vertical start [11:8]

Byte 1

Bit	Mode	Function
7:0	W	Window 2 horizontal start [7:0]

Byte 2

Bit	Mode	Function
7:0	W	Window 2 vertical start [7:0]

Window 2 end position**Address: 10Ah**

Byte 0

Bit	Mode	Function
7:4	W	Window 2 horizontal end [11:8]
3:0	W	Window 2 vertical end [11:8]



REALTEK

RTD2261W/2271W/2281W Series-GR

Byte 1

Bit	Mode	Function
7:0	W	Window 2 horizontal end [7:0]

Byte 2

Bit	Mode	Function
7:0	W	Window 2 vertical end [7:0]

Window 2 control

Address: 10Bh

Byte 0

Bit	Mode	Function
7	W	Window 2 shadow color index in 64-color LUT [5]
6	W	Window 2 border color index in 64-color LUT [5]
5	W	Window 2 color index in 64-color LUT [5]
4:0	--	Reserved

Byte 1

Bit	Mode	Function
7:5	--	Reserved
4:0	W	Window 2 color index in 64-color LUT [4:0]

Byte 2

default: 00h

Bit	Mode	Function
7	W	Blend function 0: Disable 1: Enable
6:5	W	Reserved
4	W	Shadow/Border/3D button 0: Disable 1: Enable
3:1	W	Window 2 Type 000: Shadow Type 1 001: Shadow Type 2 010: Shadow Type3 011: Shadow Type 4 100: 3D Button Type 1 101: 3D Button Type 2 110: Reserved 111: Border



REALTEK

RTD2261W/2271W/2281W Series-GR

0	W	Window 2 Enable 0: Disable 1: Enable
---	---	--

Window 3 Shadow/Border/Gradient**Address: 10Ch**

Byte 0

Bit	Mode	Function
7	W	Window 3 shadow color index in 64-color LUT [4]
6	W	Window 3 border color index in 64-color LUT [4]
5:3	W	Window 3 shadow/border width or 3D button thickness in pixel unit 000~111: 1 ~ 8 pixel
2:0	W	Window 3 shadow/border height in line unit 000~111: 1 ~ 8 line It must be the same as bit [5:3] for 3D button thickness

Byte 1

Bit	Mode	Function
7:4	W	Window 3 shadow color index in 64-color LUT [3:0] For 3D window, it is the left-top/bottom border color
3:0	W	Window 3 border color index in 64-color LUT [3:0] For 3D window, it is the right-bottom/top border color

Byte 2

Bit	Mode	Function
7:0	W	Reserved

Window 3 start position**Address: 10Dh**

Byte 0

Bit	Mode	Function
7:4	W	Window 3 horizontal start [11:8]
3:0	W	Window 3 vertical start [11:8]

Byte 1

Bit	Mode	Function
7:0	W	Window 3 horizontal start [7:0]

Byte 2

Bit	Mode	Function
7:0	W	Window 3 vertical start [7:0]



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RTD2261W/2271W/2281W Series-GR

Window 3 end position**Address: 10Eh**

Byte 0

Bit	Mode	Function
7:4	W	Window 3 horizontal end [11:8]
3:0	W	Window 3 vertical end [11:8]

Byte 1

Bit	Mode	Function
7:0	W	Window 3 horizontal end [7:0]

Byte 2

Bit	Mode	Function
7:0	W	Window 3 vertical end [7:0]

Window 3 control**Address: 10Fh**

Byte 0

Bit	Mode	Function
7	W	Window 3 shadow color index in 64-color LUT [5]
6	W	Window 3 border color index in 64-color LUT [5]
5	W	Window 3 color index in 64-color LUT [5]
4:0	--	Reserved

Byte 1

Bit	Mode	Function
7:5	--	Reserved
4:0	W	Window 3 color index in 64-color LUT [4:0]

Byte 2

default: 00h

Bit	Mode	Function
7	W	Blend function 0: Disable 1: Enable
6:5	W	Reserved
4	W	Shadow/Border/3D button 0: Disable 1: Enable
3:1	W	Window 3 Type



REALTEK

RTD2261W/2271W/2281W Series-GR

		000: Shadow Type 1 001: Shadow Type 2 010: Shadow Type3 011: Shadow Type 4 100: 3D Button Type 1 101: 3D Button Type 2 110: Reserved 111: Border
0	W	Window 3 Enable 0: Disable 1: Enable

Window 4 Shadow/Border/Gradient**Address: 110h**

Byte 0

Bit	Mode	Function
7	W	Window 4 shadow color index in 64-color LUT [4]
6	W	Window 4 border color index in 64-color LUT [4]
5:3	W	Window 4 shadow/border width or 3D button thickness in pixel unit 000~111: 1 ~ 8 pixel
2:0	W	Window 4 shadow/border height in line unit 000~111: 1 ~ 8 line It must be the same as bit [5:3] for 3D button thickness

Byte 1

Bit	Mode	Function
7:4	W	Window 4 shadow color index in 64-color LUT [3:0] For 3D window, it is the left-top/ bottom border color
3:0	W	Window 4 border color index in 64-color LUT [3:0] For 3D window, it is the right-bottom/top border color

Byte 2

Bit	Mode	Function
7:0	W	Reserved

Window 4 start position**Address: 111h**

Byte 0

Bit	Mode	Function
7:4	W	Window 4 horizontal start [11:8]



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3:0	W	Window 4 vertical start [11:8]
-----	---	--------------------------------

Byte 1

Bit	Mode	Function
7:0	W	Window 4 horizontal start [7:0]

Byte 2

Bit	Mode	Function
7:0	W	Window 4 vertical start [7:0]

Window 4 end position**Address: 112h**

Byte 0

Bit	Mode	Function
7:4	W	Window 4 horizontal end [11:8]
3:0	W	Window 4 vertical end [11:8]

Byte 1

Bit	Mode	Function
7:0	W	Window 4 horizontal end [7:0]

Byte 2

Bit	Mode	Function
7:0	W	Window 4 vertical end [7:0]

Window 4 control**Address: 113h**

Byte 0

Bit	Mode	Function
7:0	--	Reserved

Byte 1

Bit	Mode	Function
7:4	--	Reserved
3:0	W	Window 4 color index in 64-color LUT [3:0]

Byte 2

default: 00h

Bit	Mode	Function
7	W	Blend function 0: Disable 1: Enable
6:5	W	Reserved
4	W	Shadow/Border/3D button 0: Disable



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RTD2261W/2271W/2281W Series-GR

		1: Enable
3:1	W	Window 4 Type 000: Shadow Type 1 001: Shadow Type 2 010: Shadow Type3 011: Shadow Type 4 100: 3D Button Type 1 101: 3D Button Type 2 110: Reserved 111: Border
0	W	Window 4 Enable 0: Disable 1: Enable

Window 5 Shadow/Border/Gradient**Address: 114h**

Byte 0

Bit	Mode	Function
7	W	Window 5 shadow color index in 64-color LUT [4]
6	W	Window 5 border color index in 64-color LUT [4]
5:3	W	Window 5 shadow/border width or 3D button thickness in pixel unit 000~111: 1 ~ 8 pixel
2:0	W	Window 5 shadow/border height in line unit 000~111: 1 ~ 8 line It must be the same as bit [5:3] for 3D button thickness

Byte 1

Bit	Mode	Function
7:4	W	Window 5 shadow color index in 64-color LUT [3:0] For 3D window, it is the left-top/bottom border color
3:0	W	Window 5 border color index in 64-color LUT [3:0] For 3D window, it is the right-bottom/top border color

Byte 2

Bit	Mode	Function
7	W	R Gradient Polarity 0: Decrease 1: Increase
6	W	G Gradient Polarity 0: Decrease



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RTD2261W/2271W/2281W Series-GR

		1: Increase
5	W	B Gradient Polarity 0: Decrease 1: Increase
4:3	W	Gradient level 00: 1 step per level 01: Repeat 2 step per level 10: Repeat 3 step per level 11: Repeat 4 step per level
2	W	Enable Red Color Gradient
1	W	Enable Green Color Gradient
0	W	Enable Blue Color Gradient

Window 5 start position**Address: 115h**

Byte 0

Bit	Mode	Function
7:4	W	Window 5 horizontal start [11:8]
3:0	W	Window 5 vertical start [11:8]

Byte 1

Bit	Mode	Function
7:0	W	Window 5 horizontal start [7:0]

Byte 2

Bit	Mode	Function
7:0	W	Window 5 vertical start [7:0]

Window 5 end position**Address: 116h**

Byte 0

Bit	Mode	Function
7:4	W	Window 5 horizontal end [11:8]
3:0	W	Window 5 vertical end [11:8]

Byte 1

Bit	Mode	Function
7:0	W	Window 5 horizontal end [7:0]

Byte 2

Bit	Mode	Function
7:0	W	Window 5 vertical end [7:0]

Window 5 control



REALTEK

RTD2261W/2271W/2281W Series-GR

Address: 117h

Byte 0

Bit	Mode	Function
7	W	Window 5 shadow color index in 64-color LUT [5]
6	W	Window 5 border color index in 64-color LUT [5]
5	W	Window 5 color index in 64-color LUT [5]
4	W	Saturated color mode for gradient (refer to ADDR 15A for saturated color setting) 0: disable 1: enable
3	W	Reversed color mode for gradient (valid while [4] is 1) 0: disable 1: enable
2:0	--	Reserved

Byte 1

Bit	Mode	Function
7:5	W	111: 7 level per gradient 110: 6 level per gradient 101: 5 level per gradient 100: 4 level per gradient 011: 3 level per gradient 010: 2 level per gradient 001: 1 level per gradient 000: 8 level per gradient
4:0	W	Window 5 color index in 64-color LUT [4:0]

Byte 2

default: 00h

Bit	Mode	Function
7	W	Blend function 0: Disable 1: Enable
6	W	Gradient function 0: Disable 1: Enable
5	W	Gradient direction 0: Horizontal



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RTD2261W/2271W/2281W Series-GR

		1: Vertical
4	W	Shadow/Border/3D button 0: Disable 1: Enable
3:1	W	Window 5 Type 000: Shadow Type 1 001: Shadow Type 2 010: Shadow Type3 011: Shadow Type 4 100: 3D Button Type 1 101: 3D Button Type 2 110: Reserved 111: Border
0	W	Window 5 Enable 0: Disable 1: Enable

Window 6 Shadow/Border/Gradient**Address: 118h**

Byte 0

Bit	Mode	Function
7	W	Window 6 shadow color index in 64-color LUT [4]
6	W	Window 6 border color index in 64-color LUT [4]
5:3	W	Window 6 shadow/border width or 3D button thickness in pixel unit 000~111: 1 ~ 8 pixel
2:0	W	Window 6 shadow/border height in line unit 000~111: 1 ~ 8 line It must be the same as bit [5:3] for 3D button thickness

PS: This is for non-rotary, rotate 270, rotate 90 and 180.

Byte 1

Bit	Mode	Function
7:4	W	Window 6 shadow color index in 64-color LUT [3:0] For 3D window, it is the left-top/ bottom border color
3:0	W	Window 6 border color index in 64-color LUT [3:0] For 3D window, it is the right-bottom/top border color

Byte 2

Bit	Mode	Function



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RTD2261W/2271W/2281W Series-GR

7	W	R Gradient Polarity 0: Decrease 1: Increase
6	W	G Gradient Polarity 0: Decrease 1: Increase
5	W	B Gradient Polarity 0: Decrease 1: Increase
4:3	W	Gradient level 00: 1 step per level 01: Repeat 2 step per level 10: Repeat 3 step per level 11: Repeat 4 step per level
2	W	Enable Red Color Gradient
1	W	Enable Green Color Gradient
0	W	Enable Blue Color Gradient

Window 6 start position**Address: 119h**

Byte 0

Bit	Mode	Function
7:4	W	Window 6 horizontal start [11:8]
3:0	W	Window 6 vertical start [11:8]

Byte 1

Bit	Mode	Function
7:0	W	Window 6 horizontal start [7:0]

Byte 2

Bit	Mode	Function
7:0	W	Window 6 vertical start [7:0]

Window 6 end position**Address: 11Ah**

Byte 0

Bit	Mode	Function
7:4	W	Window 6 horizontal end [11:8]
3:0	W	Window 6 vertical end [11:8]

Byte 1



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Bit	Mode	Function
7:0	W	Window 6 horizontal end [7:0]

Byte 2

Bit	Mode	Function
7:0	W	Window 6 vertical end [7:0]

Window 6 control**Address: 11Bh**

Byte 0

Bit	Mode	Function
7	W	Window 6 shadow color index in 64-color LUT [5]
6	W	Window 6 border color index in 64-color LUT [5]
5	W	Window 6 color index in 64-color LUT [5]
4	W	Saturated color mode for gradient (refer to ADDR 15C for saturated color setting) 0: disable 1: enable
3	W	Reversed color mode for gradient (valid while [4] is 1) 0: disable 1: enable
2:0	--	Reserved

Byte 1

Bit	Mode	Function
7:5	W	111: 7 level per gradient 110: 6 level per gradient 101: 5 level per gradient 100: 4 level per gradient 011: 3 level per gradient 010: 2 level per gradient 001: 1 level per gradient 000: 8 level per gradient
4:0	W	Window 6 color index in 64-color LUT [4:0]

Byte 2

default: 00h

Bit	Mode	Function
7	W	Blend function 0: Disable 1: Enable



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6	W	Gradient function 0: Disable 1: Enable
5	W	Gradient direction 0: Horizontal 1: Vertical
4	W	Shadow/Border/3D button 0: Disable 1: Enable
3:1	W	Window 6 Type 000: Shadow Type 1 001: Shadow Type 2 010: Shadow Type3 011: Shadow Type 4 100: 3D Button Type 1 101: 3D Button Type 2 110: Reserved 111: Border
0	W	Window 6 Enable 0: Disable 1: Enable

Window 7 Shadow/Border/Gradient**Address: 11Ch**

Byte 0

Bit	Mode	Function
7	W	Window 7 shadow color index in 64-color LUT [4]
6	W	Window 7 border color index in 64-color LUT [4]
5:3	W	Window 7 shadow/border width or 3D button thickness in pixel unit 000~111: 1 ~ 8 pixel
2:0	W	Window 7 shadow/border height in line unit 000~111: 1 ~ 8 line It must be the same as bit [5:3] for 3D button thickness

PS: This is for non-rotary, rotate 270, rotate 90 and 180.

Byte 1

Bit	Mode	Function
7:4	W	Window 7 shadow color index in 64-color LUT [3:0]



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		For 3D window, it is the left-top/bottom border color
3:0	W	Window 7 border color index in 64-color LUT [3:0] For 3D window, it is the right-bottom/top border color

Byte 2

Bit	Mode	Function
7	W	R Gradient Polarity 0: Decrease 1: Increase
6	W	G Gradient Polarity 0: Decrease 1: Increase
5	W	B Gradient Polarity 0: Decrease 1: Increase
4:3	W	Gradient level 00: 1 step per level 01: Repeat 2 step per level 10: Repeat 3 step per level 11: Repeat 4 step per level
2	W	Enable Red Color Gradient
1	W	Enable Green Color Gradient
0	W	Enable Blue Color Gradient

Window 7 start position**Address: 11Dh**

Byte 0

Bit	Mode	Function
7:4	W	Window 7 horizontal start [11:8]
3:0	W	Window 7 vertical start [11:8]

Byte 1

Bit	Mode	Function
7:0	W	Window 7 horizontal start [7:0]

Byte 2

Bit	Mode	Function
7:0	W	Window 7 vertical start [7:0]

Window 7 end position**Address: 11Eh**

Byte 0



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RTD2261W/2271W/2281W Series-GR

Bit	Mode	Function
7:4	W	Window 7 horizontal end [11:8]
3:0	W	Window 7 vertical end [11:8]

Byte 1

Bit	Mode	Function
7:0	W	Window 7 horizontal end [7:0]

Byte 2

Bit	Mode	Function
7:0	W	Window 7 vertical end [7:0]

Window 7 control

Address: 11Fh

Byte 0

Bit	Mode	Function
7	W	Window 7 shadow color index in 64-color LUT [5]
6	W	Window 7 border color index in 64-color LUT [5]
5	W	Window 7 color index in 64-color LUT [5]
4	W	Saturated color mode for gradient (refer to ADDR 15E for saturated color setting) 0: disable 1: enable
3	W	Reversed color mode for gradient (valid while [4] is 1) 0: disable 1: enable
2:0	--	Reserved

Byte 1

Bit	Mode	Function
7:5	W	111: 7 level per gradient 110: 6 level per gradient 101: 5 level per gradient 100: 4 level per gradient 011: 3 level per gradient 010: 2 level per gradient 001: 1 level per gradient 000: 8 level per gradient
4:0	W	Window 7 color index in 64-color LUT [4:0]



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RTD2261W/2271W/2281W Series-GR

Byte 2

default: 00h

Bit	Mode	Function
7	W	Blend function 0: Disable 1: Enable
6	W	Gradient function 0: Disable 1: Enable
5	W	Gradient direction 0: Horizontal 1: Vertical
4	W	Shadow/Border/3D button 0: Disable 1: Enable
3:1	W	Window 7 Type 000: Shadow Type 1 001: Shadow Type 2 010: Shadow Type3 011: Shadow Type 4 100: 3D Button Type 1 101: 3D Button Type 2 110: Reserved 111: Border
0	W	Window 7 Enable 0: Disable 1: Enable

Window 8 Shadow/Border/Gradient

Address: 120h

Byte 0

Bit	Mode	Function
7	W	Window 8 shadow color index in 64-color LUT [4]
6	W	Window 8 border color index in 64-color LUT [4]
5:3	W	Window 8 shadow/border width or 3D button thickness in pixel unit 000~111: 1 ~ 8 pixel
2:0	W	Window 8 shadow/border height in line unit



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		000~111: 1 ~ 8 line It must be the same as bit [5:3] for 3D button thickness
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PS: This is for non-rotary, rotate 270, rotate 90 and 180.

Byte 1

Bit	Mode	Function
7:4	W	Window 8 shadow color index in 64-color LUT [3:0] For 3D window, it is the left-top/bottom border color
3:0	W	Window 8 border color index in 64-color LUT [3:0] For 3D window, it is the right-bottom/top border color

Byte 2

Bit	Mode	Function
7	W	R Gradient Polarity 0: Decrease 1: Increase
6	W	G Gradient Polarity 0: Decrease 1: Increase
5	W	B Gradient Polarity 0: Decrease 1: Increase
4:3	W	Gradient level 00: 1 step per level 01: Repeat 2 step per level 10: Repeat 3 step per level 11: Repeat 4 step per level
2	W	Enable Red Color Gradient
1	W	Enable Green Color Gradient
0	W	Enable Blue Color Gradient

Window 8 start position

Address: 121h

Byte 0

Bit	Mode	Function
7:4	W	Window 8 horizontal start [11:8]
3:0	W	Window 8 vertical start [11:8]

Byte 1

Bit	Mode	Function
7:0	W	Window 8 horizontal start [7:0]



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Byte 2

Bit	Mode	Function
7:0	W	Window 8 vertical start [7:0]

Window 8 end position**Address: 122h**

Byte 0

Bit	Mode	Function
7:4	W	Window 8 horizontal end [11:8]
3:0	W	Window 8 vertical end [11:8]

Byte 1

Bit	Mode	Function
7:0	W	Window 8 horizontal end [7:0]

Byte 2

Bit	Mode	Function
7:0	W	Window 8 vertical end [7:0]

Window 8 control**Address: 123h**

Byte 0

Bit	Mode	Function
7	W	Window 8 shadow color index in 64-color LUT [5]
6	W	Window 8 border color index in 64-color LUT [5]
5	W	Window 8 color index in 64-color LUT [5]
4	W	Saturated color mode for gradient (refer to ADDR 160 for saturated color setting) 0: disable 1: enable
3	W	Reversed color mode for gradient (valid while [4] is 1) 0: disable 1: enable
2:0	--	Reserved

Byte 1

Bit	Mode	Function
7:5	W	111: 7 level per gradient 110: 6 level per gradient 101: 5 level per gradient 100: 4 level per gradient



REALTEK

RTD2261W/2271W/2281W Series-GR

		011: 3 level per gradient 010: 2 level per gradient 001: 1 level per gradient 000: 8 level per gradient
4:0	W	Window 8 color index in 64-color LUT [4:0]

Byte 2

default: 00h

Bit	Mode	Function
7	W	Blend function 0: Disable 1: Enable
6	W	Gradient function 0: Disable 1: Enable
5	W	Gradient direction 0: Horizontal 1: Vertical
4	W	Shadow/Border/3D button 0: Disable 1: Enable
3:1	W	Window 8 Type 000: Shadow Type 1 001: Shadow Type 2 010: Shadow Type 3 011: Shadow Type 4 100: 3D Button Type 1 101: 3D Button Type 2 110: Reserved 111: Border
0	W	Window 8 Enable 0: Disable 1: Enable

Window 9 Shadow/Border/Gradient

Address: 124h

Byte 0

Bit	Mode	Function
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REALTEK

RTD2261W/2271W/2281W Series-GR

7	W	Window 9 shadow color index in 64-color LUT [4]
6	W	Window 9 border color index in 64-color LUT [4]
5:3	W	Window 9 shadow/border width or 3D button thickness in pixel unit 000~111; 1 ~ 8 pixel
2:0	W	Window 9 shadow/border height in line unit 000~111; 1 ~ 8 line It must be the same as bit [5:3] for 3D button thickness

PS: This is for non-rotary, rotate 270, rotate 90 and 180.

Byte 1

Bit	Mode	Function
7:4	W	Window 9 shadow color index in 64-color LUT [3:0] For 3D window, it is the left-top/bottom border color
3:0	W	Window 9 border color index in 64-color LUT [3:0] For 3D window, it is the right-bottom/top border color

Byte 2

Bit	Mode	Function
7	W	R Gradient Polarity 0: Decrease 1: Increase
6	W	G Gradient Polarity 0: Decrease 1: Increase
5	W	B Gradient Polarity 0: Decrease 1: Increase
4:3	W	Gradient level 00: 1 step per level 01: Repeat 2 step per level 10: Repeat 3 step per level 11: Repeat 4 step per level
2	W	Enable Red Color Gradient
1	W	Enable Green Color Gradient
0	W	Enable Blue Color Gradient

Window 9 start position

Address: 125h

Byte 0

Bit	Mode	Function



REALTEK

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7:4	W	Window 9 horizontal start [11:8]
3:0	W	Window 9 vertical start [11:8]

Byte 1

Bit	Mode	Function
7:0	W	Window 9 horizontal start [7:0]

Byte 2

Bit	Mode	Function
7:0	W	Window 9 vertical start [7:0]

Window 9 end position**Address: 126h**

Byte 0

Bit	Mode	Function
7:4	W	Window 9 horizontal end [11:8]
3:0	W	Window 9 vertical end [11:8]

Byte 1

Bit	Mode	Function
7:0	W	Window 9 horizontal end [7:0]

Byte 2

Bit	Mode	Function
7:0	W	Window 9 vertical end [7:0]

Window 9 control**Address: 127h**

Byte 0

Bit	Mode	Function
7	W	Window 9 shadow color index in 64-color LUT [5]
6	W	Window 9 border color index in 64-color LUT [5]
5	W	Window 9 color index in 64-color LUT [5]
4	W	Saturated color mode for gradient (refer to ADDR 162 for saturated color setting) 0: disable 1: enable
3	W	Reversed color mode for gradient (valid while [4] is 1) 0: disable 1: enable
2:0	--	Reserved

Byte 1



REALTEK

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Bit	Mode	Function
7:5	W	111: 7 level per gradient 110: 6 level per gradient 101: 5 level per gradient 100: 4 level per gradient 011: 3 level per gradient 010: 2 level per gradient 001: 1 level per gradient 000: 8 level per gradient
4:0	W	Window 9 color index in 64-color LUT [4:0]

Byte 2 default: 00h

Bit	Mode	Function
7	W	Blend function 0: Disable 1: Enable
6	W	Gradient function 0: Disable 1: Enable
5	W	Gradient direction 0: Horizontal 1: Vertical
4	W	Shadow/Border/3D button 0: Disable 1: Enable
3:1	W	Window 9 Type 000: Shadow Type 1 001: Shadow Type 2 010: Shadow Type3 011: Shadow Type 4 100: 3D Button Type 1 101: 3D Button Type 2 110: Reserved 111: Border
0	W	Window 9 Enable 0: Disable 1: Enable

Window 4-1 Shadow/Border/Chessboard



REALTEK

RTD2261W/2271W/2281W Series-GR

Address: 200h

Byte 0

Bit	Mode	Function
7	W	Window 4-1 shadow color index in 64-color LUT [4]
6	W	Window 4-1 border color index in 64-color LUT [4]
5:3	W	Window 4-1 shadow/border width or 3D button thickness in pixel unit 000~111: 1 ~ 8 pixel
2:0	W	Window 4-1 shadow/border height in line unit 000~111: 1 ~ 8 line It must be the same as bit [5:3] for 3D button thickness

Byte 1

Bit	Mode	Function
7:4	W	Window 4-1 shadow color index in 64-color LUT [3:0] For 3D window, it is the left-top/bottom border color
3:0	W	Window 4-1 border color index in 64-color LUT [3:0] For 3D window, it is the right-bottom/top border color

Byte 2

Bit	Mode	Function
7:0	W	Reserved

Window 4-1 start position**Address: 201h**

Byte 0

Bit	Mode	Function
7:4	W	Window 4-1 horizontal start [11:8]
3:0	W	Window 4-1 vertical start [11:8]

Byte 1

Bit	Mode	Function
7:0	W	Window 4-1 horizontal start [7:0]

Byte 2

Bit	Mode	Function
7:0	W	Window 4-1 vertical start [7:0]

**Window 4-1 end position****Address: 202h**

Byte 0

Bit	Mode	Function
7:4	W	Window 4-1 horizontal end [11:8]
3:0	W	Window 4-1 vertical end [11:8]

Byte 1

Bit	Mode	Function
7:0	W	Window 4-1 horizontal end [7:0]

Byte 2

Bit	Mode	Function
7:0	W	Window 4-1 vertical end [7:0]

**Window 4-1 control****Address: 203h**

Byte 0

Bit	Mode	Function
7	W	Window 4-1 shadow color index in 64-color LUT [5]
6	W	Window 4-1 border color index in 64-color LUT [5]
5	W	Window 4-1 color index in 64-color LUT [5]
4:0	--	Reserved

Byte 1

Bit	Mode	Function
7:5	--	Reserved
4:0	W	Window 4-1 color index in 64-color LUT [4:0]

Byte 2

default: 00h

Bit	Mode	Function
7	W	Blend function 0: Disable 1: Enable
6:5	W	Reserved
4	W	Shadow/Border/3D button 0: Disable 1: Enable
3:1	W	Window 4-1 Type 000: Shadow Type 1 001: Shadow Type 2 010: Shadow Type3 011: Shadow Type 4 100: 3D Button Type 1 101: 3D Button Type 2 110: Reserved 111: Border
0	W	Window 4-1 Enable 0: Disable 1: Enable



REALTEK

RTD2261W/2271W/2281W Series-GR

Window 4-2 Shadow/Border/Chessboard**Address: 204h**

Byte 0

Bit	Mode	Function
7	W	Window 4-2 shadow color index in 64-color LUT [4]
6	W	Window 4-2 border color index in 64-color LUT [4]
5:3	W	Window 4-2 shadow/border width or 3D button thickness in pixel unit 000~111: 1 ~ 8 pixel
2:0	W	Window 4-2 shadow/border height in line unit 000~111: 1 ~ 8 line It must be the same as bit [5:3] for 3D button thickness

Byte 1

Bit	Mode	Function
7:4	W	Window 4-2 shadow color index in 64-color LUT [3:0] For 3D window, it is the left-top/bottom border color
3:0	W	Window 4-2 border color index in 64-color LUT [3:0] For 3D window, it is the right-bottom/top border color

Byte 2

Bit	Mode	Function
7:0	W	Reserved

Window 4-2 start position**Address: 205h**

Byte 0

Bit	Mode	Function
7:4	W	Window 4-2 horizontal start [11:8]
3:0	W	Window 4-2 vertical start [11:8]

Byte 1

Bit	Mode	Function
7:0	W	Window 4-2 horizontal start [7:0]

Byte 2

Bit	Mode	Function
7:0	W	Window 4-2 vertical start [7:0]

**Window 4-2 end position****Address: 206h**

Byte 0

Bit	Mode	Function
7:4	W	Window 4-2 horizontal end [11:8]
3:0	W	Window 4-2 vertical end [11:8]

Byte 1

Bit	Mode	Function
7:0	W	Window 4-2 horizontal end [7:0]

Byte 2

Bit	Mode	Function
7:0	W	Window 4-2 vertical end [7:0]

**Window 4-2 control****Address: 207h**

Byte 0

Bit	Mode	Function
7	W	Window 4-2 shadow color index in 64-color LUT [5]
6	W	Window 4-2 border color index in 64-color LUT [5]
5	W	Window 4-2 color index in 64-color LUT [5]
4:0	--	Reserved

Byte 1

Bit	Mode	Function
7:5	--	Reserved
4:0	W	Window 4-2 color index in 64-color LUT [4:0]

Byte 2

default: 00h

Bit	Mode	Function
7	W	Blend function 0: Disable 1: Enable
6:5	W	Reserved
4	W	Shadow/Border/3D button 0: Disable 1: Enable
3:1	W	Window 4-2 Type 000: Shadow Type 1 001: Shadow Type 2 010: Shadow Type3 011: Shadow Type 4 100: 3D Button Type 1 101: 3D Button Type 2 110: Reserved 111: Border
0	W	Window 4-2 Enable 0: Disable 1: Enable



REALTEK

RTD2261W/2271W/2281W Series-GR

Window 4-3 Shadow/Border/Chessboard**Address: 208h**

Byte 0

Bit	Mode	Function
7	W	Window 4-3 shadow color index in 64-color LUT [4]
6	W	Window 4-3 border color index in 64-color LUT [4]
5:3	W	Window 4-3 shadow/border width or 3D button thickness in pixel unit 000~111: 1 ~ 8 pixel
2:0	W	Window 4-3 shadow/border height in line unit 000~111: 1 ~ 8 line It must be the same as bit [5:3] for 3D button thickness

Byte 1

Bit	Mode	Function
7:4	W	Window 4-3 shadow color index in 64-color LUT [3:0] For 3D window, it is the left-top/bottom border color
3:0	W	Window 4-3 border color index in 64-color LUT [3:0] For 3D window, it is the right-bottom/top border color

Byte 2

Bit	Mode	Function
7:0	W	Reserved

Window 4-3 start position**Address: 209h**

Byte 0

Bit	Mode	Function
7:4	W	Window 4-3 horizontal start [11:8]
3:0	W	Window 4-3 vertical start [11:8]

Byte 1

Bit	Mode	Function
7:0	W	Window 4-3 horizontal start [7:0]

Byte 2

Bit	Mode	Function
7:0	W	Window 4-3 vertical start [7:0]

**Window 4-3 end position****Address: 20Ah**

Byte 0

Bit	Mode	Function
7:4	W	Window 4-3 horizontal end [11:8]
3:0	W	Window 4-3 vertical end [11:8]

Byte 1

Bit	Mode	Function
7:0	W	Window 4-3 horizontal end [7:0]

Byte 2

Bit	Mode	Function
7:0	W	Window 4-3 vertical end [7:0]



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RTD2261W/2271W/2281W Series-GR

Window 4-3 control**Address: 20Bh**

Byte 0

Bit	Mode	Function
7	W	Window 4-3 shadow color index in 64-color LUT [5]
6	W	Window 4-3 border color index in 64-color LUT [5]
5	W	Window 4-3 color index in 64-color LUT [5]
4:0	--	Reserved

Byte 1

Bit	Mode	Function
7:5	--	Reserved
4:0	W	Window 4-3 color index in 64-color LUT [4:0]

Byte 2

default: 00h

Bit	Mode	Function
7	W	Blend function 0: Disable 1: Enable
6:5	W	Reserved
4	W	Shadow/Border/3D button 0: Disable 1: Enable
3:1	W	Window 4-3 Type 000: Shadow Type 1 001: Shadow Type 2 010: Shadow Type3 011: Shadow Type 4 100: 3D Button Type 1 101: 3D Button Type 2 110: Reserved 111: Border
0	W	Window 4-3 Enable 0: Disable 1: Enable



REALTEK

RTD2261W/2271W/2281W Series-GR

Window 4-4 Shadow/Border/Chessboard**Address: 20Ch**

Byte 0

Bit	Mode	Function
7	W	Window 4-4 shadow color index in 64-color LUT [4]
6	W	Window 4-4 border color index in 64-color LUT [4]
5:3	W	Window 4-4 shadow/border width or 3D button thickness in pixel unit 000~111: 1 ~ 8 pixel
2:0	W	Window 4-4 shadow/border height in line unit 000~111: 1 ~ 8 line It must be the same as bit [5:3] for 3D button thickness

Byte 1

Bit	Mode	Function
7:4	W	Window 4-4 shadow color index in 64-color LUT [3:0] For 3D window, it is the left-top/bottom border color
3:0	W	Window 4-4 border color index in 64-color LUT [3:0] For 3D window, it is the right-bottom/top border color

Byte 2

Bit	Mode	Function
7:0	W	Reserved

Window 4-4 start position**Address: 20Dh**

Byte 0

Bit	Mode	Function
7:4	W	Window 4-4 horizontal start [11:8]
3:0	W	Window 4-4 vertical start [11:8]

Byte 1

Bit	Mode	Function
7:0	W	Window 4-4 horizontal start [7:0]

Byte 2

Bit	Mode	Function
7:0	W	Window 4-4 vertical start [7:0]

**Window 4-4 end position****Address: 20Eh**

Byte 0

Bit	Mode	Function
7:4	W	Window 4-4 horizontal end [11:8]
3:0	W	Window 4-4 vertical end [11:8]

Byte 1

Bit	Mode	Function
7:0	W	Window 4-4 horizontal end [7:0]

Byte 2

Bit	Mode	Function
7:0	W	Window 4-4 vertical end [7:0]

**Window 4-4 control****Address: 20Fh**

Byte 0

Bit	Mode	Function
7	W	Window 4-4 shadow color index in 64-color LUT [5]
6	W	Window 4-4 border color index in 64-color LUT [5]
5	W	Window 4-4 color index in 64-color LUT [5]
4:0	--	Reserved

Byte 1

Bit	Mode	Function
7:5	--	Reserved
4:0	W	Window 4-4 color index in 64-color LUT [4:0]

Byte 2

default: 00h

Bit	Mode	Function
7	W	Blend function 0: Disable 1: Enable
6:5	W	Reserved
4	W	Shadow/Border/3D button 0: Disable 1: Enable
3:1	W	Window 4-4 Type 000: Shadow Type 1 001: Shadow Type 2 010: Shadow Type3 011: Shadow Type 4 100: 3D Button Type 1 101: 3D Button Type 2 110: Reserved 111: Border
0	W	Window 4-4 Enable 0: Disable 1: Enable



REALTEK

RTD2261W/2271W/2281W Series-GR

Window 4-5 Shadow/Border/Chessboard**Address: 210h**

Byte 0

Bit	Mode	Function
7	W	Window 4-5 shadow color index in 64-color LUT [4]
6	W	Window 4-5 border color index in 64-color LUT [4]
5:3	W	Window 4-5 shadow/border width or 3D button thickness in pixel unit 000~111: 1 ~ 8 pixel
2:0	W	Window 4-5 shadow/border height in line unit 000~111: 1 ~ 8 line It must be the same as bit [5:3] for 3D button thickness

Byte 1

Bit	Mode	Function
7:4	W	Window 4-5 shadow color index in 64-color LUT [3:0] For 3D window, it is the left-top/bottom border color
3:0	W	Window 4-5 border color index in 64-color LUT [3:0] For 3D window, it is the right-bottom/top border color

Byte 2

Bit	Mode	Function
7:0	W	Reserved

Window 4-5 start position**Address: 211h**

Byte 0

Bit	Mode	Function
7:4	W	Window 4-5 horizontal start [11:8]
3:0	W	Window 4-5 vertical start [11:8]

Byte 1

Bit	Mode	Function
7:0	W	Window 4-5 horizontal start [7:0]

Byte 2

Bit	Mode	Function
7:0	W	Window 4-5 vertical start [7:0]

**Window 4-5 end position****Address: 212h**

Byte 0

Bit	Mode	Function
7:4	W	Window 4-5 horizontal end [11:8]
3:0	W	Window 4-5 vertical end [11:8]

Byte 1

Bit	Mode	Function
7:0	W	Window 4-5 horizontal end [7:0]

Byte 2

Bit	Mode	Function
7:0	W	Window 4-5 vertical end [7:0]

**Window 4-5 control****Address: 213h**

Byte 0

Bit	Mode	Function
7	W	Window 4-5 shadow color index in 64-color LUT [5]
6	W	Window 4-5 border color index in 64-color LUT [5]
5	W	Window 4-5 color index in 64-color LUT [5]
4:0	--	Reserved

Byte 1

Bit	Mode	Function
7:5	--	Reserved
4:0	W	Window 4-5 color index in 64-color LUT [4:0]

Byte 2

default: 00h

Bit	Mode	Function
7	W	Blend function 0: Disable 1: Enable
6:5	W	Reserved
4	W	Shadow/Border/3D button 0: Disable 1: Enable
3:1	W	Window 4-5 Type 000: Shadow Type 1 001: Shadow Type 2 010: Shadow Type3 011: Shadow Type 4 100: 3D Button Type 1 101: 3D Button Type 2 110: Reserved 111: Border
0	W	Window 4-5 Enable 0: Disable 1: Enable



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RTD2261W/2271W/2281W Series-GR

Window 4-6 Shadow/Border/Chessboard**Address: 214h**

Byte 0

Bit	Mode	Function
7	W	Window 4-6 shadow color index in 64-color LUT [4]
6	W	Window 4-6 border color index in 64-color LUT [4]
5:3	W	Window 4-6 shadow/border width or 3D button thickness in pixel unit 000~111: 1 ~ 8 pixel
2:0	W	Window 1 shadow/border height in line unit 000~111: 1 ~ 8 line It must be the same as bit [5:3] for 3D button thickness

Byte 1

Bit	Mode	Function
7:4	W	Window 4-6 shadow color index in 64-color LUT [3:0] For 3D window, it is the left-top/bottom border color
3:0	W	Window 4-6 border color index in 64-color LUT [3:0] For 3D window, it is the right-bottom/top border color

Byte 2

Bit	Mode	Function
7:0	W	Reserved

Window 4-6 start position**Address: 215h**

Byte 0

Bit	Mode	Function
7:4	W	Window 4-6 horizontal start [11:8]
3:0	W	Window 4-6 vertical start [11:8]

Byte 1

Bit	Mode	Function
7:0	W	Window 4-6 horizontal start [7:0]

Byte 2

Bit	Mode	Function
7:0	W	Window 4-6 vertical start [7:0]

**Window 4-6 end position****Address: 216h**

Byte 0

Bit	Mode	Function
7:4	W	Window 4-6 horizontal end [11:8]
3:0	W	Window 4-6 vertical end [11:8]

Byte 1

Bit	Mode	Function
7:0	W	Window 4-6 horizontal end [7:0]

Byte 2

Bit	Mode	Function
7:0	W	Window 4-6 vertical end [7:0]

**Window 4-6 control****Address: 217h**

Byte 0

Bit	Mode	Function
7	W	Window 4-6 shadow color index in 64-color LUT [5]
6	W	Window 4-6 border color index in 64-color LUT [5]
5	W	Window 4-6 color index in 64-color LUT [5]
4:0	--	Reserved

Byte 1

Bit	Mode	Function
7:5	--	Reserved
4:0	W	Window 4-6 color index in 64-color LUT [4:0]

Byte 2

default: 00h

Bit	Mode	Function
7	W	Blend function 0: Disable 1: Enable
6:5	W	Reserved
4	W	Shadow/Border/3D button 0: Disable 1: Enable
3:1	W	Window 4-6 Type 000: Shadow Type 1 001: Shadow Type 2 010: Shadow Type3 011: Shadow Type 4 100: 3D Button Type 1 101: 3D Button Type 2 110: Reserved 111: Border
0	W	Window 4-6 Enable 0: Disable 1: Enable



REALTEK

RTD2261W/2271W/2281W Series-GR

Window 4-7 Shadow/Border/Chessboard**Address: 218h**

Byte 0

Bit	Mode	Function
7	W	Window 4-7 shadow color index in 64-color LUT [4]
6	W	Window 4-7 border color index in 64-color LUT [4]
5:3	W	Window 4-7 shadow/border width or 3D button thickness in pixel unit 000~111: 1 ~ 8 pixel
2:0	W	Window 4-7 shadow/border height in line unit 000~111: 1 ~ 8 line It must be the same as bit [5:3] for 3D button thickness

Byte 1

Bit	Mode	Function
7:4	W	Window 4-7 shadow color index in 64-color LUT [3:0] For 3D window, it is the left-top/bottom border color
3:0	W	Window 4-7 border color index in 64-color LUT [3:0] For 3D window, it is the right-bottom/top border color

Byte 2

Bit	Mode	Function
7:0	W	Reserved

Window 4-7 start position**Address: 219h**

Byte 0

Bit	Mode	Function
7:4	W	Window 4-7 horizontal start [11:8]
3:0	W	Window 4-7 vertical start [11:8]

Byte 1

Bit	Mode	Function
7:0	W	Window 4-7 horizontal start [7:0]

Byte 2

Bit	Mode	Function
7:0	W	Window 4-7 vertical start [7:0]

**Window 4-7 end position****Address: 21Ah**

Byte 0

Bit	Mode	Function
7:4	W	Window 4-7 horizontal end [11:8]
3:0	W	Window 4-7 vertical end [11:8]

Byte 1

Bit	Mode	Function
7:0	W	Window 4-7 horizontal end [7:0]

Byte 2

Bit	Mode	Function
7:0	W	Window 4-7 vertical end [7:0]

**Window 4-7 control****Address: 21Bh**

Byte 0

Bit	Mode	Function
7	W	Window 4-7 shadow color index in 64-color LUT [5]
6	W	Window 4-7 border color index in 64-color LUT [5]
5	W	Window 4-7 color index in 64-color LUT [5]
4:0	--	Reserved

Byte 1

Bit	Mode	Function
7:5	--	Reserved
4:0	W	Window 4-7 color index in 64-color LUT [4:0]

Byte 2

default: 00h

Bit	Mode	Function
7	W	Blend function 0: Disable 1: Enable
6:5	W	Reserved
4	W	Shadow/Border/3D button 0: Disable 1: Enable
3:1	W	Window 4-7 Type 000: Shadow Type 1 001: Shadow Type 2 010: Shadow Type3 011: Shadow Type 4 100: 3D Button Type 1 101: 3D Button Type 2 110: Reserved 111: Border
0	W	Window 4-7 Enable 0: Disable 1: Enable



REALTEK

RTD2261W/2271W/2281W Series-GR

Window 4-8 Shadow/Border/Chessboard**Address: 21Ch**

Byte 0

Bit	Mode	Function
7	W	Window 4-8 shadow color index in 64-color LUT [4]
6	W	Window 4-8 border color index in 64-color LUT [4]
5:3	W	Window 4-8 shadow/border width or 3D button thickness in pixel unit 000~111: 1 ~ 8 pixel
2:0	W	Window 4-8 shadow/border height in line unit 000~111: 1 ~ 8 line It must be the same as bit [5:3] for 3D button thickness

Byte 1

Bit	Mode	Function
7:4	W	Window 4-8 shadow color index in 64-color LUT [3:0] For 3D window, it is the left-top/bottom border color
3:0	W	Window 4-8 border color index in 64-color LUT [3:0] For 3D window, it is the right-bottom/top border color

Byte 2

Bit	Mode	Function
7:0	W	Reserved

Window 4-8 start position**Address: 21Dh**

Byte 0

Bit	Mode	Function
7:4	W	Window 4-8 horizontal start [11:8]
3:0	W	Window 4-8 vertical start [11:8]

Byte 1

Bit	Mode	Function
7:0	W	Window 4-8 horizontal start [7:0]

Byte 2

Bit	Mode	Function
7:0	W	Window 4-8 vertical start [7:0]

**Window 4-8 end position****Address: 21Eh**

Byte 0

Bit	Mode	Function
7:4	W	Window 4-8 horizontal end [11:8]
3:0	W	Window 4-8 vertical end [11:8]

Byte 1

Bit	Mode	Function
7:0	W	Window 4-8 horizontal end [7:0]

Byte 2

Bit	Mode	Function
7:0	W	Window 4-8 vertical end [7:0]

**Window 4-8 control****Address: 21Fh**

Byte 0

Bit	Mode	Function
7	W	Window 4-8 shadow color index in 64-color LUT [5]
6	W	Window 4-8 border color index in 64-color LUT [5]
5	W	Window 4-8 color index in 64-color LUT [5]
4:0	--	Reserved

Byte 1

Bit	Mode	Function
7:5	--	Reserved
4:0	W	Window 4-8 color index in 64-color LUT [4:0]

Byte 2

default: 00h

Bit	Mode	Function
7	W	Blend function 0: Disable 1: Enable
6:5	W	Reserved
4	W	Shadow/Border/3D button 0: Disable 1: Enable
3:1	W	Window 4-8 Type 000: Shadow Type 1 001: Shadow Type 2 010: Shadow Type3 011: Shadow Type 4 100: 3D Button Type 1 101: 3D Button Type 2 110: Reserved 111: Border
0	W	Window 4-8 Enable 0: Disable 1: Enable



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RTD2261W/2271W/2281W Series-GR

Window Special Control

Window 0

Address: 150h

Byte 0

Bit	Mode	Function
7:0	W	Window 0 RED saturated color [7:0]

Byte 1

Bit	Mode	Function
7:0	W	Window 0 GRN saturated color [7:0]

Byte 2

Bit	Mode	Function
7:0	W	Window 0 BLU saturated color [7:0]

Address: 151h

Byte 0

Bit	Mode	Function
7:0	W	Reserved

Byte 1

Bit	Mode	Function
7:0	W	Reserved

Byte 2

Bit	Mode	Function
7:0	W	Reserved

Window 1

Address: 152h

Byte 0

Bit	Mode	Function
7:0	W	Reserved

Byte 1

Bit	Mode	Function
7:0	W	Reserved

Byte 2

Bit	Mode	Function
7:0	W	Reserved



REALTEK

RTD2261W/2271W/2281W Series-GR

Address: 153h

Byte 0

Bit	Mode	Function
7:0	W	Reserved

Byte 1

Bit	Mode	Function
7:0	W	Reserved

Byte 2

Bit	Mode	Function
7:0	W	Reserved

Window 2

Address: 154h

Byte 0

Bit	Mode	Function
7:0	W	Reserved

Byte 1

Bit	Mode	Function
7:0	W	Reserved

Byte 2

Bit	Mode	Function
7:0	W	Reserved

Address: 155h

Byte 0

Bit	Mode	Function
7:0	W	Reserved

Byte 1

Bit	Mode	Function
7:0	W	Reserved

Byte 2

Bit	Mode	Function
7:0	W	Reserved

Window 3

Address: 156h



REALTEK

RTD2261W/2271W/2281W Series-GR

Byte 0

Bit	Mode	Function
7:0	W	Reserved

Byte 1

Bit	Mode	Function
7:0	W	Reserved

Byte 2

Bit	Mode	Function
7:0	W	Reserved

Address: 157h

Byte 0

Bit	Mode	Function
7:0	W	Reserved

Byte 1

Bit	Mode	Function
7:0	W	Reserved

Byte 2

Bit	Mode	Function
7:0	W	Reserved

Window 4**Address: 158h**

Byte 0

Bit	Mode	Function
7:0	W	Reserved

Byte 1

Bit	Mode	Function
7:0	W	Reserved

Byte 2

Bit	Mode	Function
7:0	W	Reserved

Address: 159h

Byte 0

Bit	Mode	Function
7:0	W	Reserved



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RTD2261W/2271W/2281W Series-GR

Byte 1

Bit	Mode	Function
7:0	W	Reserved

Byte 2

Bit	Mode	Function
7:0	W	Reserved

Window 5

Address: 15Ah

Byte 0

Bit	Mode	Function
7:0	W	Window 5 RED saturated color [7:0]

Byte 1

Bit	Mode	Function
7:0	W	Window 5 GRN saturated color [7:0]

Byte 2

Bit	Mode	Function
7:0	W	Window 5 BLU saturated color [7:0]

Address: 15Bh

Byte 0

Bit	Mode	Function
7:0	W	Reserved

Byte 1

Bit	Mode	Function
7:0	W	Reserved

Byte 2

Bit	Mode	Function
7:0	W	Reserved

Window 6

Address: 15Ch

Byte 0

Bit	Mode	Function
7:0	W	Window 6 RED saturated color [7:0]

Byte 1

Bit	Mode	Function
7:0	W	Reserved



REALTEK

RTD2261W/2271W/2281W Series-GR

7:0	W	Window 6 GRN saturated color [7:0]
-----	---	------------------------------------

Byte 2

Bit	Mode	Function
7:0	W	Window 6 BLU saturated color [7:0]

Address: 15Dh

Byte 0

Bit	Mode	Function
7:0	W	Reserved

Byte 1

Bit	Mode	Function
7:0	W	Reserved

Byte 2

Bit	Mode	Function
7:0	W	Reserved

Window 7**Address: 15Eh**

Byte 0

Bit	Mode	Function
7:0	W	Window 7 RED saturated color [7:0]

Byte 1

Bit	Mode	Function
7:0	W	Window 7 GRN saturated color [7:0]

Byte 2

Bit	Mode	Function
7:0	W	Window 7 BLU saturated color [7:0]

Address: 15Fh

Byte 0

Bit	Mode	Function
7:0	W	Reserved

Byte 1

Bit	Mode	Function
7:0	W	Reserved

Byte 2

Bit	Mode	Function
7:0	W	Reserved



REALTEK

RTD2261W/2271W/2281W Series-GR

7:0	W	Reserved
-----	---	----------

Window 8

Address: 160h

Byte 0

Bit	Mode	Function
7:0	W	Window 8 RED saturated color [7:0]

Byte 1

Bit	Mode	Function
7:0	W	Window8 GRN saturated color [7:0]

Byte 2

Bit	Mode	Function
7:0	W	Window 8 BLU saturated color [7:0]

Address: 161h

Byte 0 default: 0xxx_xxxx

Bit	Mode	Function
7	R/W	Window8 Chessboard color function: 0:disable (default) 1:enable
6:0	--	Reserved

Byte 1

Bit	Mode	Function
7:6	--	Reserved
5:0	R/W	Window8 Chessboard color1

Byte 2

Bit	Mode	Function
7:6	--	Reserved
5:0	R/W	Window8 Chessboard color2

Window 9

Address: 162h

Byte 0



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RTD2261W/2271W/2281W Series-GR

Bit	Mode	Function
7:0	W	Window 9 RED saturated color [7:0]

Byte 1

Bit	Mode	Function
7:0	W	Window 9 GRN saturated color [7:0]

Byte 2

Bit	Mode	Function
7:0	W	Window 9 BLU saturated color [7:0]

Address: 163h

Byte 0

Bit	Mode	Function
7	W	Chessboard color function: 0:disable 1:enable
6:0	--	Reserved

Byte 1

Bit	Mode	Function
7:6	--	Reserved
5:0	W	Chessboard color1

Byte 2

Bit	Mode	Function
7:6	--	Reserved
5:0	W	Chessboard color2

Window Special Control**Window 4-1****Address: 164h**

Byte 0

Bit	Mode	Function
7	W	Window 4-1 Chessboard color function: 0:disable 1:enable (Reserved)
6:0	--	Reserved



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RTD2261W/2271W/2281W Series-GR

Byte 1

Bit	Mode	Function
7:6	--	Reserved
5:0	W	Chessboard color1 (Reserved)

Byte 2

Bit	Mode	Function
7:6	--	Reserved
5:0	W	Chessboard color2 (Reserved)

Window 4-2

Address: 166h

Byte 0

Bit	Mode	Function
7	W	Window 4-2 Chessboard color function: 0:disable 1:enable (Reserved)
6:0	--	Reserved

Byte 1

Bit	Mode	Function
7:6	--	Reserved
5:0	W	Chessboard color1 (Reserved)

Byte 2

Bit	Mode	Function
7:6	--	Reserved
5:0	W	Chessboard color2 (Reserved)

Window 4-3

Address: 168h

Byte 0



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RTD2261W/2271W/2281W Series-GR

Bit	Mode	Function
7	W	Window 4-3 Chessboard color function: 0:disable 1:enable
6:0	--	Reserved

Byte 1

Bit	Mode	Function
7:6	--	Reserved
5:0	W	Chessboard color1

Byte 2

Bit	Mode	Function
7:6	--	Reserved
5:0	W	Chessboard color2

Window 4-4

Address: 16Ah

Byte 0

Bit	Mode	Function
7	W	Window 4-4 Chessboard color function: 0:disable 1:enable
6:0	--	Reserved

Byte 1

Bit	Mode	Function
7:6	--	Reserved
5:0	W	Chessboard color1

Byte 2

Bit	Mode	Function
7:6	--	Reserved
5:0	W	Chessboard color2

Window 4-5

Address: 16Ch



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RTD2261W/2271W/2281W Series-GR

Byte 0

Bit	Mode	Function
7	W	Window 4-5 Chessboard color function: 0:disable 1:enable
6:0	--	Reserved

Byte 1

Bit	Mode	Function
7:6	--	Reserved
5:0	W	Chessboard color1

Byte 2

Bit	Mode	Function
7:6	--	Reserved
5:0	W	Chessboard color2

Window 4-6

Address: 16Eh

Byte 0

Bit	Mode	Function
7	W	Window 4-6 Chessboard color function: 0:disable 1:enable
6:0	--	Reserved

Byte 1

Bit	Mode	Function
7:6	--	Reserved
5:0	W	Chessboard color1

Byte 2

Bit	Mode	Function
7:6	--	Reserved
5:0	W	Chessboard color2

Window 4-7



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RTD2261W/2271W/2281W Series-GR

Address: 170h

Byte 0

Bit	Mode	Function
7	W	Window 4-7 Chessboard color function: 0:disable 1:enable
6:0	--	Reserved

Byte 1

Bit	Mode	Function
7:6	--	Reserved
5:0	W	Chessboard color1

Byte 2

Bit	Mode	Function
7:6	--	Reserved
5:0	W	Chessboard color2

Window 4-8

Address: 172h

Byte 0

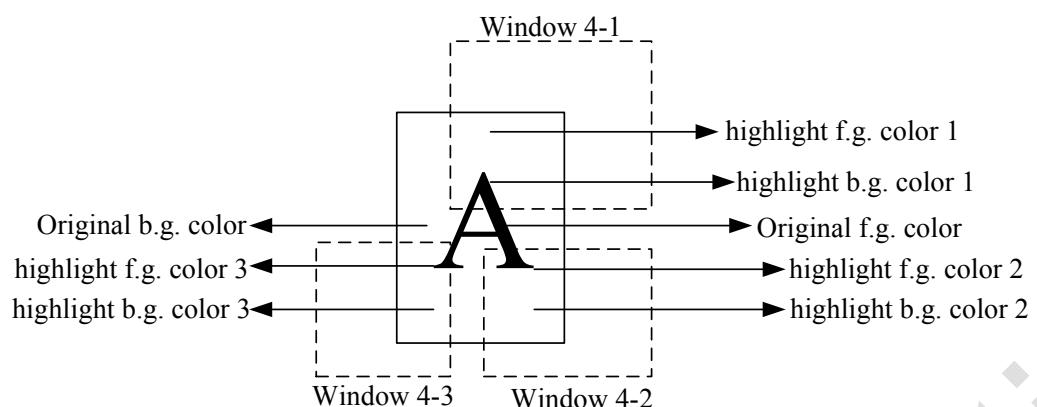
Bit	Mode	Function
7	W	Window 4-8 Chessboard color function: 0:disable 1:enable
6:0	--	Reserved

Byte 1

Bit	Mode	Function
7:6	--	Reserved
5:0	W	Chessboard color1

Byte 2

Bit	Mode	Function
7:6	--	Reserved
5:0	W	Chessboard color2



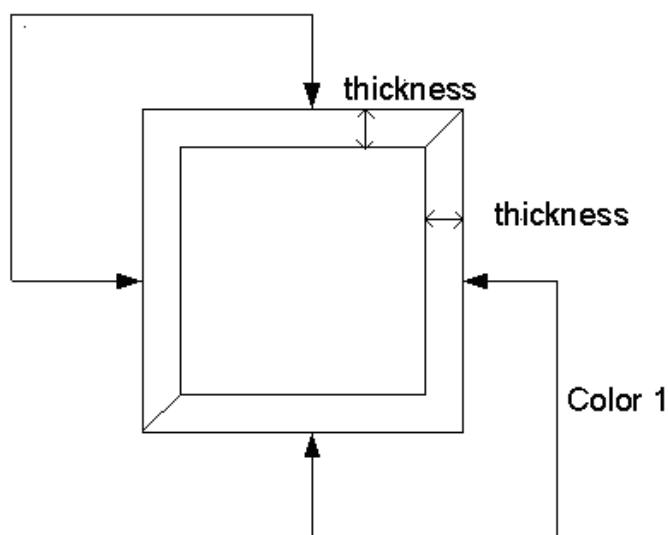
Highlight function of window4-1, window4-2 and window4-3



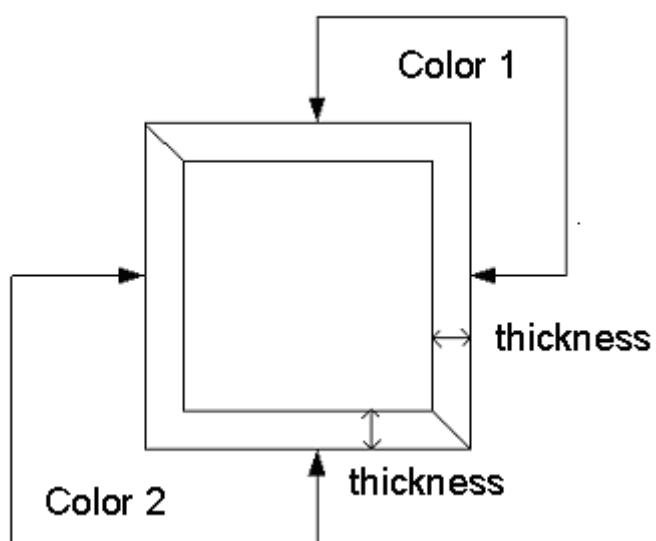
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RTD2261W/2271W/2281W Series-GR

Color 2



3D Button Type 1

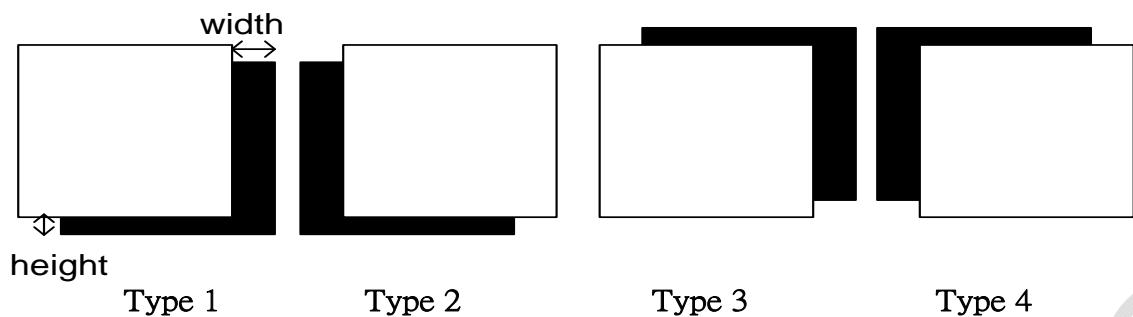


3D Button Type 2

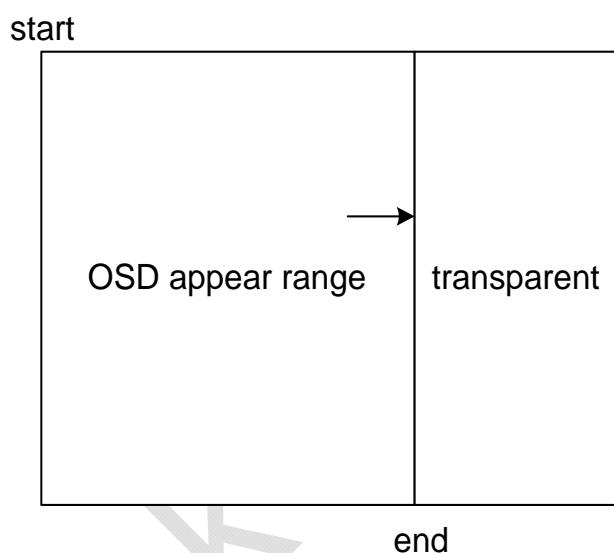


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RTD2261W/2271W/2281W Series-GR



Shadow in all direction



Window mask fade/in out function

***Frame control registers*****Address: 000h**

Byte 0

Bit	Mode	Function
7:0	R/W	Vertical Delay [10:3] The bits define the vertical starting address. Total 2048 step unit: 1 line

Vertical delay minimum should set 1

Byte 1

Bit	Mode	Function
7:0	R/W	Horizontal Delay [9:2] The bits define the horizontal starting address. Total 1024 step unit: 4 pixels

Horizontal delay minimum should set 2

Byte 2

default: xxxx_xxx0b

Bit	Mode	Function
7:6	R/W	Horizontal Delay bit [1:0]
5:3	R/W	Vertical Delay [2:0]
2:1	R/W	Display zone, for smaller character width 00: middle 01: left 10: right 11: reserved
0	R/W	OSD enable 0: OSD circuit is inactivated 1: OSD circuit is activated

- When OSD is disabled, Double Width (address 0x003 Byte1[1]) must be disabled to save power.
- These three bytes have their own double-buffer.



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RTD2261W/2271W/2281W Series-GR

Address 001h ~ Address002h are reserved

Address: 002h

Byte 2

Default: 00h

Bit	Mode	Function
7	R/W	Reserved to 0
6	R/W	Window 9 priority 0: lower than font 1: higher than font
5	R/W	Window 8 priority 0: lower than font 1: higher than font
4	R/W	blending type 2 match color 0: match blending type 2 color bit[3:0] 1: match blending type 2 color bit[5:0]
3:2	R/W	Blending color from 64-color LUT [5:4] (blending type 2)
1:0	R/W	Char shadow/border color [5:4]

Address: 003h

Byte 0

Default: 00h

Bit	Mode	Function
7	R/W	Specific color blending (blending type 2) 0: Disable 1: Enable
6:5	R/W	Window 7special function 00: disable 01: blending (blending type 3) 10: window 7 mask region appear 11: window 7 mask region transparent
4	R/W	OSD vertical start input signal source select 0: Select DVS as OSD VSYNC input 1: Select ENA as OSD VSYNC input
3:0	R/W	Blending color from 64-color LUT [3:0] (blending type 2)

Byte 1

Default: 00h

Bit	Mode	Function
7:4	R/W	Char shadow/border color [3:0]
3: 2	R/W	Alpha blending type (blending type 1) 00: Disable alpha blending



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RTD2261W/2271W/2281W Series-GR

		01: Only window blending 10: All blending 11: Window and Character background blending
1	R/W	Double width enable (For all OSD including windows and characters) 0: Normal 1: Double
0	R/W	Double Height enable (For all OSD including windows and characters) 0: Normal 1: Double

Total blending area = blending type1 area + blending type 2 area + blending type 3 area

Byte 2

Default: 00h

Bit	Mode	Function
7:6	R/W	Font downloaded swap control 0x: No swap 10: CCW 11: CW
5	R	Buffer Empty 0: Empty 1: Not Empty
4	R	Buffer Valid 0: Done 1: Buffer is writing to SDRAM
3	R/W	Reset Buffer Write 1 to reset and auto-clear after finished.
2	R/W	Hardware Rotation Enable 0: Disable 1: Enable (Default) OSD compression function must be enabled simultaneously.
1	R/W	Global Blinking Enable 0: Disable 1: Enable
0	R/W	Rotation 0: Normal (data latch 24 bit per 24 bit) 1: Rotation (data latch 18 bit per 24 bit)

Bit	7	6	5	4	3	2	1	0



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RTD2261W/2271W/2281W Series-GR

Firmware	A	B	C	D	E	F	G	H
CW	A	E	B	F	C	G	D	H
CCW	E	A	F	B	G	C	H	D

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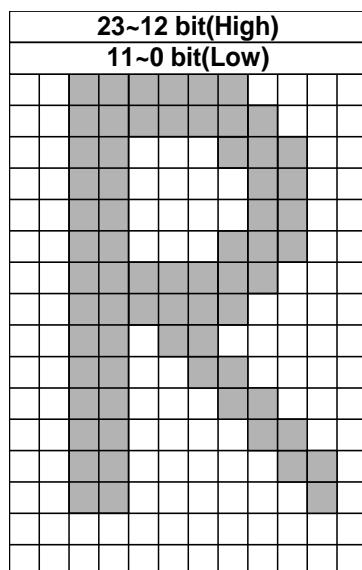


Figure 3 Non-rotated memory alignments

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6

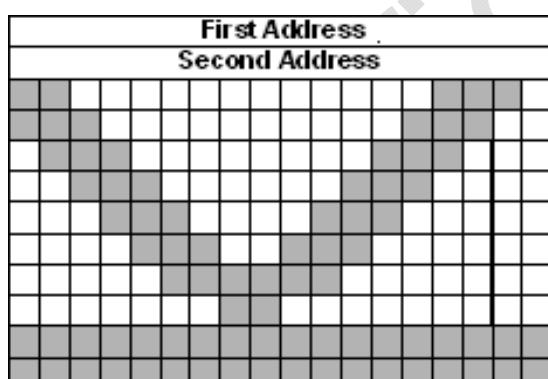


Figure 4 Rotated memory alignments

Base address offset

Address: 004h

Byte 0

Bit	Mode	Function
7:0	R/W	Font Select Base Address[7:0]

Byte 1

Bit	Mode	Function
7:4	R/W	Font Select Base Address[11:8]
3:0	R/W	Font Base Address[3:0]

Byte 2

Bit	Mode	Function
7:0	R/W	Font Base Address[11:4]

When OSD Special Function for POP-ON is enabled (OSD[008]), Font Select Base Address here will not be



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RTD2261W/2271W/2281W Series-GR

effective.

OSD Compression

Address: 005h

Byte 0

Bit	Mode	Function
7:4	R/W	4-bit value for VLC code 0
3:0	R/W	4-bit value for VLC code 100

Byte 1

Bit	Mode	Function
7:4	R/W	4-bit value for VLC code 1010
3:0	R/W	4-bit value for VLC code 1011

Byte 2

Bit	Mode	Function
7:4	R/W	4-bit value for VLC code 1100
3:0	R/W	4-bit value for VLC code 1101 0

Address: 006h

Byte 0

Bit	Mode	Function
7:4	R/W	4-bit value for VLC code 1101 1
3:0	R/W	4-bit value for VLC code 1110 0

Byte 1

Bit	Mode	Function
7:4	R/W	4-bit value for VLC code 1110 10
3:0	R/W	4-bit value for VLC code 1110 11

Byte 2

Bit	Mode	Function
7:4	R/W	4-bit value for VLC code 1111 00
3:0	R/W	4-bit value for VLC code 1111 01

Address: 007h

Byte 0

Bit	Mode	Function
7:4	R/W	4-bit value for VLC code 1111 100
3:0	R/W	4-bit value for VLC code 1111 101

Byte 1

Bit	Mode	Function
7:4	R/W	4-bit value for VLC code 1111 110



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RTD2261W/2271W/2281W Series-GR

7:4	R/W	4-bit value for VLC code 1111_110
3:0	R/W	4-bit value for VLC code 1111_1110

Byte 2

default: xxxx_x0000b

Bit	Mode	Function
7:3	--	reserved
2	R/W	Write 3-byte decoded-data into SRAM each time for acceleration 0: disable 1: enable active when compression and hardware rotation function are both enabled.
1	R/W	Decide to decode which kind of data 0: decode compressed data 1: decode non-compressed data
0	R/W	OSD compression (4bit/symbol, VLC code 1111_1111 represents the end of data) (only for SRAM) 0: disable 1: enable

Note:

1. If enable OSD compression or auto load (double buffer), only one byte can be read after writing address at 0x90, 0x91.
2. For OSD compression, MSB 4 bits of original byte is first transferred to corresponding VLC code, and then LSB 4 bits is transferred. VLC code is placed from LSB to MSB of compression font. For example, 4-bit value for VLC code 1100 is 4'b0101, and 4-bit value for VLC code 100 is 4'b0001. Original data 0x15 is transferred to compression x0011001.
3. OSD double buffer and compression can't be enabled simultaneous.
4. When power-down mode or lack of crystal clock, OSD compression font can't be write.
5. After OSD enable, it is better to delay 1 DVS to start writing OSD compression data.
6. While decoding non-compressed data, it is necessary to reset compression function while decode is done. Because this is the only way to reset compression circuit and ready for next decode job
7. ADDR007 Byte2 bit[2] is designed to accelerate the speed of writing compression/rotation data into SRAM. When the bit is enabled, 3-byte data will be written to SRAM for each cycle and it is supposed to be used while **compression** and **hardware rotation function** are both enabled. Besides, the result of the acceleration will have the best performance while the burst write mode is enabled at the same time. However the burst write setting should be constrained by the two conditions as following:
 - (1) Time of MCU write cycle > 18 x ($T_{m2pll/2}$)
 - (2) Time of MCU write cycle > ((4 x ($T_{m2pll/2}$) + 9 x T_{DCLK}) x 9) / 7



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OSD Special Function

Address: 008h

Byte 0

Default: 0x00

Bit	Mode	Function
7	R/W	OSD Special Function Enable 0: Disable 1: Enable
6	R/W	OSD Special Function Select (Effective only when Bit[7]=1) 0: ROLL-UP 1: POP-ON
5	R/W	OSD Vertical Boundary Function Enable 0: Disable 1: Enable
4	R/W	Reserved to 0
3	R/W	OSD 2 font function 0: disable (row & font select command refer to the FRAM ADDR 004) 1: enable (row command of font A refer to the ADDR 008 byte 1 row command of font B refer to the ADDR 008 byte 2 font select command of font A refer to the ADDR 009 FS0 font select command of font B refer to the ADDR 009 FS1)
2:1	R/W	Reserved to 0
0	R/W	Display Base Select (Effective only when Bit[7:6]=11'b) 0: Base 0 1: Base 1

Byte 1

Default: 0x00

Bit	Mode	Function
7:0	R/W	Row Command Base 0 [7:0]

Byte 2

Default: 0x00

Bit	Mode	Function
7:0	R/W	Row Command Base 1 [7:0]

Address: 009h

Byte 0

Default: 0x00

Bit	Mode	Function
7:4	R/W	Font Select Base 0 [11:8]
3:0	R/W	Font Select Base 1 [11:8]

Byte 1

Default: 0x00

Bit	Mode	Function



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7:0	R/W	Font Select Base 0 [7:0]
-----	-----	--------------------------

Byte 2 Default: 0x00

Bit	Mode	Function
7:0	R/W	Font Select Base 1 [7:0] (Not effective when ROLL-UP)

Address: 00Ah

Byte 0 Default: 0x00

Bit	Mode	Function
7	R/W	Reserved
6:4	R/W	OSD Vertical Upper Boundary [10:8]
3	R/W	Reserved
2:0	R/W	OSD Vertical Lower Boundary [10:8]

Byte 1 Default: 0x00

Bit	Mode	Function
7:0	R/W	OSD Vertical Upper Boundary [7:0]

Byte 2 Default: 0x00

Bit	Mode	Function
7:0	R/W	OSD Vertical Lower Boundary [7:0]

Address: 00Bh

Byte 0 Default: 0x00

Bit	Mode	Function
7	R/W	Font Base Address[12]
6	R/W	Window 6 Special Blending Function 0: OFF 1: ON
5:4	R/W	Blending Type of Window 7 00: NO Blending for both F/B 01: NO Blending for Foreground 10: NO Blending for Background 11: Both Blending for F/B
3:2	R/W	Blending Type of Window 6 00: NO Blending for both F/B 01: NO Blending for Foreground 10: NO Blending for Background 11: Both Blending for F/B
1:0	--	Reserved

Byte 1 Default: 0x00

Bit	Mode	Function
-----	------	----------



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7	R/W	2-bit font char select offset [7]
6:0	R/W	2-bit font char select offset [6:0]

Byte 2 Default: 0x00

Bit	Mode	Function
7:0	--	Reserved

Address: 00Ch

Byte 0 Default: 0x00

Bit	Mode	Function
7:4	R/W	FONT A horizontal delay [11:8]
3:0	R/W	FONT A vertical delay [11:8]

Byte 1 Default: 0x00

Bit	Mode	Function
7:0	R/W	FONT A horizontal delay [7:0]

Byte 2 Default: 0x00

Bit	Mode	Function
7:0	R/W	FONT A vertical delay [7:0]

Address: 00Dh

Byte 0 Default: 0x00

Bit	Mode	Function
7:4	R/W	FONT B horizontal delay [11:8] (valid only while 2 font function enabled)
3:0	R/W	FONT B vertical delay [11:8] (valid only while 2 font function enabled)

Byte 1 Default: 0x00

Bit	Mode	Function
7:0	R/W	FONT B horizontal delay [7:0] (valid only while 2 font function enabled)

Byte 2 Default: 0x00

Bit	Mode	Function
7:0	R/W	FONT B vertical delay [7:0] (valid only while 2 font function enabled)

Address: 00Eh

Byte 0 default: x0xx_xxxx

Bit	Mode	Function
7	--	Reserved
6	R/W	Highlight function for window4-1 0: Disable (default) 1: Enable
5:0	R/W	Foreground color1 for highlight



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Byte 1

Bit	Mode	Function
7	--	Reserved
6	--	Reserved
5:0	R/W	Background color1 for highlight

Note: Background color1[3:0]=4'b0000 is special for transparent

Byte 2

Bit	Mode	Function
7	--	Reserved
6	--	Reserved
5:0	R/W	Character border/shadow color1 for highlight

Address: 00Fh

Byte 0 default: x0xx_xxxx

Bit	Mode	Function
7	--	Reserved
6	R/W	Highlight function for window4-2 0: Disable (default) 1: Enable
5:0	R/W	Foreground color2 for highlight

Byte 1

Bit	Mode	Function
7	--	Reserved
6	--	Reserved
5:0	R/W	Background color2 for highlight

Note: Background color2[3:0]=4'b0000 is special for transparent

Byte 2

Bit	Mode	Function
7	--	Reserved
6	--	Reserved
5:0	R/W	Character border/shadow color2 for highlight

Address: 010h

Byte 0 default: x0xx_xxxx

Bit	Mode	Function
7	--	Reserved



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6	R/W	Highlight function for window4-3 0: Disable (default) 1: Enable
5:0	R/W	Foreground color3 for highlight

Byte 1

Bit	Mode	Function
7	--	Reserved
6	--	Reserved
5:0	R/W	Background color3 for highlight

Note: Background color3[3:0]=4'b0000 is special for transparent

Byte 2

Bit	Mode	Function
7	--	Reserved
6	--	Reserved
5:0	R/W	Character border/shadow color3 for highlight

Note: 1. This highlight function only supports 1-bit font & blank.

2. If highlight function on, the color of blank will become foreground color.
3. The priority of these three windows: window4-3 > window4-2 >window4-1. If these three windows are overlapped, the highlight color of foreground, background and character border/shadow would be only displayed the setting of window4-3.

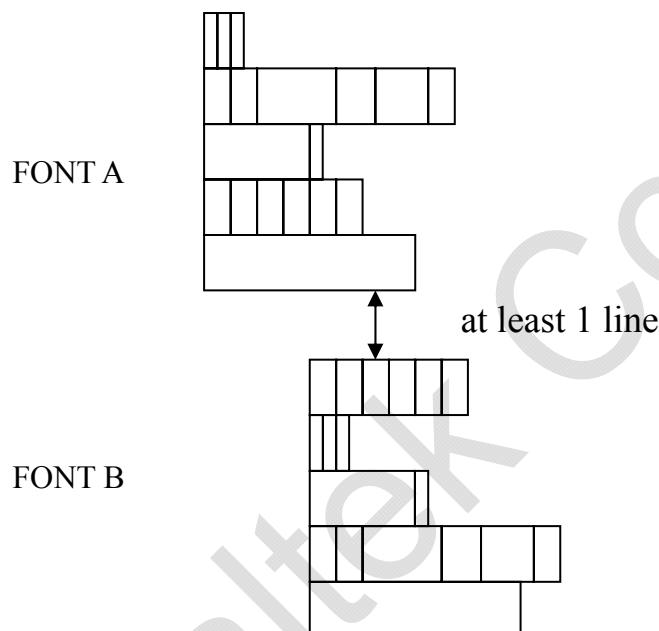
Note:

1. When OSD Special Function for POP-ON is enabled, Font Select Base Address in OSD[004] will not be effective anymore.
2. When OSD Vertical Boundary Function is enabled, OSD image above upper boundary and below lower boundary will be invisible.
3. When ROLL-UP function is enabled, OSD will always start from the row-command pointed by Base0, and after the row-command pointed by Base1 has been dealt with, the next row-command will be the first one in OSD SRAM. Row-command processing will terminate in the row-command before the one pointed by Base0. (For example, R1 is pointed by Base0, and R5 is pointed by Base1. OSD will show R1 as the first row, followed by R2, R3, R4, R5, and R0 as last row.)
4. When POP-ON function is enabled, OSD will start from the row command pointed by the base selected as display base(selected by OSD[008][0.0]), and terminate when end-command is encountered. That is, all row-command will be separated into two non-overlay subset which is enclosed by the row-command pointed by base and end-command.
5. While 2 font function is enabled (selected by OSD [008][0.3]), FONT A & FONT B can't be overlapped

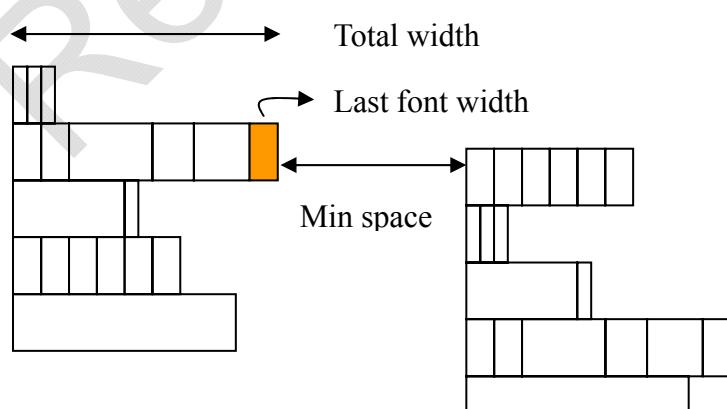


6. While 2 font function is enabled (selected by OSD [008][0.3]), for vertical case, lines between of FONT A & FONTB must be larger than 1
7. While 2 font function is enabled (selected by OSD [008][0.3]), for horizontal case, pixels between of FONT A & FONT B must follow the rules as following:

Vertical case



horizontal case





Min space = 13

OSD SRAM (Map and font registers)

R0	R1	R2	Rn	End											
C01	C02	B03	C04	...	C11	C12										
...																
...																
...	Cn1	Cn2	...	1-bit font start		...										
...																
...	2-bit font start		...													
...																
4-bit font start	...															
...																
...																

16.5k bytes SRAM

1. Row Command

R0	R1	R2	R3	R....	Rn	End
----	----	----	----	-------	----	-----

Row Command R0~Rn represent the start of new row. Each command contains 3 bytes data which define the length of a row and other attributes. OSD End Command represent the end of OSD. R0 is set in address 0 of SRAM.

2. Character/Blank Command (Font Select)

Character Command is used to select which character font is show. Each command contains three bytes which specify its attribute and 1,2 or 4bit per pixel. Blank Command represents blank pixel to separate the preceding character and following character. Use two or more Blank Command if the character distance exceeds 255 pixel.

The Font Select Base Address in Frame Control Register represents the address of the first character in Row 0, that is, C01 in the above figure. The following character/blank is write in the next address. C11 represents the first character in Row1, C12 represents the second character in Row1, and so on.

The address of the first character Cn1 in Row n = Font Select Base Address + Row 0 font base length + Row 1 font base length + ...+Row n-1 font base length.

3. Font

User fonts are stored as bit map data. For normal font, one font has 12x18 pixel, and for rotation font, one has 18x12 pixel. One pixel use 1, 2 or 4 bits.

For 12x18 font,

One 1-bit font requires $9 * 24$ bit SRAM

One 2-bit font requires $18 * 24$ bit SRAM

One 4-bit font requires $36 * 24$ bit SRAM

For 18x12 font,

One 1-bit font requires $9 * 24$ bit SRAM

One 2-bit font requires $18 * 24$ bit SRAM

One 4-bit font requires $36 * 24$ bit SRAM

Font Base Address in Frame Control Register point to the start of 1-bit font.

For normal (12x18) font:

1-bit Font, if CS = 128, Real Address of Font = Font Base Address + $9 * 128$

2-bit Font, if CS = 128, Real Address of Font = Font Base Address + $18 * 128$

4-bit Font, if CS = 128, Real Address of Font = Font Base Address + $36 * 128$

For rotational (18x12) font:

1-bit Font, if CS = 128, Real Address of Font = Font Base Address + $9 * 128$

2-bit Font, if CS = 128, Real Address of Font = Font Base Address + $18 * 128$

4-bit Font, if CS = 128, Real Address of Font = Font Base Address + $36 * 128$

where CS is Character Selector in Character Command.

Note that Row Command, Font Select and Font share the same OSD SRAM.

When we download the font, we have to set the Frame control 003h byte2 [7:6]

] to set the method of hardware bit swap. If the OSD is Counter-Clock-Wise rotated, we have to set to 0x01 (the 8 bits of every byte of font SRAM downloaded by firmware will be in a sequence of “7 5 3 1 6 4 2 0” (from MSB to LSB) and should be rearranged to “7 6 5 4 3 2 1 0” by hardware). If it is Clock-Wise rotated, we have to set to 0x10 (the 8 bits of every byte of font SRAM downloaded by firmware will be in a sequence of “6 4 2 0 7 5 3 1” (from MSB to LSB) and should be rearranged to “7 6 5 4 3 2 1 0” by hardware). After we finish the downloading or if we don’t have to rotate the OSD, we have to set it to 0x00.

**Row Command**

Byte 0

Bit	Mode	Function
7	W	1: Row Start Command 0: OSD End Command Each row must start with row-command, last word of OSD map must be end-command
6	R/W	VBI OSD function enable (not valid while rotation enabled) 0: normal OSD function as usual 1: support VBI OSD functions like underline, B/F separated blink and 512 fonts select
5	W	1-bit font selection 0: font select from 0-511 1: font select from 512-1023
4:2	W	Character border/shadow 000: None 001: Border 100: Shadow (left-top) 101: Shadow (left-bottom) 110: Shadow (right-top) 111: Shadow (right-bottom)
1	W	Double character width 0: x1 1: x2
0	W	Double character height 0: x1 1: x2

Byte 1

Bit	Mode	Function
7:3	W	Row height (1~32)
2:0	W	Column space 0~7 pixel column space When Char is doubled, so is column space.

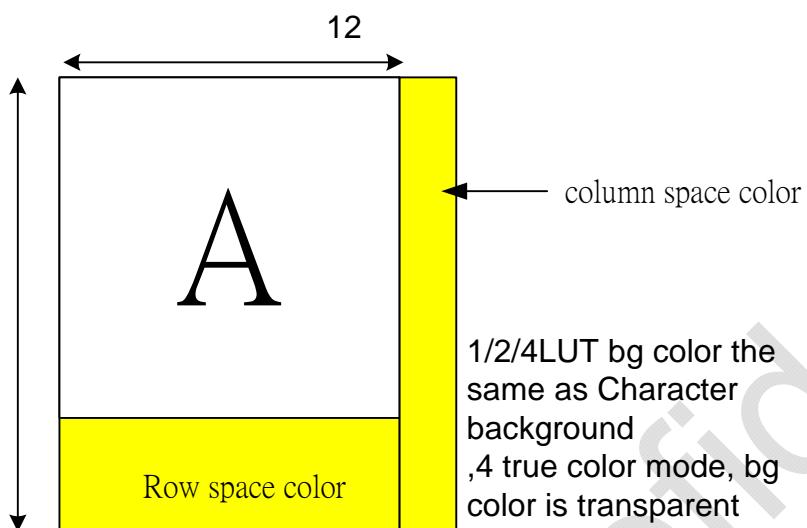
Notice:

When character height/width is doubled, the row height/column space definition also twice. If the row height is larger than character height, the effect is just like space between rows. If it is smaller



than character height, it will drop last several bottom line of character.

When using 1/2/4LUT font, column space and font smaller than row height, the color of column space and row space is the same as font background color, only 4 bit true color font mode, the color is transparent



Byte 2

Bit	Mode	Function
7:0	W	Row length unit: font base

Character Command (For blank)

Byte 0

Bit	Mode	Function
7	W	0
6	W	Blinking effect 0: Disable 1: Enable
5:4	W	01
3:0	W	Reserved

Byte 1

Bit	Mode	Function
7:0	W	Blank pixel length

At least 3 pixels, and can't exceed 255 pixels.



Byte 2

Bit	Mode	Function
7:6	W	Reserved
5:0	W	Blank color – select one of 64-color LUT (0 is special for transparent)

Character Command (For 1-bit RAM font)

Byte 0

Bit	Mode	Function
7	W	Use combined with [5:4]
6	W	Character Blinking effect 0: Disable 1: Enable
5:4	W	{[7], [5:4]} (Font type 000: 1-bit RAM Font When Row command Byte 0[5] is 0 Font select from 0-255 When Row command Byte 0[5] is 1 Font select from 512-767 Color palette from 16-31 001: Blank 010: 1-bit RAM Font When Row command Byte 0[5] is 0 Font select from 256-511 When Row command Byte 0[5] is 1 Font select from 768-1023 Color palette from 0-15 011: 1-bit RAM Font When Row command Byte 0[5] is 0 Font select from 256-511 When Row command Byte 0[5] is 1 Font select from 768-1023 Color palette from 16-31



		<p>100: 1-bit RAM Font When Row command Byte 0[5] is 0 Font select from 0-255 When Row command Byte 0[5] is 1 Font select from 512-767 Color palette from 0-15</p> <p>101: 4-bit RAM Font Font select from 0-255 Color palette from 0-63</p> <p>110: 2-bit RAM Font Font select from 0-254 (with Frame Ctrl register 00B byte1 [6:0]) Color palette from 0-15</p> <p>111: 2-bit RAM Font Font select from 0-254 (with Frame Ctrl register 00B byte1 [6:0]) Color palette from 16-31)</p>
	W	<p>VBI OSD disable: Character width (only for 1-pixel font, doubled when specifying double-width in Row/Blank command register) For 12x18 font: 0100: 4-pixel 0101: 5-pixel 0110: 6-pixel 0111: 7-pixel 1000: 8-pixel 1001: 9-pixel 1010: 10-pixel 1011: 11-pixel 1100: 12-pixel For 18x12 Font (rotated) 0000: 4-pixel 0001: 5-pixel 0010: 6-pixel 0011: 7-pixel 0100: 8-pixel 0101: 9-pixel 0110: 10-pixel 0111: 11-pixel 1000: 12-pixel 1001: 13-pixel 1010: 14-pixel 1011: 15-pixel 1100: 16-pixel 1101: 17-pixel 1110: 18-pixel 1111: 36-pixel VBI OSD enable: While VBI OSD enable, 1 bit font will be NO rotated and 12-pixel fonts always. Then the [3:0] setting will be as following: [3]: character select[8] support 512 font while VBI OSD enable [2]: additional blinking effect {[6], [2]} 00: NO blink for both F/B 01: Only blink for Foreground 10: Only blink for Background</p>



		11: Both blink for F/B [1]: Underline enable underline will be at 17th & 18th line and got the same color with foreground [0]: Reserved
--	--	--

When using border/shadow/ effect, the width of the 1-bit font should at least 6 pixel.

Byte 1

Bit	Mode	Function
7:0	W	Character Select [7:0]

Byte 2

Bit	Mode	Function
7:4	W	Foreground color Select one of 16-color from color LUT
3:0	W	Background color Select one of 16-color from color LUT (0 is special for transparent)

Character command (For 2-bit RAM Font)

Byte 0

Bit	Mode	Function
7	W	1
6	W	MSB of Foreground color 11, Background 00
5	W	1
4	W	0: color palette 0-15 1: color palette 16-31
3:1	W	Foreground color 11 Select one of 8 color from color LUT Add Byte0 [6] as MSB for 16-color LUT.
0	W	Background color 00 Bit[2] Select one of 8 color from color LUT

Byte 1

Bit	Mode	Function
7	W	MSB of Foreground color 10, Foreground 01
6:0	W	Character Select [6:0]

Byte 2

Bit	Mode	Function
7:6	W	Background color 00 Bit[1:0]



		Select one of 8 color from color LUT While 0 is special for transparent Add Byte0 [6] as MSB for 16-color LUT. Once we fill 0000 or 1000(MSB follow Byte0[6]), BG appears transparent.
5:3	W	Foreground color 10 Select one of 8 color from color LUT Add Byte0 [4] as MSB for 16-color LUT.
2:0	W	Foreground color 01 Select one of 8 color from color LUT Add Byte0 [4] as MSB for 16-color LUT.

Character command (For 4-bit RAM font)

Byte 0

Bit	Mode	Function
7	W	1
6	W	Character Blinking effect 0: Disable 1: Enable
5:4	W	01 (Font type 00: 1-bit RAM Font 01: 4-bit RAM Font 1x: 2-bit RAM Font)
3:0	W	(for Byte1[7] = 0) select one color from 16-color LUT as background

Byte 1

Bit	Mode	Function
7:0	W	Character Select [7:0]

- When 4-bit look-up table mode , color of column space is the same as background.
- When 4-bit look-up table mode and pixel value is 0000, and byte0[3:0]=0000 means transparent.
- When true color mode and pixel value is 0000 , it is transparent .

Byte 2

Bit	Mode	Function
7:6	W	Color select 12 13 14 15



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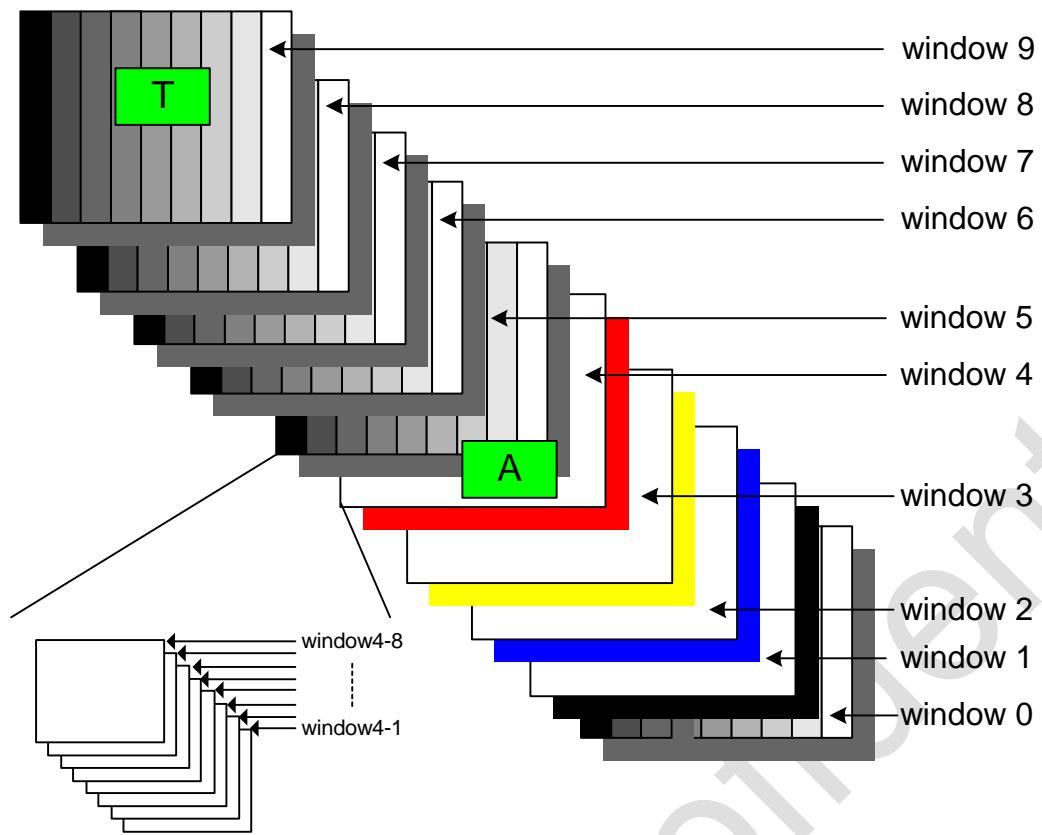
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		00: color select 12 13 14 15 01: color select 28 29 30 31 10: color select 44 45 46 47 11: color select 60 61 62 63
5:4	W	Color select 8 9 10 11 00: color select 8 9 10 11 01: color select 24 25 26 27 10: color select 40 41 42 43 11: color select 56 57 58 59
3:2	W	Color select 4 5 6 7 00: color select 4 5 6 7 01: color select 20 21 22 23 10: color select 36 37 38 39 11: color select 52 53 54 55
1:0	W	Color select 0 1 2 3 00: color select 0 1 2 3 01: color select 16 17 18 19 10: color select 32 33 34 35 11: color select 48 49 50 51



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Display Priority

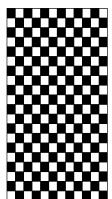
Display Priority

We have six windows with gradient and twelve windows without gradient, the window priority is as above, character should be always on the top layer of the window.

Pattern gen.

Use OSD to replace display pattern generator.

Chess Board: make a font as below



If we want to fill to the full 1280x1024 screen with character, we need 1280*1024 pixels.
Required character is:

Using 12*18 font

$$1280/12 = 106.7 \rightarrow 107$$

$$1024/18 = 56.9 \rightarrow 57$$

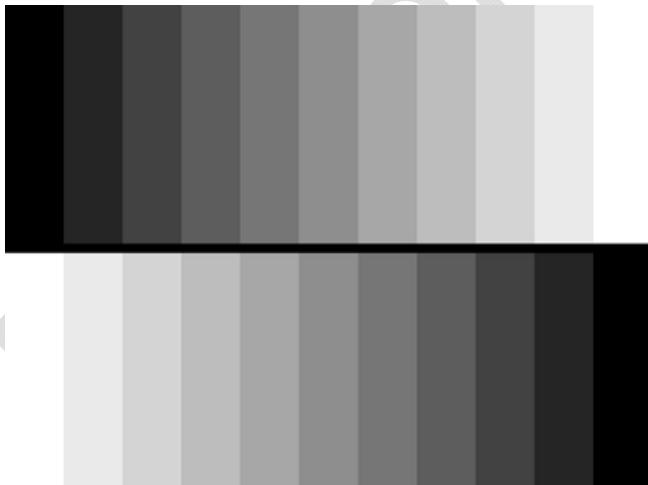
$$107*57 = 6099 \text{ character}$$

The required number of character map is larger than RAM size. We must turn on double width or double height function to reduce the half of character map.

So the basic unit to chessboard is 2x2 pixel. You can use larger chessboard instead of 2x2 pixels unit, such as 4x4 and so on.

Gray level

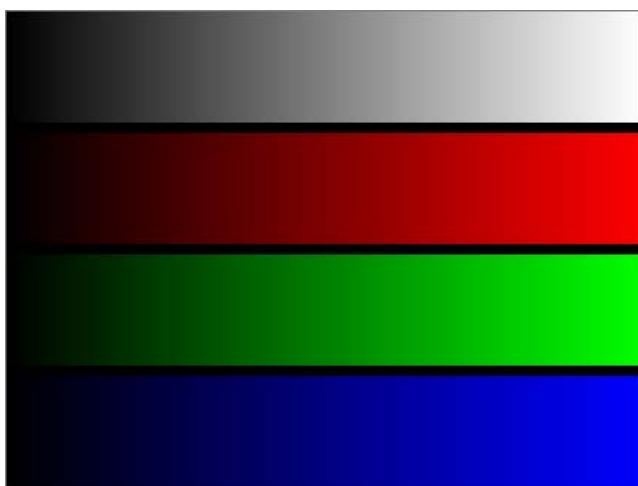
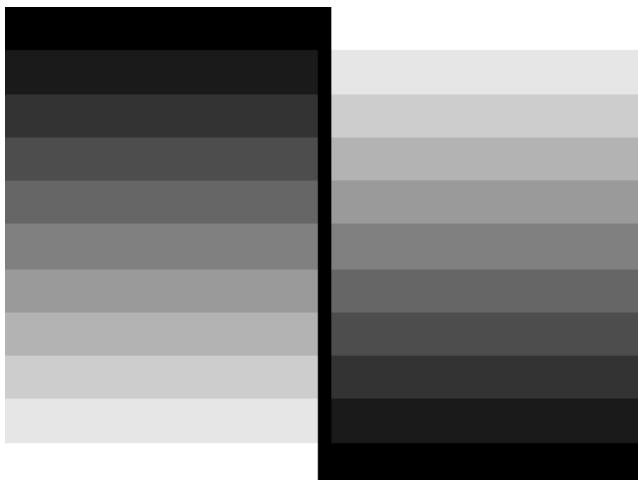
We can display 256 gray level by gradient window, 8 and 16 gray level by character map. 32 and 64 gray level is not supported.





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6. Electric Specification

DC Characteristics

Table 3 Absolute Maximum Ratings

PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS
Voltage on Input (5V tolerant)	V _{IN}	-1		5	V
Supply Voltage	PVCC	3.0	3.3	3.6	V
Electrostatic Discharge	V _{ESD}			±2.5	kV
Latch-Up	I _{LA}			±100	mA
Ambient Operating Temperature	T _A	0		70	°C
Storage temperature (plastic)	T _{STG}	-55		125	°C
Thermal Resistance (Junction to Air)	θ _{JA}			38	°C/W
Junction Acceptable Temperature	T _j			125	°C

PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS
Reset pulse period	Trst-en ¹	1120			ns
Power on reset period	Tpor-rst ²	293			ms

1. 16 * x'tal_cycle(1/14.3Mhz)

2. 65536*64*Xtal_cycle(1/14.3Mhz)



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7. Mechanical Specification

128 Pin Package (QFP)

