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Product No.: WM-08010

Product Specification of 802.11b/g WLAN Module

HW Prepared by： James Date : 2008-09-24

SW Prepared by： Date :

Checked by： Date :

Approved by： Date :

Concurrence (MD): Date :

Concurrence (PM): Date :

1 REVISION HISTORY

Version No.	Revised Date	Revised by	Description	Notes
0.1	2008-09-09	James	Preliminary specification released	Proposal
0.2	2008-09-22	James	Modify Pin Description of the Pin 5	Proposal
0.3	2008-09-24	James	Modify information of Application note	Proposal

INDEX

1. Introduction

The purpose of this document is to define the product specification for 802.11b/g WiFi module that simultaneously provides WiFi connections. All the data in this document is based on the Data sheet of MTK MT5921P MAC/BB WLAN Chip, and other documents which are used in the design.

FEATURES

- Small footprint: 9.0 × 9.0 × 1.5 mm max.
- Support Orthogonal Frequency Division Multiplexing (OFDM), Complementary Code Keying (CCK) and Direct Sequence Spread Spectrum (DSSS) to provide a variety of data rates.
- Shared clock, EEPROM, and full RF front ends integrated for WiFi
- Support ad-hoc and infrastructure modes
- Support 32 multicast address filters
- Programmable TX/RX FIFO size
- 802.1H packet format translation
- 802.11 auto rate control
- Support BT co-existence
- Up to 12 pair-wise keyed peers
- 802.11 b/g/e/i/h/k/w compatible
- TX/RX on-the-fly encryption/decryption
- 64/128-bit Wired Equivalent Privacy (WEP), Temporal Key Integrity Protocol (TKIP), and Advanced Encryption Standard (AES-CCMP)
- Support 802.11 IBSS and infrastructure power save
- Support low power consumption sleep mode via 32 KHz clock
- Support hardware scan
- Background scan for specific SSID networks
- Support 802.11e optional U-APSD, Admission Control Procedure, and DLS
- TCP/UDP/IP checksum generation/verification
- Wakeup by specific packet (pattern search)

- Support CCX5
- Support thermo-sensor to resist temperature change
- Immune from EM interference with metal shielding
- Frequency band: 2.4 to 2.497GHz (1 to 14 channels)
- Support SDIO, eHPI interface
- Support for IEEE 802.11e QoS
- Support for IEEE 802.11i advanced security
- Support for Fixed Mobile Convergence - UMA (Unlicensed Mobile Access) and IMS (IP Multimedia Subsystem)
- 40MHZ crystal embedded
- RoHS complaint
- Embedded OS supported

APPLICATIONS

- Smartphone / PDA / PDA phone / WiFi phone / DSC / DVC with WiFi connectivity

OS SUPPORT

Item	Host Operating System	SDIO interface	eHPI interface
1	WinCE/Win Mobile (V6.0/6.1)	Available	Not yet
2	Linux	Available	Available

1.1 Block Diagram Topology

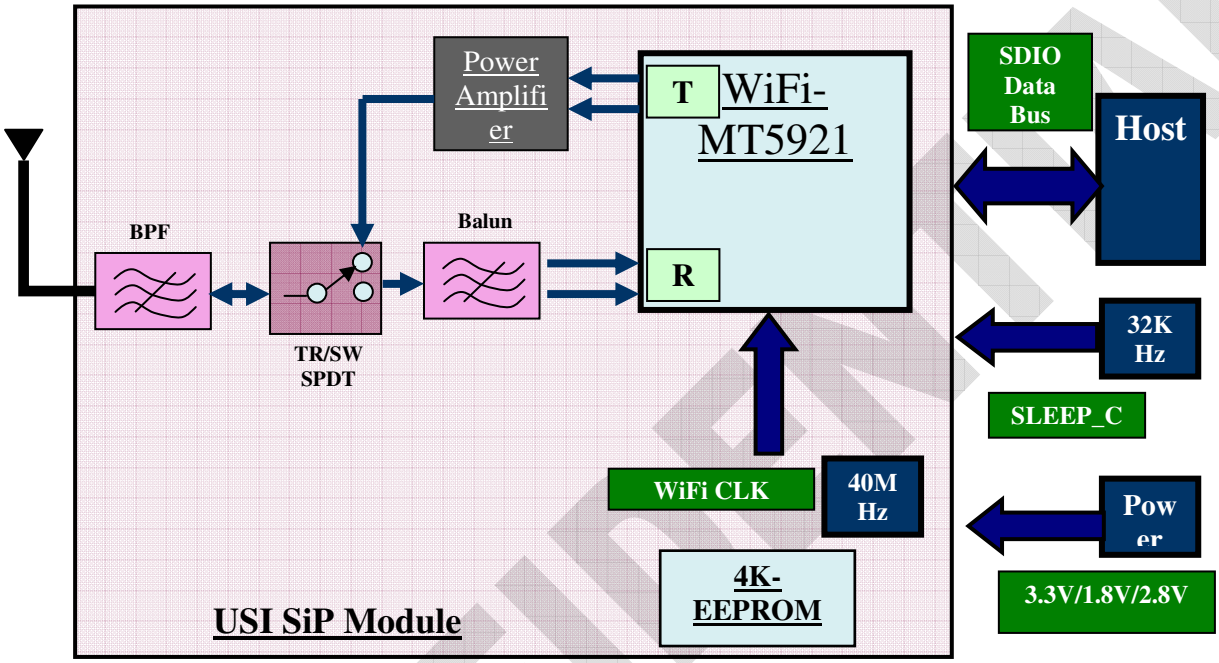


Figure1-Block Diagram of WiFi Module

1.2 GENERAL SPECIFICATION

Network Standard	IEEE 802.11g/b Compliant
Host Interface	SDIO v1.0: SDIO 1-bit, SDIO 4-bit, SDIO eHPI interface
Frequency Band	2400 to 2497MHz (channel 1 to 14)
Data Transfer Mode	OFDM & DSSS
Modulation	64QAM (54, 48Mbps), 16QAM (36, 24Mbps), QPSK (18, 12Mbps), BPSK (9, 6Mbps); CCK (11, 5.5 Mbps), DQPSK (2 Mbps), DBPSK (1Mbps)
Access Method	Ad hoc mode, Infrastructure mode
Media Access Protocol	CSMA/CA (Carrier Sense Multiple Access with Collision Avoidance)
Antenna	External single antenna support. The output impedance is 50Ω.

1.3 Module Pinout

1.3.1 Pin Assignment

The module will conform to the following pinout, shown in the following diagram (top view)

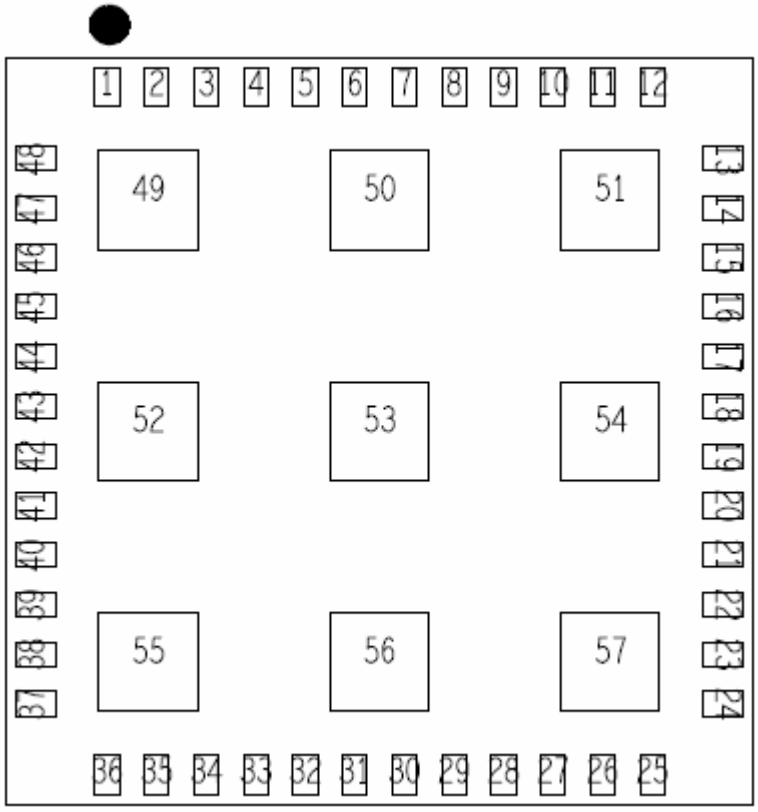


Figure2-Required Pinout for WiFi Module

1.3.2 Pin Description

Pin Number	Pin Name	I/O	Power Domain	Description
1	WLAN_ACT	IO	DVDD28	WLAN_ACT for 2-/3-/4-wire mode. BT-coexistence
2	BT_PRI	I	DVDD28	BT_PRI for 2-/3-/4-wire mode. BT-coexistence
3	OSC_EN	O		Oscillator enable
4	GND	P		Ground
5	PAVDD33	P	PAVDD33	3.3V power supply for RF PA.
6	GPIO2	IO	DVDD28	• General purpose IO 2 • 3.3V/2.8V interrupt output • Daisy chain input for external oscillator control
7	LED1	O	DVDD33	LED Control
8	MODE1	I	DVDD33	Mode select bit 1
9	MODE0	I	DVDD33	Mode select bit 0
10	GPIO0	IO	DVDD28	•General purpose IO 0 •BT_ACT for 3-/4-wire mode BT-coexistence •Daisy chain input for external oscillator control
11	GND	P		Ground
12	GND	P		Ground
13	ANT_OUT	I/O		RF IO port (50 Ohms)
14	GND	P		Ground
15	D5	IO	DVDDMIO	eHPI8/16 data bus bit 5
16	D6	IO	DVDDMIO	eHPI8/16 data bus bit 6
17	GND	P		Ground
18	VDD18	P	VDD18	1.8V power input
19	D7	IO	DVDDMIO	eHPI8/16 data bus bit 7
20	D8	IO	DVDDMIO	eHPI16 data bus bit 8
21	D9	IO	DVDDMIO	eHPI16 data bus bit 9
22	D10	IO	DVDDMIO	eHPI16 data bus bit 10
23	D11	IO	DVDDMIO	eHPI16 data bus bit 11
24	D12	IO	DVDDMIO	eHPI16 data bus bit 12
25	D14	IO	DVDDMIO	eHPI16 data bus bit 14
26	D4	IO	DVDDMIO	eHPI8/16 data bus bit 4

Pin Number	Pin Name	I/O	Power Domain	Description
27	D2	IO	DVDDMIO	• eHPI8/16 data bus bit 2 • SDIO data bus bit 2
28	D3	IO	DVDDMIO	• eHPI8/16 data bus bit 3 • SDIO data bus bit 3
29	GND	P		Ground
30	CS_N	IO	DVDDMIO	• eHPI8/16 chip select • SDIO command bus
31	A0	I	DVDDMIO	• eHPI8/16 address select • SDIO clock input
32	GPIO1	IO	DVDD28	• General purpose IO 1 • BT_FREQ signal for 4-wire mode BT-coexistence • Daisy chain input for external oscillator control
33	D0	IO	DVDDMIO	• eHPI8/16 data bus bit 0 • SDIO data bus bit 0
34	D13	IO	DVDDMIO	eHPI16 data bus bit 13
35	D1	IO	DVDDMIO	• eHPI8/16 data bus bit 1 • SDIO data bus bit 1
36	INT_N	O	DVDDMIO	Host interface interrupt output
37	EXT_RST_N	I	DVDD28	External HW Reset
38	WE_N	I	DVDDMIO	eHPI8/16 write strobe
39	OE_N	I	DVDDMIO	eHPI8/16 read strobe
40	D15	I/O	DVDDMIO	eHPI16 data bus bit 15
41	DVDDMIO	I	DVDDMIO	Host interface power input
42	GND	P		Ground
43	XIN_32K	I	DVDD33	Digital 32.768 KHz clock input
44	GND	P		Ground
45	DVDD28	I	DVDD28	2.8V digital power input
46	GND	P		Ground
47	DVDD33	I	DVDD33	3.3V digital power input
48	GND	P		Ground
49 ~ 57	GND	P		Ground

▪ 1.4 Mechanical Dimensions

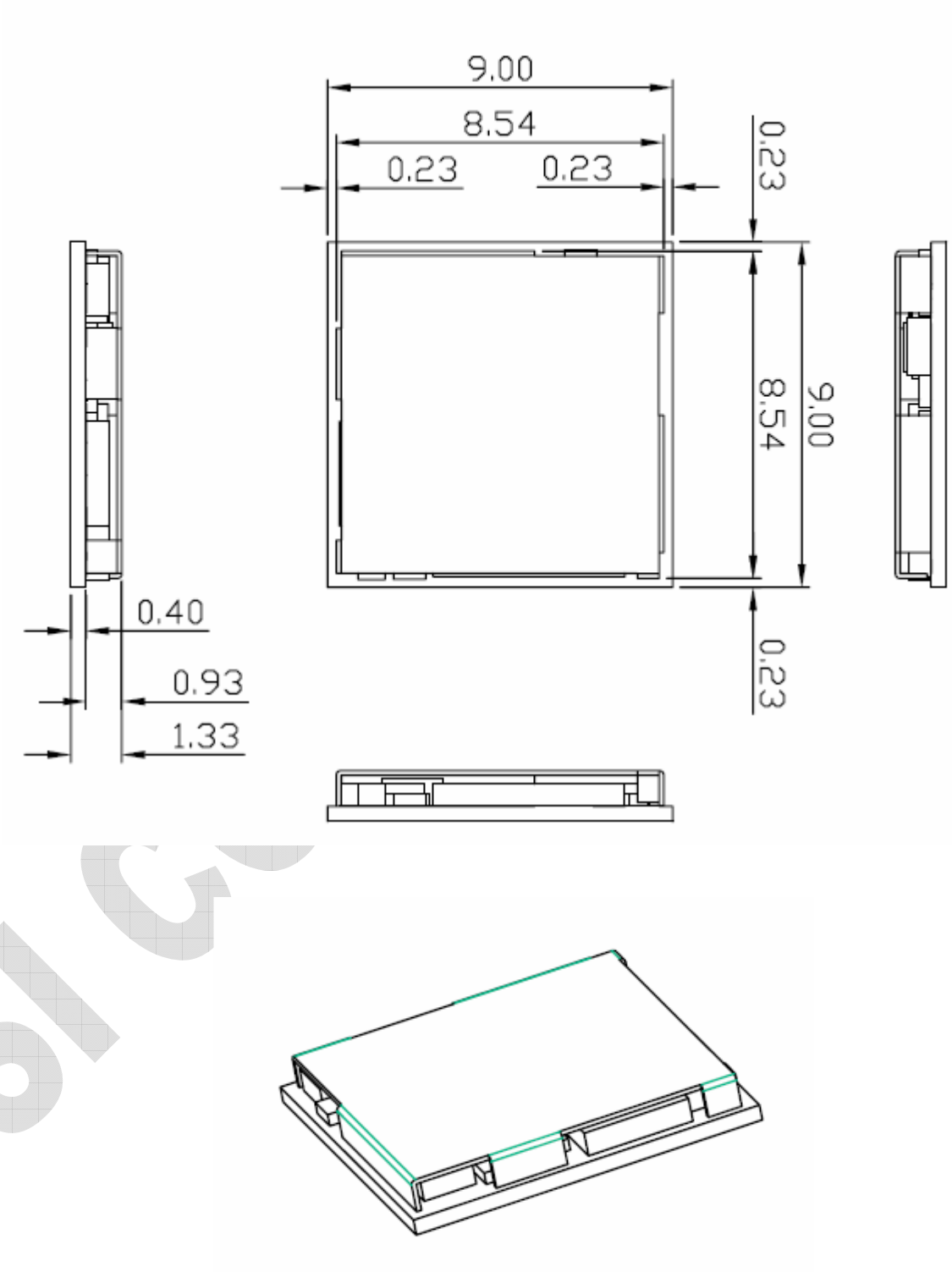
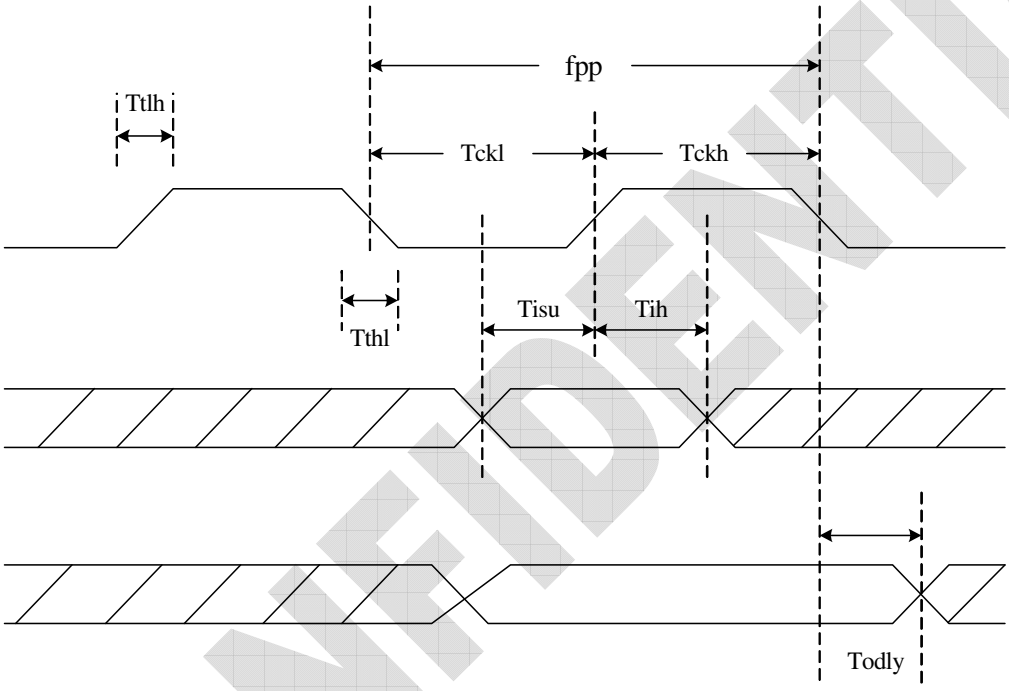


Figure4 - Mechanical of WiFi Module

2 HOST INTERFACE

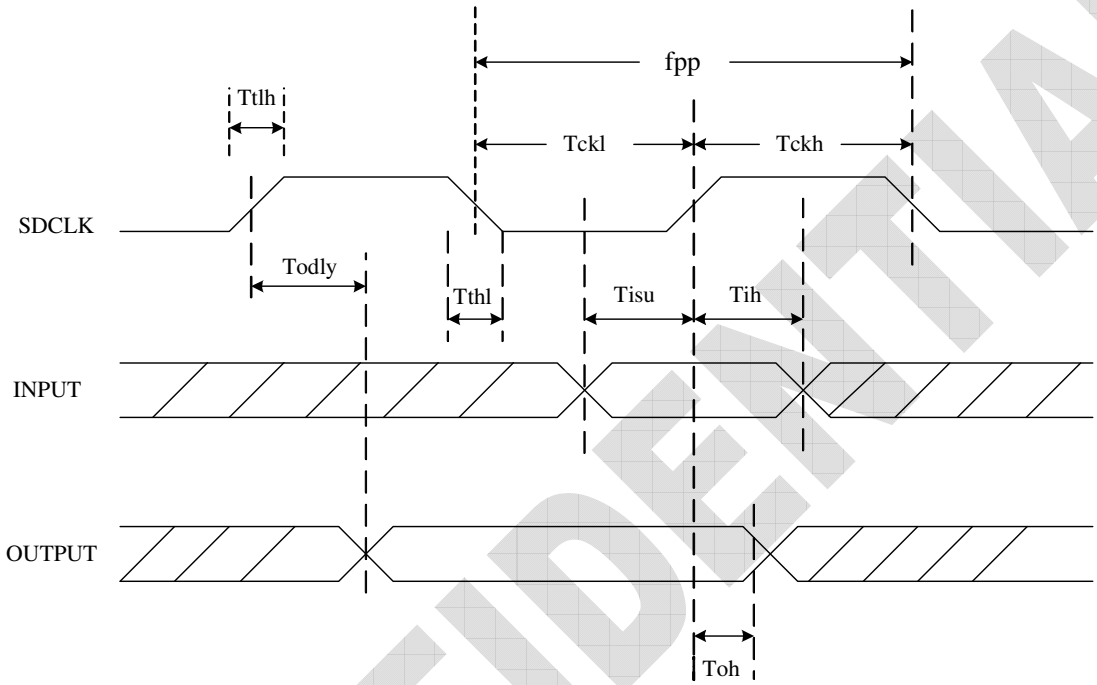
The Combo module provides SDIO interface. The timing for interface is described as follows.

2.1 SDIO HOST INTERFACE PROTOCAL TIMING (25MHZ)



Symbol	Parameter	Min	Typ	Max	Units
fpp	Clock Frequency	0		25	MHz
Tckl	Clock Low Time	10			ns
Tckh	Clock High Time	10			ns
Ttlh	Clock Rise Time			10	ns
Tthl	Clock Fall Time			10	ns
Tisu	Input Setup Time	5			ns
Tih	Input Hold Time	5			ns
Todly	Output Delay Time	0		11	ns

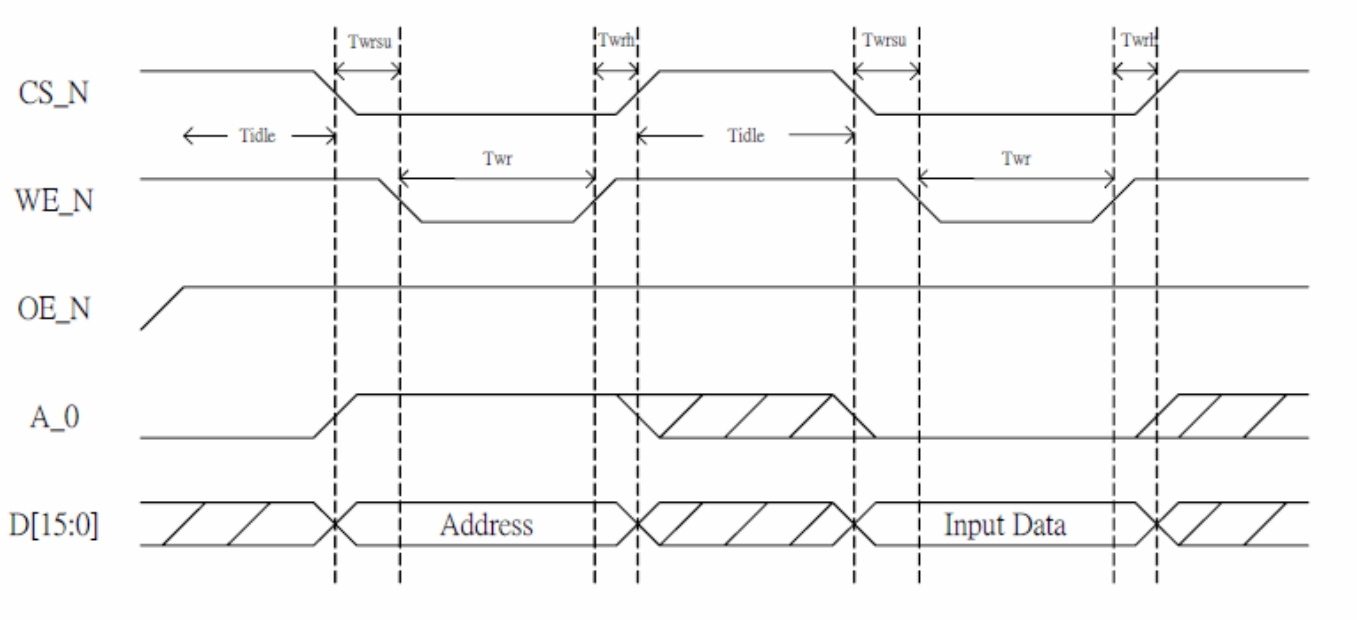
2.2 SDIO HOST INTERFACE PROTOCAL (50MHZ)



Symbol	Parameter	Min	Typ	Max	Units
fpp	Clock Frequency			50	MHz
Tckl	Clock Low Time	7			ns
Tckh	Clock High Time	7			ns
Ttlh	Clock Rise Time			3	ns
Tthl	Clock Fall Time			3	ns
Tisu	Input Setup Time	6			ns
Tih	Input Hold Time	2			ns
Toh	Output Hold Time	2.5			ns
Todly	Output Delay Time	0		12	

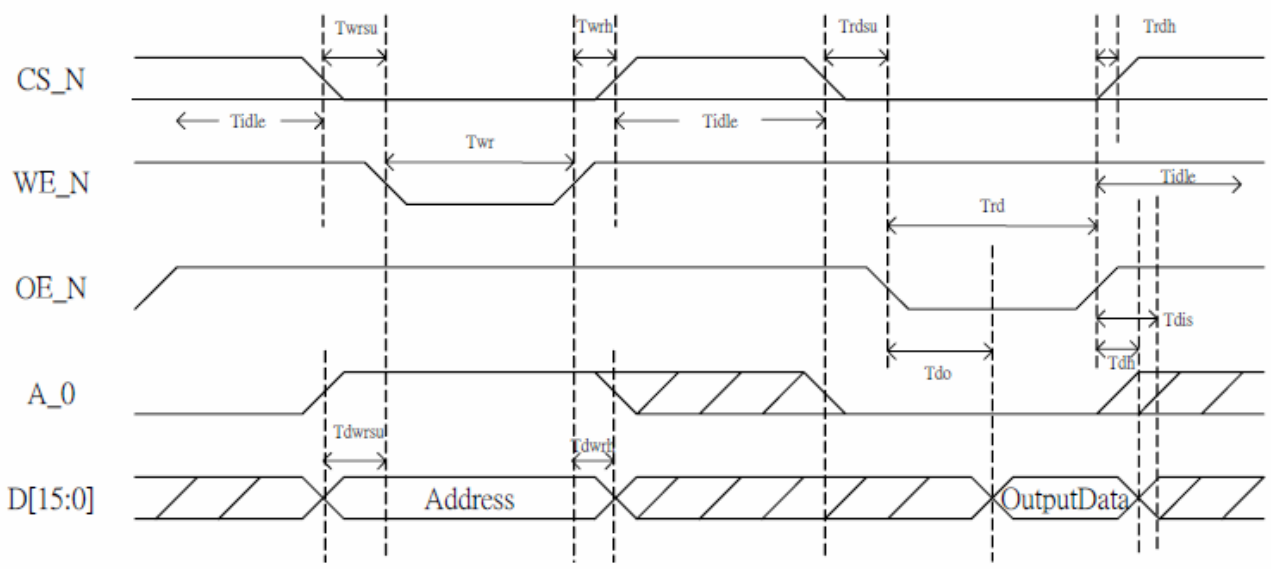
2.3 EHPI INTERFACE

2.3.1 WITER CYCLE



Symbol	Parameter	Min	Typ	Max	Units
Twr	Write Pulse Width	76			ns
Twrsu	Control & Data vs WE_N setup time	0			ns
Twrh	Control & Data vs WE_N hold time	0			ns
Tidle	Twice Access cycle space Time	76			ns

2.3.2 READ CYCLE

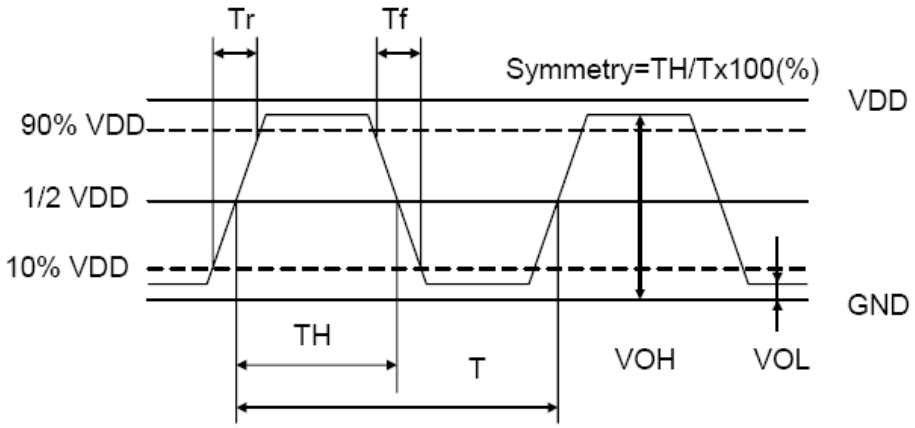


Symbol	Parameter	Min	Typ	Max	Units
Twr	Write Pulse Width	76			ns
Twrsu	Control vs WE_N setup time	0			ns
Twrh	Control vs WE_N hold time	0			ns
Tdwrsu	Data & A_0 vs WE_N setup time	18			ns
Tdwrh	Data & A_0 vs WE_N hold time	18			ns
Tidle*	Twice Access cycle space Time	76/152*			ns
Trd	Read Pulse Width	76			ns
Trdsu	Control vs OE_N setup time	0			ns
Trdh	Control vs OE_N hold time	0			ns
Tdo	Output Data Delay Time			65	ns
Tdh	Output Data Hold Time	0			ns
Tdis	Output Disable Time			20	ns

* When read BBCR, the Tidle between write and read operation should be 152ns. Otherwise, the Tidle is 76ns.

2.4 EXTERNAL 32 KHZ INPUT CLOCK

The figure below shows the timing requirement for the external 32KHz input clock.



	Parameters	SYM.	Electrical Spec.				Notes
			MIN	TYPE	MAX	UNITS	
1	Nominal Frequency	-		32.768000		KHz	-
2	Frequency Stability	-		±30		ppm	-
3	Operating Temperature	Topr	-40	25	85	℃	-
4	Storage Temperature	Tstg	-55	~	125	℃	-
5	Supply Voltage	VDD	2.97	3.3	3.63	V	-
6	Current Consummption	Icc	-	-	3	mA	-
7	Enable Control	-		Yes		-	Pad 1
8	Output Load : CMOS	CL		15		pF	-
9	Output Voltage High	VoH	Vdd-0.4	-	-	V	-
10	Output Voltage Low	VoL	-	-	0.33	V	-
11	Rise Time	Tr	-	200	350	ns	10%→90%VDD Level
12	Fall Time	Tf	-	200	350	ns	90%→10%VDD Level
13	Symmetry (Duty ratio)	TH/T	45	~	55	%	-
14	Start-up Time	Tosc	-	-	3	ms	To 90% of Final Amplitude
15	Enable Voltage High	V_{IH}	$0.7V_{DD}$	-	-	V	-
16	Disable Voltage Low	V_{IL}	-	-	$0.3V_{DD}$	V	-
17	Aging	-		±5		ppm/yr.	1st. Year at 25℃

2.5 EXTERNAL 40 MHZ INPUT CLOCK

Electrical Characteristics :

[1] Operating Conditions :

Item	Symbol	MIN.	TYP.	MAX.	Unit	Condition
Operating Temperature Range	Topt	-20		70	℃	
Storage Temperature Range	Tstg	-40		90	℃	
Load Capacitance	CL		10		pF	
Drive Level	DL			100	μW	

[2] Frequency Stability :

Item	Symbol	MIN.	TYP.	MAX.	Unit	Condition
Tolerance	dF/Fo	-10		10	ppm	Refer to Center Frequency @25±3℃
Stability Over Temperature	dF/F25	-10		10	ppm	Refer to Operating Temperature
Trim Sensitivity Over Load	TS	10			ppm/pF	@CL
Aging	dF/F25	-2		2	ppm	Per Year

dF/Fo: Frequency Deviation Refer to Center Frequency

dF/F25: Frequency Deviation Refer to 25 ℃ Frequency

3 DC CHARACTERISTICS

Symbol	Parameter	Min	Typ.	Max.	Umit
PAVDD33	Supply voltage	3.0	3.3	3.6	V
	Supply current (transmit OFDM 54M @ 14 dBm)		94	170	mA
	Supply current (transmit CCK 11M @ 16 dBm)		114	170	mA
VDD18	Supply voltage	1.7	1.8	1.9	V
	Supply current (transmit OFDM 54M @ 14 dBm)		115	150	mA
	Supply current (transmit CCK 11M @ 16 dBm)		125	150	mA
	Supply current (receiver mode)		120	150	mA
	Supply current (sleep mode)		120		uA
DVDD33	Supply voltage	2.52	2.6~3.3	3.63	V
	Supply current (transmit mode)		4.0	10	mA
	Supply current (receiver mode)		2.8	10	mA
	Supply current (sleep mode)		16		uA
DVDD28	Supply voltage	2.52	2.6~3.3	3.63	V
	Supply current (transmit mode)		0.4	10	mA
	Supply current (receiver mode)		0.4	10	mA
	Supply current (sleep mode)		10		uA
DVDDMIO	Supply voltage	1.62	1.8~3.3	3.63	V
	Supply current (transmit mode)		0.6	5	mA
	Supply current (receiver mode)		0.6	5	mA
	Supply current (sleep mode)		12		uA

4 RADIO SPECIFICATIONS

The performance of WM-08010 is given as follows.

4.1 WiFi RF Specification

Condition: DVDD33=DVDD28=DVDDMIO=3.3V, VDD18=1.8V, PAVDD33=3.3V

4.1.1 WiFi RF Transmitter Specification

802.11g Transmit

Item	Condition	Min.	Typ.	Max.	Unit
Operating frequency range		Channel 1		Channel 14	
Transmit power level	54Mbps OFDM	13	14	15	dBm
Transmit center frequency tolerance		-10	0	10	ppm
RF carrier suppression	Channel estimation phase		-40	-30	dB
Transmit modulation accuracy	54Mbps		-31.5	-28	dB
	48Mbps		-30	-27	dB
	36Mbps		-29.5	-26	dB
	24Mbps		-28	-25	dB
	18Mbps		-27	-24	dB
	12Mbps		-26.5	-23	dB
	9Mbps		-26	-22	dB
	6Mbps		-26	-21	dB
Transmit spectral mask (6/9/12/18/24/36/48/54 Mbps)	Fc-20MHz<F<Fc-11MHz &Fc+11MHz<F<Fc+22MHz				dB
	F<Fc-30MHz & F>Fc-20MHz			-28	dBr
Transmit spectral flatness	Channel estimation phase +/- 16 sub-carriers	-2		2	dBr
	Channel estimation phase +/-17 ~ +/-26 sub-carriers	-4		2	dB

802.11b Transmit					
Item	**Condition**	**Min.**	**Typ.**	**Max.**	**Unit**
Operating frequency range		Channel 1		Channel 14	
Transmit power level	2M DQPSK	15	16	17	dBm
Transmit center frequency tolerance		-10	0	10	ppm
Transmit spectral mask	Fc-22MHz<F<Fc-11MHz & Fc+11MHz<F<Fc+22MHz(1/2/5.5/11Mbps; channel 1~13)			-30	dBr
	F<Fc-22MHz & F>Fc+22MHz(1/2/5.5/11Mbps; channel 1~13)			-50	dBr
	90% power of occupied BW (Channel 14, Japan filter)	13.75			MHz
	99% power of occupied BW (Channel 14, Japan filter)			26	MHz
Transmit power -on	10% ~ 90 %		0.2	2	us
Transmit power -down	90% ~ 10 %		0.2	2	us
RF carrier suppression	DSB carrier suppression		-46	-35	dB
Transmit modulation accuracy	1/2/5.5/11 Mbps	4	8	20	%

4.1.2 WiFi RF Receiver Specification

802.11g Receiver					
Item	**Condition**	**Min.**	**Typ.**	**Max.**	**Unit**
Operating frequency range		Channel 1		Channel 14	
Receiver minimum input	54Mbps		-73.5	-70	dBm
level sensitivity (PER<10 %)	48Mbps		-73.5	-70	ppm
	36Mbps		-80	-77	dBm
	24Mbps		-80	-77	dBm
	18Mbps		-87	-84	dBm
	12Mbps		-87	-84	dBm
	9Mbps		-90.5	-87	dBm
	6Mbps		-90.5	-87	dBm
Receiver maximum input level (PER<10%)	6/9/12/18/24/36/48/54	-5			dBm
Receiver non-adjacent channel rejection (PER<10%)	54Mbps	15	28		dB
	48Mbps	16	30		dB
	36Mbps	20	35		dB
	24Mbps	24	39		dB
	18Mbps	27	41		dB
	12Mbps	29	42		dB
	9Mbps	31	46		dB
	6Mbps	32	47		dB
Receiver adjacent channel rejection (PER<10%)	54Mbps	-1	15		dB
	48Mbps	0	19		dB
	36Mbps	4	21		dB
	24Mbps	8	27		dB
	18Mbps	11	29		dB
	12Mbps	13	30		dB
	9Mbps	15	30		dB
	6Mbps	16	31		dB

802.11b Receiver					
Item	**Condition**	**Min.**	**Typ.**	**Max.**	**Unit**
Receiver minimum input level sensitivity (PER< 8 %)	11Mbps		-87.5	-84	dBm
	5.5Mbps		-91.5	-88	dBm
	2Mbps		-93.5	-90	dBm
	1Mbps		-94.5	-91	dBm
Receiver maximum input level sensitivity (PER< 8 %)	1/2/5.5/11 Mbps	3	8		dBm
Receiver adjacent channel rejection (PER< 8 %)	11Mbps	35	38		dB

5 ELECTRICAL SPECIFICATION

5.1 Absolute Maximum Ratings

Symbol	Parameter	Min	Typ	Max	Units
DVDD33	3.3V ~ 2.8V digital I/O power supply	2.52	2.8 ~3.3	3.63	V
DVDD28	3.3V ~ 2.8V digital I/O power supply	2.52	2.8	3.63	V
PAVDD33	3.3V ~ 2.8V Analog power supply		2.8 ~3.3	3.63	
DVDDMIO	3.3V ~ 1.8V digital I/O power supply	1.62	1.8 ~3.3	3.63	V
VDD18	1.8V AFE power supply	1.7	1.8	1.9	V
Voltage Ripple	+/-2%, 10KHz~100KHz, Max. values not exceeding Operating voltage	-	-	2	%
Storage Temperature	-20° to 105° Celsius	-20	25	105	Celsius
Humidity Range	Max 95%	Non condensing, relative humidity			

5.2 Recommended Operating Range

The Combo module withstands the operational requirements as listed in the table below.

Operating Temperature	-20° to 70° Celsius	
Humidity Range	Max 95%	Non condensing, relative humidity

5.2.1 SUPPLY VOLTAGE

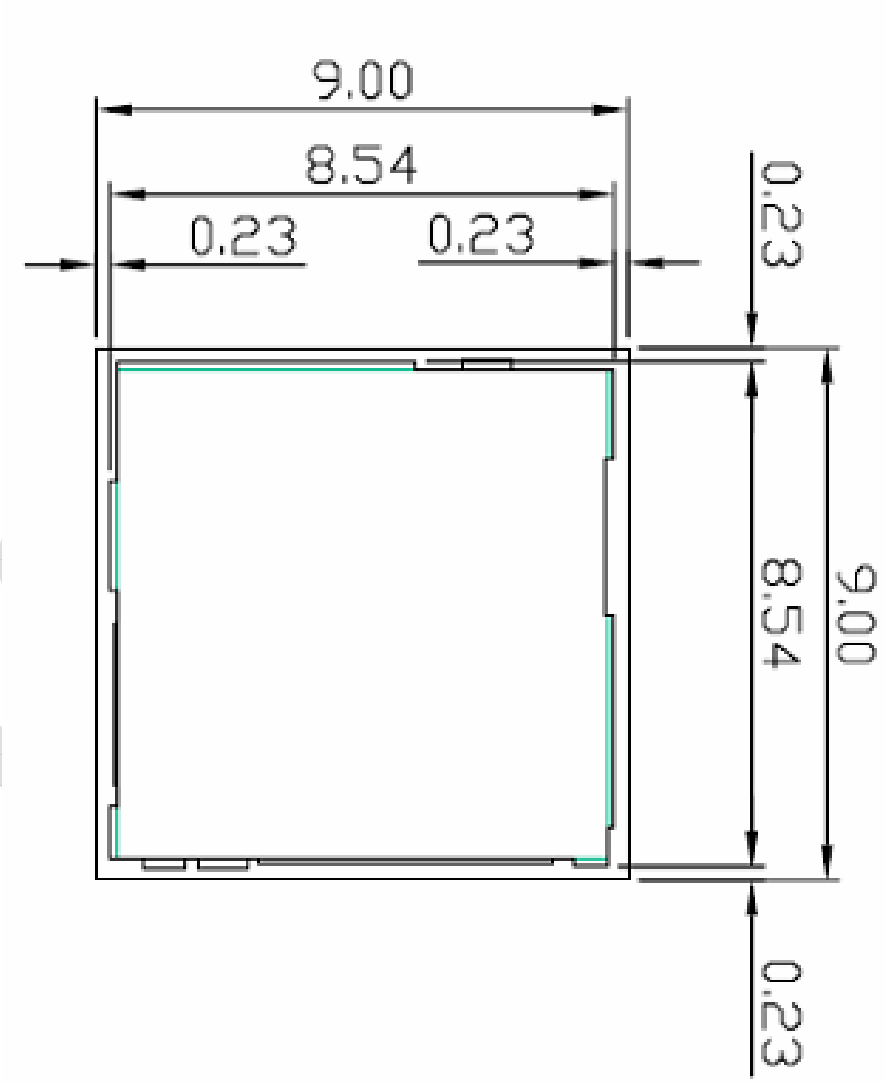
Symbol	Parameter	Min	Max	Units
DVDD33	3.3V ~ 2.8V digital I/O power supply	2.52	3.63	V
DVDD28	3.3V ~ 2.8V digital I/O power supply	2.52	3.63	V
PAVDD33	3.3V ~ 2.8V Analog power supply	2.52	3.63	V
DVDDMIO	3.3V ~ 1.8V digital I/O power supply	1.62	3.63	V
VDD18	1.8V AFE power supply	1.7	1.9	V

6 MECHANICAL DRAWING AND SOLDERING

6.1 MODULE OUTLINE

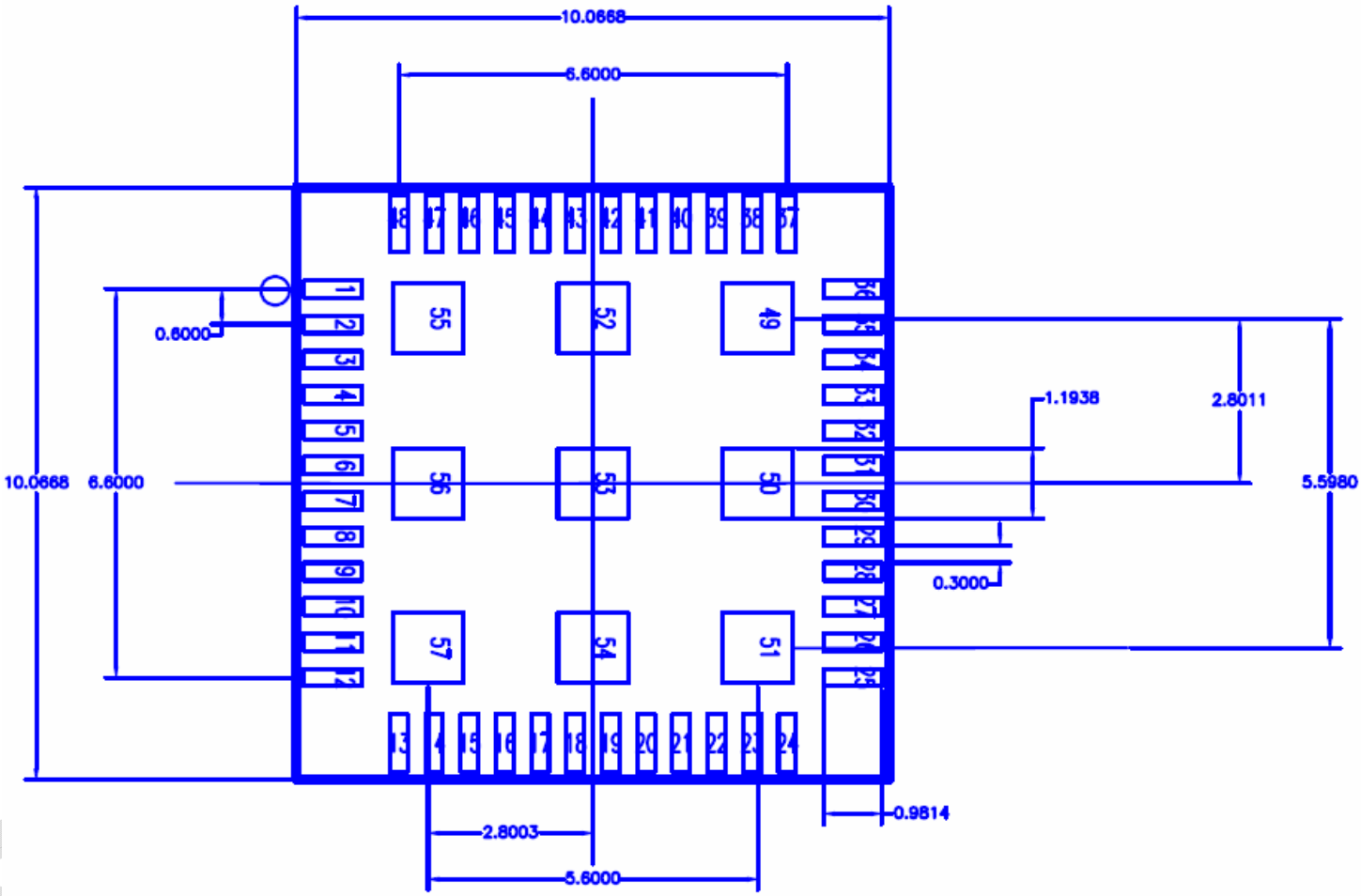
Module Dimension: 9(W) x 9(L) x 1.4(H) mm

UNIT: mm

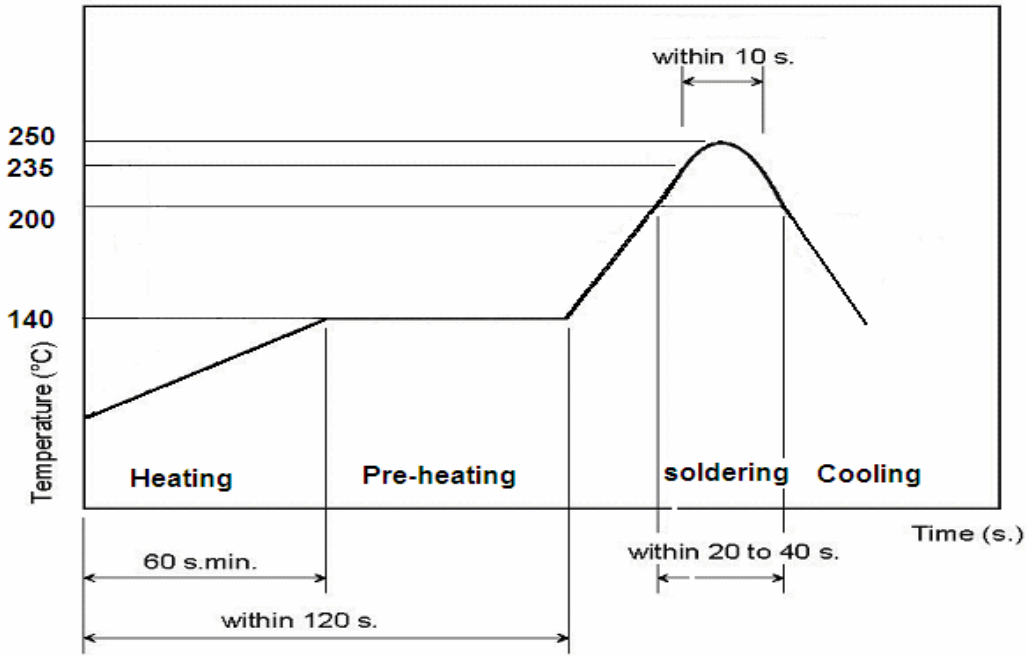


6.2 RECOMMENDED FOOTPRINT

UNIT: mm
TOP VIEW

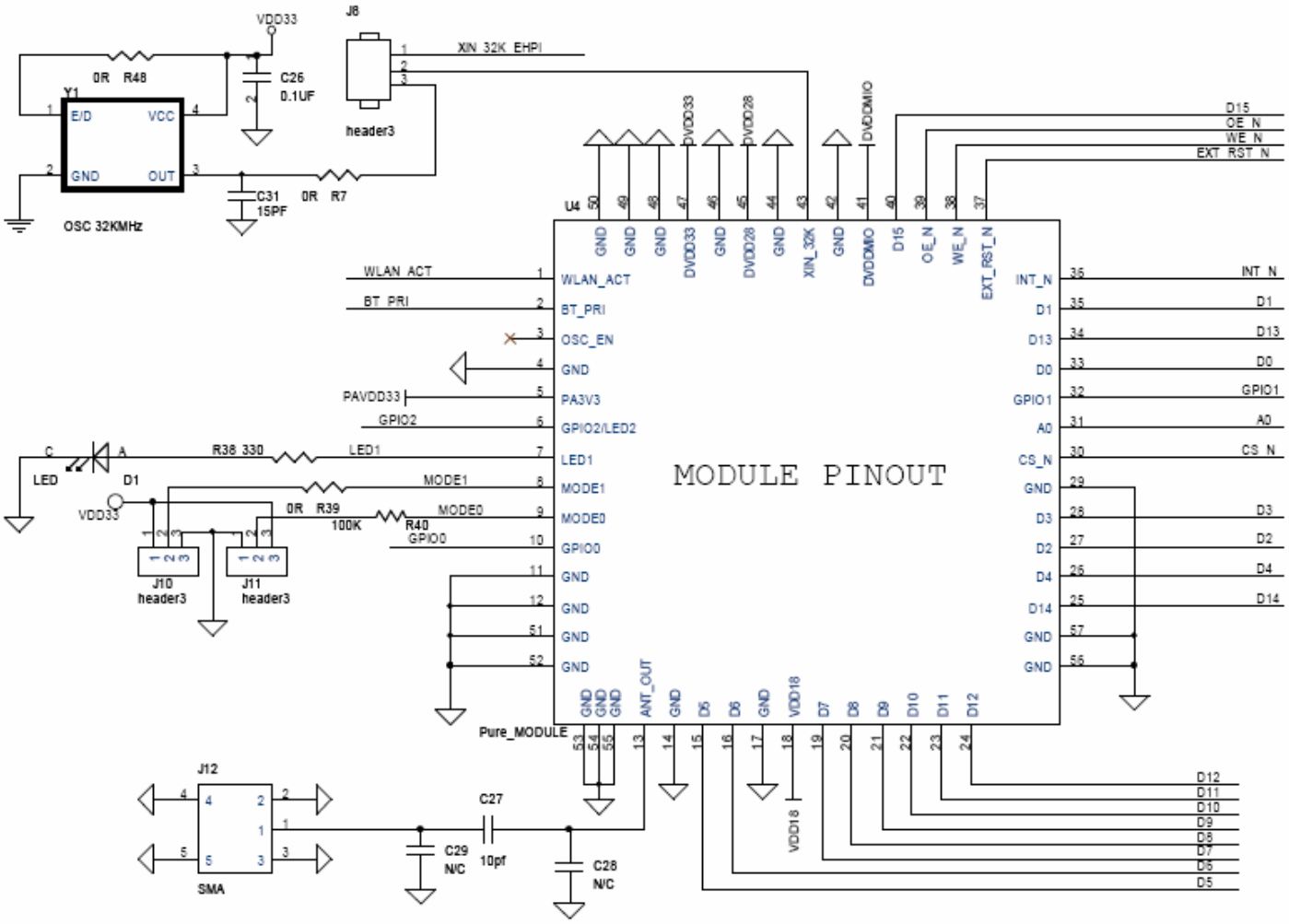


6.3 RECOMMENDED REFLOW PROFILE



7 APPLICATION CIRCIT

7.1 EHPI AND SDIO INTERFACE APPLICATION CIRCUIT



MODE SELECTION

	Mode0	Mode1
eHPI16	0	1
eHPI8	1	1
SDIO	0	0

SDIO INTERFACE MAPPING

SDIO_D0	D0
SDIO_D1	D1
SDIO_D2	D2
SDIO_D3	D3
SDIO_CLK	A0
SDIO_CMD	CS_N

7.2 APPLICATION NOTE

- π-network is reserved for antenna narching or 2nd harmonic rejection. Theπ-network's value in the application circuit referable.
- The BT_ACT should be pulled low if this pin isn't connected to Bluetooth module.
- An external 32.768 KHz signal is necessary under deep sleep mode.
- Below is GPIO application note.

		Default State	WiFi BT co-existence function				
	MT5921 Pins	PTA Disabled	No need PTA	1-wire	2-wire	3-wire	4-wire
HW	GPIO0	GND/Pull-low	GND	GND	GND	Pull-low	Pull-low
	GPIO1	GND/Pull-low	GND	GND	GND	Pull-low	Pull-low
	WLAN_ACT	-	-	-	-	-	-
	BT_PRI	NC/BT's pin only	NC	BT's pin only	BT's pin only	BT's pin only	BT's pin only

Table 7-1: GPIO0/GPIO1/WLAN_ACT/BT_PRI hardware setting

*Pull-low/high is controlled by HW PTA; SW cannot set internal pull-low/high by register IOUDR.

1. If we support 1/2/3/4-wise simultaneously, HW GPIO0~1 shall be pull-down.
2. If we support 1/2/3-wise simultaneously, HW GPIO0 shall be pull-down, but GPIO1 can be GND.
3. If we support 1/2-wise simultaneously, HW GPIO 0~1 can be GND.
4. If 1-wise PTA is used, upper layer shall inform MT5921 driver to disable PTA when BT is power off.

Note: it is not permitted to have GPIO1 daisy chain and 4-wire PTA function simultaneously.

		Default State	Other function	
	MT5921 Pins	If not used	Interrupt (2.8V)	Shared OSC
HW	GPIO2	GND	Host-wakeup	Other device(daisy chain)

Table 7-2: GPIO2 hardware setting

About GPIO2 setting, SW registry setting will have priority to EEPROM setting.