



Aufgabenstellung für den Großen Beleg

Student: Fredo Erxleben
Studiengang: Informatik
Matrikelnummer: 33 00 664

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Thema: **Graphical Support for the
Design and Evaluation of Configurable Logic Blocks**

Configurable hardware is a key technology to implement custom digital circuitry without having to cope with the immense costs of producing custom silicon on recent technology nodes. It is essential for making non-high-volume and flexible circuitry economically feasible.

Configurable logic blocks (CLBs) contribute heavily to the flexibility of configurable hardware. They form a repetitive structure that adopts a custom circuit by programming connection points, data-path multiplexers or truth tables.

The design of CLBs is a critical engineering challenge, which must trade off the occupied silicon area against the flexibility and computational strength provided by it. While the manufacturers of programmable gate arrays have to deal with this task naturally, the goal of this project is to make the basic exploration of CLB designs easily accessible for a broad audience by initiating an intuitive graphical design and evaluation tool. Essential features that should be implemented within the scope of this project are the graphical input of a combinational CLB circuit and the integration of an available SAT-based boolean matching flow for strength evaluation. Besides a statistical strength evaluation across a corpus of boolean functions, also the visualization of specific CLB configurations for concrete implementable functions shall be enabled by a suitable back annotation. The integration into an established tool like qucs is desirable.

1. Literature review on CLB evaluation and boolean matching.
2. Selection of a set of suitable tools for the implementation and integration of the envisioned solution.
3. Implementation of the CLB design and evaluation inside the chosen ecosystem of tools.
4. Demonstration and evaluation of the achieved functionality also identifying future enhancements.
5. Written documentation of the conducted research, the implemented design and its evaluation.

Betreuer: Dr.-Ing. Thomas B. Preußner
Betreuender Hochschullehrer: Prof. Dr.-Ing. habil. Rainer G. Spallek

Student

Betreuender Hochschullehrer

Verteiler: HSL, Betreuer, Student