

adc\_soc.Esta placa posee un circuito de conversión analógica a digital que utiliza conectores SMD como interfaz de entrada y proporción de bits de resolución y una frecuencia de muestreo de hasta 150 MSPS (Megasamples per Second).

blockdiagram.jpg Diagrama en bloques de la placa ADC – SoC de TerasIC tomado del manual correspondiente.

Quartus Prime book, software producido por Altera para el análisis y síntesis de diseños realizados en HDL. Permite compilar diseños, realizar simulaciones y generar código de configuración para dispositivos FPGA.

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