

1)

a) 8->1000      A->1010      9->1001

1000 1010 1001

b) E->1110      F->1111      3->0011

1110 1111 0011

c) 0001->2    1110->E    0001->2

2E2

d) 1111->F    1110->E    1101->D    1011->B

FEDB

2)

43->C    6F->o    6D->m    70->p    75->u    74->t    65->e    72->r

Mesaj=Computer

3)

a) 5->00101    1->00001    00001'in two's complement=11111

00101+11111=100100 (overflow)

b) 5->00101    11->01011    01011'in two's complement=10101

00101+10101=11010 (no overflow)

4)

a) 01001011 AND 10101011=00001011

b) 01001011 OR 10101011=11101011

c) 01001011 XOR 10101011=11100000

5)

a) 7123-> would cause the result of OR ing the contents of registers 2 and 3 to be placed in register 1

b) 2BCD-> would cause the value CD to be placed in register B.

6)

load R1,[0xA0]

load R2,[0xA1]

load R3,0xF0

load R4,0x0F

and R1,R1,R3

and R2,R2,R4

addi R5,R1,R2

store R5,[0xA2]

halt